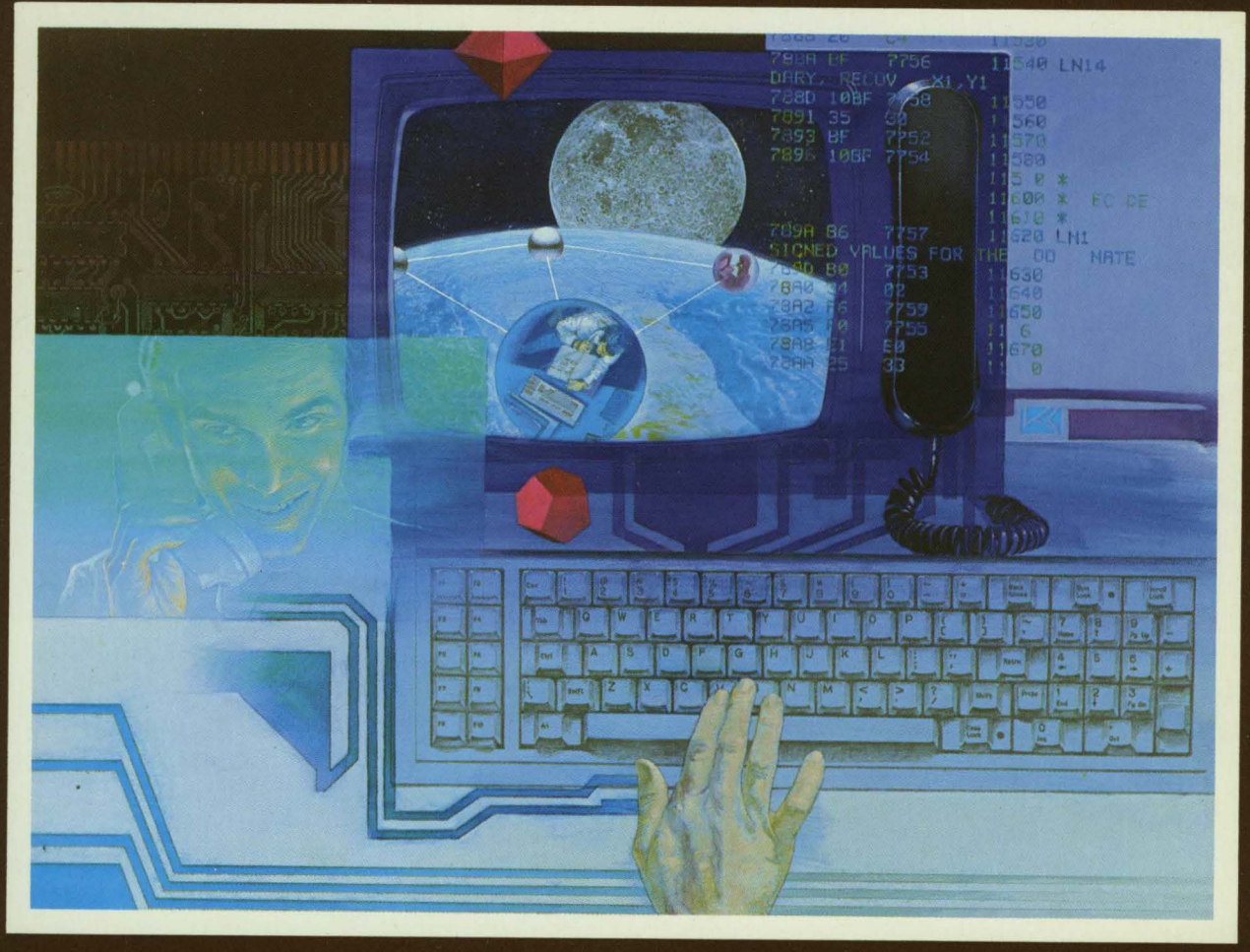
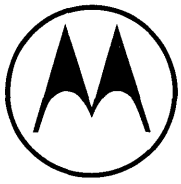
DL136
REV 1

MOTOROLA INC.



TELECOMMUNICATIONS DEVICE DATA



MOTOROLA

TELECOMMUNICATIONS DEVICE DATA

Prepared by
Technical Information Center

Motorola is a major supplier of Semiconductors to Telecommunications equipment manufacturers worldwide, and our data manuals for such standard products as dedicated MOS and Bipolar Telecom ICs, CMOS Special Circuits, High-Speed CMOS, ECL, TTL, Linear, Power Transistors, Microprocessors, and Memories, are on the reference shelves of designers throughout the industry.

This data book pulls together Motorola's Semiconductor Products which are dedicated to applications in Telecommunications. It reflects both the growing portfolio of Motorola devices for Telecommunications and the need for designers to have product information at hand in a convenient form.

Many of the products presented here are new, for new applications in an industry which is presently one of the most dynamic and fastest growing—Telecommunications. It was possible only to include a limited amount of application material. Hence these products are supported by applications and product specialists within the Motorola Semiconductor organizations. Should you require further details or assistance in designing with any of these devices, your Motorola Semiconductor Sales Office can put you in touch with the relevant expertise within our organization.

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Series B

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ALPHANUMERIC INDEX

This index includes all Motorola devices used specifically in telecommunication applications. Information for the devices identified with page numbers appears in this book. All other devices are fully characterized in the book referenced at the right of the device number.

Linear — See DL128, Linear and Interfaces Integrated Circuits
MECL — See DL122R1, MECL Device Data
MCU — See DL132R1, Single-Chip Microcomputer Data
MPU — See DL133, 8-Bit Microprocessor & Peripheral Data
Opto — See DL118R1, Optoelectronics Device Data
RZD — See DL125, Rectifier and Zener Diodes Data
SF — See DL130, CMOS/NMOS Special Functions Data
SS — See DL126, Small-Signal Transistor Data

Selection Guides

1

SELECTOR GUIDE

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SS — See DL126, Small-Signal Transistor Data

MODEMS

*Contact your Motorola representative for the most up-to-date information.

Data Sheets 2

MOTOROLA

MC3416

Specifications and Applications Information

4 x 4 x 2 CROSSPOINT SWITCH

The MC3416 consists of a pair of 4 x 4 matrices of dielectrically isolated SCR's, triggered by a common selection matrix. The device is intended for switching analog signals in communication systems. The use of dielectric isolation processing provides excellent crosstalk isolation while maintaining minimal insertion loss.

The selection array consists of PNP transistors with the input thresholds compatible with either McMOS or MTTL logic families.

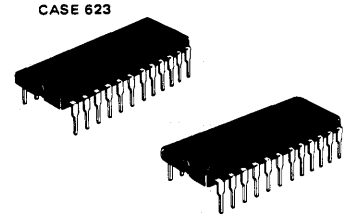
The MC3416 is a monolithic pin-for-pin replacement for the discontinued MCBH7601 hybrid device.

- Low Series Resistance – r_{on} = 6.0 Ohms (Typ) @ I_{AK} = 20 mA
- High Series Resistance – r_{off} = 100 MΩ (Min)
- Pin Compatible with MCBH7601 or RC4444
- High Breakdown Voltage – 30 V (Typ)
- Selection Matrix Compatible with TTL or CMOS Logic Levels
- Dielectric Isolation Insures Low Crosstalk and Low Insertion Loss

4 x 4 x 2 CROSSPOINT SWITCH

DIELECTRICALLY ISOLATED MONOLITHIC INTEGRATED CIRCUIT

L SUFFIX
CERAMIC PACKAGE
CASE 623



P SUFFIX
PLASTIC PACKAGE
CASE 649

FIGURE 1 – REPRESENTATIVE CELL SCHEMATIC
(Repeated 16 Times)

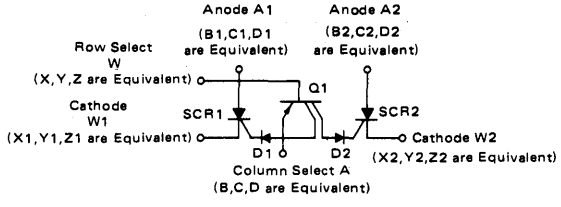
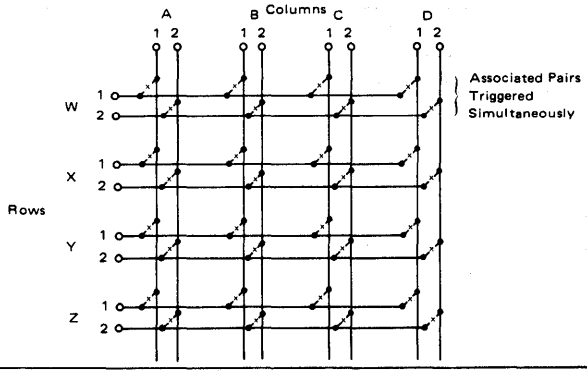
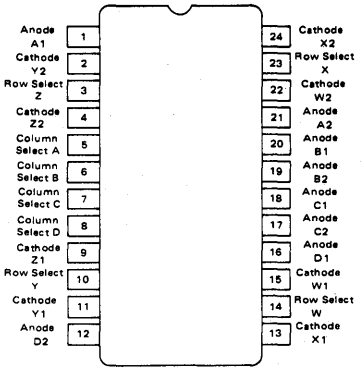


FIGURE 2 – MATRIX CONFIGURATION AND NOMENCLATURE
(X Indicates a Possible Connection)



PIN CONNECTIONS



MAXIMUM RATINGS (Unless otherwise noted, $T_A = 25^oC$)

Rating	Symbol	Value	Unit
Anode-Cathode Current — Continuous (only one SCR at a time)	I_{AK}	150	mA
Enable Current	I_{En}	10	mA
Operating Ambient Temperature Range	T_A	0 to +70	^oC
Storage Temperature Range	T_{stg}	-65 to +150	^oC
Junction Temperature Range	T_J	150°C	^oC

ELECTRICAL CHARACTERISTICS (Unless otherwise noted, $T_A = 0$ to 70^oC)

Characteristic	Symbol	Min	Max	Unit
Anode Cathode Breakdown Voltage ($I_{AK} = 25\mu A$)	BV_{AK}	25	—	Vdc
Cathode-Anode Breakdown Voltage ($I_{KA} = 25\mu A$)	BV_{KA}	25	—	Vdc
Base-Cathode Breakdown Voltage ($I_{BK} = 25\mu A$)	BV_{BK}	25	—	Vdc
Cathode-Base Breakdown Voltage ($I_{KB} = 25\mu A$)	BV_{KB}	25	—	Vdc
Base-Emitter Breakdown Voltage ($I_{BE} = 25\mu A$)	BV_{BE}	25	—	Vdc
Emitter-Cathode Breakdown Voltage ($I_{EK} = 25\mu A$)	BV_{EK}	25	—	Vdc
OFF State Resistance ($V_{AK} = 10$ V)	r_{off}	100	—	MΩ
Dynamic ON Resistance (Center Current = 10 mA) (See Figure 8) (Center Current = 20 mA)	r_{on}	 4.0 2.0	 12 10	Ω
Holding Current (See Figure 10)	I_H	0.7	3.0	mA
Enable Current ($V_{BE} = 1.5$ V) (See Figure 7)	I_{En}	4.0	—	mA
Anode-Cathode ON Voltage ($I_{AK} = 10$ mA) ($I_{AK} = 20$ mA)	V_{AK}	 — —	 1.0 1.1	V
Gate Sharing Current Ratio @ Cathodes (Under Select Conditions with Anodes Open) (See Figure 3)	G_{Sh}	0.8	1.25	mA/mA
Inhibit Voltage ($V_B = 3.0$ V) (See Figure 9)	V_{inh}	—	0.3	V
Inhibit Current ($V_B = 3.0$ V) (See Figure 9)	I_{inh}	—	0.1	mA
OFF State Capacitance ($V_{AK} = 0$ V) (See Figure 6)	C_{off}	—	2.0	pF
Turn-ON Time (See Figure 4)	t_{on}	—	1.0	μs
Minimum Voltage Ramp (Which Could Fire the SCR Under Transient Conditions)	dv/dt	800	—	V/μs

FIGURE 3 – TEST CIRCUIT

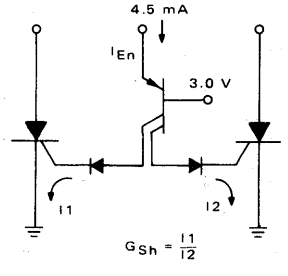


FIGURE 4 – TEST CIRCUIT FOR dv/dt AND t_{on}

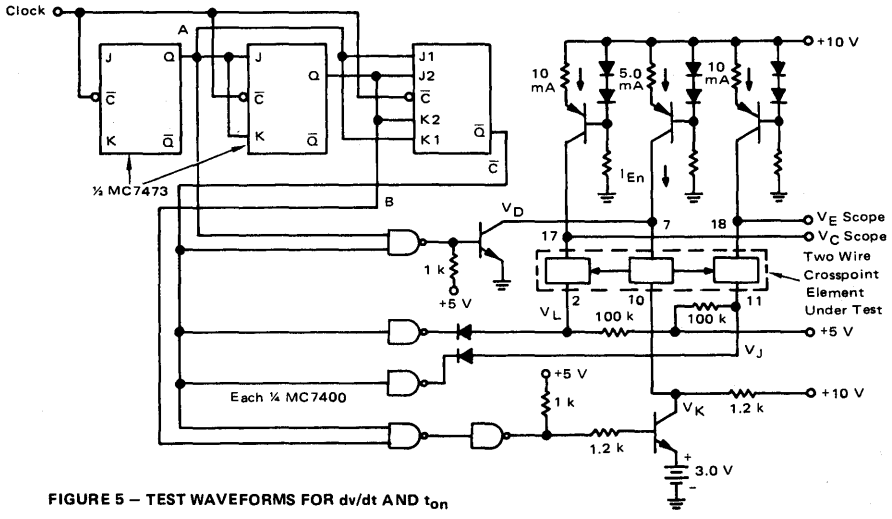


FIGURE 5 – TEST WAVEFORMS FOR dv/dt AND t_{on}

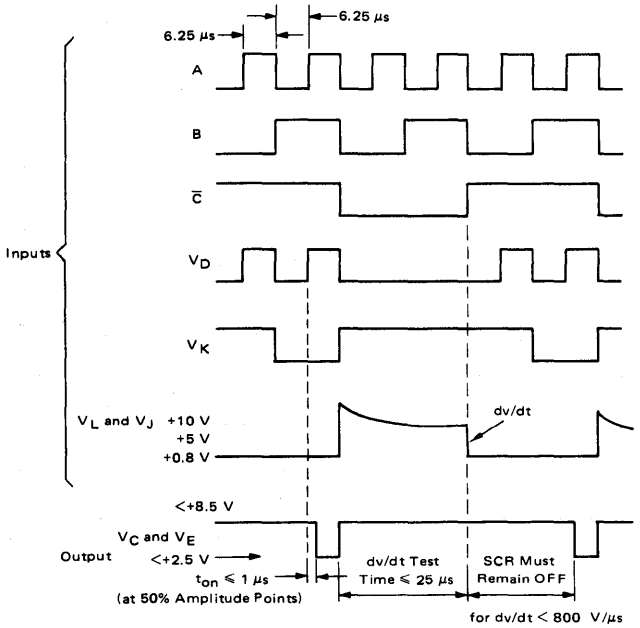


FIGURE 6 – TEST CIRCUIT FOR OFF-STATE CAPACITANCE

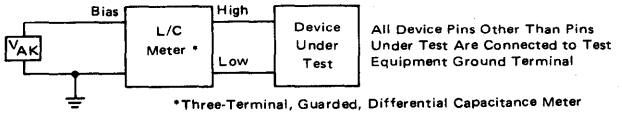


FIGURE 7 – ENABLE CURRENT
(Both SCR's Must Turn On)

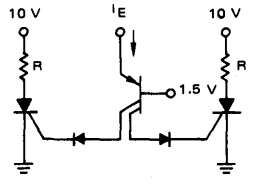


FIGURE 8 – THE CROSSPOINT SCR
I-V CHARACTERISTIC (I_G = 0)

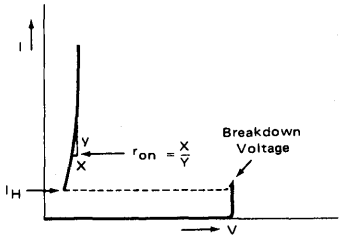
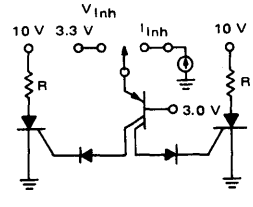


FIGURE 9 – INHIBIT VOLTAGE AND INHIBIT
CURRENT (Both SCR's Must Remain OFF)



2

TYPICAL CHARACTERISTICS

FIGURE 10 – HOLDING CURRENT versus AMBIENT TEMPERATURE

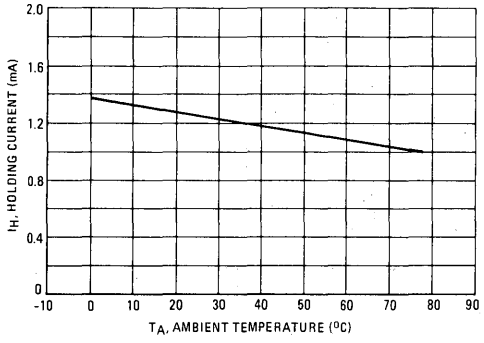


FIGURE 11 – ANODE-CATHODE ON VOLTAGE versus CURRENT AND TEMPERATURE

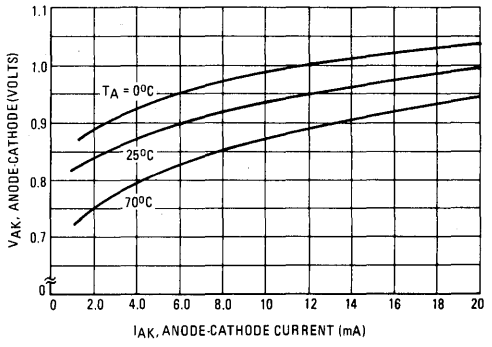


FIGURE 12 – DIFFERENCE IN ANODE-CATHODE ON VOLTAGE (Between Associate Pairs of SCR's) versus ANODE-CATHODE CURRENT

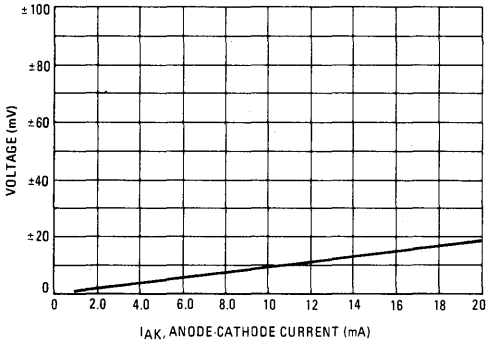


FIGURE 13 – OFF-STATE CAPACITANCE versus ANODE-CATHODE VOLTAGE

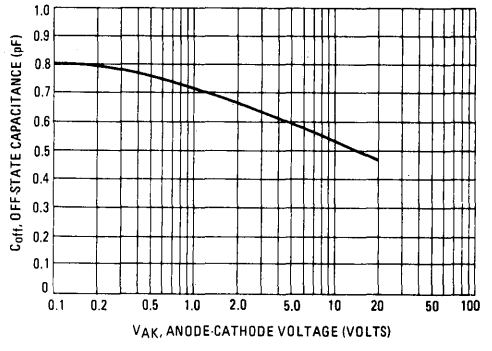


FIGURE 14 – DYNAMIC ON RESISTANCE versus ANODE-CATHODE CURRENT

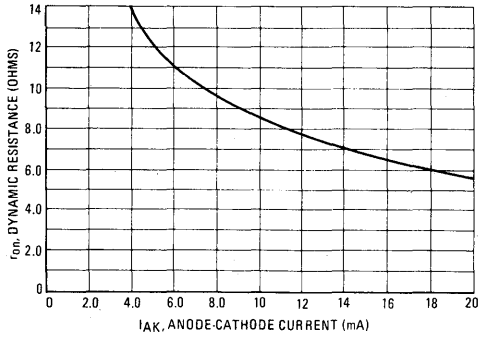


FIGURE 15 – DYNAMIC ON RESISTANCE versus AMBIENT TEMPERATURE

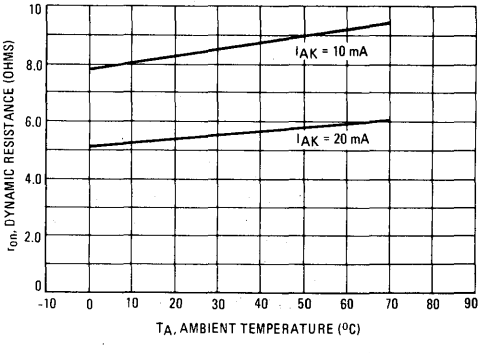


FIGURE 16 – FEEDTHROUGH versus SIGNAL FREQUENCY

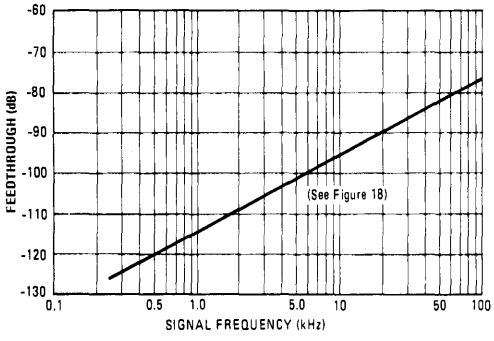


FIGURE 17 – CROSSTALK versus SIGNAL FREQUENCY

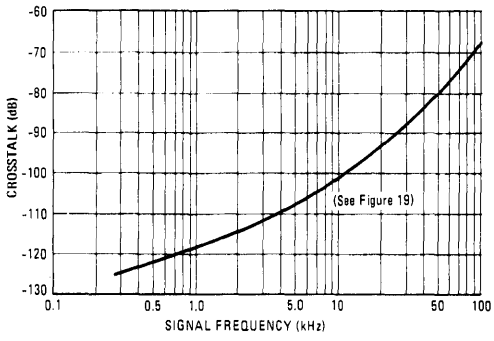


FIGURE 18 – TEST CIRCUIT FOR FEEDTHROUGH versus FREQUENCY

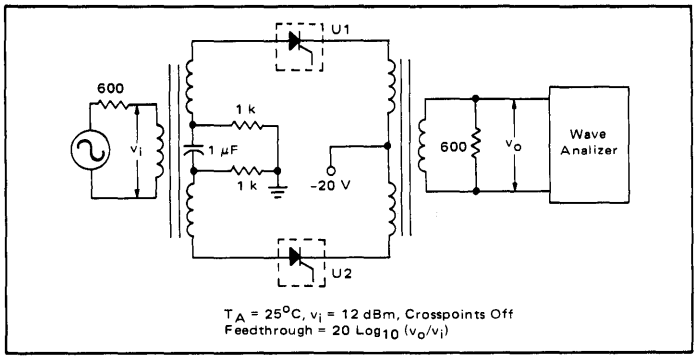


FIGURE 19 – TEST CIRCUIT FOR CROSSTALK versus FREQUENCY

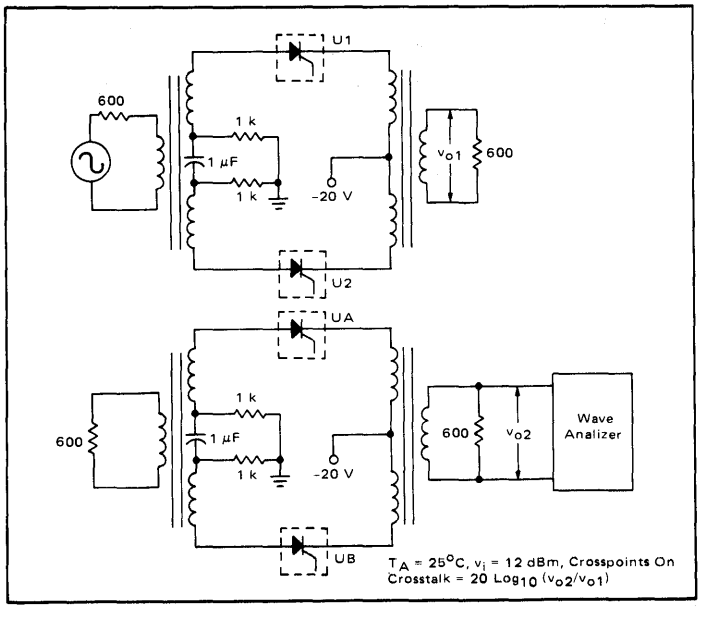
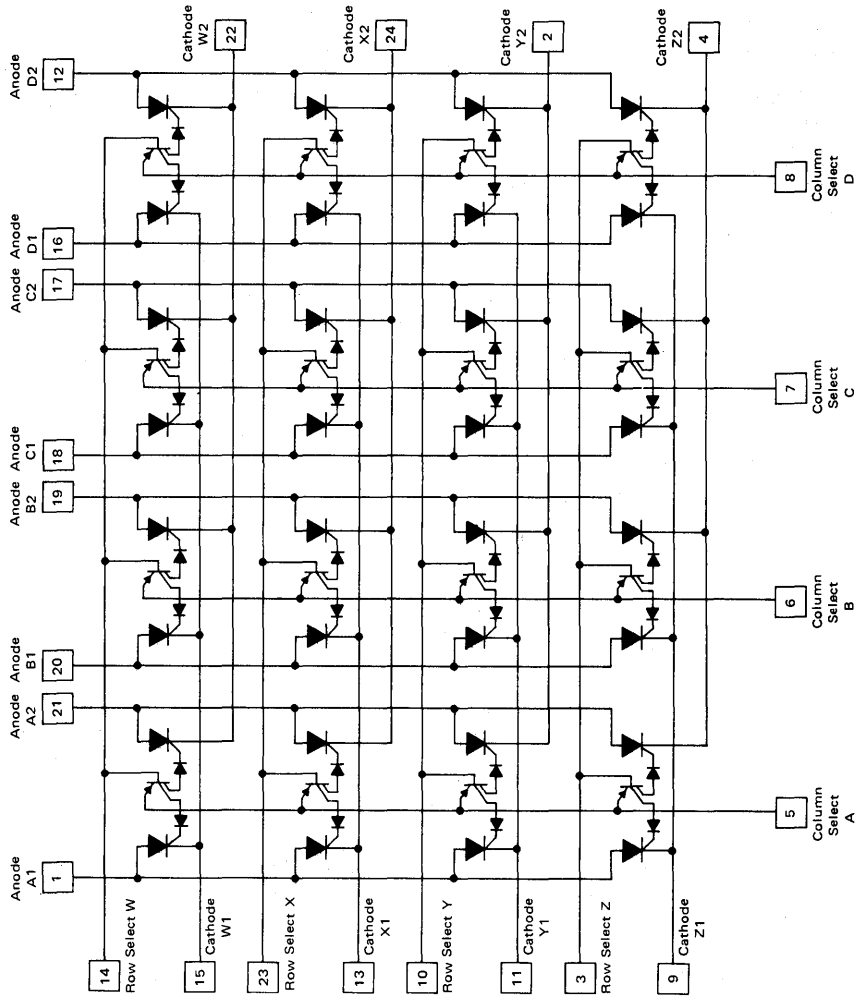


FIGURE 20 – REPRESENTATIVE SCHEMATIC DIAGRAM



TELEPHONE APPLICATION OF THE CROSSPOINT SWITCH

The MC3416 crosspoint switch is designed to provide a low-loss analog switching element for telephony signals. It can be addressed and controlled from standard binary decoders and is CMOS compatible. With proper system organization the MC3416 can significantly reduce the size and cost of existing crosspoint matrices.

SIGNAL PATH CONSIDERATIONS

The MC3416 is a balanced 4 x 4 2-wire crosspoint array. It is ideal for balanced transmission systems, but may be applied effectively in a number of single ended applications. Multiple chips may be interconnected to form larger crosspoint arrays. The major design constraint in using SCR crosspoints is that a forward dc current must be maintained through the SCR to retain an ac signal path. This requires that each subscriber-input to the array be capable of sourcing dc current as well as its ac signal. With each subscriber acting as a dc source, each trunk output then acts as a current sink. The instrument-to-trunk connection in Figure 21 shows this configuration. However, with each subscriber acting as a dc source, some method of interconnecting them without a trunk must be provided. Such a local or intercom termination is shown in Figure 22. Here both subscribers source dc current and exchange ac signals. The central current sink accepts current from both subscribers while the high output impedance of the current sink does not disturb the system.

These configurations are system compatible. The dc

FIGURE 21 – INSTRUMENT-TO-TRUNK CONNECTION

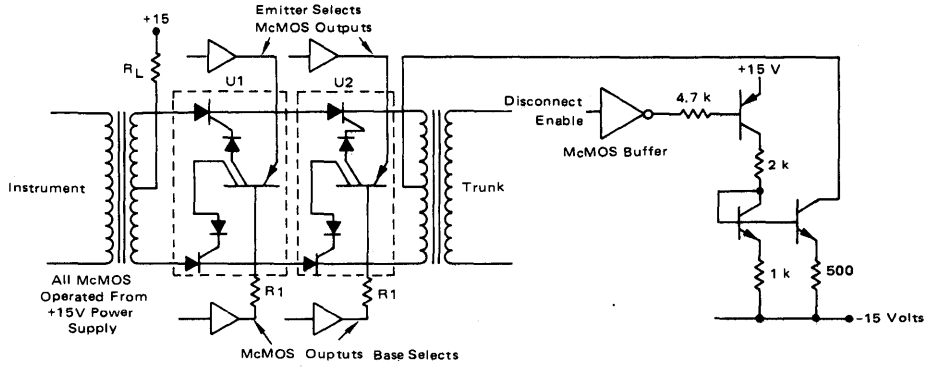
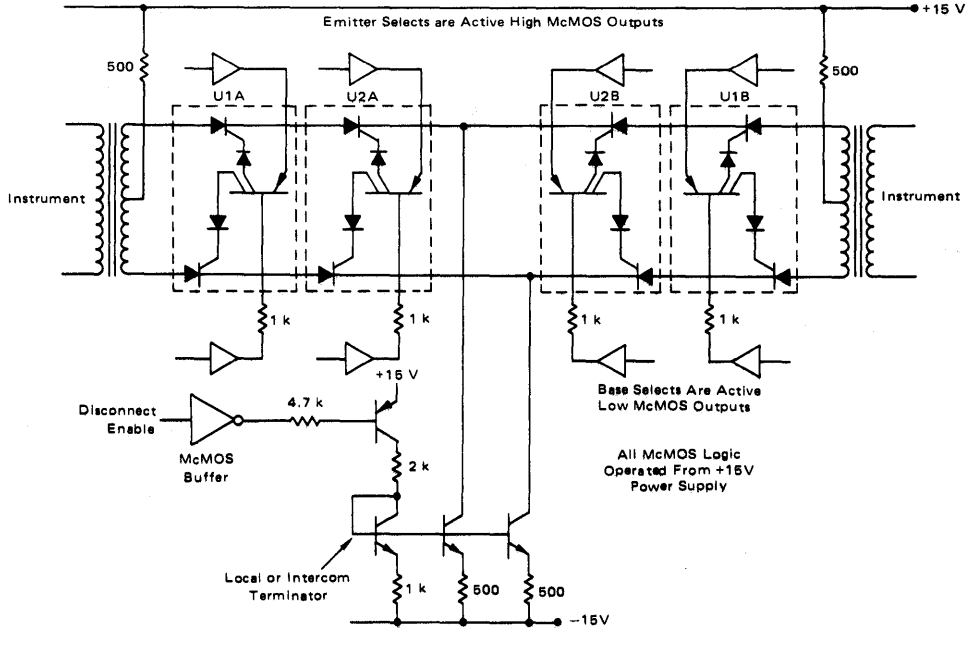


FIGURE 22 – TYPICAL INSTRUMENT TO INSTRUMENT CONNECTION

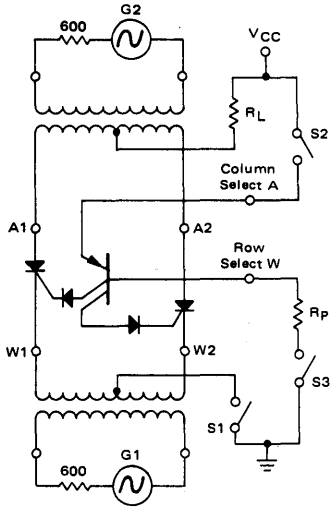


current restriction is not a restriction in the design of an efficient crosspoint array. Because of the current sink terminations, a signal path may use differing numbers of crosspoints in any connection or in two sides of the same connection further relaxing restrictions in array design.

Figure 23 demonstrates circuit operation. S1, S2, and S3 are open. The Crosspoint SCR's are off as they have no gate drive or dc current path through S1. By closing S2 and S3, gate drive is provided, but the SCR's still remain off as there is no dc current path to hold them on. Close S1 and the circuit is enabled, but with S2 and S3 off there is still no signal path. Closing S2 and S3 with S1 closed – current is injected into both gates and they switch on. DC current through R_L splits around the center-tapped winding and flows through each SCR, back through the lower winding and through S1 to ground. If S2 and S3 are opened, that current path still remains and the SCRs remain on. If an ac signal is injected at either G1 or G2, it will be transmitted to the other signal port with negligible loss in the SCR's. To disconnect the ac signal path the SCR's must be commutated off. By opening S1 the dc current path is interrupted and the SCR's switch off. The ac signal path is disconnected. With S1 closed the circuit is enabled and may be addressed again from S2 and S3. This circuit demonstrates a balanced transmission configuration. The transmission characteristics of the SCR's simulate a relay contact in that the ac signal does not incur a contact voltage drop across the crosspoint. The memory characteristics of the crosspoint are demonstrated by the selective application of S1, S2, and S3.

The selection of R_L is governed by the power supply voltage and the desired dc current. If 10 mA is to flow through each SCR then R_L must pass 20 mA. Thus, $(V_{CC} - V_{AK})/R_L = 20$ mA. The selection of Rp is governed by the characteristics for crosspoint turn on. Adequate enable current must be injected into the column select and Rp should drop at least 1.5 Volts. The PNP transistor has a typical gain of one. Thus, Rp should pass at least 2 mA to provide 4 mA column select current.

FIGURE 23– CROSSPOINT OPERATION DEMONSTRATION CIRCUIT



S1	S2	S3	LINE CONDITION
ON	X	OFF	Enabled, Not Connected
ON	OFF	X	Enabled, Not Connected
ON	ON	ON	Addressed and Connected
ON	X	X	G1 Connected to G2
OFF	X	X	Disconnected.
X = irrelevant			

ADDRESSING CONSIDERATIONS

The MC3416 crosspoint switch is addressed by selecting and turning on the PNP transistor that controls the SCR pair desired. The drive requirements of the MC3416 can be met with standard McMOS outputs. A particular crosspoint is addressed by putting a logical "1" on the emitter and a logical "0" on the base of the appropriate transistor. A resistor in the base circuit of the transistor is required to limit the current and must also drop 1.5 Volts to assure forward bias of the two diodes in the collector circuits. The gate current required for SCR turn on is 1 mA typically. The McMOS one-of-n decoders listed in Table I provide both active high and active low outputs and are well suited for standard addressing organizations. The major design constraint in organizing the addressing structure is that any signal path which is to be addressed must create a dc path from a source to a sink. If that path requires two crosspoints they must be addressed simultaneously. Of course, once the path is selected, the addressing hardware is free to initiate other signal paths. To meet the dc path

APPLICATIONS INFORMATION (continued)

requirement, crosspoint arrays should be designed in blocks such that any given dc path requires only one crosspoint per block. A signal path, however, may still use two crosspoints in the same block by sequentially addressing two dc paths to the same terminator. For example, the left or right pairs of crosspoints in Figure 22 must be addressed simultaneously but the left pair may be addressed in sequence after addressing the right pair. This is not a difficult constraint to meet and it does not require unnecessary addressing hardware.

TABLE I

	Active High Outputs	Active Low Outputs
Dual Binary to 1 of 4	MC14555	MC14556
4-bit latch/4 to 16	MC14514	MC14515
BCD to Decimal Decode	MC14028	

DISCONNECT TECHNIQUES

Since the crosspoint switch maintains signal paths by keeping dc currents through active SCR's, disconnects are easily accomplished by interrupting the dc current path. This can be done anywhere in the circuit, but if the disconnect is done at the terminator then all signal paths established to that terminator are broken simultaneously. In both Figures 21 and 22 this is done by turning off the current sink circuit with a McMOS buffer gate. MC14049 or MC14050 buffers will drive the transistor switch. Once a disconnect is completed, the terminator may be re-enabled and used for another call. Usage of the terminators may be easily monitored with optoelectronic couplers in the collectors of the current sinks without disturbing transmission characteristics.

See Application Note AN-760 for additional applications suggestions.

THERMAL INFORMATION

The maximum power consumption an integrated circuit can tolerate at a given operating ambient temperature can be found from the equation:

$$P_{D(T_A)} = \frac{T_{J(max)} - T_A}{R_{\theta JA(Typ)}}$$

Where: $P_{D(T_A)}$ = Power Dissipation allowable at a given operating ambient temperature. This must be greater than the sum of the products of the supply voltages and supply currents at the worst case operating condition.

$T_{J(max)}$ = Maximum Operating Junction Temperature as listed in the Maximum Ratings Section

T_A = Maximum Desired Operating Ambient Temperature

$R_{\theta JA(Typ)}$ = Typical Thermal Resistance Junction to Ambient

MOTOROLA

MC3417, MC3517
MC3418, MC3518

Specifications and Applications Information

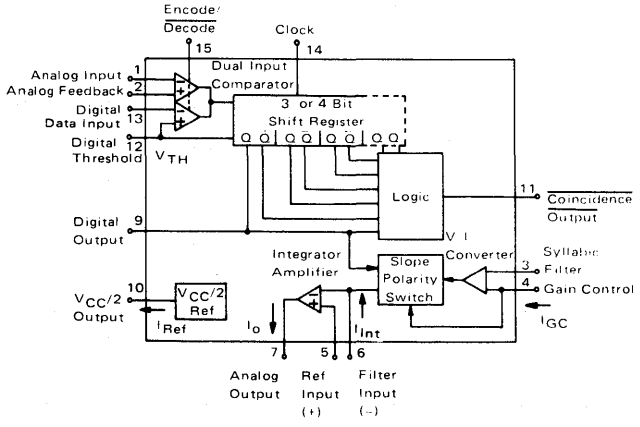
2

CONTINUOUSLY VARIABLE SLOPE DELTA MODULATOR/DEMODULATOR

Providing a simplified approach to digital speech encoding/decoding, the MC3517/18 series of CVSDs is designed for military secure communication and commercial telephone applications. A single IC provides both encoding and decoding functions.

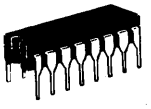
- Encode and Decode Functions on the Same Chip with a Digital Input for Selection
- Utilization of Compatible I^2L – Linear Bipolar Technology
- CMOS Compatible Digital Output
- Digital Input Threshold Selectable ($V_{CC}/2$ reference provided on chip)
- MC3417/MC3517 has a 3-Bit Algorithm (General Communications)
- MC3418/MC3518 has a 4-Bit Algorithm (Commercial Telephone)

CVSD BLOCK DIAGRAM



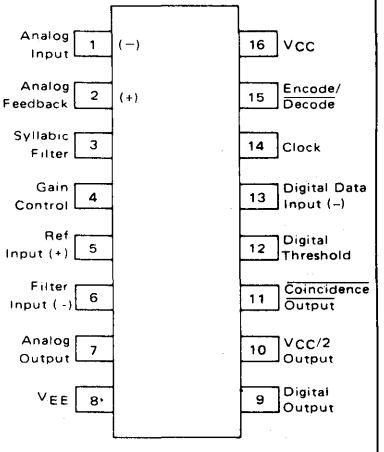
CONTINUOUSLY VARIABLE SLOPE DELTA MODULATOR/DEMODULATOR

LASER-TRIMMED INTEGRATED CIRCUIT



L SUFFIX
CERAMIC PACKAGE
CASE 620

PIN CONNECTIONS



ORDERING INFORMATION

Device	Package	Temperature Range
MC3417L	Ceramic DIP	0°C to +70°C
MC3418L	Ceramic DIP	0°C to +70°C
MC3517L	Ceramic DIP	−55°C to +125°C
MC3518L	Ceramic DIP	−55°C to +125°C

MAXIMUM RATINGS

(All voltages referenced to V_{EE}, T_A = 25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.4 to +18	Vdc
Differential Analog Input Voltage	V_{ID}	±5.0	Vdc
Digital Threshold Voltage	V_{TH}	−0.4 to V_{CC}	Vdc
Logic Input Voltage (Clock, Digital Data, Encode/$\overline{\text{Decode}}$)	V_{Logic}	−0.4 to +18	Vdc
Coincidence Output Voltage	$V_{O(Con)}$	−0.4 to +18	Vdc
Syllabic Filter Input Voltage	$V_{I(Syl)}$	−0.4 to V_{CC}	Vdc
Gain Control Input Voltage	$V_{I(GC)}$	−0.4 to V_{CC}	Vdc
Reference Input Voltage	$V_{I(Ref)}$	$V_{CC}/2$ − 1.0 to V_{CC}	Vdc
$V_{CC}/2$ Output Current	I_{Ref}	−25	mA

ELECTRICAL CHARACTERISTICS

(V_{CC} = 12 V, V_{EE} = Gnd, T_A = 0°C to +70°C for MC3417/18, T_A = −55°C to +125°C for MC3517/18 unless otherwise noted.)

Characteristic	Symbol	MC3417/MC3517			MC3418/MC3518			Unit
		Min	Typ	Max	Min	Typ	Max	
Power Supply Voltage Range (Figure 1)	V_{CCR}	4.75	12	16.5	4.75	12	16.5	Vdc
Power Supply Current (Figure 1) (Idle Channel)	I_{CC}							mA
(V_{CC} = 5.0 V)		–	3.7	5.0	–	3.7	5.0	
(V_{CC} = 15 V)		–	6.0	10	–	6.0	10	
Clock Rate	SR	–	16 k	–	–	32 k	–	Samples/s
Gain Control Current Range (Figure 2)	I_{GCR}	0.001	–	3.0	0.001	–	3.0	mA
Analog Comparator Input Range (Pins 1 and 2) (4.75 V ≤ V_{CC} ≤ 16.5 V)	V_I	1.3	–	V_{CC} − 1.3	1.3	–	V_{CC} − 1.3	Vdc
Analog Output Range (Pin 7) (4.75 V ≤ V_{CC} ≤ 16.5 V, I_O = ± 5.0 mA)	V_O	1.3	–	V_{CC} − 1.3	1.3	–	V_{CC} − 1.3	Vdc
Input Bias Currents (Figure 3) (Comparator in Active Region)	I_{IB}							μA
Analog Input (I1)		–	0.5	1.5	–	0.25	1.0	
Analog Feedback (I2)		–	0.5	1.5	–	0.25	1.0	
Syllabic Filter Input (I3)		–	0.06	0.5	–	0.06	0.3	
Reference Input (I5)		–	−0.06	−0.5	–	−0.06	−0.3	
Input Offset Current (Comparator in Active Region)	I_{IO}							μA
Analog Input/Analog Feedback |I1 − I2| — Figure 3		–	0.15	0.6	–	0.05	0.4	
Integrator Amplifier |I5 − I6| — Figure 4		–	0.02	0.2	–	0.01	0.1	
Input Offset Voltage V/I Converter (Pins 3 and 4) — Figure 5	V_{IO}	–	2.0	6.0	–	2.0	6.0	mV
Transconductance	gm							mA/mV
V/I Converter, 0 to 3.0 mA		0.1	0.3	–	0.1	0.3	–	
Integrator Amplifier, 0 to ± 5.0 mA Load		1.0	10	–	1.0	10	–	
Propagation Delay Times (Note 1)								μs
Clock Trigger to Digital Output	t_{PLH}	–	1.0	2.5	–	1.0	2.5	
(C_L = 25 pF to Gnd)	t_{PHL}	–	0.8	2.5	–	0.8	2.5	
Clock Trigger to Coincidence Output	t_{PLH}	–	1.0	3.0	–	1.0	3.0	
(C_L = 25 pF to Gnd) (R_L = 4 kΩ to V_{CC})	t_{PHL}	–	0.8	2.0	–	0.8	2.0	
Coincidence Output Voltage — Low Logic State ($I_{OL(Con)}$ = 3.0 mA)	$V_{OL(Con)}$	–	0.12	0.25	–	0.12	0.25	Vdc
Coincidence Output Leakage Current — High Logic State (V_{OH} = 15.0 V, 0°C ≤ T_A ≤ 70°C)	$I_{OH(Con)}$	–	0.01	0.5	–	0.01	0.5	μA

NOTE 1. All propagation delay times measured 50% to 50% from the negative going (from V_{CC} to +0.4 V) edge of the clock.

ELECTRICAL CHARACTERISTICS (continued)

Characteristic	Symbol	MC3417/MC3517 Min	MC3417/MC3517 Typ	MC3417/MC3517 Max	MC3418/MC3518 Min	MC3418/MC3518 Typ	MC3418/MC3518 Max	Unit
Applied Digital Threshold Voltage Range (Pin 12)	V_{TH}	+1.2	–	V_{CC} – 2.0	+1.2	–	V_{CC} – 2.0	Vdc
Digital Threshold Input Current (1.2 V ≤ V_{th} ≤ V_{CC} – 2.0 V)	$I_{I(th)}$							μA
(V_{IL} applied to Pins 13, 14 and 15)		–	–	5.0	–	–	5.0	
(V_{IH} applied to Pins 13, 14 and 15)		–	– 10	–50	–	–10	–50	
Maximum Integrator Amplifier Output Current	I_O	±5.0	–	–	±5.0	–	–	mA
V_{CC}/2 Generator Maximum Output Current (Source only)	I_{Ref}	+10	–	–	+10	–	–	mA
V_{CC}/2 Generator Output Impedance (0 to +10 mA)	z_{Ref}	–	3.0	6.0	–	3.0	6.0	Ω
V_{CC}/2 Generator Tolerance (4.75 V ≤ V_{CC} ≤ 16.5 V)	ϵ_r	–	–	±3.5	–	–	±3.5	%
Logic Input Voltage (Pins 13, 14 and 15)								Vdc
Low Logic State	V_{IL}	Gnd	–	V_{th} – 0.4	Gnd	–	V_{th} – 0.4	
High Logic State	V_{IH}	V_{th} + 0.4	–	18.0	V_{th} + 0.4	–	18.0	
Dynamic Total Loop Offset Voltage (Note 2) – Figures 3, 4 and 5	ΣV_{offset}							mV
I_{GC} = 12.0 μA, V_{CC} = 12 V								
T_A = 25°C		–	–	–	–	± 0.5	± 1.5	
0°C ≤ T_A ≤ +70°C MC3417/18		–	–	–	–	± 0.75	± 2.3	
–55°C ≤ T_A ≤ +125°C MC3517/18		–	–	–	–	± 1.5	± 4.0	
I_{GC} = 33.0 μA, V_{CC} = 12 V								
T_A = 25°C		–	± 2.5	± 5.0	–	–	–	
0°C ≤ T_A ≤ +70°C MC3417/18		–	± 3.0	± 7.5	–	–	–	
–55°C ≤ T_A ≤ +125°C MC3517/18		–	±4.5	±10	–	–	–	
I_{GC} = 12.0 μA, V_{CC} = 5.0 V								
T_A = 25°C		–	–	–	–	± 1.0	± 2.0	
0°C ≤ T_A ≤ +70°C MC3417/18		–	–	–	–	± 1.3	± 2.8	
–55°C ≤ T_A ≤ +125°C MC3517/18		–	–	–	–	± 2.5	± 5.0	
I_{GC} = 33.0 μA, V_{CC} = 5.0 V								
T_A = 25°C		–	± 4.0	± 6.0	–	–	–	
0°C ≤ T_A ≤ +70°C MC3417/18		–	± 4.5	± 8.0	–	–	–	
–55°C ≤ T_A ≤ +125°C MC3517/18		–	± 5.5	± 10	–	–	–	
Digital Output Voltage								Vdc
(I_{OL} = 3.6 mA)	V_{OL}	–	0.1	0.4	–	0.1	0.4	
(I_{OH} = –0.35 mA)	V_{OH}	V_{CC} – 1.0	V_{CC} – 0.2	–	V_{CC} – 1.0	V_{CC} – 0.2	–	
Syllabic Filter Applied Voltage (Pin 3) (Figure 2)	$V_{I(Syl)}$	+3.2	–	V_{CC}	+3.2	–	V_{CC}	Vdc
Integrating Current (Figure 2)	$\|I_{Int}\|$							
(I_{GC} = 12.0 μA)		8.0	10	12	8.0	10	12	μA
(I_{GC} = 1.5 mA)		1.45	1.50	1.55	1.45	1.50	1.55	mA
(I_{GC} = 3.0 mA)		2.75	3.0	3.25	2.75	3.0	3.25	mA
Dynamic Integrating Current Match (I_{GC} = 1.5 mA) Figure 6	$V_{O(Ave)}$	–	± 100	± 250	–	± 100	± 250	mV
Input Current – High Logic State	I_{IH}							μA
(V_{IH} = 18 V)								
Digital Data Input		–	–	+5.0	–	–	+5.0	
Clock Input		–	–	+5.0	–	–	+5.0	
Encode/$\overline{\text{Decode}}$ Input		–	–	+5.0	–	–	+5.0	
Input Current – Low Logic State	I_{IL}							μA
(V_{IL} = 0 V)								
Digital Data Input		–	–	–10	–	–	–10	
Clock Input		–	–	–360	–	–	–360	
Encode/$\overline{\text{Decode}}$ Input		–	–	–36	–	–	–36	
Clock Input, V_{IL} = 0.4 V		–	–	–72	–	–	–72	

NOTE 2. Dynamic total loop offset (ΣV_{offset}) equals V_{IO} (comparator) (Figure 3) minus V_{IOX} (Figure 5). The input offset voltages of the analog comparator and of the integrator amplifier include the effects of input offset current through the input resistors. The slope polarity switch current mismatch appears as an average voltage across the 10 k integrator resistor. For the MC3417/MC3517, the clock frequency is 16.0 kHz. For the MC3418/MC3518, the clock frequency is 32.0 kHz. Idle channel performance is guaranteed if this dynamic total loop offset is less than one-half of the change in integrator output voltage during one clock cycle (ramp step size). Laser trimming is used to insure good idle channel performance.

DEFINITIONS AND FUNCTION OF PINS

Pin 1 – Analog Input

This is the analog comparator inverting input where the voice signal is applied. It may be ac or dc coupled depending on the application. If the voice signal is to be level shifted to the internal reference voltage, then a bias resistor between pins 1 and 10 is used. The resistor is used to establish the reference as the new dc average of the ac coupled signal. The analog comparator was designed for low hysteresis (typically less than 0.1 mV) and high gain (typically 70 dB).

Pin 2 – Analog Feedback

This is the non-inverting input to the analog signal comparator within the IC. In an encoder application it should be connected to the analog output of the encoder circuit. This may be pin 7 or a low pass filter output connected to pin 7. In a decode circuit pin 2 is not used and may be tied to $V_{CC}/2$ on pin 10, ground or left open.

The analog input comparator has bias currents of 1.5 μA max, thus the driving impedances of pins 1 and 2 should be equal to avoid disturbing the idle channel characteristics of the encoder.

Pin 3 – Syllabic Filter

This is the point at which the syllabic filter voltage is returned to the IC in order to control the integrator step size. It is an NPN input to an op amp. The syllabic filter consists of an RC network between pins 11 and 3. Typical time constant values of 6 ms to 50 ms are used in voice codecs.

Pin 4 – Gain Control Input

The syllabic filter voltage appears across C_S of the syllabic filter and is the voltage between V_{CC} and pin 3. The active voltage to current (V-I) converter drives pin 4 to the same voltage at a slew rate of typically 0.5 V/μs. Thus the current injected into pin 4 (I_{GC}) is the syllabic filter voltage divided by the R_X resistance. Figure 6 shows the relationship between I_{GC} (x-axis) and the integrating current, I_{Int} (y-axis). The discrepancy, which is most significant at very low currents, is due to circuitry within the slope polarity switch which enables trimming to a low total loop offset. The R_X resistor is then varied to adjust the loop gain of the codec, but should be no larger than 5.0 kΩ to maintain stability.

Pin 5 – Reference Input

This pin is the non-inverting input of the integrator amplifier. It is used to reference the dc level of the output signal. In an encoder circuit it must reference the same voltage as pin 1 and is tied to pin 10.

Pin 6 – Filter Input

This inverting op amp input is used to connect the integrator external components. The integrating current (I_{Int}) flows into pin 6 when the analog input (pin 1) is high with respect to the analog feedback (pin 2) in the encode mode or when the digital data input (pin 13) is high in the decode mode. For the opposite states, I_{Int} flows out of Pin 6. Single integration systems require a capacitor and resistor between pins 6 and 7. Multipole configurations will have different circuitry. The resistance between pins 6 and 7 should always be between 8 kΩ and 13 kΩ to maintain good idle channel characteristics.

Pin 7 – Analog Output

This is the integrator op amp output. It is capable of driving a 600-ohm load referenced to $V_{CC}/2$ to +6 dBm and can otherwise be treated as an op amp output. Pins 5, 6, and 7 provide full access to the integrator op amp for designing integration filter networks. The slew rate of the internally compensated integrator op amp is typically 0.5 V/μs. Pin 7 output is current limited for both polarities of current flow at typically 30 mA.

Pin 8 – V_{EE}

The circuit is designed to work in either single or dual power supply applications. Pin 8 is always connected to the most negative supply.

Pin 9 – Digital Output

The digital output provides the results of the delta modulator's conversion. It swings between V_{CC} and V_{EE} and is CMOS or TTL compatible. Pin 9 is inverting with respect to pin 1 and non-inverting with respect to pin 2. It is clocked on the falling edge of pin 14. The typical 10% to 90% rise and fall times are 250 ns and 50 ns respectively for V_{CC} = 12 V and C_L = 25 pF to ground.

Pin 10 – $V_{CC}/2$ Output

An internal low impedance mid-supply reference is provided for use of the MC3417/18 in single supply applications. The internal regulator is a current source and must be loaded with a resistor to insure its sinking capability. If a +6 dBmo signal is expected across a 600 ohm input bias resistor, then pin 10 must sink 2.2 V/600 Ω = 3.66 mA. This is only possible if pin 10 sources 3.66 mA into a resistor normally and will source only the difference under peak load. The reference load resistor is chosen accordingly. A 0.1 μF bypass capacitor from pin 10 to V_{EE} is also recommended. The $V_{CC}/2$ reference is capable of sourcing 10 mA and can be used as a reference elsewhere in the system circuitry.

Pin 11 – $\overline{\text{Coincidence Output}}$

The duty cycle of this pin is proportional to the voltage across C_S. The coincidence output will be low whenever the content of the internal shift register is all 1s or all 0s. In the MC3417 the register is 3 bits long

DEFINITIONS AND FUNCTIONS OF PINS (continued)

while the MC3418 contains a 4 bit register. Pin 11 is an open collector of an NPN device and requires a pull-up resistor. If the syllabic filter is to have equal charge and discharge time constants, the value of R_P should be much less than R_S. In systems requiring different charge and discharge constants, the charging constant is $R_S C_S$ while the decaying constant is $(R_S + R_P)C_S$. Thus longer decays are easily achievable. The NPN device should not be required to sink more than 3 mA in any configuration. The typical 10% to 90% rise and fall times are 200 ns and 100 ns respectively for R_L = 4 kΩ to +12 V and C_L = 25 pF to ground.

Pin 12 – Digital Threshold

This input sets the switching threshold for pins 13, 14, and 15. It is intended to aid in interfacing different logic families without external parts. Often it is connected to the $V_{CC}/2$ reference for CMOS interface or can be biased two diode drops above V_{EE} for TTL interface.

Pin 13 – Digital Data Input

In a decode application, the digital data stream is applied to pin 13. In an encoder it may be unused or may be used to transmit signaling message under the control of pin 15. It is an inverting input with respect to pin 9. When pins 9 and 13 are connected, a toggle flip-flop is formed and a forced idle channel pattern can be transmitted. The digital data input level should be maintained for 0.5 μs before and after the clock trigger for proper clocking.

Pin 14 – Clock Input

The clock input determines the data rate of the codec circuit. A 32K bit rate requires a 32 kHz clock. The switching threshold of the clock input is set by pin 12. The shift register circuit toggles on the falling edge of the clock input. The minimum width for a positive-going pulse on the clock input is 300 ns, whereas for a negative-going pulse, it is 900 ns.

Pin 15 – Encode/$\overline{\text{Decode}}$

This pin controls the connection of the analog input comparator and the digital input comparator to the internal shift register. If high, the result of the analog comparison will be clocked into the register on the falling edge at pin 14. If low, the digital input state will be entered. This allows use of the IC as an encoder/decoder or simplex codec without external parts. Furthermore, it allows non-voice patterns to be forced onto the transmission line through pin 13 in an encoder.

Pin 16 – V_{CC}

The power supply range is from 4.75 to 16.5 volts between pin V_{CC} and V_{EE}.

FIGURE 1 – POWER SUPPLY CURRENT

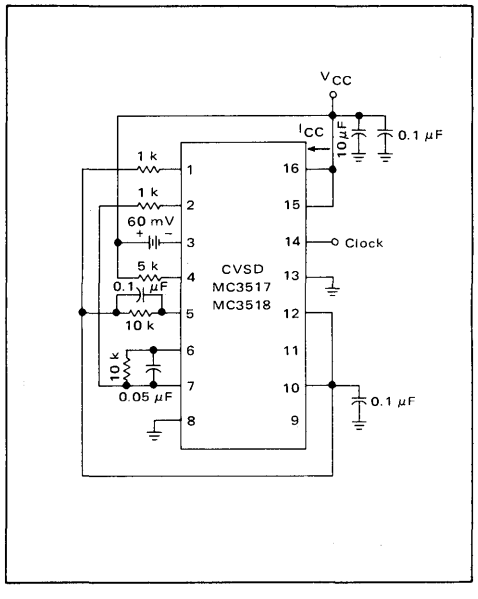
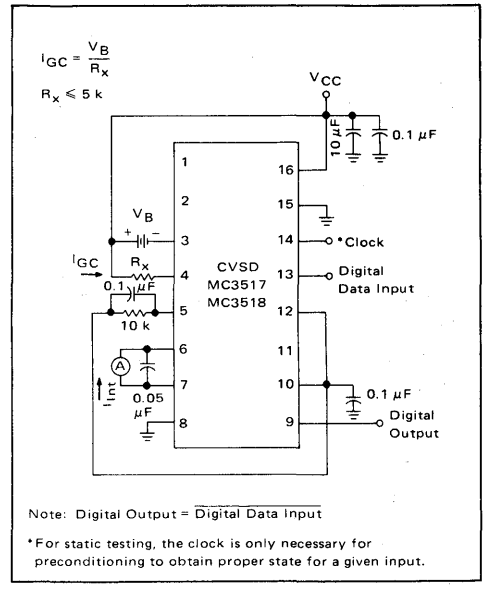


FIGURE 2 – I_{GCR}, GAIN CONTROL RANGE and I_{Int} – INTEGRATING CURRENT



Note: Digital Output = $\overline{\text{Digital Data Input}}$

*For static testing, the clock is only necessary for preconditioning to obtain proper state for a given input.

FIGURE 12 – CVSD WAVEFORMS

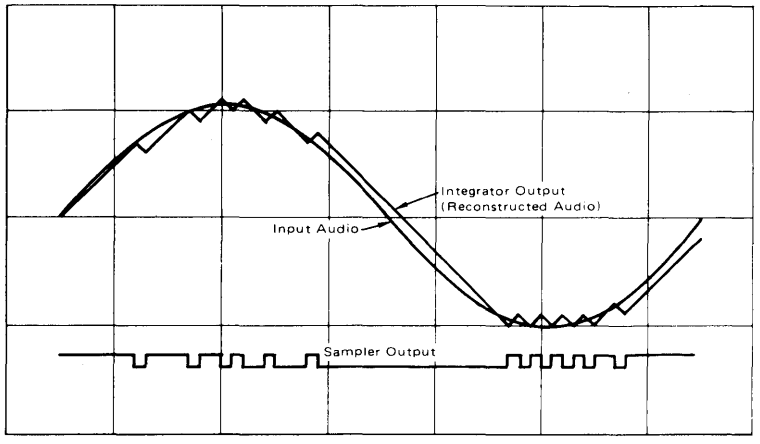


FIGURE 13 – BLOCK DIAGRAM OF THE CVSD DECODER

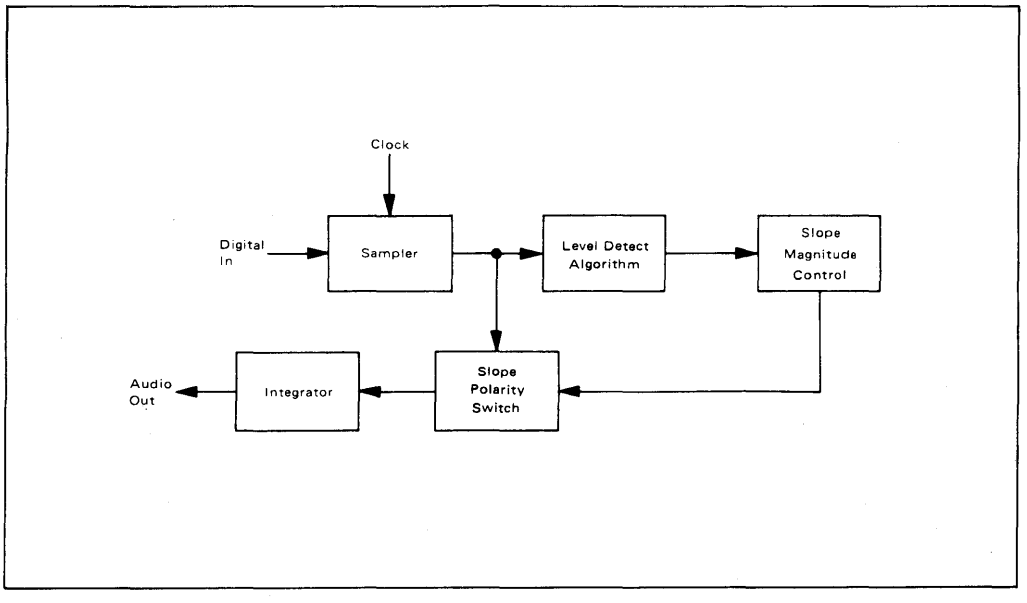
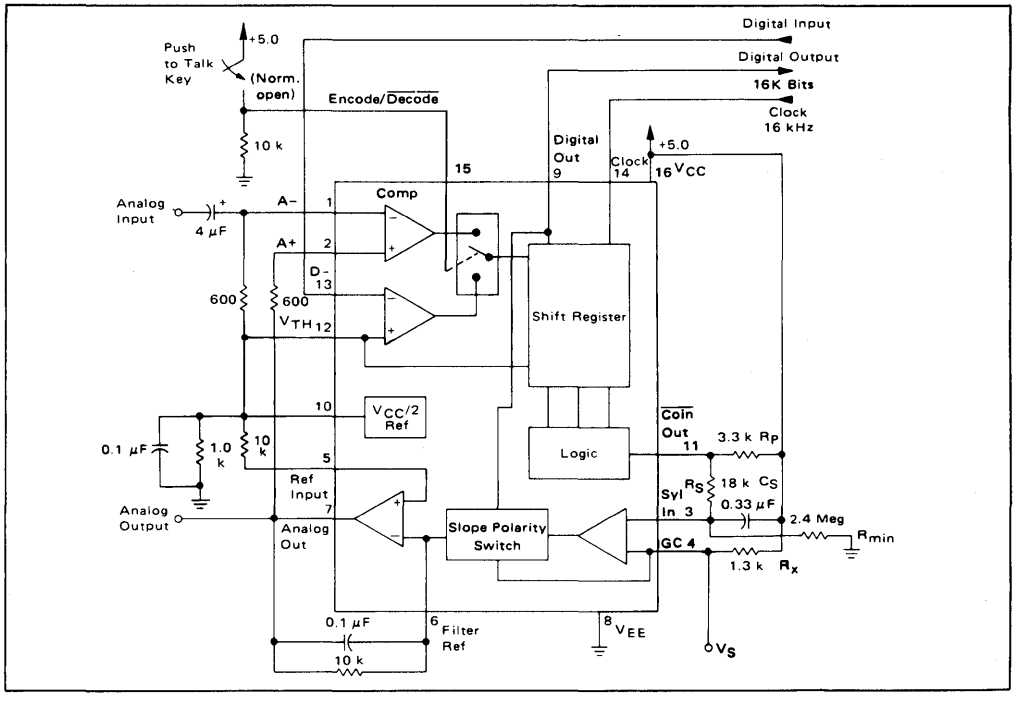


FIGURE 14 – 16 kHz SIMPLEX VOICE CODEC
(Using MC3417, Single Pole Companding and Single Integration)



CIRCUIT DESCRIPTION

The continuously variable slope delta modulator (CVSD) is a simple alternative to more complex conventional conversion techniques in systems requiring digital communication of analog signals. The human voice is analog, but digital transmission of any signal over great distance is attractive. Signal/noise ratios do not vary with distance in digital transmission and multiplexing, switching and repeating hardware is more economical and easier to design. However, instrumentation A to D converters do not meet the communications requirements. The CVSD A to D is well suited to the requirements of digital communications and is an economically efficient means of digitizing analog inputs for transmission.

The Delta Modulator

The innermost control loop of a CVSD converter is a simple delta modulator. A block diagram CVSD Encoder is shown in Figure 11. A delta modulator consists of a comparator in the forward path and an integrator in the feedback path of a simple control loop. The inputs to the comparator are the input analog signal and the integrator output. The comparator output reflects the sign of the difference between the input voltage and the integrator output. That sign bit is the digital output and also controls the direction of ramp in the integrator. The comparator is normally clocked so as to produce a synchronous and band limited digital bit stream.

If the clocked serial bit stream is transmitted, received, and delivered to a similar integrator at a remote point, the remote integrator output is a copy of the transmitting control loop integrator output. To the extent that the integrator at the transmitting locations tracks the input signal, the remote receiver reproduces the input signal. Low pass filtering at the receiver output will eliminate most of the quantizing noise, if the clock rate of the bit stream is an octave or more above the bandwidth of the input signal. Voice bandwidth is 4 kHz and clock rates from 8 k and up are possible. Thus the delta modulator digitizes and transmits the analog input to a remote receiver. The serial, unframed nature of the data is ideal for communications networks. With no input at the transmitter, a continuous one zero alternation is transmitted. If the two integrators are made leaky, then during any loss of contact the receiver output decays to

CIRCUIT DESCRIPTION (continued)

zero and receive restart begins without framing when the receiver reacquires. Similarly a delta modulator is tolerant of sporadic bit errors. Figure 12 shows the delta modulator waveforms while Figure 13 shows the corresponding CVSD decoder block diagram.

The Companding Algorithm

The fundamental advantages of the delta modulator are its simplicity and the serial format of its output. Its limitations are its ability to accurately convert the input within a limited digital bit rate. The analog input must be band limited and amplitude limited. The frequency limitations are governed by the nyquist rate while the amplitude capabilities are set by the gain of the integrator.

The frequency limits are bounded on the upper end; that is, for any input bandwidth there exists a clock frequency larger than that bandwidth which will transmit the signal with a specific noise-level. However, the amplitude limits are bounded on both upper and lower ends. For a signal level, one specific gain will achieve an optimum noise level. Unfortunately, the basic delta modulator has a small dynamic range over which the noise level is constant.

The continuously variable slope circuitry provides increased dynamic range by adjusting the gain of the integrator. For a given clock frequency and input bandwidth the additional circuitry increases the delta modulator's dynamic range. External to the basic delta modulator is an algorithm which monitors the past few outputs of the delta modulator in a simple shift register. The register is 3 or 4 bits long depending on the application. The accepted CVSD algorithm simply monitors the contents of the shift register and indicates if it contains all 1s or 0s. This condition is called coincidence. When it occurs, it indicates that the gain of the integrator is too small. The coincidence output charges a single pole low pass filter. The voltage output of this syllabic filter controls the integrator gain through a pulse amplitude modulator whose other input is the sign bit or up/down control.

The simplicity of the all ones, all zeros algorithm should not be taken lightly. Many other control algorithms using the shift register have been tried. The key to the accepted algorithm is that it provides a measure of the average power or level of the input signal. Other techniques provide more instantaneous information about the shape of the input curve. The purpose of the algorithm is to control the gain of the integrator and to increase the dynamic range. Thus a measure of the average input level is what is needed.

The algorithm is repeated in the receiver and thus the level data is recovered in the receiver. Because the algorithm only operates on the past serial data, it changes the nature of the bit stream without changing the channel bit rate.

The effect of the algorithm is to compand the input signal. If a CVSD encoder is played into a basic delta modulator, the output of the delta modulator will reflect the shape of the input signal but all of the output will be at an equal level. Thus the algorithm at the output is needed to restore the level variations. The bit stream in the channel is as if it were from a standard delta modulator with a constant level input.

The delta modulator encoder with the CVSD algorithm provides an efficient method for digitizing a voice input in a manner which is especially convenient for digital communciations requirements.

APPLICATIONS INFORMATION

CVSD DESIGN CONSIDERATIONS

A simple CVSD encoder using the MC3417 or MC3418 is shown in Figure 14. These ICs are general purpose CVSD building blocks which allow the system designer to tailor the encoder's transmission characteristics to the application. Thus, the achievable transmission capabilities are constrained by the fundamental limitations of delta modulation and the design of encoder parameters. The performance is not dictated by the internal configuration of the MC3417 and MC3418. There are seven design considerations involved in designing these basic CVSD building blocks into a specific codec application.

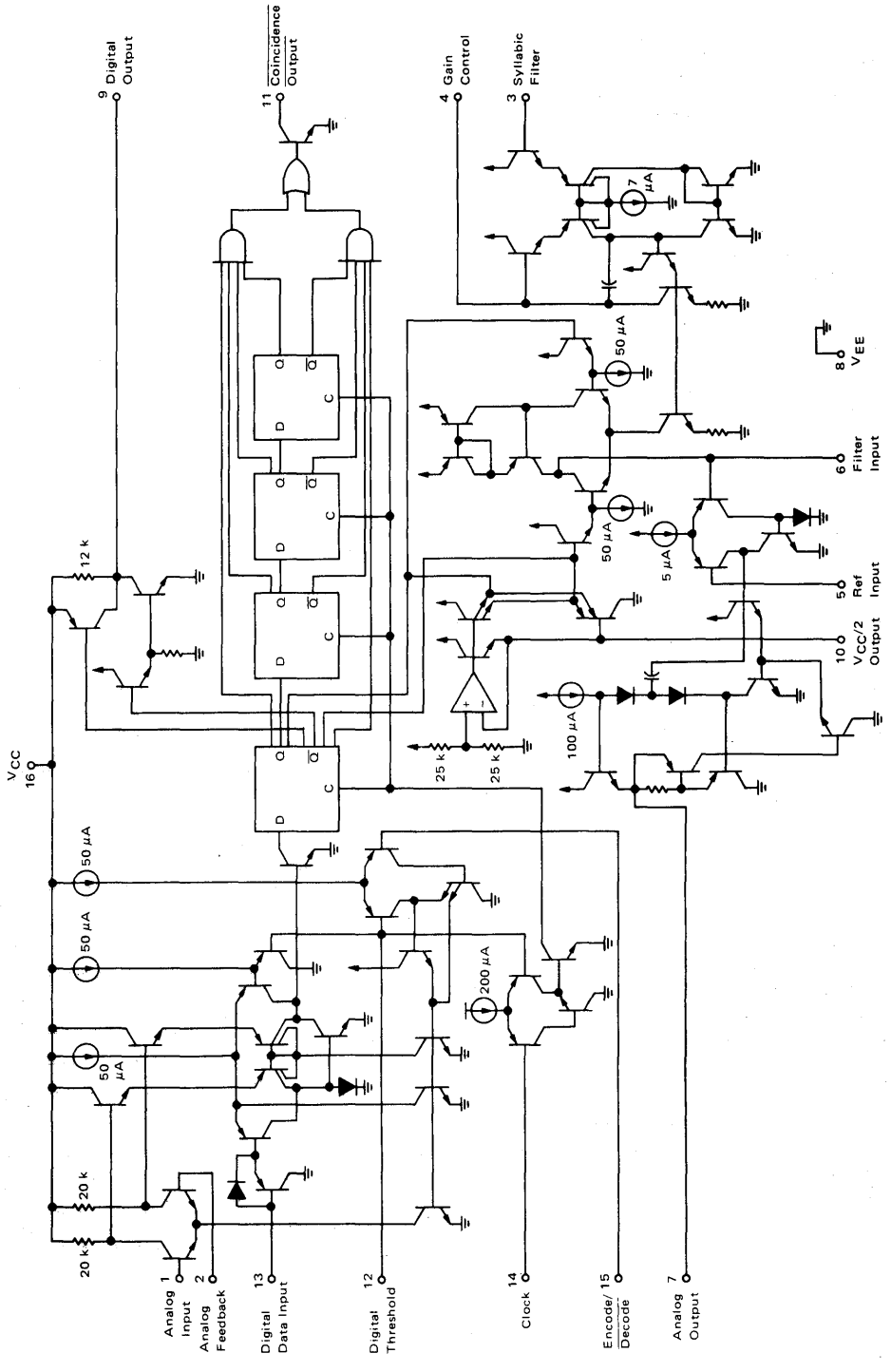
These are listed below:

1. Selection of clock rate
2. Required number of shift register bits
3. Selection of loop gain
4. Selection of minimum step size
5. Design of integration filter transfer function
6. Design of syllabic filter transfer function
7. Design of low pass filter at the receiver

The circuit in Figure 14 is the most basic CVSD circuit possible. For many applications in secure radio or other intelligible voice channel requirements, it is entirely sufficient. In this circuit, items 5 and 6 are reduced to their simplest form. The syllabic and integration filters are both single pole networks. The selection of items 1 through 4 govern the codec performance.

2

CVSD CIRCUIT SCHEMATIC



CVSD DESIGN CONSIDERATIONS (continued)

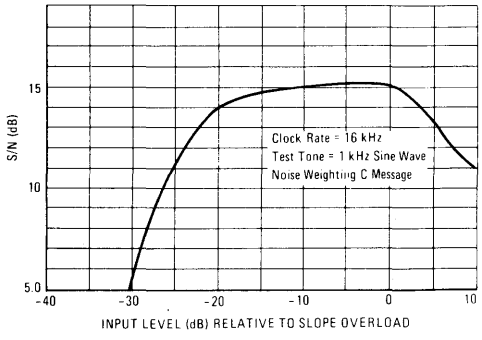
Layout Considerations

Care should be exercised to isolate all digital signal paths (pins 9, 11, 13, and 14) from analog signal paths (pins 1-7 and 10) in order to achieve proper idle channel performance.

Clock Rate

With minor modifications the circuit in Figure 14 may be operated anywhere from 9.6 kHz to 64 kHz clock rates. Obviously the higher the clock rate the higher the S/N performance. The circuit in Figure 14 typically produces the S/N performance shown in Figure 15. The selection of clock rate is usually dictated by the bandwidth of the transmission medium. Voice bandwidth systems will require no higher than 9600 Hz. Some radio systems will allow 12 kHz. Private 4-wire telephone systems are often operated at 16 kHz and commercial telephone performance can be achieved at 32K bits and above. Other codecs may use bit rates up to 200K bits/sec.

FIGURE 15 – SIGNAL-TO-NOISE PERFORMANCE OF MC3417 WITH SINGLE INTEGRATION, SINGLE-POLE AND COMPANDING AT 16K BITS – TYPICAL



Shift Register Length (Algorithm)

The MC3417 has a three-bit algorithm and the MC3418 has a four-bit algorithm. For clock rates of 16 kHz and below, the 3-bit algorithm is well suited. For 32 kHz and higher clock rates, the 4-bit system is preferred. Since the algorithm records a fixed past history of the input signal, a longer shift register is required to obtain the same internal hsitory. At 16 bits and below, the 4-bit algorithm will produce a slightly wider dynamic range at the expense of level change response. Basically the MC3417 is designed for low bit rate systems and the MC3418 is intended for high performance, high bit rate system. At bit rates above 64K bits either part will work well.

Selection of Loop Gain

The gain of the circuit in Figure 14 is set by resistor R_X. R_X must be selected to provide the proper integrator step size for high level signals such that the companding ratio does not exceed about 25%. The companding ratio is the active low duty cycle of the coincidence output on pin 11 of the codec circuit. Thus the system gain is dependent on:

1. The maximum level and frequency of the input signal.
2. The transfer function of the integration filter.

For voice codecs the typical input signal is taken to be a sine wave at 1 kHz of 0 dBmo level. In practice, the useful dynamic range extends about 6 dB above the design level. In any system the companding ratio should not exceed 30%.

To calculate the required step size current, we must describe the transfer characteristics of the integration filter. In the basic circuit of Figure 14, a single pole of 160 Hz is used.

$$R = 10\ k\Omega,\ C = 0.1\ \mu F$$

$$\frac{V_O}{I_i} = \frac{1}{C(S + 1/RC)} \cong \frac{K}{S + \omega_O}$$

$$\omega_O = 2\pi f$$

$$10^3 = \omega_O = 2\pi f$$

$$f = 159.2\ Hz$$

Note that the integration filter produces a single-pole response from 300 to 3 kHz. The current required to move the integrator output a specific voltage from zero is simply:

$$I_i = \frac{V_O}{R} + \frac{C_d V_O}{dt}$$

Now a 0 dBmo sine wave has a peak value of 1.0954 volts. In 1/8 of a cycle of a sine wave centered around the zero crossing, the sine wave changes by approximately its peak value. The CVSD step should trace that change. The required current for a 0 dBm 1 kHz sine wave is:

$$I_i = \frac{1.1\ V}{*2(10\ k\Omega)} + \frac{0.1\ \mu F(1.1)}{0.125\ ms} = 0.935\ mA$$

*The maximum voltage across RI when maximum slew is required is:

$$\frac{1.1\ V}{2}$$

Now the voltage range of the syllabic filter is the power supply voltage, thus:

$$R_X = 0.25(V_{CC})\ \frac{1}{0.935\ mA}$$

A similar procedure can be followed to establish the proper gain for any input level and integration filter type.

CVSD DESIGN CONSIDERATIONS (continued)

Minimum Step Size

The final parameter to be selected for the simple codec in Figure 14 is idle channel step size. With no input signal, the digital output becomes a one-zero alternating pattern and the analog output becomes a small triangle wave. Mismatches of internal currents and offsets limit the minimum step size which will produce a perfect idle channel pattern. The MC3417 is tested to ensure that a 20 mVp-p minimum step size at 16 kHz will attain a proper idle channel. The idle channel step size must be twice the specified total loop offset if a one-zero idle pattern is desired. In some applications a much smaller minimum step size (e.g., 0.1 mV) can produce quiet performance without providing a 1-0 pattern.

To set the idle channel step size, the value of R_{min} must be selected. With no input signal, the slope control algorithm is inactive. A long series of ones or zeros never occurs. Thus, the voltage across the syllabic filter capacitor (C_S) would decay to zero. However, the voltage divider of R_S and R_{min} (see Figure 14) sets the minimum allowed voltage across the syllabic filter capacitor. That voltage must produce the desired ramps at the analog output. Again we write the filter input current equation:

$$I_i = \frac{V_o}{R} + C\frac{dV_o}{dt}$$

For values of V_o near $V_{CC}/2$ the V_o/R term is negligible; thus

$$I_i = C_S\frac{\Delta V_o}{\Delta T}$$

where ΔT is the clock period and ΔV_o is the desired peak-to-peak value of the idle output. For a 16K-bit system using the circuit in Figure 14

$$I_i = \frac{0.1\,\mu F \;\; 20\text{ mV}}{62.5\,\mu s} = 33\,\mu A$$

The voltage on C_S which produces a 33 μA current is determined by the value of R_X.

$$I_i R_X = V_S min;\ \text{for } 33\,\mu A,\ V_S min = 41.6\text{ mV}$$

In Figure 14 R_S is 18 kΩ. That selection is discussed with the syllabic filter considerations. The voltage divider of R_S and R_{min} must produce an output of 41.6 mV.

$$V_{CC}\frac{R_S}{R_S + R_{min}} = V_S min \qquad R_{min} \simeq 2.4\text{ M}\Omega$$

Having established these four parameters — clock rate, number of shift register bits, loop gain and minimum step size — the encoder circuit in Figure 14 will function at near optimum performance for input levels around 0 dBm.

INCREASING CVSD PERFORMANCE

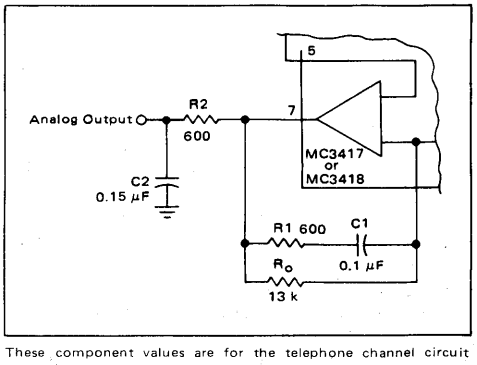
Integration Filter Design

The circuit in Figure 14 uses a single-pole integration network formed with a 0.1 μF capacitor and a 10 kΩ resistor. It is possible to improve the performance of the circuit in Figure 14 by 1 or 2 dB by using a two-pole integration network. The improved circuit is shown.

The first pole is still placed below 300 Hz to provide the 1/S voice content curve and a second pole is placed somewhere above the 1 kHz frequency. For telephony circuits, the second pole can be placed above 1.8 kHz to exceed the 1633 touchtone frequency. In other communication systems, values as low as 1 kHz may be selected. In general, the lower in frequency the second pole is placed, the greater the noise improvement. Then, to ensure the encoder loop stability, a zero is added to keep the phase shift less than 180°. This zero should be placed slightly above the low-pass output filter break frequency so as not to reduce the effectiveness of the second pole. A network of 235 Hz, 2 kHz and 5.2 kHz is typical for telephone applications while 160 Hz, 1.2 kHz and 2.8 kHz might be used in voice only channels. (Voice only channels can use an output low-pass filter which breaks at about 2.5 kHz.) The two-pole network in Figure 16 has a transfer function of:

$$\frac{V_o}{I_i} = \frac{R_0R_1\left(S + \frac{1}{R_1C_1}\right)}{R_2C_2(R_0 + R_1)\left(S + \frac{1}{(R_0 + R_1)C_1}\right)S + \left(\frac{1}{R_2C_2}\right)}$$

FIGURE 16 – IMPROVED FILTER CONFIGURATION



These component values are for the telephone channel circuit poles described in the text. The R2, C2 product can be provided with different values of R and C. R2 should be chosen to be equal to the termination resistor on pin 1.

INCREASING CVSD PERFORMANCE (continued)

Thus the two poles and the zero can be selected arbitrarily as long as the zero is at a higher frequency than the first pole. The values in Figure 16 represent one implementation of the telephony filter requirement.

The selection of the two-pole filter network effects the selection of the loop gain value and the minimum step size resistor. The required integrator current for a given change in voltage now becomes:

$$I_i = \frac{V_o}{R_0} + \left(\frac{R_2C_2}{R_0} + \frac{R_1C_1}{R_0} + C_1\right)\frac{\Delta V_o}{\Delta T} + \left(R_2C_2C_1 + \frac{R_1C_1R_2C_2}{R_0}\right)\frac{\Delta V_o{}^2}{\Delta T^2}.$$

The calculation of desired gain resistor R_X then proceeds exactly as previously described.

Syllabic Filter Design

The syllabic filter in Figure 14 is a simple single-pole network of 18 kΩ and 0.33 μF. This produces a 6.0 ms time constant for the averaging of the coincidence output signal. The voltage across the capacitor determines the integrator current which in turn establishes the step size. The integrator current and the resulting step size determine the companding ratio and the S/N performance. The companding ratio is defined as the voltage across C_S/V_{CC}.

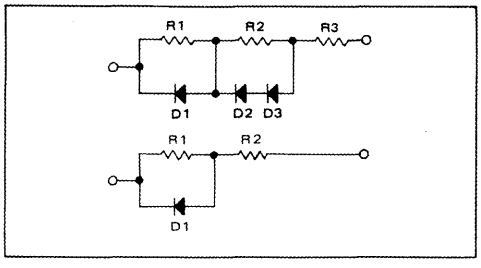
The S/N performance may be improved by modifying the voltage to current transformation produced by R_X. If different portions of the total R_X are shunted by diodes, the integrator current can be other than $(V_{CC} - V_S)/R_X$. These breakpoint curves must be designed experimentally for the particular system application. In general, one would wish that the current would double with input level. To design the desired curve, supply current to pin 4 of the codec from an external source. Input a signal level and adjust the current until the S/N performance is optimum. Then record the syllabic filter voltage and the current. Repeat this for all desired signal levels. Then derive the resistor diode network which produces that curve on a curve tracer.

Once the network is designed with the curve tracer, it is then inserted in place of R_X in the circuit and the forced optimum noise performance will be achieved from the active syllabic algorithm.

Diode breakpoint networks may be very simple or moderately complex and can improve the usable dynamic range of any codec. In the past they have been used in high performance telephone codecs.

Typical resistor-diode networks are shown in Figure 17.

FIGURE 17 – RESISTOR-DIODE NETWORKS



If the performance of more complex diode networks is desired, the circuit in Figure 18 should be used. It simulates the companding characteristics of nonlinear R_X elements in a different manner.

Output Low Pass Filter

A low pass filter is required at the receiving circuit output to eliminate quantizing noise. In general, the lower the bit rate, the better the filter must be. The filter in Figure 20 provides excellent performance for 12 kHz to 40 kHz systems.

TELEPHONE CARRIER QUALITY CODEC USING MC3418

Two specifications of the integrated circuit are specifically intended to meet the performance requirements of commercial telephone systems. First, slope polarity switch current matching is laser trimmed to guarantee proper idle channel performance with 5 mV minimum step size and a typical 1% current match from 15 μA to 3 mA. Thus a 300 to 1 range of step size variation is possible. Second, the MC3418 provides the four-bit algorithm currently used in subscriber loop telephone systems. With these specifications and the circuit of Figure 18, a telephone quality codec can be mass produced.

The circuit in Figure 18 provides a 30 dB S/Nc ratio over 50 dB of dynamic range for a 1 kHz test tone at a 37.7K bit rate. At 37.7K bits, 40 voice channels may be multiplexed on a standard 1.544 megabit T1 facility. This codec has also been tested for 10^{-7} error rates with asynchronous and synchronous data up to 2400 baud and for reliable performance with DTMF signaling. Thus, the design is applicable in telephone quality subscriber loop carrier systems, subscriber loop concentrators and small PABX installations.

The Active Companding Network

The unique feature of the codec in Figure 18 is the step size control circuit which uses a companding ratio reference, the present step size, and the present syllabic filter output to establish the optimum companding ratios and step sizes for any given input level. The companding ratio of a CVSD codec is defined as the duty cycle of the coincidence output. It is the parameter measured by the syllabic filter and is the voltage across C_S divided by the voltage swing of the coincidence output. In Figure 18, the voltage swing of pin 11 is 6 volts. The operating companding ratio is analoged by the voltage between pins 10 and 4 by means of the virtual short across pins 3 and 4 of the V to I op amp within the integrated circuit. Thus, the instantaneous companding ratio of the codec is always available at the negative input of A1.

The diode D1 and the gain of A1 and A2 provide a companding ratio reference for any input level. If the output of A2 is more than 0.7 volts below $V_{CC}/2$, then the positive input of A1 is ($V_{CC}/2$ – 0.7). The on diode drop at the input of A1 represents a 12% companding ratio (12% = 0.7 V/6 V).

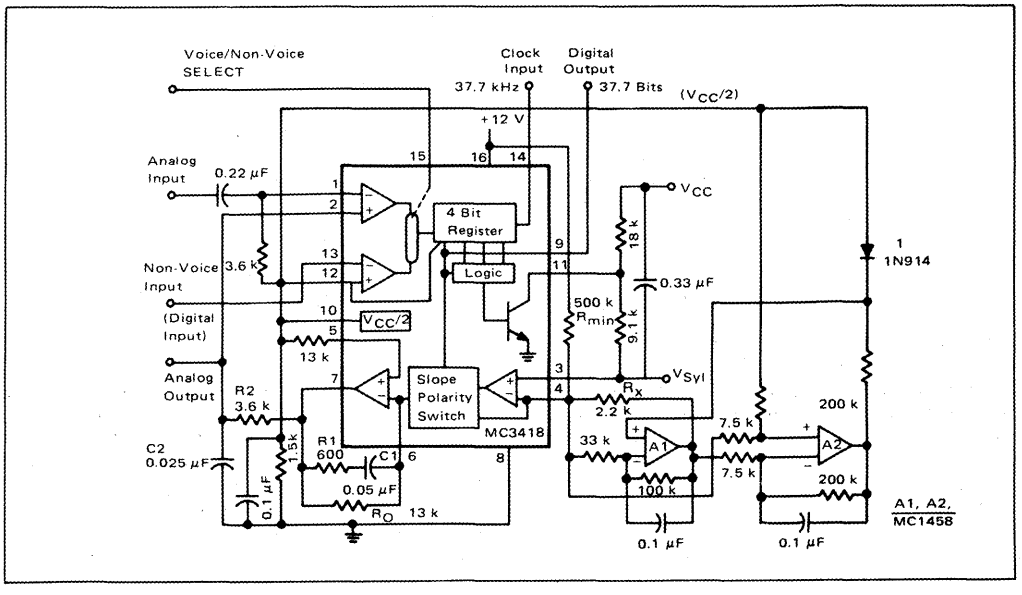
The present step size of the operating codec is directly related to the voltage across R_X, which established the integrator current. In Figure 18, the voltage across R_X is amplified by the differential amplifier A2 whose output is single ended with respect to pin 10 of the IC.

For large signal inputs, the step size is large and the output of A2 is lower than 0.7 volts. Thus D1 is fully on. The present step size is not a factor in the step size control. However, the difference between 12% companding ratio and the instantaneous companding ratio at pin 4 is amplified by A1. The output of A1 changes the voltage across R_X in a direction which reduces the difference between the companding reference and the operating ratio by changing the step size. The ratio of R4 and R3 determines how closely the voltage at pin 4 will be forced to 12%. The selection of R3 and R4 is initially experimental. However, the resulting companding control is dependent on R_X, R3, R4, and the full diode drop D1. These values are easy to reproduce from codec to codec.

For small input levels, the companding ratio reference becomes the output of A2 rather than the diode drop. The operating companding ratio on pin 4 is then compared to a companding ratio smaller than 12% which is determined by the voltage drop across R_X and the gain of A2

FIGURE 18 – TELEPHONE QUALITY DELTAMOD CODER

(Both double integration and active companding control are used to obtain improved CVSD performance. Laser trimming of the integrated circuit provides reliable idle channel and step size range characteristics.)



INCREASING CVSD PERFORMANCE (continued)

Thus the two poles and the zero can be selected arbitrarily as long as the zero is at a higher frequency than the first pole. The values in Figure 16 represent one implementation of the telephony filter requirement.

The selection of the two-pole filter network effects the selection of the loop gain value and the minimum step size resistor. The required integrator current for a given change in voltage now becomes:

$$I_i = \frac{V_o}{R_0} + \left(\frac{R_2C_2}{R_0} + \frac{R_1C_1}{R_0} + C_1\right)\frac{\Delta V_o}{\Delta T} + \left(R_2C_2C_1 + \frac{R_1C_1R_2C_2}{R_0}\right)\frac{\Delta V_o{}^2}{\Delta T^2}.$$

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Syllabic Filter Design

The syllabic filter in Figure 14 is a simple single-pole network of 18 kΩ and 0.33 μF. This produces a 6.0 ms time constant for the averaging of the coincidence output signal. The voltage across the capacitor determines the integrator current which in turn establishes the step size. The integrator current and the resulting step size determine the companding ratio and the S/N performance. The companding ratio is defined as the voltage across C_S/V_{CC}.

The S/N performance may be improved by modifying the voltage to current transformation produced by R_X. If different portions of the total R_X are shunted by diodes, the integrator current can be other than $(V_{CC} - V_S)/R_X$. These breakpoint curves must be designed experimentally for the particular system application. In general, one would wish that the current would double with input level. To design the desired curve, supply current to pin 4 of the codec from an external source. Input a signal level and adjust the current until the S/N performance is optimum. Then record the syllabic filter voltage and the current. Repeat this for all desired signal levels. Then derive the resistor diode network which produces that curve on a curve tracer.

Once the network is designed with the curve tracer, it is then inserted in place of R_X in the circuit and the forced optimum noise performance will be achieved from the active syllabic algorithm.

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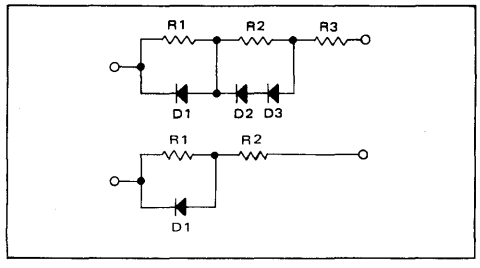

If the performance of more complex diode networks is desired, the circuit in Figure 18 should be used. It simulates the companding characteristics of nonlinear R_X elements in a different manner.

Output Low Pass Filter

A low pass filter is required at the receiving circuit output to eliminate quantizing noise. In general, the lower the bit rate, the better the filter must be. The filter in Figure 20 provides excellent performance for 12 kHz to 40 kHz systems.

TELEPHONE CARRIER QUALITY CODEC USING MC3418

Two specifications of the integrated circuit are specifically intended to meet the performance requirements of commercial telephone systems. First, slope polarity switch current matching is laser trimmed to guarantee proper idle channel performance with 5 mV minimum step size and a typical 1% current match from 15 μA to 3 mA. Thus a 300 to 1 range of step size variation is possible. Second, the MC3418 provides the four-bit algorithm currently used in subscriber loop telephone systems. With these specifications and the circuit of Figure 18, a telephone quality codec can be mass produced.

The circuit in Figure 18 provides a 30 dB S/Nc ratio over 50 dB of dynamic range for a 1 kHz test tone at a 37.7K bit rate. At 37.7K bits, 40 voice channels may be multiplexed on a standard 1.544 megabit T1 facility. This codec has also been tested for 10^{-7} error rates with asynchronous and synchronous data up to 2400 baud and for reliable performance with DTMF signaling. Thus, the design is applicable in telephone quality subscriber loop carrier systems, subscriber loop concentrators and small PABX installations.

TELEPHONE CARRIER QUALITY CODEC USING MC3418 (continued)

The Active Companding Network

The unique feature of the codec in Figure 18 is the step size control circuit which uses a companding ratio reference, the present step size, and the present syllabic filter output to establish the optimum companding ratios and step sizes for any given input level. The companding ratio of a CVSD codec is defined as the duty cycle of the coincidence output. It is the parameter measured by the syllabic filter and is the voltage across C_S divided by the voltage swing of the coincidence output. In Figure 18, the voltage swing of pin 11 is 6 volts. The operating companding ratio is analoged by the voltage between pins 10 and 4 by means of the virtual short across pins 3 and 4 of the V to I op amp within the integrated circuit. Thus, the instantaneous companding ratio of the codec is always available at the negative input of A1.

The diode D1 and the gain of A1 and A2 provide a companding ratio reference for any input level. If the output of A2 is more than 0.7 volts below $V_{CC}/2$, then the positive input of A1 is ($V_{CC}/2$ – 0.7). The on diode drop at the input of A1 represents a 12% companding ratio (12% = 0.7 V/6 V).

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For small input levels, the companding ratio reference becomes the output of A2 rather than the diode drop. The operating companding ratio on pin 4 is then compared to a companding ratio smaller than 12% which is determined by the voltage drop across R_X and the gain of A2

FIGURE 18 – TELEPHONE QUALITY DELTAMOD CODER

(Both double integration and active companding control are used to obtain improved CVSD performance. Laser trimming of the integrated circuit provides reliable idle channel and step size range characteristics.)

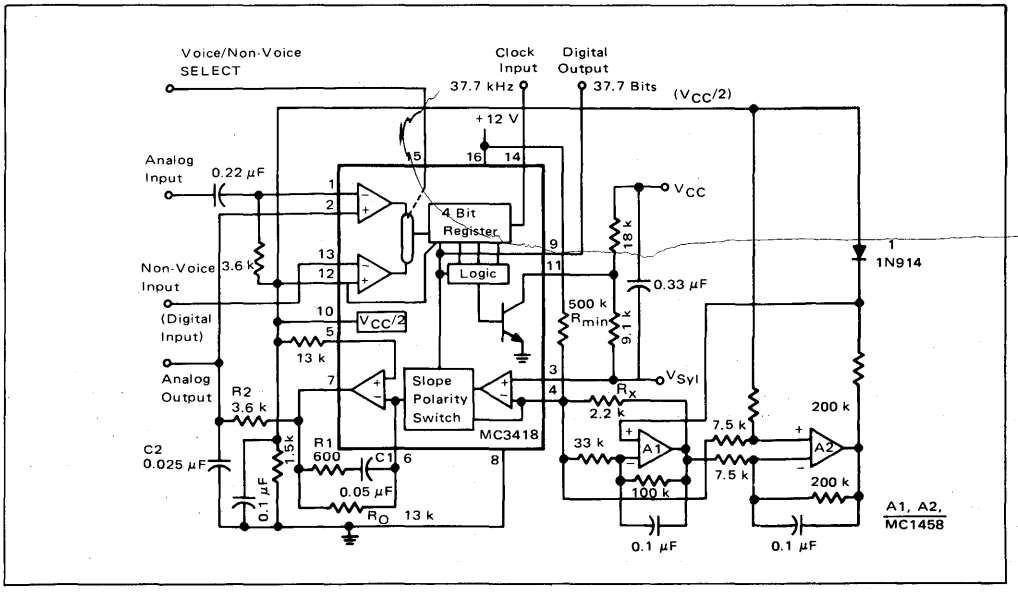
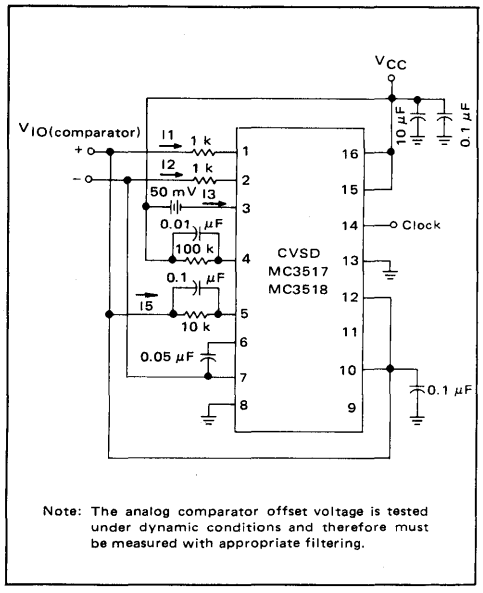


FIGURE 3 – INPUT BIAS CURRENTS, ANALOG COMPARATOR OFFSET VOLTAGE AND CURRENT



Note: The analog comparator offset voltage is tested under dynamic conditions and therefore must be measured with appropriate filtering.

FIGURE 4 – INTEGRATOR AMPLIFIER OFFSET VOLTAGE AND CURRENT

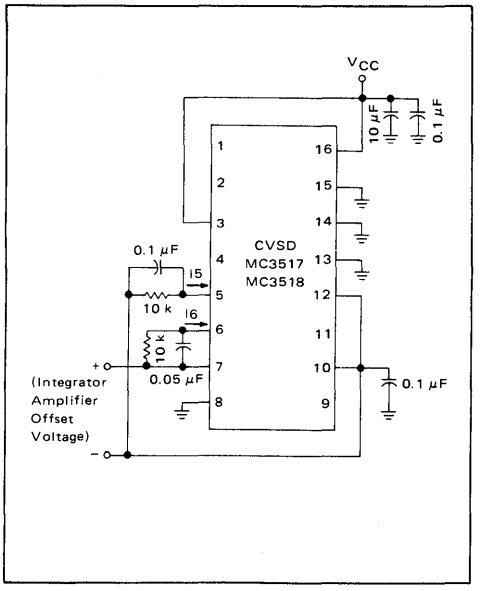
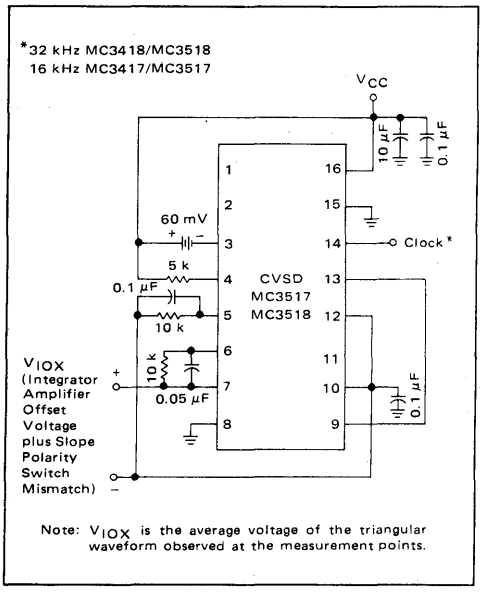
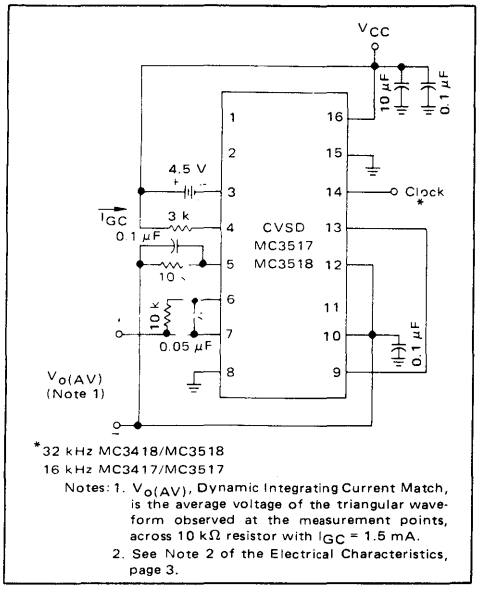


FIGURE 5 – V/I CONVERTER OFFSET VOLTAGE, V_{IO} and V_{IOX}



Note: V_{IOX} is the average voltage of the triangular waveform observed at the measurement points.

FIGURE 6 – DYNAMIC INTEGRATING CURRENT MATCH



*32 kHz MC3418/MC3518
16 kHz MC3417/MC3517

Notes: 1. $V_{o(AV)}$, Dynamic Integrating Current Match, is the average voltage of the triangular waveform observed at the measurement points, across 10 kΩ resistor with I_{GC} = 1.5 mA.
2. See Note 2 of the Electrical Characteristics, page 3.

TYPICAL PERFORMANCE CURVES

FIGURE 7 – TYPICAL I_{Int} versus I_{GC} (Mean ± 2σ)

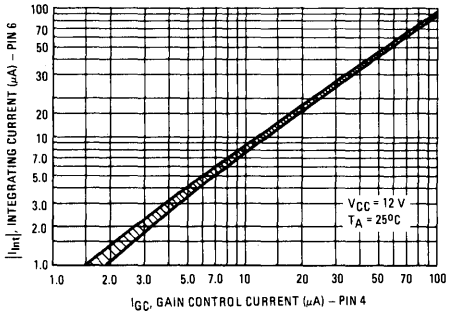


FIGURE 8 – NORMALIZED DYNAMIC INTEGRATING CURRENT MATCH versus V_{CC}

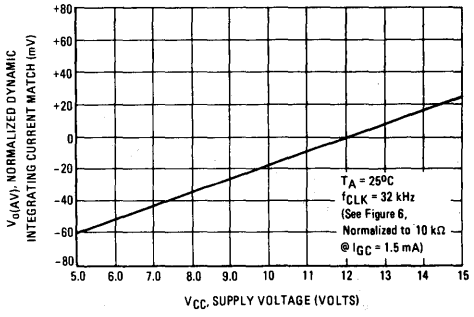


FIGURE 9 – NORMALIZED DYNAMIC INTEGRATING CURRENT MATCH versus CLOCK FREQUENCY

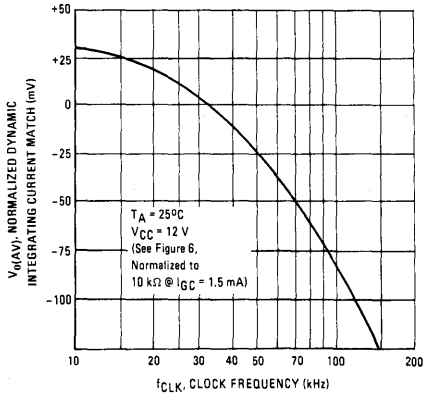


FIGURE 10 – DYNAMIC TOTAL LOOP OFFSET versus CLOCK FREQUENCY

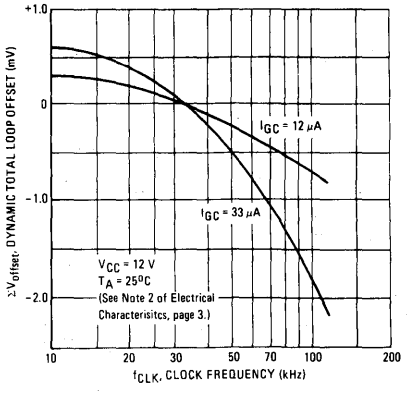


FIGURE 11 – BLOCK DIAGRAM OF THE CVSD ENCODER

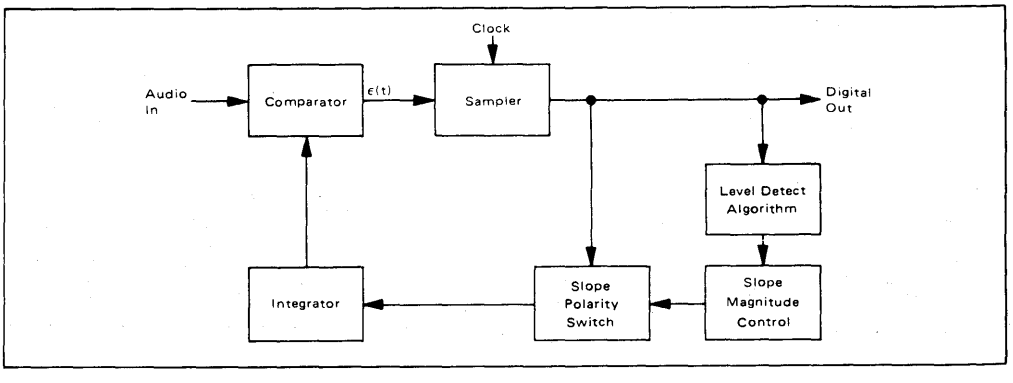
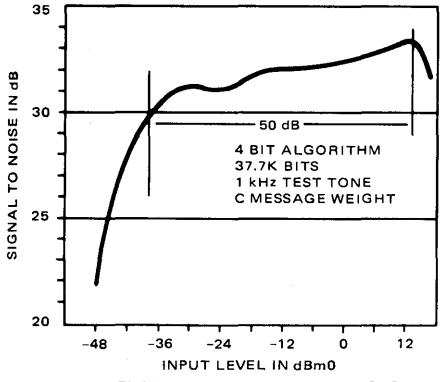
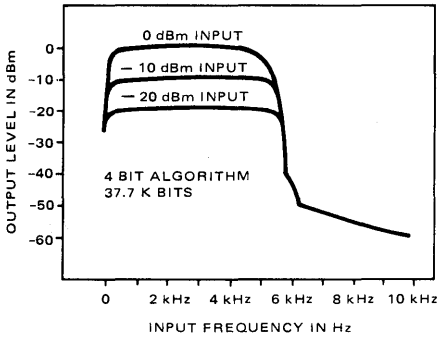


FIGURE 19 – SIGNAL-TO-NOISE PERFORMANCE AND FREQUENCY RESPONSE
(Showing the improvement realized with the circuit in Figure 18.)

a. SIGNAL-TO-NOISE PERFORMANCE OF TELEPHONY QUALITY DELTAMODULATOR



b. FREQUENCY RESPONSE versus INPUT LEVEL (SLOPE OVERLOAD CHARACTERISTIC)



and A1. The gain of A2 is also experimentally determined, but once determined, the circuitry is easily repeated.

With no input signal, the companding ratio at pin 4 goes to zero and the voltage across R_X goes to zero. The voltage at the output of A2 becomes zero since there is no drop across R_X. With no signal input, the actively controlled step size vanished.

The minimum step size is established by the 500 k resistor between V_{CC} and $V_{CC}/2$ and is therefore independently selectable.

The signal to noise results of the active companding network are shown in Figure 19. A smooth 2 dB drop is realized from +12 dBm to −24 under the control of A1. At −24 dBm, A2 begins to degenerate the companding reference and the resulting step size is reduced so as to extend the dynamic range of the codec by 20 dBm.

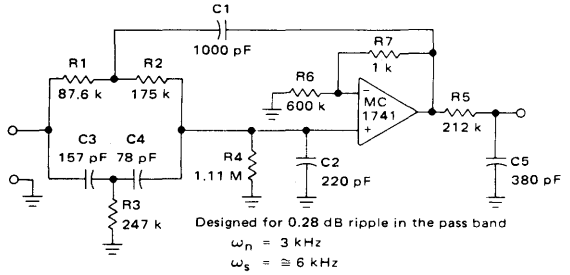
The slope overload characteristic is also shown. The active companding network produces improved performance with frequency. The 0 dBm slope overload point is raised to 4.8 kHz because of the gain available in controlling the voltage across R_X. The curves demonstrate that the level linearity has been maintained or improved.*

The codec in Figure 18 is designed specifically for 37.7K bit systems. However, the benefits of the active companding network are not limited to high bit rate systems. By modifying the crossover region (changing the gain of A2), the active technique may be used to improve the performance of lower bit rate systems.

The performance and repeatability of the codec in Figure 18 represents a significant step forward in the art and cost of CVSD codec designs.

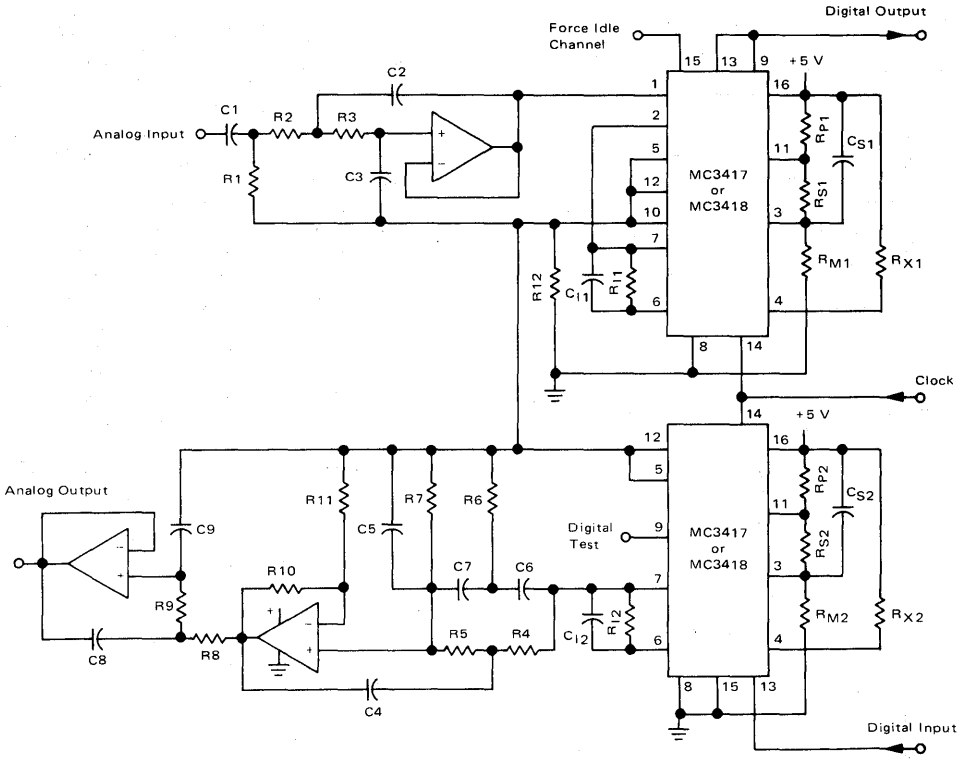
*A larger value for C2 is required in the decoder circuit than in the encoder to adjust the level linearity with frequency. In Figure 18, 0.050 μF would work well.

FIGURE 20 – HIGH PERFORMANCE ELLIPTIC FILTER FOR CVSD OUTPUT



Designed for 0.28 dB ripple in the pass band
ω_n = 3 kHz
ω_s = ≅ 6 kHz
AdB at ω_s and above 29.5 dB

FIGURE 21 – FULL DUPLEX/32K BIT CVSD VOICE CODEC USING MC3517/18 AND MC3503/6 OP AMP



Codec Components

R_{X1}, R_{X2} – 3.3 kΩ
R_{P1}, R_{P2} – 3.3 kΩ
R_{S1}, R_{S2} – 100 kΩ
R_{I1}, R_{I2} – 20 kΩ
R_{12} – 1 kΩ
R_{M1}, R_{M2} – 5 MΩ (MC3417)
Minimum step size = 20 mV
R_{M1}, R_{M2} – 15 MΩ (MC3418)
Minimum step size = 6 mV

C_{S1}, C_{S2} – 0.05 μF
C_{I1}, C_{I2} – 0.05 μF

2 MC3417 (or MC3418)
1 MC3403 (or MC3406)

Note: All Res. 5%
All Cap. 5%

Input Filter Specifications

12 dB/Octave Rolloff above 3.3 kHz
6 dB/Octave Rolloff below 50 Hz

Output Filter Specifications

Break Frequency – 3.3 kHz
Stop Band – 9 kHz
Stop Band Atten. – 50 dB
Rolloff – 40 dB/Octave

Filter Components

R1 – 965 Ω	C1 – 3.3 μF
R2 – 72 kΩ	C2 – 837 pF
R3 – 72 kΩ	C3 – 536 pF
R4 – 63.46 kΩ	C4 – 1000 pF
R5 – 127 kΩ	C5 – 222 pF
R6 – 365.5 kΩ	C6 – 77 pF
R7 – 1.645 MΩ	C7 – 38 pF
R8 – 72 kΩ	C8 – 837 pF
R9 – 72 kΩ	C9 – 536 pF
R10 – 29.5 kΩ	
R11 – 72 kΩ	

Note: All Res. 0.1% to 1%.
All Cap. 1.0%

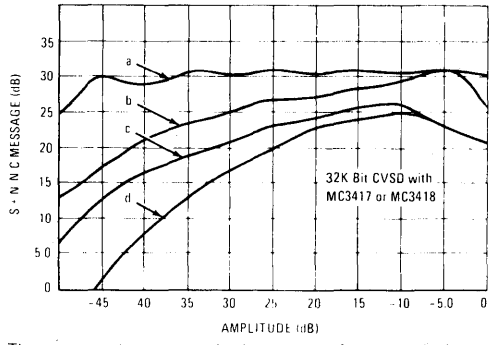
COMPARATIVE CODEC PERFORMANCE

The salient feature of CVSD codecs using the MC3517 and MC3518 family is versatility. The range of codec complexity tradeoffs and bit rate is so wide that one cannot grasp the interdependency of parameters for voice applications in a few pages.

Design of a specific codec must be tailored to the digital channel bandwidth, the analog bandwidth, the quality of signal transmission required and the cost objectives. To illustrate the choices available, the data in Figure 22 compares the signal-to-noise ratios and dynamic range of various codec design options at 32K bits. Generally, the relative merits of each design feature will remain intact in any application. Lowering the bit rate will reduce the dynamic range and noise performance of all techniques. As the bit rate is increased, the overall performance of each technique will improve and the need for more complex designs diminishes.

Non-voice applications of the MC3517 and MC3518 are also possible. In those cases, the signal bandwidth and amplitude characteristics must be defined before the specification of codec parameters can begin. However, in general, the design can proceed along the lines of the voice applications shown here, taking into account the different signal bandwidth requirements.

FIGURE 22 – COMPARATIVE CODEC PERFORMANCE – SIGNAL-TO-NOISE RATIO FOR 1 kHz TEST TONE



These curves demonstrate the improved performance obtained with several codec designs of varying complexity.

Curve a – Complex companding and double integration (Figure 18 – MC3418)
Curve b – Double integration (Figure 21 using Figure 6 – MC3418)
Curve c – Single integration (Figure 21 – MC3418) with 6 mV step size
Curve d – Single integration (Figure 21 – MC3417) with 25 mV step size

THERMAL INFORMATION

The maximum power consumption an integrated circuit can tolerate at a given operating ambient temperature, can be found from the equation:

$$P_{D(T_A)} = \frac{T_{J(max)} - T_A}{R_{\theta JA}\,(Typ)}$$

Where: $P_{D(T_A)}$ = Power Dissipation allowable at a given operating ambient temperature. This must be greater than the sum of the products of the supply voltages and supply currents at the worst-case operating condition.

$T_{J(max)}$ = Maximum Operating Junction Temperature specified in the Maximum Ratings Section
T_A = Maximum Desired Operating Ambient Temperature
$R_{\theta JA}(Typ)$ = Typical Thermal Resistance Junction to Ambient

MOTOROLA

MC3419-1L
MC3419A-1L
MC3419C-1L

2

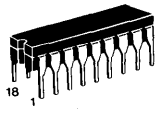
TELEPHONE LINE-FEED CIRCUIT

. . . designed as the heart of a circuit to provide BORSHT functions for telephone service in Central Office, PABX, and Subscriber Carrier equipment. This circuit provides dc power for the telephone (Battery), Overvoltage protection, Supervision features such as hook status and dial pulsing, two-wire differential to four-wire single-ended conversions and suppression of longitudinal signals at the two-wire input (Hybrid), and facilitates ringing insertion, Ring trip detection and Testing.

- Totally Upward Compatible with the MC3419
- All Key Parameters Externally Programmable
- Current Sensing Outputs Monitor Status of Both Tip and Ring Leads for Auxiliary Functions such as: Ground Key, Ring Trip, Message Waiting Lamp, etc.
- On-Hook Power Below 5.0 mW
- Digital Hook Status Output
- Powerdown Input
- Ground Fault Protection
- Operates from Single −20 V to −56 V Power Source
- Size and Weight Reduction Over Conventional Approaches
- The sale of this product is licensed under Patent No. 4,004,109. All royalties related to this patent are included in the unit price.

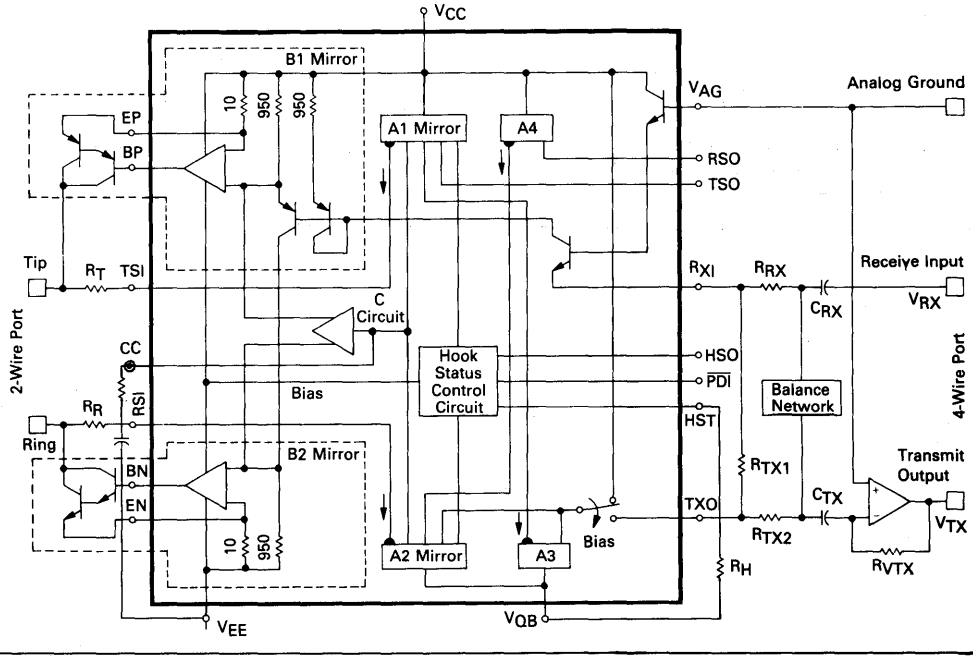
SUBSCRIBER LOOP INTERFACE CIRCUIT (SLIC)

BIPOLAR LASER-TRIMMED INTEGRATED CIRCUIT



L SUFFIX
CERAMIC PACKAGE
CASE 726-01

FUNCTIONAL BLOCK DIAGRAM



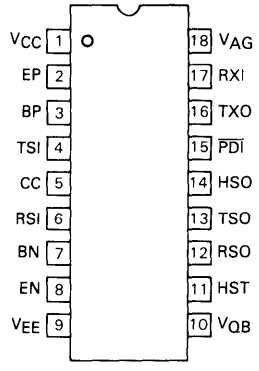
MAXIMUM RATINGS (Voltages Referenced to V_{CC}.)

Rating	Symbol	Value	Unit
Voltage	V_{EE} V_{QB}	−60 V_{EE} − 1.0 V	Vdc
Powerdown Input Voltage Range	$V_{\overline{PDI}}$	+15 to −15	Vdc
Sense Current Steady State Pulse — Figure 4	I_{TSI}, I_{RSI}	 100 200	mAdc
Storage Temperature Range	T_{stg}	−65 to +150	°C
Operating Junction Temperature (θ_{JA} = 100°C/W Typ)	T_J	150	°C

OPERATING CONDITIONS (Voltages Referenced to V_{CC}.)

Rating	Symbol	Value	Unit
Operating Ambient Temperature Range	T_A	0 to +70	°C
Loop Current	I_L	10 to 120	mA
Voltage	V_{EE} V_{QB}	−20 to −56 −20 to V_{EE}	Vdc
Analog Ground (I_L = 0 to 60 mA) (I_L = 0 to 120 mA)	V_{AG}	 0 to −12 −2.5 to −12	Vdc
Supervisory Output Voltage Compliance Range	V_{RSO}, V_{TSO}	−2.0 to −20	Vdc
Hook Status Output	V_{HSO}	+15 to −20	Vdc
Loop Resistance	R_L	0 to 2500	Ω

PIN CONNECTIONS



TRANSMISSION CHARACTERISTICS (R_L = 600 Ω unless otherwise noted.)

Characteristic	Figure	Symbol	Min	Typ	Max	Unit
Transmit and Receive Gain Variation (Insertion Loss) (1.0 kHz @ 0 dBm Input)	1	V_{TX}/V_L, V_L/V_{RX}				dB
MC3419-1			−0.3	0	+0.3	
MC3419A-1			−0.15	0	+0.15	
MC3419C-1			−0.4	0	+0.4	
Transhybrid Rejection (Input — 1 kHz @ 0 dBm) Fixed (1%) Resistor Balance Network	1	V_{TX}/V_{RX}				dB
MC3419-1, MC3419C-1			−23	−35	—	
MC3419A-1			−33	−40	—	
Trimmed Balance Network All Types			—	−55	—	
Level Linearity (−48 to +3.0 dBm, referenced to 0 dBm @ 1 kHz)	1					dB
Transmission		V_{TX}/V_L	−0.1	0	+0.1	
Reception		V_L/V_{RX}	−0.1	0	+0.1	
Frequency Response (200–3400 Hz referenced to 1.0 kHz @ 0 dBm)	1					dB
Transmission		V_{TX}/V_L	−0.1	0	+0.1	
Reception		V_L/V_{RX}	−0.1	0	+0.1	
Total Distortion @ 1.0 kHz, 0 dBm (C-Message Filtered)	1	V_L/V_{RX} V_{TX}/V_L	— —	−60 −60	— —	dB

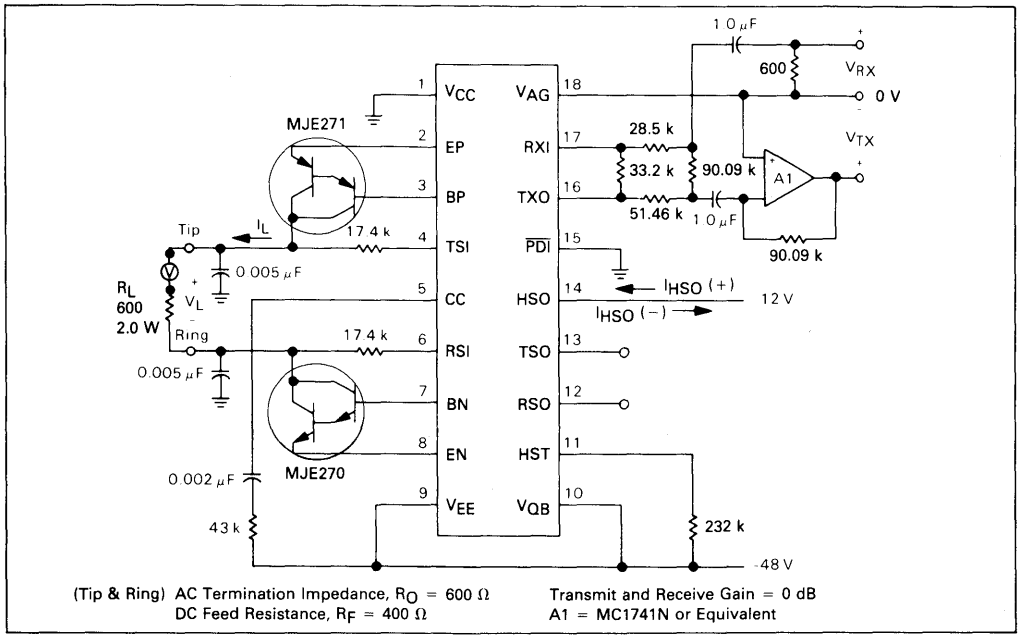
TRANSMISSION CHARACTERISTICS (continued) (R_L = 600 Ω unless otherwise noted.)

Characteristic	Figure	Symbol	Min	Typ	Max	Unit
Idle Channel Noise (V_{RX} = 0 V)	1	V_{TX}, V_L				dBrnC
MC3419-1, MC3419A-1			—	3.0	10	
MC3419C-1			—	4.0	13	
Return Loss (referenced to 600 ohms) @ 1.0 kHz, 0 dBm	1	$20 \text{ Log } \left\lvert \frac{R_0 - 600}{R_0 + 600} \right\rvert$				
MC3419A-1			36	—	—	dB
MC3419-1, MC3419C-1			30	—	—	dB
Longitudinal Induction (60 Hz) (I_{LON} = 35 mA RMS)	2	V_{TX}	—	5.0	—	dBrnC
Longitudinal Balance	2	V_{TX}/V_{LON}, V_L/V_{LON}				dB
MC3419-1 (200–3000 Hz)			−45	—	—	
MC3419A-1 (200–1000 Hz)			−50	—	—	
MC3419A-1 (3000 Hz)			−48	—	—	
MC3419C-1 (200–3000 Hz)			−40	—	—	

ELECTRICAL CHARACTERISTICS (V_{EE} = −48 V, V_{QB} = V_{EE}, V_{AG} = 0 V, R_L = 600 Ω, T_A = 25°C unless otherwise noted.)

Characteristic	Figure	Symbol	Min	Typ	Max	Unit
Propagation Delay	1	T_P, V_{RX} to V_L	—	750	—	ns
		V_{RX} to I_{TX}	—	1.2	—	μs
Supply Current — On-Hook (V_{EE} = V_{QB} = 56 V, R_L > 100 MΩ)	3	I_{VCC}				μA
MC3419-1, MC3419A-1			—	40	200	
MC3419C-1			—	100	500	
On-Hook Power Dissipation (R_L > 100 MΩ)	3	P_D				mW
MC3419-1, MC3419A-1			—	1.0	—	
MC3419C-1			—	2.5	—	
Power Supply Noise Rejection (1.0 kHz @ 1.0 V_{RMS})	3	V_{TX}/V_{ee}				dB
MC3419-1, MC3419A-1			−40	—	—	
MC3419C-1			−30	—	—	
Quiet Battery Noise Rejection (1.0 kHz @ 1.0 V_{RMS})	3	V_{TX}/V_{qb}	—	−6.0	—	dB
Sense Current	4					mA/mA
Tip		I_{TSO}/I_{TSI}	0.15	0.17	0.19	
Ring		I_{RSO}/I_{RSI}	0.15	0.17	0.19	
Fault Currents	1					mA
Tip to V_{CC}		I_{Tip}	—	0	—	
Ring to V_{CC}		I_{Ring}	—	2.5	—	
Tip to Ring		I_{Loop}	—	120	—	
Tip and Ring to V_{CC}		I_{Tip} and I_{Ring}	—	2.5	—	
Analog Ground Current	1	I_{VAG}	—	0.1	2.0	μA
Powerdown Logic Levels		$I_{\overline{PDI}}$	—	−1.0	−10	μA
		V_{IH}	−1.2	—	—	Vdc
		V_{IL}	—	—	−4.0	Vdc
Hook Status Output Current	1	I_{HSO}				
(R_L < 2.5 kΩ, V_{HSO} = +0.4 Vdc)			+1.0	+3.0	—	mA
V_{HSO} = −0.4 Vdc)			−0.4	−1.5	—	mA
(R_L > 10 kΩ, V_{HSO} = +12 Vdc)			—	0	+50	μA
V_{HSO} = −12 Vdc)			—	0	−2.0	μA

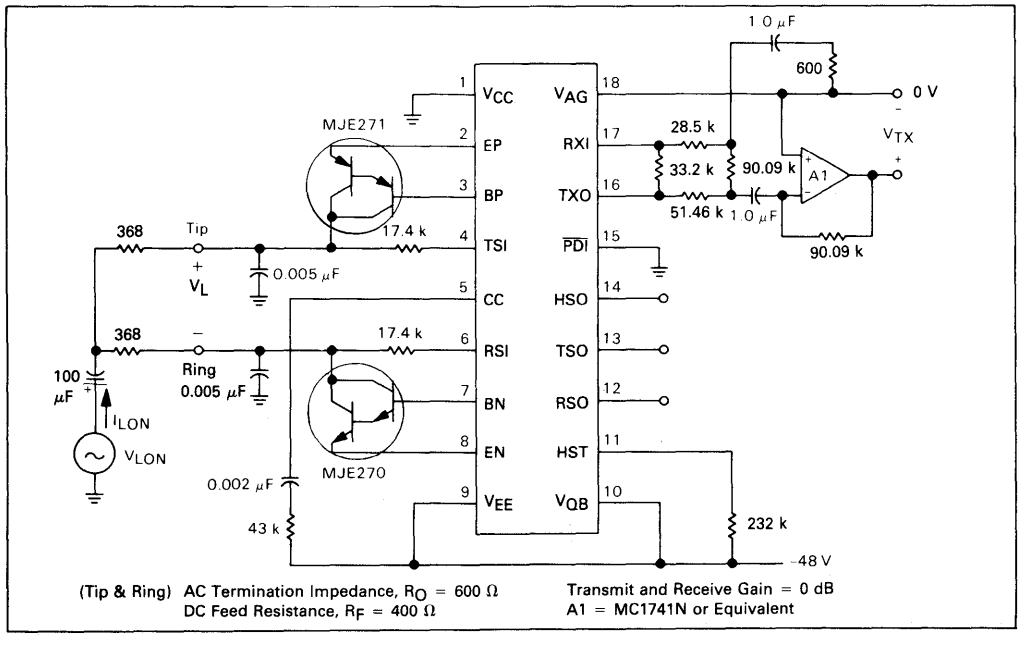
FIGURE 1 — AC TEST CIRCUIT



(Tip & Ring) AC Termination Impedance, R_O = 600 Ω
DC Feed Resistance, R_F = 400 Ω

Transmit and Receive Gain = 0 dB
A1 = MC1741N or Equivalent

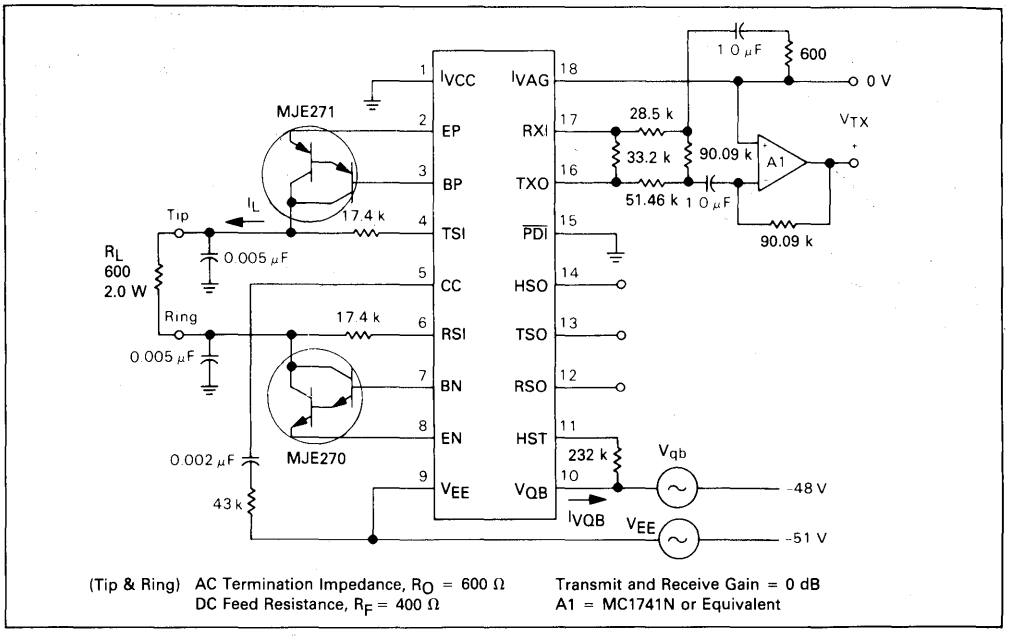
FIGURE 2 — LONGITUDINAL BALANCE TEST CIRCUIT



(Tip & Ring) AC Termination Impedance, R_O = 600 Ω
DC Feed Resistance, R_F = 400 Ω

Transmit and Receive Gain = 0 dB
A1 = MC1741N or Equivalent

FIGURE 3 — SUPPLY NOISE REJECTION TEST CIRCUIT



(Tip & Ring) AC Termination Impedance, R_O = 600 Ω
DC Feed Resistance, R_F = 400 Ω

Transmit and Receive Gain = 0 dB
A1 = MC1741N or Equivalent

FIGURE 4 — TSO AND RSO SUPERVISORY OUTPUT TEST CIRCUIT

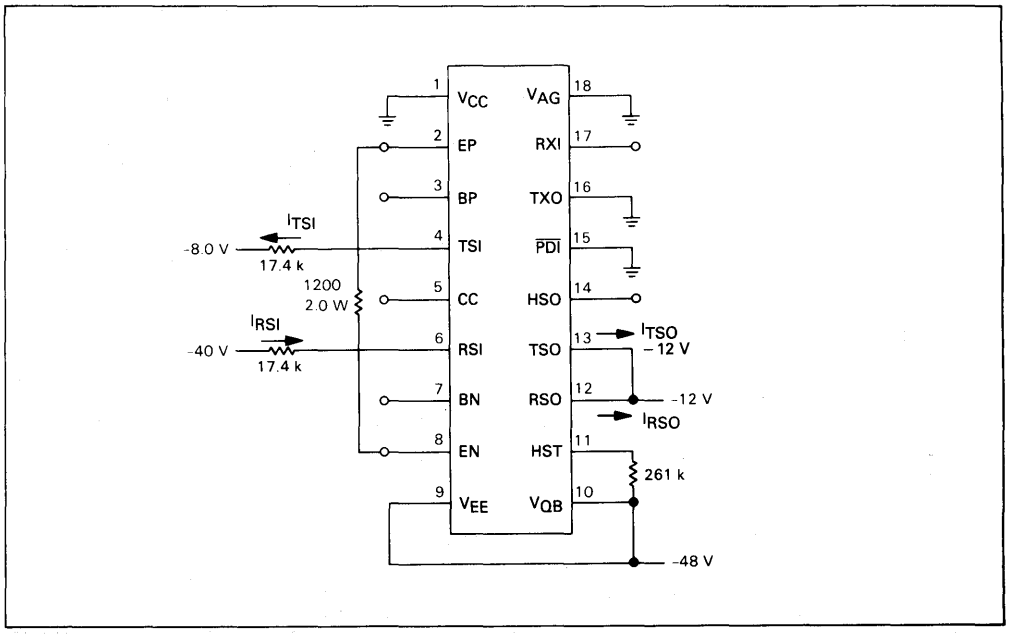


FIGURE 5 — QUIET BATTERY CURRENT I_{VQB} versus LOOP CURRENT I_L

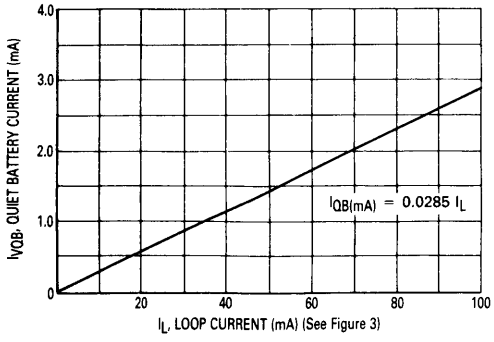
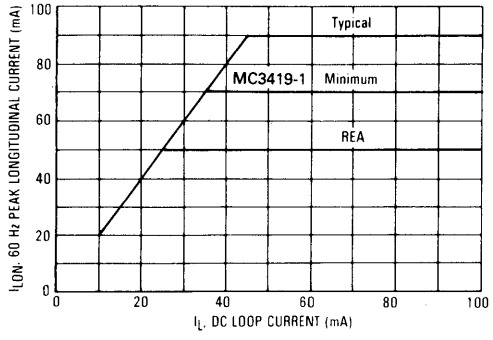


FIGURE 6 — LONGITUDINAL CAPACITY



2

PIN DESCRIPTIONS

Pin	Name	Function
1	V_{CC}	The positive supply voltage. This point is ground in typical applications.
2, 8	EP & EN	Loop current sensing inputs. These are connected to the emitters of the PNP and NPN Darlington transistors. They are tied through 10 Ω resistors to V_{CC} and V_{EE}, respectively. The maximum continuous current through these inputs is 240 mA.
3, 7	BP & BN	Base drive outputs. These pins drive the bases of the PNP and NPN transistors and are able to sink or source, respectively, up to 5.0 mA.
4, 6	TSI & RSI	Tip and Ring voltage Sensing Inputs. They are low impedance inputs (approximately 600 Ω each i.e., 400 Ω + 3 diodes) that translate the voltages on Tip and Ring to a current through resistors R_T and R_R. TSI is referenced to V_{CC} and RSI is referenced to V_{QB}. These pins have 6.0 V zener diodes (to their respective reference) for protection against overvoltage line surges.
5	CC	Compensation Capacitor pin. This pin is used to stabilize the longitudinal or common mode circuitry.
9	V_{EE}	Negative supply voltage. This pin ties to the chip substrate. Its operating voltage range is −20 V to −56 V. It can withstand −60 V without damage and can sustain a voltage surge to −75 V for less than 4.0 ms without significant degradation of performance. Most of the loop current and bias currents flow through this pin.
10	V_{QB}	Quiet Battery Voltage reference. This is the voltage reference for the RSI pin. Its voltage must not go more negative than V_{EE}. The current through this pin, while powered up, is proportional to the loop current, allowing it to be used for loop current limiting. The voltage on this pin, less 4 volts, is the "effective battery feed voltage for the 2-wire lines even though most of the power comes from the V_{EE} supply.
11	HST	Hook Status Threshold programming resistor input. R_H determines the value of loop resistance at which on-hook and off-hook status is switched.
12	RSO	Ring Sense current Output. This output reflects the voltage status of the Ring terminal for voltages more positive than V_{QB}. The current is sourced from this output, it is one-sixth I_{RSI}, its voltage range is 0 to −20 V and its saturation voltage is approximately −2.0 V.
13	TSO	Tip Sense current Output. This output reflects the voltage status of the Tip terminal for voltages more negative than V_{CC}. The current is sourced from this output, it is one-sixth I_{TSI}, its voltage range is 0 V to −20 V and its saturation voltage is approximately −2.0 V.
14	HSO/$\overline{\text{HSO}}$	Hook Status Output. This is a digital output that reflects the condition of the loop resistance. If loop resistance is less than a predetermined value established by R_H, usually $R_L < 2.5$ kΩ, the HSO pin will be active, i.e., with positive voltage logic (a resistor tied from a +5.0 V or +12 V supply to HSO), this pin will sink current to V_{CC} ($V_{HSO} \cong 0$ V); with negative voltage logic (a resistor tied from a −12 V supply to HSO), this pin will source current from V_{CC} ($V_{HSO} \cong 0$ V). If loop resistance is greater than a predetermined value again established by the same resistor R_H, usually $R_L > 10$ kΩ, the HSO pin is inactive, i.e., V_{HSO} = logic supply voltage.
15	$\overline{\text{PDI}}$	Powerdown Input pin. This pin is used to deny service to the subscriber. A logic level "0" ($V_{IL} <$ −4.0 V) powers down the MC3419-1 except for HSO, TSO and RSO. The voltage range of this high impedance input pin is ±15 V.
16	TXO	Transmit current Output. This output sinks current to V_{QB} and is proportional to $I_{TSI} + I_{RSI}$ by a ratio of K1 where: K1 = 0.51. Its saturation voltage is V_{QB} + 2.5 V typ. (+3.5 V over the temperature range). This pin is only active during the off-hook power-up condition.
17	RXI	Receive Input. This input sums ac currents from TXO and the receive voltage input (V_{RX}) and sources all the dc current to TXO. It has a low input impedance (15 Ω) typically biased 4.5 V below the V_{AG} pin voltage during off-hook power-up conditions. During powerdown conditions, the voltages on RXI and TXO can drift up to V_{AG}.
18	V_{AG}	Analog Ground Voltage reference input. The input impedance of this pin is much greater than 1.0 MΩ. It should be ac coupled to system ground and could be direct coupled if system ground is between 0 V and −12 V. AC coupling requires 300 kΩ to V_{CC} and 0.1 μF to system ground. If V_{CC} and system ground are common, tie V_{AG} directly to V_{CC}. If dc loop currents are allowed to go higher than 60 mA, V_{AG} should be biased from −2.5 V to −12 V to avoid problems at high ambient temperatures.

FUNCTIONAL DESCRIPTION

Referring to the functional block diagram on page 1, line sensing resistors (R_R and R_T) at the TSI and RSI pins convert voltages at the Tip and Ring terminals into currents which are fed into current mirrors* A1 and A2. An output of A1 is mirrored by A3 and summed together with an output of A2 at the TXO terminal. Thus, a differential to single-ended conversion is performed from the ac line signals to the TXO output.

All the dc current at the TXO output is fed back through the RXI terminals to the B1 mirror input. The inputs to B1 and B2 are made equal by mirroring the B1 input current to the B2 input through a unity gain output of the B1 mirror. Both B1 and B2 mirrors have high gain outputs (x95) which drive the subscriber lines with balanced currents that are equal in amplitude and 180° out of phase. The feedback from the TXO output, through the B-Circuit mirrors, to the subscriber line produces a dc feed resistance significantly less, but proportional to the loop sensing resistors.

In most line-interface systems, the ac termination impedance is desired to be greater than the dc feed impedance. A differential ac generator on the subscriber loop would be terminated by the dc feed impedance if the total ac current at the TXO output were returned to the B1 input along with the dc current. Instead, the MC3419-1 system diverts part of the ac current from the B-Circuit mirrors. This decreases the ac feedback current, causing the ac termination impedance at the line interface to be greater than the dc feed impedance.

The ac current that is diverted from the B1 mirror input is coupled to a current-to-voltage converter circuit that has a low input impedance. This circuit consists of an op amp (external to the MC3419-1) and a feedback resistor which produces the transmit output voltage (V_{TX}) at the 4-wire interface. Transmission gain is programmed by the op amp feedback resistor (R_{VTX}).

Reception gain is realized by converting the ac coupled receive input voltage (V_{RX}) to a current through an external resistor (R_{RX}) at the low impedance RXI terminal. This current is summed at RXI with the dc and ac feedback current from the A-Circuit mirrors and drives the B1 mirror input. The B-Circuit mirror outputs drive the 2-wire port with balanced ac current proportional to the receive input voltage. Reception gain is programmed by the R_{RX} resistor.

Since receive input signals are transmitted through the MC3419-1 to the 2-wire port, and the 2-wire port signals are returned to the 4-wire transmit output, a means of cancellation must be provided to maintain 4-wire signal separation (transhybrid rejection). Cancellation is complicated because the gain from the receive port to the transmit port depends on the impedance of the subscriber loop. A passive "balance network" is used to achieve transhybrid rejection by cancelling, at the low impedance input to the transmit op amp, the current reflected by the loop impedance to the 4-wire transmit output. For a resistive loop impedance, a single resistor provides the cancellation. For reactive loops, the balance network should be reactive.

Longitudinal (common-mode) currents that may be present on the subscriber lines are suppressed in the MC3419-1 by two methods. The first is inherent in the mirror configuration. Positive-going longitudinal currents into Tip and Ring create common-mode voltages that cause a decreasing current through the Tip Sensing resistor and an increasing current through the Ring Sensing resistor. When these equal and opposite signal currents are reflected through the A-Circuit mirrors and summed together at TXO, the total current at TXO remains unchanged. Therefore, the ac currents due to the common-mode signal are cancelled before reaching the transmit output.

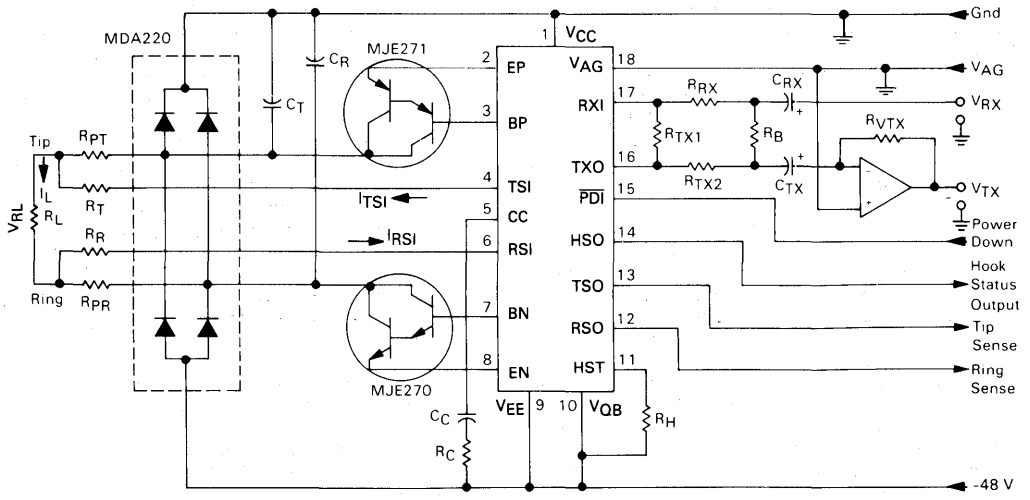
The second longitudinal suppression method is more dominant, since it limits the amplitude of common-mode voltages that appear at the Tip and Ring terminals.

A common-mode suppression circuit detects common-mode inputs and drives the loop with balanced currents to reduce the input amplitude. Subtracting currents from outputs of the A1 and A2 mirrors produces a signal current at the CC terminal in response to the common-mode voltage at Tip and Ring. A transconductance amplifier (C-Circuit) generates a current proportional to the CC terminal voltage which is summed with the current from the RXI terminal at the inputs of current mirrors B1 and B2. The weighting and polarity of the summing networks produce common-mode B1 and B2 mirror output currents at the 2-wire port. The common-mode input impedance is inversely proportional to the gain of the longitudinal suppression circuit. R_C and C_C compensate the common-mode feedback loop. At 60 Hz with typical component values, the 2-wire common-mode impedance is less than 5 Ω.

The longitudinal suppression circuit output currents are generated by modulating dc current fed to the loop by the B1 and B2 current mirrors. This configuration avoids the increased power dissipation attributed to current mode loop drive because dc and longitudinal currents are not cumulatively sourced to the loop. However, driving common-mode currents through the B-circuit current mirrors in this manner limits the longitudinal suppression capability. The suppression circuit is unable to reverse 2-wire current polarities to maintain a low-impedance termination when longitudinal currents exceed the dc loop current. At low dc loop currents, the common-mode signal capability, known as longitudinal capacity, is limited by the loop current (Figure 6). At high-loop currents, longitudinal capacity is limited by the maximum voltage swing of the CC terminal and is therefore independent of dc loop current.

*A current mirror is a circuit which behaves as a current controlled current source. It has a single low-impedance input terminal with respect to a reference point and one or more high impedance outputs.

FIGURE 7 — BASIC SLIC CIRCUIT



The hook status control circuit supplies the bias currents to activate the B-Circuit op amps and other sections of the MC3419-1. To activate the bias currents, the control circuit compares the current through the sense resistors, R_R and R_T, and the load resistance R_L with the current through the hook status threshold programming resistor, R_H, by using outputs from both A1 and A2 mirrors. The A1 mirror output sources current to the R_H resistor. (This reduces all internal currents to near zero during the on-hook state in order to eliminate unnecessary power consumption.) If this current is large enough the voltage on the HST pin will trip an internal comparator, then another circuit compares the current from the A1 output with that of an A2 output. These currents must match within ±15%. If so, HSO will be activated and the bias circuits will turn on provided the voltage on $\overline{PDI}$ is greater than −1.2 V. The HSO pin can have either a pull-up resistor or a pull-down resistor and when activated it will switch to V_{CC} (0 volts).

Once the MC3419-1 is powered up, a circuit with a gain of 20 feeds current to the R_H resistor in order to keep the bias circuitry active. (The sense resistors are paralleled with the Darlington transistors which reduces the sense input currents.) Should the sense input currents drop below one-twentieth of the required power-up current, the bias currents will be removed, forcing a power-down condition.

Current mode analog signal processing is critically dependent on voltage to current conversion at the 2-wire and 4-wire inputs. Precise, low-noise voltage sensing through resistors R_T, R_R and R_{RX} requires quiet, low impedance terminations at terminals TSI, RSI and RXI respectively. For 2-wire signals, terminal V_{QB} isolates the loop-sensing resistors and current mirrors from noise at the high-current V_{EE} terminal. External filtering from V_{CC} to V_{QB} ("quiet battery" terminal) ensures loop voltages are sensed without interference from system supply noise. V_{EE} noise rejection at audio frequencies is typically 60 dB or greater.

Receive input terminal RXI is referenced to the V_{AG} terminal which references the 4-wire input to the "analog ground" of the 4-wire signal source, thus isolating the input from power ground voltage transients. This isolation offers 70 dB of noise rejection at audio frequencies.

SYSTEM EQUATIONS

K1 — The current gain from $I_{TSI} + I_{RSI}$ to TXO only during an off-hook power-up condition. K1 = 0.51 ± 1%.

K2 — The current gain from RXI to the collectors of the off-chip Darlington transistors only during an off-hook power-up condition. K2 = 95 ± 1%.

For simplicity, the following equations do not use K1 or K2. Instead the actual numerical value is used, for instance (1 + [2]K1K2) = 1 + 1.02 x 95 = 97.9 is approximately 98.

R_L — Loop resistance. This is a load resistance from Tip to Ring and can be either ac or dc depending on context.

LOOP CURRENT REGULATIONS

FIGURE 8(a)

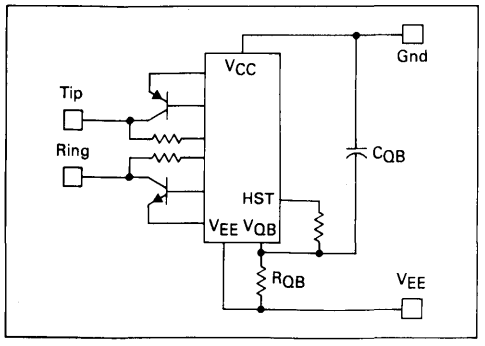


FIGURE 9(a)

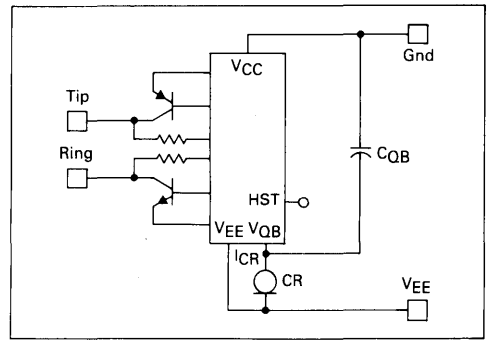


FIGURE 8(b)

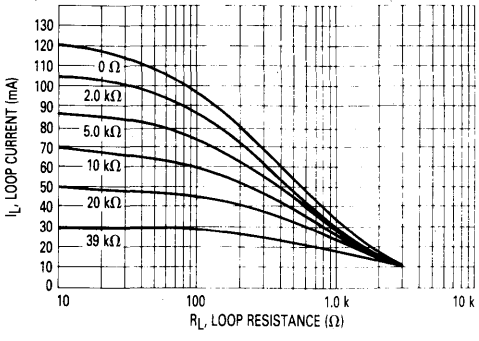
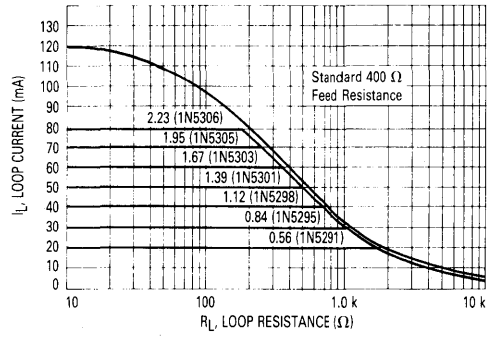


FIGURE 9(b)



SYSTEM EQUATIONS (continued)

Z_L — Loop impedance. This is used only to connote a complex impedance loading on Tip and Ring.

I_L — Loop current. The dc current flow through R_L.

R_F — Dc feed resistance. The synthesized resistance from which battery (V_{CC} and V_{EE}) current is fed to R_L. The battery feed resistance is balanced differential feed. See Figure 7. (This assumes $V_{QB} = V_{EE}$.) The first order equation is:

$$R_F = \frac{R_R + R_T + 1200\ \Omega}{98} \quad (1)$$

Because of the diode voltage drops on TSI and RSI, the actual dc feed resistance is higher. The second order equation is:

$$R_F = \frac{|V_{QB}|(98\ R_L + R_R + R_T + 1200\ \Omega)}{98\ (|V_{QB}| - 4.0\ V)} - R_L \quad (2)$$

ignoring the effects of R_L

$$R_F = \frac{|V_{QB}|(R_R + R_T + 1200\ \Omega)}{98\ (|V_{QB}| - 4.0\ V)} \quad (3)$$

So:

$$R_R = R_T = \frac{49R_F\ (|V_{QB}| - 4.0\ V)}{|V_{QB}|} - 600 \quad (4)$$

The minimum value for R_R and R_T is 5.0 kΩ.

The first order value of R_F can not be greater than the desired value of the termination impedance (usually 600 Ω or 900 Ω). To achieve dc feed resistances that are greater, a resistor can be placed between V_{QB} and V_{EE} along with a filter capacitor C_{QB} which restores the desired termination impedance and filters power supply noise. A diode should also be placed between V_{QB} and V_{EE} to prevent damage in case a catastrophic power supply failure occurs.

I_{VQB} — This is the current that is sourced from the V_{QB} pin and is proportional to the currents into and out of RSI and TSI. When the SLIC is in the off-hook power-up mode, I_{VQB} is also proportional to I_L.

$$I_{VQB} = 2.15\, I_{RSI} + 0.7\, I_{TSI} \quad (5)$$

$$I_{VQB} = 0.029\, I_L \quad (6)$$

R_{FQ} — Dc feed resistance. The synthesized resistance from which battery current is fed to R_L, see Figure 8. (This assumes V_{QB} is tied to V_{EE} through a resistor R_{QB}.) R_{QB} synthesizes additional dc feed resistance to the R_F value previously stated.

When using R_{QB}, the dc feed is effectively balance fed from V_{CC} and V_{QB} instead of V_{EE}. The sense resistors (R_R and R_T) should be selected to make R_F (first order) less than the termination impedance.

$$R_{FQ} = \frac{|V_{EE}|(98R_L + R_R + R_T + 1200 + 2.85R_{QB})}{98(|V_{EE}| - 4.0\ V)} - R_L \quad (7)$$

Ignoring R_L, this simplifies to:

$$R_{FQ} = \frac{|V_{EE}|(R_R + R_T + 1200 + 2.85R_{QB})}{98(|V_{EE}| - 4.0\ V)} \quad (8)$$

Therefore:

$$R_{QB} = \frac{98R_{FQ}(|V_{EE}| - 4.0\ V) - |V_{EE}|(R_R + R_T + 1200\ \Omega)}{2.85|V_{EE}|} \quad (9)$$

C_{QB} — Power supply noise filter capacitor.

$$C_{QB} = \frac{2.85\, R_{QB} + R_R + R_T + 1200\ \Omega}{2\pi f\, R_{QB}\,(R_R + R_T + 1200\ \Omega)} \quad (10)$$

Figure 9B shows R_{QB} replaced with a current regulating device such as Motorola's 1N5283 family.

I_{CRQB} — The current that is sourced to a current regulating device from the V_{QB} pin. When this current reaches the regulated value, the voltage differential between V_{EE} and V_{QB} increases causing the effective battery voltage to decrease which limits I_L to a maximum value as determined below:

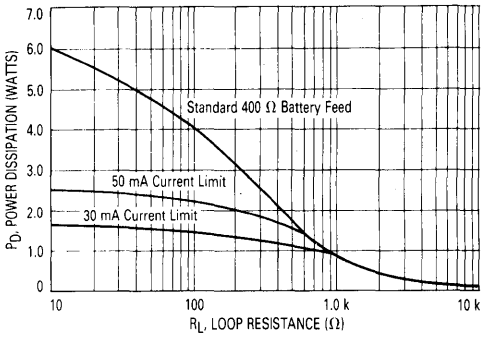
$$I_L = 34.5\, I_{CRQB} \quad (11)$$

The graph, Figure 9B, shows loop current versus loop resistance using several values of I_{CRQB}. The closest current regulating diode part number to that value is also shown. A typical value for C_{QB} in this case is 10 μF, 60 Vdc.

Figure 10 shows how power can be conserved on the shorter loop lengths by utilizing current limiting techniques.

Overvoltage protection on the 2-wire port is achieved with the MDA220 diode bridge and the protection resistors R_{PR} and R_{PT}. Whenever the voltage on the 2-wire port exceeds the power supply rails (V_{CC} and V_{EE}), the MDA220 diodes will forward bias and "clamp" to the rail voltage. The current is limited by the protection resistors. These resistors should be as large in value as possible. However, if they are too large, they will interfere with the performance of the SLIC under worst case conditions.

FIGURE 10 — TOTAL SLIC POWER DISSIPATION versus LOOP RESISTANCE



$$R_{PT} < R_T/196 - 15 \quad (12)$$

Using the voltage of V_{QB} when I_L is at its minimum off-hook value (Typ. 20 mA):

$$R_{PR} < R_R/196 + 25|V_{EE} - V_{QB}| - 15 \quad (13)$$

The tolerance of these resistors is not critical due to placement inside a closed loop. Positive temperature co-efficient resistors (PTC) may be considered here. Consult resistor manufacturers for component selections that will meet the surge current and peak voltage requirements.

Because the MC3419-1 is a broadband device it requires compensation components to keep its circuits stable.

C_R & C_T — Compensates the longitudinal gain of the A and the B circuit mirrors. Their values range from 2000 pF to 5000 pF.

R_C & C_C — Compensates the longitudinal "C" circuitry. Their values can be ratioed according to:

$$R_C \times C_C = R_T \times C_T. \quad (14)$$

Two off-chip power Darlington transistors are used with the MC3419-1. These transistors reduce any temperature gradiant problems with the precision matched devices on-chip and they alleviate thermal stress conditions that could occur for every on-hook and off-hook transition. The power dissipation in these devices is:

$$P_{QT} = I_L{}^2(R_T/98 - R_{PT} - 4) + (2.0\ V)I_L \quad (15)$$

$$P_{QR} = I_L\,[|V_{EE}| - 2 - I_L(R_T/98 + R_L + R_{PR} + 16)] \quad (16)$$

where $I_L = |V_{EE}|/R_{FQ}$ or $I_L(max)$ in current limited designs.

SYSTEM EQUATIONS (continued)

R_H — The resistor that determines the hook status threshold values of R_L. R_H is selected from a graph of the following two equations:

Off-hook threshold

$$R_H = 6(R_L + R_R + R_T) \quad (17)$$

On-hook threshold

$$R_H = 27.25\,[R_L + 0.01(R_R + R_T)] \quad (18)$$

FIGURE 11 — HOOK STATUS DETECTION

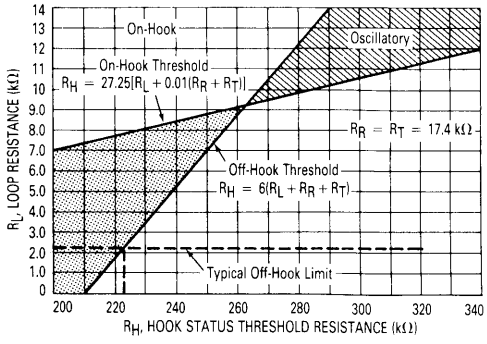


Figure 11 shows such a graph using 17.4 kΩ as the values for R_R and R_T. Note the oscillatory condition to the right of the crossing point. Selection of R_H in this region is usually not a problem since the majority of telephone lines do not fall into this resistance range. R_H always ties to V_{QB} and HST and will give reliable hook status information regardless of power supply voltages and $\overline{PDI}$.

R_O — Termination impedance of the 2-wire port. This impedance is greater than the dc feed resistance R_F because of a current splitting network in the feedback loop, R_{TX1} and R_{TX2}.

K3 — A constant, formed by R_{TX1} and R_{TX2}, between 0 and 1, which determines the ratio of the first order value of R_F to R_O.

$$R_O = \frac{R_R + R_T + 1200\ \Omega}{1 + 97K3} \quad (19)$$

So:

$$K3 = \frac{R_R + R_T + 1200\ \Omega - R_O}{97R_O} \quad (20)$$

and

$$K3 = \frac{R_{TX2} + Z_{in}}{R_{TX1} + R_{TX2} + Z_{in}} \quad (21)$$

Z_{in} — The input impedance of the current to voltage converter op amp. This impedance is usually negligible, it can be used to sway the selection of a 1% component value.

$$Z_{in} = \frac{(R_R + R_T + 1200\ \Omega)\,G_{TX}}{1020\,(1 - K3)} = \frac{R_{VTX}}{1000} \quad (22)$$

R_{TX1} — Feeds most of the TXO dc current to the RXI pin. To keep TXO from saturation the maximum value of R_{TX1} is as follows:

$$R_{TX1} < \frac{(R_R + R_T + 1200\ \Omega)\,(|V_{QB}|min - |V_{AG}|max - 6.5\ V)}{|V_{QB}|min - 5.4\ V} \quad (23)$$

Where:

$$|V_{QB}|min = \frac{(R_R + R_T + 1200\ \Omega)\,(|V_{EE}|min - 4)}{(R_R + R_T + 1200\ \Omega + 2.8\ R_{QB})} \quad (24)$$

or if a current regulator diode is used:

$$R_{TX1} < \frac{0.01\ I_L(max)\,(R_R + R_T + 600\ \Omega) - |V_{AG}|max - 3.9\ V}{0.01\ I_L(max)} \quad (25)$$

It is beneficial to make R_{TX1} as large as possible. Typical values range from 15 k to 24 kΩ.

$$R_{TX2} = \frac{K3\,R_{TX1}}{1 - K3} - Z_{in} \quad (26)$$

$$C_{TX} = \frac{R_R + R_T + 1200\ \Omega}{7R_{TX2}} \quad \text{The result is in } \mu F. \quad (27)$$

G_{TX} — The voltage gain from the 2-wire port to V_{TX} which is adjustable by R_{VTX}.

$$G_{TX} = \frac{1.02\,(1 - K3)\,R_{VTX}}{R_R + R_T + 1200\ \Omega} \quad (28)$$

$$R_{VTX} = \frac{G_{TX}(R_R + R_T + 1200\ \Omega)}{1.02\,(1 - K3)} \quad (29)$$

G_{RX} — The voltage gain from the V_{RX} input to the 2-wire port which is adjustable by R_{RX}.

$$G_{RX} = \frac{-95\,R_L\,(R_R + R_T + 1200\ \Omega)}{R_{RX}\,[(R_R + R_T + 1200\ \Omega) + R_L(1 + 97K3)]} \quad (30)$$

$$G_{RX} = \frac{-95\,R_L\,R_O}{R_{RX}(R_L + R_O)} \quad (31)$$

$$R_{RX} = \frac{95\,R_L\,R_O}{G_{RX}(R_L + R_O)} \quad (32)$$

$$C_{RX} > \frac{R_{RX} + R_B}{2\pi\,f\,R_{RX}R_B} \quad (33)$$

Where f is the minimum passband frequency, usually 200 Hz.

Transhybrid Rejection — The voltage gain from V_{RX} to V_{TX}. It is expressed in dB, the number should be negative and the larger the value the better. Transhybrid rejection is achieved by summing a current from the V_{RX} input (R_B) with the TXO current that flows to the current to voltage converter. R_B balances a resistive load, R_L.

$$R_B = \frac{R_{RX}(1 + 97K3)\,(R_O + R_L)}{97R_L\,(1 - K3)} \quad (34)$$

FIGURE 12 — BALANCE NETWORK FOR CAPACITIVE LINES

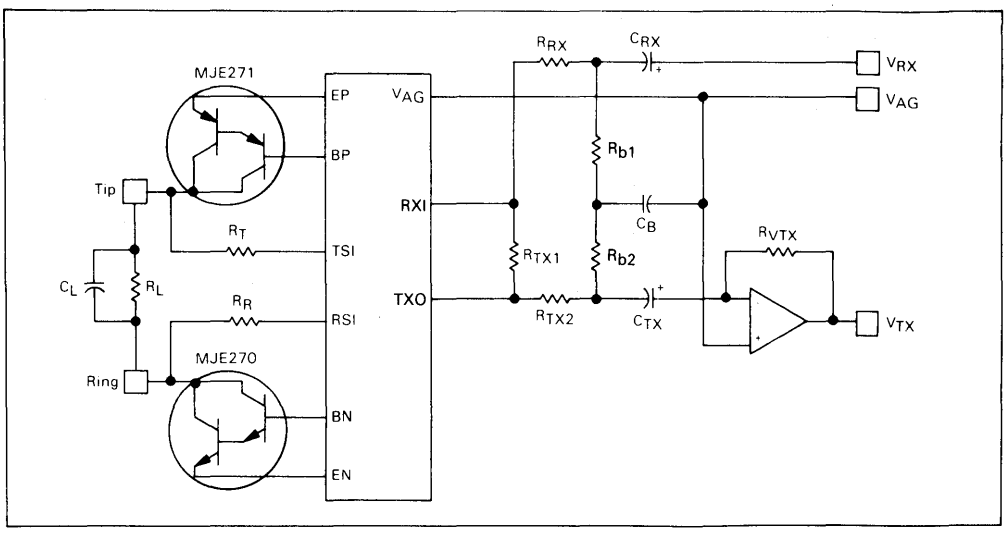
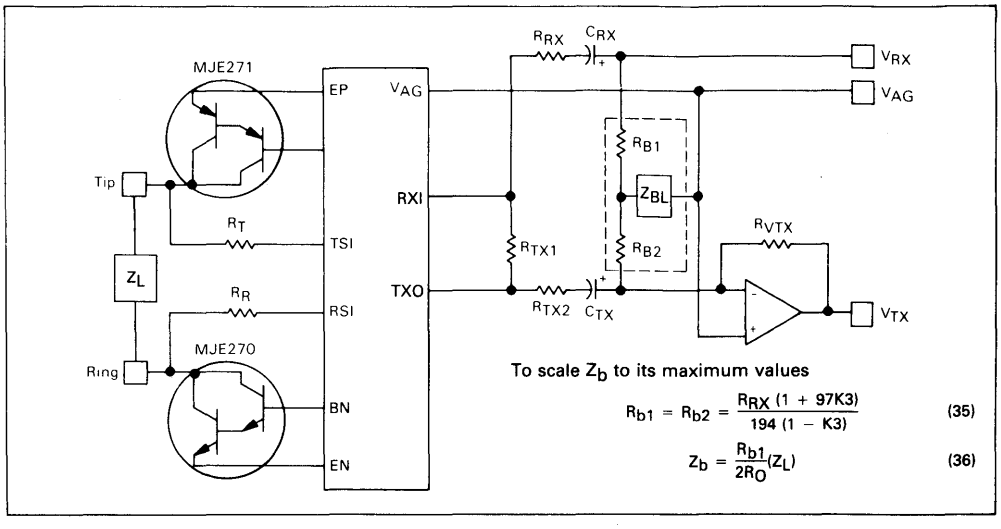


FIGURE 13 — BALANCE NETWORK FOR COMPLEX LOAD IMPEDANCES



To scale Z_b to its maximum values

$$R_{b1} = R_{b2} = \frac{R_{RX}\,(1 + 97K3)}{194\,(1 - K3)} \quad (35)$$

$$Z_b = \frac{R_{b1}}{2R_O}(Z_L) \quad (36)$$

When the 2-wire port has a parallel R and C load, then (see Figure 12):

$$R_{b1} = \frac{R_{RX}(R_R + R_T + 1200\ \Omega)}{97R_L\,(1 - K3)} \quad (37)$$

$$R_{b2} = \frac{R_{RX}(R_R + R_T + 1200\ \Omega)}{97R_O(1 - K3)} \quad (38)$$

$$C_b = \frac{R_L C_L}{R_{b2}} \quad (39)$$

When it is desirable to balance complex load impedances using component values that are equal to the load values (see Figure 13) then:

$$R_{b1} = \frac{R_{RX}(1 + 97K3)}{194(1 - K3)} + \sqrt{\left[\frac{R_{RX}(1 + 97K3)}{194(1 - K3)}\right]^2 - \frac{R_O R_{RX}(1 + 97K3)}{97(1 - K3)}} \quad (40)$$

$$R_{b2} = \frac{R_{RX}(1 + 97K3)}{97(1 - K3)} - R_{b1} \quad (41)$$

$$Z_b = Z_L \quad (42)$$

R_{b1} and R_{b2} values are interchangeable.

SYSTEM EQUATIONS (continued)

The Tip and Ring Sense Output currents are proportional to the currents out of and into TSI and RSI, respectively.

$$I_{TSO} = \frac{I_{TSI}}{6} \quad (43)$$

$$I_{RSO} = \frac{I_{RSI}}{6} \quad (44)$$

$$I_{TSO} = \frac{|V_{Tip} - V_{CC}| - 2.0\ V}{6\ (R_T + 600\ \Omega)} \text{ for } V_{Tip} < V_{CC} \quad (45)$$

$$I_{RSO} = \frac{|V_{Ring} - V_{QB}| - 2.0\ V}{6(R_R + 600\ \Omega)} \text{ for } V_{Ring} > V_{QB} \quad (46)$$

Digital interfacing to the MC3419-1 $\overline{PDI}$ pin and the HSO pin is shown in Figures 14a, 14b and 14c. If the $\overline{PDI}$ pin is not used it should be terminated to V_{CC} and if HSO is not used, it can be left open.

Figure 15 is an application circuit showing solid state ringing insertion using an MOC3030 zero-crossing detector optocoupled triac to replace the conventional electromechanical relay. This device inserts the ringing signal on a zero voltage crossing which eliminates noise in adjacent cable pairs and removes the signal on a zero current crossing which eliminates inductive voltage spikes that commonly destroy relay contacts. The ringing generator provides a continuous 40 V to 120 V RMS signal from 15 to 66 Hz superimposed upon −48 Vdc. Ringing cadencing is inserted with the Ring Enable Input. The 2N6558 and MPSA42 replace the MJE270 for systems that use ringing generator voltages greater than 70 V_{RMS}. The MDA220 diode bridge is replaced with a series 1N4007 on the Tip lead and a shunting 1N4004 to V_{EE} and to allow ringing voltage

FIGURE 14 — INTERFACE-TO-DIGITAL LOGIC

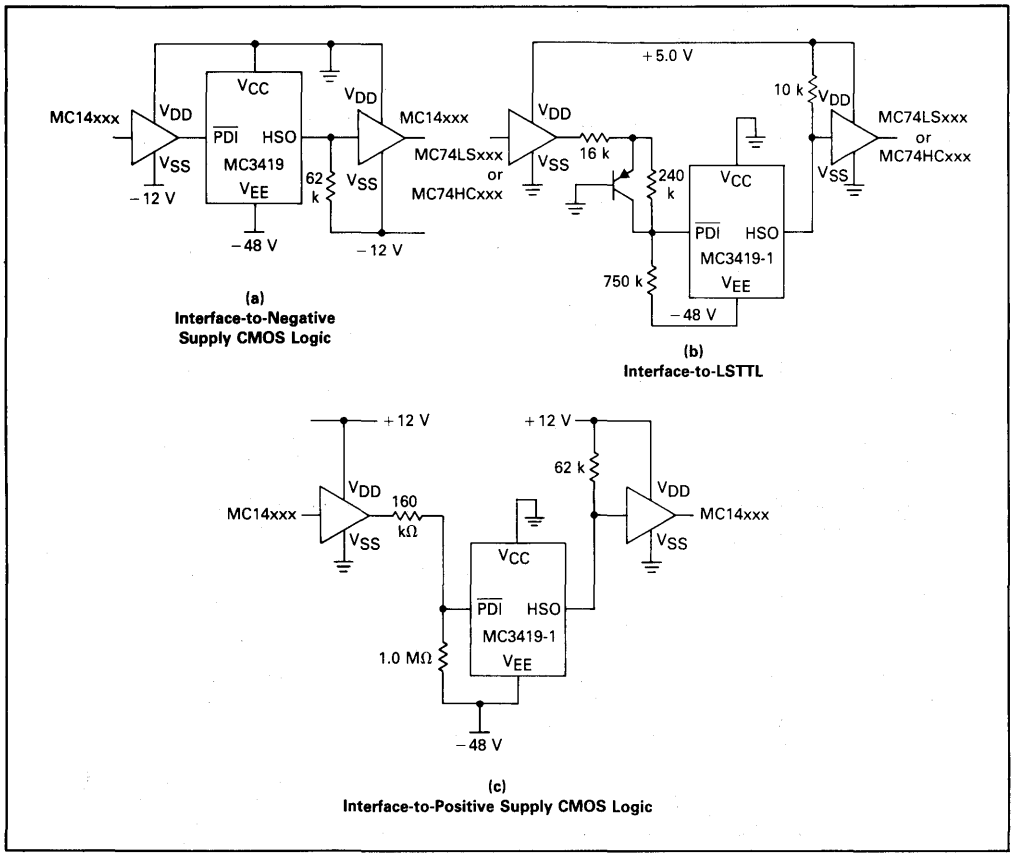
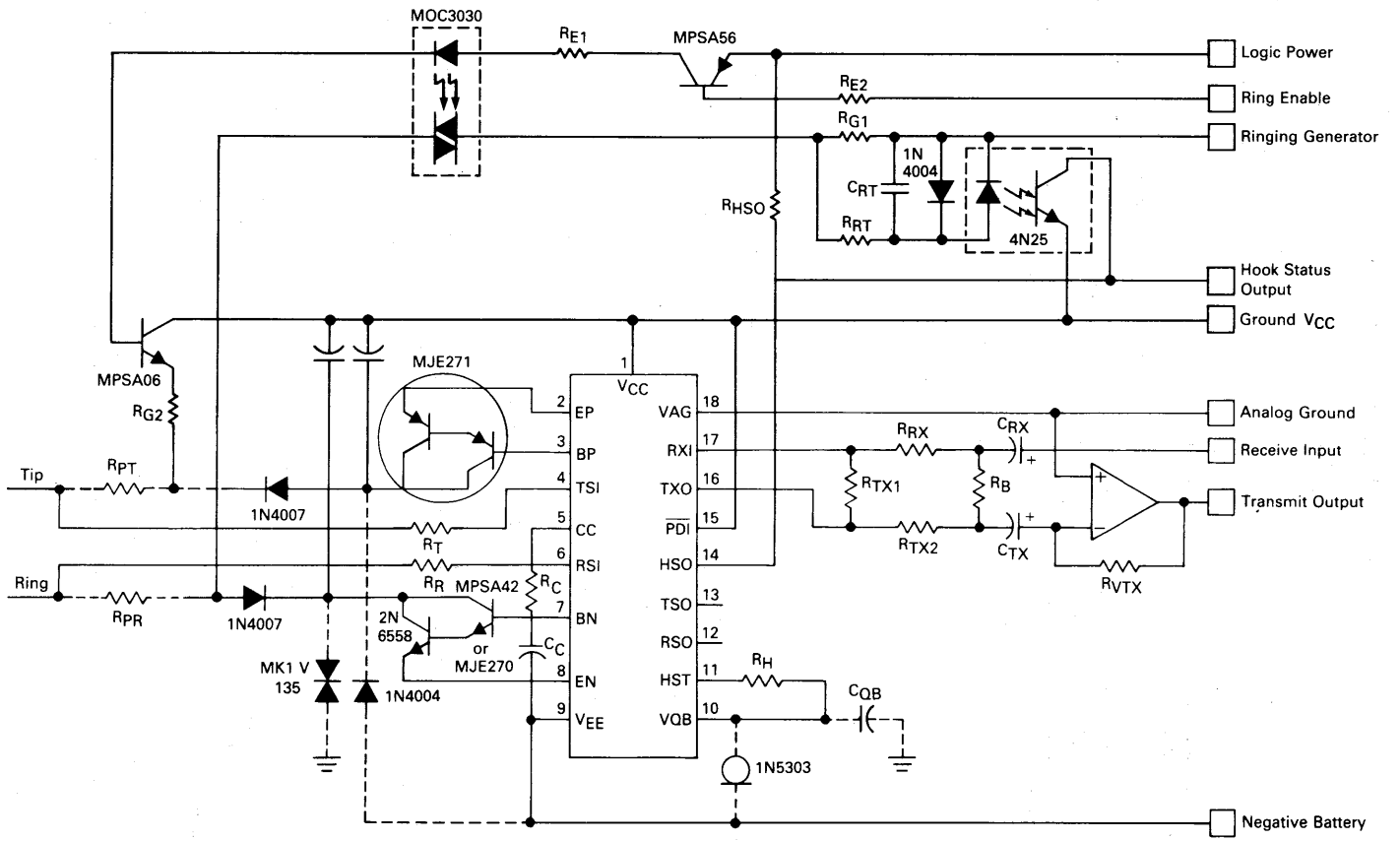


FIGURE 15 — PBX LINE CIRCUIT



– – – – Indicates Optional Components

SYSTEM EQUATIONS (continued)

on the Ring lead to exceed the power supply voltages, a 1N4007 and an MK1V-135 (Sidac) are used for protection. The forward voltage drop across the 1N4007, during normal operation, will not affect the parametric characteristics of the MC3419-1 since it is "inside" a feedback circuit. If the MJE270 is used, the MK1V-135 should be replaced with a lower voltage Sidac or MO•sorb transient suppressor.

An optocoupled transistor circuit is used for ring trip detection on long lines. It samples only the ac and dc ringing signal current and uses a simple one pole filter to eliminate the low level ac signal. Under worst case conditions this circuit will ring trip in 1½ to 4 cycles. In systems serving only short loops (<700 Ω), if R_{G1} and R_{G2} are 620 Ω or greater, the optotransistor circuit is not needed, the Hook Status Output will perform ring trip on a Zero Crossing. The Ring Enable input and the Hook Status Output interface with standard CMOS and TTL logic.

The op amp in this circuit is an integral part of the following codecs, filters or combos:

MC3417/8 — MC145414
MC14404/6/7 — MC14413/4
MC14401/2/3/5

2

LONG LINES OFF-PREMISE LINES

Specifications

R_F	— 200 Ω	R_O	— 600 Ω	Off-Hook	— <2500 Ω
I_L(max)	— 60 mA	R_X Gain	— 0 dB 200–3400 Hz	On-Hook	— >10 kΩ
R_L(max)	— 1900 Ω	T_X Gain	— 0 dB 200–3400 Hz	Protection	— 1000 V
				Ringer Equivalent	— 5

V_{Logic}	—	+5.0 V
V_{EE}	—	−42 to −56 Volts
$V_{Ringing}$	—	(40 V to 120 V_{RMS}) + V_{EE}

Parts List

MPSA56	R_R	—	9.09 k	1%	Matched
2N3905	R_T	—	9.09 k	1%	if desired
2N6558	R_{PT}	—	47 Ω	5%	
MPSA42	R_{PR}	—	75 Ω	5%	
MJE271	R_{G1}	—	620 Ω	5%	
1N4007	R_{G2}	—	100 Ω	5%	
MK1V135	R_{E1}	—	91 Ω	5%	
1N4007	R_{E2}	—	3.0 k	5%	
1N4007	R_{RT}	—	20 k	5%	
1N5303	R_C	—	24 k	5%	
1N4004	R_H	—	127 k	1–3%	
MC3419-1	R_{HSO}	—	10 k	5%	

MOC3030	R_{TX1}	—	12.1 k	1%	
4N25	R_{TS2}	—	5.76 k	1%	
	R_{RX}	—	28.7 k	1%	
	R_B	—	28.0 k	1%	
	R_{VTX}	—	28.6 k	1%	
	C_T		0.004 μF		
	C_R	—	0.004 μF		
	C_C	—	0.001 μF		
	C_{RX}	—	1.0 μF/20 V		
	C_{TX}	—	2.0 μF/40 V		
	C_{RT}	—	20 μF/5.0 V		
	C_{QB}	—	10 μF/60 V		

SHORT LINES ON-PREMISE LINES

Specifications

R_F	—	500 Ω	
R_L(max)	—	700 Ω	
Ring Trip	—	<50 ms	
Ringer Equivalent	—	2.5	
R_O	—	600 Ω	
R_X Gain	—	−5.0 dB	
T_X Gain	—	0 dB	
V_{Logic}	—	+5.0 Volts	
V_{EE}	—	−20 to −56 Volts	
$V_{Ringing}$	—	(40 V to 70 V_{RMS}) + V_{EE}	

Parts List

MJE271	R_R	—	19.6 k	1%	
MJE270	R_T	—	19.6 k	1%	
MPSA56	R_{G1}	—	620 Ω	5%	
2N3905	R_{G2}	—	620 Ω	5%	
1N4007	R_{E1}	—	91 Ω	5%	
1N4007	R_{E2}	—	3.0 k	5%	
MC3419C-1	R_H	—	330 k	5%	

MOC3030				R_{HSO}	— 10 k 5%
				R_{TX1}	— 19.6 k 1%
C_T	—	0.004 μF		R_{TX2}	— 42.2 k 1%
C_R	—	0.004 μF		R_{RX}	— 69.8 k 1%
C_C	—	0.004 μF		R_B	— 301 k 1%
C_{RX}	—	0.1 μF		R_{VTX}	— 127 k 1%
C_{TX}	—	0.5 μF		R_C	— 56 k 5%

MOTOROLA

MC34F19
MC34F19A

Advance Information

2

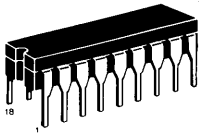
TELEPHONE LINE FEED AND 2- TO 4-WIRE CONVERSION CIRCUIT

. . . designed to replace the hybrid transformer circuit in Central Office, PABX and Subscriber carrier equipment, providing signal separation for two-wire differential to four-wire single-ended conversions and suppression of longitudinal signals at the two-wire input. It provides dc line current for powering the telset, operating from up to a 56 V supply.

- All Key Parameters Externally Programmable
- Current Sensing Outputs Monitor Status of Both Tip and Ring Leads
- On-Hook Power Below 5.0 mW
- Digital Hook Status Output
- Power Down Input
- Ground Fault Protection
- Size and Weight Reduction Over Conventional Approaches
- The sale of this product is licensed under patent No. 4,004,109. All royalties related to this patent are included in the unit price.

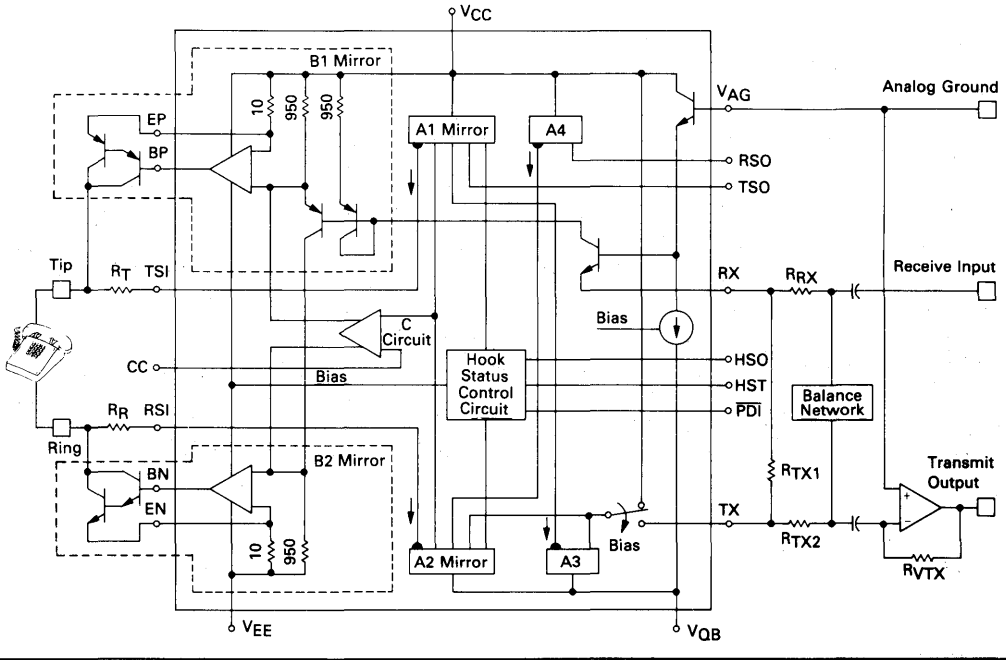
SUBSCRIBER LOOP INTERFACE CIRCUIT (SLIC)

BIPOLAR THIN-FILM INTEGRATED CIRCUIT



L SUFFIX
CERAMIC PACKAGE
CASE 726-01

FUNCTIONAL BLOCK DIAGRAM



This document contains information on a new product. Specifications and information herein are subject to change without notice.

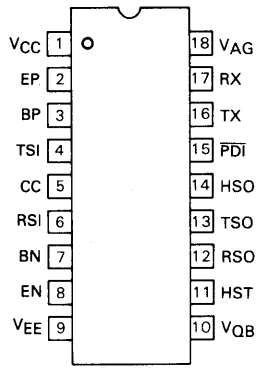
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Voltage (Referenced to V_{CC})	V_{EE} V_{QB}	−60 V_{EE} − 1	Vdc
Sense Current Steady State Pulse — Figure 4	I_{TSI}, I_{RSI}	 100 200	mAdc
Storage Temperature Range	T_{stg}	−65 to +150	°C
Operating Junction Temperature (θ_{JA} = 100°C/W Typ)	T_J	150	°C

OPERATING CONDITIONS

Rating	Symbol	Value	Unit
Operating Ambient Temperature Range	T_A	0 to +70	°C
Loop Current	I_L	20 to 120	mA
Voltage	V_{EE} V_{QB}	−20 to −56 −20 to V_{EE}	Vdc
Analog Ground (I_L = 0 to 60 mA (I_L = 0 to 120 mA)	V_{AG}	 0 to −12 −2.5 to −12	Vdc
Supervisory Output Voltage	V_{RSO}, V_{TSO}, V_{HSO}	−2.0 to −20	Vdc

PIN CONNECTIONS



PIN DESCRIPTIONS

Name	Function
V_{CC}	The most positive supply voltage. This point is Earth Ground in most typical applications.
BP & BN	Are the base drive outputs for the PNP and NPN Darlington transistors.
EP & EN	Are loop current sensing inputs and are connected to the emitter of the PNP & NPN Darlington transistors.
TSI & RSI	Are the tip and ring current sensing inputs. They are low impedance inputs (approximately 600 Ω each) that translate the voltage on tip and ring to a current through Resistors R_T and R_R.
CC	Compensation capacitor input.
V_{EE}	Is the most negative supply voltage.
V_{QB}	Is the quiet battery connection. The voltage on this pin must not go more negative than V_{EE}.
HST	Hook Status Threshold programming resistor input pin. This pin programs the value of loop resistance which determines on-hook or off-hook status.
RSO	Ring Sense current Output. This output reflects the status of the Ring terminal. The current is sourced from this output and is one-sixth I_{RSI}.
TSO	Tip Sense current Output. This output reflects the status of the Tip terminal. The current is sourced from this output and is one-sixth I_{TSI}.
HSO	Hook Status Output. This is a digital output (open collector PNP) that sources current when the loop resistance is less than the threshold resistance value set by R_H.
$\overline{PDI}$	Power-Down Input pin. A logic level "0" powers down the MC34F19.
TX	Transmit current output. This output sinks current proportional to (I_{TSI} + I_{RSI})/2.
RX	Receive input. This input sums the currents from the TX output and signal input. This pin has a low input impedance.
V_{AG}	Analog ground reference supply voltage input.

ELECTRICAL CHARACTERISTICS (V_{EE} = −48 V, V_{QB} = −48 V, V_{AG} = −6.0 V, R_L = 900 Ω, T_A = 25°C unless otherwise noted.)

Characteristic	Figure	Symbol	Min	Typ	Max	Unit
Transhybrid Gain Variation (1.0 kHz @ 0 dBm Input) Transmission/Reception	1	V_{TX}/V_L, V_L/V_{RX}	−0.3	0	+0.3	dB
Transhybrid Rejection (1.0 kHz @ 0 dBm Input) Fixed (1%) Resistor Balance Network Trimmed Balance Network	1	V_{TX}/V_{RX}	 −23 —	 — −55	 — —	dB
Level Linearity (−48 to +3.0 dBm, referenced to output @ 1.0 kHz @ 0 dBm) Transmission Reception	1	 V_{TX}/V_L V_L/V_{RX}	 −0.1 −0.1	 0 0	 +0.1 +0.1	dB
Frequency Response (200–3400 Hz, referenced to output @ 1.0 kHz @ 0 dBm) Transmission Reception	1	 V_{TX}/V_L V_L/V_{RX}	 −0.1 −0.1	 0 0	 +0.1 +0.1	dB
Total Distortion C-Message Filtered	1	V_L/V_{RX} V_{TX}/V_L	— —	−60 −60	— —	dB
Idle Channel Noise	1	V_{TX}	—	—	10	dBrnc0
Termination Resistance Tolerance @ 1.0 kHz	1	ΔP_o	—	—	±5.0	%
Longitudinal Induction — 60 Hz (I_L = 30 to 100 mA, I_{LON} = 35 mA RMS)	2	V_{TX}	—	5.0	—	dBrnc0
Longitudinal Balance MC34F19 (200–3000 Hz) MC34F19A (200–1000 Hz) MC34F19A (3000 Hz)	2	V_{TX}/V_{LON}	 −45 −50 −48	 — — —	 — — —	dB
Propagation Delay	1	T_P, V_{RX} to V_L V_{RX} to I_{TX}	— —	750 1.2	— —	ns μs
Power Dissipation (R_L > 100 MΩ)		P_D	—	1.0	—	mW
Supply Current — On-Hook (V_{EE} = V_{QB} = −56 V, R_L > 100 MΩ)		I_{CC}	—	40	200	μA
Power Supply Noise Rejection (1.0 kHz @ 1.0 V RMS)	3	V_{TX}/v_{ee}	−40	—	—	dB
Quiet Battery Noise Rejection (1.0 kHz @ 1.0 V RMS)	3	V_{TX}/v_{qb}	—	−6.0	—	dB
Sense Current Tip Ring	4	 I_{TSO}/I_{TSI} I_{RSO}/I_{RSI}	 0.15 0.15	 0.17 0.17	 0.19 0.19	mA/mA
Fault Currents — On-Hook Tip to V_{CC} Ring to V_{CC} Tip to Ring Tip & Ring to V_{CC}	1	 I_{Tip} I_{Ring} I_{Loop} I_{Tip} & I_{Ring}	 — — — —	 0 2.5 120 2.5	 — — — —	mA
Analog Ground Current		I_{AG}	—	1.0	10	μA
Power Down Logic Levels		$I_{\overline{PDI}}$ V_{IH} V_{IL}	— −1.2 −20	−1.0 0 —	— — −4.0	μA Vdc Vdc
Hook Status Output Current (R_L < 2.5 kΩ, $\overline{PDI}$ = Logic 1) (R_L > 10 kΩ, or $\overline{PDI}$ = Logic 0)	1	I_{HSO}	 200 —	 400 0	 — 2.0	μA

FUNCTIONAL DESCRIPTION

Referring to the functional block diagram, line-sensing resistors at TSI and RSI convert voltages at the Tip and Ring terminals into currents which are fed into current mirrors* A1 and A2. The output of A1 is mirrored by A3 and summed together with an output of A2 at the TX terminal. Thus, a differential to single-ended conversion is performed from the ac line signals to the TX output.

All the dc current at the TX output is fed back through the RX terminal to the B1 mirror input. The inputs to B1 and B2 are made equal by mirroring the B1 input current to the B2 input through a low gain output (x1) of the B1 mirror. Both B1 and B2 mirrors have high gain outputs (x95) which drive the subscriber lines with balanced currents that are equal in amplitude and 180° out of phase. The feedback from the TX output, through the B-Circuit mirrors, to the subscriber line produces a dc feed resistance significantly less than the loop sensing resistors.

In most line-interface systems, the ac termination impedance is desired to be greater than the dc feed impedance. A differential ac generator on the subscriber loop would be terminated by the dc feed impedance if the total ac current at the TX output were returned to the B1 input along with the dc current. Instead, the MC34F19 system diverts part of the ac current from the B-Circuit mirrors. This decreases the ac feedback current, causing the ac termination impedance at the line interface to be greater than the dc feed impedance.

The ac current that is diverted from the B1 mirror input is coupled to a current-to-voltage converter circuit that has a low input impedance. This circuit consists of an op amp and a feedback resistor external to the MC34F19 which produce the transmit output at the 4-wire interface. The transhybrid transmission gain is programmed by the op amp feedback resistor.

Transhybrid reception is realized by converting the ac coupled receive input voltage to a current through an external resistor at the low impedance RX terminal. This current is summed at RX with the dc and ac feedback current from the A-Circuit mirror and drives the B1 mirror input. The B-Circuit mirror outputs drive the line with balanced ac current proportional to the receive input voltage. The transhybrid reception gain is programmed by the resistor at the RX input.

Since receive input signals are transmitted through the MC34F19 to the 2-wire port, and the 2-wire port signals are returned to the 4-wire transmit output, a means of cancellation must be provided to maintain 4-wire signal separation (transhybrid rejection). Cancellation is complicated because the gain from the receive port to the transmit port depends on the impedance of the subscriber loop. A passive "balance network" is used to achieve transhybrid rejection by cancelling, at the low impedance input to the transmit op amp, the current reflected by the loop impedance to the 4-wire transmit output. For a resistive loop impedance, a single resistor provides the cancellation. For reactive loops, the balance network should be reactive.

Longitudinal (common-mode) currents that may be present on the subscriber lines are suppressed in the MC34F19 by two methods. The first mode of suppression is inherent in the mirror configuration. Positive-going longitudinal currents into Tip and Ring create common-mode voltages that cause a decreasing current through the Tip Sensing resistor and an increasing current through the Ring Sensing resistor. When these equal and opposite signal currents are reflected through the A-Circuit and summed together at TX, the total current at TX remains unchanged. Therefore, the ac currents due to the common-mode signals are cancelled before reaching the transmit output.

The second longitudinal suppression method is dominant, since it limits the amplitude of common-mode voltages that appear at the Tip and Ring terminals. Through an error-detecting circuit, the input of which is a difference current between outputs of A1 and A2, the impedance at Tip and Ring to longitudinal currents is kept very low. This is accomplished with a high gain C-Circuit which produces B1 and B2 output currents that are equal and in phase to cancel the longitudinal line currents. Operation of this circuit does not affect the dc line-current or the processing of normal differential line signals.

The hook-status control circuit supplies the bias currents to activate the B-Circuit op amps and other sections of the MC34F19. If the $\overline{PDI}$ pin is a logic "one," the control circuit senses two outputs from the A1 and A2 mirrors. If both of these output currents are greater than the preprogrammed current at the HST terminal, the control circuit supplies currents to power up the SLIC. At the same time it activates a digital status output, HSO.

In addition to the digital hook status output, the condition of Tip and Ring can be monitored at the TSO and RSO outputs of the MC34F19. These outputs source currents proportional to the TSI and RSI input currents respectively, and operate independently of the $\overline{PDI}$ logic input.

The MC34F19 has two negative battery terminals. V_{EE} supplies the high current through the B2 mirror to drive the line. B2 has a high output impedance and battery noise will not be coupled to the line from the V_{EE} terminal. However, V_{QB} is quite sensitive to noise, since the line-sensing resistor is referenced to this pin through the A2 mirror, and should be bypassed with a filter network to guarantee a high rejection of battery noise.

The V_{AG} input also plays a key role in reducing power-supply related noise that can occur when the MC34F19 system is coupled to a switching system. The analog ground isolates the 4-wire receive and transmit signal paths from noise on the system power ground by establishing a common ac signal reference.

*A current mirror is a circuit which behaves as a current controlled, current source. It has a single low-impedance input terminal and one or more high impedance outputs.

2

FIGURE 1 — AC TEST CIRCUIT

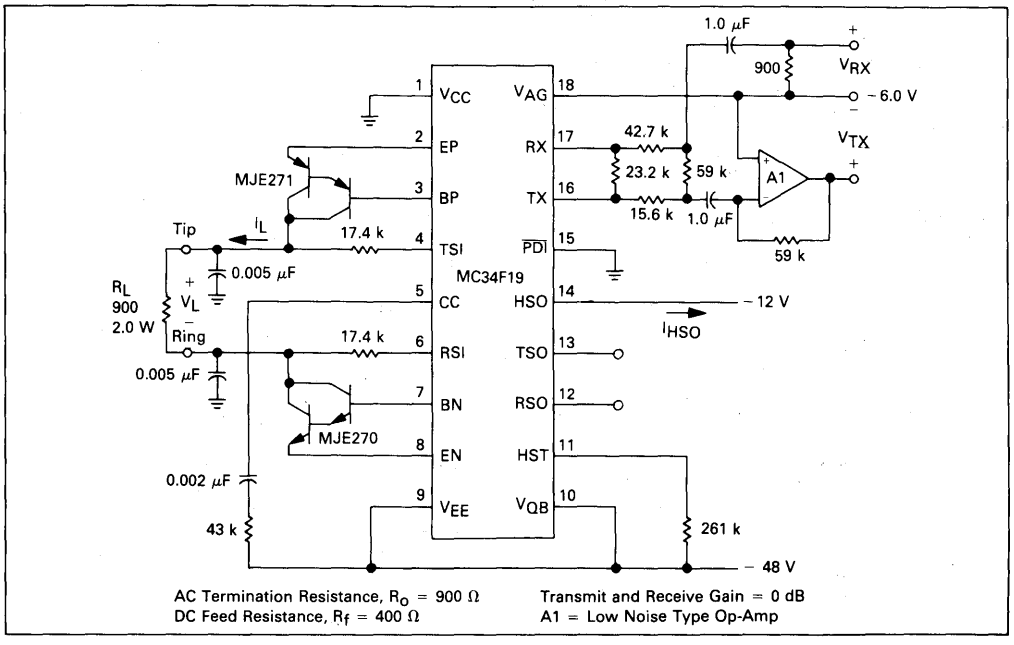


FIGURE 2 — LONGITUDINAL BALANCE TEST CIRCUIT

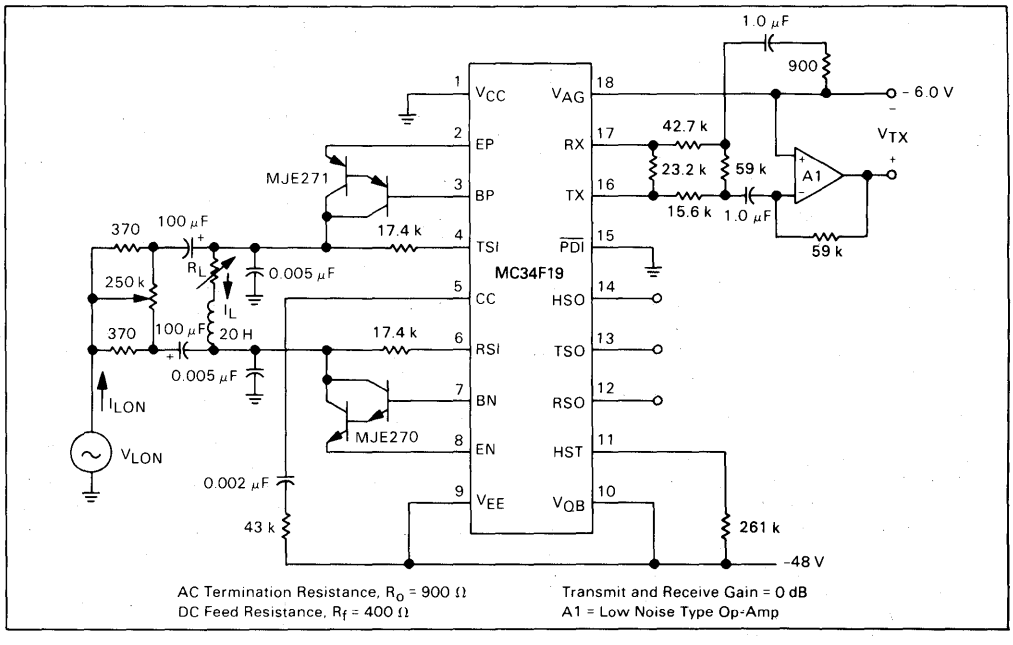


FIGURE 3 — SUPPLY NOISE REJECTION TEST CIRCUIT

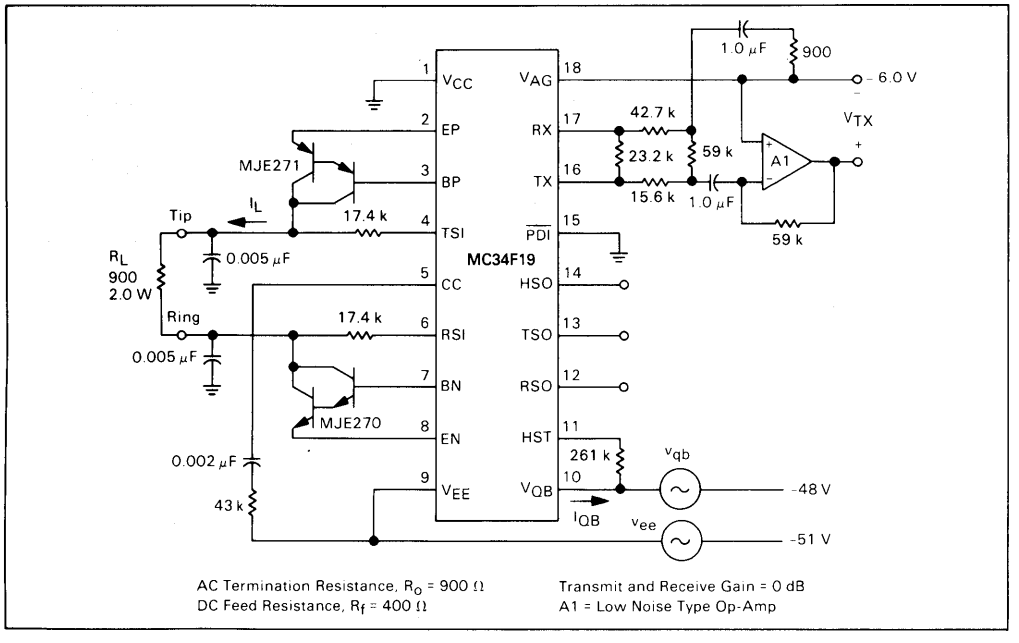


FIGURE 4 — TSO AND RSO SUPERVISORY OUTPUT TEST CIRCUIT

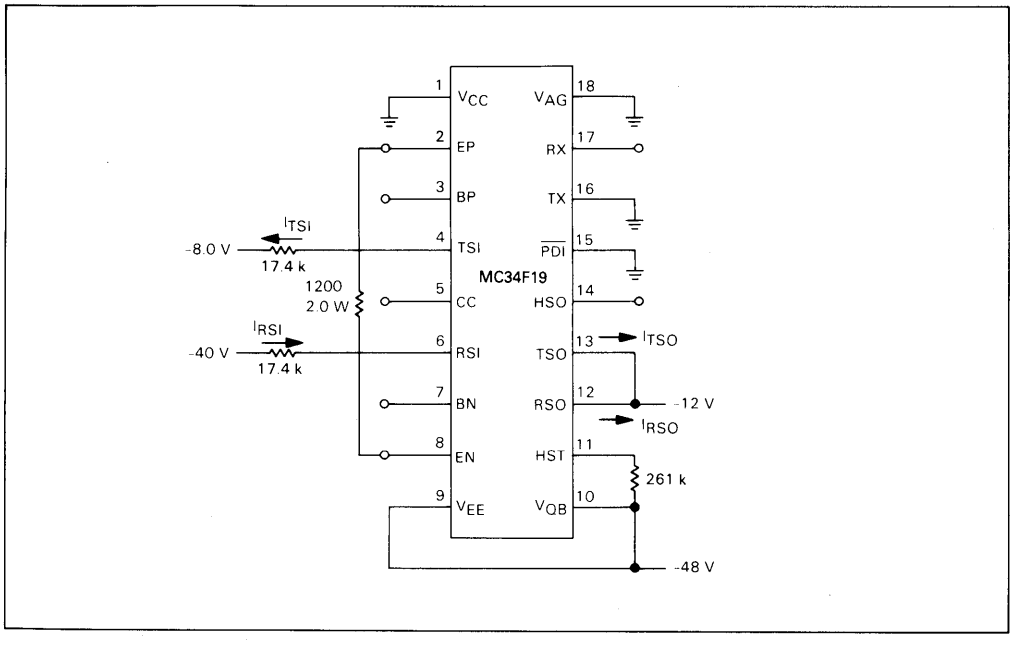


FIGURE 5 — QUIET BATTERY versus LOOP CURRENT

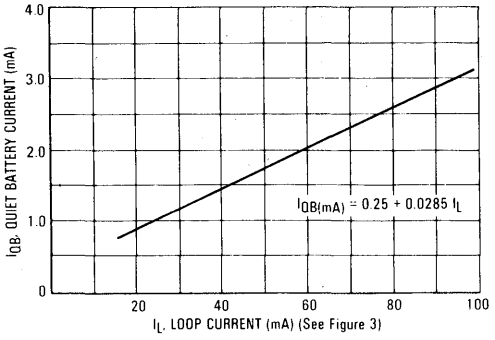
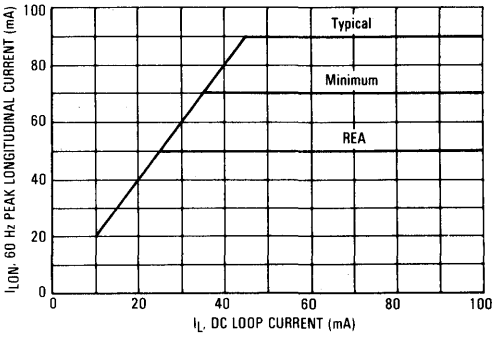


FIGURE 6 — LONGITUDINAL CAPACITY



APPLICATIONS INFORMATION

The Motorola Subscriber Loop Interface Circuit (SLIC) is comprised of a bipolar laser-trimmed integrated circuit, MC34F19, two complimentary Darlington power transistors, MJE270 and 271, a bridge rectifier, MDA220, ten resistors, and five capacitors, as shown in Figure 7. The op amp providing the V_{TX} output may be a separate component or may be one of the two op amps included in the MC14413 or MC14414 PCM filter packages. The circuit of Figure 7 will provide:

- Adjustable resistive dc power feed
- Adjustable maximum loop range
- Adjustable ac termination impedance
- 2-wire balanced to 4-wire single ended conversion
- Adjustable transmit and receive gains
- Independent transhybrid null
- Ring-to-ground, Tip-to-ground, and Ring- and Tip-to-ground fault current limiting (2.5 mA)
- Rejection of longitudinal or common mode interference from dc to greater than 4.0 kHz
- 1500 volt secondary lightning transient protection
- Temporary power-line fault protection
- On-hook power-down (less than 10 mW)
- Floating 4-wire common input for noise rejection
- Hook-status output signal
- Power-down control for subscriber service denial
- Continuous Tip and Ring status monitoring outputs
- Wide battery range (20 V to 56 V)

In addition, the SLIC can provide the following optional features:

- Constant current battery feed
- Current limiting battery feed
- Battery noise suppression
- Adjustable frequency response

DC Characteristics

When the telephone is on-hook, the Tip and Ring terminals of the SLIC are essentially open and the MC34F19 is in a quiescent state. In this condition, current is being supplied to the line only through R_R and R_T and power dissipation in the MC34F19 is limited primarily to leakage currents.

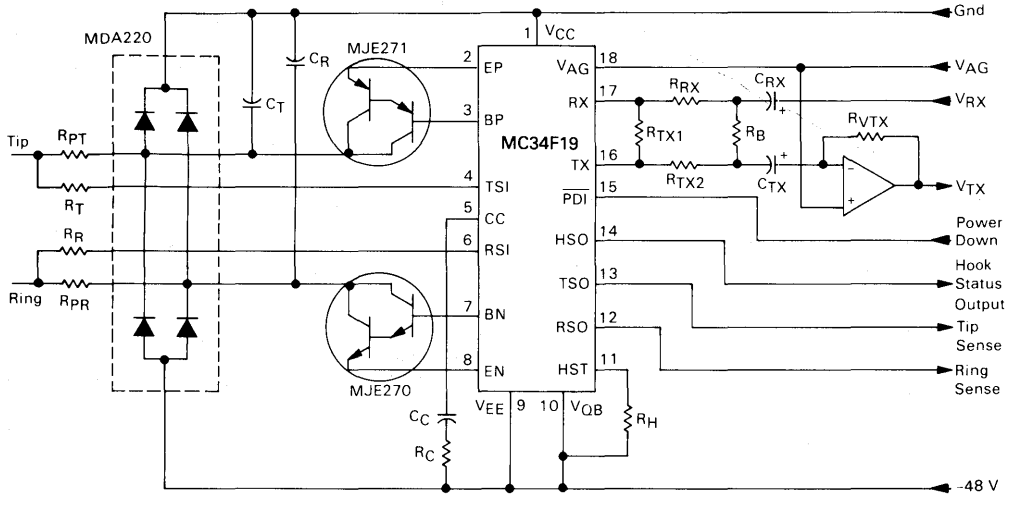
In the off-hook state, the MC34F19 powers itself up and provides current to the line. The off-hook dc feed resistance with which the SLIC drives the line is given by

$$R_F = \frac{(R_R + R_T + 1200)|V_{QB}|}{98\,(|V_{QB}| - 4)} \qquad (1)$$

The v alues of R_R and R_T can be derived from equation (1) to provide the desired dc feed resistance once V_{QB} is known.

$$R_R = R_T = \frac{49\,(|V_{QB}| - 4)\,R_F}{|V_{QB}|} - 600 \qquad (2)$$

FIGURE 7 — SLIC CIRCUIT



The line-feed current flows between ground and V_{EE}; however, the control electronics is referenced to V_{QB} and ground. Therefore, the dc feed resistance appears to be referenced to V_{QB} and ground.

The matching of R_R and R_T is critical to a number of ac performance parameters as shown in Figures 8, 9 and 10. One percent tolerance or better is recommended for these resistors. In addition, these resistors must withstand any voltage transients on the line. Resistors able to withstand voltage transients of 1000 V or more are recommended.

2

FIGURE 8 — RETURN LOSS versus TIP/RING RESISTOR MISMATCH

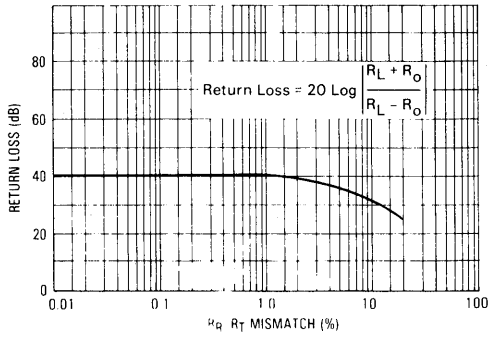


FIGURE 9 — TRANSHYBRID REJECTION versus TIP/RING RESISTOR MISMATCH

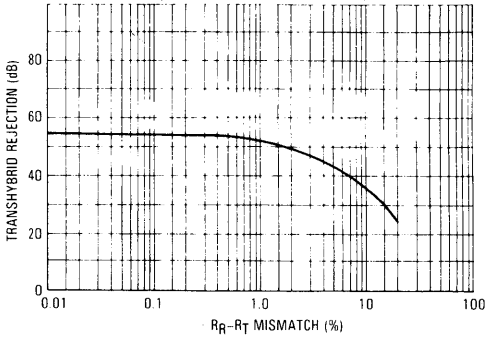


FIGURE 10 — IMPEDANCE BALANCE versus TIP/RING RESISTOR MISMATCH

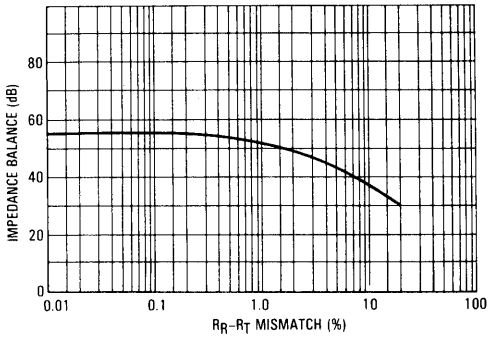
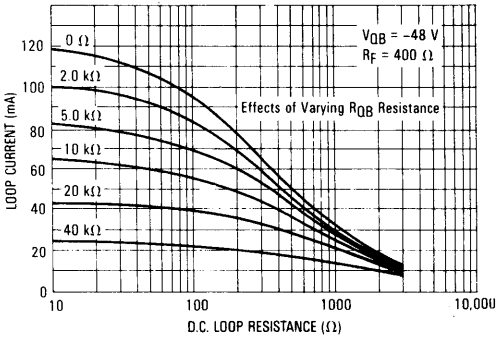


FIGURE 11 — LOOP CURRENT versus LOOP RESISTANCE



Power dissipation on short loops can be significantly reduced by either of two methods of current limiting. The dc feed resistance R_F is shown in equation (1) to be a function of V_{QB} as well as R_T and R_R. The current I_{QB} from the V_{QB} pin is proportional to loop current. Therefore, a resistor R_{QB} placed between the V_{QB} pin and V_{EE} supply will reduce the V_{QB} supply voltage as the loop current increases. This slightly increases the value of R_F while at the same time reducing the effective value of the battery voltage, thereby limiting loop current. Figure 11 can be used to determine the value of R_{QB} that will yield the desired maximum loop current.

Figure 20 shows how a current regulator device can be used in place of R_{QB} to provide a constant current line-feed characteristic up to the loop resistance where the constant current equals the resistive feed current. At that point, the line-feed will appear resistive. Typical current regulator values for various loop currents are shown in Figure 12. The Motorola 1N5283 series of current regulator diodes are recommended. The current sourced to the current regulator diode in the off-hook mode is:

$$I_{QB} = 0.0285\, I_L + 0.25 + \frac{|V_{QB}| - 4}{R_H} \qquad 3(a)$$

I_L in mA, R_H in kΩ

FIGURE 12 — LOOP CURRENT REGULATION

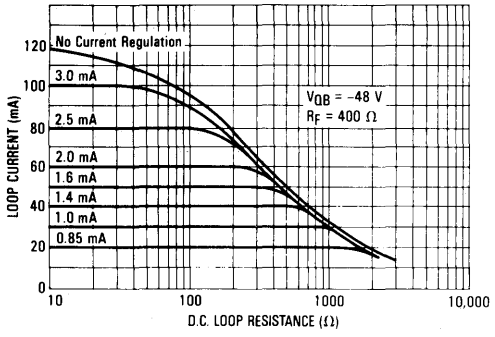


FIGURE 13 — TOTAL SLIC POWER DISSIPATION

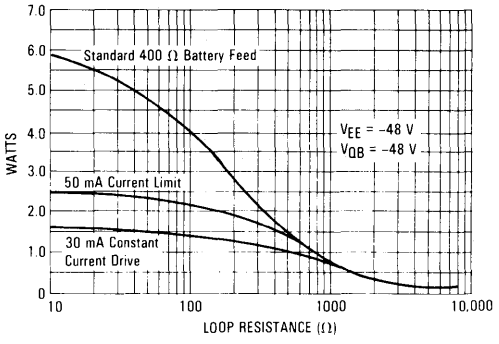


FIGURE 14 — HOOK STATUS DETECTION

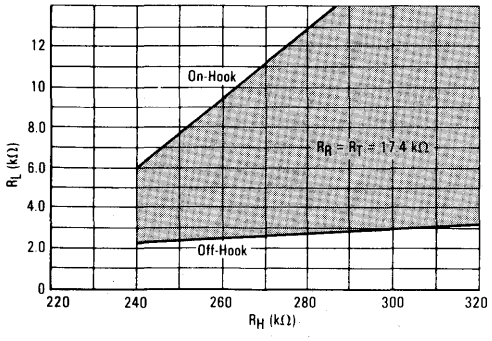
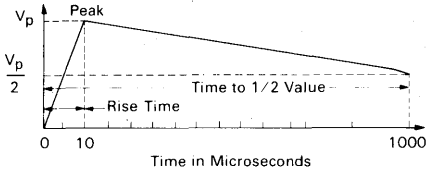


FIGURE 15 — TRANSIENT VOLTAGE WAVE SHAPE



In the on-hook mode the current is:

$$I_{QB} = 2.15\ I_{RSI} + 0.7\ I_{TSI} \qquad 3(b)$$

Figure 13 is a graph of SLIC power dissipation for both 400 Ω resistive battery feed and constant current battery feed, (or current limiting) showing the power savings of constant current techniques.

Either R_{QB} or the current regulator diode and a capacitor to V_{CC} provide an effective means of filtering any noise on the V_{EE} line and prevent it from reaching the V_{QB} pin.

The loop resistances which the SLIC recognizes as on-hook and off-hook are determined by R_H.

$$R_L \text{ (On-Hook)} \geq 0.17\ R_H - (R_R + R_T) \qquad 4(a)$$

$$R_L \text{ (Off-Hook)} \leq 0.011\ R_H - 0.010\ (R_R + R_T) \qquad 4(b)$$

The value of R_H can be selected from Figure 14. All loop resistances below the shaded area at the point where R_H was selected are recognized as off-hook. All loop resistances above the shaded area at the value of R_H are recognized as on-hook. The shaded area represented an undefined region where the hook status output may indicate either on-hook or off-hook due to element tolerances and comparator hysteresis.

Transient Protection

The SLIC shown in Figure 7 will withstand positive or negative voltage transients on Tip and Ring up to 1500 V_{peak} having the waveshape shown in Figure 15. The resistors R_{PT}, R_{PR}, R_T, and R_R must be chosen to withstand such a voltage transient without arching across or failing due to the resulting current surge. The values of R_{PT} and R_{PR} should be between 30 and 50 Ω. Tolerance of 20% is adequate. The values of R_T and R_R are determined per equation (2). The peak currents at RSI and TSI should not exceed 200 mA during these transients.

The circuit of Figure 7 will also withstand crosses to ac power lines of up to 700 V_{RMS} for 11 cycles of the 60 Hz line per REA Form 522a. The ability to withstand continuous power-line crosses is determined mainly by the power handling ability of R_{PT}, R_{PR}, R_T, and R_R. The circuit wiring to the MDA220 diode bridge must be adequate to handle the large voltages and currents caused by transients, as well.

None of the pins on the MC34F19 should be operated more positive than V_{CC} or more negative than V_{EE}. However, under transient conditions, EP and BP may

go up to one volt more positive than V_{CC} and BN, EN, and V_{QB} may go up to one volt more negative than V_{EE} without permanent damage to the MC34F19. When a capacitor is used on the V_{QB} pin in conjunction with R_{QB}, a 1N4001 or similar diode is recommended between V_{EE} and V_{QB}. The diode cathode should be connected to V_{QB}. For single short transients of less than one millisecond, EP and BP may exceed V_{CC} and EN and BN may exceed V_{EE} by up to 30 V.

Transmission Characteristics

The ac termination impedance R_O of the SLIC is determined by R_T, R_R, and the ratio of R_{TX2} to R_{TX1}.

$$R_O = \frac{R_T + R_R + 1200}{1 + 97K_5} \quad (5)$$

$$K_5 = \frac{R_{TX2}}{R_{TX2} + R_{TX1}} \quad (6)$$

The required value of K_5 is derived from equation (5) after choosing R_O.

$$K_5 = \frac{1}{97}\left[\frac{R_T + R_R + 1200}{R_O} - 1\right] \quad (7)$$

The value of R_{TX1} must be selected first to assure that the internal current mirrors in the MC34F19 do not saturate at the minimum voltage provided at V_{QB}. The value of R_{TX1} is determined by:

$$R_{TX1} = \frac{(R_R + R_T + 1200)(|V_{QB}| \text{ min} - |V_{AG}| \text{ max} - 6.5)}{|V_{QB}| \text{ min} - 5.4} \quad (8)$$

If current limiting or constant current-feed is used where the minimum value of V_{QB} may not be known, R_{TX1} is found by:

$$R_{TX1} = \frac{0.01\ L_{L(max)}(R_R + R_T + 600) - |V_{AG}|(max) - 3.9}{0.01\ I_{L(max)}} \quad (9)$$

The value of R_{TX2} may be derived from equation (6).

$$R_{TX2} = \frac{K_5 R_{TX1}}{1 - K_5} \quad (10)$$

Transhybrid reception gain (G_{RX}) from V_{RX} to Tip and Ring is given by:

$$G_{RX} = \frac{95\ R_L\ R_O}{(R_L + R_O)\ R_{RX}} \quad (11)$$

The value of R_{RX} may be calculated to provide the desired G_{RX} for a given R_O and R_L.

$$R_{RX} = \frac{95\ R_L\ R_O}{(R_L + R_O)\ G_{RX}} \quad (12)$$

Transhybrid transmission gain (G_{TX}) from Tip and Ring to V_{TX} is given by:

$$G_{TX} = \frac{1.02\ R_{VTX}\ (1 - K_5)}{R_R + R_T + 1200} \quad (13)$$

The value of R_{VTX} may be calculated to provide the desired G_{TX}.

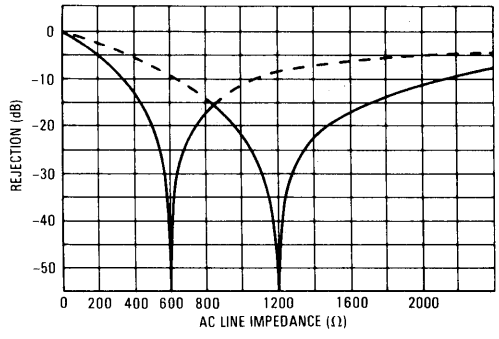
$$R_{VTX} = \frac{(R_R + R_T + 1200)\ G_{TX}}{1.02\ (1 - K_5)} \quad (14)$$

Transhybrid rejection is achieved with the SLIC by taking advantage of the 180° phase reversal of the current at the TX pin with respect to the V_{RX} input. A balance resistor, R_B, is placed between the V_{RX} input and the virtual ground point between C_{TX} and R_{TX2}. The value of this resistor is selected to exactly cancel out the return current from the TX pin and is determined by:

$$R_B = \frac{R_{RX}(1 + 97K_5)(R_O + R_L)}{97(1 - K_5)(R_L)} \quad (15)$$

Maximum rejection will only occur at one value of R_L across Tip and Ring, as shown in Figure 16, for a given value of R_B. Figure 16 shows that more than one value of R_B may be required to provide adequate rejection over wide ranges of loop resistance.

FIGURE 16 — TRANSHYBRID REJECTION



Maximum rejection on a line that is reactive can be obtained with the circuit shown in Figure 17. This will balance any capacitive load on the line, where

$$R_{B1} = \frac{R_{RX}(R_R + R_T + 1200)}{97\ R_L\ (1 - K_5)} \quad (16)$$

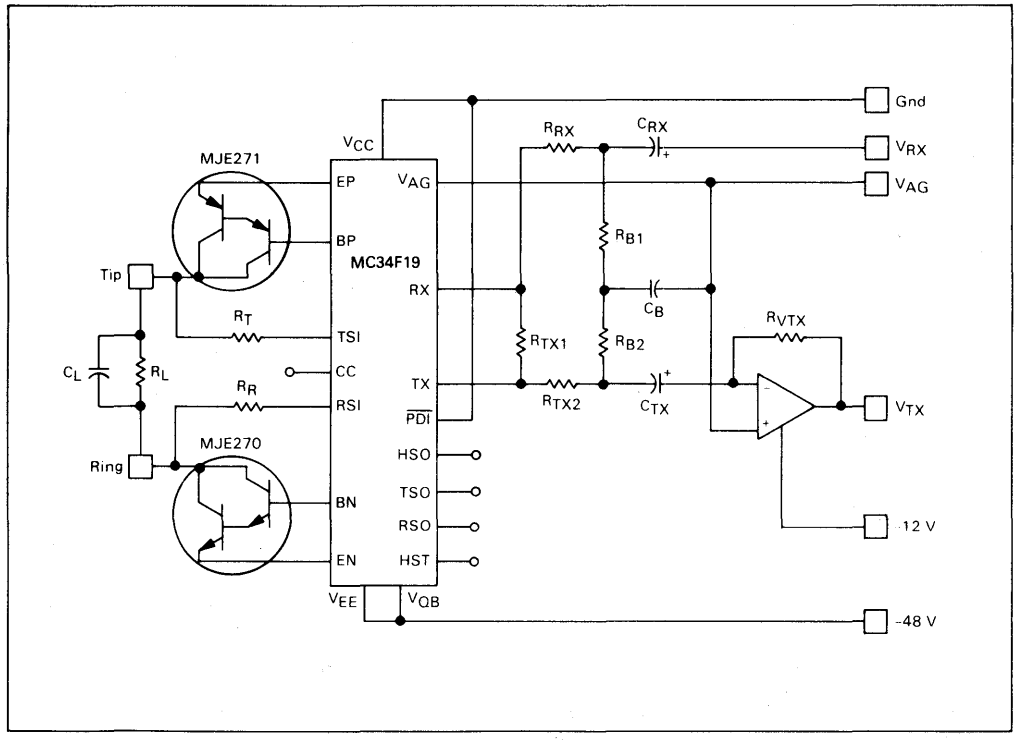
$$R_{B2} = \frac{R_{RX}(R_R + R_T + 1200)}{97\ R_O\ (1 - K_5)} \quad (17)$$

$$C_B = \frac{R_L\ C_L}{R_{B2}} \quad (18)$$

Signaling and Supervision

The $\overline{PDI}$ function shuts off all power to the subscriber with the exception of the small current provided by R_R and R_T. The power-down state occurs when a logic low-level, any voltage more negative than $V_{CC} - 4.0$ V but not exceeding -20 V, is applied to the $\overline{PDI}$ pin.

FIGURE 17 — BALANCE NETWORK FOR REACTIVE LINES



The $\overline{PDI}$ pin is designed to be TTL compatible if the logic power supplies are 0 V and −5.0 V. It is also compatible with CMOS powered from 0 V and −12 V supplies, otherwise a level-shifter is required. If the power-down feature is not desired, this pin can be tied to V_{CC}.

Hook status is indicated by the presence or absence of current at the Hook Status Output (HSO). On-hook status is indicated by no current output at HSO. When an off-hook condition is detected by the MC34F19, the HSO pin sources a dc current of at least 200 μA. A resistor can be used to translate the current into a voltage for further processing by the digital logic. This pin also passes dial pulse information. If the $\overline{PDI}$ pin is at a logic low level, HSO is inactive.

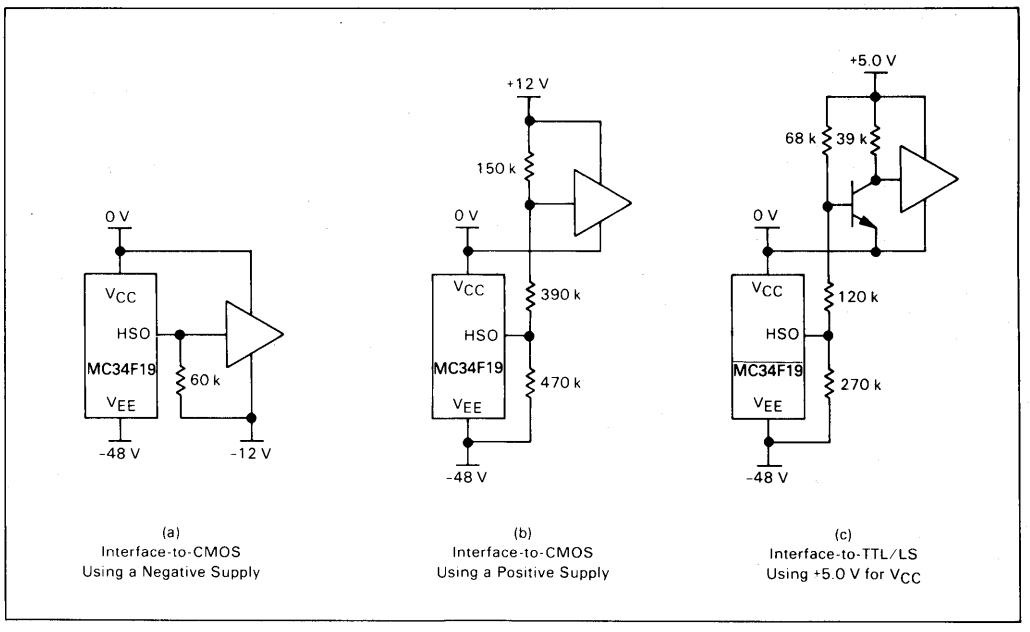
Figures 18 (a), 18 (b), and 18 (c) show suggestions for interfacing with various digital logic levels.

The Tip Sense Output (TSO) and the Ring Sense Output (RSO) both source current that is proportional to the current that flows into and out of their respective inputs — the Tip Sense Input (TSI) and Ring Sense Input (RSI). The output currents are 1/6 that of the input currents. These outputs may be used as full time monitors of the line condition since they remain active even if the MC34F19 is in the power-down state. Figure 19 shows how these outputs can be used for the ring-trip function and ring-fault indicator.

Ringing is the last function to describe on Figure 19. There are several ways of inserting the ringing signals on a line, any one of which the SLIC can be adapted to. Figure 19 shows one method.

When the ringing relay is enabled, the ring side of the SLIC is disconnected. The tip side of the line is connected to a grounded resistor (R_{G1}) to provide a complete signal path for the ring generator signal. While the phone is on-hook, the ringing signal is capacitively coupled to the tip line through the high impedance of the bell ringer and a capacitor in the phone. The dc currents are low and therefore the dc voltage drop

FIGURE 18 — INTERFACE-TO-DIGITAL LOGIC



(a) Interface-to-CMOS Using a Negative Supply

(b) Interface-to-CMOS Using a Positive Supply

(c) Interface-to-TTL/LS Using +5.0 V for V_{CC}

across R_{G1} is low. When the subscriber goes off-hook, the impedance of the phone drops to a few hundred Ω of dc resistance and R_{G1} gets a large dc current along with a large ac current. The sensing resistor (R_T) will sense this change and the TSO output of the MC34F19 will also reflect this change by an increased voltage drop on the R_{TS} resistor. The capacitor (C_{TS}) will filter the ac component of the signal. A comparator can now be used to determine the hook status and disable the ring delay.

Design Example

This example will illustrate the design procedure for a SLIC to meet the following specifications:

V_{EE} = −48 V ± 6.0 V
V_{AG} = −6.0 V ± 1.0 V
400 Ω resistive dc feed
Current limiting at 60 mA
Maximum loop resistance of 2500 Ω
900 Ω ac termination resistance
Transmit gain of 0 dB
Receive gain of 0 dB
Balanced for 600 Ω line resistance

The V_{QG} supply will be derived from the −48 V V_{EE} supply through a 1N5305 current regulator diode to provide loop current limiting at 60 mA. The voltage drop across the 1N5305 is less than 2.0 V until it reaches regulation and may be ignored in the calculation of R_T and R_R. C_{QB} is 10 μF at 60 V. From equation (2).

$$R_T = R_R = \frac{49\,(48-4)\,400}{48} - 600$$
$$= 17367\ \Omega$$

The closest standard value with ±1.0% tolerance is 17.4 kΩ. 17.4 kΩ will be used in all the rest of the equations.

The protection resistors (R_{PR} and R_{PT}) should be 30 Ω to 50 Ω. For this example we will use 40 Ω ±20%. C_T and C_R are stabilization capacitors whose values, including line capacity, should be a minimum of 2000 pF.

R_C and C_C are determined by $(R_T + 600)\,C_T = R_C C_C$. 18 kΩ ±5.0% and 2000 pF will be used for R_C and C_C.

The value of R_H is determined from Figure 14. To guarantee off-hook detection at the maximum loop resistance of 2500 Ω, R_H can be 261 kΩ ±1.0%, which is a standard value. A 270 kΩ ±5.0% resistor can be used if the on-hook resistance of the loop is specified larger than 14 kΩ.

To obtain the desired 900 Ω ac termination resistance (R_O), K_5 is first calculated using equation (7).

$$K_5 = \frac{1}{97}\left[\frac{17400 + 17400 + 1200}{900} - 1\right]$$
$$= 0.402$$

The value of R_{TX1} is calculated from equation (9) since V_{QB} is supplied from a current regulator diode.

$$R_{TX1} = \frac{(0.01)(0.06)(17400+17400+600)-7-3.9}{(0.01)(0.06)}$$
$$= 17233\ \Omega$$

17233 Ω is the largest value of R_{TX1} that can be used. A 16.9 kΩ ±1.0% resistor is the standard value selected. From equation (10), R_{TX2} is now calculated.

$$R_{TX2} = \frac{(0.402)(16900)}{(1-0.402)}$$
$$= 11361\ \Omega$$

A 11.3 kΩ ±1.0% resistor is selected. When selecting R_{TX2}, select the nearest standard value lower than the calculated value. This is because C_{TX} adds a small impedance to the value of R_{TX2} and the virtual ground node (negative input to the current to voltage converter) will also add a slight amount of impedance to R_{TX2}. The impedance of the virtual ground point is

$$Z_{in} = \frac{R_{VTX}}{1+A}$$

where A is the open loop gain of the op amp. At 1.0 kHz, Z_{in} will probably range from 50 Ω to 100 Ω. The C_{TX} capacitor, 1.0 μF (50 V) adds a reactance of 160 Ω to the value of R_{TX2} so the total impedance is:

$$\sqrt{(11300+75)^2+(160)^2} = 11376\ \Omega$$

With the nominal values selected for R_{TX1}, R_{TX2}, C_{TX} and Z_{in}, K_5 nominal value is 0.4007 and R_O nominal value is 903 Ω.

Transhybrid reception gain (G_{RX}) is set to 0 dB (voltage gain of one) by calculating R_{RX} using equation (12). A nominal line resistance (R_L) of 900 Ω will be assumed.

$$R_{RX} = \frac{(95)(900)(903)}{(900+903)(1)}$$
$$= 42821\ \Omega$$

A 43.2 kΩ ±1.0% resistor should be used for R_{RX}. Use a 1.0 μF 20 V capacitor for C_{RX}.

Transhybrid transmission gain (G_{TX}) is set for unity gain by calculating R_{VTX}, using equation (13).

$$R_{VTX} = \frac{(17400+17400+1200)(1)}{(1-0.4007)}$$
$$= 60070\ \Omega$$

A 60.4 kΩ ±1.0% resistor should be used for R_{VTX}.

The balance resistor (R_B) is selected to maximize transhybrid rejection with R_L of 600 Ω using equation (15).

$$R_B = \frac{43200\,[1+97\,(0.4007)]\,(903+600)}{97\,(1-0.4007)(600)}$$
$$= 74216\ \Omega$$

A 75 kΩ ±1.0% resistor would be selected.

The digital Hook Status Output resistor (R_{HS}) is determined from a consideration of the type of logic with which the output must interface and the power supply voltages of that logic. Assuming CMOS at V_{DD} = 0 V and V_{SS} = 12 V, then

$$R_{HS} = \frac{V_{SS}}{I_{HS}}$$
$$= \frac{12\ V}{200\ \mu A}$$
$$= 60\ k\Omega$$

A 62 kΩ ±5.0% resistor is suitable.

The complete SLIC design is shown in Figure 20, along with the codec, filter, time-slot assigner/channel controller, and reference voltage needed for a complete line circuit.

2

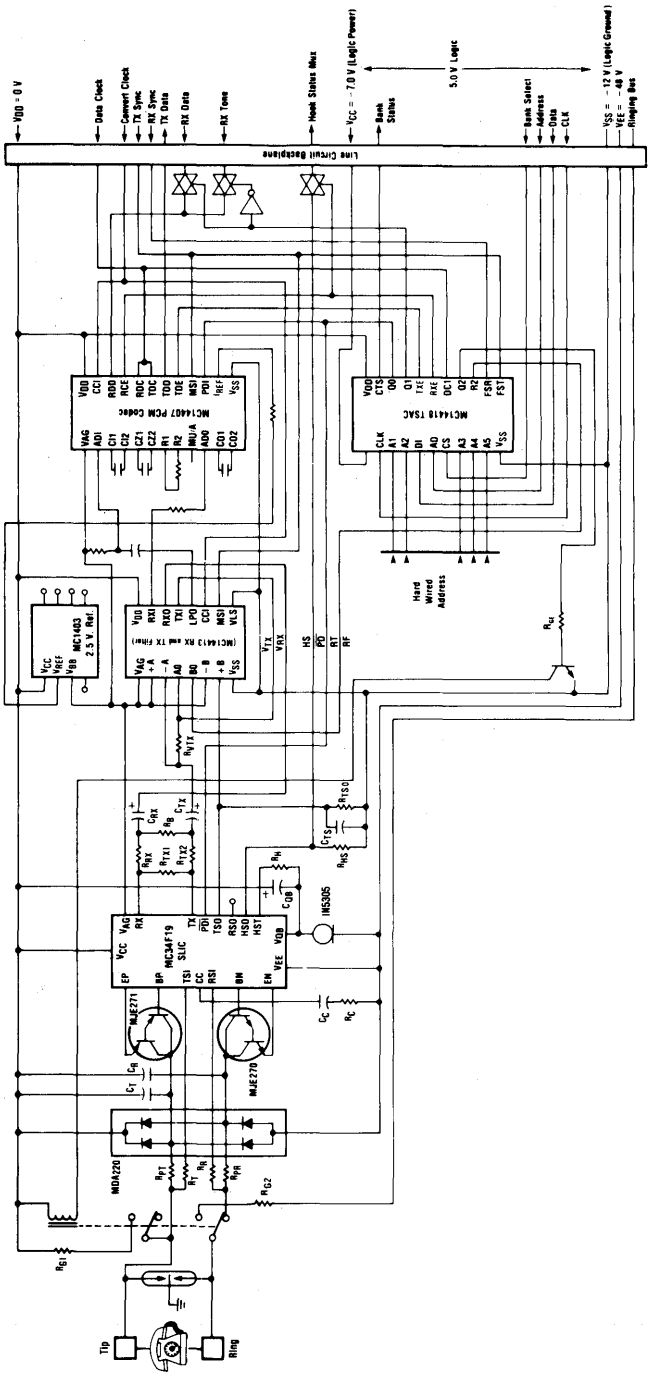
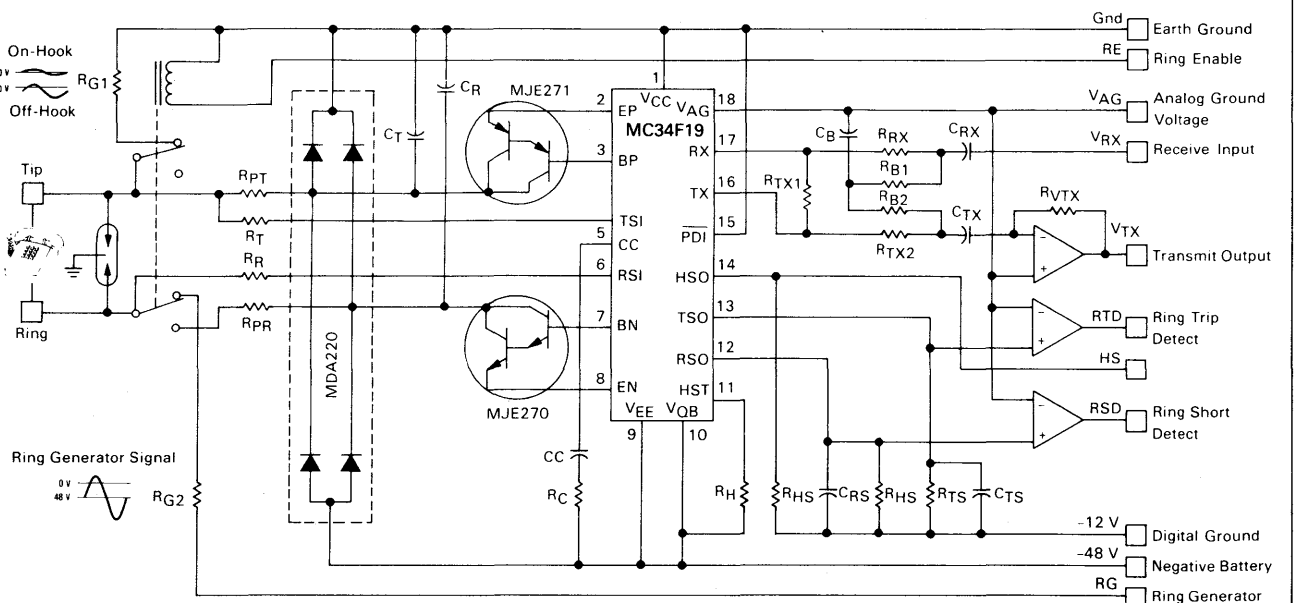


FIGURE 20 — LINE CIRCUIT USING SLIC, FILTER, CODEC AND TSAC

FIGURE 19 — RING INSERTION



Note: Ring Relay is shown in energized position

MOTOROLA

MC6172
(Formerly MC6862)

MOS
(N-CHANNEL, SILICON-GATE)

2400 bps MODULATOR

2

2400 bps DIGITAL MODULATOR

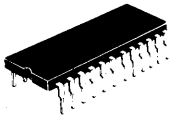
The MC6172 is a MOS subsystem designed to be integrated into a wide range of equipment utilizing serial data communication.

The modulator provides the necessary modulation and control functions to implement a serial data communication link over a voice grade channel, utilizing differential phase shift keying (DPSK) at bit rates of 1200 or 2400 bps. Phase options are provided for both the U.S. and international markets. The MC6172 can be implemented into a wide range of data handling systems, including stand-alone modems, data storage devices, remote data commuication terminals, and I/O interfaces for counters.

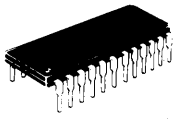
N-channel silicon-gate technology permits the MC6172 to operate using a single voltage supply and be fully TTL compatible.

The modulator is compatible with the MC6173 demodulator to provide medium-speed data communications capability.

- Clear-to-Send Delay Options
- 511-Bit CCITT Test Pattern
- Terminal Interfaces are TTL Compatible
- Compatible Functions for 201B/C Data Sets
- CCITT and U.S. Phase Options
- 1200/2400 bps Operation
- Answer-Back Tone
- The MC6173 Is the Companion Demodulator
- Application Note Available — AN-870

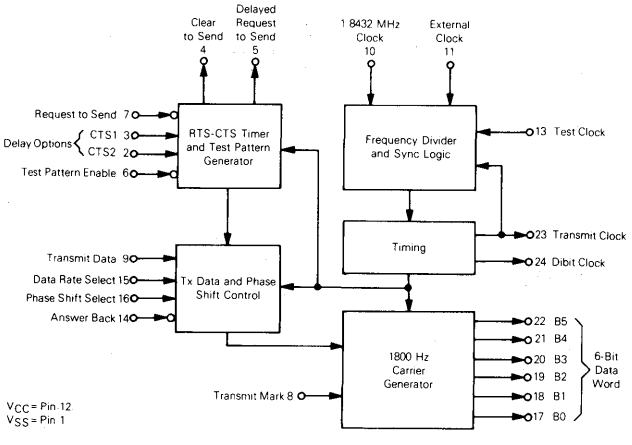


L SUFFIX
CERDIP PACKAGE
CASE 623

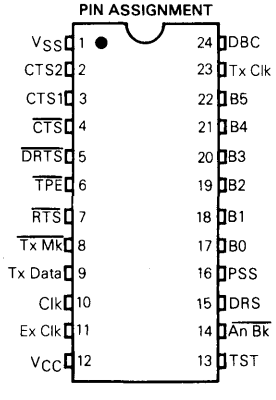


P SUFFIX
PLASTIC PACKAGE
CASE 709

BLOCK DIAGRAM



PIN ASSIGNMENT



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	V
Input Voltage	V_{in}	−0.3 to +7.0	V
Operating Temperature Range	T_A	T_L to T_H 0 to 70	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Resistance Plastic Package Cerdip Package	θ_{JA}	 120 65	°C/W

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{CC}).

2

POWER CONSIDERATIONS

The average chip-junction temperature, T_J, in °C can be obtained from:

$$T_J = T_A + (P_D \bullet \theta_{JA}) \quad (1)$$

Where:

$T_A \equiv$ Ambient Temperature, °C

$\theta_{JA} \equiv$ Package Thermal Resistance, Junction-to-Ambient, °C/W

$P_D \equiv P_{INT} + P_{PORT}$

$P_{INT} \equiv I_{CC} \times V_{CC}$, Watts – Chip Internal Power

$P_{PORT} \equiv$ Port Power Dissipation, Watts – User Determined

For most applications $P_{PORT} \ll P_{INT}$ and can be neglected. P_{PORT} may become significant if the device is configured to drive Darlington bases or sink LED loads.

An approximate relationship between P_D and T_J (if P_{PORT} is neglected) is:

$$P_D = K \div (T_J + 273°C) \quad (2)$$

Solving equations 1 and 2 for K gives:

$$K = P_D \bullet (T_A + 273°C) + \theta_{JA} \bullet P_D^2 \quad (3)$$

Where K is a constant pertaining to the particular part. K can be determined from equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

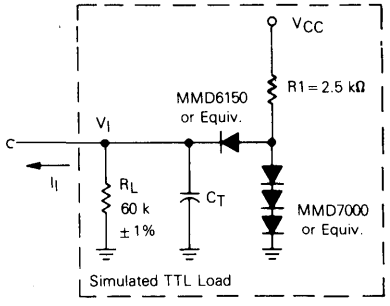
DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0 ±0.25 Vdc, V_{SS} = 0, $T_A = T_L$ to T_H, all outputs loaded as shown in Figure 1 unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Input High Voltage	V_{IH}	V_{SS} + 2.0	–	V_{CC}	V
Input Low Voltage	V_{IL}	V_{SS}	–	V_{SS} + 0.8	V
Input Current ($V_{in} = V_{SS}$) CTS1, CTS2, PSS, DRS, $\overline{An\ Bk}$, and $\overline{Tx\ MK}$ $\overline{RTS}$ and $\overline{TPE}$	I_{in}	– –	– –	−0.2 −1.6	mA
Input Leakage Current (V_{in} = 5.25 V, $V_{CC} = V_{SS}$)	I_{IL}	–	–	2.5	μA
Output High Voltage (I_{OH} = −0.04 mA, Load A) (I_{OH} = 0.0 mA, Load B)	 V_{OH1} V_{OH2}	 V_{SS} + 2.4 V_{CC} − 0.5 V	 – –	 V_{CC} V_{CC}	V
Output Low Voltage (I_{OL} = 1.6 mA, Load A)	V_{OL}	V_{SS}	–	V_{SS} + 0.4	V
Input Capacitance (f = 0.1 MHz, T_A = 25°C)	C_{in}	–	5.0	–	pF
Internal Power Dissipation (Measured at $T_A = T_L$) (All inputs at V_{SS} except Pin 13 = 57.6 kHz and ALL outputs open)	P_{int}	–	210	315	mW
Input Transition Times, All Inputs Except 1.8432 MHz Input (From 10% to 90% points)	t_r, t_f	–	–	1.0*	μs
Input Transition Times, 1.8432 MHz Input (From 0.8 V to 2.0 V)	t_r, t_f	–	–	40	ns
Input Clock Duty Cycle, 1.8432 MHz Input (Measured at 1.5 V level)	D.C.	30	–	70	%
Tx Data Setup Time (Figure 2)	t_{su}	35	–	–	μs
Tx Data Hold Time (Figure 2)	t_h	35	–	–	μs
Output Transition Times	t_r, t_f	–	–	5.0	μs

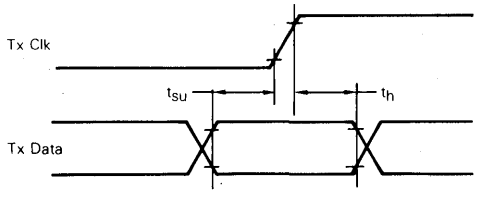
*Maximum Input Transition Times are ≤ 0.1 × Pulse Width or the specified maximum of 1.0 μs, whichever is smaller.

FIGURE 1 — OUTPUT TEST LOAD



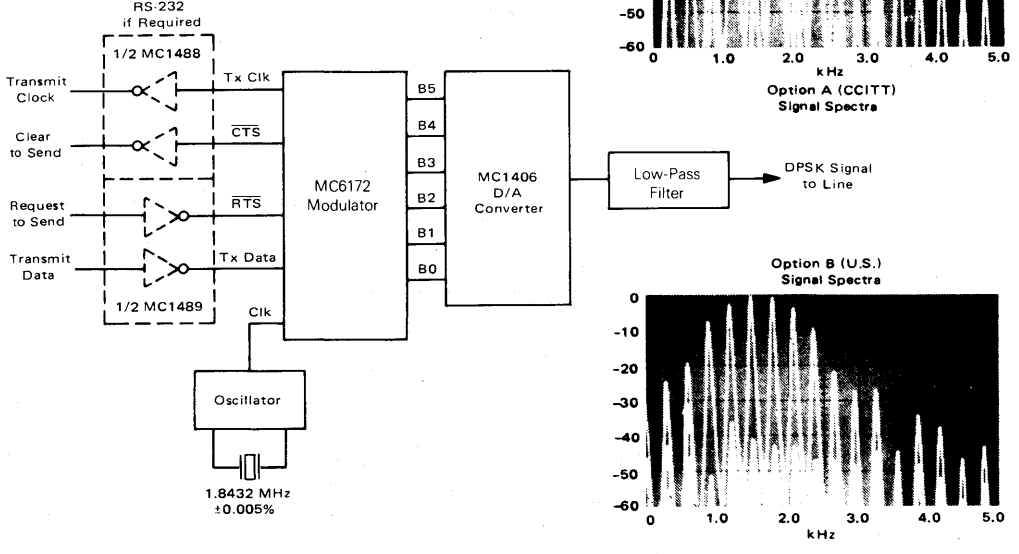
C_T = 20 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

FIGURE 2 — TRANSMIT DATA SETUP AND HOLD TIME



Note: Timing measurements are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts, unless otherwise noted.

FIGURE 3 — 2400 bps MODULATOR INTERFACE

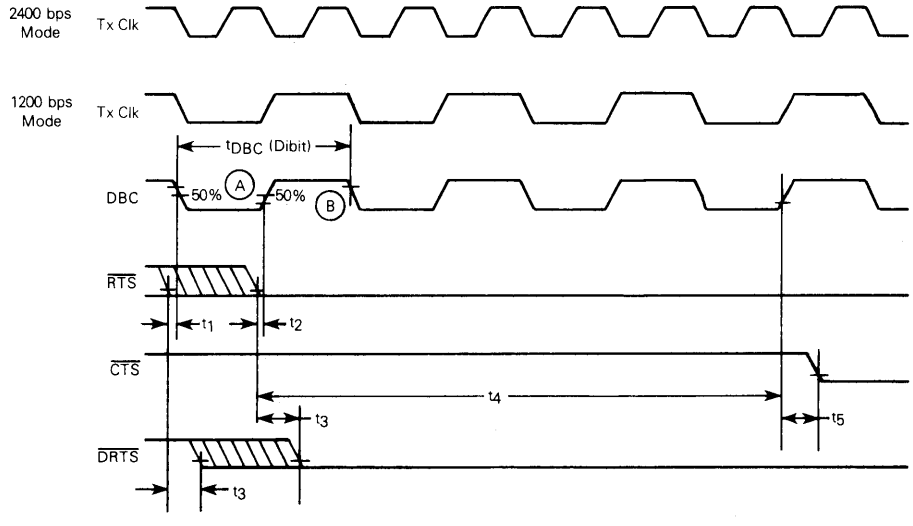


DELAY TIMINGS (See Figures 4 and 5)

Characteristic	Symbol	Min	Typ	Max	Unit
$\overline{RTS}$ to DBC Delay	t_1	–	–	8	μs
DBC to $\overline{RTS}$ Delay	t_2	45	–	–	μs
$\overline{RTS}$-$\overline{DRTS}$ Delay	t_3	–	–	35	μs
$\overline{RTS}$-$\overline{CTS}$ Delay					
CTS1 = 0, CTS2 = 1	t_4*	0	–	35	μs
CTS1 = 1, CTS2 = 0		8.55	–	9.35	ms
CTS1 = 1, CTS2 = 1		24.9	–	26.4	ms
CTS1 = 0, CTS2 = 0		147.0	–	154.0	ms
$\overline{CTS}$-DBC Delay					
CTS1 = 1, CTS2 = 0	t_5	–	–	35	μs
CTS1 = 1, CTS2 = 1		–	–	35	
CTS1 = 0, CTS2 = 0		–	–	35	
$\overline{RTS}$ to $\overline{CTS}$ Low	t_6	–	–	1.60	ms
$\overline{RTS}$ Min Delay	t_7	–	–	1.67	ms
DBC to $\overline{DRTS}$ Delay	t_8	–	–	35	μs
DBC Cycle Time	t_{DBC}	833.28	833.33	833.37	μs

*The reference frequency tolerance is not included.

FIGURE 4 – $\overline{RTS}$-$\overline{CTS}$ AND $\overline{RTS}$-$\overline{DRTS}$ DELAYS



$\overline{RTS}$-$\overline{CTS}$ delay options are selected by the CTS1 and CTS2 inputs, and are stated as time delay interval t_4. An $\overline{RTS}$ input signal synchronized about point A will synchronize $\overline{CTS}$ with the positive transition of DBC (Dibit Clock). Delay t_4 is measured with respect to the negative transition of $\overline{RTS}$.

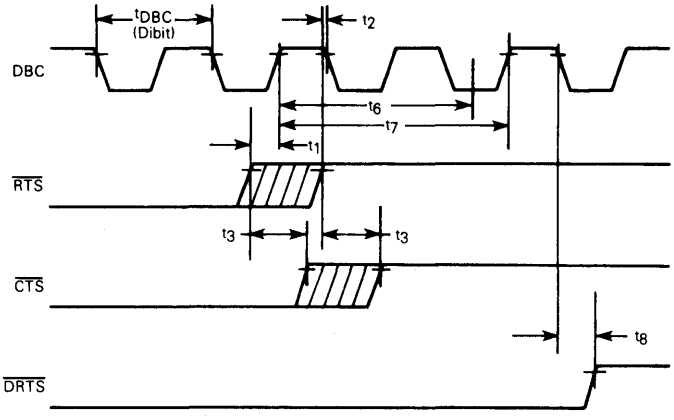
$\overline{RTS}$ signals synchronized with the positive transition of DBC (point B), will result in the same $\overline{CTS}$ delay (t_4). For this case the negative transition of $\overline{CTS}$ is synchronized with the negative transition of DBC with delay t_4 measured with respect to the negative transition of $\overline{RTS}$.

$\overline{DRTS}$ will go low within t_3 of the negative transition of $\overline{RTS}$. With the exception of the no-delay option, $\overline{CTS}$ will go low within t_5 of the positive transition of DBC, following the t_4 delay selected. This applies when $\overline{RTS}$ is synchronized to Point A as shown.

If $\overline{RTS}$ goes high and remains high ≥ 20 μs within time interval t_4, a reset of the internal $\overline{RTS}$-$\overline{CTS}$ timer function will occur. If $\overline{RTS}$ goes high for less than 20 μs, the circuit may or may not respond to this momentary loss of the $\overline{RTS}$ signal.

Note: Timing measurements are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts, unless otherwise noted.

FIGURE 5 — LOSS OF $\overline{RTS}$ TO $\overline{DRTS}$ DELAY



A positive transition of $\overline{RTS}$ after $\overline{CTS}$ has become active can result in different functional characteristics of the $\overline{CTS}$ and $\overline{DRTS}$ output signals, depending on the time duration that $\overline{RTS}$ remains inactive.

Under all conditions, $\overline{CTS}$ will go high within t_3 following a positive transition of $\overline{RTS}$. If $\overline{RTS}$ goes high in the shaded region shown (i.e., synchronized to the positive transition of DBC) and remains high beyond the time interval defined as t_7, then $\overline{DRTS}$ will go high within t_8 of the next negative transition of DBC. If $\overline{RTS}$ were to go low after t_7, the $\overline{RTS}$-$\overline{CTS}$ delay times given in Figure 4 will result.

If $\overline{RTS}$ goes high in the shaded region shown, and then returns low within time interval t_6, the negative transition of $\overline{CTS}$ will follow within 35 μs, and $\overline{DRTS}$ will remain in the active or low state. Under these conditions, the normal $\overline{RTS}$-$\overline{CTS}$ delay times are not encountered when $\overline{RTS}$ is reactivated. If $\overline{RTS}$ goes low for less than 20 μs, the circuit may or may not respond

NOTE: Timing measurements are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts, unless otherwise noted.

DEVICE OPERATION

GENERAL

Figure 3 shows the modulator and its intra-connections. The data to be transmitted is presented in synchronous serial format to the modulator for conversion to DPSK signals used in transmission. The modulator output is digital; therefore, a D/A converter and a filter transform the signal to an analog form.

The control functions provide four different Clear-to-Send delay options. An Answer-Back tone is available for automatic answering applications. The modulator has a built-in 511-bit pseudorandom pattern generator for use in system diagnostic tests.

INPUT/OUTPUT FUNCTIONS

Request to Send ($\overline{RTS}$)

The $\overline{RTS}$ signal from the data terminal controls transmission from the modulator. A low level on $\overline{RTS}$ activates the modulator data output. A constant mark, for synchronization, is sent during the $\overline{RTS}$ to $\overline{CTS}$ delay interval. Termination of the transmission is accomplished by taking $\overline{RTS}$ high (see Figures 4 and 5).

Delayed Request to Send ($\overline{DRTS}$)

This output can be used to control transmission as specified by the Transmit Mark control input. $\overline{DRTS}$ follows the negative transition of $\overline{RTS}$, and goes negative within t_3 of the negative transition of $\overline{RTS}$ (Figure 4). The delay from a positive transition of $\overline{RTS}$ to a positive transition of $\overline{DRTS}$ is shown in Figure 5. The $\overline{DRTS}$ delay allows data within the modulator to be transmitted before transmission is inhibited.

Clear to Send ($\overline{CTS}$)

$\overline{CTS}$ follows $\overline{RTS}$ to both the logic 0 and logic 1 levels. The delay from a negative transition of $\overline{RTS}$ to a negative $\overline{CTS}$ transition is selectable by external strapping of CTS1 and CTS2. The delay from a positive transition of $\overline{RTS}$ to a positive $\overline{CTS}$ transition is less than t_4.

$\overline{CTS}$ will go low within t_5 after the positive transition of the Dibit Clock (see Figure 4) except when the non-delay option is selected. For the no-delay option, $\overline{CTS}$ follows $\overline{RTS}$ within t_5.

$\overline{RTS}$-$\overline{CTS}$ Delay Options (CTS1, CTS2)

The $\overline{RTS}$-$\overline{CTS}$ delays are selectable according to the following strapping options

$\overline{RTS}$-$\overline{CTS}$ Delay	CTS1	CTS2
0.0 + 0.035 ms, −0.0 ms	0	1
8.55 to 9.35 ms	1	0
24.90 to 26.4 ms	1	1
147.0 to 154.0 ms	0	0

Transmit Mark (Tx Mk)

The Transmit Mark control allows the system designer to select whether the Delayed Request to Send activitates and deactivates the transmission on the modulator chip or off the chip in the output amplifier.

When Tx Mk is high, transmission is controlled on the modulator chip, and occurs from the chip only when $\overline{DRTS}$ or Answer Back is in the logic 0 state (see Figure 6).

When Tx Mk is low, transmission is controlled off the modulator chip. In this mode, the modulator chip transmits marks at all times except when data or an Answer-Back tone is being transmitted (see Figure 6).

Test Pattern Enable ($\overline{TPE}$)

A 511-bit test pattern generator is contained on the modulator chip. This pattern is in accord with CCITT specification V52.

The 511-bit test pattern is activated by applying a logic 0 to $\overline{TPE}$. A mark (logic 1) condition on the Transmit Data input with $\overline{TPE}$ activated (logic 0) causes the test pattern to appear at the data output. A space (logic 0) condition on Tx Data with $\overline{TPE}$ activated causes the test pattern data to appear inverted at the data output.

Although the Motorola 2400 bps modulator contains a CCITT 511 test pattern generator it does not incorporate the 511 data randomizer or scrambler.

Random data applied to Tx Data with TPE activated causes the test pattern data to be scrambled (exclusive NORed) with the data, and the result appears at the data output.

The MC6173 demodulator does contain a built-in data descrambler, which is enabled by $\overline{TPE}$ input going active. To scramble data using the modulator, the circuit in Figure 7 must precede the Tx Data input of the modulator. Tx Data is added to the scrambler output pattern. Then the data is delayed by a full data bit before being transmitted by the modem. This assures a proper Transmit Data/Transmit Clock phase relationship.

If the data scrambler is to be an optional feature, then the transmit data multiplexer would also have to be built. This is selected by the Test Pattern Enable signal or any other signal that is found suitable.

The scrambling of data in the data comm environment is not done in an attempt to encrypt information in the normal sense of the word. Rather, the purpose of the scrambling of data is to guarantee that with respect to the modem carrier, there is always random data on the line with little chance for a long string of ones or zeros to exist. This is particularly important if an adaptive equalizer is being incorporated at the demodulator. The adaptive equalizer will require reasonably evenly distributed data to optimize its statistical response to the incoming signal. The normally used code is the CCITT 511 sequence which is exclusive ORed with data.

The test pattern generator can be enabled only when $\overline{CTS}$ and $\overline{RTS}$ are logic 0. If $\overline{TPE}$ is activated outside this time interval, the previously stated $\overline{RTS}$-$\overline{CTS}$ and $\overline{RTS}$-$\overline{DRTS}$ delays, shown in Figures 4 and 5, are not valid.

Data-Rate Select (DRS)

The modulator can transmit at either 2400 bps or 1200 bps. Both data rates utilize an 1800 Hz carrier signal and employ phase shifting at 1200 Hz. The 2400 bps rate is obtained by encoding two bits of data into each phase shift. The 2400 Hz rate is selected by applying a logic 1 to the Data-Rate Select lead. The 1200 Hz rate is selected by applying a logic 0 to DRS.

Phase-Shift Select (PSS)

Option A (CCITT) or Option B (U.S.) phase shift can be selected for 2400 bps operation. The input data format and phase shift relationship for these two options are as follows:

Data	PSS = 0 Option A*	PSS = 1 Option B
00	0°	+45°
01	+90°	+135°
11	+180°	+225°
10	+270°	+315°

*See example Figure 8.

FIGURE 6 — TRANSMIT MARK CONTROL

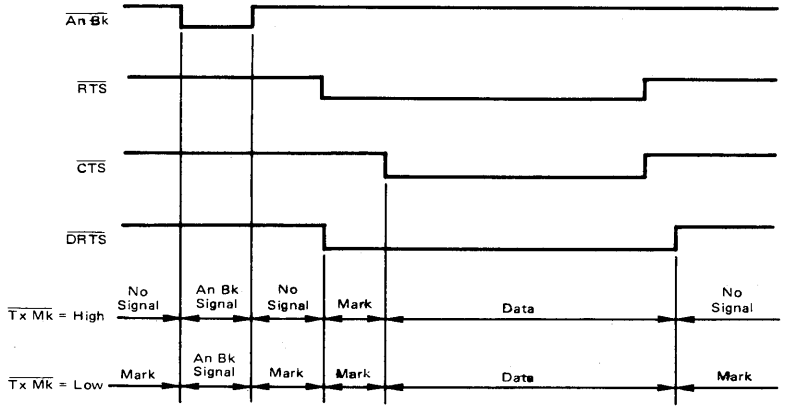


FIGURE 7 — MODULATOR CCITT 511 DATA SCRAMBLER

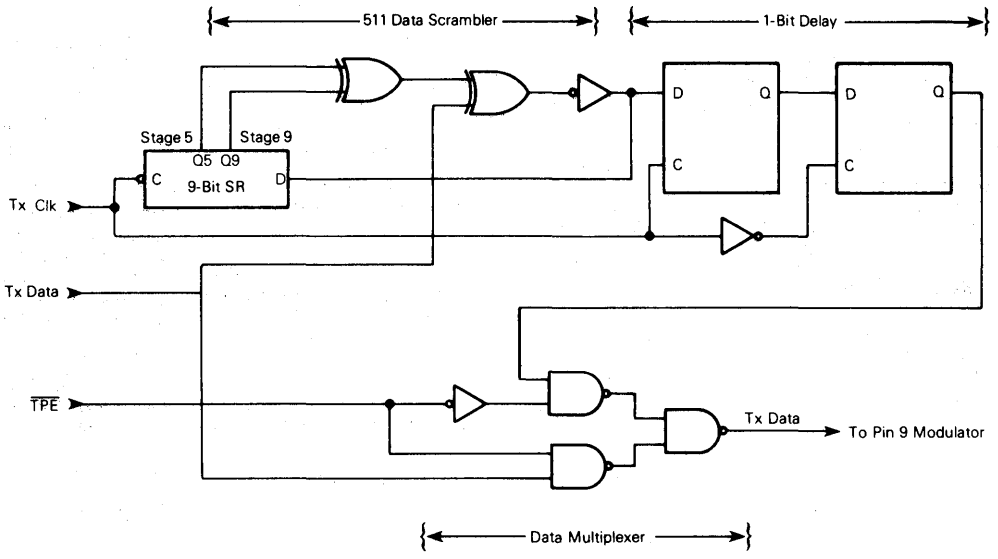
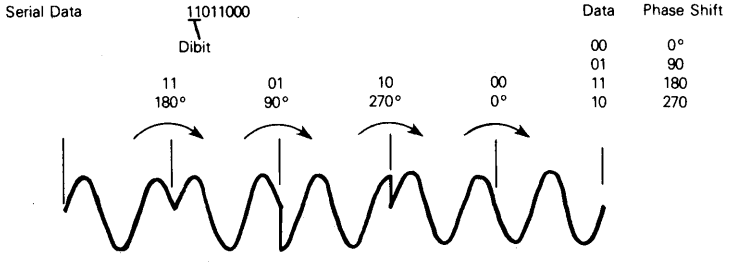


FIGURE 8 — EXAMPLE-CARRIER PHASE SHIFTS FOR OPTION A



For 1200 bps operation, Option C (CCITT) or Option D (U.S.) phase shift can be selected:

Data	PSS = 0 Option C	PSS = 1 Option D
0	+90°	+45°
1	+270°	+225°

Option C is selected by applying a logic 0 to the Phase Shift Select lead when the Data Rate Select lead is strapped for 1200 bps operation (logic 0). Option D is selected by applying a logic 1 to PSS with DRS at logic 0. The phase shifts shown are the difference in phase between the signal at the end of one dibit period and the new signal at the beginning of the next dibit.

Transmit Data (Tx Data)

Transmit Data is the serial binary information presented for DPSK modulation. A high level represents a mark. For timing, see Transmit Clock (Figure 4).

Transmit Clock (Tx Clk)

A 2400/1200 Hz Transmit Clock output is provided for the communication terminal. The Transmit Data signal is sampled on the positive transition of Transmit Clock. The Transmit Data to Transmit Clock setup and hold time requirements are shown in the Electrical Characteristics Table and in Figure 2.

Dibit Clock (DBC)

A 1200 Hz Dibit Clock identifies the modulation timing. This signal goes negative less than 100 μs prior to the start of dibit modulation.

External Clock (Ex Clk)

A 2400/1200 Hz clock signal applied to the External Clock lead causes Transmit Clock to be synchronized with Ex Clk. This input must have an accuracy within ±0.005%.

When no transitions occur on this input, the internal clock provides the 2400/1200 Hz transmit timing signal. Fast synchronization of Tx Clk to Ex Clk is not provided on the chip. *When Ex Clk is not used, it should be tied to either the logic 0 or logic 1 state.*

1.8432 MHz (Clk)

This input must be a square wave with rise and fall times of less than 40 ns and a 50 ±20% duty cycle. The clock accuracy must be written ±0.005%.

Answer Back ($\overline{\text{An Bk}}$)

A logic 0 level applied to Answer Back causes a 2025 Hz carrier to be generated on the modulator chip instead of a phase shifted 1800 Hz carrier. A logic 1 level applied to $\overline{\text{An Bk}}$ enables the modulator to generate the normal phase shifted 1800 Hz carrier signal, as shown in Figure 6. The time delay from a transition on $\overline{\text{An Bk}}$ to the appropriate signal at the modulator chip output is less than 2 ms.

Activation of $\overline{\text{An Bk}}$ (a logic 0) will disable all other operation modes including the $\overline{\text{Tx Mk}}$ function, and will reset $\overline{\text{CTS}}$ to an inactive state along with the $\overline{\text{RTX-CTS}}$ internal timer. $\overline{\text{An Bk}}$ should therefore be activated only before initiating $\overline{\text{RTS}}$ or after loss of the $\overline{\text{DRTS}}$ output signal. The combination of a logic 0 on $\overline{\text{An Bk}}$ with a logic 0 on $\overline{\text{TPE}}$ is not used in normal system operation, and hence is used as a reset input during device test.

Digital Output (B0-B5)

These outputs are designed to interface with a 6-bit digital-to-analog converter. The resultant signal out of the D/A is the differential phase shift keyed signal quantized at a 14.4 kHz rate. A low-pass filter can then be used to smooth the data transitions. B0 is the least-significant bit, and the positive level the active state.

Test Clock (TST)

A test signal input is provided to decrease test time of the chip. *In normal operation this input must be strapped low.*

MOTOROLA

MC6173

2

2400 bps DIGITAL DEMODULATOR

The MC6173 is a MOS subsystem designed to be integrated into a wide range of equipment utilizing serial data communication.

The demodulator provides the necessary demodulation and control functions to implement a serial data communication link over a voice grade channel, utilizing differential phase shift keying (DPSK) at bit rates of 1200 or 2400 bps. Phase options are provided for both the U.S. and international markets. The MC6173 can be implemented into a wide range of data handling systems, including stand-alone modems, data storage devices, remote data communication terminals, and I/O interfaces for counters.

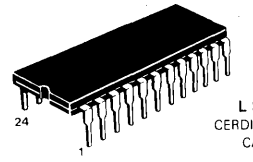
N-channel silicon gate technology permits the MC6173 to operate using a single voltage supply and be fully TTL compatible.

The demodulator is compatible with the M6800 microcomputer family, and provides medium-speed data communications capability.

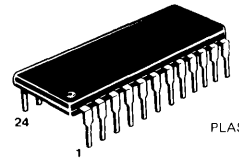
- Compatible with MC6172 Modulator
- 511-Bit CCITT V.52 Test Pattern
- Terminal Interfaces Are TTL Compatible
- Compatible Functions for 201B/C and V.26 Data Sets
- CCITT and U.S. Phase Options
- 1200/2400 bps Operation

MOS
(N-CHANNEL, SILICON-GATE)

2400 bps DEMODULATOR

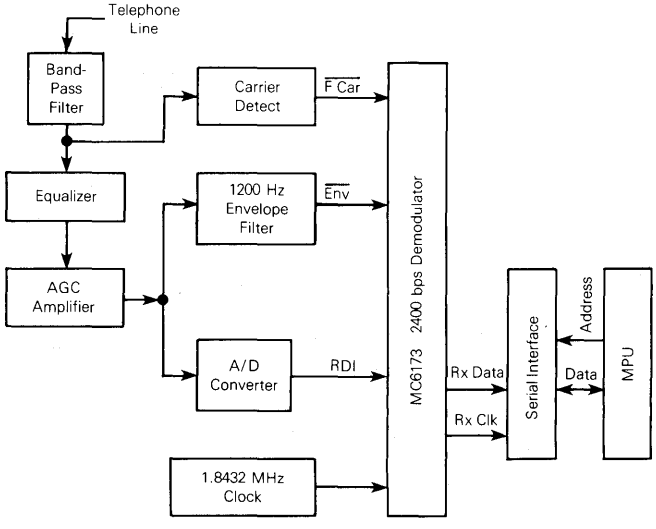


L SUFFIX
CERDIP PACKAGE
CASE 623

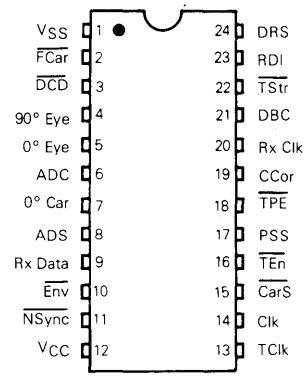


P SUFFIX
PLASTIC PACKAGE
CASE 709

FIGURE 1 — TYPICAL APPLICATIONS



PIN ASSIGNMENT



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	V
Input Voltage	V_{in}	−0.3 to +7.0	V
Operating Temperature Range	T_A	0 to 70	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C
Thermal Resistance	θ_{JA}	82.5	°C/W

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{SS}).

2

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5.0 ±0.25 Vdc, V_{SS}=0, T_A=T_L to T_H all outputs loaded as shown in Figure 3 unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input High Voltage	V_{IH}	V_{SS}+2.0	–	V_{CC}	V
Input Low Voltage	V_{IL}	V_{SS}	–	V_{SS}+0.8	V
Input Current (V_{in}=V_{IL}) Pins 3, 11, 13, 15, 16, 17, 18, 22, 24	I_{IL}	–	–	−0.2	mA
Input Leakage Current (V_{in}=5.25 Vdc, V_{CC}=V_{SS}) Pins 2, 10, 14, 23	I_{in}	–	–	2.5	μA
Output High Voltage (I_{OH}= −0.04 mA, Load A) (I_{OH}=0.0 mA, Load B)	V_{OH1} V_{OH2}	V_{SS}+2.4 V_{CC}−0.5 V	– –	V_{CC} V_{CC}	V
Output Low Voltage (I_{OL}=1.6 mA, Load A)	V_{OL}	V_{SS}	–	V_{SS}+0.4	V
Input Capacitance (f=0.1 MHz, T_A=25°C)	C_{in}	–	5.0	–	pF
Internal Power Dissipation (measured at T_A=T_L) (All Inputs at V_{SS} except Pin 13=57.6 kHz and ALL Outputs Open)	P_{Int}	–		630	mW
Input Transition Times, 1.8432 MHz Input (From 0.8 V to 2.0 V)	t_r t_f	– –	– –	40 40	ns
Input Transition Times, All Inputs Except 1.8432 MHz Input (From 10% to 90% Points)	t_r,t_f	–	–	1.0*	μs
Output Transition Times (From 10% to 90% Points)	t_r,t_f	–	–	5.0	μs
Input Clock Duty Cycle, 1.8432 MHz Input (Measured at 1.5 V level)	D.C.	30	–	70	%
Data Setup Time	t_{DS}	770	–	–	ns
Rx Data Setup Time	t_{su}	35	–	–	μs
Data Hold Time	$t_{h(D)}$	0	–	–	ns
Rx Data Hold Time	t_h	35	–	–	μs
Data-Clamp Delay Time Option 1 Option 2 Option 3 Option 4	 t_{DCD1} t_{DCD2} t_{DCD3} t_{DCD4}	 5.7 4.135 20.795 104.135	 6 4.17 20.83 104.17	 6.3 4.205 20.865 104.205	 ns ms ms ms
A/D Clock to A/D Strobe Delay Time	t_{ADCD}	1.06	–	1.11	μs
Envelope-to-Dibit Clock Delay Time	t_{ED}	140	–	220	μs
Clock Frequency, ±0.005%	f_{Clk}	–	1.8432	–	MHz
A/D Clock Cycle Time (f_{Clk}/4)	t_{cyc}	–	2.17	–	μs
A/D Clock Pulse Width	$t_{w(ADC)}$	940	1000	1040	ns
A/D Strobe Pulse Width	$t_{w(ADS)}$	–	10.85	–	ns
New Sync Input Pulse Width	t_{w} (NSync)	0.84	–	–	ms

*Maximum input transition times are ≤ 0.1X pulse width or the specified maximum of 1.0 μs, whichever is smaller.

FIGURE 2 — DEMODULATOR BLOCK DIAGRAM

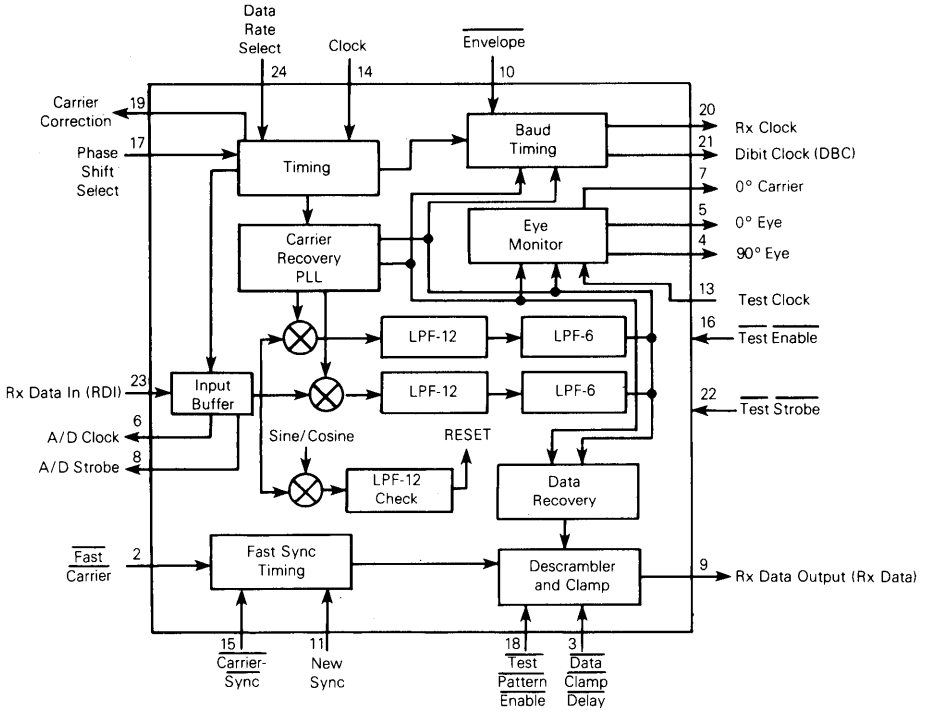
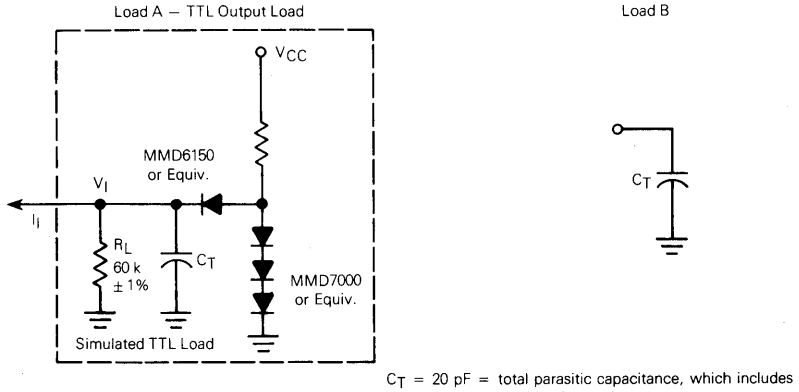


FIGURE 3 — OUTPUT TEST LOADS



C_T = 20 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances

GENERAL DESCRIPTION

The MC6173 Phase-Shift Key (PSK) Demodulator serves as an integral part of a system to recover synchronous data from an 1800 Hz PSK modulated carrier. Data rates of 1200 and 2400 bits-per-second are available. In the case of 1200 bps operation, the MC6173 detects phase shifts of 0 to 180 degrees to represent digital "0s" and "1s". When 2400 bps operations is desired, the MC6173 detects phase shifts of 0, 90, 180, and 270 (option A) or 45, 135, 225, and 315 (option B) degrees to represent two bits of data called dibits. These phase shifts decode to 00, 01, 10, and 11, respectively. In either data rate, the 1800 Hz carrier is modulated at a 1200 rate.

Figure 1 shows the MC6173 demodulator in a typical application. The band-pass filter, equalizer, analog-to-digital (A/D) converter, 1200 Hz envelope filter, AGC amplifier, and 1800 Hz carrier detector are external to the MC6173. The band-pass filter passes roughly 300 Hz to 3000 Hz eliminating noise, 60 Hz and 120 Hz pickup, and harmonics of 1800 Hz. The output of this filter is fed to the equalizer which adjusts phase versus amplitude such that a constant amplitude is maintained regardless of phase and is fed into the carrier detect circuit. The AGC amplifier provides a constant level signal regardless of the input level from the equalizer. The output of the AGC amplifier drives two basic sections of external circuitry, i.e., the A/D converter, and 1200 Hz envelope filter.

The A/D converter samples each 1200 Hz cycle or dibit 12 times. After each sample, digital data is clocked serially to the MC6173 receiver data input (RDI). The MC6173 generates the sampling clock for AD Strobe (ADS) and the serial clock (ADC) from the 1.8432 MHz internal oscillator.

The 1200 Hz envelope filter recovers the 1200 Hz component of the equalizer output during fast training and generates a 1200 Hz square wave. This square wave is connected to the envelope ($\overline{Env}$) input and is used for internal timing.

The carrier detect circuit is used to signal the fast carrier ($\overline{FCar}$) input that a carrier is present. Immediately after $\overline{FCar}$ has received a negative transition, the internal phase-lock loop temporarily widens its band width so that it can quickly adjust the internal timing of the MC6173 with respect to the 1200 Hz $\overline{Env}$ input (this is called fast Sync or fast training). The timing adjustments are made so that each dibit can be sampled at the most advantageous places.

The internal circuitry digests the dibit samples and produces the digital data (Rx Data) along with the receive data clock (Rx Clk). These two signals are used to drive a serial-to-parallel interface such as an MC6852 Synchronous Serial Interface Adapter.

PIN DESCRIPTION

FAST CARRIER ($\overline{FCar}$), Pin 2 – A negative transition on this input will force a period of approximately 8.3 ms of fast training for both baud and carrier timing.* Fast Sync or fast training allows for large corrections to be made in the internal timing of the demodulator. After the fast training period, the timing should be reasonably well adjusted. Small adjustments are made automatically to maintain proper phase relationships internally after the fast-train period.

The $\overline{FCar}$ input, which normally comes from the carrier threshold detect circuits, must remain at a low level during the entire period of baud and carrier synchronization.

A positive level on the $\overline{FCar}$ input will disable the baud and carrier correction circuitry. Baud and carrier timing are then direct derivatives of the 1.8432 MHz clock as illustrated in Figure 4.

The first positive edge of the envelope ($\overline{Env}$) input will be totally asynchronous to the demodulator. This will be $\pm$ ½ cycle of the 2400 clock ($\pm$208 μs). The nine following positive edges will introduce added tolerance equal to nine times the offset of $\overline{Env}$ from the absolute 1200 Hz (as defined by the 1.8432 MHz $\pm$0.005% clock). Thus . . .

$$\text{Max Fast Train Time} = 4.17\ \text{ms} + 9\ f_{Env} + 0.21\ \text{ms}$$
$$= 4.38\ \text{ms} + 9/f_{Env}$$
$$\text{Min Fast Train Time} = 4.17\ \text{ms} - 0.21\ \text{ms} + 9/f_{Env}$$
$$= 3.96\ \text{ms} + 9/f_{Env}$$

DATA-CLAMP DELAY ($\overline{DCD}$), Pin 3 – Data-clamp delay enables the selection of one of four delays during which Rx Data is held to a logic-high condition. This delay is measured from the negative edge of $\overline{FCar}$. The four options are available at one pin through the use of the internal multiplexing in the demodulator. Options 3 and 4 are available by demultiplexing the dibit clock as demonstrated in Figure 5. The available delay options are listed in Table 1, these times will be approximate due to their direct relationship to the $\overline{Env}$ input during the first 8.3 ms. Also, these times are further dependent upon carrier offset. The delays given in Table 1 assume no carrier offset and that $\overline{Env}$ is synchronous with the Tx Clk. Figure 4 is illustrative of the timing and sequencing of this circuit.

A scheme for programming the data-clamp delay is illustrated in Figure 5. The $\overline{DCD}$ input may either be a constant high or low level which will produce options 1 and 2. If the input "A" is exclusive ORed with the dibit clock options 3 and 4 are produced at the same input pin.

ENVELOPE ($\overline{Env}$), Pin 10 – The envelope input comes from the 1200 Hz envelope detection circuitry. Envelope detection will normally consist of a 1200 Hz filter and a voltage comparator to generate an approximate limited square wave. This is normally derived from a constant mark signal sent by the modulator for Sync acquisition purposes.

Each positive edge that is input to $\overline{Env}$ will reset both baud timing and the dibit clock to a logic "0". The optimum timing of the positive transition at the $\overline{Env}$ input will be t_{ED} prior to the falling edge of the dibit clock. Timing is illustrated in Figure 6.

$\overline{Env}$ will be effective in the training of baud timing and dibit clock only if $\overline{FCar}$ is in the active low state.

Minimum positive pulse width at the $\overline{Env}$ is $\geq$2.17 μs.

NEW-SYNC ($\overline{NSync}$), Pin 11 – This input port is normally controlled by the business machine. If $\overline{FCar}$ is at an active low, then an active low pulse in excess of 0.84 ms on the $\overline{NSync}$ lead will put the demodulator into the fast-Sync

*The postive transition of the 1200 Hz signal, present at the $\overline{Env}$ input, provides a divide-by-20 counter with every other clock. This will cause approximately 8.3 ms of fast training to the incoming signal at the demodulator.

FIGURE 4 — DEMODULATOR SYNC TIMING DIAGRAM

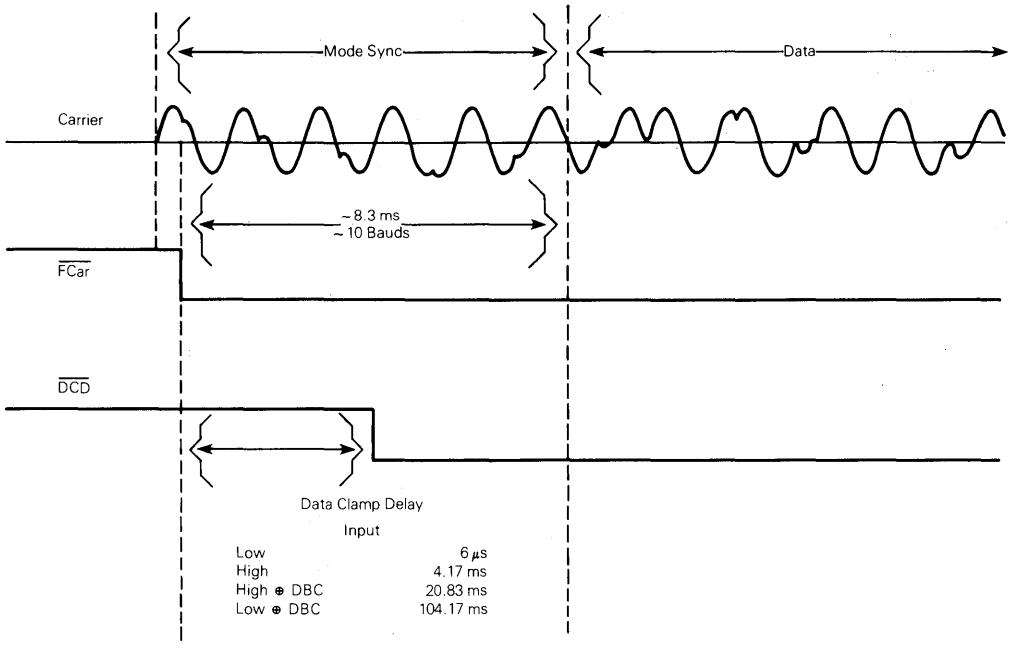


TABLE 1 — DATA-CLAMP DELAY OPTIONS

Option	A	C	$\overline{DCD}$	Data-Clamp Delay
1	1	0	0	6 μs
2	0	0	1	4.17 ms ± 35 μs
3	1	DBC	DBC	20.83 ms ± 35 μs
4	0	DBC	$\overline{DBC}$	104.17 ms ± 35 μs

FIGURE 5 — DATA-CLAMP DELAY DEMULTIPLEXER

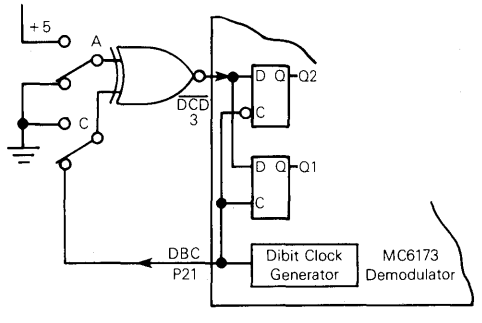
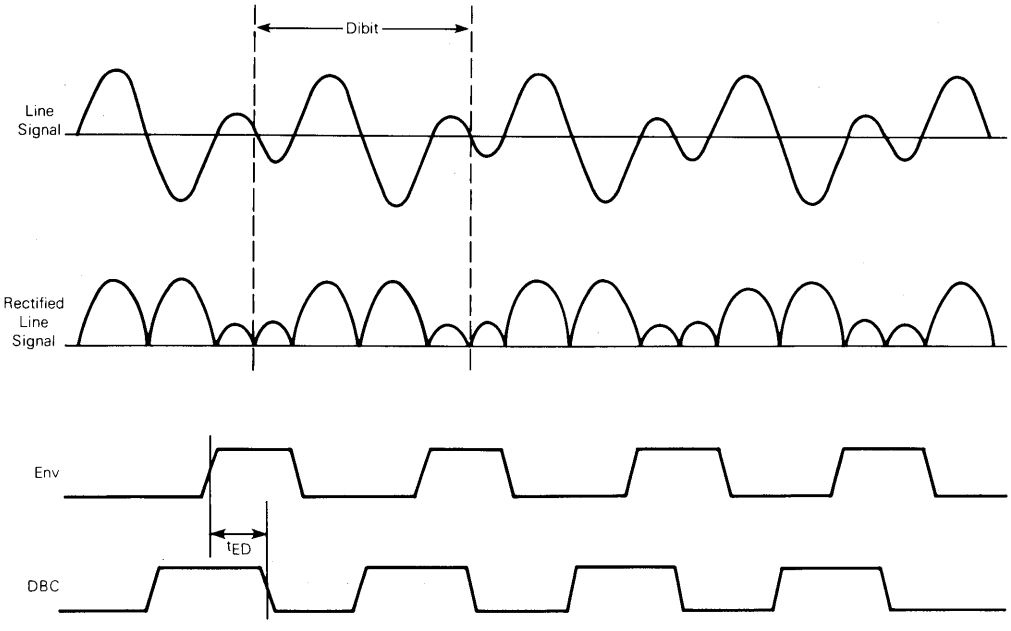


FIGURE 6 – ENVELOPE CLOCK TIMING DIAGRAM



or fast-train mode (these terms are synonymous).

Activation of $\overline{\text{NSync}}$ allows large corrections to be made to both baud and carrier timing similar to initial activation of the $\overline{\text{FCar}}$ lead. These corrections will be applied for approximately 8.3 ms. The receiver must complete the 8.3 ms period of fast Sync before another $\overline{\text{NSync}}$ is recognized.

$\overline{\text{CARRIER-SYNC}}$ ($\overline{\text{CarS}}$), Pin 15 – When $\overline{\text{CarS}}$ is taken to an active low, baud timing will be taken from the $\overline{\text{Env}}$ input. In addition, the slow carrier correction will be doubled in the 2400 baud mode as defined by the data-rate select (DRS) and phase-shift select (PSS) inputs. (This is not the same as the fast training that is incorporated when $\overline{\text{FCar}}$ or $\overline{\text{NSync}}$ are active, which is a changing of the bandwidth of the internal phase-lock loop [PLL]). This widening of the PLL band width will allow a faster search and lock on the 1800 Hz carrier. This Carrier-Sync mode will remain active as long as $\overline{\text{CarS}}$ is held in the active state. The normal application of this option would be to extend the training or Sync time under the mark input data condition that exceeds 8.3 ms.

If $\overline{\text{FCar}}$ is at a logic "1" inactive state, this input is ignored by the demodulator.

A/D CLOCK (ADC), Pin 6 – This output will allow, in a serial format, the six A/D data bits plus sign information to be synchronously clocked into the demodulator. (See Figure 8.)

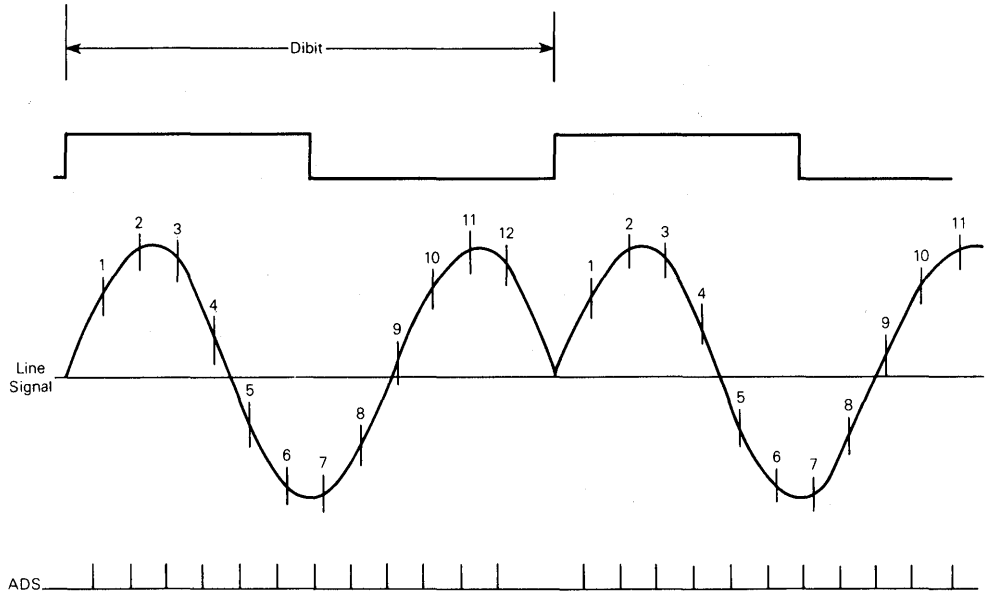
There are nine 1 μs positive pulses occuring at a 460 kHz rate. The first pulse, along with ADS, is used to begin the A/D conversion sequence. The next seven positive edges strobe data serially from the A/D converter to the demodulator input (RDI) enabling the demodulator to properly decode the A/D data.

This signal is also used to clock 0 and 90 degree eye data out of the demodulator. This is described in the Eye Pattern section. When $\overline{\text{TEn}}$ is low, ADC monitors check accumulator output (see $\overline{\text{TEn}}$).

A/D STROBE (ADS), Pin 8 – A positive going, approximately 11 μs, pulse is used as an enable signal for a sample and hold circuit prior to the A/D converter. The negative edge of this pulse is used to start the conversion process. Pulse rate of this signal is 14.4 kHz which allows each dibit to be sampled 12 times. (See Figure 7.) When $\overline{\text{TEn}}$ is low, ADS monitors zero crossings (see $\overline{\text{TEn}}$).

RECEIVER DATA INPUT (RDI), Pin 23 – The digital decode of the line signal magnitude, as sampled by the A/D, is input to the demodulator at this port. The data format is scaled binary. This sign bit occurs on the second A/D clock, followed by six magnitude bits which begin with the most-significant bit as shown in Figure 8. The data is strobed syn-

FIGURE 7 — ANALOG TO DIGITAL SAMPLE SCHEME



chronously with the positive edges of the ADC.

A logic one in the sign bit slot will represent a positive value. The magnitude of the six data bits increases from 000000 to 111111 with all ones always representing the most-positive value as illustrated below:

Sign	MSB					LSB	Value
1	1	1	1	1	1	1	+63
1	0	0	0	0	0	0	0
0	1	1	1	1	1	1	−0
0	0	0	0	0	0	0	−63

RECEIVE DATA OUTPUT (Rx Data), Pin 9 — This pin is the demodulator output for mark and space serial data. Data is synchronous with the receiver clock output with the positive going edge of the receiver clock occurring in the center of the data bit. A mark is represented by a logic high ("1") level except for the conditions described under PSS and $\overline{TPE}$.

The Rx Data output is inhibited in a logic-high level when $\overline{FCar}$ is in the inactive high state. The delay from the positive edge of $\overline{FCar}$ to the inhibiting of data is 2 μs.

RECEIVE CLOCK (Rx Clk), Pin 20 — The receive clock output provides the 2400 Hz $\pm$0.005% timing signal to the business machine for sampling the demodulated received data marks and spaces (Rx Data). Receive clock is present at the demodulator chip output at all times; is not clamped to an inactive state when the carrier detected is not presented on $\overline{FCar}$; nor is Rx Clk clamped by any other combination of inputs to the demodulator.

Timing corrections to the receive clock, that are generated internally, are made following $\overline{FCar}$ going active. As described in $\overline{FCar}$, if $\overline{CarS}$ is held active the receive clock is continuously updated from dibit Sync.

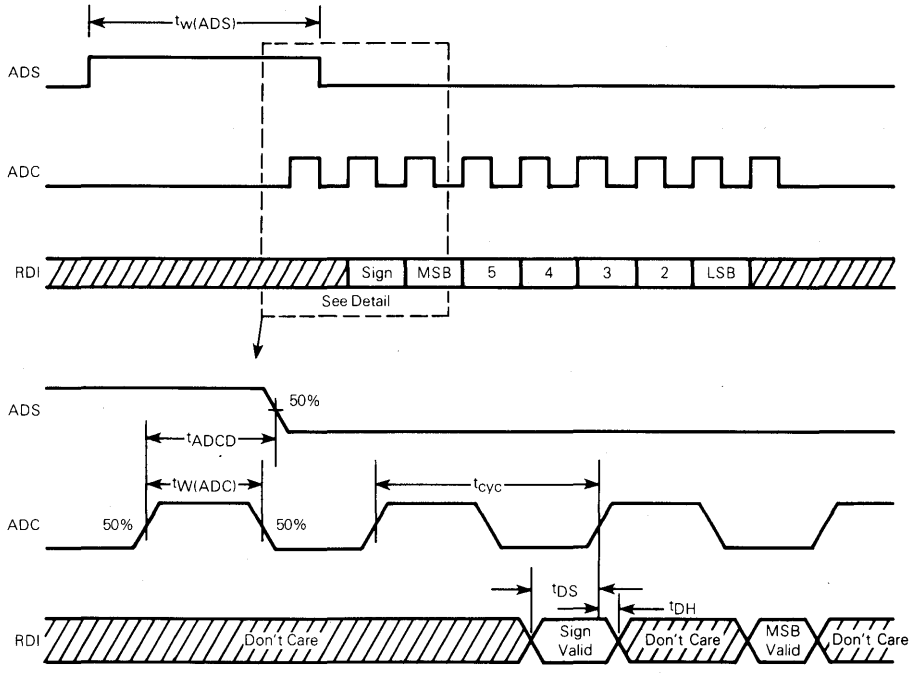
The positive transition of the Receive Clock, which occurs in the middle of the data bit, should be used to strobe data from the demodulator, under normal operating conditions. When $\overline{TPE}$ scrambler/descrambler is being incorporated, then the negative edge of the Rx Clk will occur in the center of the data bit.

Receive Clock will be 2400 bps or 1200 bps depending on the logic input at the DRS input. The Rx Clk edges described above apply to either 2400 bps or 1200 bps data rates.

Under $\overline{TPE}$ active, the Dibit relation to Rx Clk does not change. See Figure 9 for relative timing of Rx Clk, DBC and Rx Data.

Figure 10 depicts the requirements at the demodulator if the data scrambler is being incorporated. The exclusive Nor gating of $\overline{TPE}$ and Rx Clk would then maintain proper phasing of Rx Clk as it goes to the RS-232 driver. This circuit would be required since the positive edge of Receive Clock is a Data Communications Standard.

FIGURE 8 – ANALOG-TO-DIGITAL TIMING DIAGRAM



DATA RATE SELECT (DRS), Pin 24 – The following levels are valid for either phase-shift select:

Logic high equals 2400 bps,
Logic low equals 1200 bps.

PHASE-SHIFT SELECT (PSS), Pin 17 – Option A (CCITT) or option B (U.S.) phase shift can be selected for 2400 bps operation. The input data format and phase shift relationship for these two options are as follows:

Data	PSS = 0 Option A (Degrees)	PSS = 1 Option B (Degrees)
00	0	+45
01	+90	+135
11	+180	+225
10	+270	+315

For 1200 bps operation, option A (CCITT) or option B (U.S.) phase shift can be selected as follows:

Data	PSS = 0 Option A (Degrees)	PSS = 1 Option B (Degrees)
0	+90	+45
1	+270	+225

The phase shifts shown are the difference in phase between the signal at the end of one dibit period and the new signal at the beginning of the next dibit.

If the logic level inputs to PSS are EXORed with DBC (dibit clock) or $\overline{DBC}$, then the test-pattern enable option may be selected and produce the compliment of normal data at Rx Data as explained in the $\overline{TPE}$ description. (See Figure 11.)

$\overline{\text{TEST-PATTERN ENABLE}}$ ($\overline{TPE}$), Pin 18 – Incorporated in the demodulator is the 511-bit test pattern shift register that is in accord with CCITT specification V52. This is the pattern that is generated by feedback from the 5th and 9th stages of a 9-bit shift register.

When the $\overline{TPE}$ input is allowed to be pulled up internally, there is normal data flow through the receiver. When the $\overline{TPE}$ input is pulled low, the incoming data is passed through this self-synchronous decoder which will produce the inverse of the 511-bit CCITT V52 pattern.

$\overline{TPE}$ works in coordination with PSS. If PSS is directly pulled high or low to represent option A or option B, then the presence of the 511-test pattern at the (RDI) input and $\overline{TPE}$ active will result in logic "1" condition at Rx Data output. If the DBC option is being utilized at the PSS input and $\overline{TPE}$ is active while the 511-bit test pattern is being received, the receiver data output will equal a logic "0". These options (Figure 11) are summarized in Table 2.

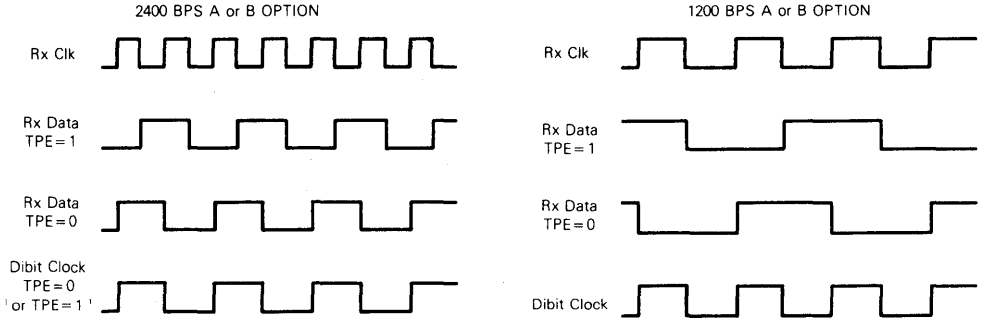
This assumes the modulator is sending the 511-bit test pattern with Rx Data being either a constant mark (logic "1") or space (logic "0"). If a logic "0" is received in options 1 or 2 or a logic "1" is received in options 3 or 4, then a transmission error has occurred. The number of errors-per-unit time is a measure of the transmission line quality.

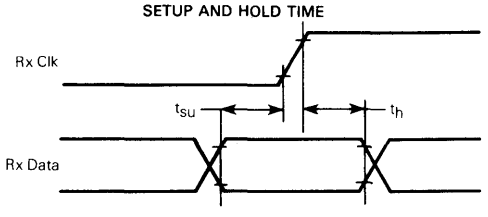
A feature of the above type of pattern detector is that it will be self-synchronizing. It should be pointed out that there will be at least two error counts each time an error is detected.

If the $\overline{TPE}$ input is in the active state, it is important to note that the Rx Clk phase changes. The necessary circuit to regain proper phase is shown in Figure 10.

A scheme for programming the phase-shift select is illustrated in Figure 11. The PSS input may either be a constant high or low level which will produce options 1 and 2. If the input "A" is exclusive ORed with the dibit clock, options 3 and 4 are produced at the same input pin.

FIGURE 9 — CLOCK TIMING DIAGRAM





Note: Timing measurements are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts, unless otherwise noted.

FIGURE 10 — DEMODULATOR DATA SCRAMBLER RECEIVE CLOCK PHASE CORRECTION REQUIREMENTS

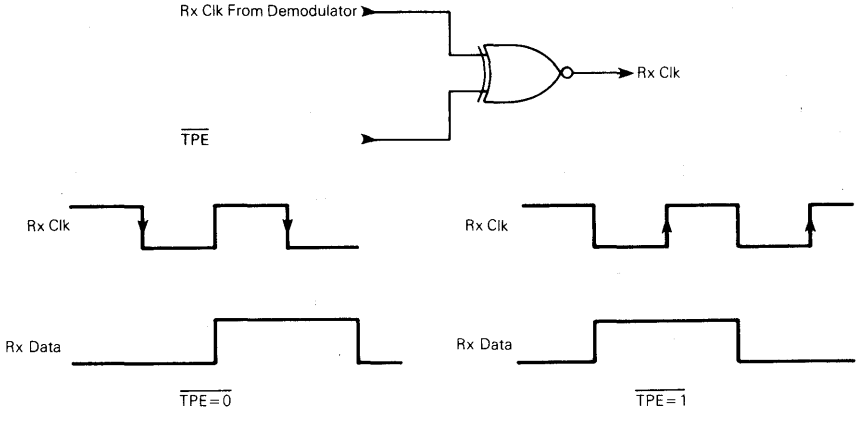


FIGURE 11 — PHASE-SHIFT SELECT DEMULTIPLEXER FOR TEST PATTERN ENABLE

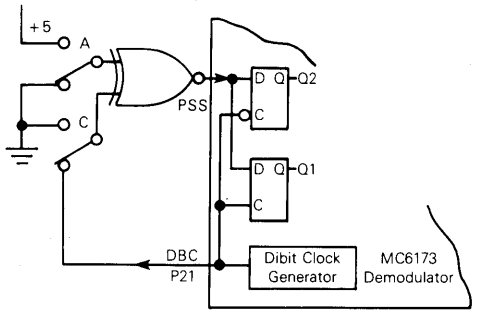


TABLE 2 — TEST PATTERN ENABLE OPTIONS

Option	$\overline{TPE}$	A	C	Phase Option	PSS	Output State
1	0	1	0	A	0	Rx Data Output = 1
2	0	0	0	B	1	Rx Data Output = 1
3	0	1	DBC	A	DBC	Rx Data Output = 0
4	0	0	DBC	B	$\overline{DBC}$	Rx Data Output = 0

CLOCK (Clk), Pin 14 — A 1.8432 MHz signal input ±0.005% is required at this port. The clock requirements are the same as the modulator clock specifications. See Figure 12 for a suggested clock circuit.

The receive clock is generated by dividing down the 1.8432 MHz. Since receive clock accuracy must be at least ±0.005%, the clock source must be of the same accuracy.

TEST-CLOCK (TClk), Pin 13 — This input is used for production testing of the demodulator device. In normal operation this pin should be left open which will enable the internal pullup resistor.

Pin 5	0 Degree Eye
Pin 4	90 Degree Eye
Pin 7	0 Degree Carrier
Pin 19	Carrier Correction

These test outputs are explained in the test enable ($\overline{TEN}$) description below.

$\overline{TEST}$ $\overline{ENABLE}$ ($\overline{TEn}$), Pin 16; 0° Eye, Pin 5; 90° Eye, Pin 4; 0° Car, Pin 7; CCor, Pin 19 — These pins allow the monitoring of ten internal points within the demodulator. A low level on $\overline{TEn}$ is normally associated with testing of the demodulator such as in a production test environment or incoming testing. Activation of $\overline{TEn}$ affects internal timing.

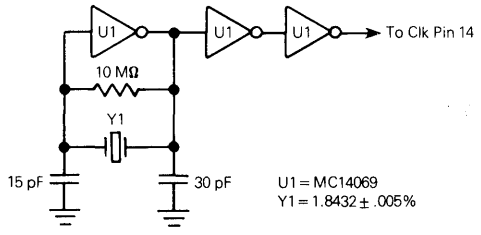
TABLE 3 — INTERNAL MONITORS

Output	$\overline{TEn}$	Function
ADS	H	See Description Under ADS (Pin 8)
(Pin 8)	L	Monitors Zero Crossings
ADC	H	See Description Under ADC (Pin 6)
(Pin 6)	L	Monitors Check Accumulator Output
0 Degree Eye	H	Monitors 0 Degree Eye 2s Complement Information from 6 Tap Filter
(Pin 5)	L	Monitors 0 Degree Eye 2s Complement Information from 12 Tap Filter
90 Degree Eye (Pin 4)	H	Monitors 90 Degree Eye 2s Complement Information from 12 Tap Filter
0°Car	H	Monitors 0 Degree Carrier
(Pin 7)	L	Monitors Check Accumulator Compare Errors
CCor	H	Monitors Carrier Correction Enable
(Pin 19)	L	Monitors Carrier Correction Direction

DIBIT CLOCK (DBC), Pin 21 — This output is a 1200 Hz clock which is derived from incoming data envelope and provides a dibit reference. This signal is representative of "data derived timing." When studying the quality of the demodulated signal, through the use of eye patterns, this output is necessary for proper synchronization of the oscilloscope.

$\overline{TEST}$ $\overline{STROBE}$ ($\overline{TStr}$), Pin 22 — This input is used to facilitate testing of the demodulator during the manufacturing process. It should be left unconnected which will result in

FIGURE 12 – OSCILLATOR CONFIGURATION



the internal pullup resistor causing the high level on this pin.

V_{SS} Pin 1 = The most negative supply, typically ground.

V_{CC} Pin 12 = The most positive supply, typically 5 volts.

DATA SCRAMBLER

The scrambling of data in the data communication environment is not done in an attempt to encrypt information in the normal sense of the word. Rather, the purpose of the scrambling of data is to guarantee that, with respect to the modem carrier, there is always random data on the line with little chance for a long string of "1s" or "0s" to exist. This is particularly important if an adaptive equalizer is being incorporated in the modem as the adaptive equalizer will require reasonably evenly distributed data to optimize its statistical response to the incoming signal. The normally used code is the CCITT 511 sequence which is EXORed with data.

The Motorola 2400 bps modulator contains a CCITT 511-bit test-pattern generator. It does not, however, incorporate the 511 data randomizer or scrambler. To scramble data using the MC6172 modulator, the circuit in Figure 10 must precede the Tx Data input of the modulator. Tx Data is added to the scrambler output pattern; then, the data is delayed by a full data bit before being transmitted by the modem. This assures a proper transmit-data/transmit-clock phase relationship. If the data scrambler is to be an optional feature, then the transmit-data multiplexer would also have to be built. This is selected by the test-pattern enable signal or any other signal that is found suitable.

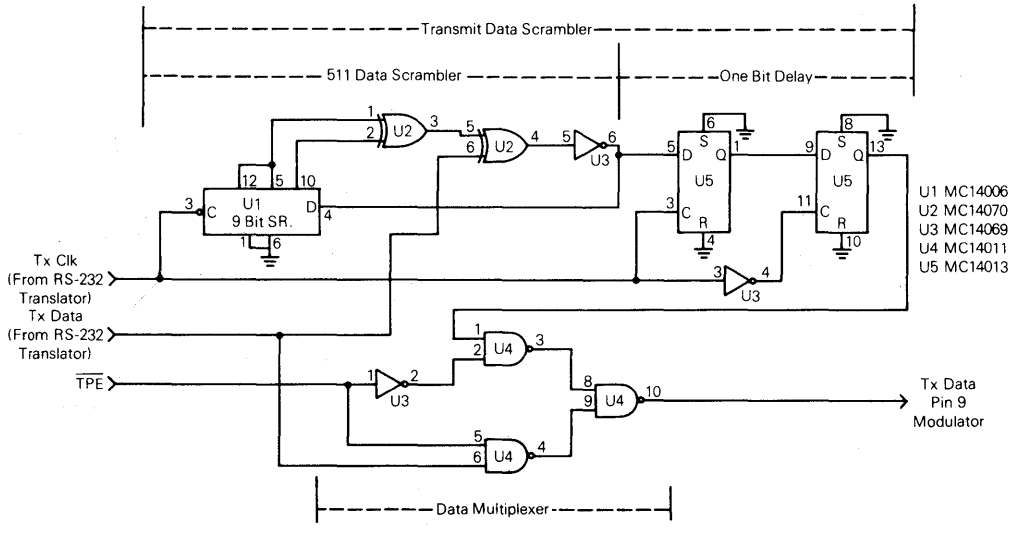
The demodulator does contain a built-in data descrambler which is enabled by the $\overline{TPE}$ input going active. The receive phasing, with respect to data, changes when $\overline{TPE}$ goes active. The exclusive NOR gating of $\overline{TPE}$ and Rx Clk, as shown in Figure 10 will maintain proper phase of Rx Clk. This circuit is required since the clocking of data on a positive edge is a data communications standard.

EYE PATTERN

When performing an evaluation of an 2400 bps modem, one common point of comparison is the quality of the eye patterns produced by the demodulator. The eye pattern may also be used as an indicator of the incoming signal with respect to level and line perturbations. Eye patterns are for test and evaluation only and are not used in the demodulation of the incoming signal.

Timing information in the Motorola 2400 bps demodulator is derived directly from the demodulated data signal. This is referred to as data derived timing. The advantage of data

FIGURE 13 – MODULATOR CCITT 511 DATA SCRAMBLER

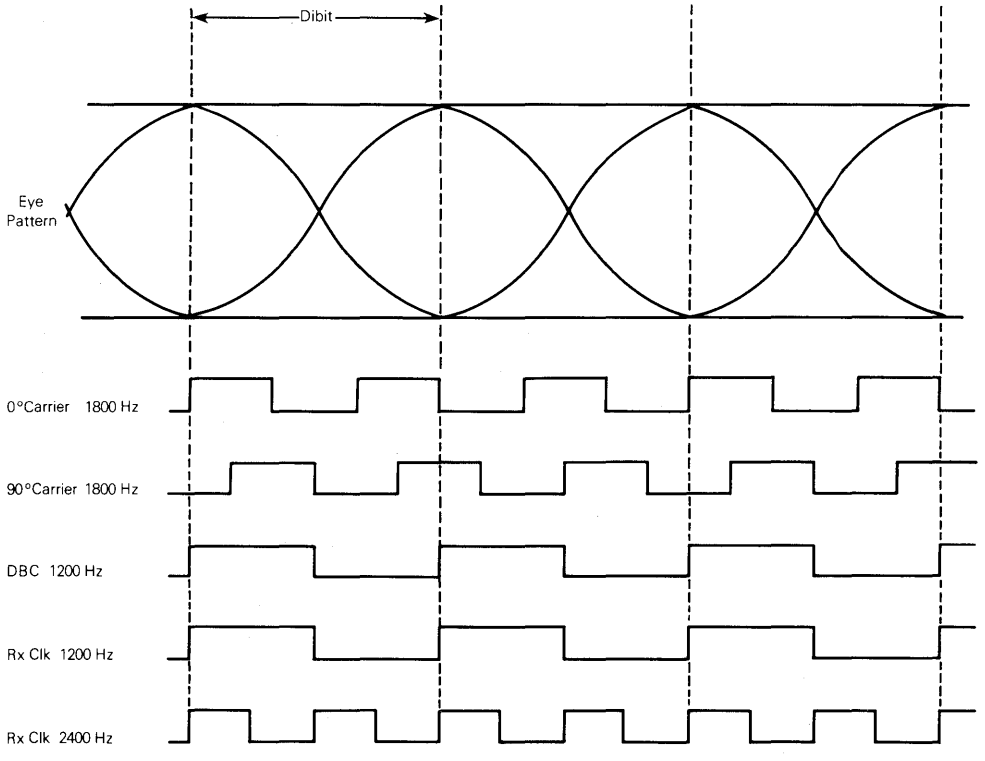


derived time is that it allows data to be sampled at optimum times. The demodulated signals, in differential phase-shift keying, take the form of "eye patterns" as shown in Figure 14. The demodulator, in optimizing its performance for minimum error rates, strobes data at the point of maximum eye opening. The demodulator constantly examines the eye opening to assure that the data sample is being taken at exactly the optimum point. As a result of constantly adjusting timing control, correct sampling is maintained. This technique provides improvements in reception that are significant, especially in a poor communications media environment.

The circuit in Figure 16 is required to observe the eye patterns. This circuit was built using Motorola CMOS devices. The 0 and 90 degree eye data is strobed from pins 4 and 5, respectively, into the shift register by the A/D clock. The A/D strobe then latches the data sample into the "D" type storage devices. The output of the storage devices taken across the scaled resistors will then represent the appropriate value of the sample taken. To properly observe the actual eye patterns, it is necessary to Sync on dibit clock while observing the 0 to 90 degree eye data. Overlaying the two patterns produces a two-level digital-eye pattern from which the quality of the incoming signal may be judged.

Figures 15 thru 17 show a typical receive/demodulator and transmit/modulator circuit, respectively. The transmit filter illustrated in Figure 17 limits the bandwidth of the signal to those frequencies allowed on a telephone line. The receive filter and equalizer in Figure 15 clean up and normalize the incoming signal for the A/D network, 1200 Hz envelope detector, and 1800 Hz carrier detector.

FIGURE 14 — EYE PATTERN



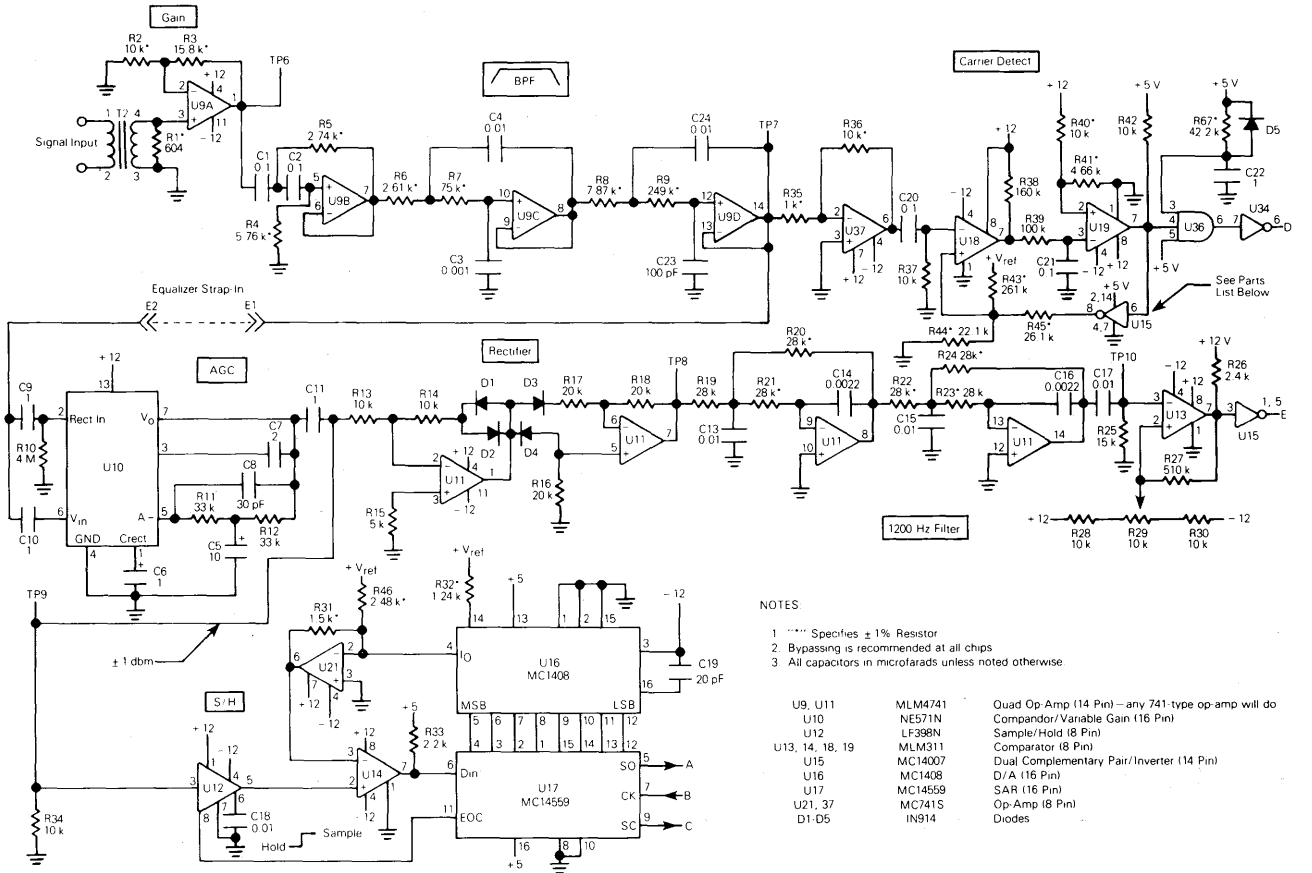
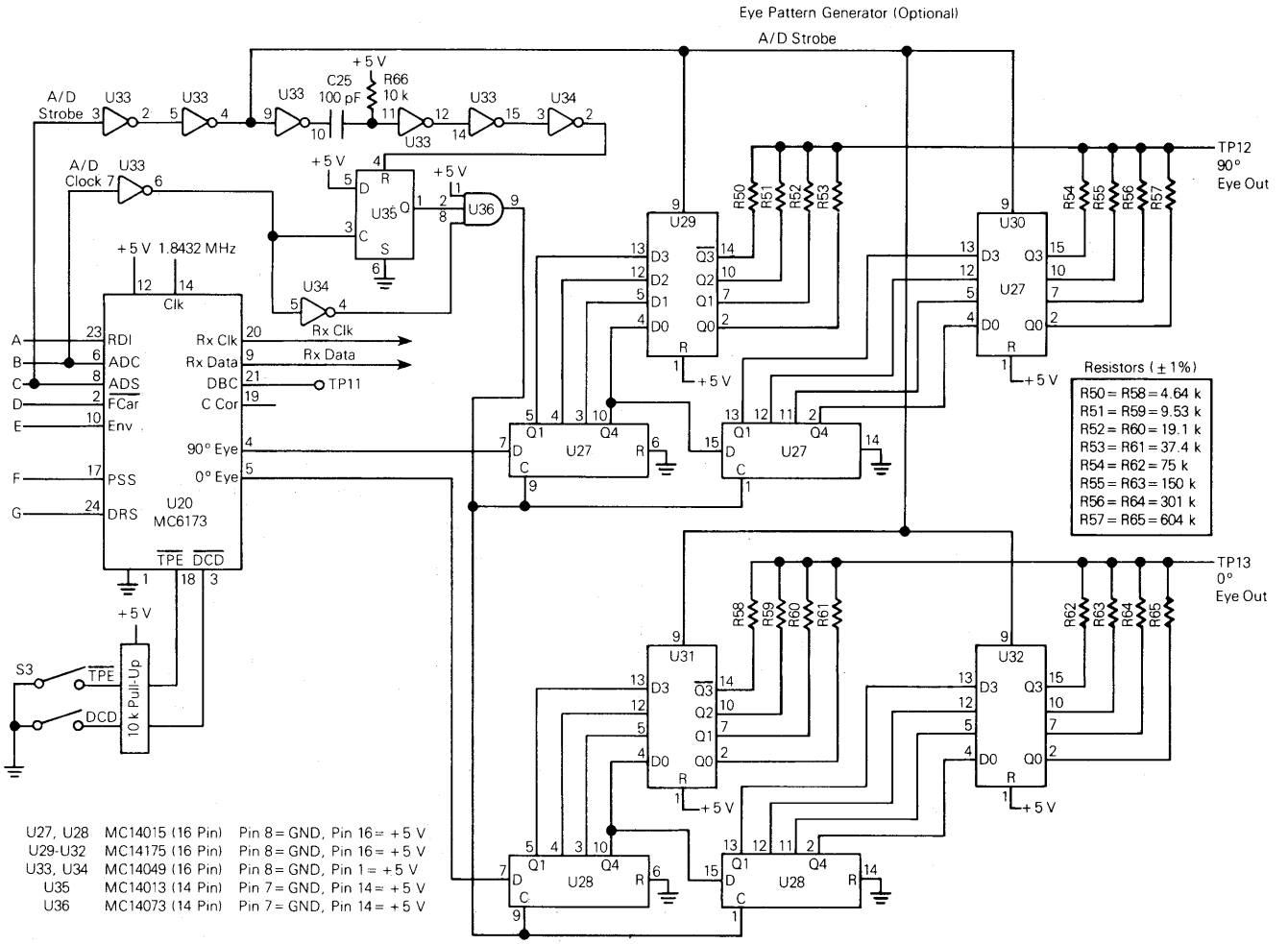
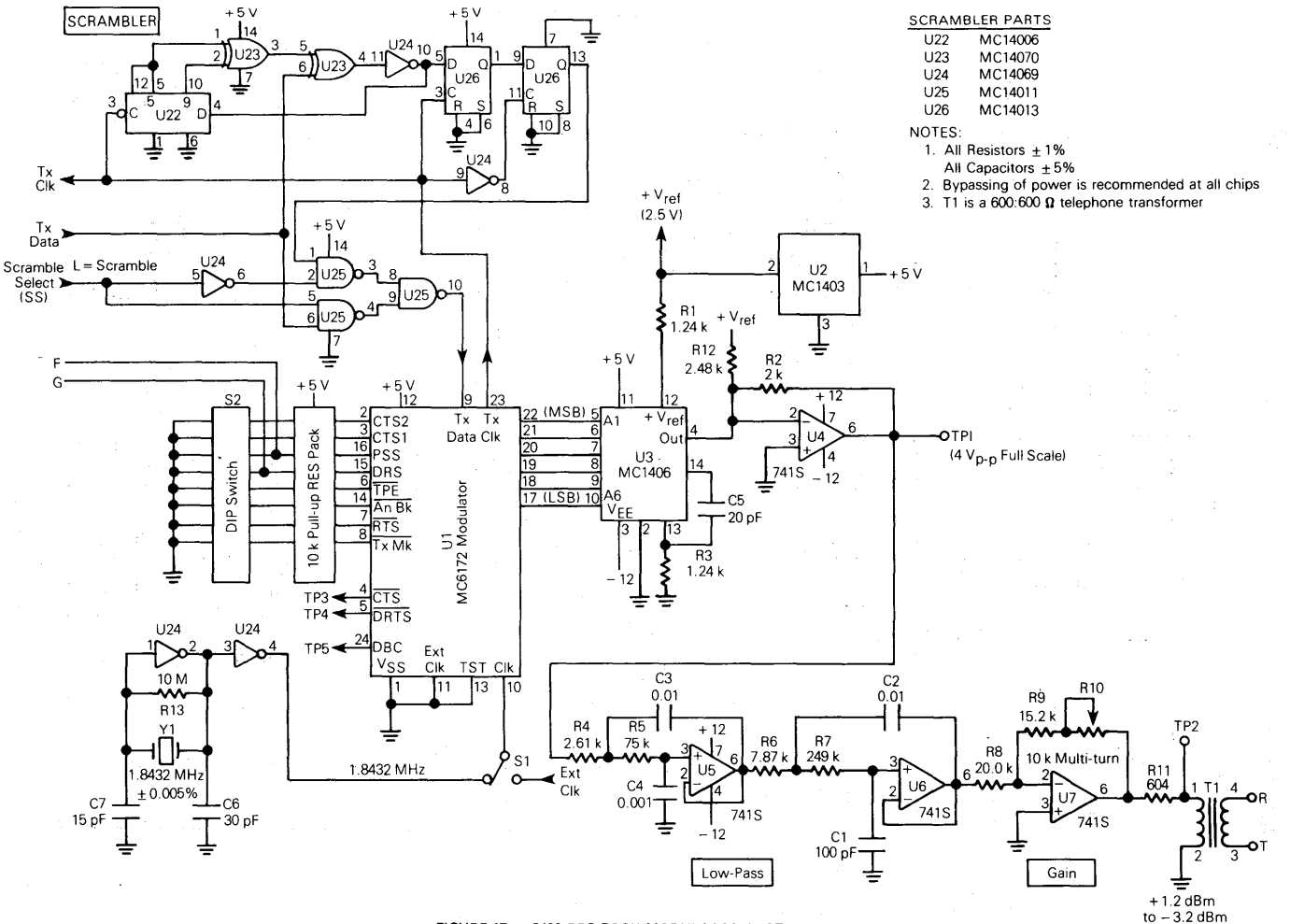


FIGURE 15 – 2400 BPS DPSK DEMODULATOR SYSTEM



U27, U28	MC14015 (16 Pin)	Pin 8 = GND, Pin 16 = +5 V
U29-U32	MC14175 (16 Pin)	Pin 8 = GND, Pin 16 = +5 V
U33, U34	MC14049 (16 Pin)	Pin 8 = GND, Pin 1 = +5 V
U35	MC14013 (14 Pin)	Pin 7 = GND, Pin 14 = +5 V
U36	MC14073 (14 Pin)	Pin 7 = GND, Pin 14 = +5 V

FIGURE 16 — 2400 BPS DPSK DEMODULATOR SYSTEM



SCRAMBLER PARTS

U22	MC14006
U23	MC14070
U24	MC14069
U25	MC14011
U26	MC14013

NOTES:
1. All Resistors ±1%
   All Capacitors ±5%
2. Bypassing of power is recommended at all chips
3. T1 is a 600:600 Ω telephone transformer

FIGURE 17 — 2400 BPS DPSK MODULATOR SYSTEM

MOTOROLA

MC6860

0-600 bps DIGITAL MODEM

The MC6860 is a MOS subsystem designed to be integrated into a wide range of equipment utilizing serial data communications.

The modem provides the necessary modulation, demodulation and supervisory control functions to implement a serial data communications link, over a voice grade channel, utilizing frequency shift keying (FSK) at bit rates up to 600 bps. The MC6860 can be implemented into a wide range of data handling systems, including stand alone modems, data storage devices, remote data communication terminals and I/O interfaces for minicomputers.

N-channel silicon-gate technology permits the MC6860 to operate using a single-voltage supply and be fully TTL compatible.

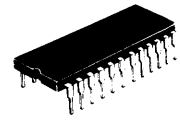
The modem is compatible with the M6800 microcomputer family, interfacing directly with the Asynchronous Communications Interface Adapter to provide low-speed data communications capability.

- Originate and Answer Mode
- Crystal or External Reference Control
- Modem Self Test
- Terminal Interfaces TTL-Compatible
- Full-Duplex or Half-Duplex Operation
- Automatic Answer and Disconnect
- Compatible Functions for 100 Series Data Sets
- Compatible Functions for 1001A/B Data Couplers

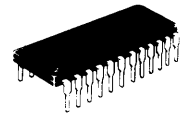
MOS

(N-CHANNEL, SILICON-GATE)

0-600 bps
DIGITAL MODEM

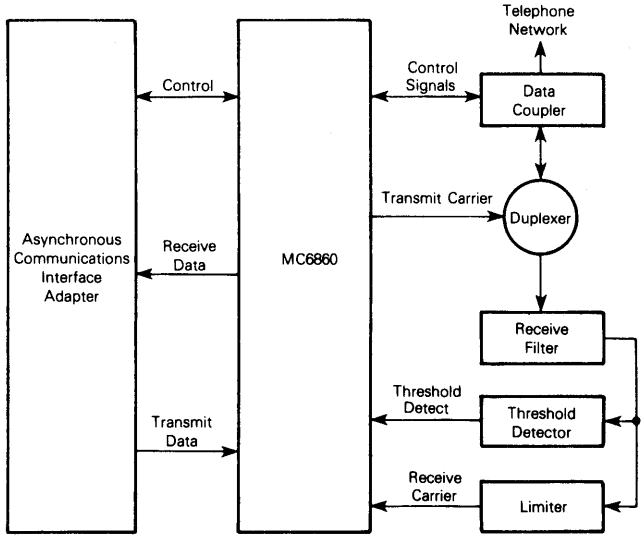


L SUFFIX
CERAMIC PACKAGE
CASE 623

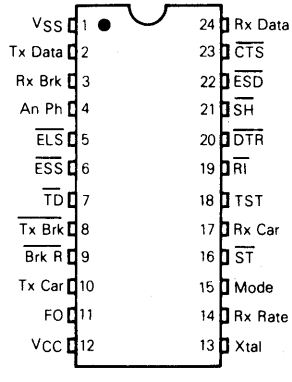


P SUFFIX
PLASTIC PACKAGE
CASE 709

FIGURE 1 — TYPICAL MC6860 SYSTEM CONFIGURATION



PIN ASSIGNMENT



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	V
Input Voltage	V_{in}	−0.3 to +7.0	V
Operating Temperature Range	T_A	0 to 70	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	Value	Unit
Thermal Resistance Ceramic Plastic	θ_{JA}	 65 120	°C/W

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{CC}).

POWER CONSIDERATIONS

The average chip-junction temperature, T_J, in °C can be obtained from:

$$T_J = T_A + (P_D \bullet \theta_{JA}) \quad (1)$$

Where:

T_A ≡ Ambient Temperature, °C

θ_{JA} ≡ Package Thermal Resistance, Junction-to-Ambient, °C/W

$P_D \equiv P_{INT} + P_{PORT}$

$P_{INT} \equiv i_{CC} \times V_{CC}$, Watts — Chip Internal Power

P_{PORT} ≡ Port Power Dissipation, Watts — User Determined

For most applications $P_{PORT} \ll P_{INT}$ and can be neglected. P_{PORT} may become significant if the device is configured to drive Darlington bases or sink LED loads.

An approximate relationship between P_D and T_J (if P_{PORT} is neglected) is:

$$P_D = K \div (T_J + 273°C) \quad (2)$$

Solving equations 1 and 2 for K gives:

$$K = P_D \bullet (T_A + 273°C) + \theta_{JA} \bullet P_D^2 \quad (3)$$

Where K is a constant pertaining to the particular part. K can be determined from equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

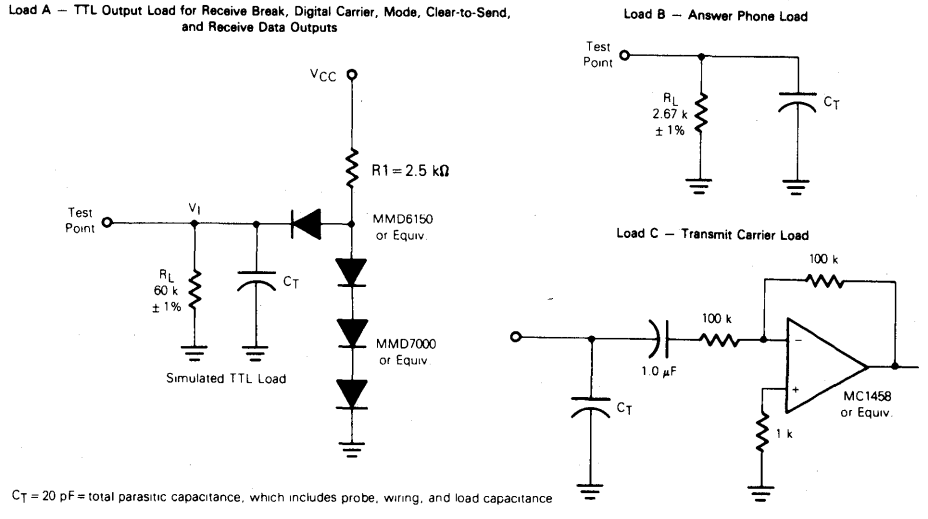
DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0 ±5% Vdc, all voltages referenced to V_{SS} = 0, $T_A = T_L$ to T_H, all outputs loaded as shown in Figure 2 unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input High Voltage, All Inputs Except Crystal	V_{IH}	2.0	–	V_{CC}	V
Input Low Voltage, All Inputs Except Crystal	V_{IL}	V_{SS}	–	0.80	V
Crystal Input Voltage (Crystal Input Driven from an External Reference, Input Coupling Capacitor = 200 pF, Duty Cycle = 50 ± 5%)	V_{in}	1.5	–	2.0	V_{p-p}
Input Current ($V_{in} = V_{SS}$) All Inputs Except Rx Car, Tx Data, $\overline{TD}$, $\overline{TST}$, $\overline{RI}$, $\overline{SH}$	I_{in}	–	–	−0.2	mA
$\overline{RI}$, $\overline{SH}$ Inputs		–	–	−1.6	
Input Leakage Current (V_{in} = 7.0 V, $V_{CC} = V_{SS}$, T_A = 25°C)	I_{IL}	–	–	1.0	μA
Output High Voltage, All Outputs Except An Ph and Tx Car (I_{OH1} = −0.04 mA, Load A)	V_{OH1}	2.4	–	V_{CC}	V
Output Low Voltage, All Outputs Except An Ph and Tx Car (I_{OL1} = 1.6 mA, Load A)	V_{OL1}	V_{SS}	–	0.40	V
Output High Current, An Ph (V_{OH2} = 0.8 V, Load B)	I_{OH2}	0.30	–	–	mA
Output Low Voltage, An Ph (I_{OL2} = 0, Load B)	V_{OL2}	V_{SS}	–	0.30	V
Input Capacitance (f = 0.1 MHz, T_A = 25°C)	C_{in}	–	5.0	–	pF
Output Capacitance (f = 0.1 MHz, T_A = 25°C)	C_{out}	–	10	–	pF
Transmit Carrier Output Voltage (Load C)	V_{CO}	0.20	0.35	0.50	V(RMS)
Transmit Carrier Output 2nd Harmonic (Load C)	V_{2H}	−25	−32	–	dB
Input Transition Times, All Inputs Except Crystal (Operating in the Crystal Input Mode; from 10% to 90% Points)	t_r	–	–	1.0*	μs
	t_f	–	–	1.0*	
Input Transition Times, Crystal Input (Operating in External Input Reference Mode)	t_r	–	–	30	ns
	t_f	–	–	30	
Output Transition Times, All Outputs Except Tx Car (From 10% to 90% Points)	t_r	–	–	5.0	μs
	t_f	–	–	5.0	
Internal Power Dissipation (All Inputs at V_{SS} and All Outputs Open) (Measured at $T_A = T_L$)	P_{INT}	–	–	340	mW

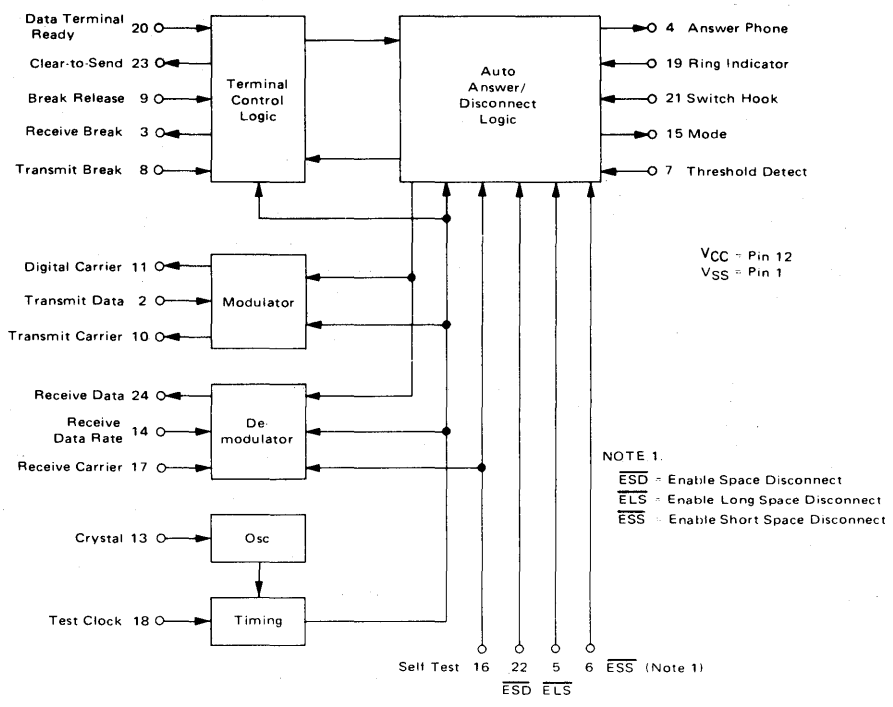
*Maximum Input Transition Times are ≤ 0.1 × Pulse Width or the specified maximum of 1.0 μs, whichever is smaller.

FIGURE 2 — OUTPUT TEST LOADS



CT = 20 pF = total parasitic capacitance, which includes probe, wiring, and load capacitance

FIGURE 3 — BLOCK DIAGRAM



DEVICE OPERATION*

GENERAL

Figure 1 shows the modem and its interconnections. The data to be transmitted is presented in serial format to the modulator for conversion to FSK signals for transmission on the telephone line (refer to Figure 3). The modulator output is buffered before driving the line.

The FSK signal from the remote modem is received via the telephone line and filtered to remove extraneous signals such as the local Transmit Carrier. This filtering can be either a bandpass which passes only the desired band of frequencies or a notch which rejects the known interfering signal. The desired signal is then limited to preserve the axis crossings and fed to the demodulator where the data is recovered from the received FSK carrier.

The Supervisory Control provides the necessary commands and responses for handshaking with the remote modem, along with the interface signals to the data coupler and communication terminal. If the modem is a built-in unit, all input-output (I/O) logic need not be RS-232 compatible. The use of MC1488 and MC1489A line drivers and receivers will provide a RS-232 interface conforming to the EIA specification.

ANSWER MODE

Automatic answering is first initiated by a receipt of a Ring Indicator ($\overline{RI}$) signal. This can be either a low level for at least 51 ms as would come from a CBS data coupler, or at least 20 cycles of a 20-47 Hz ringing singal (low level ≥ 50% of the duty cycle) as would come from a CBT data coupler. The presence of the Ring Indicator signal places the modem in the Answer Mode; if the Data Terminal Ready line is low, indicating the communication terminal is ready to send or receive data, the Answer Phone output goes high. This output is designed to drive a transistor switch which will activate

*See Tables 1 and 2 for delay time tolerances.

the Off Hook (OH) and Data Transmission (DA) relays in the data coupler. Upon answering the phone the 2225-Hz Transmit Carrier is turned on.

The originate modem at the other end detects this 2225-Hz signal and after a 450 ms delay (used to disable any echo suppressors in the telephone network) transmits a 1270-Hz signal which the local answering modem detects, provided the amplitude and frequency requirements are met. The amplitude threshold is set external to the modem chip. If the signal level is sufficient the $\overline{TD}$ input should be low for 20 μs at least once every 32 ms. The absence of a threshold indication for a period greater than 51 ms denotes the loss of Receive Carrier and the modem begins hang-up procedures. Hang-up will occur 17 s after $\overline{RI}$ has been released provided the handshaking routine is not re-established. The frequeny tolerance during handshaking is $\pm$ 100 Hz from the Mark frequency.

After the 1270-Hz signal has been received for 150 ms, the Receive Data is unclamped from a Mark condition and data can be received. The Clear-to-Send output goes low 450 ms after the receipt of carrier and data presented to the answer modem is transmitted. Refer to Figure 4.

AUTOMATIC DISCONNECT

Upon receipt of a space of 150 ms or greater duration, the modem clamps the Receive Break high. This condition exists until a Break Release command is issued at the receiving station. Upon receipt of a 0.3 s space, with Enable Short Space Disconnect at the most negative voltage (low), the modem automatically hangs up. If Enable Long Space Disconnect is low, the modem requires 1.5 s of continuous space to hang up. Refer to Figure 5.

ORIGINATE MODE

Upon receipt of a Switch Hook ($\overline{SH}$) command the modem function is placed in the Originate Mode. If the Data Terminal Ready input is enabled (low) the modem will provide a logic high output at Answer Phone. The modem is now ready to receive the 2225-Hz signal from the remote answering modem. It will continue to look for this signal until 17 s after $\overline{SH}$ has been released. Disconnect occurs if the handshaking routine is not established.

Upon receiving 2225 $\pm$ 100 Hz for 150 ms at an acceptable amplitude, the receive Data output is unclamped from a Mark condition and data reception can be accomplished. 450 ms after receiving a 2225-Hz signal, a 1270-Hz signal is transmitted to the remote modem. 750 ms after receiving the 2225-Hz signal, the Clear-to-Send output is taken low and data can now be transmitted as well as received. Refer to Figure 6.

INITIATE DISCONNECT

In order to command the remote modem to automatically hang up, a disconnect signal is sent by the local modem. This is accomplished by pulsing the normally low Data Terminal Ready into a high state for greater than 34 ms. The local modem then sends a 3 s continuous space and hangs up provided the Enable Space Disconnect is low. If the remote modem hangs up before 3 s, loss of Threshold Detect will cause loss of Clear-to-Send, which marks the line in Answer Mode and turns the carrier off in the Originate Mode.

If $\overline{ESD}$ is high the modem will transmit data until hang-up occurs 3 s later. Receive Break is clamped 150 ms following the Data Terminal Ready interrupt. Refer to Figure 7.

INPUT/OUTPUT FUNCTIONS

Figure 8 shows the I/O interface for the low speed modem. The following is a description of each individual signal:

Receiver Carrier (Rx Car)

The Receive Carrier is the FSK input to the demodulator. The local Transmit Carrier must be balanced or filtered out and the remaining signal hard limited. The conditioned receive carrier is measured by the MC6860. Any half-cycle period greater than or equal to 429 $\pm$ 1.0 μs for the low band or 235 $\pm$ 1.0 μs for the high band is detected as a space. Resultant peak phase jitter is as follows:

Data Rate Bits per Second	Answer Mode ϕ_J (Peak %)	Originate Mode ϕ_J (Peak %)
300	7.0	3.7
200	4.7	2.5
150	3.5	1.8
110	2.6	1.4

Ring Indicator ($\overline{RI}$)

The modem function will recognize the receipt of a call from the CBT data coupler if at least 20 cycles of the 20-47 Hz ringing singal (low level $\geq$ 50% of the duty cycle) are present. The CBS data coupler $\overline{RI}$ signal must be level-converted to TTL according to the EIA RS-232 specification before interfacing it with the modem function. The receipt of a call from the CBS data coupler is recognized if the $\overline{RI}$ signal is present for at least 51 ms. This input is held high except during ringing. An $\overline{RI}$ signal automatically places the modem function in the Answer Mode.

Switch Hook ($\overline{SH}$)

$\overline{SH}$ interfaces directly with the CBT data coupler and via the EIA RS-232 level conversion for the CBS data coupler. An $\overline{SH}$ signal automatically places the modem function in the Originate Mode.

$\overline{SH}$ is low during origination of a call. The modem will automatically hang up 17 s after releasing $\overline{SH}$ if the handshaking routine has not been accomplished.

Threshold Detect ($\overline{TD}$)

This input is derived from an external threshold detector. If the signal level is sufficient, the $\overline{TD}$ input must be low for 20 μs at least once every 32 ms to maintain normal operation. An insufficient signal level indicates the absence of the Receive Carrier; an absence for less than 32 ms will not cause channel establishment to be lost; however, data during this interval will be invalid.

If the signal is present and the level is acceptable at all times, then the threshold input can be low permanently.

Loss of threshold for 51 ms or longer results in a loss of Clear-to-Send. The Transmit Carrier of the originate modem is clamped off and a constant Mark is transmitted from the answer modem.

TIMING DIAGRAMS

FIGURE 4 — ANSWER MODE

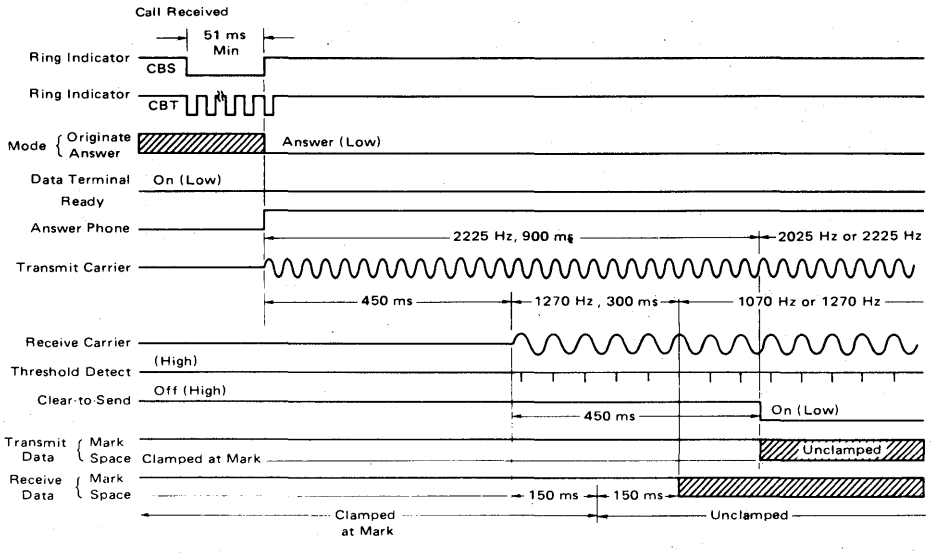


FIGURE 5 — AUTOMATIC DISCONNECT — LONG OR SHORT SPACE

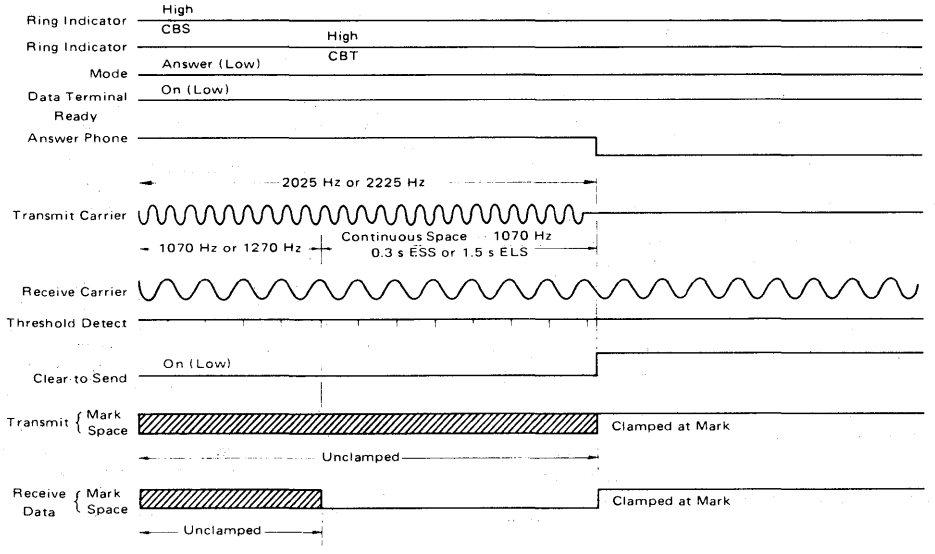


FIGURE 6 — ORIGINATE MODE

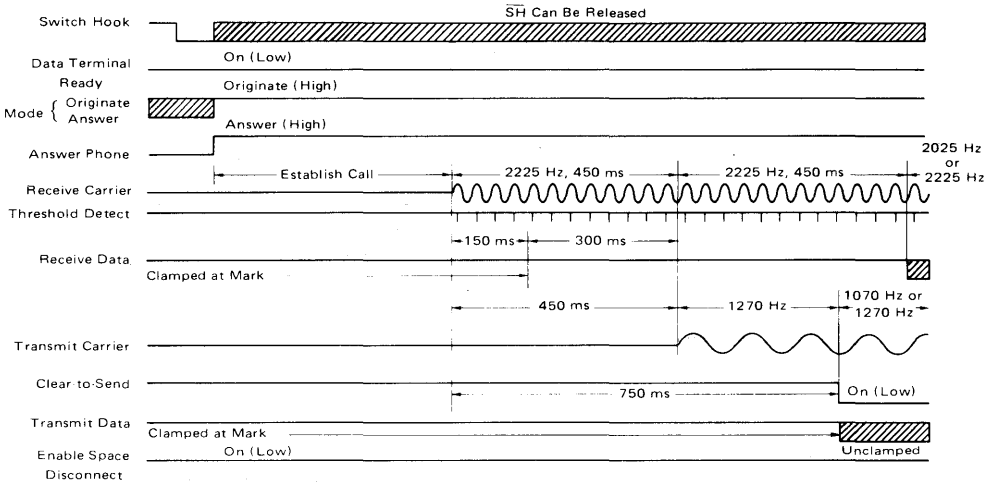
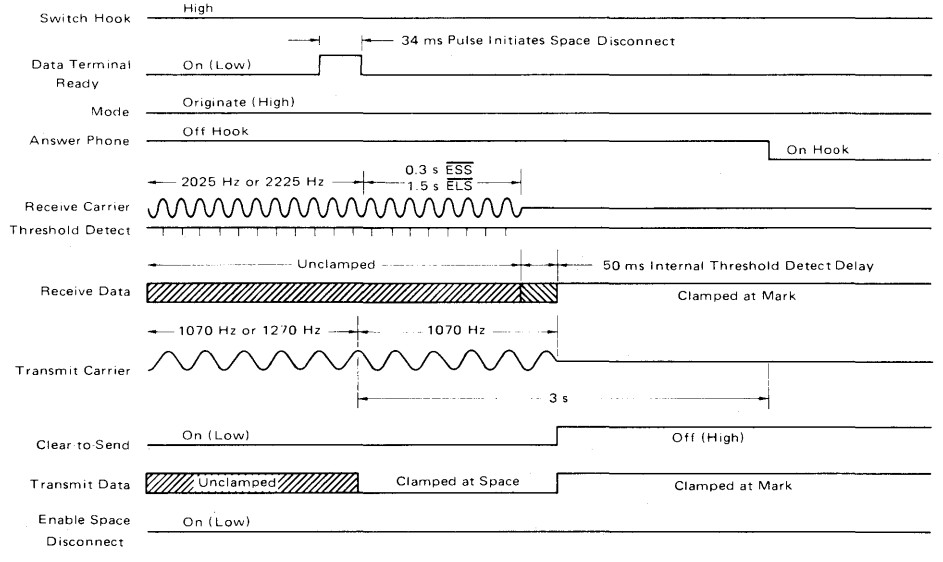


FIGURE 7 — INITIATE DISCONNECT



Receive Data Rate (Rx Rate)

The demodulator has been optimized for signal-to-noise performance at 300 bps and 600 bps. The Receive Data Rate input must be low for 0-600 bps and should be high for 0-300 bps.

Transmit Data (Tx Data)

Transmit Data is the binary information presented to the modem function for modulation with FSK techniques. A high level represents a Mark.

Data Terminal Ready ($\overline{DTR}$)

The Data Terminal Ready signal must be low before the modem function will be enabled. To initiate a disconnect, $\overline{DTR}$ is held high for 34 ms minimum. A disconnect will occur 3 s later.

Break Release ($\overline{Brk\ R}$)

After receiving a 150 ms space signal, the clamped high condition of the Receive Break output can be removed by holding Break Release low for at least 20 μs.

Transmit Break ($\overline{Tx\ Brk}$)

The Break command is used to signal the remote modem to stop sending data.

A Transmit Break (low) greater than 34 ms forces the modem to send a continuous space signal for 233 ms. Transmit Break must be initiated only after $\overline{CTS}$ has been established. This is a negative edge sense input. Prior to initiating $\overline{Tx\ Brk}$, this input must be held high for a minimum of 34 ms.

Enabled Space Disconnect ($\overline{ESD}$)

When $\overline{ESD}$ is strapped low and $\overline{DTR}$ is pulsed to initiate a disconnect, the modem transmits a space for either 3 s or until a loss of threshold is detected, whichever occurs first. If $\overline{ESD}$ is strapped high, data instead of a space is transmitted. A disconnect occurs at the end of 3 s.

Enable Short Space Disconnect ($\overline{ESS}$)

$\overline{ESS}$ is a strapping option which, when low, will automatically hang up the phone upon receipt of a continuous space for 0.3 s. *$\overline{ESS}$ and $\overline{ELS}$ must not be simultaneously strapped low.*

Enable Long Space Disconnect ($\overline{ELS}$)

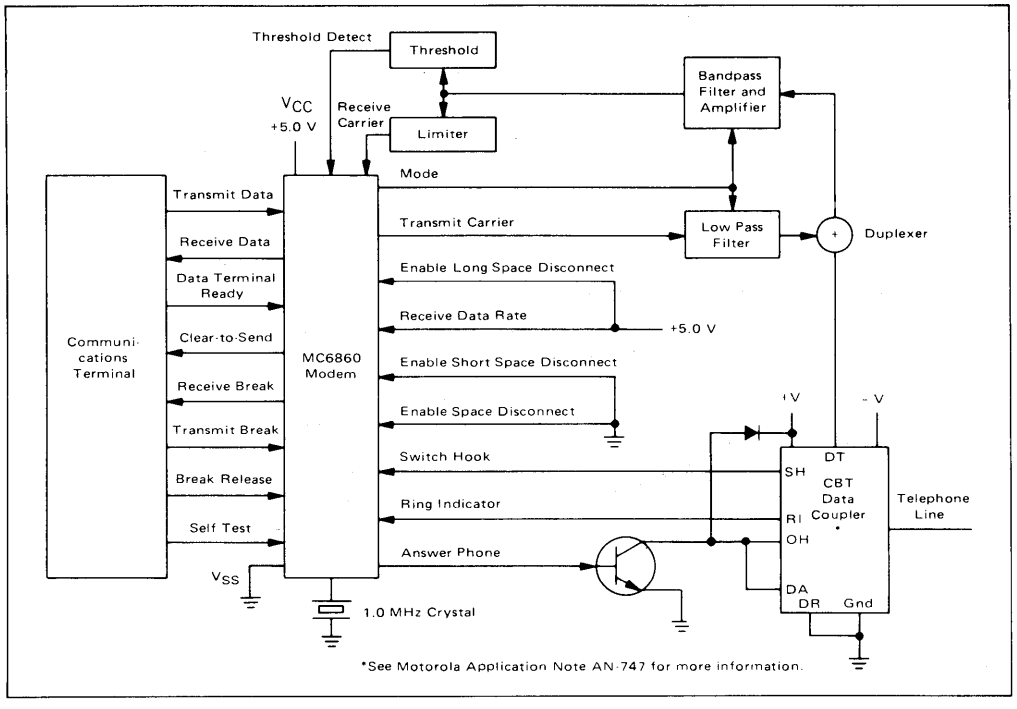
$\overline{ELS}$ is a strapping option which, when low, will automatically hang up the phone upon receipt of a continuous space for 1.5 s.

Crystal (Xtal)

A 1.0 MHz crystal with the following parameters is required to utilize the on-chip oscillator. A 1.0-MHz square wave can also be fed into this input to satisfy the clock requirement.

Mode:	Parallel
Frequency:	1.0 MHz ±0.1%
Series Resistance:	750 ohms max
Shunt Capacitance:	7.0 pF max
Temperature:	0-70°C
Test Level:	1.0 mW
Load Capacitance:	13 pF

FIGURE 8 — I/O INTERFACE CONNECTIONS FOR MC6860 (ORIGINATE/ANSWER MODEM)



When utilizing the 1.0 MHz crystal, external parasitic capacitance, including crystal shunt capacitance, must be ≤9 pF at the crystal input. Reliable crystal oscillator start-up requires that the V_{CC} power-on transition time be >15 milliseconds.

Test Clock (TST)

A test signal input is provided to decrease the test time of the chip. In normal operation this input *must be strapped low.*

Self Test ($\overline{ST}$)

When a low voltage level is placed on this input, the demodulator is switched to the modulator frequency and demodulates the transmitted FSK signal. Channel establishement, which occurred during the initial handshake, is not lost during self test. The Mode Control ouput changes state during Self Test, permitting the receive filters to pass the local Transmit Carrier.

$\overline{ST}$	$\overline{SH}$	$\overline{RI}$	Mode
H	⊓*	H	H
H	H	L	L
L	⊓*	H	L
L	H	L	H

*Note maximum $\overline{SH}$ low time in Table 1.

Answer Phone (An Ph)

Upon receipt of Ring Indicator or Switch Hook signal and Data Terminal Ready, the Answer Phone output goes high [$(\overline{SH}+\overline{RI})\cdot\overline{DTR}$]. This signal drives the base of a transistor which activates the Off Hook, and Data Transmission control lines in the data coupler. Upon call completion, the Answer Phone signal returns to a low level.

Mode

The Mode output indicates the Answer (low) or Originate (high) status of the modem. This output changes state when a Self Test command is applied.

Clear-To-Send ($\overline{CTS}$)

A low on the $\overline{CTS}$ output indicates the Transmit Data input has been unclamped from a steady Mark, thus allowing data transmission.

Receive Data (Rx Data)

The Receive Data output is the data resulting from demodulating the Receive Carrier. A Mark is a high level.

Receive Break (Rx Brk)

Upon receipt of a continuous 150 ms space, the modem automatically clamps the Receive Break output high. This output is also clamped high until Clear-to-Send is established.

Digital Carrier (FO)

A test signal output is provided to decrease the chip test time. The signal is a square wave at the transmit frequency.

Transmit Carrier (Tx Car)

The Transmit Carrier is a digitally-synthesized sine wave (Figure 9) derived from the 1.0 MHz crystal reference. The frequency characteristics are as follows:

Mode	Data	Transmit Frequency	Tolerance*
Originate	Mark	1270 Hz	−0.15 Hz
Originate	Space	1070 Hz	0.90 Hz
Answer	Mark	2225 Hz	−0.31 Hz
Answer	Space	2025 Hz	−0.71 Hz

*The reference frequency tolerance is not included.

The proper output frequency is transmitted within 3.0 μs following a data bit change with no more than 2.0 μs phase discontinuity. The typical output level is 0.35 V (RMS) into 100 k ohm load impedance.

The second harmonic is typically 32 dB below the fundamental (see Figure 10).

POWER-ON RESET

Power-on reset is provided on-chip to insure that when power is first applied the Answer Phone output is in the low (inactive) state. This holds the modem in the inactive or idle mode until a $\overline{SH}$ or $\overline{RI}$ signal has been applied. Once power has been applied, a momentary loss of power at a later time may not be of sufficient time to guarantee a chip reset through the power-on reset circuit.

To insure initial power-on reset action, the external parasitic capacitance on $\overline{RI}$ and $\overline{SH}$ should be <30 pF. Capacitance values >30 pF may require the use of an external pullup resistor to V_{CC} on these inputs in addition to the pullup devices already provided on chip.

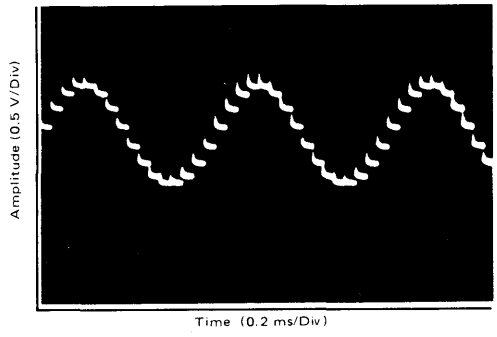


FIGURE 9 — TRANSMIT CARRIER SINE WAVE

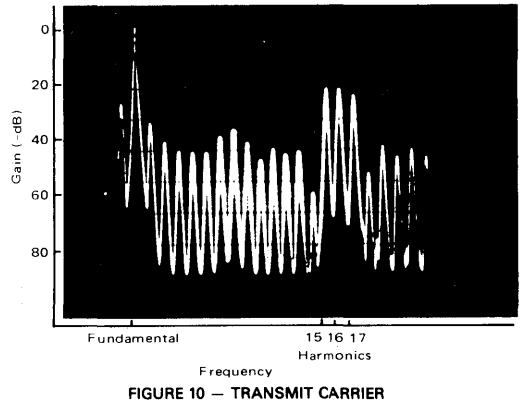


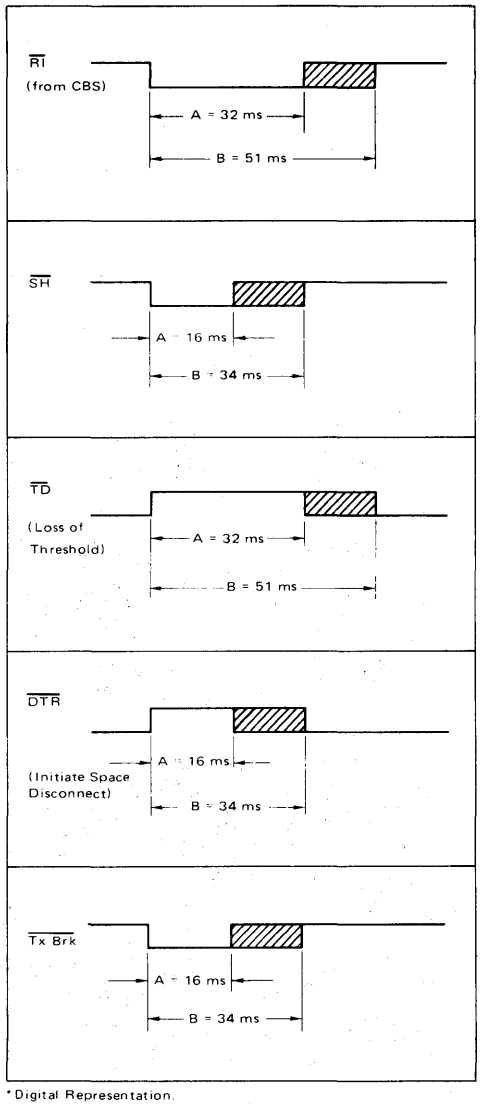
FIGURE 10 — TRANSMIT CARRIER FREQUENCY SPECTRUM

TABLE 1 – ASYNCHRONOUS INPUT PULSE WIDTH AND OUTPUT DELAY VARIATIONS
(Time delays specified do not include the 1-MHz reference tolerance.)

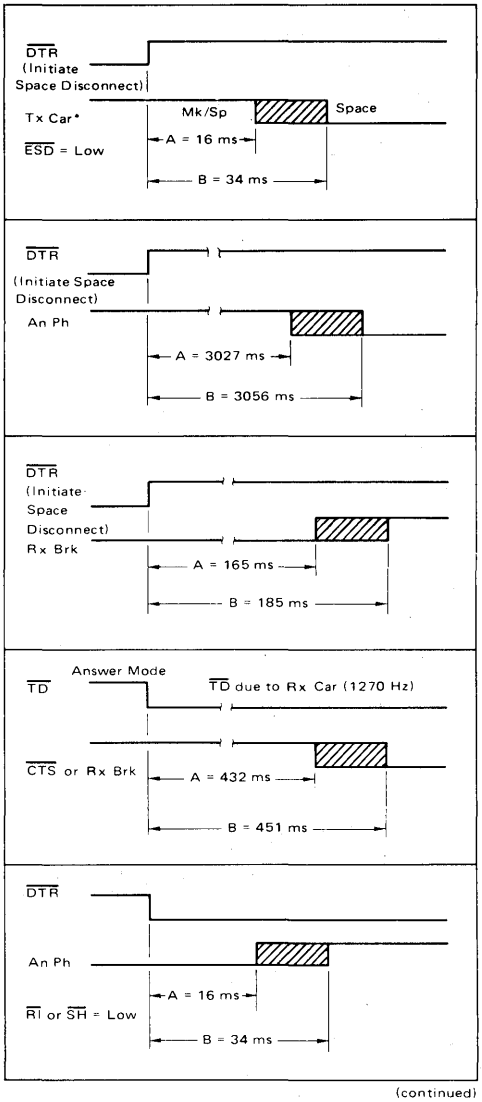
Due to the asynchronous nature of the input signals with respect to the circuit internal clock, a delay variation or input pulse width requirement will exist. Time delay A is the maximum time for which no response will occur. Time delay B is the minimum time required to guarantee an input response. Input signal widths in the cross-hatched region (i.e., greater than A but less than B) may or may not be recognized as valid.

For output delays, time A is the minimum delay before an output will respond. Time B is the maximum delay for an output to respond. Output signal response may or may not occur in the cross-hatched region (i.e., greater than A but less than B).

INPUT PULSES



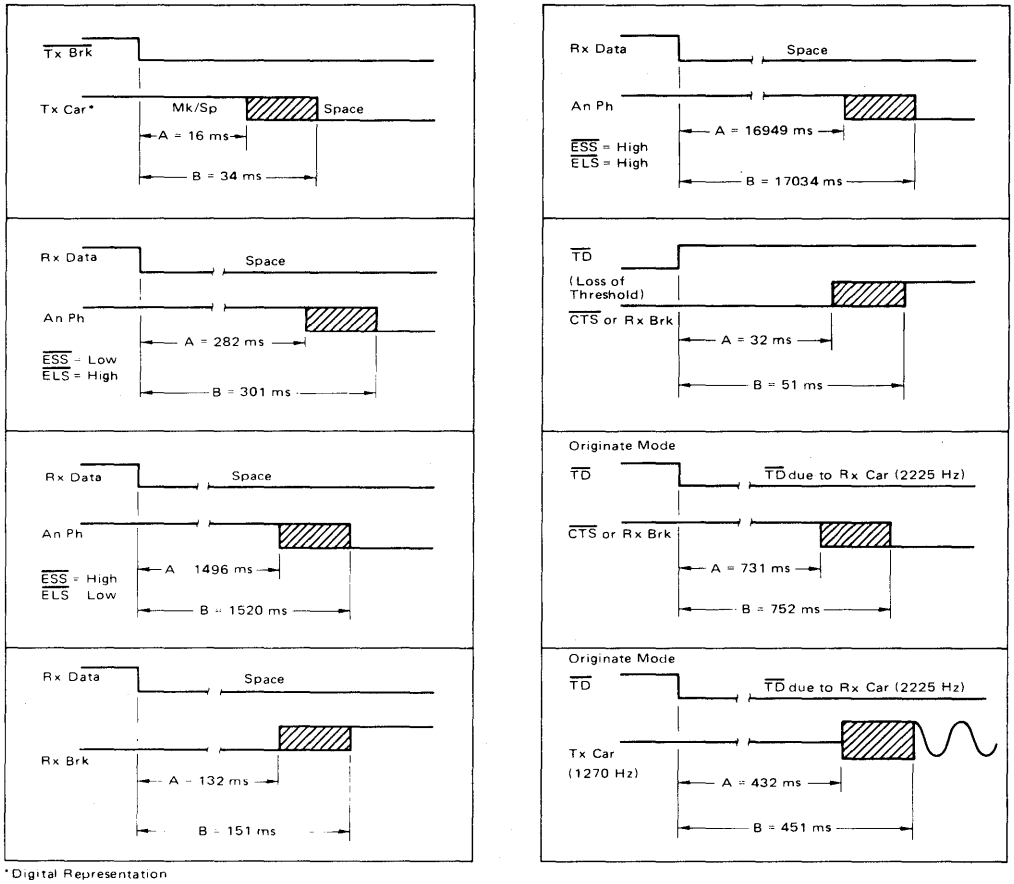
OUTPUT DELAYS



*Digital Representation.

(continued)

TABLE 1 – OUTPUT DELAY VARIATIONS (continued)



*Digital Representation

TABLE 2 – TRANSMIT BREAK AND DISCONNECT DELAYS

Function Description	Min	Max	Unit
$\overline{\text{Tx Brk}}$ (Space Duration)	232	235	ms
Space Disconnect (Space Duration) ($\overline{\text{DTR}}$ = High, $\overline{\text{ESD}}$ and $\overline{\text{TD}}$ = Low)	3010	3023	ms
Loss of Carrier Disconnect (Measured from positive edge of $\overline{\text{CTS}}$ to negative edge of An Ph, with $\overline{\text{RI}}$, $\overline{\text{SH}}$, and $\overline{\text{TD}}$ = High)	16965	17034	ms
Override Disconnect (Measured from positive edge of $\overline{\text{RI}}$ or $\overline{\text{SH}}$ to negative edge of An Ph, with $\overline{\text{TD}}$ = High)	16916	17101	ms

FIGURE 11 — FLOW DIAGRAM

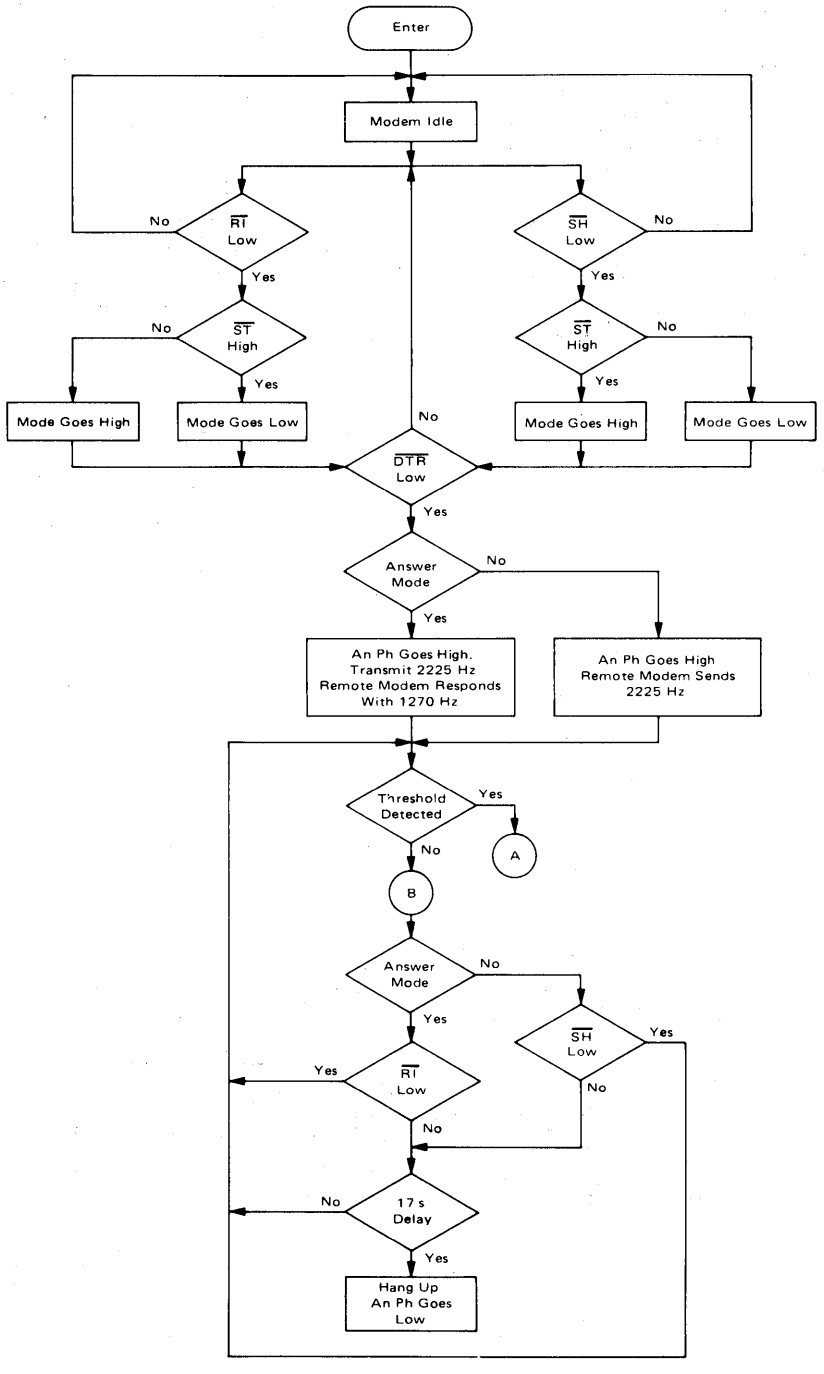
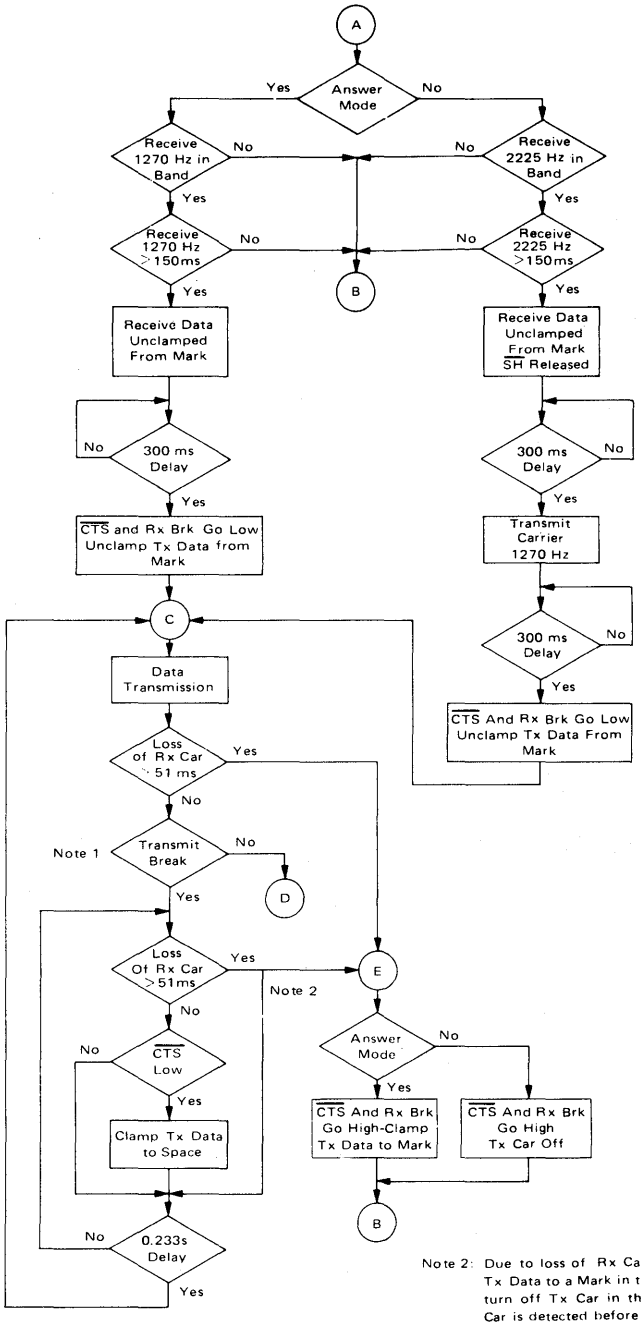


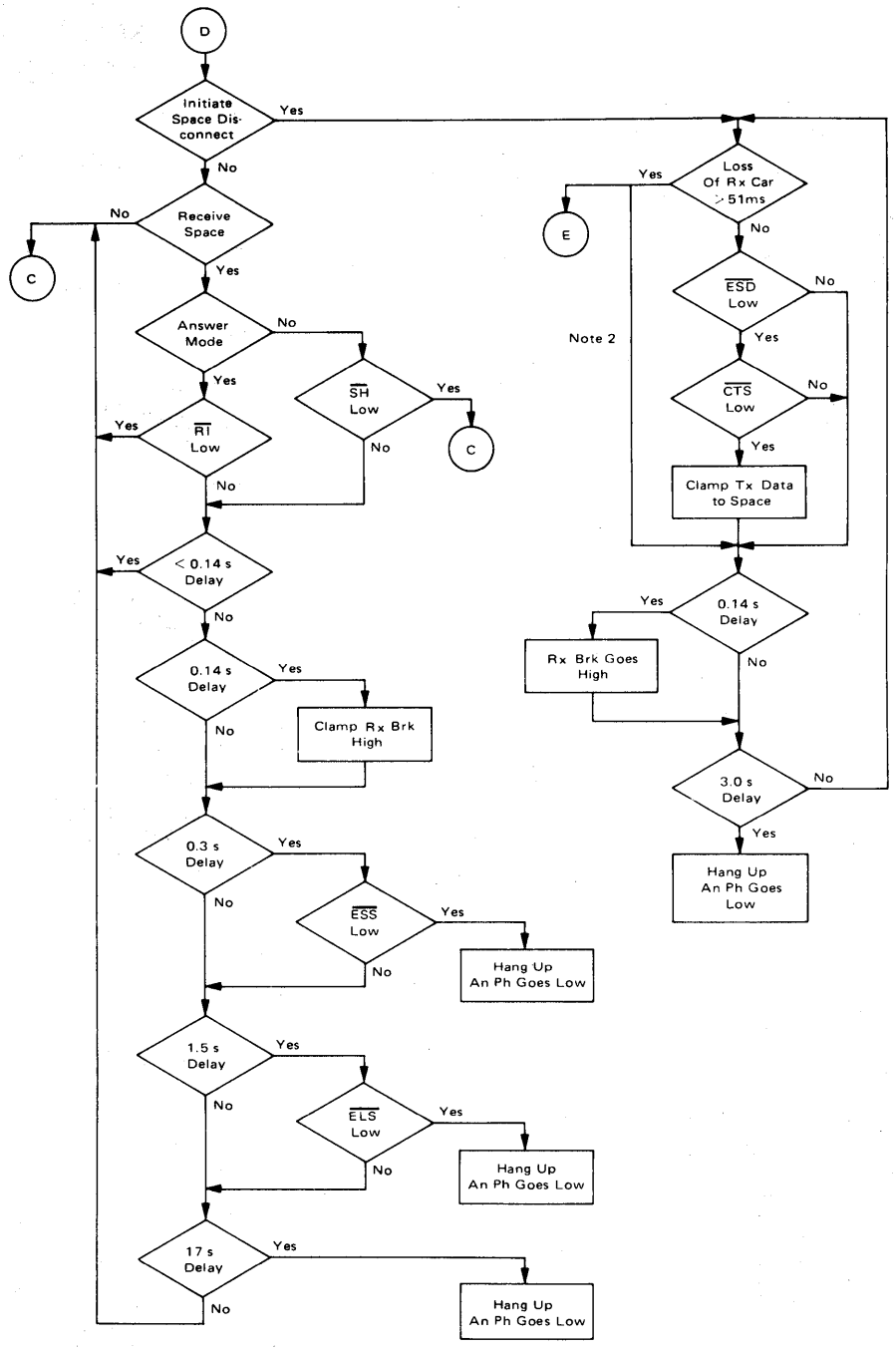
FIGURE 11 — FLOW DIAGRAM (CONTINUED)



Note 1: Transmit Break, Initiate Space Disconnect, and Receive Space are mutually exclusive events.

Note 2: Due to loss of Rx Car, the modem will clamp Tx Data to a Mark in the Answer Mode and will turn off Tx Car in the Originate Mode. If Rx Car is detected before completion of Tx Brk or Initiate Space Disconnect, normal operation of Tx Brk or Initiate Space Disconnect will continue until completion of their respective time delays.

FIGURE 11 — FLOW DIAGRAM (CONCLUDED)



MOTOROLA

MC14400
MC14401
MC14402
MC14403
MC14405

CMOS LSI

(LOW-POWER COMPLEMENTARY MOS)

CODEC-FILTER
PCM MONO-CIRCUIT

2

CODEC-FILTER PCM-MONO-CIRCUIT

The MC14400, MC14401, MC14402, MC14403, and MC14405 are all per channel codec-filter PCM mono-circuits. These devices perform the voice digitizing and recovery, as well as the band limiting and signal restoration necessary in PCM systems. The MC14400 and MC14403 are general purpose devices that are offered in a 16-pin package. They are designed to operate in both synchronous and asynchronous applications and contain an on-chip precision voltage reference. The MC14401 is the same device, but offered in an 18-pin package. In addition, it offers the user the capability of selecting from three peak overload voltages (2.5, 3.15 and 3.78 V). The MC14405 is a synchronous device in a 16-pin package intended for instrument use. The MC14402 is the full feature device which presents all of the options available on the chip. This device is packaged in a 22-pin DIP and 28-pin chip carrier package, and contains all the features of the MC14400 and MC14401 plus several more. Most of these features can be made available in a lower pin count package tailored to a specific user's application. Contact the factory for further details.

The devices were designed to be upward compatible with the MC14404/06/07 codecs and other industry standard codecs. They also maintain compatibility with Motorola's family of TSACs (MC14416/MC14417/MC14418) as well as the MC3419 SLIC.

The PCM codec-filter mono-circuits utilize CMOS due to its reliable low-power performance and proven capability for complex analog/ digital LSI functions.

MC14400

- 16-Pin Package
- On-Chip Precision Voltage Reference (3.15 V)
- Power Dissipation — 45 mW at 2.048 MHz at 10 V
  0.1 mW Powered Down at 10 V
- Compatibility with Various Supply Configurations: ±5, ±6, +10, +12 Volts (5%)
- Pin Selectable TTL and CMOS Digital Levels
- Automatic Prescale Divide of Any One of 5 Clock Frequencies (128 kHz, 1.536 MHz, 1.544 MHz, 2.048 MHz, or 2.56 MHz) to Generate the Internal Sequencing Clock
- Pin Selection of Both A-LAW/Mu-LAW Companding and D3/D4 or CCITT Digital Formats
- Output Drive Capability for 600 and 900 Ohm Loads of +12 dBm
- Synchronous and Asynchronous Operation
- On-Chip Attendent Interrupt Conferencing
- Transmit Bandpass and Receive Low-Pass Filters on Chip

MC14401 — All of the Above Plus:

- 18-Pin Package
- Selectable Peak Overload Voltages (2.5, 3.15 and 3.78 Volts)
- Access to the "Minus" Input of the Tx Input Op Amp

MC14402 — All of the Above Plus:

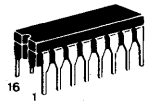
- 22-Pin Package
- Variable Data Clocks (64 kHz to 3.088 MHz)
- Access to Transmit Input Amplifier
- An External Precision Reference May Be Used
- External Gain Adjust for Complex SLIC Configurations

MC14403

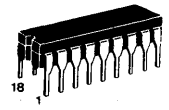
- 16-Pin Package
- Same Device as MC14400 with Access to Transmit Input Amplifier with Single Ended Receive Output
- MSI Tied Internally to TDE

MC14405

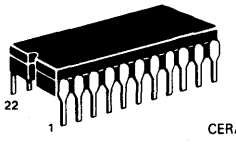
- 16-Pin Package
- Same Device as MC14403 with Common 64 kHz to 3.088 MHz Data Clocks



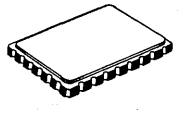
MC14400/03/05
L SUFFIX
CERAMIC PACKAGE
CASE 620



MC14401
L SUFFIX
CERAMIC PACKAGE
CASE 726



MC14402
L SUFFIX
CERAMIC PACKAGE
CASE 736



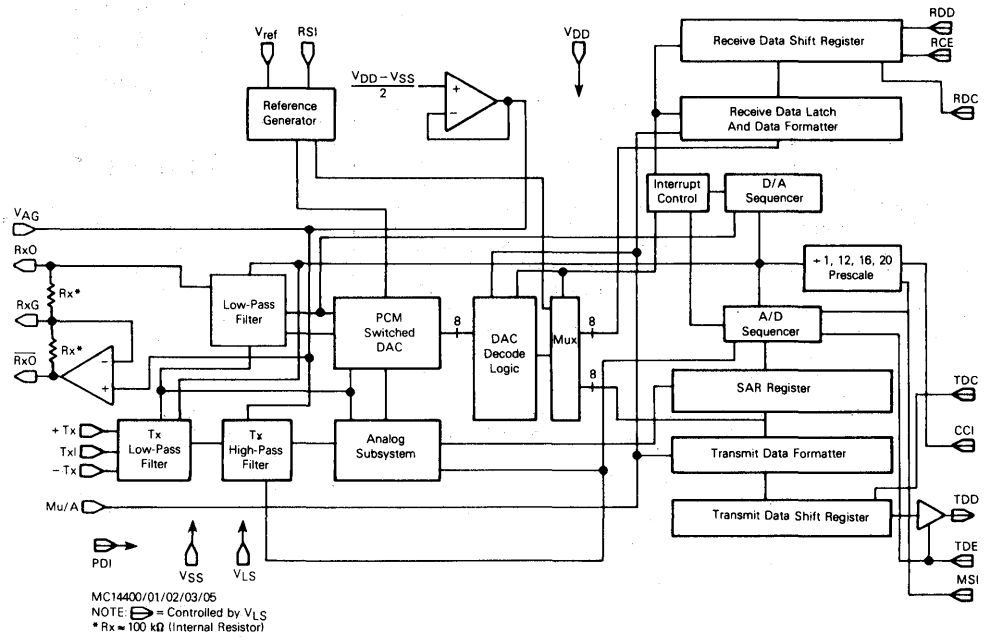
MC14402
Z SUFFIX
28-PIN CHIP CARRIER
CASE 763

ORDERING INFORMATION

MC14XXXXX

- 1 CCITT (G7.12)
- 2 D3/D4 (PUB 43801)
- L Ceramic Package
- Z Leadless Ceramic Package

PCM MONO-CIRCUIT BLOCK DIAGRAM



DEVICE DESCRIPTIONS

There are five distinct versions of the Motorola PCM mono-circuit.

MC14400

The MC14400 PCM mono-circuit is a PCM codec-filter intended for standard word interleaved synchronous or asynchronous applications. The TDC pin on this device is the input to both the TDC and CCI functions in the pin description. Consequently, for MSI = 8 kHz, TDC can be one of five discrete frequencies. These are 128 kHz (40 to 60% duty) 1.536, 1.544, 2.048 or 2.56 MHz. (For other data clock frequencies see MC14402 or MC14405.) The internal reference is set for 3.15 volts peak full scale, and the full scale input level at TxI and output level at RxO is 6.3 volts peak-to-peak. This is the +3 dBm0 level of the PCM mono-circuit. All other functions are described in the pin description.

MC14401

The MC14401 PCM mono-circuit offers the same features and is for the same application as the MC14400, but offers two additional pins and features. The reference select input allows the full scale level of the device to be set at 2.5 Vp, 3.15 Vp or 3.78 Vp. The – Tx pin allows for external transmit gain adjust and simplifies interface to the MC3419 SLIC. Otherwise, it is identical to MC14400.

MC14402

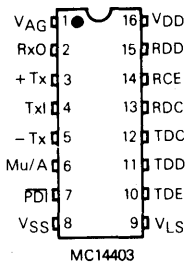
The MC14402 PCM mono-circuit is the full featured 22-pin device. It is intended for use in applications requiring maximum flexibility. The MC14402 contains all the features of the MC14400 and MC14401. The MC14402 is intended for bit interleaved or word interleaved operation with data clock frequencies which are non standard or time varying. One of the five standard frequencies (listed above) is applied to the CCI input and the data clock inputs can be any frequency between 64 kHz and 3.088 MHz. The V_{ref} pin allows for use of an external shared reference or selection of the internal reference and RxG and + Tx provide maximum flexibility for analog interface.

MC14403

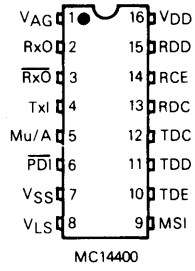
The MC14403 PCM mono-circuit is intended for standard word interleaved asynchronous or synchronous applications. TDC can be one of five discrete frequencies. These are 128 kHz (40 to 60% duty) 1.536, 1.544, 2.048 or 2.56 MHz. (For other data clock frequencies see MC14402 or MC14405.) The internal reference is set of 3.15 volts peak full scale, and the full scale input level at TxI and output level at RxO is 6.3 volts peak-to-peak. This is the +3 dBm0 level of the PCM mono-circuit. The + Tx and – Tx inputs provide maximum flexibility for analog interface. All other functions are described in the pin description.

MC14405

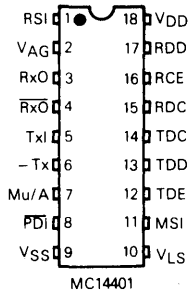
The MC14405 PCM mono-circuit is intended for word interleaved synchronous applications. The MC14405 has all the features of the MC14403 but internally connects TDC and RDC (see pin description) to the DC pin. One of five standard frequencies (listed above) should be applied to CCI and the DC input can be any frequency between 64 kHz and 3.088 MHz.



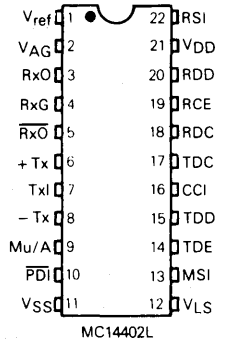
MC14403



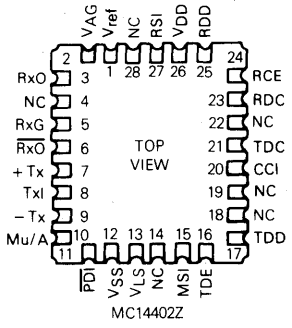
MC14400



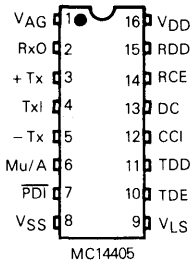
MC14401



MC14402L



MC14402Z



MC14405

MAXIMUM RATINGS (Voltage Referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	$V_{DD} - V_{SS}$	−0.5 to 13	V
Voltage, Any Pin to V_{SS}	V	−0.5 to V_{DD} + 0.5	V
DC Current Drain per Pin (Excluding V_{DD}, V_{SS})	I	10	mAdc
Operating Temperature Range	T_A	−40 to +85	°C
Storage Temperature Range	T_{stg}	−85 to +150	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Pins	0 to 70°C Min	25°C Typ	0 to 70°C Max	Unit
DC Supply Voltage	V_{CC} to V_{SS}	6	10 to 12	13	V
Power Dissipation CMOS Mode 10 V TTL Mode 10 V	V_{DD} to V_{SS}	– –	45 75	70 110	mW
Power Down Dissipation 10 V	V_{DD} to V_{SS}	–	0.1	1.0	mW
Frame Rate Transmit and Receive	MSI	7.5	8.0	8.5	kHz
Data Rate MC14400, MC14401, and MC14403 (Must Use One of These Frequencies) ±2%	TDC, RDC	– – – – –	128 1536 1544 2048 2560	– – – – –	kHz
Data Rate MC14402, MC14405		64	–	3088	kHz
Full Scale Output and Input Levels MC14400, MC14403, MC14405		–	3.15	–	
MC14401 and MC14402, $V_{ref} = V_{SS}$ RSI = V_{DD} RSI = V_{SS} RSI = V_{AG}	RxO, TxI	– – –	3.78 3.15 2.50	– – –	Vp

DIGITAL LEVELS (T_A = 0 to 70°C)

Parameter		Symbol	V_{DD} to V_{SS}	Min	Typ	Max	Unit
CMOS Mode							
TDE, RCE, RDD, $\overline{PDI}$, RDC, TDC, DC, CCI, MSI	"0"	–	12	–	5.25	3.6	V
	"1"	–	12	8.4	6.75	–	
TTL Mode							
TDE, RCE, RDD, $\overline{PDI}$, RDC, TDC, DC, CCI, MSI	"0"	–	10	–	V_{LS} + 1.0	V_{LS} + 0.8	V
	"1"	–	10	V_{LS} + 2.0	V_{LS} + 1.8	–	
TDD Output Current							
(TTL Mode)	V_{OH} = 2.4 V	I_{OH}	10	150	–	–	μA
	V_{OL} = 0.8 V	I_{OL}	–	1.6	–	–	ma

ANALOG TRANSMISSION PERFORMANCE

(V_{DD} = +5 V ±5%, V_{SS} = −5 V ±5%, 0 dBm0 = +6 dBm@600 Ω, V_{LS} = V_{AG} = 0, T_A = 0 to 70°C, TDC = RDC; TDE = RCE = 8 kHz)

Characteristic	E to E		A/D		D/A		Unit
	Min	Max	Min	Max	Min	Max	
Absolute Gain (0 dBm0 @ 1.02 kHz)	−0.3	+0.3	−0.3	+0.3	−0.3	+0.3	dB
Gain vs Level Tone (Relative to −10 dBm0, 1.02 kHz)							
+3 to −40 dBm0	−0.4	+0.4	−0.2	+0.2	−0.2	+0.2	dB
−40 to −50 dBm0	−0.8	+0.8	−0.4	+0.4	−0.4	+0.4	
−55 dBm0	−1.6	+1.6	−1.0	+1.0	−0.8	+0.8	
Gain vs Level — Pseudo Noise (A-Law Only, MC144XXL1 Only) (Relative to −10 dBm0)							dB
−10 to −55 dBm0	−0.45	+0.45	–	–	–	–	
−60 dBm0	−0.90	+0.90	–	–	–	–	
Total Distortion — 1.02 kHz Tone (C Message)							
0 to −30 dBm0	35	–	35	–	36	–	dB
−40 dBm0	29	–	29	–	30	–	
−45 dBm0	24	–	24	–	25	–	
Total Distortion with Noise (A-Law Only, MC144XXL1 Only)							
−3 dBm0	27.5	–	–	–	–	–	dB
−6 to −27 dBm0	35	–	–	–	–	–	
−34 dBm0	33.1	–	–	–	–	–	
−40 dBm0	28.5	–	–	–	–	–	
−55 dBm0	13.5	–	–	–	–	–	
Idle Noise							
(Mu Law, C Message)	–	18	–	18	–	13	dBrnCo
(A Law, Psophometric — MC144XXL1 Only)	–	−68	–	−68	–	−75	dBmOp
Frequency Response (Relative to −10 dBm0, 1.02 kHz)							
15 to 60 Hz	–	−23	–	−23	–	0.15	dBm0
300 to 3000 Hz	−0.30	+0.30	−0.15	+0.15	−0.15	+0.15	
3400 Hz	−1.6	0	−0.8	0	−0.8	0	
4000 Hz	–	−28	–	−14	–	−14	
4600 Hz	–	−60	–	−32	–	−30	
Inband Spurious (1.02 kHz@0 dBm0)							dBm0
300 to 3400 Hz	–	−43	–	−43	–	−43	
Out-of-Band Spurious (0 to 12 kHz in, @0 dBm0)							
0 to 3400 Hz	–	−30	–	−30	–	–	dBm0
3400 to 4600 Hz	–	−28	–	–	–	–	
4600 Hz to 12 kHz	–	−30	–	–	–	–	
Idle Noise Selective							
@ 8 kHz with V_{AG} = TxI Measure at RxO, 30 Hz Bandwidth	–	−50	–	–	–	–	dBm0
Group Delay Difference							
0 dBm0, TDC, RDC = 2.048 MHz							
500 to 600 Hz	–	80	–	–	–	–	μsec
600 to 1000 Hz	–	60	–	–	–	–	
1000 to 2600 Hz	–	140	–	–	–	–	
2600 to 2800 Hz	–	80	–	–	–	–	
Go to Return Crosstalk @0 dBm0							
TxI to TDD @ RxO RDD to RxO @ TDD	–	–	–	−65	–	−65	dBm0
Absolute Group Delay @ 1.02 kHz							
TDC = RDC = 2.048 MHz	–	460	–	–	–	–	μs

ANALOG ELECTRICAL CHARACTERISTICS (V_{DD} = (10-12 V) ±5%, 0 to 70°C)

Characteristic		Symbol	Min	Typ	Max	Unit
Input Current	– Tx, + Tx, (TxI for MC14400)	I_{in}		±0.01	±30	nA
AC Input Impedance (1 kHz)	TxI (for MC14400) to V_{AG}	Z_{in}	100	200	–	kΩ
AC Input Impedance (1 kHz)	– Tx, + Tx to V_{AG}	Z_{in}	1.5	5.0	–	MΩ
Input Common Mode Voltage Range V_{DD} = 10.0 V	– Tx, + Tx	V_{ICR}	+1.5	–	+8.0	V
Output Voltage Range						
RL = 20 k to V_{AG}	RxO, $\overline{RxO}$	V_{OR} to	−4.0	–	+4.0	
RL = 600 to V_{AG}	Each	V_{AG}	−3.2	–	+3.2	V
RL = 900 to V_{AG}	Output		−3.9	–	+3.9	
Output Current RxO, $\overline{RxO}$	$V_{OH} = V_{DD} - 0.8$	–	−5.0	–	–	mA
	$V_{OL} = 0.8$	–	+5.0	–	–	
Power Supply Rejection Ratio	RxO to V_{AG}	PSRR	30	40	–	dB
V_{DD} = 12 V ±0.05 V peak @ 1 kHz	$\overline{RxO}$ to V_{AG}		30	40	–	
Shared External Reference	V_{ref} to V_{AG}		2.0	–	3.8	V
V_{ref} Input Current		I_{in}	–	0.3	–	mA
V_{AG} Output Current	Source	I_{VAG}		200		μA
	Sink	I_{VAG}		8.0		mA

MODE CONTROL LOGIC (V_{SS} = 0 V, 0 to 70°C)

Characteristics		V_{DD} Vdc	Min	Typ	Max	Unit
V_{LS} Voltage for TTL Mode		10	0	–	6.0	V
		12	0	–	8.0	
V_{LS} Voltage for CMOS Mode		10	9.5	–	–	V
		12	11.5	–	–	
Mu/A Select Voltage						
Mu-Law Mode		10	9.5	–	–	
		12	11.5	–	–	
Sign Magnitude Mode		10	4.0	–	6.0	
		12	5.0	–	7.0	V
A-Law Mode		10	–	–	0.5	
		12	–	–	0.5	
Reference Select Voltage	3.78 V Mode	10	9.5	–	–	V
		12	11.5	–	–	
	2.5 V Mode	10	4.0	–	6.0	V
		12	5.0	–	7.0	
	3.15 V Mode	10	–	–	0.5	V
		12	–	–	0.5	
V_{ref} Mode Voltage	External Reference Mode	10	4.0	–	–	V
		12	5.0	–	–	
	Internal Reference Mode	10	–	–	0.5	
		12	–	–	0.5	
Analog Test Mode Selection Frequency, MSI = CCI		10	–	128	–	kHz
See Pin Description; Test Modes		12	–	128	–	

SWITCHING CHARACTERISTICS (V_{DD} = (10 to 12 V), T_A = 0 to 70°C, C_L = 50 pF CMOS or TTL Mode)

Characteristic			Symbol	Min	Typ	Max	Unit
Output Rise Time Output Fall Time		TDD	t_{TLH} t_{THL}	–	30	80	ns
Input Rise Time Input Fall Time		DC, TDE, CCI, RCE, RDC, TDC, MSI	t_{TLH} t_{THL}	–	–	4	μs
Pulse Width		DC, TDE Low, CCI, RCE, RDC, TDC, MSI	t_{WH}	100	–	–	ns
Clock Pulse Frequency		DC, TDC, RDC	f_{CL}	64	–	3088	kHz
Clock Pulse Frequency (MSI = 8 kHz) This Pin Will Accept One of These 5 Discrete Clock Frequencies and Compensate to Produce Internal Sequencing.		CCI 1 2 3 4 5	f_{CL1} f_{CL2} f_{CL3} f_{CL4} f_{CL5}	– – – – –	128 1536 1544 2048 2560	– – – – –	kHz
Propagation Delay Time	TTL	TDE to TDD Low Impedance	t_{P1}	85	130	180	ns
	CMOS	TDE to TDD Low Impedance	t_{P1}	50	100	160	
	TTL	TDE to TDD High Impedance	t_{P2}	–	50	75	
	CMOS	TDE to TDD High Impedance	t_{P2}	–	20	40	
	TTL	TDC* to TDD	t_{P3}	–	120	180	
	CMOS	TDC* to TDD	t_{P3}	–	80	160	
TDE Rising Edge to TDC Falling Edge Setup Time			t_{su1} t_{su2}	20 100	– –	– –	ns ns
RCE Rising Edge to RDC Falling Edge Setup Time			t_{su3} t_{su4}	20 100	– –	– –	ns ns
MSI Rising Edge to CCI Falling Edge Setup Time			t_{su6} t_{su7}	20 100	– –	– –	ns ns
RDD Valid to RDC Falling Edge Setup Time			t_{su5}	60	40	–	ns
RDD Hold Time from RDC Falling Edge			t_h	100	60	–	ns

*For the sign bit, t_{P3} is measured from TDE or TDC, whichever is last.

PIN DESCRIPTION

DIGITAL

V_{LS} selects CMOS or TTL compatibility for all digital I/Os. $V_{LS} = V_{DD}$; all I/O is CMOS, (V_{DD} to V_{SS} swing). $V_{LS} < V_{DD} - 4$ volts; all I/O is TTL with switchpoint 1.4 V above V_{LS}. The pins controlled by V_{LS} are inputs MSI, CCI, TDC, RDC, TDE, RCE, RDD, $\overline{PDI}$ and output TDD. In TTL applications V_{LS} is Digital GND.

MSI is a continuous 8 kHz (for sampling rate) signal which is used as a time base for internally selecting a prescale divider for CCI input. MSI should be tied to the frame sync or system sync signal, but has no relation to transmit or receive data timing, except as described under TDE. MSI should be derived from the transmit timing in asynchronous applications. In many applications MSI can be tied to TDE. (MSI is tied to TDE in MC14403/05.)

CCI input is designed to accept five discrete clock frequencies. These are 128 kHz 40 to 60% duty cycle, 1.536 MHz, 1.544 MHz, 2.048 MHz or 2.56 MHz. The frequency at this input is compared with MSI and prescale divided to produce the internal sequencing clock at 128 kHz (or 16 times the sampling rate). The four clocks in the MHz frequency range have only minimum pulse width duty cycle requirements. In the asynchronous applications, CCI should be derived from transmit timing. (CCI is tied to TDC in MC14400/01/03).

TDC is the transmit data bit rate input. It can be any frequency from 64 kHz to 3.088 MHz, and is often tied in common to CCI if the data rate is equal to one of the five discrete frequencies. This clock is the shift clock for the transmit shift register and leading edges produce successive data bits at TDD. In asynchronous applications, TDE should be derived from this clock. (TDC and RDC are tied together in MC14405 and are called DC.)

TDE serves two functions for the transmit data timing. It establishes the transmit sync in conjunction with MSI. If the leading edges of TDE occur at 8 kHz and both MSI and TDE are derived from TDC, then the MSI relationship is transparent and TDE is simply transmit sync. The leading edge of TDE produces the sign bit at TDD during the current TDC period. The TDC shifts out the remaining bits at the TDC rate. The TDD pin is active as long as TDE is high. If there is more than one TDE leading edge per frame, then the first TDE after MSI is the Tx sync. Thus, TDE may be taken low to three state TDD after the first leading edge. The additional TDE high periods before the next MSI merely un-three-states TDD. This can be used for bit interleaved systems. In asynchronous applications, TDE is derived from TDC.

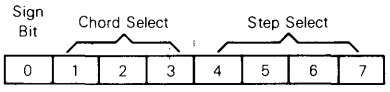
TDD is the digital data output. It operates in sync with TDC and TDE. It is a three-state output. TDC, TDE, and TDD independently control transmit data timing. The data format (Mu-Law, A-Law or sign magnitude) is controlled by Mu/A. This output may be made high-speed CMOS compatible using a pullup resistor.

RDC is the receive data clock and works in conjunction with RCE and RDD to produce all receive data timing. These three signals must be synchronous, but can be asynchronous with all other digital pins. RDC provides the receive register clock. The RDC clock may be any frequency from 64 kHz to 3.088 MHz.

RCE – The rising edge of RCE should identify the sign bit of a receive word on RDD. The next falling edge of RDC, after a rising RCE, loads the first bit of the PCM word into the receive register. The next seven falling edges enter the remainder of the PCM word. On the ninth rising edge, the receive word is transferred to the receive buffer register and the A/D sequence is interrupted to commence the decode process. In the asynchronous mode and with an 8 kHz transmit sample rate, the receive sample rate should be between 7.5 and 8.5 kHz. Two receive words may be decoded each transmit frame to allow on chip conferencing.

RDD is the digital data input. It operates synchronously with RDC and RCE. The data format is determined by the Mu/A pin.

Code	Sign/ Magnitude	Mu-Law	A-Law (CCITT)
+ full scale	1111 1111	1000 0000	1010 1010
+ zero	1000 0000	1111 1111	1101 0101
− zero	0000 0000	0111 1111	0101 0101
− full scale	0111 1111	0000 0010	0010 1010



Note: Starting from sign magnitude, to change format:
To Mu-Law –
MSB is unchanged (sign)
invert remaining seven bits
if code is 0000 0000, change to 0000 0010 (for zero code suppression)
To A-Law –
MSB is unchanged (sign)
invert odd numbered bits
ignore zero code suppression

Mu/A Select – This pin selects the companding law and the data format at TDD and RDD.

Mu/A = V_{DD}; Mu255 Companding D3 Data Format with Zero Code Supress

Mu/A = V_{AG}; Mu255 Companding with Sign Magnitude Data Format

Mu/A = V_{SS}; A-law Companding with CCITT Data Format Bit Inversions

$\overline{PDI}$ – The power down input disables the bias circuitry and gates off all clock inputs. This puts the TxI, RxO, $\overline{RxO}$, and T_{DD} outputs into a high impedance state. The power dissipation is reduced to 0.1 mW when $\overline{PDI} = V_{LS}$ or V_{SS}. The circuit operates normally with $\overline{PDI} = V_{DD}$ or with a logic high as defined by connection at V_{LS}. T_{DD} will not come out of high impedance for two MSI cycles after $\overline{PDI}$ goes high.

DC – In the MC14405, TDC and RDC are internally connected to this pin.

ANALOG

V_{AG} Analog Ground

Each version of the PCM mono-circuit produces its own analog ground internally. The DC voltage is approximately $(V_{DD} - V_{SS})/2$. All analog functions within the device use this as a reference point for signal processing. In symetric dual supply systems (±5, ±6, etc.), V_{AG} may externally be tied to the system analog ground supply. The V_{AG} output will sink more than 8 mA of current, but can source only 200 μA. When RxO or $\overline{RxO}$ are output drives for 600 or 900 loads tied to V_{AG}, a pullup resistor to V_{DD} will be required to boost the source current capability if V_{AG} is not tied to the supply ground.

V_{ref} Positive Voltage Reference Input (MC14402 Only)

The V_{ref} pin provides for the supply of an external voltage reference or for the selection of an internal reference within the PCM mono-circuit. If V_{ref} is tied to V_{SS}, the internal reference is selected. If $V_{ref} > V_{AG}$, then the external mode is selected. In each case, the overload or full scale gains of the codec are selected by the reference select pin (RSI). Both the internal and external references are inverted within the PCM mono-circuit for negative input voltage such that only one reference is required.

External Mode – In the external reference mode ($V_{ref} > V_{AG}$), a 2.5 volt reference like the MC1403 is connected from V_{ref} to V_{AG}. A single external reference may be shared by tying together a number of V_{ref}s and V_{AG}s from different PCM mono-circuits. In special applications, the reference voltage may be between 2 and 4 volts. However, the gain selection logic associated with RSI must be considered to arrive at the desired PCM mono-circuit gain.

Internal Mode – In the internal reference mode ($V_{ref} = V_{SS}$), an internal reference supplies the reference voltage for the PCM mono-circuit.

RSI Reference Select Input (MC14401/02 Only)

The RSI input allows the selection of three different overload or full scale voltages independent of the internal or external reference mode. The selection of maximum signed level is made by connecting RSI to V_{DD}, V_{AG} or V_{SS}. The various modes of operation are summarized in the table below. The internal reference is designed to give internal gains equal to those obtained with an external 2.5 volt reference.

RxO and $\overline{RxO}$ Receive Analog Outputs

These two complimentary outputs are generated from the output of the receive filter. They are equal in magnitude and out of phase. The maximum signal output of each is equal to the maximum peak-to-peak signal described with the reference. If a 2.5 V reference is used with RSI tied to V_{AG} and a +3 dBm0 sine wave is decoded, the RxO output will be a 5 V peak-to-peak signal. $\overline{RxO}$ will also have a signal output of 5 V peak-to-peak. External loads may be connected from RxO to $\overline{RxO}$ for a 6 dB push-pull signal gain or from either RxO or $\overline{RxO}$ to V_{AG}. With RSI tied to V_{SS}, each output will drive 600 Ω to +9 dBm. With RSI tied to V_{DD}, each output will drive 900 Ω to +9 dBm.

ADDITIONAL PIN DESCRIPTIONS

RxG Receive Output Gain Adjust (MC14402 Only)

If RxG is left open, then the output signal at RxO will be inverted and output at $\overline{RxO}$. Thus the push-pull gain to a load from RxO to $\overline{RxO}$ is two times the output level at RxO. If external resistors are applied from RxO to RxG (RI) and from RxG to $\overline{RxO}$ (RG), the gain of $\overline{RxO}$ can be set differently from −1. These resistors should be in the range of 10 kΩ. The RxO output level is unchanged by the resistors and the $\overline{RxO}$ gain is equal to minus RG/RI(VRxO). The purpose of RxG is to allow external receive gain adjustment. The circuit for RxG and $\overline{RxO}$ is shown in the block diagram.

+ Tx Positive Tx Amplifier Input (MC14402/03/05 Only)
− Tx Negative Tx Amplifier Input (MC14401/02/03/05 Only)

The TxI pin is the input to the transmit bandpass filter. If + Tx or − Tx are available, then there is an internal amplifier preceding the filter whose pins are + Tx, − Tx and TxI. These pins allow access to the amplifier terminals to tailor the input gain with external resistors. The resistors should be in the range of 10 k. If + Tx is not available, it is internally tied to V_{AG}. If − Tx and + Tx are not available, the TxI is a unity gain high impedance input.

TxI Analog Input

TxI is the input to the transmit filter. It is also the output of the transmit gain amplifiers of the MC14401/02/03/05. The input impedance is greater than 100 k to V_{AG} in the MC14400. The TxI input has an internal gain of 1.0, such that a +3 dBm0 signal at TxI corresponds to the peak-to-peak swing of RxO described above. For ±2.5 V shared references and RSI = V_{AG}, the +3 dBm0 input should be 5.0 volt peak-to-peak.

Power Supplies

V_{DD} – Most Positive Supply. V_{DD} is typically 10 to 12 volts.

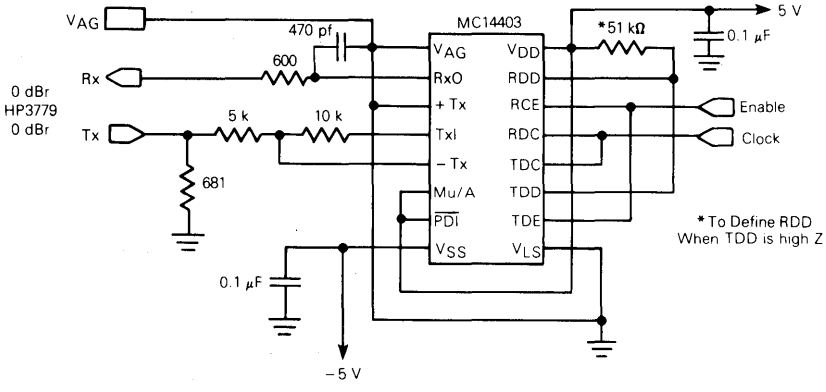
V_{SS} – Most Negative Supply. This is the most negative supply pin.

For single-supply systems, these are the only power pins. V_{LS} will be tied to V_{SS} or V_{DD} and V_{AG} is an output. In dual-supply systems, V_{LS} may be digital ground and V_{AG} may be analog ground.

Testing Considerations (MC14400/01/02 Only)

An analog test mode is activated by connecting MSI and CCI to 128 kHz. In this mode, the input of the codec (the output of the Tx filter) is available on the PDI pin. This input is a DC auto zeroed access to the A/D side of the codec. If monitored with a high-impedance buffer, the output of the Tx low-pass filter can also be measured at the PDI pin. This test mode allows independent evaluation of the transmit low-pass filter and A/D side of the codec. The receive channel of the mono-circuit is tested with the codec and filter together.

TEST CIRCUIT



OPTIONS AVAILABLE BY PIN SELECTION

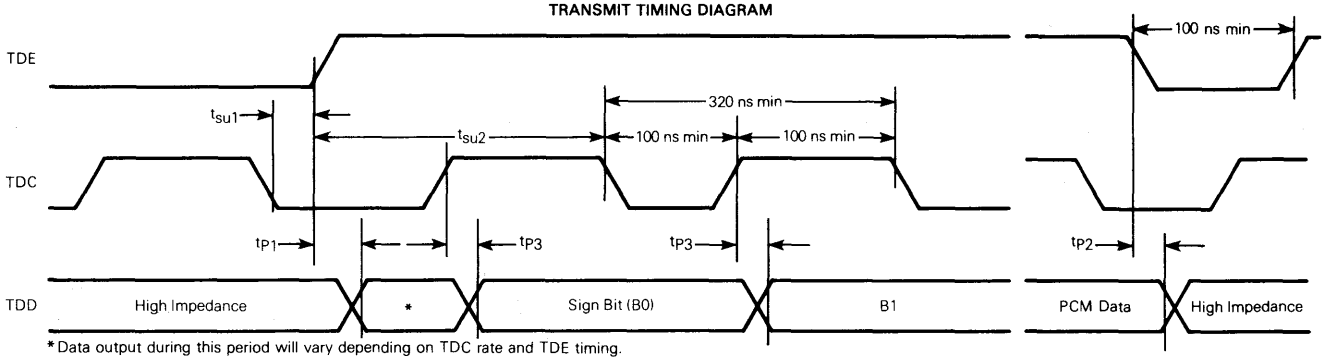
RSI* Pin Level	V_{ref}* Pin Level	Peak-to-Peak Overload Voltage (TxI, RxO)
V_{DD}	V_{SS}	7.56 V_{PP}
V_{DD}	$V_{AG}+V_{EXT}$	(3.02 × V_{EXT}) V_{PP}
V_{AG}	V_{SS}	5 V_{PP}
V_{AG}	V_{AG} + V_{EXT}	(2 × V_{EXT}) V_{PP}
V_{SS}	V_{SS}	6.3 V_{PP}
V_{SS}	V_{AG} + V_{EXT}	(2.52 × V_{EXT}) V_{PP}

*On MC14400/03/05, RSI and V_{ref} tied internally to V_{SS}.
On MC14401, V_{ref} tied internally to V_{SS}.

SUMMARY OF OPERATION CONDITIONS USER PROGRAMMED THROUGH PINS V_{DD}, V_{AG}, AND V_{SS}

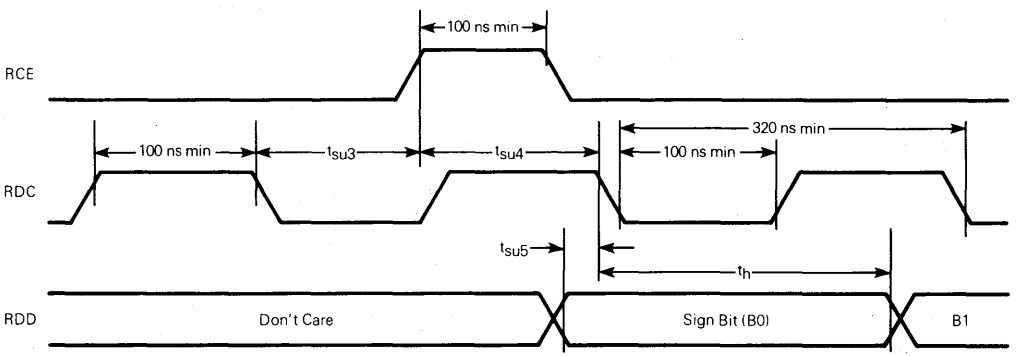
Pin Programmed / Logic Level	Mu/A	RSI Peak Overload Voltage	V_{LS}
V_{DD}	Mu-Law Companding Curve and D3/D4 Digital Formats with Zero Code Suppress	3.78	CMOS Logic Levels
V_{AG}	Mu-Law Companding Curve and Sign Magnitude Data Format	2.50	TTL Levels V_{AG} Up
V_{SS}	A-Law Companding Curve and CCITT Digital Format	3.15	TTL Levels V_{SS} Up

TRANSMIT TIMING DIAGRAM

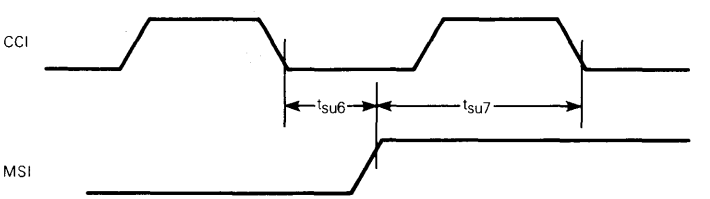


*Data output during this period will vary depending on TDC rate and TDE timing.

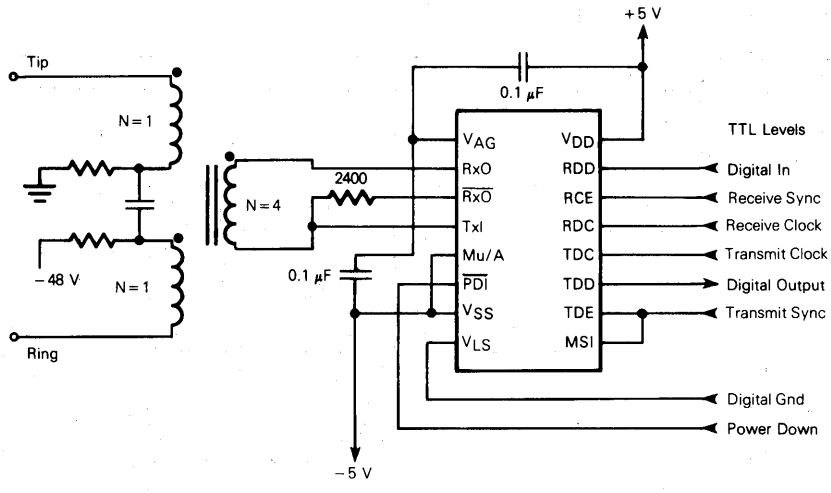
RECEIVE TIMING DIAGRAM



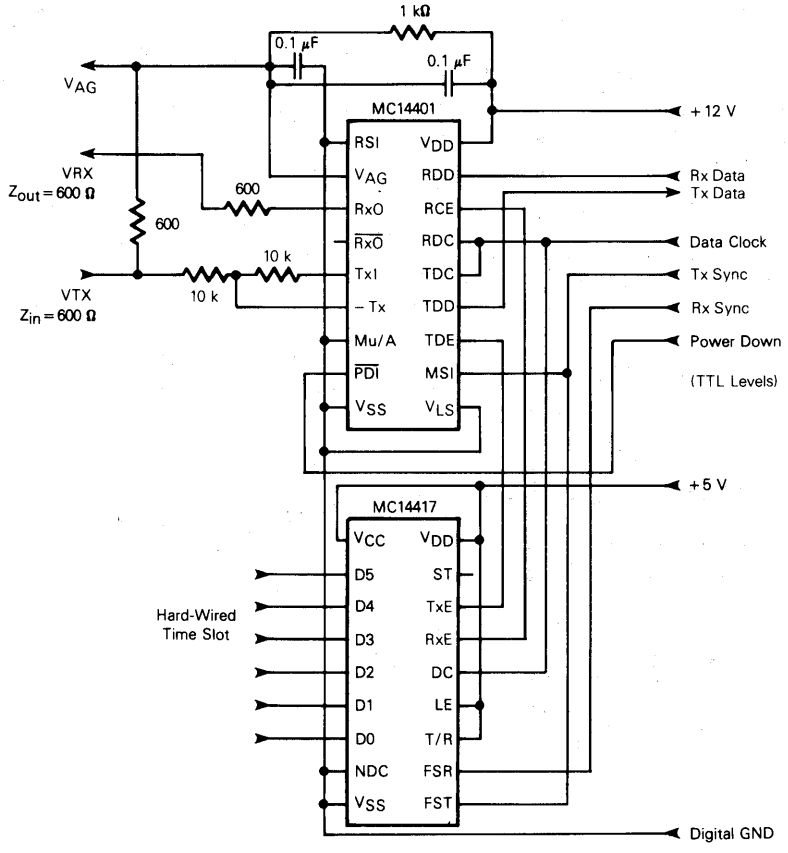
CCI/MSI TIMING DIAGRAM



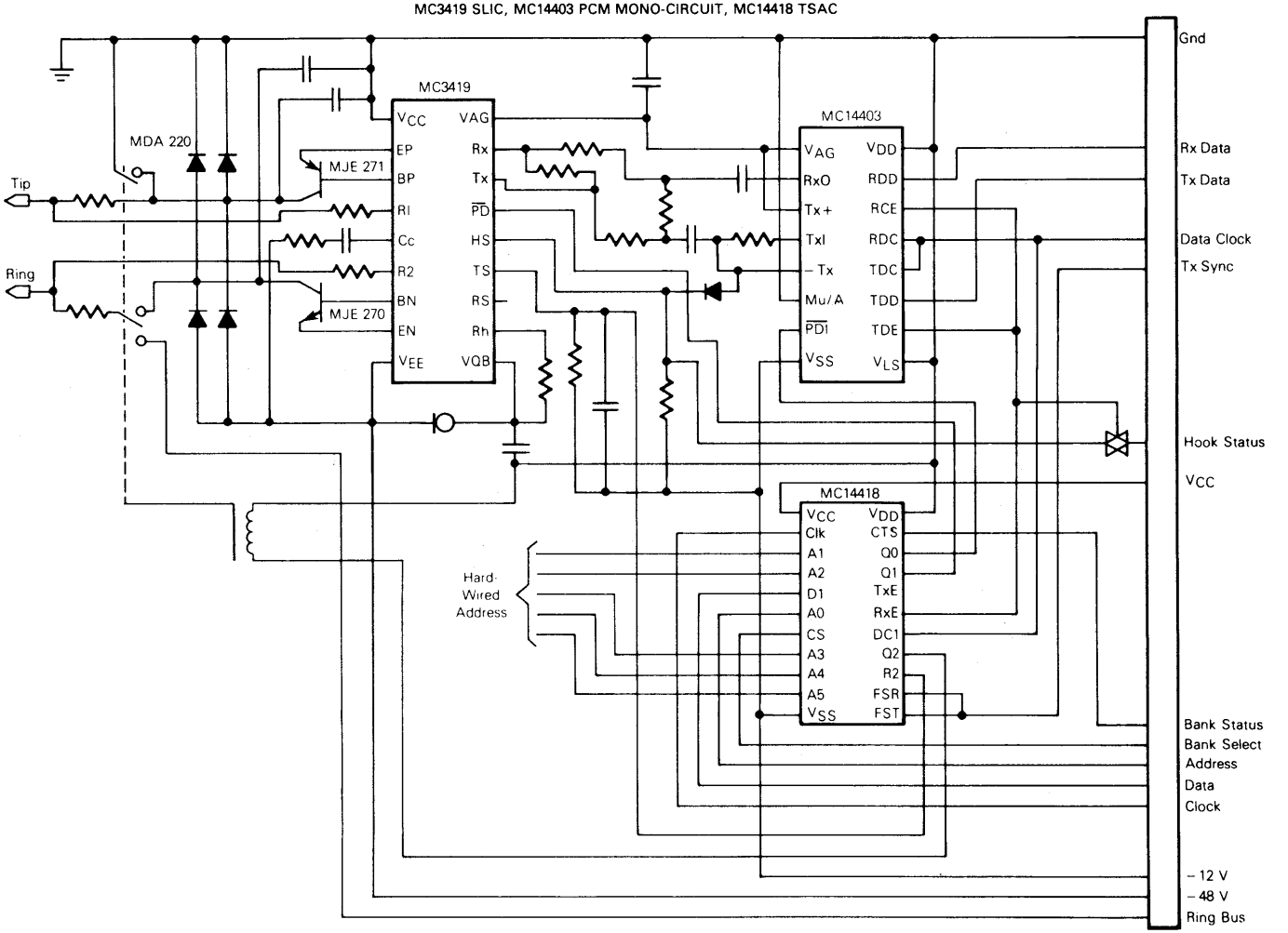
THE BASIC VOICE CHANNEL USING THE MC14400 PCM CODEC/FILTER MONO-CIRCUIT



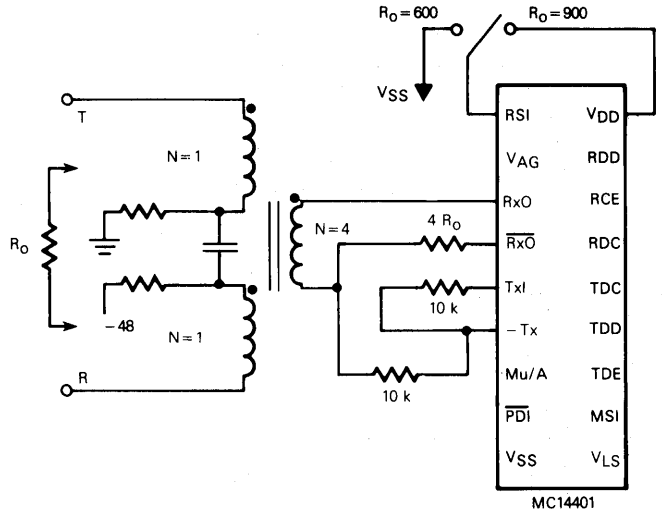
MC14401 PCM MONO-CIRCUIT WITH MC14417 TSAC



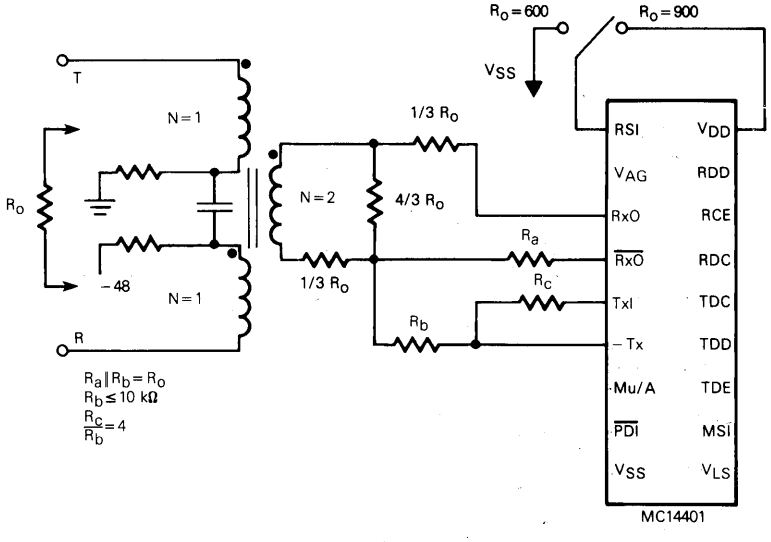
A COMPLETE SINGLE PARTY CHANNEL UNIT USING
MC3419 SLIC, MC14403 PCM MONO-CIRCUIT, MC14418 TSAC



HYBRID INTERFACES TO MC14401 PCM CODEC FILTER MONO-CIRCUIT

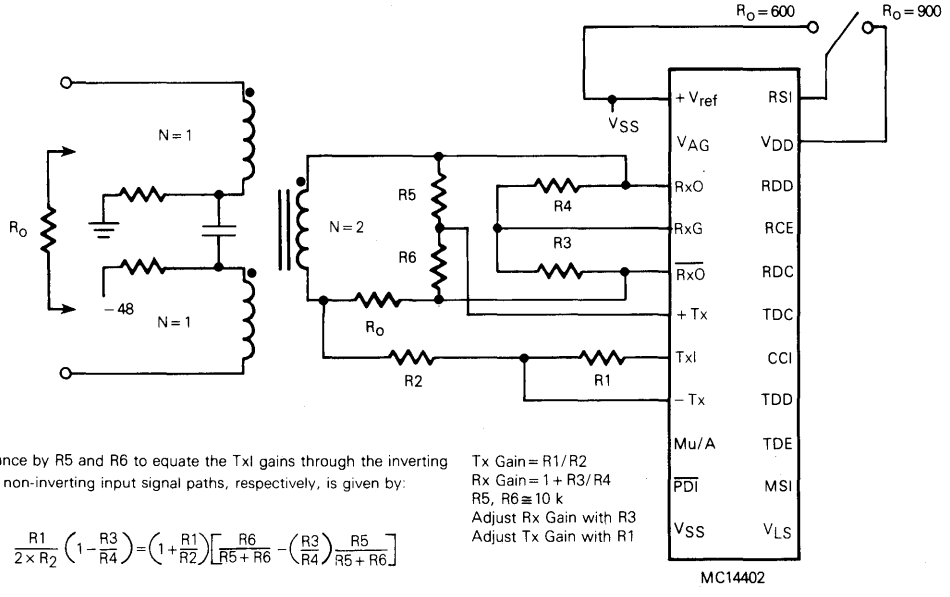


Simplified Transformer Hybrid Using MC14401



"T" Padded Transformer Hybrid Using MC14401

HYBRID INTERFACES TO THE MC14402 PCM CODEC/FILTER MONO-CIRCUIT

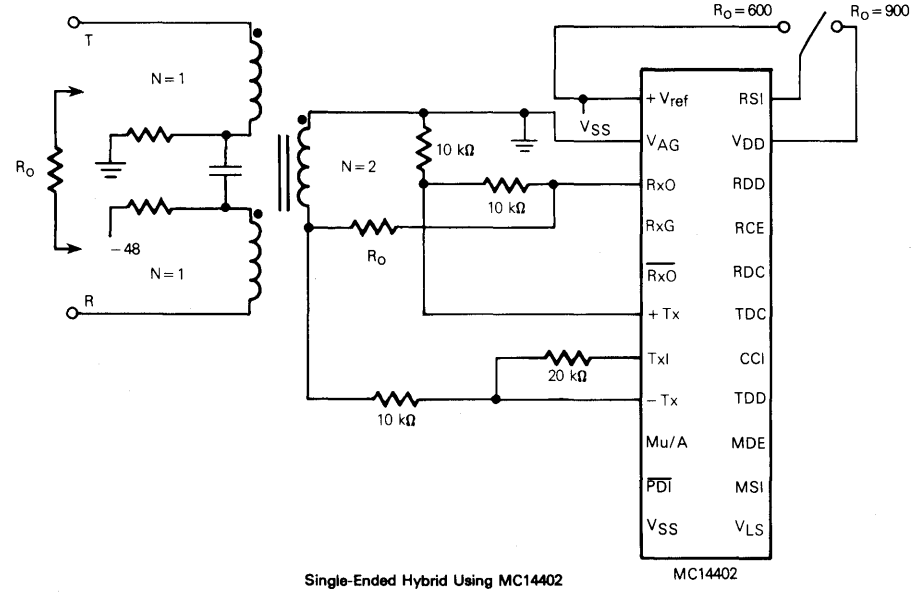


Balance by R5 and R6 to equate the TxI gains through the inverting and non-inverting input signal paths, respectively, is given by:

$$\frac{R1}{2 \times R_2}\left(1-\frac{R3}{R4}\right)=\left(1+\frac{R1}{R2}\right)\left[\frac{R6}{R5+R6}\right]-\left(\frac{R3}{R4}\right)\left[\frac{R5}{R5+R6}\right]$$

Tx Gain = R1/R2
Rx Gain = 1 + R3/R4
R5, R6 ≅ 10 k
Adjust Rx Gain with R3
Adjust Tx Gain with R1

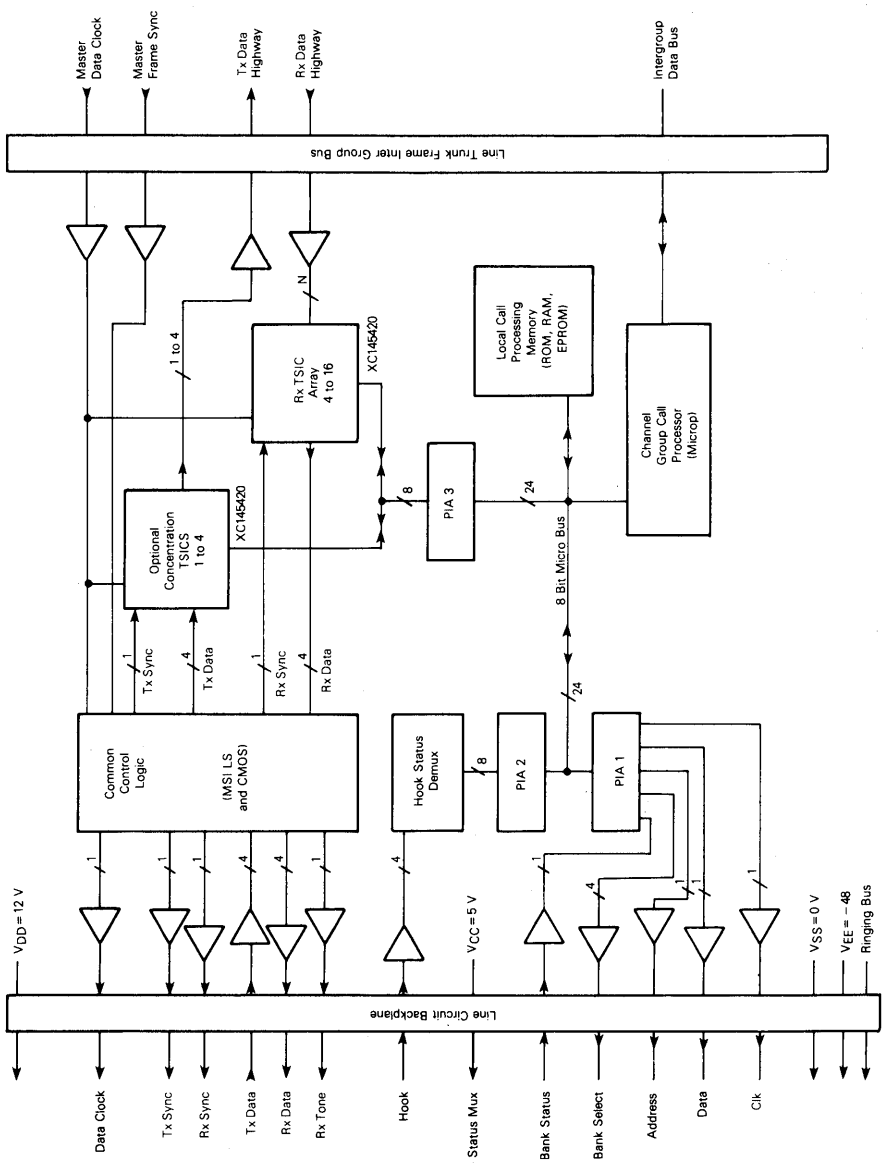
Universal Transformer Hybrid Using MC14402



Single-Ended Hybrid Using MC14402

2

128 CHANNEL GROUP COMMON CONTROL
IN A TYPICAL SWITCHING SYSTEM



NOTE: See single party line drawing for line card details.

MOTOROLA

MC14408
MC14409

CMOS LSI

(LOW-POWER COMPLEMENTARY MOS)

BINARY TO PHONE PULSE CONVERTER SUBSYSTEM

2

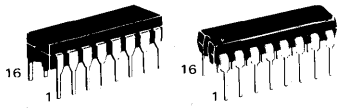
BINARY TO PHONE PULSE CONVERTER SUBSYSTEM

The MC14408 and the MC14409 are devices designed to convert a four bit binary input code to a number of serial output pulses corresponding to the value of the input code.

The devices can be used in telephone pulse dialing applications when combined with their companion device, the MC14419 (2-of-8 keypad-to-binary code converter). The devices have been partitioned to allow convenient addition of RAM memory and controls for repertoire dialing applications.

The MC14408 and MC14409 perform identical functions with the exception of the signal output at the DRO (Dial Rotating Output). In the MC14408, DRO remains high during continuous outpulsing of all digits and in the MC14409 DRO is low between each digit pulse burst.

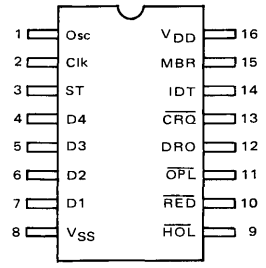
- On-Chip Oscillator
- Diode Protection on All Inputs
- Dialing of Numbers Up to 16 Digits Long
- Memory Storage (FIFO) and Re-Dialing (single pin) of Last Telephone Number
- Hold Interrupt Control for Additional Interdigit Delays (such as a Wait for Intermediate Dial Tones)
- Selectable Dialing Rate (10 pps or 20 pps)
- Selectable Interdigit Time (300 or 800 ms @ 10 pps; 150 or 400 ms @ 20 pps)
- Selectable Make-Break Ratio (61% or 67%)
- Buffered Outputs Compatible with Discrete Transistor Driver Interface, One Low-power Schottky TTL Load or Two Low-power TTL Loads Over the Rated Temperature Range.
- Low Power Dissipation — I_{DD} (operating with oscillator) = 470 μA typ @ V_{DD} = 5.0 Vdc, f_{Osc} = 16 kHz, C_L = 50 pF



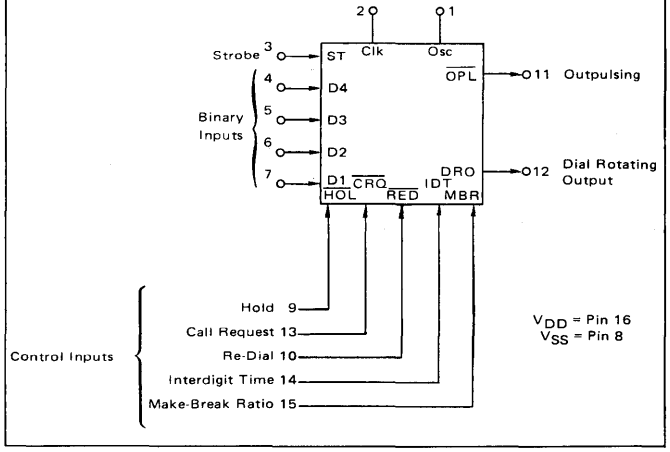
L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

PIN ASSIGNMENT



BLOCK DIAGRAM



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8.)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +6.0	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range	T_A	-40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	-40°C Min	-40°C Max	25°C Min	25°C Typ	25°C Max	+85°C Min	+85°C Max	Unit
Supply Voltage	V_{DD}	–	3.0	6.0	3.0	5.0	6.0	3.0	6.0	Vdc
Output Voltage "0" Level	V_{out}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
"1" Level		5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
Noise Immunity										
($\triangle V_{out} \leq 0.5$ Vdc)	V_{NL}	5.0	1.5	–	1.5	2.25	–	1.4	–	Vdc
($\triangle V_{out} \leq 0.5$ Vdc)	V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	Vdc
Output Drive Current	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-1.0	–	-0.80	-1.7	–	-0.60	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.20	–	-0.16	-0.36	–	-0.12	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
Input Current	I_{in}	6.0	–	0.3	–	±0.00001	±0.30	–	1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	12	–	5.0	12	–	12	pF
Operating Supply Current	I_{DD}	3	–	250	–	160	200	–	200	μAdc
f_{cl} = 16 kHz (operating		5	–	700	–	470	550	–	550	
with Osc)		6	–	1250	–	740	1000	–	1000	

FIGURE 1
TIMING DIAGRAM — DATA AND STROBE INPUTS

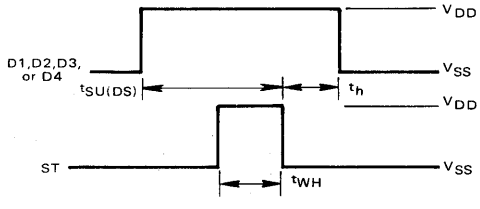
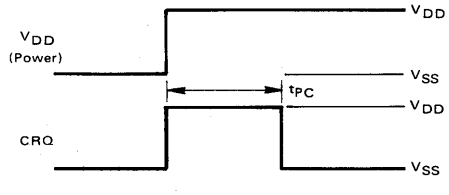


FIGURE 2
TIMING DIAGRAM — CALL REQUEST



If power is turned off after each call, CRQ must stay high after power is applied (for a duration of t_{PC}) to ensure no spurious outpulsing. For this use the redial function is invalid.

SWITCHING CHARACTERISTICS (C_L = 50 pF, T_A = 25°C)

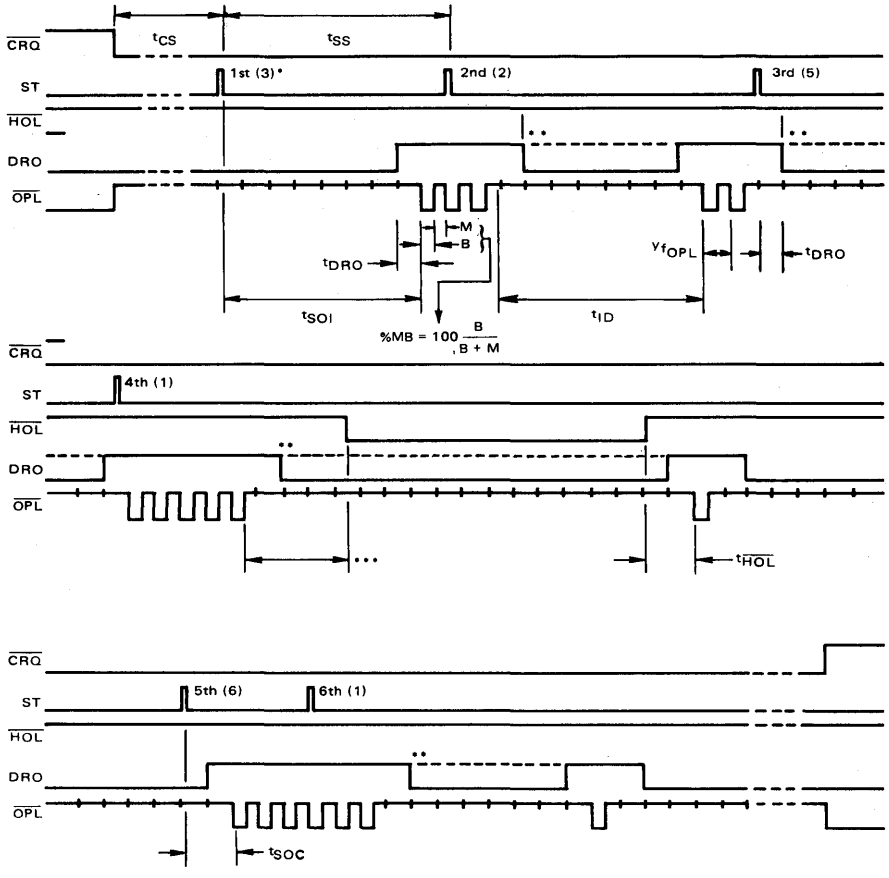
Characteristic	Symbol	V_{DD}	Min	Typ	Max	Unit
Output Rise Time** t_{TLH} = (3.0 ns/pF) C_L + 30 ns	t_{TLH}	5.0	–	180	400	ns
Output Fall Time** t_{THL} = (1.5 ns/pF) C_L + 25 ns	t_{THL}	5.0	–	100	200	ns
Power Up to Call Request Pause	t_{PC}	3 to 6	48/f_{cl}*	–	–	ms
Call Request to First Strobe Pulse	t_{CS}	3 to 6	48/f_{cl}*	–	–	ms
Strobe to Strobe Separation Time	t_{SS}	3 to 6	48/f_{cl}*	–	–	ms
Strobe Pulse Width	t_{WH}	3 to 6	1.0	–	–	μs
Strobe to Data Hold Time	t_h	3 to 5	–	150	400	ns
Clock Frequency***	f_{cl}	3 to 6	12.5	16	100	kHz
Percent Break to Make Ratio	%MB	3 to 6				%
(MBR = 0)			–	61	–	
(MBR = 1)			–	67	–	
Outpulsing Rate (f_{OPL} = *f_{cl}/1.6)	f_{OPL}	3 to 6				pps
f_{cl} = 16 kHz			–	10	–	
f_{cl} = 32 kHz			–	20	–	
Interdigit Time	t_{ID}	3 to 6				ms
t_{ID} = (5 x IDT + 3)/f_{OPL}						
IDT = 0						
f_{OPL} = 10 pps			–	300	–	
f_{OPL} = 20 pps			–	150	–	
IDT = 1						
f_{OPL} = 10 pps			–	800	–	
f_{OPL} = 20 pps			–	400	–	
Strobe to Output Time	t_{SOI}	3 to 6				ms
Initial Outpulsing Stream						
IDT = 0						
f_{OPL} = 10 pps			300	–	400	
f_{OPL} = 20 pps			150	–	200	
IDT = 1						
f_{OPL} = 10 pps			800	–	900	
f_{OPL} = 20 pps			400	–	450	
Continued Outpulsing Stream	t_{SOC}	3 to 6				ms
IDT = 0 or 1						
f_{OPL} = 10 pps			100	–	200	
f_{OPL} = 20 pps			50	–	100	
Hold to Outpulse Time	t_{HOL}	3 to 6				ms
IDT = 0 or 1						
f_{OPL} = 10 pps			100	–	200	
f_{OPL} = 20 pps			50	–	100	
Dial Rotating Overlap Time	t_{DRO}	3 to 6				ms
f_{OPL} = 10 pps			–	100	–	
f_{OPL} = 20 pps			–	50	–	
Data to Strobe Setup Time (f_{cl} = 16 kHz)	$t_{SU(DS)}$	3 to 6	1.5	–	–	μs
Re-dial Pulse Width (f_{cl} = 16 kHz)	–	3 to 6	–	200	–	ms

*f_{cl} in kHz

**The formula given is for the typical characteristics only.

*** Minimum clock pulse width = 1.0 μs.

FIGURE 3
PHONE DIALER SYSTEM TIMING DIAGRAM



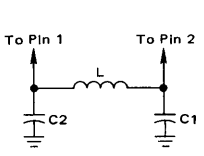
Notes:

(*)1st, 2nd, 3rd, etc., denotes Strobe pulse sequence — i.e., which digit in the phone number is being dialed. The number in parentheses denotes the numerical value of the digit being dialed. The examples define the various voltage — level and timing requirements, not a complete phone number.

(**)For the MC14408 the DRO signal will remain high provided digits remain in the memory, or a digit for continuing outpulsing is strobed in before the anticipated falling edge of the most significant digit in the memory. (i.e., [200 % MB] ms after the most significant outpulsing edge). The time from Strobe to DRO can be 0 to 100 ms.

(***)For the HOL signal to hold a next digit (e.g. the 4th, etc.,) the HOL falling edge must not appear after [t_{ID}-%MB + 100] ms the last outpulsing edge of the previous digit.

FIGURE 4
COMPONENT SELECTION FOR OSCILLATOR/CLOCK FREQUENCY



$f_{cl} = \sqrt{\frac{7.118}{LC}}$ where f_{cl} in kHz, L in mH,
C = C1 = C2 in μF

$\%f_{cl} = -0.5\,[\%C + \%L] \pm 3.0$ where $\%f_{cl}$, %C, %L are the frequency capacitor, and inductor tolerances in percent. The ±3.0% accounts for supply voltage and ambient temperature variations.

EXAMPLE

L	%L	C=C1=C2	%C	f_{cl}	$\%f_{cl}$	OUTPULSING RATE $f_{OPL} = f_{cl}/1.6$
5.0 mH	±5.0	0.04 μF	±5.0	≈16 kHz	±8.0	≈10 pps
5.0 mH	±5.0	0.01 μF	±5.0	≈32 kHz	±8.0	≈20 pps

FIGURE 5
TRUTH TABLE

INPUTS							OUTPUTS	
$\overline{CRQ}$	D4 D3 D2 D1	ST	$\overline{RED}$	$\overline{HOL}$	IDT	MBR	$\overline{OPL}$	DRO †
1	X X X X	X	X	X	X	X	0	0
0	X X X X	0	1	1	X	X	1 (Steady State)	0 (Steady State)
0	X X X X (nth Digit)	⊓	1	1	X	X	Number of pulses (⊓) of nth digit = binary combination of D4, D3, D2, D1. *	1 During outpulsing 0 Otherwise
0	X X X X	0	⊓	1	X	X	Digits of number in memory re-sent.	1 During outpulsing 0 Otherwise
0	X X X X	X	1	0	X	X	1 { After conclusion of digit being outpulsed.	0 { After conclusion of digit being outpulsed
X	X X X X	X	X	X	0 1	X	300 ms Interdigit time 800 ms Interdigit time } f_{cl} = 16 kHz	
X	X X X X	X	X	X	X	0 1	61% (≈1.6:1) Make-Break Ratio 67% (≈2:1) Make-Break Ratio	

X = Don't Care
* With the exception of 0000 which will give 10 pulses.
† Refer to timing diagram Figure 3.

FIGURE 6
MEMORY CLEAR

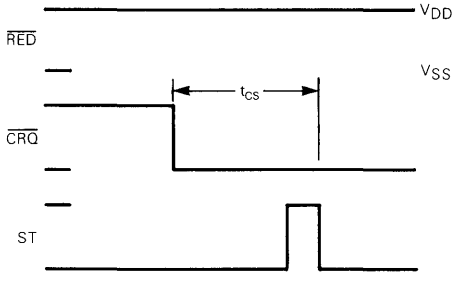
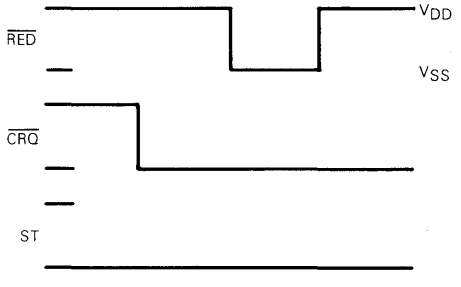


FIGURE 7
REDIAL SEQUENCE



DEVICE OPERATION

OSCILLATOR (Osc, Pin 1)

This pin is an input to the internal oscillator and feedback connection for the L-C π-network. An external clock signal, if desired can be applied to Osc.

CLOCK (Clk, Pin 2)

This pin is an output from the internal oscillator and feedback connection for the L-C π-network and provides the system clock for the MC14419 bounce eliminator circuitry.

STROBE INPUT (ST, Pin 3)

This Strobe input, when high (ST = V_{DD}), signifies that the data at the D1, D2, D3, and D4 inputs is valid, and enters the 4-bit number into the internal FIFO (First-In, First-Out) memory for subsequent outpulsing. The first strobe pulse after a call is requested (CRQ = low) clears the memory of any previous number and enters the first digit of the new number. Successive strobe pulses will store up to a maximum of 16 digits in the internal FIFO memory, which ignores all digits entered in excess of that amount until a new call is requested.

DATA INPUTS (D4, D3, D2, D1, Pins 4, 5, 6, 7)

These pins are the Data inputs to the internal memory. A binary coded digit number entered will result in an equivalent number of pulses at the $\overline{OPL}$ (outpulsing) output, except for the code 0000, which will outpulse 10 pulses.

NEGATIVE POWER SUPPLY (V_{SS}, Pin 8)

This pin is the negative power supply connection. Normally this pin is system ground.

HOLD ($\overline{HOL}$, Pin 9)

When taken low ($\overline{HOL}$ = V_{SS}), the Hold input disables the outpulsing at the completion of the digit being outpulsed. When taken high, outpulsing resumes. This feature can be used in multi-dial-tone phone systems to provide longer interdigit pauses when necessary.

RE-DIAL ($\overline{RED}$, Pin 10)

The Re-Dial input, when taken low ($\overline{RED} = V_{SS}$) automatically outpulses the digits entered into memory after the last time a call was requested. (See Redial Sequence Diagram Figure 6.)

OUTPULSING ($\overline{OPL}$, Pin 11)

The Outpulsing output sends out bursts of pulses equivalent to the digits of the telephone number stored in the memory. The duty cycle and interdigit time of the digit pulse bursts are controlled, respectively by the MBR (Pin 15) and IDT (Pin 14).

DIAL ROTATING OUTPUT (DRO, Pin 12)

The Dial Rotating (also known as "Off Normal") Output provides a signal which indicates that digit pulse bursts are being sent. In the MC14409, DRO goes high (V_{DD}) at the beginning of the first digit pulse burst and goes low (V_{SS}) between succeeding consecutive digit pulse bursts. In the MC14408, however, DRO goes high at the beginning of the first digit pulse burst and remains high until the last digit pulse burst of the telephone number has been sent (see Timing Diagram, Figure 3).

CALL REQUEST ($\overline{CRQ}$, Pin 13)

The Call Request input when taken low ($\overline{CRQ} = V_{SS}$) resets internal counters and prepares the internal logic to either accept new digit inputs to be dialed, or to re-dial (see RED, Pin 10) the digits stored in the memory. The Relationship Between Memory Clear and Redial is shown in Figure 7.

INTERDIGIT TIME (IDT, Pin 14)

The Interdigit Timing input determines the length of time between consecutive digit pulse bursts. See the Interdigit Time (t_{ID}) in the switching characteristics for the length of time.

MAKE-BREAK RATIO (MBR, Pin 15)

The Make-to-Break Ratio input controls the duty cycle of the digit pulse bursts at the $\overline{OPL}$ output. For MBR = V_{DD}, duty cycle = 67% low, 33% high; and for MBR = V_{SS}, duty cycle = 61% low, 39% high.

POSITIVE POWER SUPPLY (V_{DD}, Pin 16)

This pin is the package positive power supply pin.

FIGURE 8 — KEYPAD TO PULSE DIALER FLOW DIAGRAM

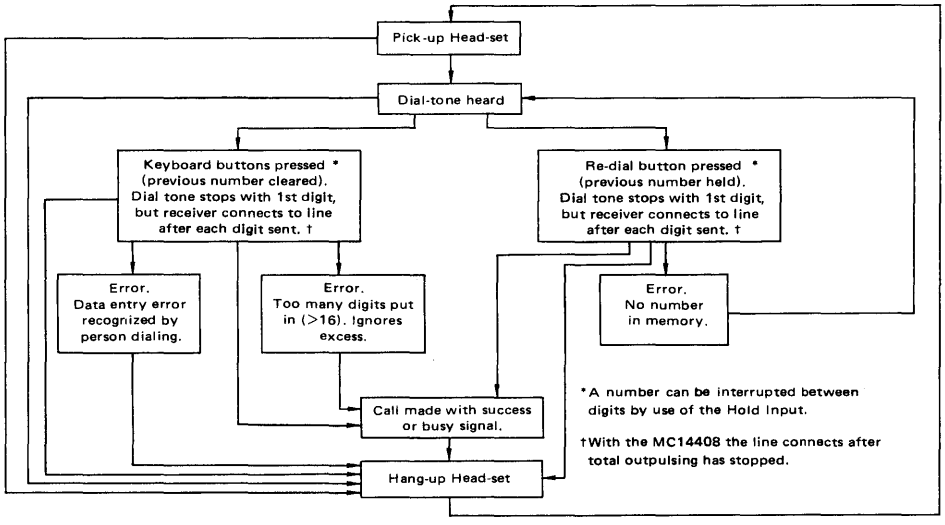


FIGURE 9 — PHONE DIALER SYSTEM

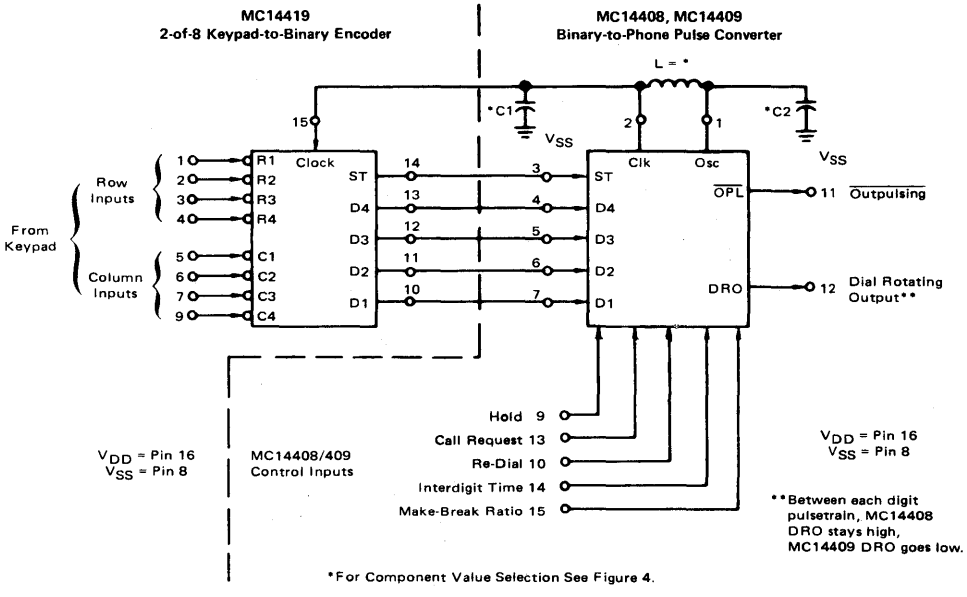


FIGURE 10 — STANDARD K-500 TELEPHONE

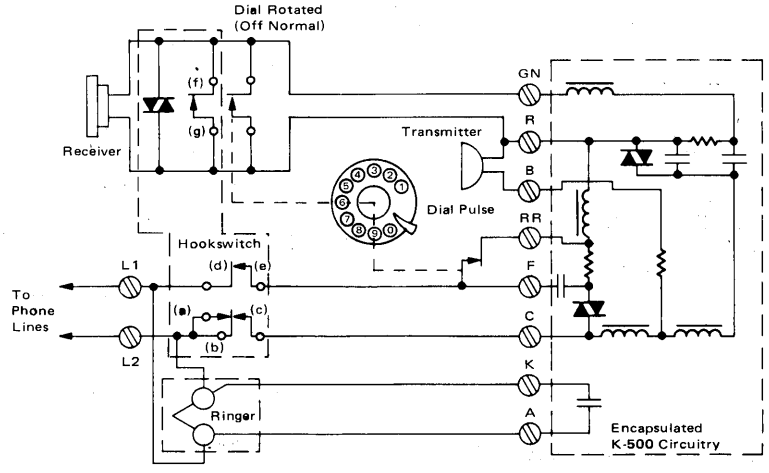
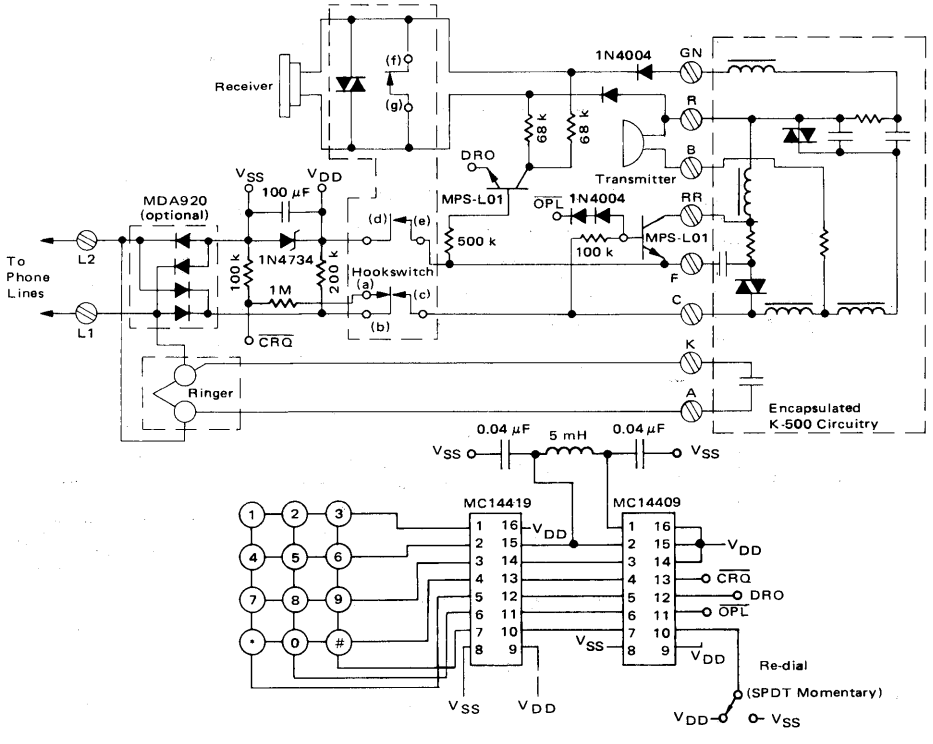


FIGURE 11 — MODIFIED K-500 TELEPHONE



MOTOROLA

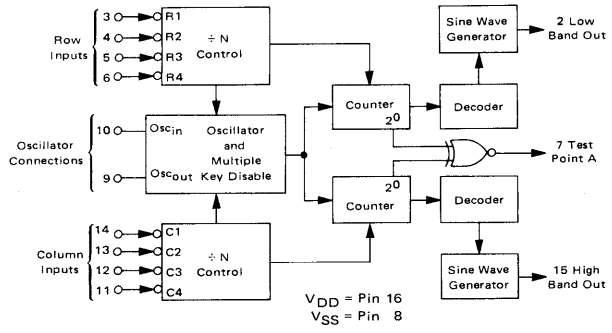
MC14410

2-OF-8 TONE ENCODER

The MC14410 2-of-8 tone encoder is constructed with complementary MOS enhancement mode devices. It is designed to accept digital inputs in a 2-of-8 code format and to digitally synthesize the high and low band sine waves specified by telephone tone dialing systems. The inputs are normally originated from a 4 x 4 matrix keypad, which generates 4 row and 4 column input signals in a 2-of-8 code format (1 row and 1 column are simultaneously connected to V_{SS}). The master clocking for the MC14410 is achieved from a crystal controlled oscillator which is included on the chip. Internal clocks, which operate the logic, are enabled only by one or more row and column signals being activated simultaneously. The two sine wave outputs have NPN bipolar structures on the same substrate which allows for low output impedance and large source currents. Applications of this device include telephone tone dialing, radio and mobile telephones, process control, point-of-sale terminals, and credit card verification terminals.

- Diode Protection on All Inputs
- Noise Immunity = 45% of V_{DD} Typical
- Supply Voltage Range = 4.4 Vdc to 6.0 Vdc
- On-Chip Oscillator (Crystal or External Clock Source may be applied to Pin 10)
- On-Chip Pull-Up Resistors on Row and Column Inputs
- Designed with Multiple Key Lockout (Eliminates Need for Mechanical Lockout in Keypad)
- Two Sine Wave Generators On-Chip
- Frequency Accuracy ±0.2%
- Low Harmonic Distortion
- Single Tone Capability
- Fast Oscillator Turn-On and Turn-Off Times

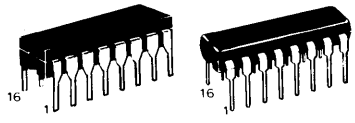
BLOCK DIAGRAM



CMOS LSI

(LOW-POWER COMPLEMENTARY MOS)

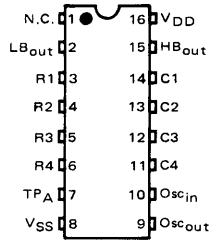
2-OF-8 TONE ENCODER



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

PIN ASSIGNMENT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit. A destructive high-current mode may occur if V_{in} and V_{out} are not constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Due to the sourcing capability of this circuit, damage can occur to the device if V_{DD} is applied, and the outputs are shorted to V_{SS} and are at a peak sinewave voltage.

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8.)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +6.0	Vdc
Input Voltage, All Inputs	V_{in}	V_{SS} -0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range	T_A	-40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	-40°C Min	-40°C Max	25°C Min	25°C Typ	25°C Max	+85°C Min	+85°C Max	Unit
Supply Voltage	V_{DD}	–	4.4	6.0	4.4	5.0	6.0	4.4	6.0	Vdc
Output Voltage "0" Level Pins 7 and 9	V_{out}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
"1" Level		5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
Input Voltage (V_O = 4.5 or 0.5 Vdc) "0" Level	V_{IL}	5.0	–	1.5	–	2.25	1.5	–	1.5	Vdc
(V_O = 0.5 or 4.5 Vdc) "1" Level	V_{IH}	5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
Output Drive Current (V_{OH} = 2.5 Vdc) Source Pin 7	I_{OH}	5.0	-0.05	–	-0.05	-0.4	–	-0.04	–	mAdc
Pin 9			-0.23	–	-0.20	-1.7	–	-0.16	–	
(V_{OL} = 0.4 Vdc) Sink Pin 7	I_{OL}	5.0	0.05	–	0.05	0.20	–	0.04	–	mAdc
Pin 9			0.23	–	0.20	0.78	–	0.16	–	
Input Pull-Up Resistor Source Current (V_{in} = 0 Vdc) Pins 3-6, 11-14	I_{IL}	6.0	–	140	–	30	100	–	80	μAdc
Input Capacitance (V_{in} = 0 Vdc)	C_{in}	–	–	–	–	5.0	–	–	–	pF
Quiescent Current	I_Q	4.4	–	0.48	–	0.2	0.4	–	0.33	mAdc
		6.0	–	1.3	–	0.55	1.1	–	0.9	
Total Supply Current (Dynamic plus Quiescent) (R_L = 15 kΩ, f = 1 MHz)	I_T	4.4	–	1.7	–	0.7	1.4	–	1.15	mAdc
		6.0	–	3.5	–	1.45	2.9	–	2.4	
Low Band Output Voltage Swing Pin 2 Only (R_L = 100 k)	V_{Lpp}	4.4	400	600	500	600	700	550	750	mVpp
		6.0	800	1000	900	1000	1100	950	1150	
High Band Output Voltage Swing Pin 15 Only (R_L = 100 k)	V_{Hpp}	4.4	600	900	700	850	1000	800	1100	mVpp
		6.0	1000	1400	1100	1350	1500	1200	1600	
Low Band–High Band Voltage Differential	ΔV	5.0	–	–	–	2.5	–	–	–	dB
Low Band–High Band Pin 2,15 Output Impedance AC only	z_o	–	–	–	–	80	–	–	–	Ω
Low Band–High Band Pin 2,15 2nd thru 14th Harmonics (R_L = 15 kΩ)	V_{2H}–V_{14H}	4.4 to 6.0	–	-20	–	-30	-25	–	-25	dB
Maximum Clock Pulse Frequency	f_{cl}	4.4	–	–	–	1.0	–	1.1	–	MHz
Turn-on Time (Power on to oscillation)	t_{on}	5.0	–	–	–	8.0	–	–	–	ms

TABLE 1 – FUNCTIONAL TRUTH TABLE

ACTIVE LOW INPUTS		OUTPUTS	
Activated Row Lines	Activated Column Lines	Low Band Pin 2	High Band Pin 15
None	X**	dc level	dc level
X**	None	dc level	dc level
One	One	f_L*	f_H*
Two or more	One	dc level	f_H*
One	Two or more	f_L*	dc level
Two or more	Two or more	dc level	dc level

*See Table 2
**X = Don't care

TABLE 2 – OUTPUT FREQUENCY TABLE

Input Line Activated (low)	Frequency Generated**	
	f_L (Hz)	f_H (Hz)
R1	697	–
R2	770	–
R3	852	–
R4	941	–
C1	–	1209
C2	–	1336
C3	–	1477
C4	–	1633

**All frequencies are accurate to ±0.2% (crystal tolerance not included).

2

FIGURE 1 – TYPICAL SINE WAVE OUTPUT
(Pins 2 or 15, No External Filtering)

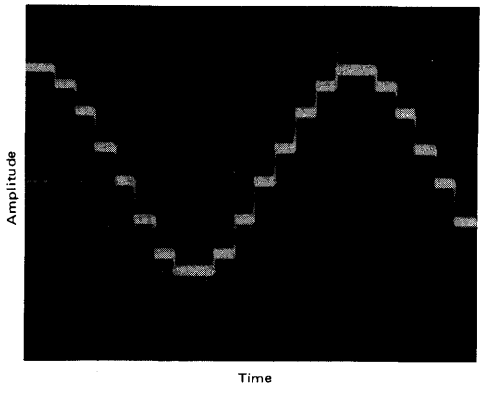


FIGURE 2 – TYPICAL FREQUENCY SPECTRUM
(Pins 2 or 15, No External Filtering)

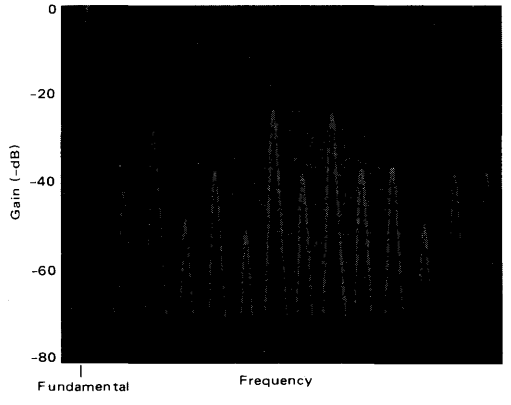


FIGURE 3 – TYPICAL CRYSTAL CIRCUIT

R_f = 15 MΩ ± 10%

CRYSTAL SPECIFICATION

Crystal Mode	Parallel
Frequency	1 MHz ± 0.1%
R_S	540Ω typ
C_0	7.0 pF typ
Temperature Range	-40°C to +85°C
Test Level	1 mW
Test Set	TS–330/TSM or Equivalent

*Recommended Crystals: CTS KNIGHT

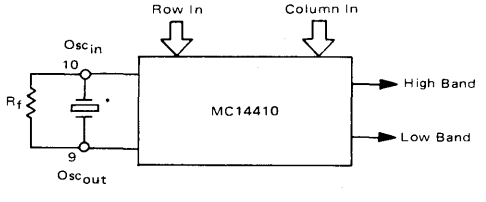


FIGURE 4 – TYPICAL TELEPHONE INTERFACE APPLICATION

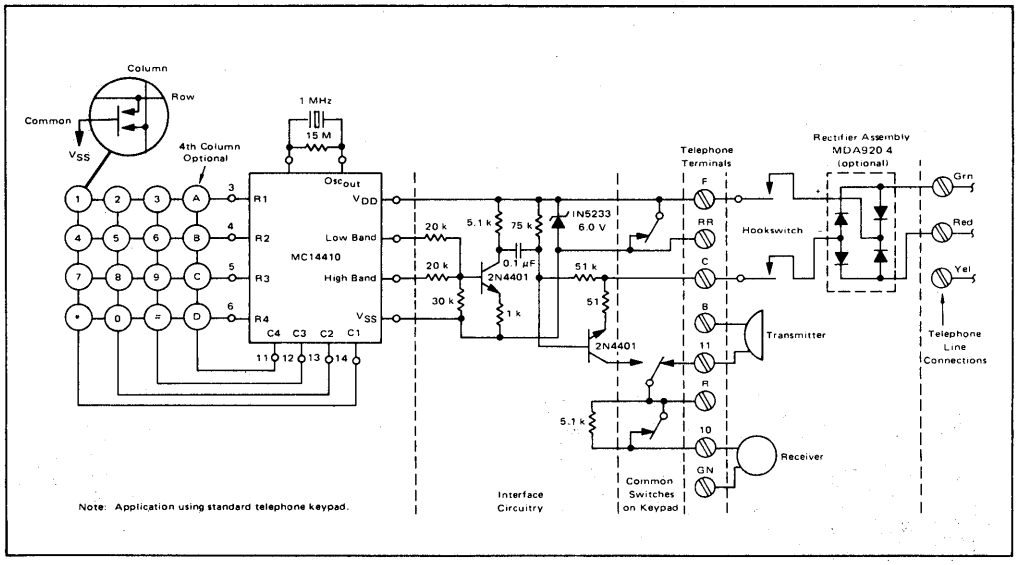


FIGURE 5 – LOW LEVEL OUTPUT TONE GENERATOR APPLICATION

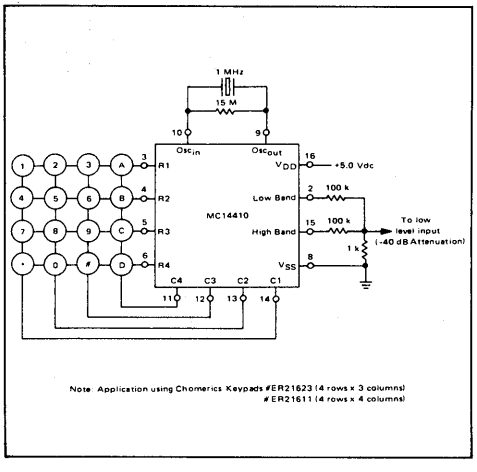
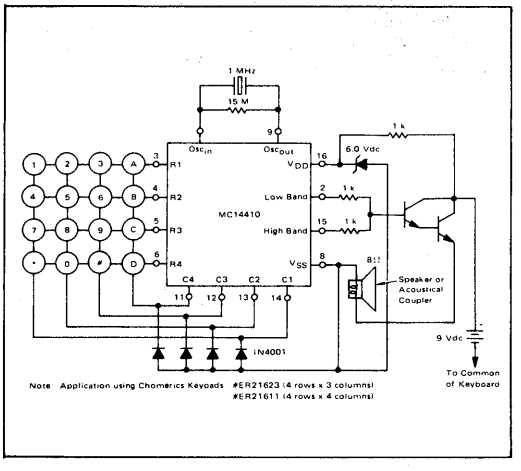


FIGURE 6 – BATTERY POWERED OPERATION (Driving Audio Speaker)



MOTOROLA

MC14411

BIT RATE GENERATOR

The MC14411 bit rate generator is constructed with complementary MOS enhancement mode devices. It utilizes a frequency divider network to provide a wide range of output frequencies.

A crystal controlled oscillator is the clock source for the network. A two-bit address is provided to select one of four multiple output clock rates.

Applications include a selectable frequency source for equipment in the data communications market, such as teleprinters, printers, CRT terminals, and microprocessor systems.

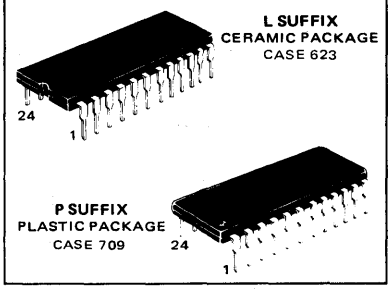
- Single 5.0 Vdc (±5%) Power Supply
- Internal Oscillator Crystal Controlled for Stability (1.8432 MHz)
- Sixteen Different Output Clock Rates
- 50% Output Duty Cycle
- Programmable Time Bases for One of Four Multiple Output Rates
- Buffered Outputs Compatible with Low Power TTL
- Noise Immunity = 45% of V_{DD} Typical
- Diode Protection on All Inputs
- External Clock May be Applied to Pin 21
- Internal Pullup Resistor on Reset Input

CMOS LSI

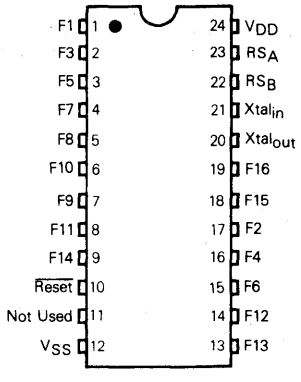
(LOW-POWER COMPLEMENTARY MOS)

BIT RATE GENERATOR

2



PIN ASSIGNMENT

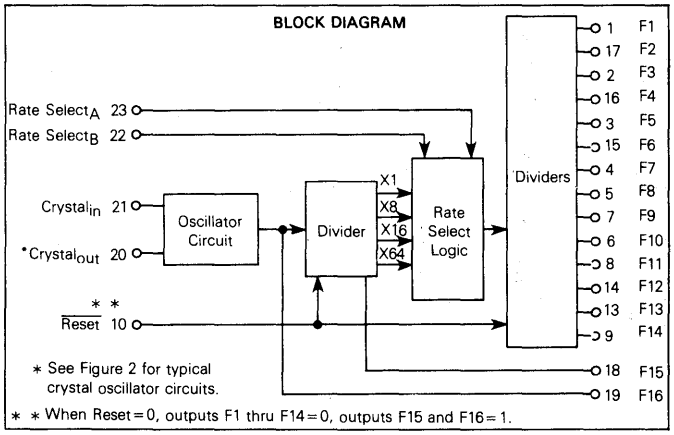


V_{DD} = Pin 24
V_{SS} = Pin 12

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 12.)

Rating	Symbol	Value	Unit
DC Supply Voltage Range	V_{DD}	5.25 to −0.5	V
Input Voltage, All Inputs	V_{in}	V_{DD} + 0.5 to V_{SS} − 0.5	V
DC Current Drain per Pin	I	10	mA
Operating Temperature Range	T_A	−40 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

BLOCK DIAGRAM



* See Figure 2 for typical crystal oscillator circuits.

* * When Reset = 0, outputs F1 thru F14 = 0, outputs F15 and F16 = 1.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	−40°C Min	−40°C Max	25°C Min	25°C Typ	25°C Max	+85°C Min	+85°C Max	Unit
Supply Voltage	V_{DD}	–	4.75	5.25	4.75	5.0	5.25	4.75	5.25	V
Output Voltage "0" Level	V_{out}	5.0	–	0.05	–	0	0.05	–	0.05	V
"1" Level		5.0	4.95	–	4.95	5.0	–	4.95	–	V
Input Voltage (V_O = 4.5 or 0.5 V)	V_{IL}	5.0	–	1.5	–	2.25	1.5	–	1.5	V
(V_O = 0.5 or 4.5 Vdc)	V_{IH}	5.0	3.5	–	3.5	2.75	–	3.5	–	V
Output Drive Current (V_{OH} = 2.5 V) Source	I_{OH}	5.0	−0.23	–	−0.20	−1.7	–	−0.16	–	mA
(V_{OL} = 0.4 V) Sink	I_{OL}	5.0	0.23	–	0.20	0.78	–	0.16	–	mA
Input Current Pins 21, 22, 23	I_{in}	–	–	±0.1	–	±0.00001	±0.1	–	±1.0	μA
Pin 10		5.0	–	–	−1.5	–	−7.5	–	–	μA
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	–	–	–	pF
Quiescent Dissipation	P_Q	5.0	–	2.5	–	0.015	2.5	–	15	mW
Power Dissipation**† (Dynamic plus Quiescent) (C_L = 15 pF)	P_D	5.0	$P_D = (7.5\ mW/MHz)\ f + P_Q$							mW
Output Rise Time** t_r = (3.0 ns/pF) C_L + 25 ns	t_{TLH}	5.0	–	–	–	70	200	–	–	ns
Output Fall Time** t_f = (1.5 ns/pF) C_L + 47 ns	t_{THL}	5.0	–	–	–	70	200	–	–	ns
Input Clock Frequency	f_{CL}	5.0	–	1.85	–	–	1.85	–	1.85	MHz
Clock Pulse Width	$t_{W(C)}$	–	200	–	200	–	–	200	–	ns
Reset Pulse Width	$t_{W(R)}$	–	500	–	500	–	–	500	–	ns

†For dissipation at different external capacitance (C_L) refer to corresponding formula:
$P_T(C_L = P_D + 2.6 \times 10^{-3}(C_L - 15\ pF)\ V_{DD}{}^2 f$
where: P_T, P_D in mW, C_L in pF, V_{DD} in Vdc, and f in MHz.
**The formula given is for the typical characteristics only.

TABLE 1 — OUTPUT CLOCK RATES

Rate Select B	Rate Select A	Rate
0	0	X1
0	1	X8
1	0	X16
1	1	X64

Output Number	Output Rates (Hz) X64	X16	X8	X1
F1	614.4 k	153.6 k	76.8 k	9600
F2	460.8 k	115.2 k	57.6 k	7200
F3	307.2 k	76.8 k	38.4 k	4800
F4	230.4 k	57.6 k	28.8 k	3600
F5	153.6 k	38.4 k	19.2 k	2400
F6	115.2 k	28.8 k	14.4 k	1800
F7	76.8 k	19.2 k	9600	1200
F8	38.4 k	9600	4800	600
F9	19.2 k	4800	2400	300
F10	12.8 k	3200	1600	200
F11	9600	2400	1200	150
F12	8613.2	2153.3	1076.6	134.5
F13	7035.5	1758.8	879.4	109.9
F14	4800	1200	600	75
F15	921.6 k	921.6 k	921.6 k	921.6 k
F16*	1.843 M	1.843 M	1.843 M	1.843 M

*F16 is buffered oscillator output.

FIGURE 1 — DYNAMIC SIGNAL WAVEFORMS

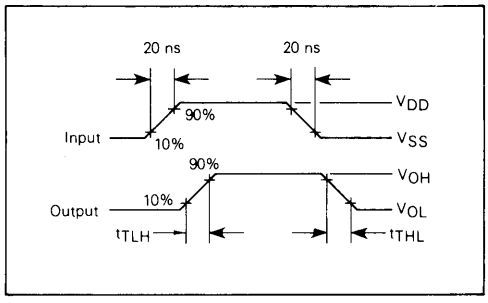
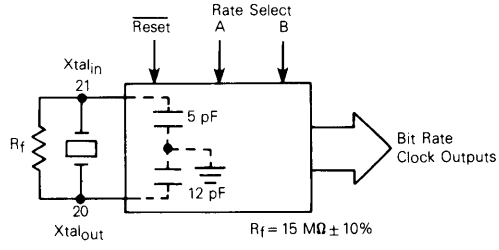


FIGURE 2 — TYPICAL CRYSTAL OSCILLATOR CIRCUIT



Crystal Specifications

Crystal Mode	Parallel
Frequency	1.8432 MHz ±0.05%@13 pF
R_S	540 Ω max
C_0	7.0 pF max
Temperature Range	0 to 70°C
Test Level	1 mW
Test Set	TS — 330/TSM or Equivalent

*Suggested Crystal Suppliers:
Tyco, CTS Knights

Circuit diagrams utilizing Motorola products are included as a means of illustrating typical semiconductor applications; consequently, complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of Motorola Inc., or others.

MOTOROLA

MC14412

2

CMOS LSI

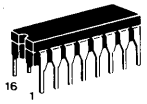
(LOW-POWER COMPLEMENTARY MOS)

UNIVERSAL LOW SPEED (0-600 bps) MODEM

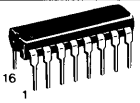
UNIVERSAL LOW SPEED MODEM (0-600 bps)

The MC14412 contains a complete FSK (Frequency-Shift Keying) modulator and demodulator compatible with both foreign (C.C.I.T.T. standards) and U.S.A. low speed (0 to 600 (bps) communication networks.

- On-Chip Crystal Oscillator with External Crystal
- Echo Suppressor Disable Tone Generator
- Originate and Answer Modes
- Simplex, Half-Duplex, and Full-Duplex Operation
- On-Chip Sine Wave Generator
- Modem Self Test Mode
- Single Supply:
  V_{DD} = 4.75 to 15 Vdc MC14412FP, MC14412 FL
  V_{DD} = 4.75 to 6.0 Vdc MC14412VP, MC14412VL
- Selectable Data Rates: 0-300, 0-600 bps
- Post Detection Filter
- TTL or CMOS Compatible Inputs and Outputs



L SUFFIX
CERAMIC PACKAGE
CASE 620

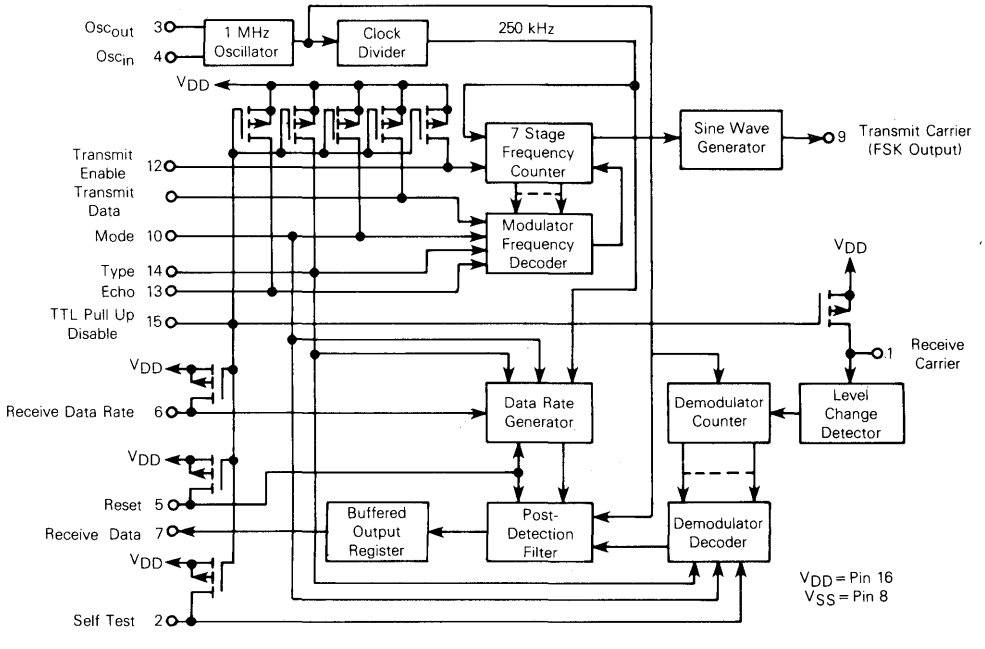


P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC144XX — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- F 4.75 to 15 Vdc
- V 4.75 to 6.0 Vdc

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD}** Vdc	−40°C Min	−40°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit
Output Voltage Pin 7 Only										
"0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	V
$V_{in} = V_{DD}$ or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	V
$V_{in} = 0$ or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage*										
"0" Level										
($V_O = 4.5$ or 0.5 V)	V_{IL}	5.0	–	1.5	–	2.25	1.5	–	1.5	V
($V_O = 9.0$ or 1.0 V)		10	–	3.0	–	4.50	3.0	–	3.0	
($V_O = 13.5$ or 1.5 V)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level										
Pin 15		5 to 15	$V_{DD} - 0.75$	–	$V_{DD} - 0.8$	$V_{DD} - 2$	–	$V_{DD} - 0.85$	–	
($V_O = 0.5$ or 4.5 V)		5.0	3.5	–	3.5	2.75	–	3.5	–	
($V_O = 1.0$ or 9.0 V)	V_{IH}	10	7.0	–	7.0	5.50	–	7.0	–	V
($V_O = 1.5$ or 13.5 V)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current										
Pin 7 Only										
($V_{OH} = 2.5$)	I_{OH}	5	−0.62	–	−0.5	−1.5	–	−0.35	–	mA
($V_{OH} = 9.5$)		10	−0.62	–	−0.5	−1.0	–	−0.35	–	
($V_{OH} = 13.5$)		15	−1.8	–	−1.5	−3.6	–	−1.1	–	
($V_{OL} = 0.4$)	I_{OL}	4.75	2.3	–	2.0	4.0	–	1.6	–	mA
($V_{OL} = 0.5$)		10	5.3	–	4.5	10	–	3.6	–	
($V_{OL} = 1.5$)		15	15	–	13	35	–	10	–	
Input Current (Pin 15 = V_{DD})	I_{in}	–	–	–	–	±0.00001	±0.1	–	–	µA
Input Pull-Up Resistor Source Current (Pin 15 = V_{SS}, $V_{in} = 2.4$ Vdc) Pins 1, 2, 5, 6, 10, 11 12, 13, 14	I_P	5	285	–	250	460	–	205	–	µA
Input Capacitance	C_{in}	–	–	–	–	5.0	–	–	–	pF
Total Supply Current (Pin 15 = V_{DD})	I_T	5	–	4.5	–	1.1	4.0	–	3.5	mA
		10	–	13	–	4.0	12	–	11	
		15	–	27	–	8.0	25	–	23	
Modulator/Demodulator Frequency Accuracy (Excluding Crystal)	ACC	5 to 15	–	–	–	0.5	–	–	–	%
Transmit Carrier Output 2nd Harmonic	V_{2H}	5	–	–	−20	−25	–	–	–	dB
		15	–	–	−25	−32	–	–	–	
Transmit Carrier Output Voltage ($R_L = 100$ kΩ) (Pin 9)	V_{out}	5	–	–	0.2	0.30	–	–	–	V_{RMS}
		10	–	–	0.5	0.85	–	–	–	
		15	–	–	1.0	1.5	–	–	–	
Maximum Receive Carrier Rise and Fall Times (Pin 1)	t_r, t_f	5	–	15	–	–	15	–	15	µs
		10	–	5.0	–	–	5.0	–	5.0	
		15	–	4.0	–	–	4.0	–	4.0	
Maximum Oscillator Frequency	f_{max}	5	–	–	1.2	5	–	–	–	MHz
Minimum Clock Pulse Width	t_w	5	–	–	–	50	350	–	–	ns

*DC Noise Immunity (V_{IL}, V_{IH}) is defined as the maximum voltage change from an ideal "0" or "1" input level, that the circuit will withstand before accepting an erroneous input.

**Note: Only 5-Volt specifications apply to MC14412VP devices.

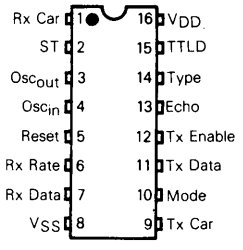
MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8)

Rating	Symbol	Value	Unit
DC Supply Voltages MC14412FP, FL MC14412VP, VL	V_{DD}	−0.5 to 15 −0.5 to 6.0	V
Input Voltages, All Inputs	V_{in}	V_{DD} + 0.5 to V_{SS} − 0.5	V
DC Current Drain per Pin (except Pin 8, 7)	I	10	mA
DC Current Drain (Pin 8, 7)	I	35	mA
Operating Temperature Range	T_A	−40 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

PIN ASSIGNMENT



DEVICE OPERATION

GENERAL

Figure 1 shows the modem in a system application. The data to be transmitted is presented in serial format to the modulator for conversion to FSK signals for transmission over the telephone network. The modulator output is buffered/amplified before driving the 600 ohm telephone line.

The FSK signal from the remote modem is received via the telephone line and filtered to remove extraneous signals such as the local Transmit Carrier. This filtering can be either a bandpass which passes only the desired band of frequencies or a notch which rejects the known interfering signal. The desired signal is then limited to preserve the axis crossings and fed to the demodulator where the data is recovered from the received FSK carrier.

INPUT/OUTPUT FUNCTIONS

Figure 2 shows the I/O interface for the MC14412 low-speed modem. The following is a description of each individual signal.

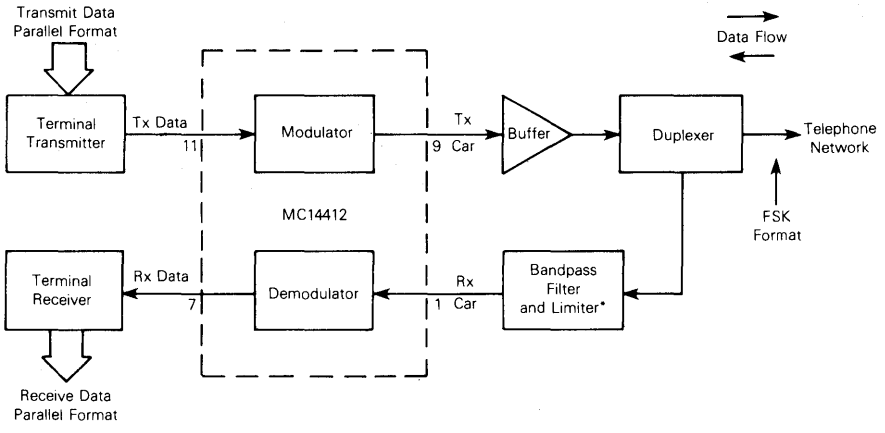
TYPE (Pin 14)

The Type input selects either the U.S. or C.C.I.T.T. operational frequencies for both transmitting and receiving data. When the Type input = "1", the U.S. standard is selected and when the Type input = "0", the C.C.I.T.T. standard is selected.

TRANSMIT DATA (Tx Data, Pin 11)

Transmit Data is the binary information input. Data entered for transmission is modulated using FSK techniques. When operating in the U.S. standard (Type = "1") a logic "1" input level represents a Mark or when operating in the CCITT standard (Type = "0") a logic "1" input level represents a Mark.

FIGURE 1 — TYPICAL LOW-SPEED MODEM APPLICATION



Since the modulator and demodulator sections of the MC14412 are functionally equivalent to those of the MC6860, additional application information can be obtained from the following Motorola publications:

AN-731 Low-speed Modem Fundamentals

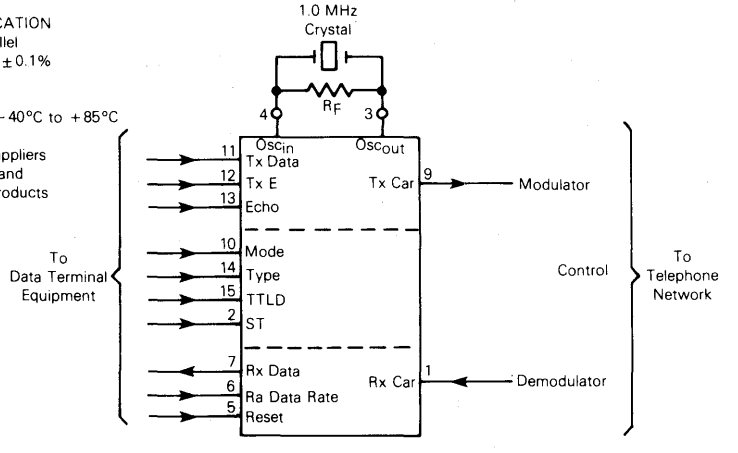
AN-747 Low-speed Modem System Design Using the MC6860

EB-49 Application Performance of the MC6860 MODEM.

FIGURE 2 — MC14412 INPUT/OUTPUT SIGNALS

*CRYSTAL SPECIFICATION
Crystal Mode — Parallel
Frequency — 1 MHz ±0.1%
R_S = 540 Ω typ
C_O = 7 pF typ
Temperature Range −40°C to +85°C
Test Level — 1 mW
Suggested Crystal Suppliers
Tyco, CTS Knight and
Motorola Crystal Products

R_F = 15 mΩ ±20%



TRANSMIT CARRIER (Tx Car, Pin 9)

The Transmit Carrier is a digital-synthesized sine wave derived from a 1.0 MHz oscillator reference. The Tx CAR has an AC output impedance of 5 kΩ typical. The frequency characteristics are as follows:

United States Standard
Type = "1"
Echo = "0"

Mode		Tx Data		Tx Car
Originate	"1"	Mark	"1"	1270 Hz
Originate	"1"	Space	"0"	1070 Hz
Answer	"0"	Mark	"1"	2225 Hz
Answer	"0"	Space	"0"	2025 Hz

C.C.I.T.T. Standard
Type = "0"
Echo = "0"

Mode		Tx Data		Tx Car
Channel	"1"	Mark	"1"	980 Hz
No. 1	"1"	Space	"0"	1180 Hz
Channel	"0"	Mark	"1"	1650 Hz
No. 2	"0"	Space	"0"	1850 Hz

Echo Suppressor Disable Tone
Type = "0"
Echo = "1"

Mode	Tx Data	Tx Car
Chan. No. 2 "0"	"1"	2100 Hz

TRANSMIT ENABLE (Tx Enable, Pin 12)

The Transmit Carrier output is enabled when the Tx Enable input = "1". No output tone can be transmitted when Tx Enable = "0".

MODE (Pin 10)

The Mode input selects the pair of transmitting and receive frequencies used during modulation and demodulation. When Mode = "1", the U.S. originate mode is selected (Type input = "1") or the C.C.I.T.T. Channel No. 1 (Type input = "0"). When mode = "0", the U.S. answer mode is selected (Type input = "1") or the C.C.I.T.T. Channel No. 2 (Type input = "0").

ECHO (Pin 13)

When the Echo input = "1" (Type = "0", Mode = "0", Tx Data = "1") the modulator will transmit a 2100 Hz tone for disabling line echo suppressors. During normal data transmission, this input should be low = "0".

RECEIVE DATA (Rx Data, Pin 7)

The Receive Data output is the digital data resulting from demodulating the Receive Carrier.

RECEIVE CARRIER (Rx Car, Pin 1)

The Receive Carrier is the FSK input to the demodulator. This input must have either a CMOS or TTL compatible logic level input (see TTL pull-up disable) at a duty cycle of 50% ±2%, that is a square wave resulting from a signal limiter.

RECEIVE DATA RATE (Rx Rate, Pin 6)

The demodulator has been optimized for signal to noise performance at 300, and 600 bps.

Data Rate	Rx Rate
0-300 bps	"1"
0-600 bps	"0"

SELF TEST (ST, Pin 2)

When a high level (ST = "1") is placed on this input, the demodulator is switched to the modulator frequency and demodulates the transmitted FSK signal.

RESET (Pin 5)

This input is provided to decrease the test time of the chip. In normal operation, this input may be used to disable the demodulator (Reset = "1") — otherwise it should be tied low = "0". The reset pin does not reset Rx data pin 7.

CRYSTAL (Osc_{in}, Osc_{out}, Pin 4, Pin 3, respectively)

A 1.0 MHz crystal is required to utilize the on chip oscillator. A 1.0 MHz square wave clock can also be applied to the Osc_{in} input to satisfy the clock requirement (see Figure 2).

When utilizing the 1.0 MHz crystal, external parasitic capacitance, including crystal shunt capacitance, must be <9 pF at the crystal input (pin 4). Pin 3 is capable of driving only one CMOS input.

TTL PULL-UP DISABLE (TTLD, Pin 15)

To improve TTL interface compatibility, all of the inputs to the MODEM have controllable P-Channel devices which act as pull-up resistors when TTLD input is low ("0"). When the input is taken high ("1") the pull-up is disabled, thus reducing power dissipation when interfacing with CMOS. Pin 15 should be taken high ("1") with V_{DD} greater than 6 volts.

FIGURE 3 — M6800 MICROCOMPUTER FAMILY BLOCK DIAGRAM

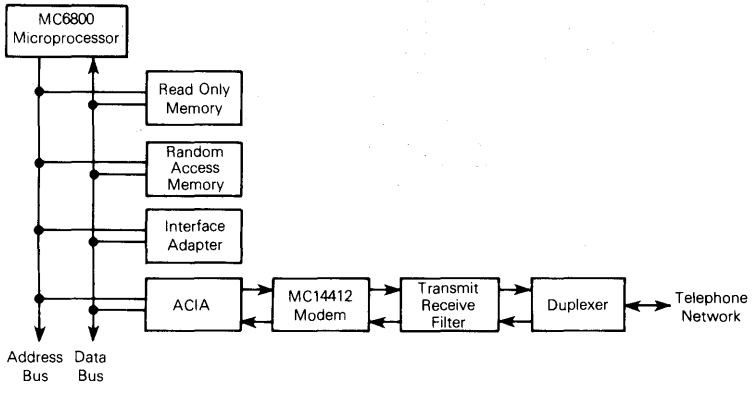


FIGURE 4 — TRANSMIT CARRIER SINEWAVE

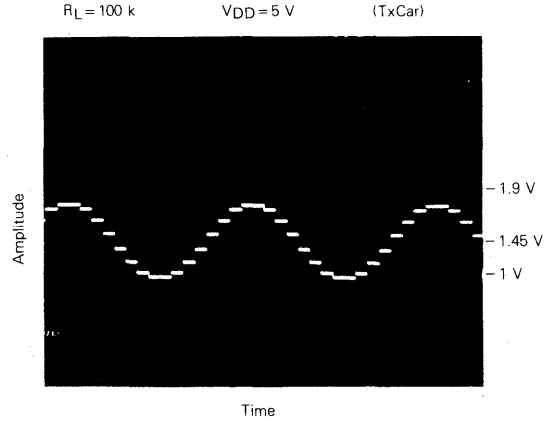
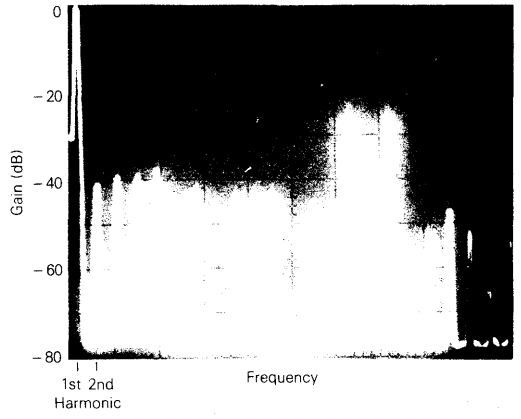


FIGURE 5 — TYPICAL TRANSMIT CARRIER FREQUENCY SPECTRUM



MOTOROLA

MC14413-1
MC14413-2
MC14414-1
MC14414-2

CMOS LSI

(LOW-POWER COMPLEMENTARY MOS)

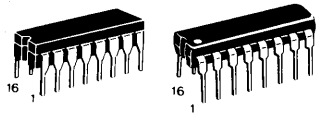
PULSE CODE MODULATION SAMPLED DATA FILTERS

2

PULSE CODE MODULATION SAMPLED DATA FILTERS

The MC14413-1, -2 and MC14414-1, -2 are sampled data, switched capacitor filter ICs intended to provide the band limiting and signal restoration filtering necessary in PCM Codec voice digitization systems. Both ICs are capable of operating from either a single or split power supply and can be powered-down when not in use. Included on both chips are two totally uncommitted op amps for use elsewhere in the systems as I to V converters, gain adjust buffers, etc.

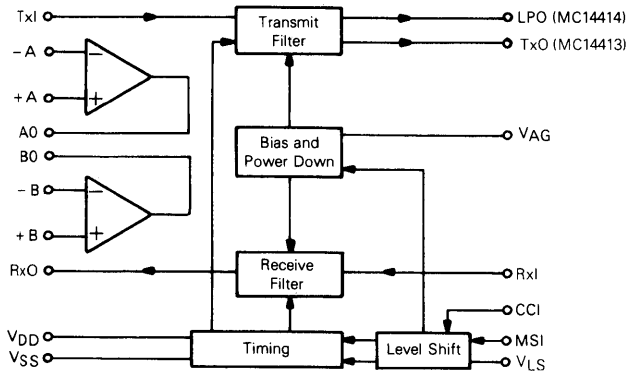
- Transmit Band-pass and Receive Low-pass (MC14413-1, -2)
- Transmit and Receive Low-pass (MC14414-1, -2)
- D3/D4 Specifications (MC14414-2/13-2)
- CCITT Specification (MC14414-1/13-1)
- Low Operating Power Consumption — 30 mW (Typical)
- Power Down Capability — 1 mW (Maximum)
- Single Supply Capability when Used with MC14404/6/7 Codecs
- ±5 to ±8 Volt Power Supply Ranges
- Receive Filter Compatible with 15% to 100% Duty Cycle PAM Inputs with Sinx/x Correction
- No Precision Components Required (MC14413-1, -2)
- TTL Compatible Inputs Using V_{LS} Pin
- Two Operational Amplifiers Available to Reduce System Component Count



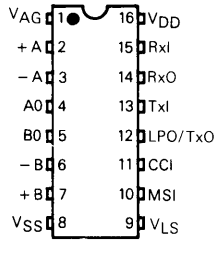
L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

BLOCK DIAGRAM



PIN ASSIGNMENT



MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}-V_{SS}	−0.5 to 18	V
Input Voltage, All Pins	V_{in}	−0.5 to V_{DD} +0.5	V
DC Current Drain per Pin (Excluding V_{DD}, V_{SS})	I	10	mA
Operating Temperature Range	T_A	−40 to 85	°C
Storage Temperature Range	T_{stg}	−65 to 150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
DC Supply Voltage	V_{DD}-V_{SS}	10	12	16	V
Convert Clock Frequency	CCI	50	128	400	kHz
Master Sync Frequency	MSI	–	8	32	kHz

DIGITAL ELECTRICAL CHARACTERISTICS (V_{SS} = 0 V)

Characteristic	Symbol	V_{DD}	0°C		25°C			85°C		Unit
		Vdc	Min	Max	Min	Typ	Max	Min	Max	
Operating Current	I_{DD}	12	–	5.0	–	2.0	4.3	–	5.0	mA
Power-Down Current (PDI = V_{SS})	I_{PD}	12	–	50	–	10	40	–	50	μA
Input Capacitance	C_{in}	12	–	–	–	5.0	7.5	–	–	pF
MODE CONTROL LOGIC LEVELS										
V_{LS} Power-Down Mode	V_{IH}	12 15	11.5 14.5	– –	11 14	11 13	– –	11.5 14.5	– –	V
V_{LS} TTL Mode	–	12 15	2 2	9.0 11.0	2.0 2.0	– –	9 12.0	2 2	9.0 11.0	V
V_{LS} CMOS Mode	V_{IL}	12 15	– –	0.8 0.8	– –	– –	0.8 0.8	– –	0.8 0.8	V
V_{AG} Power-Down Mode	V_{IH}	12 15	11.5 14.5	– –	11.5 14.5	10.5 13.5	– –	11.5 14.5	– –	V
V_{AG} Analog-Ground Mode	V_{IL}	12 15	– –	9.0 12.0	– –	– –	9.0 12.0	– –	9.0 12.0	V
CMOS LOGIC LEVELS ($V_{LS} = V_{SS}$)										
Input Current CCI	I_{in}	12	–	±1.0	–	±0.00001	±0.3	–	±1.0	μA
Input Current MSI "1" Level (Internal Pulldown Resistors) "0" Level	I_{in}	12 12	– –	200 −1.0	– –	50 −0.00001	100 −0.3	– –	200 −1.0	μA
Input Voltage CCI, MSI "0" Level	V_{IL}	12 15	– –	– –	– –	5.25 6.75	3.60 4.0	– –	– –	V
"1" Level	V_{IH}	12 15	– –	– –	9.0 11.5	6.75 8.25	– –	– –	– –	V
TTL LOGIC LEVELS (V_{LS} = 6 V, V_{SS} = 0 V)										
Input Current CCI	I_{in}	12	–	±1.0	–	±0.00001	±0.3	–	±1.0	μA
Input Current MSI "1" Level (Internal Pulldown Resistor) "0" Level	I_{in}	12 12	– –	200 −1.0	– –	30 −0.00001	– −0.3	– –	200 −1.0	μA
Input Voltage CCI, MSI "0" Level "1" Level	V_{IL} V_{IH}	12 12	– –	– –	– V_{LS} + 2.0	– –	V_{LS} + 0.8 –	– –	– –	V

ANALOG ELECTRICAL CHARACTERISTICS (V_{DD} = 12 V)

Characteristic		Symbol	0°C		25°C			85°C		Unit
			Min	Max	Min	Typ	Max	Min	Max	
Input Current	V_{AG}	I_{in}	–	±30	–	–	±10	–	±30	μA
Input Current	RxI, TxI	I_{in}	–	–	–	±0.00001	±1.0	–	±1.0	μA
AC Input Impedance (1 kHz)	RxI, TxI	Z_{in}	1.0	–	1.0	2.0	–	1.0	–	MΩ
Input Common Mode Voltage Range	TxI, RxI	V_{ICR}	–	–	1.5	–	10.5	–	–	V
Output Voltage Range	TxO, LPO, RxO									
(R_L = 20 kΩ to V_{AG})		V_{OR}	1.5	10.5	1.5	–	10.5	1.5	10.5	V
(R_L = 600 Ω to V_{AG})			2.0	9.3	2.0	–	9.3	2.0	9.3	
(R_L = 900 Ω to V_{AG})			1.5	10.5	1.5	–	10.5	1.5	10.5	
Small Signal Output Impedance (1 kHz)	TxO (MC14413)		–	–	–	50	–	–	–	
	LPO (MC14414)	Z_o	–	–	–	50	–	–	–	Ω
	RxO		–	–	–	50	–	–	–	
Output Current										
(V_O = 11 V)	TxO, LPO, RxO	I_{OH}	–5	–	–5	–6.0	–	–5	–	mA
(V_O = 1 V)	TxO, LPO, RxO	I_{OL}	5	–	5	7	–	5	–	

OP AMP PERFORMANCE ($V_{DD} - V_{SS}$ = 12 V)

Characteristic		0°C		25°C			85°C		Unit
		Min	Max	Min	Typ	Max	Min	Max	
Input Offset Voltage		–	±80	–	–	±70	–	±80	mV
Open Loop Gain	Z_L = 600 Ω + 200 pF to V_{AG}	–	–	–	45	–	–	–	dB
Input Bias Current		–	–	–	±0.1	–	–	–	μA
Output Voltage Range									
(R_L = 20 kΩ to V_{AG})		–	–	1.5	–	10.5	–	–	V
(R_L = 600 Ω to V_{AG})		–	–	2.0	–	9.3	–	–	
(R_L = 900 Ω to V_{AG})		–	–	1.5	–	10.5	–	–	
Output Current	V_{OH} 10.5	–	5.1	–	7.0	–	–	5.1	mA
	V_{OL} 0.5	–	–5.1	–	–7.0	–	–	–5.1	
Output Noise		–	0	–	–3	–	–	0	dBrnc0
Slew Rate		–	–	–	2	–	–	–	V/μs

RECEIVE FILTER SPECIFICATIONS

($V_{DD} - V_{SS}$ = 12 V, CCI = 128 kHz, MSI = 8 kHz, includes sinx/x correction, V_{in} = –10 dBm0, full scale = +3 dBm0, 7 V p-p)

Characteristic		0°C		25°C			85°C		Unit
		Min	Max	Min	Typ	Max	Min	Max	
Gain (1020 Hz)		–0.3	0.30	–	±0.2	–	–0.30	0.30	dB
Pass-band Ripple (50 Hz to 3000 Hz)	Relative to 1.02 kHz@0 dBm0	–0.15	+0.15	–	±0.08	–	–0.15	+0.15	dB
Out of Band Rejection Relative to 1.02 kHz@0 dBm0	MC14414/13-1	–	–0.9	–	–0.5	–0.9	–	–0.9	
3400 Hz	MC14414/13-2	–	–1.5	–	–0.8	–1.5	–	–1.5	dB
4000 Hz-4600 Hz		–14	–	–14.2	–15.5	–	–14	–	
4600 Hz-64 kHz		–28	–	–30	–33	–	–28	–	
Output Noise (RXI = V_{AG})	ref to 900 Ω	–	–	–	8	12	–	–	dBrnc0
Dynamic Range		–	–	81	83	–	–	–	dB
Absolute Delay Difference									
1150 to 2300 kHz Delay		–	22	–	12	22	–	22	μs
1000 to 2500 kHz Delay		–	35	–	25	35	–	35	
800 to 2700 kHz Delay		–	41	–	31	41	–	41	
Crosstalk 0 dBm@3 kHz		–	–	–	76	–	–	–	dB
Power Supply Rejection Ratio V_{DD} = 12 V + 0.1 Vrms@1 kHz		–	–	–	40	–	–	–	dB

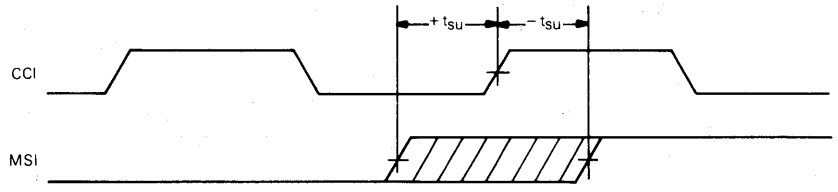
TRANSMIT FILTER SPECIFICATIONS ($V_{DD} - V_{SS} = 12$ V, CC = 128 kHz, MSI = 8 kHz, $V_{in} = -10$ dBm0, full scale = +3 dBm0, 7 Vp-p)

Characteristic		0°C		25°C			85°C		Unit
		Min	Max	Min	Typ	Max	Min	Max	
Gain (1020 Hz)	MC14413-1, -2	−0.3	+0.3	–	±0.2	–	−0.3	+0.3	dB
	MC14414-1, -2	−0.25	0.25	–	±0.15	–	−0.25	0.25	
Pass-band Ripple (300 Hz to 3000 Hz)	Relative to 1.02 kHz@0 dBm0	−0.15	0.15	–	±0.08	–	−0.15	0.15	dB
Rejection									dB
50 Hz (Relative to 1.02 kHz)	MC14413-1, -2 Only	−24	–	−26	−28	–	−24	–	
60 Hz	MC14413-1, -2 Only	−22	–	−22.7	−25	–	−22	–	
180 Hz		–	−0.8	–	−0.3	–	–	−0.8	
3400 Hz	MC14414-1/13-1	–	−0.8	–	−0.5	−0.8	–	−0.8	
	MC14414-2/13-2	–	−1.5	–	−0.6	−1.5	–	−1.5	
4000 Hz-4600 Hz		−14	–	−14	−15.5	–	−14	–	
4600 Hz-64 kHz		−32	–	−32	−33	–	−32	–	
Output Noise (300 Hz-3400 Hz)	MC14413-1, -2	–	15	–	10	15	–	15	dBrnc0
	MC14414-1, -2	–	12	–	7	10	–	12	
Dynamic Range (7 V p-p Max)	MC14413-1, -2	–	–	78	84	–	–	–	dB
	MC14414-1, -2	–	–	81	87	–	–	–	
Absolute Delay Difference									μs
1150 to 2300 kHz Delay		–	22	–	12	22	–	22	
1000 to 2500 kHz Delay		–	35	–	25	35	–	35	
800 to 2700 kHz Delay		–	41	–	31	41	–	41	
Crosstalk 0 dBm@3 kHz	RXO, TXO	–	–	–	76	–	–	–	dB
Power Supply Rejection Ratio	$V_{DD} = 12\text{ V} + 0.1\ V_{RMS}$@1 kHz	–	–	–	40	–	–	–	dB

SWITCHING CHARACTERISTICS ($V_{DD} - V_{SS} = 10$ V)

Characteristics		Symbol	0 to 70°C			Units
			Min	Typ	Max	
Input Rise Time Input Fall Time	CCI, MSI	t_{TLH} t_{THL}	–	–	4	μs
Pulse Width	CCI, MXI	t_{WH}	200	–	–	ns
Clock Pulse Frequency	CCI	f_{CL}	50	–	500	kHz
CCI Duty Cycle		–	40	–	60	%
Setup Time MSI Rising Edge to CCI Rising Edge (CCI = 128 kHz)*		t_{su}	−3.0	–	+3.0	μs

*Specifications assume use of 50% duty cycle for clocks.



FUNCTIONAL DESCRIPTION OF PINS

Pin 1 — V_{AG} (Analog Ground)

This pin should be held at approximately (V_{DD}-V_{EE})/2. All analog inputs and outpus are referenced to this pin. If this pin is brought to within approximately 1.0 V of V_{DD}, the chip will be powered down.

Pin 2 — +A

Noninverting input of op-amp A..

Pin 3 — −A

Inverting input of op-amp A.

Pin 4 — A0

Output of uncommitted op-amp A.

Pin 5 — B0

Output of uncommitted op-amp B.

Pin 6 — −B

Inverting input of op-amp B.

Pin 7 — +B

Non-inverting input of op-amp B.

Pin 8 — V_{SS}

This is the most negative supply pin and digital ground for the package.

Pin 9 — V_{LS} (Logic Shift Voltage)

The voltage on this pin determines the logic compatibility for the CCI and MSI inputs. If V_{LS} is within 0.8 V of V_{SS}, the thresholds will be for CMOS operating between V_{DD} and V_{SS}. If V_{LS} is within 1.0 V of V_{DD}, the chip will power down. If V_{LS} is between $V_{DD}-2$ V and $V_{SS}+2$ V, the thresholds for logic inputs at CCI and MSI will be between $V_{LS}+0.8$ V and $V_{LS}+2.0$ V for TTL compatibility.

Pin 10 — MSI (Master Sync Input)

This pin should receive a low-to-high transition concurrent with each new PAM sample received at the receive filter input, ADI. A new transmit filter output sample will be presented 8 CCI clocks after this.

Pin 11 — CCI (Convert Clock Input)

Normally, a 128 kHz clock signal should be applied to this pin to operate both filters at fo = 3100 Hz. For other break frequencies use the following equation: fo = 0.02422 f clock.

Pin 12 — TxO (Transmit Band-pass Output — MC14413-1, -2)

This is the output of the transmit band-pass filter. It is 100% duty cycle PAM at 8 kHz.

Pin 12 — LPO (Transmit Low-pass Output — MC14414-1, -2)

This is the output of the transmit low-pass filter. It is 100% duty cycle PAM at CCI frequency, normally 128 kHz.

Pin 13 — TxI (Transmit Input)

This is the transmit-filter input.

Pin 14 — RxO (Receive Output)

This pin is the output of the receive filter. It is 100% duty cycle PAM at the same frequency as the CCI pin, normally 128 kHz.

Pin 15 — RxI (Receive Input)

This is the receive filter input. It will accept 15% to 100% duty cycle PAM at 8 kHz.

Pin 16 — V_{DD}

Nominally 12 volts.

NOTE: Both V_{AG} and V_{LS} are high-impedance inputs.

PCM FILTER DESCRIPTION

Transmit Filter Description

The transmit filter in both the MC14413-1, -2 and MC14414-1, -2 consists of a 5-pole elliptic low-pass section operating at a sampling rate of 128 kHz. This filter provides the band limiting necessary to prevent aliasing of the input signal in the codec. Since the transmit filter itself samples at a 128 kHz rate, its input (TxI) signal should be band limited to 124 kHz. If energy above 124 kHz could be present, a single-pole RC pre-filter should precede the transmit filter.

In addition to the low-pass section, the transmit filter of the MC14413-1, -2 incorporates a 3 pole Chebychev high-pass filter to provide 50/60 Hz and 15 Hz rejection. Although the MC14414-1, -2 does not include this filter, it can be externally realized using one of the on-board uncommitted op amps as an active filter. This is shown in Figures 10 and 11.

Both the MC14413-1, -2 and MC14414-1, -2 can be used in cascade to produce a sharper rolloff. This is especially useful in testing the MC14413-1, -2 since the 8 kHz PAM from the Tx filter will be sampled and sinx/x corrected by applying the Tx output to the RxI input and observing RxO.

Receive Filter Description

The receive filter sections of the MC14413-1, -2 and MC14414-1, -2 are identical and are 5-pole elliptic low-pass filters operating at a sampling rate of 128 kHz. These filters are used to smooth the PAM output of the PCM Codec. They are similar to the transmit low-pass sections with the exception that they include a 1/8 duty cycle 8 kHz pre-sampler on their inputs (RxI).

This circuitry resamples the codec's PAM output and thereby effecively eliminates the sinx/x distortion normally associated with 15% to 100% 8 kHz PAM pulse trains and eliminates the need to predistort the receive filter's pass-band characteristic.

In normal use as a codec's receive filter, MSI will be an 8 kHz signal. With the MC14407 codec family, the filter MSI is the same as the codec MSI. With other codecs, the MSI signal is receive sync.

The MC14414 may also be used in analog applications by disabling the sinx/x correction. If MSI and CCI are tied together, the receive filter has the same frequency response as the transmit filter and a gain of 18 dB.

Timing And Synchronization

Timing and synchronization of the MC14413-1, -2 and MC14414-1, -2 are provided by the CCI and MSI inputs. A 128 kHz signal should be applied to CCI. An 8 kHz signal, whose low-to-high transition coincides with a new output sample from the PCM codec, should be applied to MSI. The rising edges of theCCI and MSI signals should be skewed no more than 3.0 μs for proper operation.

Logic levels of these signals can be either TTL or CMOS compatible. Choice of logic level can be user determined by applying the appropriate voltage to the level shift control pin, V_{LS}.

Power Down

Both the MC14413-1, -2 and MC14414-1, -2 may be powered down in either of two ways: by bringing V_{AG} to within 0.5 V of V_{DD} or by bringing V_{LS} to within 0.5 V of V_{DD}.

If used on a single supply with the MC14406/7 PCM Codec, the filter IC will power down automatically when the codec does, since the codec raises its V_{AG} pin to V_{DD} in power down. When used in a split supply configuration, the circuit shown in Figure 7 may be utilized.

FIGURE 1 — RECEIVE FILTER TYPICAL AND GUARANTEED PERFORMANCE (MC14413-1, -2/MC14414-1, -2, SINX/X CORRECTION INCLUDED)

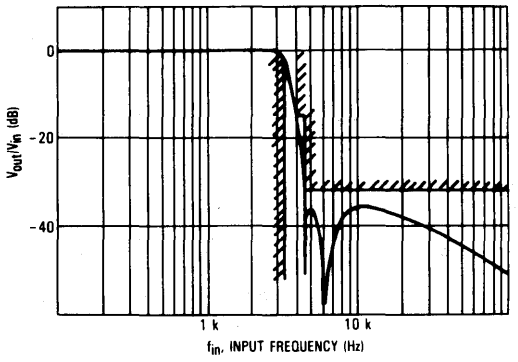


FIGURE 2 — RECEIVE FILTER TYPICAL AND GUARANTEED PASS-BAND PERFORMANCE (MC14413-1, -2/MC14414-1, -2)

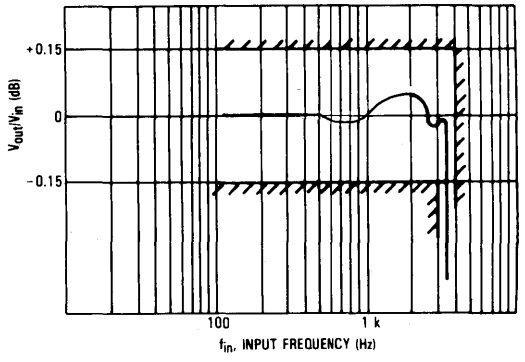


FIGURE 3 — TRANSMIT FILTER TYPICAL AND GUARANTEED PERFORMANCE (MC14413-1, -2 AND MC14414-1, -2 USING FIGURES 10 AND 11)

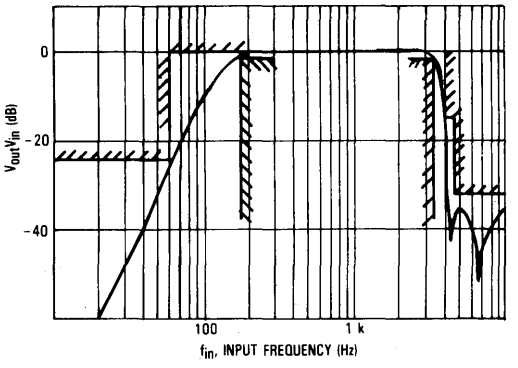


FIGURE 4 — TRANSMIT FILTER TYPICAL AND GUARANTEED PASS-BAND PERFORMANCE (MC14413-1, -2 AND MC14414-1, -2 USING FIGURES 10 AND 11)

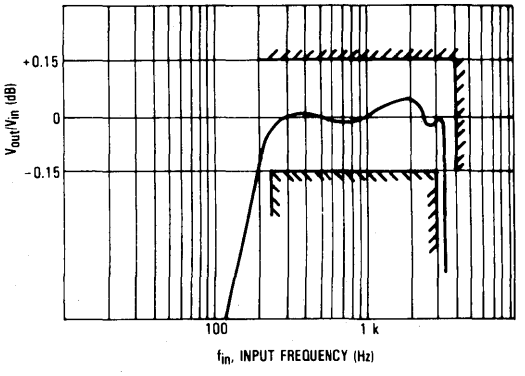


FIGURE 5 — TRANSMIT FILTER TYPICAL AND GUARANTEED PASS-BAND PERFORMANCE (MC14414-1, -2)

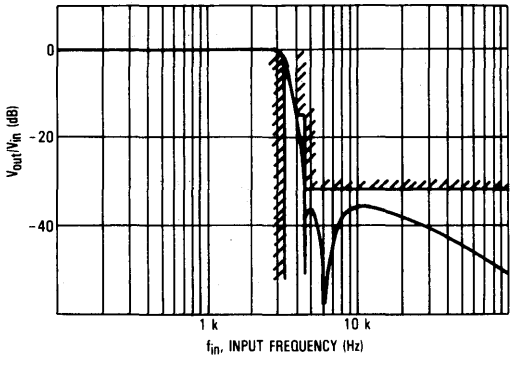


FIGURE 6 — TRANSMIT FILTER TYPICAL AND GUARANTEED PERFORMANCE (MC14414-1, -2)

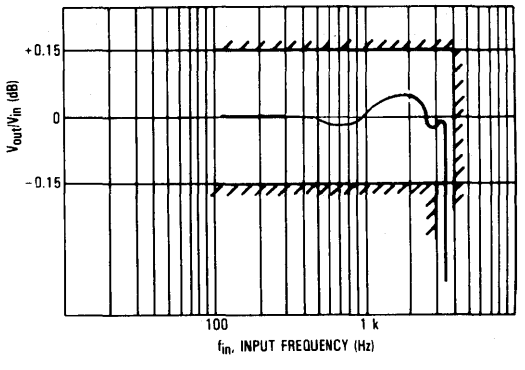


FIGURE 7 — TYPICAL CIRCUIT CONFIGURATION
USING THE MC14407 CODEC AND MC14413-1, -2 FILTER
(SPLIT SUPPLY)

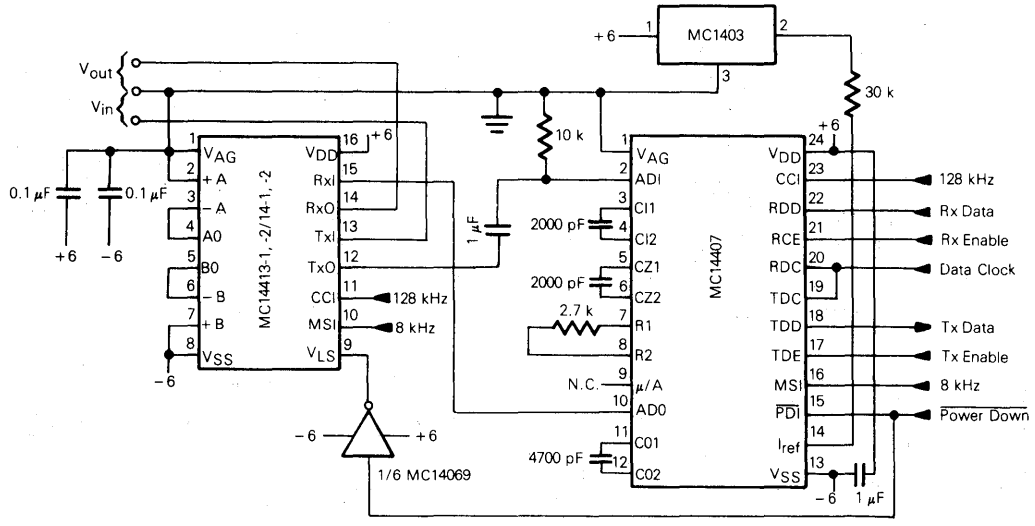
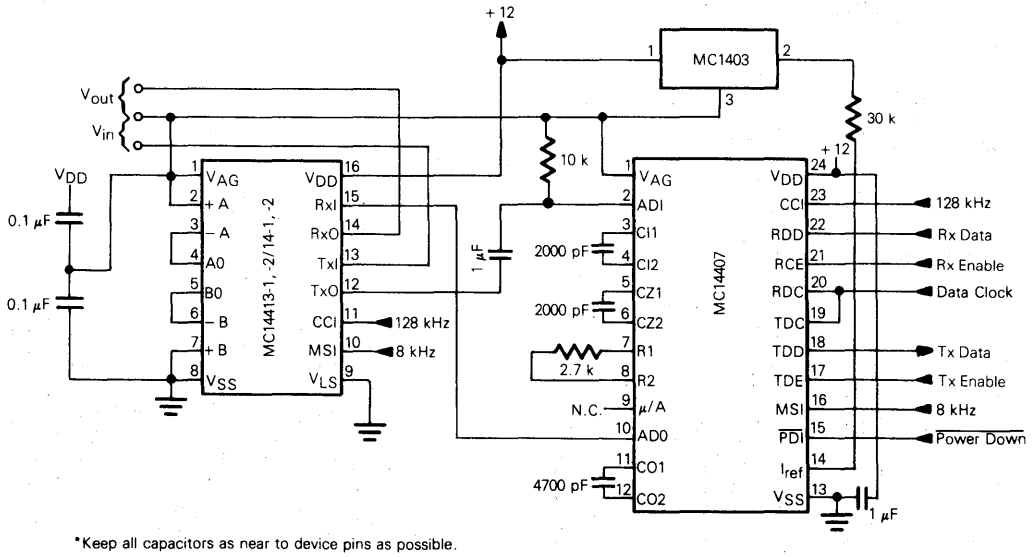
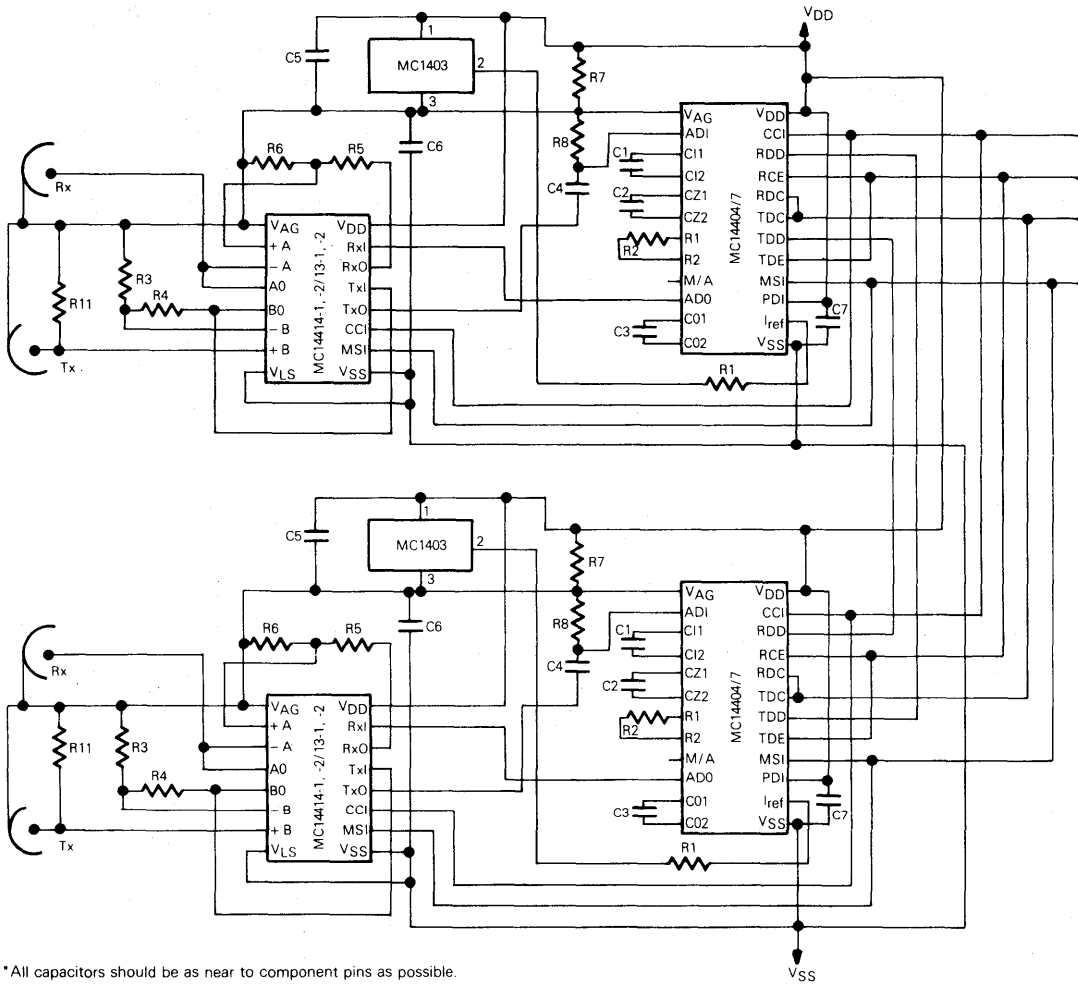


FIGURE 8 — TYPICAL CIRCUIT CONFIGURATION
USING THE MC14407 CODEC AND MC14413-1, -2 FILTER
(SINGLE SUPPLY)



*Keep all capacitors as near to device pins as possible.

FIGURE 9 — MOTOROLA CODEC FILTER EVALUATION BOARD



C1, C2*	2000 pF	20%
C3*	4700 pF	20%
C5, C6*	0.1 μF	20%
C7, C4*	1 μF	20%
R1	30 k	1%
R2	2.7 k	1%
R3	237 k	1%
R4	169 k	1%
R5	20 k	1%
R6	33 k	1%
R7	4.7 k	10%
R8,	10 k	10%
R11	900	1%

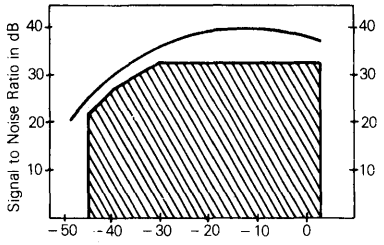
*All capacitors should be as near to component pins as possible.
*In noisy environments, R3-R6 should be 10 kΩ or less to minimize pickup.

2

TYPICAL END-TO-END CHANNEL PERFORMANCE FOR MOTOROLA
MC14413-1, -2/14-1, -2-MC14404/7 CODEC AND FILTER

MC14407/13-2
SPECIFICATION BELL PUB 43801

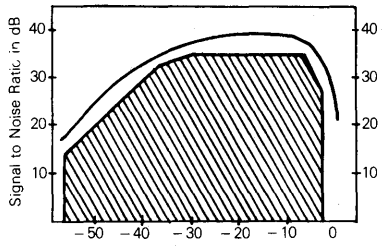
QUANTIZING DISTORTION
SINUSOIDAL INPUT
C MESSAGE WEIGHTED



Input Level (dBm) Referenced to 0 dBm0 @ 1.02 kHz

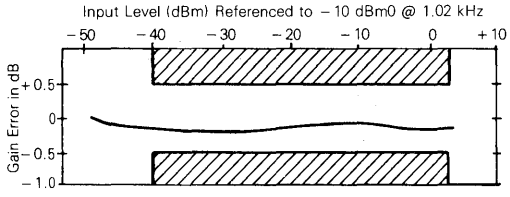
MC14404/13-1
SPECIFICATION CCITT G7.12

QUANTIZING DISTORTION
PSEUDO RANDOM NOISE
3 kHz FLAT WEIGHTING

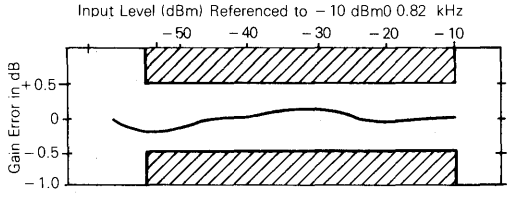


Input Level (dBm) Referenced to 0 dBm0 @ 0.82 kHz

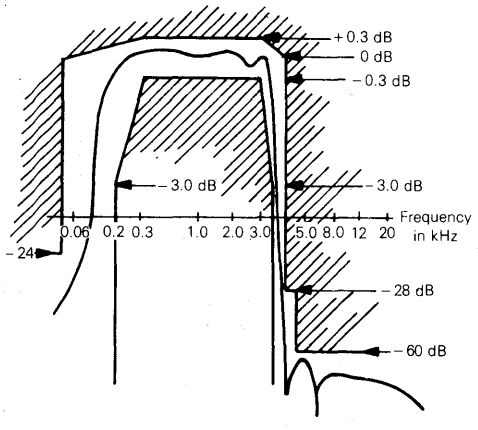
SINUSOIDAL GAIN TRACKING



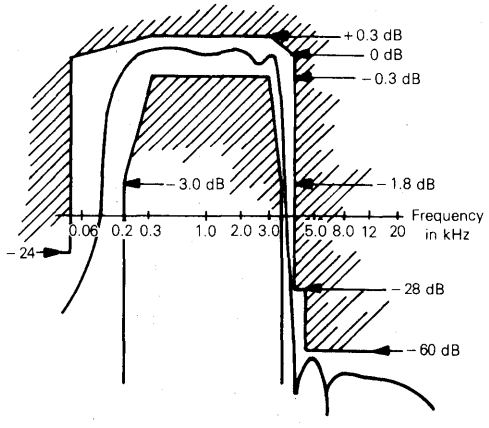
PSEUDO-RANDOM NOISE GAIN TRACKING



GAIN vs FREQUENCY, SINUSOIDAL



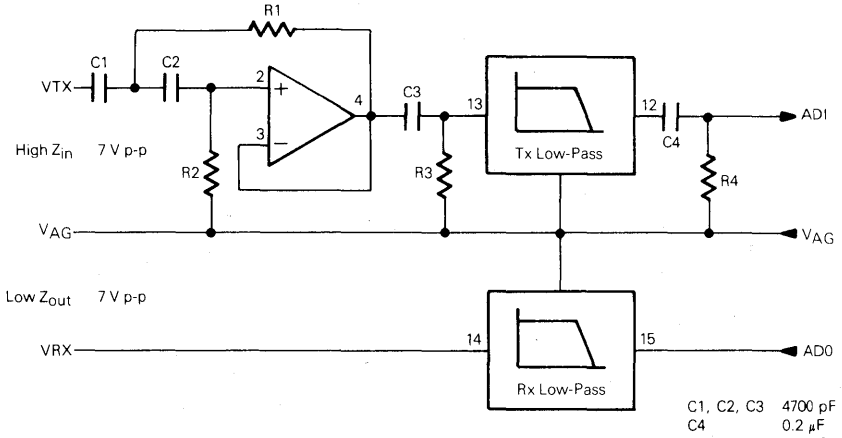
GAIN vs FREQUENCY, SINUSOIDAL



TYPICAL END-TO-END PERFORMANCE OF MOTOROLA CODEC AND FILTER
(All measurements made using HP3779B PCM Test Set)

Specification	Typical Performance of MC14407/4 Codec and MC14413 Filter	Bell System D4 Voice Frequency Requirements PUB 43801	CCITT G7.12 Voice Frequency Requirements
Channel Saturation	+3 dBm0	+3 dBm0	+3 dBm0
Gain Tracking with 1 kHz Tone			
+3 to −40 dBm0	±0.2 dB	≤ ±0.5 dB	≤ ±0.5 dB
−40 to −50 dBm0	±0.3 dB	≤ ±1.0 dB	≤ ±1.0 dB
−55 dBm0	±0.5 dB	≤ ±3.0 dB	≤ ±3.0 dB
Quantizing Distortion @ 1 kHz			
+3 to −30 dBm0	37 dB	≥ 33 dB	> 33 dB
−35 dBm0	34 dB	≥ 30 dB	≥ 30 dB
−40 dBm0	31 dB	≥ 27 dB	≥ 27 dB
−45 dBm0	25 dB	≥ 22 dB	≥ 22 dB
Idle Channel Noise with VTX = V_{AG}	16 dBrnc0	≤ 23 dBrnc0	≤ −65 dBm0P
Quiet Code Noise (all 1's at decoder (RDD) input)	10 dBrnc0	≤ 15 dBrnc0	≤ −75 dBm0P
Selective Response @ Multiplex of 8 kHz	−60 dBm0	See Frequency Response	≤ −50 dBm0
Frequency Response @ 0 dBm0 Input			
50 Hz Gain Relative to 1.02 kHz	−28 dB	−	≤ −24 dB
60 Hz Gain or 0.820 kHz	−24 dB	≤ −20 dB	−
200 to 300 Hz Ripple	±0.20 dB	≤ ±0.3 dB	≤ ±0.5 dB
3400 Hz Gain	−1.0 dB	≥ −3.0 dB	≥ −1.8 dB
4000 Hz Gain	−32 dB	≤ −28 dB	≤ −28 dB
≥ 4600 Hz Gain	< −62 dB	≤ −60 dB	≤ −60 dB
Single Frequency Spurious Response			
In Band with Input 1 kHz @ 0 dBm	≤ −44 dB	≤ −40 dB	≤ −40 dB
Out of Band with Input 0 to 12 kHz @ 0 dBm	≤ −32.5 dB	≤ −28 dB	≤ −25 dB
Differential Delay Distortion			
1150 to 2300	58 μs	≤ 60 μs	
1000 to 2500	72 μs	≤ 100 μs	
900 to 2700	91 μs	≤ 200 μs	

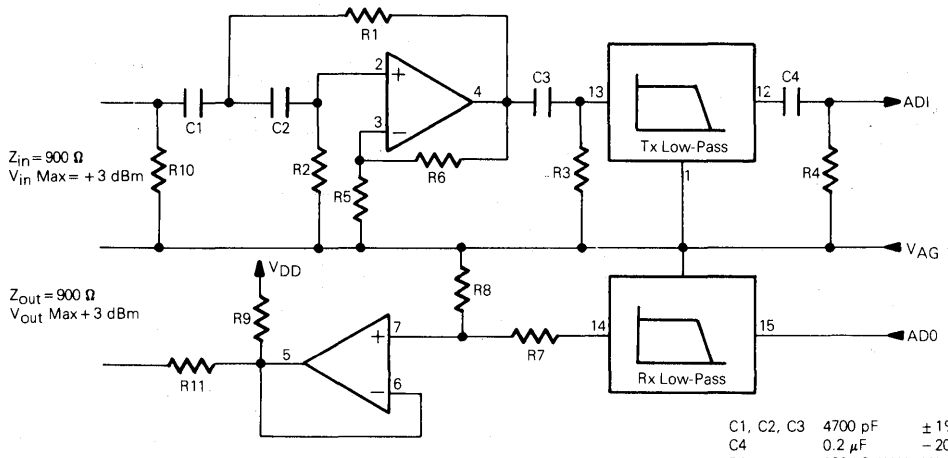
FIGURE 10 — FILTER SCHEMATIC FOR MC14414-1, -2 WITH 60 Hz REJECT FILTER



C1, C2, C3	4700 pF	±1%
C4	0.2 μF	−20% +80%
R1	112 kΩ ¼ W	1%
R2	620 kΩ ¼ W	1%
R3	223 kΩ ¼ W	1%
R4	100 kΩ ¼ W	10%

*In noisy environments, R1-R4 should be 10 kΩ or less to minimize pickup.

FIGURE 11 — FILTER SCHEMATIC FOR MC14414-1, -2 WITH 60 Hz REJECTION AND 900 TERMINATION



C1, C2, C3	4700 pF	±1%
C4	0.2 μF	−20% +80%
R1	236 kΩ ¼ W	1%
R2	294 kΩ ¼ W	1%
R3	223 kΩ ¼ W	1%
R4	100 kΩ ¼ W	10%
R5	200 kΩ ¼ W	1%
R6	169 kΩ ¼ W	1%
R7	24 kΩ ¼ W	1%
R8	33 kΩ ¼ W	1%
R9	1.8 kΩ ¼ W	10%
R10	900 Ω ¼ W	1%
R11	900 Ω ¼ W	1%

*In noisy environments, R1-R8 should be 10 kΩ or less.

FIGURE 12 — TYPICAL 2-WIRE PORT INTERFACE USING MC14413

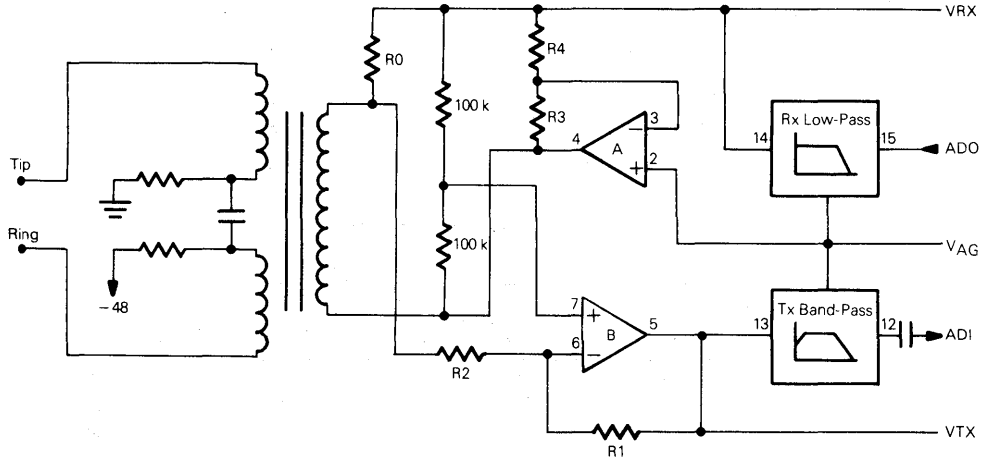
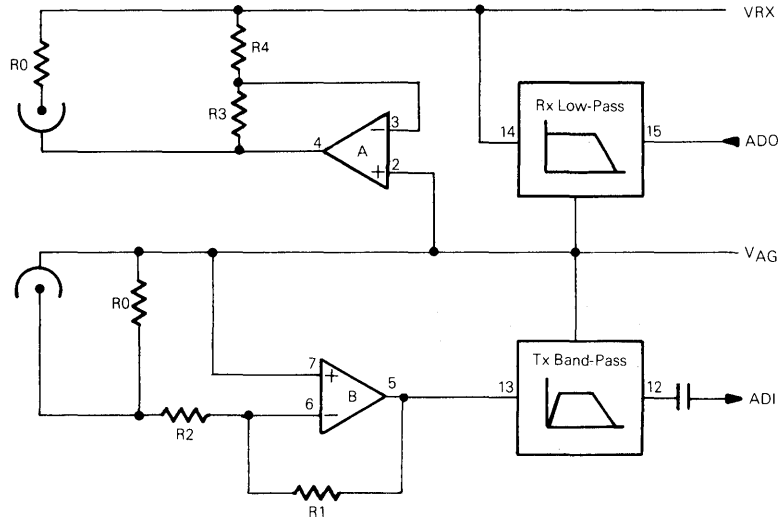


FIGURE 13 — TYPICAL 4-WIRE PORT INTERFACE USING MC14413



Full Scale Voltage at TxO (LPO) RxI	Port Impedance (RO)	Relative Level	R1	R2	R3	R4
5 V p-p	600	4.16 dBr	161 k	100 k	23.9 k	100 k
	900	2.4 dBr	198 k	150 k	51.8 k	100 k
6.2 V p-p, +9 dBm	600	6.00 dBr	100 k	100 k	Short	Open
	900	4.26 dBr	245 k	150 k	18.5	100 k
7.6 V p-p, +9 dBm	900	6.00 dBr	150 k	150 k	Short	Open

Interface to 2-wire or 4-wire ports using the MC14413-1,-2/14-1, -2 is shown in Figures 12 and 13, respectively. The table above shows some voltages typically used with the filter and the appropriate resistor values for cases in which the codec/filter OTLP is less than or equal to the 0 dBm level. If the codec/filter overload voltage is greater than required for 0 dBm levels in the load, the RxO output can be voltage divided by two resistors and the extra op amp used as a voltage follower.

FIGURE 14 — GENERATOR FOR 128 kHz IN SYSTEM USING 2.048 MHz CLOCK

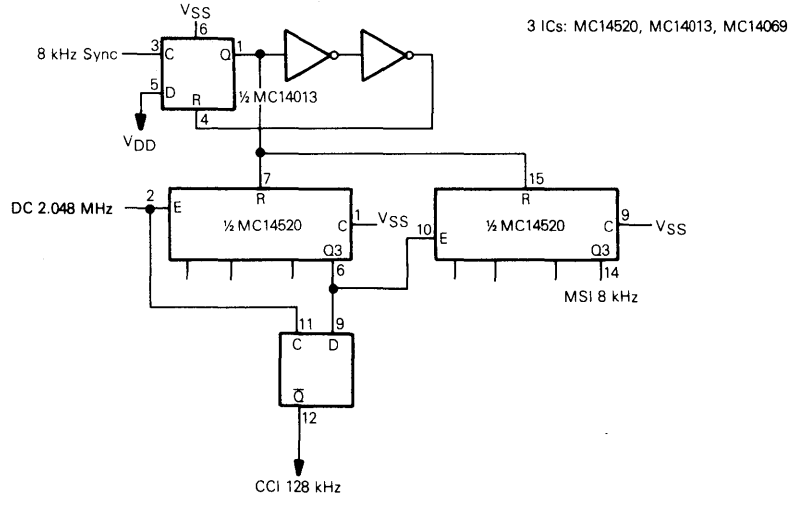


FIGURE 15 — 128 kHz FREQUENCY SYNTHESIZER USING 8 kHz INPUT

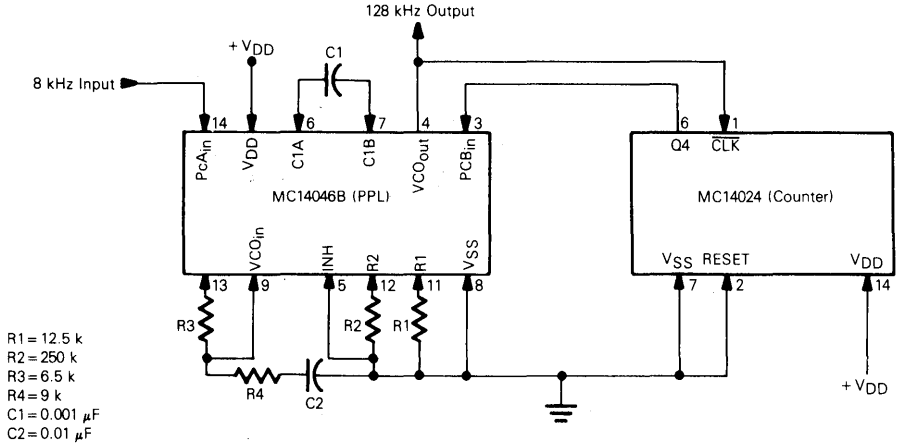


FIGURE 16 — GENERATION OF 128 kHz IN SYSTEM USING 1.544 MHz CLOCK

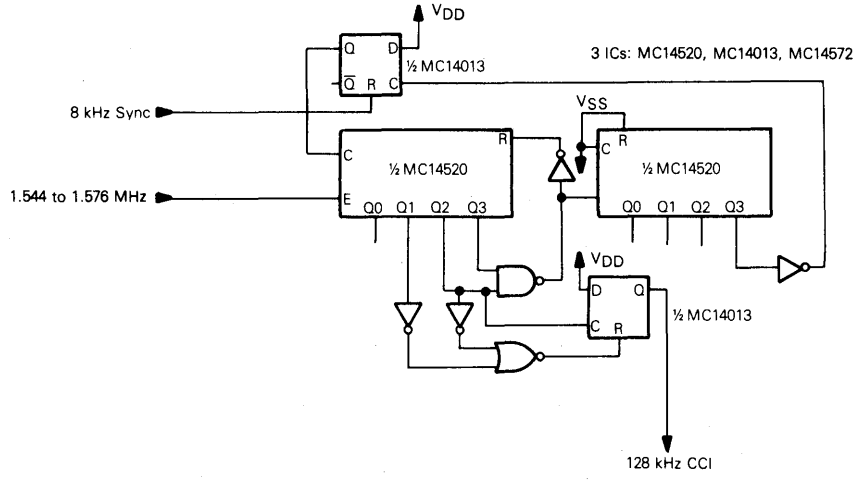
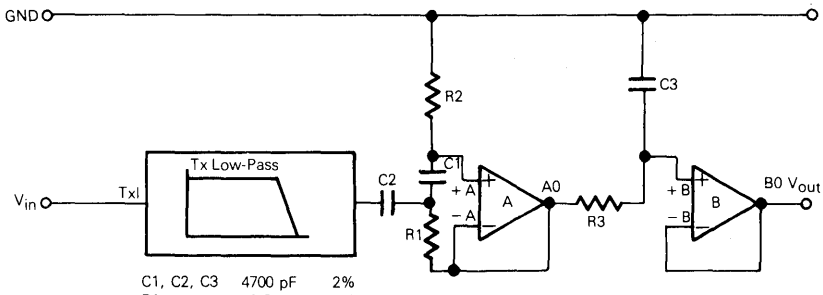


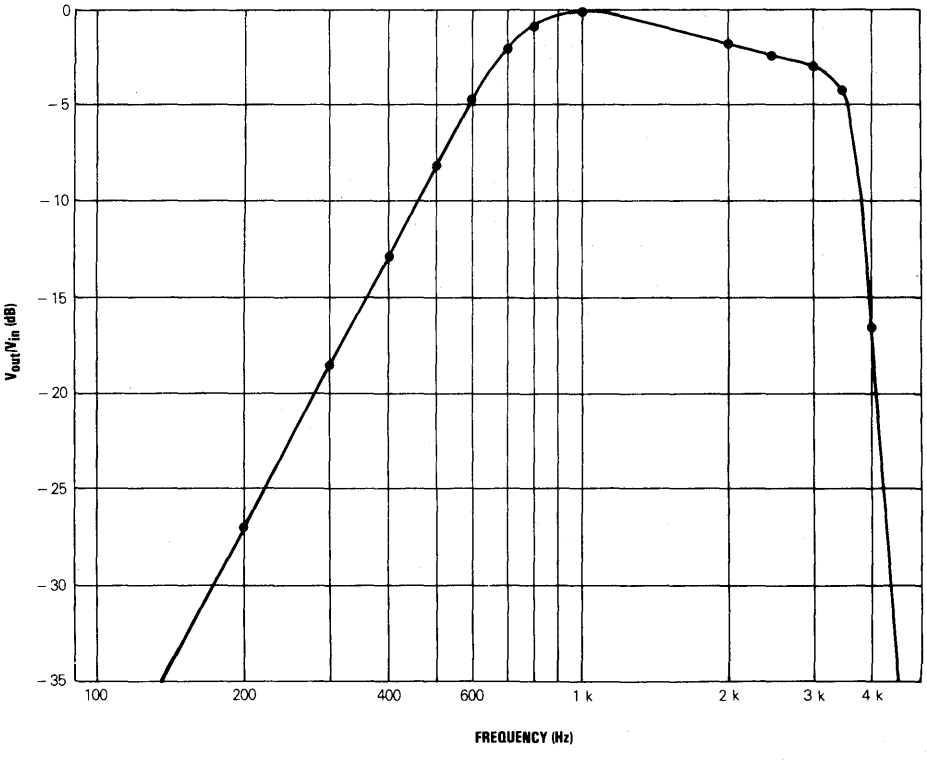
FIGURE 17 — TELEPHONY C-MESSAGE FILTER USING MC14414-1, -2 FILTER



C1, C2, C3	4700 pF	2%
R1	19.6 k	1%
R2	97.6 k	1%
R3	8.25 k	1%

V_{AG}, V_{LS} connected to GND
MSI, CCI connected to 134 kHz TTL clock
0.1 μF, V_{DD} to V_{AG} and V_{SS} to V_{AG}
Rx Filter can also be used and will provide 18 dB of input gain
$V_{DD} = +5$ V, $V_{SS} = -5$ V

NOTE: Op Amps A and B are the free op amps on the MC14414-1, -2 filter.



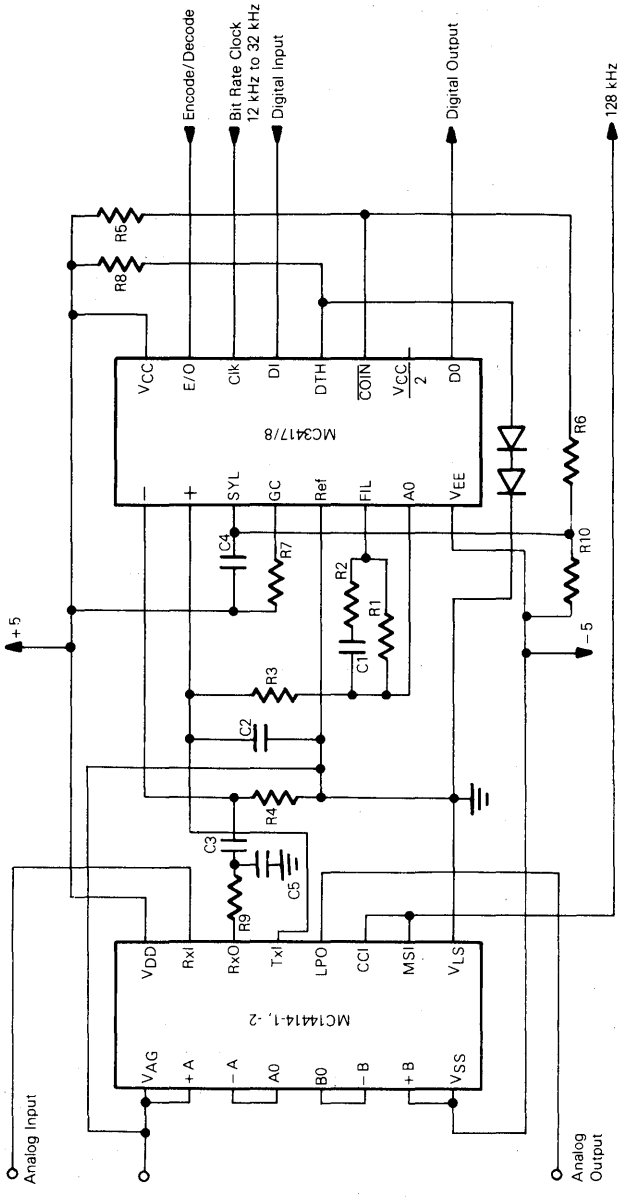


FIGURE 18 — DELTAMOD VOICE DIGITIZER USING MC3417 AND MC14414-1, -2

C1	0.1 μF	20%
C2	0.01 μF	20%
C3	0.01 μF	
C4	0.33 μF	
C5	0.1 μF	
R1	9.1 k	5%
R2	510 Ω	5%
R3	7.5 k	5%
R4	15 k	5%
R5	8.2 k	5%
R6	47 k	5%
R7	5.1 k	5%
R8	10 k	5%
R9	200 Ω	5%
R10	22 mΩ	5%

MOTOROLA

MC14416
MC14418

PER CHANNEL, ADDRESSABLE TIME SLOT ASSIGNER CIRCUITS (TSACs)

The MC14416 and MC14418 are per channel devices that allow variable codec time slot assignment to be programmed through a serial microprocessor port (0-63 time slots): Both devices have independent transmit and receive frame syncs and enables. They also include chip select and clear to send signals which simplify system design.

The MC14418 provides the additional addressing capability which allows a parallel bus back plane in the channel group. In addition, the MC14418 provides control bits which can be used for the power down, ring enable and ring trip functions on a line circuit.

The MC14416 provides the ability to multiplex off hook signals for a bank of TSACs.

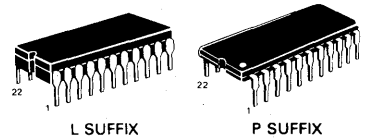
Both devices are fabricated using the CMOS technology for reliable low power performance. The MC14418 is the full featured device produced in a 22-pin package. The MC14416 without the addressing capability is offered in a 16-pin package.

- Low Power
- 5-Volt Interface on Microprocessor Port
- 5-16 Volt Output Logic Levels
- Independent Transmit and Receive Frame Syncs and Enables
- Up to 64 Time Slots Per Frame
- For Use With Up to 2.56 MHz Clocks
- Provides Power Down Control for Line Circuits
- Compatible with MC14400/01/02/03/05 and MK5116 Codecs
- Provides the Ring Enable and Ring Trip Functions (MC14418)
- Allows Use of a Parallel Backplane for Line Circuits Due to the Hard Wired Address Feature (MC14418)
- Off-Hook Multiplex Control (MC14416)
- CMOS Metal Gate for High Reliability

MOS LSI

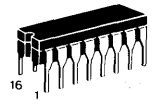
(LOW-POWER COMPLEMENTARY MOS)

TSAC
TIME SLOT ASSIGNER
CIRCUITS

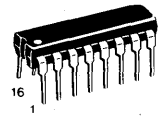


L SUFFIX
CERAMIC PACKAGE
CASE 736

P SUFFIX
PLASTIC PACKAGE
CASE 708

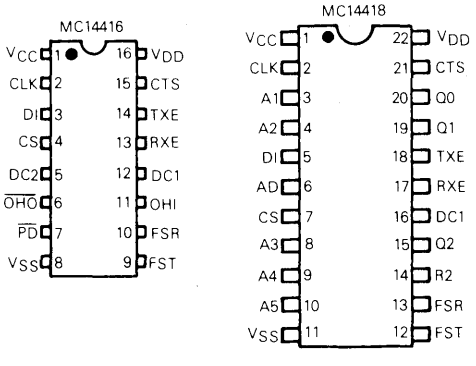


L SUFFIX
CERAMIC PACKAGE
CASE 620

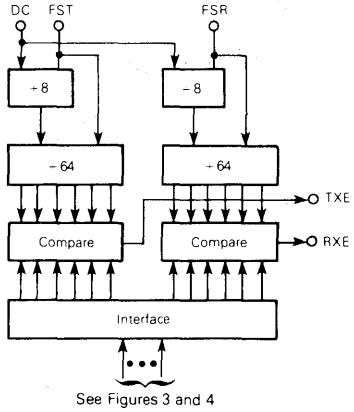


P SUFFIX
PLASTIC PACKAGE
CASE 648

PIN ASSIGNMENTS



BLOCK DIAGRAM



See Figures 3 and 4

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	−0.5 to +18	Vdc
Level Shift Voltage	V_{CC}	−0.5 to V_{DD}	Vdc
Input Voltage Inputs Referenced to V_{DD} to V_{CC}	 V_{in1} V_{in2}	 −0.5 to V_{DD} +0.5 −0.5 to V_{DD} +0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range	T_A	−40 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +165	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

ELECTRICAL CHARACTERISTICS ($T_A = 25°C$)

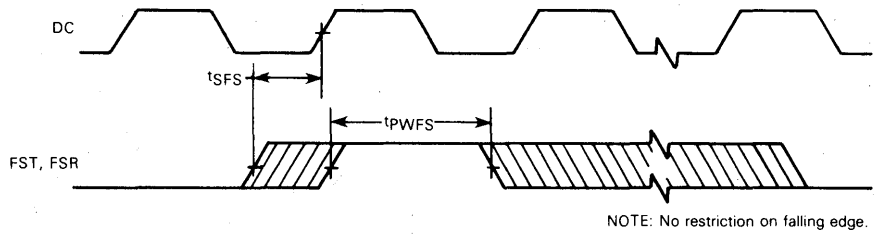
Characteristic	Symbol	V_{DD}	Min	Typ	Max	Unit
DC Supply Voltage $V_{SS}=0$ V	V_{DD}	–	4.5	12	16	V
DC Supply Voltage $V_{SS}=0$ V	V_{CC}	–	4.5	5	V_{DD}	V
Output Current TXE, RXE, Q0, Q1, Q2, $\overline{P_D}$						
($V_{OL}=0.4$ V)	I_{OL}	5	0.51	–	–	mAdc
($V_{OL}=1.0$ V)		12	2.0	4.0	–	
($V_{OH}=4.6$ V)	I_{OH}	5	−0.20	–	–	mAdc
($V_{OH}=1.0$ V)		12	−2.0	−4.0	–	
Output Current CTS, OHO						
($V_{OL}=0.8$ V)	I_{OL}	5	3.0	5.5	–	mAdc
($V_{OL}=0.8$ V)		12	6.6	11.5	–	
($V_{OL}=1.5$ V)		12	12.0	20.0	–	
($V_{OH}=0.8$ V)	I_{OH}	5	−8	−20	−40	µAdc
($V_{OH}=2.0$ V)		5	−6	−18	−40	
($V_{OH}=0.8$ V)		12	−40	−100	−200	
($V_{OH}=2.0$ V)		12	−35	−90	−200	
($V_{OH}=10.5$ V)		12	−15	−30	−60	
Input Voltage (CMOS) "0" Level FST, FSR, R2, DC1, DC2, A1, A2	V_{IL}	5 12	– –	– –	1.0 2.4	Vdc
A3, A4, A5, OHI "1" Level	V_{IH}	5 12	4.0 9.6	– –	– –	Vdc
Input Current OHI (Active Pull Down)	I_{inH}	5 12	+1.5 +10	+4.0 +25	+15 +100	µAdc
Input Voltage (TTL) "0" Level CLK, CS, AD, DI	V_{IL}	5 12	– –	– –	0.8 0.8	Vdc
$V_{CC}=5$ V "1" Level	V_{IH}	5 12	2.00 2.00	– –	– –	Vdc
Input Current	I_{in}	15	–	$\pm 10^{-5}$	±0.1	µAdc
Input Capacitance	C_{in}	–	–	5	7.5	pF
Total Supply Current (Outputs Unloaded) $V_{DD}=12$ V DC1 at 2.048 MHz $V_{DD}=5$ V	I_T	12 5	– –	3 2	6 4	mAdc
Total Supply Current (Power Down) MC14418 Only After CTS = V_{DD} CLK, CS, AD, DI Inputs ≤ 0.6 V	I_{PD}	–	–	–	0.1	mAdc

SWITCHING CHARACTERISTICS ($C_L = 50$ pF, $T_A = 25°C$, unless otherwise noted)

Characteristic	Symbol	Fig.	V_{DD}	Min	Typ	Max	Unit
Output Rise Time TXE, RXE, Q0, Q1, Q2, $\overline{P_D}$	t_r	–	5 12	– –	100 50	200 100	ns
Output Fall Time TXE, RXE, Q0, Q1, Q2, $\overline{P_D}$	t_f	–	5 12	– –	100 50	200 100	ns
Frame Sync Setup Time	t_{SFS}	1	5 12	−150 −75	– –	+150 +75	ns
Frame Sync Pulse Width	t_{PWFS}	1	5 12	200 100	– –	– –	ns
Propagation Delay – DC to TXE, RXE (Note 1) $C_L = 20$ pF	t_{PLHE}, t_{PHLE}	1	5 12	– –	130 80	180 125	ns
Data Clock Frequency	f_{DC}	–	5 12	– –	– –	2.048 2.6	MHz
Data Clock Pulse Width (at $f_{DC(MAX)}$)	t_{PWDC}	1	5 12	200 140	244 192	293 260	ns
Clock Frequency	f_{CLK}	–	5 12	00 00	– –	0.3 0.3	MHz
Clock Pulse Width (at $f_{CLK(MAX)}$)	t_{PWC}	2	5 12	0.5 0.5	– –	– –	μs
Address and Data Setup Time	t_{su}	2	5 12	300 300	– –	– –	ns
Address and Data Hold Time	t_h	2	5 12	200 200	– –	– –	ns
Propagation Delay DC1 to CTS	t_{PCL}	2	5 12	– –	– –	250 150	ns
DC1 or FST to CTS 10K Pullup or Equivalent	t_{PCH}	2	5 12	– –	– –	300 200	ns
Propagation Delay DC to PD	t_{PQ}	2	5 12	– –	– –	300 200	ns
DC to Q0-Q2	t_{PQ}	2	5 12	– –	– –	300 200	ns
Propagation Delay – R to Q2	t_P	2	5 12	– –	100 50	200 100	ns
Chip Select Setup Time Leading CS to Falling CLK	t_{SCS}	2	5 12	1 1	–	–	μs
Chip Select Hold Time Falling CTS to Falling CS	t_{HCS}	2	5 12	10 10	– –	– –	ns

NOTE 1: For time slot 0, t_{PHLE} and t_{PLHE} are measured from leading edge of DC or FST (FSR), whichever occurs last.

FIGURE 1 — TIMING DIAGRAMS



NOTE: No restriction on falling edge.

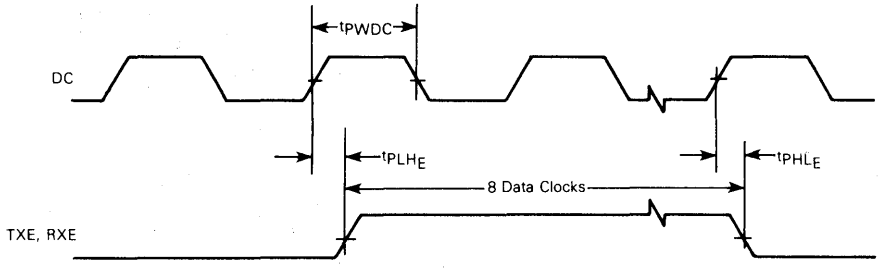
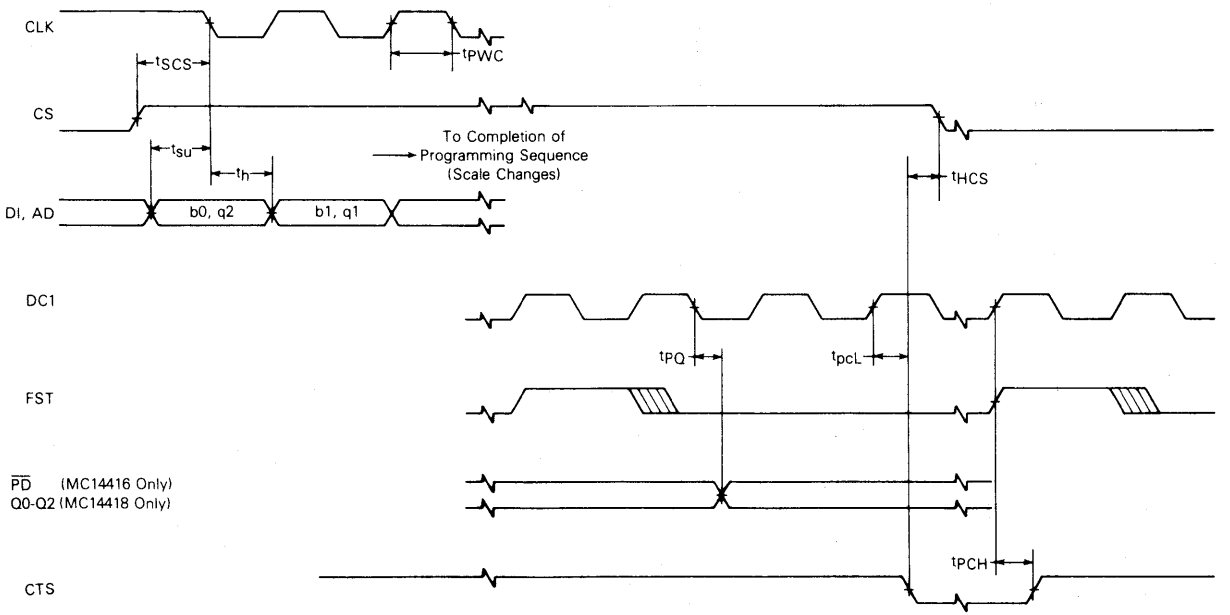


FIGURE 2 — PROPAGATION DELAYS FOR PROCESSOR INTERFACE PINS



NOTE: t_{PCH} is measured from the rising edge of the latter of FST or DC1.

FIGURE 3 — MC14418 22 PIN

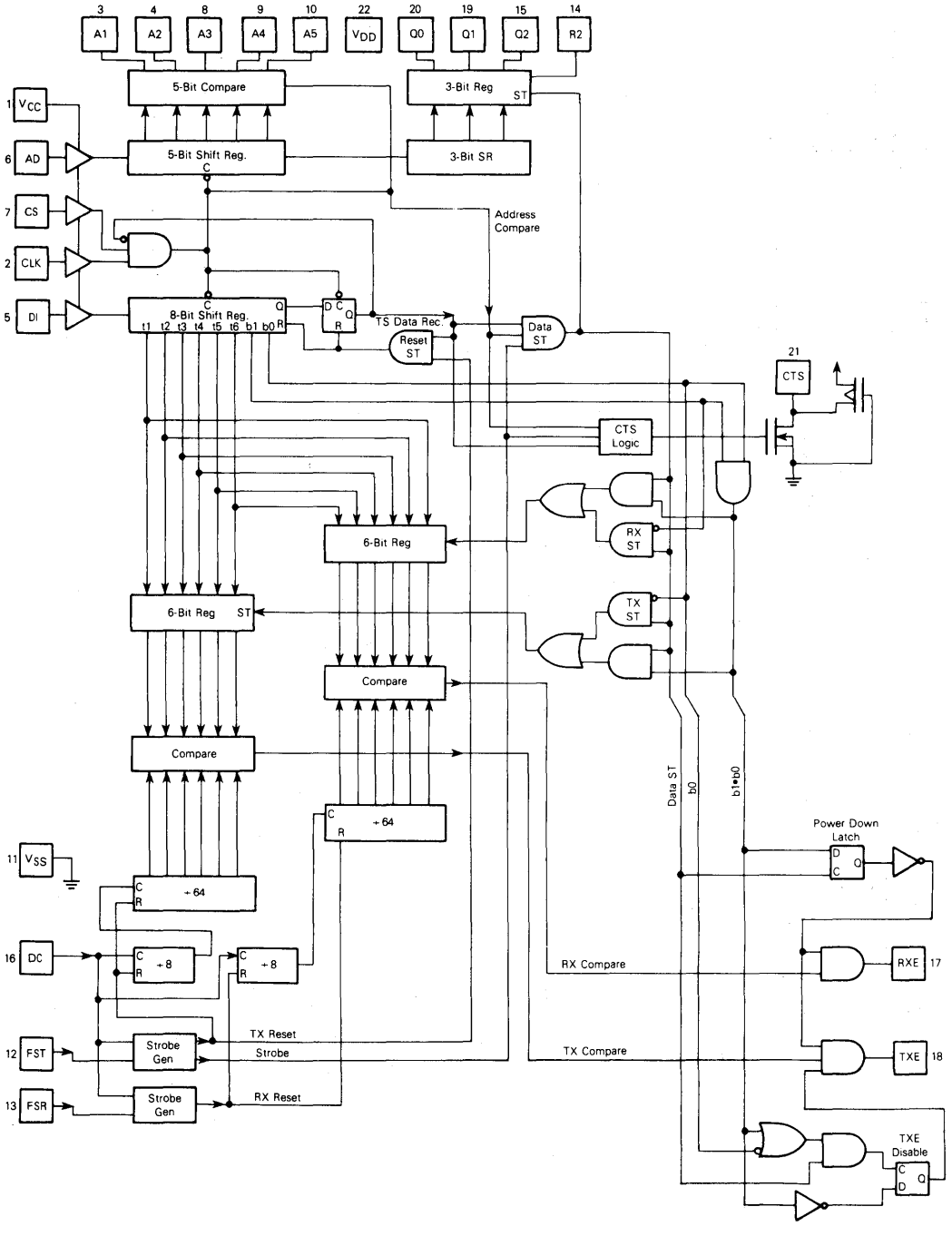
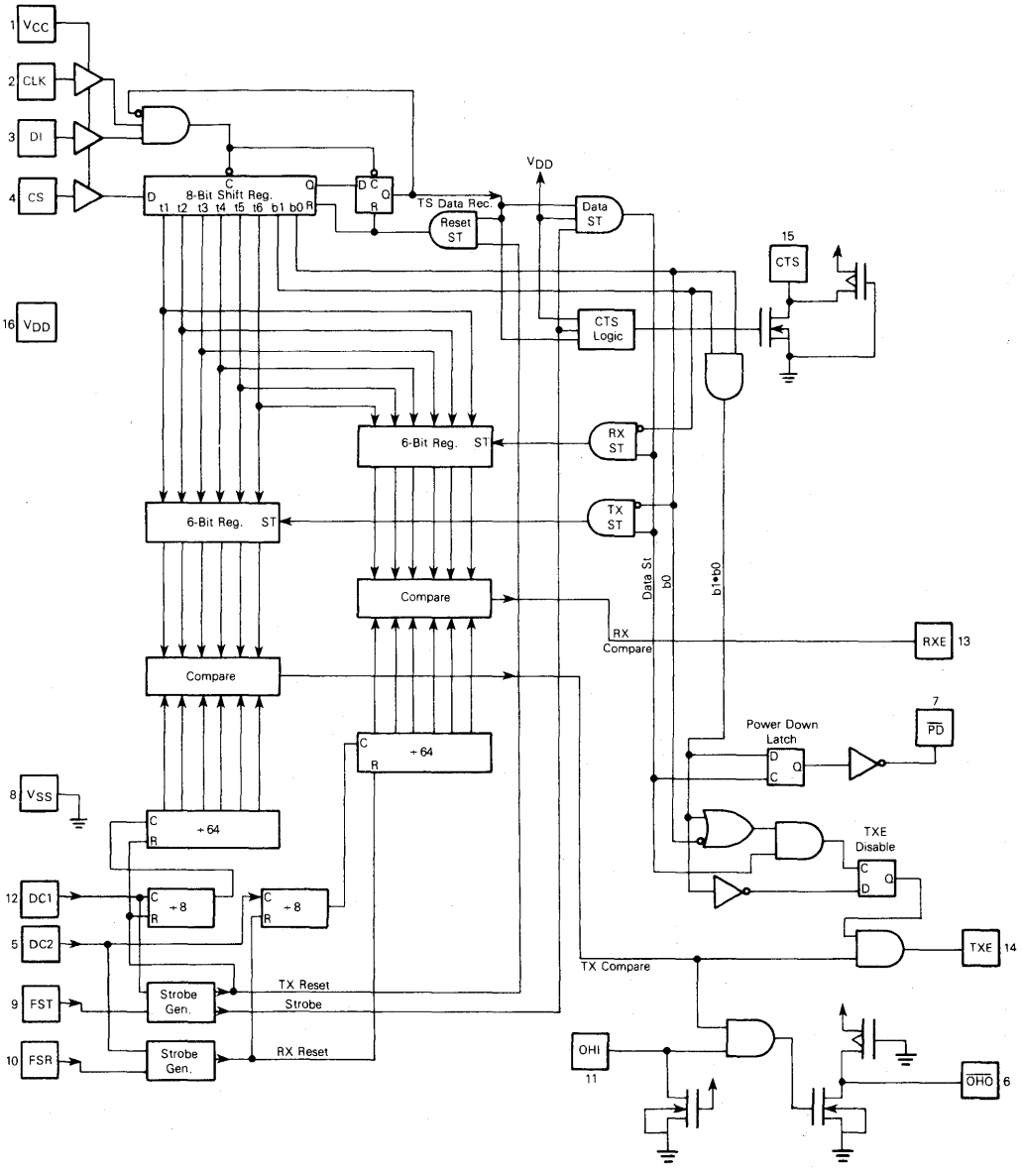


FIGURE 4 — MC14416 16 PIN



GENERAL DEVICE DESCRIPTION

The MC14416 and MC14418 TSACs are microprocessor peripherals intended to be used to control and supervise per channel codec subscriber channel units. The TSACs consist of three basic functions.

The Serially Programmable Microprocessor Port consists of V_{CC}, CLK, DI, CS and CTS for the MC14416 and further includes AD and A1 through A5 for the MC14418. This port allows the call processing microprocessor to access load data into each TSAC. See the applications section for a detailed description of the microprocessor port. Figure 5 defines the data word bit assignments.

The Supervision Controls consist of Q0, Q1, Q2, R2 on the MC14418 and OHI, $\overline{OHO}$ and $\overline{PD}$ on the MC14416. These functions provide data path for the supervision and control of user selected requirements in the subscriber channel unit. Figure 3 shows some typical uses of these bits.

The Time Slot Computation section of the chip derives separate transmit and receive time slot outputs (TXE and RXE) for the controlled codec from the bit rate clock and sync pins DC1, DC2, FST and FSR, respectively. The computed time slot is then derived from the information received through the microprocessor port.

PIN DESCRIPTIONS

V_{CC} (Positive Supply for Microprocessor Port) — If this is a 5-volt supply, AD, DI, CS and CLK are TTL compatible CMOS inputs. V_{CC} may be any voltage from 4.5 V to V_{DD} allowing either TTL or CMOS compatibility.

CS (Chip Select Input) — For the MC14418, the pin is used to select a bank of TSACs.

For the MC14416, the CS is used to select that individual TSAC. All CSs are normally held low. To PROGRAM A SPECIFIC TSAC, CS must go high prior to the first falling edge of CLK. CS must stay high until the selected CTS goes low to guarantee a valid access.

CS is synchronous with DI, AD and CLK. CS can be asynchronous with DC1, DC2, FST or FSR. (This pin is normally intended to be set by a microprocessor.)

CLK (Microprocessor Clock Input) — Serial data is entered through the AD and DI pins under the control of CLK. The data is entered on the trailing edge of CLK. CLK is synchronous with CS, AD and DI and can be asynchronous with the TSAC's data clocks (DC1 or DC2).

DI (Serial Time Slot Data and Mode Input) — 8-bit words are clocked into the device through DI under the control of CLK after CS is brought high. The first 2 bits of DI control the various programming modes while the last 6 bits are time slot data. (See Figure 5 for the format of the DI word.)

AD (Serial Address and Control Bits Input — MC14418 only) — 8-bit words are clocked into the device through AD under the control of CLK after CS is brought high. AD words are loaded in parallel with the DI words. The first 3 bits of AD program the control bits Q0, Q1, and Q2 while the last 5 bits are compared with the hardware address on A1 through A5 to identify a specific TSAC in a bank. (See Figure 5 for the format of the AD words.)

A1-A5 (Codec Address Inputs — MC14418 only) — These five pins provide a unique identity for each TSAC. The TSAC address pins are either hardwired on the PC board or in the channel bank backplane. The processor loads the 5-bit address data into AD, and each MC14418 in the selected bank compares this data to the hardwired address set by its A1-A5 to determine if the time slot data loaded into DI is intended for that TSAC. By this process, only one of 32 TSACs in a bank will accept the transmitted time slot data. A1-A5 are CMOS inputs, logical "1" = V_{DD} and logical "0" = V_{SS}.

Q0, Q1, Q2 (Status Bit Outputs — MC14418 Only) — These three bits are programmed by the first 3 bits of the 8-bit word which is loaded into AD. The bits are used for the basic control functions of a line circuit. See the applications section (ref. Figure 11) for an example of how these status bits are used. In this example, Q1 selects to receive data streams, Q0 is used for the power down control, and Q2 is used for the ring enable. These are CMOS outputs.

R2 (Reset Input for Q2) — The R2 input provides a direct reset of the Q2 output. When R2 is taken high, Q2 is set to "0" independent of all other TSAC functions. See the applications section (ref Figure 11) for an example of how this reset bit is used, i.e., the ring trip signal is used to reset Q2 which is the ring enable. This combination of R2 and Q2 allows a simple solution to the ring trip function.

CTS (Clear to Send Output) — This output provides a simple diagnostic capability for the processor TSAC combination. The selected TSAC outputs the CTS signal after it has accepted data. This output goes low three data clock cycles after the next FST, and returns high on the subsequent FST. For the MC14418, only the TSAC which accepts transmitted data will respond with CTS low. All other TSACs in the bank will leave CTS high. The CTS output is an open drain transistor with a weak internal pullup. Normally a bank of CTS outputs are wire ORed together to provide a single diagnostic bus, which can be used to verify that transmitted data was properly acknowledged by some TSAC in the bank.

CTS may also be used to strobe additional supervision data into a selected channel unit, due to its dependence upon the address selection logic of the MC14418.

DC1, DC2 (Data Clock Input) — The data clock input establishes the bit rate of the TSAC and its associated codec. It is intended to be between 1.536 and 2.56 MHz and is the same as the codec's bit rate clock. Both TSACs divide

these inputs by eight to derive the time slot rate. For the MC14418, DC1 provides the data rate clock for both transmit and receive time slot computation. The MC14416 derives transmit timing from DC1 and receive timing from DC2. They are CMOS compatible inputs.

FST, FSR (Frame Sync Transmit and Frame Sync Receive Inputs) — These inputs are leading-edge sensitive synchronization pulses for establishing the position of time slot zero in the transmit and receive frames, respectively.

The rising edge of DC (1 or 2) associated with the rising edge of FST or FSR identifies the sign bit period of time slot zero. See Figures 6 and 7 for detailed timing. In the MC14418, both zero time slots are derived from DC1 but may be different by an integral number of bits. In the MC14416, FST and DC1 derive the transmit time slot zero, while FSR and DC2 derive the receive time slot zero independently. DC1 and DC2 can be asynchronous. FSR and FST are CMOS inputs.

TXE, RXE (Transmit Enable and Receive Enable Outputs) — These are the outputs of the time slot computation circuitry. Each output is high for eight data clocks; i.e., an integral number of time slots after the rising edge of FST and FSR for TXE and RXE, respectively. The binary number entered in the last 6 bits of the DI input indicates the number of eight data clock intervals (time slots) between FST or FSR and the eight data clock time slot, when TXE or RXE will be high. These are CMOS B series outputs which will drive one TTL LS input when V_{DD} is five volts. See Figure 6 and Figure 7 for detailed timing and numbering.

TABLE 1 — BASIC OPERATION OF MC14418

Input Conditions				Action to Outputs After Next FST						
TS Data Received	Address Compare	b0	b1	CTS	TX Reg. Load	RX Reg. Load	TXE Disabled	RXE Disabled	Data Reg. (Q0-Q2) Load	Time Slot Counters Running
No	X	X	X	1	No	No	No Change	No Change	No	No Change
Yes	No	X	X	1	No	No	No Change	No Change	No	No Change
Yes	Yes	0	0	0	Yes	Yes	No	No	Yes	Yes
Yes	Yes	0	1	0	Yes	No	No	No	Yes	Yes
Yes	Yes	1	0	0	No	Yes	No Change	No	Yes	Yes
Yes	Yes	1	1	0	X	Yes	Yes	Yes	Yes	No

TABLE 2 — BASIC OPERATION OF MC14416

Input Conditions					Action to Outputs After Next FST			
TX Data Received	CS	b0	b1	CTS	TX Reg. Load	RX Reg. Load	TXE Disabled	$\overline{PD}$ Output
No	X	X	X	1	No	No	No Change	No Change
Yes	0	X	X	1	No	No	No Change	No Change
Yes	1	0	0	0	Yes	Yes	No	1
Yes	1	0	1	0	Yes	No	No	1
Yes	1	1	0	0	No	Yes	No Change	1
Yes	1	1	1	0	No	No	Yes	0

Note 1: The $\overline{OHO}$ output remains operational when TXE is disabled.

FIGURE 5 — FORMAT FOR DI AND AD WORDS

MC14418	DI Word Input First Bit Sent								AD Word Input First Bit Sent							
Results of Bit Pattern	Mode		Time Slot Data						Status Bits			Address Data				
	b0	b1	t6	t5	t4	t3	t2	t1	q2	q1	q0	a5	a4	a3	a2	a1
Assign TSAC 16 to the first time slot (TSO) for both receive and transmit and set its status bit to 011	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0
Assign TSAC 1 to time slot 8 for receive only and set status bits to 011	1	0	0	0	1	0	0	0	0	1	1	0	0	0	0	1
Assign TSAC 8 to time slot 2 for transmit only and set status bits to 011	0	1	0	0	0	0	1	0	0	1	1	0	1	0	0	0
Program TSAC 4 to idle (no time slot outputs) and set status bits to 011	1	1	X	X	X	X	X	X	0	1	1	0	0	1	0	0
Codec 1 is powered down (80 = 0)	X	X	X	X	X	X	X	X	0	1	0	0	0	0	0	1
Line circuit associated with codec 2 is programmed to ring the line (See Fig. 13)	X	X	X	X	X	X	X	X	1	1	1	0	0	0	1	0

MC14416

Assign the selected TSAC to the first time slot (TSO) for both receive and transmit and set $\overline{PD} = 1$	0	0	0	0	0	0	0	0
Assign the selected TSAC to time slot 8 for receive only and set $\overline{PD} = 1$	1	0	0	0	1	0	0	0
Assign the selected TSAC to time slot 2 for transmit only and set $\overline{PD} = 1$	0	1	0	0	0	0	1	0
Power down the selected TSAC, i.e., $\overline{PD}$ to "0"	1	1	X	X	X	X	X	X

*See Figures 12 and 13 for the hardware implementations using MC14418 and MC14416.

FIGURE 6 — DATA MULTIPLEX TIMING FOR 2.048 MHz

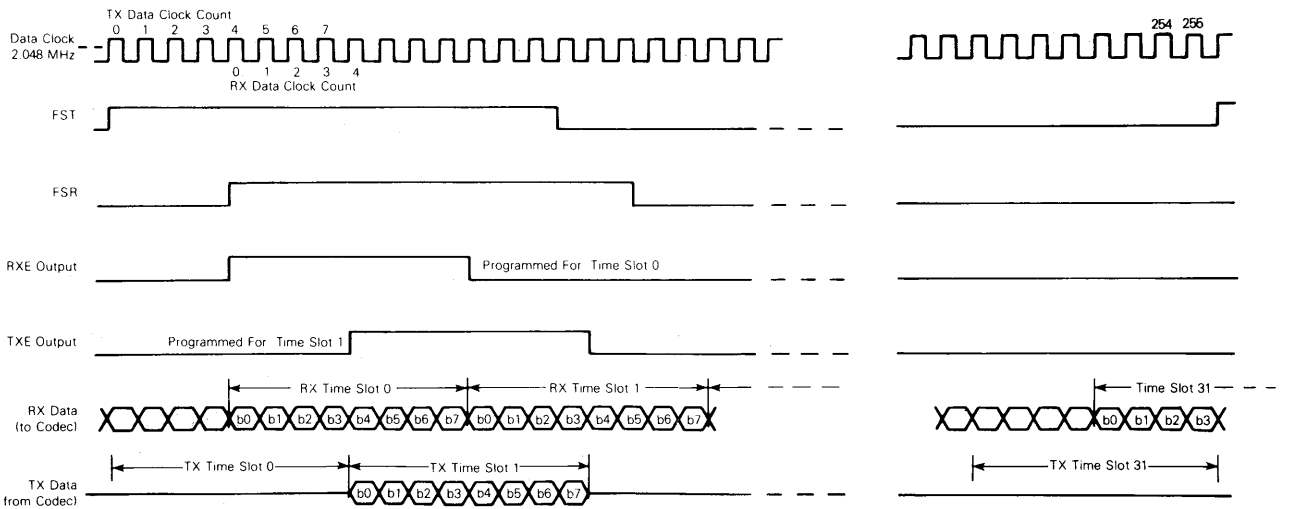
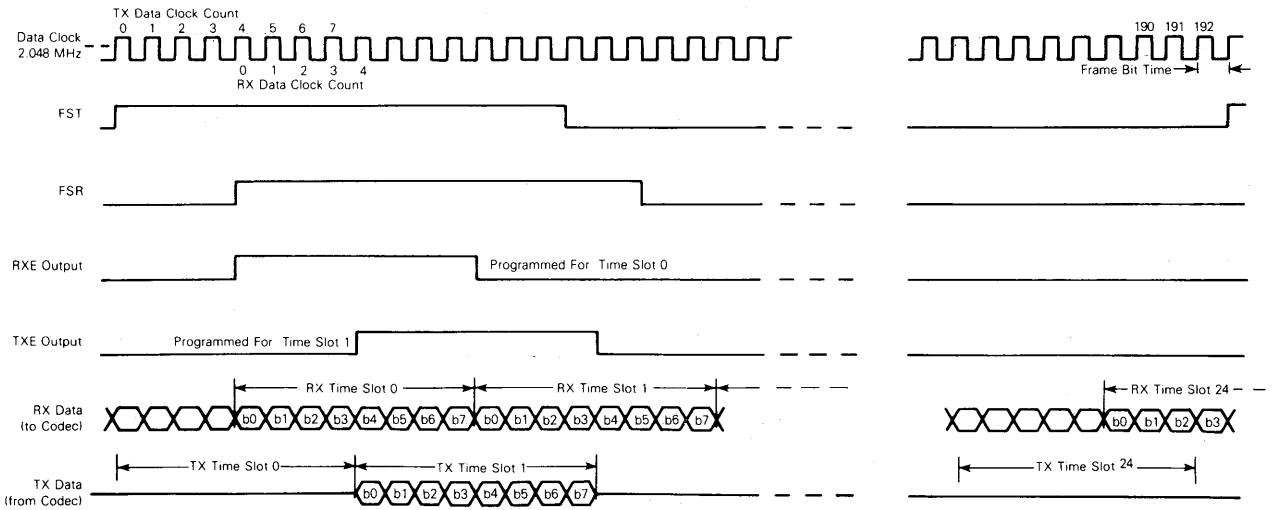


FIGURE 7 — DATA MULTIPLEX TIMING FOR 1.544 MHz



$\overline{PD}$ (Power Down Output — MC14416 Only) — The $\overline{PD}$ output is normally high. It is set high whenever b0 or b1 is a zero and the TSAC is programmed. If b0 and b1 are both one, then PD will be set low. This output is intended to be used to power down other circuitry in the channel unit when the channel unit is idle. This is a CMOS B series output which will drive one TTL LS load when V_{DD} is five volts.

OHI (Off Hook Input — MC14416 Only) — The OHI is a CMOS input with an internal pull-down resistor. A DC level at this pin will appear at the OHO output during the programmed TXE time slot.

$\overline{OHO}$ (Off Hook Output Inverted — MC14416 Only) — During the programmed transmit time slot, the data at OHI appears inverted at $\overline{OHO}$; otherwise $\overline{OHO}$ will be pulled high passively. The $\overline{OHO}$ output is an open drain N-channel transistor with a weak pull-up to V_{DD}. A number of these outputs can be wire ORed together to form a hook status bus consisting of a serial stream of hook information from a bank of channels. When the MC14416 powers down its codec, the TXE output is disabled; but the $\overline{OHO}$ output continues to multiplex out OHI and transmit time slot information during the previously entered transmit time slot.

V_{SS} — This is the most negative supply pin and digital ground for the package.

V_{DD} — This is the most positive supply. V_{DD} is typically 12 V with an operation range of 5 to 16 volts. All logic outputs swing the full supply voltage.

APPLICATIONS

The following section is intended to facilitate device understanding through several application examples. Included are Data Multiplex Timing Diagrams, a description of the TSAC Microprocessor port, a sample program, two circuit configurations using Motorola's devices, a systems drawing and two suggested clock circuits for obtaining codec data and control clocks.

In Figures 6 and 7 are shown Data Multiplex Timing Diagrams for 2.048 MHz and 1.544 MHz data clocks. The major points to be seen from these examples are:

1) Receive and transmit programming for the MC14418 are bit synchronous and word asynchronous. The MC14416 can be completely asynchronous.
2) The rising edges of FST and FSR initiate the programming frame for transmit and receive channels, respectively, and identify transmit and receive time slot "0," respectively.
3) Time slots identify eight data clock words. In this example: the transmit time slot is programmed as time slot "1." Therefore, bits 8 through 15 after FST are time slot "1."
4) For the 1.544 MHz clock, the framing bit is at the very end of the frame.

TSAC Microprocessor Port (MC14418 and MC14416) — The MC14418 provides four pins with 5-volt microprocessor input characteristics. These are AD, CS, CLK, and DI. The input supply for these inputs is V_{CC}. The CTS output is an open drain device with a weak pull up to V_{DD}. Typically, these five pins are bused in parallel to 24 or 32 TSACs per processor port. If desired, AD, CLK, DI, and CTS may be bused to greater than 32 TSACs by using the CS input as a group select. A microprocessor port of eight bits can thus control four groups of 32 TSACs with no additional decoding, as shown in Figure 8.

In order to program any given codec to a transmit or receive time slot, the processor simply exercises the corresponding 8-bit port.

Beginning with CS1 to CS4 low, all TSACs in the bank have their data registers in the Ready for Data Mode. The microprocessor takes the appropriate CS high and clocks in two bits of data into the 32 selected TSACs through DI and AD using CLK. The microprocessor presents data on the leading edge of CLK and the TSACs clock in data on the trailing edge of CLK. After eight CLK pulses (high, then low) the 32 selected TSACs will have two new 8-bit words; one in the data register through DI and one in the address register through AD. The unique TSAC, whose last 5 bits of the address register match its hardwired address on A1 through A5, acknowledges the new data. After the next FST, the selected TSAC will pull CTS low. This event notifies the processor that its transmission has been recognized. If CTS occurs at any other time, the processor can recognize the fault condition and restart the transmission using the reset function of the TSAC chip select. The uniquely selected TSAC will load its new program data into the appropriate TIME SLOT register on the next leading edge of FST. The bank of 32 TSACs will internally reset to the Ready for Data Mode when the transmission is completed, after the next FST. The TSAC, which was uniquely selected, and which has CTS low, will clear CTS to the pulled-up condition with the next FST. The processor may now program a new time slot immediately, with or without returning the selected CS low. Time Slot data can thus be sent at the rate of once every 256 μsec. for 8 kHz sampling (FST). The processor need not operate in an interrupt mode even though the TSAC's DC and CLK are asynchronous.

The processor port of the MC14416 works similarly to the MC14418, but will accept data if CS is high, and does not compare a hardwired address to the address word.

Figure 11 shows the typical signal timing for programming the microprocessor port.

To demonstrate the programming of the TSAC, consider the following configuration. A microprocessor is used to control four groups of thirty-two TSACs through an eight-bit PIA port. Four of the PIA lines are used for group select lines. The other four lines are dedicated to CLK, DI, AD, and CTS. The TSACs are programmed by serially loading bits into the DI and AD leads. Data bits are latched on the falling edge of CLK. The PIA port is connected as shown in Figure 9. The flow chart in Figure 10 and the following program illustrate one method of TSAC programming.

Before running the following program, the address, time slot, and group number must be entered in appropriate locations. During execution, CS (group select), AD, and DI words are arranged for serial presentation to the TSACs. The bits are presented with CLK high and are latched in with the falling edge of CLK. After eight passes through the loop, the TSAC is programmed, and CTS falls on the third data clock pulse after the next FST. The program waits for CTS to go high again before removing CS to prevent aborting the TSAC's programming. This program allows a maximum rate of programming equal to one TSAC per two frames.

FIGURE 8 — TYPICAL 8-BIT PORT

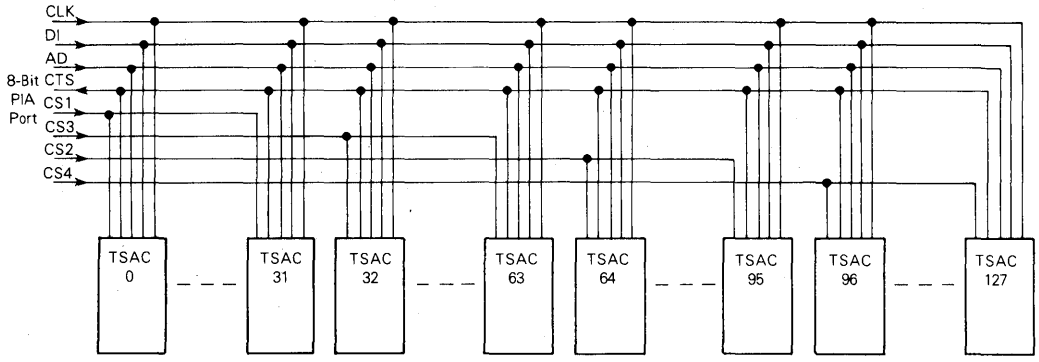


FIGURE 9 — PIA PORT ASSIGNMENT

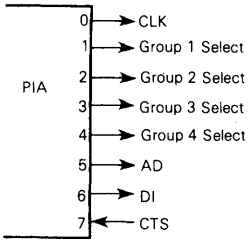
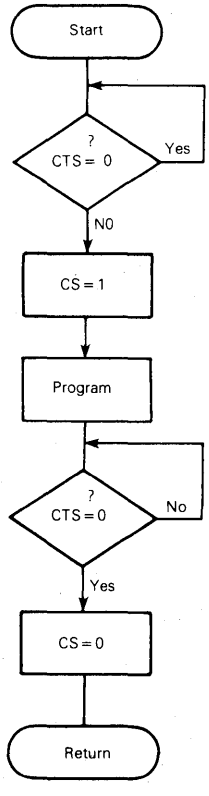


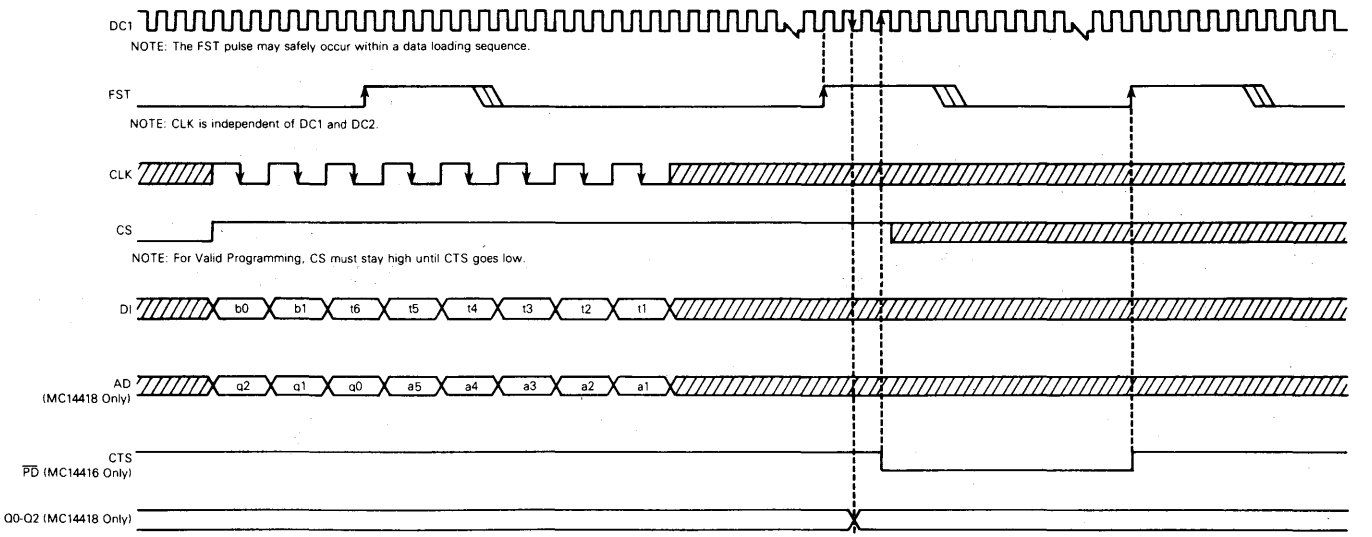
FIGURE 10 — TSAC PROGRAMMING FLOW CHART



Instructions for use:
Load in AD word (Q2, Q1, Q0, A5, A4, A3, A2, A1)
DI word (b0, b1, t6, t5, t4, t3, t2, t1)
group word
Start routine.

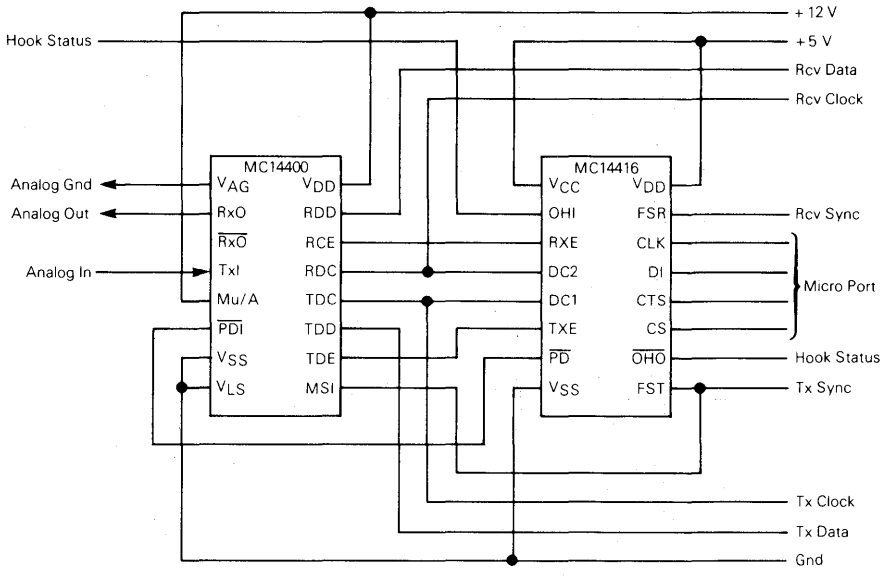
```
        LDAA GROUP      STORE GROUP # IN ACCA
        DECA            CHECK IF EQ. TO ONE
        BNE ONE         IF NOT GO TO NEXT TEST
        LDAB #03        EQUALS ONE
        STAB SELECT     LOAD PROPER SELECT BITS IN SELECT WORD
        BRA START       JUMP TO NEXT PART
ONE     DECA            IS GROUP EQ. TO TWO?
        BNE TWO         IF NOT GO TO NEXT TEST
        LDAB #05        LOAD PROPER SELECT BITS IN SELECT WORD
        STAB SELECT
        BRA START       JUMP TO NEXT PART
TWO     DECA            CHECK IF EQ. TO THREE
        BNE THREE       IF NOT IS EQ. TO FOUR
        LDAB #09        LOAD PROPER SELECT BITS IN SELECT WORD
        STAB SELECT
        BRA START       JUMP TO NEXT PART
THREE   LDAB #11        LOAD GROUP SELECT BITS FOR GROUP FOUR
        STAB SELECT
START   LDAA #00        INITIALIZE PIA
        STAA CONTRLB    INITIALIZE PIA
        LDAA #7F        INITIALIZE PIA
        STAA DDRB       INITIALIZE PIA
        LDAA #04        INITIALIZE PIA
        STAA CONTRLB    INITIALIZE PIA
        LDAB #80        TEST FOR CTS HIGH
WAIT    BITB PIAOUT     WAIT FOR CTS HIGH
        BEQ WAIT
        LDAA #01        NOW CTS IS HIGH, SET CLK HI AND LEAVE CS LOW
        STAA PIAOUT
        LDAA #08        INITIALIZE LAP COUNTER
        STAA COUNTER
        LDX 00          MOVE AD AND DI INPUTS
        STX 02          TO SHIFT LOCATIONS
        LDAA SELECT     BRING CS HIGH
        STAA PIAOUT
LOOP    LDAA SELECT     START BIT STUFFING
        ROL 0002        CHECK AD WORD
        BCC 02          CHECK AD WORD
        ORAA 20         CHECK AD WORD
        ROL 0003        CHECK DI WORD
        BCC 02          CHECK DI WORD
        ORAA 40         CHECK DI WORD
        STAA PIAOUT     WRITE BITS TO TSAC
        DECA            WRITE FALLING EDGE OF CLK
        NOP             WRITE FALLING EDGE OF CLK
        NOP             WRITE FALLING EDGE OF CLK
        STAA PIAOUT     WRITE FALLING EDGE OF CLK
        DEC COUNTER     DECREMENT LAP COUNTER
        BNE LOOP        TEST FOR LOOP COMPLETION
        LDAB #80        TEST AND WAIT FOR CTS LOW
ISITLO  BITB PIAOUT     TEST AND WAIT FOR CTS LOW
        BNE ISITLO      TEST AND WAIT FOR CTS LOW
        CLR PIAOUT      REMOVE CS (GROUP SELECT)
        RTS             RETURN FROM SUBROUTINE
```

FIGURE 11 — MICROPROCESSOR PORT TIMING



NOTE: For the MC14416, the CTS line is pulled low by the device selected by the CS pin.
For the MC14418, the CTS line is pulled low by the device whose address matches the data loaded in through the AD pin.

FIGURE 12 — TYPICAL CIRCUIT CONFIGURATION USING MC14416 IN CONJUNCTION WITH MC14400



2

FIGURE 13 — A COMPLETE SINGLE PARTY CHANNEL UNIT USING MC3419 SLIC, MC14403 PCM MONO-CIRCUIT, MC14418 TSAC

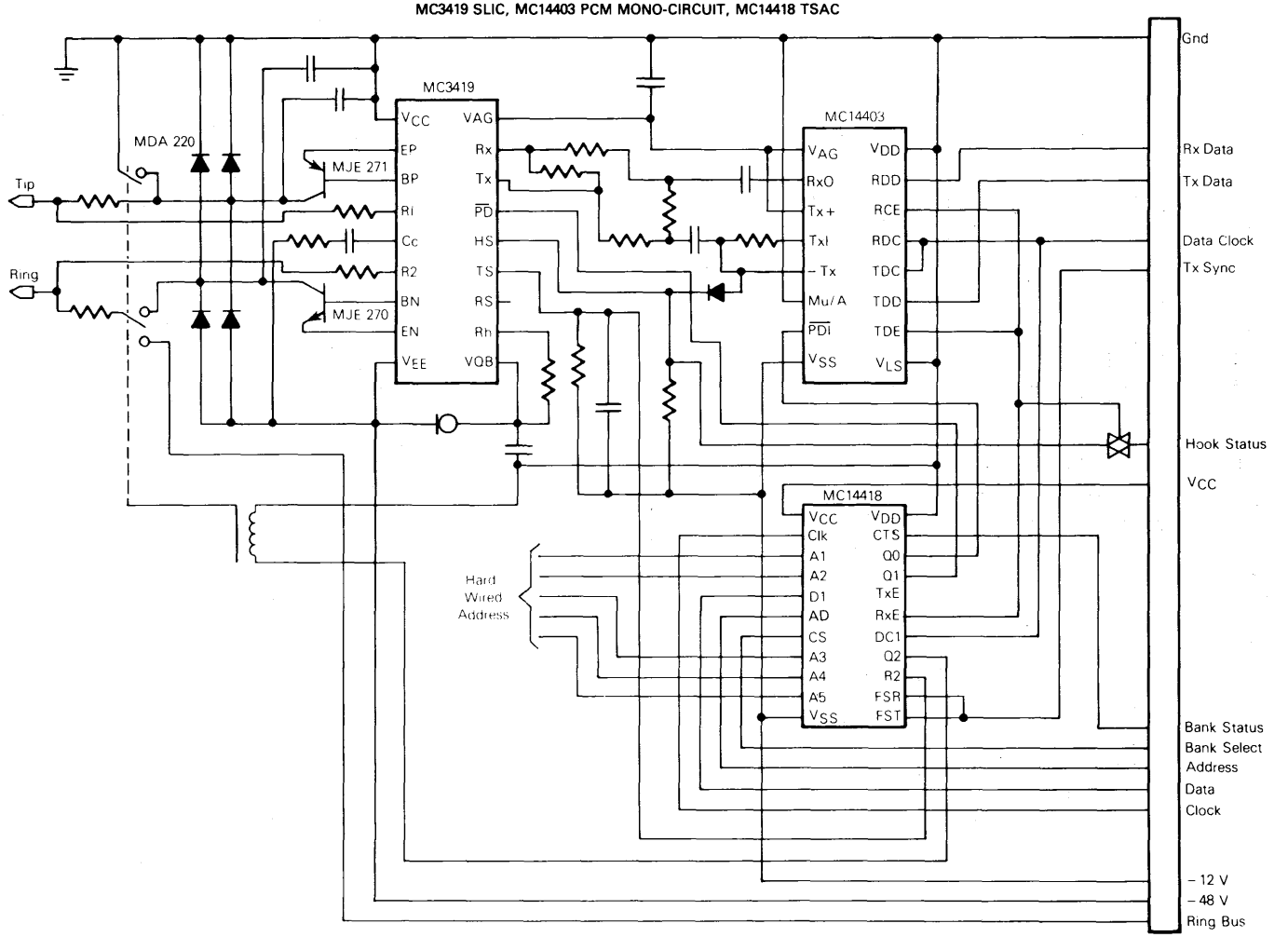
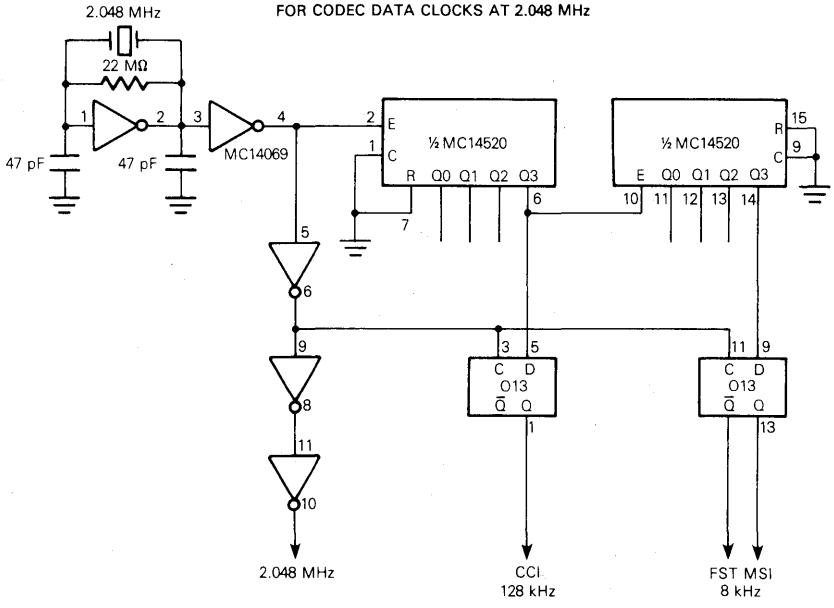


FIGURE 14 — CLOCK CIRCUIT AND TIMING
FOR CODEC DATA CLOCKS AT 2.048 MHz



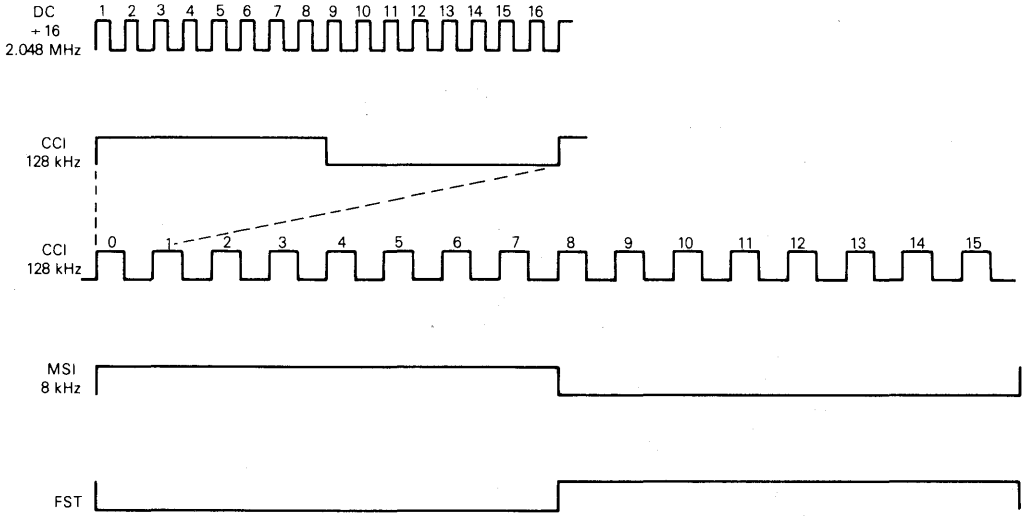
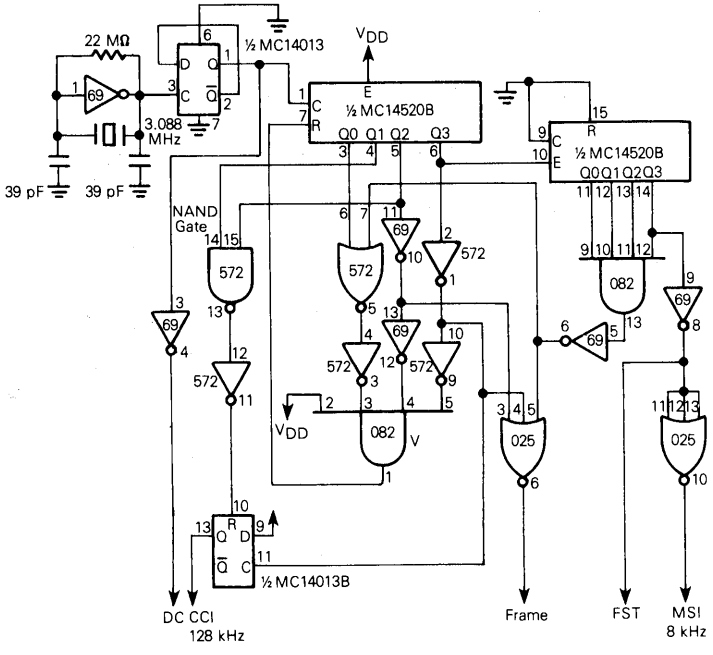
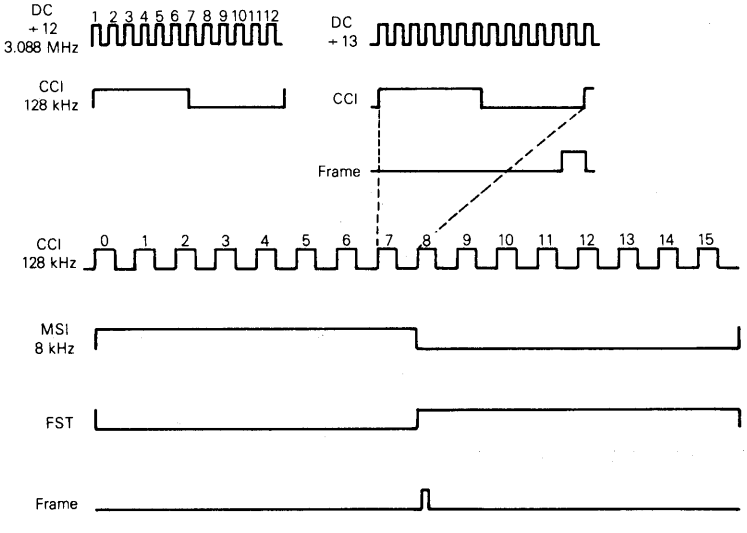


FIGURE 15 — CLOCK CIRCUIT AND TIMING
FOR CODEC DATA CLOCKS AT 1.544 MHz





MOTOROLA

MC14417

CMOS LSI
(LOW-POWER COMPLEMENTARY MOS)

TSAC
TIME SLOT ASSIGNER
CIRCUIT

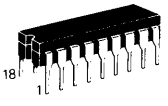
2

BASIC TIME SLOT ASSIGNER CIRCUIT (TSAC)

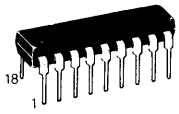
The MC14417 is a per channel Time Slot Assigner Circuit (TSAC) that produces 8-bit receive and transmit time slots for a PCM Codec. The pins D0 to D5 are the time slot data inputs which can be either hard-wired on the printed circuit board for fixed time slot assignment, or externally programmed through the use of these pins and the latch enable function. The receive and transmit frame syncs and enables are independent. In addition, a T/R (TXE/RXE swap) input is provided which allows a simplified switching mechanism for a small systems architecture (i.e., key systems).

The MC14417 can operate from a single 5-volt supply for TTL levels or up to 16-volts for CMOS levels. The MC14417 is fabricated using the CMOS technology for reliable low-power performance.

- TTL and CMOS Level Compatibility
- 5 to 16 Volt Operation
- Low Operating Power Consumption
- For Use With Up to 2.56 MHz Clocks
- Independent Transmit and Receive Frame Syncs and Enables
- Up to 64 Time Slots Per Frame
- Compatible with MC14400/01/02/03/05 PCM Mono-Circuits
- Allows Swapping of Transmit Enable (TXE) and Receive Enable (RXE) Signals
- CMOS Metal Gate for High Reliability



L SUFFIX
CERAMIC PACKAGE
CASE 726

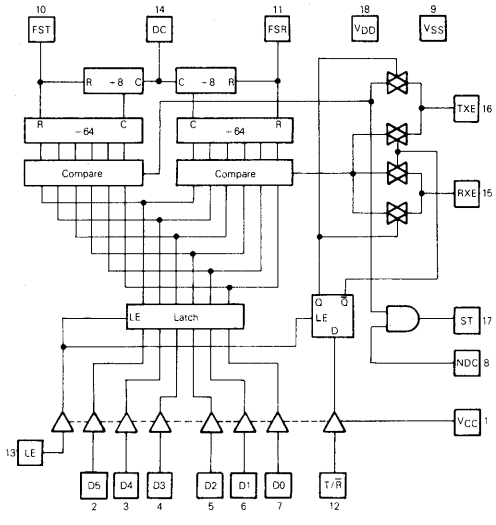


P SUFFIX
PLASTIC PACKAGE
CASE 707

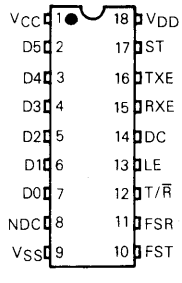
ORDERING INFORMATION

MC14XXX — Suffix Denotes
- L Ceramic Package
- P Plastic Package

BLOCK DIAGRAM



PIN ASSIGNMENT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	−0.5 to 18	V
Level Shift Voltage	V_{CC}	−0.5 to V_{DD}	V
Input Voltage Inputs Referenced to V_{DD} to V_{CC}	 V_{in1} V_{in2}	 −0.5 to V_{DD} + 0.5 −0.5 to V_{DD} + 0.5	V
DC Current Drain per Pin	I	10	mA
Operating Temperature Range	T_A	−40 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +165	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C)

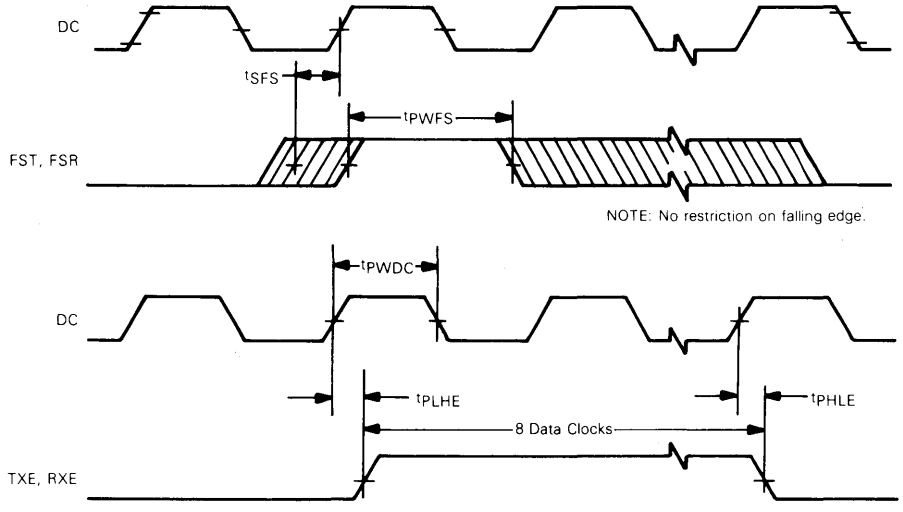
Characteristic		Symbol	V_{DD}	Min	Typ	Max	Unit
DC Supply Voltage, V_{SS} = 0 V		V_{DD}	–	4.5	12	16	V
DC Supply Voltage, V_{SS} = 0 V		V_{CC}	–	4.5	5	V_{DD}	V
Output Current TXE, RXE, ST (V_{OL} = 0.4 V) (V_{OL} = 1.0 V)		I_{OL}	5 12	0.51 2.0	– 4.0	– –	mA
(V_{OH} = 4.6 V) (V_{OH} = 11.0 V)		I_{OH}	5 12	−0.2 −2.0	– −4.0	– –	mA
Input Voltage (CMOS) FST, FSR, DC1, DC2, NDC	"0"	V_{IL}	5 12	– –	– –	1.0 2.4	V
	"1"	V_{IH}	5 12	4.0 9.6	– –	– –	V
Input Voltage (TTL) D0-D5, LE, T/$\overline{R}$, V_{CC} = 5 V	"0"	V_{IL}	5 12 16	– – –	– – –	0.8 0.8 0.7	V
	"1"	V_{IH}	5 12	2.0 2.0	– –	– –	V
Total Supply Current (Outputs Unloaded) DC1 at 2.048 MHz		I_T	5 12	– –	1.5 2.5	– –	mA

SWITCHING CHARACTERISTICS (C_L = 50 pF, T_A = 25°C, Unless Otherwise Noted)

Characteristic	Symbol	V_{DD}	Min	Typ	Max	Unit
Output Rise Time, TXE, RXE, ST	t_r	5 12	– –	100 50	200 100	ns
Output Fall Time, TXE, RXE, ST	t_f	5 12	– –	100 50	200 100	ns
Frame Sync Setup Time (See Figure 1)	t_{SFS}	5 12	−150 −75	– –	+150 +75	ns
Frame Sync Pulse Width	t_{PWFS}	5 12	200 100	– –	– –	ns
Propagation Delay (Note 1) DC1 to TXE, DC2 to RXE, C_L = 20 pF	t_{PHLE}, t_{PLHE}	5 12	– –	130 80	180 125	ns
Data Clock Frequency	f_{DC}	5 12	– –	– –	2.048 2.6	MHz
Data Clock Pulse Width at f_{DC} (Max)	t_{PWDC}	5 12	200 140	244 192	293 260	ns
LE Pulse Width	t_{PWLE}	5 12	1 1	– –	– –	μs
NDC to ST Propagation Delay		5 12	– –	– –	120 80	ns
FST to ST Propagation Delay		5 12	– –	– –	200 130	ns

NOTE 1: For time slot 0, t_{PHLE} and t_{PLHE} are measured from the leading edge of DC or FST (FSR), whichever occurs last.

FIGURE 1 — TIMING DIAGRAMS



PIN DESCRIPTIONS

V_{CC} (Positive Supply) — The V_{CC} power supply controls the inputs LE, D0-D5 and T/$\overline{R}$. It can be supplied by any voltage from 4.5 to V_{DD}. In typical usage, V_{CC} is 5 volts for TTL or microprocessor compatibility of the control inputs to the TSAC while V_{DD} and V_{SS} are connected to the Codec supplies.

D5-D0 (Parallel Time Slot Data Inputs) — The six inputs to the input-storage latch are the time-slot data. D0 is the least-significant bit while D5 is the most-significant. The binary word at this input represents the number of 8 bit time slots from FST and FSR where TXE and RXE will occur, respectively. These can be 5-volt input compatible with TTL and are internally level shifted to the V_{DD} supply.

LE (Latch Enable Input with Internal Pull-Up) — This input allows the data D0 through D5 and T/$\overline{R}$ bits to be latched in the input-storage latch. If LE is held high, then the inputs to the latch are combinational and directly applied to the compare circuits. When LE is pulled low, the input values applied at D0 through D5 and T/$\overline{R}$ are latched and held in the storage latch.

T/$\overline{R}$ (TXE/RXE Swap Input with Internal Pull-Up) — This input allows the TXE and RXE inputs to be swapped. When T/$\overline{R}$ is a one, the TXE output is derived from FST and RXE from FSR. If T/$\overline{R}$ is a zero, the derivation is reversed. If FST and FSR are eight data clocks apart, then two TSAC channels programmed to the same D0 through D5 and different T/$\overline{R}$ bits will create a completed conversation. This feature is intended for use in simplifying small-key systems.

DC (Data Clock Input) — The data clock input establishes the bit rate for the TSAC. This is typically 1.544 or 2.048 MHz but can be any frequency up to 2.56 MHz. The data clock is divide-by-8 for both transmit- and receive-time slots. The data clock input is a CMOS compatible input between V_{DD} and V_{SS}.

FST (Frame Sync Transmit Input) — This input identifies the beginning of the zero-transmit time slot by resetting the divide-by-8 and divide-by-64 counters. FST is a CMOS compatible input between V_{DD} and V_{SS}. The TXE output will begin and end on one 8-bit word boundary which is synchronized with the FST input. The FST signal should be aligned with the leading edge of data clock and is typically 8 kHz.

FSR (Frame Sync Receive Input) — The FSR input provides the same functions for the RXE output as FST did for TXE. The FSR and FST inputs can be any number of data clocks different, or can be the same.

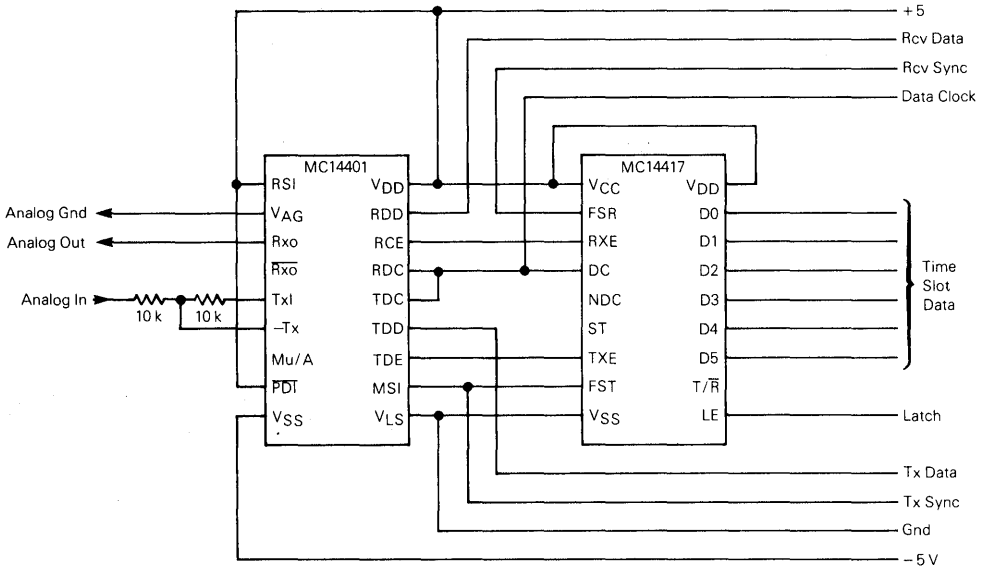
TXE, RXE (Transmit-Enable and Receive-Enable Outputs) — These outputs are used to control the transmitting and receiving of data words to and from Codecs. Each output swings from V_{DD} to V_{SS} and is eight data clocks long. TXE and RXE go high at the beginning of the programmed time slot and low at the end. TXE is derived from FST and RXE is derived from FSR, provided the T/$\overline{R}$ bit is high.

ST (Strobe Output) — The strobe output is provided to allow simplified input data storage or off-hook multiplexing control. ST is the logical AND of an enable signal (NDC) and the TXE time slot period. Thus, ST can only be high during a programmed TXE time slot. Since no other TSAC in a bank can have the same TXE programming, the ST output on any TSAC can be used to uniquely identify that TSAC by a pulse input on NDC. In many applications ST is used to control the LE input.

NDC (New Data Clock Input with Internal Pull-Up) — This input can be used in conjunction with ST to strobe data into a TSAC bank. NDC can be used to enable the strobe output.

V_{DD}, V_{SS} — The TSAC will operate from any single supply from 4.5 to 16 volts. The TSAC can be used in a 5-volt-only system by making both V_{CC} and V_{DD} 5 volts.

FIGURE 2 — MOTOROLA MONO-CIRCUIT/TSAC COMBINATIONS



The MC14417 TSAC offers simple flexible time slot assignment for the PCM mono-circuit. Assignments are wired or latched into the data port. The MC14401 offers supply flexibility of ±5, ±6, +12, or +10 V with 18 pin packages and TTL compatibility.

MOTOROLA

MC14419

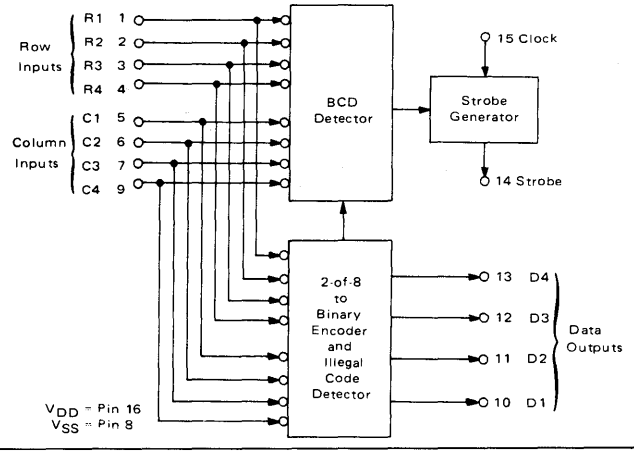
2-OF-8 KEYPAD-TO-BINARY ENCODER

The MC14419 is designed for phone dialer system applications, but finds many applications as a keypad-to-binary encoder. The device contains a 2-of-8 to binary encoder, a strobe generator, and an illegal state detector. The encoder has four row inputs and four column inputs, and is designed to accept inputs from 16 keyswitches arranged in a 4 × 4 matrix. For an output on the four data lines, one and only one row along with one and only one column input line must be activated. All other combinations are suppressed by the illegal state detector to eliminate false data output.

The strobe generator produces a strobe pulse when any of the 10 keys corresponding to numerals 0 through 9 are depressed. The strobe output can be used to eliminate erroneous data entry due to contact bounce. For a strobe output to occur, the key row and column input lines must remain stable for 80 clock pulses after activation. When the contact bounce has settled and 80 clock pulses have occurred, the output will be a single strobe pulse equal in width to that of the clock low state. The strobe generator will output one and only one pulse each time a numerical key is depressed. After the pulse has occurred, noise and bounce due to contact break will not cause another strobe pulse. With a 16 kHz input clock frequency, the pulse occurs 5 ms after the last bounce.

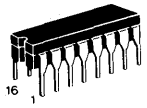
- Suppressed Output for Illegal Input Codes
- On-Chip Pullup Resistors for Row and Column Inputs
- Clock Input Conditioning Circuit
- Low Current Drain in Standby Mode
  5.0μA Typical @ 5.0 Vdc
- Subsystem Complement to the MC14408/14409 Phone Pulse Converter
- Codes for Numbers 0-9 Produce a Strobe Pulse
- One Key Rollover Feature

BLOCK DIAGRAM

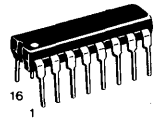


CMOS
(LOW-POWER COMPLEMENTARY MOS)

2-OF-8 KEYPAD-TO-BINARY ENCODER



L SUFFIX
CERAMIC PACKAGE
CASE 620



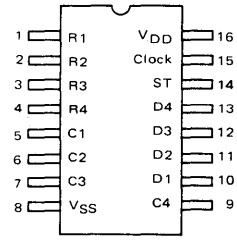
P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXX

Suffix	Denotes
L	= Ceramic
P	= Plastic

PIN ASSIGNMENT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

2

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8.)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	+6.0 to -0.5	Vdc
Input Voltage, All Inputs	V_{in}	V_{DD} + 0.5 to V_{SS} -0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range	T_A	-40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	-40°C Min	-40°C Max	25°C Min	25°C Typ	25°C Max	+85°C Min	+85°C Max	Unit
Supply Voltage Operating Range	V_{DD}	–	3.0	6.0	3.0	5.0	6.0	3.0	6.0	Vdc
Output Voltage "0" Level	V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	Vdc
"1" Level		5.0	4.99	–	4.99	5.0	–	4.95	–	Vdc
Noise Immunity ($\Delta V_{out} \leq 0.8$ Vdc)	V_{NL}	5.0	1.5	–	1.5	2.25	–	1.4	–	Vdc
	V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	Vdc
Output Drive Current (V_{OH} = 2.5 Vdc) Source	I_{OH}	5.0	-0.23	–	-0.20	-1.7	–	-0.16	–	mAdc
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.23	–	0.20	0.78	–	0.16	–	mAdc
Input Leakage Current ($V_{in} = V_{DD}$)	I_{IH}	5.0	–	–	–	10	–	–	–	pAdc
Pullup Resistor Source Current (Row and Column Inputs) ($V_{in} = V_{SS}$)	I_{IL}	5.0	265	460	190	250	330	125	215	μAdc
Input Capacitance ($V_{in} = V_{SS}$)	C_{in}	–	–	–	–	5.0	–	–	–	pF
Standby Supply Current (f_{clock} = 16 kHz, No Keys Depressed)	I_{DDS}	3.0	–	3.0	–	1.0	3.0	–	6.0	μAdc
		5.0	–	15	–	5.0	15	–	30	
		6.0	–	60	–	20	60	–	120	
Standby Supply Current as a Function of Clock Frequency* (No Keys Depressed)	I_{DDS}	5.0	I_{DDS} = 0.09 μA/kHz + 3.0 μA							μAdc

*The formula given is for the typical characteristics only.

SWITCHING CHARACTERISTICS (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ	Max	Unit
Output Rise and Fall Times, D1 thru D4 (Figure 1)	t_r, t_f	5.0	–	300	–	ns
Propagation Delay Time, Row or Column Input to Data Output (Figure 1)	t_{PLH}, t_{PHL}	5.0	–	1000	–	ns
Clock Pulse Frequency Range	PRF	3.0 to 6.0	4.0	16	80	kHz

FIGURE 1 – SWITCHING TIME WAVEFORMS

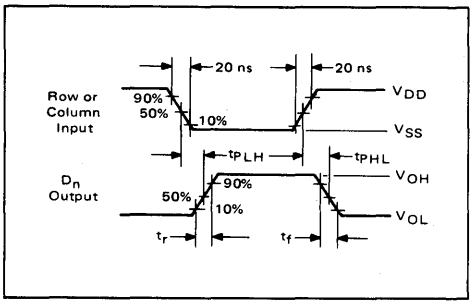
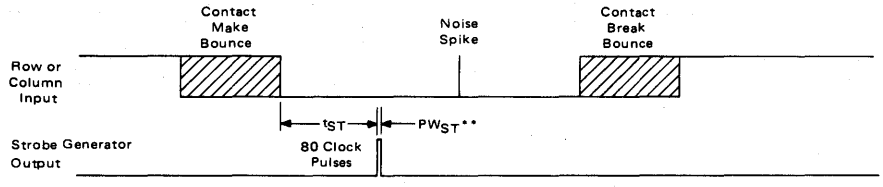


FIGURE 2 – TYPICAL STROBE PULSE DELAY TIMES

PRF Clock Frequency kHz	t_{ST}* Strobe Pulse Delay Time ms
4.0	20
8.0	10
16	5.0
32	2.5
80	1.0

*t_{ST} = (1/PRF) • 80, with PRF in kHz, t_{ST} in ms.

FIGURE 3 – STROBE GENERATOR TIMING DIAGRAM



**PW_{ST} = Strobe Pulse Width = Low State Clock Pulse Width (PW_L).

TRUTH TABLE

	Inputs								Outputs				
	Row				Column								
Key**	R4	R3	R2	R1	C4	C3	C2	C1	D4	D3	D2	D1	Strobe
1	1	1	1	0	1	1	1	0	0	0	0	1	⎍
2	1	1	1	0	1	1	0	1	0	0	1	0	⎍
3	1	1	1	0	1	0	1	1	0	0	1	1	⎍
A	1	1	1	0	0	1	1	1	1	1	0	0	0
4	1	1	0	1	1	1	1	0	0	1	0	0	⎍
5	1	1	0	1	1	1	0	1	0	1	0	1	⎍
6	1	1	0	1	1	0	1	1	0	1	1	0	⎍
B	1	1	0	1	0	1	1	1	1	1	0	1	0
7	1	0	1	1	1	1	1	0	0	1	1	1	⎍
8	1	0	1	1	1	1	0	1	1	0	0	0	⎍
9	1	0	1	1	1	0	1	1	1	0	0	1	⎍
C	1	0	1	1	0	1	1	1	1	1	1	0	0
*	0	1	1	1	1	1	1	0	1	0	1	0	0
0	0	1	1	1	1	1	0	1	0	0	0	0	⎍
#	0	1	1	1	1	0	1	1	1	0	1	1	0
D	0	1	1	1	0	1	1	1	1	1	1	1	0
	All Other Combinations								0	0	0	0	0

**See Figure 4 for keypad designation.

2

FIGURE 4 – TYPICAL KEYPAD INTERFACE APPLICATION

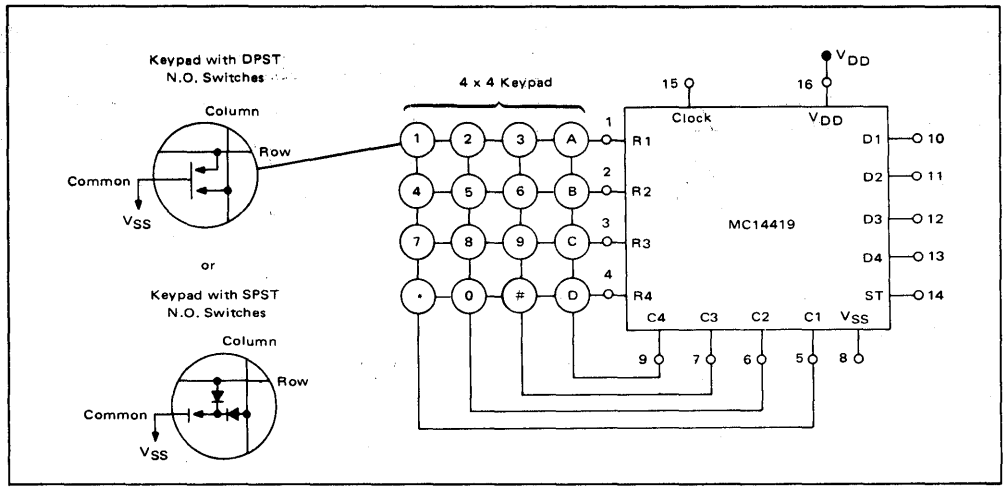
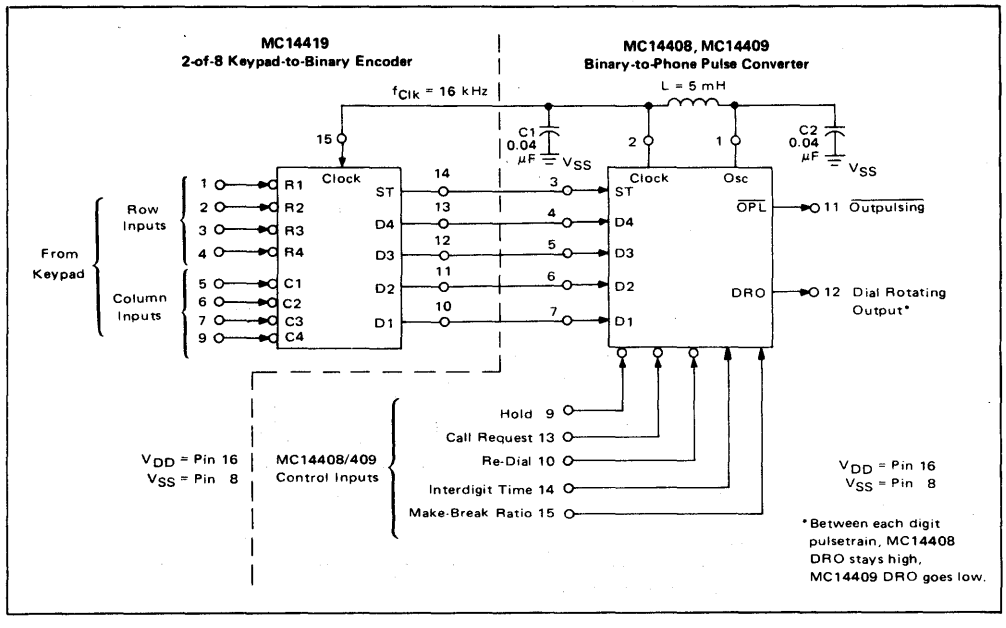


FIGURE 5 – PHONE DIALER SYSTEM



MOTOROLA

MC34010A
MC34011A

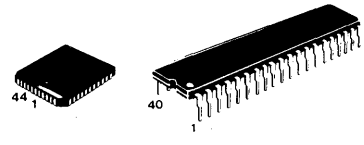
Advance Information

ELECTRONIC TELEPHONE CIRCUIT

- Provides All Basic Telephone Station Apparatus Functions in a Single IC, Including DTMF Dialer, Tone Ringer, Speech Network and Line Voltage Regulator
- DTMF Generator Uses Low-Cost Ceramic Resonator with Accurate Frequency Synthesis Technique
- Tone Ringer Drives Piezoelectric Transducer and Satisfies EIA RS-470 Impedance Signature Requirements
- Speech Network Provides Two–Four Wire Conversion with Adjustable Sidetone Utilizing an Electret Transmitter
- On-Chip Regulator Insures Stable Operation Over Wide Range of Loop Lengths
- I^2L Technology Provides Low 1.4 Volt Operation and High Static Discharge Immunity
- MC34010A Provides Microprocessor Interface Port for Automatic Dialing Features

ELECTRONIC TELEPHONE CIRCUIT

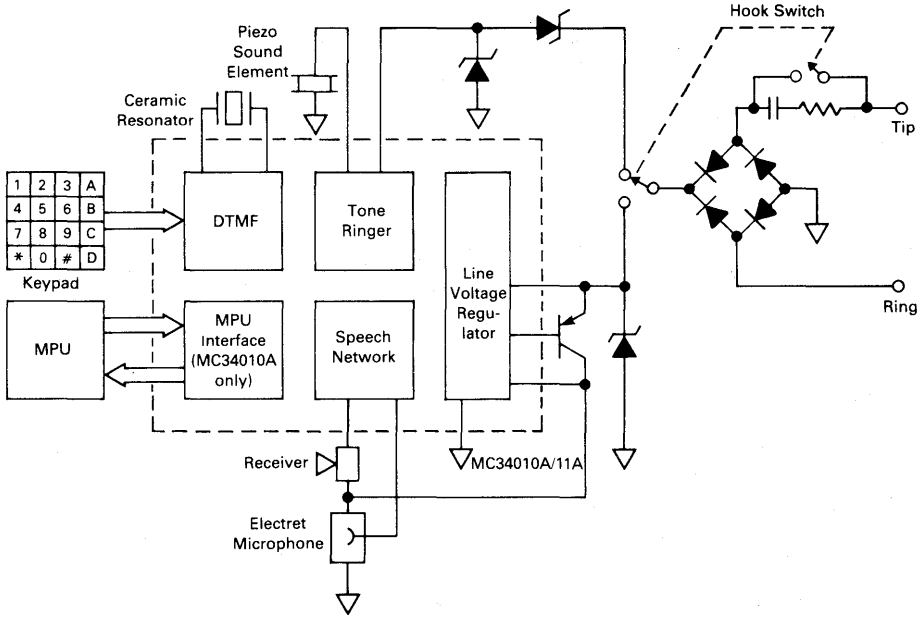
BIPOLAR LINEAR/I^2L



44-PIN PLCC CASE 777-01

P SUFFIX PLASTIC PACKAGE CASE 711-03

FIGURE 1 — ELEMENTS OF THE MC34010A/11A ELECTRONIC TELEPHONE

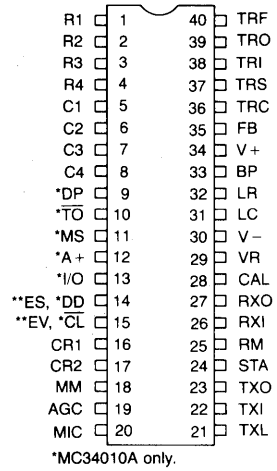


This document contains information on a new product. Specifications and information herein are subject to change without notice.

MAXIMUM RATINGS (Voltage References to V−)

Parameter	Value	Unit
V+ Terminal Voltage (Pin 34)	+18, −1.0	V
VR Terminal Voltage (Pin 29)	+2.0, −1.0	V
RXO Terminal Voltage (Pin 27)	+2.0, −1.0	V
TRS Terminal Voltage (Pin 37)	+35, −1.0	V
TRO (With Tone Ringer Inactive) Terminal Voltage	+2.0, −1.0	V
R1–R4 Terminal Current (Pins 1–4) C1–C4 (Pins 5–8)	±100	mA
$\overline{CL}$, $\overline{TO}$, DD, I/O, A+ (MC34010A only)	+12, −1.0	V
Operating Ambient Temperature Range	−20 to +60	°C
Storage Temperature Range	−65 to +150	°C

PIN CONNECTIONS



*MC34010A only.
**MC34011A only.

GENERAL CIRCUIT DESCRIPTION

Introduction

The MC34010A/11A Electronic Telephone Circuits (ETC) provide all the necessary elements of a tone dialing telephone in a single IC. The functional blocks of the ETC include the DTMF dialer, speech network, tone ringer, and dc line interface circuit (Figure 1). The MC34010A also provides a microprocessor interface port that facilitates automatic dialing features.

Low voltage operation is a necessity for telephones in networks where parallel telephone connections are common. An electronic speech network operating in parallel with a conventional telephone may receive line voltages below 2.5 volts. DTMF dialers operate at similarly low-line voltages when signaling through battery powered station carrier equipment. These low voltage requirements have been addressed by realizing the MC34010A/11A in a bipolar/I^2L technology with appropriate circuit techniques. The resulting speech and dialer circuits maintain specified performance with instantaneous input voltage as low as 1.4 volts.

Line Voltage Regulator

The dc line interface circuit (Figure 3) determines the dc input characteristic of the telephone. At low input voltages (less than 3 volts) the ETC draws only the

FIGURE 3 — DC LINE INTERFACE BLOCK DIAGRAM

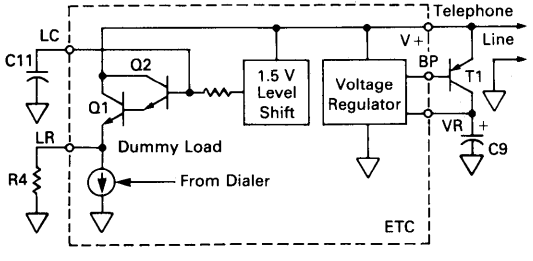
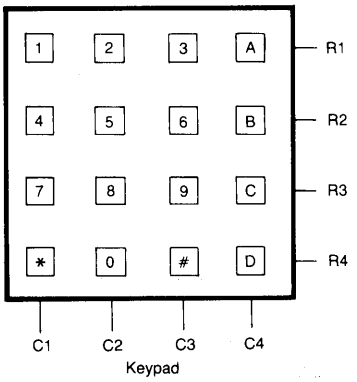


FIGURE 2 — MPU INTERFACE CODES



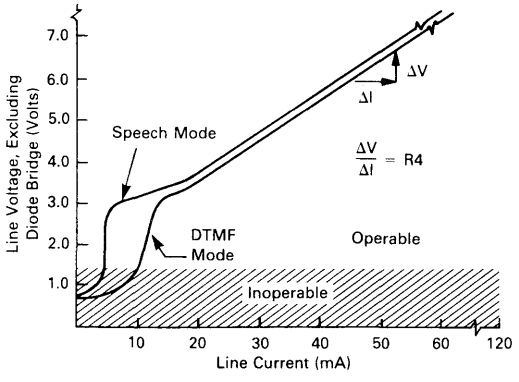
Keypad

Key	Row	Column	Code (B3–B0)
1	1	1	1111
2	1	2	0111
3	1	3	1011
4	2	1	1101
5	2	2	0101
6	2	3	1001
7	3	1	1110
8	3	2	0110
9	3	3	1010
0	4	2	0100
A	1	4	0011
B	2	4	0001
C	3	4	0010
D	4	4	0000
*	4	1	1100
#	4	3	1000

GENERAL CIRCUIT DESCRIPTION (continued)

speech and dialer bias currents through the VR regulator. As input voltage increases, Q1 conducts the excess dc line current through resistor R4. The 1.5 volt level shift prevents saturation of Q2 with telephone line signals up to 2.0 volts peak (+5.2 dBm). A constant current (dummy load) is switched off when the DTMF dialer is activated to reduce line current transients. Figure 4 illustrates the dc voltage/current characteristic of an MC34010A/11A telephone.

FIGURE 4 — DC V-I CHARACTERISTIC OF THE ETC



Speech Network

The speech network (Figure 5) provides the two-to-four wire interface between the telephone line and the instrument's transmitter and receiver. An electret microphone biased from VR drives the transmit amplifier. For very loud talkers, the peak limiter circuit reduces the transmit input level to maintain low distortion. The transmit amplifier output signal is inverted at the STA terminal and driven through an external R-C network to control the receiver sidetone level. The switched ac resistance at the RM terminal reduces receiver signal when dialing and suppresses clicks due to hook or keypad switch transitions. When transmitting, audio signal currents (i_{TXO} and i_{RXO}) flow through the voltage regulator pass transistor (T1) to drive the telephone line. This feature has two consequences: 1) In the transmitting mode the receiver sidetone current i_{RXO} contributes to the total signal on the line along with i_{TXO}; 2) The ac impedance of the telephone is determined by the receiver impedance and the voltage gain from the line to the receiver amplifier output.

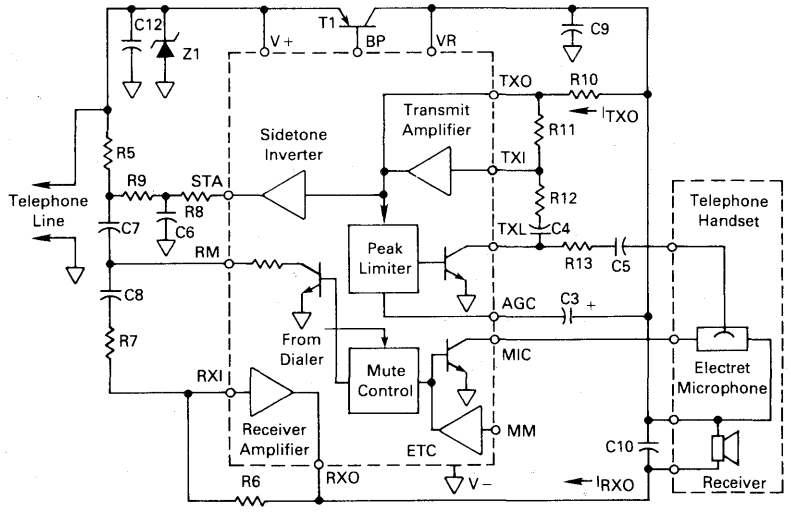
Equalization Circuit (MC34011A Only)

The equalization circuit varies the transmit, receive and sidetone gains with loop current to compensate for losses in long lines. The LR terminal voltage varies directly as the dc loop current. The equalization circuit senses this voltage and switches in external resistors between V+ and V− and across capacitor C6 (Figure 5) when the loop current exceeds a threshold level. The speech network operates with full transmit, receive and sidetone gains for long loops. On short loops the LR voltage exceeds the threshold and these gains are reduced. The threshold detection circuit has a dc hysteresis to prevent distortion of speech signals when the telephone is operated at the threshold current.

DTMF Dialer

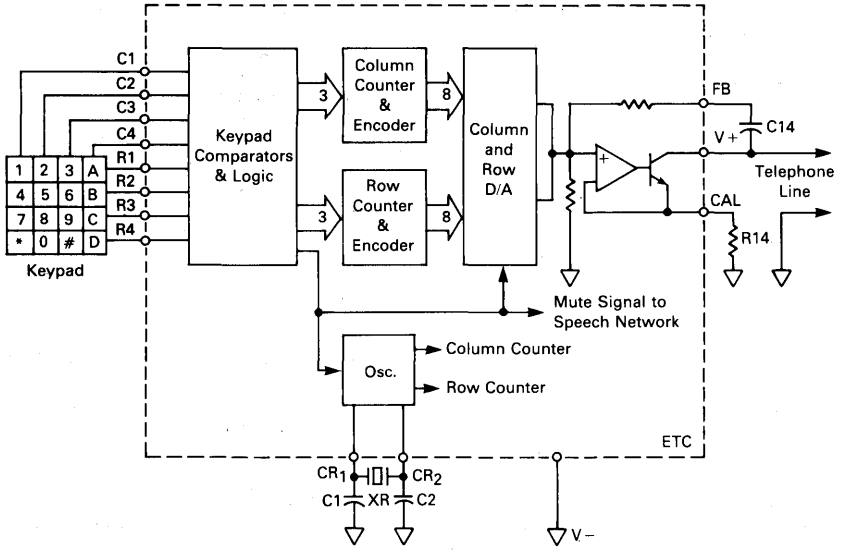
Keypad interface comparators activate the DTMF row and column tone generators (Figure 6) when a row and column input are connected through a SPST keypad. The keypad interface is designed to function with contact resistances up to 1.0 kΩ and leakage resistances as low as 150 kΩ. Single tones may be initiated by depressing two keys in the same row or column.

FIGURE 5 — SPEECH NETWORK BLOCK DIAGRAM



The programmable counters employ a novel design to produce non-integer frequency ratios. The various DTMF tones are synthesized with frequency division errors less than ±0.16% (Table 1). Consequently an inexpensive ceramic resonator can be used instead of a quartz crystal as the DTMF frequency reference. Total frequency error less than ±0.8% can be achieved with ±0.3% ceramic resonator. The row and column D/A converters produce 16-step approximations of sinusoidal waveforms. Feedback through terminal FB reduces the DTMF output impedance to approximately 2.0 kΩ to satisfy return loss specifications.

FIGURE 6 — DTMF DIALER BLOCK DIAGRAM



Tone Ringer

The tone ringer (Figure 7) generates a warbling square wave output drive to a piezo sound element when the ac line voltage exceeds a predetermined threshold level. The threshold detector uses a current mode comparator to prevent on/off chatter when the output current reduces the voltage available at the ringer input. When the average current into the tone ringer exceeds the threshold level, the ringer output TRO commences driving the piezo transducer. This output current sourced from TRI increases the average current measured by the threshold detector. As a result, hysteresis is produced beween the tone ringer on and off thresholds. The output frequency at TRO alternates between $f_O/8$ and $f_O/10$ at a warble rate of $f_O/640$, where f_O is the ringer oscillator frequency.

Microprocessor Interface (MC34010A Only)

The MPU interface connects the keypad and DTMF sections of the ETC to a microprocessor for storing and retrieving numbers to be dialed. Figure 8 shows the major blocks of the MPU interface section and the interconnections between the keypad interface, DTMF generator and microprocessor. Each button of a 12 or 16 number keypad is represented by a four-bit code (Figure 2). This four-bit code is used to load the programmable counters to generate the appropriate row and column tones. The code is transferred serially to or from the microprocessor when the shift register is clocked by the microprocessor. Data is transferred through the I/O terminal, and the direction of data flow is determined by the Data Direction (DD) input terminal. In the manual dialing mode, DD is a Logic "0" and the four-bit code from the keypad is fed to the DTMF generator by the digital multiplexer and also output on the I/O terminal through the four-bit shift register. The data sequence on the I/O terminal is B3, B2, B1, B0 and is transferred on the negative edge of the clock input ($\overline{CL}$). In this mode the shift register load enable circuit cycles the register between the load and read modes such that multiple read cycles may be run for a single-key closure. Six complete clock cycles are required to output data from the ETC and reload the register for a second look.

In the automatic dialing mode, DD is a Logic "1" and the four-bit code is serially entered in the sequence B3, B2, B1, B0 into the four-bit shift register. Thus, only four clock cycles are required to transfer a number into the ETC. The keypad is disabled in this mode. A Logic "1" on the Tone Output ($\overline{TO}$) will disable tone outputs until valid data from the microprocessor is in place. Subsequently $\overline{TO}$ is switched to a Logic "0" to enable the DTMF generator. Figures 9 and 10 show the timing waveforms for the manual and automatic dialing modes and Table 2 specifies timing limitations.

The keypad decoder's exclusive OR circuit generates the DP and MS output signals. The DP output indicates (when at a Logic "1") that one, and only one, key is

depressed, thereby indicating valid data is available to the MPU. The DP output can additionally be used to initiate a data transfer sequence to the microprocessor. The MS output (when at a Logic "1") indicates the DTMF generator is enabled and the speech network is muted.

Pin A+ is to be connected to a source of 2.5 to 10 volts (generally from the microprocessor circuit) to enable the pullup circuits on the microprocessor interface outputs (DP, MS, I/O). Additionally, this voltage will power the entire circuitry (except Tone Ringer) in the absence of voltage at V+. This permits use of the transmit and receive amplifiers, keypad interface, and DTMF generator for non-typical telephone functions.

See Figure 47 for a typical interconnection to an MC6821 PIA (Peripheral Interface Adapter). Connection to a port on any other class of microprocessor will be similar.

FIGURE 7 — TONE RINGER BLOCK DIAGRAM

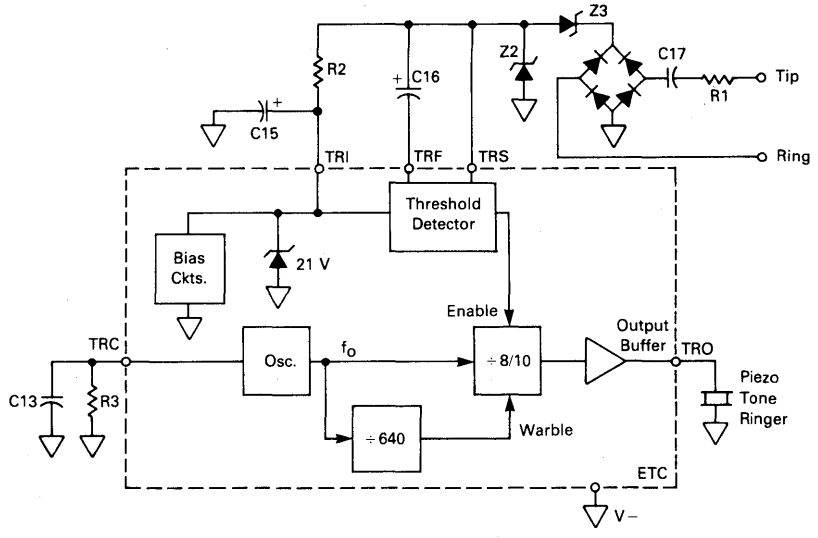
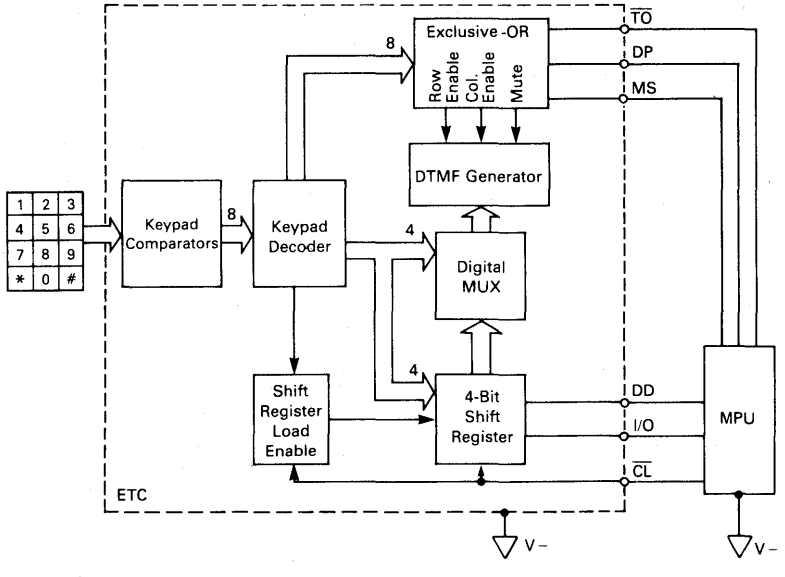


FIGURE 8 — MICROPROCESSOR INTERFACE BLOCK DIAGRAM (MC34010A ONLY)



2

FIGURE 9 — OUTPUT DATA CYCLE FROM MC34010A

NOTE: $\overline{TO}$ may be low (Tone generator enabled) if desired.

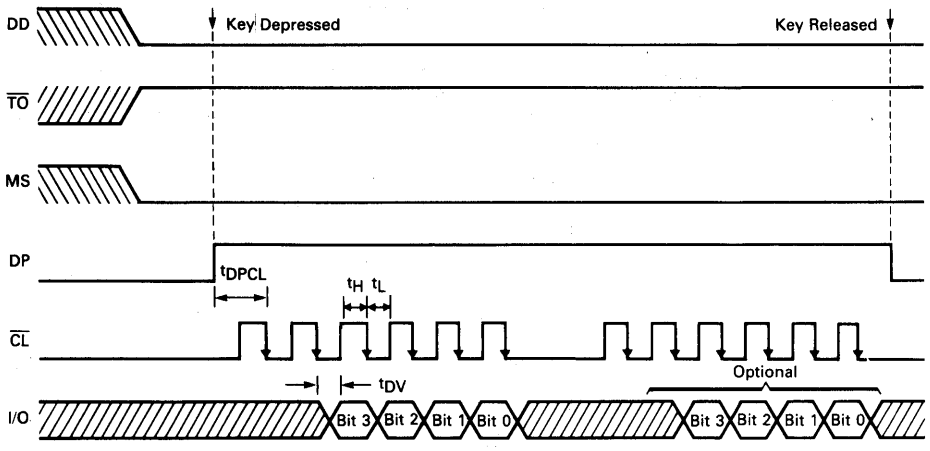


FIGURE 10 — INPUT DATA CYCLE TO MC34010

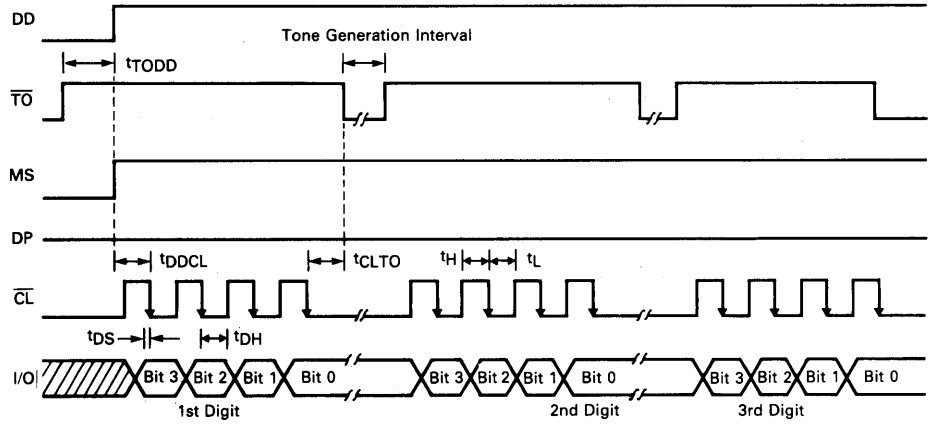


TABLE 1 — FREQUENCY SYNTHESIZER ERRORS

	DTMF Standard (Hz)	Tone Output Frequency with 500 kHz Oscillator	% Deviation from Standard
Row 1	697	696.4	−0.086
Row 2	770	769.2	−0.104
Row 3	852	853.2	+0.141
Row 4	941	939.8	−0.128
Column 1	1209	1207.7	−0.108
Column 2	1336	1336.9	+0.067
Column 3	1477	1479.3	+0.156
Column 4	1633	1634.0	+0.061

TABLE 2 — TIMING LIMITATIONS

Symbol	Parameter	Min	Typ	Max	Unit	Ref
f_{CL}	Clock Frequency	0	20	30	kHz	
t_H	Clock High Time	15	—	—	μs	Figs. 9,10
t_L	Clock Low Time	15	—	—	μs	Figs. 9,10
t_r,t_f	Clock Rise, Fall Time	—	—	2.0	μs	
t_{DV}	Clock Transition to Data Valid	—	—	10	μs	Fig. 9
t_{DPCL}	Time from DP High to $\overline{CL}$ Low	20	—	—	μs	Fig. 9
t_{DDCL}	Time from DD High to $\overline{CL}$ Low	20	—	—	μs	Fig. 10
t_{DS}	Data Setup Time	10	—	—	μs	Fig. 10
t_{DH}	Data Hold Time	10	—	—	μs	Fig. 10
t_{CLTO}	Time from $\overline{CL}$ Low to $\overline{TO}$ Low	10	—	—	μs	Fig. 10
t_{TODD}	Time from $\overline{TO}$ High to DD High	20	—	—	μs	Fig. 10

PIN DESCRIPTION

(See Figures 47 & 48 for external component identifications.)

PIN (PLCC)	PIN (DIP)	Designation	Function
1–4	1–4	R1–R4	Keypad inputs for Rows 1 through 4. When open, internal 8.0 kΩ resistors pull up the row inputs to a regulated (≈1.1 volt) supply. In normal operation, a row and a column input are connected through a SPST switch by the telephone keypad. Row inputs can also be activated by a Logic "0" (<500 mV) from a microprocessor port.
7–10	5–8	C1–C4	Keypad inputs for Columns 1 through 4. When open, internal 8.0 kΩ resistors pull down the column inputs to V−. In normal operation, connecting any column input to any row input produces the respective row and column DTMF tones. In addition to being connected to a row input, column inputs can be activated by a Logic "1" (>600 mV and <3.0 volt).
11	9	DP*	Depressed Pushbutton (Output) — Normally low; A Logic "1" indicates one and only one, button of the DTMF keypad is depressed.
12	10	$\overline{TO}$*	$\overline{\text{Tone Output}}$ (Input) — When a Logic "1," disables the DTMF generator. Keypad is not disabled.
13	11	MS*	Mute/Single Tone (Output) — A Logic "1" indicates a row and/or column tone is being generated. A Logic "0" indicates tone generator is disabled.
14	12	A+*	MPU Power Supply (Input) — Enables pullups on the microprocessor section outputs. Additionally, this voltage will power the entire circuit (except Tone Ringer) in the absence of voltage at V+.
15	13	I/O*	Input/Output — Serial Input or Output data (determined by DD input) to or from the microprocessor for storing or retrieving telephone numbers. Guaranteed to be a Logic "1" on powerup if DD = Logic "0."
16	14	DD*	Data Direction (Input) — Determines direction of data flow through I/O pin. As a Logic "1," I/O is an input to the DTMF generator. As a Logic "0," I/O outputs keypad entries to the microprocessor.
		ES**	Sidetone Equalization terminal connects an external resistor between the junction of R8, R9 and V−. At loop currents greater than the equalization threshold this resistor is switched in to reduce the sidetone level.
17	15	$\overline{CL}$*	$\overline{\text{Clock}}$ (Input) — Serially shifts data in or out of I/O pin. Data is transferred on negative edge typically at 20 kHz.
		EV**	Voice Equalization terminal connects an external resistor between V+ and V−, for loop length equalization. At loop currents greater than the equalization threshold this resistor is switched in by the equalization circuit to reduce the transmit and receive gains.
18,19	16,17	CR1, CR2	Ceramic Resonator oscillator input and feedback terminals, respectively. The DTMF dialer is intended to operate with a 500 kHz ceramic resonator from which row and column tones are synthesized.
20	18	MM	Microphone Mute. The MM pin provides a means to mute the microphone and transmit amplifier in response to a digital control signal. When this pin is connected to a Logic "1" (>2.0 V) the microphone dc return path and the transmit amplifier output are disabled.
21	19	AGC	Automatic Gain Control low-pass filter terminal. Capacitor C3 connected between AGC and VR sets the attack and decay time of the transmit limiter circuit. This capacitor also aids in reducing clicks in the receiver due to hook-switch transients and DTMF on/off transients. In conjunction with internal resistors, C3 (1.0 μF) forms a timer which mutes the receiver amplifier for approximately 20 milliseconds after the user goes off-hook or releases a DTMF Key.
22	20	MIC	Microphone negative supply terminal. The dc current from the electret microphone is returned to V− through the MIC terminal which is connected to the collector of an on-chip NPN transistor. The base of this transistor is controlled either internally by the mute signal from the DTMF generator, or externally by the logic input pin MM.
24	21	TXL	Transmit Input Limiter. An internal variable resistance element at the TXL terminal controls the transmitter input level to prevent clipping with high signal levels. Coupling capacitors C4 and C5 prevent dc current flow through TXL. The dynamic range of the transmit peak limiter is controlled by resistors R12 and R13.
25	22	TXI	Transmit amplifier Input. TXI is the input to the transmit amplifier from an electret microphone. AC coupling capacitors allow the dc offset at TXI to be maintained approximately 0.6 V above V− by feedback through resistor R11 from TXO.
26	23	TXO	Transmit Amplifier Output. The transmit amplifier output drives ac current through the voltage regulator pass-transistor T1 via resistor R10. The dc bias voltage at TXO is typically 0.6 volts above V−. The transmit amplifier gain is controlled by the R11/(R12 + R13) ratio.

**MC34011A only.
*MC34010A only.

(continued)

PIN DESCRIPTION (continued)

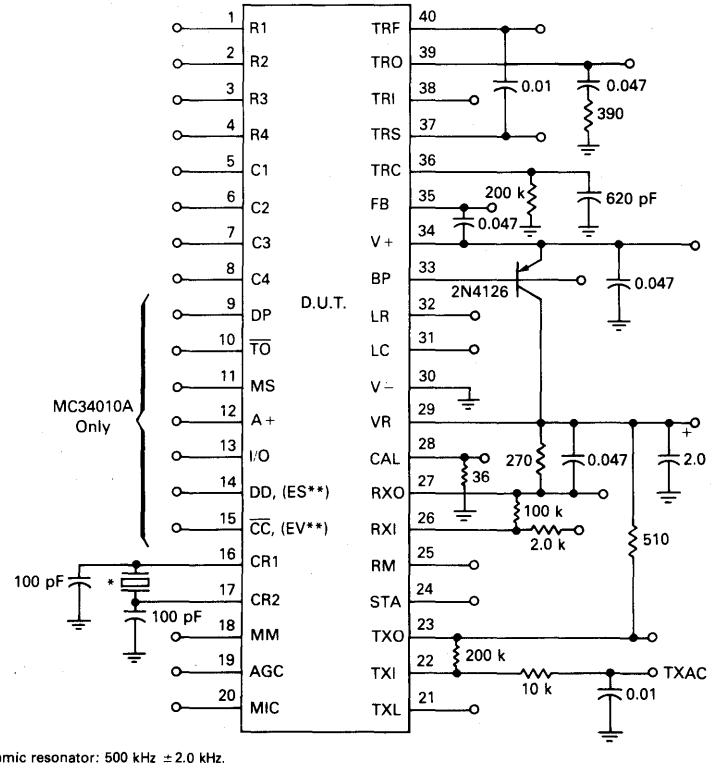
PIN (PLCC)	PIN (DIP)	Designation	Function
27	24	STA	SideTone Amplifier output. STA is the output of the sidetone inverter amplifier whose input is driven by the transmit signal at TXO. The inverted transmit signal from STA subtracts from the receiver amplifier input current from V+, thus reducing the receiver sidetone level. Since the transmitted signal at V+ is phase shifted with respect to TXO by the reactive impedance of the phone line, the signal from STA must be similarly phase-shifted in order to provide adequate sidetone reduction. This phase relationship between the transmit signal at TXO and the sidetone cancellation signal from STA is controlled by R8, R9, and C6.
28	25	RM	Receiver Amplifier Mute. A switched resistance at the RM terminal attenuates the receiver amplifier input signal produced by DTMF dialing tones at V+. RM also mutes clicks at the receiver which result from keypad or hook switch transitions. The ac resistance at RM is typically 540 Ω in the mute mode and 200 kΩ otherwise. Coupling capacitors C7 and C8 prevent dc current flow through RM.
29	26	RXI	Receiver Amplifier Input. RXI is the input terminal of the receiver amplifier which is driven by ac signals from V+ and STA. Input coupling capacitor C8 allows RXI to be biased approximately 0.6 volts above the V− via feedback resistor R6.
30	27	RXO	Receiver Amplifier Output. This terminal is connected to the open-collector NPN output transistor of the receiver amplifier. DC bias current for the output device is sourced through the receiver from VR. The bias voltage at RXO is typically 0.6 volts above the V−. Capacitor C10 from RXO to VR provides frequency compensation for the receiver amplifier.
31	28	CAL	Amplitude CALibration terminal for DTMF dialer. Resistor R14 from the CAL pin to V− controls the DTMF output signal level at Tip and Ring.
32	29	VR	Voltage Regulator output terminal. VR is the output of a 1.1 volt voltage regulator which supplies power to the speech network amplifiers and DTMF generator during signaling. To improve regulator efficiency at low line current conditions, an external PNP pass-transistor T1 is used in the regulator circuit. Capacitor C9 frequency compensates the VR regulator to prevent oscillation.
33	30	V−	The dc common (more negative input) connected to Tip and Ring through the polarity guard bridge.
34	31	LC	DC Load Capacitor. Capacitor C11 from LC to V− forms a low-pass filter which prevents the resistor at LR from loading ac speech and DTMF signals.
35	32	LR	DC Load Resistor. Resistor R4 from LR to V− determines the dc input resistance at Tip and Ring. This resistor is external not only to enable programming the dc resistance but also to avoid high on-chip power dissipation with short telephone lines. It acts as a shunt load conducting the excess dc line current. At low line voltages (<3.0 volts), no current flows through LR.
36	33	BP	Base of a PNP Pass-transistor. Under long-loop conditions where low line voltages would cause VR to fall below 1.1 volts, BP drives the PNP transistor T1 into saturation, thereby minimizing the voltage drop across the pass transistor. At line voltages which maintain VR above 1.1 volts, BP biases T1 in the linear region thereby regulating the VR voltage. Transistor T1 also couples the ac speech signals from the transmit amplifier to Tip and Ring at V+.
37	34	V+	The more positive input to the regulator, speech, and DTMF sections connected to Tip and Ring through the polarity guard diode bridge.
38	35	FB	FeedBack terminal for DTMF output. Capacitor C14 connected from FB to V+ provides ac feedback to reduce the output impedance to Tip and Ring when tone dialing.
40	36	TRC	Tone Ringer oscillator Capacitor and resistor terminal. The relaxation oscillator frequency f_O is set by resistor R3 and capacitor C13 connected from TRC to V−. Typically, $f_O = (R3C13 + 8.0\ \mu s)^{-1}$.
41	37	TRS	Tone Ringer Input Sense. TRS is the most positive input terminal of the tone ringer and the reference for the threshold detector.
42	38	TRI	Tone Ringer Input terminal. TRI is the positive supply voltage terminal for tone ringer circuitry. Current is supplied to TRI through resistor R2. When the average voltage across R2 exceeds an internal reference voltage (typically 1.6 volts) the tone ringer output is enabled.
43	39	TRO	Tone Ringer Output terminal. The frequency of the square wave output signal at TRO alternates from $f_O/8$ to $f_O/10$ at a warble rate of $f_O/640$. Typical output frequencies are 1000 Hz and 800 Hz with a 12.5 Hz warble rate. TRO sources or sinks up to 20 mA to produce an output voltage swing of 18 volts peak-to-peak across the piezo transducer. Tone ringer volume control can be implemented by a variable resistor in series with the piezo transducer.
44	40	TRF	Tone Ringer Input Filter capacitor terminal. Capacitor C16 connected from TRF to TRS forms a low-pass filter. This filter averages the signal across resistor R2 and presents this dc voltage to the input of the threshold detector. Line voltage transients are rejected if the duration is insufficient to charge C16 to 1.6 volts.

ELECTRICAL CHARACTERISTICS (continued)

TONE RINGER

Characteristic	Test Method	Symbol	Min	Typ	Max	Unit
TRI Terminal Voltage	14	V_{TRI}	20	21.5	23	Vdc
TRS Terminal Input Current V_{TRS} = 24 volts V_{TRS} = 30 volts	 15a 15b	I_{TRS}	 70 0.4	 120 0.8	 170 1.5	 μA mA
TRF Threshold Voltage	16a	V_{TRF}	1.2	1.6	1.9	Vdc
TRF Threshold Hysteresis	16b	ΔV_{TRF}	100	200	400	mVdc
TRF Filter Resistance	17	R_{TRF}	30	50	75	kΩ
High Tone Frequency	18	f_H	920	1000	1080	Hz
Low Tone Frequency	18	f_L	736	800	864	Hz
Warble Frequency	18	f_W	11.5	12.5	13.5	Hz
Tone Ringer Output Voltage	19	$V_{o(p-p)}$	18	20	22	Vp-p

FIGURE 11 — GENERAL TEST CIRCUIT

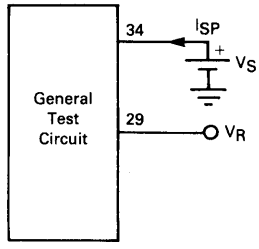


Notes:
1. *Selected ceramic resonator: 500 kHz ±2.0 kHz.
2. Capacitances in μF unless noted.
3. All resistances in ohms.
4. Pin numbers in this Figure and in Test Circuits are for the DIP package.

**MC34011A only.

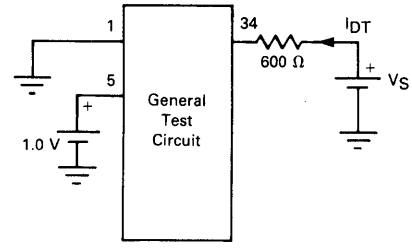
2

FIGURE 12 — TEST ONE



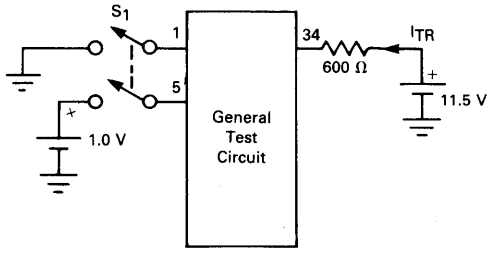
a. Measure V_R with V_S = 1.7 V
b. Measure I_{SP} with V_S = 1.7 V
c. Measure I_{SP} with V_S = 5.0 V

FIGURE 13 — TEST TWO



a. Measure I_{DT} with V_S = 11.5 V.
b. Measure I_{DT} with V_S = 26 V. Calculate $\Delta I_{DT} = |I_{DT}|_{26\ V} - |I_{DT}|_{11.5\ V}$

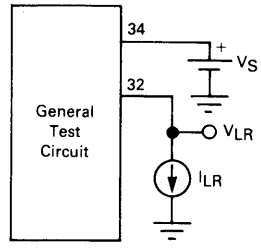
FIGURE 14 — TEST THREE



With S_1 open measure I_{TR}. Close S_1 and again measure I_{TR}. Calculate:

$$\Delta I_{TR} = |I_{TR}|_{S_1\ Closed} - |I_{TR}|_{S_1\ Open}$$

FIGURE 15 — TEST FOUR



a. Set V_S = 5.0 V and I_{LR} = 10 mA. Measure V_{LR}. Calculate $\Delta V_{LR} = V_S - V_{LR}$
b. Repeat Test 4a with V_S = 18 V and I_{LR} = 110 mA

ELECTRICAL CHARACTERISTICS (T_A = 25°C)

KEYPAD INTERFACE CIRCUIT

Characteristic	Test Method	Symbol	Min	Typ	Max	Unit
Row Input Pullup Resistance m^{th} Row Terminal: m = 1,2,3,4	7	R_{Rm}	5.0	8.0	11	kΩ
Column Input Pulldown Resistance n^{th} Column Terminal: n = 1,2,3,4	8	R_{Cn}	5.0	8.0	11	kΩ
Ratio of Row-to-Column Input Resistances $K_{m,n} = \frac{R_{Rm}}{R_{Cn}}$, m = 1,2,3,4 / n = 1,2,3,4	7 & 8	$K_{m,n}$	0.88	1.0	1.12	—
Row Terminal Open Circuit Voltage	7a	V_{ROC}	950	1100	1200	mVdc
Row Threshold Voltage for m^{th} Row Terminal: m = 1,2,3,4	9	V_{Rm}	0.70 V_{ROC}	—	—	Vdc
Column Threshold Voltage for n^{th} Column Terminal: n = 1,2,3,4	10	V_{Cn}	—	—	0.30 V_{ROC}	Vdc

MICROPROCESSOR INTERFACE (MC34010A only)

Voltage Regulator Output A+ Regulator	29	$V_{R/A+}$	0.95	1.1	1.3	V
A+ Input Current Off-Hook	28a	I_A(off)	—	50	150	μA
A+ Input Current On-Hook	28b	I_A(on)	4.0	6.0	9.0	mA
Input Resistance (DD, $\overline{TO}$, $\overline{CL}$)	30	R_{in}	50	100	150	kΩ
Input Current (I/O)	31	I_{in}	—	80	200	μA
Input High Voltage (DD, $\overline{TO}$, $\overline{CL}$, I/O)	—	V_{IH}	2.0	—	A+	V
Input Low Voltage (DD, $\overline{TO}$, $\overline{CL}$, I/O)	—	V_{IL}	—	—	0.8	V
Output High Voltage (MS, DP, I/O)	32	V_{OH}	2.4	4.0	—	V
Output Low Voltage (MS, DP, I/O)	33	V_{OL}	—	0.1	0.4	V

LINE VOLTAGE REGULATOR

Voltage Regulator Output	1a	V_R	1.0	1.1	1.2	Volts
V+ Current in DTMF Mode	2a	I_{DT}	8.0	12	14.5	mA
Change in I_{DT} with Change in V+ Voltage	2b	ΔI_{DT}	—	0.8	2.0	mA
V+ Current in Speech Mode		I_{SP}				mA
V+ = 1.7 V	1b		3.0	5.0	7.0	
V+ = 5.0 V	1c		8.0	11	15	
Speech to DTMF Mode Current Difference	3	ΔI_{TR}	−2.0	2.0	3.5	mA
LR Level Shift		ΔV_{LR}				Vdc
V+ = 5.0 V, I_{LR} = 10 mA	4a		2.4	2.9	3.5	
V+ = 18 V, I_{LR} = 110 mA	4b		2.6	3.3	4.0	
LC Terminal Resistance	5	R_{LC}	30	50	75	kΩ
Load Regulation	6	ΔV_R	−20	−6.0	20	mVdc

ELECTRICAL CHARACTERISTICS (continued)

SPEECH NETWORK

Characteristic	Test Method	Symbol	Min	Typ	Max	Unit
MIC Terminal Saturation Voltage	20	V_{MIC}	—	60	125	mVdc
MIC Terminal Leakage Current	21a	I_{MIC}	—	0.0	5.0	μA
MM Terminal Input Resistance	21b	R_{MM}	50	100	170	kΩ
TXO Terminal Bias	22a	B_{TXO}	0.48	0.53	0.68	—
TXI Terminal Input Bias Current	22b	I_{TXI}	—	50	400	nA
TXO Terminal Positive Swing	22c	$V_{TXO}(+)$	—	25	60	mVdc
TXO Terminal Negative Swing	22d	$V_{TXO}(-)$	—	130	200	mVdc
Transmit Amplifier Closed-Loop Gain	23a	G_{TX}	16.5	19	20	V/V
Sidetone Amplifier Gain	23b	G_{STA}	0.40	0.45	0.54	V/V
STA Terminal Output Current	24	I_{STA}	50	100	250	μA
RXO Terminal Bias	25a	B_{RXO}	0.48	0.52	0.68	—
RXI Terminal Input Bias Current	25b	I_{RXI}	—	100	400	nA
RXO Terminal Positive Swing	25c	$V_{RXO}(+)$	—	1.0	20	mVdc
RXO Terminal Negative Swing	25d	$V_{RXO}(-)$	—	40	100	mVdc
TXL Terminal OFF Resistance	26a	$R_{TXL}(OFF)$	125	200	300	kΩ
TXL Terminal ON Resistance	26b	$R_{TXL}(ON)$	—	20	100	Ω
RM Terminal OFF Resistance	27a	$R_{RM}(OFF)$	125	180	300	kΩ
RM Terminal ON Resistance	27b	$R_{RM}(ON)$	410	570	770	Ω

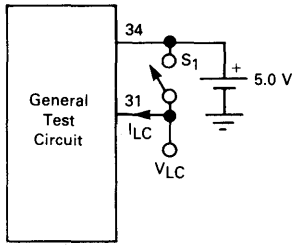
DTMF GENERATOR

Row Tone Frequency	Row 1	11a, 11b	f_{Rm}	692.9	696.4	699.9	Hz
	Row 2			765.3	769.2	773.0	
	Row 3			848.9	853.2	857.5	
	Row 4			935.1	939.8	944.5	
Column Tone Frequency	Column 1	11c, 11d	f_{Cn}	1201.6	1207.7	1213.7	Hz
	Column 2			1330.2	1336.9	1343.6	
	Column 3			1471.9	1479.3	1486.7	
	Column 4			1625.2	1633.4	1641.5	
Row Tone Amplitude		11e	V_{Row}	0.38	0.45	0.55	V_{rms}
Column Tone Amplitude		11f	V_{Col}	0.48	0.55	0.67	V_{rms}
Column Tone Pre-emphasis		11g	dB_{CR}	0.5	1.8	3.0	dB
DTMF Distortion		12	% Dis	—	4.0	6.0	%
DTMF Output Resistance		13	R_o	1.0	2.5	3.0	kΩ

EQUILIZATION CONTROL (MC34011A Only)

ES Terminal OFF Resistance	34a	$R_{ES}(OFF)$	100	200	325	kΩ
Equilization Threshold Voltage	34b	V_E	1.4	1.6	2.0	Vdc
Equilization Threshold Hysteresis	34c	ΔV_E	75	200	300	mVdc
EV Terminal OFF Resistance	35a	$R_{EV}(OFF)$	100	200	325	kΩ
EV Terminal ON Resistance	35b	$R_{EV}(ON)$	—	20	50	Ω

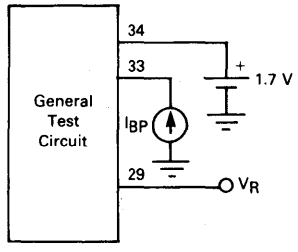
FIGURE 16 — TEST FIVE



With S_1 open measure V_{LC}.
Close S_1 and measure I_{LC}.
Calculate:

$$R_{LC} = \frac{5.0 - V_{LC}}{I_{LC}}$$

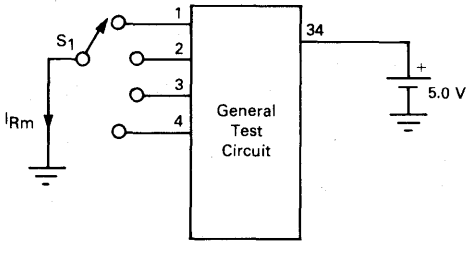
FIGURE 17 — TEST SIX



Set I_{BP} = 0.0 μA and measure V_R.
Set I_{BP} = 150 μA and measure V_R. Calculate:

$$\Delta V_R = V_R\Big|_{0.0\ \mu A} - V_R\Big|_{150\ \mu A}$$

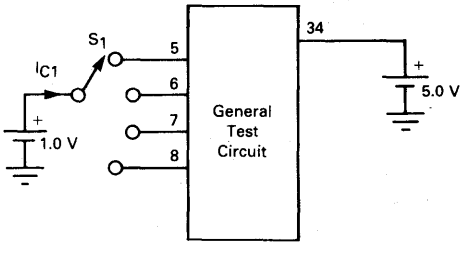
FIGURE 18 — TEST SEVEN



Subscript m corresponds to row number.

a. Set S_1 to Terminal 2 and measure voltage at Terminal 1 (V_{ROC}).
b. Set S_1 to Terminal 1 (m = 1) and measure I_{R1}. Calculate:
$R_{R1} = V_{ROC} \div I_{R1}$
c,d,e. Repeat Test 7b for m = 2,3,4.

FIGURE 19 — TEST EIGHT

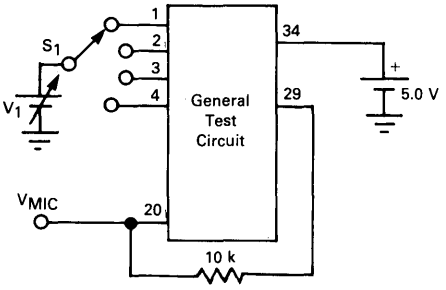


Subscript n corresponds to column number.

a. Set S_1 to Terminal 5 (n = 1) and measure I_{C1}. Calculate:
$R_{C1} = 1.0\ V \div I_{C1}$
b,c,d. Repeat Test 8a for n = 2,3,4.

2

FIGURE 20 — TEST NINE

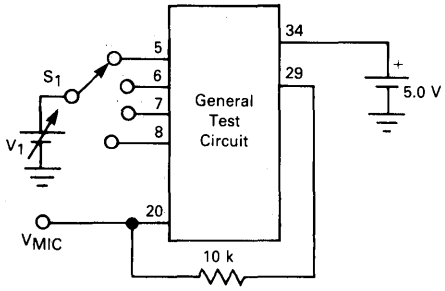


m corresponds to row number.

a. Set S_1 to Terminal 1 (m = 1) with V_1 = 1.0 Vdc. Verify V_{MIC} is Low (V_{MIC} < 0.3 Vdc). Decrease V_1 to 0.70 V_{ROC} and verify V_{MIC} switches high. (V_{MIC} > 0.5 Vdc). V_{ROC} is obtained from Test 7a.

b,c,d. Repeat Test 9a for rows 2,3, and 4. (m = 2,3,4)

FIGURE 21 — TEST TEN

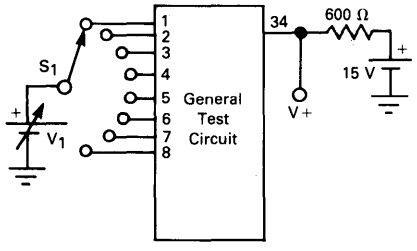


n corresponds to column number.

a. Set S_1 to Terminal 5 (n = 1) with V_1 = 0 Vdc. Verify V_{MIC} is low (V_{MIC} < 0.3 Vdc). Increase V_1 to 0.30 V_{ROC} and verify V_{MIC} switches high, (V_{MIC} > 0.5 Vdc). V_{ROC} is obtained from Test 7a.

b,c,d. Repeat Test 10a for columns 2,3, and 4. (n = 2,3,4)

FIGURE 22 — TEST ELEVEN



m corresponds to row number.
n corresponds to column number.

a. With V_1 = 0.0 V set S_1 to Terminal 1 (m = 1) and measure frequency of tone at V+.

b. Repeat Test 11a for rows 2,3 and 4. (m = 2,3,4).

c. With V_1 = 1.0 V set S_1 to Terminal 5. (n = 1) and measure frequency of tone at V+.

d. Repeat Test for columns 2,3, and 4. (n = 2,3,4).

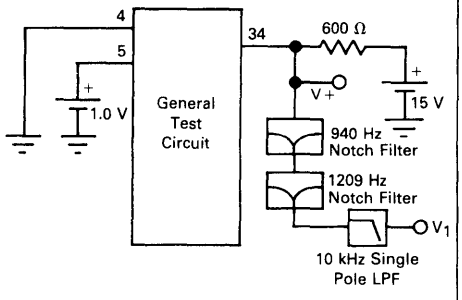
e. Set S_1 to Terminal 4 and V_1 = 0.0 V. Measure row tone amplitude at V+ (V_{ROW}).

f. Set S_1 to Terminal 8 and V_1 = 1.0 V. Measure column tone amplitude at V+. (V_{COL}).

g. Using results of Tests 11e and 11f, calculate:

$$dB_{CR} = 20 \log_{10} \frac{V_{COL}}{V_{ROW}}$$

FIGURE 23 — TEST TWELVE

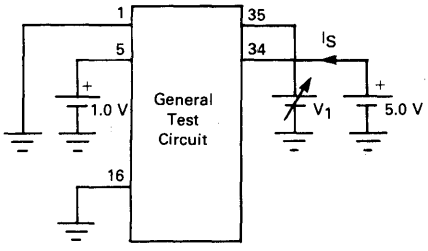


Note: The notch filters must have 50 dB attenuation at their respective center frequencies.

Measure V+ and V_1 with a true rms voltmeter. Calculate:

$$\% \text{ DIS} = \frac{V_1(\text{rms})}{V+(\text{rms})} \times 100$$

FIGURE 24 — TEST THIRTEEN

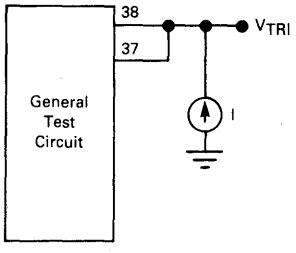


Measure I_S at V_1 = 1.8 V and V_1 = 2.8 V.

Calculate:

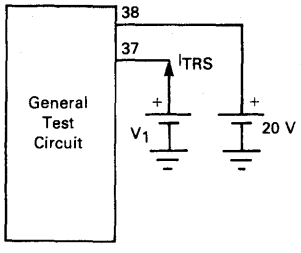
$$R_O = 1.0\ V \div \left[|I_S|_{2.8\ V} - |I_S|_{1.8\ V} \right]$$

FIGURE 25 — TEST FOURTEEN



Set I = 1.0 mA and measure V_{TRI}.

FIGURE 26 — TEST FIFTEEN

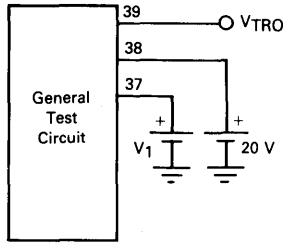


a. Measure I_{TRS} with V_1 = 24 V.

b. Measure I_{TRS} with V_1 = 30 V.

2

FIGURE 27 — TEST SIXTEEN



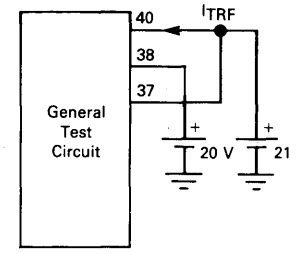
a. Increase V_1 from 21 V until V_{TRO} switches on. Note that V_{TRO} will be an 16 V_{pp} square wave. Record this value of V_1. Calculate:

$V_{TRF} = V_1 - 20\ V$

b. Decrease V_1 from its setting in Test 16a until V_{TRO} ceases switching. Record this value of V_1. Calculate:

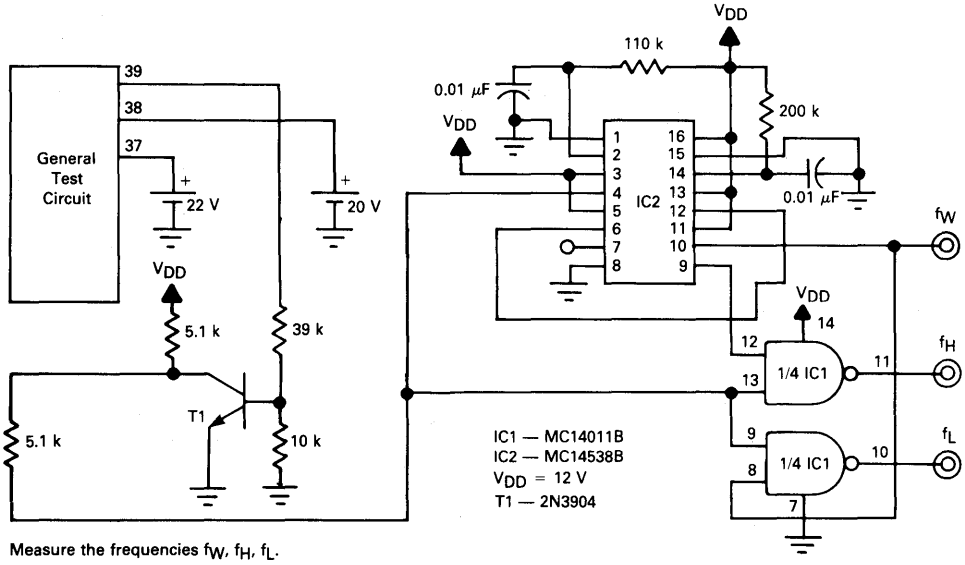
$$\Delta V_{TRF} = V_{1\,\text{Test 16a}} - V_{1\,\text{Test 16b}}$$

FIGURE 28 — TEST SEVENTEEN



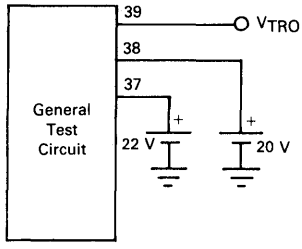
Measure I_{TRF}. Calculate: $R_{TRF} = 1.0 \div I_{TRF}$.

FIGURE 29 — TEST EIGHTEEN



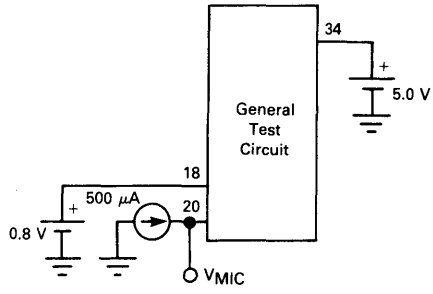
Measure the frequencies f_W, f_H, f_L.

FIGURE 30 — TEST NINETEEN



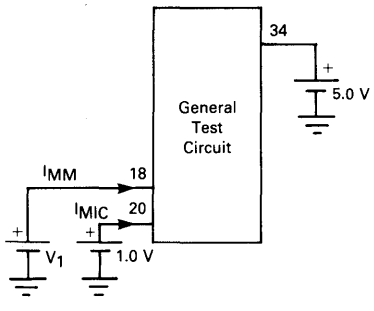
Measure V_{TRO} peak-to-peak voltage swing.
Using V_{TRI} from Test 14 Calculate:
$V_{o(p-p)} = V_{TRI} - 20\ V + V_{TRO}$

FIGURE 31 — TEST TWENTY



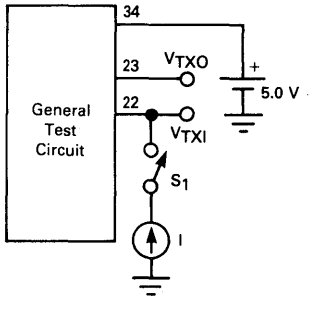
Measure V_{MIC}

FIGURE 32 — TEST TWENTY-ONE



a. Set V_1 = 2.0 V and measure I_{MIC}.
b. Set V_1 = 5.0 V and measure I_{MM}.
Calculate: $R_{MM} = 5.0\ V \div I_{MM}$

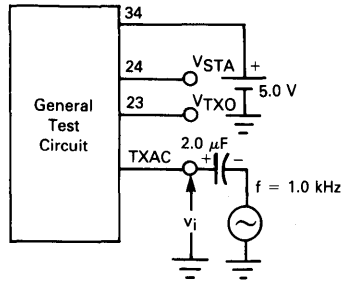
FIGURE 33 — TEST TWENTY-TWO



a. With S_1 open, measure V_{TXO}. Using V_R obtained in Test 1 Calculate: $B_{TXO} = V_{TXO} \div V_R$
b. With S_1 open, measure V_{TXO} and V_{TXI}. Calculate: $I_{TXI} = (V_{TXO} - V_{TXI}) \div 200\ k\Omega$
c. Close S_1 and set I = −10 μA. Measure V_{TXO}. Calculate: $V_{TXO}(+) = V_R - V_{TXO}$ where V_R is obtained from Test 1.
d. Close S_1 and set I = +10 μA. Measure V_{TXO}. $V_{TXO}(-) = V_{TXO}$.

2

FIGURE 34 — TEST TWENTY-THREE



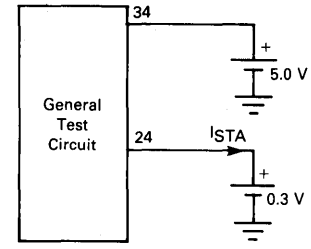
a. Set the generator for v_i = 3.0 mV_{rms}. Measure ac voltage V_{TXO}. Calculate:

$$G_{TX} = \frac{V_{TXO}}{v_i}$$

b. Measure ac voltage V_{STA}. Using V_{TXO} from Test 23a calculate:

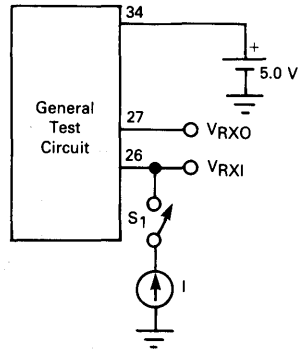
$$G_{STA} = \frac{V_{STA}}{V_{TXO}}$$

FIGURE 35 — TEST TWENTY-FOUR



Measure I_{STA}.

FIGURE 36 — TEST TWENTY-FIVE



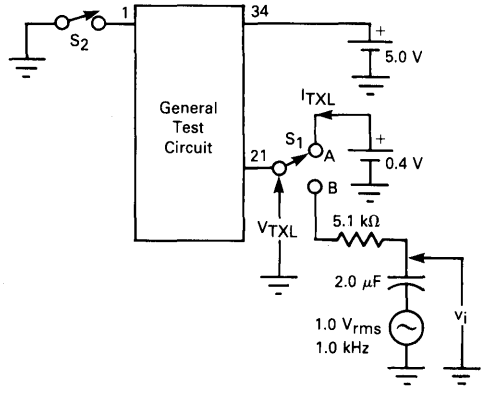
a. With S_1 open, measure V_{RXO}. Using V_R obtained in Test 1, calculate: $B_{RXO} = V_{RXO} \div V_R$.

b. With S_1 open, measure V_{RXO} and V_{RXI}. Calculate: $I_{RXI} = (V_{RXO} - V_{RX1}) \div 100\ k\Omega$

c. Close S_1 and set I = −10 μA. Measure V_{RXO}. Using V_R obtained in Test 1, calculate: $V_{RXO}(+) = V_R - V_{RXO}$.

d. Close S_1 and set I = +10 μA and measure V_{RXO}. $V_{RXO}(-) = V_{RXO}$.

FIGURE 37 — TEST TWENTY-SIX

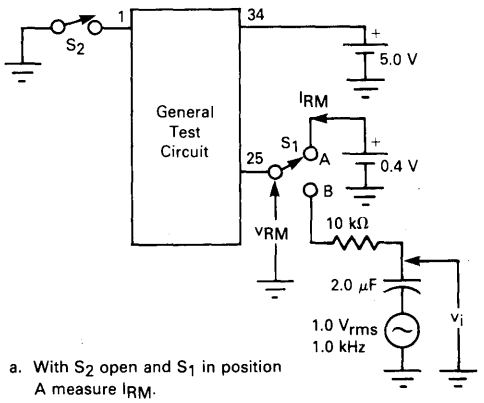


a. Set S_1 to position A with S_2 open. Measure I_{TXL}. Calculate: R_{TXL} (OFF) = 0.4 V ÷ I_{TXL}.

b. Set S_1 to position B and close S_2. Measure ac voltages v_i and V_{TXL}. Calculate:

$$R_{TXL}\ (ON) = \frac{V_{TXL}}{v_i - V_{TXL}} \times 5.1\ k\Omega$$

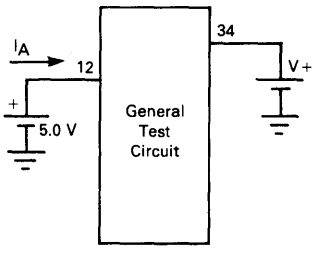
FIGURE 38 — TEST TWENTY-SEVEN



a. With S_2 open and S_1 in position A measure I_{RM}.
Calculate: $R_{RM}(OFF) = 0.4\ V \div I_{RM}$

b. Close S_2 and switch S_1 to position B. Measure ac voltages v_i and V_{RM}.
Calculate:
$$R_{RM}(ON) = \frac{V_{RM}}{v_i - V_{RM}} \times 10\ k\Omega$$

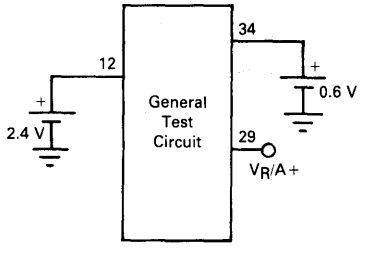
FIGURE 39 — TEST TWENTY-EIGHT



a. Set V+ = 1.4 V. Measure $I_A(OFF)$

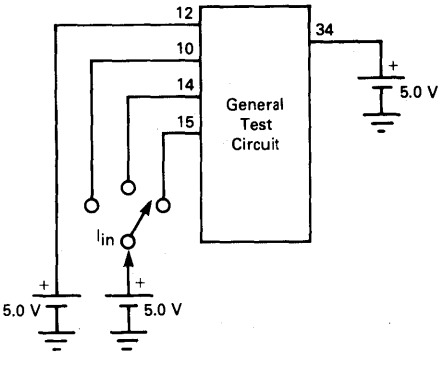
b. Set V+ = 0.6 V. Measure $I_A(ON)$

FIGURE 40 — TEST TWENTY-NINE



Measure $V_R/A+$

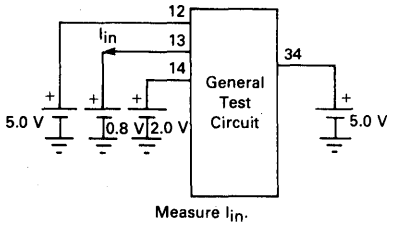
FIGURE 41 — TEST THIRTY



Measure I_{in} at each of three inputs. For each, calculate:
$R_{in} = 5.0\ V/I_{in}$

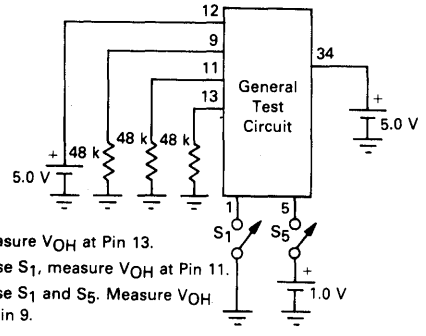
2

FIGURE 42 — TEST THIRTY-ONE



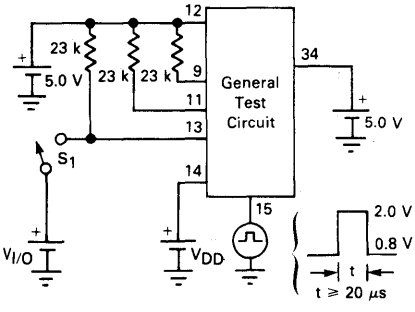
Measure I_{in}.

FIGURE 43 — TEST THIRTY-TWO



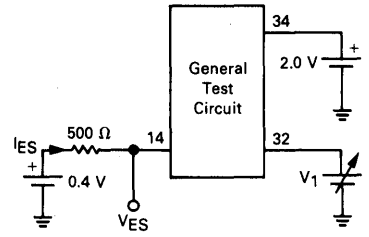
a. Measure V_{OH} at Pin 13.
b. Close S_1, measure V_{OH} at Pin 11.
c. Close S_1 and S_5. Measure V_{OH} at Pin 9.

FIGURE 44 — TEST THIRTY-THREE



a. Set V_{DD} to 0.8 V Measure V_{OL} voltages at Pins 9 and 11.
b. Close S_1. Force $V_{I/O}$ to 0.8 V and V_{DD} to 2.0 V. Apply 4 clock pulses to Pin 15. Open S_1 and decrease V_{DD} to 0.8 V. Measure V_{OL} at Pin 13.

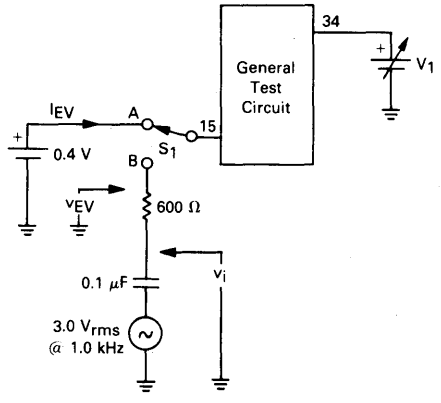
FIGURE 45 — TEST THIRTY-FOUR



a. Set V_1 = 0 V. Measure I_{ES}. Calculate R (OFF) = 0.4 ÷ I_{ES}.
b. Increase V_1 until V_{ES} SWITCHES low (<200 mV). Measure V_1. $V_E = V_1$.
c. Decrease V_1 from the value in Test 34b until V_{ES} switches high (>200 mV). Measure V_1. Calculate $\Delta V_E = V_1 - V_1$

Test 34b — Test 34c

FIGURE 46 — TEST THIRTY-FIVE



a. With S_1 in position A set V_1 = 2.0 V. Measure I_{EV} Calculate R_{EV}(OFF) = 0.4 ÷ I_{EV}.
b. Set V_1 = 5.0 V and Set S_1 to position B. Measure v_i and v_{EV}. Calculate

$$R_{EV}(ON) = \frac{v_{EV}}{v_i - v_{EV}} \times 600\ \Omega$$

APPLICATIONS INFORMATION

Figures 47 & 48 specify typical application circuits for the MC34010A and MC34011A. Complete listings of external components are provided at the end of this section along with nominal component values.

The hook switch and polarity guard bridge configuration is one of several options. If two bridges are used, one for the tone ringer and the other for speech and dialer circuits, then the hook switch can be simplified. Component values should be varied to optimize telephone performance parameters for each application.

The relationships between the application circuit components and certain telephone parameters are briefly described in the following:

On-Hook Input Impedance

R1, C17, and Z3 are the significant components for on-hook impedance. C17 dominates at low frequencies, R1 at high frequencies and Z3 provides the non-linearity required for 2.5 V and 10 V impedance signature tests. C17 must generally be ≤ 1.0 μF to satisfy 5.0 Hz impedance specifications. (EIA RS-470)

Tone Ringer Output Frequencies

R3 and C13 control the frequency (f_O) of a relaxation oscillator. Typically $f_O = (R3C13 + 8.0\ \mu s)^{-1}$. The output tone frequencies are $f_O/10$ and $f_O/8$. The warble rate is $f_O/640$. The tone ringer will operate with f_O from 1.0 kHz to 10 kHz. R3 should be limited to values between 150 k and 300 k.

Tone Ringer Input Threshold

After R1, C17, and Z3 are chosen to satisfy on-hook impedance specifications, R2 is chosen for the desired ring start threshold. Increasing R2 reduces the ac input voltage required to activate the tone ringer output. R2 should be limited to values between 0.8 k and 2.0 kΩ.

Off-Hook DC Resistance

R4 conducts the dc line current in excess of the speech and dialer bias current. Increasing R4 increases the input resistance of the telephone for line currents above 10 mA. R4 should be selected between 30 Ω and 120 Ω.

Off-Hook AC Impedance

The ac input impedance is equal to the receive amplifier load impedance (at RXO) divided by the receive amplifier gain (voltage gain from V+ to RXO). Increasing the impedance of the receiver increases the impedance of the telephone. Increasing the gain of the receiver amplifier decreases the impedance of the telephone.

DTMF Output Amplitude

R14 controls the amplitude of the row and column DTMF tones. Decreasing R14 increases the level of tones generated at V+. The ratio of the row and column tone amplitudes is internally fixed. R14 should be greater than 20 Ω to avoid excessive current in the DTMF output amplifier.

Transmit Output Level

R10 controls the maximum signal amplitude produced at V+ by the transmit amplifier. Decreasing R10 increases the transmit output signal at V+. R10 should be greater than 220 Ω to limit current in the transmit amplifier output.

Transmit Gain

The gain from the microphone to the telephone line varies directly with R11. Increasing R11 increases the signal applied to R10 and the ac current driven through R10 to the telephone line. The closed loop-gain from the microphone to the TXO terminal should be greater than 10 to prevent transmit amplifier oscillations.

Note: Adjustments to transmit level and gain are complicated by the addition of receiver sidetone current to the transmit amplifier output current at V+. Normally the sidetone current from the receiver will increase the transmit signal (if the current in the receiver is in phase with that in R10). Thus the transmit gain and sidetone levels cannot be adjusted independently.

Receiver Gain

Feedback resistor R6 adjusts the gain at the receiver amplifier. Increasing R6 increases the receiver amplifier gain.

Sidetone Level

Sidetone reduction is achieved by the cancellation of receiver amplifier input signals from R9 and R5. R8, R15, and C6 determine the phase of the sidetone balance signal in R9. The ac voltage at the junction of R8 and R9 should be 180° out of phase with the voltage at V+. R9 is selected such that the signal current in R9 is slightly greater than that in R5. This insures that the sidetone current in the receiver adds to the transmit amplifier output current.

Microprocessor Interface (MC34010A Only)

The six microprocessor interface lines (DP, $\overline{TO}$, MS, DD, I/O, and $\overline{CL}$) can be connected directly to a port, as shown in Figure 47. The DP line (Depressed Pushbutton) is also connected to an interrupt line to signal the microprocessor to begin a read data sequence when storing a number into memory. The MC34010A clock speed requirement is slow enough (typically 20 kHz) so that it is not necessary to divide down the processor's system clock, but rather a port output can be toggled. This facilitates synchronizing the clock and data transfer, eliminating the need for hardware to generate the clock.

The DD pin must be maintained at a Logic "0" when the microprocessor section is not in use, so as to permit normal operation of the keypad.

When the microprocessor interface section is not in use, the supply voltage at Pin 12 (A+) may be disconnected to conserve power. Normally the speech circuitry is powered by the voltage supplied at the V+ terminal (Pin 34) from the telephone lines. During this time, A+ powers only the active pullups on the three microprocessor outputs (DP, MS, and I/O). When the telephone is "on-hook," and V+ falls below 0.6 volts, power is then supplied to the telephone speech and dialer circuitry from A+. Powering the circuit from the A+ pin permits communication with a microprocessor, and/or use of the transmit and receiver amplifiers, while the telephone is "on-hook."

Equalization of Speech Network (MC34011A Only)

Resistors R17 and R18 are switched into the circuit when the voltage at the LR terminal exceeds the equalization threshold voltage (typically 1.65 V). R17 reduces the transmit and receive gains for loop currents greater than the threshold (short loops) by attenuating signals at tip and ring. R18 reduces the sidetone level which would otherwise increase when R17 is switched into the circuit. The voltage V_{LR} at LR terminal is given by

$V_{LR} = (I_L - I_S) \times R4.$

where I_L = loop current

I_S = dummy load current (6.0 mA) + speech network current (4.0 mA).

Thus resistor R4 is selected to activate the equalization circuit at the desired loop current. However, R4 must be selected keeping in mind the fact that it also controls the dc resistance of the telephone. Capacitors C18 and C19 prevent dc current flow into the EV and ES terminals. This reduces clicks and also prevents changes in the dc characteristic of the telephone when the EV and ES terminals are switched to low impedance.

FIGURE 47 — MC34010A ELECTRONIC TELEPHONE APPLICATION CIRCUIT

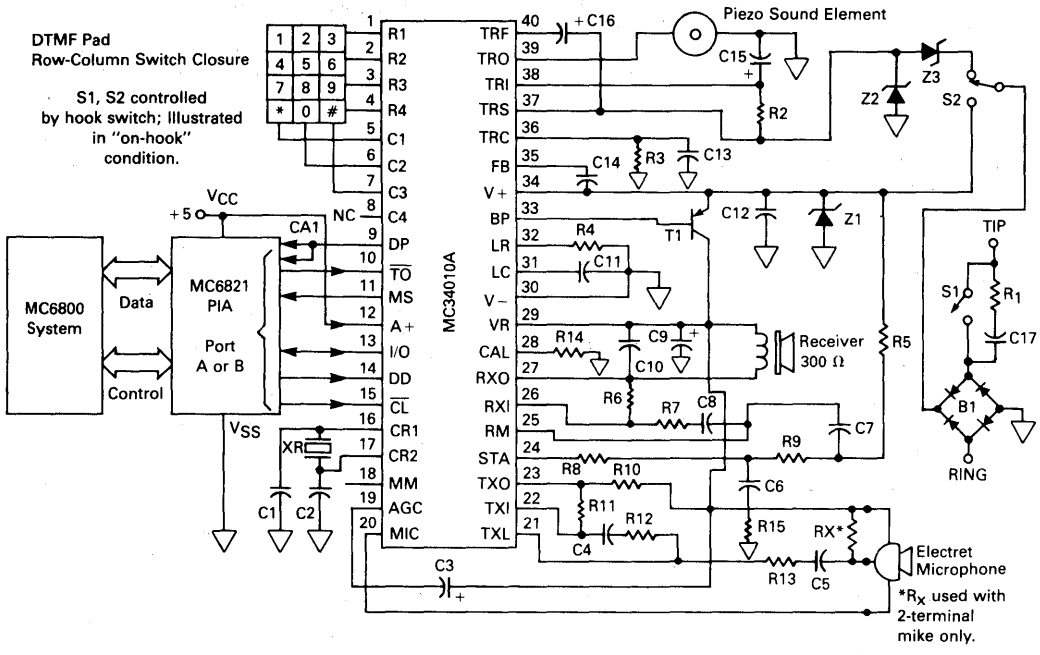
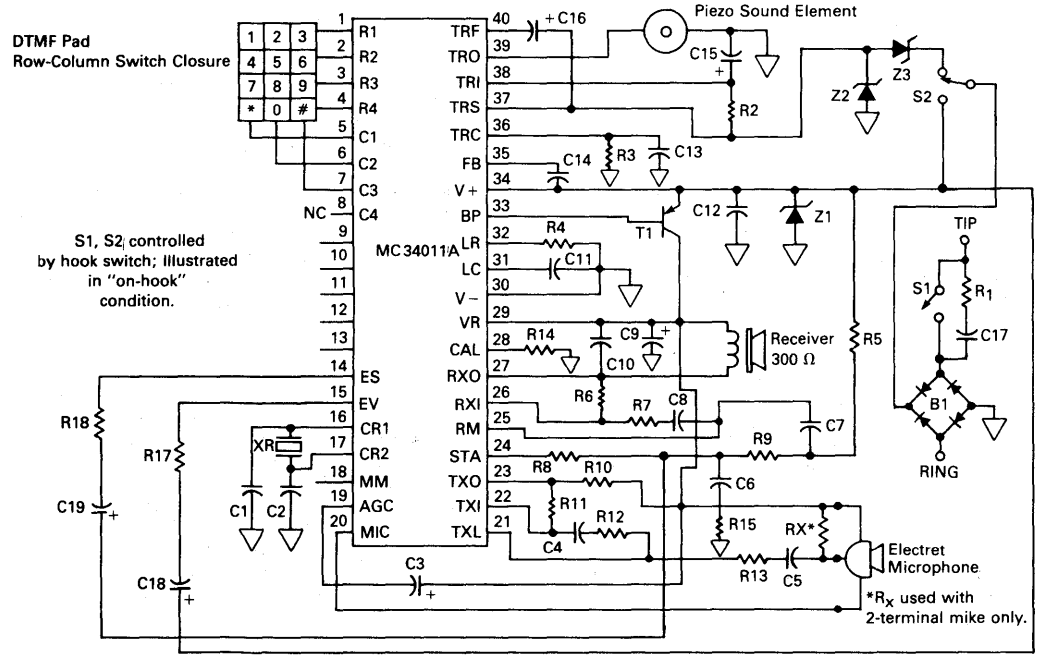


FIGURE 48 — MC34011A ELECTRONIC TELEPHONE APPLICATION CIRCUIT



EXTERNAL COMPONENTS

(Component Labels Referenced to Figures 47 & 48)

Capacitors	Nominal Value	Description
C1, C2	100 pF	Ceramic Resonator oscillator capacitors.
C3	1.0 μF, 3.0 V	Transmit limiter low-pass filter capacitor: controls attack and decay time of transmit peak limiter.
C4, C5	0.1 μF	Transmit amplifier input capacitors: prevent dc current flow into TXL pin and attenuate low-frequency noise on microphone lead.
C6	0.05 μF	Sidetone network capacitor: provides phase-shift in sidetone path to match that caused by telephone line reactance.
C7, C8	0.05 μF	Receiver amplifier input capacitors: prevent dc current flow into RM terminal and attenuates low frequency noise on the telephone line.
C9	2.2 μF, 3.0 V	VR regulator capacitor: frequency compensates the VR regulator to prevent oscillation.
C10	0.01 μF	Receiver amplifier output capacitor: frequency compensates the receiver amplifier to prevent oscillation.
C11	0.1 μF	DC load filter capacitor: prevents the dc load circuit from attenuating ac signals on V+.
C12	0.01 μF	Telephone line bypass capacitor: terminates telephone line for high frequency signals and prevents oscillation in the VR regulator.
C13	620 pF	Tone ringer oscillator capacitor: determines clock frequency for tone and warble frequency synthesizers.
C14	0.1 μF	DTMF output feedback capacitor: ac couples feedback around the DTMF output amplifier which reduces output impedance.
C15	4.7 μF, 25 V	Tone ringer input capacitor: filters the rectified tone ringer input signal to smooth the supply potential for oscillator and output buffer.
C16	1.0 μF, 10 V	Tone ringer filter capacitor: integrates the voltage from current sense resistor R2 at the input of the threshold detector.
C17	1.0 μF, 250 Vac Non-polarized	Tone ringer line capacitor: ac couples the tone ringer to the telephone line; partially controls the on-hook input impedance of telephone.
C18	25 pF, 25 V	Speech equalization coupling capacitor. Prevents dc current flow into SPE terminal. (optional)
C19	5.0 μF, 3.0 V	Sidetone equalization coupling capacitor. Prevents dc current flow into STE terminal. (optional)

Resistors	Nominal Value	Description
R1	6.8 k	Tone ringer input resistor: limits current into the tone ringer from transients on the telephone line and partially controls the on-hook impedance of the telephone.
R2	1.8 k	Tone ringer current sense resistor: produces a voltage at the input of the threshold detector in proportion to the tone ringer input current.
R3	200 k	Tone ringer oscillator resistor: determines the clock frequency for tone and warble frequency synthesizers.
R4	82, 1.0 W	DC load resistor: conducts all dc line current in excess of the current required for speech or dialing circuits; controls the off-hook dc resistance of the telephone.
R5, R7	150 k, 56 k	Receiver amplifier input resistors: couple ac input signals from the telephone line to the receiver amplifier; signal in R5 subtracts from that in R9 to reduce sidetone in receiver.
R6	200 k	Receiver amplifier feedback resistor: controls the gain of the receiver amplifier.
R8, R9	1.5 k, 30 k	Sidetone network resistors: drive receiver amplifier input with the inverted output signal from the transmitter; phase of signal in R9 should be opposite that in R5.
R10	270	Transmit amplifier load resistor: converts output voltage of transmit amplifier into a current that drives the telephone line; controls the maximum transmit level.
R11	200 k	Transmit amplifier feedback resistor: controls the gain of the transmit amplifier.
R12, R13	4.7 k, 4.7 k	Transmit amplifier input resistors: couple signal from microphone to transmit amplifier; control the dynamic range of the transmit peak limiter.
R14	36	DTMF calibration resistor: controls the output amplitude of the DTMF dialer.
R15	2.0 k	Sidetone network resistor (optional): reduces phase shift in sidetone network at high frequencies.
R17	600	Speech equalization resistor. Reduces transmit and receive gain when EV terminal switches on. (optional)
R18	5.1 k	Sidetone equalization resistor. Reduces sidetone level when ES terminal switches on. (optional)
R_X	3.0 k	Microphone bias resistor: sources current from VR to power a 2-terminal electret microphone; R_X is not used with 3-terminal microphones.

EXTERNAL COMPONENTS (continued)

Semiconductors	Electret Mic	Receiver
B1 = MDA101A, or equivalent, or 4-1N4005 T1 = 2N4126 or equivalent Z1 = 18 V, 1.5 W, 1N5931A Z2 = 30 V, 1.5 W, 1N5936A Z3 = 4.7 V, 1/2 W, 1N750 XR — muRata Erie CSB 500 kHz Resonator, or equivalent Piezo — PBL 5030BC Toko Buzzer or equivalent	2 Terminal, Primo EM-95 (Use R_X) or equivalent 3 Terminal, Primo 07A181P (Remove R_X) or equivalent	Primo Model DH-34 (300 Ω) or equivalent

MOTOROLA

MC34012-1
MC34012-2
MC34012-3

Advance Information

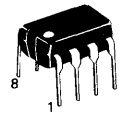
TELEPHONE TONE RINGER

- Complete Telephone Bell Replacement Circuit with Minimum External Components
- On-Chip Diode Bridge and Transient Protection
- Direct Drive for Piezoelectric Transducers
- Base Frequency Options—MC34012-1: 1.0 kHz
  MC34012-2: 2.0 kHz
  MC34012-3: 500 Hz
- Input Impedance Signature Meets Bell and EIA Standards
- Rejects Rotary Dial Transients

TELEPHONE
TONE RINGER

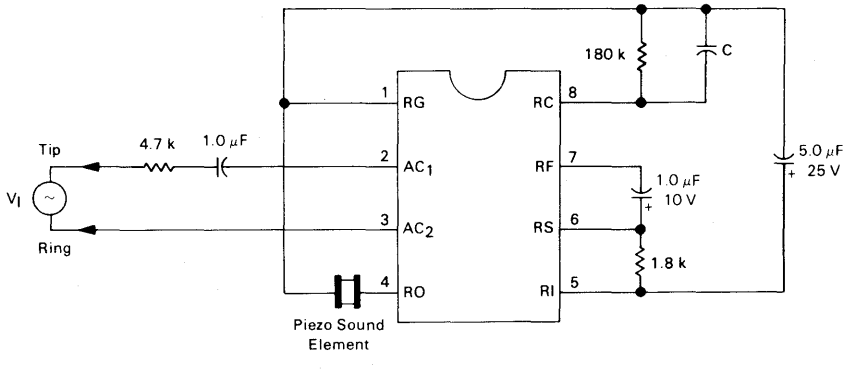
BIPOLAR LINEAR/I^2L

N SUFFIX
PLASTIC PACKAGE
CASE 626-04



D SUFFIX
PLASTIC PACKAGE
CASE 751-01
SO-8

APPLICATION CIRCUIT



MC34012-1: C = 1000 pF
MC34012-2: C = 500 pF
MC34012-3: C = 2000 pF

This document contains information on a new product. Specifications and information herein are subject to change without notice.

CIRCUIT DESCRIPTION

The MC34012 Tone Ringer derives its power supply by rectifying the ac ringing signal. It uses this power to activate a tone generator and drive a piezo-ceramic transducer. The tone generation circuitry includes a relaxation oscillator and frequency dividers which produce high and low frequency tones as well as the tone warble frequency. The relaxation oscillator frequency f_o is set by resistor R2 and capacitor C2 connected to pin RC. The oscillator will operate with f_o from 1.0 kHz to 10 kHz with the proper choice of external components (See Figure 1).

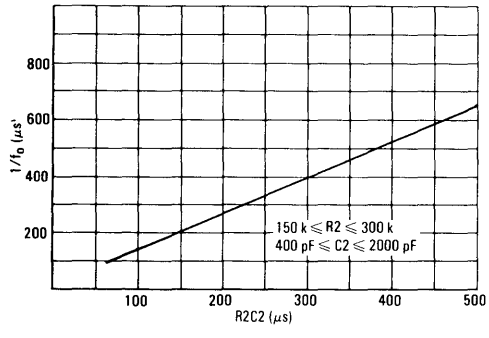
The frequency of the tone ringer output signal at pin RO alternates between $f_o/4$ to $f_o/5$. The warble rate at which the frequency changes is $f_o/320$ for the MC34012-1, $f_o/640$ for the MC34012-2, or $f_o/160$ for the MC34012-3. With a 4.0 kHz oscillator frequency, the MC34012-1 produces 800 Hz and 1000 Hz tones with a 12.5 Hz warble rate. The MC34012-2 generates 1600 Hz and 2000 Hz tones with a similar 12.5 Hz warble frequency from an 8.0 Hz oscillator frequency. The MC34012-3 will produce 400 Hz and 500 Hz tones with a 12.5 Hz warble rate from a 2.0 kHz oscillator frequency. The tone ringer output circuit can source or sink 20 mA with an output voltage swing of 20 volts peak-to-peak. Volume control is readily implemented by adding a variable resistance in series with the piezo transducer.

Input signal detection circuitry activates the tone ringer output when the ac line voltage exceeds programmed threshold level. Resistor R3 determines the ringing signal amplitude at which an output signal will be generated at RO. The ac ringing signal is rectified by the internal diode bridge. The rectified input signal produces a current through R3 which is input at terminal RI. The voltage across resistor R3 is filtered by capacitor C3 at the input to the threshold circuit. When the voltage on capacitor C3 exceeds 1.7 volts, the threshold comparator enables the tone ringer output. Line transients produced by pulse dialing telephones do not charge capacitor C3 sufficiently to activate the tone ringer output.

Capacitors C1 and C4 and resistor R1 determine the 10 volt, 24 Hz signature test impedance. C4 also provides filtering for the output stage power supply to prevent droop in the square wave output signal. Six diodes in series with the rectifying bridge provide the necessary non-linearity for the 2.5 volt, 24 Hz signature tests.

An internal shunt voltage regulator between the RI and RG terminals provides dc voltage to power output stage, oscillator, and frequency dividers. The dc voltage at RI is limited to approximately 22 volts in regulation. To protect the IC from telephone line transients, an SCR is triggered when the regulator current exceeds 50 mA. The SCR diverts current from the shunt regulator and reduces the power dissipation within the IC.

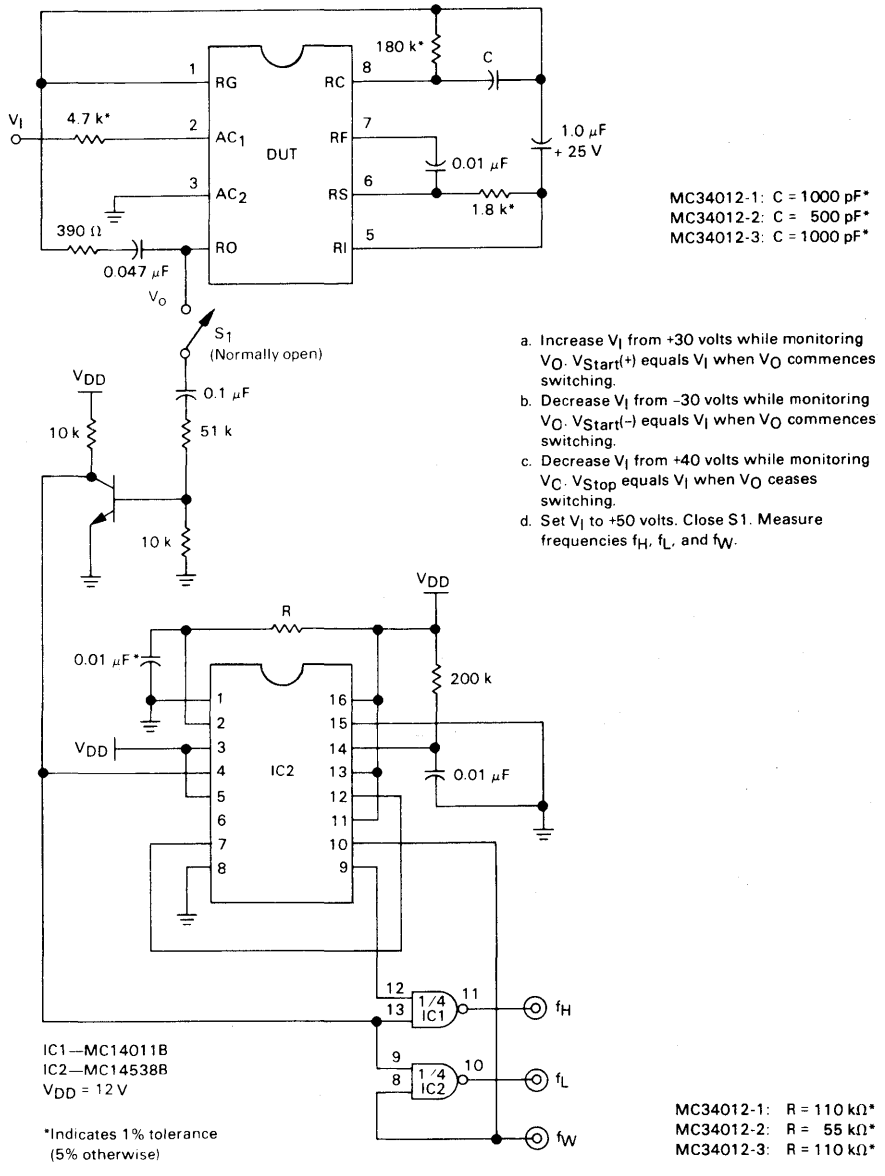
FIGURE 1 — OSCILLATOR PERIOD ($1/f_o$) versus OSCILLATOR R2 C2 PRODUCT



EXTERNAL COMPONENTS

R1	Line input resistor. R1 controls the tone ringer input impedance. It also influences ringing threshold voltage and limits current from line transients. (Range: 2.0 kΩ to 10 kΩ).
C1	Line input capacitor. C1 ac couples the tone ringer to the telephone line and controls ringer input impedance at low frequencies. (Range: 0.4 μF to 2.0 μF).
R2	Oscillator resistor. (Range: 150 kΩ to 300 kΩ).
C2	Oscillator capacitor. (Range: 400 pF to 2000 pF).
R3	Input current sense resistor. R3 controls the ringing threshold voltage. Increasing R3 decreases the ring-start voltage. (Range: 0.8 kΩ to 2.0 kΩ).
C3	Ringing threshold filter capacitor. C3 filters the ac voltage across R3 at the input of the ringing threshold comparator. It also provides dialer transient rejection. (Range: 0.5 μF to 5.0 μF).
C4	Ringer supply capacitor. C4 filters supply voltage for the tone generating circuits. It also provides an ac current path for the 10 V_{rms} ringer signature impedance. (Range: 1.0 μF to 10 μF).

FIGURE 2 — TEST ONE



MC34012-1: C = 1000 pF*
MC34012-2: C = 500 pF*
MC34012-3: C = 1000 pF*

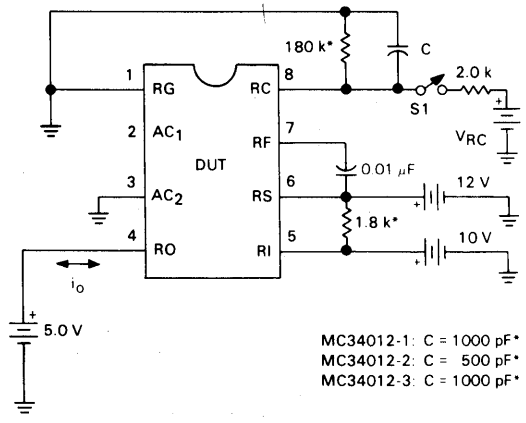
a. Increase V_I from +30 volts while monitoring V_O. $V_{Start}(+)$ equals V_I when V_O commences switching.
b. Decrease V_I from −30 volts while monitoring V_O. $V_{Start}(-)$ equals V_I when V_O commences switching.
c. Decrease V_I from +40 volts while monitoring V_C. V_{Stop} equals V_I when V_O ceases switching.
d. Set V_I to +50 volts. Close S1. Measure frequencies f_H, f_L, and f_W.

IC1—MC14011B
IC2—MC14538B
V_{DD} = 12 V

*Indicates 1% tolerance (5% otherwise)

MC34012-1: R = 110 kΩ*
MC34012-2: R = 55 kΩ*
MC34012-3: R = 110 kΩ*

FIGURE 3 – TEST TWO



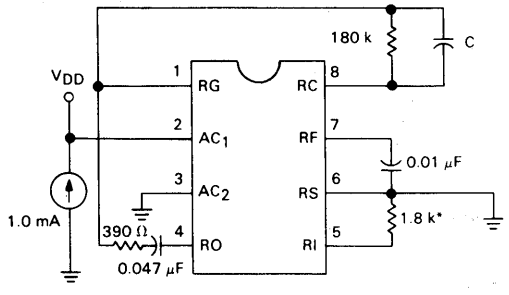
MC34012-1: C = 1000 pF*
MC34012-2: C = 500 pF*
MC34012-3: C = 1000 pF*

With V_{RC} = 3.5 volts, close S1. Measure the current at Pin 4 (I_{O1}). Repeatedly switch V_{RC} between 3.5 volts and 0 volts until Pin 4 current changes polarity. Measure this opposite polarity current (I_{O2}).
Calculate:

$I_O = I_{O1} + I_{O2}$

*Indicates 1% tolerance (5% otherwise)

FIGURE 4 – TEST THREE



MC34012-1: C = 1000 pF*
MC34012-2: C = 500 pF*
MC34012-3: C = 1000 pF*

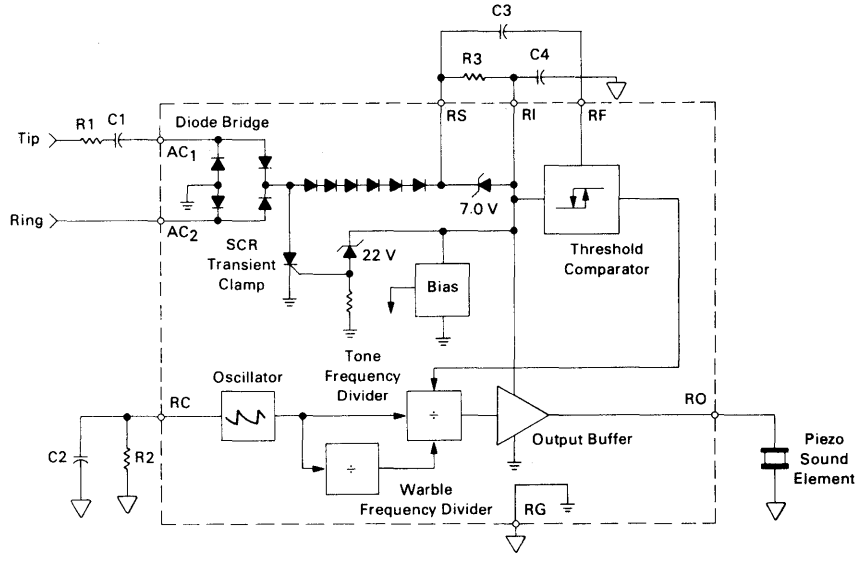
Measure voltage at Pin 2.

*Indicates 1% tolerance (5% otherwise)

ELECTRICAL CHARACTERISTICS (T_A = 25°C)

Characteristic	Test	Symbol	Min	Typ	Max	Units
Ringing Start Voltage ($V_{Start} = V_I$ @ Ring Start)						Vdc
$V_I > 0$	1a	$V_{Start(+)}$	31	34.5	38	
$V_I < 0$	1b	$V_{Start(-)}$	-31	-34.5	-38	
Ringing Stop Voltage ($V_{Stop} = V_I$ @ Ring Stop)	1c	V_{Stop}				Vdc
MC34012-1			16	20	25	
MC34012-2			13	18	22	
MC34012-3			16	20	25	
Output Frequencies (V_I = 50 V)	1d					Hz
MC34012-1 High Tone		f_H	967	1040	1113	
Low Tone		f_L	774	832	890	
Warble Tone		f_W	12	13	14	
MC34012-2 High Tone		f_H	1934	2080	2226	
Low Tone		f_L	1548	1664	1780	
Warble Tone		f_W	12	13	14	
MC34012-3 High Tone		f_H	967	1040	1113	
Low Tone		f_L	774	832	890	
Warble Tone		f_W	24	26	28	
Output Voltage (V_I = 50 V)	6	V_O	19	20	23	V_{p-p}
Output Short-Circuit Current	2	I_O	35	50	80	mA_{p-p}
Input Diode Voltage (I_I = 1.0 mA)	3	V_D	4.6	5.1	5.6	Vdc
Input Voltage—SCR Off (I_I = 30 mA)	4a	V_{off}	37	42	47	Vdc
Input Voltage—SCR On (I_I = 100 mA)	4b	V_{on}	3.2	4.2	6.0	Vdc
Threshold Filter Resistance $R_{RF} = 2.0\ V/I_{RF}$	5	R_{RF}	30	50	80	kΩ

BLOCK DIAGRAM



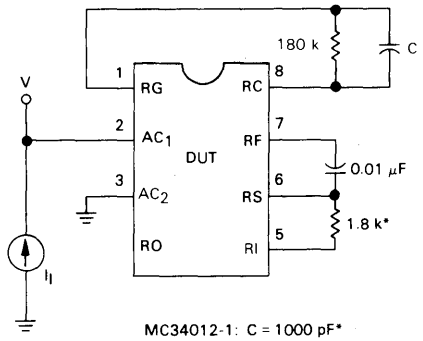
APPLICATION CIRCUIT PERFORMANCE

Characteristic	Typical Value	Units
Output Tone Frequencies MC34012-1 MC34012-2 MC34012-3 Warble Frequency	 832/1040 1664/2080 416/520 13	 Hz
Output Voltage ($V_I \geq 60\ V_{rms}$, 20 Hz)	20	V_{p-p}
Output Duty Cycle	50	%
Ringing Start Input Voltage (20 Hz)	36	V_{rms}
Ringing Stop Input Voltage (20 Hz)	28	V_{rms}
Maximum ac Input Voltage ($\leq$ 68 Hz)	150	V_{rms}
Impedance When Ringing $V_I = 40\ V_{rms}$, 15 Hz $V_I = 130\ V_{rms}$, 23 Hz	 20 10	kΩ
Impedance When Not Ringing $V_I = 10\ V_{rms}$, 24 Hz $V_I = 2.5\ V_{rms}$, 24 Hz $V_I = 10\ V_{rms}$, 5.0 Hz $V_I = 3.0\ V_{rms}$, 200-3200 Hz	 28 >1.0 55 >1.0	 kΩ MΩ kΩ MΩ
Maximum Transient Input Voltage ($T \leq 2.0$ ms)	1500	V

PIN DESCRIPTIONS

Name	Description
AC_1, AC_2	The input terminals to the full-wave diode bridge. The ac ringing signal from the telephone line energizes the ringer through this bridge.
RS	The positive output of diode bridge to which an external current sense resistor is connected.
RI	The positive supply terminal for the oscillator, frequency divider and output buffer circuits.
RF	The terminal for the filter capacitor used in detection of ringing input signals.
RO	The tone ringer output terminal through which the sound element is driven.
RG	The negative output of the diode bridge and the negative supply terminal of the tone generating circuitry.
RC	The oscillator terminal for the external resistor and capacitor which control the tone ringer frequencies.

FIGURE 5 — TEST FOUR

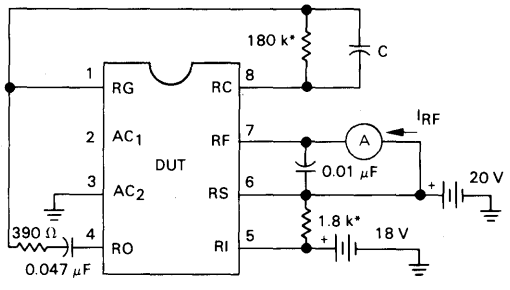


a. Set I_I to 30 mA. Measure voltage at Pin 2 (V_{off}).
b. Set I_I to 100 mA. Measure voltage at Pin 2 (V_{on}).

MC34012-1: C = 1000 pF*
MC34012-2: C = 500 pF*
MC34012-3: C = 1000 pF*

*Indicates 1% tolerance (5% otherwise)

FIGURE 6 — TEST FIVE



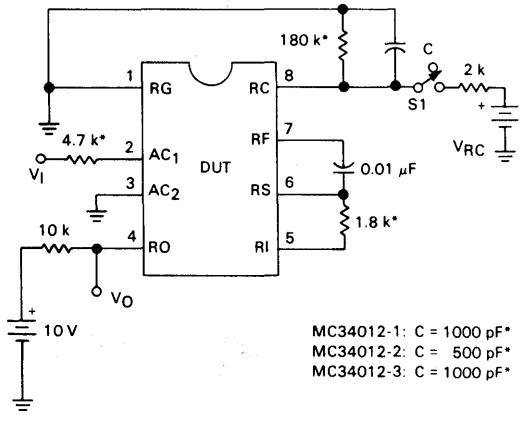
Measure current into Pin 7 (I_{RF}).
Calculate:

R_{RF} = 2 volts ÷ I_{RF}

MC34012-1: C = 1000 pF*
MC34012-2: C = 500 pF*
MC34012-3: C = 1000 pF*

*Indicates 1% tolerance (5% otherwise)

FIGURE 7 — TEST SIX



With V_{RC} = 3.5 volts, close S1. Set V_I to 50 volts. Measure dc voltage at Pin 4 (V_{O1}). Repeatedly change V_{RC} between 3.5 volts and 0 volts until Pin 4 changes state. Measure the new voltage at Pin 4 (V_{O2}). Calculate the peak-to-peak output voltage:

$$V_{Op\text{-}p} = | V_{O2} - V_{O1} |$$

*Indicates 1% tolerance (5% otherwise)

MOTOROLA

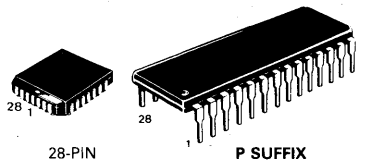
MC34013A

TELEPHONE SPEECH NETWORK AND TONE DIALER

- Linear/I^2L Technology Provides Low 1.4 Volt Operation in Both Speech and Dialing Modes
- Speech Network Provides 2-4 Wire Conversion with Adjustable Sidetone Utilizing an Electret Microphone
- DTMF Generator Uses Low-Cost Ceramic Resonator with Accurate Frequency Synthesis Technique
- On-Chip Regulator Insures Stable Operation Over Wide Range of Loop Lengths
- Dialer Mutes Speech Network with Internal Delay for Click Suppression on DTMF Key Release

SPEECH NETWORK AND TONE DIALER

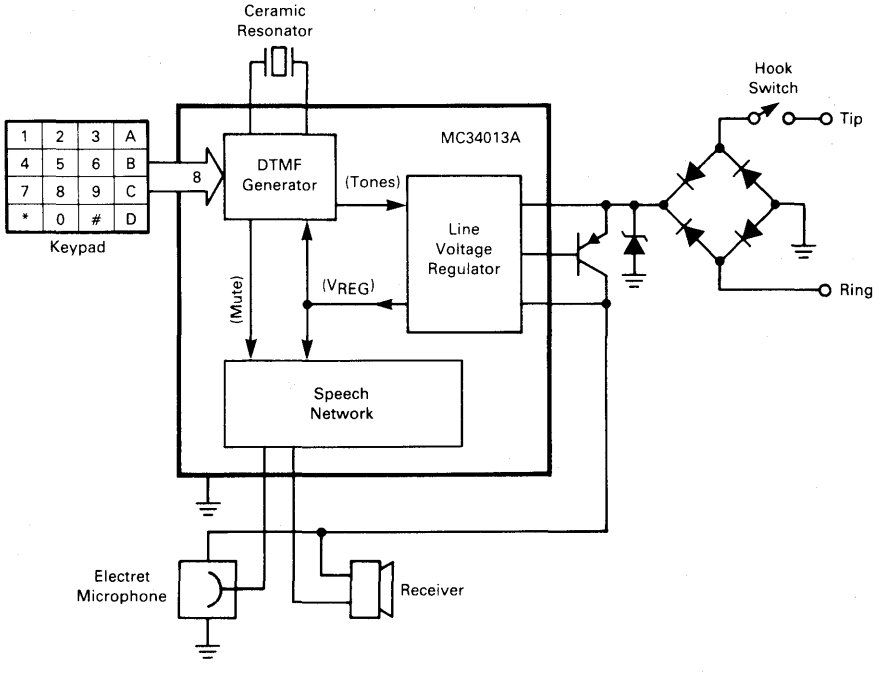
BIPOLAR LINEAR/I^2L



28-PIN
QUAD PACK
CASE 776-01

P SUFFIX
PLASTIC PACKAGE
CASE 710-02

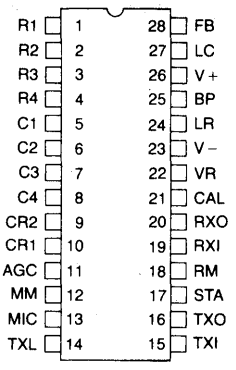
FIGURE 1 — FUNCTIONAL BLOCK DIAGRAM



MAXIMUM RATINGS (Voltage References to V−)

Parameter	Value	Unit
V+ Terminal Voltage (Pin 26)	+18, −1.0	V
VR Terminal Voltage (Pin 22)	+2.0, −1.0	V
RXO Terminal Voltage (Pin 20)	+2.0, −1.0	V
R1–R4 Terminal Current (Pins 1–4) C1–C4 (Pins 5–8)	±100	mA
Operating Ambient Temperature Range	−20 to +60	°C
Storage Temperature Range	−65 to +150	°C

PIN CONNECTIONS



2

GENERAL CIRCUIT DESCRIPTION

The MC34013A Electronic Speech Network and Tone Dialer provides a frequency synthesizer for DTMF dialing, analog amplifiers for speech transmission and a dc line interface circuit that terminates the telephone line. When mated with the MC34012 Tone Ringer, a complete tone dialing telephone can be produced with just two ICs.

Low voltage operation is a necessity for telephones in networks where parallel telephone connections are common. An electronic speech network operating in parallel with a conventional telephone may receive line voltages below 2.5 volts. DTMF dialers operate at similarly low-line voltages when signaling through battery powered station carrier equipment. These low voltage requirements have been addressed by realizing the MC34013A in a bipolar/I^2L technology with appropriate circuit techniques. The resulting speech and dialer circuits maintain specified performance with instantaneous input voltage as low as 1.4 volts.

Line Voltage Regulator

The dc line interface circuit (Figure 2) determines the dc input characteristic of the telephone. At low input voltages (less than 3 volts) the IC draws only the speech and dialer bias currents through the VR regulator. As input voltage increases, Q1 conducts the excess dc line current through resistor R12. The 1.5 volt level shift prevents saturation of Q2 with telephone line signals up to 2.0 volts peak (+5.2 dBm). A constant current (dummy load) is switched off when the DTMF dialer is activated to reduce line current transients. Figure 3 illustrates the dc voltage/current characteristic of an MC34013A telephone.

Speech Network

The speech network (Figure 4) provides the two-to-four wire interface between the telephone line and the instrument's transmitter and receiver. An electret microphone biased from VR drives the transmit amplifier. For very loud talkers, the peak limiter circuit reduces the transmit input level to maintain low distortion. The transmit amplifier output signal is inverted at the STA terminal and driven through an external R-C network to control the receiver sidetone level. The switched ac resistance at the RM terminal reduces receiver signal

FIGURE 2 — DC LINE INTERFACE BLOCK DIAGRAM

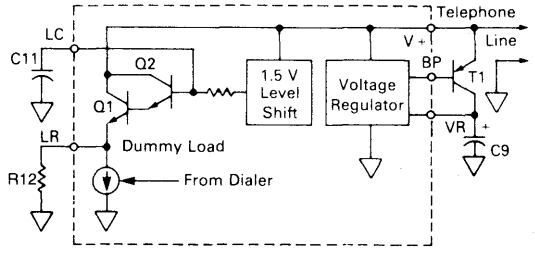
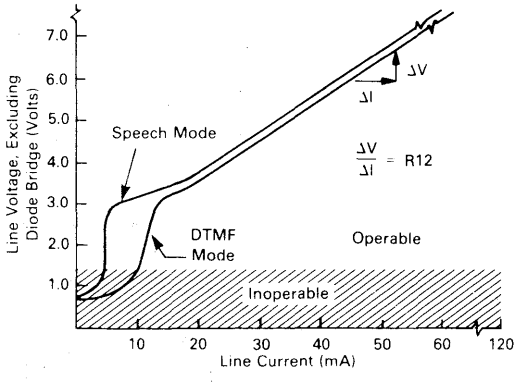
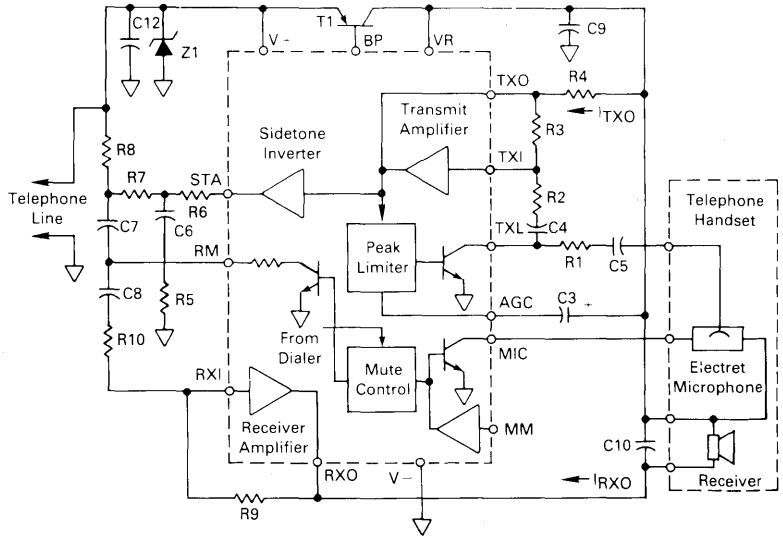


FIGURE 3 — DC V-I CHARACTERISTIC



GENERAL CIRCUIT DESCRIPTION (continued)

FIGURE 4 — SPEECH NETWORK BLOCK DIAGRAM



when dialing and suppresses clicks due to hook or keypad switch transitions. When transmitting, audio signal currents (i_{TXO} and i_{RXO}) flow through the voltage regulator pass transistor (T1) to drive the telephone line. This feature has two consequences: 1) In the transmitting mode the receiver sidetone current i_{RXO} contributes to the total signal on the line along with i_{TXO}; 2) The ac impedance of the telephone is determined by the receiver impedance and the voltage gain from the line to the receiver amplifier output.

DTMF Dialer

Keypad interface comparators activate the DTMF row and column tone generators (Figure 5) when a row and column input are connected through a SPST keypad. The keypad interface is designed to function with contact resistances up to 1.0 kΩ and leakage resistances as low as 150 kΩ. Single tones may be initiated by depressing two keys in the same row or column.

The programmable counters employ a novel design to produce non-integer frequency ratios. The various DTMF tones are synthesized with frequency division errors less than ±0.16% (Table 1). Consequently an inexpensive ceramic resonator can be used instead of a quartz crystal as the DTMF frequency reference. Total frequency error less than ±0.8% can be achieved with ±0.3% ceramic resonator. The row and column D/A converters produce 16-step approximations of sinusoidal waveforms. Feedback through terminal FB reduces the DTMF output impedance to approximately 2.0 kΩ to satisfy return loss specifications. (EIA RS-470)

FIGURE 5 — DTMF DIALER BLOCK DIAGRAM

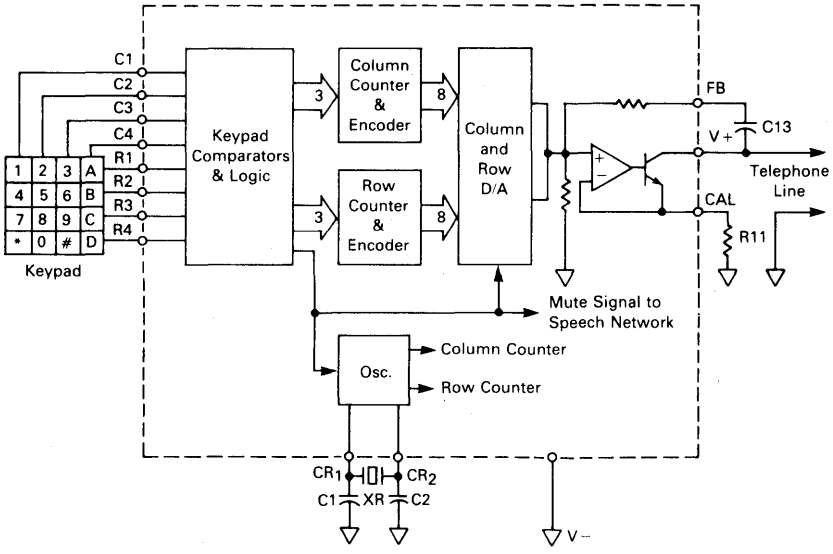


TABLE 1 — FREQUENCY SYNTHESIZER ERRORS

	DTMF Standard (Hz)	Tone Output Frequency with 500 kHz Oscillator	% Deviation from Standard
Row 1	697	696.4	−0.086
Row 2	770	769.2	−0.104
Row 3	852	853.2	+0.141
Row 4	941	939.8	−0.128
Column 1	1209	1207.7	−0.108
Column 2	1336	1336.9	+0.067
Column 3	1477	1479.3	+0.156
Column 4	1633	1634.0	+0.061

ELECTRICAL CHARACTERISTICS (T_A = 25°C)

LINE VOLTAGE REGULATOR

Characteristic	Test Method	Symbol	Min	Typ	Max	Unit
Voltage Regulator Output	1a	V_R	1.0	1.1	1.2	Volts
V+ Current in DTMF Mode	2a	I_{DT}	8.0	12	14.5	mA
Change in I_{DT} with Change in V+ Voltage	2b	ΔI_{DT}	—	0.8	2.0	mA
V+ Current in Speech Mode		I_{SP}				mA
V+ = 1.7 V	1b		3.0	5.0	7.0	
V+ = 5.0 V	1c		8.0	11	15	
Speech to DTMF Mode Current Difference	3	ΔI_{TR}	−2.0	2.0	3.5	mA
LR Level Shift		ΔV_{LR}				Vdc
V+ = 5.0 V, I_{LR} = 10 mA	4a		2.4	2.9	3.5	
V+ = 18 V, I_{LR} = 110 mA	4b		2.6	3.3	4.0	
LC Terminal Resistance	5	R_{LC}	30	50	75	kΩ
Load Regulation	6	ΔV_R	−20	−6.0	20	mVdc

ELECTRICAL CHARACTERISTICS (continued)

KEYPAD INTERFACE CIRCUIT

Characteristic	Test Method	Symbol	Min	Typ	Max	Unit
Row Input Pullup Resistance m^{th} Row Terminal: m = 1,2,3,4	7	R_{Rm}	5.0	8.0	11	kΩ
Column Input Pulldown Resistance n^{th} Column Terminal: n = 1,2,3,4	8	R_{Cn}	5.0	8.0	11	kΩ
Ratio of Row-to-Column Input Resistances $K_{m,n} = \frac{R_{Rm}}{R_{Cn}}$, m = 1,2,3,4 / n = 1,2,3,4	7 & 8	$K_{m,n}$	0.88	1.0	1.12	—
Row Terminal Open Circuit Voltage	7a	V_{ROC}	950	1100	1200	mVdc
Row Threshold Voltage for m^{th} Row Terminal: m = 1,2,3,4	9	V_{Rm}	0.70 V_{ROC}	—	—	Vdc
Column Threshold Voltage for n^{th} Column Terminal: n = 1,2,3,4	10	V_{Cn}	—	—	0.30 V_{ROC}	Vdc

DTMF GENERATOR

Row Tone Frequency	Row 1 Row 2 Row 3 Row 4	11a, 11b	f_{Rm}	692.9 765.3 848.9 935.1	696.4 769.2 853.2 939.8	699.9 773.0 857.5 944.5	Hz
Column Tone Frequency	Column 1 Column 2 Column 3 Column 4	11c, 11d	f_{Cn}	1201.6 1330.2 1471.9 1625.2	1207.7 1336.9 1479.3 1633.4	1213.7 1343.6 1486.7 1641.5	Hz
Row Tone Amplitude		11e	V_{Row}	0.38	0.45	0.55	V_{rms}
Column Tone Amplitude		11f	V_{Col}	0.48	0.55	0.67	V_{rms}
Column Tone Pre-emphasis		11g	dB_{CR}	0.5	1.8	3.0	dB
DTMF Distortion		12	% Dis	—	4.0	6.0	%
DTMF Output Resistance		13	R_o	1.0	2.5	3.0	kΩ

SPEECH NETWORK

MIC Terminal Saturation Voltage	14	V_{MIC}	—	60	125	mVdc
MIC Terminal Leakage Current	15a	I_{MIC}	—	0.0	5.0	μA
MM Terminal Input Resistance	15b	R_{MM}	50	100	170	kΩ
TXO Terminal Bias	16a	B_{TXO}	0.48	0.56	0.68	—
TXI Terminal Input Bias Current	16b	I_{TXI}	—	50	400	nA
TXO Terminal Positive Swing	16c	$V_{TXO}(+)$	—	25	60	mVdc
TXO Terminal Negative Swing	16d	$V_{TXO}(-)$	—	130	200	mVdc
Transmit Amplifier Closed-Loop Gain	17a	G_{TX}	16.5	19	20	V/V
Sidetone Amplifier Gain	17b	G_{STA}	0.40	0.45	0.54	V/V
STA Terminal Output Current	18	I_{STA}	50	100	250	μA
RXO Terminal Bias	19a	B_{RXO}	0.48	0.56	0.68	—
RXI Terminal Input Bias Current	19b	I_{RXI}	—	100	400	nA
RXO Terminal Positive Swing	19c	$V_{RXO}(+)$	—	1.0	20	mVdc
RXO Terminal Negative Swing	19d	$V_{RXO}(-)$	—	40	100	mVdc
TXL Terminal OFF Resistance	20a	$R_{TXL}(OFF)$	125	200	300	kΩ
TXL Terminal ON Resistance	20b	$R_{TXL}(ON)$	—	20	100	Ω
RM Terminal OFF Resistance	21a	$R_{RM}(OFF)$	125	180	300	kΩ
RM Terminal ON Resistance	21b	$R_{RM}(ON)$	410	570	770	Ω

PIN DESCRIPTION

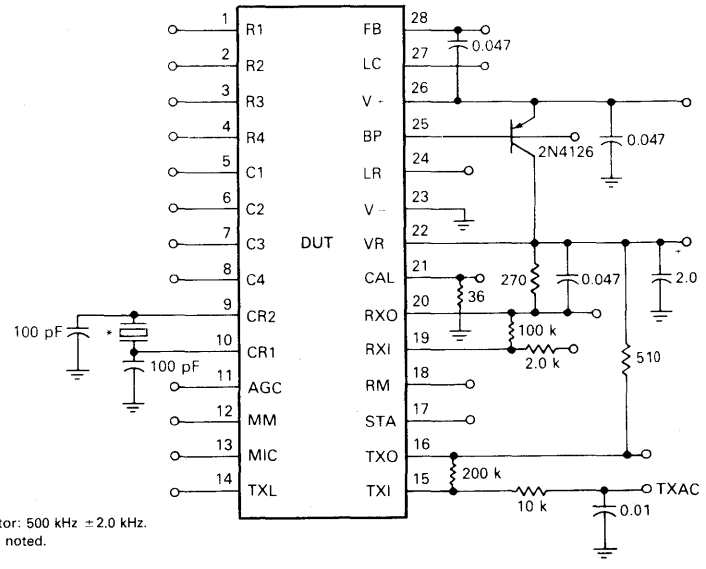
(See Figure 28 for external component identifications.)

Pin	Designation	Function
1–4	R1–R4	Keypad inputs for Rows 1 through 4. When open, internal 8.0 kΩ resistors pull up the row inputs to a regulated (≈1.1 volt) supply. In normal operation, a row and a column input are connected through a SPST switch by the telephone keypad. Row inputs can also be activated by a Logic "0" (<500 mV) from a microprocessor port.
5–8	C1–C4	Keypad inputs for Columns 1 through 4. When open, internal 8.0 kΩ resistors pull down the column inputs to V−. In normal operation, connecting any column input to any row input produces the respective row and column DTMF tones. In addition to being connected to a row input, column inputs can be activated by a Logic "1" (>500 mV and <3.0 volt).
10,9	CR1, CR2	Ceramic Resonator oscillator input and feedback terminals, respectively. The DTMF dialer is intended to operate with a 500 kHz ceramic resonator from which row and column tones are synthesized.
11	AGC	Automatic Gain Control low-pass filter terminal. Capacitor C3 connected between AGC and VR sets the attack and decay time of the transmit limiter circuit. This capacitor also aids in reducing clicks in the receiver due to hook-switch transients and DTMF on/off transients. In conjunction with internal resistors, C3 (1.0 μF) forms a timer which mutes the receiver amplifier for approximately 20 milliseconds after the user goes off-hook or releases a DTMF Key.
12	MM	Microphone Mute. The MM pin provides a means to mute the microphone and transmit amplifier in response to a digital control signal. When this pin is connected to a Logic "1" (>2.0 V) the microphone dc return path and the transmit amplifier output are disabled.
13	MIC	MICrophone negative supply terminal. The dc current from the electret microphone is returned to V− through the MIC terminal which is connected to the collector of an on-chip NPN transistor. The base of this transistor is controlled either internally by the mute signal from the DTMF generator, or externally by the logic input pin MM.
14	TXL	Transmit Input Limiter. An internal variable resistance element at the TXL terminal controls the transmitter input level to prevent clipping with high signal levels. Coupling capacitors C4 and C5 prevent dc current flow through TXL. The dynamic range of the transmit peak limiter is controlled by resistors R1 and R2.
15	TXI	Transmit Amplifier Input. TXI is the input to the transmit amplifier from an electret microphone. AC coupling capacitors allow the dc offset at TXI to be maintained approximately 0.6 V above V− by feedback through resistor R3 from TXO.
16	TXO	Transmit Amplifier Output. The transmit amplifier output drives ac current through the voltage regulator pass-transistor T1 via resistor R4. The dc bias voltage at TXO is typically 0.6 volts above V−. The transmit amplifier gain is controlled by the R3/(R1 + R2) ratio.
17	STA	SideTone Amplifier output. STA is the output of the sidetone inverter amplifier whose input is driven by the transmit signal at TXO. The inverted transmit signal from STA subtracts from the receiver amplifier input current from V+, thus reducing the receiver sidetone level. Since the transmitted signal at V+ is phase shifted with respect to TXO by the reactive impedance of the phone line, the signal from STA must be similarly phase-shifted in order to provide adequate sidetone reduction. This phase relationship between the transmit signal at TXO and the sidetone cancellation signal from STA is controlled by R5, R6, and C6.
18	RM	Receiver Amplifier Mute. A switched resistance at the RM terminal attenuates the receiver amplifier input signal produced by DTMF dialing tones at V+. RM also mutes clicks at the receiver which result from keypad or hook switch transitions. The ac resistance at RM is typically 540 Ω in the mute mode and 200 kΩ otherwise. Coupling capacitors C7 and C8 prevent dc current flow through RM.
19	RXI	Receiver Amplifier Input. RXI is the input terminal of the receiver amplifier which is driven by ac signals from V+ and STA. Input coupling capacitor C8 allows RXI to be biased approximately 0.6 volts above the V− via feedback resistor R9.
20	RXO	Receiver Amplifier Output. This terminal is connected to the open-collector NPN output transistor of the receiver amplifier. DC bias current for the output device is sourced through the receiver from VR. The bias voltage at RXO is typically 0.6 volts above the V−. Capacitor C10 from RXO to VR provides frequency compensation for the receiver amplifier.

PIN DESCRIPTION (continued)

Pin	Designation	Function
21	CAL	Amplitude CALibration terminal for DTMF dialer. Resistor R11 from the CAL pin to V− controls the DTMF output signal level at Tip and Ring.
22	VR	Voltage Regulator output terminal. VR is the output of a 1.1 volt voltage regulator which supplies power to the speech network amplifiers and DTMF generator during signaling. To improve regulator efficiency at low line current conditions, an external PNP pass-transistor T1 is used in the regulator circuit. Capacitor C9 frequency compensates the VR regulator to prevent oscillation.
23	V−	The dc common (more negative input) connected to Tip and Ring through the polarity guard bridge.
24	LR	DC Load Resistor. Resistor R12 from LR to V− determines the dc input resistance at Tip and Ring. This resistor is external not only to enable programming the dc resistance but also to avoid high on-chip power dissipation with short telephone lines. It acts as a shunt load conducting the excess dc line current. At low line voltages (<3.0 volts), no current flows through LR.
25	BP	Base of a PNP Pass-transistor. Under long-loop conditions where low line voltages would cause VR to fall below 1.1 volts, BP drives the PNP transistor T1 into saturation, thereby minimizing the voltage drop across the pass transistor. At line voltages which maintain VR above 1.1 volts, BP biases T1 in the linear region thereby regulating the VR voltage. Transistor T1 also couples the ac speech signals from the transmit amplifier to Tip and Ring at V+.
26	V+	The more positive input to the regulator, speech, and DTMF sections connected to Tip and Ring through the polarity guard diode bridge.
27	LC	DC Load Capacitor. Capacitor C11 from LC to V− forms a low-pass filter which prevents the resistor at LR from loading ac speech and DTMF signals.
28	FB	FeedBack terminal for DTMF output. Capacitor C13 connected from FB to V+ provides ac feedback to reduce the output impedance to Tip and Ring when tone dialing.

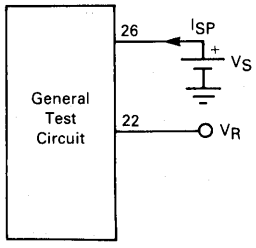
FIGURE 6 — GENERAL TEST CIRCUIT



Notes:
1. *Selected ceramic resonator: 500 kHz ±2.0 kHz.
2. Capacitances in μF unless noted.
3. All resistances in ohms.

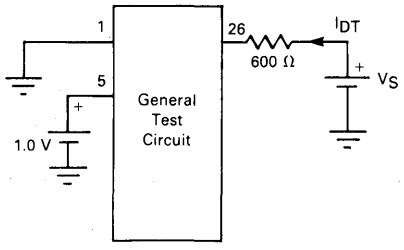
2

FIGURE 7 — TEST ONE



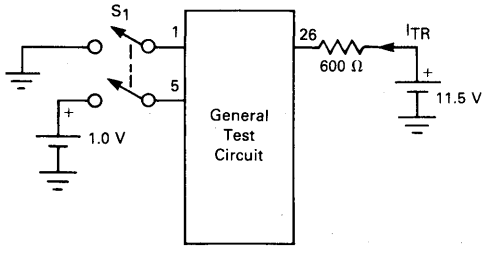
a. Measure V_R with V_S = 1.7 V
b. Measure I_{SP} with V_S = 1.7 V
c. Measure I_{SP} with V_S = 5.0 V

FIGURE 8 — TEST TWO



a. Measure I_{DT} with V_S = 11.5 V
b. Measure I_{DT} with V_S = 26 V. Calculate $\Delta I_{DT} = I_{DT}\big|_{26\ V} - I_{DT}\big|_{11.5\ V}$

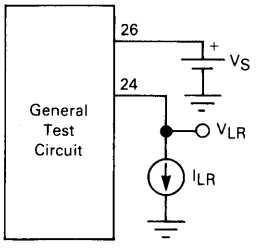
FIGURE 9 — TEST THREE



With S_1 open measure I_{TR}. Close S_1 and again measure I_{TR}. Calculate:

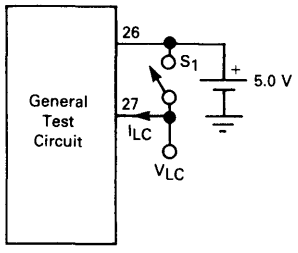
$$\Delta I_{TR} = I_{TR}\big|_{S_1\ Closed} - I_{TR}\big|_{S_1\ Open}$$

FIGURE 10 — TEST FOUR



a. Set V_S = 5.0 V and I_{LR} = 10 mA. Measure V_{LR}. Calculate $\Delta V_{LR} = V_S - V_{LR}$
b. Repeat Test 4a with V_S = 18 V and I_{LR} = 110 mA

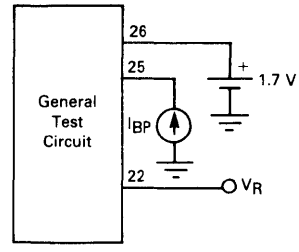
FIGURE 11 — TEST FIVE



With S_1 open measure V_{LC}.
Close S_1 and measure I_{LC}.
Calculate:

$$R_{LC} = \frac{5.0 - V_{LC}}{I_{LC}}$$

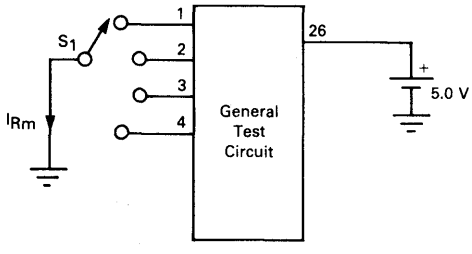
FIGURE 12 — TEST SIX



Set I_{BP} = 0.0 μA and measure V_R.
Set I_{BP} = 150 μA and measure V_R. Calculate:

$$\Delta V_R = |V_R|_{0.0\ \mu A} - |V_R|_{150\ \mu A}$$

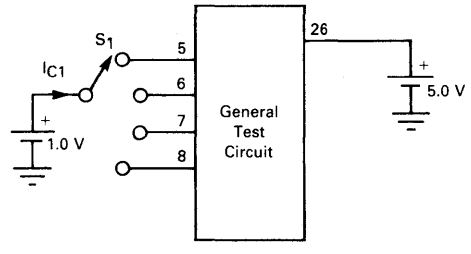
FIGURE 13 — TEST SEVEN



Subscript m corresponds to row number.

a. Set S_1 to Terminal 2 and measure voltage at Terminal 1 (V_{ROC}).
b. Set S_1 to Terminal 1 (m = 1) and measure I_{R1}. Calculate:
$R_{R1} = V_{ROC} \div I_{R1}$
c,d,e. Repeat Test 7b for m = 2,3,4.

FIGURE 14 — TEST EIGHT

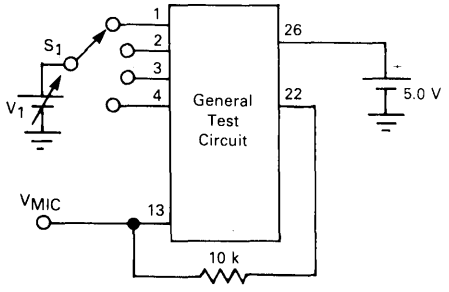


Subscript n corresponds to column number.

a. Set S_1 to Terminal 5 (n = 1) and measure I_{C1}. Calculate:
$R_{C1} = 1.0\ V \div I_{C1}$
b,c,d. Repeat Test 8a for n = 2,3,4.

2

FIGURE 15 — TEST NINE

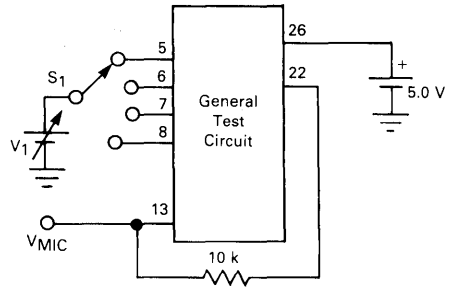


m corresponds to row number.

a. Set S_1 to Terminal 1 (m = 1) with V_1 = 1.0 Vdc. Verify V_{MIC} is Low (V_{MIC} < 0.3 Vdc). Decrease V_1 to 0.70 V_{ROC} and verify V_{MIC} switches high. (V_{MIC} > 0.5 Vdc). V_{ROC} is obtained from Test 7a.

b,c,d. Repeat Test 9a for rows 2,3, and 4. (m = 2,3,4)

FIGURE 16 — TEST TEN

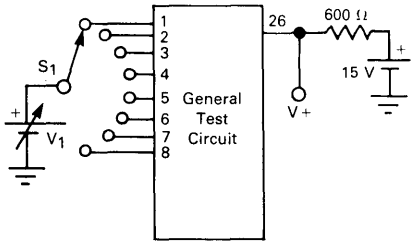


n corresponds to column number.

a. Set S_1 to Terminal 5 (n = 1) with V_1 = 0 Vdc, Verify V_{MIC} is low (V_{MIC} <0.3 Vdc). Increase V_1 to 0.30 V_{ROC} and verify V_{MIC} switches high, (V_{MIC} > 0.5 Vdc). V_{ROC} is obtained from Test 7a.

b,c,d. Repeat Test 10a for columns 2,3, and 4. (n = 2,3,4)

FIGURE 17 — TEST ELEVEN



m corresponds to row number.
n corresponds to column number.

a. With V_1 = 0.0 V set S_1 to Terminal 1 (m = 1) and measure frequency of tone at V+.

b. Repeat Test 11a for rows 2,3 and 4. (m = 2,3,4).

c. With V_1 = 1.0 V set S_1 to Terminal 5. (n = 1) and measure frequency of tone at V+.

d. Repeat Test for columns 2,3, and 4. (n = 2,3,4).

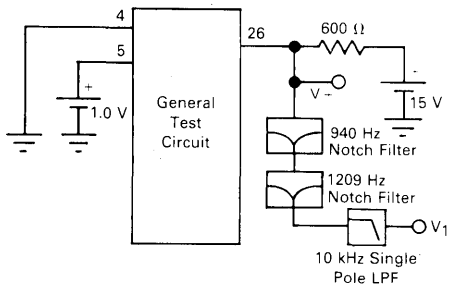
e. Set S_1 to Terminal 4 and V_1 = 0.0 V. Measure row tone amplitude at V+ (V_{ROW}).

f. Set S_1 to Terminal 8 and V_1 = 1.0 V. Measure column tone amplitude at V+. (V_{COL}).

g. Using results of Tests 11e and 11f, calculate:

$$dB_{CR} = 20 \log_{10} \frac{V_{COL}}{V_{ROW}}$$

FIGURE 18 — TEST TWELVE

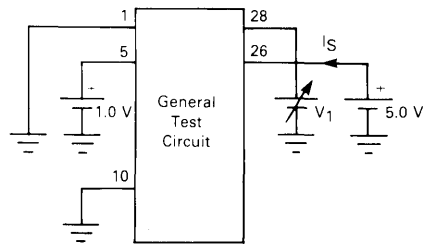


Note: The notch filters must have 50 dB attenuation at their respective center frequencies.

Measure V+ and V_1 with a true rms voltmeter. Calculate:

$$\% \text{ DIS} = \frac{V_1(\text{rms})}{V+(\text{rms})} \times 100$$

FIGURE 19 — TEST THIRTEEN

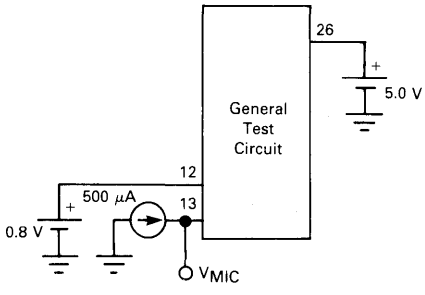


Measure I_S at V_1 = 1.8 V and V_1 = 2.8 V.

Calculate:

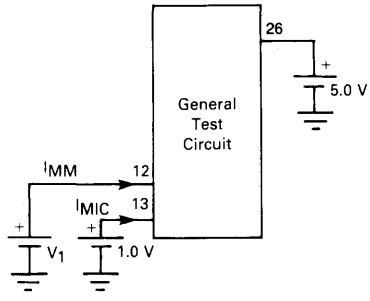
$$R_O = 1.0\ \text{V} \div \left[I_S \Big|_{2.8\ \text{V}} - I_S \Big|_{1.8\ \text{V}} \right]$$

FIGURE 20 — TEST FOURTEEN



Measure V_{MIC}

FIGURE 21 — TEST FIFTEEN

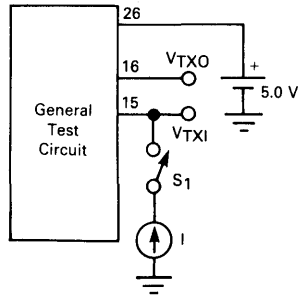


a. Set V_1 = 2.0 V and measure I_{MIC}.

b. Set V_1 = 5.0 V and measure I_{MM}.
Calculate: $R_{MM} = 5.0\ \text{V} \div I_{MM}$

2

FIGURE 22 — TEST SIXTEEN



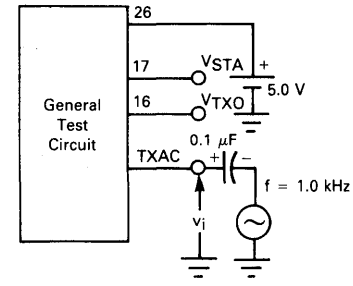
a. With S_1 open, measure V_{TXO}. Using V_R obtained in Test 1 Calculate: $B_{TXO} = V_{TXO} \div V_R$

b. With S_1 open, measure V_{TXO} and V_{TXI}. Calculate: $I_{TXI} = (V_{TXO} - V_{TXI}) \div 200\ k\Omega$

c. Close S_1 and set $I = -10\ \mu A$. Measure V_{TXO}. Calculate: $V_{TXO}(+) = V_R - V_{TXO}$ where V_R is obtained from Test 1.

d. Close S_1 and set $I = +10\ \mu A$. Measure V_{TXO}. $V_{TXO}(-) = V_{TXO}$.

FIGURE 23 — TEST SEVENTEEN



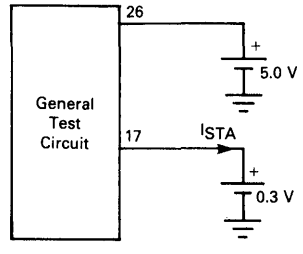
a. Set the generator for $v_i = 3.0\ mV_{rms}$. Measure ac voltage V_{TXO}. Calculate:

$$G_{TX} = \frac{V_{TXO}}{v_i}$$

b. Measure ac voltage V_{STA}. Using V_{TXO} from Test 17a calculate:

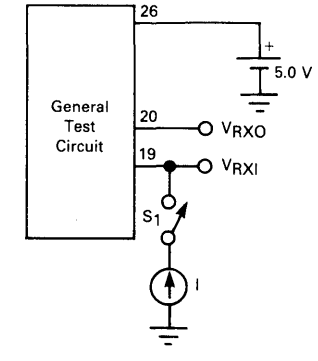
$$G_{STA} = \frac{V_{STA}}{V_{TXO}}$$

FIGURE 24 — TEST EIGHTEEN



Measure I_{STA}.

FIGURE 25 — NINETEEN



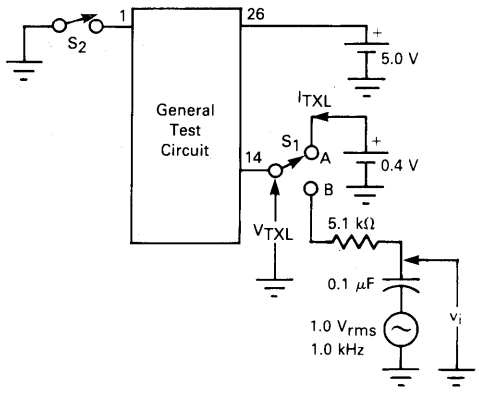
a. With S_1 open, measure V_{RXO}. Using V_R obtained in Test 1, calculate: $B_{RXO} = V_{RXO} \div V_R$.

b. With S_1 open, measure V_{RXO} and V_{RXI}. Calculate: $I_{RXI} = (V_{RXO} - V_{RX1}) \div 100\ k\Omega$

c. Close S_1 and set $I = -10\ \mu A$. Measure V_{RXO}. Using V_R obtained in Test 1, calculate: $V_{RXO}(+) = V_R - V_{RXO}$.

d. Close S_1 and set $I = +10\ \mu A$ and measure V_{RXO}. $V_{RXO}(-) = V_{RXO}$.

FIGURE 26 — TEST TWENTY

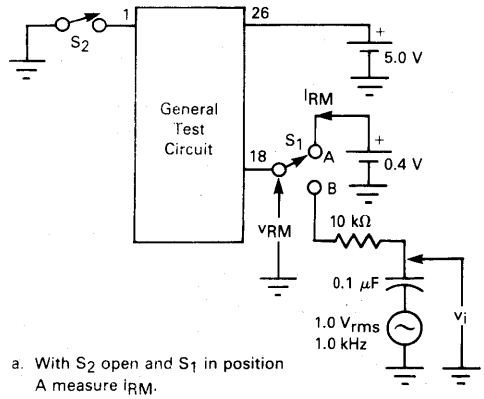


a. Set S_1 to position A with S_2 open. Measure I_{TXL}.
Calculate: R_{TXL} (OFF) = 0.4 V ÷ I_{TXL}.

b. Set S_1 to position B and close S_2. Measure ac voltages v_i and V_{TXL}. Calculate:

$$R_{TXL}(ON) = \frac{V_{TXL}}{v_i - V_{TXL}} \times 5.1\ k\Omega$$

FIGURE 27 — TEST TWENTY-ONE



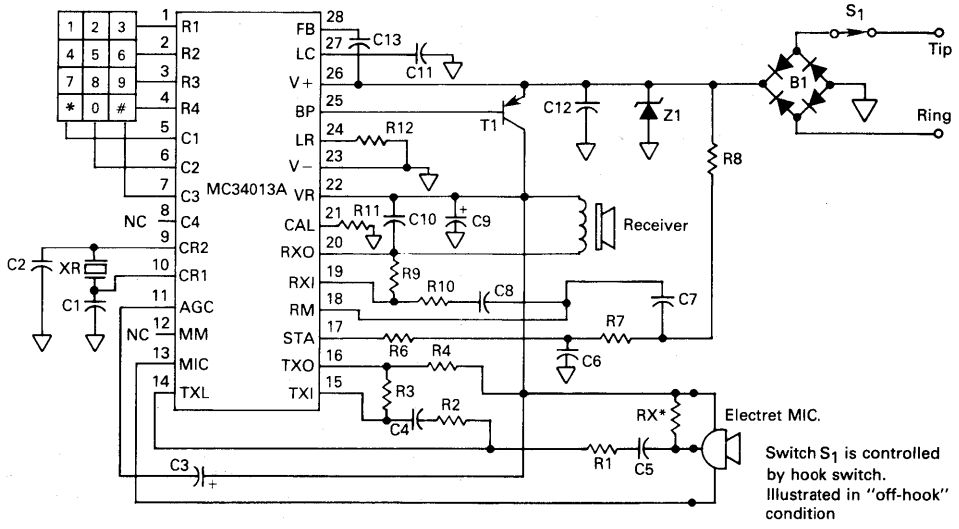
a. With S_2 open and S_1 in position A measure I_{RM}.
Calculate: $R_{RM}(OFF) = 0.4\ V \div I_{RM}$

b. Close S_2 and switch S_1 to position B. Measure ac voltages v_i and V_{RM}.
Calculate:

$$R_{RM}(ON) = \frac{V_{RM}}{v_i - V_{RM}} \times 10\ k\Omega$$

FIGURE 28 — APPLICATION CIRCUIT

DTMF Pad
Row-Column Switch Closure



*RX used with 2-terminal mike only.

APPLICATIONS INFORMATION

Figure 28 specifies a typical application circuit for the MC34013A. Complete listings of external components are provided at the end of this section along with nominal component values. Component values should be varied to optimize telephone performance parameters for each application. The relationships between the application circuit components and certain telephone parameters are briefly described in the following:

Off-Hook DC Resistance

R12 conducts the dc line current in excess of the speech and dialer bias current. Increasing R12 increases the input resistance of the telephone for line currents above 10 mA. R12 should be selected between 30 Ω and 120 Ω.

Off-Hook AC Impedance

The ac input impedance is equal to the receive amplifier load impedance (at RXO) divided by the receive amplifier gain (voltage gain from V+ to RXO). Increasing the impedance of the receiver increases the impedance of the telephone. Increasing the gain of the receiver amplifier decreases the impedance of the telephone.

DTMF Output Amplitude

R11 controls the amplitude of the row and column DTMF tones. Decreasing R11 increases the level of tones generated at V+. The ratio of the row and column tone amplitudes is internally fixed. R11 should be greater than 20 Ω to avoid excessive current in the DTMF output amplifier.

Transmit Output Level

R4 controls the maximum signal amplitude produced at V+ by the transmit amplifier. Decreasing R4 increases the transmit output signal at V+. R4 should be greater than 220 Ω to limit current in the transmit amplifier output.

Transmit Gain

The gain from the microphone to the telephone line varies directly with R3. Increasing R3 increases the signal applied to R4 and the ac current driven through R4 to the telephone line. The closed loop-gain from the microphone to the TXO terminal should be greater than 10 to prevent transmit amplifier oscillations.

Note: Adjustments to transmit level and gain are complicated by the addition of receiver sidetone current to the transmit amplifier output current at V+. Normally the sidetone current from the receiver will increase the transmit signal (if the current in the receiver is in phase with that in R4). Thus the transmit gain and sidetone levels cannot be adjusted independently.

Receiver Gain

Feedback resistor R9 adjusts the gain at the receiver amplifier. Increasing R9 increases the receiver amplifier gain.

Sidetone Level

Sidetone reduction is achieved by the cancellation of receiver amplifier input signals from R8. R6, R7 and C6 determine the phase of the sidetone balance. The ac voltage at the junction of R6 and R7 should be 180° out of phase with the voltage at V+. R7 is selected such that the signal current in R7 is slightly greater than that in R8. This insures that the sidetone current in the receiver adds to the transmit amplifier output current.

EXTERNAL COMPONENTS

(Component Labels Referenced to Figure 28)

Capacitors	Nominal Value	Description
C1, C2	100 pF	Ceramic Resonator oscillator capacitors.
C3	1.0 μF, 3.0 V	Transmit limiter low-pass filter capacitor: controls attack and decay time of transmit peak limiter.
C4, C5	0.1 μF	Transmit amplifier input capacitors: prevent dc current flow into TXL pin and attenuate low-frequency noise on microphone lead.
C6	0.05 μF	Sidetone network capacitor: provides phase-shift in sidetone path to match that caused by telephone line reactance.
C7, C8	0.05 μF	Receiver amplifier input capacitors: prevent dc current flow into RM terminal and attenuates low frequency noise on the telephone line.
C9	2.2 μF, 3.0 V	VR regulator capacitor: frequency compensates the VR regulator to prevent oscillation.
C10	0.01 μF	Receiver amplifier output capacitor: frequency compensates the receiver amplifier to prevent oscillation.
C11	0.1 μF	DC load filter capacitor: prevents the dc load circuit from attenuating ac signals on V+.
C12	0.01 μF	Telephone line bypass capacitor: terminates telephone line for high frequency signals and prevents oscillation in the VR regulator.
C13	0.1 μF	DTMF output feedback capacitor: ac couples feedback around the DTMF output amplifier which reduces output impedance.

Resistors	Nominal Value	Description
R12	82, 1.0 W	DC load resistor: conducts all dc line current in excess of the current required for speech or dialing circuits; controls the off-hook dc resistance of the telephone.
R8, R10	150 k, 56 k	Receiver amplifier input resistors: couple ac input signals from the telephone line to the receiver amplifier; signal in R8 subtracts from that in R7 to reduce sidetone in receiver.
R9	200 k	Receiver amplifier feedback resistor: controls the gain of the receiver amplifier.
R6, R7	1.5 k, 30 k	Sidetone network resistors: drive receiver amplifier input with the inverted output signal from the transmitter; phase of signal in R7 should be opposite that in R8.
R4	270	Transmit amplifier load resistor: converts output voltage of transmit amplifier into a current that drives the telephone line; controls the maximum transmit level.
R3	200 k	Transmit amplifier feedback resistor: controls the gain of the transmit amplifier.
R1, R2	4.7 k, 4.7 k	Transmit amplifier input resistors: couple signal from microphone to transmit amplifier; control the dynamic range of the transmit peak limiter.
R11	36	DTMF calibration resistor: controls the output amplitude of the DTMF dialer.
R_X	3.0 k	Microphone bias resistor: sources current from VR to power a 2-terminal electret microphone; R_X is not used with 3-terminal microphones.

Semiconductors	Electret Mic	Receiver
B1 = MDA106A, or equivalent, or 4-1N4005 T1 = 2N4126 or equivalent Z1 = 18 V, 1.5 W, 1N5931A XR — muRata CSB500 or equivalent	2 Terminal, Primo EM-95 (Use R_X) or equivalent 3 Terminal, Primo 07A181P (Remove R_X) or equivalent	Primo Model DH-34 (300 Ω) or equivalent

MOTOROLA

MC34014

Specifications and Applications Information

2

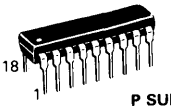
TELEPHONE SPEECH NETWORK WITH DIALER INTERFACE

The MC34014 is a Telephone Speech Network integrated circuit which incorporates adjustable transmit, receive, and sidetone functions, a dc loop interface circuit, tone dialer interface, and a regulated output voltage for a pulse/tone dialer. Also included is an equalization circuit which compensates gains for line length variations. The conversion from 2-to-4 wire is accomplished with a supply voltage as low as 1.5 volts. The MC34014 is packaged in a standard 18-pin (0.3" wide) plastic DIP, and a 20-pin surface mount PLCC package.

- Transmit, Receive, and Sidetone Gains Set by External Resistors
- Loop Length Equalization for Transmit, Receive, and Sidetone Functions
- Operates Down to 1.5 volts (V+) in Speech Mode
- Provides Regulated Voltage for CMOS Dialer
- Speech Amplifiers Muted During Pulse and Tone Dialing
- DTMF Output Level Adjustable with a Single Resistor
- Compatible with 2-Terminal Electret Microphones
- Compatible with Receiver Impedances of 150 Ω and Higher

TELEPHONE SPEECH NETWORK WITH DIALER INTERFACE

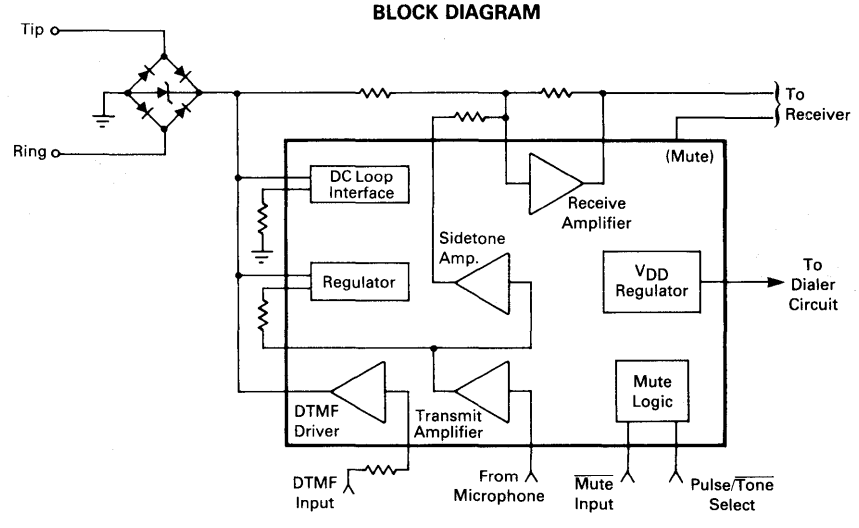
SILICON MONOLITHIC INTEGRATED CIRCUIT



P SUFFIX
PLASTIC PACKAGE
CASE 707-02

FN SUFFIX
PLASTIC PACKAGE
CASE 775-01
PLCC-20

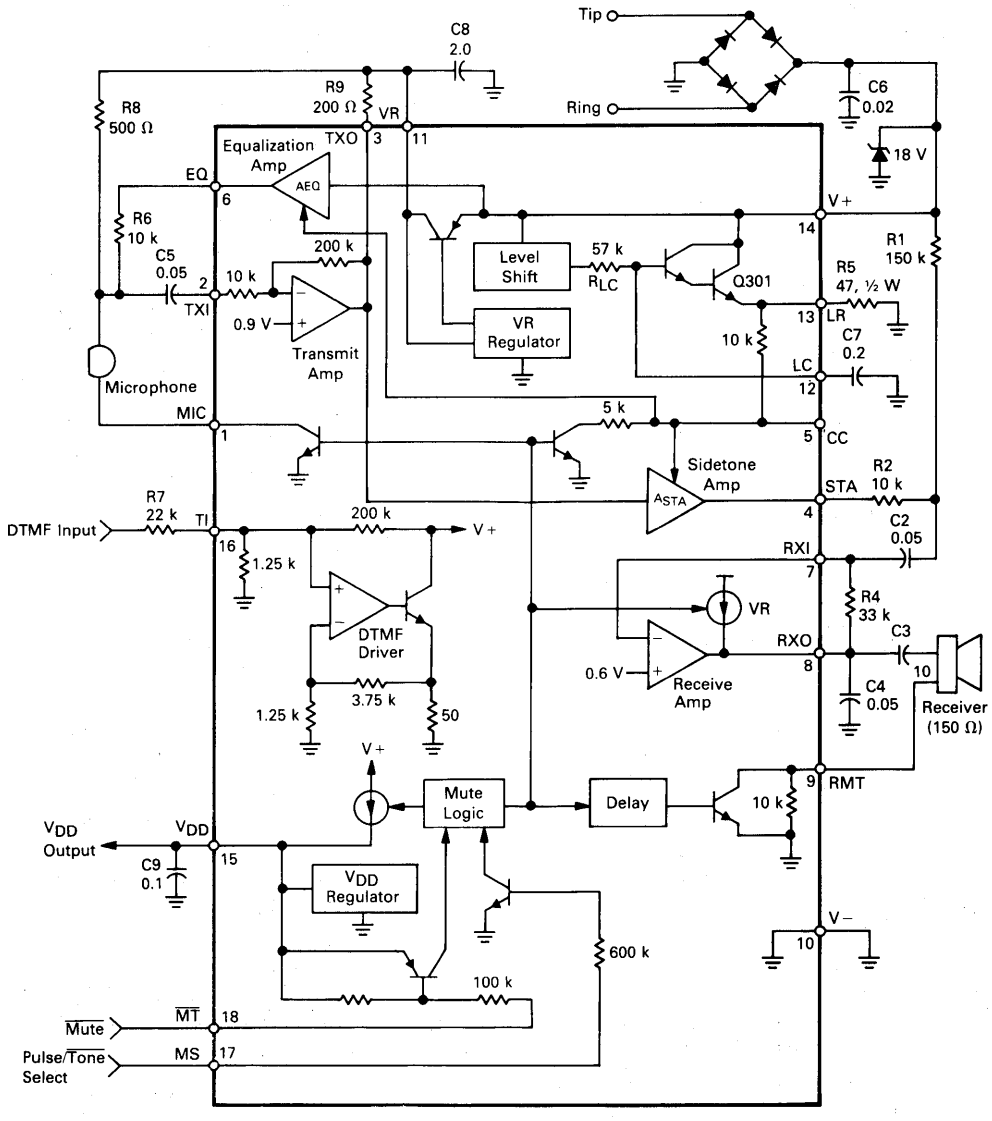
BLOCK DIAGRAM



PIN DESCRIPTION (See Figure 1)

Pin # PLCC	Pin # DIP	Name	Description
2	1	MIC	Microphone negative supply. Bias current from the electret microphone is returned to V− through this pin, through an open collector NPN transistor whose base is controlled by an internal mute signal. During dialing, the transistor is off, disabling the microphone.
3	2	TXI	Transmit amplifier input. Input impedance is 10 kΩ. Signals from the microphone are input through capacitor C5 to TXI.
4	3	TXO	Transmit amplifier output. The ac signal current from this output flows through the V_R series pass transistor via R9 to drive the line at V+. Increasing R9 will decrease the signal at V+. The output is biased at ≈0.65 V to allow for maximum swing of ac signals. The closed loop gain from TXI to TXO is internally set at 26 dB.
6	4	STA	Sidetone amplifier output. Input to this amplifier is TXO. The signal at STA cancels the sidetone signals in the receive amplifier. The signal level at STA increases with loop length.
7	5	CC	Compensation Capacitor. A capacitor from CC to ground will compensate the loop length equalization circuit when additional stability is required. In most applications, CC remains open.
8	6	EQ	Equalization amplifier output. A portion of the V+ signal is present on this pin to provide negative feedback around the transmit amplifier. The feedback decreases with increasing loop length, causing the ac impedance of the circuit to increase.
9	7	RXI	Receive amplifier input. Input impedance is >100 kΩ. Signals from the line and sidetone amplifier are summed at RXI.
10	8	RXO	Receive Amplifier output. RXO is biased by a 2.5 mA current source. Feedback maintains the dc bias voltage at ≈0.65 V. Increasing R4 (between RXO and RXI) will increase the receive gain. C4 stabilizes the amplifier. C3 couples the signals to the receiver. The 2.5 mA current source is reduced to 0.4 mA when dialing.
11	9	RMT	Receiver Mute. The ac receiver current is returned to V− through an open collector NPN transistor and a parallel 10 kΩ resistor. The base of the NPN is controlled by an internal mute signal. During dialing the transistor is off, leaving the 10 kΩ resistor in series with the receiver.
12	10	V−	Negative supply. The most negative input connected to Tip and Ring through the polarity guard diode bridge.
13	11	VR	Regulated voltage output. The VR voltage is regulated at 1.2 V and biases the microphone and the speech circuits. An internal series pass PNP transistor allows for regulation with a line voltage as low as 1.5 V. Capacitor C8 stabilizes the regulator.
14	12	LC	DC load capacitor. An external capacitor C7 and an internal resistor form a low pass filter between V+ and LR to prevent ac signals from being loaded by the dc load resistor R5. Forcing LC to V− will turn off the dc load current and increase the V+ voltage.
15	13	LR	DC load resistor. Resistor R5 from LR to V− determines the dc resistance of the telephone, and removes power dissipation from the chip. The LR pin is biased 2.8 volts below the V+ voltage (4.5 volts in the tone dialing mode).
16	14	V+	Positive supply. V+ is the positive line voltage (from Tip & Ring) through the polarity guard bridge. All sections of the MC34014 are powered by V+.
18	15	V_{DD}	V_{DD} regulator. V_{DD} is the output of a shunt type regulator with a nominal voltage of 3.3 V. The nominal output current is increased from 550 μA to 2 mA when dialing. Capacitor C9 stabilizes the regulator and sustains the V_{DD} voltage during pulse dialing.
19	16	TI	Tone input. The DTMF signal from a dialer circuit is input at TI through an external resistor R7. The current at TI is amplified to drive the line at V+. Increasing R7 will reduce the DTMF output levels. The input impedance at TI is nominally 1.25 kΩ.
20	17	MS	Mode select. This pin is connected through an internal 600 kΩ resistor to the base of an NPN transistor. A Logic "1" (>2.0 V) selects the pulse dialing mode. A Logic "0" (<0.3 V) selects the tone dialing mode.
1	18	$\overline{MT}$	Mute input. $\overline{MT}$ is connected through an internal 100 kΩ resistor to the base of a PNP transistor, with the emitter at V_{DD}. A Logic "0" (<1.0 V) will mute the network for either pulse or tone dialing. A Logic "1" (>V_{DD} − 0.3 V) puts the MC34014 into the speech mode.

FIGURE 1 — TEST CIRCUIT



NOTE: Pin numbers are for 18 pin DIP.

ABSOLUTE MAXIMUM RATINGS (Voltages referred to V−, T_A = 25°C) (See Note 1.)

Parameter	Value	Units
V+ Voltage	−1.0, +18	Vdc
V_{DD} (externally applied, V+ = 0)	−1.0, +6	Vdc
V_{LR}	−1.0, V+ − 3.0	Vdc
$\overline{MT}$, MS Inputs	−1.0, V_{DD} +1.0	Vdc
Storage Temperature	−65, +150	°C

NOTE 1: Devices should not be operated at these values. The "Recommended Operating Conditions" provide conditions for actual device operation.

RECOMMENDED OPERATING CONDITIONS

Parameter	Value	Units
V+ Voltage (Speech Mode) (Tone Dialing Mode)	+1.5 to +15 +3.3 to +15	Vdc Vdc
I_{TXO} (Instantaneous)	0 to 10	mA
Ambient Temperature	20 to +60	°C

ELECTRICAL CHARACTERISTICS (Refer to Figure 1) (T_A = 25°C)

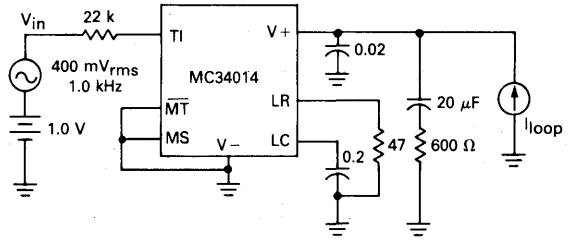
Parameter	Symbol	Min	Typ	Max	Units
LINE INTERFACE					
V+ Voltage	V+				Vdc
I_{loop} = 20 mA (Speech/Pulse Mode)		2.6	3.2	3.8	
I_{loop} = 30 mA (Speech/Pulse Mode)		3.0	3.7	4.4	
I_{loop} = 120 mA (Speech/Pulse Mode)		7.0	8.2	9.5	
I_{loop} = 20 mA (Tone Mode)		4.1	4.9	5.7	
I_{loop} = 30 mA (Tone Mode)		4.6	5.4	6.2	
V+ Current (Pin 12 Grounded)	I+				mA
V+ = 1.7 V (Speech Mode)		4.0	6.6	8.5	
V+ = 12 V (Speech/Pulse Modes)		5.5	8.4	12.5	
V+ = 12 V (Tone Mode)		6.0	8.8	14.0	
LR Level Shift (V+ − V_{LR})	ΔV_{LR}				Vdc
(Speech/Pulse Mode)		—	2.7	—	
(Tone Mode)		—	4.3	—	
LC Terminal Resistance	R_{LC}	36	57	94	kΩ
VOLTAGE REGULATORS					
VR Voltage (V+ = 1.7 V)	V_R	1.1	1.2	1.3	Vdc
Load Regulation (0 mA < I_R < 6.0 mA)	ΔV_{RLD}	—	20	—	mV
Line Regulation (2.0 V < V+ < 6.5 V)	ΔV_{RLN}	—	25	—	mV
V_{DD} Voltage (V+ = 4.5 V)	V_{DD}	3.0	3.3	3.8	Vdc
Load Regulation (0 < I_{DD} < 1.6 mA)					
(Dialing Mode)	ΔV_{DDLD}	—	0.25	—	Vdc
Line Regulation (All Modes) (4.0 V < V+ < 9.0 V)	ΔV_{DDLN}	—	50	—	mV
Max. Output Current (Speech Mode)	I_{DDSP}	375	550	1000	μA
Max. Output Current (Dialing Mode)	I_{DDDL}	1.6	2.0	3.6	mA
V_{DD} Leakage Current (V+ = 0, V_{DD} = 3.0 V)	I_{DDLK}		—	1.5	μA
SPEECH AMPLIFIERS					
Transmit Amplifier					
Gain (TXI to TXO)	A_{TXO}	—	20	—	V/V
TXO Bias Voltage (Speech/Pulse Mode)	V_{TXOSP}	0.45	0.52	0.60	x V_R
TXO Bias Voltage (Tone Mode Mode)	V_{TXODL}	VR−25	VR−5.0	—	mV
TXO High Voltage (Speech/Pulse Mode)	V_{TXOH}	VR−25	VR−5.0	—	mV
TXO Low Voltage (Speech/Pulse Mode)	V_{TXOL}	—	125	250	mV
TXI Input Resistance	R_{TXI}	—	10	—	kΩ
Receive Amplifier					
RXO Bias Voltage (All Modes)	V_{RXO}	0.45	0.52	0.60	x VR
RXO Source Current (Speech Mode)	I_{RXOSP}	1.5	2.0	—	mA
RXO Source Current (Pulse/Tone Mode)	I_{RXODL}	200	400	—	μA
RXO High Voltage (All Modes)	V_{RXOH}	VR−100	VR−50	—	mV
RXO Low Voltage (All Modes)	V_{RXOL}	—	50	150	mV

ELECTRICAL CHARACTERISTICS — (continued) (T_A = 25°C)

Parameter	Symbol	Min	Typ	Max	Units
MICROPHONE, RECEIVER CONTROLS					
MIC Saturation Voltage (Speech Mode, I = 500 μA)	$V_{OL_{MIC}}$	—	50	125	mV
MIC Leakage Current (Dialing Mode, Pin 1 = 3.0 V)	$I_{MIC_{LK}}$	—	0	5.0	μA
RMT Resistance (Speech Mode) (Dialing Mode)	$R_{RMT_{SP}}$ $R_{RMT_{DL}}$	— 5.0	8.0 10	15 18	Ω kΩ
RMT Delay (Dialing to Speech)	t_{RMT}	2.0	4.0	20	ms
DIALING INTERFACE					
$\overline{MT}$ Input Resistance	R_{MT}	58	100	—	kΩ
$\overline{MT}$ Input High Voltage	V_{IHMT}	$V_{DD}-0.3$	—	—	Vdc
$\overline{MT}$ Input Low Voltage	V_{ILMT}	—	—	1.0	Vdc
MS Input Resistance	R_{MS}	280	600	—	kΩ
MS Input High Voltage	V_{IHMS}	2.0	—	—	Vdc
MS Input Low Voltage	V_{ILMS}	—	—	0.3	Vdc
TI Input Resistance	R_{TI}	—	1.25	—	kΩ
DTMF Gain (See Figure 2) ($V+/V_{in}$)	A_{DTMF}	3.2	4.8	6.2	dB
SIDETONE AMPLIFIER					
Gain (TXO to STA)	A_{STA}				dB
(Speech Mode) @ V_{LR} = 0.5 V		—	−15	—	
(Speech Mode) @ V_{LR} = 2.5 V		—	−21	—	
(Pulse Mode) @ V_{LR} = 0.2 V		—	−15	—	
(Pulse Mode) @ V_{LR} = 1.0 V		—	−21	—	
STA Bias Voltage (All Modes)	V_{STA}	0.65	0.8	0.9	x V_R
EQUALIZATION AMPLIFIER					
Gain (V+ to EQ)	A_{EQ}				dB
(Speech Mode) @ V_{LR} = 0.5 V		—	−12	—	
(Speech Mode) @ V_{LR} = 2.5 V		—	−2.5	—	
(Pulse Mode) @ V_{LR} = 0.2 V		—	−12	—	
(Pulse Mode) @ V_{LR} = 1.0 V		—	−2.5	—	
EQ Bias Voltage	V_{EQ}				Vdc
(Speech Mode) @ V_{LR} = 0.5 V		—	0.66	—	
(Pulse Mode) @ V_{LR} = 0.5 V		—	1.3	—	
(Speech, Pulse) @ V_{LR} = 2.5 V		—	3.3	—	

NOTE: Typical values are not tested or guaranteed.

FIGURE 2 — DTMF DRIVER TEST



SYSTEM SPECIFICATIONS (T_A = 25°C) (See Figures 1–4)

Parameter		Min	Typ	Max	Unit
Tip-Ring Voltage (including polarity guard bridge drop of 1.4 V)					Vdc
(Speech Mode)	I_{loop} = 5.0 mA	—	2.4	—	
	I_{loop} = 10 mA	—	3.9	—	
	I_{loop} = 20 mA	—	4.6	—	
	I_{loop} = 40 mA	—	5.6	—	
	I_{loop} = 60 mA	—	6.6	—	
Transmit					
Gain from V_S to V+ (Figure 3) (I_{loop} = 20 mA)		28	30	31	dB
Gain change as I_{loop} is increased to 60 mA		−6.0	−4.5	−3.6	dB
Distortion		—	2.0	—	%
Output noise		—	11	—	dBrnc
Receive					
V_{RXO}/V_S (f = 1.0 kHz, I_{loop} = 20 mA) (See Figure 4)		−16	−15	−13	dB
Receive gain change as I_{loop} is increased to 60 mA		−5.0	−3.0	−2.0	dB
Distortion		—	2.0	—	%
Sidetone Level					dB
$V_{RXO}/V+$ (Figure 3)					
	I_{loop} = 20 mA	—	−36	—	
	I_{loop} = 60 mA	—	−21	—	
Sidetone Cancellation $\left[\frac{V_{RXO}}{V+}\text{ (Figure 4)}\right]$ dB − $\left[\frac{V_{RXO}}{V+}\text{ (Figure 3)}\right]$ dB	I_{loop} = 20 mA	20	26	—	dB
DTMF Driver		3.2	4.8	6.2	dB
$V+/V_{in}$ (Figure 2)	I_{loop} = 20 mA				
AC Impedance					Ω
Speech mode (incl. C_6, See Figure 4)	I_{loop} = 20 mA	—	750	—	
Z_{ac} = (600)V+/(V_S − V+)	I_{loop} = 60 mA	—	300	—	
Tone mode (including C_6)	20 mA < I_{loop} < 60 mA	—	1650	—	

NOTE: Typicals are not tested or guaranteed.

FIGURE 3 — TRANSMIT AND SIDETONE LEVEL TEST

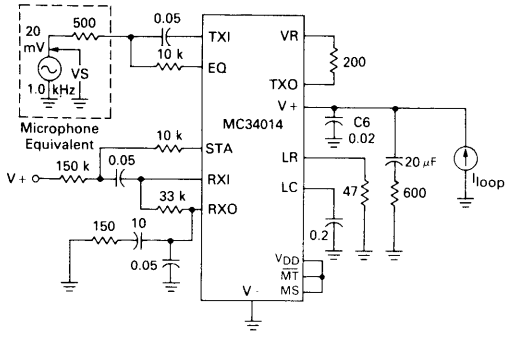
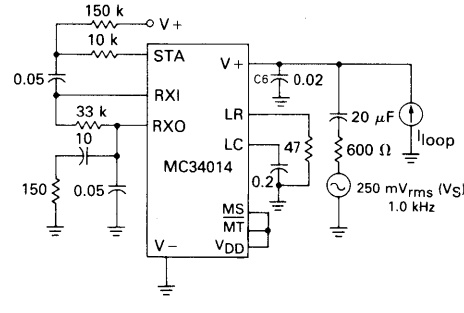


FIGURE 4 — AC IMPEDANCE, RECEIVE AND SIDETONE CANCELLATION TEST



DESIGN GUIDELINES (Refer to Figure 1)

INTRODUCTION

The MC34014 is a speech network meant for connection to the Tip & Ring lines through a polarity guard bridge. The circuit incorporates four amplifiers: transmit, receive, sidetone, and equalization. Some parameters of each amplifier are set by external components, and in addition, the gains of the sidetone and equalization amplifiers vary with loop current.

The line interface portion determines the dc voltage versus loop current characteristics, and provides the required regulated voltages for internal and external use.

The dialer interface provides three modes of operation: speech (non-dialing), pulse dialing, and tone (DTMF) dialing. When switching to either dialing mode some parameters of the various sections are changed in order to optimize the circuit operation for that mode. The following table summarizes those changes:

TABLE 1 — OPERATING PARAMETERS AS A FUNCTION OF OPERATING MODE

Function	Speech	Pulse	Tone
LR Level Shift ($V+ - V_{LR}$)	2.7 V	2.7 V	4.3 V
V_{DD} Source Current	550 μA	2.0 mA	2.0 mA
Transmit Amplifier	Functional	Functional	Inoperative
MIC Switch (Pin 1)	On	Off	Off
Equalization Amplifier	See Transfer Curves — Figure 8		
Sidetone Amplifier	See Transfer Curves — Figure 6		
Receive Amplifier Output Current	2.5 mA	400 μA	400 μA
RMT (Pin 9) Impedance	8.0 Ω	10 kΩ	10 kΩ
DTMF Amplifier	Inoperative	Inoperative	Functional
CC Voltage	$V_{LR}/3$	V_{LR}	V_{LR}

DC LINE INTERFACE (Figure 5)

The dc line interface circuit (Pins 10, 12–14) sets the dc voltage characteristics with respect to the loop current. The loop current enters at Pin 14 where the internal circuitry of the MC34014 draws 5–6 mA. Pin 3 sinks (typically) 3 mA through R_9. The remainder of the loop current is passed through Q_{301} and R_5. The resulting voltage across the entire circuit is therefore equal to the voltage across R_5, plus the level shift voltage from Pin 13 (LR) to Pin 14 (V+), nominally 2.7 volts in the speech and pulse modes. In the tone mode, the level shift increases to 4.3 volts, the internal current changes slightly (Figure 6), and the current required at Pin 3 decreases to near zero. These changes increase the equivalent dc resistance of the circuit, raising the voltage at V+ to ensure adequate voltage at V_{DD} for the external tone dialer. See Figure 7 for typical voltage versus loop current characteristics.

Capacitor C_7 at Pin 12 provides high frequency rolloff (above 10 Hz) so that R_5 does not load down the speech and DTMF signals.

The voltage at V_R is an internally regulated 1.2 volt supply which provides the bias currents for the microphone and the transmit amplifier output (Pin 3), as well as internal bias for the various amplifiers. Capacitor C_8 stabilizes the regulator. The use of an (internal) PNP transistor allows V_R to be regulated with a V+ voltage as low as 1.5 volts.

FIGURE 5 — DC LINE INTERFACE

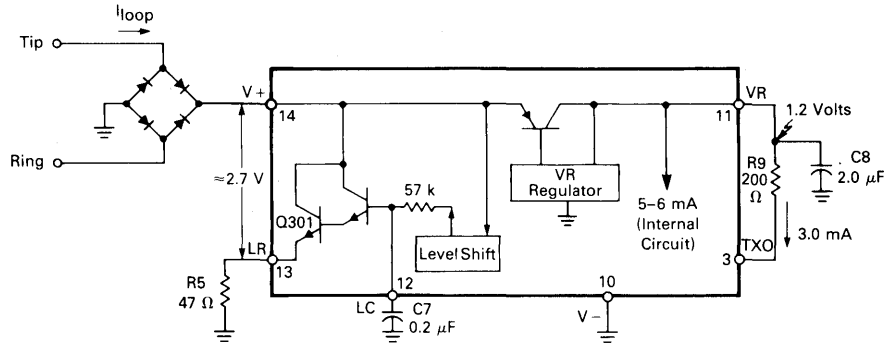


FIGURE 6 — INTERNAL CURRENT versus VOLTAGE

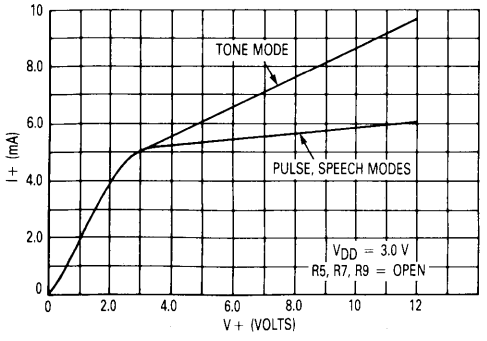
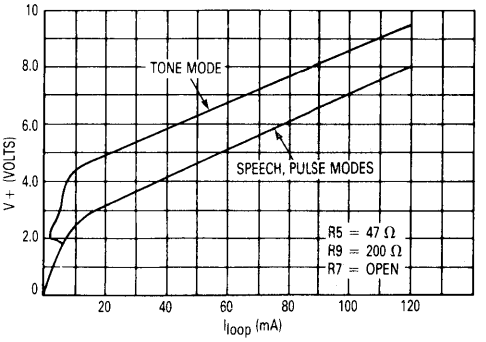


FIGURE 7 — CIRCUIT VOLTAGE versus LOOP CURRENT



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TRANSMIT AMPLIFIER

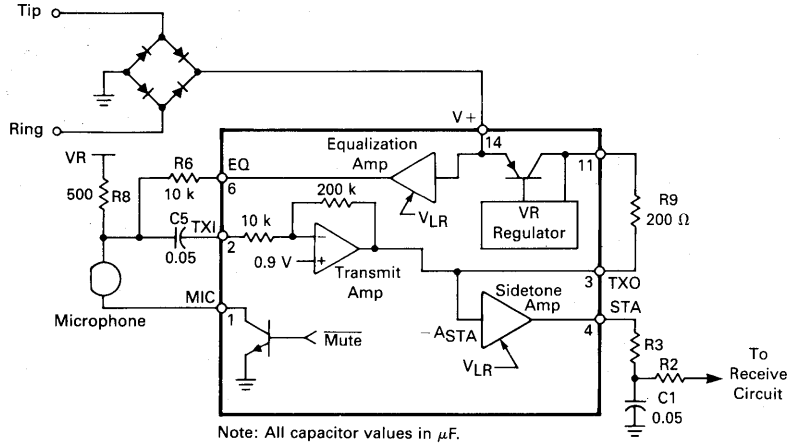
The transmit amplifier (from TXI to TXO) is inverting, with a fixed internal gain of 20 V/V (26 dB), and a typical input impedance of 10 kΩ (Figure 8). The input bias currents are internally supplied, allowing capacitive coupling of the microphone signals to the amplifier.

In the speech and pulse modes, the dc bias level at TXO is typically 0.52 x VR (≈0.63 V), which permits the output to swing 0.55 volts in both positive and negative directions without clipping. The ac voltage signal at TXO (the amplified speech signal) is converted to an ac current by R_g. The ac current passes through the VR series pass transistor to V+, modulating the loop current. The voltage signal at V+ is out of phase with the signal at TXI.

In the tone dialing mode, the TXO dc bias level is clamped at approximately VR-10 mV, rendering the amplifier inoperative. This action also reduces the TXO bias current from 3.0 mA to less than 125 μA.

MIC (Pin 1) is connected to an open-collector NPN transistor, and provides the ground path for the microphone bias current. In either dialing mode, the transistor is off, disabling the microphone.

FIGURE 8 — TRANSMIT SECTION



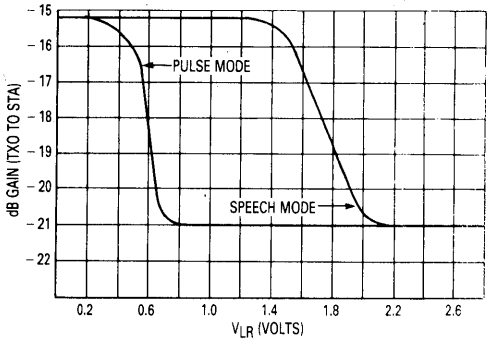
Note: All capacitor values in μF.

SIDETONE AMPLIFIER

The sidetone amplifier provides inversion of the TXO signal for the reduction of the sidetone signal at the receive amplifier (Figure 8). Resistors R_2 and R_3 determine the amount of sidetone cancellation. Capacitor C_1 provides phase shift to compensate for the phase shift created by the complex impedance of the Tip & Ring lines.

The gain of the sidetone amplifier varies with the voltage at LR (Pin 13), in effect making it a function of the loop current. The maximum gain is −15 dB (0.17 V/V) at low loop currents, and the minimum gain is −21 dB (0.09 V/V) at high loop current (see Figure 9 for transfer curves). For example, using 47 Ω for R_5, the gain would begin to decrease at ≈30 mA, and would stop decreasing at ≈57 mA (speech mode). The dc bias voltage at STA (Pin 4) changes slightly (≈50 mV) with variations in loop current. The output is inverted from TXO, which is the input to this amplifier. Since the transmit amplifier is inoperative in the tone dialing mode, the sidetone amplifier is also inoperative in that mode.

FIGURE 9 — SIDETONE AMPLIFIER GAIN



RECEIVE AMPLIFIER

The gain of the receive amplifier (from V+ to RXO) is determined according to the following equation (refer to Figure 10):

$$\frac{V_{RXO}}{V+} = \frac{R_4}{R_1} + \frac{(X_C//R_2)\,(A_{EQ})\,(A_{TXO})\,(A_{STA})\times R_A \times R_4}{((X_C//R_2)+R_3)\,(R_A+R_6)\times R_2}$$

Where $R_A = R_8//10\ k\Omega$ (10 kΩ = R_{in} of T_x Amp)
A_{EQ} = Gain of Equalization Amp
A_{TXO} = Gain of Transmit Amp (20 V/V)
A_{STA} = Gain of sidetone Amp
X_C = Impedance of C_1 at frequency of interest

The waveform at STA (Pin 4) is in phase with that at V+ (for receive signals), hence the plus sign between the terms. Due to the variations of A_{EQ} and A_{STA} with loop current, the receive gain will vary by ≈1.5 dB. If capacitor C_1 is not used, the above equation is simplified by deleting the terms containing X_C.

The output at RXO is inverted from V+ in the receive mode. In the transmit mode, the V+-to-RXO phase relationship depends on the amount of sidetone cancellation (determined by R_2 and R_3 and C_1), and can vary from 0° to 180°.

In the speech mode, the output current capability (at RXO) is typically 2.0 mA. In either dialing mode, the current capability is reduced to 400 μA in order to reduce internal current consumption. This feature is beneficial when this device is used in conjunction with a line-powered speakerphone circuit, such as the MC34018, where the majority of the loop current is needed for the speakerphone.

RMT (Pin 9) is the return path for the receiver's ac current. This pin is internally connected to an open collector NPN transistor, paralleled by a 10 kΩ resistor. In the speech mode, the transistor is on, providing a low impedance from RMT to ground. In either dialing mode, the transistor is off, muting the receive signal. This prevents loud "clicks" or loud DTMF tones from being heard in the receiver during dialing. When switching from either dialing mode to the speech mode ($\overline{MT}$ switches from low to high), the RMT pin switches back to a low impedance after a delay of 2–20 ms. The delay reduces clicks in the receiver associated with switching from the dialing to speech mode.

EQUILIZATION AMPLIFIER

The equalization amplifier gain varies with loop current, and is configured in the circuit so as to cause a variation of the network ac impedance (when looking in from the Tip & Ring lines). The gain varies with the voltage at LR (Pin 13), in effect making it a function of the loop current. The maximum gain is −2.5 dB (0.75 V/V) at high loop current, and the minimum gain is −12 dB (0.25 V/V) and low loop current (see Figure 11 for transfer curve). For example, using 47 Ω for R_5, the gain would begin to increase at ≈30 mA, and would stop increasing at ≈57 mA (speech mode). The output signal is in phase with the signal at V+, which is the input to this amplifier.

The dc bias level at EQ (Pin 6) varies with the voltage at LR (Pin 13) according to the curve of Figure 12. In most applications, this level shift is of little consequence, and may be ignored. If a particular circuit configuration should be sensitive to the shift, however, the output signal at EQ may be ac coupled to the rest of the circuit.

The equalization amplifier remains functional in all three modes, although in the tone mode, its function has no consequence when the circuit is configured as shown in Figure 1.

V_{DD} REGULATOR

The V_{DD} regulator is a shunt type regulator which supplies a nominal 3.3 volts for external dialers, and/or

other circuitry. In the speech mode, the output current capability at Pin 15 is typically 550 μA. In either dialing mode, the current capacity is increased to 2.0 mA.

V_{DD} will be regulated whenever V+ is >300 mV above the regulated value. As V+ is lowered, and the internal pass transistor becomes saturated, the circuit steers current away from the external load through an internal current source, in order that the V_{DD} capacitor (C9) does not load down speech and DTMF signals at V+. As V+ is lowered below 1 volt, Pin 15 switches to a high impedance state to prevent discharging of any storage capacitors, or batteries used for memory retention.

The V_{DD} voltage is unaffected by the choice of operating mode.

DIALER INTERFACE

The dialer interface consists of the mode control pins, $\overline{MT}$ and MS (Pins 18 and 17), and the DTMF current amplifier.

The $\overline{MT}$ pin, when at a Logic "1" ($> V_{DD} - 0.3$ V), sets the circuit into the speech mode, independent of the state of the MS pin. When the $\overline{MT}$ pin is at a Logic "0" (< 1.0 V), the dialing mode is determined by the MS pin. When MS is at a Logic "1" (> 2.0 V), the circuit is in the pulse dialing mode, and when at a Logic "0" (< 0.3 V) the tone (DTMF) mode is in effect.

The input impedance of the $\overline{MT}$ pin is typically 100 kΩ, with the input current flowing out of the pin (from V_{DD}). The input impedance of the MS pin is typically 600 kΩ, and the input current flows into the pin (Figure 1).

The DTMF amplifier (Figure 13) is a current amplifier which transmits DTMF signals to the V+ pin, and consequently onto the Tip & Ring lines. Waveforms from a DTMF dialer are input at TI (Pin 16) through a current limiting resistor (R_7). Negative feedback around the amplifier reduces the overall gain so that return loss specifications may be met. The voltage gain is calculated using the following equation:

$$\frac{V+}{V_i} = \frac{80\ R_E}{(1\ +\ 0.795R_7\ +\ 0.4R_ER_7)}$$

(R_E, R_7 in kΩ)
where $R_E = R_L//2$ kΩ (2 kΩ = internal dynamic impedance)

Using 22 kΩ for R_7, and 600 Ω for R_L, the voltage gain is a nominal 4.3 dB. The minimum loop current at which the circuit of Figure 1 will operate without distortion is 12 mA.

The DTMF amplifier is functional only in the tone dialing mode, and the waveform at V+ is inverted from that at TI. The TI pin requires a dc bias current (into the pin) of 20–50 μA, which may be supplied by the Tone dialer circuit, or by using the biasing scheme of Figure 14.

CC (PIN 5)

The CC pin (Compensation Capacitor) has two functions: 1) to provide equalization loop stability where the normal stabilizing components are ineffective; and 2) to allow optional control of the equalization functions.

In most applications, the capacitor at LC (Pin 12) provides the required stability, and no further compensation is required. In applications where changes are forced at Pin 12 and/or 13 (e.g., see Figure 23), the LC capacitor's effectiveness may be lost. The addition of a 10 μF capacitor to Pin 5 will provide the required additional compensation.

The CC pin may be used to force the loop length compensation circuits to specific modes. Grounding CC will set the sidetone and equalization amplifiers at the low loop current values. Connecting CC to V_R will set the amplifiers at the high loop current values.

Variations in the curves of Figures 9 and 11 may be obtained by using external resistors from LR to CC, and from CC to V−.

FIGURE 10 — RECEIVE CIRCUIT

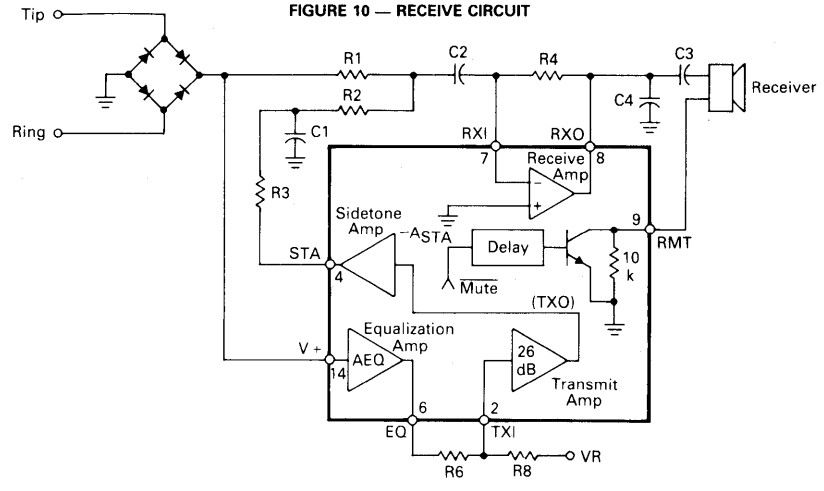


FIGURE 11 — EQUALIZATION AMPLIFIER GAIN

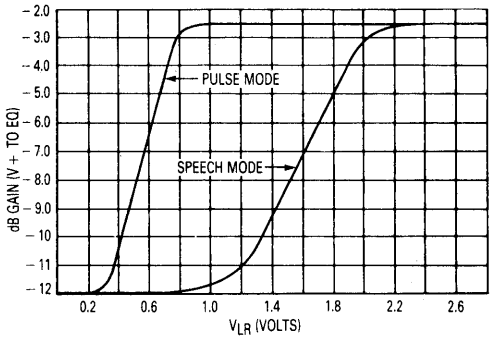


FIGURE 12 — EQ (PIN 6) DC VOLTAGE

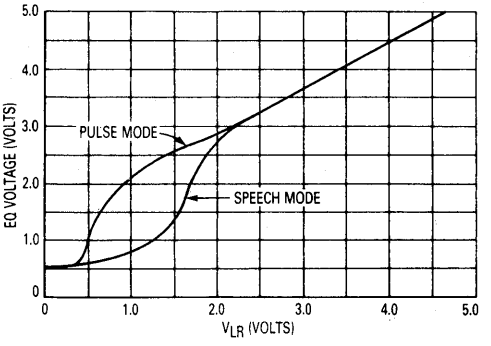


FIGURE 13 — DTMF TONE DIALER

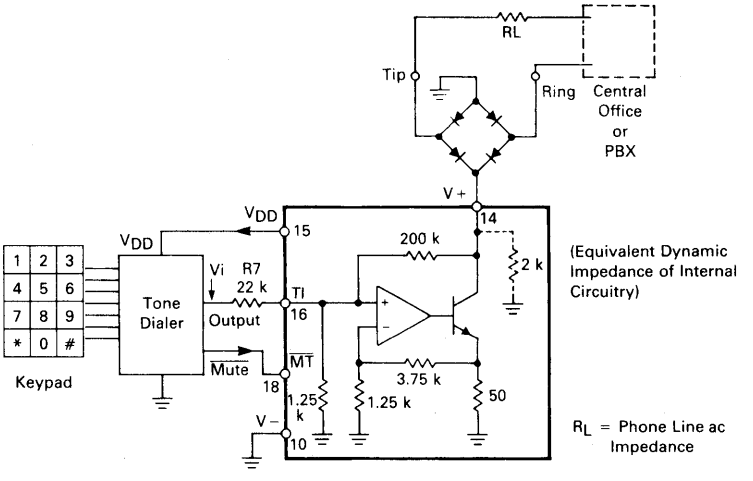
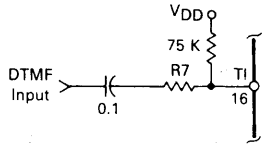


FIGURE 14 — INPUT BIASING



APPLICATIONS INFORMATION

AC IMPEDANCE

One of the basic problems with early telephones is that the performance varied with different line lengths (distance from the Central Office to the telephone). If a particular phone were optimized for short loops and then connected to a long loop, both the transmitted and receive signals would be difficult to hear. On the other hand, phones optimized for long loops would then be annoyingly loud on short loops. The process of equalization is one whereby the performance is forced to vary with loop length inversly to the expected variations. Monitoring of loop length is accomplished by monitoring the loop current at the telephone. In the MC34014, loop length equalization is provided by varying the ac impedance of the telephone circuit. In this manner the MC34014 mimics a passive network, with varistors providing the equalization.

Figure 15 depicts the situation in the receive mode. The receive signal coming from the Central Office is V_S and is independent of the loop length. Z_R is the ac impedance of the Central Office, nominally 900 Ω. Z_L is the characteristic impedance of the phone line, and is a nominal 600 Ω. The signal applied to the line (V_1) is therefore a portion of V_S. That signal is attenuated by the distributive impedance of the phone line, with a resulting signal V_2 at the telephone. The amplitude of V_2 depends on the amount of attenuation, the impedance of the phone line at the telephone and the ac impedance of the telephone (Z_{ac}), according to:

$$V_2 = \frac{V_1' \times Z_{ac}}{Z_{ac} + Z_L}$$

where V_1' is the equivalent signal source at the receive end of the phone line, providing the signal V_2 through the impedance equal to the characteristic impedance of the line (Z_L). The value of V_1' depends on how much V_1 has been attenuated by the length of phone line. By increasing Z_{ac} on long loops, V_2 is a greater portion of V_1', resulting in a stronger receive signal at the telephone.

FIGURE 15 — RECEIVE MODE

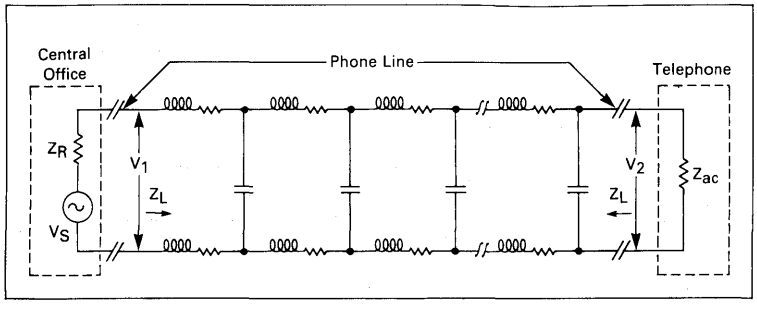
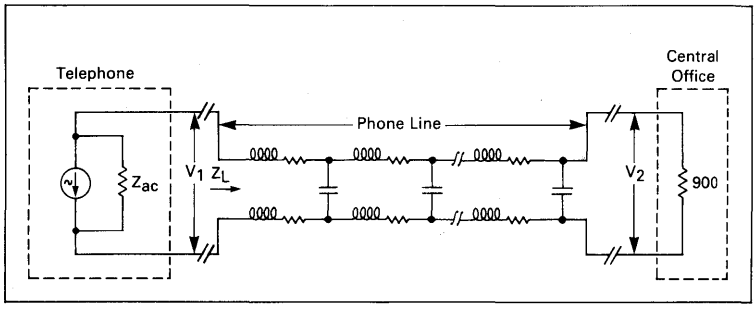


Figure 16 depicts the situation in the transmit mode. In this mode, the MC34014 is an ac current source, with a finite output impedance, modulating the loop current. The voltage signal V_1 is therefore equal to the ac signal current acting on Z_{ac} in parallel with the characteristic impedance of the phone line (Z_L). The signal is attenuated by the distributive impedance of the phone line, and so only a portion of that signal (V_2) appears at the Central Office. By increasing Z_{ac} on long loops, V_1 is increased, resulting in a higher signal level at V_2.

FIGURE 16 — TRANSMIT MODE



The ac impedance of the telephone circuit is determined by the transmit amplifier, equalization amplifier, and external resistors R_6, R_8, and R_9. In Figure 17, a portion of the receive signal at V+ appears at EQ. That signal is reduced at TXI by the R_8-R_6 divider (the electret microphone is a high impedance). The signal at TXI is then amplified by 20, and that signal (at TXO) is converted to an ac current by R9. The ac impedance of the circuit is therefore $V+/I_{TXO}$, and is defined by the following equation:

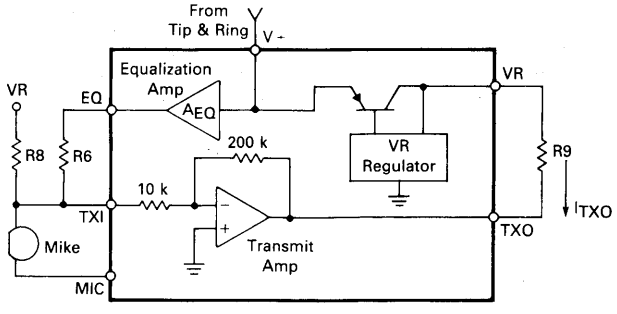
$$Z_{ac} = \frac{(1 + R_8/R_6)(R_9)}{20 \times A \times (R_8/R_6)}$$

where A = the gain of the equalization amplifier (0.25 to 0.75)

Since the gain of the equalization amplifier varies by a factor of 3, the ac impedance will vary the same amount. Using the resistor values indicated in Figure 1, the ac impedance will vary from 280 Ω (short loop) to 840 Ω (long loop).

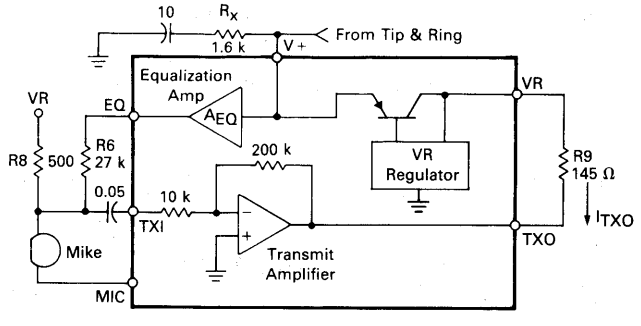
When calculating or measuring the ac impedance, capacitor C_6 (≈8.0 kΩ at 1.0 kHz) and the dynamic impedance of the MC34014 (≈10 kΩ) must be taken into account. If the microphone has an impedance lower than that of a typical electret, then its dynamic impedance must be accounted for in the above equation.

FIGURE 17 — DETERMINING AC IMPEDANCE



If a variation in Z_{ac} of less than 3:1 is desired, the circuit configuration of Figure 18 may be used. The ac impedance is the parallel combination of R_X and the impedance presented by the remainder of the circuit. With the values shown in Figure 18, the ac impedance varies from 400 Ω to 800 Ω.

FIGURE 18 — REDUCED AC IMPEDANCE VARIATION



TRANSMIT DESIGN PROCEDURE

Referring to Figure 17, first select R_9 for the desired maximum output level at Tip & Ring, assuming a signal level at TXO of 1.0 V p-p. The maximum signal level at Tip & Ring will be approximately:

$$\frac{(V_{TXO})\ (Z_L)}{R_9}$$

where Z_L is the characteristic ac impedance of the phone line. Capacitor C_6 and the ≈10 kΩ dynamic impedance of the MC34014 must also be considered in the above computation, since they are in parallel with Z_L.

The next step is to select the R_6/R_8 ratio, according to the required Z_{ac}, using the equation on the previous page. Then R_8 is selected to set the microphone sensitivity. R_8 is typically in the range of 0.5 k to 1.5 kΩ, and is dependent on the characteristics of the microphone. R_6 is then calculated from the above mentioned ratio.

HANDSET/HANDS-FREE TELEPHONE

Figure 23 indicates a circuit using the MC34014 speech network, MC34018 speakerphone circuit, and the MC34017 tone ringer to provide a complete telephone/speakerphone. Switch HS (containing one normally open and one normally closed contact) is the hook switch actuated by the handset, shown in the on-hook position. When the handset is off-hook (HS1 open, HS2 closed), power is applied to the MC34014, and consequently the handset, and the $\overline{CS}$ pin of the MC34018 is held high so as to disable it. Upon closing the two poles of switch SS, and placing switch HS in the on-hook position, power is then applied to both the MC34014 and the MC34018, and $\overline{CS}$ is held low, enabling the speakerphone function. Anytime the handset is removed from switch HS, the circuit reverts to the handset mode. The diode circuitry sets the MC34014 to the pulse dialing mode to mute the handset microphone and receiver when using the speakerphone. To compensate for the different equalization response of the MC34014 when in the pulse dialing mode (Figures 9 and 11), the 47 Ω resistor normally found at Pin 13 of the MC34014 is instead divided into two resistors (33 Ω and 15 Ω). This arrangement provides similar equalization response in both the handset and in the speakerphone modes. Since the LC capacitor (Pin 12) is ineffective in the speakerphone mode, a capacitor is added at Pin 5 (CC) to provide compensation for the equalization loop when the speakerphone mode is in effect.

FIGURE 19 — ALTERNATE MICROPHONE BIAS

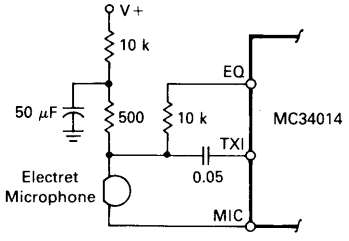
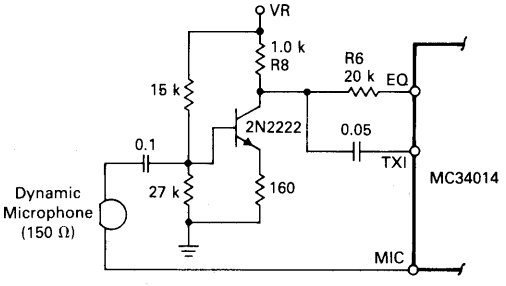


FIGURE 20 — INTERFACING A DYNAMIC MICROPHONE



The overall gain from the microphone to V+ will vary with loop current due to the influence of the equalization amplifier on TXI. The signal at EQ is out of phase with that at TXI, therefore the signal at V+ decreases as loop current (and the EQ signal) increases. Variations are typically 2.0 to 5.0 dB and depend largely on the impedance characteristics of the microphone.

ALTERNATE MICROPHONE BIASING

In the event that the microphone cannot be properly biased from the 1.2 volt VR supply, a higher voltage can be obtained by biasing from the V+ supply. The configuration shown in Figure 19, provides a higher voltage to the microphone, and also filters the speech signals at V+ from reaching it, preventing an oscillatory loop from forming. The maximum voltage limit of the microphone must be considered when biasing this way.

If a dynamic microphone is to be used in place of an electret unit, the circuit in Figure 20 will buffer its low impedance from the MC34014 circuit, maintaining the high impedance required at the junction of R_8 and R_6. The circuit shown provides a gain of ≈2.6 for the microphone signals, and can be adjusted by varying the 160 Ω resistor.

SWITCHABLE TONE/PULSE TELEPHONE

Figure 21 indicates a switchable tone/pulse telephone circuit using the MC145412 tone/pulse dialer, MC34014 speech network, and the MC34017 tone ringer. The dialer is programmable, and can store up to 10 phone numbers. As can be seen, the interface to the MC34014 is straightforward.

PULSE ONLY TELEPHONE

Figure 22 indicates a pulse only telephone circuit using the MC145409 pulse dialer, MC34014 speech network, and the MC34017 tone ringer. The dialer has last number redial, and provides a pacifier tone to the receiver during dialing.

FIGURE 21 — COMPLETE TELEPHONE WITH PULSE/TONE DIALING

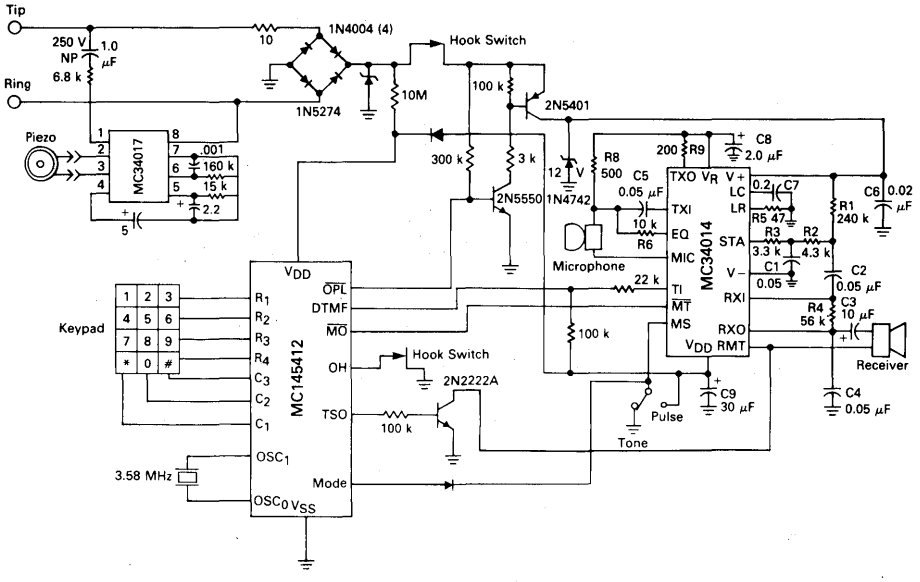


FIGURE 22 — COMPLETE TELEPHONE WITH PULSE DIALING

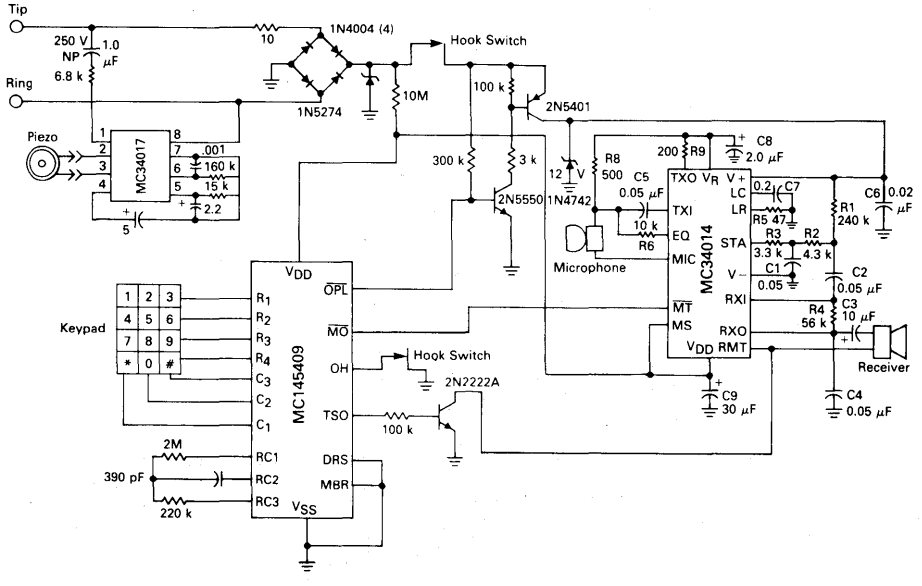
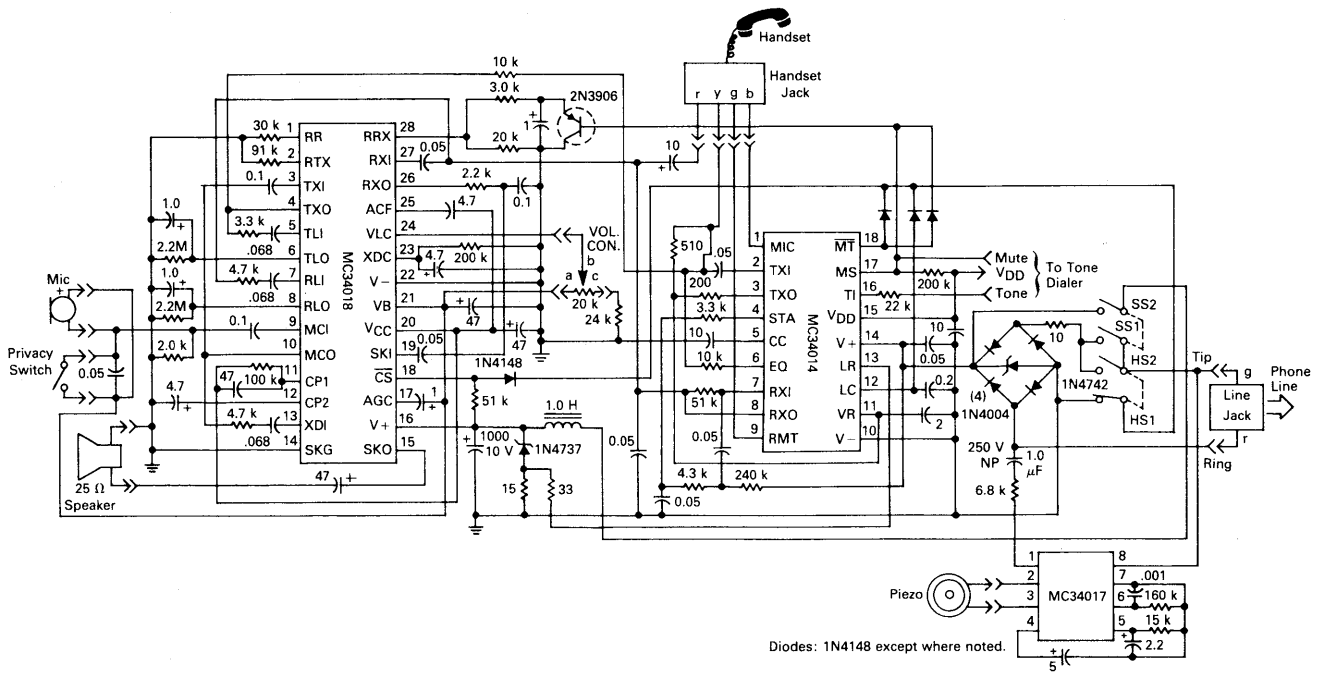


FIGURE 23 — SWITCHABLE HANDSET/HANDSFREE SYSTEM



Recommended External Components

Piezo Sounder
Models KSN 1113-1116
Motorola, Inc.
Albuquerque, N.M.
505-822-8801

Microhone/Receiver
Microphone model EM-95
Receiver model DH-34
Primo Microphone, Inc.
Elk Grove Village, Ill.
312-595-1022

Microphone Model KUC2123
Hosiden Electronics
Chicago, Ill.
312-956-7707

2

TRANSIENT PROTECTION & RFI SUPPRESSION

Protection from voltage transients is necessary in most telephone circuits, and may take the form of zener diodes, RC or LC filters, transient suppressors (MO•sorb), or a combination of the above.

Potential radio frequency interference problems should be addressed early in the electrical and mechanical design of the telephone. RFI may enter the circuitry through the Tip & Ring lines, through the microphone and/or receiver leads in the handset cord, or through any of the wiring or PC board traces. Ceramic decoupling capacitors, ferrite beads, and other RFI suppression techniques may be needed. Good PC board design techniques, such as the avoidance of loops, should be used. Long tracks on high impedance nodes should be avoided.

MOTOROLA

MC34017

Advance Information

TELEPHONE TONE RINGER

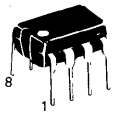
- Complete Telephone Bell Replacement Circuit with Minimum External Components
- On-Chip Diode Bridge and Transient Protection
- Direct Drive for Piezoelectric Transducers
- Push Pull Output Stage for Greater Output Power Capability
- Base Frequency Options — MC34017-1: 1.0 kHz
  MC34017-2: 2.0 kHz
  MC34017-3: 500 Hz
- Input Impedance Signature Meets Bell and EIA Standards
- Rejects Rotary Dial Transients

TELEPHONE TONE RINGER

BIPOLAR LINEAR/I^2L

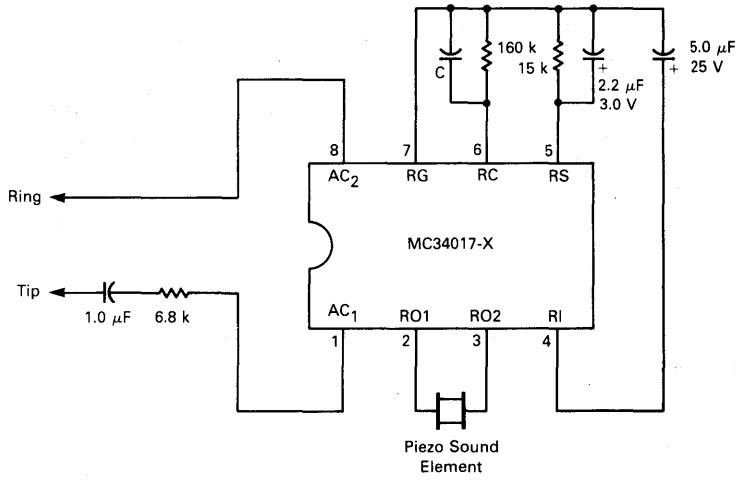
2

N SUFFIX
PLASTIC PACKAGE
CASE 626-04



D SUFFIX
PLASTIC PACKAGE
CASE 751-01
SO-8

APPLICATION CIRCUIT



MC34017-1: C = 1000 pF
MC34017-2: C = 500 pF
MC34017-3: C = 2000 pF

This document contains information on a new product. Specifications and information herein are subject to change without notice.

APPLICATION CIRCUIT PERFORMANCE (Refer to Circuit on First Page.)

Characteristic	Typical Value	Units
Output Tone Frequencies MC34017-1 MC34017-2 MC34017-3 Warble Frequency	 808/1010 1616/2020 404/505 12.5	Hz
Output Voltage ($V_I \geq 60\ V_{rms}$, 20 Hz)	37	V_{p-p}
Output Duty Cycle	50	%
Ringing Start Input Voltage (20 Hz)	36	V_{rms}
Ringing Stop Input Voltage (20 Hz)	21	V_{rms}
Maximum ac Input Voltage (≤ 68 Hz)	150	V_{rms}
Impedance When Ringing $V_I = 40\ V_{rms}$, 15 Hz $V_I = 130\ V_{rms}$, 23 Hz	 >16 12	kΩ
Impedance When Not Ringing $V_I = 10\ V_{rms}$, 24 Hz $V_I = 2.5\ V_{rms}$, 24 Hz $V_I = 10\ V_{rms}$, 5.0 Hz $V_I = 3.0\ V_{rms}$, 200–3200 Hz	 28 >1.0 55 >200	 kΩ MΩ kΩ kΩ
Maximum Transient Input Voltage (T ≤ 2.0 ms)	1500	V
Ringer Equivalence: Class A Class B	0.5 0.9	— —

PIN DESCRIPTIONS

Name	Description
AC_1, AC_2	The input terminals to the full-wave diode bridge. The ac ringing signal from the telephone line energizes the ringer through this bridge.
RS	The input of the threshold comparator to which diode bridge current is mirrored and sensed through an external resistor (R3). Nominal threshold is 1.2 volts. This pin internally clamps at 1.5 volts.
RI	The positive supply terminal for the oscillator, frequency divider and output buffer circuits.
RO1, RO2	The tone ringer output terminals through which the sound element is driven.
RG	The negative terminal of the diode bridge and the negative supply terminal of the tone generating circuitry.
RC	The oscillator terminal for the external resistor and capacitor which control the tone ringer frequencies (R2, C2).

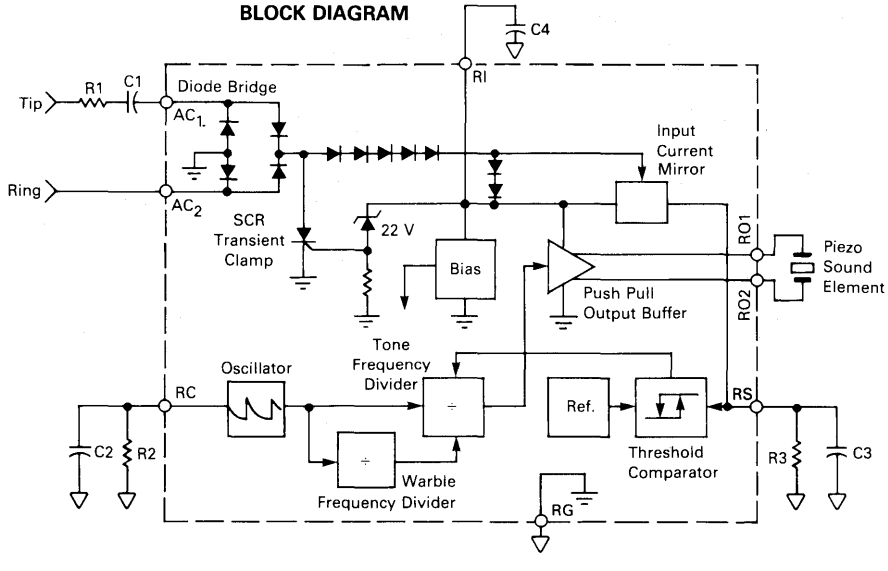
MAXIMUM RATINGS (Voltages Referenced to RG, Pin 7)

Parameter	Value	Unit
Operating AC Input Current (Pins 1, 8)	20	mA, RMS
Transient Input Current (Pins 1, 8) (T<2.0 ms)	±300	mA, peak
Voltage Applied at RC (Pin 6)	5.0	V
Voltage Applied at RS (Pin 5)	5.0	V
Voltage Applied to Outputs (Pins 2, 3)	−2.0 to V_{RI}	V
Power Dissipation (@ 25°C)	1.0	W
Operating Temperature Range	−20 to +60	°C
Storage Temperature Range	−65 to +150	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C)

Characteristic	Test	Symbol	Min	Typ	Max	Units
Ringing Start Voltage (V_{Start} = V_I @ Ring Start)						Vdc
V_I>0	1a	$V_{Start}(+)$	34	37.5	41	
V_I<0	1b	$V_{Start}(-)$	−34	−37.5	−41	
Ringing Stop Voltage (V_{Stop} = V_I @ Ring Stop)	1c	V_{Stop}				Vdc
MC34017-1			14	16	22	
MC34017-2			12	14	20	
MC34017-3			14	16	22	
Output Frequencies (V_I = 50 V)	1d					Hz
MC34017-1 High Tone		f_H	937	1010	1083	
Low Tone		f_L	752	808	868	
Warble Tone		f_W	11.5	12.5	14	
MC34017-2 High Tone		f_H	1874	2020	2166	
Low Tone		f_L	1504	1616	1736	
Warble Tone		f_W	11.5	12.5	14	
MC34017-3 High Tone		f_H	937	1010	1083	
Low Tone		f_L	752	808	868	
Warble Tone		f_W	23	25	28	
Output Voltage (V_I = 50 V)	6	V_O	34	37	43	V_{p-p}
Output Short-Circuit Current	2	I_{RO1}, I_{RO2}	35	60	80	mA_{p-p}
Input Diode Voltage (I_I = 5.0 mA)	3	V_D	5.4	6.2	6.8	Vdc
Input Voltage — SCR Off (I_I = 30 mA)	4a	V_{off}	25	33	43	Vdc
Input Voltage — SCR On (I_I = 100 mA)	4b	V_{on}	3.2	4.1	6.0	Vdc
RS Clamp Voltage (V_I = 50 V)	5	V_{clamp}	1.3	1.5	1.8	Vdc

BLOCK DIAGRAM



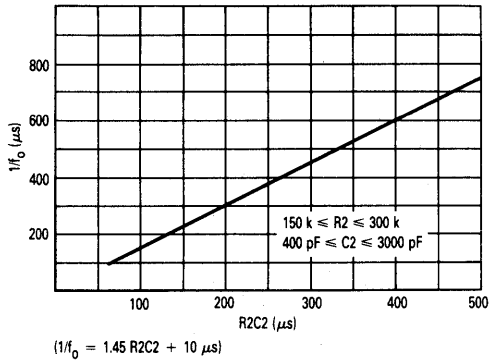
CIRCUIT DESCRIPTION

The MC34017 Tone Ringer derives its power supply by rectifying the ac ringing signal. It uses this power to activate a tone generator and drive a piezo-ceramic transducer. The tone generation circuitry includes a relaxation oscillator and frequency dividers which produce high and low frequency tones as well as the tone warble frequency. The relaxation oscillator frequency f_o is set by resistor R2 and capacitor C2 connected to pin RC. The oscillator will operate with f_o from 1.0 kHz to 10 kHz with the proper choice of external components (See Figure 1).

The frequency of the tone ringer output signal at RO1 and RO2 alternates between $f_o/4$ to $f_o/5$. The warble rate at which the frequency changes is $f_o/320$ for the MC34017-1, $f_o/640$ for the MC34017-2, and $f_o/160$ for the MC34017-3. With a 4.0 kHz oscillator frequency, the MC34017-1 produces 800 Hz and 1000 Hz tones with a 12.5 Hz warble rate. The MC34017-2 generates 1600 Hz and 2000 Hz tones with a similar 12.5 Hz warble frequency from an 8.0 kHz oscillator frequency. The MC34017-3 will produce 400 Hz and 500 Hz tones with a 12.5 Hz warble rate from a 2.0 kHz oscillator frequency. The tone ringer output circuit can source or sink 20 mA with an output voltage swing of 37 volts peak-to-peak. Volume control is readily implemented by adding a variable resistance in series with the piezo transducer.

Input signal detection circuitry activates the tone ringer output when the ac line voltage exceeds programmed threshold level. Resistor R3 determines the ringing signal amplitude at which an output signal at RO1 and RO2 will be generated. The ac ringing signal is rectified by the internal diode bridge. The rectified input signal produces a voltage across R3 which is referenced to RG. The voltage across resistor R3 is filtered by capacitor C3 at the input to the threshold circuit.

FIGURE 1 — OSCILLATOR PERIOD ($1/f_o$) versus OSCILLATOR R2 C2 PRODUCT



($1/f_o$ = 1.45 R2C2 + 10 μs)

When the voltage on capacitor C3 exceeds 1.2 volts, the threshold comparator enables the tone ringer output. Line transients produced by pulse dialing telephones do not charge capacitor C3 sufficiently to activate the tone ringer output.

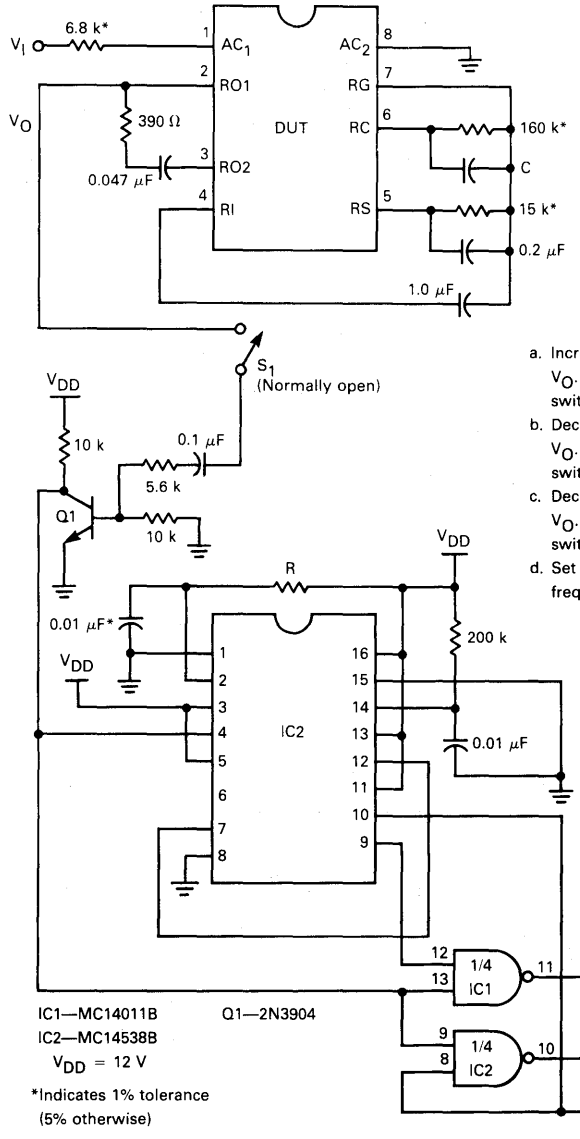
Capacitors C1 and C4 and resistor R1 determine the 10 volt, 24 Hz signature test impedance. C4 also provides filtering for the output stage power supply to prevent droop in the square wave output signal. Six diodes in series with the rectifying bridge provide the necessary non-linearity for the 2.5 volt, 24 Hz signature tests.

An internal shunt voltge regulator between the RI and RG terminals provides dc voltage to power output stage, oscillator, and frequency dividers. The dc voltage at RI is limited to approximately 22 volts in regulation. To protect the IC from telephone line transients, an SCR is triggered when the regulator current exceeds 50 mA. The SCR diverts current from the shunt regulator and reduces the power dissipation within the IC.

EXTERNAL COMPONENTS

R1	Line input resistor. R1 affects the tone ringer input impedance. It also influences ringing threshold voltage and limits current from line transients. (Range: 2.0 kΩ to 10 kΩ).
C1	Line input capacitor. C1 ac couples the tone ringer to the telephone line and controls ringer input impedance at low frequencies. (Range: 0.4 μF to 2.0 μF).
R2	Oscillator resistor. (Range: 150 kΩ to 300 kΩ).
C2	Oscillator capacitor. (Range: 400 pF to 3000 pF).
R3	Input current sense resistor. R3 controls the ringing threshold voltage. Increasing R3 decreases the ring-start voltage. (Range: 5.0 kΩ to 18 kΩ).
C3	Ringing threshold filter capacitor. C3 filters the ac voltage across R3 at the input of the ringing threshold comparator. It also provides dialer transient rejection. (Range: 0.5 μF to 5.0 μF).
C4	Ringer supply capacitor. C4 filters supply voltage for the tone generating circuits. It also provides an ac current path for the 10 V_{rms} ringer signature impedance. (Range: 1.0 μF to 10 μF).

FIGURE 2 — TEST ONE

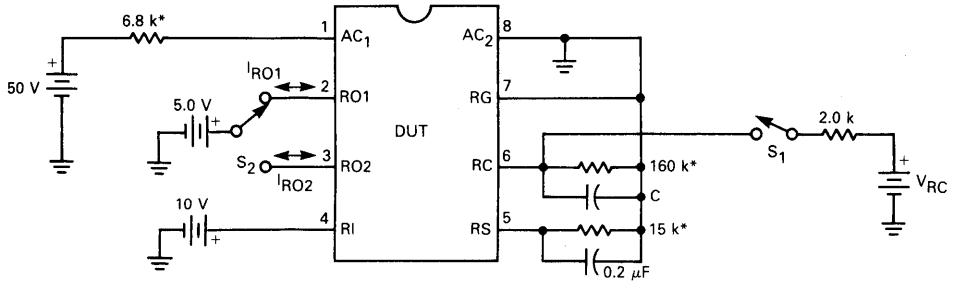


MC34017-1: C = 1000 pF*
MC34017-2: C = 500 pF*
MC34017-3: C = 1000 pF*

a. Increase V_I from +33 volts while monitoring V_O. $V_{Start}(+)$ equals V_I when V_O commences switching.
b. Decrease V_I from −33 volts while monitoring V_O. $V_{Start}(-)$ equals V_I when V_O commences switching.
c. Decrease V_I from +40 volts while monitoring V_O. V_{Stop} equals V_I when V_O ceases switching.
d. Set V_I to +50 volts. Close S1. Measure frequencies f_H, f_L, and f_W.

MC34017-1: R = 110 kΩ*
MC34017-2: R = 55 kΩ*
MC34017-3: R = 110 kΩ*

FIGURE 3 — TEST TWO



With V_{RC} = 4.0 volts, close S_1. Switch S_2 to Pin 2 and measure current at Pin 2 (Io1). Repeatedly switch V_{RC} between 4.0 volts and 0 volts until Pin 2 current changes polarity. Measure the opposite polarity current (Io2). Calculate:

$I_{RO1} = |Io1| + |Io2|$

Switch S2 to Pin 3 and repeat.

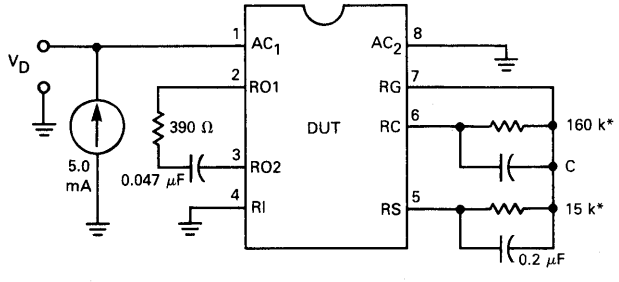
Calculate:

$I_{RO2} = |Io1| + |Io2|$

MC34017-1: C = 1000 pF*
MC34017-2: C = 500 pF*
MC34017-3: C = 1000 pF*

*Indicates 1% tolerance (5% otherwise)

FIGURE 4 — TEST THREE

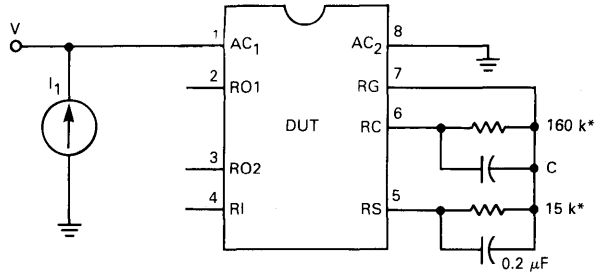


Measure voltage at Pin 1.

MC34017-1: C = 1000 pF*
MC34017-2: C = 500 pF*
MC34017-3: C = 1000 pF*

*Indicates 1% tolerance (5% otherwise)

FIGURE 5 — TEST FOUR



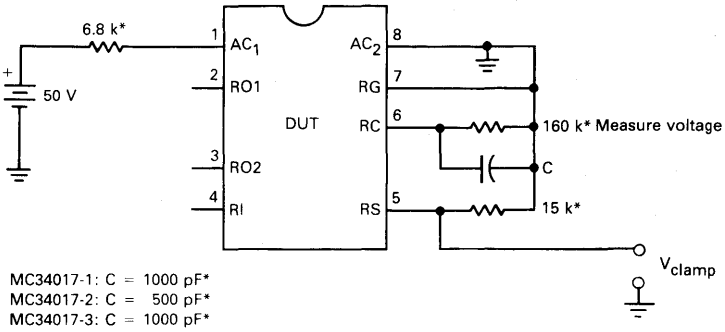
MC34017-1: C = 1000 pF*
MC34017-2: C = 500 pF*
MC34017-3: C = 1000 pF*

*Indicates 1% tolerance (5% otherwise)

a. Set I_I to 30 mA. Measure voltage at Pin 1 (V_{off}).
b. Set I_I to 100 mA. Measure voltage at Pin 1 (V_{on}).

(Each test < 30 ms)

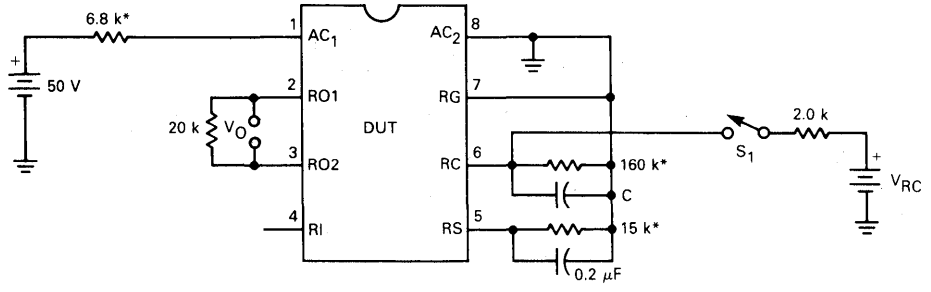
FIGURE 6 — TEST FIVE



MC34017-1: C = 1000 pF*
MC34017-2: C = 500 pF*
MC34017-3: C = 1000 pF*

*Indicates 1% tolerance (5% otherwise)

FIGURE 7 — TEST SIX



MC34017-1: C = 1000 pF*
MC34017-2: C = 500 pF*
MC34017-3: C = 1000 pF*

*Indicates 1% tolerance (5% otherwise)

With V_{RC} = 4.0 volts, close S_1. Measure dc voltage between Pins 2 and 3 (Vo1). Repeatedly switch V_{RC} between 4.0 volts and 0 volts until Pins 2 and 3 change state. Measure the new voltage between Pins 2 and 3 (Vo2).
Calculate:
$V_o = |Vo1| + |Vo2|$

MOTOROLA

MC34018

Specifications and Applications Information

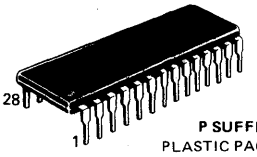
VOICE SWITCHED SPEAKERPHONE CIRCUIT

The MC34018 Speakerphone integrated circuit incorporates the necessary amplifiers, attenuators, and control functions to produce a high quality hands-free speakerphone system. Included are a microphone amplifier, a power audio amplifier for the speaker, transmit and receive attenuators, a monitoring system for background sound level, and an attenuation control system which responds to the relative transmit and receive levels as well as the background level. Also included are all necessary regulated voltages for both internal and external circuitry, allowing line-powered operation (no additional power supplies required). A Chip Select pin allows the chip to be powered down when not in use. A volume control function may be implemented with an external potentiometer. MC34018 applications include speakerphones for household and business use, intercom systems, automotive telephones, and others.

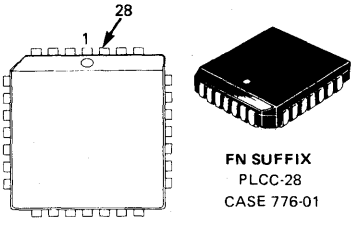
- All necessary level detection and attenuation controls for a hands-free telephone in a single integrated circuit
- Background noise level monitoring with long time constant
- Wide operating dynamic range through signal compression
- On-chip supply and reference voltage regulation
- Typical 100 mW output power (into 25 Ohms) with peak limiting to minimize distortion
- Chip Select pin for active/standby operation
- Linear Volume Control Function
- Standard 28-pin plastic DIP package (0.600 inch wide) and PLCC package

VOICE SWITCHED SPEAKERPHONE CIRCUIT

SILICON MONOLITHIC INTEGRATED CIRCUIT

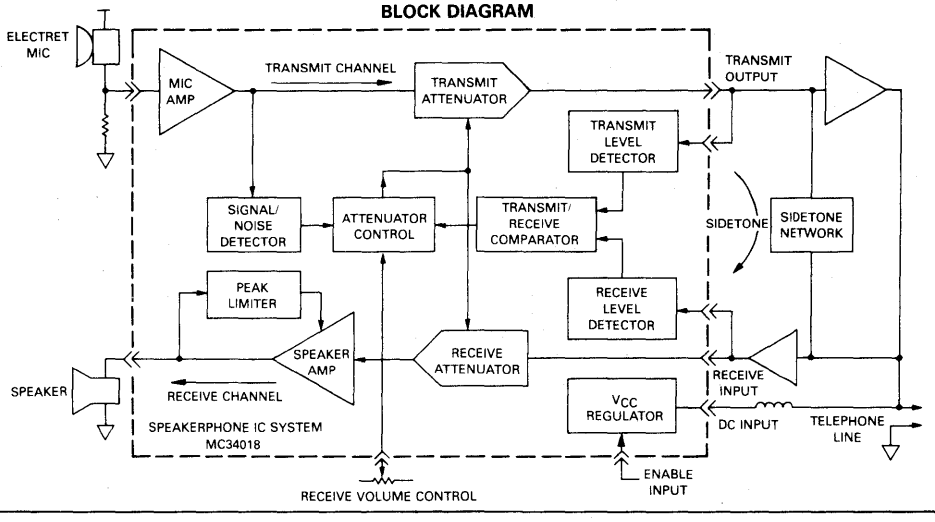


P SUFFIX
PLASTIC PACKAGE
CASE 710-02



FN SUFFIX
PLCC-28
CASE 776-01

BLOCK DIAGRAM



PIN DESCRIPTION

Pin	Name	Description
1	RR	A resistor to ground provides a reference current for the transmit and receive attenuators.
2	RTX	A resistor to ground determines the nominal gain of the transmit attenuator. The transmit channel gain is inversely proportional to the RTX resistance.
3	TXI	Input to the transmit attenuator. Input resistance is nominally 5.0 k ohms.
4	TXO	Output of the transmit attenuator. The TXO output signal drives the input of the transmit level detector, as well as the external circuit which drives the telephone line.
5	TLI	Input of the transmit level detector. An external resistor ac coupled to the TLI pin sets the detection level. Decreasing this resistor increases the sensitivity to transmit channel signals.
6	TLO	Output of the transmit level detector. The external resistor and capacitor set the time the comparator will hold the system in the transmit mode after speech ceases.
7	RLI	Input of the receive level detector. An external resistor ac coupled to the RLI pin sets the detection level. Decreasing this resistor increases the sensitivity to receive channel signals.
8	RLO	Output of the receive level detector. The external resistor and capacitor set the time the comparator will hold the system in the receive mode after the receive signal ceases.
9	MCI	Microphone amplifier input. Input impedance is nominally 10 k ohms and the dc bias voltage is approximately equal to VB.
10	MCO	Microphone amplifier output. The mic amp gain is internally set at 34 dB (50 V/V).
11	CP1	A parallel resistor and capacitor connected between this pin and V_{CC} holds a voltage corresponding to the background noise level. The transmit detector compares the CP1 voltage with the speech signal from CP2.
12	CP2	A capacitor at this pin peak detects the speech signals for comparison with the background noise level held at CP1.
13	XDI	Input to the transmit detector system. The microphone amplifier output is ac coupled to the XDI pin through an external resistor.
14	SKG	High current ground pin for the speaker amp output stage. The SKG voltage should be within 10 mV of the ground voltage at Pin 22.
15	SKO	Speaker amplifier output. The SKO pin will source and sink up to 100 mA when ac coupled to the speaker. The speaker amp gain is internally set at 34 dB (50 V/V).
16	V+	Input dc supply voltage. V+ can be powered from Tip and Ring if an ac decoupling inductor is used to prevent loading ac line signals. The required V+ voltage is 6.0 to 11 V (7.5 V nominal) at 7.0 mA.
17	AGC	A capacitor from this pin to VB stabilizes the speaker amp gain control loop, and additionally controls the attack and decay time of this circuit. The gain control loop limits the speaker amp input to prevent clipping at SKO. The internal resistance at the AGC pin is nominally 110 k ohms.
18	$\overline{CS}$	Digital chip select input. When at a Logic "0" (<0.7 V) the V_{CC} regulator is enabled. When at a Logic "1" (>1.6 V), the chip is in the standby mode drawing 0.5 mA. An open $\overline{CS}$ pin is a Logic "0". Input impedance is nominally 140 k ohms. The input voltage should not exceed 11 V.
19	SKI	Input to the speaker amplifier. Input impedance is nominally 20 k ohms.
20	V_{CC}	A 5.4 V regulated output which powers all circuits except the speaker amplifier output stage. V_{CC} can be used to power external circuitry such as a microprocessor (3.0 mA max). A filter capacitor is required. The MC34018 can be powered by a separate regulated supply by connecting V+ and V_{CC} to a voltage between 4.5 V and 6.5 V while maintaining $\overline{CS}$ at a Logic "1".
21	VB	An output voltage equal to approximately $V_{CC}/2$ which serves as an analog ground for the speakerphone system. Up to 1.5 mA of external load current may be sourced from VB. Output impedance is 250 ohms. A filter capacitor is required.
22	Gnd	Ground pin for the IC (except the speaker amplifier).
23	XDC	Transmit detector output. A resistor and capacitor at this pin hold the system in the transmit mode during pauses between words or phrases. When the XDC pin voltage decays to ground, the attenuators switch from the transmit mode to the idle mode. The internal resistor at XDC is nominally 2.6 k ohms (see Figure 1).
24	VLC	Volume control input. Connecting this pin to the slider of a variable resistor provides receive mode volume control. The VLC pin voltage should be less than or equal to VB.
25	ACF	Attenuator control filter. A capacitor connected to this pin reduces noise transients as the attenuator control switches levels of attenuation.
26	RXO	Output of the receive attenuator. Normally this pin is ac coupled to the input of the speaker amplifier.
27	RXI	Input of the receive attenuator. Input resistance is nominally 5.0 k ohms.
28	RRX	A resistor to ground determines the nominal gain of the receive attenuator. The receive channel gain is directly proportional to the RRX resistance.

Note: Pin numbers are identical for the DIP and PLCC packages.

ABSOLUTE MAXIMUM RATINGS

(Voltages referred to Pin 22) (T_A = 25°C)

Parameter	Value	Units
V+ Terminal Voltage (Pin 16)	+12, −1.0	V
$\overline{CS}$ (Pin 18)	+12, −1.0	V
Speaker Amp Ground (Pin 14)	+3.0, −1.0	V
VLC (Pin 24)	V_{CC}, −1.0	V
Storage Temperature	−65 to +150	°C

"Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The "Electrical Characteristics" tables provide conditions for actual device operation.

RECOMMENDED OPERATING CONDITIONS

Parameter	Value	Units
V+ Terminal Voltage (Pin 16)	+6.0 to +11	V
$\overline{CS}$ (Pin 18)	0 to +11	V
I_{CC} (Pin 20)	0 to 3.0	mA
VLC (Pin 24)	0.55VB to VB	V
Receive Signal (Pin 27)	0 to 250	mV_{rms}
Microphone Signal (Pin 9)	0 to 5.0	mV_{rms}
Speaker Amp Ground (Pin 14)	−10 to +10	mVdc
Ambient Temperature	−20 to +60	°C

ELECTRICAL CHARACTERISTICS (Refer to Figure 1)

Parameter	Symbol	Pin	Min	Typ	Max	Units
SUPPLY VOLTAGES						
V+ Supply Current	I_{V+}	16				
V+ = 11 V, Pin 18 = 0.7 V			—	—	9.0	mA
V+ = 11 V, Pin 18 = 1.6 V			—	—	800	μA
V_{CC} Voltage (V+ = 7.5 V)	V_{CC}	20	4.9	5.4	5.9	Vdc
Line Regulation (6.5 V < V+ < 11 V)	ΔV_{CC} LN		—	65	150	mV
Output Resistance (I_{CC} = 3.0 mA)	R_{OVCC}		—	6.0	20	ohms
Dropout Voltage (V+ = 5.0 V)	V_{CC} SAT		—	80	300	mV
VB Voltage (V+ = 7.5 V)	V_B	21	2.5	2.9	3.3	Vdc
Output Resistance (IB = 1.7 mA)	R_{OVB}		—	250	—	ohms
ATTENUATORS						
Receive Attenuator Gain (@ 1.0 kHz)		26,				
Rx Mode, Pin 24 = VB; Pin 27 = 250 mV_{rms}	G_{RX}	27	2.0	6.0	10	dB
Range (Rx to Tx Modes)	ΔG_{RX}		40	44	48	dB
Idle Mode, Pin 27 = 250 mV_{rms}	G_{RXI}		−20	−16	−12	dB
RXO Voltage (Rx Mode)	V_{RXO}		1.8	2.3	3.2	Vdc
Delta RXO Voltage (Switch from RX to TX Mode)	ΔV_{RXO}		—	—	100	mV
RXO Sink Current (Rx Mode)	I_{RXOL}		75	—	—	μA
RXO Source Current (Rx Mode)	I_{RXOH}		1.0	—	3.0	mA
RXI Input Resistance	R_{RXI}		3.5	5.0	8.0	kΩ
Volume Control Range (Rx Attenuator Gain, Rx Mode, 0.6 VB < Pin 24 < VB)	V_{CR}		24.5	—	32.5	dB

ELECTRICAL CHARACTERISTICS (continued)

Parameter	Symbol	Pin	Min	Typ	Max	Units
ATTENUATORS						
Transmit Attenuator Gain (@ 1.0 kHz)		3,				
Tx Mode, Pin 3 = 250 mV_{rms}	G_{TX}	4	4.0	6.0	8.0	dB
Range, (Tx to Rx Mode)	ΔG_{TX}		40	44	48	dB
Idle Mode, Pin 3 = 250 mV_{rms}	G_{TXI}		−16.5	−13	−8.5	dB
TXO Voltage (Tx Mode)	V_{TXO}		1.8	2.3	3.2	Vdc
Delta TXO Voltage (Switch from Tx to Rx Mode)	ΔV_{TXO}		—	—	100	mV
TXO Sink Current (Tx Mode)	I_{TXOL}		75	—	—	μA
TXO Source Current (Tx Mode)	I_{TXOH}		1.0	—	3.0	mA
TXI Input Resistance	R_{TXI}		3.5	5.0	8.0	kΩ
ACF Voltage (V_{CC} − Pin 25 Voltage)	ΔV_{ACF}	20,				
Rx Mode		25	—	150	—	mV
Rx Mode			—	6.0	—	mV
Idle Mode			—	75	—	mV
SPEAKER AMPLIFIER						
Speaker Amp Gain (Pin 19 = 20 mV_{rms})	G_{SPK}	15, 19	33	34	35	dB
SKI Input Resistance	R_{SKI}		15	22	37	kΩ
SKO Voltage (Pin 19 = Cap Couple to GND)	V_{SKO}		2.4	3.0	3.6	Vdc
SKO High Voltage (Pin 19 = 0.1 V, −100 mA load at Pin 15)	V_{SKOH}		5.5	—	—	Vdc
SKO Low Voltage (Pin 19 = −0.1 V, +100 mA load at Pin 15)	V_{SKOL}		—	—	600	mV
MICROPHONE AMPLIFIER						
Mike Amp Gain (Pin 9 = 10 mV_{rms}, 1.0 kHz)	G_{MCI}	9, 10	32.5	34	35	dB
Mike Amp Input Resistance	R_{MCI}		6.5	10	16	kΩ
LOGAMPS						
RLO Leakage Current (Pin 8 = VB + 1.0 V)	I_{LKRLO}	8	—	—	2.0	μA
TLO Leakage Current (Pin 6 = VB + 1.0 V)	I_{LKTLO}	6	—	—	2.0	μA
Transmit-Receive Switching Threshold (Ratio of ITLI to IRLI — at 20 μA — to switch Tx-Rx Comparator)	I_{TH}	5,7 25	0.8	—	1.2	
TRANSMIT DETECTOR						
XDC Voltage — Idle Mode	V_{XDC}	23	—	0	—	Vdc
Tx Mode			—	4.0	—	Vdc
CP2 Current Source	I_{CP2}	12	5.0	10	13	μA
DISTORTION						
Rx Mode — RXI to SKO (Pin 27 = 10 mV_{rms}, 1.0 kHz)	R_{XD}	27, 15	—	1.5	—	%
Tx Mode — MCI to TXO (Pin 9 = 5.0 mV_{rms}, 1.0 kHz)	T_{XD}	4,9	—	2.0	—	%

NOTES: 1. V+ = 7.5 V, $\overline{CS}$ = 0.7 V except where noted.
2. Rx Mode: Pin 7 = −100 μA, Pin 5 = +100 μA, except where noted.
Tx Mode: Pin 5, 13 = −100 μA, Pin 7 = +100 μA, Pin 11 = 0 volts.
Idle Mode: Pin 5 = −100 μA, Pin 7, 13 = +100 μA.
3. Current into a pin designated as +; current out of a pin designated as
4. Voltages referred to Pin 22. T_A = +25°C.

TEMPERATURE CHARACTERISTICS (−20 to +60°C)

Parameter	Pin	Typical Change	Units
V+ Supply Current (V+ = 11 V, Pin 18 = 0.7 V)	16	−0.2	%/°C
V+ Supply Current (V+ = 11 V, Pin 18 = 1.6 V)	16	−0.4	%/°C
V_{CC} Voltage (V+ = 7.5 V)	20	+0.1	%/°C
Attenuator Gain (Max and Min Settings)		±0.003	dB/°C
Delta RXO, TXO Voltages	4,26	±0.24	%/°C
Speaker Amp Gain	15,19	±0.003	dB/°C
Microphone Amp Gain	9,10	±0.001	dB/°C
Microphone Amp Input Resistance	9	+0.4	%/°C
Tx-Rx Switching Threshold (@ 20 μA)	5,7	±0.2	nA/°C

DESIGN GUIDELINES (Refer to Figure 1)

ATTENUATORS

The transmit and receive attenuators are complementary in function, i.e., when one is at maximum gain the other is at maximum attenuation, and vice versa. They are never both on or both off. Their main purpose is to control the transmit and receive paths to provide the half-duplex operation required of a speakerphone. The attenuators are controlled solely by the voltage at the ACF pin (Pin 25). The ACF voltage is provided by the Attenuator Control block, which receives 3 inputs: a) the Rx-Tx Comparator, b) the Transmit Detector Comparator, and c) the Volume Control. The response of the attenuators is based on the difference of the ACF voltage from V_{CC}, and therefore a simple method for monitoring the circuit operation is to monitor this voltage difference (referred to as ΔVacf). If ΔVacf is approximately 6 millivolts the transmit attenuator is fully on and the receive attenuator is fully off (transmit mode). If ΔVacf is approximately 150 millivolts the circuit is in the receive mode. If ΔVacf is approximately 75 millivolts, the circuit is in the idle mode, and the two attenuators are at gain settings approximately half way (in dB) between their fully on and fully off positions.

The maximum gain and attenuation values are determined by the three resistors RR, RTX, and RRX (Refer to Figures 2, 3 and 4). RR affects both attenuators according to its value RELATIVE to RTX and RRX, which is why Figure 4 indicates the variations versus the ratio of the other resistors to RR. (GRX and GTX are the maximum gains, and ARX and ATX are the maximum attenuations). RTX affects the gain and attenuation of only the transmit attenuator according to the curves of Figure 2, while RRX affects only the receive attenuator according to Figure 3. As can be seen from the figures, the gain difference (from on to off) is a reasonably constant 45 dB until the upper gain limit is approached. A value of 30 k is recommended for RR as a starting point, and then RTX and RRX selected to suit the particular design goals.

The input impedance of the attenuators (at TXI and RXI) is typically 5.0 kΩ, and the maximum input signal which will not cause output distortion is 250 mV_{rms} (707 mVp-p). The 4300 ohm resistor and 0.01 μF capacitor at RXO (in Figure 1) filters out high frequency components in the receive path. This helps minimize high frequency acoustic feedback problems which may occur if the filter were not present. The filter's insertion loss is 1.5 dB at 1.0 kHz. The outputs of the attenuators are inverted from their inputs.

Referring to the attenuator control block, the ΔVacf voltage at its output is determined by three inputs. The relationship of the inputs and output is summarized in the following truth table:

Tx-Rx Comp	Transmit Det Comp	Volume Control	ΔVacf	Mode
Transmit	Transmit	No Effect	6.0 mV	Transmit
Transmit	Idle	No Effect	75 mV	Idle
Receive	Transmit	Affects ΔVacf	50–150 mV	Receive
Receive	Idle	Affects ΔVacf	50–150 mV	Receive

As can be seen from the truth table, the Tx-Rx comparator dominates. The Transmit Detector Comparator is effective only in the transmit mode, and the Volume Control is effective only in the receive mode.

The Tx-Rx comparator is in the transmit position when there is sufficient transmit signal present over and above any receive signal. The Transmit Detector Comparator then determines whether the transmit signal is a result of background noise (a relatively stable signal), or speech which consists of bursts. If the signal is due to background noise, the attenuators will be put into the idle mode (ΔVacf = 75 mV). If the signal consists of speech, the attenuators will be switched to the transmit mode (ΔVacf = 6.0 mV.) A further explanation of this function will be found in the section on the Transmit Detector Circuit.

The Tx-Rx comparator is in the receive position when there is sufficient receive signal to overcome the background noise **AND** any speech signals. The ΔVacf voltage will now be 150 mV **IF** the volume control is at the maximum position, i.e. VLC (Pin 24) = VB. IF VLC is less than VB, the gain of the receive attenuator, and the attenuation of the transmit attenuator, will vary in a complementary manner as shown in Figure 5. It can be seen that at the minimum recommended operating level (VLC = 0.55 VB) the gain of the transmit attenuator is actually greater than that of the receive attenuator. The effect of varying VLC is to vary ΔVacf, with a resulting variation in the gains of the attenuators. Figure 6 shows the gain variations with ΔVacf.

The capacitor at ACF (Pin 25) smooths the transition between operating modes. This keeps down any "clicks" in the speaker or transmit signal when the ACF voltage switches.

The gain separation of the two attenuators can be reduced from the typical 45 dB by adding a resistor between Pins 20 (V_{CC}) and 25 (ACF). The effect is a reduction of the maximum ΔVacf voltage in the receive mode, while not affecting ΔVacf in the transmit mode. As an example, adding a 12 kΩ resistor will reduce ΔVacf by approximately 15 mV (to 135 mV), decrease the gain of the receive attenuator by approximately 5.0 dB, and increase the gain of the transmit attenuator by a similar amount. If the circuit requires the receive attenuator gain to be +6.0 dB in the receive mode, RRX must be adjusted (to ≈ 27 k) to re-establish this value. This change will also increase the receive attenuator gain in the transmit mode by a similar amount. The resistor at TLI may also require changing to reset the sensitivity of the transmit level detector.

LOG AMPLIFIERS
(Transmit and Receive Level Detectors)

The log amps monitor the levels of the transmit and receive signals, so as to tell the Tx-Rx comparator which mode should be in effect. The input signals are applied to the amplifiers (at TLI and RLI) through AC coupling capacitors and current limiting resistors. The value of these components determines the sensitivity of the respective amplifiers, and has an effect on the switching times between transmit and receive modes. The feedback elements for the amplifiers are back-to-back diodes which provide a logarithmic gain curve, thus allowing operation over a wide range of signal levels. The outputs of the amplifiers are rectified, having a quick rise time and a slow decay time. The rise time is determined primarily by the external capacitor (at TLO or RLO) and an internal 500 ohm resistor, and is on the order of a fraction of a millisecond. The decay time is determined by the external resistor and capacitor, and is on the order of a fraction of a second. The switching time is not fixed, but depends on the relative values of the transmit and receive signals, as well as these external components. Figure 7 indicates the dc transfer characteristics of the log amps, and Figure 8 indicates the transfer characteristics with respect to an ac input signal. The dc level at TLI, RLI, TLO, and RLO is approximately VB.

The Tx-Rx comparator responds to the voltages at TLO and RLO, which in turn are functions of the currents sourced out of TLI and RLI, respectively. If an offset at the comparator input is desired, e.g., to prevent noise from switching the system, or to give preference to either the transmit or receive channel, this may be achieved by biasing the appropriate input (TLI or RLI). A resistor to ground will cause a DC current to flow out of that input, thus forcing the output of that amplifier to be biased slightly higher than normal. This amplifier then becomes the preferred one in the system operation. Resistor values from 500 k to 10 M ohms are recommended for this purpose.

SPEAKER AMPLIFIER

The speaker amplifier has a fixed gain of 34 dB (50 V/V), and is noninverting. The input impedance is nominally 22 kΩ as long as the output signal is below that required to activate the Peak Limiter. Figure 9 indicates the typical output swing available at SKO (Pin 15). Since the output current capability is 100 mA, the lower curve is limited to a 5.0 volt swing. The output impedance depends on the output signal level and is relatively low as long as the signal level is not near the maximum limits. At 3 volts p-p the output impedance is <0.5 ohms, and at 4.5 volts p-p it is <3 ohms. The output is short circuit protected at approximately 300 mA.

When the amplifier is overdriven, the peak limiter causes a portion of the input signal to be shunted to ground, in order to maintain a constant output level. The effect is that of a gain reduction caused by a reduction of the input impedance (at SKI) to a value not less than 2.0 kΩ.

The capacitor at Pin 17 (AGC) determines the response time of the peak limiter circuit. When a large input signal is applied to SKI, the voltage at AGC (Pin 17) will drop quickly as a current source is applied to the external capacitor. When the large input signal is reduced, the current source is turned off, and an internal 110 kΩ resistor discharges the capacitor so the voltage at AGC can return to its normal value (1.9 Vdc). The capacitor additionally stabilizes the peak limiting feedback loop.

If there is a need to mute the speaker amplifier without disabling the rest of the circuit, this may be accomplished by connecting a resistor from the AGC pin to ground. A 100 kΩ resistor will reduce the gain by 34 dB (0 dB from SKI to SKO), and a 10 k resistor will reduce the gain by almost 50 dB.

TRANSMIT DETECTOR CIRCUIT

The transmit detector circuit, also known as the background noise monitor, distinguishes speech (which consists of bursts) from the background noise (a relatively constant signal). It does this by storing a voltage level, representative of the average background noise, in the capacitor at CP1 (Pin 11). The resistor and capacitor at this pin have a time constant of approximately 5 seconds (in Figure 1). The voltage at Pin 11 is applied to the inverting input of the Transmit Detector Comparator. In the absence of speech signals, the noninverting input receives the same voltage level minus an offset of 36 mV. In this condition, the output of the comparator will be low, the output transistor turned off, and the voltage at XDC (Pin 23) will be at ground. If the Tx-Rx comparator is in the transmit position, the attenuators will be in the idle mode (ΔVacf = 75 mV). When speech is presented to the microphone, the signal burst appearing at XDI reaches the noninverting input of the transmit detector comparator before the voltage at the inverting input can change, causing the output to switch high, driving the voltage at XDC up to approximately 4 volts. This high level causes the attenuator control block to switch the attenuators from the idle mode to the transmit mode (assuming the Tx-Rx comparator is in

the transmit mode). As long as the speech continues to arrive, and is maintained at a level above the background, the voltage at XDC will be maintained at a high level, and the circuit will remain in the transmit mode. The time constant of the components at XDC will determine how much time the circuit requires to return to the idle mode after the cessation of microphone speech signals, such as occurs during the normal pauses in speech.

The series resistor and capacitor at XDI (Pin 13) determine the sensitivity of the transmit detector circuit. Figure 10 indicates the change in DC voltage levels at CP2 and CP1 in response to a steady state sine wave applied at the input of the 0.068 μF capacitor and 4700 ohm resistor (the voltage change at CP1 is 2.7 times greater than the change at CP2). Increasing the resistor, or lowering the capacitor, will reduce the response at these pins. The first amplifier (between XDI and CP2) is logarithmic in order that this circuit be able to handle a wide range of signal levels (or in other words, it responds equally well to people who talk quietly and to people who shout). Figure 7 indicates the dc transfer characteristics of the log amp.

Figure 11 indicates the response at Pins 11, 12, and 23 to a varying signal at the microphone. The series of events in Figure 11 is as follows:

1) CP2 (Pin 12) follows the peaks of the speech signals, and decays at a rate determined by the 10 μA current source and the capacitor at this pin.

2) CP1 (Pin 11) increases at a rate determined by the RC at this pin after CP2 has made a positive transition. It will follow the decay pattern of CP2.

3) The noninverting input of the Transmit Detector Comparator follows CP2, gained up by 2.7, and reduced by an offset of 36 mV. This voltage, compared to CP1, determines the output of the comparator.

4) XDC (Pin 23) will rise quickly to 4 Vdc in response to a positive transition at CP2, but will decay at a rate determined by the RC at this pin. When XDC is above 3.25 Vdc, the circuit will be in the transmit mode. As it decays towards ground, the attenuators are taken to the idle mode.

MICROPHONE AMPLIFIER

The microphone amplifier is noninverting, has an internal gain of 34 dB (50 V/V), and a nominal input impedance of 10 kΩ. The output impedance is typically <15 ohms. The maximum p-p voltage swing available at the output is approximately 2.0 volts less than V_{CC}, which is substantially more than what is required in most applications. The input at MCI (Pin 9) should be ac coupled to the microphone so as to not upset the bias voltage. Generally, microphone sensitivity may be adjusted by varying the 2 k microphone bias resistor, rather than by attempting to vary the gain of the amplifier.

POWER SUPPLY

The voltage supply for the MC34018 at V+ (Pin 16) should be in the range of 6.0 to 11 volts, although the circuit will operate down to 4.0 volts. The voltage can be supplied either from Tip and Ring, or from a separate supply. The required supply current, with no signal to the speaker, is shown in Figure 12. The upper curve indicates the normal operating current when $\overline{\text{Chip Select}}$ (Pin 18) is at a Logic "0". Figure 13 indicates the average dc current required when supplying various power levels to a 25 ohm speaker. Figure 13 also indicates the minimum supply voltage required to provide the indicated power levels. The peak in the power supply current at 5.0–5.4 volts occurs as the V_{CC} circuit comes into regulation.

It is imperative that the V+ supply (Pin 16) be a good ac ground for stability reasons. If this pin is not well filtered (by a 1000 μF capacitor AT THE IC), any variation at V+ caused by the required speaker current flowing through this pin can cause a low frequency oscillation. The result is usually that the circuit will cut the speaker signal on and off at the rate of a few hertz. Experiments have shown that only a few inches of wire between the supply and the IC can cause the problem if the filter capacitor is not physically adjacent to the IC. It is equally imperative that both ground pins (Pins 14 and 22) have a low loss connection to the power supply ground.

V_{CC}

V_{CC} (Pin 20) is a regulated output voltage of 5.4 volts, +/−0.5 V. Regulation will be maintained as long as V+ is (typically) 80 mV greater than the regulated value of V_{CC}. Up to 3 milliamps can be sourced from this supply for external use. The output impedance is <20 ohms.

The 47 μF capacitor indicated for connection to Pin 20 is essential for stability reasons. It must be located adjacent to the IC.

If the circuit is deselected (see section on Chip Select), the V_{CC} voltage will go to 0 volts.

If the MC34018 is to be powered from a regulated supply (not the Tip and Ring lines) of less than 6.5 volts, the configuration of Figure 14 may be used so as to ensure that V_{CC} is regulated. The regulated voltage is applied to both V+ and V_{CC}, with $\overline{\text{CS}}$ held at a Logic "1" so as to turn off the internal regulator (the Chip Select function is not available when the circuit is used in this manner). Figure 15 indicates the supply current used by this configuration, with no signal at the speaker. When a signal is sent to the speaker, the curves of Figure 13 apply.

VB

VB is a regulated output voltage with a nominal value of 2.9 volts, +/−0.4 volts. It is derived from V_{CC} and tracks it, holding a value of approximately 54% of V_{CC}. 1.5 milliamps can be sourced from this supply at a typical output impedance of 250 ohms.

The 47 μF capacitor indicated for connection to the VB pin is required for stability reasons, and must be adjacent to the IC.

If the circuit is deselected (see section on Chip Select), the VB voltage will go to 0 volts.

CHIP SELECT

The Chip Select pin (Pin 18) allows the chip to be powered down anytime its functions are not required. A Logic "1" level in the range of 1.6 V to 11 V deselects the chip, and the resulting supply current (at V+) is shown in Figure 12. The input resistance at Pin 18 is >75 kΩ. The V_{CC} and VB regulated voltages go to 0.0 when the chip is deselected. Leaving Pin 18 open is equivalent to a Logic "0" (chip enabled).

FIGURE 1 — TEST CIRCUIT

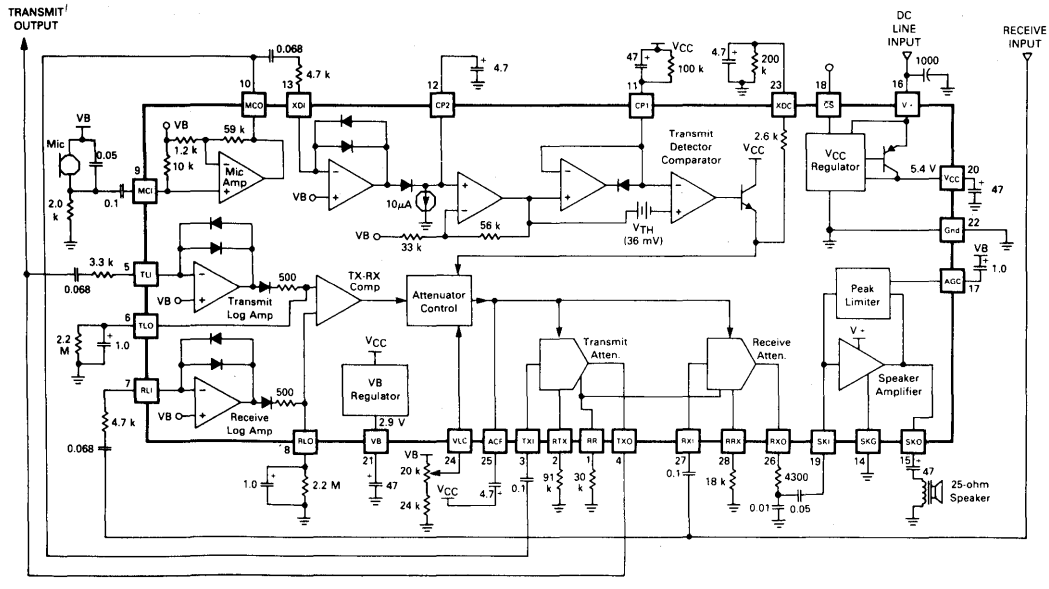


FIGURE 2 — TRANSMIT ATTENUATOR versus RTX

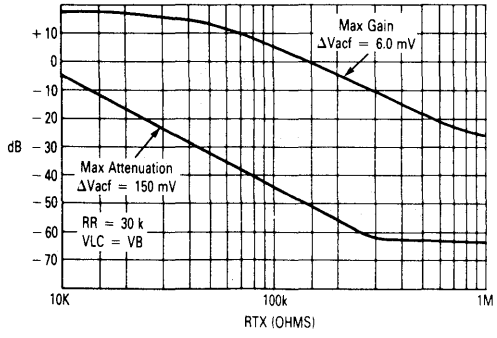


FIGURE 3 — RECEIVE ATTENUATOR versus RRX

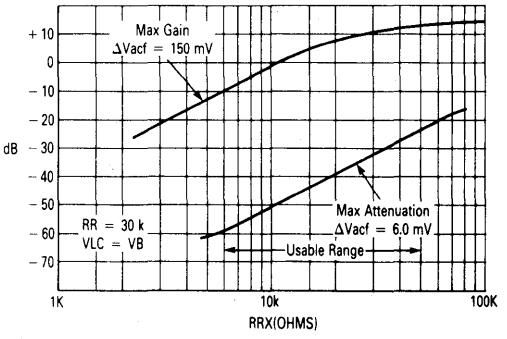


FIGURE 4 — GAIN AND ATTENUATION versus RESISTOR RATIOS

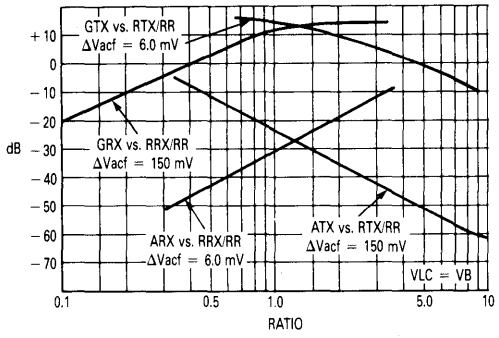


FIGURE 5 — ATTENUATOR GAIN versus VLC

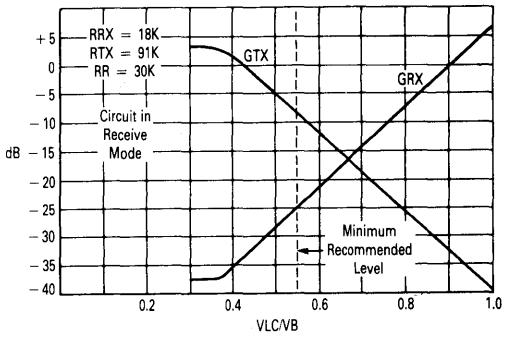


FIGURE 6 — ATTENUATOR GAIN versus ΔVacf

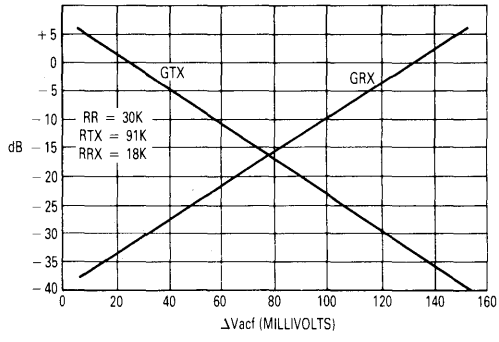


FIGURE 7 — LOG AMP TRANSFER CHARACTERISTICS

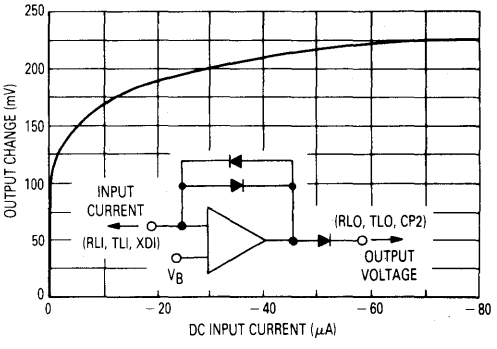


FIGURE 8 — LOG AMP TRANSFER CHARACTERISTICS

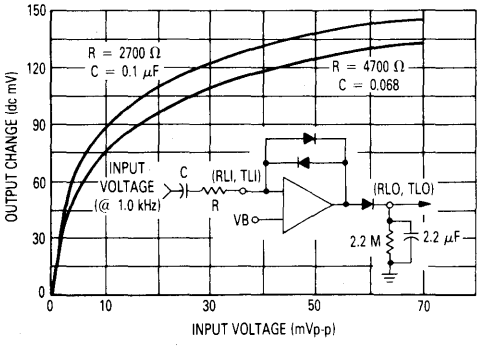


FIGURE 9 — SPEAKER AMP OUTPUT versus SUPPLY VOLTAGE

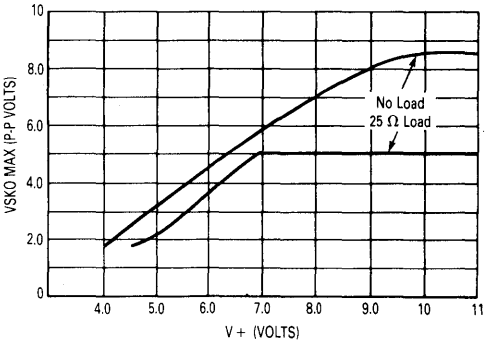


FIGURE 10 — RESPONSE AT CP2 AND CP1

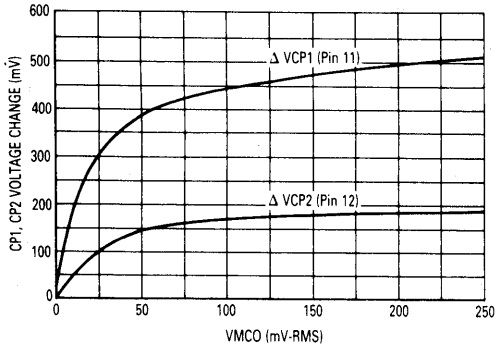


FIGURE 11 — TRANSMIT DETECTOR OPERATION

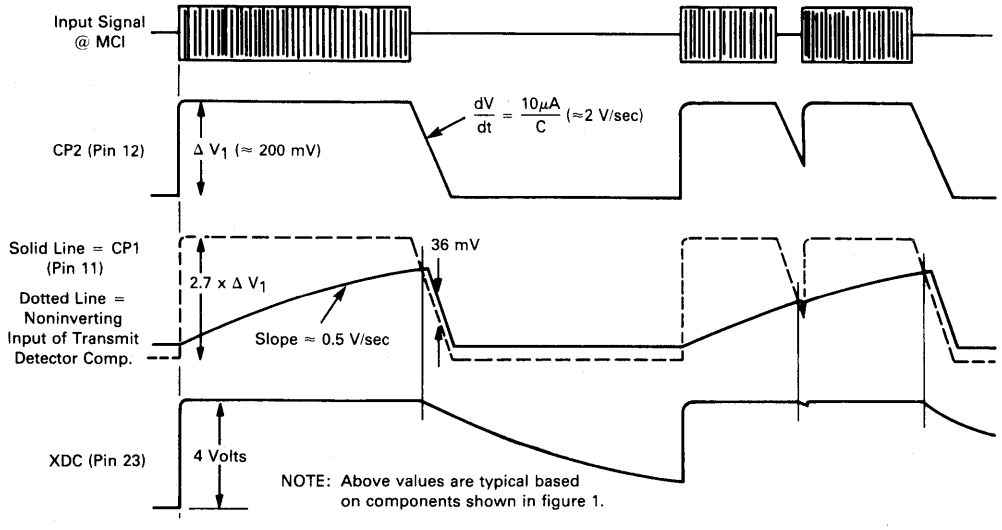


FIGURE 12 — SUPPLY CURRENT versus SUPPLY VOLTAGE

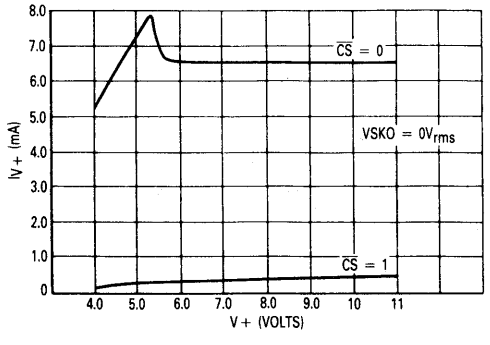


FIGURE 13 — SUPPLY CURRENT
versus SUPPLY VOLTAGE versus SPEAKER POWER

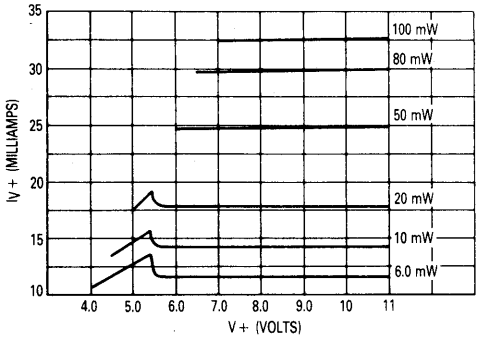


FIGURE 14 — ALTERNATE POWER SUPPLY CONFIGURATION

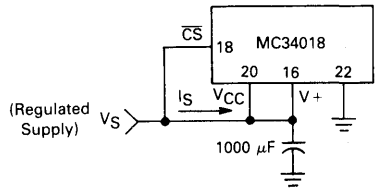
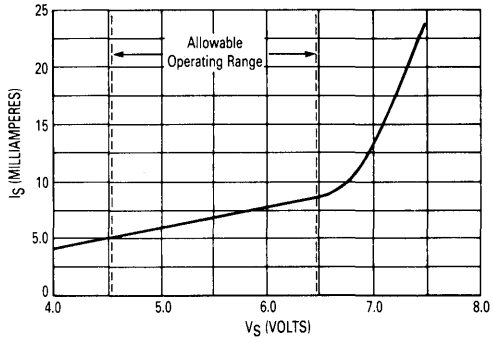


FIGURE 15 — SUPPLY CURRENT versus SUPPLY VOLTAGE (SEE FIGURE 14)



2

SWITCHING TIME

The switching times of the speakerphone circuit depend not only on the various external components, but also on the operating condition of the circuit at the time a change is to take effect. For example, the switching time from idle to transmit is generally quicker than the switching time from receive to transmit (or transmit to receive).

The components which most significantly affect the timing between the transmit and receive modes are those at Pins 5 (transmit turn-on), 6 (transmit turn-off), 7 (receive turn-on), and 8 (receive turn-off). These four timing functions are not independent, but interact since the Tx-Rx comparator operates on a RELATIVE Tx-Rx comparison, rather than on absolute values. The components at Pins 11, 12, 13, and 23 affect the timing from the transmit to the idle mode. Timing from the idle mode to transmit mode is relatively quick (due to the quick charging of the various capacitors), and is not greatly affected by the component values. Pins 5–8 do not affect the idle-to-transmit timing since the Tx-Rx comparator must already be in the transmit mode for this to occur.

The following table provides a summary of the effect on the switching time of the various components, including the volume control:

Additionally, the following should be noted:

1) The RCs at Pins 5 and 7 have a dual function in that they affect the sensitivity of the respective log amplifiers, or in other words, how loud the speech must be in order to gain control of the speakerphone circuit.

2) The RC at Pin 13 also has a dual function in that it determines the sensitivity of the transmit detector circuit.

3) The volume control affects the switching speed, and the relative response to transmit signals, in the following manner: When the circuit is in the receive mode, reducing the volume control setting increases the signal at TXO, and consequently the signal to the TLI pin. Therefore a given signal at TXI will switch the circuit into the transmit mode quicker at low volume settings.

The photographs of Figures 16 and 17 indicate experimentally obtained switching response times for the circuit of Figure 1. In Figure 16, the circuit is provided a continuous receive signal of 1.1 mVp-p at RXI (trace #3). A repetitive burst signal of 7.2 mVp-p, lasting 120

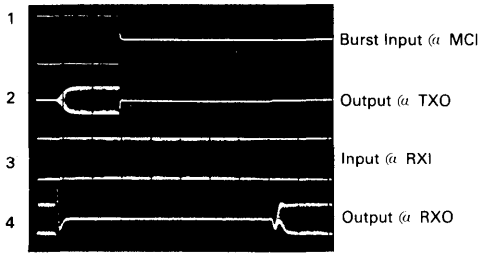
Components	Tx to Rx	Rx to Tx	Tx to Idle
RC @ Pin 5	Moderate	Significant	No effect
RC @ Pin 6	Significant	Moderate	No effect
RC @ Pin 7	Significant	Moderate	No effect
RC @ Pin 8	Moderate	Significant	No effect
RC @ Pin 11	No effect	Slight	Moderate
C @ Pin 12	No effect	Slight	Significant
RC @ Pin 13	No effect	Slight	Slight
RC @ Pin 23	No effect	Slight	Significant
V @ Pin 24	No effect	Moderate	No effect
C @ Pin 25	Moderate	Moderate	Slight

milliseconds, and repeated every 1 second, is applied to MCI (Trace #1). Trace #2 is the output at TXO, and is approximately 650 mVp-p at its maximum. Trace #4 is the output at RXO, and is approximately 2.2 mVp-p at its maximum. The time to switch from the receive mode to the transmit mode is approximately 40 ms, as indicated by the time required for TXO to turn on, and for RXO to turn off. After the signal at MCI is shut off, the switching time back to the receive mode is approximately 210 ms.

In Figure 17, a continuous signal of 7.6 mVp-p is applied to MCI (Trace #1), and a repetitive burst signal of 100 mVp-p is applied to RXI (Trace #3), lasting approximately 120 ms, and repeated every 1 second. Trace #2 is the output at TXO and is approximately 90 mVp-p at its maximum, and Trace #4 indicates the output at RXO, and is approximately 150 mVp-p at its maximum. In this sequence, the circuit switches between the idle and receive modes. The time required to switch from idle to receive is approximately 70 ms, as indicated by the first part of Traces 2 and 4. After the receive signal is shut off, the time to switch back to the idle mode is approximately 100 ms.

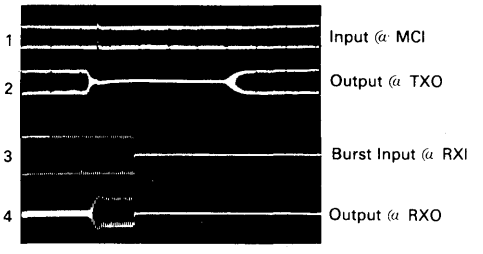
All of the above mentioned times will change significantly by varying the amplitude of the input signals, as well as by varying the external components.

FIGURE 16 — TRANSMIT-RECEIVE SWITCHING



Time Base = 40 ms/Div

FIGURE 17 — IDLE-RECEIVE SWITCHING



Time Base = 30 ms/Div

APPLICATIONS INFORMATION

The MC34018 Speakerphone IC is designed to provide the functions additionally required when a speakerphone is added to a standard telephone. The IC provides the necessary relative level detection and comparison of the speech signals provided by the talkers at the speakerphone (near end speaker) and at the distant telephone (far end speaker).

The MC34018 is designed for use with an electret type microphone, a 25 ohm speaker, and has an output power capability of (typically) 100 mW. All external components surrounding this device are passive, however, this IC does require additional circuitry to interface to the Tip and Ring telephone lines. Two suggested circuits are shown in this data sheet.

Figure 18 depicts a circuit using the MC34014 Speech Network (to provide the line interface), as well as the circuitry necessary to switch between the handset mode and the speakerphone mode. Switch HS (containing one normally open and one normally closed contact) is the hook switch actuated by the handset, shown in the on-hook position. When the handset is off-hook (HS1 open, HS2 closed), power is applied to the MC34014 speech network, and consequently the handset, and the $\overline{CS}$ pin of the MC34018 is held high so as to disable it. Upon closing the two poles of switch SS, **AND** placing switch HS in the on-hook position, power is then applied to both the MC34014 and the MC34018, and $\overline{CS}$ is held low, enabling the speakerphone function. Anytime the handset is removed from switch HS, the circuit reverts to the handset mode. The diode circuitry sets the operational mode of the MC34014 so as to optimize the speakerphone operation (see the MC34014 data sheet for further details). The tone dialer interface is meant for connection to a DTMF dialer with an active low MUTE signal. The V_{DD} supply from the MC34014 is a nominal 3.3 volts. The MC34017 and piezo sounder provide the ringing function.

Figure 19 depicts a configuration which does not include a handset, dialer, or ringer. The only controls are S1 (to make the connection to the line), S2 (a "privacy" switch), and the volume control. It is meant to be used in parallel with a normal telephone which has the dialing and ringing functions.

Figure 20 depicts a means of providing logic level signals that indicate which mode of operation the MC34018 is in. Comparator A indicates whether the circuit is in the receive or transmit/idle mode, and comparator B indicates (when in the transmit/idle mode) whether the circuit is in the transmit or idle mode. The LM393 dual comparator was chosen because of its low current requirement (<1.0 mA), low voltage requirement (as low as 2.0 volts), and low cost.

FIGURE 18 — SWITCHABLE HANDSET/HANDSFREE SYSTEM

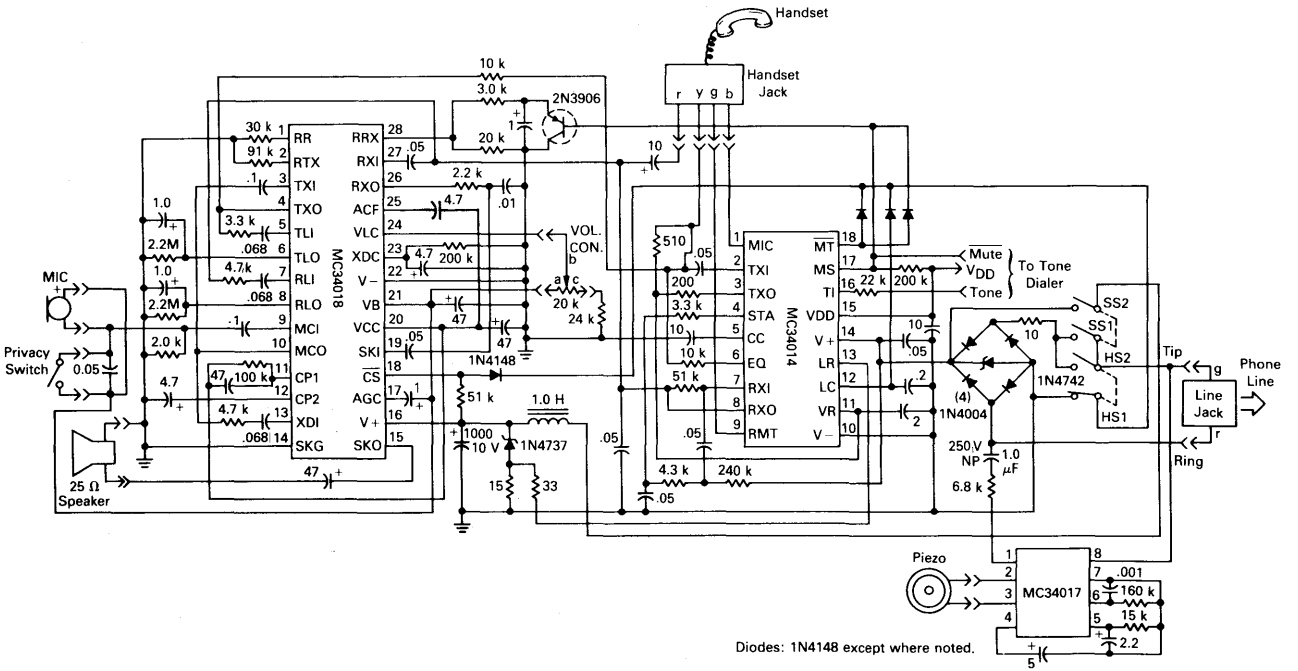
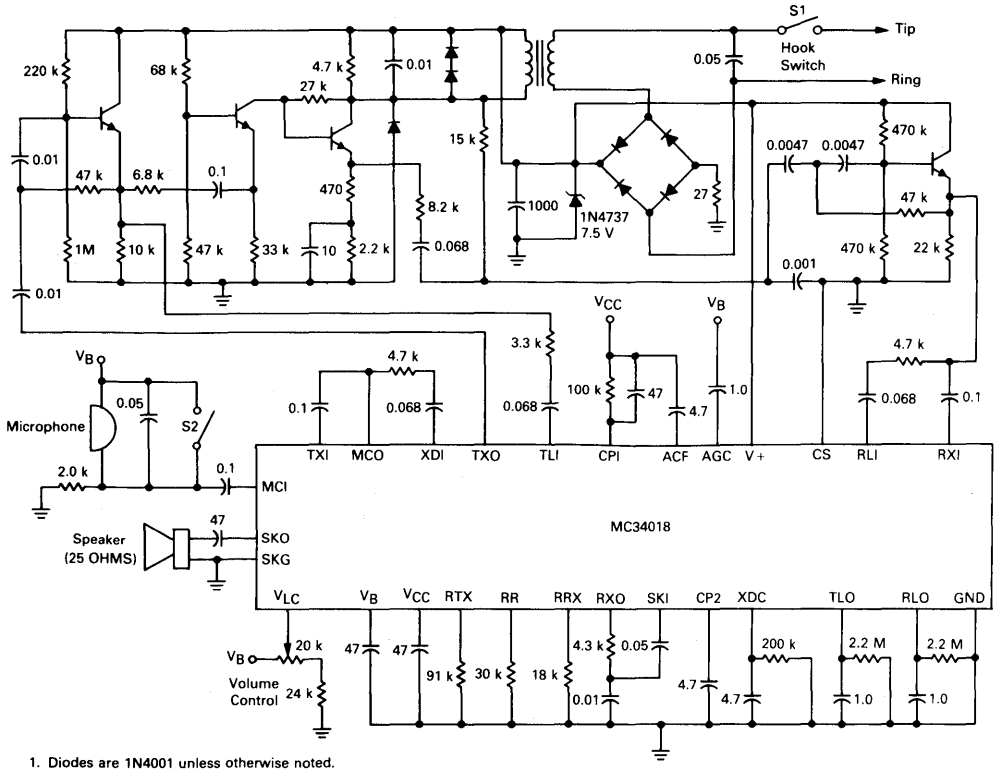
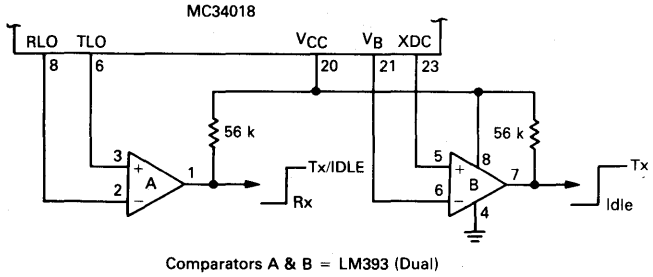


FIGURE 19 — BASIC LINE POWERED SPEAKERPHONE



1. Diodes are 1N4001 unless otherwise noted.
2. 4 Transistors are 2N3904.
3. Recommended Transformer: Microtran T2106.

FIGURE 20 — DIGITAL TRANSMIT/IDLE/RECEIVE INDICATION



Comparators A & B = LM393 (Dual)

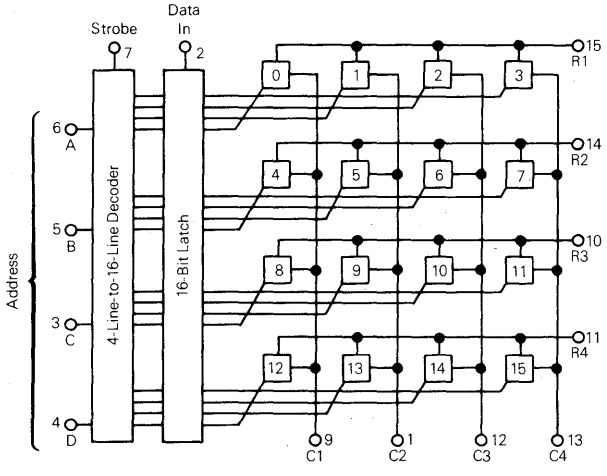
MOTOROLA

MC142100
MC145100

4 × 4 CROSSPOINT SWITCH WITH CONTROL MEMORY

The MC142100 and MC145100 consist of 16 crosspoint switches (analog transmission gates) organized in 4 rows and 4 columns. Both devices have 16 latches, each of which controls the state of a particular switch. Any of the 16 switches can be selected by applying its address to the device and a pulse to the strobe input. The selected crosspoint will turn on if during strobe, Data In was a one and will turn off if during strobe, Data In was a zero. In addition the MC145100 will reset all non-selected switches in the same row as the selected switch. Other switches are unaffected. In the MC145100, an internal power-on reset turns off all switches as power is applied.

- Internal Latches Control State of Switches
- Power-On Reset (MC145100 Only)
- Low On Resistance — Typically on 110 Ω @ 10 Vdc
- Large Analog Range ($V_{DD} - V_{SS}$)
- All Pins Are Diode Protected
- Matched Switch Characteristics
- High CMOS Noise Immunity
- MC142100 Pin-for-Pin Replacement for CD22100

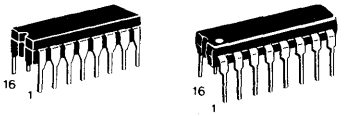


MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	−0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	−0.5 to V_{DD}+0.5	Vdc
Through Current	I	25	mAdc
Operating Temperature Range AL Device CL/CP Device	T_A	 −55 to +125 −40 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

CMOS MSI
(LOW-POWER COMPLEMENTARY MOS)

4 × 4 CROSSPOINT SWITCH WITH CONTROL MEMORY



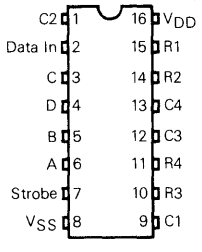
L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXX — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

PIN ASSIGNMENTS

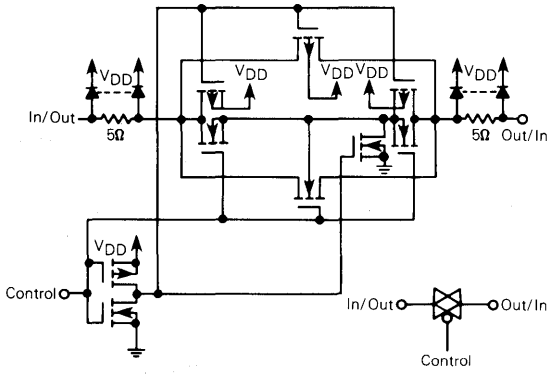


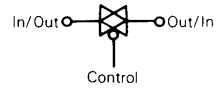
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.
Unused control inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

2

2

ANALOG TRANSMISSION GATE
(CROSSPOINT) SCHEMATIC





ELECTRICAL CHARACTERISTICS (V_{SS} = 0 V)

Characteristic		Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Operating Voltage	MC145100	V_{DD}	–	4.25	18	4.25	–	18	4.25	18	Vdc
	MC142100			3	18	3	–	18	3	18	
Input Voltage (Logic) Control Input	"0" Level	V_{IL}									Vdc
			5	–	1.5	–	2.25	1.5	–	1.5	
			10	–	3.0	–	4.50	3.0	–	3.0	
			15	–	4.0	–	6.75	4.0	–	4.0	
	"1" Level	V_{IH}									Vdc
			5	3.5	–	3.5	2.75	–	3.5	–	
			10	7.0	–	7.0	5.50	–	7.0	–	
	See Figure 1		15	11.0	–	11.0	8.25	–	11.0	–	
Input Current	AL	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μA
Pins 2, 3, 4, 5, 6, 7	CL, CP	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	
Input Capacitance (V_{in} = 0)		C_{in}									pF
Digital Inputs			10	–	–	–	7	15	–	–	
Switch Inputs/Outputs			10	–	–	–	50	75	–	–	
Feedthrough Capacitance		$C_{in/out}$	–	–	–	–	0.4	–	–	–	pF
Quiescent Current (AL)	MC145100		5	–	200	–	55	110	–	70	
		I_{DD}	10	–	400	–	115	230	–	100	μA
			15	–	600	–	170	340	–	200	
	MC142100		5	–	5	–	0.003	5	–	150	
		I_{DD}	10	–	10	–	0.004	10	–	300	μA
			15	–	20	–	0.005	20	–	600	
Quiescent Current	MC145100		5	–	250	–	55	150	–	80	
(CL, CP Device)		IDD	10	–	500	–	115	300	–	150	μA
			15	–	800	–	170	600	–	300	
	MC142100		5	–	5	–	0.003	5	–	150	
		I_{DD}	10	–	10	–	0.004	10	–	300	μA
			15	–	20	–	0.005	20	–	600	
On-State	See Figures 6-10	R_{on}	5	–	270	–	250	300	–	375	Ω
Resistance			10	–	140	–	110	170	–	230	
$V_{in} = \frac{V_{DD} - V_{SS}}{2}$			15	–	90	–	85	115	–	145	
On-State Resistance Difference		ΔR_{on}	5	–	–	–	25	30	–	–	Ω
Between Any Two Switches			10	–	–	–	15	25	–	–	
$V_{in} = \frac{V_{DD} - V_{SS}}{2}$	See Figure 6		15	–	–	–	15	20	–	–	
Input/Output Leakage	AL	$I_{in/out}$	15	–	±100	–	±0.4	+100	–	±1000	nA
Current, Switch Off	CL, CP		15	–	±300	–	±0.4	±300	–	±1000	

* T_{low} = 55°C for AL Device, −40°C for CL/CP Device.
T_{high} = +125°C for AL Device, ±85°C for CL/CP Device.

SWITCHING CHARACTERISTICS (V_{SS} = 0, T_A = 25°C, C_L = 50 pF)

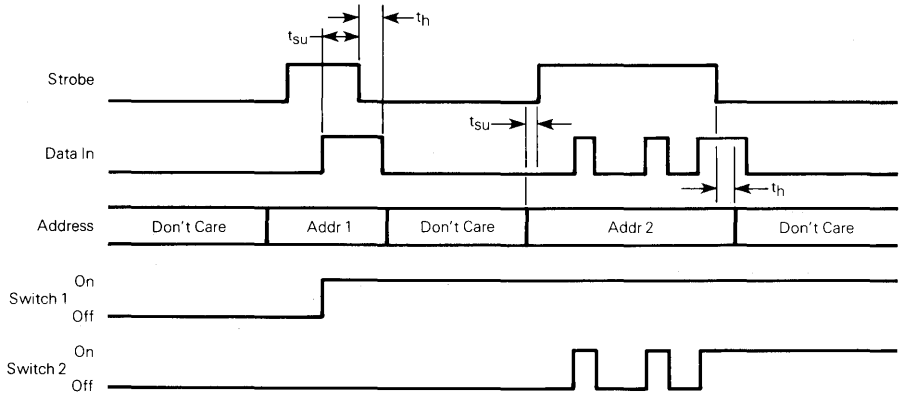
Characteristics		Symbol	V_{DD} Vdc	Min	Typ	Max	Unit
Propagation Delay Times	V_{SS} = 0 Vdc						
Input to Output		t_{PLH}, t_{PHL}	5	–	30	60	ns
			10	–	15	30	
			15	–	10	20	
Strobe to Output							
Output "1" to High Impedance	MC142100	t_{PLZ}, t_{PHZ}	5	–	350	700	ns
Output "0" to High Impedance			10	–	175	350	
			15	–	125	250	
Output "1" to High Impedance	MC145100	t_{PLZ}, t_{PHZ}	5	–	520	1040	ns
Output "0" to High Impedance			10	–	215	430	
			15	–	140	280	
High Impedance to Output "1"	MC142100	t_{PZH}, t_{PZL}	5	–	300	600	ns
High Impedance to Output "0"			10	–	150	250	
			15	–	80	160	
High Impedance to Output "1"	MC145100	t_{PZH}, t_{PZL}	5	–	550	1100	ns
High Impedance to Output "0"			10	–	200	400	
			15	–	130	260	
Data In to Output	MC142100	t_{PZH}, t_{PHZ}	5	–	300	600	ns
		t_{PZL}, t_{PLZ}	10	–	110	220	
			15	–	75	150	
Data In to Output	MC145100	t_{PZH}, t_{PHZ}	5	–	500	1000	ns
		t_{PZL}, t_{PLZ}	10	–	200	400	
			15	–	120	240	
Address to Output	MC142100	t_{PZH}, t_{PHZ}	5	–	350	700	ns
		t_{PZL}, t_{PLZ}	10	–	135	270	
			15	–	90	180	
Address to Output	MC145100	t_{PZL}, t_{PLZ}	5	–	500	1000	ns
		t_{PZH}, t_{PHZ}	10	–	180	360	
See Figure 2			15	–	115	230	
Minimum Setup Time							
Data In to Strobe	MC142100	t_{su}	5	–	50	190	ns
			10	–	10	50	
			15	–	0	30	
Data In to Strobe	MC145100	t_{su}	5	–	100	200	ns
			10	–	40	80	
			15	–	25	50	
Minimum Hold Time							
Data In to Strobe	MC142100	t_h	5	–	50	250	ns
			10	–	20	150	
			15	–	10	50	
Data In to Strobe	MC145100	t_h	5	–	40	400	ns
			10	–	10	200	
			15	–	0	80	
Minimum Set Up Time	MC142100	t_{su}	5	–	0	180	ns
Address to Strobe	MC145100		10	–	0	50	
			15	–	0	30	ns
Minimum Hold Time	MC142100	t_h	5	–	0	110	ns
Address to Strobe	MC145100		10	–	0	45	
			15	–	0	30	
Minimum Strobe Pulse Width	MC142100	t_{WH}	5	–	150	320	ns
	MC145100		10	–	50	160	
			15	–	40	80	

SWITCHING CHARACTERISTICS (continued) (V_{SS} = 0, T_A = 25°C, C_L = 50 pF)

Characteristics		Symbol	V_{DD} Vdc	Min	Typ	Max	Unit
Sine Wave Distortion (R_L = 1 kΩ, f = 1 kHz)	See Figure 3	–	10	–	0.5	–	%
Frequency Response (Switch On) (R_L = 1kΩ, 20 Log_{10} V_{out}/V_{in} = – 3.0 dB)	See Figure 3	–	10	–	15	–	MHz
Feedthrough Attenuation (Switch Off) (V_{in} = 10 V_{PP}, F = 1.6 kHz, R_L = 1 kΩ, C_L = 15 pF)	See Figure 3	–	10	–	– 80	–	dB
Frequency for Signal Crosstalk (V_{in} = 10 V_{PP}, Switch A On, Switch B Off, R_L = 1 kΩ, C_L = 15 pF)	– 40 dB – 110 dB See Figure 4	–	10 –	– –	1500 0.1	– –	kHz kHz
Crosstalk Controls to Output (R_L = 10 kΩ)	See Figure 5	–	10	–	70	–	mV

Address				Switch Selected		MC145100 Only Switches Cleared			Address				Switch Selected		MC145100 Only Switches Cleared		
A	B	C	D						A	B	C	D					
0	0	0	0	C1R1	0	1	2	3	0	0	0	1	C1R3	8	9	10	11
1	0	0	0	C2R1	1	0	2	3	1	0	0	1	C2R3	9	8	10	11
0	1	0	0	C3R1	2	0	1	3	0	1	0	1	C3R3	10	8	9	11
1	1	0	0	C4R1	3	0	1	2	1	1	0	1	C4R3	11	8	9	10
0	0	1	0	C1R2	4	5	6	7	0	0	1	1	C1R4	12	13	14	15
1	0	1	0	C2R2	5	4	6	7	1	0	1	1	C2R4	13	12	14	15
0	1	1	0	C3R2	6	4	5	7	0	1	1	1	C3R4	14	12	13	15
1	1	1	0	C4R2	7	4	5	6	1	1	1	1	C4R4	15	12	13	14

TIMING DIAGRAM
MC145100/MC142100



TEST CIRCUITS

FIGURE 1 — INPUT VOLTAGE

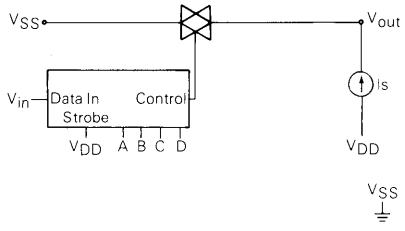


FIGURE 2 — PROPAGATION DELAY TIME

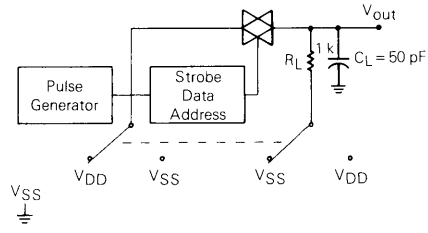


FIGURE 3 — BANDWIDTH AND FEEDTHROUGH ATTENUATION

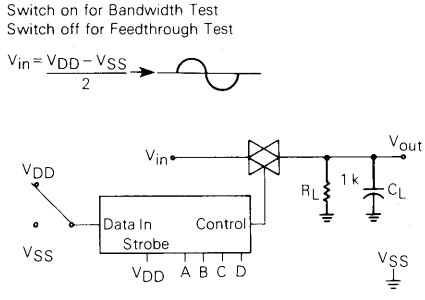


FIGURE 4 — CROSSTALK BETWEEN ANY TWO SWITCHES

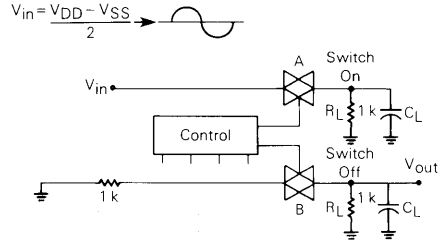


FIGURE 5 — CROSSTALK CONTROL TO OUTPUT

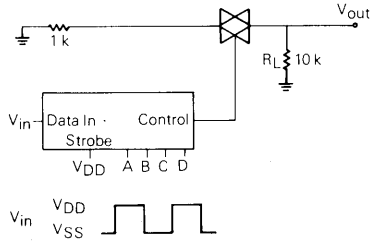
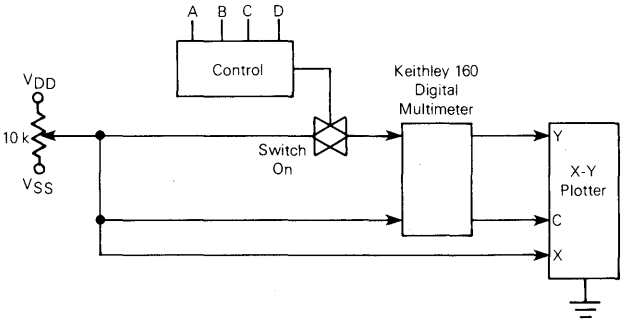


FIGURE 6 — CHANNEL RESISTANCE (R_{ON}) TEST CIRCUIT



TYPICAL RESISTANCE CHARACTERISTICS

FIGURE 7 — COMPARISON AT 25°C

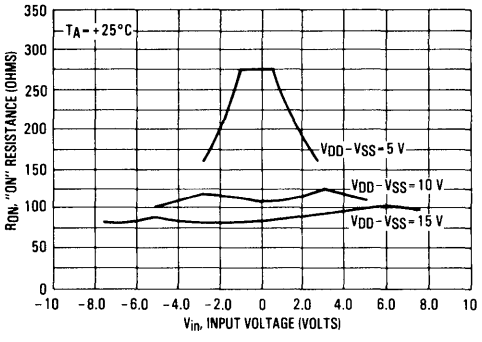


FIGURE 8 — V_{DD} = 2.5 V, V_{SS} = −2.5 V

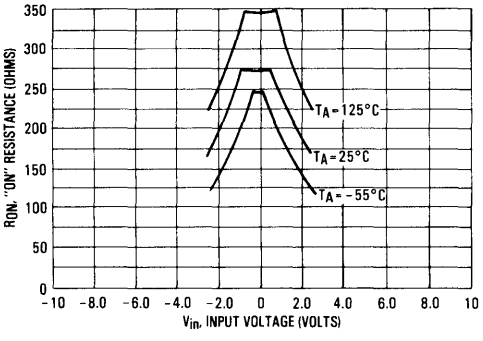


FIGURE 9 — V_{DD} = 5.0 V, V_{SS} = −5.0 V

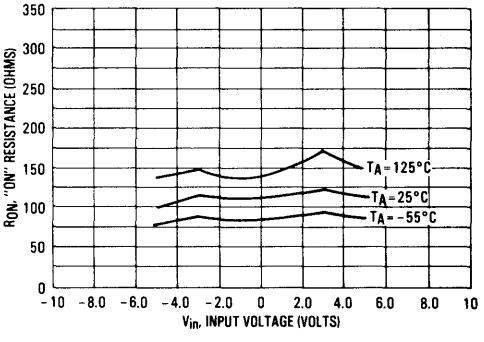
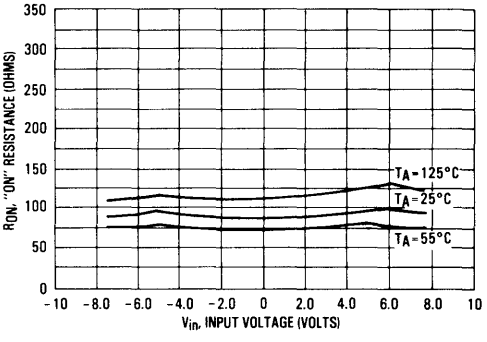


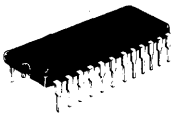
FIGURE 10 — V_{DD} = 7.5 V, V_{SS} = −7.5 V



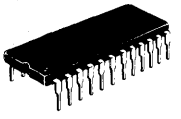
MOTOROLA

Product Preview

4×4×2 Crosspoint Switch with Control Memory



P SUFFIX
PLASTIC
CASE 649

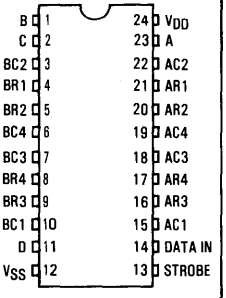


L SUFFIX
CERAMIC
CASE 623

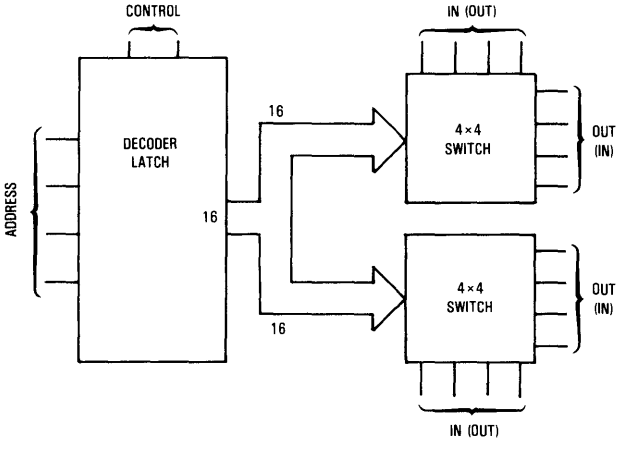
The MC142101 consists of 32 crosspoint switches organized into two 4 row-by-4 column arrays. The device has 16 latches, each of which controls the state of a particular switch in each array. The selected crosspoints will turn on, if during strobe, Data In was a one and will turn-off, if during strobe, Data In was a zero. During power-up, the latches are in indeterminate states and must be turned-off by holding strobe high, Data In low, and sequencing through all 16 addresses.

- Internal Latches Control State of Switches
- Low On Resistance — Typically 75 ohms at 10 Volts
- Large Analog Range ($V_{DD} - V_{SS}$)
- All Pins are Diode Protected
- Matched Switching Characteristics
- High CMOS Noise Immunity
- MC142101 Pin-for-Pin Replacement for CD22101

PIN ASSIGNMENT



BLOCK DIAGRAM



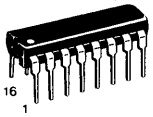
MC142103

MOTOROLA

Product Preview

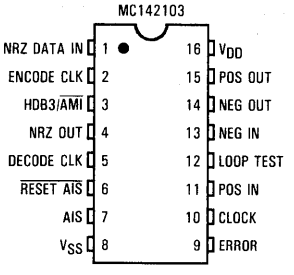
NRZ to HDB3/AMI HDB3/AMI TO NRZ

Encoder/Decoder (Transcoder) for Transmission Applications



P SUFFIX
PLASTIC PACKAGE
CASE 648-05

PIN ASSIGNMENT



The MC142103 is a high speed CMOS integrated circuit designed to perform the coding translation of clocked serial data into two streams of RZ (return to zero) digital pulses, which are externally mixed to form either HDB3 or AMI ternary signals for driving transmission lines. The MC142103 performs the reverse operation by translating two streams of clocked pulses (which have been derived from an incoming HDB3 or AMI ternary encoded signal) into a single stream of clocked binary data. The MC142103 also features loopback and error monitoring functions. The MC142103 performs the coding and decoding functions independently at clock rates from zero (dc) to 10 Mbps. The HDB3 coding and decoding are performed in a manner consistent with the CCITT G703 recommendations.

- Provides NRZ to HDB3/AMI Encoding and Decoding
- Low Power CMOS Operation
- Single 5 Volt Power Supply Operation
- Error Monitor Functions Provided
- Loopback Feature Provided
- Encode and Decode Clock Rates to 10 Mbps
- Pin Selectable HDB3/AMI Operation
- Pin Compatible with CD22103 and MJ1471

MOTOROLA

MC143403
MC143404

Advance Information

CMOS MSI

QUAD LINE DRIVER

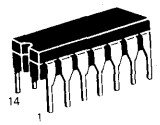
2

QUAD LINE DRIVER

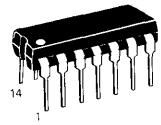
The MC143403 and MC143404 are low power, quad line drivers with true differential inputs. The device has electrical characteristics similar to the popular MC1741 and MC3403. However, the MC143403 has several distinct advantages over standard operational amplifier types. The low power quad driver, MC143403, draws only 1.5 mA (typ) and the micro power quad driver, MC143404, draws only 400 μA (typ) and provides high output drive capabilities. The common mode rejection ratio is typically 80 dB.

These units are excellent building blocks for communications, consumer, industrial and instrument applications where low power is required, particularly in telecommunications equipment. These units are useful in both battery operated communications systems and phone line powered equipment.

- Low Power and Micropower Communication Devices
- True Differential Input Stage
- Single or Split Supply Operation
- High Input Impedance
- Very Low Input Bias Current: 10 nA
- Four Drivers per Package
- Pinout Compatible with LM324 and MC3403
- Wide Input Voltage Range
- High Output Current Drive, MC143403



L SUFFIX
CERAMIC PACKAGE
CASE 632



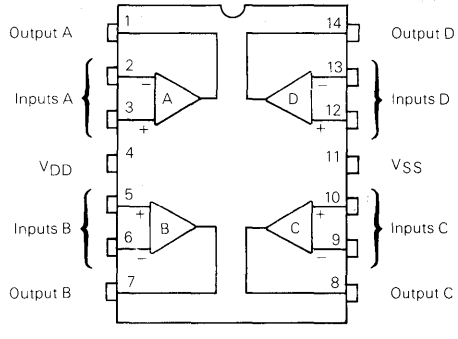
P SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

MC14XXXX

Suffix	Denotes
L	Ceramic Package
P	Plastic Package

PIN ASSIGNMENT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

This document contains information on a new product. Specifications and information herein are subject to change without notice.

2

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	−0.5 to +15	V
Input Voltage, All Inputs	V_{in}	−0.5 to V_{DD}+0.5	V
DC Current Drain per Pin	I	10	mA
Operating Temperature Range	T_A	−40 to 85	°C
Storage Temperature Range	T_{stg}	−65 to 150	°C

RECOMMENDED OPERATING CONDITIONS

DC Supply Voltage	V_{DD}	+4.75 to +12.6	V

ELECTRICAL CHARACTERISTICS (V_{SS}=0 V, T_A=0 to 70°C)

Characteristic	Symbol	V_{DD}	Min	Typ	Max	Unit
Input Offset Voltage	V_{IO}	10	–	10	±30	mV
Input Offset Current	I_{IO}	10	–	–	200	pA
Open Loop Voltage Gain, MC143404 Only, R_L=10 kΩ	A_{VOL}	12	60	70	–	dB
		10	60	70	–	
		5	60	70	–	
Open Loop Voltage Gain, MC143403 Only, R_L=600 Ω		10	45	55	–	
Common Mode Rejection Ratio	CMRR	10	50	60	–	dB
Input Bias Current	I_{IB}	10	–	–	1	nA
Output Voltage Range	V_{OR}	12	1.0	–	10.0	V
MC143404: R_L=10 kΩ		10	1.0	–	8.5	
MC143403: R_L=600 Ω		5	1.0	–	4.0	
Input Common Mode Voltage Range	V_{ICR}	12	0	–	10	V
		10	0	–	8	
		5	0	–	3	
Power Supply Current, MC143403	I_{DC}	12	–	1.5	3.0	mA
		5	–	1.5	3.0	
Power Supply Current, MC143404	I_{DC}	12	–	0.4	0.8	

ELECTRICAL CHARACTERISTICS (V_{SS}=0 V, T_A=0 to 70°C)

Characteristic	Symbol	V_{DD}	Min	Typ	Max	Unit
Small Signal Bandwidth	BW	10	–	500	–	kHz
A_V=1, R_L=10 kΩ, V_O=50 mV						
Slew Rate	SR					V/μs
MC143404: A_V=1, R_L=10 kΩ, 200 pF		10	–	1	–	
MC143403: R_L=600 Ω, 200 pF		10	–	1.5	–	
Phase Margin	ϕ_m	10	–	75	–	deg
MC143404: A_V=1, R_L=10 kΩ, 200 pF						
MC143403: R_L=600 Ω, 200 pF						
Power Supply Rejection Ratio	PSRR	10	–	60	–	dB
Average Temperature Coefficient of V_{IO}		10	–	20	–	μV/°C

FIGURE 1 — TYPICAL OPEN LOOP FREQUENCY RESPONSE

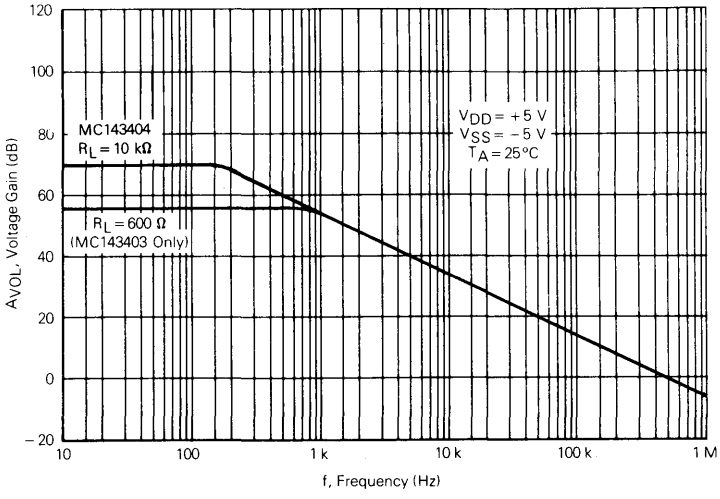


FIGURE 2 — TYPICAL POWER BANDWIDTH
(Large Signal Swing vs. Frequency)

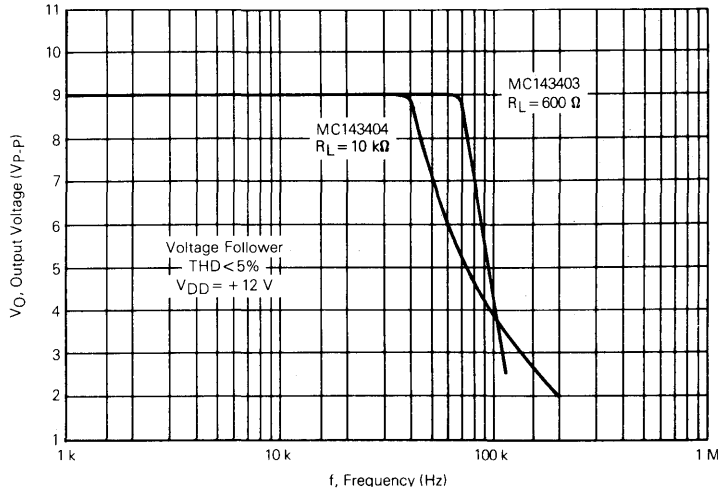


FIGURE 3 — GENERAL PURPOSE DUPLEXER (2-Wire to 4-Wire Converter)

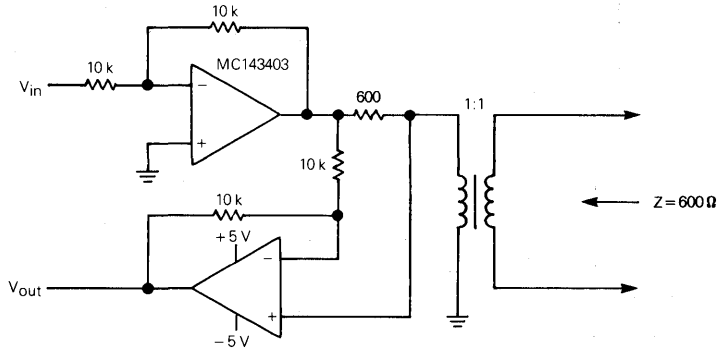
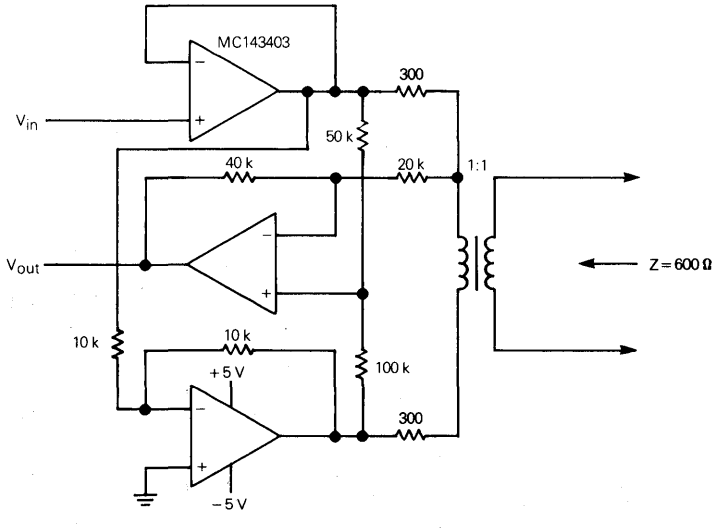


FIGURE 4 — HIGH POWER DUPLEXER (2-Wire to 4-Wire Converter)



MOTOROLA

MC145402

Product Preview

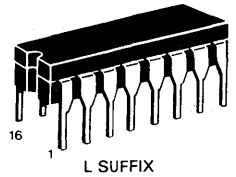
SERIAL 13-BIT LINEAR CODEC

- Provides Both 13-Bit Monotonic A/D and D/A Conversion for Signal Processing Systems in a Single IC
- 9-Bit Linearity
- On-Chip Precision Voltage Reference
- Serial Data Ports
- 2's Complement Coding
- ±5 to 6 Volt Supply Operation
- Sample Rates from 100 Hz to 32 kHz
- Input Sample and Hold Provided On-Chip
- 5 Volt CMOS Inputs: Outputs Capable of Driving Two LSTTL Loads
- Low Power Consumption: 50 mW Typical, 1 mW Power Down

CMOS LSI
LOW-POWER COMPLEMENTARY MOS

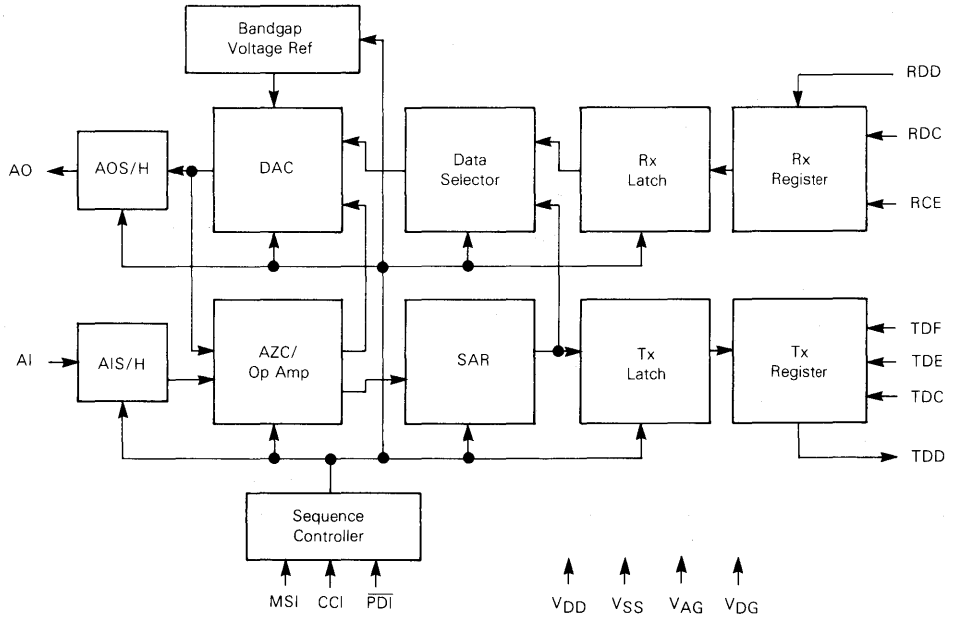
SERIAL 13-BIT LINEAR CODEC

2

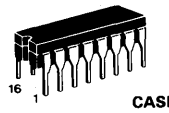


L SUFFIX
CERAMIC PACKAGE
CASE 620

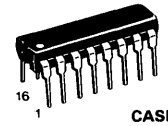
BLOCK DIAGRAM



MOTOROLA



CASE 620
CERAMIC



CASE 648
PLASTIC

2

Advance Information

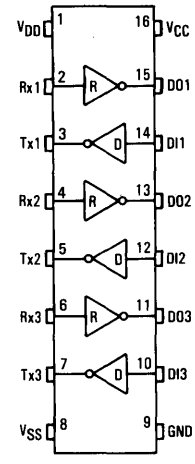
RS-232-C/V.28 Driver/Receiver

The MC145406 is a silicon-gate CMOS IC that combines 3 drivers and 3 receivers to fulfill the electrical specifications of EIA Standard RS-232-C and CCITT V.28. The drivers feature true TTL input compatibility, slew-rate-limited output, 300 ohms power-off source impedance, and output typically switching to within 25 percent of the supply rails. The receivers can handle up to ±25 volts while presenting 3 to 7 kilohms impedance. Hysteresis in the receivers aids reception of noisy signals. By combining both drivers and receivers in a single CMOS chip, the MC145406 provides an efficient, low-power solution for RS-232-C/V.28 applications.

Drivers
- ±5 to ±12 V Supply Range
- 300 Ohms Power-Off Source Impedance
- Output Current Limiting
- TTL Compatible
- Slew Rate Maximum of 30 V/μs
- Selectable Output Voltage Swing

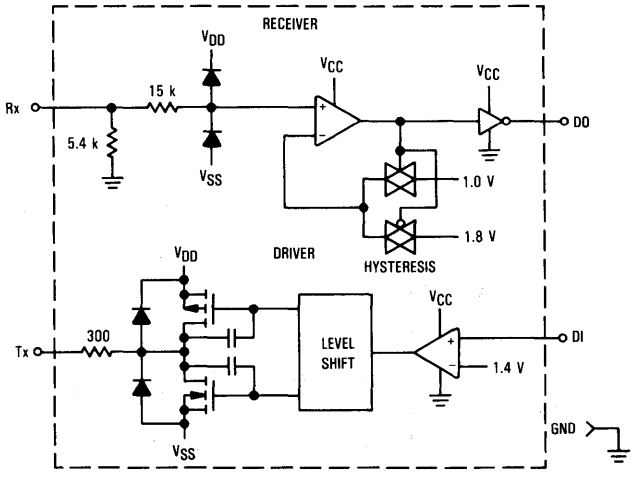
Receivers
- ±25 V Input Voltage Range
- 3 to 7 Kilohms Input Impedance
- Hysteresis on Input Switchpoint

PIN ASSIGNMENT



D = DRIVER
R = RECEIVER

FUNCTION DIAGRAM



This document contains information on a new product. Specifications and information herein are subject to change without notice.

MAXIMUM RATINGS (Voltage polarities referenced to GND)

Rating	Symbol	Value	Unit
DC Supply Voltages ($V_{DD} \geq V_{CC}$)	V_{DD} V_{SS} V_{CC}	−0.5 to 13.5 +0.5 to −13.5 −0.5 to 6.0	V
Input Voltage Range Rx1-3 inputs DI1-3 inputs	V_{IR}	−25 to +25 −0.5 to V_{DD} +0.5	V
DC Current Per Pin		±60	mA
Operating Temperature Range	T_A	−40° to +85°	°C
Storage Temperature Range	T_{stg}	−85° to +150°	°C
Power Dissipation	P_D	1.0	W

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that DI and DO be constrained to the range GND ≤ (DI or DO) ≤ V_{CC}. Also, $V_{SS} \leq$ (Tx or Rx) ≤ V_{DD}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC} for DI, and V_{SS} or V_{DD} for Rx.)

2

RECOMMENDED OPERATING CONDITIONS (T_A = −40° to 85°C GND)

Parameter	Symbol	Min	Typ	Max	Unit
DC Supply Voltage					V
V_{DD}	V_{DD}	4.5	5 to 12	13.2	
V_{SS}	V_{SS}	−4.5	−5 to −12	−13.2	
V_{CC} ($V_{DD} \geq V_{CC}$)	V_{CC}	4.5	5	5.5	
Quiescent Supply Current (outputs unloaded, inputs tied to GND)					μA
V_{DD} = +12.0 V	I_{DD}	—	140	400	
V_{SS} = −12.0 V	I_{SS}	—	340	600	
V_{CC} = +5.0 V	I_{CC}	—	300	450	

RECEIVER ELECTRICAL SPECIFICATIONS

(Voltage polarities referenced to GND = 0 V, V_{DD} = +5 to +12 V, V_{SS} = −5 to −12 V, $V_{DD} \geq V_{CC}$, T_A = −40° to 85°C)

Characteristics		Symbol	Min	Typ	Max	Unit
Input Turn-on Threshold (DO1-3 = V_{OL}) V_{CC} = 5.0 to 6.0 V	Rx1-3	V_{on}	1.35	1.80	2.35	V
Input Turn-off Threshold (DO1-3 = V_{OH}) V_{CC} = 5.0 to 6.0 V	Rx1-3	V_{off}	0.75	1.00	1.25	V
Input Threshold Hysteresis ($V_{on} - V_{off}$) V_{CC} = 5.0 to 6.0 V	Rx1-3	$V_{on} - V_{off}$	0.6	0.8	—	V
Input Resistance (Rx1-3 = ±3 to ±25 V)	Rx1-3	R_{in}	3.0	5.4	7.0	kΩ
Output Voltage High (Rx1-3 = −3 to −25 V)*	DO1-3	V_{OH}				V
I_{out} = −20 μA, V_{CC} = +5.0 V			4.9	4.9	—	
I_{out} = −1 mA, V_{CC} = +5.0 V			3.8	4.3	—	
Output Voltage Low (Rx1-3 = +3 to +25 V)*	DO1-3	V_{OL}				V
I_{out} = +20 μA, V_{CC} = +5.0 V			—	0.01	0.1	
I_{out} = +2 mA, V_{CC} = +5.0 V			—	0.2	0.5	
I_{out} = +4 mA, V_{CC} = +5.0 V			—	0.5	0.7	

*This is the range of input voltages as specified by RS-232-C to cause a receiver to be in the high or low logic state.

DRIVER ELECTRICAL SPECIFICATIONS

(Voltage polarities referenced to GND = 0 V, T_A = −40° to 85°C, V_{CC} = +5 V ±5%)

Characteristics		Symbol	Min	Typ	Max	Unit
Digital Input Voltage	DI1-3					V
Logic "0"		V_{IL}	—	—	0.8	
Logic "1"		V_{IH}	2.0	—	—	
Input Leakage Current (DI1-3 = V_{CC})	DI1-3	I_{in}	—	—	±1.0	μA
Output Voltage — High (DI1-3 = Logic 0, R_L = 3.0 kΩ)	Tx1-3	V_{OH}				V
V_{DD} = +5.0 V, V_{SS} = −5.0 V			3.5	3.9	—	
V_{DD} = +6.0 V, V_{SS} = −6.0 V			4.3	4.7	—	
V_{DD} = +12.0 V, V_{SS} = −12.0 V			9.2	9.5	—	
Output Voltage — Low (DI1-3 = Logic 1, R_L = 3.0 kΩ)	Tx1-3	V_{OL}				V
V_{DD} = +5.0 V, V_{SS} = −5.0 V			−4.0	−4.3	—	
V_{DD} = +6.0 V, V_{SS} = −6.0 V			−4.5	−5.2	—	
V_{DD} = +12.0 V, V_{SS} = −12.0 V			−10.0	−10.3	—	
Off Source Resistance (Figure 1) V_{DD} = V_{SS} = GND = 0 V, Tx1-3 = ±2.0 V	Tx1-3		300	—	—	Ω
Output Short-Circuit Current (V_{DD} = +12.0 V, V_{SS} = −12.0 V)		I_{SC}				mA
Tx1-3 shorted to GND*			—	±10	±20	
Tx1-3 shorted to ±15.0 V*			—	±40	±60	

*Specification is for one Tx output pin to be shorted at a time. Should all three driver outputs be shorted simultaneously, device dissipation limits will be exceeded.

SWITCHING CHARACTERISTICS ($T_A = -40°$ to 85°C, $V_{CC} = +5$ V ±5%, $V_{DD} = +6$ V to +12 V, $V_{SS} = -6$ V to −12 V)

Characteristics		Symbol	Min	Typ	Max	Unit
Drivers (R_L = 3 kΩ, C_L = 50 pF)*						
Propagation Delay Time						ns
Low-to-High	Tx1-3	t_{PLH}	—	200	325	
High-to-Low		t_{PHL}	—	200	325	
Output Slew Rate	Tx1-3	SR	—	±6	±30	V/μs
Receivers (C_L = 50 pF)*						
Propagation Delay Time	DO1-3					ns
Low-to-High		t_{PLH}	—	150	300	
High-to-Low		t_{PHL}	—	150	300	
Output Rise Time	DO1-3	t_r	—	250	400	ns
Output Fall Time	DO1-3	t_f	—	40	80	ns

*See Figure 2 for characteristic definitions.

PIN DESCRIPTIONS

V_{DD} — POSITIVE POWER SUPPLY (PIN 1)

The most positive power supply pin, which is typically 5 to 12 volts.

V_{SS} — NEGATIVE POWER SUPPLY (PIN 8)

The most negative power supply pin, which is typically −5 to −12 volts.

V_{CC} — DIGITAL POWER SUPPLY (PIN 16)

The digital supply pin, which is connected to the logic power supply (maximum +5.5 volts). V_{CC} *must* be less than or equal to V_{DD}.

GND — GROUND (PIN 9)

Ground return pin is typically connected to the signal ground pin of the RS-232-C connector (connector pin 7) as well as to the logic power supply ground.

Rx1, Rx2, Rx 3 — RECEIVE DATA INPUT (PINS 2, 4, 6)

These are the RS-232-C receive signal inputs whose voltages can range from +25 to −25 volts. A voltage between +3 and +25 is decoded as a space and causes the corresponding DO pin to swing to ground (0 V); a voltage between −3 and −25 volts is decoded as a mark and causes the DO pin to swing up to V_{CC}. The actual turn-on input switchpoint is typically biased at 1.8 volts above ground, and includes 800 millivolts of hysteresis for noise rejection. The nominal input impedance is 5 kilohm. An open or grounded input pin is interpreted as a mark, forcing the DO pin to V_{CC}.

DO1, DO2, DO3 — DATA OUTPUT (PINS 11, 13, 15)

These are the receiver digital output pins which swing from V_{CC} to ground. A space on the Rx pin causes DO to produce a logic zero, a mark, a logic one. Each output pin is capable of driving one LSTTL input load.

DI1, DI2, DI3 — DATA INPUT (PINS 10, 12 14)

These are the high-impedance digital input pins to the drivers. TTL compatibility is accomplished by biasing the input switchpoint at 1.4 volts above ground. Input voltage levels on these pins must be between V_{CC} and ground.

Tx1, Tx2, Tx3 — TRANSMIT DATA OUTPUT (PINS 3, 5, 7)

These are the RS-232-C transmit signal output pins which swing from V_{DD} to V_{SS}. A logic one at a DI input causes the corresponding Tx output to swing to V_{SS}. A logic zero causes the output to swing to V_{DD} (the output voltages will be slightly less than V_{DD} or V_{SS} depending upon the output load). Output slew rates are limited to a maximum of 30 volts per microsecond. These outputs are protected from short circuits to a worst case RS-232-C driver of ±15 volts. When the MC145406 is off ($V_{DD} = V_{SS} = V_{CC} = GND$), the minimum output impedance is 300 ohms.

APPLICATIONS INFORMATION

The MC145406 has been designed to meet the electrical specifications of EIA standard RS-232-C and CCITT recommendation V.28. RS-232-C defines the electrical and physical interface between Data Communication Equipment (DCE) and Data Terminal Equipment (DTE). A DCE is connected to a DTE using a cable which typically carries up to 25 leads. These leads are referred to as interchange circuits and allow the transfer of timing, data, control and test signals. Electrically, this transfer requires level shifting between the TTL logic levels of the computer or modem and the high voltage levels of RS-232-C which can range from ±3 to ±25 volts. The MC145406 provides the necessary level-shifting as well as meeting other aspects of the RS-232-C specification.

DRIVERS

As defined by the EIA specification, an RS-232-C driver presents a voltage of between ±5 to ±15 volts into a load of between 3 to 7 kilohms. A logic one at the driver input results in a voltage of between −5 to −15 volts. A logic zero results in a voltage betwen +5 to +15 volts. When operating V_{DD} and V_{SS} at ±6 to ±12 volts, the MC145406 meets this requirement. When operating at ±5 volts, the MC145406 drivers produce less than ±5 volts at the output (when terminated) which does not meet RS-232-C specification. However, the output voltages when using a ±5 volts power supply are high

enough, typically around ±4 volts, to permit proper reception by an RS-232-C receiver and can be used in applications where strict compliance to RS-232-C is not required.

Another requirement of the MC145406 driver is that it withstands a short to another driver in the RS-232-C cable. The worst-case driver that is permitted by RS-232 is a ±15 volt source that is current limited to 500 milliamperes. The MC145406 drivers can withstand a short to such a source indefinitely because of an on-chip current limiting circuit and the 300 ohm output resistors, which are required to meet the power-off resistance specification. That is, when V_{DD}, V_{SS} and V_{CC} are all at ground potential, the output resistance of an RS-232-C driver must be at least 300 ohms. The purpose of the 300 ohm resistor is to help protect other drivers that are inadvertantly connected to the Tx1-3 outputs when power to the MC145406 is off. However, if all three Tx outputs are shorted to ±15 volts while device power is off, the package dissipation of the MC145406 will be exceeded. If this situation can actually occur in a particular system then a series diode in the V_{DD} lead and one in the V_{SS} lead is recommended. In practice, a ±15 volt driver that supplies more than 20 to 30 milliamperes in a short-circuit condition will rarely be encountered.

Unlike other drivers, the MC145406 drivers feature an internally-limited output slew rate that does not exceed 30 volts per microsecond. Therefore, no external capacitors are required on the Tx1-3 outputs to limit the slew rate.

RECEIVERS

The job of an RS-232-C receiver is to level-shift voltages in the range of −25 to +25 volts down to TTL logic levels (0 to +5 volts). A voltage of between −3 and −25 volts on Rx1 is defined as a mark and produces a logic one at DO1. A voltage between +3 and +25 volts is a space and produces a logic zero. While receiving these signals, the Rx inputs must present a resistance between 3 and 7 kilohm. Nominally, the input resistance of the Rx1-3 inputs is 5.4 kilohm.

The input threshold of the Rx1-3 inputs is typically biased at 1.8 volts above ground (GND) with typically 800 millivolts of hysteresis included to improve noise immunity. The 1.8 volt bias forces the appropriate DO pin to a logic one when its Rx input is open or grounded as called for in the RS-232-C specification. Notice that TTL logic levels can be applied to the Rx inputs in lieu of normal RS-232-C signal levels. This might be helpful in situations where access to the modem or computer through the RS-232-C connector is necessary with TTL devices. However, it is important *not* to connect the RS-232-C outputs (Tx1-3) to TTL inputs since TTL operates off +5 volts only, and may be damaged by the high output voltage of the MC145406.

The DO outputs are to be connected to a TTL input (such as an input to a modem chip). These outputs will swing from V_{CC} to ground, allowing the designer to operate the DO and DI pins from digital power supply. The Tx and Rx sections are independently powered by V_{DD} and V_{SS} so that one may run logic at +5 volts and the RS-232-C signals at ±12 volts. *Caution:* V_{CC} should not exceed V_{DD} by more than 0.5 volts.

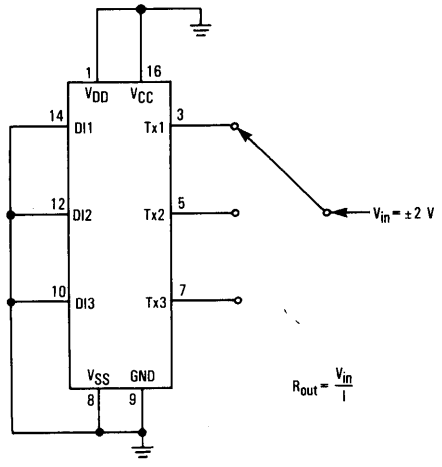
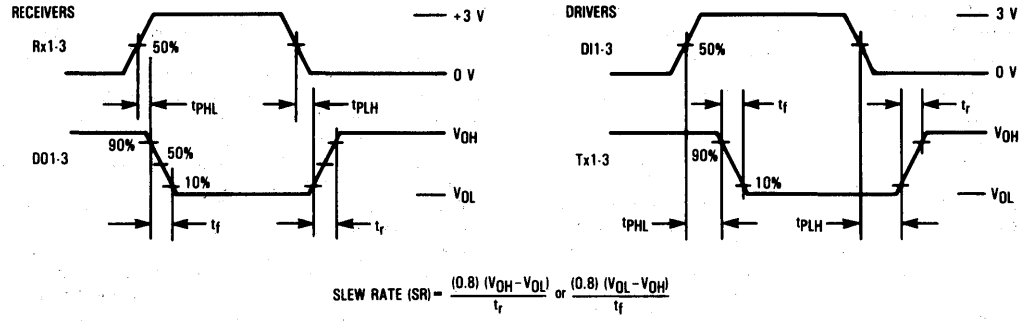
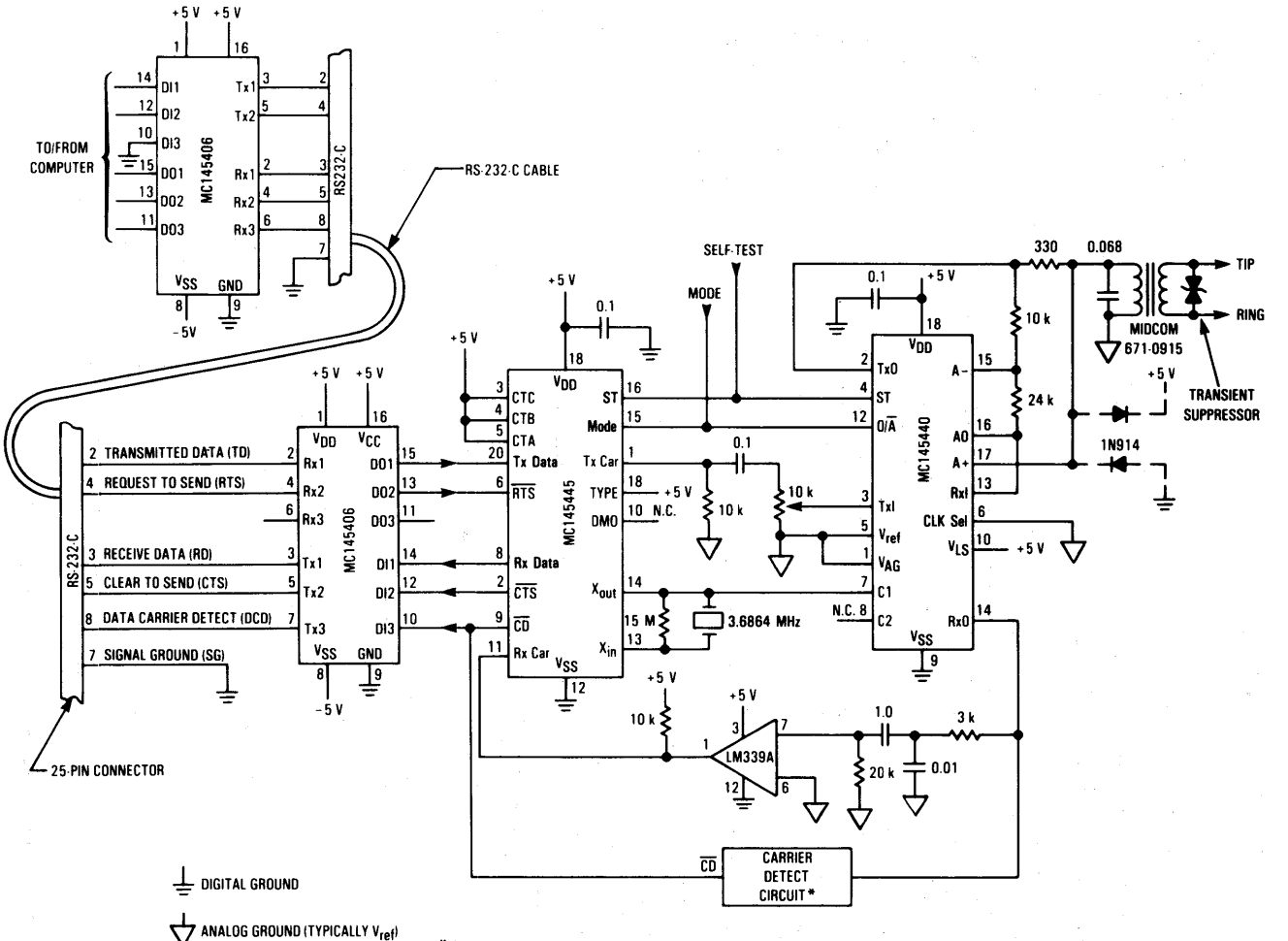


Figure 1. Power-Off Source Resistance (Drivers)



$$\text{SLEW RATE (SR)} = \frac{(0.8)\,(V_{OH}-V_{OL})}{t_r} \text{ or } \frac{(0.8)\,(V_{OL}-V_{OH})}{t_f}$$

Figure 2. Switching Characteristics



*See MC145445 Data Sheet for detailed schematic.
For V_{DD} and V_{SS}, ±6 to ±12 V must be substituted if strict compliance to RS-232-C is required.

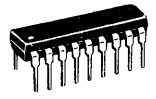
Figure 3. 5 Volt 300 Baud Modem with RS-232-C Interface

MOTOROLA

Advance Information

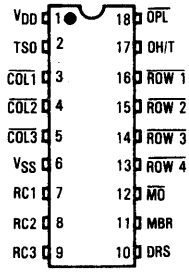
Integrated Pulse Dialer With Redial
Low-Power Silicon-Gate CMOS

2



P SUFFIX
PLASTIC
CASE 707

PIN ASSIGNMENTS



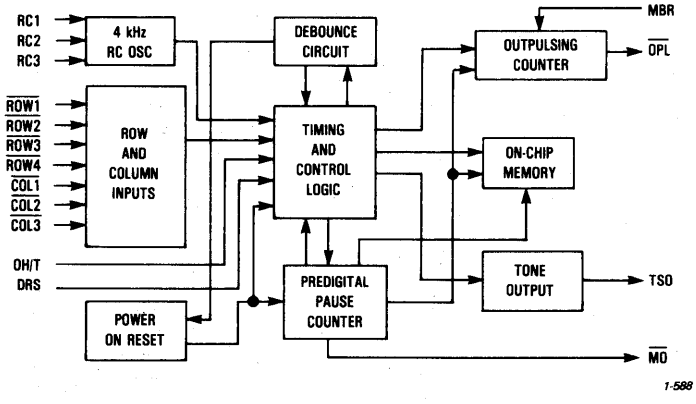
The MC145409 is a monolithic CMOS integrated circuit which converts 2-of-7 keyboard inputs into pulse signals that simulate a rotary telephone dialer. All of the features necessary for implementing a pulse dialer are provided, as well as redial. It uses an inexpensive RC oscillator, operates directly off telephone line supply, and consumes only microamperes of current when not outpulsing.

When off hook, the oscillator is enabled when a valid key input is detected. The MC145409 senses key depressions, verifies that a single key is depressed, and stores the key's code in on-chip memory. Up to 17 digits can be stored in the redial memory. After a predigital pause while memory is cleared, outpulsing begins and continues until the last entered digit is outpulsed. If the receiver has been on-hook for the minimum time, redial can be initiated by pressing either * or #.

When on-hook the oscillator is disabled, preventing excessive current draw. In this condition, key inputs will not be recognized.

- Direct Telephone Line Operation
- Silicon Gate CMOS Technology for Low-Power Operation
- 2.5 to 6.0 Volt Supply Range
- Selectable Make-Break Ratio (60% or 66%)
- Selectable Dialing Rate (10 pps or 20 pps)
- Continuous Mute
- Tone Signal Output
- Memory Redial with * or #
- Inexpensive RC Oscillator
- Uses Standard 2-of-7 Matrix with Negative Common or the Inexpensive Class-A Type Keyboard
- Pin Compatible with LR-40993

BLOCK DIAGRAM



1-588

This document contains information on a new product. Specifications and information herein are subject to change without notice.

ABSOLUTE MAXIMUM RATINGS (V_{SS} = 0 V)

Parameter	Symbol	Rating	Unit
DC Supply Voltage	V_{DD}	−0.3 to +6.0	V
Operating Temperature	T_A	−30 to +60	°C
Storage Temperature	T_{stg}	−55 to +150	°C
Power Dissipation	P_D	500	mW
Voltage On Any Pin Relative to V_{SS}	V_{in1}	−0.3	V
On Any Pin Relative to V_{DD}	V_{in2}	+0.3	

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

2

ELECTRICAL CHARACTERISTICS

Characteristic		Symbol	Min	Typ	Max	Unit
DC Supply Voltage (V_{SS} = 0 V)		V_{DD}	2.5	—	6.0	V
Operating Current (Off Hook, No Load on Outputs)		I_{DD}				μA
After Key Depression (During Outpulsing)	V_{DD} = 2.5 V		—	30	—	
	V_{DD} = 6.0 V		—	100	150	
During Key Depression	V_{DD} = 2.5 V		—	65	—	
	V_{DD} = 6.0 V		—	200	270	
Stand-by Current	V_{DD} = 2.5 V	I_{SB}	—	200	—	μA
(Off-Hook, Oscillator Disabled)	V_{DD} = 6.0 V		—	4.5	6.0	
Memory Retention Current (On-Hook)		—	—	5.0	10.0	nA
Input Voltage	"0" level	V_{IL}	—	20% of V_{DD}	—	V
MBR, DRS, OH/T, and Key Inputs (2-of-7 input mode)	"1" level	V_{IH}	—	80% of V_{DD}	—	
Keyboard Pull-up Resistance, $\overline{COL}$ 1-3, $\overline{ROW}$ 1-4		—	—	TBD	—	kΩ
Keyboard Pull-down Resistance, $\overline{COL}$ 1-3, $\overline{ROW}$ 1-4		—	—	TBD	—	kΩ
Mute Sink Current, $\overline{MO}$	V_{DD} = 2.5 V	—	500	—	—	μA
(V_{out} = 20% of V_{DD})	V_{DD} = 6.0 V		—	TBD	—	
Pulse Output Sink Current, $\overline{OPL}$	V_{DD} = 2.5 V	—	1.0	—	—	mA
(V_{out} = 20% of V_{DD})	V_{DD} = 6.0 V		—	TBD	—	
Tone Output Sink Current, TSO	V_{DD} = 2.5 V	—	250	—	—	μA
(V_{out} = 20% of V_{DD})	V_{DD} = 6.0 V		—	TBD	—	
Tone Output Source Current, TSO	V_{DD} = 2.5 V	—	250	—	—	μA
(V_{out} = 20% of V_{DD})	V_{DD} = 6.0 V		—	TBD	—	
Mute or Pulse Off Leakage Current, MBR, $\overline{OPL}$	V_{DD} = 2.5 V	—	—	TBD	—	μA
($V_{out} \approx V_{DD}$)	V_{DD} = 6.0 V		—	0.001	1.0	
Key Contact Resistance		—	—	—	1	kΩ
Keyboard Capacitance		—	—	—	30	pF

AC CHARACTERISTICS ($T_A = 25°C$, $V_{DD} = 2.5$ to 6.0 V)

Parameter		Symbol	Min	Typ	Max	Unit
Clock Frequency		f_{CL}	–	4	–	kHz
Frequency Stability		–	–	±4	–	%
Clock Start-Up Time		t_{CL}	–	1	–	ms
Tone Frequency*	DRS = V_{SS}	–	–	1	–	kHz
	DRS = V_{DD}		–	2	–	
Percent Make-Break Ratio	MBR = V_{DD}	%MBR	–	66	–	%
	MBR = V_{SS}		–	60	–	
Outpulsing Rate*	DRS = V_{SS}	f_{OPL}	–	10	–	pps
	DRS = V_{DD}		–	20	–	
Pre-Digital Pause*	f_{OPL} = 10 pps	t_{PDP}	–	900	–	ms
	f_{OPL} = 20 pps		–	450	–	
Inter-Digit Time*	f_{OPL} = 10 pps	t_{ID}	–	900	–	ms
	f_{OPL} = 20 pps		–	450	–	
Key Input Debounce Time*		t_{DB}	–	10	–	ms
Key Down Time for Valid Entry*		–	–	40	–	ms
Key Down Time for Two Key Rollover*		–	–	5	–	ms
On-Hook Time Required to Clear Memory*		–	300	–	–	ms
Mute Valid After Last Outpulse*		t_{MO}	–	5	–	ms

*Directly proportional to oscillator frequency. Parameters for f_{CL} = 4 kHz

PIN DESCRIPTIONS

V_{DD}, POSITIVE POWER SUPPLY (PIN 1)

Positive power, relative to V_{SS} can be supplied from regulated line power.

V_{SS}, NEGATIVE POWER SUPPLY (PIN 6)

Negative power, relative to V_{DD}

DRS, DIALING RATE SELECT (PIN 10)

When Pin 10 is tied to V_{SS} an output pulse rate of 10 pulse-per-second is selected. Tying Pin 10 to V_{DD} selects 20 pulse-per-second.

MBR, MAKE-BREAK RATIO (PIN 11)

The make-break ratio input controls the duty cycle of the digit pulse bursts at the $\overline{OPL}$ output as shown.

Make-Break Ratio (MBR)	Make	Break
V_{SS} (Pin 6)	40%	60%
V_{DD} (Pin 1)	34%	66%

$\overline{OPL}$, OUTPULSING (PIN 18)

The $\overline{OPL}$ output is an N-channel transistor in an open drain configuration designed to drive a bipolar transistor. This output pulls to V_{SS} during break and is open circuited during make.

$\overline{MO}$, MUTE OUTPUT (PIN 12)

The $\overline{MO}$ output is an N-channel transistor in an open drain configuration designed to drive a bipolar transistor. This output pulls to V_{SS} at the beginning of the predigital pause and remains there until the last digit is outpulsed. When not muting, this output is an open circuit.

TSO, TONE SIGNAL OUTPUT (PIN 2)

A tone signal is generated in response to a key depression for user feedback. The TSO pin is a CMOS output capable of driving an external bipolar transistor. The tone frequency is 1 kHz when a 10 pulse-per-second rate is selected and 2 kHz when 20 pulse-per-second is selected.

OH/T, ON-HOOK/TEST (PIN 17)

Connecting the OH/T pin to V_{SS} sets the MC145409 in the normal or off-hook mode. Allowing the pin to float or connecting it to V_{DD} selects the test mode.

KEYBOARD INPUTS (PINS 3, 4, 5, 13, 14, 15, 16)

The keyboard inputs allow either a single contact (Class A) keyboard, or a standard 2-of-7 keyboard with negative common. A valid key entry occurs when either a single row is connected to a single column, or a single row and column are simultaneously connected to V_{SS}. Figure 1 shows typical keyboard configurations.

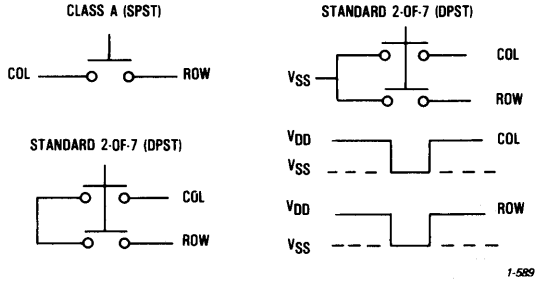
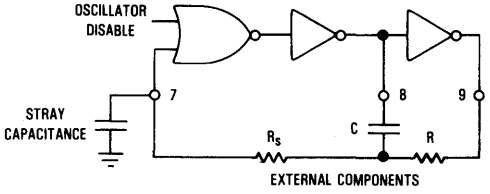


Figure 1. Keyboard Configuration

OSCILLATOR (PINS 7, 8, 9)

The MC145409 contains on-chip oscillator circuitry which will function with a minimum of external components. The oscillator is disabled when the circuit is idle. The circuit shown in Figure 2 will cause oscillation at 4 kHz with Rs = 2 MΩ, R = 220 kΩ, and C = 390 pF.



NOTE:
Minimizing the stray capacitance on pin 7 will enhance oscillator stability. The oscillator disable feature is internal to the device.

1-590

Figure 2. Oscillator Configuration

GENERAL DEVICE DESCRIPTION

When the MC145409 is on-hook, the row and column inputs are held high and keyboard entry is not accepted. A transition to off-hook resets the timing and control logic and the predigital pause counter. When in the off-hook mode, the keyboard remains static until a keyboard entry is sensed. This enables the oscillator. The row and column inputs are alternately scanned (by pulling high then low) to confirm input validity. The input is accepted only after it remains valid for 10 milliseconds of debounce time.

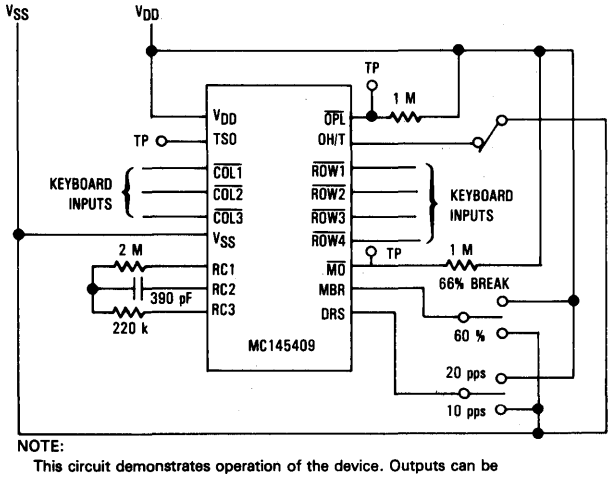
Once an input is accepted, the digit is stored in memory and outpulsing begins. The $\overline{OPL}$ output sends bursts of pulses equivalent to the digits of a telephone number stored in memory. This output drives an external bipolar transistor used to pulse the telephone line by momentarily connecting and disconnecting the speech network from line power.

During outpulsing, the $\overline{MO}$ output mutes the receiver, isolating it from the outpulsing transients.

When off-hook, the MCI45409 accepts key inputs and functions in a normal fashion. After outpulsing the last digit, the oscillator is disabled and the circuit goes to a standby mode. If the MC145409 is switched to on-hook while outpulsing, the remaining digits are outpulsed at 100 times their normal rate,

with a make-break ratio of 50/50 to facilitate testing. This is also an efficient means of resetting the circuit. Outpulsing in this mode can take up to 300 milliseconds, and when complete, the circuit is deactivated, drawing only enough current to sustain memory and the power-up-clear detect circuitry.

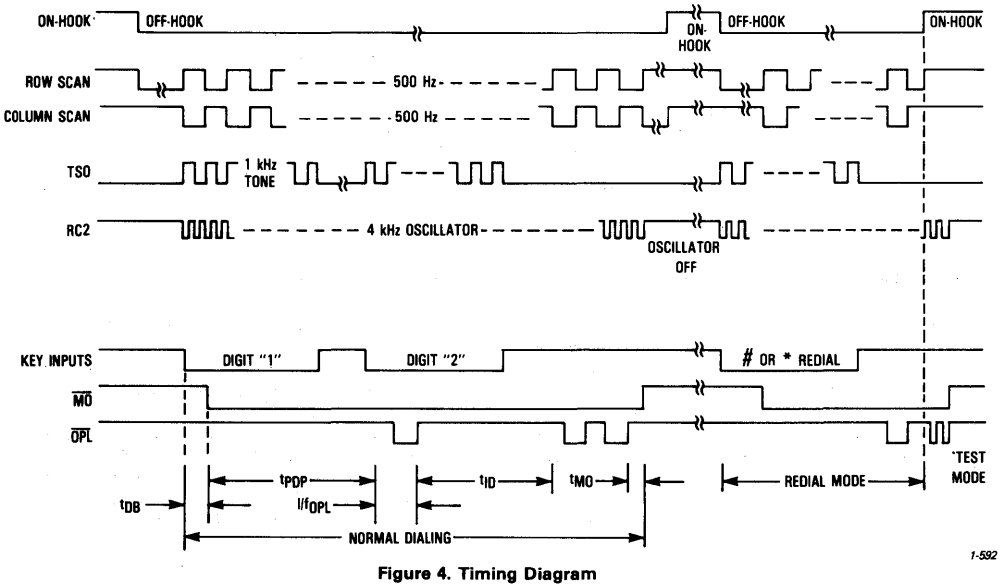
Returning to off-hook causes a positive transition on the mute output insuring connection of the speech network to the line. An initial key entry of # or * causes the number sequence stored in on-chip memory to be outpulsed. Pressing any other valid key clears memory, and the new number sequence will be outpulsed.



NOTE:
This circuit demonstrates operation of the device. Outputs can be observed at testpoints.

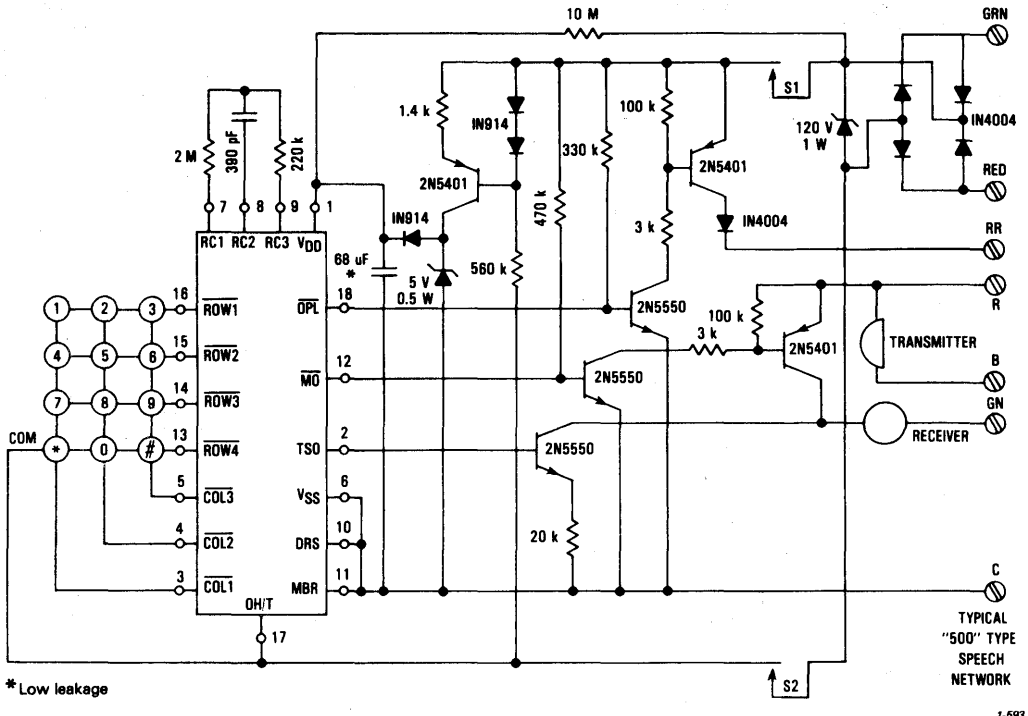
1-591

Figure 3. Evaluation Circuit



1-592

Figure 4. Timing Diagram



*Low leakage

Figure 5. Telephone Dialer Application Circuit

MOTOROLA

MC145411

Advance Information

2

BIT RATE GENERATOR

The MC145411 bit rate generator is constructed with complementary MOS enhancement mode devices. It utilizes a frequency divider network to provide a wide range of output frequencies.

A crystal controlled oscillator is the clock source for the network. A two-bit address is provided to select one of four multiple output clock rates.

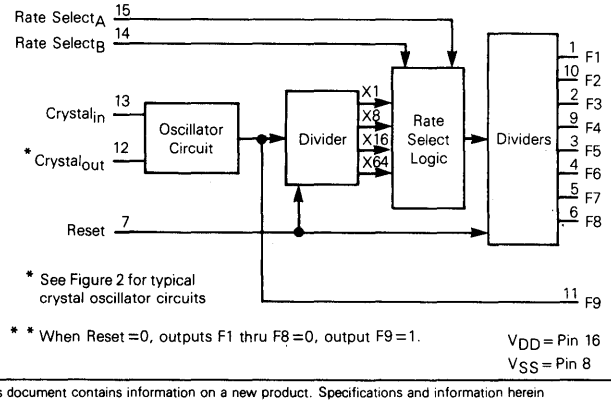
Applications include a selectable frequency source for equipment in the data communications market, such as teleprinters, printers, CRT terminals, and microprocessor systems.

- Single 5.0 V (±5%) Power Supply
- Internal Oscillator Crystal Controlled for Stability (to 4 MHz)
- 21 Different Bit Rates
- Nine Different Bit Rate Output Pins
- Programmable Time Bases for One of Four Multiple Output Rates
- 50% Output Duty Cycle
- Buffered Outputs Compatible with Low Power TTL
- Noise Immunity = 45% of V_{DD} Typical
- Diode Protection on All Inputs
- External Clock May be Applied to Pin 13
- Internal Pullup Resistor on Reset Input

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8.)

Rating	Symbol	Value	Unit
DC Supply Voltage Range	V_{DD}	5.25 to −0.5	V
Input Voltage, All Inputs	V_{in}	V_{DD} + 0.5 to V_{SS} − 0.5	V
DC Current Drain per Pin	I	10	mA
Operating Temperature Range	T_A	−40 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

BLOCK DIAGRAM



* See Figure 2 for typical crystal oscillator circuits

* * When Reset = 0, outputs F1 thru F8 = 0, output F9 = 1.

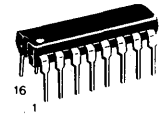
V_{DD} = Pin 16
V_{SS} = Pin 8

This document contains information on a new product. Specifications and information herein are subject to change without notice.

CMOS LSI

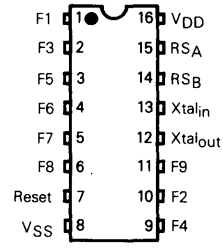
(LOW-POWER COMPLEMENTARY MOS)

BIT RATE GENERATOR



P SUFFIX
PLASTIC PACKAGE
CASE 648

PIN ASSIGNMENT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} V	0°C		25°C			+70°C		Unit
			Min	Max	Min	Typ	Max	Min	Max	
Supply Voltage	V_{DD}	–	4.75	5.25	4.75	5.0	5.25	4.75	5.25	V
Output Voltage "0" Level	V_{out}	5.0	–	0.05	–	0	0.05	–	0.05	V
"1" Level		5.0	4.99	–	4.99	5.0	–	4.99	–	V
Input Voltage										V
(V_O = 4.5 or 0.5 V)	V_{IL}	5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 0.5 or 4.5 Vdc)	V_{IH}	5.0	3.5	–	3.5	2.75	–	3.5	–	
Output Drive Current										mA
(V_{OH} = 2.5 V) Source	I_{OH}	5.0	−0.23	–	−0.20	−1.7	–	−0.16	–	
(V_{OL} = 0.4 V) Sink	I_{OL}	5.0	0.23	–	0.20	0.78	–	0.16	–	
Input Current	I_{in}									μA
Pins 13, 14, 15		–	–	±0.1	–	±0.00001	±0.1	–	±1.0	
Pin 7		5.0	–	–	−1.5	–	−7.5	–	–	
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	–	–	–	pF
Quiescent Dissipation	P_Q	5.0	–	2.5	–	0.015	2.5	–	15	mW
Power Dissipation**† (Dynamic plus Quiescent) (C_L = 15 pF)	P_D	5.0	–	–	$P_D = (7.5\ mW/MHz)\ f + P_Q$					mW
Output Rise Time** $t_r = (3.0\ ns/pF)\ C_L + 25\ ns$	t_{TLH}	5.0	–	–	–	70	200	–	–	ns
Output Fall Time** $t_f = (1.5\ ns/pF)\ C_L + 47\ ns$	t_{THL}	5.0	–	–	–	70	200	–	–	ns
Input Clock Frequency	f_{CL}	5.0	–	4.0	–	–	4.0	–	4.0	MHz
Clock Pulse Width	$t_{W(C)}$	–	200	–	200	–	–	200	–	ns
Reset Pulse Width	$t_{W(R)}$	–	500	–	500	–	–	500	–	ns

†For dissipation at different external capacitance (C_L) refer to corresponding formula:
$P_T(C_L = P_D + 2.6 \times 10^{-3}(C_L - 15\ pF)\ V_{DD}{}^2 f$
where: P_T, P_D in mW, C_L in pF, V_{DD} in V, and f in MHz.
**The formula given is for the typical characteristics only.

TABLE 1A — OUTPUT CLOCK RATES

Rate Select		Rate
B	A	
0	0	X1
0	1	X8
1	0	X16
1	1	X64

TABLE 1B — 1.843 MHz Crystal Output Rates

Output Number	Output Rates (Hz)			
	×64	×16	×08	×01
F1	614.4 k	153.6 k	76.8 k	9600
F2	230.4 k	57.6 k	28.8 k	3600
F3	153.6 k	38.4 k	19.2 k	2400
F4	115.2 k	28.8 k	14.4 k	1800
F5	76.8 k	19.2 k	9600	1200
F6	38.4 k	9600	4800	600
F7	19.2 k	4800	2400	300
F8	9600	2400	1200	150
F9*	1.843 M	1.843 M	1.843 M	1.843 M

*F9 is buffered oscillator output.

TABLE 1C — 3.6864 MHz Output Rates

Output Number	Output Rates (Hz)		
	×16	×08	×01
F1	307.2 K	153.6 k	19.2 k
F2	115.2 k	57.6 k	7200
F3	76.8 k	38.4 k	4800
F4	57.6 k	28.8 k	3600
F5	38.4 k	19.2 k	2400
F6	19.2 k	8600	1200
F7	9600	4800	600
F8	4800	2400	300
F9*	3.6864 M	3.6864 M	3,6864 M

*F9 is buffered oscillator output.

FIGURE 1 – DYNAMIC SIGNAL WAVEFORMS

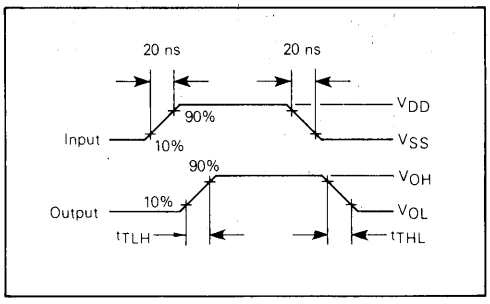
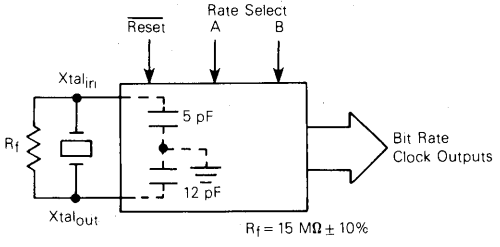


FIGURE 2 – TYPICAL CRYSTAL OSCILLATOR CIRCUIT



Crystal Specifications

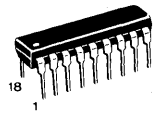
Crystal Mode	Parallel
Frequency	1.8432 MHz or 3.6864 MHz ±0.05%@13 pF
R_S	540 Ω max
C_0	7.0 pF max
Temperature Range	0 to 70°C
Test Level	1 mW
Test Set	TS – 330/TSM or Equivalent

MC145412
MC145413

MOTOROLA

Product Preview

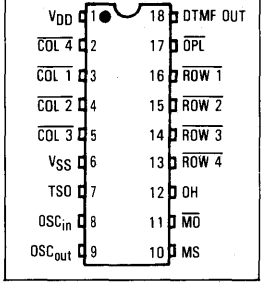
Pulse/Tone Repertory Dialer



CASE 707
PLASTIC

2

PIN ASSIGNMENT



The MC145412 and MC145413 are silicon gate, monolithic CMOS integrated circuits which convert keyboard inputs into either pulse or DTMF outputs for telephone dialing. All of the features for implementing pulse or DTMF dialing are provided. Additionally, both parts provide last number redial and repertory memory.

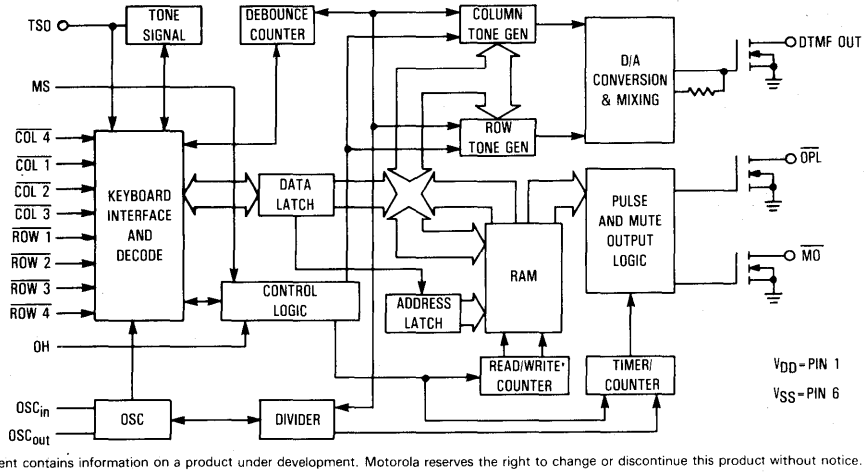
Both parts work with either a 3 × 4 or 4 × 4 keyboard, and have a four second pause input. When used with a 4 × 4 keypad, the MC145413 provides a keypad selectable pause/switch function which couples a four second pause with a switch in dialing modes (DTMF to pulse and vice versa). This dialing mode change is possible in all dialing sequences (normal, redial, and recall). The MC145412 requires manual switching of dialing modes.

The repertory memory can store nine, 18 digit numbers. Manual and automatic dialing can be cascaded in any order. During repertory memory programming, dialing outputs are disabled.

Both parts provide a 500 hertz tone signal output in the pulse dialing mode for user feedback. The mute output can be used to isolate the receiver from dialing outputs. The dialer can be controlled by an MCU.

- The MC145412 is Pin Compatible with LR4803 (Except Pin 7), and the MC145413 Adds Keypad Selectable Switching of Dialing Modes
- Single Pin Switchable Between DTMF, 10 pps and 20 pps
- Memory Storage for 9, 18 Digit Numbers, Plus Last Number Redial
- Uses Standard 2-of-7 or 2-of-8 or Form A Type Keyboards
- Uses 3.579545 MHz Colorburst Crystal
- Telephone Line Powered
- Stand Alone DTMF Dialer/Stand Alone Pulse Dialer
- Silicon Gate CMOS Technology for 2.5 - 6.0 V Low Power Operation

BLOCK DIAGRAM



2

ABSOLUTE MAXIMUM RATINGS (V_{SS} = 0 V)

Parameter	Symbol	Rating	Unit
DC Supply Voltage	V_{DD}	−0.5 to +8.0	V
Operating Temperature	T_A	−30 to +60	°C
Storage Temperature	T_{stg}	−65 to +150	°C
DC Current Drain per Pin	I	10	mA
Maximum Voltage			V
On any Pin Relative to V_{SS}	V_{in1}	−0.5	
On Any Pin Relative to V_{DD}	V_{in2}	+0.5	

ELECTRICAL CHARACTERISTICS (V_{DD} = 2.5 V, V_{SS} = 0 V, T_A = 25°C, unless noted)

Characteristics		Symbol	Min	Typ	Max	Unit
DC Supply Voltage (V_{SS} = 0 V)		V_{DD}	2.5		6.0	V
Supply Current	Pulse Mode (MS = V_{DD})	I_{DD}	–	75	–	μA
	DTMF Mode (MS = V_{SS})		–	1.0	–	mA
Memory Retention Voltage		V_{stby}	2.0	–	–	V
Memory Retention Current		I_{stby}	–	1.0	–	μA
Input Voltage	"0" level	V_{IL}	–	–	0.2V_{DD}	V
	"1" level	V_{IH}	0.8V_{DD}	–	–	
Row/Column Input Impedance	to V_{DD}	Z_{in}	–	100	–	kΩ
	to V_{SS}		–	5	–	
Mode Select Input Impedance	to V_{DD}	Z_{in}	–	100	–	kΩ
	to V_{SS}			100	–	
OH Pull-up Resistance			–	50	–	kΩ
Input Capacitance		C_{in}	–	10	–	pF
Output Sink Current (Vout = 0.5 V)	TSO pin	I_{OL}	–	500	–	μA
	$\overline{MO}$ pin		–	1.0	–	mA
	$\overline{OPL}$ pin		–	2.0	–	
TSO Output Source Current (V_{out} = 1.5 V)		I_{OH}	–	500	–	μA
Output Leakage Current	$\overline{MO}$, $\overline{OPL}$ pins	I_{lkg}	–	–	1.0	μA
DTMF Output Level (V_{DD} = 3.6 V)	Row Tone	V_{out}	–	400	–	mV RMS
(R_L = 600 Ω to V_{DD})	Column Tone		–	500	–	
DTMF Output Tone Distortion (V_{DD} = 3.6 V) (R_L = 600 Ω, 300 to 4,000 Hz)			–	5	–	%
DTMF Output Tone Leakage (V_{DD} = 3.6 V) (R_L = 600 Ω, 300 to 4,000 Hz)			–	–	−80	dBm

SWITCHING CHARACTERISTICS (T_A = 25°C, C_L = 50 pF, V_{DD} = 2.5 V unless noted, Osc. Freq. = 3.579545 Hz.)

Characteristics		Symbol	Min	Typ	Max	Unit
Row/Column Scan Frequency		f	–	250	–	Hz
Key Debounce Time		t_{DB}	–	32	–	ms
Minimum DTMF Output Duration			32	–	–	ms
DTMF Output Duration for Memory Dialing			–	100	–	ms
Inter-Digit Pause Time	DTMF (Memory Dialing)	t_{ID}	–	100	–	ms
	Pulse (All Dialing Sequences) 10 pps		–	1.0	–	s
	20 pps		–	0.5	–	
Start of Outpulsing Delay Time	10 pps	t_d	–	40	–	ms
	20 pps		–	20	–	
Make-Break Ratio (MS = V_{DD} or Open)		MBR	–	60	–	%
Outpulsing Rate	MS = Open	f_{OPL}	–	10	–	pps
	MS = V_{DD}		–	20	–	
$\overline{MO}$ Overlap Time		t_{MO}	2	–	4	ms
TSO Output Frequency		f_{TSO}	–	500	–	Hz
TSO Output Duration		t_{TSO}	20	–	32	ms

PIN DESCRIPTIONS

V_{DD}, V_{SS} – POWER SUPPLY (PIN 1, PIN 6)

DC power is supplied to the part on these two pins, with V_{DD} being the most positive. Permissible ranges are from 2.5 to 6.0 volts.

MS – MODE SELECT (PIN 10)

The MS pin is a three-state input for switching between DTMF, 10 pps, and 20 pps dialing modes. The relationship between pin connection and operating mode is shown in Table 1 below.

Table 1. Mode Select Options

MS	Dialing Mode
V_{DD}	20 pps Pulse Dialing
Open	10 pps Pulse Dialing
V_{SS}	DTMF Tone Dialing

OH – ON-HOOK (PIN 12)

Connecting the OH pin to V_{DD}, or allowing it to float sets the device in the on-hook mode. Connecting this pin to V_{SS} selects the off-hook mode. When in the on-hook mode, repertory memory can be programmed without dialing output.

TSO – TONE SIGNAL OUTPUT (PIN 7)

In the pulse dialing mode, a 500 hertz tone signal is output after a valid key input has been accepted to provide the user with audio feedback for key depression. This pin also outputs a tone when on-hook programming is taking place.

DTMF OUT – DUAL TONE MULTIFREQUENCY OUTPUT (PIN 18)

When the MS pin is set to V_{SS} the DTMF OUT pin outputs tones corresponding to the row and column of the key depressed. In the pulse dialing mode (MS = V_{DD} or open), it is high impedance. For repertory memory programming purposes, this pin will not output DTMF when the OH pin is held to V_{DD}.

$\overline{OPL}$ – OUTPULSING (PIN 17)

The $\overline{OPL}$ pin is a N-channel transistor in an open drain configuration that outputs pulses at 10 pps (MS is open) or 20 pps (MS = V_{DD}), with a make/break ratio of 40/60. In the DTMF dialing mode (MS = V_{SS}), this output is a high impedance. For repertory memory programming purposes, this pin will not outpulse when the OH pin is held to V_{DD}.

$\overline{MO}$ – MUTE OUTPUT (PIN 11)

The Mute Output is an open drain, N-channel output that pulls to V_{SS} when a key is input during the DTMF dialing mode, or during outpulsing, or while DTMF is output during auto redialing.

KEYBOARD INPUTS – (PINS 2, 3, 4, 5, 13, 14, 15, 16)

The keyboard inputs allow either a single contact (Class A) keyboard, or a standard 2-of-8 (7) keyboard with V_{SS} tied to common. A valid key entry occurs when either a single row is tied to a single column or a single row and column are simultaneously connected to V_{SS}. Typical keyboard configurations are shown in Figure 1. Connecting pin 2, $\overline{COL\ 4}$, to V_{DD} sets the part for 3×4 keyboard interface mode. Keyboard mode selection is performed at power-up.

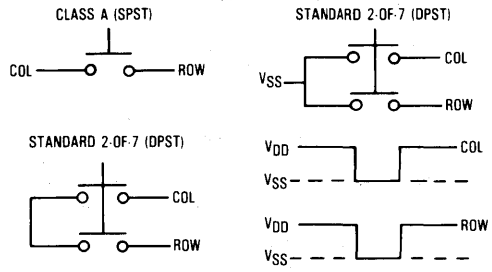


Figure 1. Keyboard Configurations

OSCin, OSCout (PIN 8, PIN 9)

A 3.579545 megahertz crystal is required as the frequency reference for the on chip oscillator. Crystal biasing is accomplished by an internal resistor and capacitors.

GENERAL DEVICE DESCRIPTION

On power-up there is a 64 millisecond initialization period during which the oscillator is enabled and the keyboard inputs are disabled. A stop code is inserted into the first digit of all ten RAM locations and the $\overline{COL\ 4}$ input is scanned. If the $\overline{COL\ 4}$ input is high (V_{DD}) the dialer is set to the 3×4 keypad mode, otherwise the 4×4 keypad mode is selected. Changing modes is not possible after this power-up period.

NORMAL DIALING

Responses to dialing sequences for 4×4 keyboards are shown in Table 2; 3×4 keyboard responses are shown in Table 3.

For normal dialing, the oscillator starts when a key is depressed. The key input is debounced for 32 millisecond. During this debounce period, while the RAM and dialing circuit are disabled, the mode select pin is scanned to determine the dialing mode (either 10 pps, or 20 pps, or DTMF). Note that if the RAM and dialing circuit are active (i.e., during dialing or associated timing), a change at the mode select pin will not be detected. The MC145413 provides a PAUSE/SWITCH function, allowing dialing mode changes to be selected from the keypad during the dialing sequence without waiting. After the debounce period, the input is checked for validity, then latched into last number redial memory. As each digit is entered, stored in the last number redial memory, and a stop code is written in the next address. This process continues until 18 digits have been entered. If a 19th digit is entered, it will be stored in the first address followed by a stop code in the second address. When dialing, the device fetches data from memory until a stop code is encountered or 18 digits have been dialed.

For a DTMF dialing sequence, the DTMF is output in 32 millisecond intervals as long as the key is depressed after the debounce period. The DTMF OUT pin is designed to drive an external bipolar transistor which can be used to modulate Tip to Ring voltage at the DTMF frequencies. With the exception of column four, multiple key inputs in any one column or row will result in the corresponding column or row frequency to be output. Multiple key depressions on a diagonal will not cause any output. When configured for the 3×4 keyboard, outputing the tone pairs for # and * require two depressions of the desired key.

When pulse dialing, each successive number is stored in last number redial memory as it is input, then outpulsed in sequence with the appropriate timing. The $\overline{OPL}$ output can be connected to an external bipolar transistor, which is used to pulse the telephone line by momentarily connecting and disconnecting the speech network from line power.

The duration of the dialing sequences can extend beyond the time taken to push the keys for both DTMF and pulse dialing modes. Although DTMF is only output as long as the key is depressed during manual dialing, each key depression causes the dialing circuit to go through a 200 millisecond cycle corresponding to the timing for DTMF auto-dialing. These times accumulate during the dialing process. For pulse dialing, outpulsing can extend well beyond the time it takes to enter the digits. Changing the input at the mode select pin will not be recognized until the accumulation of these timing sequences has elapsed.

FEATURES

For the 4×4 keyboard, a last number redial can be accomplished if the RED/P key ($\overline{COL\ 4}$, $\overline{ROW\ 1}$) is the first key depressed after a transition from on-hook to off-hook. Otherwise, the RED/P key will cause a four second pause. If the pulse mode is selected, redial can be accomplished if the first key depressed on a transition to off-hook is #. For the 3×4 keyboard, redial occurs if the sequence, *, 0 is entered. Last number redial memory can also be referred to as memory location 0. In the pulse mode, if the first key entered after a transition to off-hook is #, a redial will be initiated.

The MC145412/13 can be configured with an external battery to provide memory retention power and allow on-hook programming of the repertory memory. If the part is in the on-hook mode, and a key is depressed, the oscillator will start, and the key's code will be stored in the last number redial memory, as during off-hook operation. Dialing outputs will not be activated while the device is in the on-hook condition. After the number has been entered in the on-hook mode, it can be stored in repertory memory. For the 4×4 keyboard, pressing the STORE Key (* for 3×4 keyboard), followed by a digit (1 through 9) will store the number in the repertory memory location specified by the digit.

The RECALL key ($\overline{COL\ 4}$, $\overline{ROW\ 4}$) for the 4×4 keypad is used to recall and dial numbers stored in the repertory memory. The digit immediately following the RECALL key designates the memory location of the number to be auto-dialed. For the 3×4 keyboard, recall is accomplished by depressing the * key followed by the appropriate digit, only when the device is in the off-hook mode.

The PAUSE key ($\overline{COL\ 4}$, $\overline{ROW\ 2}$) for the MC145412 will cause a four second pause. The PAUSE/S key ($\overline{COL\ 4}$, $\overline{ROW\ 2}$) is a feature offered on the MC145413. If a pulse dialing mode is selected (MS = V_{DD} or OPEN), depressing this key will cause a four second delay, and switch dialing mode to DTMF. A subsequent PAUSE/S input will cause the dialing mode to change back to Pulse (which ever pulse mode is selected on MS). If MS = V_{SS}, pressing the PAUSE/S key will cause a four second delay but no mode change. These functions can also be stored in memory for pauses (and mode switching) during auto-dialing. Just as with manual dialing, mode changes in auto dialing will only occur if MS ≠ 0 (V_{SS}) when auto dialing is initiated.

Table 2. 4×4 Keyboard Dialing Sequences

Key	Dialing Mode	Function	Notes
RED/P	DTMF/PULSE	If first key after transition to OFF-HOOK, redial the last number. Otherwise, pause four seconds.	
PAUSE	DTMF/PULSE	Pause four seconds.	MC145412 only
PAUSE/S	DTMF/PULSE	Pause four seconds then switch dialing modes.	MC145413 only
STORE	DTMF/PULSE	Go to STORE mode. Upon input of memory location number, store contents of Last Number Redial memory into location specified.	
RECALL	DTMF/PULSE	Go to RECALL mode. Upon input of memory location number, recall and dial the number in that memory location.	
#	DTMF	Output COL 3/ROW 4 tones.	
	PULSE	If # is the first key input upon a transition to OFF-HOOK, Last Number Redial is initiated; otherwise, it is ignored.	
*	DTMF	Output COL 1/ROW 4 tones.	
	PULSE	Pause four seconds.	
0-9	DTMF/PULSE	Data input for dialing (unless preceeded by STORE or RECALL)	See STORE and RECALL functions

4×4 Key Matrix

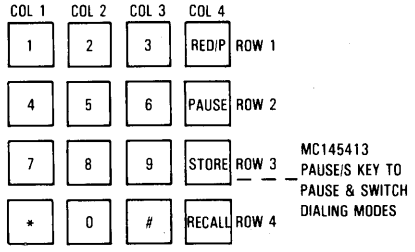


Table 3. 3×4 Keyboard Dialing Sequences

Keys	Dialing Mode	Function	Notes
0-9	DTMF/PULSE	Data input for dialing unless preceeded by * or #.	See * and #.
*	DTMF/PULSE	Go to * mode and await next input.	
*, *	DTMF	Output COL 1/ROW 4 tones.	
	PULSE	No response.	
*, #	DTMF/PULSE	Pause four seconds.	
*, 0	DTMF/PULSE	OH = V_{DD} or float (ON-HOOK) — stay in * mode.	See *, 0-9
*, 0-9	DTMF/PULSE	OH = V_{SS} (OFF-HOOK) — Recall and dial number from memory location specified by digit.	0 is last no. redial; see *, 0
*, 1-9	DTMF/PULSE	OH = V_{DD} or float (ON-HOOK) — Store number in Last Number Redial memory into memory location specified by digit.	
#	DTMF	Go to # mode and await next input.	#
	PULSE	Pause four seconds.	No # mode for PULSE
#, #	DTMF	Output COL 3/ROW 4 tones.	
	PULSE	Pause eight seconds.	
#, *	DTMF	Go to * mode.	
#, 0-9	DTMF	Output appropriate DTMF tones.	

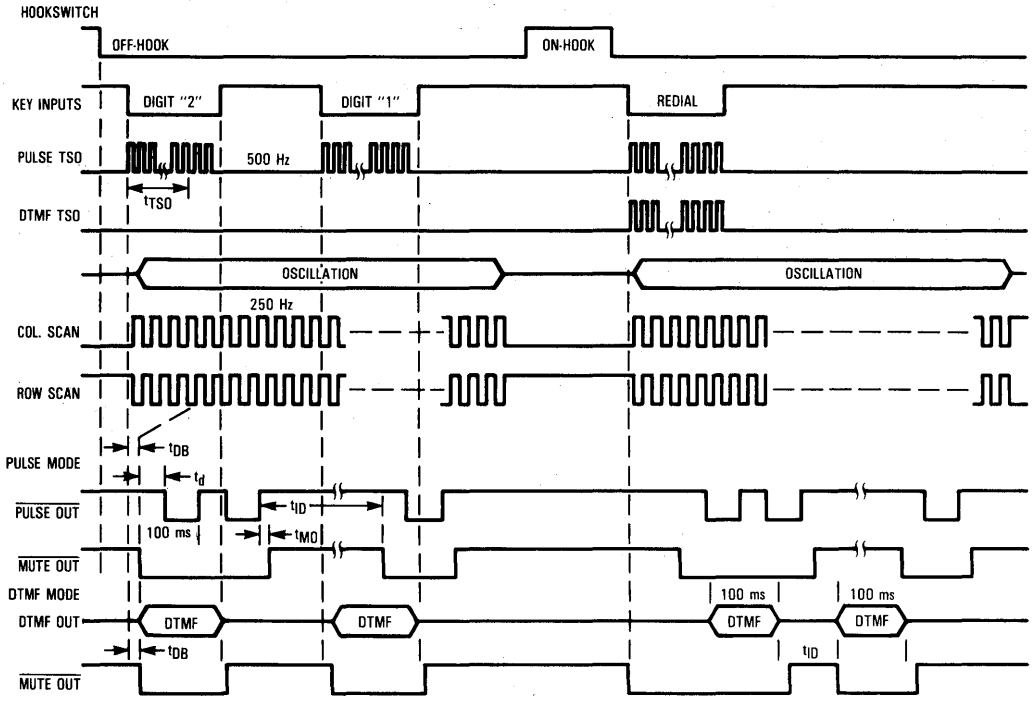


Figure 2. Timing Diagram

MOTOROLA

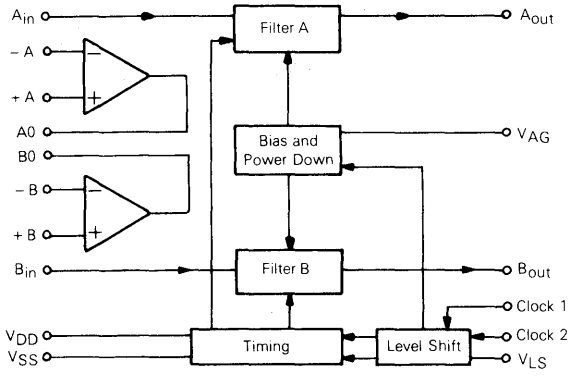
MC145414

DUAL TUNABLE LOW PASS SAMPLED DATA FILTERS

The MC145414 is sampled data, switched capacitor filter IC intended to provide band limiting and signal restoration filtering. It is capable of operating from either a single or split power supply and can be powered-down when not in use. Included on the IC are two totally uncommitted op amps for use elsewhere in the system as I to V converters, gain adjust buffers, etc.

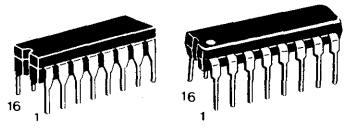
- Two General Purpose 5th Order Elliptic Low Pass Filters
- Low Operating Power Consumption — 30 mW (Typical)
- Power Down Capability — 1 mW (Maximum)
- ±5 to ±8 Volt Power Supply Ranges
- TTL or CMOS Compatible Inputs Using VLS Pin
- Two Operational Amplifiers Available to Reduce Component Count
- Useful in LPC or CVSD Speech Applications
- Passband Edges Tunable With Clock Frequency From 1.25 kHz to 10 kHz

BLOCK DIAGRAM



CMOS LSI
(LOW-POWER COMPLEMENTARY MOS)

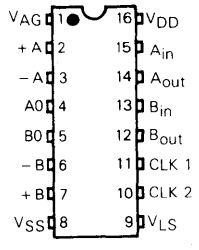
DUAL TUNABLE LOW PASS SAMPLED DATA FILTERS



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

PIN ASSIGNMENT



ORDERING INFORMATION

MC14XXXX
- L Ceramic Package
- P Plastic Package

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}-V_{SS}	−0.5 to 18	V
Input Voltage, All Pins	V_{in}	−0.5 to V_{DD} +0.5	V
DC Current Drain per Pin (Excluding V_{DD}, V_{SS})	I	10	mA
Operating Temperature Range	T_A	0 to 85	°C
Storage Temperature Range	T_{stg}	−65 to 150	°C

2

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
DC Supply Voltage	V_{DD}-V_{SS}	10	12	16	V
Clock 1, 2 Frequency	CLK 1, 2	50	128	400	kHz

DIGITAL ELECTRICAL CHARACTERISTICS (V_{SS} = 0 V)

Characteristic		Symbol	V_{DD} Vdc	25°C Min	25°C Typ	25°C Max	Unit
Operating Current		I_{DD}	12	–	2.0	4.0	mA
Power-Down Current (PDI = V_{SS})		I_{PD}	12	–	10	40	μA
Input Capacitance		C_{in}	12	–	5.0	–	pF
MODE CONTROL LOGIC LEVELS							
VLS Power-Down Mode		V_{IH}	12 15	11.5 14.5	11 13	– –	V
VLS TTL Mode		–	12 15	4.0 5.0	– –	8 9	V
VLS CMOS Mode		V_{IL}	12 15	– –	– –	0.8 0.8	V
VAG Power-Down Mode		V_{IH}	12 15	11.5 14.5	10.5 13.5	– –	V
VAG Analog-Ground Mode		V_{IL}	12 15	– –	– –	7.0 9.0	V
CMOS LOGIC LEVELS (V_{LS} = V_{SS})							
Input Current Clock 1, 2 (Internal Pulldown Resistors)	"1" Level "0" Level	I_{in}	12 12	– –	50 −0.00001	100 −0.3	μA
Input Voltage Clock 1, 2	"0" Level	V_{IL}	12 15	– –	5.25 6.75	3.0 3.5	V
	"1" Level	V_{IH}	12 15	9.0 11.5	6.75 8.25	–	V
TTL LOGIC LEVELS (VLS = 6 V, V_{SS} = 0 V)							
Input Current Clock 1, 2 (Internal Pulldown Resistor)	"1" Level "0" Level	I_{in}	12 12	– –	50 −0.00001	100 −0.3	μA
Input Voltage Clock 1, 2	"0" Level "1" Level	V_{IL} V_{IH}	12 12	– V_{LS} + 2.0	– –	VLS + 0.8 –	V

ANALOG ELECTRICAL CHARACTERISTICS (V_{DD} = 12 V)

Characteristic		Symbol	25°C			Unit
			Min	Typ	Max	
Input Current	A_{in}, B_{in}	I_{in}	–	±0.00001	±1.0	μA
Input Current	VAG	I_{in}	–	±0.00001	±10	μA
AC Input Impedance (1 kHz)	A_{in}, B_{in}	Z_{in}	–	2	–	MΩ
Input Common Mode Voltage Range	A_{in}, B_{in}, +A, −A, +B, −B	V_{ICR}	2.0	–	10.0	V
Input Offset Current	+A to −A, +B to −B	I_{ID}	–	±10	–	nA
Input Bias Current	+A, −A, +B, −B	I_{IB}	–	±0.10	±1.0	nA
Input Offset Voltage	+A to −A, +B to −B	V_{ID}	–	±10	±70	mV
Output Voltage Range (R_L = 20 kΩ to VAG, R_B = ∞) (R_L = 600 Ω to VAG, R_B = 1.6 kΩ to V_{DD}) (R_L = 900 Ω to VAG, R_B = 1.8 kΩ to V_{DD})	A0, B0, A_{out}, B_{out}	V_{OR}	 1.5 3.0 2.5	 – – –	 10.5 8.3 9.0	V
Small Signal Output Impedance (1 kHz)	A_{out} B_{out}	Z_o	– –	50 50	– –	Ω
Output Current (V_O = 10.5 V) (V_O = 1.5 V)	 A_{out}, B_{out}, A0, B0 A_{out}, B_{out}, A0, B0	 I_{OH} I_{OL}	 −200 5	 −400 7.5	 – –	 μA mA
Unity Gain Output Noise	A0, B0	–	–	15	–	μVrms

FILTER A SPECIFICATIONS

($V_{DD} - V_{SS}$ = 12 V, Clock 1, 2 = 128 kHz, V_{in} = −10 dBm0, full scale = +3 dBm0, 7 V p-p)

Characteristic		25°C			Unit
		Min	Typ	Max	
Gain (1020 Hz)		17.4	18	18.6	dB
Passband Ripple (50 Hz to 3000 Hz)		–	0.24	1.0	dB
Out of Band Response 3400 Hz 4000 Hz-4600 Hz 4600 Hz-64 kHz		 – −10 −25	 −0.8 −15.5 −33.0	 −1.5 – –	dB
Output Noise (A_{in} = VAG)	ref to 900 Ω	–	10	17	dBrnc0
Dynamic Range		76	83	–	dB
Differential Group Delay 1150 to 2300 Hz Delay 1000 to 2500 Hz Delay 800 to 2700 Hz Delay		 – – –	 – – –	 – – –	μs
Power Supply Rejection Ratio (V_{DD} = 12 V + 0.1 V_{RMS} @ 1 kHz)		–	36	–	dB
Crosstalk (A_{in} = VAG, B_{in} = 0 dBm0 Output at A_{out} at 3 kHz)		–	76	–	dB

FILTER B SPECIFICATIONS ($V_{DD} - V_{SS}$ = 12 V, Clock 1, 2 = 128 kHz, V_{in} = −10 dBm0, full scale = +3 dBm0, 7 V p-p)

Characteristic	25°C			Unit
	Min	Typ	Max	
Gain (1020 Hz)	−0.7	±0.15	+0.7	dB
Passband Ripple (300 Hz to 3000 Hz)	–	0.22	1.0	dB
Response 3400 Hz 4000 Hz-4600 Hz 4600 Hz-64 kHz	 – −10 −28	 −0.8 −15.5 −33.0	 −1.7 – –	dB
Output Noise (300 Hz-3400 Hz)	–	8	14	dBrnc0
Dynamic Range (7 V p-p Max)	79	87	–	dB
Differential Group Delay 1150 to 2300 Hz Delay 1000 to 2500 Hz Delay 800 to 2700 Hz Delay	 – – –	 – – –	 – – –	μs
Crosstalk (B_{in} = VAG, A_{in} = OdBm0 @ 3 kHz Output at B_{out} @ 3 kHz)	–	76	–	dB
Power Supply Rejection Ratio	–	36	–	dB

SWITCHING CHARACTERISTICS ($V_{DD} - V_{SS} = 10$ V, $T_A = 25°C$)

Characteristics		Symbol	0 to 70°C			Units
			Min	Typ	Max	
Input Rise Time Input Fall Time	Clock 1, 2	t_{TLH} t_{THL}	–	–	4	μs
Pulse Width	Clock 1, 2	t_{WH}	200	–	–	ns
Clock Pulse Frequency	Clock 1, 2	f_{CL}	50	–	400	kHz
Clock 1, 2 Duty Cycle		–	40	–	60	%

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FUNCTIONAL DESCRIPTION OF PINS

Pin 1 — V_{AG} (Analog Ground)
This pin should be held at approximately (V_{DD}-V_{EE})/2. All analog inputs and outputs are referenced to this pin. If this pin is brought to within approximately 1.0 V of V_{DD}, the chip will be powered down.

Pin 2 — +A
Non-inverting input of op-amp A.

Pin 3 — −A
Inverting input of op-amp A.

Pin 4 — A0
Output of uncommitted op-amp A.

Pin 5 — B0
Output of uncommitted op-amp B.

Pin 6 — −B
Inverting input of op-amp B.

Pin 7 — +B
Non-inverting input of op-amp B.

Pin 8 — V_{SS}
This is the most negative supply pin and digital ground for the package.

Pin 9 — V_{LS} (Logic Shift Voltage)
The voltage on this pin determines the logic compatibility for the Clock 1, 2 inputs. If V_{LS} is within 0.8 V of V_{SS}, the thresholds will be for CMOS operating between V_{DD} and V_{SS}. If VLS is within 1.0 V of V_{DD}, the chip will power down. If V_{LS} is between $V_{DD}-2$ V and $V_{SS}+2$ V, the thresholds for logic inputs at Clock 1, 2 will be between $V_{LS}+0.8$ V and $V_{LS}+2.0$ V for TTL compatibility.

Pin 10 — Clock 1
Always tie clock 1 and clock 2 together.

Pin 11 — Clock 2
Always tie clock 1 and clock 2 together.

Pin 12 — B_{out} (Lowpass Filter B)
This is the output of B lowpass filter.

Pin 13 — B_{in} (Lowpass Filter B)
This is the input to filter B.

Pin 14 — A_{out} (Low pass Filter A)
This pin is the output to filter A.

Pin 15 — A_{in} (Lowpass Filter A)
This is the input to filter A.

Pin 16 — V_{DD}
Nominally 12 volts.

NOTE: Both VAG and VLS are high-impedance inputs.

FILTER DESCRIPTION

FILTER A DESCRIPTION

Filter A of the MC145414 is a 5-pole elliptic tunable lowpass filter operating at a sampling rate determined by clock 1 and clock 2. This filter provides band limiting that is a direct function of clock 1 and clock 2. With a 128 kHz clock, the band limiting frequency is 3.6 kHz. By dividing the clock in half to 64 kHz, the band limiting frequency is cut in half to 1.8 kHz (as illustrated in Figure 1). Likewise by doubling the clock, the cutoff point will double (as illustrated in Figures 3 and 4). The clock frequency can be varied from 50 kHz to 400 kHz. Filter A, unlike filter B, has a gain of 18 db. Because the MC145414 is a switch capacitance filter, the sampled output signal will have switching noise present near multiples of the switching frequency; a single-pole RC filter may be required to reduce this.

To provide 50/60 Hz and 15 Hz rejection, a 3-pole Chebychev highpass filter can be externally realized with the MC145414 by using the uncommitted op-amps as an active filter. This is shown in Figure 5 and 6.

FILTER B DESCRIPTION

Filter B in the MC145414 consists of a 5-pole elliptic tunable lowpass filter operating at a sampled rate determined by clock 1 and clock 2. Filter B is functionally similar to filter A, except filter B has unity gain.

Clock 1 and 2

Logic levels of these signals can be either TTL or CMOS compatible. Choice of logic level can be user determined by applying the appropriate voltage to the level shift control pin, VLS. Clock 1, 2 pins should be tied together.

Power Down

The MC145414 may be powered down by bringing VAG to within 1.7 V of V_{CC} or by bringing VLS to within 1.7 V of V_{DD}

FIGURE 1 — FILTER A AND B LOWPASS CHARACTERISTICS WITH CLOCK 1 AND 2 AT 64 kHz

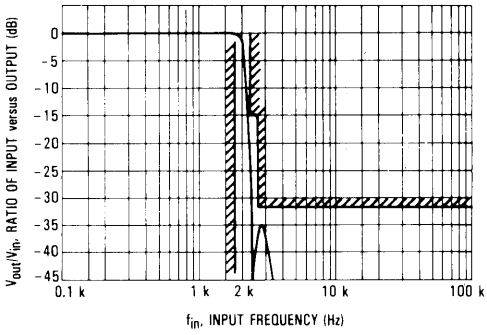


FIGURE 2 — FILTER A AND B LOWPASS CHARACTERISTICS WITH CLOCK 1 AND 2 AT 128 kHz

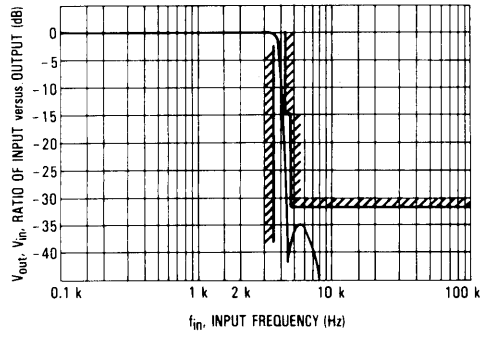


FIGURE 3 — FILTER A AND B LOWPASS CHARACTERISTICS WITH CLOCK 1 AND 2 AT 256 kHz

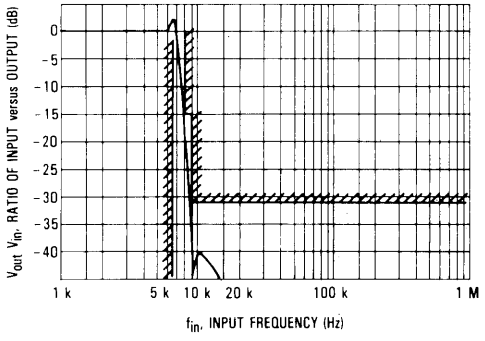


FIGURE 4 — FILTER A AND B LOWPASS CHARACTERISTICS WITH CLOCK 1 AND 2 AT 400 kHz

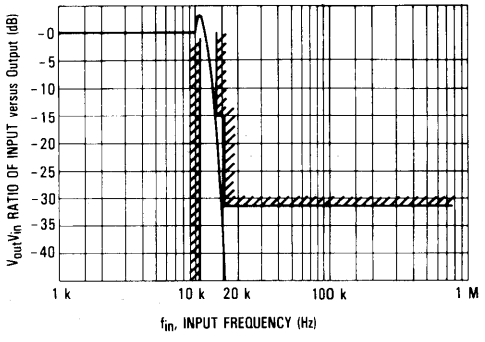
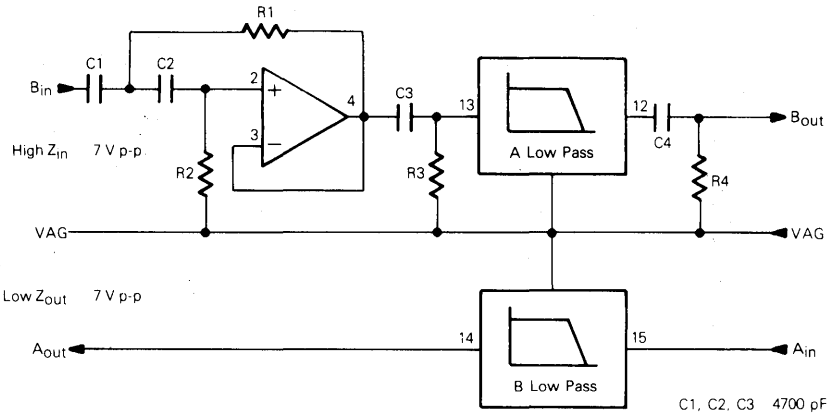


FIGURE 5 — FILTER SCHEMATIC FOR MC145414 WITH 60 Hz REJECT FILTER

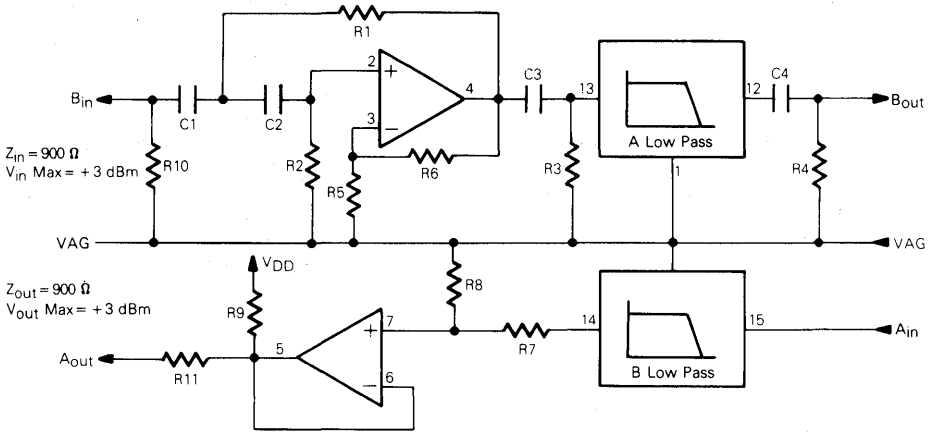


C1, C2, C3	4700 pF	±1%
C4	0.2 μF	−20% +80%
R1	112 kΩ ¼ W	1%
R2	620 kΩ ¼ W	1%
R3	223 kΩ ¼ W	1%
R4	100 kΩ ¼ W	10%

NOTE: In noisy environment, R1-R4 should be 10 kΩ or less to minimize pickup.

AD0318

FIGURE 6 — FILTER SCHEMATIC FOR MC145414 WITH 60 Hz REJECTION AND 900 TERMINATION

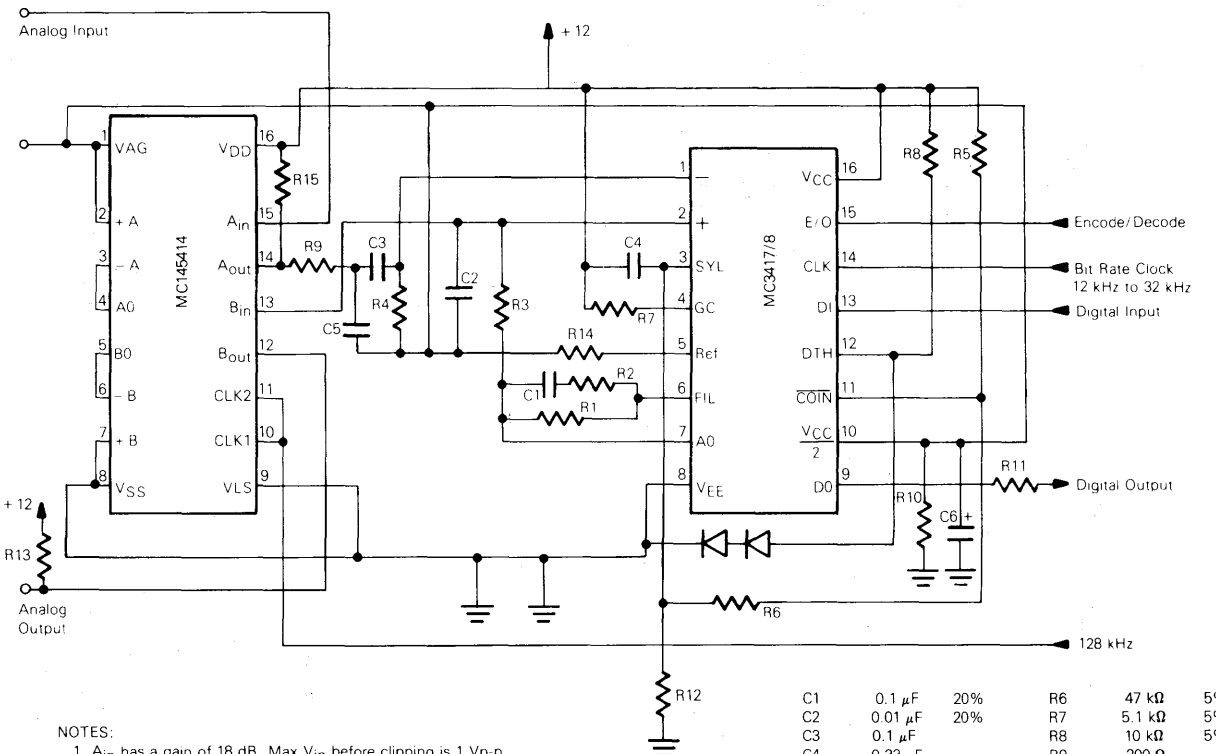


C1, C2, C3	4700 pF	±1%	R6	169 kΩ ¼ W	1%
C4	0.2 μF	−20% +80%	R7	24 kΩ ¼ W	1%
R1	236 kΩ ¼ W	1%	R8	33 kΩ ¼ W	1%
R2	294 kΩ ¼ W	1%	R9	1.8 kΩ ¼ W	10%
R3	223 kΩ ¼ W	1%	R10	900 Ω ¼ W	1%
R4	100 kΩ ¼ W	10%	R11	900 Ω ¼ W	1%
R5	200 kΩ ¼ W	1%			

AD0319

NOTE: In noisy environment, R1-R4 should be 10 kΩ or less to minimize pickup.

FIGURE 7 – DELTAMOD VOICE DIGITIZER USING MC3417 AND MC145414



NOTES:
1. A_{in} has a gain of 18 dB. Max V_{in} before clipping is 1 Vp-p.
2. Clock must be full V_{DD} to V_{SS} swing.
3. Digital I/O on MC3417/18 is TTL compatible.

C1	0.1 μF	20%	R6	47 kΩ	5%
C2	0.01 μF	20%	R7	5.1 kΩ	5%
C3	0.1 μF		R8	10 kΩ	5%
C4	0.33 μF		R9	200 Ω	
C5	0.1 μF		R10	1 kΩ	
C6	10 μF		R11	4.7 kΩ	
R1	9.6 kΩ	5%	R12	22 M	
R2	400 kΩ	5%	R13	2 kΩ	
R3	7.5 kΩ	5%	R14	10 kΩ	
R4	15 kΩ	5%	R15	2 kΩ	
R5	8.2 kΩ	5%			

MOTOROLA

MC145415

Advance Information

2

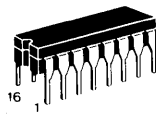
DUAL TUNABLE LINEAR PHASE LOW-PASS SAMPLED DATA FILTERS

The MC145415 is sampled data, switched capacitor filter IC intended to provide band limiting and signal restoration filtering. It is capable of operating from either a single or split power supply and can be powered-down when not in use. Included on the IC are two uncommitted comparators for use elsewhere in the system.

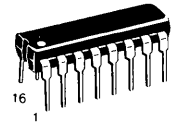
- Two Linear Phase 5th Order Low-Pass Filters
- Low Operating Power Consumption — 20 mW (Typical)
- ±2.5 to ±8 Volt Power Supply Ranges
- CMOS Compatible Inputs Using V_{DG} Pin
- Two Comparators Available to Reduce Component Count
- Useful in High Speed Data Modem Applications
- Pass-Band Edges Tunable With Clock Frequency from 1.25 kHz to 10 kHz

CMOS LSI
(LOW-POWER COMPLEMENTARY MOS)

DUAL TUNABLE LINEAR PHASE LOW-PASS SAMPLED DATA FILTERS

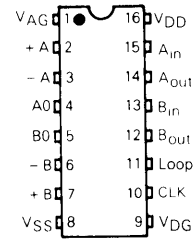


L SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648

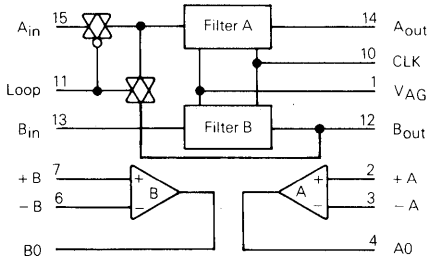
PIN ASSIGNMENT



ORDERING INFORMATION

MC14XXXX
- L Ceramic Package
- P Plastic Package

BLOCK DIAGRAM



V_{DG} = Pin 9
V_{DD} = Pin 16

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

This document contains information on a new product. Specifications and information herein are subject to change without notice.

ANALOG ELECTRICAL CHARACTERISTICS (V_{DD} = 12 V, V_{SS} = 0, V_{AG} = V_{DD}/2, T_A = −40 to 85°C)

Characteristic		Symbol	Min	Typ	Max	Unit
Input Current	A_{in}, B_{in}	I_{in}	–	±0.00001	±10	μA
Input Current	V_{AG}	I_{in}	–	±0.00001	±50	μA
AC Input Impedance (1 kHz)	A_{in}, B_{in}	Z_{in}	–	2	–	MΩ
Input Common Mode Voltage Range	A_{in}, B_{in}, +A, −A, +B, −B	V_{ICR}	2.0	–	10.0	V
Input Offset Current	+A to −A, +B to −B	I_{ID}	–	±10	–	nA
Input Bias Current	+A, −A, +B, −B	I_{IB}	–	±0.10	±1.0	nA
Input Offset Voltage	+A to −A, +B to −B	V_{ID}	–	±10	±70	mV
Output Voltage Range	A_{out}, B_{out}	V_{OR}				V
(R_L = 20 kΩ to V_{AG}, R_B = ∞)			1.5	–	10.5	
(R_L = 900 Ω to V_{AG}, R_B = 1.8 kΩ to V_{DD})			2.5	–	9.0	
(R_L = 600 kΩ to V_{AG}, R_B = 1.6 kΩ to V_{DD})			3.0	–	8.3	
Small Signal Output Impedance (1 kHz)	A_{out}	Z_o	–	50	–	Ω
	B_{out}		–	50	–	
Output Current						
(V_O = 10.5 V)	A_{out}, B_{out}	I_{OH}	−200	−400	–	μA
(V_O = 1.5 V)	A_{out}, B_{out}	I_{OL}	5	7.5	–	mA
Comparator Output Current	A0, B0					
(V_O = 9.5 V)		I_{OH}	−1.1	−2.25	–	mA
(V_O = 0.5 V)		I_{OL}	−3.0	−8.8	–	

FILTER A SPECIFICATIONS ($V_{DD} - V_{SS}$ = 12 V, Clock = 153.6 kHz, V_{in} = 0 dBm0, full scale = +3 dBm0, 0.875 V p-p, T_A = −40 to 85°C)

Characteristic	Min	Typ	Max	Unit
Gain (300 Hz)	17	18	19	dB
Responses (Ref. 300 Hz)				dB
2400 Hz	−3.6	−3.0	−2.4	
4800 Hz	−16	−13.8	−12.8	
Idle Noise (A_{in} = V_{AG}, Ref. to 600 Ω)	–	13	24	dBrnc
Dynamic Range (Full Scale Output/Idle Noise)	76	87	–	dB
Deviation From Linear Phase dc to 2400 Hz	–	2.5	–	deg
Power Supply Rejection Ratio (V_{DD} = 12 V + 0.1 V_{RMS} @ 1 kHz)	–	36	–	dB
Crosstalk (A_{in} = V_{AG}, B_{in} = 0 dBm0, Output at A_{out} at 3 kHz)	–	76	–	dB

FILTER B SPECIFICATIONS ($V_{DD} - V_{SS}$ = 12 V, Clock = 153.6 kHz, V_{in} = 0 dBm0, full scale = +3 dBm0, 7 V p-p, T_A = −40 to 85°C)

Characteristic	Min	Typ	Max	Unit
Gain (300 Hz)	−0.7	±0.15	+0.7	dB
Response (Ref. 300 Hz)				dB
2400 Hz	−3.6	−3.0	−2.4	
4800 Hz	−16	−14.1	−12.8	
Idle Noise (300 Hz, Ref to 600 Ω)	–	9	24	dBrnc
Dynamic Range (Full Scale Output/Idle Noise)	76	91	–	dB
Deviation From Linear Phase (dc to 2400 Hz)	–	2.5	–	deg
Power Supply Rejection Ratio (V_{DD} = 12 V + 0.1 V_{RMS} @ 1 kHz)	–	36	–	dB
Crosstalk (B_{in} = V_{AG}, A_{in} = 0 dBm0 @ 2 kHz, Output at B_{out})	–	76	–	dB

MAXIMUM RATINGS (V_{SS} = 0)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}-V_{SS}	−0.5 to 18	V
Input Voltage, All Pins	V_{in}	−0.5 to V_{DD} +0.5	V
DC Current Drain per Pin (Excluding V_{DD}, V_{SS})	I	10	mA
Operating Temperature Range	T_A	−40 to 85	°C
Storage Temperature Range	T_{stg}	−65 to 150	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
DC Supply Voltage	V_{DD}-V_{SS}	4.5	5	16	V
Clock Frequency*	CLK	50	128	400	kHz

*Filter frequency response may degrade slightly as clock frequency is increased above 200 kHz.

DIGITAL ELECTRICAL CHARACTERISTICS (V_{DD} = 10 V, V_{SS} = 0 V, V_{AG} = V_{DD}/2, T_A = −40 to 85°C)

Characteristic	Symbol	Min	Max	Unit
Operating Current	I_{DD}	–	4	mA
Input Capacitance	C_{in}	–	10	pF
Input Low Voltage (Pins 10, 11)	V_{IL}	–	V_{DG} + 0.3 (V_{DD} − V_{DG})	V
Input High Voltage (Pins 10, 11)	V_{IH}	0.7 × (V_{DD} − V_{DG}) + V_{DD}	–	V
Input Leakage Current (Pins 10, 11)	I_{IL}	V_{DD} − 0.3 (V_{DD} − V_{DG})	2.5	μA
V_{DG} Reference Voltage (Pin 9)	V_{DG}	V_{SS}	V_{DD} − 4.5	V

SWITCHING CHARACTERISTICS ($V_{DD} - V_{SS} = 12$ V, $T_A = -40$ to 85°C)

Characteristics	Symbol	Min	Typ	Max	Units
Input Rise Time (Pin 10)	t_{TLH}	–	–	4	μs
Input Fall Time (Pin 10)	t_{THL}	–	–	4	μs
Pulse Width (Pin 10)	t_{WH}	200	–	–	ns
Clock Pulse Frequency (Pin 10)	f_{CL}	50	–	400	kHz
Clock Duty Cycle (Pin 10)	–	40	–	60	%

FUNCTIONAL DESCRIPTION OF PINS

V_{DD} (PIN 16)
Positive supply pin.

V_{SS} (PIN 8)
This is the most negative supply pin.

V_{AG}, ANALOG GROUND (PIN 1)
This pin should be held at approximately $(V_{DD} - V_{SS})/2$. All analog inputs and outputs are referenced to this pin.

+A (PIN 2)
Non-inverting input of comparator A.

–A (PIN 3)
Inverting input of comparator A.

A0 (PIN 4)
Output of comparator A. This is a standard 'B' series CMOS output.

B0 (PIN 5)
Output of comparator B. This is a standard 'B' series CMOS output.

–B (PIN 6)
Inverting input of comparator B.

+B (PIN 7)
Non-inverting input of comparator B.

V_{DG}, DIGITAL GROUND (PIN 9)
This pin is logic ground reference for the CLK and LOOP pins.

CLK, CLOCK (PIN 10)
This is the clock input that determines the location of the cutoff frequency of the filters as given below:

$$-3 \text{ dB frequency} = f_{CLK} \div 64$$

LOOP (PIN 11)
When this pin is high, the input to filter A is disconnected from the pad and shorted to the filter B output pin. With this pin low, the loop back mode is disabled.

B_{out}, LOW-PASS FILTER B OUTPUT (PIN 12)
This is the output from Filter B.

B_{in}, LOW-PASS FILTER B INPUT (PIN 13)
This is the input to filter B.

A_{out}, LOW-PASS FILTER A OUTPUT (PIN 14)
This pin is the output from Filter A.

A_{in}, LOW-PASS FILTER A INPUT (PIN 15)
This is the input to Filter A.

NOTE: V_{AG} is a high-impedance input.

FILTER DESCRIPTION

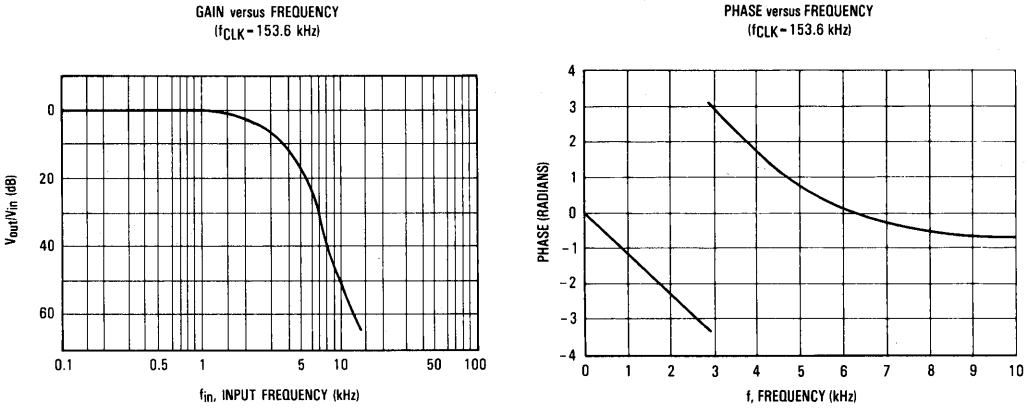
FILTER A DESCRIPTION

Filter A of the MC145415 is a 5-pole tunable linear phase low-pass filter operation at a sampling rate determined by the clock. The break frequency, which is a function of the clock, is calculated by dividing the input clock frequency by 64. With a 128 kHz clock, the band limiting frequency is 2 kHz. By dividing the clock in half to 64 kHz the band limiting frequency is cut in half to 1 kHz. Likewise, by doubling the clock, the cutoff point with double in frequency. The clock frequency can be varied from 50 kHz to 400 kHz. Filter A, unlike filter B, has a gain of 18 dB. Because the MC145415 is a switch capacitance filter, the sampled output signal will have switching components present near multiples of the switching frequency and inputs to these filters should be band-limited to under $\sim 3/4\ f_{CLK}$ to prevent aliasing.

FILTER B DESCRIPTION

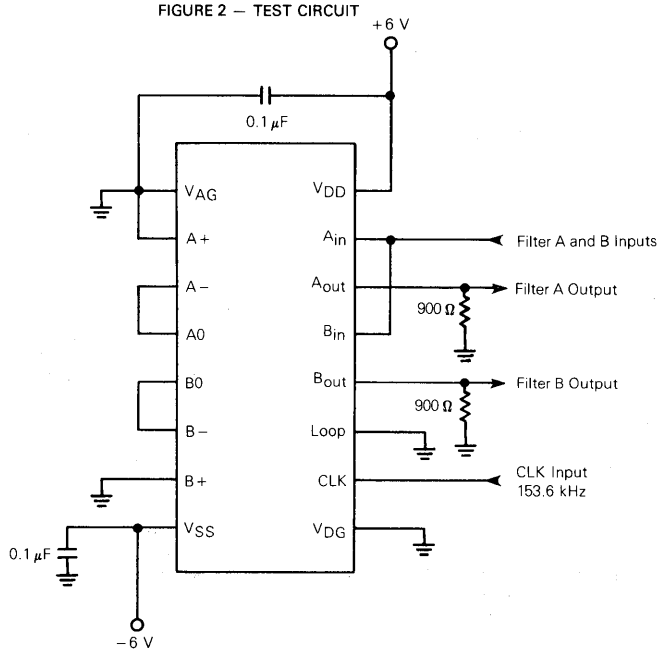
Filter B in the MC145415 consists of a 5-pole tunable linear phase low-pass filter operating at a sampled rate determined by the clock. Filter B is functionally similar to filter A, except filter B has unity gain.

FIGURE 1 — FILTER A AND B LOW-PASS CHARACTERISTICS



NOTES: 1. Break frequency is equal to the clock frequency ÷ 64.
2. Figure 1 illustrates Filter B performance.
Filter A would be 18 dB higher.

FIGURE 2 — TEST CIRCUIT

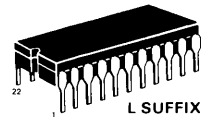


MC145418
MC145419

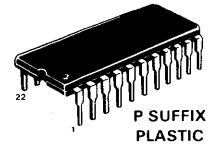
MOTOROLA

Advance Information

Digital Loop Transceivers (DLT)



L SUFFIX
CERAMIC
CASE 736



P SUFFIX
PLASTIC
CASE 708

2

The MC145418 and MC145419 DLTs are high-speed data transceivers that provide 80 kbps full duplex data communication. Intended primarily for use in digital subscriber voice/data telephone systems, these devices can also be used in any digital data transfer scheme (i.e., limited distance modems) where bidirectional data transfer is needed. These devices utilize a 256 kilobaud "squared" modified - DPSK burst modulation technique for transmission.

These devices are designed for compatibility with existing, as well as evolving, telephone switching hardware and software architectures.

The DLT chip set consists of the MC145418 master DLT for use at the telephone switch linecard and the MC145419 slave DLT for use at the remote digital telset and/or data terminal.

The devices employ CMOS technology in order to take advantage of its reliable low-power operation and proven capability for complex analog/digital LSI functions.

- Provides Full Duplex Synchronous 64 kbps Voice/Data Channel and Two 8 kbps Signalling/Data Channels
- Compatible with Existing and Evolving Telephone Switch Architectures and Call Signalling Schemes
- Full Duplex 80 Kilobits Transmission for an 8 kHz Frame Rate
- Protocol Independent
- Single 5 Volt Power Supply
- 22 Pin Package

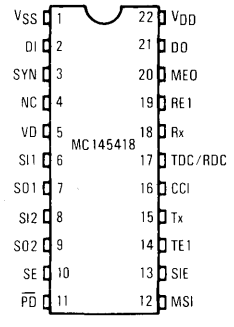
MC145418 Master DLT

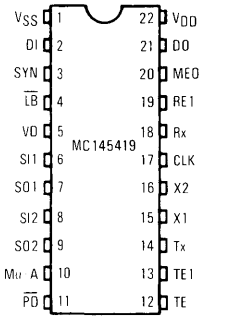
- Pin Controlled Power-Down Feature
- Signalling and Control I/O Capable of Sharing Common Bus Wiring with Other DLTs
- Variable Data Clock - 64 kHz to 2.56 MHz
- Pin Controlled Insertion/Extraction of 8 kbps Channel into LSB of 64 kbps Channel for Simultaneous Routing of Voice and Data Through PCM Voice Path of Telephone Switch

MC145419 Slave DLT

- Compatible with MC14400 Series PCM Mono-Circuits
- Pin Controlled Loop-Back Feature
- Automatic Power-Up Down Feature
- On-Chip Data Clock Recovery and Generation
- Pin Controlled 500 Hz D3 or CCITT Format PCM Tone Generator for Audible Feedback Applications

PIN ASSIGNMENTS

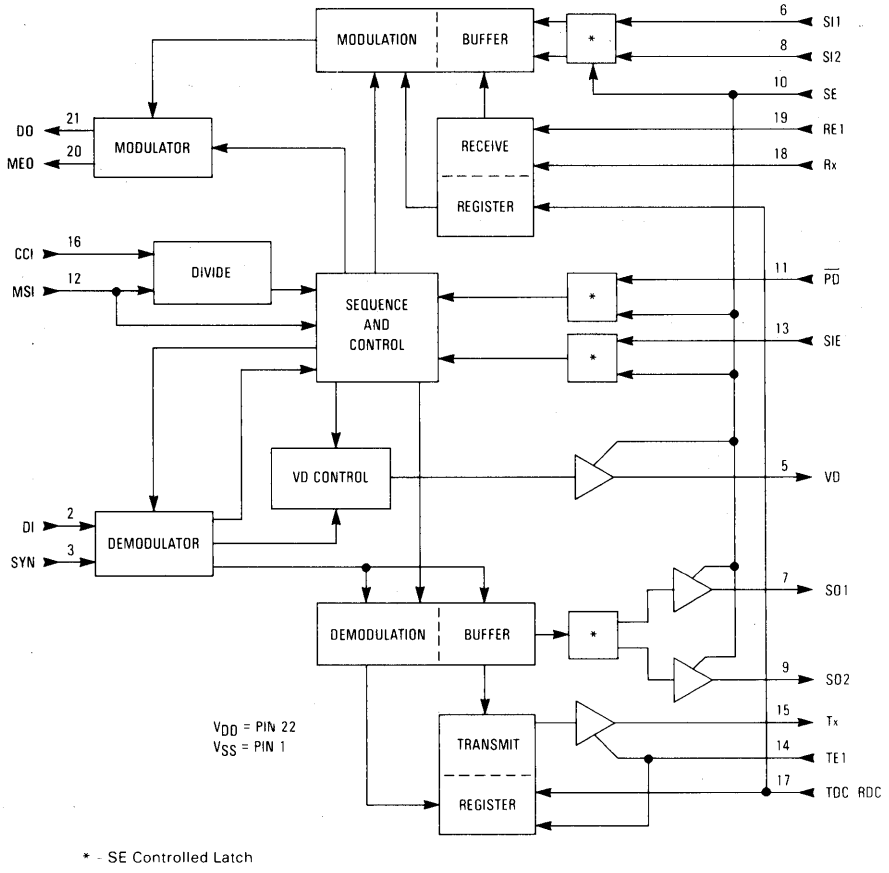




This document contains information on a new product. Specifications and information herein are subject to change without notice.

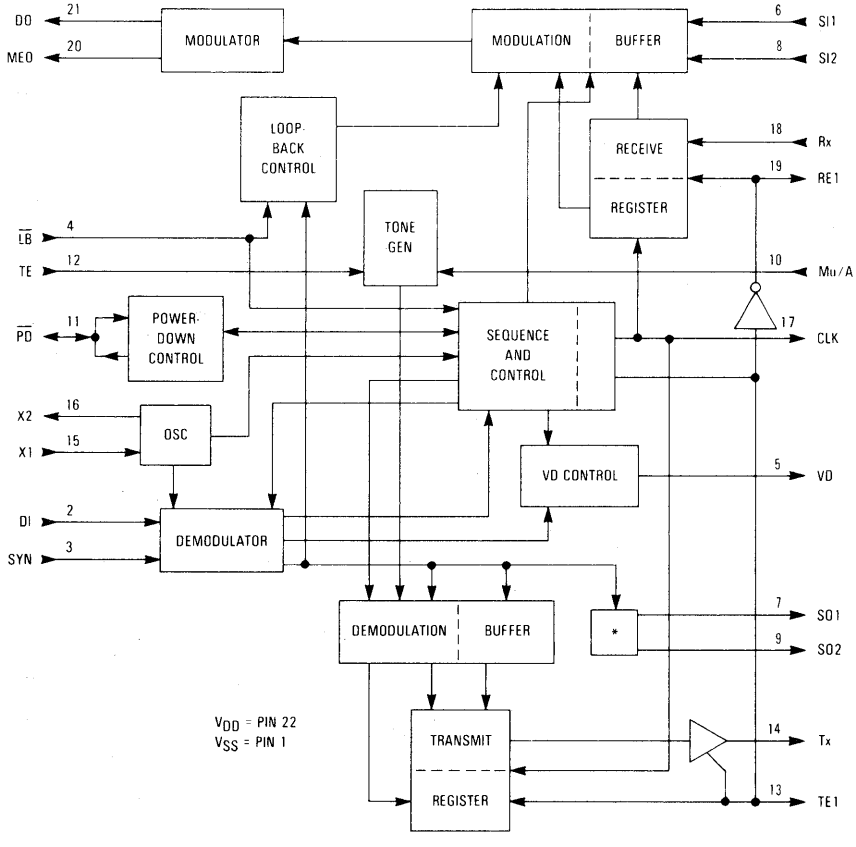
2

MC145418 MASTER DLT BLOCK DIAGRAM



* - SE Controlled Latch

MC145419 SLAVE DLT BLOCK DIAGRAM



* - Signal Bits Output Latch

ABSOLUTE MAXIMUM RATINGS (Voltage Referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to 9.0	V
Voltage, Any Pin to V_{SS}	V	-0.5 to V_{DD} +0.5	V
DC Current, Any Pin (Excluding V_{DD}, V_{SS})	I	±10	mA
Operating Temperature	T_A	-40 to +85	°C
Storage Temperature	T_{stg}	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to 70°C)

Parameter	Pins	Min	Max	Unit
DC Supply Voltage	V_{DD}	4.5	5.5	V
Power Dissipation ($\overline{PD}$ = V_{DD}, V_{DD} = 5 V)	V_{DD}	—	15	mW
Power Dissipation ($\overline{PD}$ = V_{SS}, TE = V_{SS})	V_{DD}	—	10	mW
Frame Rate MC145418	MSI	7.9	8.1	kHz
MC145418 - MC145419 Frame Rate Slip (See Note 1)	—	—	0.25	%
CCI Clock Frequency (MSI = 8 kHz)	CCI	—	2.048	MHz
Data Clock Rate MC145418	TDC, RDC	64	2560	kHz
Modulation Baud Rate (See Note 2)	DO	—	256	kHz

NOTES:
1. The MC145419 crystal frequency divided by 512 must equal the MC145418 MSI frequency ± 0.25% for optimum operation.
2. Assumes crystal frequency of 4.096 MHz for the MC145419 and 2.048 MHz CCI for the MC145418.

DIGITAL CHARACTERISTICS (V_{DD} = 5 V, T_A = 0 to 70°C)

Parameter		Min	Max	Unit
Input High Level		3.5	—	V
Input Low Level		—	1.5	V
Input Current		—	±1.0	μA
Input Capacitance			10	pF
Output High Current (Except Tx on MC145418 and Tx and $\overline{PD}$ on MC145419)	V_{OH} = 2.5 V V_{OH} = 4.6 V	-1.7 -0.36	— —	mA
Output Low Current (Except Tx on MC145418 and Tx and $\overline{PD}$ on MC145419)	V_{OL} = 0.4 V V_{OL} = 0.8 V	0.36 0.8	— —	mA
$\overline{PD}$ Output High Current (MC145419) (See Note 5)	V_{OH} = 2.5 V V_{OH} = 4.6 V	-90 -10	— —	μA
$\overline{PD}$ Output Low Current (MC145419) (See Note 5)	V_{OL} = 0.4 V V_{OL} = 0.8 V	60 100	— —	μA
Tx Output High Current	V_{OH} = 2.5 V V_{OH} = 4.6 V	-3.4 -0.7	— —	mA
Tx Output Low Current	V_{OL} = 0.4 V V_{OL} = 0.8 V	1.7 3.5	— —	mA
Tx Input Impedance (TE1 = V_{SS}, MC145418)		100	—	kΩ
Crystal Frequency (MC145419) (See Note 3)		4.0	4.4	MHz
PCM Tone (TE = V_{DD}, MC145419)		-22	-18	dBm0
Three-State Current (SO1, SO2, VD, Tx on MC145418, Tx on MC145419)		—	±1	μA
X2 - Oscillator Output High Drive Current (MC145419) (See Note 4)	V_{OH} = 4.6 V	-450	—	μA
X2 - Oscillator Output Low Drive Current (MC145419) (See Note 4)	V_{OL} = 0.4 V	450	—	μA

NOTES:
3. The MC145419 crystal frequency divided by 512 must equal the MC145418 MSI frequency ±0.25% for optimum performance.
4. Output drive when X1 is being driven from an external clock.
5. To overdrive $\overline{PD}$ from a low level to 3.5 V or a high level to 1.5 V requires a minimum of ±800 μA drive capability.

MC145418 SWITCHING CHARACTERISTICS (V_{DD} = 5 V, T_A = 25°C, C_L = 50 pF)

Parameter		Fig	Symbol	Min	Max	Unit
Input Rise Time	All Digital Inputs	1	t_r	—	4	μs
Input Fall Time	All Digital Inputs	1	t_f	—	4	μs
Pulse Width	TDC/RDC, RE1, MSI	1	$t_{W(H,L)}$	90	—	ns
CCI Duty Cycle		1	$t_{W(H,L)}$	45	55	%
Data Clock Frequency	TDC/RDC	—	t_{DC}	64	2560	kHz
Propagation Delay Time MSI to SO1, SO2, VD ($\overline{PD}$ = V_{DD}) TDC to Tx		 2 3	 t_{PLH}, t_{PHL}	 — —	 90 90	ns
MSI to TDC/RDC Setup Time		 4	t_{su3} t_{su4}	90 40	— —	ns
TE1/RE1 to TDC/RDC Setup Time		 4	t_{su3} t_{su4}	90 40	— —	ns
Rx to TDC/RDC Setup Time		5	t_{su5}	60	—	ns
Rx to TDC/RDC Hold Time		5	t_{h1}	60	—	ns
SI1, SI2 to MSI Setup Time		6	t_{su6}	60	—	ns
SI1, SI2 to MSI Hold Time		6	t_{h2}	60	—	ns
DO Valid to MEO Rising		10	t_{p7}	—	90	ns
DO Valid to MEO Falling		10	t_{p8}	—	90	ns
DI Valid to SYN Rising		11	t_{su7}	488	1200	ns
DI Valid to SYN Falling		11	t_{su8}	—	3900	ns

MC145419 SWITCHING CHARACTERISTICS (V_{DD} = 5 V, T_A = 25°C, C_L = 50 pF)

Parameter		Fig	Symbol	Min	Max	Unit
Input Rise Time	All Digital Inputs	1	t_r	—	4	μs
Input Fall Time	All Digital Inputs	1	t_f	—	4	μs
Clock Output Pulse Width	CLK	1	$t_{W(H,L)}$	3.8	4.0	μs
Crystal Frequency		—	f_{X1}	4.086	4.1	MHz
Propagation Delay Times TE1 Rising to CLK (TE = V_{DD}) TE1 Rising to CLK (TE = V_{SS}) CLK to TE1 Falling CLK to RE1 Rising RE1 Falling to CLK (TE = V_{DD}) RE1 Falling to CLK (TE = V_{SS}) CLK to Tx TE1 to SO1, SO2		 7 7 7 8 8 8 9 9	 t_{p1} t_{p1} t_{p2} t_{p3} t_{p4} t_{p4} t_{p5} t_{p6}	 -50 438 — — -50 438 — —	 50 538 40 40 50 538 90 90	ns
Rx to CLK Setup Time		5	t_{su5}	60	—	ns
Rx to CLK Hold Time		5	t_{h1}	60	—	ns
SI1, SI2 to TE1 Setup Time		6	t_{su6}	60	—	ns
SI1, SI2 to TE1 Hold Time		6	t_{h2}	60	—	ns

2

TIMING DIAGRAMS

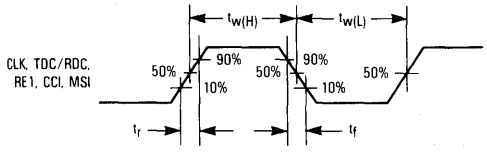


Figure 1

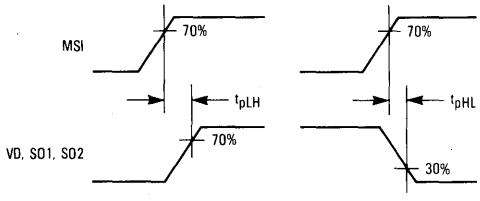


Figure 2

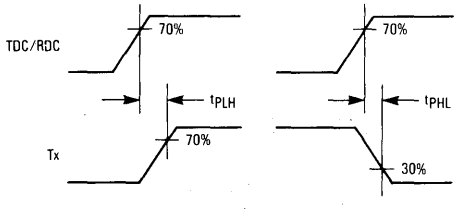


Figure 3

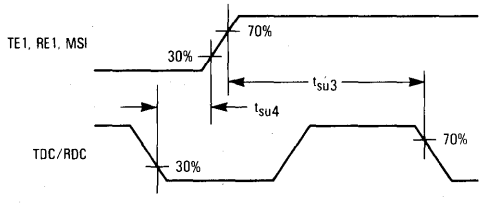


Figure 4

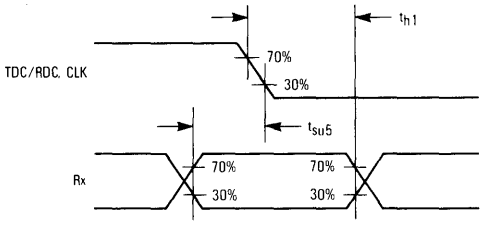
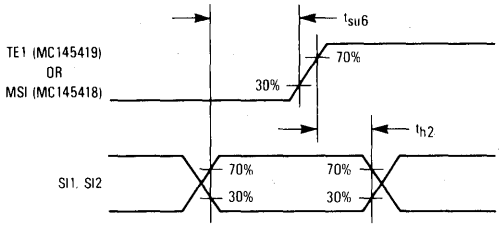


Figure 5



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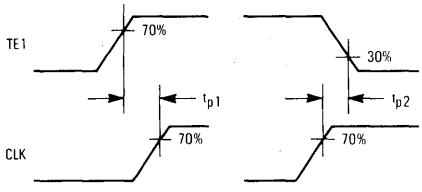

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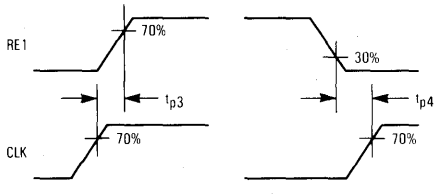


Figure 8

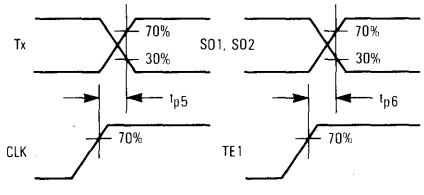


Figure 9

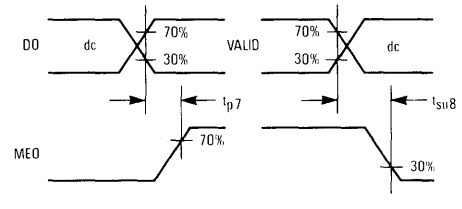


Figure 10

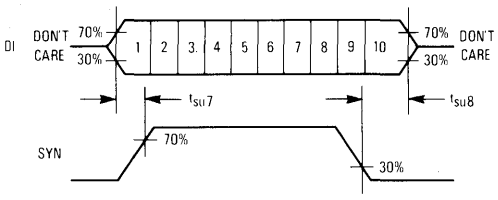


Figure 11

MC145418 MASTER DLT PIN DESCRIPTIONS

V_{DD} — POSITIVE SUPPLY

Normally 5 volts.

V_{SS} — NEGATIVE SUPPLY

This pin is the most negative supply pin, normally 0 volts.

DI — DATA INPUT

This input to the demodulator circuit should be a squared and limited version of the received line signal. (See Figure 15.)

SYN — SYNC INPUT

This input to the demodulator circuit should be a signal which is high when signal energy is detected on the line. (See Figure 14 for typical line interface circuit.)

This signal should be the output of a window comparator with a threshold of approximately 40% of the smallest received line signal. (See Figure 15.)

NC — NO CONNECTION

This pin is not available for use and should be left floating.

VD — VALID DATA OUTPUT

A high on this pin indicates that a valid line transmission has been demodulated. A valid transmission is determined by proper sync and the absence of detected bit errors. VD changes state on the leading edge of MSI when $\overline{PD}$ is high. When $\overline{PD}$ is low, VD changes state at the end of demodulation of a line transmission. VD is a standard B-series CMOS output and is high impedance when SE is held low.

SI1, SI2 — SIGNALING BIT INPUTS

Data on these pins is loaded on the rising edge of MSI for transmission to the slave. The state of these pins is internally latched if SE is held low.

SO1, SO2 — SIGNALING BIT OUTPUTS

These outputs are received signaling bits from the slave DLT and change state on the rising edge of MSI if $\overline{PD}$ is high, or at the completion of demodulation if $\overline{PD}$ is low. These outputs have standard B-series CMOS drive capability and are high impedance if the SE pin is held low.

SE — SIGNAL ENABLE INPUT

If held high, the $\overline{PD}$, SI1, SI2, and SIE inputs and the SO1, SO2, and VD outputs function normally. If held low, the states of these inputs are latched and held internally while the outputs are high impedance. This allows these pins to be bussed with those of other DLTs to a common controller.

$\overline{PD}$ — POWER-DOWN INPUT

If held low, the DLT ceases modulation. In power-down, the only active circuitry is that which is necessary to demodulate an incoming burst and output the signal and valid data bits. Internal data transfers to the transmit and receive registers cease. When brought high, the DLT powers up, and waits three positive MSI edges or until the end of an incoming transmission from the slave DLT and begins transmitting every MSI period to the slave DLT on the next rising edge of the MSI.

MSI — MASTER SYNC INPUT

This pin is the master 8 kHz input system sync and inititates modulation. MSI should be approximately leading-edge aligned with TDC/RDC.

SIE — SIGNAL INSERT ENABLE

This pin, when held high, inserts signal bit 2 received from the slave into the LSB of the outgoing PCM word at Tx and will ignore the SI2 pin and use in its place the LSB of the incoming PCM word at Rx for transmission to the slave. The PCM word to the slave will have its LSB forced low in this mode. In this manner, signal bit 2 to/from the slave DLT is inserted into the PCM words the master sends and receives from the backplane for routing through the PABX for simultaneous voice/data communication. The state of this pin is internally latched if the SE pin is brought and held low.

TE1 — TRANSMIT DATA ENABLE 1 INPUT

This pin controls the outputting of data on the Tx pin. While TE1 is high, the Tx data is presented on the eight rising edges of TDC/RDC. TE1 is also a high-impedance control of the Tx pin. If MSI occurs during this period, new data will be transferred to the Tx output register in the ninth high period of TDC/RDC after TE1 rises; otherwise, it will transfer on the rising edge of MSI. TE1 and TDC/RDC should be approximately leading-edge aligned.

Tx — TRANSMIT DATA OUTPUT

This three-state output pin presents new voice data on the rising edges of TDC/RDC when TE1 is high. (See TE1.)

CCI — CONVERT CLOCK INPUT

A 2.048 MHz clock signal should be applied to this pin. This signal is used for internal sequencing and control. This signal should be coherent with MSI for optimum performance but may be asynchronous if slightly worse error rate performance can be tolerated.

TDC/RDC — TRANSMIT/RECEIVE DATA CLOCK

This pin is the transmit and receive data clock and can be 64 kHz to 2.56 MHz. Data is output at the Tx pin while TE1 is high on the eight rising edges of TDC/RDC after the rising edge of TE1. Data on the Rx pin is loaded into the receive register of the DLT on the eight falling edges of TDC/RDC after a positive transition on RE1. This clock should be approximately leading-edge aligned with MSI.

Rx — RECEIVE DATA

Voice data is clocked into the DLT from this pin on the falling edges of TDC/RDC under the control of RE1.

RE1 — RECEIVE DATA ENABLE 1 INPUT

A rising edge on this pin will enable data on the Rx pin to be loaded into the receive data register on the next falling edges of the data clock, RDC. RE1 and RDC should be approximately leading-edge aligned.

DO — DATA OUTPUT

This B-series output is the square wave Modified - DPSK modulation waveform to be externally buffered and applied to the line. This output is valid only when the MEO output pin is high and is undefined while MEO is low. The external line driver should drive the line in a tri-level manner, controlled by DO and MEO as shown in Figure 15.

MEO — MODULATION ENABLE OUTPUT

This pin, when high, defines the valid data at the DO pin to be valid.

MC145419 SLAVE DLT PIN DESCRIPTIONS

V_{DD} — POSITIVE SUPPLY

Normally 5 volts.

V_{SS} — NEGATIVE SUPPLY

This pin is the most negative supply pin, normally 0 volts.

DI — DATA INPUT

This input to the demodulator circuit should be a squared and limited version of the received line signal. (See Figure 15.)

SYN — SYNC INPUT

This input to the demodulator circuit should be a signal which is high when signal energy is detected on the line. (See Figure 14 for typical line interface circuit.)

This signal should be the output of a window comparator with a threshold of approximately 40% of the smallest received line signal. (See Figure 15.)

$\overline{LB}$ — LOOP-BACK CONTROL

When this pin is held low and $\overline{PD}$ is high (the DLT is receiving transmissions from the master), the DLT will use the eight bits of demodulated PCM data in place of the eight bits of Rx data in the return burst to the master, thereby looping the part back on itself for system testing. SI1 and SI2 operate normally in this mode. CLK will be held low during loop-back operation.

VD — VALID DATA OUTPUT

A high on this pin indicates that a valid line transmission has been demodulated. A valid transmission is determined by proper sync and the absence of detected bit errors. VD changes state on the leading edge of TE1. If no transmissions from the master have been received in the last 250 μs (derived from the internal oscillator), VD will go low without TE1 rising since TE1 is not generated in the absence of received transmissions from the master. (See TE pin description for the one exception to this.)

SI1, SI2 — SIGNALING BIT INPUTS

Data on these pins is loaded on the rising edge of TE1 for transmission to the master. If no transmissions from the master are being received and $\overline{PD}$ is high, data on these pins will be loaded into the part on an internal signal. Therefore, data on these pins should be steady until synchronous communication with the master has been established, as indicated by the high on VD.

SO1, SO2 — SIGNALING BIT OUTPUTS

These outputs are received signaling bits from the master DLT and change state on the rising edge of TE1. These outputs have standard B-series CMOS output drive capability.

$\overline{PD}$ — POWER-DOWN INPUT/OUTPUT

This is a bidirectional pin with weak output drivers such that it can be overdriven externally. When held low, the DLT is powered down and the only active circuitry is: that which is necessary for demodulation, TE1/RE1/CLK generation upon demodulation: the outputting of data received from the master and updating of VD status. When held high, the DLT is powered up and transmits in response to received transmissions from the master. If no received bursts from the master have occured when powered up, for 250 μs (derived from the internal oscillator frequency), the DLT will generate a free running 125 μs internal clock from the internal oscillator and will burst a transmission to the master every other internal 125 μs clock using data on the SI1 and SI2 pins and the last data word loaded into the receive register. The weak output drivers will try to force $\overline{PD}$ high when a transmission from the master is demodulated and will try to force it low if 250 μs have passed without a transmission from the master. This allows the slave DLT to self power-up and down in demand powered-loop systems.

TE — TONE ENABLE

A high on this pin generates a 500 Hz square wave PCM tone and inserts it in place of the demodulated voice PCM word from the master for outputting to the Tx pin to the telset mono-circuit. A high on TE will generate TE1 and CLK from the internal oscillator when the slave is not receiving bursts from the master so that the PCM square wave can be loaded into the mono-circuit. This feature allows the user to provide audio feedback for the telset keyboard depressions except during loop-back. During loop-back of the slave DLT, CLK is defeated so a tone cannot be generated in this mode.

TE1 — TRANSMIT DATA ENABLE 1 OUTPUT

This is a standard B-series CMOS output which goes high after the completion of demodulation of an incoming transmission from the master. It remains high for eight CLK periods and then low until the next burst from the master is demodulated. While high, the voice data just demodulated is output on the first eight rising edges of CLK at the Tx pin. The signaling data just demodulated is output on SO1 and SO2 on TE1's rising edge, as is VD.

Tx — TRANSMIT DATA OUTPUT

This is a standard B-series CMOS output. Voice data is output on this pin on the rising edges of CLK while TE1 is high and is high-impedance when TE1 is low.

X1 — CRYSTAL INPUT

A 4.096 MHz crystal is tied between this pin and X2. A 10 MΩ resistor across X1 and X2 and 25 pF capacitors from X1 and X2 to V_{SS} are required for stability and to insure start-up. X1 may be driven by an external CMOS clock signal if X2 is left open.

X2 — CRYSTAL OUTPUT

This pin is capable of driving one external CMOS input and 15 pF of additional capacitance. (See X1.)

CLK — CLOCK OUTPUT

This is a standard B-series CMOS output which provides the data clock for the telset mono-circuit. It is generated by dividing the oscillator down to 128 kHz and starts upon the completion of demodulation of an incoming burst from the master. At this time, CLK begins and TE1 goes high. CLK will remain active for 16 periods, at the end of which it will remain low until another transmission from the master is demodulated. In this manner, sync from the master is established in the slave and any clock slip between the master and the slave is absorbed each frame. CLK is generated in response to an incoming burst from the master; however, if TE is brought high, then CLK and TE1/RE1 are generated from the internal oscillator until TE is brought low or an incoming burst from the master is received. CLK is disabled when $\overline{LB}$ is held low.

Rx — RECEIVE DATA INPUT

Voice data from the telset mono-circuit is input on this pin on the first eight falling edges of CLK after RE1 goes high.

Mu/A — TONE DIGITAL FORMAT INPUT

This pin determines if the PCM code of the 500 Hz square wave tone, generated when TE is high, is D3 (Mu/A = 1) or CCITT (Mu/A = 0) format.

RE1 — RECEIVE DATA ENABLE 1 OUTPUT

This is a standard B-series CMOS output which is the inverse of TE1 (see TE1). Data is clocked into Rx on the falling edges of CLK while RE1 is high.

DO — DATA OUTPUT

This B-series output is the square wave Modified-DPSK modulation waveform to be externally buffered and applied to the line. This output is valid only when the MEO output pin is high and is undefined while MEO is low. The external line driver should drive the line in a tri-level manner, controlled by DO and MEO as shown in Figure 15.

MEO — MODULATION ENABLE OUTPUT

This pin, when high, defines the valid data at the DO pin to be valid.

BACKGROUND

The MC145418 Master and MC145419 Slave DLT transceiver ICs main application is to bidirectionally transmit the digital signals present at a codec/filter-digital PABX backplane interface over transmission mediums such as telephone wire pairs or fiber optics. This allows the remoting of the mono-circuit in a digital telephone set and enables each set to have a high speed data access to the PABX switching facility. In effect, the DLT allows each PABX subscriber direct access to the inherent 64 kbps data routing capabilities of the PABX.

The DLT provides a means for transmitting and receiving 64 kbps of voice data and 16 kbps of signaling data. The DLT is a two chip set consisting of a Master and a Slave. The master DLT replaces the codec/filter and SLIC on the PABX linecard, and transmits and receives data over the intended transmission medium to the telset. The DLT appears to the linecard and backplane as if it were a PCM codec/filter and has almost the same digital interface features as the MC14400 series mono-circuits. The slave DLT is located in the telset and interfaces the mono-circuit to the transmission medium. By hooking two DLTs back-to-back, a repeater can also be formed. The master and slave DLTs operate in a frame synchronous manner, sync being established at the slave by the timing of the master's transmission. The master's sync is derived from the PABX frame sync.

The communication between master and slave DLTs require a single data link in the transmission medium. Eight bits of voice data and two bits of signaling data are transmitted and received each frame in a half duplex manner; i.e., the slave waits until the transmission from the master is completely received before transmitting back to the master. Transmission occurs at 256 kHz bit rate using a "squared" modified form of DPSK. This "ping-pong" mode will allow transmission of data at distances up to 2 km before turnaround delay becomes a problem. The DLT is so defined as to allow this data to be handled by the linecard, backplane, and PABX as if it were just another voice conversation. This allows existing PABX hardware and software to be unchanged and yet provides switched 64 kbps voice or data communications throughout its service area by simply replacing a subscriber's linecard and telset. A feature in the master allows one of the two signaling bits to be inserted and extracted from the backplane PCM word to allow simultaneous voice and data transmission through the PABX. The slave DLT has a loop-back feature by which the device can be tested in the user system.

The slave DLT has the additional feature of providing a 500 Hz Mu or A law coded square wave to the mono-circuit when the TE pin is brought high. This can be used to provide audio feedback in the telset during keyboard depressions.

Although the DLT was originally designed for a PABX environment, it can be used in any digital synchronous serial environment; such as, computer to computer communications or industrial control.

CIRCUIT DESCRIPTION

GENERAL

The DLT consists of a modulator, demodulator, two intermediate data buffers, sequencing and control logic, and transmit and receive data registers. The data registers inter-

face to the linecard or mono-circuit digital interface signals, the modulator and demodulator provide Modified - DPSK transmission and reception, while the intermediate data registers buffer data between these two sections. The DLT is intended to operate on a single 5 volt supply and can be driven by TTL or CMOS logic.

MASTER OPERATION

In the master, data is loaded into the receive register each frame from the Rx pin under the control of the TDC/RDC clock and the receive data enable, RE1. RE1 controls loading of eight serial bits, henceforth referred to as the voice data word. Each MSI, these words are transferred out of the receive register to the modulation buffer for subsequent modulation onto the line. The modulation buffer takes the received voice data word and the two signaling data input bits on SI1 and SI2 loaded on the MSI rising edge and formats the ten bits into a specific order. This data field is then transmitted in a 256 kHz "squared" Modified-DPSK burst to the remote slave DLT. An example of the modulated data field at DO is shown with the Modulation Enable Output (MEO) in Figure 15. V2-V1 is the differentially driven waveform onto the line in a twisted pair application.

The received signal coming into the demodulator should be a squared digital version of the line signal, shown as DI in Figure 15. The SYN signal which is the output of a window comparator is internally integrated and used by the demodulator's synchronization circuitry along with the first zero crossing of DI to establish the exact position (in time) of the incoming burst for demodulation purposes. The SYN pulse or pulses (output of the window comparator circuitry) must be present for the first eight baud periods of the incoming burst. They may persist longer but they must not occur within one full baud period before the arrival of the following burst. Upon demodulating the return burst from the slave, the decoded data is transferred to the demodulation buffer and the signaling bits are stripped ready to be output on SO1 and SO2 at the next MSI. The voice data word is loaded into the transmit register as described in the TE1 pin description for outputting via the Tx pin at the TDC/RDC data clock rate under the control of TE1. VD is output on the rising edge of MSI. Timing diagrams for the master are shown in Figure 12.

SLAVE OPERATION

In the slave, the synchronizing event is the detection of an incoming transmission from the master as indicated by the completion of demodulation. (The SYN signal and DI function the same as in the Master.) When an incoming burst from the master is demodulated, several events occur. As in the master, data is transferred from the demodulator to the demodulation buffer and the signaling bits are stripped for outputting at SO1 and SO2. Data in the receive register is transferred to the modulation buffer. TE1 goes high loading in data at SI1 and SI2, which will be used in the transmission burst to the master along with the data in the transmit data buffer. At the same time SO1, SO2, and VD are output. Modulation of the burst begins four 256 kHz periods after the completion of demodulation.

While TE1 is high, data is output at Tx on the rising edges of CLK. On the ninth rising edge of CLK, TE1 goes low, RE1 goes high, and data is input to the receive register from the Rx pin on the next eight falling edges of CLK.

The CLK pin is a 128 kHz output that is formed by dividing down the 4.096 MHz crystal frequency by 32. Slippage between the frame rate of the master (as represented by the completion of demodulation of an incoming transmission from the master) and the crystal frequency is absorbed by holding the 16th low period of CLK until the next completion of demodulation. This is shown in the slave DLT timing diagram of Figure 13.

POWER-DOWN OPERATION

In the master, when $\overline{PD}$ is low, the DLT stops modulating and only that circuitry necessary to demodulate the incoming bursts and output the signaling and VD data bits is active. In this mode, if the DLT receives a burst from the slave, the SO1, SO2, and VD pins will be updated upon completion of the demodulation instead of on the rising edge of MSI. The state of these pins will not change until either three rising MSI edges have occurred without the reception of a burst from the slave or until another burst is demodulated, whichever occurs first.

When $\overline{PD}$ is brought high, the master DLT will wait either three rising MSI edges or until the MSI rising edge following the demodulation of an incoming burst before transmitting to the slave. The data for the first transmission to the slave after power-up is loaded into the DLT during the RE1 period prior to the burst for Rx data, and on the present rising edge of MSI for signaling data.

In the slave, $\overline{PD}$ is a bidirectional pin with weak output drivers such that it can be overdriven externally. When held low, the DLT slave is powered down and only that circuitry necessary for demodulation, TE1/RE1/CLK generation upon demodulation, the outputting of Tx data, signaling bits, and VD is active. When held high, the DLT slave is powered up and transmits normally in response to received transmissions from the master. If no bursts have been received from the master within 250 μs after power-up (derived from the internal oscillator frequency), the DLT generates an internal 125 μs free-running clock from the internal oscillator. The slave DLT then bursts a transmission to the master DLT every other 125 μs clock period using data loaded into the Rx pin during the last RE1 period and SI1, SI2 data loaded in on the internal 125 μs clock edge. The weak output drivers will try to force $\overline{PD}$ high when a transmission from the master is demodulated and will try to force it low if 250 μs have passed without a transmission from the master. This allows the slave DLT to self power-up and down in demand powered-loop systems.

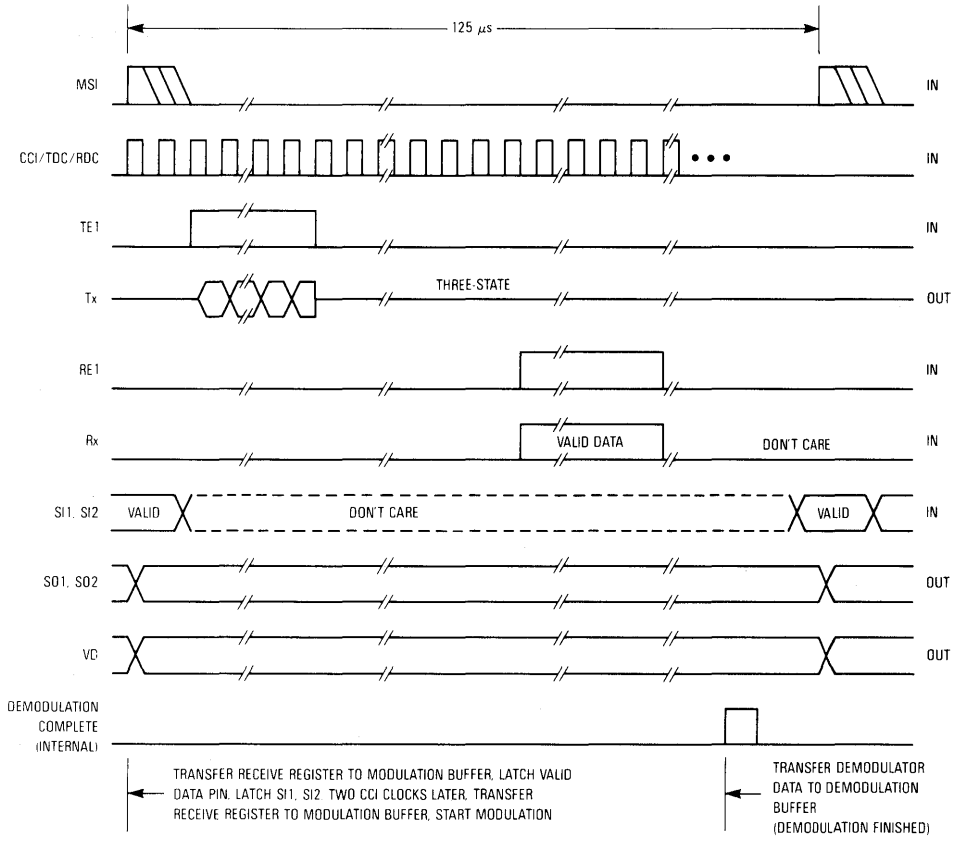


Figure 12. Master DLT Timing

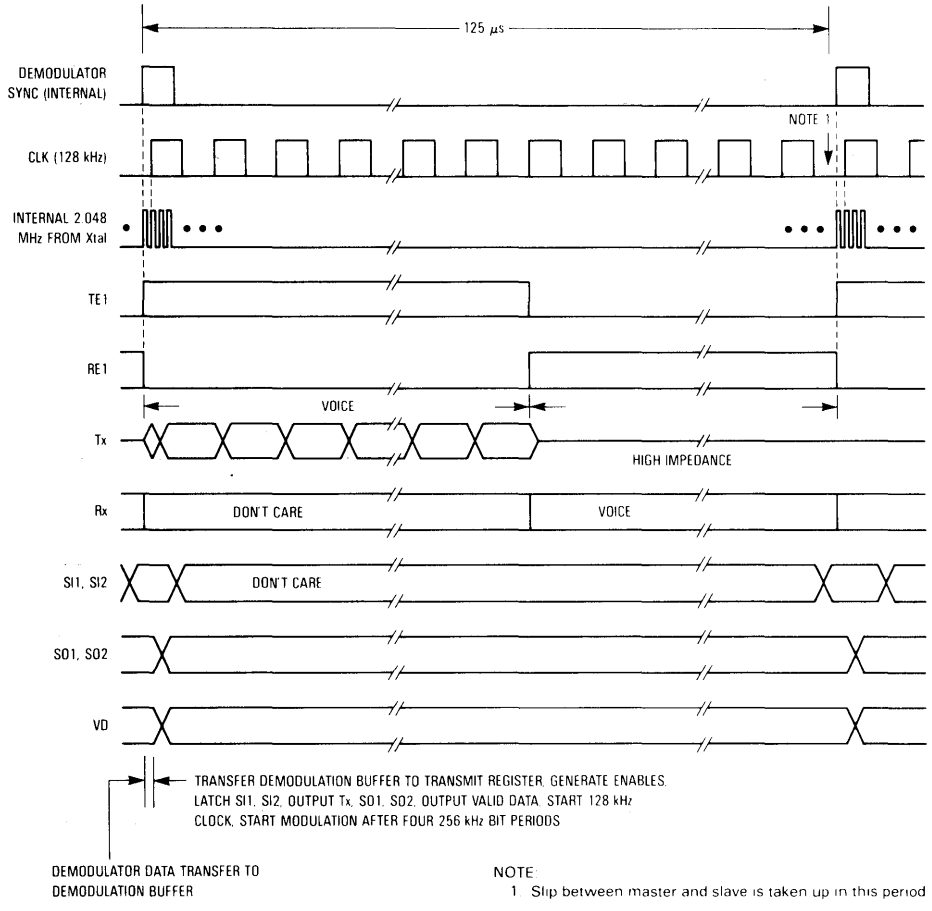


Figure 13. Slave DLT Timing

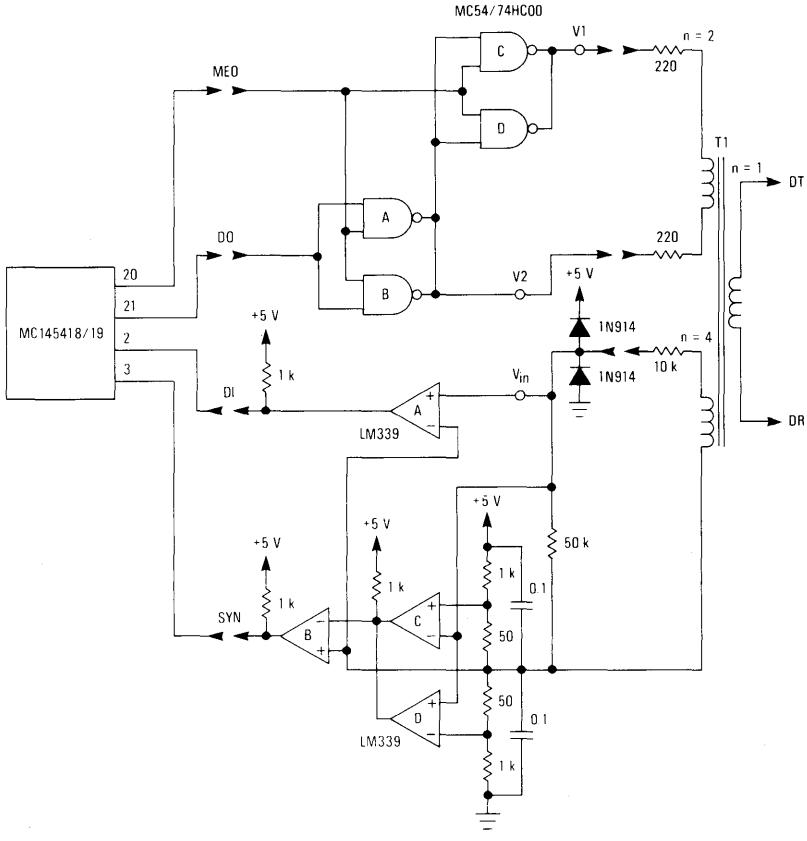
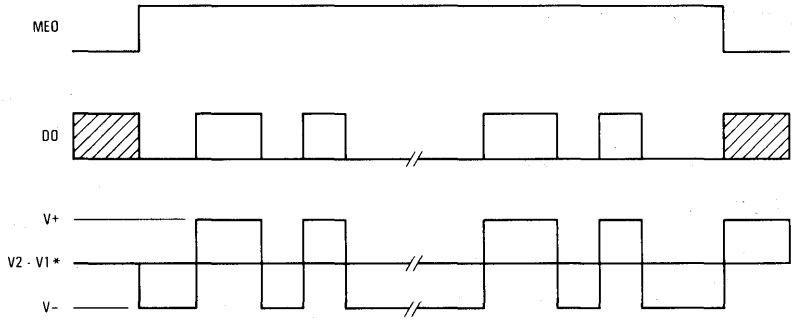
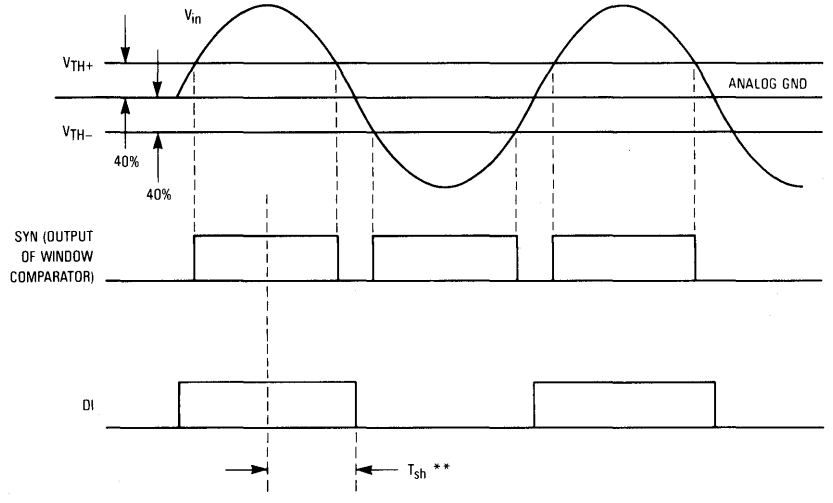


Figure 14. Typical DLT Line Interface



*See Figure 14 for voltages V2, V1. |V+| must equal |V-| within 5%. V2-V1, when MEO is low, must equal (V+ - V-) 2 within 5%



**T_{sh} - SYN should be high a minimum of three 4.096 MHz clock periods before the first zero crossing as indicated by DI state change.

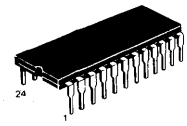
Figure 15. Line Driver Waveforms

MC145421
MC145425

MOTOROLA

Product Preview

160 kbps ISDN Universal Digital Loop Transceivers



L SUFFIX
CERDIP
CASE 623

2

The MC145421 and MC145425 UDLTs are high speed data transceivers capable of providing 160 kbps full duplex data communication over 26 awg and larger twisted pair cable up to 1 km in length and up to 2 km with the addition of a simple passive equalizer. These devices are primarily used in digital subscriber voice and data telephone systems. In addition, the devices meet and can exceed the CCITT's recommendation for data transfer rates for ISDNs on a single twisted pair. The devices utilize a 512 kilobaud MDPSK burst modulation technique to supply the 160 kbps full duplex data transfer rates.

The MC145421 and MC145425 UDLTs are designed for upward compatibility with the existing MC145422 and MC145426 80 kbps UDLTs as well as compatibility with existing and evolving telephone switching hardware and software architectures.

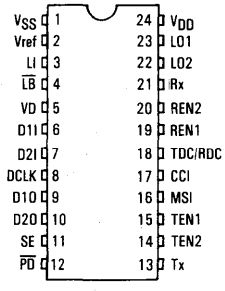
The MC145421 (Master) UDLT is designed for use at the telephone switch line card while the MC145425 (Slave) UDLT is designed for use at the remote digital telset or data terminal.

These devices employ CMOS technology in order to take advantage of its proven capability for complex analog and digital LSI functions.

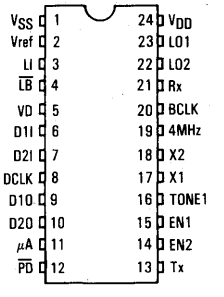
- Provides Synchronous Full Duplex 160 kbps Voice and Data Capabilities in a 2B + 2D Format for ISDN Compatibility
- Provides CCITT Basic Access Data Transfer Rate (2B + D) for ISDNs on a Single Twisted Wire Pair up to 2 km
- Compatible with Existing and Evolving Telephone Switch Architectures and Call Signalling Schemes
- Automatic Threshold Adjustment for Optimum Performance Over Varying Signal Attenuations
- Protocol Independent
- Single 5 V Power Supply

PIN ASSIGNMENTS

MC145421



MC145425



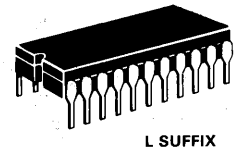
MOTOROLA

MC145422
MC145426

2

Advance Information

Universal Digital-Loop Transceivers (UDLT)



L SUFFIX
CERAMIC
CASE 736

The MC145422 and MC145426 UDLTs are high-speed data transceivers that provide 80 kilobits per second full duplex data communication over 26 AWG and larger twisted pair cable up to two kilometers in distance. Intended primarily for use in digital subscriber voice/data telephone systems, these devices can also be used in remote data acquisition and control systems. These devices utilize a 256 kilobaud modified differential phase shift keying burst modulation technique for transmission to minimize RFI/EMI and crosstalk. Simultaneous power distribution and duplex data communication can be obtained using a single twisted pair wire.

These devices are designed for compatibility with existing, as well as evolving, telephone switching hardware and software architectures.

The UDLT chip-set consists of the MC145422 master UDLT for use at the telephone switch linecard and the MC145426 slave UDLT for use at the remote digital telset and/or data terminal.

The devices employ CMOS technology in order to take advantage of its reliable low-power operation and proven capability for complex analog/digital LSI functions.

- Provides Full Duplex Synchronous 64 Kilobits-Per-Second Voice/Data Channel and Two Eight Kilobits-Per-Second Signaling Data Channels Over One 26 AWG Wire Pair Up to Two Kilometers
- Compatible with Existing and Evolving Telephone Switch Architectures and Call Signaling Schemes
- Automatic Detection Threshold Adjustment for Optimum Performance Over Varying Signal Attenuations
- Protocol Independent
- Single Five Volt Power Supply
- 22 Pin Package

MC145422 Master UDLT

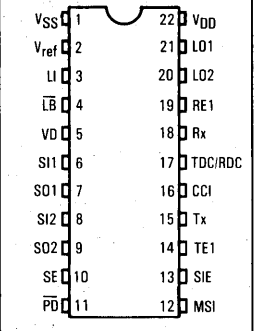
- Pin Controlled Power-Down and Loop-Back Features
- Signaling and Control I/O Capable of Sharing Common Bus Wiring with Other UDLTs
- Variable Data Clock—64 kHz to 2.56 MHz
- Pin Controlled Insertion/Extraction of Eight Kilobits/Second Channel into LSB of 64 Kilobits/Second Channel for Simultaneous Routing of Voice and Data Through PCM Voice Path of Telephone Switch

MC145426 Slave UDLT

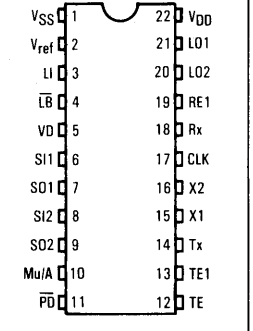
- Compatible with MC14400 Series PCM Mono-Circuits
- Pin Controlled Loop-Back Feature
- Automatic Power-Up/Down Feature
- On-Chip Data Clock Recovery and Generation
- Pin Controlled 500 Hz D3 or CCITT Format PCM Tone Generator for Audible Feedback Applications

PIN ASSIGNMENTS

MC145422

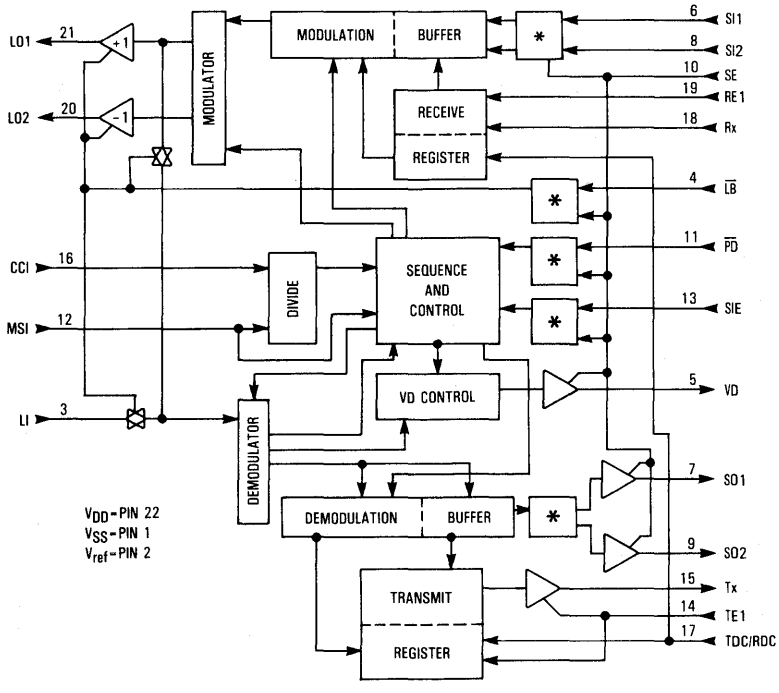


MC145426



This document contains information on a new product. Specifications and information herein are subject to change without notice.

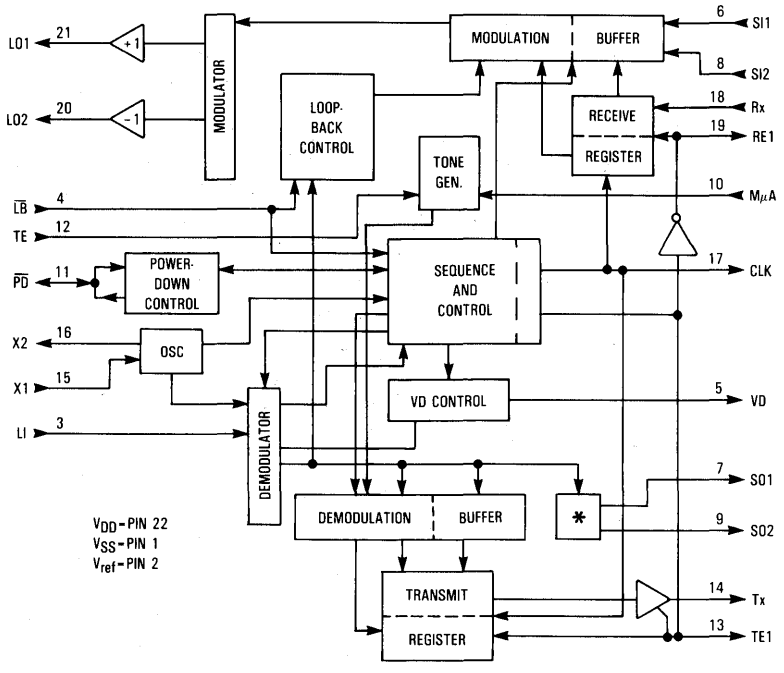
MC145422 MASTER UDLT BLOCK DIAGRAM



* — SE controlled latch

2

MC145426 SLAVE UDLT BLOCK DIAGRAM



*—Signal Bits Output Latch

ABSOLUTE MAXIMUM RATINGS (Voltage Referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}-V_{SS}	−0.5 to 9.0	V
Voltage, Any Pin to V_{SS}	V	−0.5 to V_{DD} + 0.5	V
DC Current, Any Pin (Excluding V_{DD}, V_{SS})	I	±10	mA
Operating Temperature	T_A	−40 to +85	°C
Storage Temperature	T_{stg}	−85 to +150	°C

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to 70°C)

Parameter	Pins	Min	Max	Unit
DC Supply Voltage	V_{DD}	4.5	5.5	V
Power Dissipation (PD = V_{DD}, V_{DD} = 5 V)	V_{DD}	–	80	mW
Power Dissipation (PD = V_{SS}, TE = V_{SS})	V_{DD}	–	75	mW
Frame Rate MC145422	MSI	7.9	8.1	kHz
MC145422-MC145426 Frame Rate Slip (See Note 1)	–	–	0.25	%
CCI Clock Frequency (MSI = 8 kHz)	CCI	–	2.048	MHz
Data Clock Rate MC145422	TDC, RDC	64	2560	kHz
Modulation Baud Rate (See Note 2)	LO1, LO2	–	256	kHz

NOTES: 1. The MC145426 crystal frequency divided by 512 must equal the MC145422 MSI frequency ±0.25% for optimum operation.
2. Assumes crystal frequency of 4.096 MHz for the MC145426 and 2.048 MHz CCI for the MC145422.

DIGITAL CHARACTERISTICS (V_{DD} = 5 V, T_A = 0 to 70°C)

Parameter		Min	Max	Unit
Input High Level		3.5	–	V
Input Low Level		–	1.5	V
Input Current	Except LI LI	−1.0 −100	1.0 100	μA
Input Capacitance		–	7.5	pF
Output High Current (Except Tx on MC145422 and Tx and $\overline{PD}$ on MC145426)	V_{OH} = 2.5 V V_{OH} = 4.6 V	−1.7 −0.36	– –	mA
Output Low Current (Except Tx on MC145422 and Tx and $\overline{PD}$ on MC145426)	V_{OL} = 0.4 V V_{OL} = 0.8 V	0.36 0.8	– –	mA
$\overline{PD}$ Output High Current (MC145426) (See Note 7)	V_{OH} = 2.5 V V_{OH} = 4.6 V	−90 −10	– –	μA
$\overline{PD}$ Output Low Current (MC145426) (See Note 7)	V_{OL} = 0.4 V V_{OL} = 0.8 V	60 100	– –	μA
Tx Output High Current	V_{OH} = 2.5 V V_{OH} = 4.6 V	−3.4 −0.7	– –	mA
Tx Output Low Current	V_{OL} = 0.4 V V_{OL} = 0.8 V	1.7 3.5	– –	mA
Tx Input Impedance (TE1 = V_{SS}, MC145422)		100	–	kΩ
Crystal Frequency (MC145426, Note 3)		4.0	4.4	MHz
PCM Tone (TE = V_{DD}, MC145426)		−22	−18	dBm0
Three-State Current (SO1, SO2, VD, Tx on MC145422, Tx on MC145426)		–	±1	μA
V_{ref} Voltage (See Note 6)		2	3	V
X2—Oscillator Output High Drive Current (MC145426) (See Note 5)	V_{OH} = 4.6 V	−450	–	μA
X2—Oscillator Output Low Drive Current (MC145426) (See Note 5)	V_{OL} = 0.4 V	450	–	μA

ANALOG CHARACTERISTICS (V_{DD} = 5 V, T_A = 0 to 70°C)

Parameter		Min	Max	Unit
Modulation Differential Amplitude (R_L = 440 Ω)	LO1 to LO2	4.5	6.0	V_{p-p}
Modulation Differential DC Offset		0	300	mV
Demodulator Input Amplitude (See Note 4)		0.050	2.5	V peak
Demodulator Input Impedance		50	150	kΩ

NOTES:
3. The MC145426 crystal frequency divided by 512 must equal the MC145422 MSI frequency ±0.25% for optimum performance.
4. The input level into the demodulator to reliably demodulate incoming bursts. Input referenced to V_{ref}.
5. Output drive when X1 is being driven from an external clock.
6. V_{ref} typically (9/20 V_{DD}-V_{SS})
7. To overdrive $\overline{PD}$ from a low level to 3.5 V or a high level to 1.5 V requires a minimum of ±800 μA drive capability.

MC145422 SWITCHING CHARACTERISTICS (V_{DD} = 5 V, T_A = 25°C, C_L = 50 pF)

Parameter		Fig	Symbol	Min	Max	Unit
Input Rise Time	All Digital Inputs	1	t_r	–	4	μs
Input Fall Time	All Digital Inputs	1	t_f	–	4	μs
Pulse Width	TDC/RDC, RE1, MSI	1	$t_{w(H,L)}$	90	–	ns
CCI Duty Cycle		1	$t_{w(H,L)}$	45	55	%
Data Clock Frequency	TDC/RDC	–	t_{DC}	64	2560	kHz
Propagation Delay Time						ns
MSI to SO1, SO2, VD ($\overline{PD}$ = V_{DD})		2	t_{PLH}, t_{PHL}	–	90	
TDC to Tx		3		–	90	
MSI to TDC/RDC Setup Time			t_{su3}	90	–	ns
		4	t_{su4}	40	–	
TE1/RE1 to TDC/RDC Setup Time			t_{su3}	90	–	ns
		4	t_{su4}	40	–	
Rx to TDC/RDC Setup Time		5	t_{su5}	60	–	ns
Rx to TDC/RDC Hold Time		5	t_{h1}	60	–	ns
SI1, SI2 to MSI Setup Time		6	t_{su6}	60	–	ns
SI1, SI2 to MSI Hold Time		6	t_{h2}	60	–	ns

MC145426 SWITCHING CHARACTERISTICS (V_{DD} = 5 V, T_A = 25°C, C_L = 50 pF)

Parameter		Fig	Symbol	Min	Max	Unit
Input Rise Time	All Digital Inputs	1	t_r	–	4	μs
Input Fall Time	All Digital Inputs	1	t_f	–	4	μs
Clock Output Pulse Width	CLK	1	$t_{w(H,L)}$	3.8	4.0	μs
Crystal Frequency		–	f_{X1}	4.086	4.1	MHz
Propagation Delay Times						ns
TE1 Rising to CLK (TE = V_{DD})		7	t_{P1}	50	50	
TE1 Rising to CLK (TE = V_{SS})		7	t_{P1}	438	538	
CLK to TE1 Falling		7	t_{P2}	–	40	
CLK to RE1 Rising		8	t_{P3}	–	40	
RE1 Falling to CLK (TE = V_{DD})		8	t_{P4}	−50	50	
RE1 Falling to CLK (TE = V_{SS})		8	t_{P4}	438	538	
CLK to Tx		9	t_{P5}	–	90	
TE1 to SO1, SO2		9	t_{P6}	–	90	
Rx to CLK Setup Time		5	t_{su5}	60	–	ns
Rx to CLK Hold Time		5	t_{h1}	60	–	ns
SI1, SI2 to TE1 Setup Time		6	t_{su6}	60	–	ns
SI1, SI2 to TE1 Hold Time		6	t_{h2}	60	–	ns

SWITCHING WAVEFORMS

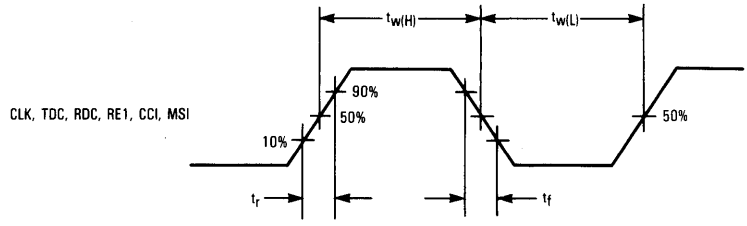


Figure 1

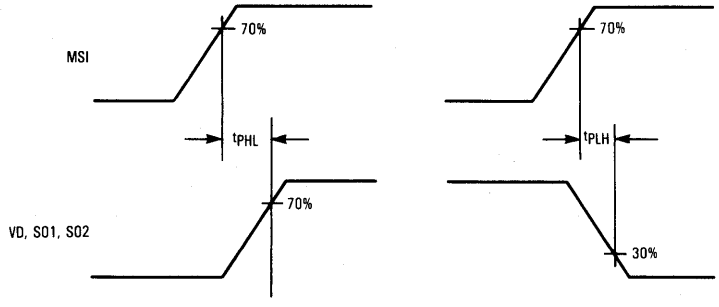


Figure 2

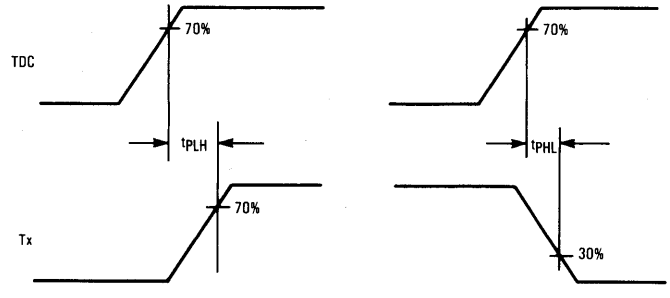


Figure 3

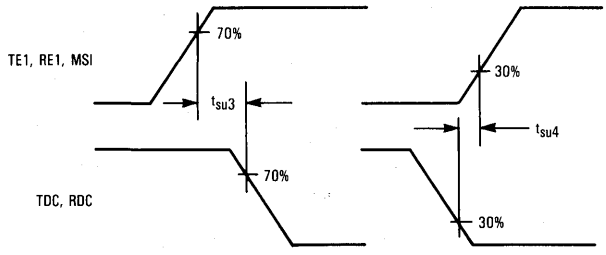


Figure 4

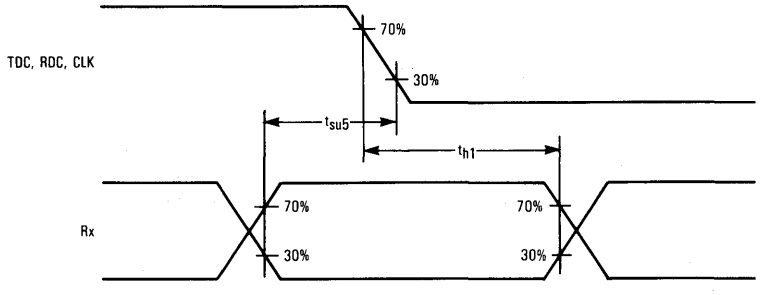


Figure 5

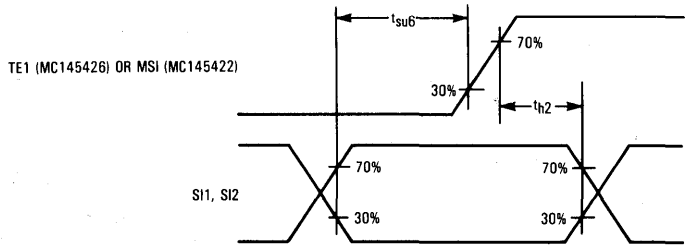


Figure 6

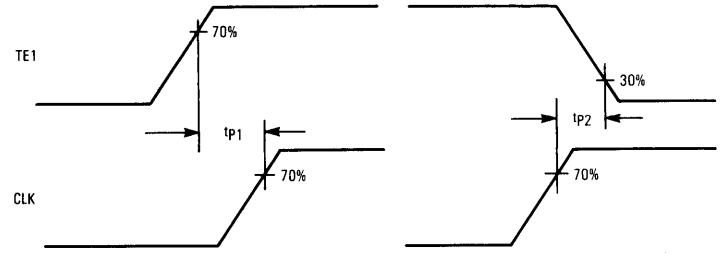


Figure 7

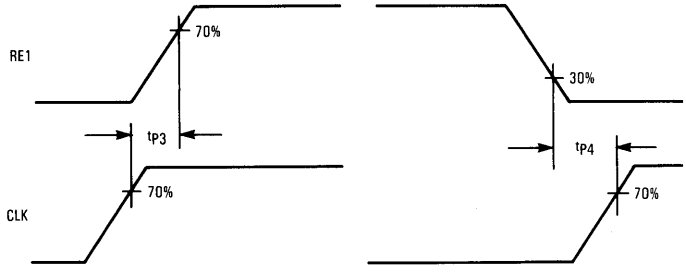


Figure 8

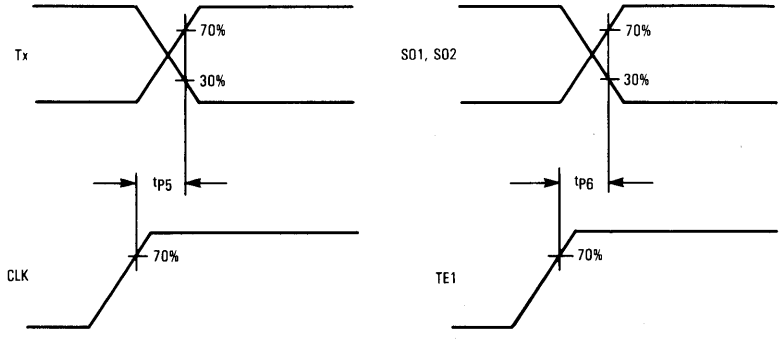


Figure 9

MC145422 MASTER UDLT PIN DESCRIPTIONS

V_{DD}—POSITIVE SUPPLY

Normally 5 volts.

V_{SS}—NEGATIVE SUPPLY

This pin is the most negative supply pin, normally 0 volts.

V_{ref}—REFERENCE OUTPUT

This pin is the output of the internal reference supply and should be bypassed to V_{DD} and V_{SS} by 0.1 μF capacitors. No external dc load should be placed on this pin.

LI—LINE INPUT

This input to the demodulator circuit has an internal 100 k resistor tied to the internal reference node so that an external capacitor and/or line transformer may be used to couple the input signal to the part with no dc offset.

$\overline{LB}$—LOOP-BACK CONTROL

A low on this pin disconnects the LI pin from internal circuitry, drives LO1, LO2 to V_{ref} and internally ties the modulator output to the demodulator input which loops the part on itself for testing in the system. The state of this pin is internally latched if the SE pin is brought and held low. Loop-Back is active only when $\overline{PD}$ is high.

VD—VALID DATA OUTPUT

A high on this pin indicates that a valid line transmission has been demodulated. A valid transmission is determined by proper sync and the absence of detected bit errors. VD changes state on the leading edge of MSI when $\overline{PD}$ is high. When $\overline{PD}$ is low, VD changes state at the end of demodulation of a line transmission. VD is a standard B-series CMOS output and is high impedance when SE is held low.

SI1, SI2—SIGNALING BIT INPUTS

Data on these pins is loaded on the rising edge of MSI for transmission to the slave. The state of these pins is internally latched if SE is held low.

SO1, SO2—SIGNALING BIT OUTPUTS

These outputs are received signaling bits from the slave UDLT and change state on the rising edge of MSI if $\overline{PD}$ is high, or at the completion of demodulation if $\overline{PD}$ is low. These outputs have standard B-series CMOS drive capability and are high impedance if the SE pin is held low.

SE—SIGNAL ENABLE INPUT

If held high, the $\overline{PD}$, $\overline{LB}$, SI1, SI2, and SIE inputs and the SO1, SO2, and VD outputs function normally. If held low, the state of these inputs are latched and held internally while the outputs are high impedance. This allows these pins to be bussed with those of other UDLTs to a common controller.

$\overline{PD}$—POWER-DOWN INPUT

If held low, the UDLT ceases modulation. In power-down, the only active circuitry is that which is necessary to demodulate an incoming burst and output the signal and valid data bits. Internal data transfers to the transmit and receive registers cease. When brought high, the UDLT powers-up, and waits three positive MSI edges or until the end of an incoming transmission from the slave UDLT and begins transmitting every MSI period to the slave UDLT on the next rising edge of the MSI.

MSI—MASTER SYNC INPUT

This pin is the system sync and initiates the modulation on the twisted pair. MSI should be approximately leading-edge aligned with TDC/RDC.

SIE—SIGNAL INSERT ENABLE

This pin, when held high, inserts signal bit 2 received from the slave into the LSB of the outgoing PCM word at Tx and will ignore the SI2 pin and use in place the LSB of the incoming PCM word at Rx for transmission to the slave. The PCM word to the slave will have LSB forced low in this mode. In this manner, signal bit 2 to/from the slave UDLT is inserted into the PCM words the master sends and receives from the backplane for routing through the PABX for simultaneous voice/data communication. The state of this pin is internally latched if the SE pin is brought and held low.

TE1—TRANSMIT DATA ENABLE 1 INPUT

This pin controls the outputting of data on the Tx pin. While TE1 is high, the Tx data is presented on the eight rising edges of TDC/RDC. TE1 is also a high-impedance control of the Tx pin. If MSI occurs during this period, new data will be transferred to the Tx output register in the ninth high period of TDC/RDC after TE1 rises; otherwise, it will transfer on the rising edge of MSI. TE1 and TDC/RDC should be approximately leading-edge aligned.

Tx—TRANSMIT DATA OUTPUT

This three-state output pin presents new voice data during the high periods of TDC/RDC when TE1 is high (see TE1).

CCI—CONVERT CLOCK INPUT

A 2.048 MHz clock signal should be applied to this pin. The signal is used for internal sequencing and control. This signal should be coherent with MSI for optimum performance but may be asynchronous if slightly worse error rate performance can be tolerated.

TDC/RDC—TRANSMIT/RECEIVE DATA CLOCK

This pin is the transmit and receive data clock and can be 64 kHz to 2.56 MHz. Data is output at the Tx pin while TE1 is high on the eight rising edges of TDC/RDC after the rising edge of TE1. Data on the Rx pin is loaded into the receive register of the UDLT on the eight falling edges of TDC/RDC after a positive transition on RE1. This clock should be approximately leading-edge aligned with MSI.

Rx—RECEIVE DATA

Voice data is clocked into the UDLT from this pin on the falling edges of TDC/RDC under the control of RE1.

RE1—RECEIVE DATA ENABLE 1 INPUT

A rising edge on this pin will enable data on the Rx pin to be loaded into the receive data register on the next eight falling edges of the data clock, TDC/RDC. RE1 and TDC/RDC should be approximately leading-edge aligned.

LO1, LO2—LINE DRIVER OUTPUTS

These outputs drive the twisted pair line with 256 kHz modified DPSK bursts each frame and are push-pull. These pins are driven to V_{ref} when not modulating the line.

MC145426 SLAVE UDLT PIN DESCRIPTIONS

V_{DD}—POSITIVE SUPPLY

Normally 5 volts.

V_{SS}—NEGATIVE SUPPLY

This pin is the most negative supply pin, normally 0 volts.

V_{ref}—REFERENCE OUTPUT

This pin is the output of the internal reference supply and should be bypassed to V_{DD} and V_{SS} by 0.1 μF capacitors. No external dc load should be placed on this pin.

LI—LINE INPUT

This input to the demodulator circuit has an internal 100 kilohm resistor tied to the internal reference node (V_{ref}) so that an external capacitor and/or line transformer may be used to couple the signal to this part with no dc offset.

$\overline{LB}$—LOOP-BACK CONTROL

When this pin is held low and $\overline{PD}$ is high (the UDLT is receiving transmissions from the master), the UDLT will use the eight bits of demodulated PCM data in place of the eight bits of Rx data in the return burst to the master, thereby looping the part back on itself for system testing. SI1 and SI2 operate normally in this mode. CLK will be held low during loop-back operation.

VD—VALID DATA OUTPUT

A high on this pin indicates that a valid line transmission has been demodulated. A valid transmission is determined by proper sync and the absence of detected bit errors. VD changes state on the leading edge of TE1. If no transmissions from the master have been received in the last 250 μs (derived from the internal oscillator), VD will go low without TE1 rising since TE1 is not generated in the absence of received transmissions from the master (see TE pin description for the one exception to this).

SI1, SI2—SIGNALING BIT INPUTS

Data on these pins is loaded on the rising edge of TE1 for transmission to the master. If no transmissions from the master are being received and $\overline{PD}$ is high, data on these pins will be loaded into the part on an internal signal. Therefore, data on these pins should be steady until synchronous communication with the master has been established, as indicated by the high on VD.

SO1, SO2—SIGNALING BIT OUTPUTS

These outputs are received signaling bits from the master UDLT and change state on the rising edge of TE1. These outputs have standard B-series CMOS output drive capability.

$\overline{PD}$—POWER-DOWN INPUT/OUTPUT

This is a bidirectional pin with weak output drivers such that it can be overdriven externally. When held low, the UDLT is powered down and the only active circuitry is: that which is necessary for demodulation, TE1/RE1/CLK generation upon demodulation the outputting of data received from the master and updating of VD status. When held high, the UDLT is powered-up and transmits in response to received transmissions from the master. If no received bursts from the master have occurred when powered-up, for 250 μs (derived from the internal oscillator frequency), the UDLT will generate a free running 125 μs internal clock from the internal oscillator and will burst a transmission to the master every other internal 125 μs clock using data on the SI1 and SI2 pins and the last data word loaded into the receive register. The weak output drivers will try to force $\overline{PD}$ high when a transmission from the master is demodulated and will try to force it low if 250 μs have passed without a transmission from the master. This allows the slave UDLT to self power-up and down in demand powered loop systems.

TE—TONE ENABLE

A high on this pin generates a 500 Hz square wave PCM tone and inserts it in place of the demodulated voice PCM word from the master for outputting to the Tx pin to the telset mono-circuit. A high on TE will generate TE1 and CLK from the internal oscillator when the slave is not receiving bursts from the master so that the PCM square wave can be loaded into the mono-circuit. This feature allows the user to provide audio feedback for the telset keyboard depressions except during Loop-Back. During Loop-Back of the slave UDLT, CLK is defeated so a tone cannot be generated in this mode.

TE1—TRANSMIT DATA ENABLE 1 OUTPUT

This is a standard B-series CMOS output which goes high after the completion of demodulation of an incoming transmission from the master. It remains high for eight CLK periods and then low until the next burst from the master is demodulated. While high, the voice data just demodulated is output on the first eight rising edges of CLK at the Tx pin. The signaling data just demodulated is output on SO1 and SO2 on TE1's rising edge, as is VD.

Tx—TRANSMIT DATA OUTPUT

This is a standard B-series CMOS output. Voice data is output on this pin on the rising edges of CLK while TE1 is high and is high impedance when TE1 is low.

X1—CRYSTAL INPUT

A 4.096 MHz crystal is tied between this pin and X2. A 10 megohm resistor across X1 and X2 and 25 pF capacitors from X1 and X2 to V_{SS} are required for stability and to insure start-up. X1 may be driven by an external CMOS clock signal if X2 is left open.

X2-CRYSTAL OUPUT

This pin is capable of driving one external CMOS input and 15 pF of additional capacitance. (SEE X1)

CLK—CLOCK OUTPUT

This is a standard B-series CMOS output which provides the data clock for the telset mono-circuit. It is generated by dividing the oscillator down to 128 kHz and starts upon the completion of demodulation of an incoming burst from the master. At this time, CLK begins and TE1 goes high. CLK will remain active for 16 periods, at the end of which it will remain low until another transmission from the master is demodulated. In this manner, sync from the master is established in the slave and any clock slip between the master and the slave is absorbed each frame. CLK is generated in response to an incoming burst from the master; however, if TE is brought high, then CLK and TE1/RE1 are generated from the internal oscillator until TE is brought low or an incoming burst from the master is received. CLK is disabled when $\overline{LB}$ is held low.

Rx—RECEIVE DATA INPUT

Voice data from the telset mono-circuit is input on this pin on the first eight falling edges of CLK after RE1 goes high.

Mu/A—TONE DIGITAL FORMAT INPUT

This pin determines if the PCM code of the 500 Hz square wave tone, generated when TE is high, is D3 (Mu/A = 1) or CCITT (Mu/A = 0) format.

RE1-RECEIVE DATA ENABLE 1 OUTPUT

This is a standard B-series CMOS output which is the inverse of TE1 (see TE1).

LO1, LO2—LINE DRIVER OUTPUTS

These outputs drive the twisted pair line with 256 kHz modified DPSK bursts each frame and are push-pull. These pins are driven to V_{ref} when the device is not modulating.

BACKGROUND

The MC145422 master and MC145426 slave UDLT transceiver ICs main application is to bidirectionally transmit the digital signals present at a codec/filter-digital PABX backplane interface over normal telephone wire pairs. This allows the remoting of the mono-circuit in a digital telephone set and enables each set to have a high speed data access to the PABX switching facility. In effect, the UDLT allows each PABX subscriber direct access to the inherent sixty-four kilobits per second data routing capabilities of the PABX.

The UDLT provides a means for transmitting and receiving sixty-four kilobits of voice data and sixteen kilobits-per-second of signaling data in two wire format over normal telephone pairs. The UDLT is a two chip set consisting of a master and a slave. The master UDLT replaces the codec/filter and SLIC on the PABX line card, and transmits and receives data over the wire pair to the telset. The UDLT appears to the linecard and backplane as if it were a PCM codec/filter and has almost the same digital interface features as the MC14400 series mono-circuits. The slave UDLT is located in the telset and interfaces the mono-circuit to the wire pair. By hooking two UDLTs back-to-back, a repeater can also be formed. The master and slave UDLTs operate in a frame synchronous manner, sync being established at the slave by the timing of the master's transmission. The master's sync is derived from the PABX frame sync.

The UDLT operates using one twisted pair. Eight bits of voice data and two bits of signaling data are transmitted and received each frame in a half duplex manner; i.e., the slave waits until the transmission from the master is completely received before transmitting back to the master. Transmission occurs at 256 kilohertz bit rate using a modified form of DPSK. This "ping-pong" mode will allow transmission of data at distances up to two kilometers before turnaround delay becomes a problem. The UDLT is so defined as to allow this data to be handled by the linecard, backplane, and PABX as if it were just another voice conversation. This allows existing PABX hardware and software to be unchanged and yet provides switched sixty-four kilobits per second voice or data communications throughout its service area by simply replacing a subscriber's linecard and telset. A feature in the master allows one of the two signaling bits to be inserted and extracted from the backplane PCM word to allow simultaneous voice and data transmission through the PABX. Both UDLTs have a loop-back feature by which the device can be tested in the user system.

The slave UDLT has the additional feature of providing a 500 hertz Mu or A-law coded square wave to the mono-circuit when the TE pin is brought high. This can be used to provide audio feedback in the telset during keyboard depressions.

CIRCUIT DESCRIPTION

GENERAL

The UDLT consists of a modulator, demodulator, two intermediate data buffers, sequencing and control logic, and transmit and receive data registers. The data registers interface to the linecard or mono-circuit digital interface signals, the modulator and demodulator interface the twisted pair transmission medium, while the intermediate data registers buffer data between these two sections. The UDLT is intended to operate on a single five volt supply and can be driven by TTL or CMOS logic.

MASTER OPERATION

In the master, data from the linecard is loaded into the receive register each frame from the Rx pin under the control of the TDC/RDC clock and the receive data enable, RE1. RE1 controls loading of eight serial bits, henceforth referred to as the voice data word. Each MSI, these words are transferred out of the receive register to the modulation buffer for subsequent modulation onto the line. The modulation buffer takes the received voice data word and the two signaling data input bits on SI1 and SI2 loaded on the MSI transition and formats the ten bits into a specific order. This data field is then transmitted in a 256 kilohertz modified DPSK burst onto the line to the remote slave UDLT.

Upon demodulating the return burst from the slave, the decoded data is transferred to the demodulation buffer and the signaling bits are stripped ready to be output on SO1 and SO2 at the next MSI. The voice data word is loaded into the transmit register as described in the TE1 pin description for outputting via the Tx pin at the TDC/RDC data clock rate under the control of TE1. VD is output on the rising edge of MSI. Timing diagrams for the master are shown in Figure 10.

SLAVE OPERATION

In the slave, the synchronizing event is the detection of an incoming line transmission from the master as indicated by the completion of demodulation. When an incoming burst from the master is demodulated, several events occur. As in the master, data is transferred from the demodulator to the demodulation buffer and the signaling bits are stripped for outputting at SO1 and SO2. Data in the receive register is transferred to the modulation buffer. TE1 goes high loading in data at SI1 and SI2, which will be used in the transmission burst to the master along with the data in the transmit data buffer, and outputting SO1, SO2, and VD. Modulation of the burst begins four 256 kilohertz periods after the completion of demodulation.

While TE1 is high, voice data is output on Tx to the telset mono-circuit on the rising edges of the data clock output on the CLK pin. On the ninth rising edge of CLK, TE1 goes low, RE1 goes high, and voice data from the mono-circuit is input to the receive register from the Rx pin on the next eight falling edges of CLK. RE1 is TE1 inverted and is provided to facilitate interface to the mono-circuit.

The CLK pin 128 kilohertz output is formed by dividing down the 4.096 megahertz crystal frequency by thirty-two. Slippage between the frame rate of the master (as represented by the completion of demodulation of an incoming transmission from the master) and the crystal frequency is absorbed by holding the sixteenth low period of CLK until the next completion of demodulation. This is shown in the slave UDLT timing diagram of Figure 11.

POWER-DOWN OPERATION

In the master, when $\overline{PD}$ is low, the UDLT stops modulating and only that circuitry necessary to demodulate the incoming bursts and output the signaling and VD data bits is active. In this mode, if the UDLT receives a burst from the slave, the SO1, SO2, and VD pins will change state upon completion of the demodulation instead of the rising edge of MSI. The state of these pins will not change until either three rising MSI edges have occurred without the reception of a burst from the slave or until another burst is demodulated, whichever occurs first.

When $\overline{PD}$ is brought high, the master UDLT will wait either three rising MSI edges or until the MSI rising edge following the demodulation of an incoming burst before transmitting to the slave. The data for the first transmission to the slave after power—up is loaded into the UDLT during the RE1 period prior to the burst in the case of voice, and on the present rising edge of MSI for signaling data.

In the slave, $\overline{PD}$ is a bidirectional pin with weak output drivers such that it can be overdriven externally. When held low, the UDLT slave is powered—down and only that circuitry necessary for demodulation, TE1/RE1/CLK generation upon demodulation, and the outputting of voice and signaling bits is active. When held high, the UDLT slave is powered-up and transmits normally in response to received transmissions from the master. If no bursts have been received from the master within 250 μs after power-up (derived from the internal oscillator frequency), the UDLT generates an internal 125 μs free-running clock from the internal oscillator. The slave UDLT then bursts a transmission to the master UDLT every other 125 μs clock period using data loaded into the Rx pin during the last RE1 period and SI1, SI2 data loaded in on the internal 125 μs clock edge. The weak output drivers will try to force $\overline{PD}$ high when a transmission from the master is demodulated and will try to force it low if 250 μs have passed without a transmission from the master. This allows the slave UDLT to self power-up and down in demand powered-loop systems.

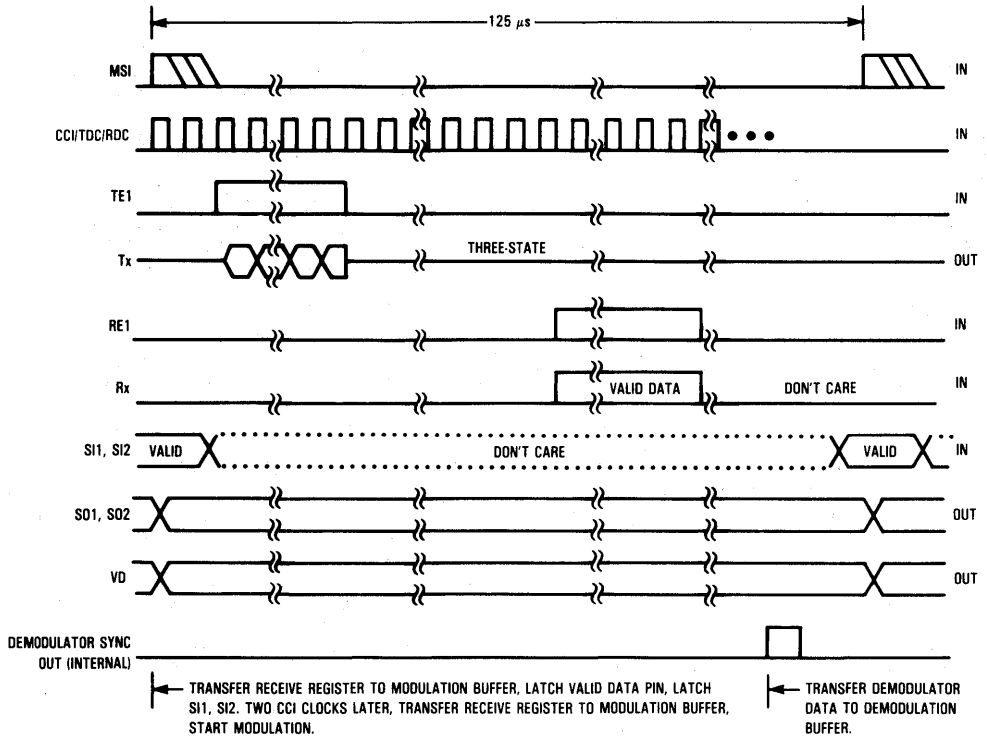
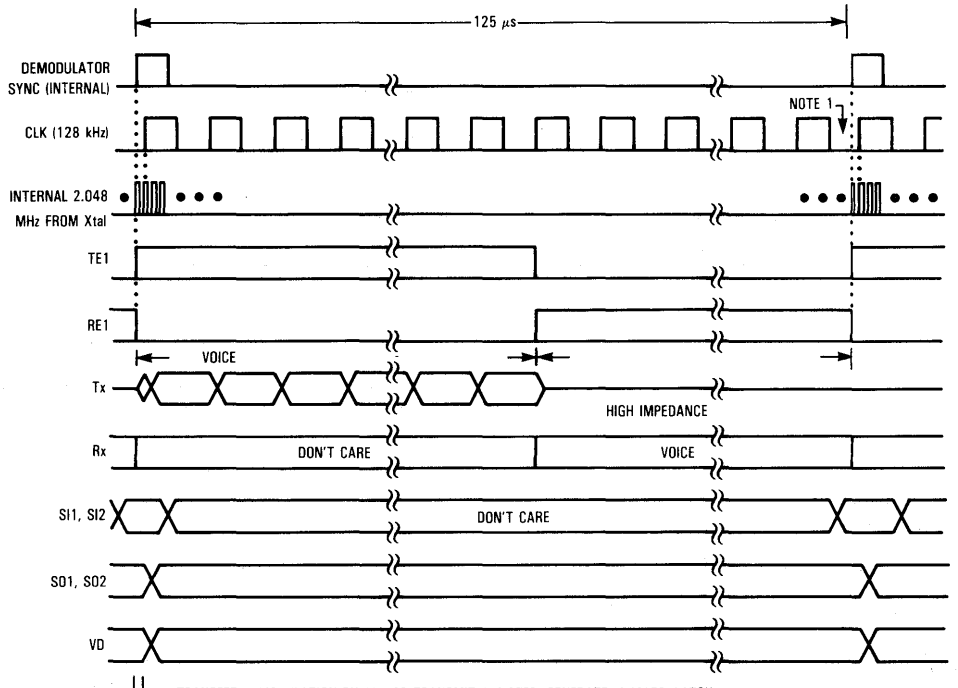


Figure 10. Master UDLT Timing



NOTE:
1. Slip between master and slave is taken up in this period.

Figure 11. Slave UDLT Timing

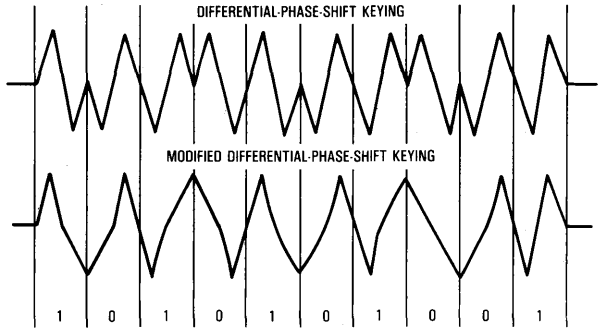
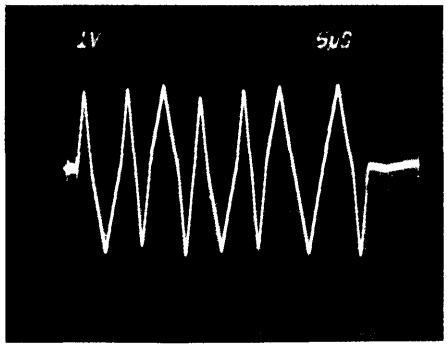


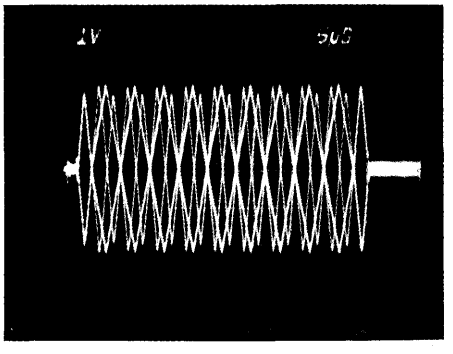
Figure 12. Modified Differential Phase Shift Keying

Both the Differential-Phase Shift Keying and the Modified Differential-Phase-Shift Keying waveforms are shown above. The DPSK encodes data as phase reversals of a 256 kHz carrier. A "0" is indicated by a 180 degree phase shift between bit boundaries, while the signal continues in phase to indicate a "1". This method needs no additional bits to indicate the start of the burst.

The Modified DPSK waveform actually used in the transceivers is a slightly modified form of DPSK, as shown in the figure. The phase-reversal cusps of the DPSK waveform have been replaced by a 128 kHz half cycle to lower the spectral content of the waveform, which, save for some key differences, appears quite similar to frequency-shift keying. The burst always begins and ends with a half cycle of 256 kHz, which helps locate bit boundaries.



13a–BIT PATTERN–1010101000

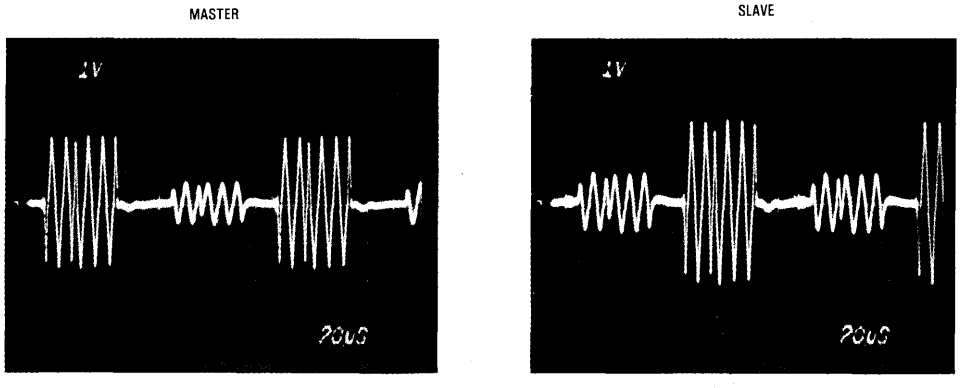


13b–BIT PATTERN–RANDOM

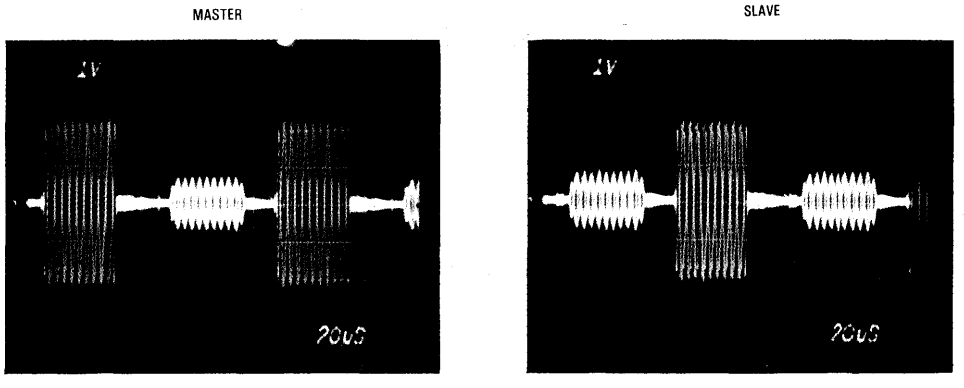
The bit pattern shown above in Figure 13a shows a stable waveform due to the even number of phase changes or zeros. The waveform shown in Figure 13b shows random data patterns being modulated.

Figure 13. Typical Modulated Waveforms

"Ping pong" signals on 3000 feet of 26 AWG twisted pair wire as viewed at LI (Line Input) of the master ULDT and the slave UDLT.



BIT PATTERN–1010101000



BIT PATTERN–RANDOM

Figure 14. Typical Signal Waveforms at Demodulator

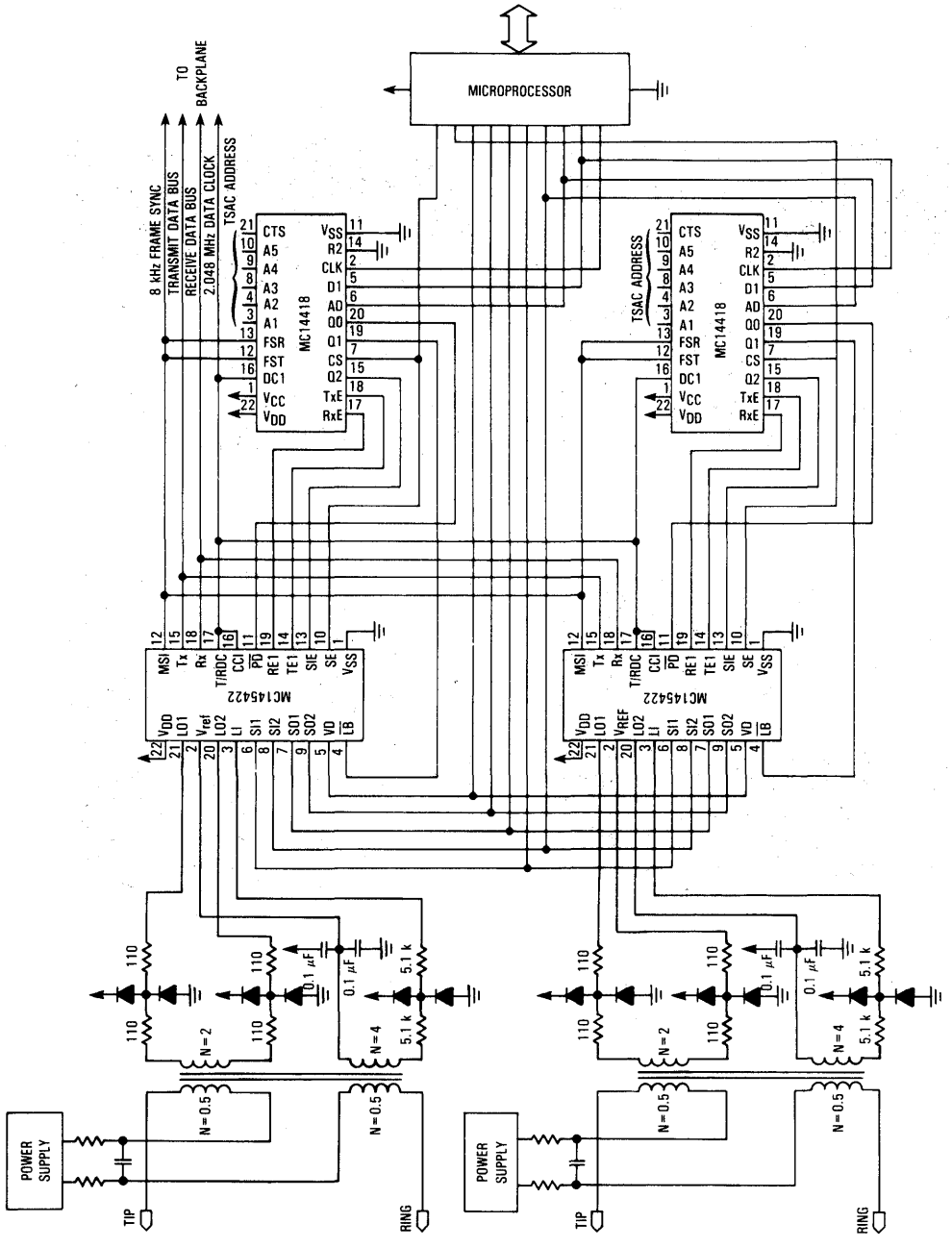


Figure 15. Typical Multichannel Digital Line Card

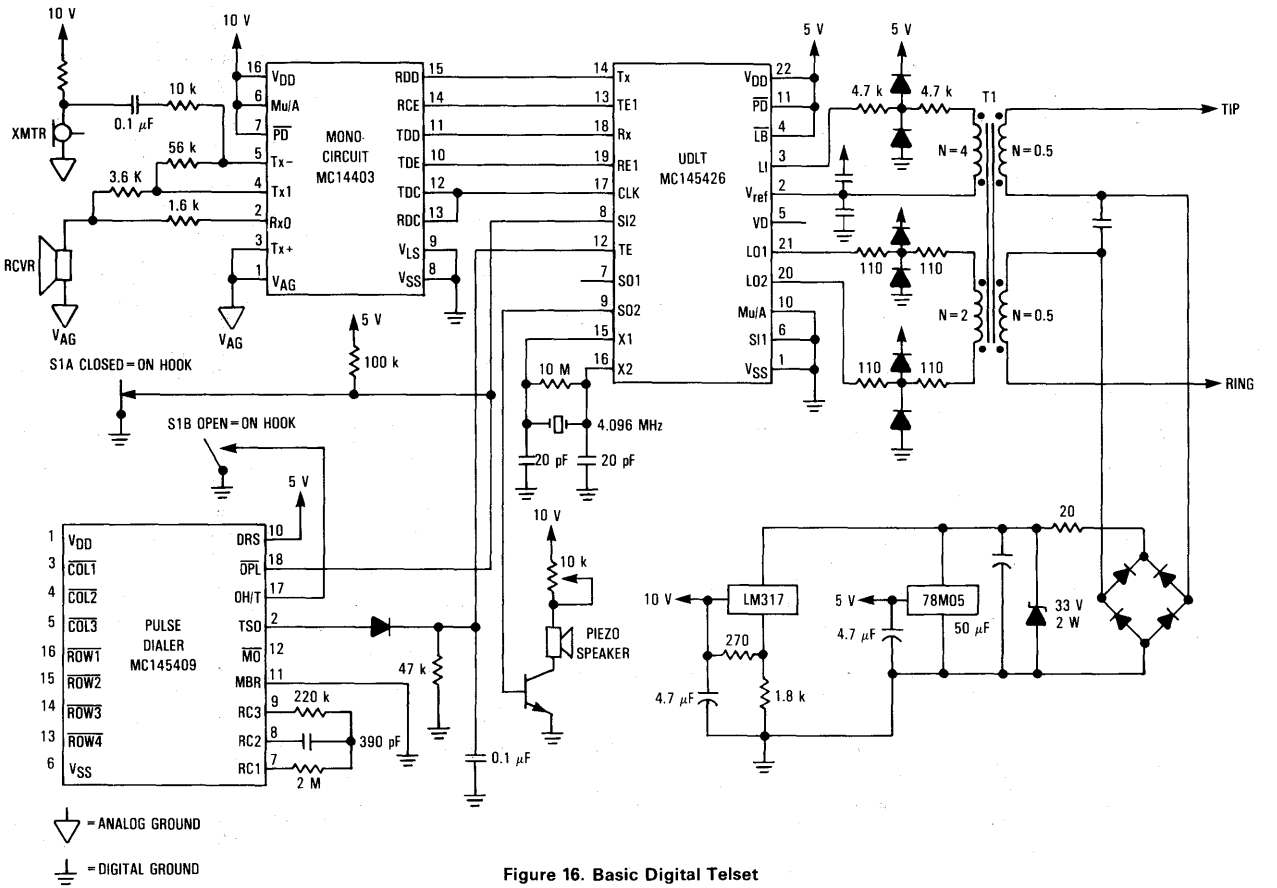


Figure 16. Basic Digital Telset

2

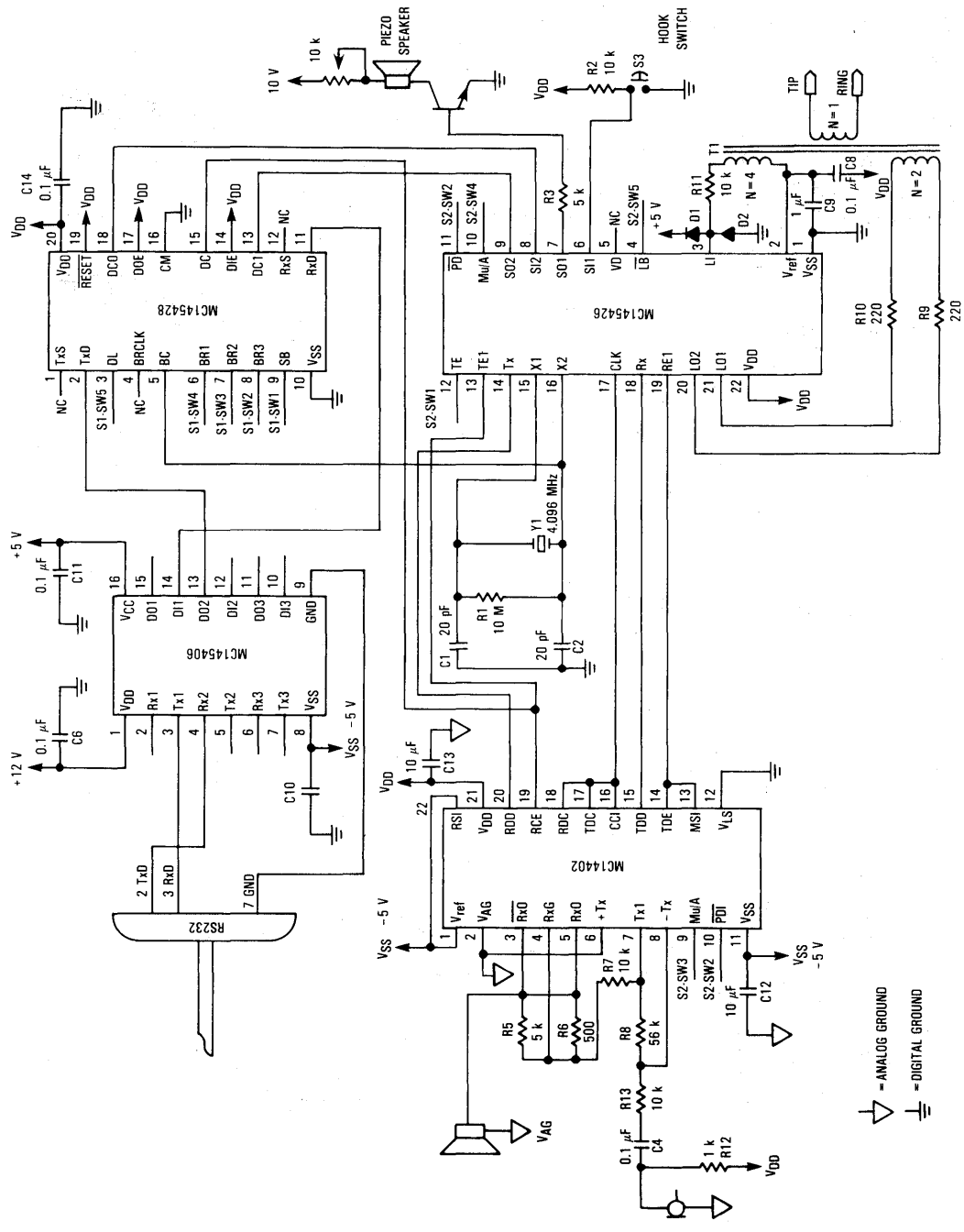


Figure 17. Full Featured Digital Telset

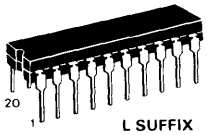
MC145428

MOTOROLA

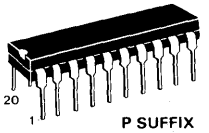
Advance Information

Data Set Interface

Asynchronous-To-Synchronous Synchronous-To-Asynchronous Converter



L SUFFIX
CERAMIC
CASE 732



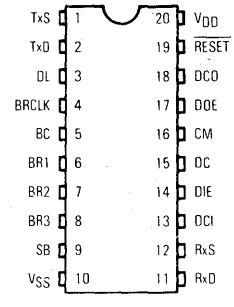
P SUFFIX
PLASTIC
CASE 738

2

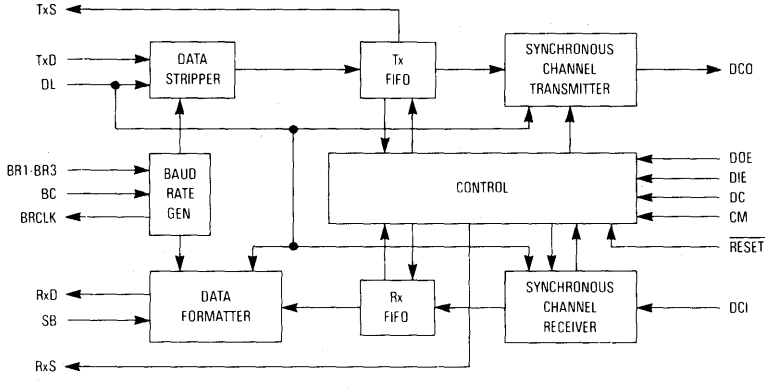
The MC145428 Data Set Interface provides asynchronous to synchronous and synchronous to asynchronous data conversion. It is ideally suited for voice/data digital telsets supplying an RS-232 compatible data port into a synchronous transmission link. Other applications include, data multiplexers, concentrators, data-only switching and PBX-based local area networks. This low power CMOS device directly interfaces with either the 64 kbps or 8 kbps channel of Motorola's MC145422 and MC145426 Universal Digital Loop Transceivers (UDLTs), as well as the MC145418 and MC145419 Digital Loop Transceivers (DLTs).

- Provides the Interface Between Asynchronous Data Ports and Synchronous Transmission Links
- Up to 128 kbps Asynchronous Data Rate Operation
- Up to 2.1 Mbps Synchronous Data Rate Operation
- On-board Bit Rate Clock Generator with Pin Selectable Bit Rates of 300, 1200, 2400, 4800, 9600, 19200 and 38400 bps or an Externally Supplied 16 Times Bit Rate Clock
- Accepts Asynchronous Data Words of Eight or Nine Bits in Length
- False Start Detection Provided
- Automatic Sync Insertion and Checking
- Single 5 Volt Power Supply
- Low Power Consumption of 5 mW Typical
- Applications Notes AN943 and AN946

PIN ASSIGNMENT



BLOCK DIAGRAM



This document contains information on a new product. Specifications and information herein are subject to change without notice.

MAXIMUM RATINGS (Voltages Referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD} - V_{SS}	-0.5 to 6.0	V
Voltage, Any Pin to V_{SS}	V	-0.5 to V_{DD} +0.5	V
DC Current, Any Pin (Excluding V_{DD}, V_{SS})	I	+10	mA
Operating Temperature	T_A	-40 to +85	°C
Storage Temperature	T_{stg}	-85 to +150	°C

DIGITAL CHARACTERISTICS (V_{DD} = 4.5 to 5.5 V, T_A = 0 to 70°C)

Parameter	Symbol	V_{DD}	Min	Max	Unit
Input High Level	V_{IH}	5	3.5	—	V
Input Low Level	V_{IL}	5	—	1.5	V
Input Current	I_{in}	—	—	+1.0	μA
Input Capacitance	C_{in}	—	—	7.5	pF
Output High Current (Source)	I_{OH}				mA
V_{OH} = 2.5 V		5	-1.7	—	
V_{OH} = 4.6 V		5	-0.36	—	
Output Low Current	I_{OL}				mA
V_{OL} = 0.4 V		5	0.36	—	
V_{OL} = 0.8 V		5	0.8	—	
Operating Current (DC = 128 kHz, BC = 4.096 MHz)	I_{DD}	5	—	2.0	mA

SWITCHING CHARACTERISTICS (C_L = 50 pF, V_{DD} = 5 V, T_A = 25°C)

Characteristic	Min	Typ	Max	Unit
Baud Clock Bit Rate Input Frequency				MHz
(BR1, BR2, BR3) = (0,0,0)	—	—	2.1	
(BR1, BR2, BR3) = non-zero	—	—	4.1	
Baud Clock Pulse Width	100	—	—	ns
Data Clock Frequency	—	—	2.1	MHz
Data Clock Pulse Width	200	—	—	ns

MC145428 DSI PIN DESCRIPTIONS

V_{DD}, POSITIVE POWER SUPPLY

The most positive power supply pin, normally 5 volts.

V_{SS}, NEGATIVE POWER SUPPLY

The most negative supply pin, normally 0 volts.

TxD, TRANSMIT DATA INPUT

Input for asynchronous data. Idle is logic high; break is 11 baud or more of logic low. One stop bit is required.

RxD, RECEIVE DATA OUTPUT

Output for asynchronous data. The number of stop bits and the data word length are selected by the SB and DL pins. Idle is logic high; break is a continuous logic low.

TxS, TRANSMIT STATUS OUTPUT

This pin will go low if the transmit FIFO holds 2 or more data words or if $\overline{\text{RESET}}$ is low.

RxS, RECEIVE STATUS OUTPUT

This pin will go low if framing of the synchronous channel is lost or not established or if $\overline{\text{RESET}}$ is low, or if the receive FIFO is overwritten.

SB, STOP BITS INPUT

This pin controls the number of stop bits the DATA FORMATTER will re-create when outputting data at the RxD asynchronous output. A high on this pin selects two stop bits; a low selects one stop bit.

DL, DATA LENGTH INPUT

This pin instructs the DSI to look for either 8 or 9 bits of data to be input at the TxD asynchronous input between the start and stop bits. The DL input also instructs the DSI's SYNCHRONOUS CHANNEL RECEIVER and SYNCHRONOUS CHANNEL TRANSMITTER to expect 8 or 9 bit data words and also instructs the DSI's DATA FORMATTER to re-create 8 or 9 data bits between the start and stop bits when outputting data at its RxD asynchronous output. A high on this pin selects a 9 bit data word; a low selects an 8 bit data word length.

MC145428 DSI PIN DESCRIPTIONS — cont'd.

BC, BAUD CLOCK INPUT

This pin serves as an input for an externally supplied 16 times data clock. Otherwise, the BC pin expects a 4.096 MHz clock signal which is internally divided to obtain the 16 times clock for the most frequently used standard bit rates (see BR1-BR3 pin description).

BRCLK, 16 TIMES CLOCK INTERNAL OUTPUT

This pin outputs the internal 16 times asynchronous data rate clock.

BR1, BR2, BR3, BIT RATE SELECT INPUTS

These three pins select the asynchronous bit rate, either externally supplied at the BC pin (16 times clock) or one of the internally supplied bit rates. (See Table 1.)

DCO, DATA CHANNEL OUTPUT

This pin is a three-state output pin. Synchronous data is output when DOE is high. This pin will go high impedance when DOE or $\overline{\text{RESET}}$ are low. When CM is low, synchronous data is output on DCO on the falling edges of DC as long as DOE is high. When CM is high, synchronous data is output on DCO on the rising edges of DC, while DOE is held high. No more than eight data bits can be output during a given DOE high interval when CM = high. This feature allows the DSI to interface directly with the MC145422/26 Universal Digital Loop Transceivers (UDLT's) and PABX time division multiplexed highways.

DOE, DATA OUTPUT ENABLE INPUT

See DCO pin description and the SYNCHRONOUS CHANNEL INTERFACE section.

DIE, DATA INPUT ENABLE INPUT

See DCI pin description and the SYNCHRONOUS CHANNEL INTERFACE section.

DC, DATA CLOCK INPUT

See DCI and DCO pin descriptions and the SYNCHRONOUS CHANNEL INTERFACE section.

CM, CLOCK MODE INPUT

See the SYNCHRONOUS CHANNEL INTERFACE section and the SYNCHRONOUS CLOCKING MODE SUMMARY. (See Table 2.)

$\overline{\text{RESET}}$, RESET INPUT

When held low, this pin clears the internal FIFO's, forces the TxD asynchronous input to appear high to the DSI's internal circuitry, forces TxS and RxS low. When returned high, normal operation results.

When the $\overline{\text{RESET}}$ input is returned high the DSI's SYNCHRONOUS CHANNEL RECEIVER will not accept or transfer any incoming data words on the DCI pin to the Rx FIFO until one "flag" word is input at the DCI pin. (Also see RxS pin description.)

DCI, DATA CHANNEL INPUT

Synchronous data is input on this pin on the falling edges of DC when DIE is high.

Table 1. Programmable Baud Rates

BR3	BR2	BR1	Bit Rate (bps)	BC in MHz	BRCLK
0	0	0	Variable 0 to 128 kbps	0 to 2.1 MHz	0 to 2.1 MHz
0	0	1	38.4 k	4.096	614.4 kHz
0	1	0	19.2 k	4.096	307.2 kHz
0	1	1	9600	4.096	153.6 kHz
1	0	0	4800	4.096	76.8 kHz
1	0	1	2400	4.096	38.4 kHz
1	1	0	1200	4.096	19.2 kHz
1	1	1	300	4.096	4.8 kHz

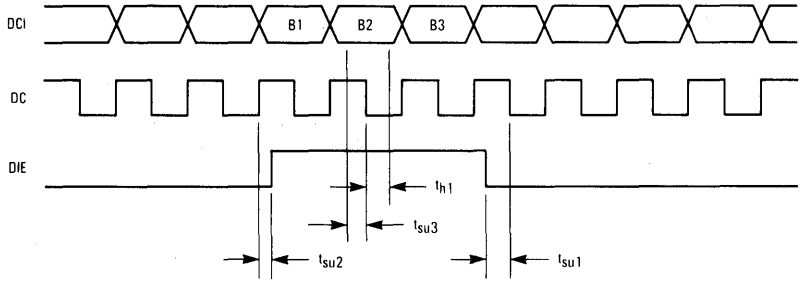
CM = LOW, SYNCHRONOUS CHANNEL RECEIVER INPUT SWITCHING CHARACTERISTICS

(C_L = 50 pF, V_{DD} = 5 V, T_A = 25°C) (See Figure 1A)

Characteristic	Symbol	Min	Typ	Max	Unit	Notes
DIE Fall Before DC Falls	t_{su1}	40	-9	—	ns	1
DIE Rise After Rise of DC	t_{su2}	40	+24	—	ns	2
DCI Data Stable Before DC Falling Edge	t_{su3}	40	-5	—	ns	3
DCI Data Stable After DC Falling Edge	t_{h1}	40	0	—	ns	4

2

NOTES:
1. Time DIE must fall before DC falls in order to avoid reading the bit after B3.
2. Time DC must be high before DIE rise in order to avoid clocking in the bit before B1. (See Synchronous Channel Interface for further details and see Figure 1A.)
3. Time data must be stable on the DCI pin before falling edge of the data clock DC.
4. Time data must be stable on the DCI pin after the falling edge of the data clock DC.



NOTE: When CM = 0, data bits are read into the DSI's SYNCHRONOUS CHANNEL RECEIVER at the DCI pin on the falling edge of the signal formed by the LOGICAL NAND of $\overline{DC}$ and DIE.
i.e. ψ of $\overline{DC}$ • DIE

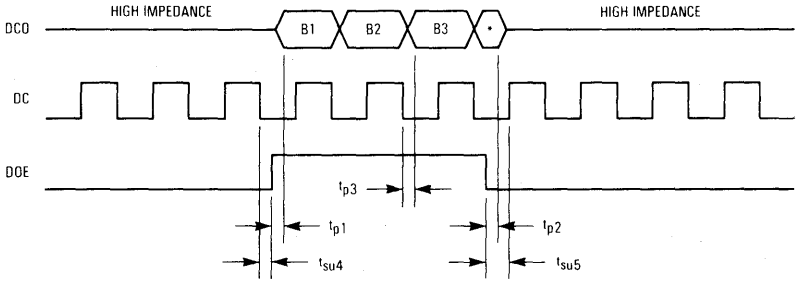
Figure 1A. CM = Low, Synchronous Channel Receiver Input Switching Characteristics

CM = LOW, SYNCHRONOUS CHANNEL TRANSMITTER OUTPUT SWITCHING CHARACTERISTICS

(C_L = 50 pF, V_{DD} = 5 V, T_A = 25°C) (See Figure 1B)

Characteristic	Symbol	Min	Typ	Max	Unit	Notes
DC Falling to DOE Rising	t_{su4}	0	10	—	ns	5
DOE Falling to DC Rising	t_{su5}	40	-5	—	ns	6
DOE Rising to DCO Active	t_{p1}	50	28	—	ns	7
DOE Falling to High-Z of DCO	t_{p2}	50	26	—	ns	8
DC Falling to DCO	t_{p3}	80	71	—	ns	9

NOTES:
5. Time DC must be low before the rising edge of DOE in order to avoid clocking out a data bit before B1. (See Synchronous Channel Interface section for further details and also Figure 1B.)
6. Time DOE must be low before the rising edge of DC in order for the (*) bit to be output in the B1 position in the next cycle.
7. Propagation delay time from the rising edge of DOE to the low output impedance state of the DCO pin.
8. Propagation delay time from the falling edge of DOE to the high output impedance state of the DCO pin.
9. Propagation delay time from the falling edge data of the data clock DC to valid data on the DCO pin.



*This bit will be output in the B1 position on the next cycle of DOE.

NOTE: When CM = Low, data bits are advanced from the DSI's SYNCHRONOUS CHANNEL TRANSMITTER at the DCO pin on the rising edge of the signal formed by the LOGICAL NAND of DC and DOE. i.e. ↑ of $\overline{DC \bullet DOE}$

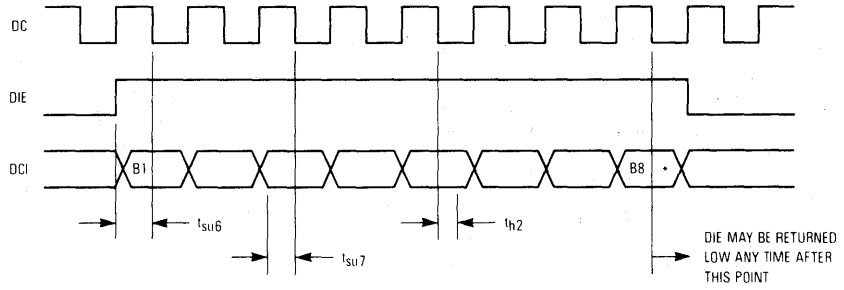
Figure 1B. CM = Low, Synchronous Channel Transmitter Output Switching Characteristics

CM = HIGH, SYNCHRONOUS CHANNEL RECEIVER INPUT SWITCHING CHARACTERISTICS

(C_L = 50 pF, V_{DD} = 5 V, T_A = 25°C) (See Figure 1C)

Characteristic	Symbol	Min	Typ	Max	Unit	Notes
DIE Rising to DC Falling	t_{su6}	100	76	—	ns	10
DCI to DC Falling	t_{su7}	40	-4	—	ns	11
DC Falling to DCI	t_{h2}	20	0	—	ns	12

NOTES:
10. Time DIE must be high before the falling edge of DC in order for the data bit to be accepted by the synchronous data input of the DSI. (See Synchronous Channel Interface for further details.)
11. Time DCI data must be stable before the falling edge of the data clock DC.
12. Time DCI data must be stable after the falling edge of the data clock DC.



*Last bit accepted.

NOTE: When CM = 1, data bits are read into the DSI's SYNCHRONOUS CHANNEL RECEIVER at the DCI pin on the falling edge of the signal formed by the LOGICAL AND of DC and DIE. (DC • DIE)

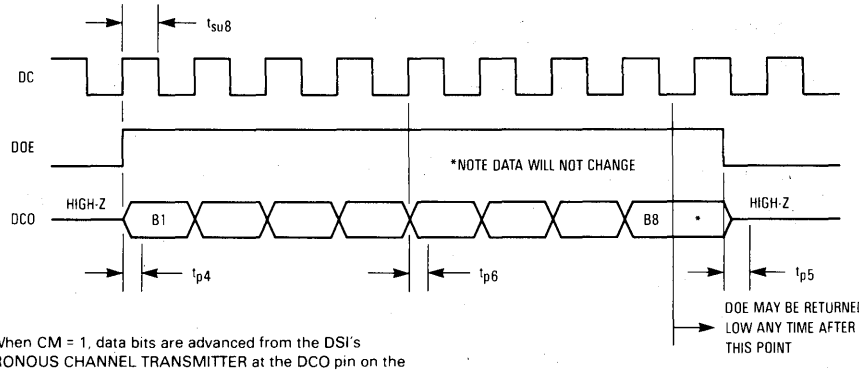
Figure 1C. CM = High, Synchronous Channel Receiver Input Switching Characteristics

CM = HIGH, SYNCHRONOUS CHANNEL TRANSMITTER OUTPUT SWITCHING CHARACTERISTICS

(C_L = 50 pF, V_{DD} = 5 V, T_A = 25°C) (See Figure 1D)

Characteristic	Symbol	Min	Typ	Max	Unit	Notes
DC Falling to DOE Rising	t_{su8}	100	82	—	ns	13
DOE Rising to Active Data on DCO	t_{p4}	105	87	—	ns	14
DOE Falling to High-Z on DCO	t_{p5}	50	28	—	ns	15
DC Rising to DCO	t_{p6}	100	74	—	ns	16

NOTES:
13. Time DOE must be high before the falling edge of the data clock DC.
14. Time delay between the rise of the DOE pin and the time the DCO reaches the low impedance state.
15. Time delay between the fall of the DOE pin and the time the DCO pin reaches the high impedance state.
16. Delay from the rising edge of the data clock DC to the valid data on the DCO pin.



NOTE: When CM = 1, data bits are advanced from the DSI's SYNCHRONOUS CHANNEL TRANSMITTER at the DCO pin on the rising edge of the signal formed by the LOGICAL AND of DC and DOE. (DC • DOE)

Figure 1D. CM = High, Synchronous Channel Transmitter Output Switching Characteristics

CIRCUIT DESCRIPTION

The MC145428 Data Set Interface provides a means for conversion of an asynchronous (start/stop format) data channel to a synchronous data channel and synchronous to asynchronous data channel conversion. Although primarily intended to facilitate the implementation of RS-232 compatible asynchronous data ports in digital telephone sets using the MC145422/26 UDLTs, this device is also useful in many applications that require the conversion of synchronous and asynchronous data.

TRANSMIT CIRCUIT

Asynchronous data is input on the TxD pin. This data is expected to consist of a start bit (logic low) followed by eight or nine data bits and one or more stop bits (logic high). The length of the data word is selected by the DL pin. The data baud rate is selected with the BR1, BR2, and BR3 pins to obtain the internal sampling clock. This internal sampling clock is selected to be 16 times the baud rate at the TxD pin. An externally supplied 16 times clock may also be used, in which case, the BR1, BR2, and BR3 pins should all be at logic zero and the 16 times sampling clock supplied at the BC pin.

Data input at the TxD pin is stripped of start and stop bits and is loaded into a four-word deep FIFO register. A break condition is also recognized at the TxD pin and this information is relayed to the synchronous channel transmitter which codes this condition so it may be re-created at the remote receiving device.

The synchronous channel transmitter sends one bit at a time under control of the DC, CM, and DOE pins. The synchronous channel transmitter transmits one of three possible data patterns based on whether or not the top of the Tx FIFO is full and whether or not a break condition has been recognized by the data stripper. When no data is available at the top of the Tx FIFO for transmission, the synchronous data transmitter sends a special synchronizing flag pattern (01111110). When a break condition is detected by the data stripper and no data is available at the top of the Tx FIFO, the break pattern (11111110) is sent. Figure 2A depicts this operation.

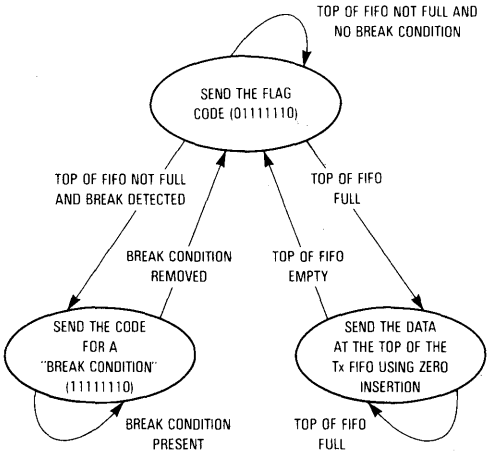


Figure 2A. Synchronous Data Channel Transmitter Operation

When stripped data words reach the top of the Tx FIFO they are loaded into the SYNCHRONOUS CHANNEL TRANSMITTER and are sent using a special zero insertion technique. When stripped data is being transmitted, the synchronous data transmitter will insert a binary 0 after any succession of five continuous 1's of data. Therefore, using this technique, no pattern of (01111110) or (11111110) can occur while sending data. This also allows the DSI to synchronize itself to the incoming synchronous data word boundaries based on the data alone.

The receive section of the DSI (synchronous channel receiver) performs the reverse operation by removing a binary 0 that follows five continuous 1's in order to recover the transmitted data. (Note that a binary 1 which follows five continuous 1's is not removed so that flags and breaks may be detected.) Figure 2B shows an example of this process.

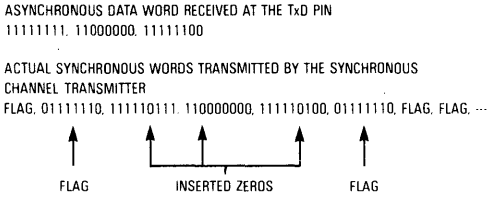


Figure 2B. Data Format Protocol

If the incoming data rate at TxD exceeds the rate at which it is output at DCO, the FIFO will fill. The TxS pin will go low when the FIFO contains two or more words. TxS may, therefore, be used as a local Clear-to-Send control line at the asynchronous interface port to avoid transmit data over-runs.

In order to insure synchronization during the transfer of a continuous stream of data the DSI's synchronous channel transmitter will insert a flag synchronizing word (01111110) every 61st data word. The DSI's synchronous channel receiver checks for this synchronizing word and if not present, the loss of synchronization will be indicated by the RxS pin being latched low until the flag synchronizing word is received. Note that under these conditions the data will continue to output at RxD.

RECEIVE CIRCUIT

Data incoming from the synchronous channel is loaded into the MC145428 at the DCI pin under the control of the DC and DIE pins (see SYNCHRONOUS CHANNEL INTERFACE section). Framing information, break code detection, and data word recovery functions are performed by the SYNCHRONOUS CHANNEL RECEIVER. Recovered data words are loaded into the four word deep Rx FIFO. When the recovered data words reach the top of the Rx FIFO they are taken by the DATA FORMATTER, start and stop bits are re-inserted and the re-constructed asynchronous data is output at the RxD pin at the same baud rate as the transmit side. The number of stop bits and word length are those selected by the SB and DL pins.

Loss of framing, if it occurs, is indicated by the RxS pin going low. Data will continue to be output under these conditions, but RxS will remain low until frame synchronization, i.e., the detection of a framing flag word, is re-established. If the output data rate is less than the data rate of the incoming synchronous data channel, data will be lost at a rate of one word at a time due to the bottom word on the Rx FIFO being overwritten. In order to prevent data loss (in the form of asynchronous terminal to asynchronous terminal over-runs) due to clock slip between remote DSI links, (during long bursts of continuous data) the DSI purposely reduces the length of the stop bit which it re-creates at its RxD output by 1/32nd. This action allows the originator of a transmission (of asynchronous data) to be up to 3% faster than the receive device is expecting for any given data rate. This tolerance is well within the normally expected differences in clock frequencies between remote stations. If the Rx FIFO is overwritten the RxS line will pulse low for one DC clock period following the over-writing of the bottom level of the Rx FIFO.

INITIALIZATION

Initialization is accomplished by use of the $\overline{\text{RESET}}$ pin. When held low, the internal FIFOs are cleared, the TxD input appears high to the data strippers internal circuitry, DCO is forced to a high impedance state, TxS and RxS are forced low. When brought high normal operation resumes and the synchronous channel transmitter sends the flag code until data has reached the top of the Tx FIFO. Note that the TxS line will immediately go high after $\overline{\text{RESET}}$ goes high, while RxS

will remain low until framing is detected. The synchronous channel receiver section of the DSI is forced into a "HOLD" state while the $\overline{\text{RESET}}$ line is low. The synchronous channel receiver remains in the "HOLD" state after $\overline{\text{RESET}}$ goes high until a flag code word (01111110) is received at the DCI pin. While in the "HOLD" state no data words can be transferred to the Rx FIFO and, therefore, the DATA FORMATTER and RxD line are held in the MARK idle state. After receiving the flag code pattern the RxS line goes high and normal operation proceeds. $\overline{\text{RESET}}$ should be held low when power is first applied to the DSI. $\overline{\text{RESET}}$ may be tied high permanently, if a short period of undefined operation at initial power application can be tolerated.

SYNCHRONOUS CHANNEL INTERFACE

The synchronous channel interface is generally operated in one of three basic modes of operation. The first is a continuous mode. A new data bit is clocked out of the DCO pin on each successive falling edge of the DC clock, and a new data bit is accepted by the DSI at its DCI pin on each successive falling edge of the DC clock. In this mode of operation, the CM control line is always low and the DOE and DIE enable control lines are always high. This is the typical setup when interfacing the DSI to the 8 kbps signal bit inputs and outputs of the MC145422/26 UDLTs. (See Figures 3A and 4.)

The second synchronous clocking mode is one in which 8 bits at a time are clocked out of the SYNCHRONOUS CHANNEL TRANSMITTER, and 8 bits are read by the SYNCHRONOUS CHANNEL RECEIVER at a time. The transferring of these 8 bit groups of data would normally be repeated on some cyclic basis. An example is a time division multiplexed data highway. In this mode (CM = 1), the rising edge of the enable signal DIE and DOE should be roughly aligned to the rising edge of the DC clock signal. When enabled, the data is clocked out on the rising edge of the DC clock through the DCO pin and clocked in on the falling edge of the DC clock through the DCI pin. A variation of this clocking mode is to transfer less than 8 bits of data into or out of the DSI on a cyclic basis. If less than eight bits are to be transmitted and received, enable pins DIE and DOE should be returned low while the DC clock is low. This is illustrated in Figure 3D where five bits are being clocked out of the DSI through the DCO pin and four bits are being input to the DSI through the DCI pin.

This restriction does not apply if eight bits are to be clocked into or out of the synchronous channels of the DSI; i.e., the DSI has internal circuitry to prevent more than eight clocks following the rising edge of the respective enable signals). Figure 3B illustrates a timing diagram depicting an eight bit data format. If the DOE enable is held high beyond the eight clock periods the last data bit B8 will remain at the output of the DCO pin until the DOE enable is brought low to reinitialize the sequence. Similarly the DSI's SYNCHRONOUS CHANNEL RECEIVER will read (at its DCI input) a maximum of eight data bits for any given DIE high period.

The CM = high mode, using 8 bits of data, is the typical setup for interfacing the DSI to the 64 kbps channel of the MC145422 or MC145426 Universal Digital Loop Transceivers. (See Figure 3B and Figure 5.)

In the third mode of operation, an unlimited variable number of data bits may be clocked into or out of the synchronous side of the DSI at a time. When the CM line is low, any number of data bits may be clocked into or out of the DSI's synchronous channels provided that the respective enable signal is high. Figure 3C illustrates three data bits being clocked out of the DCO pin and three data bits being clocked into the DCI pin.

In the CM = low mode of operation, an internal clock is formed, which is the logical NAND of DC, DOE and $\overline{\text{CM}}$, ($\overline{\text{DC} \bullet \text{DOE} \bullet \overline{\text{CM}}}$). It is on the rising edge of this signal that a new data bit is clocked out of the DCO pin. Therefore, the DOE signal should be raised and lowered following the falling edge of the DC clock (i.e., when the DC clock is low).

Also in the CM = low mode of operation, another internal clock is formed which is the logical NAND of $\overline{\text{DC}}$, DIE, and $\overline{\text{CM}}$ ($\overline{\overline{\text{DC}} \bullet \text{DIE} \bullet \overline{\text{CM}}}$). It is on the falling edge of this signal that a new bit is clocked into the DCI pin. Therefore the DIE signal should be raised and lowered following the rising edge of the DC clock (i.e., when the DC clock is high).

The following table summarizes when data bits are advanced from the synchronous channel transmitter and when data bits are read by the synchronous channel receiver dependent on the CM control line. (Shown below in Table 2.)

Table 2. Synchronous Clocking Mode Summary

Mode	Bits Advanced From The Synchronous Channel Transmitter On;	Bits Read By The Synchronous Channel Receiver On:
CM = 0	The rising edge of an internal clock formed by the logical NAND of DOE and DC. i.e. ↑ of $\overline{\text{DOE} \bullet \text{DC}}$	The falling edge of an internal clock formed by the logical NAND of DIE and $\overline{\text{DC}}$. i.e. ↓ of $\overline{\text{DIE} \bullet \overline{\text{DC}}}$
CM = 1	The rising edge of an internal clock formed by the logical AND of DOE and DC. i.e. ↑ of DOE • DC	The falling edge of an internal clock formed by the logical AND of DIE and DC. i.e. ↓ of DIE • DC

TIMING DIAGRAMS

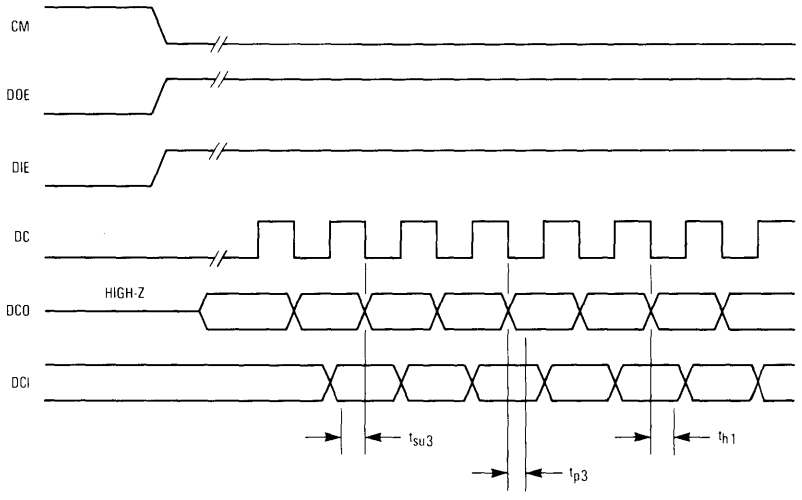


Figure 3A. Synchronous I/O, Continuous Bit Rate, Clock Mode Low

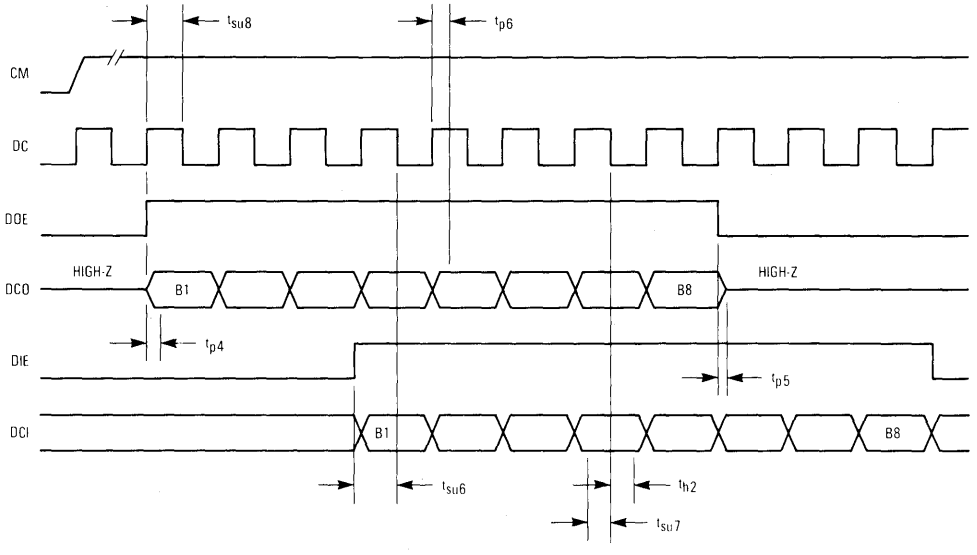


Figure 3B. Synchronous I/O, Eight Bit, Clock Mode High

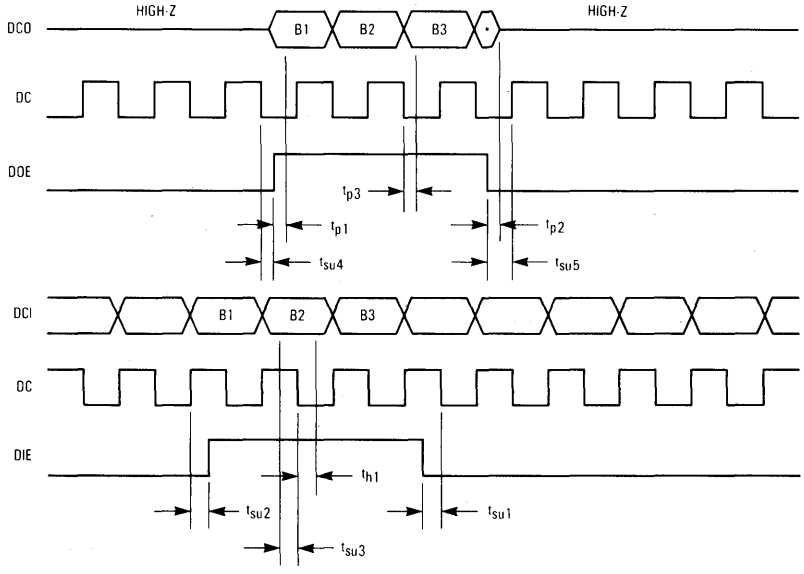


Figure 3C. Synchronous I/O, Variable Bit Length, Clock Mode Low

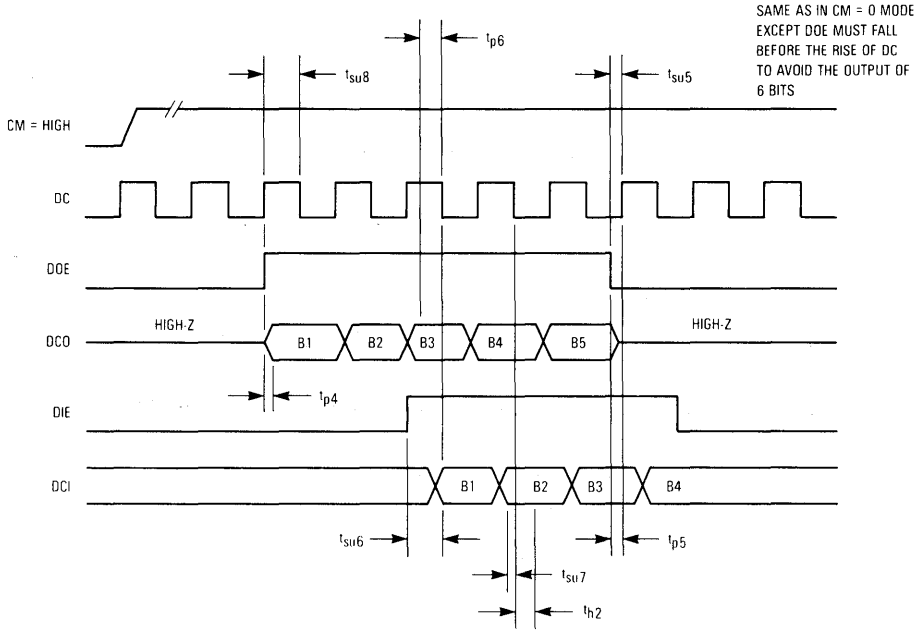
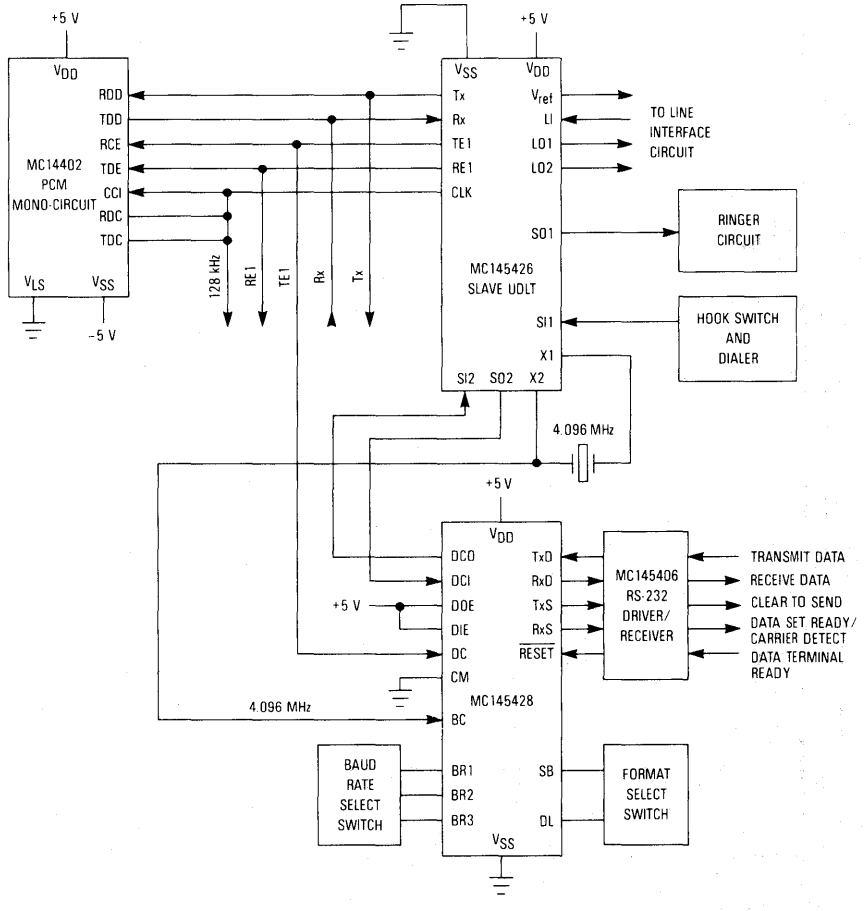
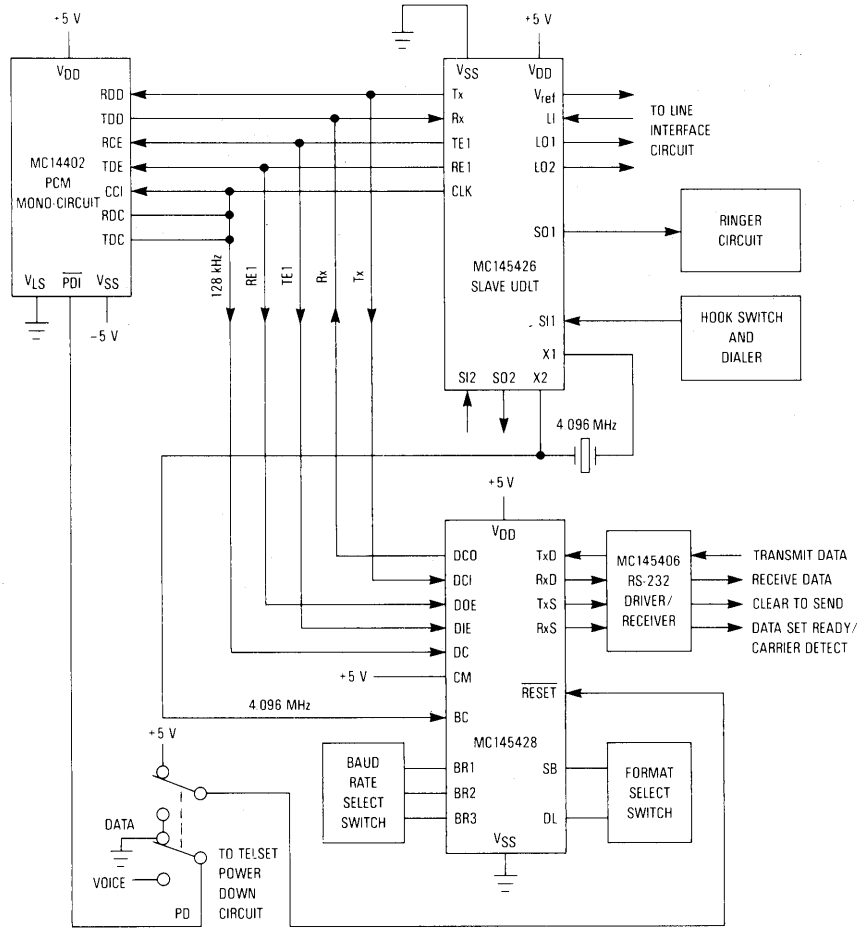


Figure 3D. Synchronous I/O, Variable Bit Length, Clock Mode High



NOTE: Some pin connections on the MC145426 and MC14402 have been omitted. Consult MC145426 and MC14402 data sheets for more details.

Figure 4. Digital Telset RS-232 Port Using 8 Kilobits/Second Channel of MC145426



NOTE: Some pin connections on the MC145426 and MC14402 have been omitted. Consult MC145426 and MC14402 data sheets for more details.

Figure 5. Digital Telset RS-232 Port Using 64 Kilobits/Second Channel of MC145426 for Voice or Data

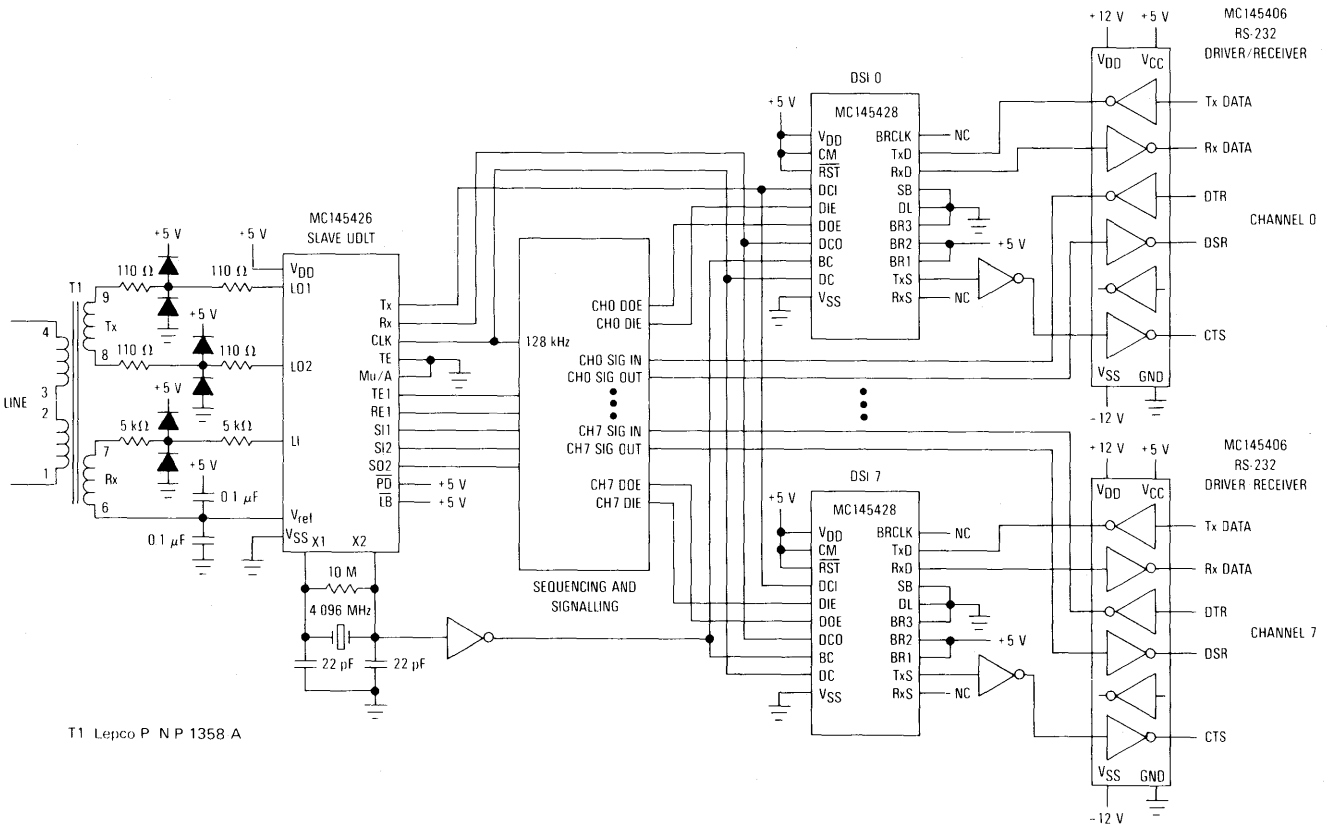


Figure 6. Multiplexing Eight RS-232 Telset Ports Into 64 Kilobits/Second Channel of MC145426

MOTOROLA

MC145429

Advance Information

2

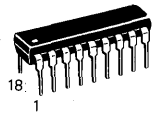
TELSET AUDIO INTERFACE CIRCUIT

The MC145429 is a silicon-gate CMOS Telset Audio Interface Circuit (TAIC) intended for microcomputer controlled digital or analog telset applications. The device provides the interface between a codec/filter or analog speech network and the telset mouthpiece, earpiece, ringer/speaker amplifier, and an auxiliary input and output. The configuration of the device is programmed via a serial digital data port. Features provided on the device include:

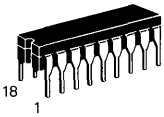
- Independent Adjustment of Earpiece, Speaker, and Ringer Volume
- Transient Suppression Circuitry to Prevent Acoustic "Pops"
- Receive Low-Pass Filter for 8 kHz Attenuation
- Sixteen Possible Audio Configurations
- Power-Down Mode with Data Retention
- 20 dB Mouthpiece Input Gain
- Receive to Transmit Loopback Test Mode
- Provision for Auxiliary Input and Output
- Externally Adjustable Auxiliary Input Gain
- PCM Mono-circuit Compatible Power Supply Range
- Digital Output for Speaker Amplifier Control
- Versatile Logic Input Levels
- 18-Pin Package

CMOS
(LOW-POWER COMPLEMENTARY MOS)

TELSET
AUDIO INTERFACE
CIRCUIT

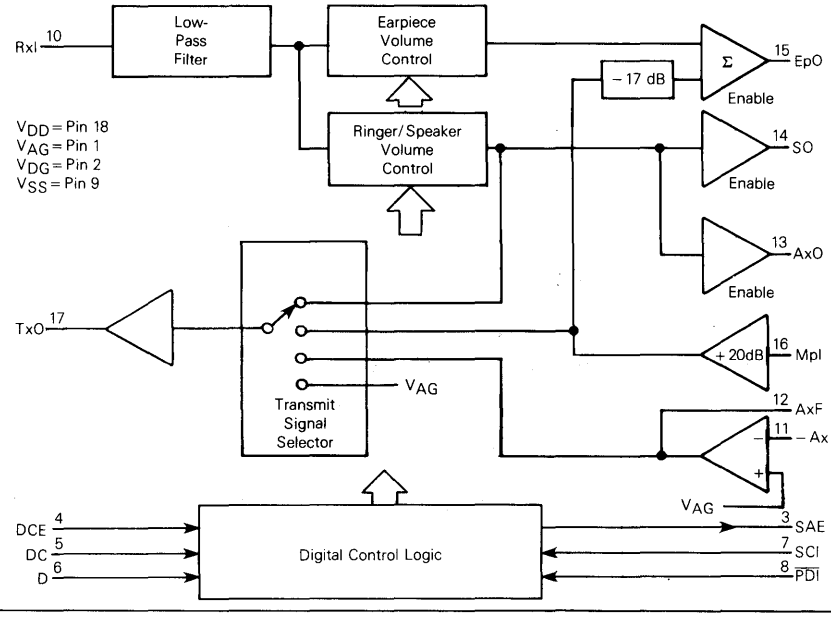


P SUFFIX
PLASTIC PACKAGE
CASE 707



L SUFFIX
CERAMIC PACKAGE
CASE 726

SIMPLIFIED BLOCK DIAGRAM

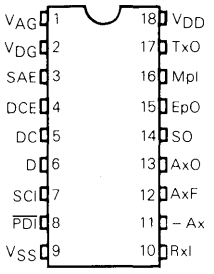


This document contains information on a new product. Specifications and information herein are subject to change without notice.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
DC Supply Voltage	$V_{DD}-V_{SS}$	−0.5 to 13	V
Voltage, Any Pin to V_{SS}	V	−0.5 to V_{DD}+0.5	V
DC Current Drain per Pin (Excluding V_{DD}, V_{SS})	I	10	mA
Operating Temperature Range	T_A	−40 to +85	°C
Storage Temperature Range	T_{stg}	−85 to +150	°C

PIN ASSIGNMENTS



RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
DC Supply Voltage	$V_{DD}-V_{SS}$	6	10 to 12	13	V
DC Supply Voltage Nominally $(V_{DD}-V_{SS})/2$	$V_{DD}-V_{DG}$	3	5 to 7	7.5	V
Power Dissipation	P_D				mW
$V_{DD}-V_{SS}$ = 10 V		–	25	50	
$V_{DD}-V_{SS}$ = 12 V		–	30	60	
Power-Down Dissipation	P_D				mW
$V_{DD}-V_{SS}$ = 12 V		–	3	5	
Full Scale Input Levels					Vpk
$V_{DD}-V_{SS}$ = 10 V RxI, AxF		–	–	3.15	
MpI		–	–	0.315	
$V_{DD}-V_{SS}$ = 12 V RxI, AxF		–	–	3.8	
MpI		–	–	0.38	
Sampling Clock Input Frequency		–	128	–	kHz

TRANSMISSION CHARACTERISTICS

(V_{DD} to V_{SS} = 10 to 12 V ±5%; T_A = 0 to 70°C; 0 dBm0 = 6 dBm ref 600 Ω; +3.17 dBm0 = 3.15 Vp; SCI = 128 kHz)

Characteristic		Min	Max	Unit
Gain				dB
840 Hz @ 0 dBm0, Max Gain Setting	RxI to EpO	−0.3	0.3	
	RxI to SO	−0.3	0.3	
	RxI to AxO	−0.3	0.3	
	RxI to TxO	−0.3	0.3	
	AxF to TxO	−0.3	0.3	
840 Hz @ −20 dBm0	MpI to TxO	19.5	20.5	
	MpI to EpO	2.5	3.5	
Gain vs Volume				dB
Relative to Volume Setting, with 840 Hz @ 0 dBm0 Input				
(−3 to −21 dB)	RxI to EpO	−0.5	0.5	
(−5 to −35 dB)	RxI to SO or AxO	−0.5	0.5	
Idle Noise				
0 to 15 kHz, AxF = −Ax, RxI = MpI = 600 Ω to V_{AG}	TxO, EpO, SO, or AxO	–	−75.0	dBm0
C-Message		–	9.0	dBrnC0
In-Band Spurious Outputs				dBm0
840 Hz @ 0 dBm0, 0.3 to 3.4 kHz, 2nd and 3rd Harmonic		–	−43.0	
Out-Band Spurious Outputs				dBm0
840 Hz @ 0 dBm0, 0 to 20 kHz		–	−40.0	
Gain vs Frequency				dB
Relative to 840 Hz @ 0 dBm0				
(0.3 to 3.0 kHz, All Gain Paths)		−0.25	0.25	
(3.4 kHz, Rx Path)		−1.0	0.25	
(8.0 kHz, Rx Path)		–	−26.0	
Crosstalk				dBm0
840 Hz @ 0 dBm0	Rx to Tx and Tx to Rx	–	−65.0	
Isolation from Any Input to Any Deselected Output				dBm0
Input = 840 Hz @ 0 dBm0		–	−75.0	

ANALOG ELECTRICAL CHARACTERISTICS ($V_{DD} - V_{SS} = 10$ to 12 V ±5%, $T_A = 0$ to 70°C)

Characteristic		Min	Typ	Max	Unit
Input Leakage Current	SCI, D, DC, DCE, RxI, – Ax	–	±10	±30	nA
	V_{AG}, MpI	–	±50	±60	μA
AC Input Impedance	RxI	100	200	–	kΩ
	MpI to V_{AG}	8	10	–	
$\overline{PDI}$ Internal Input Pull Down Resistor Impedance to V_{SS}		50	100	200	kΩ
Output Voltage Range	TxO, EpO, SO, AxO				V
$V_{DD} - V_{SS} = 10$ V, $R_L = 600$ to V_{AG}		–3.2	–	3.2	
$V_{DD} - V_{SS} = 12$ V, $R_L = 900$ to V_{AG}		–3.8	–	3.8	
Output Current	TxO, EpO, SO, AxO				mA
Source		–5.5	–	–	
Sink		5.5	–	–	
Power Supply Rejection Ratio	TxO, EpO, SO, AxO	20	30	–	dB
$V_{AC} = 100$ mVrms, 0 to 20 kHz, V_{DD}, V_{SS}					

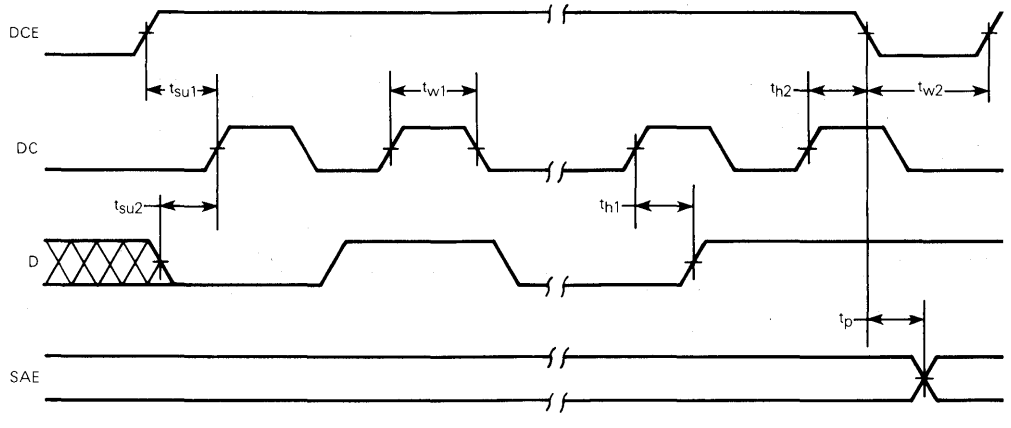
DIGITAL ELECTRICAL CHARACTERISTICS ($T_A = 0$ to 70°C, $V_{DD} = 5.0$ V, $V_{SS} = -5.0$ V, V_{DG}, $V_{AG} = 0$)

Characteristic		Symbol	Min	Max	Unit
Logic Input Voltage ($V_{DG} = 0$ V)	SCI, D, DC, DCE, $\overline{PDI}$				V
V_{SS} to V_{DD} Mode		V_{IL}	–	–3.5	
		V_{IH}	2.0	–	
V_{DG} to V_{DD} Mode		V_{IL}	–	0.8	
		V_{IH}	2.0	–	
V_{SS} to V_{DG} Mode		V_{IL}	–	–3.5	
		V_{IH}	–1.5	–	
Logic Output Voltage ($V_{DG} = 0$ V, $\lvert I_O \rvert < 1$ μA)	SAE	V_{OL}	–	–4.95	V
		V_{OH}	4.95	–	
Output Current ($V_O = -4.5$ V)	SAE	I_{OL}	0.9	–	mA
($V_O = 4.5$ V)		I_{OH}	–0.3	–	

SWITCHING CHARACTERISTICS ($T_A = 0$ to 70°C, $V_{DD} = 5.0$ V, $V_{SS} = -5.0$ V, V_{DG}, $V_{AG} = 0$)

Characteristic		Symbol	Min	Max	Unit
Maximum Frequency	DC (Data Clock)	f_{max}	–	1.0	MHz
Minimum Pulse Width	DC	t_{w1}	0.5	–	μs
Minimum Pulse Width Low (SCI = 128 kHz)	DCE	t_{w2}	33	–	
Propagation Delay (SCI = 128 kHz)	DCE to SAE	t_p	30	60	μs
Setup Times	DCE to DC	t_{su1}	0.5	–	μs
	D to DC	t_{su2}	0.5	–	
Hold Times	D to DC	t_{h1}	0.5	–	μs
	DCE to DC	t_{h2}	0.5	–	

FIGURE 1 — DATA INPUT TIMING



PIN DESCRIPTIONS

V_{DD}, POSITIVE POWER SUPPLY (PIN 18) – Typically +3 to +6.5 volts with V_{AG} = 0 volts.

V_{SS}, NEGATIVE POWER SUPPLY (PIN 9) – Typically −3 to −6.5 with V_{AG} = 0 volts.

V_{AG}, ANALOG GROUND (PIN 1) – Typically 0 volts supplied by a mono-circuit in digital telset applications. All analog signals are referenced to this pin.

V_{DG}, DIGITAL GROUND (PIN 2) – Typically common to logic ground. All internal digital logic operates between V_{DG} and V_{DD}. V_{DG} preferably equals $(V_{DD} - V_{SS})/2$.

SAE, SPEAKER AMPLIFIER ENABLE (PIN 3) – The SAE output will be at V_{DD} whenever the external speaker amplifier is required, otherwise SAE is at V_{SS}.

DCE, DATA CLOCK ENABLE (PIN 4) – This digital input enables the serial data entry circuitry and also latches the serial data into the appropriate data register.

DC, DATA CLOCK (PIN 5) – This digital input allows data on the D pin to be shifted into the serial input data register on rising edges of DC whenever DCE is active.

D, DATA (PIN 6) – Digital data, required to set the configuration or gain of the audio interface, is applied to the D pin and will be shifted into the serial input register by DC whenever DCE is active.

SCI, SAMPLING CLOCK INPUT (PIN 7) – The clock applied to this digital input is used to sample the audio signals. This frequency is nominally 128 kHz and is typically provided by the slave Universal Digital Loop Transceiver such as the MC145426 in digital telset applications. This clock must be applied during data transfers.

$\overline{PDI}$, POWER-DOWN INPUT (PIN 8) – This pin allows all analog circuitry on the device to be powered down while retaining all digital data. An internal pull-down resistor connected to V_{SS} will insure the powered-down state during system power up.

RxI, RECEIVE INPUT (PIN 10) – This pin is the input to the receive low-pass filter and volume controls, and is typically driven from RxO of a mono-circuit in digital telset applications.

−Ax, INVERTING AUXILIARY INPUT (PIN 11), AxF, AUXILIARY FEEDBACK (PIN 12) – These two pins are the inverting input and output, respectively, of the auxiliary input operational amplifier and are used to set the gain of the auxiliary input. The noninverting input of the Ax amp is internally connected to V_{AG}.

AxO, AUXILIARY OUTPUT (PIN 13) – This output drives the input to an external auxiliary circuit and will be at V_{AG} when disabled.

SO, SPEAKER OUTPUT (PIN 14) – This output drives an external speaker amplifier, and when disabled will be at V_{AG}.

EpO, EARPIECE OUTPUT (PIN 15) – This output drives the handset earpiece which may require a series resistor to set the correct signal level. This output will be at V_{AG} when disabled.

MpI, MOUTHPIECE INPUT (PIN 16) – The mouthpiece microphone circuit is connected to this pin.

TxO, TRANSMIT OUTPUT (PIN 17) – This is the audio output pin of the device and is typically used to drive the TxI pin of a mono-circuit in digital telset applications.

DEVICE OPERATION

The telset audio interface IC consists of two major sections: an analog subsystem and a digital subsystem. The digital subsystem provides an interface to a microcomputer and generates the necessary control signals to configure the analog subsystem as desired.

ANALOG SUBSYSTEM

The analog subsystem provides the low-pass filtering, audio-signal routing, gain adjustment, and signal summing required for a digital or analog telset application. This subsystem consists of a receive and a transmit signal path.

RECEIVE SIGNAL PATH

The receive audio signal, typically from the RxO output of a PCM mono-circuit or a speech network, is input to the audio interface via the RxI pin. Once buffered into the device and passed through the low-pass filter, the audio signal has four possible destinations: earpiece output, speaker output, auxiliary output, or loopback to the TxO output.

The audio path to the earpiece output consists of an earpiece volume control and summing output amplifier. The volume control is an eight-step attenuation circuit with −3 dB steps and unity gain at the maximum setting. The steps are selected by a 3-bit binary code with 0_8 and 7_8, the minimum and maximum settings, respectively. The output of the earpiece volume control is summed (0 dB gain) with a sidetone (−17 dB gain) from the mouthpiece input. The earpiece output is capable of driving an earpiece transducer which typically requires 200 mVp-p into 150 ohms. The gain to the earpiece to attain the proper sound pressure level may be adjusted with a resistor in series with the earpiece. When the audio interface is configured such that the earpiece is not selected, the earpiece volume control and the summing output amplifier are powered down.

The audio path to the speaker output consists of a volume control and an output driver. The volume control is an eight-step attenuation circuit with −5 dB steps and unity gain at the maximum setting. The steps are selected by a 3-bit binary code with 0_8 and 7_8, the minimum and maximum settings, respectively. The binary code may be from either of two volume registers: the speaker volume register, selected when the speaker is used for voice, or the ringer volume register, selected when the speaker is used for ringing. The register used is determined by the current configuration of the audio interface. The output of the volume control is fed into a unity gain output buffer which is intended to drive a speaker power amplifier. The speaker/ringer volume control and output buffer power down when not selected.

The auxiliary output is similar to the speaker output and is powered down when not needed. This output can be used to drive a conference phone circuit or the receive portion of a modem.

The three analog outputs, EpO, SO, and AxO, have a transient suppression circuit which eliminates the possibility of acoustic "pops" during configuration or volume changes. This same circuit keeps the output at V_{AG} when it is not selected. When enabled, the output signal slews directly from V_{AG} to the audio signal.

The other possible destination for the receive audio is the TxO audio output. This is an audio loopback configuration

which allows a system to test the operation of the audio path in the telset. In the loopback configuration, the output of the ringer/speaker volume control is switched into the TxO output amplifier input.

TRANSMIT SIGNAL PATH

The transmit portion of the analog subsystem consists of a unity gain output driver which has three possible inputs. The input selection depends upon the current configuration of the audio interface. One of these inputs is used in the loopback configuration discussed above. The auxiliary inputs, AxF and – Ax, allow gain adjustment from an auxiliary circuit, and the third input, Mpl, is from the mouthpiece microphone and is amplified 20 dB by the input amplifier. Two configurations allow use of the auxiliary inputs as a mouthpiece input without sidetone, which is useful in analog telset applications.

DIGITAL SUBSYSTEM

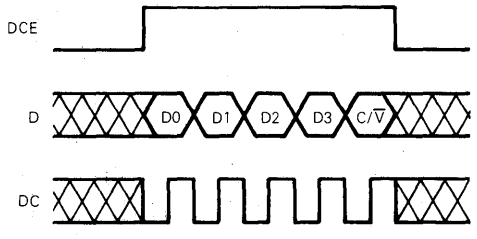
The digital subsystem provides a three-wire serial input which allows a microcomputer to program the audio configuration of the audio interface.

Data is clocked into the audio interface using the DCE, DC, and D pins. DCE going high enables the data input circuitry. While DCE is high, data appearing on the D pin is clocked into the serial input data register on rising edges of DC. The falling edge of DCE latches the serial data into the appropriate register.

The serial data input format consists of five bits as shown in Figure 2.

Configuration/$\overline{\text{Volume}}$ bit (C/$\overline{\text{V}}$), loaded last, indicates the type of data contained in the data field D0-D3. When C/$\overline{\text{V}}$ is a "1", the data indicates the device configuration to be established. When C/$\overline{\text{V}}$ is a "0", the data indicates a volume level. The volume control which receives the data depends upon the current configuration of the audio interface.

FIGURE 2 – DATA FORMAT



When C/$\overline{\text{V}}$ is "1", D0-D3 are loaded into the configuration register. The four configuration register bits then address a ROM which has outputs to control the analog subsystem elements, enable the appropriate volume register, select the appropriate volume register for the speaker/ringer volume control, and provide the SAE output.

When C/$\overline{\text{V}}$ is "0", the data bits D1-D3 are loaded into the volume register which has been selected by the ROM. For volume changes, only D1-C/$\overline{\text{V}}$ need be transferred. However, if five bits are loaded into the serial input data register and C/$\overline{\text{V}}$ is low, D0 will be ignored.

If six or more data bits are clocked in while DCE is high, the last five bits clocked will be accepted when DCE goes low.

The digital input SCI is used by the analog subsystem as a sampling clock for signal processing and by the data input circuitry as a sequencing clock during data transfers.

The $\overline{\text{PDI}}$ input, when low, powers down the analog subsystem; however, all data is retained in the data registers and data may still be loaded into the serial input data register as usual as long as SCI is present. An internal pull-down resistor to V_{SS} is connected to $\overline{\text{PDI}}$ to insure the power-down state upon application to V_{DD} and V_{SS}.

The five digital inputs are DCE, DC, D, SCI and PDI. After one logic transition change, the input logic determines which of the three possible input voltage swings is used, and responds accordingly to future input levels.

There are two input logic circuits per input pin. The first operates from V_{DG} to V_{DD} with TTL levels referenced from V_{DG}. The second circuit uses V_{DG} as the positive supply and V_{SS} as the negative, sensing CMOS input levels from V_{SS} to V_{DG}. The internal logic looks at the output of these two circuits and determines the input logic levels used. This permits logic level swings of V_{SS} to V_{DG}, V_{DG} to V_{DD}, or V_{SS} to V_{DD}.

CONFIGURATION MODES

The audio interface configuration set provides a total of 16 possible configurations. A description of each of the modes follows.

LOOPBACK

This is a system test mode which loops received audio through the ringer/system volume control and out the TxO output amp.

The ring volume register controls the ringer/speaker volume control and new volume data enters the same register.

STANDBY

This mode accomplishes the same result as the $\overline{\text{PDI}}$ pin except for powering down the TxO amplifier. All other amplifiers are powered down and all transmission gates are turned off. Volume data is latched into the ring volume register.

STANDARD A

The standard A mode resembles that of the ordinary telephone. Rxl audio is passed through the earpiece volume control and summed with a sidetone from the mouthpiece before being presented to the earpiece. Tx audio originates at the mouthpiece input, receives 20 dB of gain, and is then passed to the TxO output. New volume data is stored in the earpiece volume register. Transmit mute in this mode disable the path from the mouthpiece amplifier to the TxO amplifier.

RING

This is a receive only mode in which the receive audio is passed through the ringer/speaker volume control and output via the SO output. The ring volume register is selected to properly attenuate the ringing signal in the ringer/speaker volume control and any new volume data is written into the same register. Transmit mute has no effect in this mode and SAE goes high.

ON HOOK DIALING

This mode will allow a user to dial without taking the handset off hook. Audible feedback from the speaker could indicate dial tone, key depressions, etc. Receive audio passes through the ringer/speaker volume control and out the SO output. The transmit signal will originate at the auxiliary input which could be used for a DTMF dialer input. The speaker volume register is applied to the volume control and new volume data is latched into the same register. Mute will disable the transmit path from the auxiliary input. SAE will be high in this mode, enabling the speaker amplifier.

RECEIVER MONITOR A

This mode is similar to the standard A mode except the receive audio is also applied to the speaker output. Receive audio passes through both volume controls and out the EpO and SO pins. The speaker volume register controls the ringer/speaker volume control and new volume data is written into the speaker volume register. Transmit audio is taken from the mouthpiece input and output via the TxO amplifier. Transmit mute disables and mouthpiece amp to TxO amp path. SAE is high, enabling the speaker amplifier.

AUXILIARY

A suggested application for this mode would be for an optional conference phone circuit to be connected to the auxiliary input and output pins. Basically, a conference phone is a voice activated half-duplex controller which allows hands free conversation without audio feedback problems. Another useful application would be to connect a modem to the auxiliary input and output, thus eliminating the requirement for several components. In this mode the receive audio is passed through the ringer/speaker volume control and out the AxO pin. The SAE pin goes high, enabling the speaker amplifier. The transmit audio enters the audio interface via the auxiliary input amplifier and is connected directly to the TxO output amp. The speaker volume register controls the volume control and new volume data enters the same register. Transmit mute disables AxF from the input to the TxO output amp, disables AxO and enables the SO output.

STANDARD B

This mode is identical to the Standard A mode with one exception: the TxO signal originates at the auxiliary input instead of Mpl. This allows use of the Telset Audio Interface in applications that generate sidetone in a speech network. Mute disables the transmit path from the auxiliary input.

RECEIVE MONITOR B

This mode is identical to the Receive Monitor A mode with the same exception as the Standard B mode described above.

MODE AND VOLUME CONTROL

The data patterns required to program the audio interface mode or set the volume levels are summarized in Figures 3 and 4.

FIGURE 3 — MODE CONTROL SUMMARY

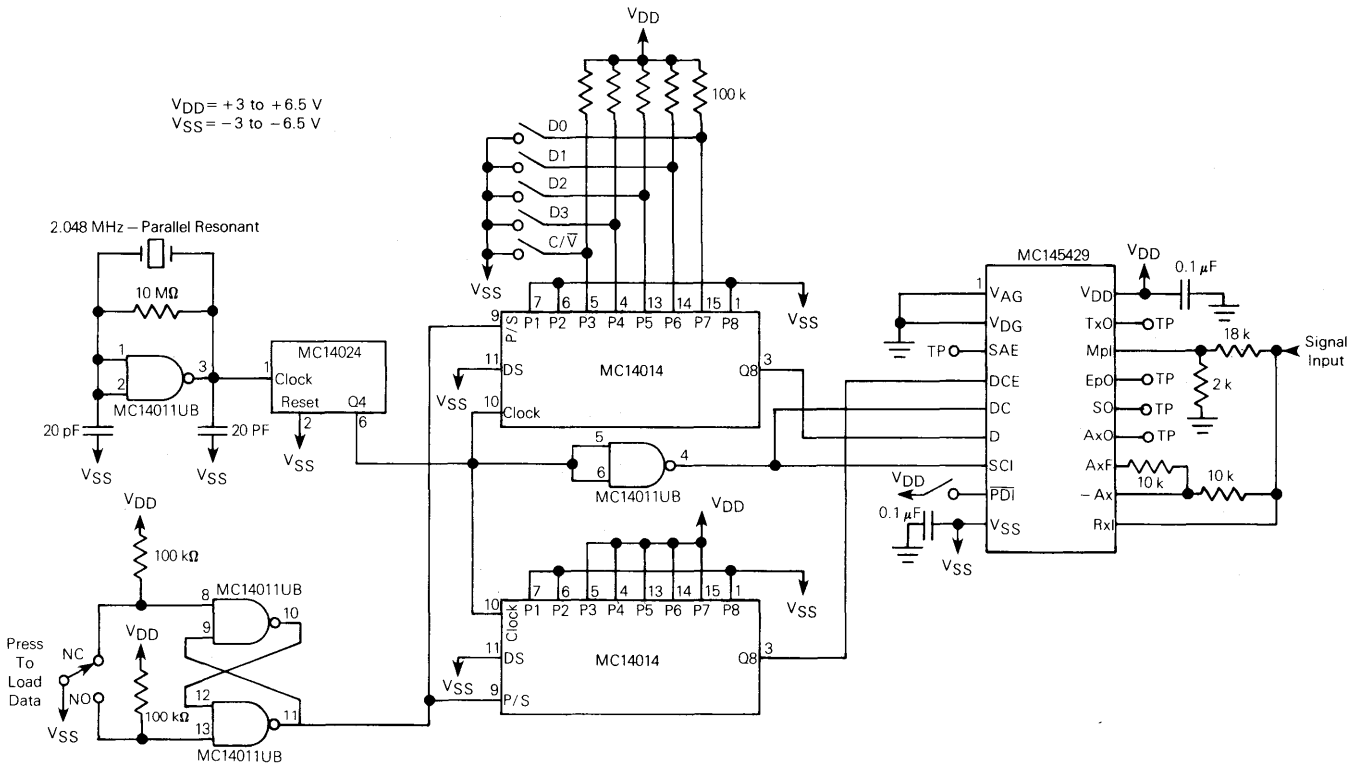
Mode	C/$\overline{V}$	D3	D2	D1	D0	Volume Register Selected	SAE State
Loopback	1	0	0	0	0	Ring	0
Standby	1	0	0	0	1	Ring	0
Standard A	1	0	0	1	0	Earpiece	0
Standard A/Mute	1	0	0	1	1	Earpiece	0
Ring	1	0	1	0	0	Ring	1
Ring/Mute	1	0	1	0	1	Ring	1
On-Hook Dialing	1	0	1	1	0	Speaker	1
On-Hook Dialing/Mute	1	0	1	1	1	Speaker	1
Receive Monitor A	1	1	0	0	0	Speaker	1
Receiver Monitor A/Mute	1	1	0	0	1	Speaker	1
Auxiliary	1	1	0	1	0	Speaker	1
Auxiliary/Mute	1	1	0	1	1	Speaker	1
Standard B	1	1	1	0	0	Earpiece	0
Standard B/Mute	1	1	1	0	1	Earpiece	0
Receive Monitor B	1	1	1	1	0	Speaker	1
Receive Monitor B/Mute	1	1	1	1	1	Speaker	1

FIGURE 4 — VOLUME CONTROL SUMMARY

Attenuation (dB)						
Earpiece	Speaker/ Ringer	C/$\overline{V}$	D3	D2	D1	D0
0	0	0	1	1	1	X
3	5	0	1	1	0	X
6	10	0	1	0	1	X
9	15	0	1	0	0	X
12	20	0	0	1	1	X
15	25	0	0	1	0	X
18	30	0	0	0	1	X
21	35	0	0	0	0	X

X = Don't Care

FIGURE 5 — TEST CIRCUIT



2

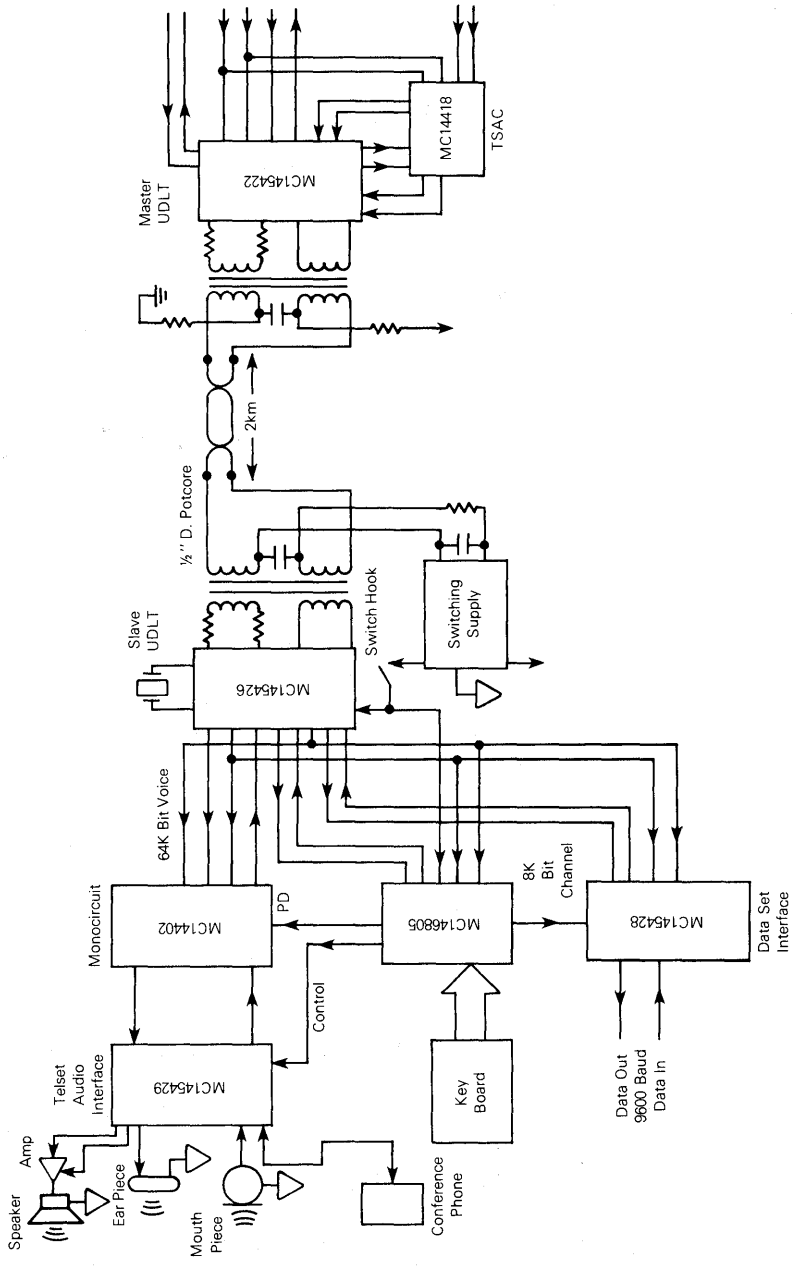


FIGURE 6 — DIGITAL WORK STATION

MOTOROLA

MC145432

Advance Information

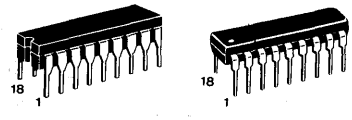
2600 Hz TONE SIGNALLING FILTER

This device contains a bypassable 6 pole 2600 Hz notch filter, a 2600 Hz band-pass filter and a 2600 Hz sinewave generator for SF signalling/detection applications.

- ±5 V to ±8 V Single or Split Supply Operation
- Low Power Consumption, 80 mW @ 10 V
  200 mW @ 15 V
- On-Board Crystal Oscillator or External Clocks
- Notch Filter Gain Adjustable
- Uncommitted Op Amp Capable of Driving 600 Ω Loads
- TTL or CMOS Compatible Inputs
- 18-Pin Package

CMOS
(LOW-POWER COMPLEMENTARY MOS)

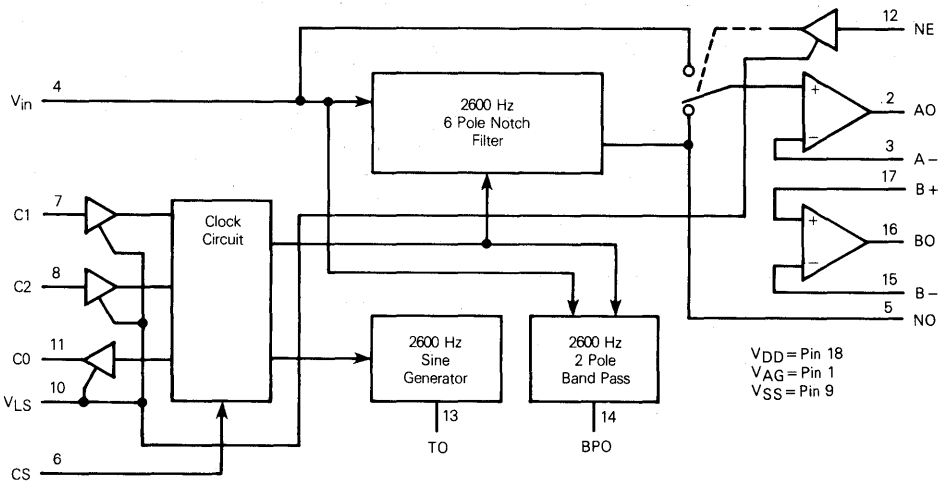
2600 Hz TONE SIGNALLING FILTER



L SUFFIX
CERAMIC PACKAGE
CASE 726

P SUFFIX
PLASTIC PACKAGE
CASE 707

BLOCK DIAGRAM

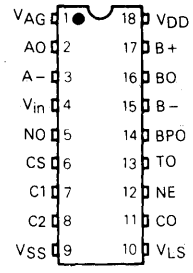


This document contains information on a new product. Specifications and information herein are subject to change without notice.

MAXIMUM RATINGS (V_{SS} = 0 V)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	−0.5 to 18	V
Input Voltage, All Pins	V_{in}	−0.5 to V_{DD} + 0.5	V
DC Current Drain Per Pin (Not V_{DD} or V_{SS})	I	10	mA
Operating Temperature Range	T_A	−40 to 85	°C
Storage Temperature Range	T_{stg}	−65 to 150	°C

PIN ASSIGNMENT



RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
DC Supply Voltage	$V_{DD} - V_{SS}$	9.5	15	16	V

DIGITAL ELECTRICAL CHARACTERISTICS (V_{SS} = 0 V, V_{DD} = 10 V, T_A = −40 to 85°C)

Characteristic		Symbol	Min	Typ	Max	Unit
Operating Current (CMOS Mode) @ 2.048 MHz		I_{DD}	–	8.0	10	mA
(TTL Mode) @ 2.048 MHz			–	12	15	
Input Capacitance		Cin	–	5.0	7.5	pF
MODE CONTROL LOGIC LEVELS						
V_{LS} (TTL Mode)		–	V_{SS}	–	V_{DD} − 4	V
V_{LS} (CMOS Mode)		V_{IH}	V_{DD} − 0.5	–	V_{DD}	V
Clock Select (CS), $V_{AG} = (V_{DD} - V_{SS})/2$	State 1	V_{IH}	V_{DD} − 0.5	–	V_{DD}	V
	State 2	V_{IM}	V_{AG} − 0.5	–	V_{AG} + 0.5	
	State 3	V_{IL}	V_{SS}	–	V_{SS} + 0.5	
TTL LOGIC LEVELS (V_{LS} = 0 V, V_{SS} = 0 V)						
Input Current (C1, C2, CS, NE)	"1" Level	I_{IH}	–	–	±0.3	μA
	"0" Level	I_{IL}	–	–	±0.3	
Input Voltage (C1, C2, CS, NE)	"1" Level	V_{IH}	V_{LS} + 2.0	–	–	V
	"0" Level	V_{IL}	–	–	V_{LS} + 0.8	
Output Voltage (CO) I_O = 8 mA	"1" Level	V_{OH}	2.4	–	–	V
I_O = 2.5 mA	"0" Level	V_{OL}	–	–	0.8	
CMOS LOGIC LEVELS ($V_{LS} = V_{DD}$, V_{SS} = 0 V)						
Input Current (C1, C2, CS, NE)	"1" Level	I_{IH}	–	–	±0.3	μA
	"0" Level	I_{IL}	–	–	±0.3	
Input Voltage (C1, C2, CS, NE)	"1" Level	V_{IH}	7.5	5.6	–	V
	"0" Level	V_{IL}	–	4.4	3.0	
Output Current (CO)	V_{OH} = 9.5 V	I_{OH}	−1.3	−2.25	–	mA
	V_{OL} = 0.5 V	I_{OL}	1.1	2.25	–	

ANALOG ELECTRICAL CHARACTERISTICS (V_{DD} = 10 V, V_{AG} = V_{DD}/2, V_{SS} = 0 V, T_A = 0 to 70°C)

Characteristic		Symbol	Min	Typ	Max	Unit
DC Input Current (V_{AG})		I_I	–	–	±50	μA
DC Input Current (V_{in})		I_I	–	–	±10	μA
AC Input Impedance (1 kHz) (V_{in})		Z_{in}	0.2	0.1	–	MΩ
Input Voltage Range (V_{in})		V_{in}	V_{SS} + 1.5	–	V_{DD} – 1.5	V
Output Drive Current (TO, BPO, NO)	V_{OH} = V_{DD} – 1.2 V V_{OL} = V_{SS} + 1.2 V	I_{OH} I_{OL}	–0.4 +0.9	– –	– –	mA

OP AMP PERFORMANCE (V_{DD} = 10 V, V_{AG} = V_{DD}/2, V_{SS} = 0 V, NE = V_{SS}, V_{LS} = V_{DD}, T_A = 0 to 70°C)

Characteristic		Symbol	Min	Typ	Max	Unit
Input Offset Voltage (AO, BO)		V_{IO}	–50		+50	MV
Open Loop Gain (AO, BO)	Z_L = 600 Ω + 200 pF to V_{AG}	A_{OL}	–	45		dB
Input Bias Current (V_{in}, A–, B–, B+)		I_{IB}	–	±0.1	–	μA
Output Voltage Range (AO, BO) (R_L = 20 kΩ to V_{AG}) (R_L = 900 Ω to V_{AG}) (R_L = 600 Ω to V_{AG})		V_O	 1.0 1.1 1.8	 – – –	 9.0 8.9 8.2	V
Output Current (AO, BO)	V_{OH} = V_{DD} – 1.2 V VOL = V_{SS} + 1.2 V	I_{OH} I_{OL}	–5 +5	– –	– –	mA
Output Noise (AO, BO), 900 Ω		P_N	–	3	–	dBrnc
Slew Rate (AO, BO)		S_R	–	2	–	V/μs

NOTCH FILTER CHARACTERISTICS (V_{DD} = 10 V, V_{AG} = V_{DD}/2, CS = V_{SS} = 0 V, T_A = 0 to 70°C, NE = V_{DD})

Characteristics	Min	Max	Unit
Input Overload Voltage	–	7.0	Vpp
Gain (+2 dBm into 900 Ω @ 1 kHz)	–0.5	+0.5	dB
Idle Noise, V_{in} = V_{AG}, 900 Ω	–	25	dBrnC
Pass-Band Gain, Ref. 1 kHz Note Figure 1 300 Hz to 2 kHz 2 kHz to 2.2 kHz 2.2 kHz to 2.4 kHz 2.8 kHz to 3 kHz 3 kHz to 3.38 kHz 3.38 kHz to 4 kHz	 –0.25 –0.5 –5.0 –5.0 –0.5 –0.5	 +0.25 +0.5 +0.5 +0.5 +0.5 +0.5	dB
Rejection, Ref. 1 kHz 2.58 kHz to 2.59 kHz 2.59 kHz to 2.61 kHz 2.61 kHz to 2.62 kHz	 –45 –55 –45	 – – –	dB
Output Offset	–500	+500	mV

BY-PASS CHARACTERISTICS (V_{in} to AO, NE Low, V_{DD} = 10 V, V_{AG} = V_{DD}/2, CS = V_{SS} = 0, T_A = 0 to 70°C)

Characteristics	Min	Max	Unit
Gain, 400 Hz to 4 kHz	−0.1	+0.1	dB
Noise, V_{in} = V_{AG}, 900 Ω	–	23	dBrnC
Output Offset	−50	+50	mV

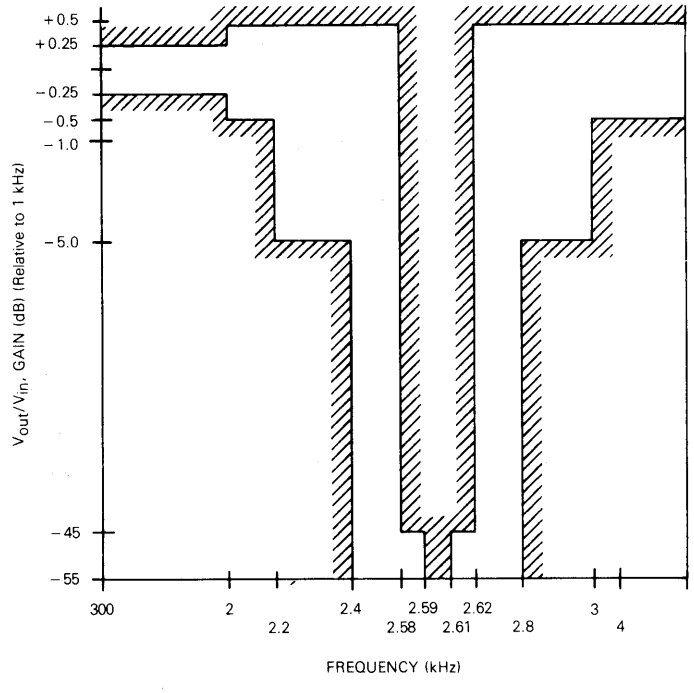
BAND-PASS CHARACTERISTICS (V_{DD} = 10 V, V_{AG} = V_{DD}/2, CS = V_{SS} = 0, T_A = 0 to 70°C)

Characteristics	Min	Max	Unit
Center Frequency, f_o	2590	2610	Hz
Q	20	23	–
Gain (+2 dBm into 900 Ω @ 2.6 kHz)	−0.5	+0.5	dB
Idle Noise, V_{in} = V_{AG}, 900 Ω	–	45	dBrnC
Output Offset	−500	+500	mV

TONE OUT CHARACTERISTICS (V_{DD} = 10 V, V_{AG}/2, CS = V_{SS} = 0, T_A = 0 to 70°C)

Characteristics	Min	Max	Unit
Center Frequency	2598	2602	Hz
Output Level	0.40	0.725	Vp-p
Output Offset	−300	+300	mV

FIGURE 1 — NOTCH RESPONSE PARAMETER



PIN DESCRIPTIONS

V_{DD}, POSITIVE POWER SUPPLY (PIN 18)
Most positive supply.

V_{SS}, NEGATIVE POWER SUPPLY (PIN 9)
Most negative supply.

V_{AG}, ANALOG GROUND (PIN 1)
This pin is a high impedance input which serves as analog ground reference. This pin is nominally held at $(V_{DD}-V_{SS})/2$.

AO, OP-AMP OUT (PIN 2)
A−, OP-AMP IN (PIN 3)
These pins are for the output buffer amp which is capable of driving 600 Ω loads. A− is the inverting input of this amp while AO is its output. This amp buffers either the output of the notch filter or the input signal at V_{in} depending on the state of the NE pin.

V_{in}, INPUT (PIN 4)
This pin is the input to the notch filter, band-pass filter, and notch by-pass switch.

NO, NOTCH OUTPUT (PIN 5)
This pin is the output of the notch filter and can drive 20 kΩ loads.

NE, NOTCH ENABLE (PIN 12)
When high (see V_{LS} pin) the notch filter output is applied to the line buffer output amp. When held low (see V_{LS} pin) the input at V_{in} is applied to this op amp.

TO, TONE OUTPUT (PIN 13)
A 2600 Hz sine wave is output at this pin. This pin can drive a 20 kΩ load.

BPO, BAND-PASS OUT (PIN 14)
This pin is the output of the 2600 Hz band-pass filter and can drive a 20 kΩ load.

B+, OP-AMP NONINVERTING INPUT (PIN 17)
This pin is the noninverting input to the uncommitted op-amp provided on the circuit.

B−, OP-AMP INVERTING INPUT (PIN 15)
This pin is the inverting input of the uncommitted op-amp provided on the circuit.

BO, OP-AMP OUTPUT (PIN 16)
This pin is the inverting input of the uncommitted op-amp provided on the circuit.

CS, CLOCK SELECT (PIN 6)
C1, C2, CLOCK INPUTS (PINS 7 AND 8)
When held at V_{DD}, CS selects the internal crystal oscillator clock mode. A 3.579545 MHz crystal is connected between pins C1 and C2. A 10 MΩ resistor should be tied across C1 and C2 along with 20 pF capacitors to V_{SS} to insure stable oscillator operation. When tied to V_{SS}, a 2.048 MHz external clock should be applied to C2. When tied to V_{AG}, a 1.536 MHz external clock should be applied to C2. In both external clock modes, C1 should be tied to V_{SS}.

V_{LS}, LOGIC SHIFT VOLTAGE (PIN 10)
This pin determines CMOS or TTL level compatibility for C1, C2, NE and CO. If tied to V_{DD}, CMOS device levels are expected; if tied to a voltage less than $V_{DD}-4$ V, TTL levels are expected with V_{LS} equal to logic ground.

CO, CLOCK OUTPUT (PIN 11)
A 128 kHz square wave is available at this pin. This is the sample clock of both the notch and band-pass filters.

FIGURE 2A — FREQUENCY SELECTION TABLE

Clock Select (CS)	Clock Source	Filter Switching Frequency f_s	Notch/Bandpass Center Frenquency f_c	Digital Clock Out (CO)
V_{DD}	Crystal (C1, C2)	Clock (Hz) / 28	Clock (Hz) / 1376	f_s
V_{AG}	External ($C1=V_{SS}$)	Clock (Hz) / 12	Clock (Hz) / 590	f_s
V_{SS}	External ($C1=V_{SS}$	Clock (Hz) / 16	Clock (Hz) / 787.7	f_s

NOTE: Switching Frequency (f_s) Range = 10 kHz to 256 kHz

FIGURE 2B — FREQUENCY SELECTION TABLE

Clock Select (CS)	Clock Source	Filter Switching Frequency	Clock Out (CO)	Tone Out (TO)
V_{DD}	Crystal (C1, C2)	3.579 MHz	127.8 kHz	2601 Hz
V_{AG}	External ($C1=V_{SS}$)	1.536 MHz	128 KHz	2603.4 Hz
V_{SS}	External ($C1=V_{SS}$)	2.048 MHz	128 kHz	2599 Hz

FIGURE 3 – TEST CIRCUIT

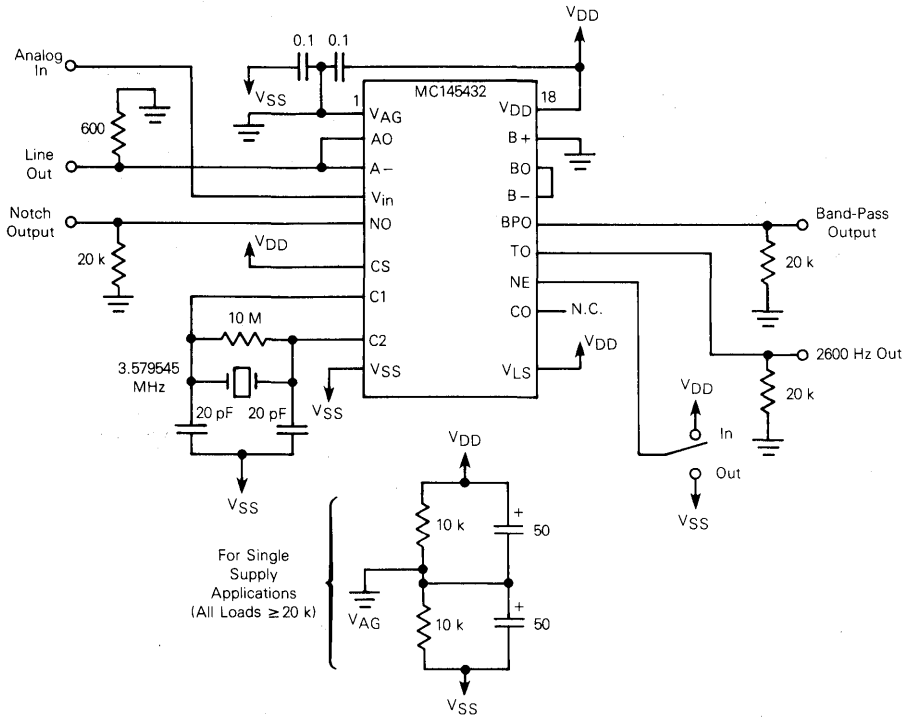
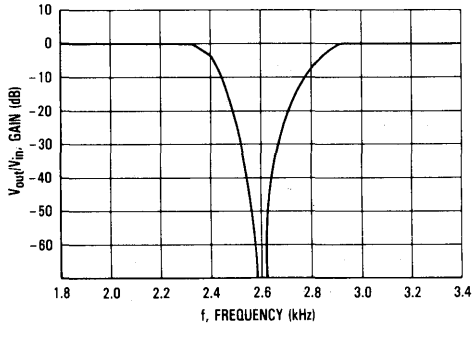
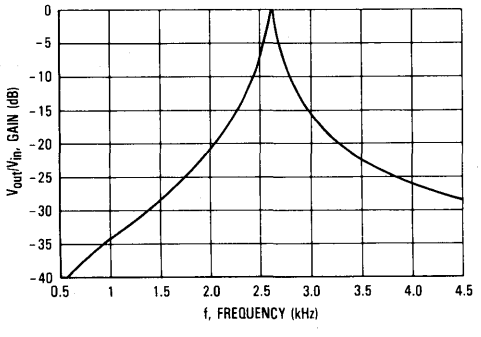


FIGURE 4—TYPICAL RESPONSE CURVES

NOTCH FREQUENCY RESPONSE



BAND-PASS FREQUENCY RESPONSE



MOTOROLA

MC145433

Advance Information

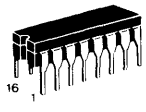
TUNABLE NOTCH/BAND-PASS FILTERS

This device contains a 6-pole filter and 4-pole band-pass filter which are frequency programable.

- ±5 to ±8 V Supply Operation
- Low Power Consumption, 150 mW Typical
- Tuneable Notch and Band-pass Filters
- On-board Crystal Oscillator or External Clocks
- Clock Output Pin
- An Uncommitted Op-Amp Is Provided, Capable of Driving 600 Ω Loads
- Notch Filter Output Gain Adjustable
- TTL or CMOS Compatible Inputs
- 16-Pin Package

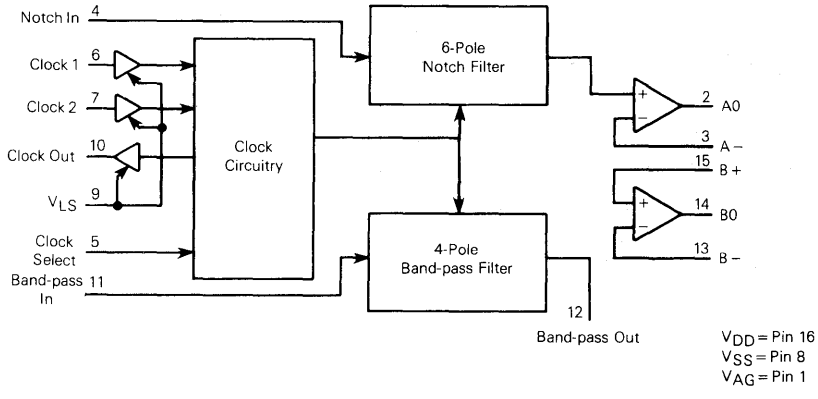
CMOS
(LOW-POWER COMPLEMENTARY MOS)

TUNEABLE NOTCH/ BAND-PASS FILTER



L SUFFIX
CERAMIC PACKAGE
CASE 620

BLOCK DIAGRAM



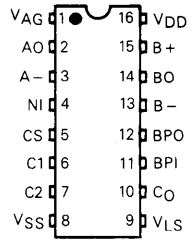
This document contains information on a new product. Specifications and information herein are subject to change without notice.

2

MAXIMUM RATINGS (V_{SS} = 0 V)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	−0.5 to 18	V
Input Voltage, All Pins	V_{in}	−0.5 to V_{DD} + 0.5	V
DC Current Drain Per Pin (Not V_{DD} or V_{SS})	I	10	mA
Operating Temperature Range	T_A	−40 to 85	°C
Storage Temperature Range	T_{stg}	−65 to 150	°C

PIN ASSIGNMENT



RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
DC Supply Voltage	$V_{DD} - V_{SS}$	9.5	15	16	V

DIGITAL ELECTRICAL CHARACTERISTICS (V_{SS} = 0 V, V_{DD} = 10 V, T_A = −40 to 85°C)

Characteristic		Symbol	Min	Typ	Max	Unit
Operating Current (CMOS Mode) @ 2.048 MHz		I_{DD}	−	10	18	mA
(TTL Mode) @ 2.048 MHz			−	15	22	
Input Capacitance		Cin	−	5.0	7.5	pF
MODE CONTROL LOGIC LEVELS						
V_{LS} (TTL Mode)		−	V_{SS}	−	V_{DD} − 4	V
V_{LS} (CMOS Mode)		V_{IH}	V_{DD} − 0.5	−	V_{DD}	V
Clock Select (CS), $V_{AG} = (V_{DD} - V_{SS})/2$	State 1	V_{IH}	V_{DD} − 0.5	−	V_{DD}	V
	State 2	V_{IM}	V_{AG} − 0.5	−	V_{AG} + 0.5	
	State 3	V_{IL}	V_{SS}	−	V_{SS} + 0.5	
TTL LOGIC LEVELS (V_{LS} = 0 V, V_{SS} = 0 V)						
Input Current (C1, C2, CS)	"1" Level	I_{IH}	−	−	±0.3	μA
	"0" Level	I_{IL}	−	−	±0.3	
Input Voltage (C1, C2, CS)	"1" Level	V_{IH}	V_{LS} + 2.0	−	−	V
	"0" Level	V_{IL}	−	−	V_{LS} + 0.8	
Output Voltage (CO) I_O = 8 mA	"1" Level	V_{OH}	2.4	−	−	V
I_O = 2.5 mA	"0" Level	V_{OL}	−	−	0.8	
CMOS LOGIC LEVELS ($V_{LS} = V_{DD}$, V_{SS} = 0 V)						
Input Current (C1, C2, CS)	"1" Level	I_{IH}	−	−	±0.3	μA
	"0" Level	I_{IL}	−	−	±0.3	
Input Voltage (C1, C2, CS)	"1" Level	V_{IH}	7.5	5.6	−	V
	"0" Level	V_{IL}	−	4.4	3.0	
Output Current (CO)	V_{OH} = 9.5 V	I_{OH}	−1.3	−2.25	−	mA
	V_{OL} = 0.5 V	I_{OL}	1.1	2.25	−	

ANALOG ELECTRICAL CHARACTERISTICS (V_{DD} = 10 V, V_{AG} = V_{DD}/2, V_{SS} = 0 V, T_A = 0 to 85°C)

Characteristic		Symbol	Min	Typ	Max	Unit
DC Input Current (V_{AG})		I_I	–	–	±75	μA
DC Input Current (NI and BPI)		I_I	–	–	±10	μA
AC Input Impedance (1 kHz) (NI and BPI)		Z_{in}	0.2	0.1	–	MΩ
Input Voltage Range (NI and BPI)		V_{in}	V_{SS} + 1.5	–	V_{DD} – 1.5	V
Output Drive Current (BPO)	V_{OH} = V_{DD} – 1.2 V V_{OL} = V_{SS} + 1.2 V	I_{OH} I_{OL}	–0.4 +0.9	– –	– –	mA

OP AMP PERFORMANCE (V_{DD} = 10 V, V_{AG} = V_{DD}/2, V_{SS} = 0 V, V_{LS} = V_{DD}, T_A = 0 to 85°C)

Characteristic		Symbol	Min	Typ	Max	Unit
Input Offset Voltage (BO)		V_{IO}	–50	–	+50	MV
Open Loop Gain (BO)	Z_L = 600 Ω + 200 pF to V_{AG}	A_{OL}	–	45	–	dB
Input Bias Current (A–, B–, B+)		I_{IB}	–	±0.1	–	μA
Output Voltage Range (BO) (R_L = 20 kΩ to V_{AG}) (R_L = 900 Ω to V_{AG}) (R_L = 600 Ω to V_{AG})		V_O	 1.0 1.1 1.8	 – – –	 9.0 8.9 8.2	V
Output Current (BO)	V_{OH} = V_{DD} – 1.2 V V_{OL} = V_{SS} + 1.2 V	I_{OH} I_{OL}	–5 +5	– –	– –	mA
Output Noise (BO), 900 Ω		P_N	–	–3	–	dBrnC
Slew Rate (BO)		S_R	–	2	–	V/μs

NOTCH FILTER CHARACTERISTICS (V_{DD} = 10 V, V_{AG} = V_{DD}/2, CS = V_{SS} = 0 V, T_A = 0 to 85°C, BPI = V_{AG})

Characteristics	Min	Max	Unit
Input Overload Voltage	–	7.0	Vpp
Gain (+2 dBm into 900 Ω @ 1 kHz)	–1.0	+1.0	dB
Idle Noise, NI = V_{AG}, R_L = 900 Ω	–	28	dBrnC
Pass-Band Gain, Ref. 1 kHz (Note Figure 1) 300 Hz to 2.2 kHz 2.2 kHz to 2.4 kHz 2.8 kHz to 3 kHz 3 kHz to 4 kHz	 –1.0 –7.0 –7.0 –1.0	 +1.0 +1.0 +1.0 +1.0	dB
Rejection, Ref. 1 kHz 2.58 kHz to 2.62 kHz	 –45	 –	dB
Output Offset	–750	+750	mV
Dynamic Range (VFS/Idle Noise)	–70	–	dB

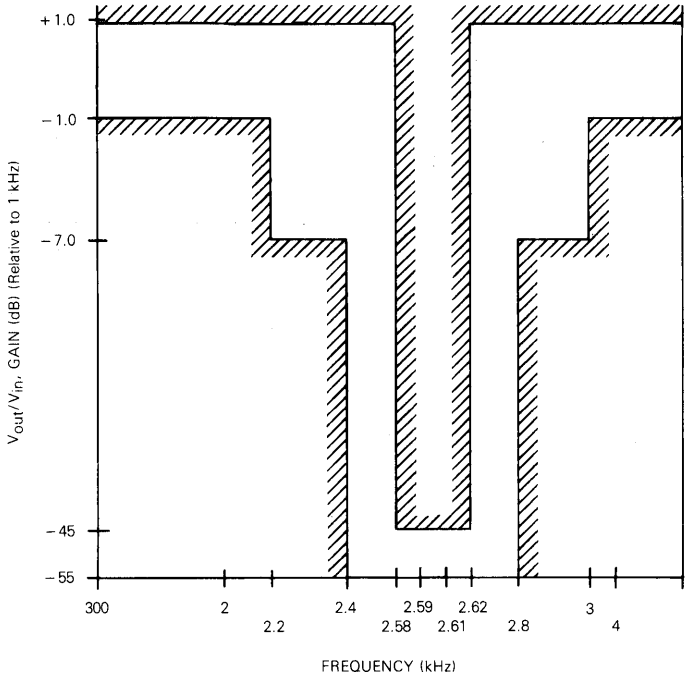
BAND—PASS FILTER ELECTRICAL CHARACTERISTICS (V_{DD} = 10 V, NI = V_{AG}, V_{AG} = V_{DD}/2, V_{SS} = 0 V, T_A = 0 to 85°C)

Characteristic*	Symbol	Min	Typ	Max	Unit
Full Scale Input Voltage (+3 dbm0)	V_{FS}	7	–	–	V_{PP}
Gain (+2 dBm into 900 Ω @ 2.6 kHz	A_r	−1	0.0	+1	dB
Idle Noise, BPI = V_{AG}, R_L = 900 Ω	P_N	–	–	35	dBrnC
Dynamic Range (V_{FS}/Idle Noise)	DR	63	–	–	dB
Total Harmonic Distortion (0 dbm into 900 Ω)	THD	–	–	1.0	%
Output offset		−500	–	+500	mV
Q (−3db bandwidth/center frequency)	Q	28	–	38	–

DIGITAL SWITCHING CHARACTERISTICS (V_{DD} = 10 V, V_{SS} = 0, V_{AG} = V_{DD}/2 T_A = 0 to 85°C)

Characteristic		Symbol	Min	Typ	Max	Unit
Input Rise and Fall Times	C1, C2	t_r, t_f	–	–	1.5	μs
Input Pulse Width (TTL Mode)	C1, C2	t_W	200	–	–	ns
Clock Frequency (TTL Mode)	C1, C2	f_C	–	–	2.048	MHz
Clock Frequency (CMOS Mode)	C1, C2	f_C	–	–	6	MHz
Crystal Frequency	C1, C2	f_x	1	–	6	MHz
Input Pulse Width (CMOS Mode)	C1, C2	t_W	125	–	–	ns
Switching Frequency (Internal)		f_s	10	–	256	kHz

NOTCH RESPONSE PARAMETER



PIN DESCRIPTIONS

V_{DD} (PIN 16)
Most positive supply, nominally +12 V to +15 V.

V_{SS} (PIN 8)
Most negative supply, nominally 0 V.

V_{AG} (PIN 1)
Analog ground. This pin is a high impedance input which serves as analog ground reference. This pin is nominally held at $(V_{DD} - V_{SS})/2$.

CS, CLOCK SELECT (PIN 5)
This pin controls the configuration of the digital section of the circuit. Three different clock divide configurations can be obtained by tying this pin to either V_{DD}, V_{AG} or V_{SS}.

V_{LS}, LOGIC SHIFT VOLTAGE (PIN 9)
This determines the logic levels expected at the digital input C1 and C2. If tied to V_{DD}, CMOS logic levels are expected; if tied to a voltage less than $V_{DD} - 4$ V, TTL levels are expected with V_{LS} equal to logic ground. This pin also controls the output swing at pin CO in a similar manner, i.e., TTL or CMOS levels.

CO, CLOCK OUT (PIN 10)
This pin is the digital clock output pin. It is equal to the switching frequency, f_s of the notch and band-pass filters.

C1, C2, CLOCK 1, CLOCK 2 (PINS 6 AND 7)
When CS is tied to V_{DD}, a 1 to 4 MHz crystal is tied to C1 and C2. The switching frequency, f_s, of both filters is determined by the crystal frequency and is given by:

$$\frac{f\ \text{crystal}}{28} = f_s$$

With CS tied to V_{AG}, an external clock frequency must be applied into C1 and C2 tied together. The switching frequency f_s for the notch and band-pass filters are equal to the external clock frequency divided by 16. When CS is tied to V_{SS}, operation is identical to that when tied to V_{AG}, except that the clock is divided by 1 instead of 16.

NI, NOTCH INPUT (PIN 4)
This pin is the analog input to the notch filter.

AO, OP-AMP OUT (PIN 2), A−, OP-AMP INOUT (PIN 3)
These pins are for the output buffer amp of the notch filter. A− is the inverting input of this amp while AO is its output. This op-amp is capable of driving a 600 ohm load.

B+, OP-AMP NONINVERTING INPUT (PIN 15)
This pin is the non inverting input to the uncommitted op-amp provided on chip.

B−, OP-AMP INVERTING INPUT (PIN 13)
This pin is the inverting input to the uncommitted op-amp.

BO, OP-AMP OUTPUT (PIN 14)
This pin is the output of this uncommitted op-amp. This op-amp is capable of driving a 600 ohm load.

BPI, BAND-PASS IN (PIN 11)
This is the input to the band-pass filter.

BPO, BAND-PASS OUT (PIN 12)
This is the output of the band-pass filter.

FUNCTIONAL TRUTH TABLE

Clock Select CS	Clock	Filter Switching Frequency f_s	Notch/Bandpass Center Frequency f_c	Digital Clock Out CO
V_{DD}	Crystal	$\frac{\text{Clock (Hz)}}{28}$	$\frac{\text{Clock (Hz)}}{137.844}$	f_s
V_{AG}	External	$\frac{\text{Clock (Hz)}}{16}$	$\frac{\text{Clock (Hz)}}{787.69}$	f_s of Notch
V_{SS}	External	Clock (Hz)	$\frac{\text{Clock (Hz)}}{49.23}$	f_s of Notch

NOTE: Switching Frequency (f_s) Range = 10 kHz to 256 kHz

FIGURE 1 — TEST CIRCUIT

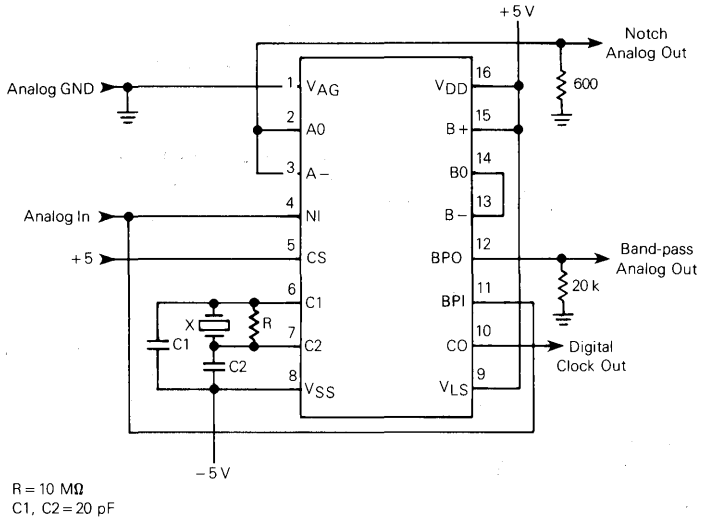


FIGURE 2 — TYPICAL NOTCH FILTER RESPONSE CURVES

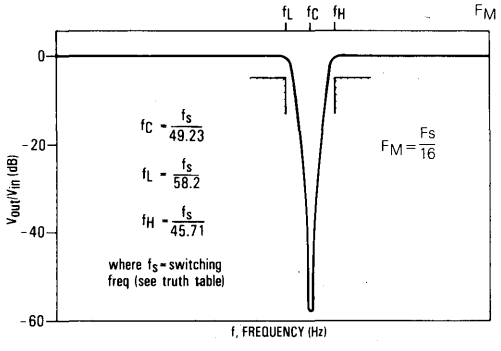
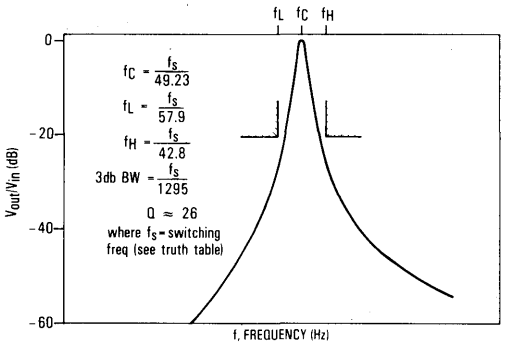


FIGURE 3 — TYPICAL BAND-PASS FILTER RESPONSE CURVES



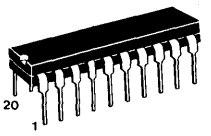
MC145439

MOTOROLA

Product Preview

NRZ to AMI, HDB3, B6ZS, B8ZS AMI, HDB3, B6Z6, B8ZS to NRZ

Encoder/Decoder (Transcoder) for Transmission Applications



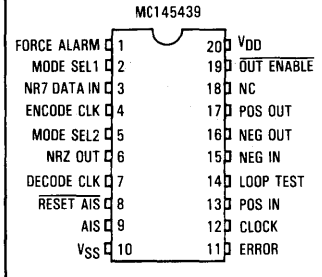
P SUFFIX
PLASTIC
CASE 738

2

The MC145439 is a high speed CMOS integrated circuit designed to perform the coding translation of clocked serial data into two streams of RZ (return to zero) digital pulses, which are externally mixed to form either AMI, HDB3, B6ZS, or B8ZS ternary signals for driving transmission lines. The MC145439 performs the reverse operation by translating two streams of clocked pulses (which have been derived from an incoming AMI, HDB3, B6ZS, or B8ZS ternary encoded signal) into a single stream of clocked binary data. The MC145439 also features loopback and error monitoring functions. The MC145439 performs the coding and decoding functions independently at clock rates from zero(dc) to 10 Mbps. The HDB3 coding and decoding are performed in a manner consistent with the CCITT G703 recommendations.

- NRZ to AMI, HDB3, B6ZS, B8ZS Encoding and Decoding
- Low Power of CMOS Operation
- Single 5 Volt Power Supply Operation
- Error Monitor Functions Provided
- Loopback Feature Provided
- Encode and Decode Clock Rates to 10 Mbps
- Pin Selectable Modes of Operation
- Force Alarm and Output Enable Function
- Pin Compatible with HC-5560

PIN ASSIGNMENT



MOTOROLA

MC145440

2

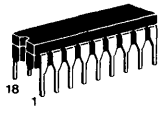
BELL 103 300 BAUD MODEM BAND-PASS FILTER

The MC145440 is a 300 baud modem filter designed to be used with the MC14412, MC145445, or MC6860 modems. These modem/filter combinations fulfill the major requirements of a complete Bell 103 300 baud modem system. The MC145441 is also available to fulfill the CCITT V.21 equivalent filtering function. Features of the MC145440 include:

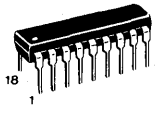
- Low Band Band-pass Filter
- High Band Band-pass Filter
- Bell 103 Frequency Compatible
- Spare Operational Amplifier
- Answer or Originate Mode
- Self Test Loopback Configuration
- Single or Split Power Supply Operation
- 18-Pin Package

CMOS
(LOW-POWER COMPLEMENTARY MOS)

300 BAUD MODEM BAND-PASS SWITCHED CAPACITOR FILTER

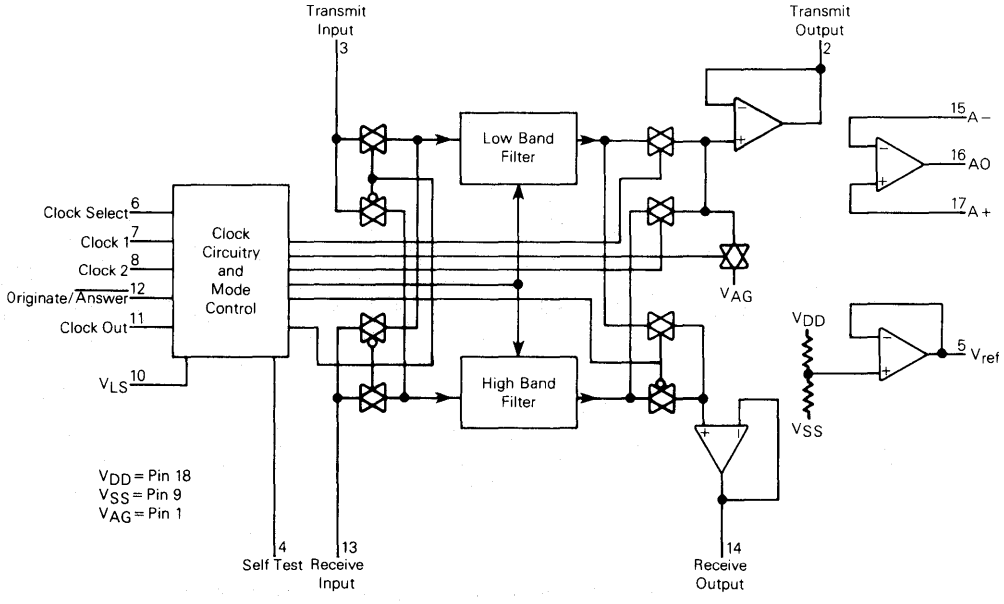


L SUFFIX
CERAMIC PACKAGE
CASE 726



P SUFFIX
PLASTIC PACKAGE
CASE 707

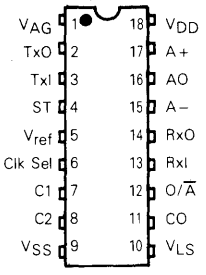
BLOCK DIAGRAM



MAXIMUM RATINGS (V_{SS} = 0 V)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	−0.5 to 18	V
Input Voltage, all pins	V_{in}	−0.5 to V_{DD}+0.5	V
DC Current Drain per pin (Not V_{DD} or V_{SS})	I	10	mA
Operating Temperature Range	T_A	−40 to 85	°C
Storage Temperature Range	T_{stg}	−65 to 150	°C

PIN ASSIGNMENT



RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
DC Supply Voltage	V_{DD}-V_{SS}	4.5	10	16	V

DIGITAL ELECTRICAL CHARACTERISTICS (T_A = −40 to 85°C)

Characteristic		Symbol	Min	Typ	Max	Unit
Operating Current, V_{DD} = 10 V, V_{SS} = 0 V, 1 MHz Crystal		I_{DD}	–	–	10	mA
Input Capacitance		C_{in}	–	5.0	7.5	pF
Mode Control Logic Levels						
V_{LS}	TTL Mode	–	V_{SS}	–	V_{DD}−4.0	V
	CMOS Mode	V_{IH}	V_{DD}−0.5	–	V_{DD}	
Clock Select (CS)	State 1, 4.0 MHz	V_{IH}	V_{DD}−0.5	–	V_{DD}	V
	State 2, 3.684 MHz	V_{IM}	(V_{DD}−V_{SS})/2−0.5	–	(V_{DD}−V_{SS})/2+0.5	
	State 3, 1.0 MHz	V_{IL}	V_{SS}	–	V_{SS}+0.5	
O/Ā TTL Logic Levels (V_{DD} = 5 V, V_{SS} = −5 V, V_{LS} = 0 V)						
Input Current	"1" level	I_{IH}	–	–	+0.3	μA
	"0" Level	I_{IL}	−0.3	–	–	
Input Voltage	"1" level	V_{IH}	V_{LS}+2.0	–	–	V
	"0" level	V_{IL}	–	–	V_{LS}+0.8	
ST, C1, O/Ā CMOS Logic Levels (V_{LS} = V_{DD}, V_{SS} = 0 V)						
Input Current	"1" level	I_{IH}	–	–	+0.3	μA
	"0" level	I_{IL}	−0.3	–	–	
Input Voltage	"1" level, V_{DD} = 10 V	V_{IH}	7.5	5.75	–	V
	"0" level, V_{DD} = 10 V	V_{IL}	–	4.25	3.0	
CO Output Characteristics (V_{DD} = 10, V_{SS} = 0 V)						
TTL Output Voltage (TTL Mode)	"1" level, I_O = 8 mA	V_{OH}	2.4	–	–	V
	"0" level, I_O = 2.5 mA	V_{OL}	–	–	0.8	
CMOS Output Current	V_{DD} = 10 V, V_{OH} = 9.5 V	I_{OH}	−1.3	−2.25	–	mA
	V_{DD} = 10 V, V_{OL} = 0.5 V	I_{OL}	1.1	2.25	–	

ANALOG ELECTRICAL CHARACTERISTICS (V_{DD} = 10 V, V_{AG} = 5 V, V_{SS} = 0 V, T_A = 0 to 70°C)

Characteristic	Symbol	Min	Typ	Max	Unit
DC Input Current (V_{AG})	I_I	−50	–	+50	μA
DC Input Current (TxI, RxI)	I_I	−10	–	+10	μA
AC Input Impedance (TxI, RxI)	Z_{in}	0.2	1.0	–	MΩ
Input Voltage Range (TxI, RxI)	V_{in}	V_{SS}+1.5	–	V_{DD}−1.5	V

OP-AMP CHARACTERISTICS (V_{DD} = 5 to 10 V, V_{AG} = V_{DD}/2, V_{SS} = 0 V, T_A = 0 to 70°C)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Offset Voltage (AO)	I_{IO}	−50	–	+50	mV
Open Loop Gain (R_L = 10 kΩ)	A_{OL}	–	45	–	dB
Input Bias Current (A+, A−)	I_{IB}	–	±0.1	–	μA
Output Noise (900 Ω)	P_N	–	−3	–	dBrnC
Slew Rate	S_R	–	2	–	V/μs
Output Voltage Swing (R_L = 600 Ω to V_{AG})	–	1.5 V	–	V_{DD}−1.5 V	V

DIGITAL SWITCHING CHARACTERISTICS (V_{DD} = 5 V, V_{SS} = 0 V, T_A = 25°C)

Characteristic		Symbol	Min	Typ	Max	Unit
Input Rise and Fall Times	C1, O/A, ST	t_r, t_f	–	–	4	μs
Input Pulse Width	(TTL Mode) O/A	t_w	200	–	–	ns
	(CMOS Mode) C1, O/A, ST	t_w	125	–	–	
Clock Frequency (Driven by External Clock) (C1 Pin)	(CMOS)	f_c	–	1.0	4.0	MHz
Crystal Frequency	C1, C2	f_x	1.0	–	4.0	MHz

2

LOW-BAND FILTER CHARACTERISTICS (V_{DD} = 10 V, V_{AG} = V_{DD}/2, V_{SS} = 0 V, T_A = 0 to 70°C)

Characteristic		Symbol	Min	Typ	Max	Unit
Full Scale Input Voltage (+3 dBmO)		V_{FS}	2.13	–	–	V_{P-P}
Gain at 1170 Hz, 0 dBmO		A_r	9.0	10.0	11.0	dB
Idle Noise, Input = V_{AG}, 900 Ω load		P_N	–	20	26	dBrnC
Dynamic Range (Full Scale Output/Idle Noise)		DR	72	78	–	dB
Total Harmonic Distortion		THD	–	1.0	–	%
Pass-Band Ripple	1070 Hz to 1270 Hz	–	–	–	2	dBp-p
Pass-band Response, Ref. 1070 Hz, 0 dBmO	1270 Hz	–	−1.5	–	1.5	dB
Rejection (Ref. 1170 Hz)	2025 Hz to 2225 Hz	–	−55	–	–	dB
Differential Group Delay	1070 Hz to 1270 Hz	–	–	–	600	μs

HIGH-BAND FILTER CHARACTERISTICS (V_{DD} = 10 V, V_{AG} = V_{DD}/2, V_{SS} = 0 V, T_A = 0 to 70°C)

Characteristic		Symbol	Min	Typ	Max	Unit
Full Scale Input Voltage (+3 dBmO)		V_{FS}	2.13	–	–	V_{P-P}
Gain at 2125 Hz, 0 dBmO		A_r	9.0	10.0	11.0	dB
Idle Noise, Input = V_{AG}, 900 Ω load		P_N	–	20	26	dBrnC
Dynamic Range (Full Scale Output/Idle Noise)		DR	72	78	–	dB
Total Harmonic Distortion		THD	–	1.0	–	%
Pass-Band Ripple	2025 Hz to 2225 Hz	–	–	–	2	dBp-p
Pass-band Response, Ref. 2025 Hz, 0 dBmO	2225 Hz	–	−1.5	–	1.5	dB
Rejection (Ref. 2125 Hz)	1070 Hz to 1270 Hz	–	−55	–	–	dB
Differential Group Delay	2025 Hz to 2225 Hz	–	–	–	600	μs

V_{ref} CHARACTERISTICS (V_{DD} = 5 to 15 V, V_{ref} = V_{DD}/2, V_{SS} = 0 V, T_A = 0 to 70°C)

Characteristic		Symbol	Min	Typ	Max	Unit
V_{ref} Output Voltage	I_O = ±5 mA	V_{ref}	−250	±75	+250	mV

PIN DESCRIPTIONS

V_{DD} (PIN 18) – Positive power supply.

V_{SS} (PIN 9) – Negative power supply.

V_{AG} (PIN 1) – Analog ground. In single supply applications, V_{AG} is driven from V_{ref}.

V_{ref} (PIN 5) – This pin provides an output DC voltage at approximately (V_{DD}-V_{SS})/2 for use as an external analog ground in single supply applications. In symmetric dual power supply applications, V_{ref} is not used.

V_{LS}, LOGIC SHIFT VOLTAGE (PIN 10) – This pin determines the input/output logic level compatibility of O/$\overline{A}$ and CO. When the voltage on this pin is greater than $V_{DD}-0.5$ V and less than V_{DD}, these digital inputs and outputs are CMOS compatible. When the voltage on this pin is less than $V_{DD}-4$ V and greater than V_{SS}, these digital inputs and outputs are TTL compatible, and V_{LS} is connected to digital ground.

C1, C2, CLOCK 1, CLOCK 2 (PIN 7, PIN 8) – These pins connect to an internal crystal oscillator. In operation, a parallel resonant crystal is connected from C1 to C2 as well as a 10 MΩ resistor in parallel with the crystal and 20 pF capacitors from C1 and C2 to V_{SS}. Crystal frequencies of 1.0, 3.6864, or 4.0 MHz may be used. Alternatively, an external CMOS level signal at the crystal frequency may be applied to C1 in lieu of the crystal, capacitors, and resistor. The inverted clock signal will appear at C2 and will be a CMOS output from V_{SS} to V_{DD}.

Clk Sel, CLOCK SELECT (PIN 6) – This pin is a three-state selector used to select one of the three crystal/clock options. When at V_{DD}, V_{AG}, or V_{SS}, this pin selects the 4.0, 3.6864, or 1.0 MHz crystal/clock option, respectively, for C1 and C2.

Clock Select Pin 6	Clock Frequency *	Clock Output Pin 11
V_{DD}	4.0 MHz	1.0 MHz
V_{AG}	3.6864 MHz	N/A
V_{SS}	1.0 MHz	1.0 MHz

*Use either an external clock to drive C1 Pin 7 or external crystal across C1 and C2 Pins 7 and 8.

CO, CLOCK OUT (PIN 11) – This provides a 1.0 MHz output clock signal when either the 1.0 or 4.0 MHz clock is selected and is typically used to drive the clock input to a MC14412 or MC6860 modem. The clock output is not usable when the 3.6864 MHz option is used. The logic family compatibility (CMOS or TTL) of this output is determined by V_{LS}.

O/$\overline{A}$, ORIGINATE, ANSWER (PIN 12) – The mode of the device, originate or answer, is selected with this pin. In the originate mode, selected with a logic "1", the low band band-pass filter is switched into the transmit path and the high band band-pass filter is switched into the receive path. In the answer mode, the filters switch position. The input levels of this pin are determined by V_{LS}.

TxI, TRANSMIT INPUT (PIN 3) – TxI is the input to the transmit band-pass filter which is the low band filter in the originate mode and the high band filter in the answer mode. In the self test mode, this input is routed to the appropriate band-pass filter input so as to pass the modulated data to the demodulator.

TxO, TRANSMIT OUTPUT (PIN 2) – This pin is the output of the Tx output amplifier and typically drives the modulated data into the duplexer or hybrid circuit (see ST pin).

RxI, RECEIVE INPUT (PIN 13) – RxI is the input to the receive band-pass filter which is the high band filter in the originate mode and the low band filter in the answer mode. In the self test mode, this input is disabled.

RxO, RECEIVE OUTPUT (PIN 14) – The output of the receive band-pass filter, whether low band or high band, is provided at RxO. Typically, this signal is capacitively coupled to the input of the external carrier detector and limiter. The AC coupling capacitor is required because of the variable DC offset of the receive filter.

ST, SELF TEST (PIN 4) – A "1" on ST puts the device into a self test mode which routes the modulated carrier from TxI, through the appropriate filter,and out RxO back to the receive carrier input of the modem. TxO remains at V_{AG} during a self test operation. This pin is a standard CMOS input regardless of the state of V_{LS}.

A+ (PIN 17) – This is the noninverting input to the spare operational amplifier.

A– (PIN 15) – This is the inverting input to the spare operational amplifier.

AO (PIN 16) – This is the output of the spare operational amplifier.

FUNCTIONAL DESCRIPTION

This device is capable of four basic analog configurations determined by the state of O/$\overline{A}$ and ST. The normal (non-self test) and self test modes in both the answer and originate modes will be discussed.

In the normal originate mode, O/$\overline{A}$ is a "1" and self test, ST, is a "0". When in this mode, the Tx carrier from the modem is input on TxI and routed through the low band band-pass filter. The filter output is switched to the input of the Tx op-amp which typically drives the Tx carrier off chip into a duplexer circuit which could be implemented with the spare operational amplifier. The output of the duplexer drives RxI which is switched to the input of the high band band-pass filter. The filter output is available at RxO which is typically the input to a limiter and carrier detector.

The normal answer mode is established by a "0" on both O/$\overline{A}$ and ST. This mode is identical to the normal originate mode with one exception: the band-pass filters swap positions, i.e., the high band band-pass filter is switched into the transmit path, and the low band band-pass filter is switched into the receive path.

When used with the MC14412 in the self test mode, the device will function as follows. A "1" on the self test pin of both devices enables the self test mode. The modem switches its demodulator to its modulator frequency and demodulates its own modulated carrier. The modem filter switches the transmit carrier of the modem from TxI through the low band filter and out the RxO pin to the limiter when in the originate mode. When the system is in the answer mode, the modulated signal is instead routed through the high-band filter. TxO will remain at mid-supply (V_{AG}) during self test operations.

FIGURE 1 — TEST CIRCUIT

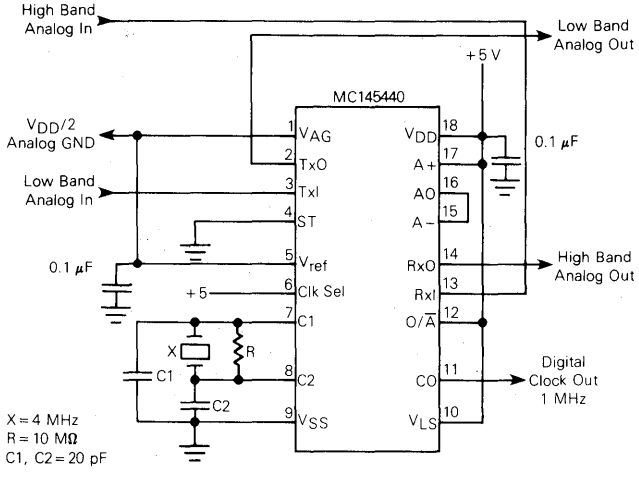


FIGURE 2 — MC145440 FREQUENCY RESPONSE

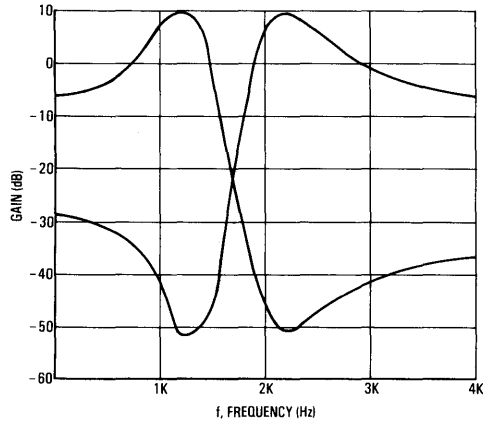
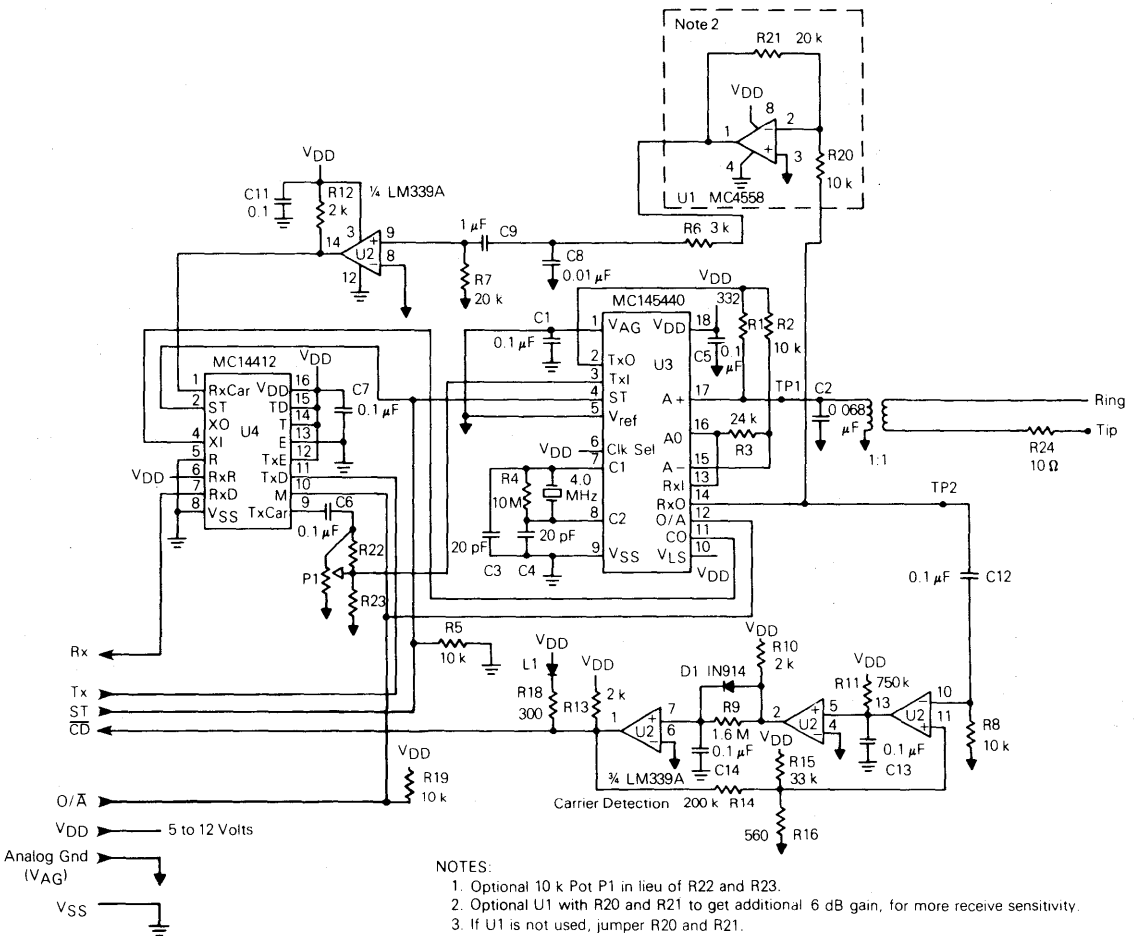


FIGURE 3 — TYPICAL MC145440 APPLICATION (+5 V SINGLE SUPPLY)



NOTES:
1. Optional 10 k Pot P1 in lieu of R22 and R23.
2. Optional U1 with R20 and R21 to get additional 6 dB gain, for more receive sensitivity.
3. If U1 is not used, jumper R20 and R21.

MOTOROLA

MC145441

Advance Information

2

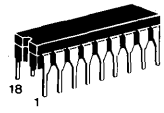
CCITT V.21 300 BAUD MODEM BAND-PASS FILTER

The MC145441 is a 300 baud modem filter designed to be used with the MC14412 or MC145445 modems. These modem/filter combinations fulfill the major requirements of a complete CCITT V.21 300 baud modem system. The MC145440 is also available to fulfill the Bell 103 equivalent filtering function. Features of the MC145441 include:

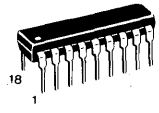
- Low Band Band-Pass Filter
- High Band Band-Pass Filter
- Spare Operational Amplifier
- Answer or Originate Mode
- Self Test Loopback Configuration (Optional)
- Single or Split Power Supply Operation
- 18-Pin Package
- CCITT V.21 Compatible

CMOS
(LOW-POWER COMPLEMENTARY MOS)

300 BAUD MODEM BAND-PASS SWITCHED CAPACITOR FILTER

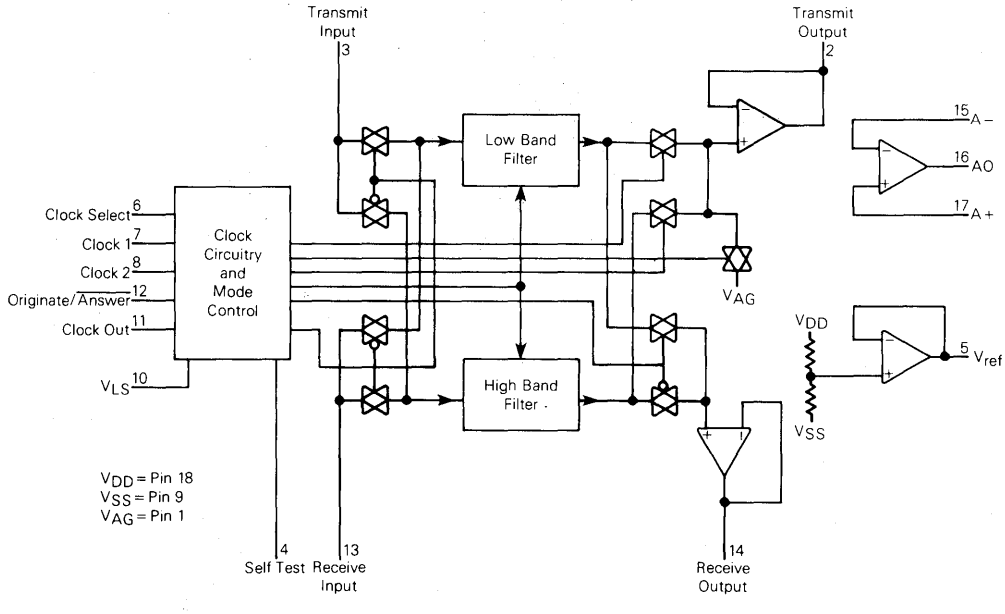


L SUFFIX
CERAMIC PACKAGE
CASE 726



P SUFFIX
PLASTIC PACKAGE
CASE 707

BLOCK DIAGRAM



This document contains information on a new product. Specifications and information herein are subject to change without notice.

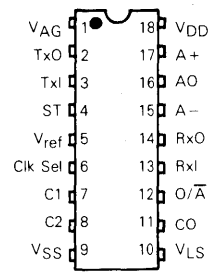
MAXIMUM RATINGS (V_{SS} = 0 V)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	−0.5 to 18	V
Input Voltage, all pins	V_{in}	−0.5 to V_{DD} + 0.5	V
DC Current Drain per pin (Not V_{DD} or V_{SS})	I	10	mA
Operating Temperature Range	T_A	−40 to 85	°C
Storage Temperature Range	T_{stg}	−65 to 150	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
DC Supply Voltage	V_{DD}-V_{SS}	4.5	10	16	V

PIN ASSIGNMENT



DIGITAL ELECTRICAL CHARACTERISTICS (T_A = −40 to 85°C)

Characteristic		Symbol	Min	Typ	Max	Unit
Operating Current, V_{DD} = 10 V, V_{SS} = 0 V, 1 MHz Crystal		I_{DD}	–	–	10	mA
Input Capacitance		C_{in}	–	5.0	7.5	pF
Mode Control Logic Levels						
V_{LS}	TTL Mode	–	V_{SS}	–	V_{DD} − 4.0	V
	CMOS Mode	V_{IH}	V_{DD} − 0.5	–	V_{DD}	
Clock Select (CS)	State 1, 4.0 MHz	V_{IH}	V_{DD} − 0.5	–	V_{DD}	V
	State 2, 3.684 MHz	V_{IM}	(V_{DD} − V_{SS})/2 − 0.5	–	(V_{DD} − V_{SS})/2 + 0.5	
	State 3, 1.0 MHz	V_{IL}	V_{SS}	–	V_{SS} + 0.5	
O/Ā TTL Logic Levels (V_{DD} = 5 V, V_{SS} = −5 V, V_{LS} = 0 V)						
Input Current	"1" level	I_{IH}	–	–	+ 0.3	μA
	"0" Level	I_{IL}	− 0.3	–	–	
Input Voltage	"1" level	V_{IH}	V_{LS} + 2.0	–	–	V
	"0" level	V_{IL}	–	–	V_{LS} + 0.8	
ST, C1, O/Ā CMOS Logic Levels (V_{LS} = V_{DD}, V_{SS} = 0 V)						
Input Current	"1" level	I_{IH}	–	–	+ 0.3	μA
	"0" level	I_{IL}	− 0.3	–	–	
Input Voltage	"1" level, V_{DD} = 10 V	V_{IH}	7.5	5.75	–	V
	"0" level, V_{DD} = 10 V	V_{IL}	–	4.25	3.0	
CO Output Characteristics (V_{DD} = 10, V_{SS} = 0 V)						
TTL Output Voltage (TTL Mode)	"1" level, I_O = 8 mA	V_{OH}	2.4	–	–	V
	"0" level, I_O = 2.5 mA	V_{OL}	–	–	0.8	
CMOS Output Current	V_{DD} = 10 V, V_{OH} = 9.5 V	I_{OH}	− 1.3	− 2.25	–	mA
	V_{DD} = 10 V, V_{OL} = 0.5 V	I_{OL}	1.1	2.25	–	

ANALOG ELECTRICAL CHARACTERISTICS (V_{DD} = 10 V, V_{AG} = 5 V, V_{SS} = 0 V, T_A = 0 to 70°)

Characteristic	Symbol	Min	Typ	Max	Unit
DC Input Current (V_{AG})	I_I	− 50	–	+ 50	μA
DC Input Current (TxI, RxI)	I_I	− 10	–	+ 10	μA
AC Input Impedance (TxI, RxI)	Z_{in}	0.2	1.0	–	MΩ
Input Voltage Range (TxI, RxI)	V_{in}	V_{SS} + 1.5	–	V_{DD} − 1.5	V

OP-AMP CHARACTERISTICS (V_{DD} = 5 to 10 V, V_{AG} = V_{DD}/2, V_{SS} = 0 V, T_A = 0 to 70°C)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Offset Voltage (AO)	I_{IO}	− 50	–	+ 50	mV
Open Loop Gain (R_L = 10 kΩ)	A_{OL}	–	45	–	dB
Input Bias Current (A+, A−)	I_{IB}	–	± 0.1	–	μA
Output Noise (900 Ω)	P_N	–	− 3	–	dBrnC
Slew Rate	S_R	–	2	–	V/μs
Output Voltage Swing (R_L = 600 Ω to V_{AG})	–	1.5 V	–	V_{DD} − 1.5 V	V

DIGITAL SWITCHING CHARACTERISTICS (V_{DD} = 5 V, V_{SS} = 0 V, T_A = 25°C)

Characteristic		Symbol	Min	Typ	Max	Unit
Input Rise and Fall Times	C1, O/A, ST	t_r, t_f	–	–	4	μs
Input Pulse Width	(TTL Mode) O/A	t_W	200	–	–	ns
	(CMOS Mode) C1, O/A, ST	t_W	125	–	–	
Clock Frequency (Driven by External Clock) (C1 Pin)	(CMOS Mode)	f_C	–	1.0	4.0	MHz
Crystal Frequency	C1, C2	f_X	1.0	–	4.0	MHz

LOW-BAND FILTER CHARACTERISTICS (V_{DD} = 10 V, V_{AG} = V_{DD}/2, V_{SS} = 0 V, T_A = 0 to 70°C)

Characteristic		Symbol	Min	Typ	Max	Unit
Full Scale Input Voltage (+3 dBmO)		V_{FS}	2.13	–	–	V_{P-P}
Gain at 1080 Hz, 0 dBmO		A_r	9.0	10.0	11.0	dB
Idle Noise, Input = V_{AG}, 900 Ω load		P_N	–	−70	−64	dBmp
Dynamic Range (Full Scale Output/Idle Noise)		DR	72	78	–	dB
Total Harmonic Distortion		THD	–	1.0	–	%
Power Supply Rejection Ratio		PSRR	–	20	–	dB
Pass-Band Ripple	980 Hz to 1180 Hz	–	–	–	2	dBp-p
Pass-band Response, Ref. 980 Hz, 0 dBmO	1180 Hz	–	−1.5	–	1.5	dB
Rejection (Ref. 1080 Hz)	1650 Hz to 1850 Hz	–	−55	–	–	dB
Differential Group Delay	980 Hz to 1180 Hz	–	–	–	600	μs

HIGH-BAND FILTER CHARACTERISTICS (V_{DD} = 10 V, V_{AG} = V_{DD}/2, V_{SS} = 0 V, T_A = 0 to 70°C)

Characteristic		Symbol	Min	Typ	Max	Unit
Full Scale Input Voltage (+3 dBmO)		V_{FS}	2.13	–	–	V_{P-P}
Gain at 1750 Hz, 0 dBmO		A_r	9.0	10.0	11.0	dB
Idle Noise, Input = V_{AG}, 900 Ω load		P_N	–	−70	−64	dBmp
Dynamic Range (Full Scale Output/Idle Noise)		DR	72	78	–	dB
Total Harmonic Distortion		THD	–	1.0	–	%
Power Supply Rejection Ratio		PSRR	–	20	–	dB
Pass-Band Ripple	1650 Hz to 1850 Hz	–	–	–	2	dBp-p
Pass-band Response, Ref. 1650 Hz, 0 dBmO	1850 Hz	–	−1.5	–	1.5	dB
Rejection (Ref. 1750 Hz)	980 Hz to 1180 Hz	–	−55	–	–	dB
Differential Group Delay	1650 Hz to 1850 Hz	–	–	–	600	μs

V_{ref} CHARACTERISTICS (V_{DD} = 5 to 15 V, V_{ref} = V_{DD}/2, V_{SS} = 0 V, T_A = 0 to 70°C)

Characteristic		Symbol	Min	Typ	Max	Unit
V_{ref} Output Voltage	I_O = ±5 mA	V_{ref}	−250	±75	+250	mV

PIN DESCRIPTIONS

V_{DD} (PIN 18) – Positive power supply.

V_{SS} (PIN 9) – Negative power supply.

V_{AG} (PIN 1) – Analog ground. In single supply applications, V_{AG} is driven from V_{ref}.

V_{ref} (PIN 5) – This pin provides an output DC voltage at approximately $(V_{DD}-V_{SS})/2$ for use as an external analog ground in single supply applications. In symmetric dual power supply applications, V_{ref} is not used.

V_{LS}, LOGIC SHIFT VOLTAGE (PIN 10) – This pin determines the input/output logic level compatibility of O/$\overline{A}$ and CO. When the voltage on this pin is greater than $V_{DD}-0.5$ V and less than V_{DD}, these digital inputs and outputs are CMOS compatible. When the voltage on this pin is less than $V_{DD}-4$ V and greater than V_{SS}, these digital inputs and outputs are TTL compatible, and V_{LS} is connected to digital ground.

C1, C2, CLOCK 1, CLOCK 2 (PIN 7, PIN 8) – These pins connect to an internal crystal oscillator. In operation, a parallel resonant crystal is connected from C1 to C2 as well as a 10 MΩ resistor in parallel with the crystal and 20 pF capacitors from C1 and C2 to V_{SS}. Crystal frequencies of 1.0, 3.6864, or 4.0 MHz may be used. Alternatively, an external CMOS level signal at the crystal frequency may be applied to C1 in lieu of the crystal, capacitors, and resistor. The inverted clock signal will appear at C2 and will be a CMOS output from V_{SS} to V_{DD}.

Clk Sel, CLOCK SELECT (PIN 6) – This pin is a three-state selector used to select one of the three crystal/clock options. When at V_{DD}, V_{AG}, or V_{SS}, this pin selects the 4.0, 3.6864, or 1.0 MHz crystal/clock option, respectively, for C1 and C2.

Clock Select Pin 6	Clock Frequency *	Clock Output Pin 11
V_{DD}	4.0 MHz	1.0 MHz
V_{AG}	3.6864 MHz	N/A
V_{SS}	1.0 MHz	1.0 MHz

*Use either an external clock to drive C1 Pin 7 or external crystal across C1 and C2 Pins 7 and 8.

CO, CLOCK OUT (PIN 11) – This provides a 1.0 MHz output clock signal when either the 1.0 or 4.0 MHz clock is selected and is typically used to drive the clock input to a MC14412 or MC6860 modem. The clock output is not usable when the 3.6864 MHz option is used. The logic family compatibility (CMOS or TTL) of this output is determined by V_{LS}.

O/$\overline{A}$, ORIGINATE, ANSWER (PIN 12) – The mode of the device, originate or answer, is selected with this pin. In the originate mode, selected with a logic "1", the low band band-pass filter is switched into the transmit path and the high band band-pass filter is switched into the receive path. In the answer mode, the filters switch position. The input levels of this pin are determined by V_{LS}.

TxI, TRANSMIT INPUT (PIN 3) – TxI is the input to the transmit band-pass filter which is the low band filter in the originate mode and the high band filter in the answer mode. In the self test mode, this input is routed to the appropriate band-pass filter input so as to pass the modulated data to the demodulator.

TxO, TRANSMIT OUTPUT (PIN 2) – This pin is the output of the Tx output amplifier and typically drives the modulated data into the duplexer or hybrid circuit (see ST pin).

RxI, RECEIVE INPUT (PIN 13) – RxI is the input to the receive band-pass filter which is the high band filter in the originate mode and the low band filter in the answer mode. In the self test mode, this input is disabled.

RxO, RECEIVE OUTPUT (PIN 14) – The output of the receive band-pass filter, whether low band or high band, is provided at RxO. Typically, this signal is capacitively coupled to the input of the external carrier detector and limiter. The AC coupling capacitor is required because of the variable DC offset of the receive filter.

ST, SELF TEST (PIN 4) – A "1" on ST puts the device into a self test mode which routes the modulated carrier from TxI, through the appropriate filter,and out RxO back to the receive carrier input of the modem. TxO remains at V_{AG} during a self test operation. This pin is a standard CMOS input regardless of the state of V_{LS}.

A+ (PIN 17) – This is the noninverting input to the spare operational amplifier.

A– (PIN 15) – This is the inverting input to the spare operational amplifier.

AO (PIN 16) – This is the output of the spare operational amplifier.

FUNCTIONAL DESCRIPTION

This device is capable of four basic analog configurations determined by the state of O/$\overline{A}$ and ST. The normal (non-self test) and self test modes in both the answer and originate modes will be discussed.

In the normal originate mode, O/$\overline{A}$ is a "1" and self test, ST, is a "0". When in this mode, the Tx carrier from the modem is input on TxI and routed through the low band band-pass filter. The filter output is switched to the input of the Tx op-amp which typically drives the Tx carrier off chip into a duplexer circuit which could be implemented with the spare operational amplifier. The output of the duplexer drives RxI which is switched to the input of the high band band-pass filter. The filter output is available at RxO which is typically the input to a limiter and carrier detector.

The normal answer mode is established by a "0" on both O/$\overline{A}$ and ST. This mode is identical to the normal originate mode with one exception: the band-pass filters swap positions, i.e., the high band band-pass filter is switched into the transmit path, and the low band band-pass filter is switched into the receive path.

When used with the MC14412 in the self test mode, the device will function as follows. A "1" on the self test pin of both devices enables the self test mode. The modem switches its demodulator to its modulator frequency and demodulates its own modulated carrier. The modem filter switches the transmit carrier of the modem from TxI through the low band filter and out the RxO pin to the limiter when in the originate mode. When the system is in the answer mode, the modulated signal is instead routed through the high-band filter. TxO will remain at mid-supply (V_{AG}) during self test operations.

FIGURE 1 – TEST CIRCUIT

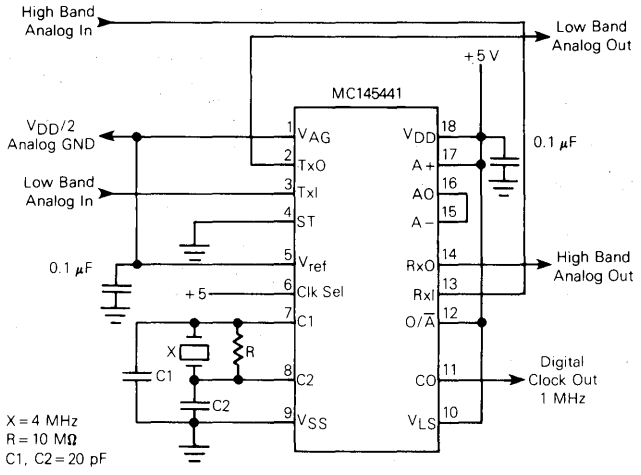


FIGURE 2 – MC145441 FREQUENCY RESPONSE

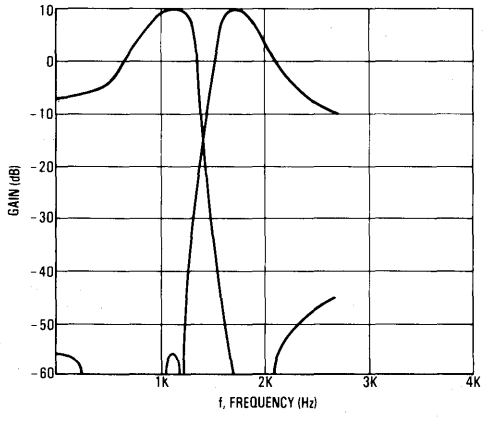
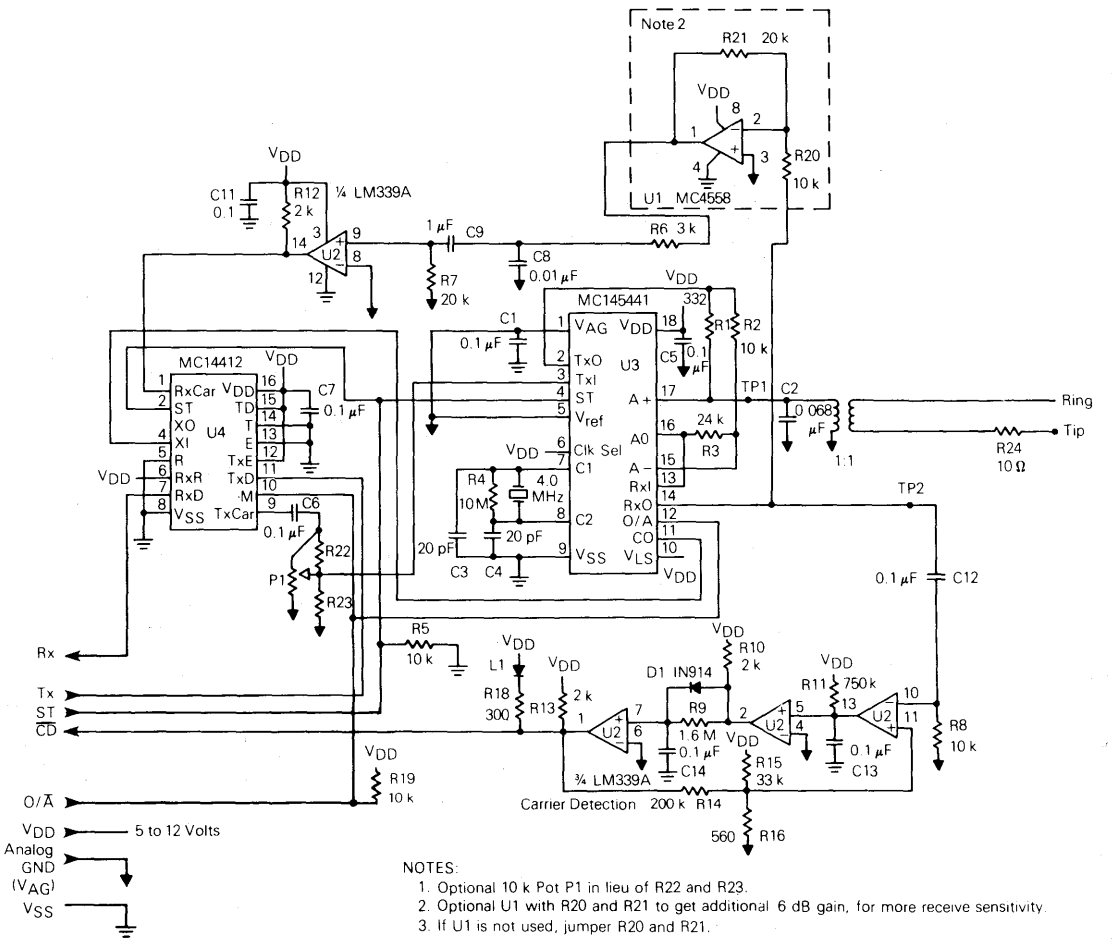


FIGURE 3 — TYPICAL MC145441 APPLICATION (+5 V SINGLE SUPPLY)



NOTES:
1. Optional 10 k Pot P1 in lieu of R22 and R23.
2. Optional U1 with R20 and R21 to get additional 6 dB gain, for more receive sensitivity.
3. If U1 is not used, jumper R20 and R21.

MOTOROLA

MC145445

2

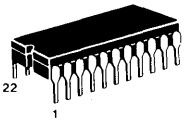
0–300 BAUD FSK MODEM

The MC145445 is a silicon-gate CMOS frequency shift keying (FSK) modem intended for use in Bell 103/113 and CCITT V. 21 applications. Features of the device include:

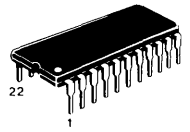
- Bell 103/113 Answer and Originate Compatible, 0-300 Baud
- CCITT V. 21 Modes 1 and 2 Compatible, 0-300 Baud
- Eight Selectable $\overline{RTS}$ to $\overline{CTS}$ Delay Options
- Answer-Back Tone Generator (U.S. and CCITT Tones)
- Carrier Detect Input
- TTL Compatible
- 22 Pin Package
- Compatible to the MC145440 Bell 103 or MC145441 CCITT V. 21 Modem Filter

CMOS

300 BAUD FSK MODEM

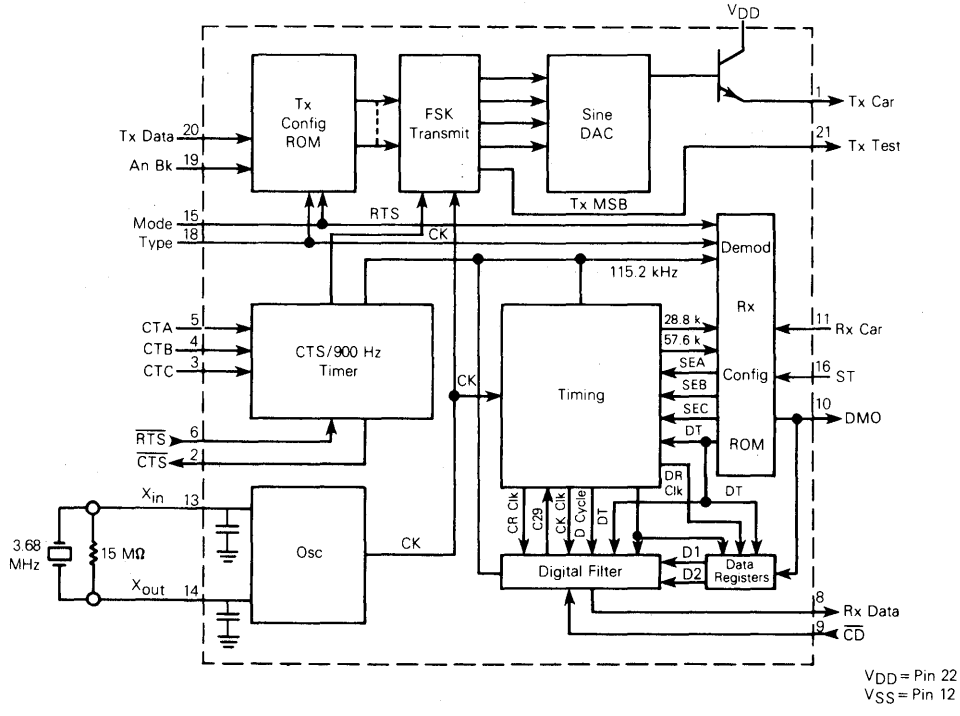


L SUFFIX
CERAMIC PACKAGE
CASE 736



P SUFFIX
PLASTIC PACKAGE
CASE 708

MC145445 300 BAUD FSK MODEM BLOCK DIAGRAM



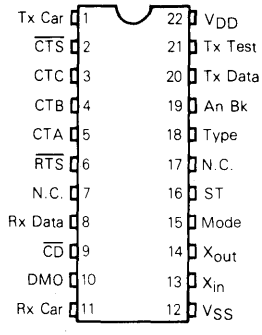
ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	10	V
Input Voltages, All Inputs	V_{in}	$V_{SS}-0.5$ to $V_{DD}+0.5$	V
DC Current Drain per Pin Pin 3-6, 9, 15, 16, 18, 19, 20 Pins 2, 8	I_{out}	 10 35	mA
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
DC Supply Voltage	$V_{DD}-V_{SS}$	4.5	5.0	6.5	V

PIN ASSIGNMENTS



DC ELECTRICAL CHARACTERISTICS ($V_{DD}=5.0$ V ±5%, $V_{SS}=0$, $0°C \le T_A \le 70°C$)

Characteristics	Symbol	Min	Typ	Max	Unit
Input High Voltage	V_{IH}	–	–	–	V
Pins 3-6, 9, 15, 16, 18, 19, 20	–	2.8	–	–	
Pin 13, 11	–	4.0	–	–	
Input Low Voltage	V_{IL}	–	–	–	V
Pin 3-6, 9, 15, 16, 18, 19, 20	–	–	–	0.5	
Pin 13, 11	–	–	–	0.6	
Input Current	I_{in}	–	–	–	μA
All Inputs (V_{IL} 0 V)	–	–	–	−5.0	
All Inputs Except Pins 11, 13, ($V_{IH}>2.8$ V) (Note 1)	–	–	–	500	
Output High Current ($V_{OH}=2.4$ V)	I_{OH}	–	–	–	mA
Pins 2, 8 (Test Load A)	–	0.75	–	–	
Pins 10, 21 (Test Load B)	–	0.75	–	–	
Output Low Current ($V_{OL}=0.4$ V)	I_{OL}	–	–	–	mA
Pins 2, 8 (Test Load A)	–	1.2	–	–	
Pins 10, 21 (Test Load B)	–	0.6	–	–	
Operating Current	I_{DD}	–	2.5	6	mA
Input Capacitance	C_{in}	–	–	–	pF
All Except Pin 13	–	–	–	12	
Pin 13 (X_{in})	–	–	8	–	
Output Capacitance	C_{out}	–	–	–	pF
All Except Pin 14	–	–	–	12	
Pin 14 (X_{out})	–	–	13	–	
Transmit Audio Signal Level (Pin 1 $R_L=10$ kΩ (Note 2)	–	0.428	0.5	0.578	Vp-p
Total Harmonic Distortion (2nd to 14th) (Note 2)	THD	–	−50	−40	dB

AC ELECTRICAL CHARACTERISTICS ($V_{DD}=5.0$ V ±5%, $V_{SS}=0$, $0°C \le T_A \le 70°C$)

Characteristics	Symbol	Min	Typ	Max	Unit
Output Rise Time (Test Load A) (Pins 2, 8)	t_r	–	20	100	ns
Output Rise Time (Test Load B) (Pins 10, 14, 21)	t_r	–	20	100	ns
Output Fall Time (Test Load A) (Pins 2, 8)	t_f	–	20	100	ns
Output Fall Time (Test Load B) (Pins 10, 14, 21)	t_f	–	20	100	ns
Input Rise and Fall Times (Except Pin 13)	t_r, t_f	–	–	1000	μs
Delay From $\overline{RTS}$ to $\overline{CTS}$	t_d	–	1	–	μs

NOTES:

1. Active pull-up devices are used on these inputs to allow interfacing to TTL devices. The I_{in} specified is a transitional load (not steady state) which is drawn when the input is brought up to 2.8 V until the internal pull-up device has raised the signal to the V_{DD} level.
2. Measured in any mode using HP-3555B dB meter (or equivalent) with 3 kHz flat filtering.

PIN DESCRIPTIONS

V_{DD}, POSITIVE POWER SUPPLY (PIN 22)
This is nominally 5.0 V.

V_{SS}, NEGATIVE POWER SUPPLY (PIN 12)
This is usually 0 volts.

Tx Car, TRANSMIT CARRIER (PIN 1)
The transmit carrier output is a 16 step digitally-synthesized sine wave with an amplitude of 0.1 V_{DD} (p-p) (±10%) and offset by a dc bias of 0.5 V_{DD} (±10%). The output load should be 10 kilohms or greater.

$\overline{CTS}$, CLEAR TO SEND (PIN 2)
The clear to send output goes low in response to a high-to-low translation of $\overline{RTS}$ following a selected delay (see CTA, CTB, CTC pin description). This output goes high immediately after loss of $\overline{RTS}$. During the time following activation of $\overline{RTS}$ and before the activation of $\overline{CTS}$, Tx Data should be held in the mark condition.

CTA, CLEAR TO SEND SELECT A (PIN 5)
CTB, CLEAR TO SEND SELECT B (PIN 4)
CTC, CLEAR TO SEND SELECT C (PIN 3)

For delay times for clear to send delay select inputs, see Table 1.

$\overline{RTS}$, REQUEST TO SEND (PIN 6)
The request to send input controls data transmission from the modulator. A low level enables the modulator output and a high level will disable the modulator. See Figure 1.

N.C., NO CONNECTION (PINS 7 AND 17)
These pins are not bonded internally. They should be left open in normal operation.

Rx Data, RECEIVE DATA (PIN 8)
The receive data output is the serial data output from the demodulator. Rx Data is clamped high when $\overline{CD}$ is not active.

$\overline{CD}$, CARRIER DETECT (PIN 9)
When carrier detect input is high (1), the Rx Data output will be clamped to a high state. When carrier detect is low (0), Rx Data output demodulates the Rx carrier input signal.

DMO, DEMODULATOR OUTPUT (PIN 10)
The demodulator output is the output of the differential delay detector. It is used for production testing of the demodulator. In normal operation, this pin should be left open.

Rx Car, RECEIVER CARRIER (PIN 11)
The receiver carrier input is the FSK input to the demodulator. This signal should be the hard-limited output of the receive filter, nominally 50%.

X_{in}, OSCILLATOR INPUT (PIN 13)
X_{out}, OSCILLATOR OUTPUT (PIN 14)
X_{in} should be driven from either an AT-cut crystal or a digital signal source at 3.6864 MHz ±0.01%. When driven by a crystal, a 15 megohm resisitor should be connected from X_{in} to X_{out} in parallel with the crystal.

MODE (PIN 15)
The mode pin selects the pair of frequencies used during modulation and demodulation. A "0" on this pin selects answer mode when Bell type is selected or channel 2 when CCITT type is selected. A "1" on this pin selects originate mode when Bell type is selected or channel 1 when CCITT type is selected.

ST, SELF TEST (PIN 16)
When a high level is placed on this pin, the demodulator is switched to the modulator frequencies (as determined by Mode and Type pins). The modulator should be looped back through the receive filter to the demodulator for self test (echo back). Loopback can be done using a hardwire scheme, or automatically using the internal loopback feature of the filter, such as found on the MC145440/41.

TYPE (PIN 18)
This pin is used to select between Bell 103/113 type operation and CCITT V.21 operation. When the type input pin is a "1", Bell operation is selected. When the type input pin is a "0", the CCITT standard is selected.

An Bk, ANSWER BACK (PIN 19)
The answer back input causes the answer back tone to be transmitted. The answer back tone is 2025 Hz for the Bell mode and 2100 Hz for the CCITT modes. When a high level is placed on the An Bk input pin, the Tx Car pin will output an answer back tone and $\overline{CTS}$ will go to a high state, regardless of the state of $\overline{RTS}$ (see Figure 1).

Tx Data, TRANSMIT DATA (PIN 20)
The transmit data input is the serial input to the modulator. A high level causes a mark frequency to be transmitted, a low level causes a space frequency to be transmitted.

Tx Test, TRANSMIT TEST (PIN 21)
The transmit test output is a square wave representation of the modulator transmit frequency. It is used for test purposes and should be left open in normal operation.

FIGURE 1 — An Bk AND $\overline{RTS}$-$\overline{CTS}$ TIMING

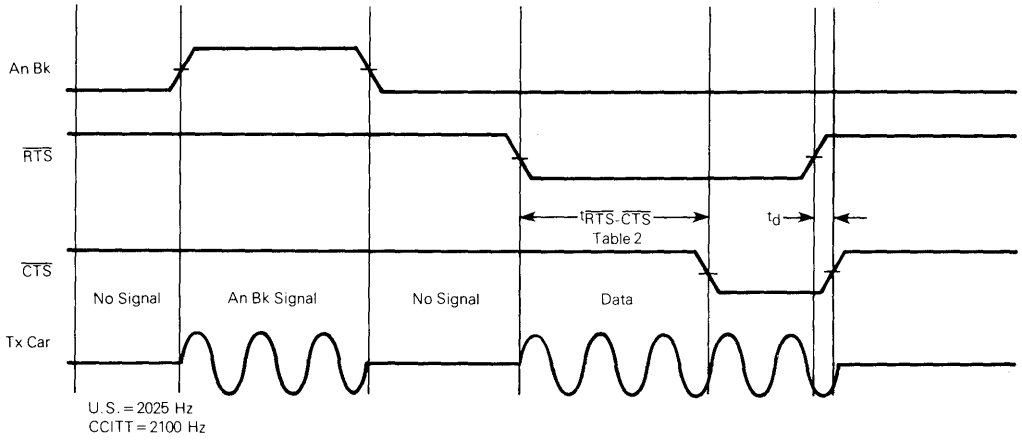


TABLE 1 — $\overline{RTS}$-$\overline{CTS}$ DELAY TIMES

CTC	CTB	CTA	Delay*
0	0	0	0 ms
0	0	1	26.7 ms
0	1	0	40.0 ms
0	1	1	60.0 ms
1	0	0	133.3 ms
1	0	1	213.3 ms
1	1	0	266.7 ms
1	1	1	426.6 ms

*All delays are ±1.7 ms.

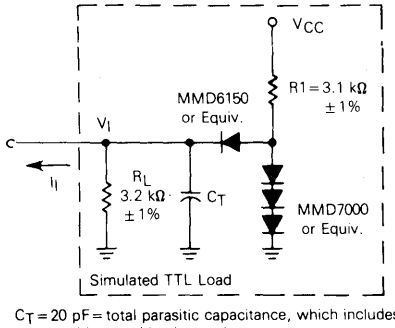
TABLE 2 — OPERATING MODES

Type	Mode	Transmit Data	Transmit Frequency Spec	Transmit Frequency Actual	Application
0	0	0	1850	1850.6	CCITT V. 21
		1	1650	1650.13	0-300 Baud, Channel 2
0	1	0	1180	1180.03	CCITT V.21
		1	980	979.9	0-300 Baud, Channel 1
1	0	0	2025	2025.5	Bell 103
		1	2225	2226.09	0-300 Baud, Answer Mode
1	1	0	1070	1069.76	Bell 103
		1	1270	1270.3	0-300 Baud, Originate Mode

Data = 0 = Space
= 1 = Mark

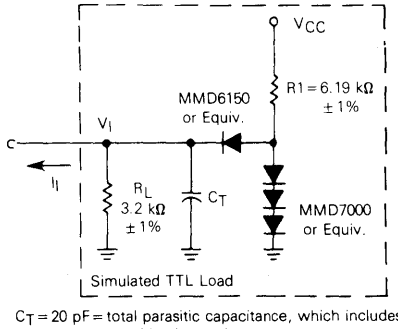
Crystal Frequency = 3.6864 MHz

FIGURE 2 — OUTPUT TEST LOAD A



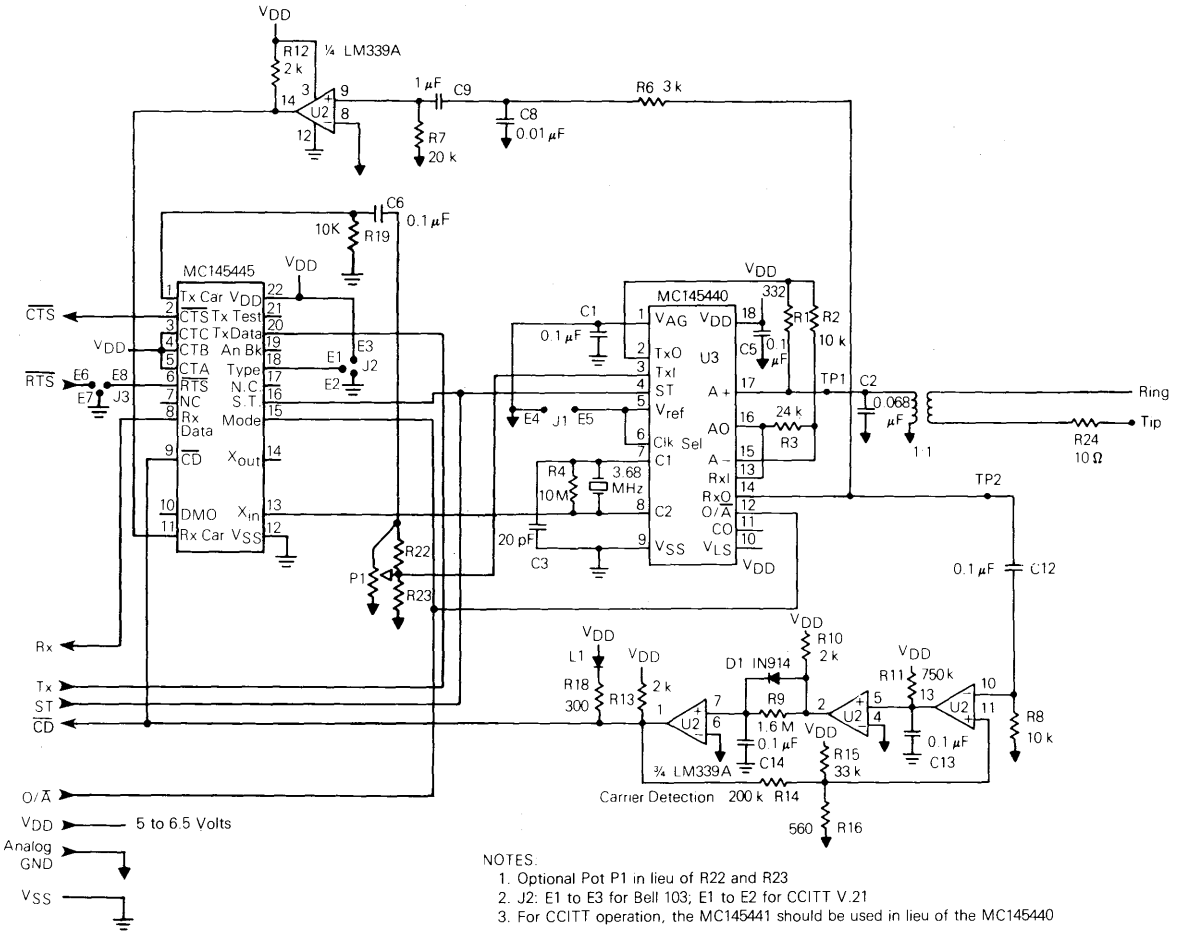
C_T = 20 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

FIGURE 3 — OUTPUT TEST LOAD B



C_T = 20 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

FIGURE 4 — TYPICAL BELL 103/113 ORIGINATE/ANSWER MODEM



NOTES.

1. Optional Pot P1 in lieu of R22 and R23
2. J2: E1 to E3 for Bell 103; E1 to E2 for CCITT V.21
3. For CCITT operation, the MC145441 should be used in lieu of the MC145440

MOTOROLA

MC145450

Advance Information

CMOS

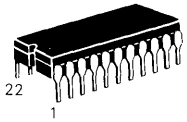
1200 BAUD
FSK MODEM

2

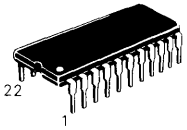
1200 BAUD FSK MODEM

The MC145450 is a silicon-gate CMOS frequency shift keying (FSK) modem intended for use in Bell 202 and CCITT V.23 applications. Features of the device include:

- Bell 202 Compatible 0 to 1800 Baud Main Channel
- 0 to 150 Baud Reverse Channel
- CCITT V.23 Mode 2 Compatible 0 to 1800 Main Channel
- CCITT V.23 0 to 75 Baud Compatible Reverse Channel
- TTL Compatible
- Eight Selectable $\overline{RTS}$-$\overline{CTS}$ Delay Options
- Soft Turn-Off Capability
- Answer Back Tone Generator (US and CCITT Tones)
- Carrier Detect Input
- 22 Pin Package

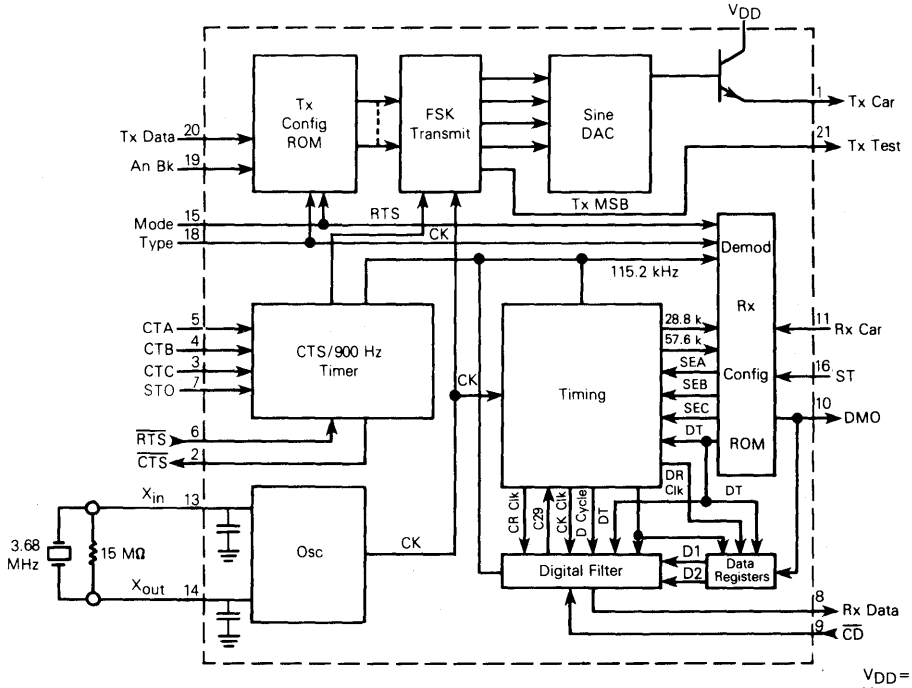


L SUFFIX
CERAMIC PACKAGE
CASE 736



P SUFFIX
PLASTIC PACKAGE
CASE 708

MC145450 1200 BAUD FSK MODEM
BLOCK DIAGRAM



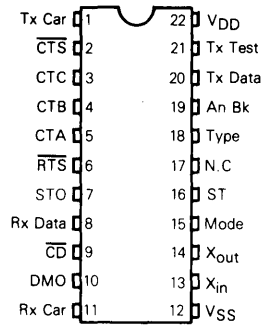
ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	10	V
Input Voltages, All Inputs	V_{in}	$V_{SS}-0.5$ to $V_{DD}+0.5$	V
DC Current Drain per Pin Pin 3-6, 9, 15, 16, 18, 19, 20 Pins 2, 8	I_{out}	 10 35	mA
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
DC Supply Voltage	$V_{DD}-V_{SS}$	4.5	5.0	6.5	V

PIN ASSIGNMENTS



DC ELECTRICAL CHARACTERISTICS ($V_{DD}=5.0$ V ±5%, $V_{SS}=0$, $T_A=0$ to 70°C)

Characteristics	Symbol	Min	Typ	Max	Unit
Input High Voltage	V_{IH}				V
Pins 3-7, 9, 15, 16, 18, 19, 20	–	2.8	–	–	
Pin 13, 11	–	4.0	–	–	
Input Low Voltage	V_{IL}				V
Pins 3-7, 9, 15, 16, 18, 19, 20		–	–	0.5	
Pin 13, 11		–	–	0.6	
Input Current	I_{in}				μA
All Inputs (V_{IL} 0 V)		–	–	−5.0	
All Inputs Except Pins 11, 13, ($V_{IH}>2.8$ V) (Note 1)		–	–	600	
Output High Current ($V_{OH}=2.4$ V)	I_{OH}				mA
Pins 2, 8 (Test Load A)		0.75	–	–	
Pins 10, 21 (Test Load B)		0.75	–	–	
Output Low Current ($V_{OL}=0.4$ V)	I_{OL}				mA
Pins 2, 8 (Test Load A)		1.2	–	–	
Pins 10, 21 (Test Load B)		0.6	–	–	
Operating Current	I_{DD}	–	2.5	6	mA
Input Capacitance	C_{in}				pF
All Except Pin 13		–	–	12	
Pin 13 (X_{in})		–	8	–	
Output Capacitance	C_{out}				pF
All Except Pin 14		–	–	12	
Pin 14 (X_{out})		–	13	–	
Transmit Audio Signal Level (Pin 1 $R_L=10$ kΩ (Note 2)	–	0.428	0.5	0.578	Vp-p
Total Harmonic Distortion (2nd to 14th) (Note 2)	THD	–	−50	−40	dB

AC ELECTRICAL CHARACTERISTICS ($V_{DD}=5.0$ V ±5%, $V_{SS}=0$, $T_A=0$ to 70°C)

Characteristics	Symbol	Min	Typ	Max	Unit
Output Rise Time (Test Load A) (Pins 2, 8)	t_r	–	20	100	ns
Output Rise Time (Test Load B) (Pins 10, 14, 21)	t_r	–	20	100	ns
Output Fall Time (Test Load A) (Pins 2, 8)	t_f	–	20	100	ns
Output Fall Time (Test Load B) (Pins 10, 14, 21)	t_f	–	20	100	ns
Input Rise and Fall Times (Except Pin 13)	t_r, t_f	–	–	1000	μs
Delay From $\overline{RTS}$ to $\overline{CTS}$ STO = Low	$t_{d(low)}$	–	1	–	μs
Delay From $\overline{RTS}$ to $\overline{CTS}$ STO = High	$t_{d(high)}$	18.3	–	21.7	ms

NOTES:

1. Active pull-up devices are used on these inputs to allow interfacing to TTL devices. The I_{in} specified is a transitional load (not steady state) which is drawn when the input is brought up to 2.8 V until the internal pull-up device has raised the signal to the V_{DD} level.
2. Measured in any mode using HP-3555B dB meter (or equivalent) with 3 kHz flat filtering.

PIN DESCRIPTIONS

V_{DD}, POSITIVE POWER SUPPLY (PIN 22)
This is nominally 5.0 V.

V_{SS}, NEGATIVE POWER SUPPLY (PIN 12)
This is usually 0 volts.

Tx Car, TRANSMIT CARRIER (PIN 1)
The transmit carrier output is a 16 step digitally-synthesized sine wave with an amplitude of 0.1 V_{DD} (p-p) (±10%) and offset by a dc bias of 0.5 V_{DD} (±10%). The output load should be 10 kilohms or greater.

$\overline{CTS}$, CLEAR TO SEND (PIN 2)
The clear to send output goes low in response to a high-to-low translation of $\overline{RTS}$ following a selected delay (see CTA, CTB, CTC pin description). This output goes high immediately after loss of $\overline{RTS}$. During the time following activation of $\overline{RTS}$ and before the activation of $\overline{CTS}$, Tx Data should be held in the mark condition.

CTA, CLEAR TO SEND SELECT A (PIN 5)
CTB, CLEAR TO SEND SELECT B (PIN 4)
CTC, CLEAR TO SEND SELECT C (PIN 3)

For delay times for clear to send delay select inputs, see Table 1.

$\overline{RTS}$, REQUEST TO SEND (PIN 6)
The request to send input controls data transmission from the modulator. A low level enables the modulator output and a high level will disable the modulator. See Figure 1.

STO, SOFT TURN OFF INPUT (PIN 7)
Activation of STO causes a 900 Hz tone to be transmitted and $\overline{CTS}$ to remain active for 20 ms following the loss of $\overline{RTS}$. See Figure 5.

Rx Data, RECEIVE DATA (PIN 8)
The receive data output is the serial data output from the demodulator. Rx Data is clamped high when $\overline{CD}$ is not active.

$\overline{CD}$, CARRIER DETECT (PIN 9)
When carrier detect input is high (1), the Rx Data output will be clamped to a high state. When carrier detect is low (0), Rx Data output demodulates the Rx carrier input signal.

DMO, DEMODULATOR OUTPUT (PIN 10)
The demodulator output is the output of the differential delay detector. It is used for production testing of the demodulator. In normal operation, this pin should be left open.

Rx Car, RECEIVER CARRIER (PIN 11)
The receiver carrier input is the FSK input to the demodulator. This signal should be the hard-limited output of the receive filter, nominally 50%.

X_{in}, OSCILLATOR INPUT (PIN 13)
X_{out}, OSCILLATOR OUTPUT (PIN 14)
X_{in} should be driven from either an AT-cut crystal or a digital signal source at 3.6864 MHz ±0.01%. When driven by a crystal, a 15 megohm resisitor should be connected from X_{in} to X_{out} in parallel with the crystal.

MODE (PIN 15)
The mode pin selects the pair of frequencies used during modulation and demodulation. A "0" on this pin selects forward channel operation; i.e. high-speed transmit and low-speed receive. A "1" on this pin selects reverse channel operation; i.e. low-speed transmit and high-speed receive.

ST, SELF TEST (PIN 16)
When a high level is placed on this pin, the demodulator is switched to the modulator frequencies and baud rate (as determined by Mode and Type pins). The modulator should be looped back through the receive filter to the demodulator for self test (echo back).

N.C. NO CONNECTION (PIN 17)
This pin is not bonded internally and should be left open in normal operation.

TYPE (PIN 18)
This pin is used to select Bell 202 type operation and CCITT V.23 operation. When the type input pin is a "1", Bell operation is selected. When the type input pin is a "0", the CCITT standard is selected.

An Bk, ANSWER BACK (PIN 19)
The answer back input causes the answer back tone to be transmitted. The answer back tone is 2025 Hz for the Bell mode and 2100 Hz for the CCITT modes. When a high level is placed on the An Bk input pin, the Tx Car pin will output an answer back tone and $\overline{CTS}$ will go to a high state, regardless of the state of $\overline{RTS}$ (see Figure 1).

Tx Data, TRANSMIT DATA (PIN 20)
The transmit data input is the serial input to the modulator. A high level causes a mark frequency to be transmitted, a low level causes a space frequency to be transmitted.

Tx Test, TRANSMIT TEST (PIN 21)
The transmit test output is a square wave representation of the modulator transmit frequency. It is used for test purposes and should be left open in normal operation.

FIGURE 1 — An Bk AND $\overline{RTS}$-$\overline{CTS}$ TIMING

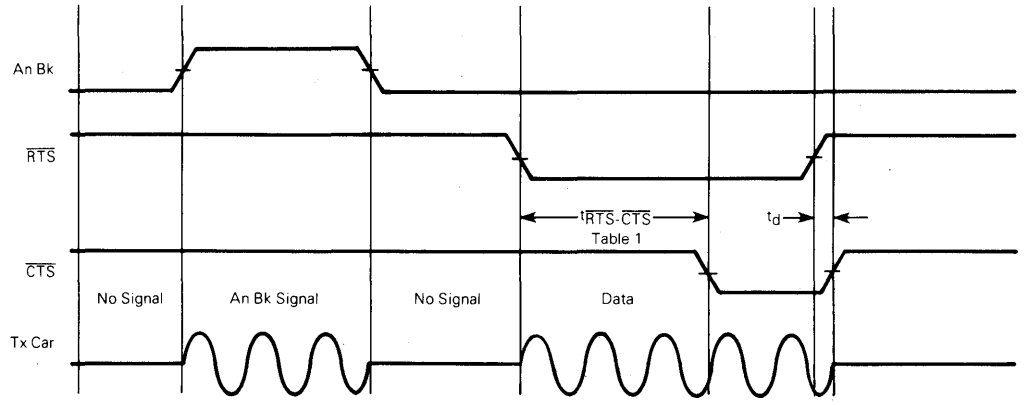


TABLE 1 — $\overline{RTS}$-$\overline{CTS}$ DELAY TIMES

CTC	CTB	CTA	Delay*
0	0	0	0 ms
0	0	1	26.7 ms
0	1	0	40.0 ms
0	1	1	60.0 ms
1	0	0	133.3 ms
1	0	1	213.3 ms
1	1	0	266.7 ms
1	1	1	426.6 ms

*All delays are ±1.7 ms.

TABLE 2 — OPERATING MODES

Type	Mode	Transmit Data	Transmit Frequency Spec	Transmit Frequency Actual	Answer Back Tone	Application
0	0	0	2100	2099.32	2100	CCITT V.23 75 Baud Receive 1200 Baud Transmit Forward Channel
		1	1300	1299.86		
0	1	0	450	450	2100	CCITT V.23 1200 Baud Receive 75 Baud Transmit Reverse Channel
		1	390	390.5		
1	0	0	2200	2199.52	2025	U.S. 150 Baud Receive 1200 Baud Transmit (Bell 202) Forward Channel
		1	1200	1200		
1	1	0	510	509.73	390	U.S. 1200 Baud Receive (Bell 202) 150 Baud Transmit Reverse Channel
		1	390	390.5		

Data = 0 = Space
= 1 = Mark

*Crystal Frequency = 3.6864 MHz

FIGURE 2 — STO TIMING

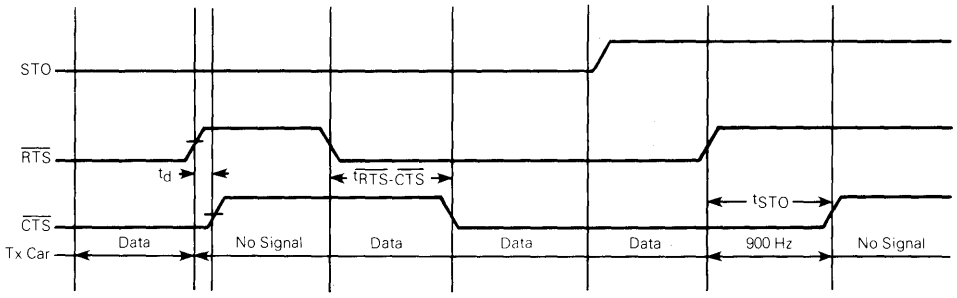
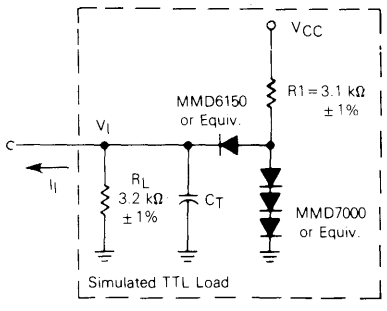
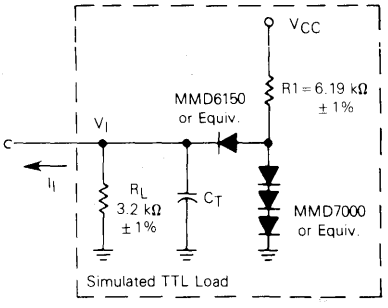


FIGURE 3 — OUTPUT TEST LOAD A



C_T = 20 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

FIGURE 4 — OUTPUT TEST LOAD B



C_T = 20 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

FIGURE 5 — TYPICAL MEDIUM-SPEED MODEM APPLICATION

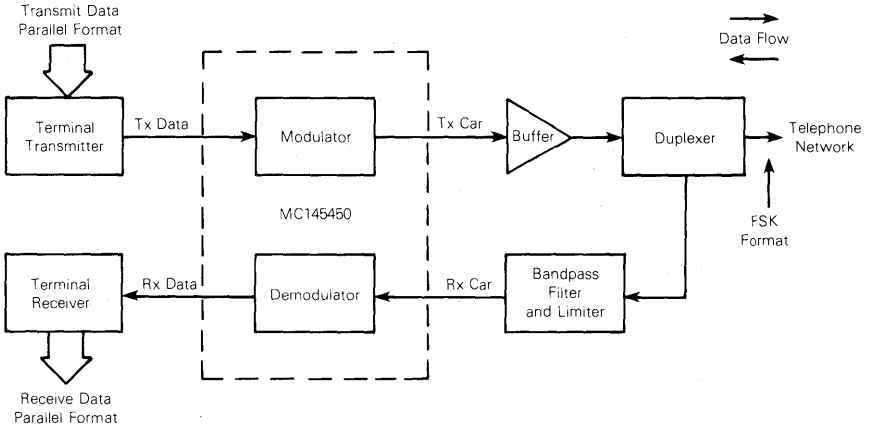
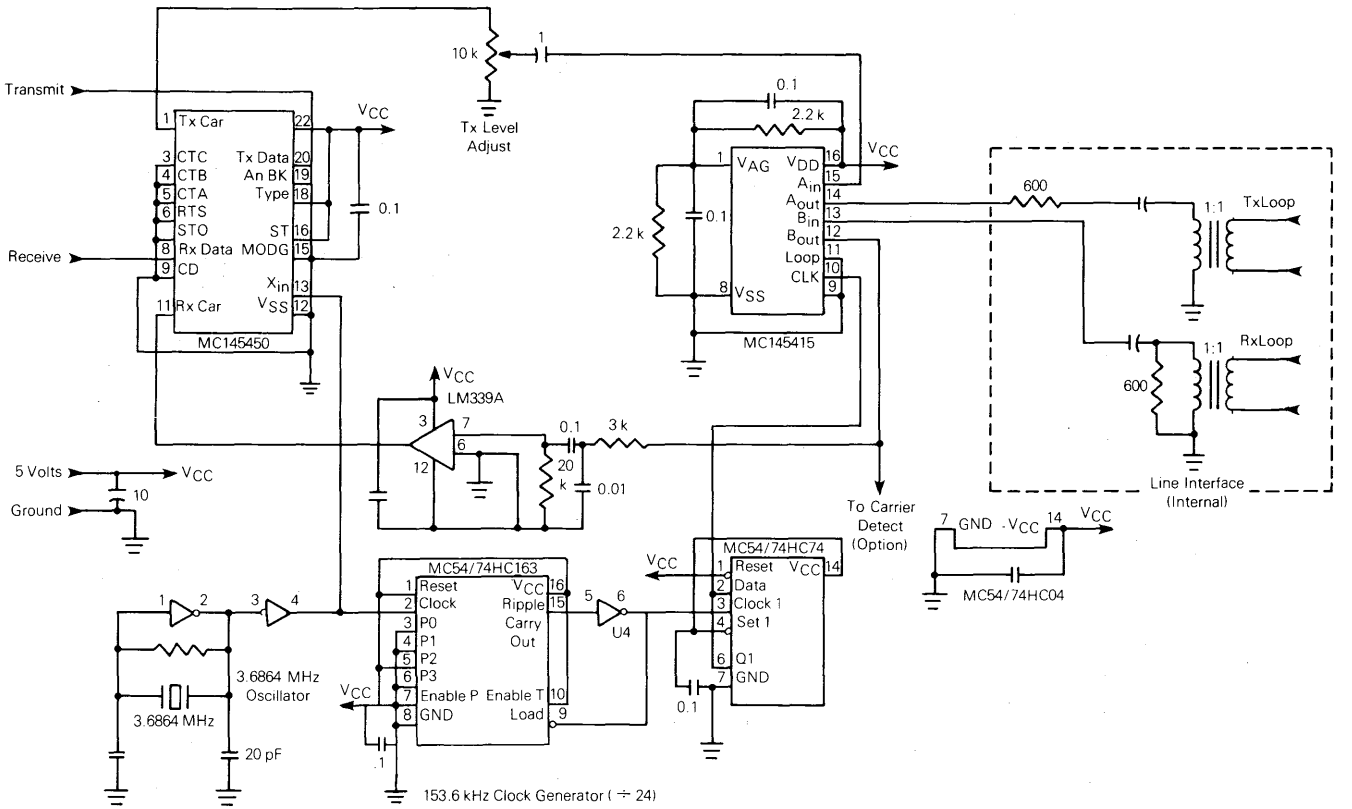


FIGURE 6 — TYPICAL 1200 BAUD 4 WIRE MODEM APPLICATION



Application Notes and Technical Articles

3

3

MOTOROLA

UNDERSTANDING TELEPHONE KEY SYSTEMS

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INTRODUCTION

This application note is intended to give an understanding of key systems and how they differ. A theoretical architecture based loosely on many of the 16 station key systems now in existence will be presented. Possible variations and the impact on overall design will also be discussed.

WHAT IS A KEY SYSTEM?

A key system is a telephone system that can be used behind a PBX or central office. Generally, key systems are designed to support as many as 100 telephones, and provide service to these phones with up to 50 percent trunking (a trunk may be either a PBX or central office line connecting the key system to the rest of the world). The telephone set has several push buttons that are not generally found on a K500-type desk set. These push buttons allow direct access to several trunks, intercom lines and system features such as hold and do-not-disturb. The major difference between a key system and a PBX is that a key system allows the user full control over individual trunks, while a PBX assigns whatever trunk is available when requested (usually this is done by dialing a "9").

HOW DOES "SQUARENESS" AFFECT THE SIZE?

There are two basic architectural types of key systems, one known as a "square" system, and the other a "non-square" system. In a square system, every subset has control over every trunk so there can be no special reserved lines. Some designs go one step further by forcing a button appearance for each station. The most obvious size limiting factor in a square system is the number of buttons on the phone. In a non-square system, each phone is provided with a subset of the available trunks. While this makes the non-square system design appear more attractive, one must understand the complexity involved. In a square system, only one set of tip and ring wire pair must be routed to the phone, and since each phone looks identical, bookkeeping by the CPU is held to a minimum. In a non-square system there must either be a separate voice pair for each trunk and intercom link, as in 1A2 system, or there must be a way to program the telephone's "profile" into the CPU so it can control the station accesses. This presents real problems as there must be some input and display device associated with the CPU plus some form of non-volatile data storage. This storage can be anything as simple as several dip switches, or as complicated as an intelligent controller that hooks into the system with a CRT terminal and programs several EEPROMs.

WHAT IS A 1A2 SYSTEM?

The 1A2 key system is an older system that relied on electro-mechanical devices to accomplish the tasks now replaced by modern integrated circuit technology. These systems generally included several pairs of tip and ring signals which led to each station, where complicated mechanical switches selected the desired pair. The connections to the outside world were metallic, and therefore were of the non-protected variety. The biggest expense was cabling and installation labor, because the system required a 25-pair cable for each phone.

WHAT IS MEANT BY "PROTECTION"?

A protected key system is designed in such a way to prevent stressful voltages reaching the trunk under any circumstances. Generally, this is accomplished by transformer coupling the trunk to the system at the interface and adding overvoltage protection. This will prevent any accidents from causing problems with the trunk, such as 110 Vac getting to the trunk from an improperly installed telephone. When a key system is not protected, it must be installed by a registered agent of the manufacturing company. Both distributor and manufacturer are burdened by expensive agency agreements if a system is not protected.

KEY SYSTEM ARCHITECTURE

A 16-station square system with protection is outlined in Figure 1. The trunk interfaces provide the necessary protection to pass the FCC requirements, plus the circuitry to condition the voice and signaling information to make them

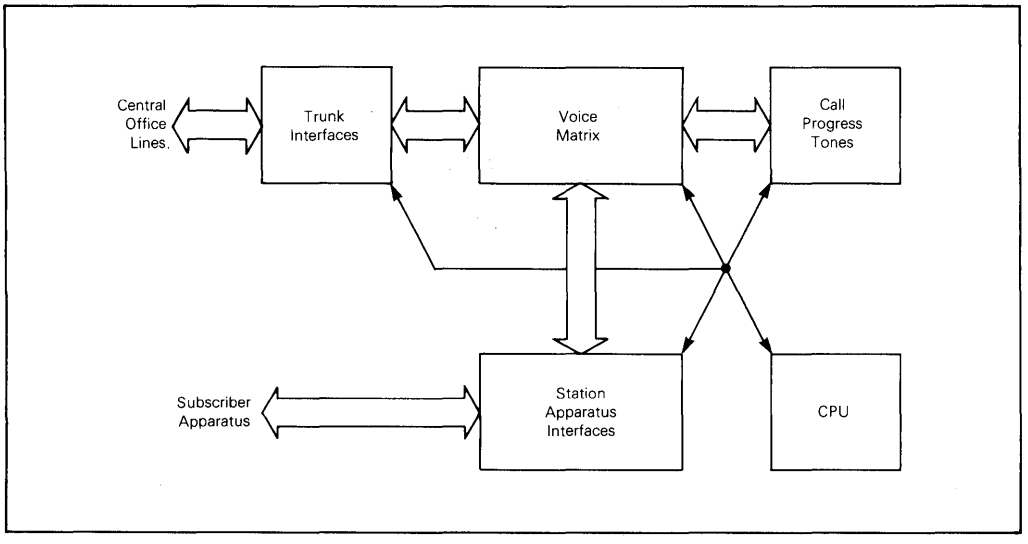


FIGURE 1 — Key System Unit

easier for the system to handle. The voice information is passed to a voice matrix, where the information can be routed to the proper destinations, and the signaling goes to the CPU to indicate what is happening at the interface. The station apparatus interfaces provide the voice and data interfaces to the phones. The progress tones are for internal supervisory signaling within the switch. The CPU is charged with the supervisory and monitoring tasks for all other parts of the system.

A much more detailed look at the voice matrix is provided in Figure 2. The voice matrix is an analog crosspoint variety which may be composed of relays or CMOS switches. Relays are a good voice switch medium for systems with eight or less stations, but the newer crosspoint ICs, such as the MC142100 and MC142101, are much more cost effective. There is some loss associated with the switches (about 100 ohms) that does not occur in the relays. In our example we will consider a $4 \times 4 \times 2$ crosspoint and the dotted lines outlining the three chips needed for the matrix. The music-on-hold (MOH) music and the tones are separated to help alleviate crosstalk within the switch structure. The design includes the ability to handle 3 trunks and 1 internal conversion. This appears to be a standard that was implemented through the years. Most systems allow expansion to either 2 more trunks or a trunk and an intercom link by adding to the matrix. Bridging more than one trunk or station can be easily accomplished by setting multiple contact points.

The loss the switch introduces into the system is the major drawback to using the CMOS crosspoint switch. The FCC requires that the electrical-to-acoustical loss of the system from the trunk to the station must not exceed 2.5 dB. A look at Figure 3A shows that a typical trunk-to-station loop has loss in two areas. The two crosspoint switches represent a typical 200 ohm resistance when they are in an on state which creates about 2.5 dB of loss in a 600 ohm system. Each transformer also introduces some loss so the electrical-to-electrical loss exceeds 2.5 dB. Changing the internal resistance of the loop minimizes the switch resistance but the transformer efficiency is greatly decreased so no advantage is found here. The loop could be amplified, but this is costly and leads to unstable circuitry so the phone must be designed to operate on different levels from a standard phone. The FCC allows another 2.5 dB of loss for a station-to-station talk path as shown in Figure 3B so the extra switches in the loop are not a problem.

Figure 4A is a block diagram of the trunk circuit. When the trunk is idle, the tip and ring are bridged by the loop relay across the ring detect circuit. This circuit signals the CPU when a call is ringing in from the central office or PBX. When the trunk is accessed by the system the loop relay connects tip and ring to the transformer. The protect circuit helps prevent surge and static damage. The battery reversal detector is an optional circuit that alerts the CPU when the tip and ring polarity has been reversed. This usually happens momentarily when a central office toll circuit has been accessed, so this is for toll restriction. The loop detect circuit is needed to indicate when the connection has been terminated by the outside caller. This prevents the hold function from locking up a trunk. If pulse dialing is to be provided a relay circuit similar to the one in Figure 4B must be added to the loop. The CPU must read the pulses from the station and transfer them to the trunk. Another possible optional circuit is a ground loop detector. This is needed to detect grounds on a groundstart trunk. These trunks use a ground to start where loopstart trunks (the most common kind) use loop continuity to start.

The station interface in Figure 5 is a four-wire design. The first pair (tip and ring) are used to provide voice communications while the second pair (D+ and D−) provide data communications. The two resistors in the voice circuit provide a current limiting function to prevent catastrophic system failures should tip and ring get shorted together. The protect circuit functions in a manner similar to the trunk protect circuit and the loop detect is used to detect the making and

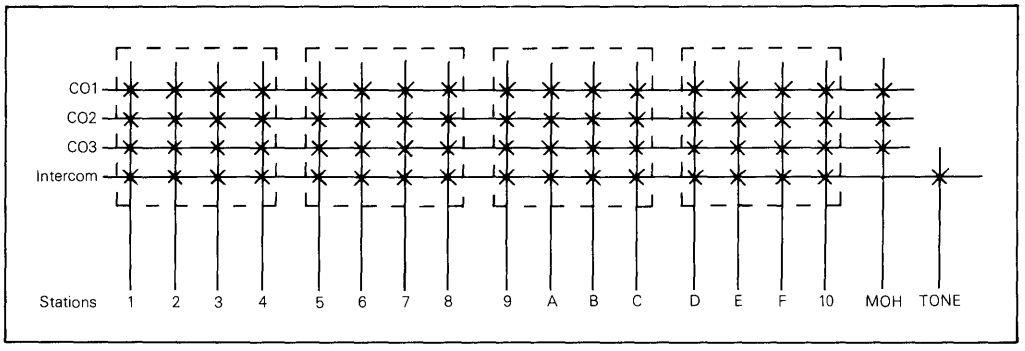


FIGURE 2 — Voice Matrix

breaking of the loop to pass pulse dialing signaling to the trunk. The resistors in the data interface do the same job in the voice circuit as does the protect circuit. The differential mode transmitter and receiver provide a serial data stream interface for the data communications. The data is generally in a half-duplex ping-pong arrangement, where the outgoing data tells the station which lamps should be on, whether the ringer is to ring, and whether the call announcer should be energized. The incoming data gives the status of the phone's hookswitch and the buttons on the keypad.

Another name for the station apparatus is the keyphone or the subset. Figure 6 is a block diagram of the subset. Tip and ring come into the subset through the hookswitch. When the handset is on-hook, the tip and ring are directed to the handsfree/call announcer circuit. This circuit is similar to a speakerphone circuit. When the handset is removed from its cradle, the tip and ring is routed to the speech network for normal telephone operation. Each voice network is powered by the battery voltage on tip and ring. The data circuit is powered by its own battery feed to help prevent crosstalk between voice and data. The data is brought into the control logic to activate the lamps, ringer, and in some cases, the handsfree/call announcer.

There are several variations on the voice and data links to the subset. Some systems impress the data, which generally has a rate well above the voice channel, onto the tip and ring for a single pair run. Extra filtering is needed to separate voice and data. Another variation connects tip and ring to the speech network causing the handsfree/call announcer to receive voice over the same wire pair as the data. This allows "off-hook call announcing" where the user can be paged via the call announcer while off-hook talking. Generally the output level of the call announcer is greatly attenuated when the handset is not in the cradle.

Another interesting variation to the architecture deals with how the dialing is controlled by the system. In this arrangement all DTMF tones or dial pulses originate at the subset and are passed through the system as though it is transparent. This is known as end-to-end signaling. An alternative is to place the pulse or tone dialer on the trunk interface and read the dial by the control logic so the dialing information is passed through the CPU to be interpreted at the trunk. The major drawback here is that there must be extra circuitry in the subset to produce aural feedback. In a normal phone the DTMF encoder mutes the speech network. Since the encoder is not here the mute is lost. The levels needed at the trunk may be uncomfortable, so they must not reach the user, therefore some feedback must be generated to indicate dialing has taken place.

Adaptation of this system into a non-square system requires several major system modifications. Since a non-square system allows only a portion of the trunks and available features to be represented as buttons on the subset, some scheme of accessing other non-appearing trunks and features must be employed. This is usually done by dial access. In a dial access system, every subset must have a dial intercom button. When this button is accessed the system must provide a dial tone and a dialing register. The dialing register must be capable of counting dial pulses and decoding DTMF data. Since DTMF decoders alone are in the $20-$30 price range the number of registers are generally restricted. This can cause bottlenecking problems when there is a need for more dial accesses than the number of registers available. There is generally a tone associated with this overload (the overload is called blocking) that indicates to the user that all circuits are busy. If all intercom links are busy when access is needed, then blocking also occurs. Now that the buttons must have some flexible assignments a data base of the subset "profiles" must be retained by the CPU. In addition to this data base duty, new software overheads are necessary for the CPU to allow dial and button accesses, as well as the addition of new, extended features such as dial intercom that are generally included in the non-square system.

There are several alternatives in operation during a power failure. One solution is called powerfail cutthrough. In this scheme certain trunks are metalically connected to certain phones. Our subset design does not support this arrangement since ringing would be impossible and the call announcer would be bridged across tip and ring when the subset is on-hook. The system can be designed so that ringing occurs in a normal manner, but a ringing generator is necessary. The ringing generator is a specialized ac power source. An alternative is battery back-up, and since most systems have a master power supply of 24-48 Vdc, this can be easily accomplished. The major advantage to this that no calls are lost on the power loss as in cut-through, and unless a sophisticated cut-through system is employed, calls are lost on the return to power which again is not a problem in a battery backed-up system. The system must be a low-power design or the battery back-up system may become prohibitively expensive.

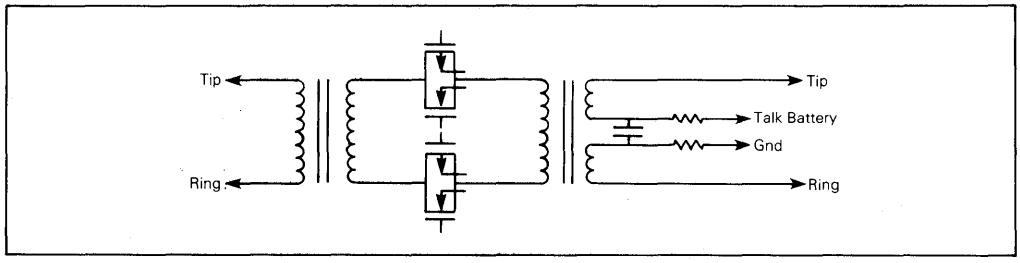


FIGURE 3A — Trunk-to-Station Loop

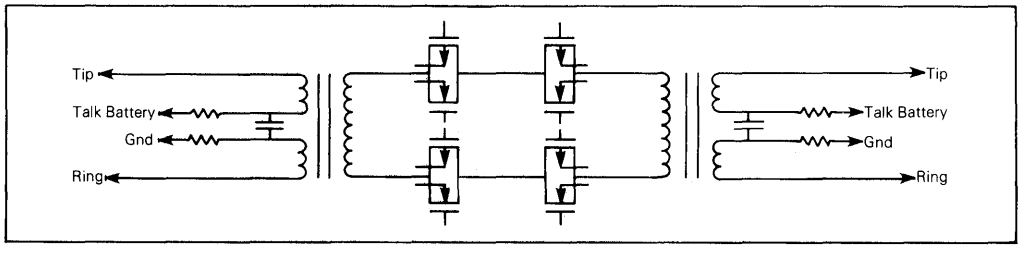


FIGURE 3B — Station-to-Station Loop

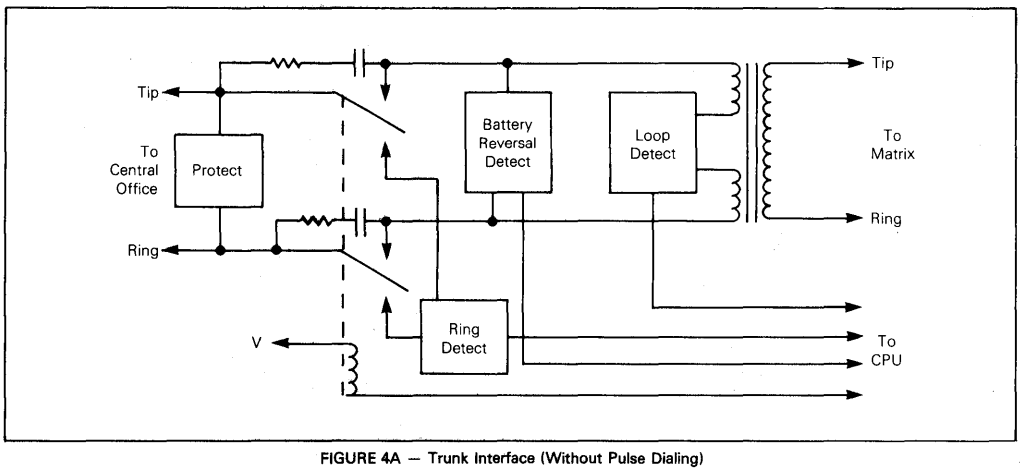


FIGURE 4A — Trunk Interface (Without Pulse Dialing)

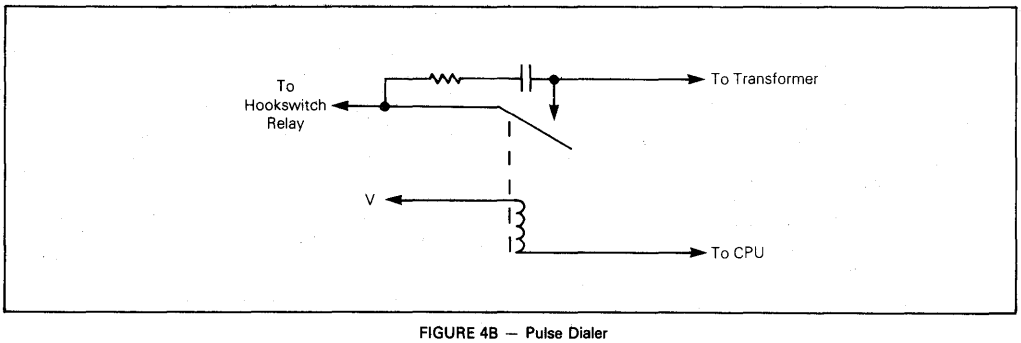


FIGURE 4B — Pulse Dialer

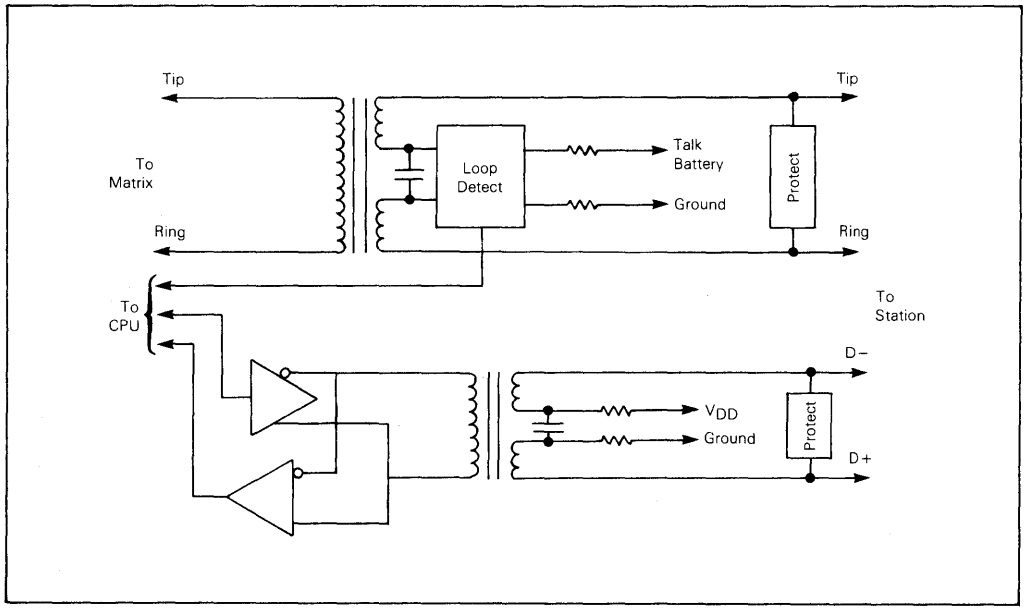


FIGURE 5 — Station Interface (Without Ring Generator)

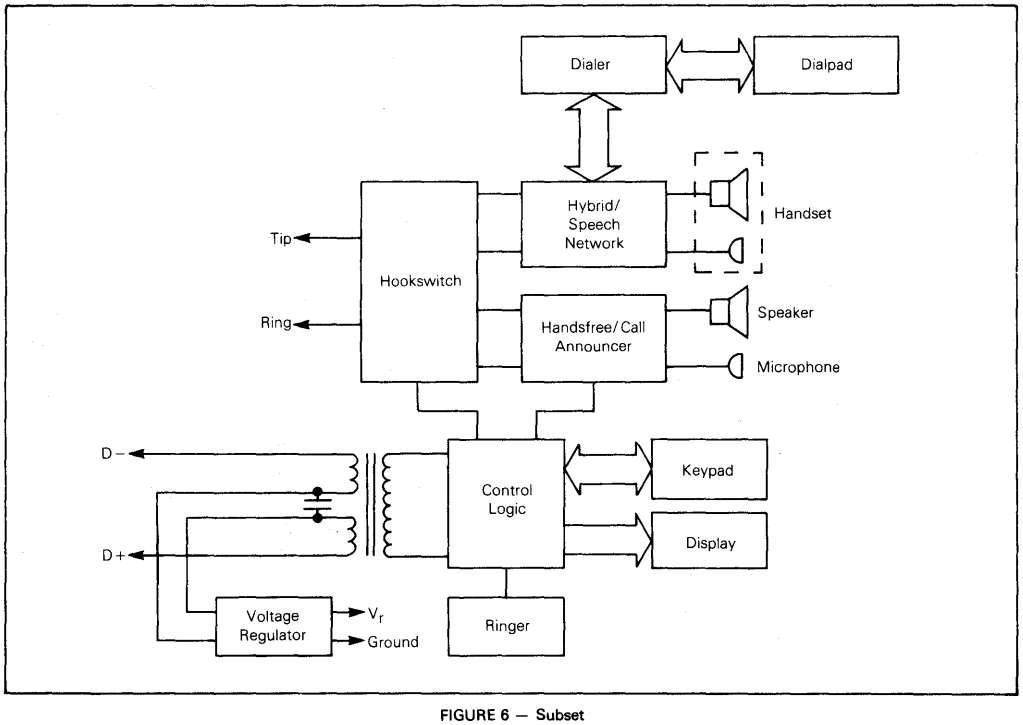


FIGURE 6 — Subset

GLOSSARY OF KEY SYSTEM FEATURES

All Call — This is where all of the call announcers are energized in the system for a general announcement. This is similar to a page except the call announcers are used instead of auxiliary amps and speakers.

Background Music — This is a feature that requires an external music source. The music is routed to all of the call announcers so that, if desired, the call announcer can provide music when the subset is idle.

Busy Lamp Field — This is an array of lamps or LEDs that indicate when each station in the system is busy or idle. This is usually abbreviated as BLF.

Call Announce — This function is performed instead of ringing. When an individual phone is call announced, the call announce circuitry is energized. A warning tone is then sent to both parties and then the parties are connected as in a conversation. The called party can talk over the call announcer as if it were a speakerphone.

Call Forward-Busy — An incoming call is routed to a secondary subset when first subset is busy.

Call Forward-Follow Me — An incoming call to one subset is routed directly to another subset.

Call Forward-No Answer — If a call is not answered in a specified period of time, the call is rerouted to a second subset.

Call Park — This feature is only used in non-square systems. When a call comes in it can be "parked," then any subset can pick the call up by accessing the parked call. This allows the subsets to pick up calls on non-appearing trunks.

Call Progress Monitor — This is a device that allows the monitoring of the calling function prior to completing the connection. All dial tones, dialing tones and ring back tones are heard over an auxiliary speaker as it would sound over a handset. This is a simplex device so no conversation can be held.

Camp On-Auto Call Back — When a called station is busy, the caller can camp on to that station so that when the subset becomes idle, it will ring. If the caller hangs up prior to the subset becoming idle, the caller's subset will ring and after he answers, the other subset will ring. The second case is known as auto call back and is an extension of the first case being camp on.

Conference — A conference is a call that has more than two parties involved in the call at one time.

Dial Intercom — A dial intercom is an intercom that when accessed allows the user to access other subsets, trunks and features with dial codes. This is only found in systems where there is not an access button for each subset.

Do Not Disturb — When this feature is activated at a subset, no incoming calls will ring the subset, however, the phone can still be used for outgoing calls. The subset will not acknowledge the call announcer either.

Direct Station Select — This allows one subset to establish an intercom call with a second subset by using a dedicated button as opposed to a dial code. This is a very popular feature in small square systems and is generally referred to as DSS.

Exclusion-Privacy — When active, this feature prevents other subsets from barging in on your call.

Executive Override-Barge In — Barge in is a feature that allows one to enter an already active conversation so that a conference is created. Executive override is the same feature applied to special phones to overcome an exclusive call (see Exclusion).

Handsfree — In an apparatus sense, this is known as speakerphone operation. In essence, a conversation is held over the subset's speaker and microphone while the handset is in the cradle. This frees the hands for other uses and several people can participate in the conversation at the handsfree end.

Music-On-Hold — This is a feature that requires an outside music source that may or may not be the same source used in background music. When someone is parked or put on hold they are provided with music instead of silence.

Page — This feature is similar to All Call except the general announcements are made over a user-supplied public address system instead of call announcers. This is especially useful in warehouse situations.

Recall — The recall feature is designed to prevent excessively long holds and call parks. When a call has exceeded the recall timeout while on hold or parked, it will ring the subset that either put it there or an attendant station.

Remote Answer — This feature exists only on non-square systems. When an incoming call rings a subset, it can be answered at another subset that does not have that particular line by invoking the remote answer feature.

Repertory Dial — This feature can be associated with either the subset or the system. This is where several commonly called phone numbers are internally stored and can be automatically dialed when accessed. This is also known as speed or abbreviated dialing.

Secretarial Intercom — This is a special case DSS where the called subset rings only while the access button is depressed. This allows private ring codes to be used between subsets to alert the users to special conditions.

Station Hunting — Station hunting is an advanced feature found usually on large, complex system. This feature allows groups of subsets to be "hunted". When a call is placed to this group, the first phone rings for a preset period of time, and if there is no answer, the second phone in the group rings. This will progress through all the subsets and the call can be answered at any subset at any time.

Tie Trunks — A tie trunk is used to link systems together. Generally the two systems are remotely located and can even be in different cities. The tie trunk does not rely on central office intervention.

Toll Restriction — This feature prevents unauthorized subsets from making toll calls.

Transfer — This feature is needed only in non-square systems and it allows a call to be moved to a subset that does not have a button appearance for that call.

MOTOROLA

TELEPHONE QUALITY CVSD CODECS USING NEW BIPOLAR LINEAR/I2L I.C.

Stephen H. Kelley
and
John J. Price

3

INTRODUCTION

Principles of continuously variable slope delta modulation for communications systems are discussed including an S plane model for a simple delta modulator with adjustable gain. A new bipolar I^2L circuit for implementing CVSD systems is presented. System performance and design techniques for a basic voice band codec and a telephone quality codec are included. Double integration and active companding ratio control techniques for improving codec performance is discussed. The emphasis is on a practical, mass producible telephone codec.

The continuously variable slope delta modulator (CVSD) is a simple alternative to more complex conversion schemes in systems requiring digital communication of analog signals. Voice and audio communications are analog, but digital transmission of any signal over great distance is more attractive. S/N ratios of the recovered signal do not vary with distance when using digital transmission; and multiplexing, switching, and repeating hardware is more economical and easier to design. However, instrumentation A to D converters do not easily meet the bandwidth constraints of communications requirements. The CVSD A to D is well suited to the requirements of digital communications and is an economical, efficient means of digitizing analog inputs for digital transmission.

THE DELTA MODULATOR

The innermost control loop of a CVSD converter is a simple delta modulator. That portion of the CVSD is shown in Figure 1. A delta modulator consists of a comparator in the forward path and an integrator in the feedback path of a simple control loop. The inputs to the comparator are the input analog signal and the integrator output. The comparator output reflects the sign of the difference between the input voltage and the integrator output. That sign bit is the digital output and controls the direction of ramp in the integrator. The comparator is clocked so as to produce a synchronous and band limited digital bit stream.

If the clocked serial bit stream is transmitted to a similar integrator at a remote point, the remote integrator output is a copy of the transmitting control loop integrator output. To the extent that the integrator at the transmitting location tracks the input signal, the remote receiver reconstructs the input signal. Low pass filtering at the receiver output will eliminate most of the quantizing noise if the clock rate of a the bit stream is an octave or more above the bandwidth of the input signal. Voice bandwidth is 4 kHz and clock rates of 8 kHz and up are possible. Thus, the delta modulator digitizes and transmits the analog input to a remote receiver. The serial, unframed nature of the data is ideal for communications networks. With no input at the transmitter, a continuous one zero alternation is transmitted. If the two integrators are made leaky, then during any loss of contact the receiver output decays to zero and receive restart begins

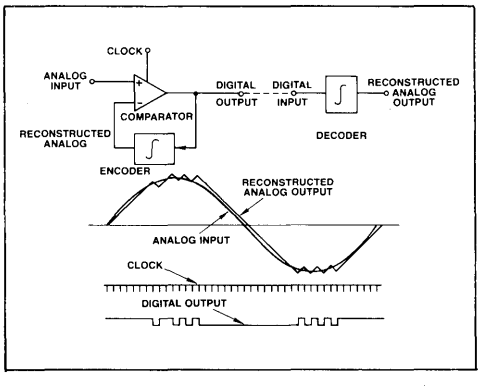


FIGURE 1 — SIMPLE DELTA MODULATION
An Analog Input Signal Can Be Digitalized and Transmitted by Synthesizing a Minimum Error Set of Voltage Ramps. The Comparator Clock Establishes the Channel Bandwidth.

without framing when the receiver reacquires. Similarly, a delta modulator is tolerant of sporatic bit errors.

The fundamental advantages of the delta modulator are its simplicity and the serial format of its output. Its limitations are its ability to accurately convert the input within a limited digital bit rate. The analog input must be frequency limited and amplitude limited. The frequency limitations are governed by the Nyquist rate while the amplitude capabilities are set by the gain of the integrator. For a given signal level, one specific gain will achieve an optimum noise level. Unfortunately, the basic delta modulator has a small dynamic range over which the noise level is constant.

THE COMPANDING ALGORITHM

The continuously variable slope circuitry provides increased dynamic range by adjusting the gain of the integrator. For a given clock frequency and input bandwidth, the additional circuitry increases the delta modulator's dynamic range. A block diagram of a complete CVSD codec is shown in Figure 2. A new bipolar/I^2L integrated circuit has been built to provide all of the active elements. External to the basic delta modulator is an algorithm which monitors the past few outputs of the delta modulator in a simple shift register. The register is 3 or 4 bits long depending on the application. The CVSD algorithm simply monitors the contents of shift register and indicates if it contains all ones or zeros. This condition is called a coincidence. When it occurs, it indicates that the gain of the integrator is too small. The coincidence output drives a low pass filter. The voltage output of this syllabic filter controls the integrator gain through a V to I converter and a slope polarity switch whose other input is the sign bit or the up/down control of the delta modulator.

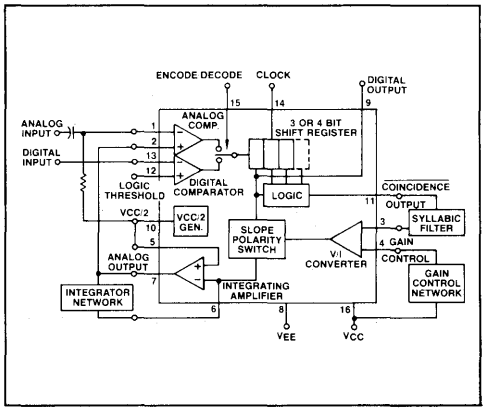


FIGURE 2 – CVSD BLOCK DIAGRAM
A Delta Modulator Is Enclosed in a Digitally Controlled Gain Loop and Composes a Continuously Variable Slope Delta Modulator. A Bipolar/I^2L Integrated Circuit Has Been Designed to Provide All the Active Circuitry Required.

The simplicity of the all ones, all zeros algorithm should not be taken lightly. Many other control algorithms using the shift register have been tried. The key to the accepted algorithm is that it provides a measure of the average power or level of the input signal. Other schemes provide more instantaneous information about the shape of the input curve. The purpose of the algorithm is to control the gain of the integrator and to increase the dynamic range. Thus, a measure of the average input level is needed. By monitoring both the coincidence of ones and zeros, the shift register performs a function similar to a full wave bridge rectifier.

The algorithm is repeated in the receiver and thus the level data is recoverable at the receiver. Because the algorithm only operates on the past serial data, it changes the nature of the bit stream without changing the channel bit rate. The bit stream in the channel is as if it were from a standard delta modulator with a constant level input.

SYLLABIC AND INTEGRATION FILTER PROPERTIES

The circuit in Figure 3 is the most basic CVSD circuit possible. For many intelligible voice channel applications, it is adequate. In this circuit, both the syllabic filter and the integration filter are composed of single-pole networks.

The integration network is chosen to meet two simple constraints. First, it must be an integrator throughout the voice band and second, it must be leaky so that bit errors can be tolerated and loss of receiver contact does not require an external reset for reacquisition. C_I 5.1 μF and $R_I = 10$ k produce a 159 Hz break/frequency and a lossy network.

The selection of the syllabic filter components illustrates an interesting property of the codec. The operation of the simple delta modulator may be investigated by deriving its S plane transfer function. The comparator is modeled with a unit limiter and a summer. The unit limiter has a describing function in S if the system is analyzed for sinusoidal inputs of the form e sin wt, that is

$$\text{Digital Output} = \frac{4A}{\pi e} \text{ e sin wt where A is the peak voltage of the unit limiter.}$$

It is obviously a non-linear element since the transfer function is dependent on the magnitude of the input signal.

The integration filter has a straightforward transfer function description:

$$\frac{\text{Analog } V_{out}}{\text{Digital } V_{out}} = \frac{Rx}{C_I(S + 1/R_I C_I)}$$

where Rx is connected from the comparator output to the integrator input and sets the gain of the simple delta modulator.

The closed loop delta modulator model is then

$$\frac{\text{Analog Vout}}{\text{e sin wt}} = \frac{1}{1 + \dfrac{4ARx}{e\, C_I\, (S + 1/R_I C_I)}}$$

Note that the response of the codec is a function of the magnitude of the input level. Closed loop CVSD systems can be analyzed for steady state inputs by substituting the syllabic filter voltage which corresponds to an applied e for A. Thus, the gain of the delta modulator is varied to accommodate the applied input level.

For a CVSD circuit to perform as an adjusted delta modulator, the model equation indicates that A ∝ e must be nearly constant. The syllabic filter time constant must be large compared to the input frequency. For a maximum input frequency of 3300 Hz, the time constant must be much larger than the 0.3 ms. Thus 3 ms is the minimum allowed RC product for the syllabic filter in voice band applications. The syllabic nature of voice is responsible for the name "syllabic filter". A CVSD codec can only effectively transmit signals whose e varies at a frequency much lower than the fundamental frequency of the signal. Conveniently, voice, modem signals and DTMF signals have this syllabic property.

In Figure 3, a 6 ms time constant is used. In Figure 5, 3 ms charge and 9 ms discharge time constants are used to improve attack time without sacrificing constant A. Voice syllables tend to have this kind of shewed envelope.

CLOCK RATE AND SHIFT REGISTER LENGTH

The prime design constraint of a CVSD channel is the channel bit rate. Since delta modulator produces a serial unframed bit stream, the bit rate and sample frequency are the same. Obviously, as the clock rate increases so will the end to end performance. Clocks from 9600 kHz to 64 kHz can be used in various applications. 16 kHz, 32 kHz, and 37.7 kHz have the greatest acceptance in practical voice communication equipment.

After fixing the system bit rate, the shift register length selection must be made. The length of the shift register determines the amount of past history which will be taken into account in predicting slope. As the clock rate changes, so does the amount of signal time recorded by the shift register. Therefore, at rates below 16 kHz a three bit algorithm produces the best results. From 16 kilobits and up, either 3 or 4 bits may be used. Four bit algorithms provide flatter S/N performance because they account for a longer average past history of steady state signals. However, the transient response to level changes is slightly degraded because of the slower companding response.

The integrated circuit is produced with either 3 or 4 bit registers and is selected by laser link cutting rather than mask option. Depending on the results of the idle channel trim corrections, the die requiring the smallest step sizes is made into a 4 bit register.

LOOP GAIN CONSIDERATIONS

The feedback gain of the CVSD codec is set by the selection of Rx in Figure 3. After the clock rate, this gain is the most critical parameter of codec performance. Since the CVSD algorithm improves the dynamic range of the delta modulator for lower level inputs, the selection of loop gain should be based on the near maximum amplitude and frequency signal which must be transmitted. Experimental data shows that a CVSD codec produces optimum S/N ratio when the companding algorithm is active between 5% and 25% of the time. Taking this into account, the gain resistor Rx can be selected by determining the required integrator current which will produce the needed step size for a specified input signal. Then the resistor should source the required current when the syllabic filter output is about 25% of its maximum value.

The current required to move the integrator output a specific voltage from zero is simply

$$I_I = \frac{Vo}{R_I} + C_I \frac{dVo}{dt}$$

Now a 0 dBmo sine wave has a peak value of 1.0954 volts. In 1/8 of a cycle of the sine wave centered around the zero crossing the sine wave changes by approximately its peak value. The CVSD step should track that change. The required current for a 0 dBm 1 kHz sine wave is

$$I_I = \frac{1.1 \text{ volt}}{*2(10k)} + \frac{0.1\ \mu F\ 1.1}{0.125 \text{ ms}} = 0.935 \text{ mA}$$

*The maximum voltage across R_I when maximum slew is required is $\frac{1.1 \text{ V}}{2}$

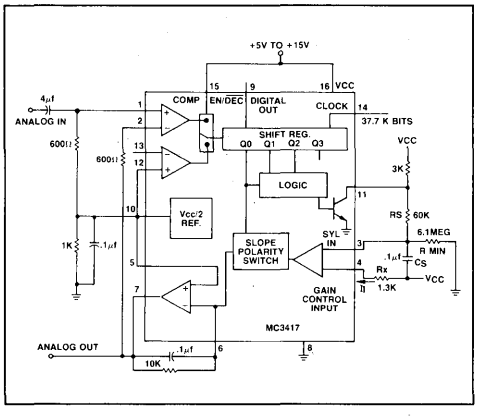


FIGURE 3 — BASIC CVSD ENCODER
Single Pole Integration and a Single Pole Syllabic Filter Are Sufficient for Many Voice Channel Applications. Selection of External Components Tailors the Integrated Circuit to the Application.

Now the voltage range of the syllabic filter is the power supply voltage, thus

$$Rx = 0.25(V_{CC}) \quad \frac{1}{0.935 \text{ mA}}$$

for a 5 volt supply Rx = 1.3 k

MINIMUM STEP SIZE

The final parameter to be determined for the simple encoder in Figure 3 is the minimum step size. With no input, the CVSD digital output becomes a one zero alternating pattern and the analog output becomes a small triangle wave. The peak to peak value of that triangle wave is the idle channel step size. Its meaning is analogous to the 1½ LSB quantization error of a conventional D to A converter. The codec

cannot resolve or transmit signal levels smaller than the minimum step size. In theory, one would wish to make this parameter go to zero. However, practical errors such as up and down ramp matching, comparator hysteresis, and filter op amp offsets combine to cause the idle channel analog output to drift away from the zero dc reference. The codec then produces two ones or two zeros in order to restore the level.

To set the idle channel step size, the value of R min must be selected. With no input signal, the slope control algorithm is inactive. A long series of ones or zeros never occurs. Thus, the voltage across the syllabic filter, the voltage divider of R_S and Rmin (see Figure 3) sets the minimum allowed voltage across the syllabic filter capacitor. That voltage divided by Rx must produce the desired ramps at the analog output. Again we write the integrator current equation

$$I_I = \frac{Vo}{R_I} + C_I \frac{dVo}{dt}. \text{ For small Vo } \frac{Vo}{R_I} \rightarrow 0.$$

$I_I = C_I \frac{\Delta Vo}{\Delta T}$ where ΔT is the clock period and ΔVo is the desired peak to peak value of the idle output.

Thus if Rx and R_S are known, R min may be calculated for any system. The design of Figure 3 is complete.

Figure 4 describes the performance of the codec in Figure 3 with two sets of curves. The codec was optimized around 0 dBm but the S/Nc ratio falls only 6 dB at −30 dBm. The low pass nature of the codec and the change of frequency response with input level is documented on the left of the figure.

S/N IMPROVEMENT USING TWO POLE INTEGRATION

One pole integration filters are not the only possibility. If a two pole integration network is used instead of the simple one pole, an S/N improvement can be realized. An encoder using such a network is shown in Figure 5. Adding a second pole in the transfer function of the integrator simply reduces the total noise bandwidth of the analog output without affecting the relevant voice energies. From another point of view, a 11110111 input to a single pole integrator produces a large ramp reversal at the 0 value since the 0 step will be in the opposite direction but equal in magnitude to the 1 ramp before and after it. Since the analog signal is band limited, it was obviously continuing to decrease at the 0 step and an error in tracking is encountered. If two pole integration is used, the 101 reversal is filtered and the 0 step is much smaller than the 1 step preceding it in the long string of ones. Thus the total error is less. A two pole filter can improve noise performance by 3 or more dB across the entire input level range.

The first pole is still placed below 300 Hz to provide the 1/S voice content curve and a second pole is placed somewhere above the 1 kHz frequency. For telephone circuits, the second pole can be placed at 1.8 kHz to exceed the 1633 DTMF frequency. The lower the second pole frequency, the greater the noise improvement. To ensure the encoder loop stability, a zero is added to keep the phase shift less than 180°. This zero should be placed slightly above the low pass output filter break frequency so as not to reduce the effectiveness of the second pole. A network of 244 Hz, 1.8 kHz and 5.3 kHz is used for telephone application in Figure 5 while 160 Hz, 1.2 kHz and 2.8 kHz might be used in voice only channels. The integration filter in Figure 5 has a transfer function of

$$\frac{V_{out}}{I_{in}} = \frac{R_0R_1\left(S+\frac{1}{R_1C_1}\right)}{R_2C_2(R_0+R_1)\left(S+\frac{1}{(R_0+R_1)C_1}\right)\left(S+\frac{1}{R_2C_2}\right)}$$

The selection of the two pole filter network affects the selection of the loop gain value and the minimum step size

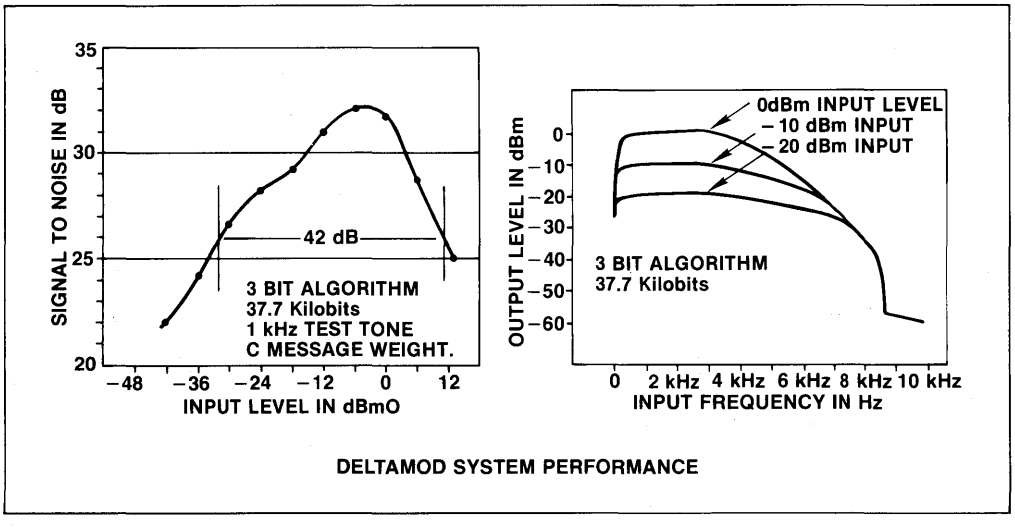


FIGURE 4 — SIGNAL TO NOISE PERFORMANCE AND FREQUENCY RESPONSE
Data Result From Testing the Circuit in Figure 3.

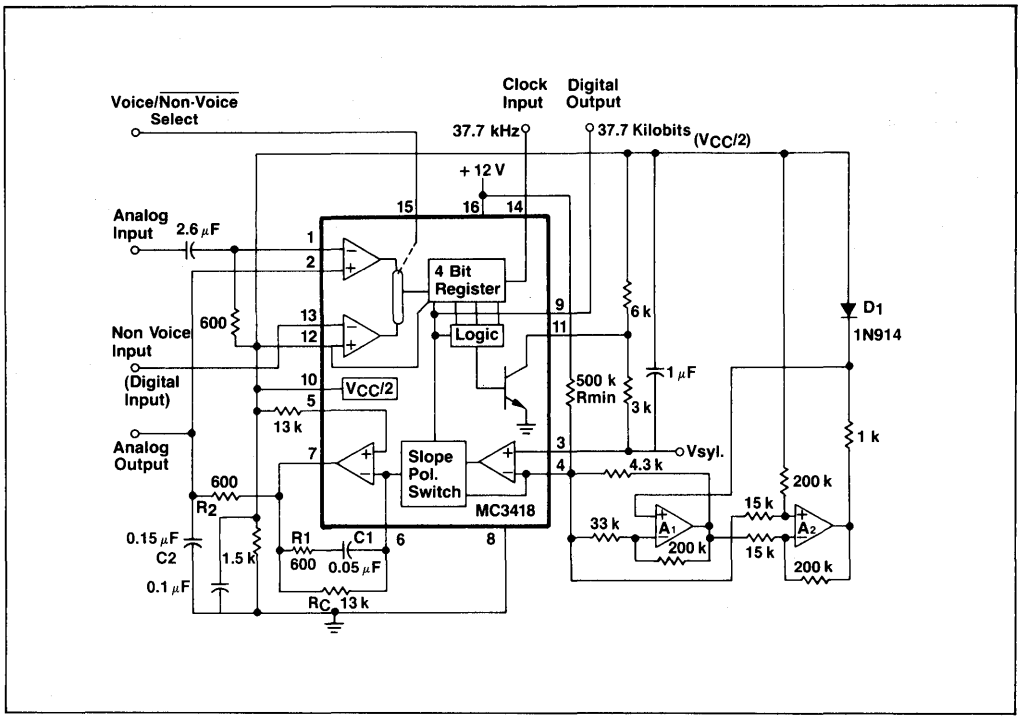


FIGURE 5 — TELEPHONE QUALITY DELTA MODULATOR CODER
Both Double Integration and Active Companding Control Are Used to Obtain Improved CVSD Performance. Laser Trimming of the Integrated Circuit Provides Reliable Idle Channel and Step Size Range Characteristics.

resistor. The required integrator current for a given change in voltage now becomes

$$I_{in} = \frac{V_{out}}{R_0} + \frac{R_2C_2}{R_0} + \frac{R_1C_1}{R_0} + C_1 \frac{\Delta V_{out}}{\Delta T} +$$

$$R_2C_2C_1 + \frac{R_1C_1R_2C_2}{R_0} \frac{\Delta V_{out2}}{\Delta T2}$$

The calculation of desired gain resistor Rx then proceeds exactly as previously described using this current equation.

SUBSCRIBER CARRIER TELEPHONE QUALITY CODEC USING MC3418

Two specifications of the integrated circuit are specifically intended to meet the performance requirements of commercial telephone systems. First, slope polarity switch current matching is laser trimmed to guarantee proper idle channel performance with 5 mV minimum step size and a typical 1% current match from 10 μA $\tau o \approx \mu\Delta$. Thus a 300 to 1 range of step size variation is possible. Second, the MC3418 provides the four bit algorithm currently used in subscriber loop telephone systems.

With these specifications and the circuit of Figure 5, a telephone quality codec can be mass produced.

The circuit in Figure 5 provides a 30 dB S/Nc ratio over 50 dB of dynamic range for a 1 kHz test tone at a 37.7 kilobit rate. At 37.7 kilobits, 40 voice channels may be multiplexed on a standard 1.544 megabit TI facility. This codec has also been tested for 10^{-7} error rates with asynchronous and synchronous data up to 2400 baud and for reliable performance with DTMF signaling. Thus, the design is applicable in telephone quality subscriber loop carrier systems, subscriber loop concentrators and small PABX installations.

THE ACTIVE COMPANDING NETWORK

The unique feature of the codec in Figure 5 is the step size control circuit which uses a companding ratio reference, the present step size, and the present syllabic filter output to establish the optimum companding ratios and step sizes for any given input level. The companding ratio of a CVSD codec is defined as the duty cycle of the coincidence output. It is the parameter measured by the syllabic filter and is the voltage across C_S divided by the voltage swing of the coincidence output. In Figure 5, the voltage swing of pin 11 is 6 volts. The operating companding ratio is analoged by the voltage between pin 10 and 4 by means of the virtual short across pin 3 and 4 of the V to I op amp within the integrated circuit. Thus, the instantaneous companding ratio of the codec is always available at the negative input of A1.

The diode D1 and the gain of A1 and A2 provide a companding ratio reference for any input level. If the output of A2 is more than 0.7 volts below $V_{CC}/2$, then the positive input of A1 is $(V_{CC}/2 - 0.7)$.

The on diode drop at the input of A1 represents a 12% companding ratio (12% = 0.7 V/6 V).

The present step size of the operating codec is directly related to the voltage across Rx which established the integrator current. In Figure 5, the voltage across Rx in a direction which reduces the difference between the companding reference and the operating ratio by changing the step size. The ratio of R4 and R3 determines how closely the voltage at pin 4 will be forced to 12%. The selection of R3 and R4 is initially experimental. However, the resulting companding control is dependent on Rx, R3, R4, and the full diode drop D1. These values are easy to reproduce from codec to codec.

For small input levels, the companding ratio reference becomes the output of A2 rather than the diode drop. The operating companding ratio on pin 4 is then compared to a companding ratio smaller than 12% which is determined by the voltage drop across Rx and the gain of A2 and A1. The gain of A2 is also experimentally determined but once determined, the circuitry is easily repeated.

With no input signal, the companding ratio at pin 4 goes to zero and the voltage across Rx goes to zero. The voltage at the output of A2 becomes zero since there is no drop across Rx. With no signal input, the actively controlled step size vanished.

The minimum step size is established by the 500 k resistor between V_{CC} and $V_{CC}/2$ and is, therefore, independently selectable.

The signal to noise results of the active companding network are shown in Figure 6. A smooth 2 dB drop is realized from +12 dBm to −24 under the control of A1. At −24 dbm, A2 begins to degenerate the companding reference and the resulting step size is reduced so as to extend the dynamic range of the codec by 20 dBm. The slope overload characteristic is also shown. The active companding network produces improved performance with frequency. The 0 dBm slope overload point is raised to 4.8 kHz because of the gain available in controlling the voltage across Rx. The curves demonstrate that the level linearity has been maintained or improved.

The codec in Figure 5 is designed specifically for 37.7 kilobit systems. However, the benefits of the active companding network are not limited to high bit rate systems. By modifying the crossover region (changing the gain of A2), the active technique may be used to improve the performance of lower bit rate systems.

The performance and repeatability of the codec in Figure 5 represents a significant step forward in the art and cost of CVSD codec designs.

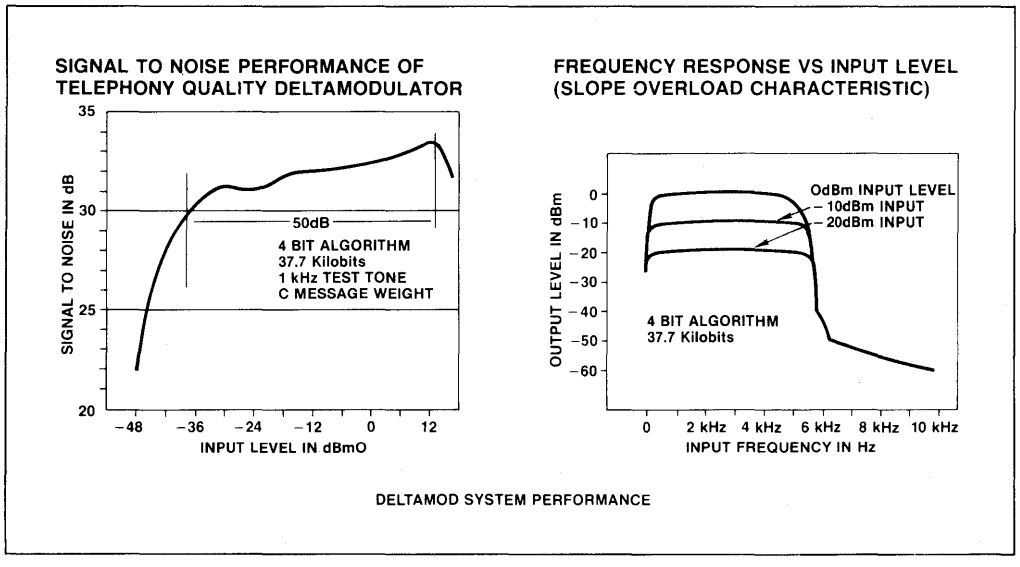


FIGURE 6 — SIGNAL TO NOISE PERFORMANCE AND FREQUENCY RESPONSE
Data Document the Improvement Realized with the Circuit in Figure 5.

Time-slot assigner chip cuts multiplexer parts count

by Henry Wurzburg
Motorola Inc., Semiconductor Group, Phoenix, Ariz.

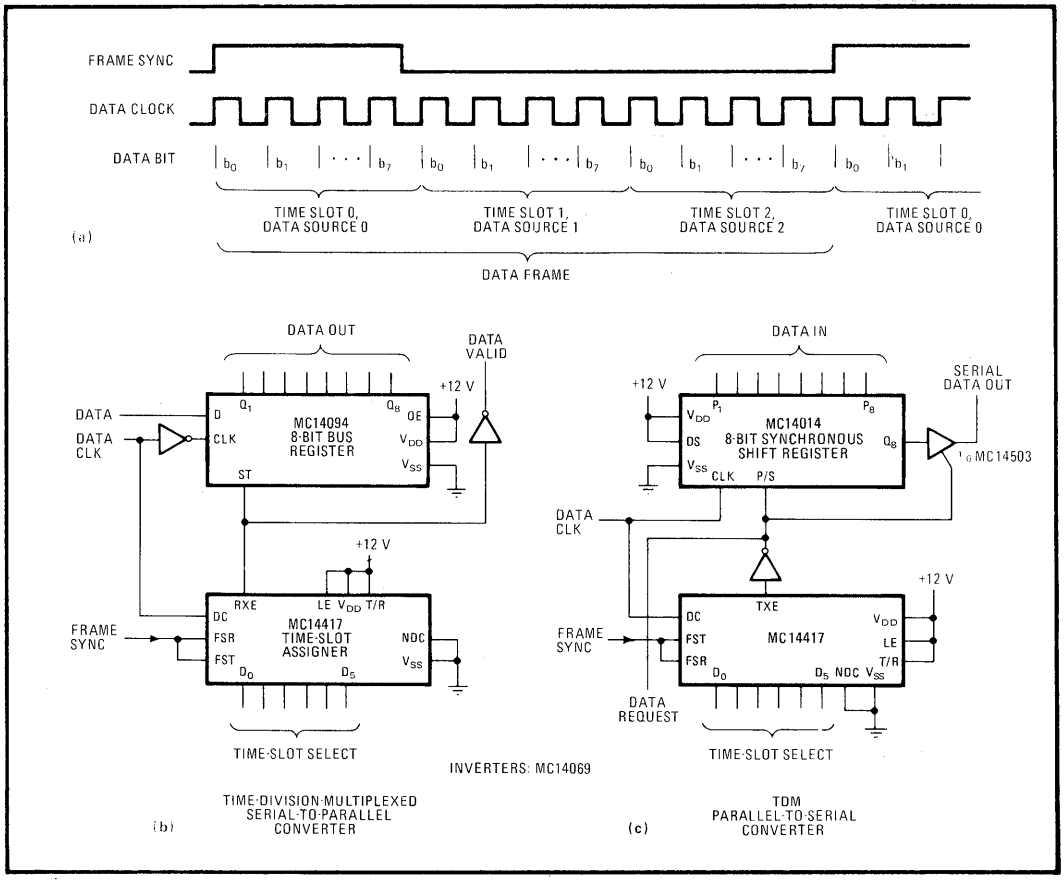
In some communications systems, particularly digital telephony equipment, it is hard to examine the data from a given source after it has been time-division-multiplexed with other data for serial transmission over a common data line. Capturing the data from its time slot and converting it into parallel form for examination usually requires many integrated circuits, since the slot must be programmable.

A special-purpose IC, the MC14417 time-slot assigner carries out this serial-to-parallel function with the aid of only a few inverters and one other IC. What's more, the cost of implementing the circuit is only a few dollars.

The timing of a simple three-slot TDM system is shown in (a). In digital telephone systems, a data frame may consist of anywhere from 24 to 40 time slots, each containing 8 bits of data transmitted at rates of up to 2.56 megabits per second.

In the all-complementary-MOS capture circuit of (b), the MC14094 shift register acts as a serial-to-parallel converter, while the 14417 computes when the data is to be captured and converted. Just which time slot it captures is determined by the binary data present at inputs D_0–D_5 of the 14417. The circuit also provides a valid-data output signal. As for speed, the circuit works for clock rates of up to 2.56 MHz with systems having up to 40 time slots.

Implementing a parallel-to-serial converter for multiplexing data onto the TDM data line is equally simple if the 14417 is used as shown in (c). Here, a three-state buffer prevents the serial data bus from being loaded during idle time-slot periods. The frequency limitations of this second circuit are the same as for the capture circuit. □



The right slot. Time-domain multiplexing (a) assigns to data from several sources specific time slots in a serial data stream. Capturing data from a specific slot is made easy with the MC14417 time-slot assigner (b), which works with the MC14094 shift register to provide data from the source dictated by the select inputs of the 14417. The versatile chip can also provide parallel-to-serial multiplexing (c).

MC14402 MONO-CIRCUIT APPLICATIONS INFORMATION

by
Richard L. Hall and Micheal D. Floyd
Telecom Systems Engineering

This application note is intended to ease customer evaluation of the Motorola MC14402 PCM mono-circuit, particularly when using the Motorola Mono-circuit Evaluation Board. Schematics and artwork of this board are given as well as layout guidelines for designing the mono-circuit into a custom PC board. Analog testing considerations are mentioned to help sidestep some of the troublesome aspects of codec/filter evaluations.

EVALUATION BOARD DESCRIPTION

The Motorola Mono-circuit Evaluation Board is a small PC board that contains all necessary clock circuitry for operating the MC14402. Coaxial connectors allow access to the analog input/output ports and the only other connections required are to the three power terminals—V_{DD}, V_{SS} and V_{AG}. The schematic for this board is shown in Figure 1 while the artwork is given in Figure 2.

The clock circuitry uses a 2.048 Mhz crystal to produce the 2.048 Mhz data clock as well as the 8 kHz sync signal. The 8 kHz sync is an 8-data-clock-wide pulse that is connected to the RCE, TDE and MSI inputs of the mono-circuit. RCE and TDE are the receive and transmit enables respectively, while MSI is the 8 kHz reference input. The 8 kHz sync is generated by the MC14417 TSAC (Time Slot Assigner Circuit).

Options are available to help evaluate different channel parameters. These include:

* 600 or 900 ohm channel impedance
* RSI peak overload voltage of 3.15 or 3.78 volts
* TTL or CMOS logic levels
* Transmit and Receive gain adjustment ($\overline{RxO}$ gain only)
* A or MU-law coding
* Power-down capability

These options are selected by solderable wire straps (S1-S6) as described in the Strapping Information Chart. The straps can be replaced by DIP switches if desired and can be obtained from:

Grayhill Inc.
561 Hillgrove Avenue
La Grange, Illinois 60525

P/N	Name	Qty
78J05	S1	1
78J02	S2,S3	2
78J01	S4-S6	3

Figure 3 shows the physical location of the strap points as well as the component layout. The solid lines indicate the normal strap positions as shipped from the factory which select Mu-law, 900 ohm, CMOS, 3.78 volts peak operation. The straps E1-E10 allow reprogramming of the clock lines to provide different clock schemes. Refer to the schematic in Figure 1 for changing these straps.

TEST CONSIDERATIONS

Input/Output Levels

Obtaining valid test data is highly dependent upon establishing the proper input/output voltage levels. However, this can be a somewhat confusing task since the mono-circuit can use three different peak overload voltages—2.5, 3.1 and 3.8 volts. The evaluation board permits selection of either 3.1 or 3.8 volts. For 3.1 volts, the proper input/output level for a 0 dBm0 test signal is +6 dBm/600 ohms (1.5455 volts rms). For 3.8 volts, 0 dBm0 corresponds to +6 dBm/900 ohms (1.893 volts rms). Usually, measurement levels are referenced

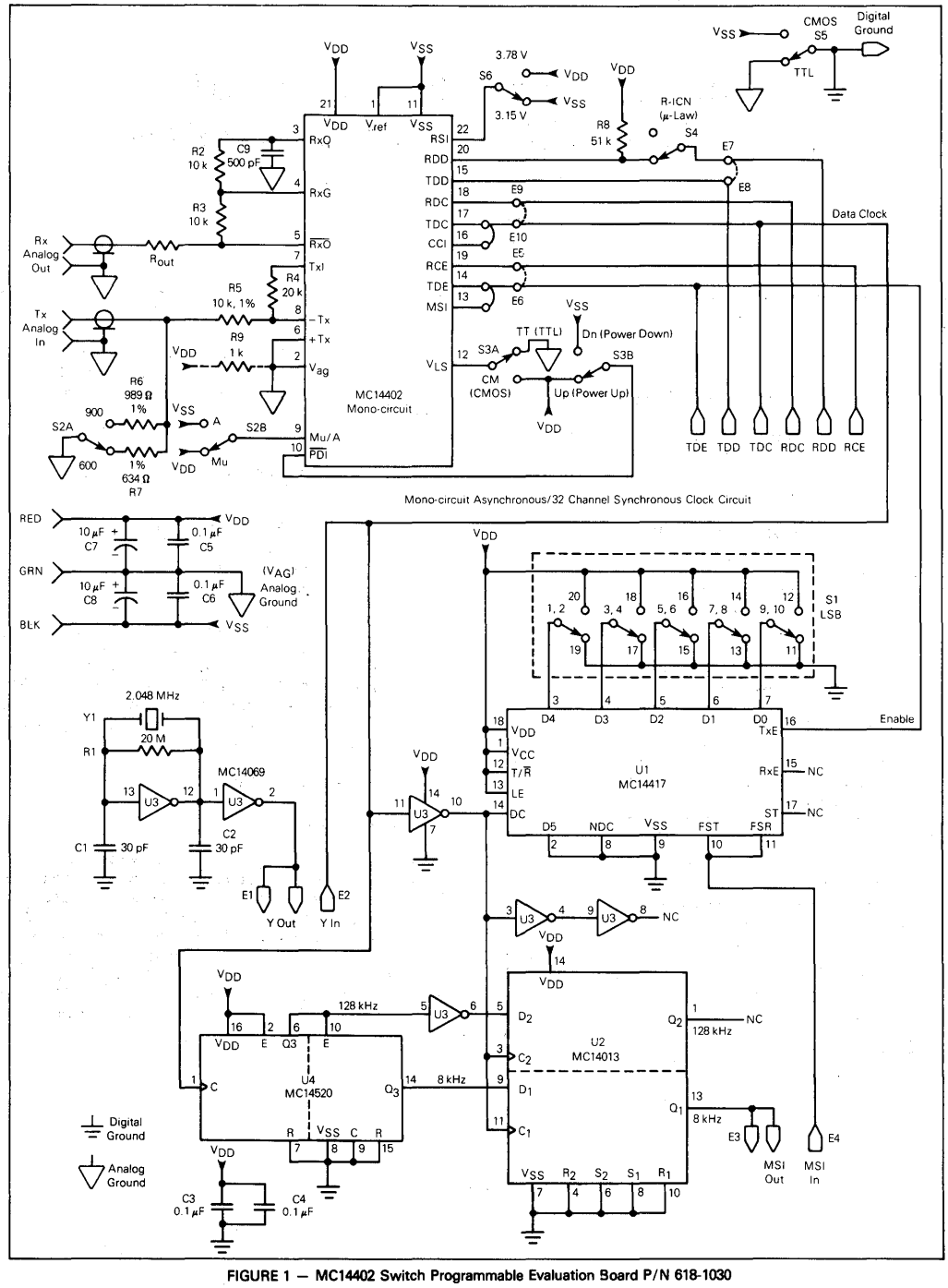


FIGURE 1 — MC14402 Switch Programmable Evaluation Board P/N 618-1030

to 0 dBm0 to avoid possible confusion over absolute levels. For example, an absolute idle noise measurement of 21 dBrnC becomes 15 dBrnC0 when referenced to 0 dBm0 (where 0 dBm0 = +6 dBm in our system).

Noise

Special care has been taken in the layout of the evaluation board to minimize noise corruption. The analog and digital sections are isolated from each other and bypassing is present to reduce high frequency noise. The use of shielded cable for analog test lines is recommended to prevent extraneous environmental noise pickup as well as the use of a power supply reasonably free of high frequency noise. A 500 pF capacitor has been put on the RxO output to bypass any radiated asynchronous noise that might be picked up at this node.

Test Equipment

There are many different pieces of telecommunications test gear on the market and most will be more than adequate for testing codec/filter parameters. However, the use of wideband measurement devices for such tests as quantizing distortion and gain tracking should be avoided since these parameters involve very low voltage levels that require a selective voltmeter function for accurate results. Also, attention should be given to correct selection of input/output parameters on programmable test gear such as the Hewlett-Packard 3779 PMA and others.

LAYOUT GUIDELINES FOR PC BOARDS

* Bypassing of both V_{DD} and V_{SS} to V_{AG} with 0.1 microfarad ceramic capacitors (or any other capacitors with good high frequency behavior) as close to the part as possible.
* Isolate analog lines from digital sections. The monocircuit pinout facilitates this by keeping digital and analog pins on opposite sides of the chip.
* Use gain-setting resistors in the range of 50 kΩ < R < 5 kΩ to avoid high impedance nodes in the analog section.
* If V_{LS} is tied to V_{AG} for TTL level selection, then this connection should be a short, direct, low inductance trace.
* In a dual supply environment, V_{DD} and V_{SS} should be connected before V_{AG} (ground).

3

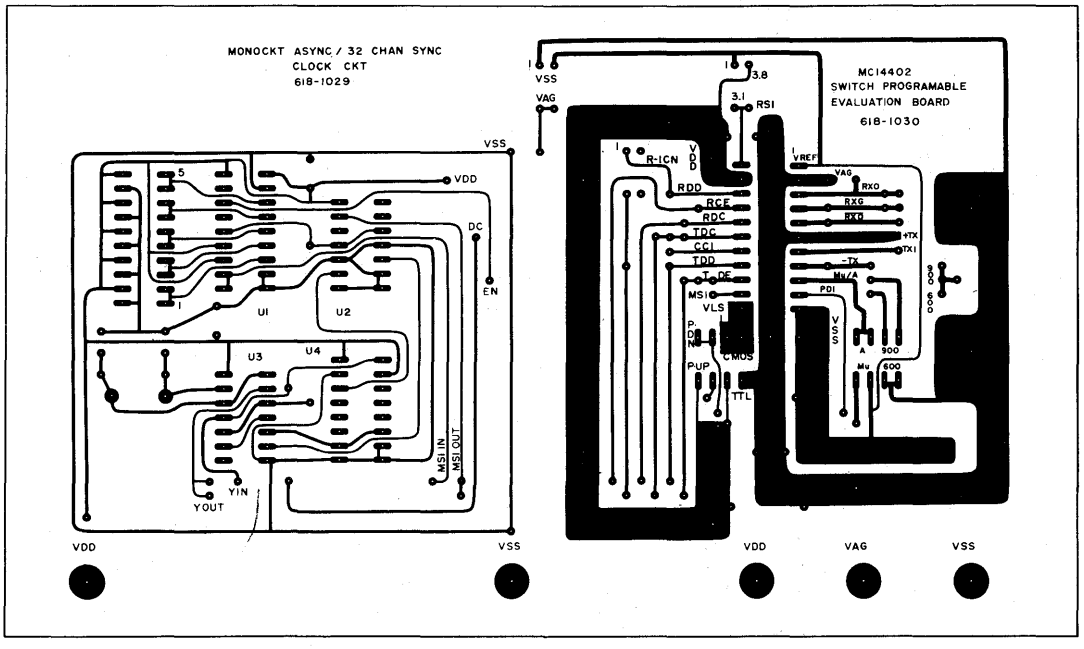
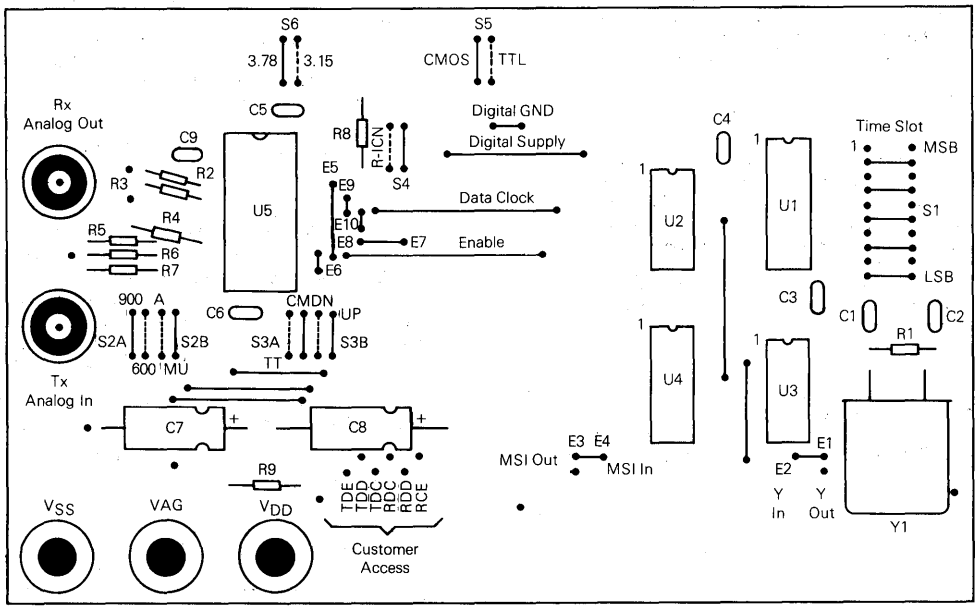


FIGURE 2 — Evaluation Board Artwork



NOTE: Solid line indicates normal strapping as shipped from factory; dashed lines indicate optional straps as described below in the Strapping Information Chart.

Reference Voltage (S6)	Reference Impedance (S2A)	Input/Output Levels (dBm)	R2	R3	R4	R5	R_{out}*
3.15 V	600 Ω	+6/+6	–	–	10 k	10 k	Jumper
		+6/0	–	–	10 k	10 k	600 Ω
		0/0	–	–	20 k	10 k	600 Ω
	900 Ω	0/0	16.6 k	10 k	16.6 k	10 k	Jumper
3.78 V	900 Ω	+6/+6	–	–	10 k	10 k	Jumper
		+6/0	–	–	10 k	10 k	900 Ω
		0/0	–	–	20 k	10 k	900 Ω
	600 Ω	0/0	12.5 k	10 k	25 k	10 k	600 Ω

* R_{out} is located between Rx analog out and $\overline{RxO}$ output underneath the board.

FIGURE 3 — Component Layout

Strapping Information Chart

S1 These straps select via U1 (MC14417 TSAC) one of 32 possible time slots in the 8 kHz frame. When used in conjunction with another board, performance in different time slots can be evaluated. (that is TDE ≠ RCE).

S2A Selects 600 or 900 ohm input impedance.

S2B Selects A or Mu-law coding.

S3A Selects either TTL(TT) or CMOS(CM) logic levels. The TTL levels swing from V_{DD} and V_{AG}; CMOS levels swing from V_{DD} to V_{SS}.

S3B Powers device up or down. DN = Powered down and UP = Powered up.

S4 Normally loops RDD to TDD. When R-ICN is strapped, Mu-law receive idle channel noise can be measured (RDD = 1 111 1111).

S5 Controls digital ground of clock logic. When CMOS is strapped, digital ground = V_{SS}; when TTL is strapped, digital ground = V_{AG}. Note that this strap must agree with the selection on S3A.

S6 Selects either 3.78 or 3.15 volts peak overload voltage.

R2,R3 Adjusts RxO output level where gain = – R3/R2 (optional).

R4,R5 Adjusts Tx Analog In level where gain = – R4/R5.

R9 A 1 kilohm pullup resistor is needed when V_{AG} output is used by itself to provide ground return for RxO or $\overline{RxO}$. If V_{AG} is tied to system power ground, this resistor can be deleted.

R_{out} Determines output impedance.

APPENDIX

A DB By Any Other Name. . .

The following is a brief discussion of decibels and how they are used in the telephone industry in an attempt to lessen the notorious confusion this term can create.

Engineers are very familiar with the equation definition of a decibel which is:

$$\text{Decibels} = \text{dB} = 20 \log \frac{V2}{V1} \qquad (1)$$

or its corollary:

$$\text{dB} = 10 \log \frac{P2}{P1}. \qquad (2)$$

The use of the logarithmic function eases the use of the large range of voltage numbers encountered in the telephone industry. A decibel is only a relative term; it defines the difference between two absolute voltage levels.

Which now brings us to the absolute decibel—the dBm (decibel milliwatt). A dBm is equivalent to a milliwatt of power delivered into a reference impedance—usually 600 ohms. An equation commonly used to calculate dBm levels can be derived from equation (2):

$$\begin{aligned} \text{dBm} &= 10 \log (P2/P_{ref}) \\ &= 10 \log (P2/0.001\ \text{W}) \\ &= 10 \log 1000\ (P2) \\ &= 10 \log \frac{1000\ (\text{Vrms}^2)}{600\ \text{ohm}} \end{aligned}$$

where reference impedance = 600 ohms.

For example, to calculate the peak-to-peak voltage of a 0 dBm sinusoidal signal:

$$\begin{aligned} 0 &= 10 \log \frac{1000\ (\text{Vrms}^2)}{600} \\ 10^0 &= (5/3)\text{Vrms}^2 \\ \text{Vrms}^2 &= 0.6 \\ \text{Vrms} &= 0.7746 \\ \text{Vp-p} &= 2(2)^{1/2}\text{Vrms} \\ &= 2.191 \text{ volts peak-to-peak.} \end{aligned}$$

In order to understand the proper level at a certain point in a system, the term dBm0 is used for reference. A dBm0 defines the nominal signal level at a test point node. Absolute levels can then be referred to in dBm0 for comparison to the nominal level. For example, suppose that at a certain point in a system 0 dBm0 = +6 dBm/600 ohms. Then a −20 dBm signal would be equal to −20−(+6) = −26 dBm0. Therefore, a −20 dBm signal would be 26 dB down from the nominal level.

Noise measurements require a different decibel unit as they usually involve some bandwidth or filtering constraint. One such unit commonly used (especially in North America) is dBrn or decibels above reference noise. The reference noise level is defined as one picowatt into 600 ohms or −90 dBm. Telephone measurements typically refer to dBrnC which is the noise level measured through a C-message weighting filter (a filter that simulates the response of the human ear). European systems use a related term called dBmp which is the dBm level noise measured through a psophometric filter. Both dBrnC and dBmp can be referenced to 0 dBm0 by adding a zero—dBrnC0 and dBm0p. Two examples are shown below to illustrate the use of these units:

1) 0 dBm0 = +6 dBm/600 ohms
   Noise measurement = 20 dBrnC
   = 14 dBrnC0

2) 0 dBm0 = +9 dBm/600 ohms
   Noise measurement = −70 dBmp
   = −79 dBm0p.

Understanding these units should help avoid any possible correlation problems between measurements and published specifications.

Telecomm ICs create low-cost phone links 4 miles long

Although the maximum recommended length for communications links over uncompensated 24 AWG twisted-pair wires is 4000 ft, a few off-the-shelf integrated circuits, when configured as a line driver, will drive a communications link with a maximum length of over 4 miles. The bandwidth of over 3000 Hz is adequate for remote control, sensing, and even private-telephone voice communications.

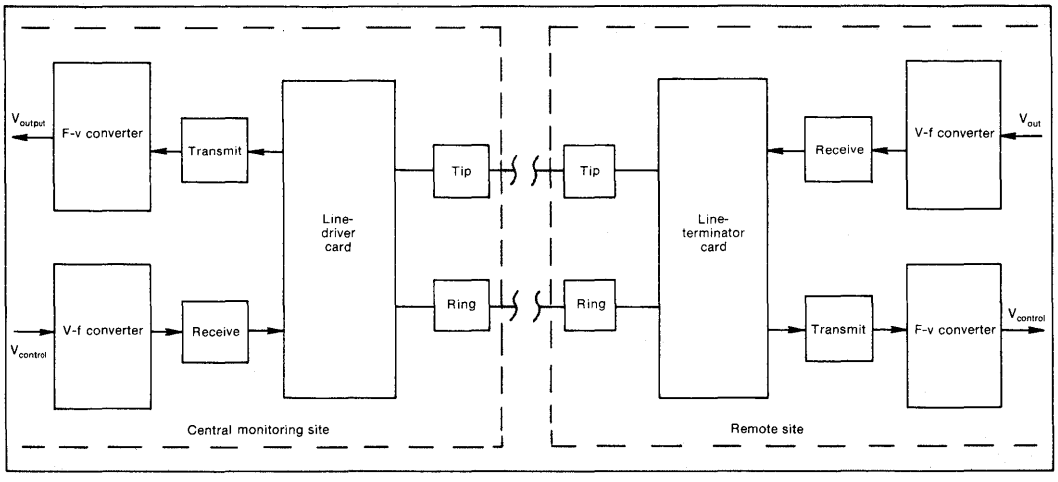
Any subscriber-loop interface circuit (SLIC) can be used to drive the line. In Fig. 1, a SLIC interfaces with voltage-to-frequency and frequency-to-voltage converters and a line terminator. Thus a dc voltage related to a process at a remote site can be measured from a central location and a corrective dc voltage can be sent in the reverse direction to adjust or control the process.

A variety of ICs can be interfaced with the basic driver for signaling or for data or voice transmission. Analog-to-digital and digital-to-analog converters—such as codecs and CVSDs (continuously variable-slope delta modulators used for voice companding)—perform the front-end data conversion for a low-cost computer link. A variety of dual-tone multifrequency (DTMF) encoders and decoders facilitate simple signaling over privately owned twisted pairs.

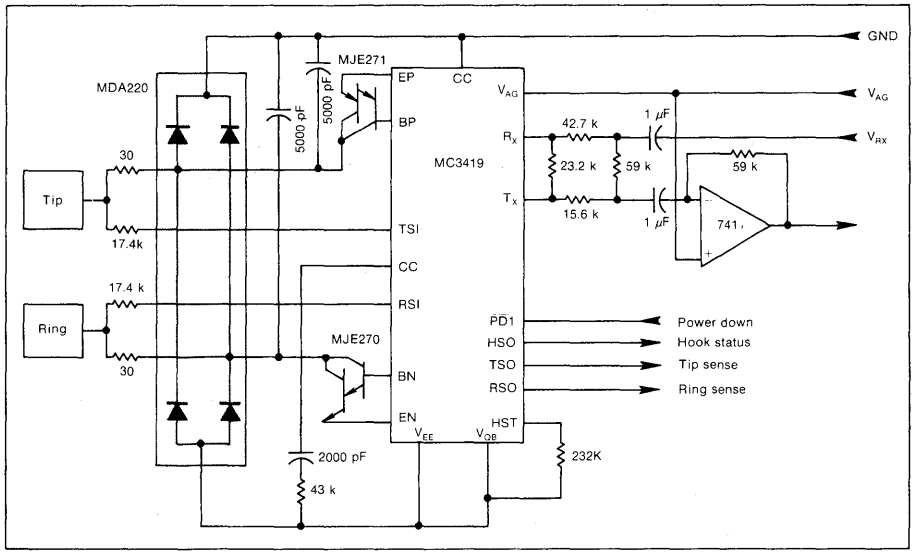
A line-driver card exemplifies the simple hardware configuration required (Fig. 2). The SLIC uses two Darlington pairs as pass transistors to handle currents of up to 120 mA. Changing the value of the 59-kΩ resistor used in the feedback path of the 741 operational amplifier will adjust the transmission output gain. The MDA220 rectifier bridge protects the circuit against lightning damage.

The line-terminator card converts a bidirectional two-wire line into two pairs of unidirectional lines, one transmit and one receive, and then amplifies the received and transmitted signals. A simple terminator can be made with the hybrid transformer and two varistors from a telephone handset. Even if a more sophisticated terminator card were built using a speech-network IC, the cost of the entire system would be less than the cost of the modems, PBX lines, or rf transceivers used for short-range, private communication links.

John Hines, Design Engineer, Motorola Inc., Bipolar Integrated Circuits Group, Linear IC Division, 5005 E. McDowell Rd., Phoenix, Ariz. 85008.



1. The maximum range of an RS-232 or RS-422 communications link can be extended to over 4 miles of uncompensated 24 AWG wires by a line-driver card based on a single-chip subscriber-loop interface circuit.



2. A line-driver card requires a SLIC, two Darlington pairs, a rectifier bridge for lightning protection, and an operational amplifier. A resistor in the op amp's feedback path adjusts the transmission output gain.

MOTOROLA

CMOS LSI INTEGRATION ENHANCES VOICE AND DATA NETWORKS

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3

INTRODUCTION

Digital Voice and Data PBXs are well accepted today as a viable communication networking solution. This type of PBX has proven to be a complete and cost effective interconnect approach toward automating the office environment.

A typical Digital Voice and Data PBX, as shown in Figure 1, can appreciate a variety of interconnect functions. Besides supporting the standard analog voice service, the PBX provides an inexpensive means for interconnecting word processors, CRT terminals, gateways to Local Area Networks (LAN) and other office equipment. The cost effectiveness of this approach is desirable because of the low connect cost and the use of twisted pair wire in lieu of coaxial or fiber optic cable.

The feasibility of the Voice and Data PBX is made possible from the development of cost effective LSI semiconductors that allow high speed data transmission over twisted pair wire. These ICs, like Motorola's Universal Digital Loop Transceivers (UDLT) allow simultaneous transmission of the 64 kbps PCM data, as well as signalling and user data between the digital phone and the PBX. With this capability, full featured digital phones and workstations, where voice and user data can simultaneously be transmitted over the existing twisted telephone wire, are made possible.

This paper will discuss Motorola's Universal Digital Loop Transceiver (UDLT) family of LSI semiconductors, that offer a cost effective approach to integrating a Voice and Data PBX.

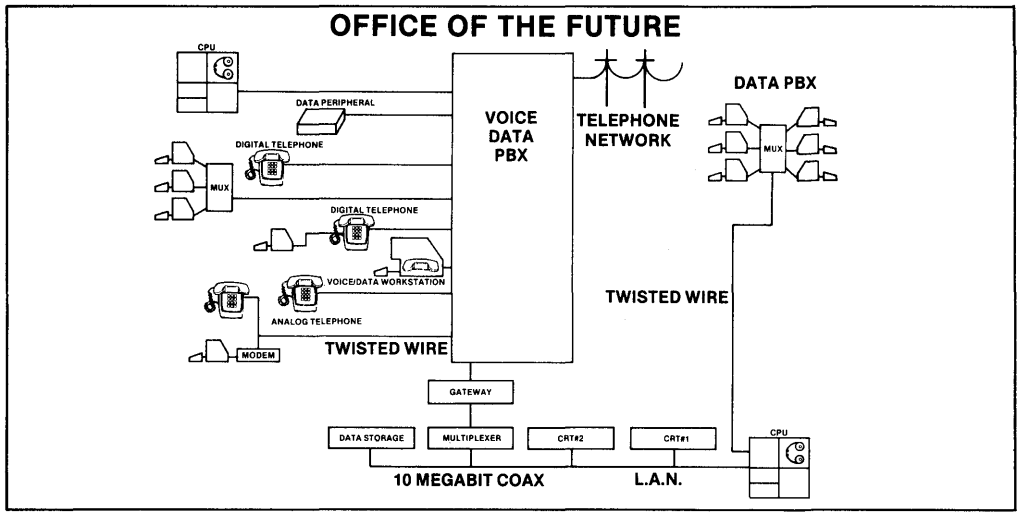

FIGURE 1

DESCRIPTION OF A VOICE AND DATA PBX

Most digital PBXs manufactured today offer the option of analog line cards, for voice services, and digital line cards, for voice and data services. This type of architecture, as shown in Figure 2, uses an interchangable back-plane compatible to both types of line cards. The interchangable back-plane allows the PBX to be structured for many combinations of analog or digital voice/data line cards.

The analog line card contains the traditional functions. For example, it includes the Time Slot Assignment Circuit (TSAC) used for logic supervision, the PCM codec/filter (mono-circuit) used for voice coding and decoding and the Subscriber Loop Interface Circuit (SLIC) used to perform the 2 to 4 wire conversion. Also, battery feed, secondary-lighting protection, line fault protection, and signal-balancing functions are included. The back-plane for the analog line card interfaces to the PCM highway and the supervision control lines.

On the digital line card, the PCM mono-circuit and SLIC have been replaced with the Master UDLT. The analog voice coding and decoding is now performed by the mono-circuit in the phone. The 64 kbps PCM data and the user data are transmitted between the Master and Slave UDLTs at a full duplex data rate of 80 kbps over the twisted wire. Due to the UDLT's unique modulation technique, data can be reliably transmitted over standard twisted wire up to 2 km with no external filtering or compensation circuitry. The Master UDLT performs the same back-plane I/O functions as the PCM mono-circuit. This allows interchanging of the analog and digital line cards in the PBX.

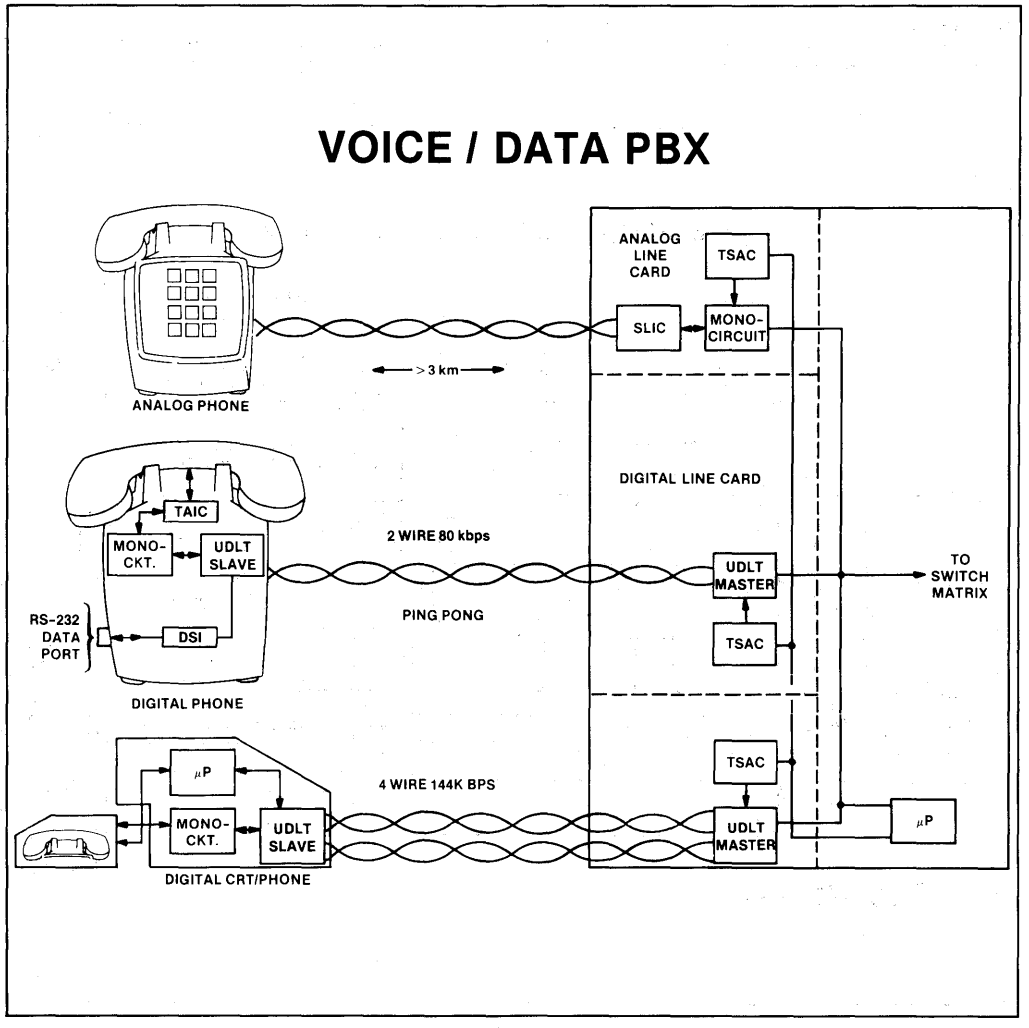

FIGURE 2

PCM MONO-CIRCUITS

Motorola's family of PCM mono-circuits incorporates the codec, filter and voltage reference functions into a single IC package. These devices perform the voice digitizing and recovery, as well as the band limiting and signal restoration necessary in PCM systems. The mono-circuits are tailored for a variety of PBX architectures. The family consists of five different device types. The MC14400, MC14403 and MC14405 are in a 16 pin package. The MC14401 is in a 18 pin package, and the MC14402 is in a 22 pin package. Figure 3 shows the functional block diagrams that make up all the mono-circuits. They are the transmit and receive filters, the DAC decoding/encoding logic, the on board selectable voltage reference and the transmit and receive digital I/O logic. Some basic features are:

- Low power CMOS technology
- Single or split power supplies
- Power supply operation at 6 to 13 volts
- On-board selectable voltage reference 2.5, 3.1 or 3.8 volts
- Data clock from 64 kHz to 3 MHz
- CMOS or TTL I/O interface
- High output drive capability—12 dBm into 600 ohms
- 16, 18, and 22 pin package options
- A-law CCITT, MU225-law D3 and MU255-law sign magnitude selectable
- 28 pin leadless chip carrier package
- No external components

The PCM mono-circuit family offers options suited for both line card and digital phone applications.

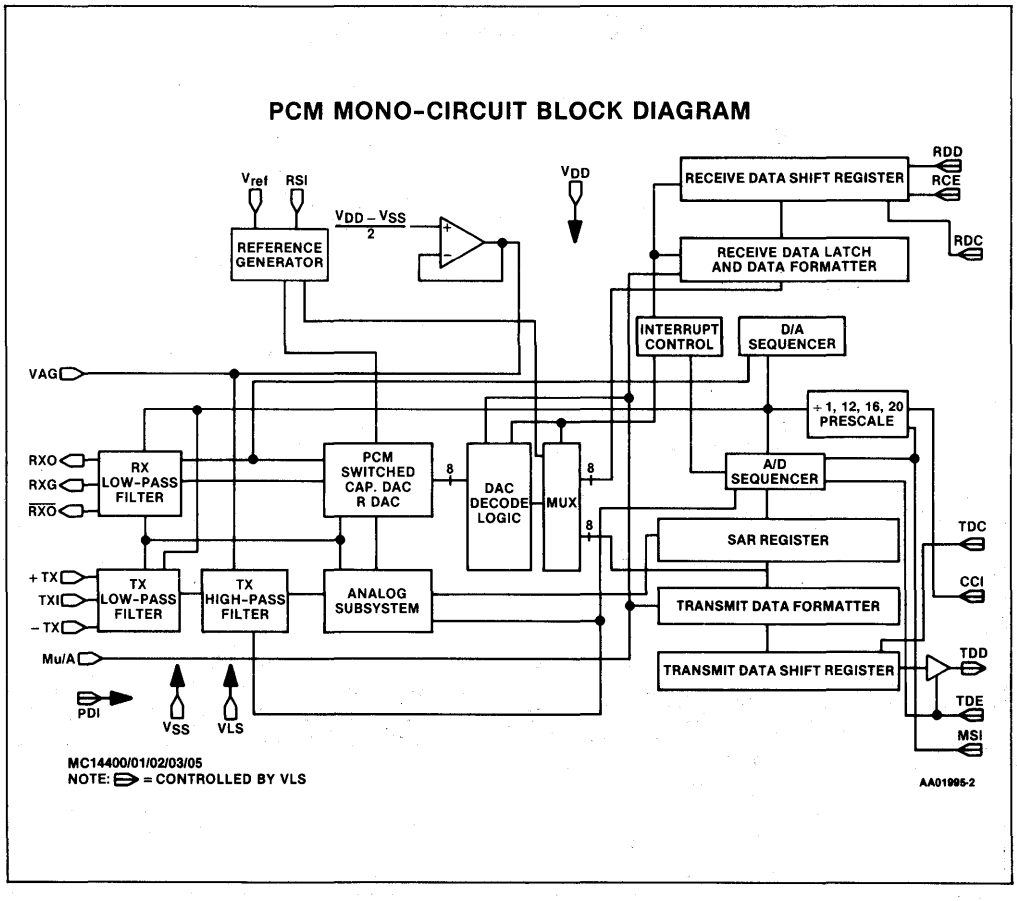

FIGURE 3

TIME SLOT ASSIGNER CIRCUIT (TSAC)

Motorola has three different per-channel TSAC ICs. The MC14418 is the full featured TSAC in a 22-pin package. In addition to performing all the supervision and control functions required in a single-party telephone line circuit, it performs the variable time slot assignment required in many digital switching applications.

The TSAC can be programmed for up to 64 8-bit time slots through a serial microprocessor port. It also has three additional MPU-programmed control bits that can be used for ring enable, power down, receive data/tone or other control and supervision functions. A reset pin is used, in conjunction with the ring enable, to perform the ring trip function. The unique addressing capability allows the use of a completely parallel back-plane for PCM codec/filter-based equipment. This scheme simplifies back-plane wiring and assembly of the channel group.

The MC14417 has the same core as the MC14418 but does not use the MPU port feature. Time slot data inputs are directed through an 8-bit parallel port. The data may be either hard wired on the printed circuit or parallel loaded by a processor using the Latch Enable function.

The MC14416 is also a subset of the MC14418. It performs the time slot assignment function using the serial MPU port, but it lacks the simplified addressing and line circuit control capabilities of the MC14418.

MASTER AND SLAVE UDLT

The MC145422 Master and MC145426 Slave UDLTs are high-speed transceivers intended to provide 80 kbps duplexed data communication over 26 AWG and larger twisted pair cable up to 2 kilometers in distance. The UDLTs allow the remoting of the mono-circuit in a digital telephone set and enable each set to have high speed data access to the PBX switching facility. In effect, the UDLTs allow each PBX subscriber direct access to the inherent 64 kbps data routing capabilities of the PBX.

The UDLT provides a means for transmitting and receiving 64 kbps of voice data and 16 kbps of signaling data. The Master UDLT replaces the codec/filter and SLIC on the PBX line card, and it transmits and receives data over the wire pair to the telset. The Master UDLT, as shown in Figure 4, appears to the line card and backplane as if it were a PCM codec/filter and has almost the same digital interface features as the MC14400 series mono-circuits. The Slave UDLT, shown in Figure 5, is located in the telset. It interfaces the mono-circuit to the twisted wire pair. The Master/Slave UDLTs operate in a frame synchronous manner, sync being established at the Slave by the timing of the Master's transmission each frame over the twisted pairs to the Slave. The Master's sync is derived from the PBX frame sync.

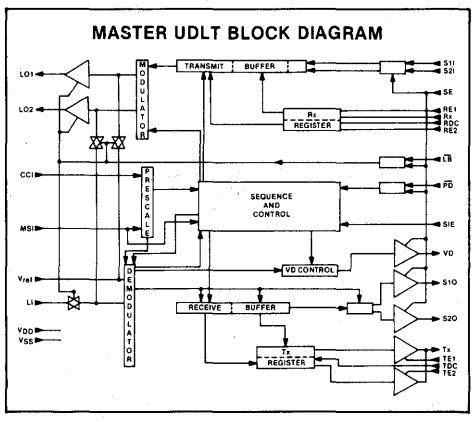

FIGURE 4

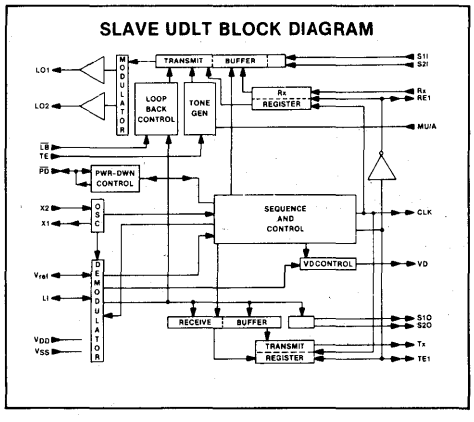

FIGURE 5

The UDLT utilizes a "ping pong" transmission technique, as shown in Figure 6. Ten bits (eight bits of PCM data and two bits of signaling data) are sent in a 256 kilobaud burst from the Master UDLT every frame or 125 μs. The Slave UDLT receives this burst and, after a short line settling interval, returns at 256 kilobaud, 10 bit burst of data to the Master UDLT. With this transmission scheme, the maximum loop length is determined by the cable delay time, number of bits in each burst, and the burst baud rate. This results in a maximum loop length of 2 km.

The UDLT uses a modified DPSK (MDPSK) modulation technique, resulting in a triangular waveform, as shown in Figure 6. This waveform results in a lower spectral content, thus low EMI and RFI radiation. The MDPSK waveform is very similar to FSK, except that the burst always begins with a 256 kHz half cycle which identifies the burst boundaries. Each baud period has no net dc bias. This eliminates any dc balancing bit requirement. Furthermore, auto equalization for phase dispersion is not required.

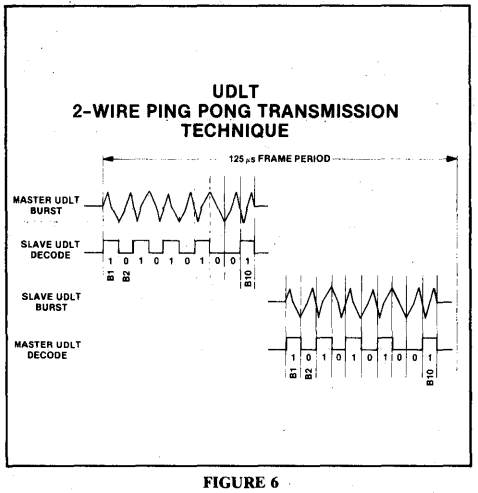

FIGURE 6

A feature of the Master UDLT allows one of two signal bits to and from the Slave to be inserted and extracted from the PCM word. This feature allows simultaneous voice and data transmission through the PBX. All UDLTs have a loopback feature by which the device can be tested in the user system.

The Slave UDLT has the additional feature of providing a 500 Hz MU or A law coded square wave to the mono-circuit when the TE pin is brought high. This feature is used to provide audio feedback in the telset during keyboard depressions.

The devices employ CMOS technology in order to take advantage of its reliable low-power operation and a proven capability for complex analog/digital LSI functions.

DATA SET INTERFACE (DSI)

The MC145428 Data Set Interface circuit, as shown in Figure 7, provides the asynchronous to synchronous data conversion to the UDLT, as well as the synchronous to asynchronous data convertion from the UDLT. The DSI IC is ideally suited to provide an interface between a RS-232 port and the UDLT. The DSI IC has an on-board baud rate generator with 7 selectable baud rates ranging from 300 to 38.4 kbps. An external baud rate generator can be used for a clock range from dc to 128 kbps. Another feature of the DSI IC is its ability to optimize the data length by stripping off the start and stop bits before being transmitted as a synchronous word. Likewise, the DSI will add the start and stop bits back to the incoming synchronous word.

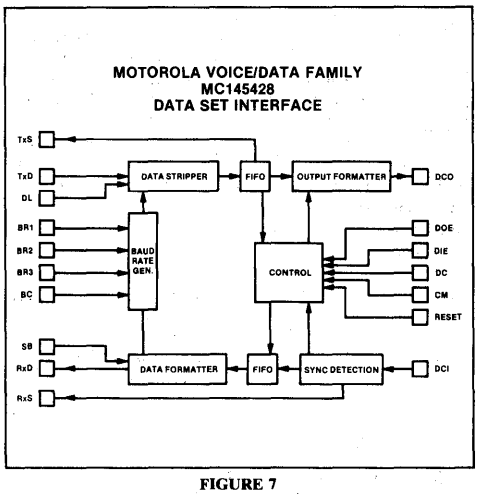

FIGURE 7

The MC145428 was designed in Si-gate CMOS technology and utilized in a 20 pin package. This IC will lend itself to a variety of data communication applications.

TELSET AUDIO INTERFACE CIRCUIT (TAIC)

The MC145429 Telset Audio Interface Circuit, as illustrated in Figure 8, enhances the digital phone by giving the microcomputer control of the analog signals between the PCM mono-circuit and the telset mouthpiece, earpiece, ringer/speaker, and auxiliary input/output.

The configuration of the device is programmed via a serial digital data port. Features of the MC145429 include:

- Independent adjustment of earpiece, speaker, and ringer volume
- 20 dB mouthpiece signal gain
- Signal routing for loopback test
- Receive low-pass filter for 8 kHz attenuation
- Sixteen possible audio configurations
- Provision for auxillary speaker phone
- Power-down mode with data retention

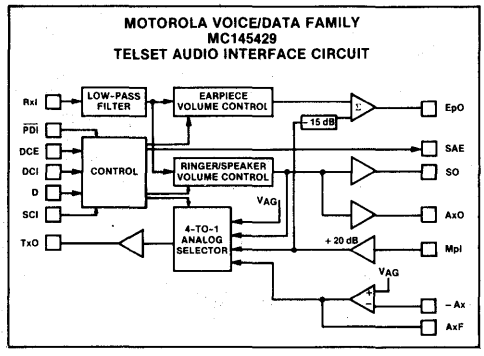

FIGURE 8

The MC145429 is designed in Si-gate CMOS technology and is implemented in a 18 pin package. This device adds ease of analog signal adjustment with software, in lieu of hardware.

DIGITAL PHONE APPLICATION

In Figure 9, a Digital Feature Phone is implemented using the MC145426 Slave UDLT, the MC14402 mono-circuit and the MC146805 CMOS microprocessor. In this application the Slave UDLT generates the clocks and frame periods for both the MPU and the mono-circuit. The Slave UDLT also transmits and receives the 64 kbps PCM voice word from the mono-circuit and the 16 kbps signaling data for the MPU. The UDLT powers down itself and the other logic automatically in an on hook mode.

The mono-circuit is used for voice coding and decoding, as well as the interface to the speaker and microphone in the handset. The RXO output pin provides the output signal to the earpiece, while the RXG pin sets the signal gain. The RXO pin provides the output for the ringing signal to the piezoelectric transducer or speaker. The TX pins are used for setting the gain of the incoming signal and side tone.

The MPU provides for the keyboard encoding, speaker enable and other features desired.

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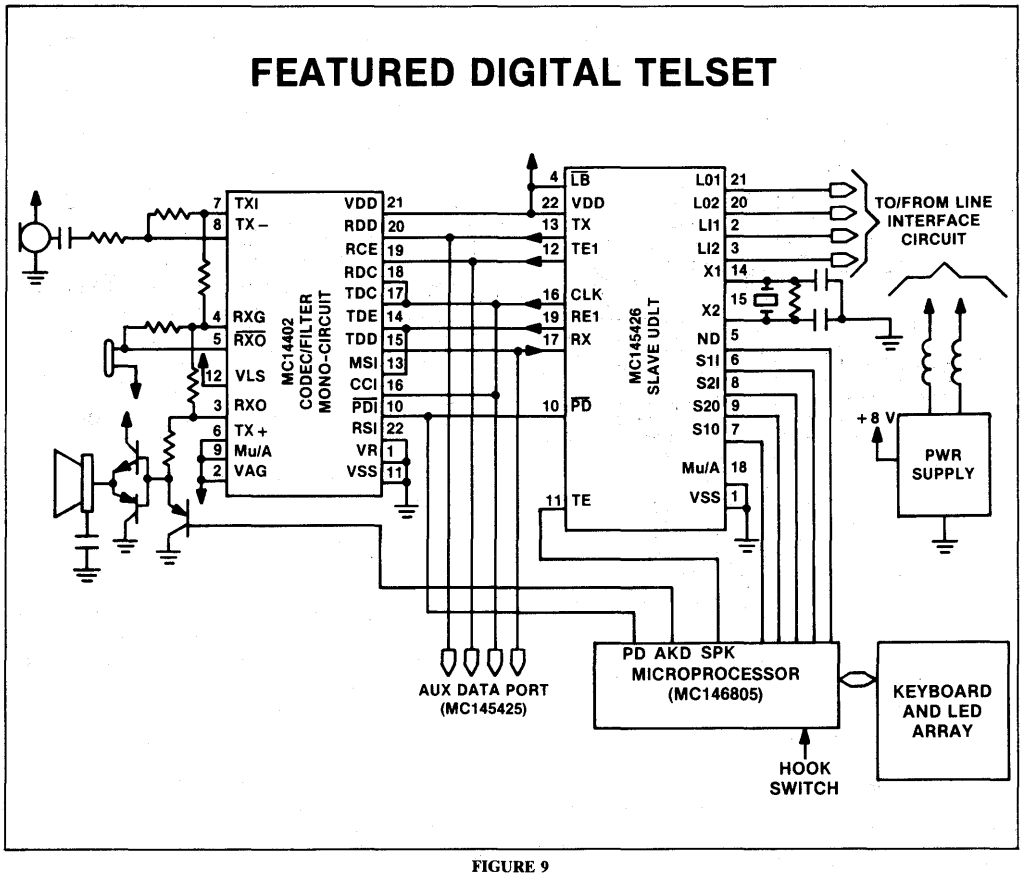


FIGURE 9

DIGITAL WORKSTATION APPLICATION

Figure 10 illustrates a more complete voice/data workstation using the full family of Motorola products. The MC145422 Master UDLT and the MC14418 Time Slot Assigner Circuit (TSAC) reside on the line card in the PBX. The TSAC is used to provide the control timing for the Master UDLT. Each 125 ms frame the 10 bits of data burst from the Master UDLT and is received by the Slave.

The MC145426 Slave UDLT outputs the 64 kbps PCM word to the MC14402 mono-circuit for data conversion to an analog signal. The analog signal from the mono-circuit is routed through the MC145429 Telset Audio Interface Circuit. This IC enables the MPU to digitally control the analog signal level of the handset and speaker phone.

The MC145428 Data Set Interface circuit adds the asychronous data port capability to the digital phone. This could be a standard RS-232 port with data select options for 300 to 19.2 kbps for simultaneous voice and data transmission or 300 to 56 kbps for data only transmission.

The MC146805 microprocessor controls power down, dialing functions, ringing speaker enable and other functions which may be desired in the workstation.

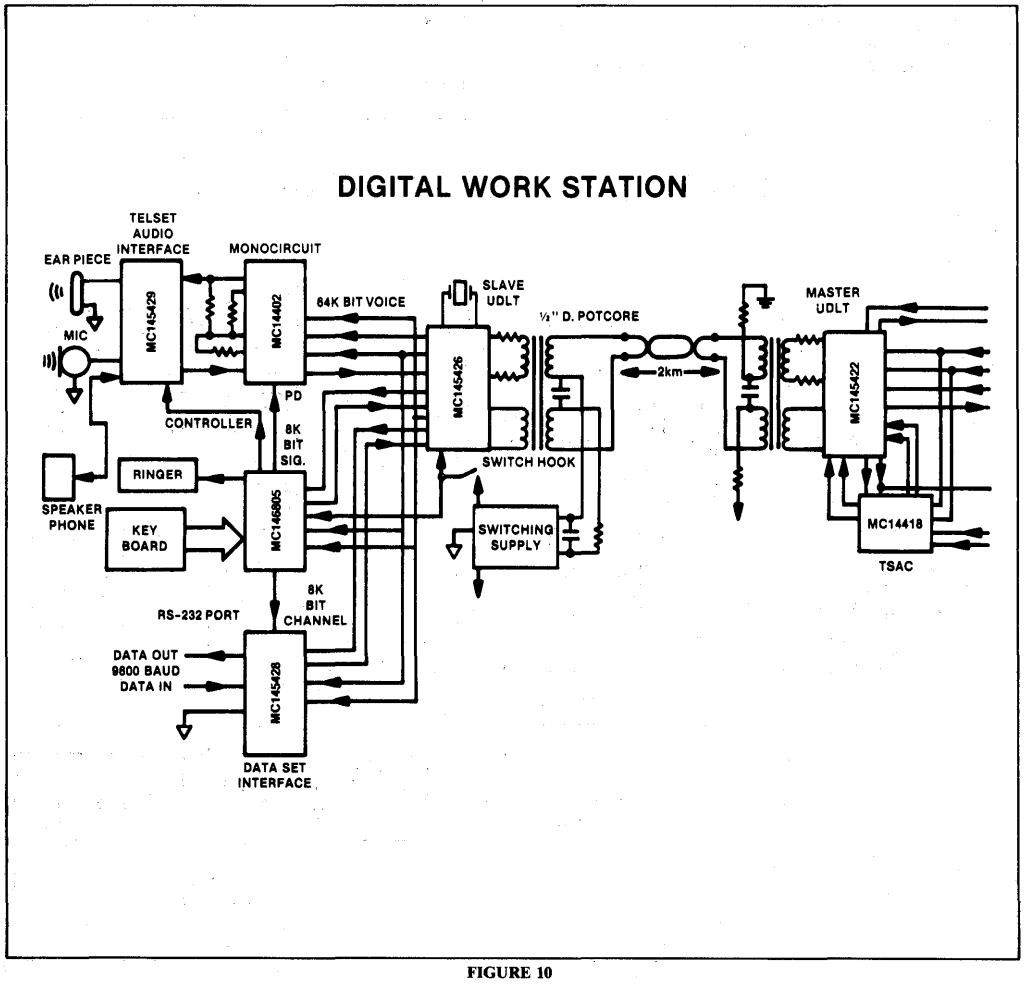


FIGURE 10

LIMITED DISTANCE MODEM APPLICATION

The UDLT family is well suited for a variety of low cost point to point high speed Limited Distance Modem (LDM) applications. In Figure 11, the Master and Slave UDLT, along with minimal control logic, make up a synchronous 64 kbps LDM. In this application, the 16 kbps channel is reserved for handshake and control lines.

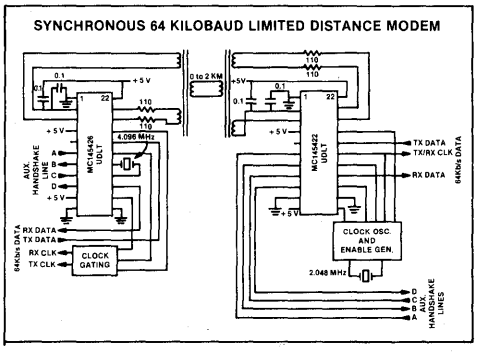


FIGURE 11

An asynchronous LDM is achieved with the addition of the MC145428 DSI ICs, as shown in Figure 12. In this application, an asynchronous data rate from 300 to 38.4 kbps can be achieved.

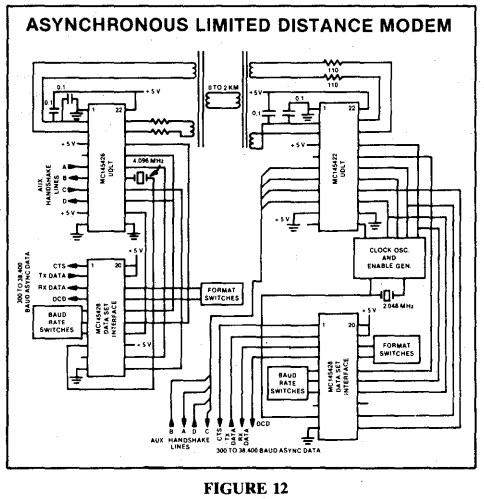


FIGURE 12

By grouping multiple DSIs together, a data multiplexer can be implemented, as shown in Figure 13. In this application, eight 9600 baud asychronous ports are being multiplexed thru one set of UDLTs.

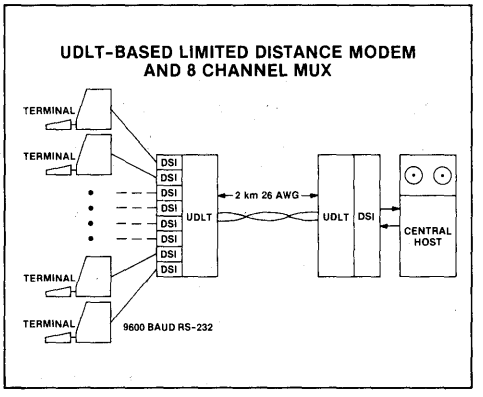


FIGURE 13

SUMMARY

Motorola's present telecom IC family makes possible a cost effective approach in developing voice and data PBXs, and LDMs. These ICs are the first generation products for the evolving voice and data market. Many more ICs are being defined and developed for the emerging voice and data products that will be needed for central office equipment and the evolving ISDN (Integrated Service Digital Network) switches.

MOTOROLA

UDLT Evaluation Board

INTRODUCTION

To help meet the demands for a cost effective solution to the ever growing voice/data world within the digital telephone and PBX realm, Motorola has created the Universal Digital Loop Transceiver (UDLT) voice/data circuit family. The purpose of this application note is to render an understanding of the UDLT voice/data family and show a typical application for these CMOS parts. This is an evaluation of the application and performance of the MC145422/26 UDLT demonstration board, which was designed and built for customer evaluation.

FUNCTION OF PARTS

UDLT's

The UDLT master (MC145422) and slave (MC145426) are transceivers that provide 80 kilobit-per-second full duplex synchronous voice and data communication to distances of two kilometers on 26 AWG twisted pair and further on heavier gauge pairs. The modulation technique used is a 256 kilobaud Modified Differential Phase Shift Keying (MDPSK) type burst. The MDPSK triangular waveform used in this modulation technique reduces radiation, EMI, and crosstalk due to its compact frequency spectrum.

The master which is used at the telephone switch linecard bursts ten bits to the slave, consisting of eight bits of voice/data and two signaling bits. The slave, which is used at the terminal or digital telephone, receives the burst from the master and upon demodulation of the burst synchronizes its clocks, and bursts ten bits back to the master. This "ping-pong" technique occurs within a 125 microsecond frame period and allows end to end full duplex, synchronous operation. This full duplex operation between the master, at the digital linecard and the slave/mono-circuit, at the digital telephone, enables each set to have high speed access to the PABX switching facility.

At the linecard a microprocessor has complete control of the master. The Signal Enable input (SE) is a three state controller pin which if held high enables the power down, loopback and the two signaling bits, thus allowing these signals to be bussed to the microprocessor. The master can be programmed via the Signal Insert Enable (SIE) pin to insert signaling bit two into the LSB of the PCM word at Tx. This allows simultaneous voice and data transmission through the PABX without the need of changing existing hardware and software. Both the master and the slave have power down and loopback features for system power conservation and testing. The power down pin on the slave is a bidirectional pin. It can be used as an input to initiate a call. When the PD pin is pulled high, the slave will continue to burst every other frame (once every 250 microseconds) until the master responds by bursting. Once the master responds, the slave synchronizes to ping-pong with the master at an eight kilohertz rate. The PD pin can be left floating as an output, in which case the slave will pull PD high until the slave stops receiving bursts from the master then it will take PD low and stop bursting until PD is brought high or the master bursts again. A three state control can be used on this pin if the designer wants to send data to the master during a power down. The slave also has a Tone Enable input pin (TE) which when held high generates a 500 hertz square wave tone at approximately −20 dBm0 which can be used in the digital telset to provide audio feedback.

MONO-CIRCUITS

Motorola's family of Pulse Code Modulation (PCM) mono-circuits incorporate a codec, filter and voltage reference into a single IC. The general block diagram for Motorola's mono-circuits is shown in Figure 1. These devices perform the digitizing and recovery, as well as the band-limiting and reconstruction filtering necessary for voice digitization in telephone systems. The mono-circuits are tailored for a variety of telephone switch architectures. The family consists of five different device types. The MC14400, MC14403, and MC14405 16 pin devices, the MC14401 18 pin device and the MC14402 22 pin device allow designers to optimize for minimal configurations or select a full set of features. The MC14403, for example, can be used where minimal space is desired for the digital phone design whereas the MC14402 is available for maximum flexibility. The mono-circuit incorporates the band-pass filter required for antialiasing and 60 hertz rejection, the A/D, the D/A, both for either U.S. Mu-Law or European A-Law companding formats, the lowpass filter required for reconstruction smoothing, on-board precision voltage reference and does not require any external components.

In this demonstration board, the full featured 22 pin MC14402 mono-circuit is used in the slave circuit showing its ability to adjust the receive gain while maintaining a low impedance output using the RxO, RxG, and $\overline{\text{RxO}}$ pins, The MC14403 is used on the master board showing a simple 16 pin solution for the telephone handset interface.

DATA SET INTERFACE (DSI)

The MC145428 Data Set Interface (DSI) provides the asynchronous to synchronous and synchronous to asynchronous data conversion. This low power five volt CMOS device is ideally suited to interface between the RS-232 compatible data port of any voice/data digital telset or terminal and the synchronous data channel of the UDLT. A block diagram of the Data Set Interface is shown in Figure 2.

There are two basic modes of operation for the synchronous channel interface. In the first mode the DSI inter-

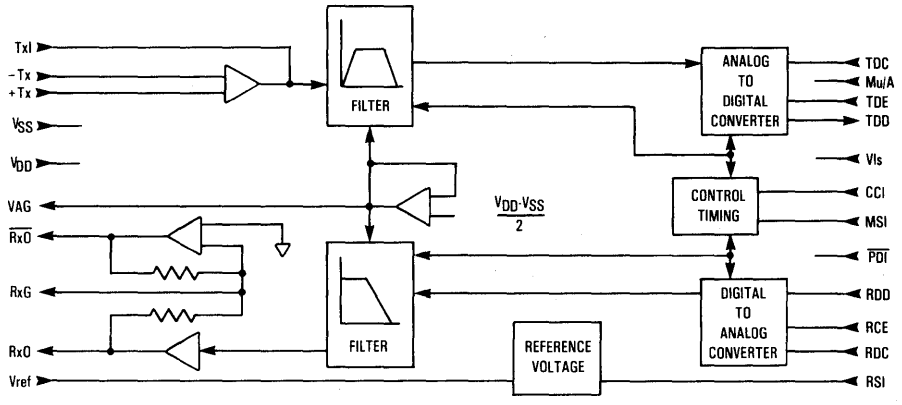


Figure 1. Block Diagram of the Mono-circuits

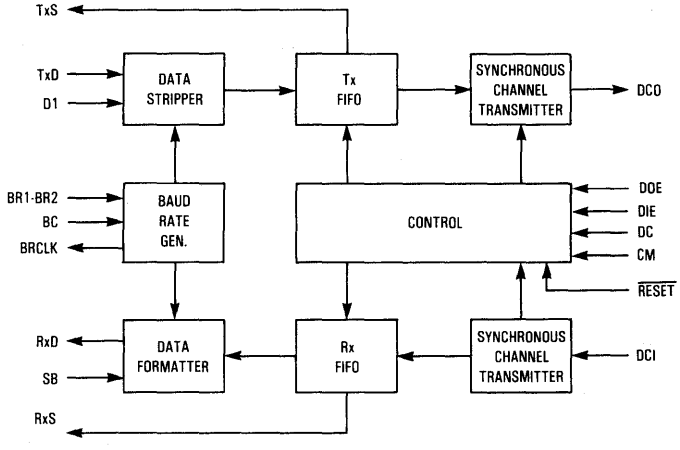


Figure 2. Block Diagram of the Data Set Interface

faces to the eight kilobits-per-second data channel of the UDLT. The Clock Mode input (CM) is tied low while the Data Output Enable (DOE) and Data Input Enable (DIE) are tied high. In this mode a new data bit is clocked out of Data Channel Output (DCO), a new data bit is clocked in at Data Channel Input (DCI), on each falling edge of the Data Clock (DC).

In the second mode of operation, the clock mode is held high. In this mode the DSI is intended to interface with the UDLT's 64 kilobits-per-second data channel. Data is clocked out under control of DOE and the rising edge of DC. Data may be clocked out at a maximum length of eight bits per enable high period. Data is clocked into DCI under control of DIE high and the falling edge of DC. The maximum word size is also eight bits per DIE high period.

Asynchronous data is input on the TxD pin from the output of the RS-232 receiver. This data must have at least one start and one stop bit and at least eight data bits, but will accept nine. The length of the data word is set by the DL pin. A high on DL selects a nine bit data word and a low selects an eight bit data word. The baud rate at which the DSI accepts data on the TxD pin, and outputs data on the RxD pin, is selected with the BR1, BR2, and BR3 pins which derive the internal sampling clock. The internal baud rate generator may be programmed to accept common asynchronous data rates from 300 to 38.4 kilobits-per-second. This internal sampling clock is 16 times the selected baud rate. If BR1-BR3 are all set to logic zero then an externally supplied 16 times clock can be used on the Baud Clock pin (BC) thus giving the user a variable data

rate from zero to 128 kilobits-per-second. For the internal baud rate generator to be accurate, a 4.096 megahertz clock must be used at the BC pin. If the internal baud rate generator dividers are used with a BC clock other than 4.096 megahertz, the data rate may be directly scaled.

Data input on the TxD pin is stripped of its start and stop bits and is loaded into the transmit FIFO register. If the transmit FIFO holds more than two data words or if RESET is held low, then the (TxS) Transmit Status output pin will go low.

Data coming in from the synchronous side is loaded into the receive FIFO, the data has its start and stop bits inserted and is output at RxD at the same baud rate as the transmit side. If the receive FIFO is overwritten, RESET is held low, or if loss of synchronization occurs by the loss of the synchronizing flag word, then the (RxS) Receive Status output pin will transition low.

RS-232 DRIVERS/RECEIVERS

The RS-232 Driver/Receiver chips interface the data terminal equipment with data communications equipment. Motorola manufactures both the MC1488 Quad Line Driver as well as the MC1489 Quad Line Receiver. Both 14 pin packages were used in this evaluation board. Motorola also manufactures the MC145406 Driver/Receiver chip which is a silicon-gate CMOS integrated circuit that combines three drivers and three receivers compatible with the electrical specifications of EIA standard RS-232-C, and CCITT V.28. This part has the capability of running with power supplies ranging from ±5 volts to ±12 volts while operating with a maximum quiescent current supply of 1.45 milliamperes. By combining both the drivers and receivers in a single CMOS chip, the MC145406 provides an efficient, low-power solution for RS-232-C/V.28 applications. A footprint for the MC145406 is included on the evaluation board design.

TRANSFORMER INTERFACE

The transformer interface between the UDLT and the twisted pair wire is of primary importance. The major transformer specifications can be determined from the specifications of the UDLT, driver/receiver, modulation technique, effective characteristic impedance of the wire, attenuation of the wire and dc current feed capacity. The UDLT has a differential output (LO1, LO2) that can drive 440 ohms differentially to five volts peak to peak. The receiver has an input threshold of ±25 millivolts. The UDLT modulation method has maximum power bandwidth from eight kilohertz to 512 kilohertz. To improve line settling between bursts, a bandwidth of 20 kilohertz to 512 kilohertz is used. The effective characteristic impedance of 26 AWG telephone twisted pair wire is approximately 110 ohms with an attenuation of 18 decibels-per-kilometer at a frequency of 256 kilohertz. The transformer configuration is shown in Figure 3.

The source impedance resistors for the LO1 and LO2 driver outputs were chosen to be 220 ohms on the transmit tap. This dictates a turns ratio of 2:1 to the line side of the transformer to result in an impedance match to the 110 ohms characteristic impedance of the twisted pair.

To set the 20 kilohertz low-frequency cut off of the transformer interface, the inductance of the transmit winding of the transformer should be 1.75 millihenries. To set the 512 kilohertz high-frequency cut off, a 0.001 microfarads capacitor is connected in parallel with the transmit tap. The turns ratio for the receive winding is determined by the maximum attenuation of the line and the threshold of the receiver detecter. With an initial amplitude of 2.5 volts peak (five volts peak to peak) at LO1 and LO2 halved by the source resistors to 1.25 volts peak at the transmit tap, which is halved again via the turns ratio to the line windings, yields 0.625 volts peak at the line side of the transformer. This 0.625 volts peak is reduced by 36 decibels or a factor of 63 to ten millivolts at the receiving transformer. The receiver of the UDLT has a positive and negative 25 millivolt threshold, which means the receive transformer tap needs a gain of approximately four to meet the needs of the receiver circuitry of the LI pin. This results in the transformer of the schematics, which may be obtained from:

Leonard Electric Products Company
85 Industrial Drive
Brownsville, Texas 78521
P/N P-1358-A

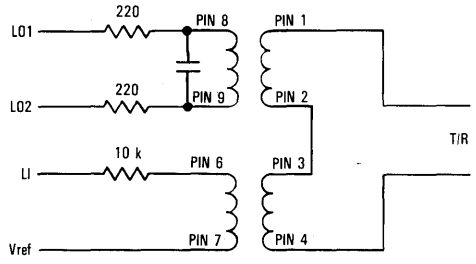


Figure 3. Transformer Configuration

The signals from LO1 and LO2 on the transmit tap are 1.25 volts peak which through the turns ratio to the receive tap becomes 2.5 volts peak at LI. This can exceed the maximum and minimum voltage specification for LI requiring input protection such as the clamping diodes on LI, shown in Figure 4.

When using battery feed through the transformer, further protection is required due to loop current induced spikes at both transmit and receive taps of the transformer. There are several factors to take into consideration when determining the specifications for battery feed current by the center tap of the line side of the transformer. The maximum power is transferred when half of the source voltage is dropped across the effect source resistance. Based on a loop length of two kilometers with a dc resistance of 270 ohms per loop kilometer, a current of 44 milliampheres is the maximum power transfer current. The loop current chosen for the specification is 100 milliampheres. The circuit of Figure 4 is an example of this type of protection.

EVALUATION BOARD DESCRIPTION

The Motorola UDLT evaluation board is a single sided PC board that consists of all the necessary circuitry for end to end operation and demonstration of the 80 kilobits-per-second full duplex synchronous data link of the UDLT master and slave. The evaluation board itself consists of two smaller boards; a master board and a slave board. These two boards may be

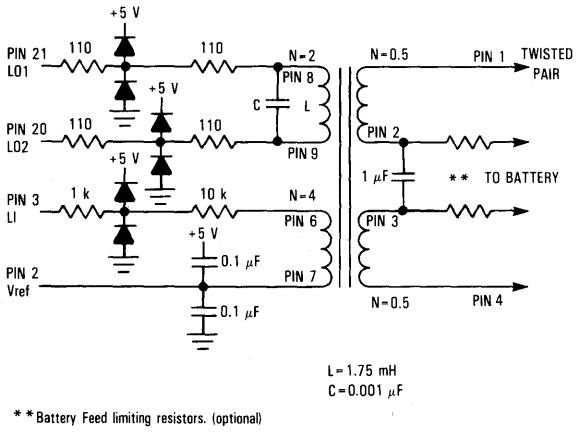


Figure 4. Application Circuit For the Transformer Interface

separated by cutting the panel in half along the two markers, shown in Figure 7. The master board schematic is shown in Figure 5 and the slave board schematic is shown in Figure 6, while the artwork is shown in Figure 7.

The master board contains the master UDLT (MC145422), DSI (MC145428), Mono-circuit (MC14403), the MC1488/1489 or MC145406 RS-232 drivers and receivers, and the necessary clock circuitry to drive these parts. The master board emulates both another digital telset plus the telephone switch interface to the slave board. The master typically is used in the digital switch at the PBX, networked with other digital and analog interface circuits.

The slave board contains the slave UDLT (MC145426), DSI (MC145428), Mono-circuit (MC14402), MC1488/1489, or MC145406 RS-232 Driver/Receiver chips. The slave side emulates a digital telephone where the analog information is digitized at the phone and the information from the phone is digital.

Both master and slave boards have their second eight kilobit signaling channel connected to a DSI for up to 9600 baud of user data simultaneously independent of voice. The baud rates are selected with switches BR1-BR3 (see strapping information). Each board has a DB-25 connector for easy connection to any terminal. Only TxD, RxD, and Ground are connected on the DB-25. Data to and from the DB-25 is fed through the MC1488, MC1489 and the MC145406 Driver/Receiver chips. The socket for the MC145406 RS-232 Driver/Receiver chip is included on each board for evaluation. This part can replace both the driver and receiver chips. Once replaced, the user at his option can cut the MC1488 and MC1489 pads out of the PC board along the dashed lines. This enables each board to fit in a K-2500 phone.

Each board has an RJ-11 socket for easy connection to any modular handset. The signal from each handset is fed through the respective mono-circuit into the 64 kilobit voice channel on the UDLTs. Both master and slave boards have space for a push button switch which can be hardwired onto the SI1, along with an LED on SO1 for signaling on channel one. This channel is optional to the user and can be used with a microprocessor in the phone or a pulse dialer. Signaling bits one and two provide eight kilobits-per-second each of protocol independent data. Switches permit access to particular features of the voice/data integrated circuits on both boards, as explained below.

STRAPPING INFORMATION

The component layout is shown in Figure 8. The layout shows the footprints for switches which can be used with wire straps. The solid lines indicate the normal strap positions which; select Mu law, 9600 baud data rate, with one start bit, eight data bits and one stop bit. The dip switches can be used if desired and can be obtained from:

Grayhill Inc.
561 Hillgrove Avenue
La Grange, Illinois 60525

P/N	Name	Qty
78J05	S1, S2	3
78J02	S3	1

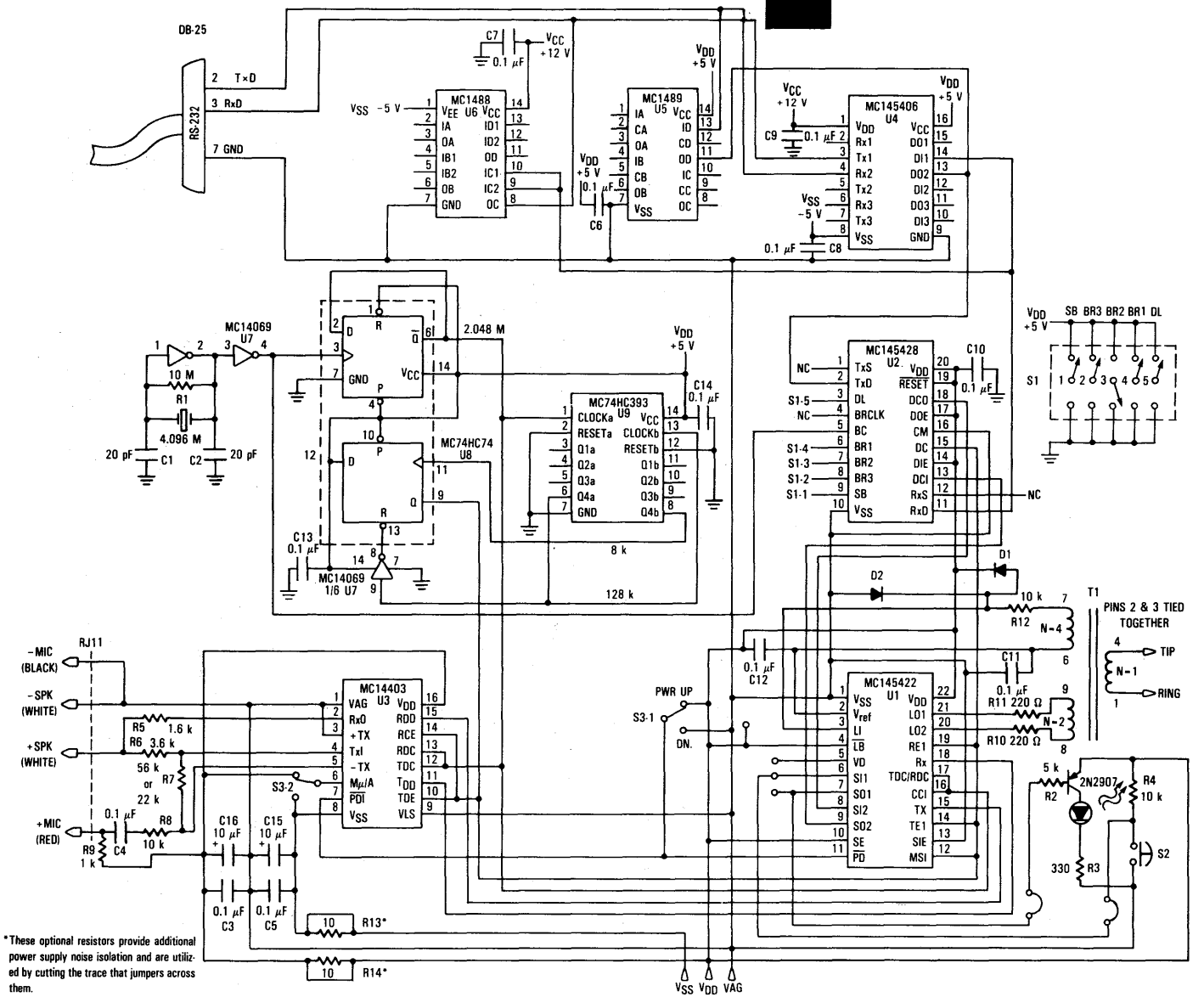
STRAPPING ON THE MASTER

S1 — These straps select via U2 (MC145428 DSI) the number of stop bits, the length of the data word and the baud rate selected for the asynchronous data.

SW1 — (SB) A high selects two stop bits; a low selects one stop bit.

SW2-SW4-(BR3-BR1) — These bit rate inputs select the asynchronous bit rate, either externally supplied at the BC pin (16 times clock) or one of the supplied bit rates shown in the table on page 2-309 of the Telecommunications data book.

SW5 — (DL) This Data Length input pin selects a nine bit data word when high or an eight bit word when low.



*These optional resistors provide additional power supply noise isolation and are utilized by cutting the trace that jumpers across them.

Figure 5. Master UDLT Demo Board

S2 — This switch is optional and is hardwired to signaling channel one for demonstration using LEDs. The footprint for this switch is included on the board.

This switch can be obtained from:

Cutler-Hammer
P/N B8500W/P281R

S3 — These straps select Mu or A laws and power down on the MC14403 Mono-circuit and MC145422 master UDLT.

SW1 — (PD) This strap when high, powers both the mono-circuit and master UDLT. When low, both parts are powered down.

SW2 — (Mu/A) Selects Mu or A law coding.

Loopback and Valid Data on the master can be accessed via pads.

STRAPPING ON THE SLAVE

S1 — Same as S1 on the master; selects asynchronous data format and bit rate.

S2 — These straps select Tone Enable, Power Down, Mu/A, and Loopback features of the slave (MC145426) as well as Mu/A and Power Down on the MC14402 Mono-circuit.

SW1 — ($\overline{TE}$) A high enables a 500 hertz tone.

SW2 — ($\overline{PD}$) Powers both the slave and mono-circuit up or down. High = powered up, and Low = powered down.

SW3 — (Mu/A) Selects Mu or A law coding for the mono-circuit.

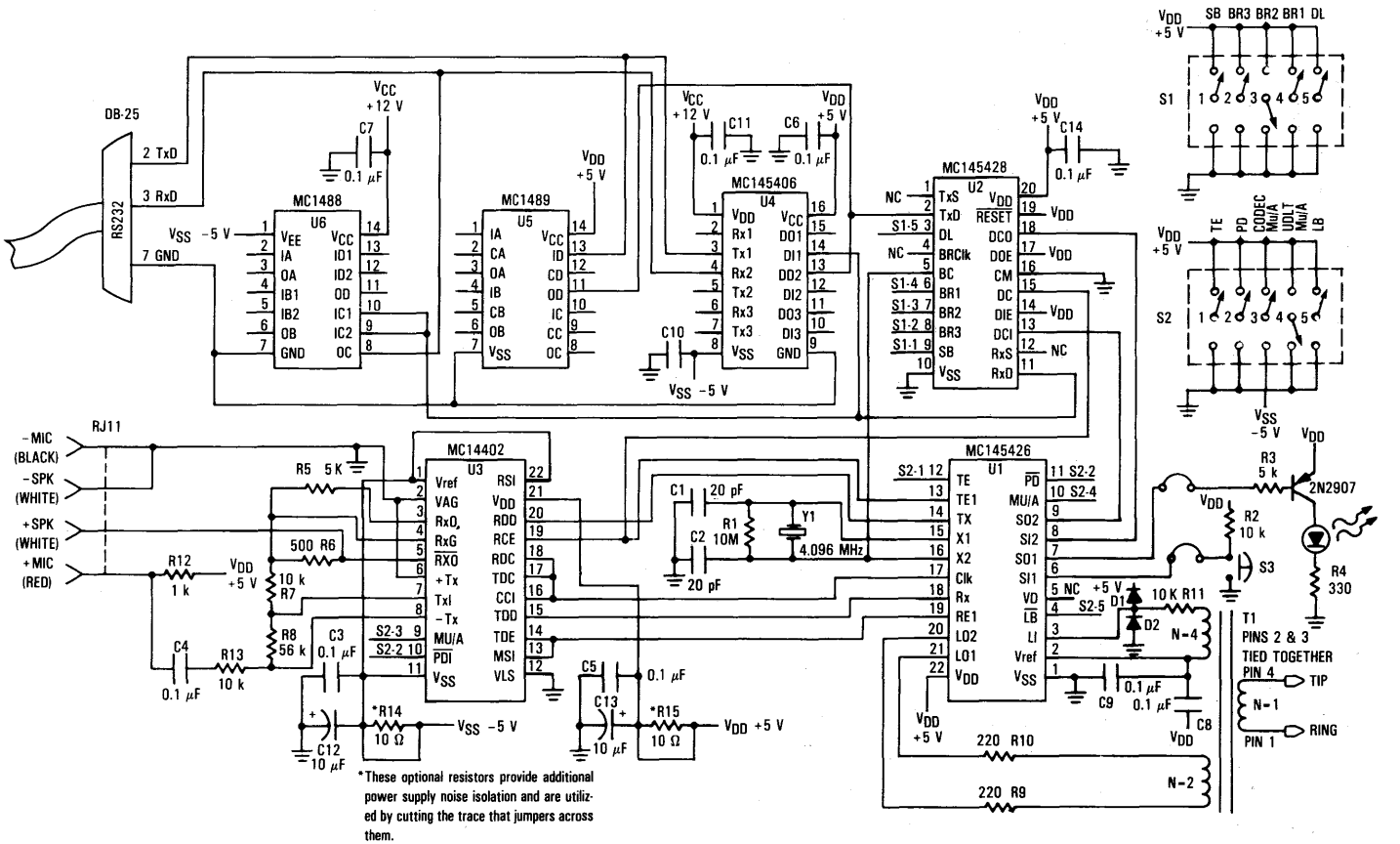
SW4 — (Mu/A) Selects Mu or A law coding for the slave UDLT.

SW5 — (LB) When low, the 64 kilobits-per-second of information coming from the master will loop through the slave and return to the master. The signaling bits are unaffected.

S3 — Same as the S2 switch on the master.

POWER SUPPLY CONSIDERATIONS/LAYOUT GUIDELINES

The power supply requirements for these boards are V_{DD} at +5 volts, V_{SS} at −5 volts and V_{CC} which is the RS-232 driver positive voltage of +7 to +12 volts for the MC1488. V_{CC} may be as low as +5 volts with the MC145406 Driver/Receiver chip. The power supply current required by each of these voltages is less than 30 milliamperes. This results in a total slave board power consumption of less than 400 milliwatts. This amount of power may be supplied by the loop using a linear supply. To isolate the RS-232 port with respect to earth ground, a switching regulator powered by the loop or an external power supply will be required. If a switching regulator is used, it should be synchronized to the eight kilohertz and 128 kilohertz clocks of the slave UDLT to reduce the affects of aliasing noise into the analog circuitry of either the UDLT or audio voice channel. This function will be supported by the MC34129 Digital Telephone Switching Power Supply Controller chip. This device has the capability to power-up and regulate on its internal oscillator. After regulation is established it can synchronize to an external clock such as the slave's 128 kilohertz clock.



*These optional resistors provide additional power supply noise isolation and are utilized by cutting the trace that jumpers across them.

Figure 6. Slave UDLT Demo Board

MASTER UDLT DEMO BOARD PARTS LIST

PART	QUANTITY (PART NUMBER)
MC145422	1-U1
MC145428	1-U2
MC14403	1-U3
MC145406	1-U4
MC1489	1-U5
MC1488	1-U6
MC14069UB	1-U7
MC74HC74	1-U8
MC74HC393	1-U9
LEPCO P-1358A	1-T1
DB25	1
RJ11	1
GRAYHILL (SPDT 78J05)	1-S1
CUTLER-HAMMER B8500W/PZ81R	1-S2
GRAYHILL (SPDT 78J02)	1-S3
BANANA JACKS	6
20 pF	2-C1 & C2
0.1 μF	12-C3-C14
10 μF	2-C15, C16
10 M	1-R1
5 K	1-R2
330 Ω	1-R3
1.6 K	1-R5
3.6 K	1-R6
56 K	1-R7
10 K	1-R8
1 K	1-R9
220 Ω	2-R10, R11
10 K	2-R12, R4
10 Ω	2-R13, R14
CRYSTAL	1-4.096 M
JUMPERS	10
DIODES 1N914	2-D1, D2
LED (T1)	1
2N2907	1
SOLDER TAIL SOCKETS	
14 PIN	5
16 PIN	2
20 PIN	1
22 PIN	1

SLAVE UDLT DEMO BOARD PARTS LIST

PART	QUANTITY (PART NUMBER)
MC145426	1-U1
MC145428	1-U2
MC14402	1-U3
MC145406	1-U4
MC1489	1-U5
MC1488	1-U6
LEPCO P-1358A	1-T1
DB25	1
RJ11	1
GRAYHILL (SPDT 78J05)	2-S1 & S2
CUTLER-HAMMER B8500W/P281R	1-S3
BANANA JACKS	6
20 pF CAPS	2-C1 & C2
0.1 μF CAPS	10-C3-C11, C14
10 μF CAPS	2-C12, C13
10 M	1-R1
5 K	1-R3
330 Ω	1-R4
5 K	1-R5
500 Ω	1-R6
10 K	1-R7
56 K	1-R8
220 Ω	2-R9, R10
10 K	3-R11, R13, R2
1 K	1-R12
10 Ω	2-R14, R15
JUMPERS	12
CRYSTAL	1-4.096 M
LED (T1)	1
DIODES 1N914	2-D1, D2
2N2907	1
SOLDER TAIL SOCKETS	
14 PIN	2
16 PIN	1
20 PIN	1
22 PIN	2

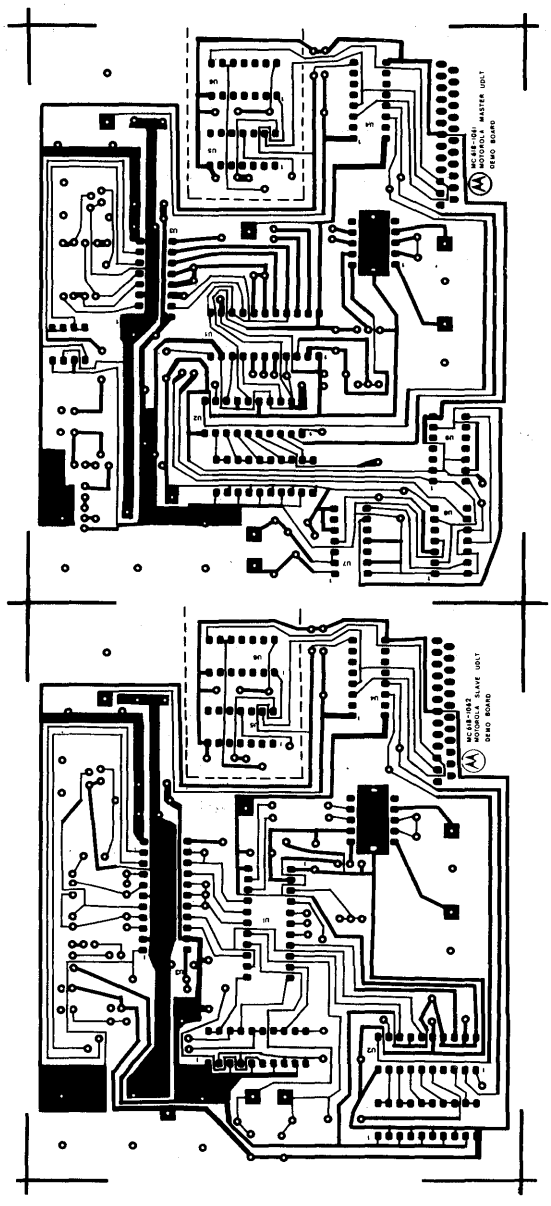


Figure 7. Artwork of UDLT Voice/Data Evaluation Board

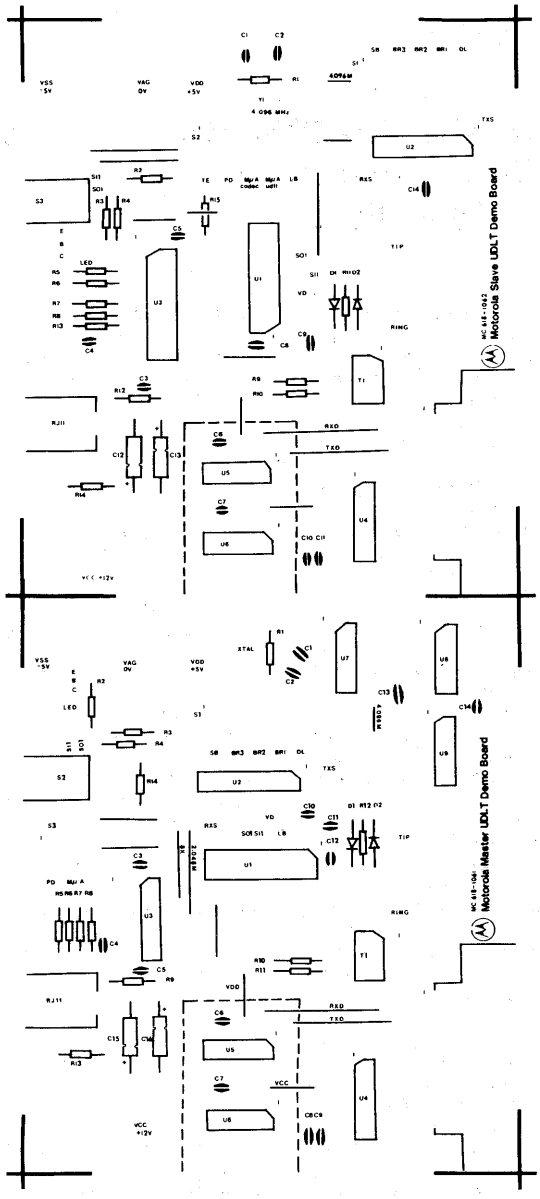


Figure 8. Component Layout

MOTOROLA

Interfacing the MC145418 and MC145419 Digital-Loop Transceivers to a Single Twisted-Wire Pair

The MC145418 master Digital-Loop Transceiver and the MC145419 slave Digital-Loop Transceiver (DLTs) provide a highly flexible digital transmission environment which can be easily adapted for use in voice/data applications over a single twisted-pair wire. The DLT is designed to promote communication between two digital synchronous serial devices over a transmission medium which can support the Modified Differential Phase Shift Keyed (MDPSK) protocol utilized between the master and slave. To further simplify interface requirements, the outputs from and inputs to the DLT, with respect to the transmission medium, are digital CMOS technology. By utilizing the inherent features of the DLT an interface can be designed that supports signaling, data and voice operation along with battery feed for digital telephone applications. The purpose of this note is to investigate the design of such an interface.

TRANSMISSION

The typical transmission scheme of the DLT takes eight bits of information from the transmit register along with two bits of information on the signaling bit inputs and creates a ten bit word that is then modulated and presented to the DO output along with a valid signal indication called MEO. The transmit register is an eight bit shift register that takes the information presented at the Rx pin and is loaded by the TDC/RDC clock on the master or CLK by the slave when RE1 is high. This information is loaded into the modulation buffer by the leading edge of MSI on the master, or TE1 on the slave. Along with these eight bits, the information resident at SI1 and SI2 are loaded into the modulation buffer to create a ten bit word. This word is modulated and transmitted at a 256 kbps data rate. The DO pin is always presenting changing data at the output so a signal called MEO is available to define when the DO is transmitting valid data. MEO will stay high for all ten bit periods and then go low so it can be used as an enable signal to enable DO onto the transmission medium, in this case the twisted-pair wire.

Since DO can start valid in either a low or a high state, there must be a way of indicating the start of a transmission that is data independent. The easiest way to do this is to use a bipolar scheme where highs and lows are represented by positive and negative voltages on the line and when no valid transmission exists, no voltage is sent to the line. By using a small pot-core transformer, an interface can be designed that uses standard HC-series CMOS digital parts for the driver in a differential drive scheme that performs in this bipolar scheme. Figure 1 shows a circuit that uses one MC74HC00 quad two-input NAND gate package. When MEO is high, DO is inverted by two of the NAND gates and they drive a feed resistor to the coupling transformer. This inverted output also goes to the other two NAND gates which re-invert it and drive the other feed resistor in a differential drive-type configuration. When MEO is low all of the NAND gate outputs are forced high, which represents a 0 volt differential potential at the transformer, so no signal is coupled through the transformer and the line receives no signal, thus fulfilling our transmission requirements.

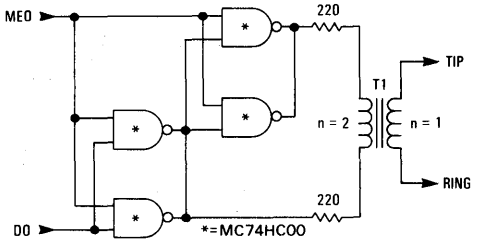


Figure 1. Transmit Interface

The HC-type devices have a low impedance output which is used to preserve the proper line impedance to the twisted-pair for optimal performance. The twisted-pair is typically a 110 ohm impedance transmission line and for the best power coupling this condition must be preserved. On the driver side of the transformer, the 110 ohm impedance is translated to 440 ohms through the 2 to 1 winding ratio of the coupling transformer. This means that the drivers see 440 ohms plus two 220 ohm resistors. Looking back into the source from the line side of the transformer, the two feed resistors are tied to low impedance sources so the net source impedance is the series combination of the feed resistors (2x220 ohms) times the transfer ratio of the transformer ($1^2/2^2$) which gives an equivalent impedance at the line of 110 ohms. This guarantees that the power transfer to the line is maximized.

RECEPTION

On the other end from the transmitter, the receiver must remove the signal from the line without disrupting the line balance and convert it into a digital MDPSK signal with an associated valid reception signal. The signal is then demodulated into ten digital bits and loaded into the demodulation buffer. When demodulation is complete, the eight bits originating from the transmit register are loaded into the receive register and the SI bits from the transmitter will be put onto the SO pins on the next MSI for the master, or TE1 for the slave. The receive register can be unloaded via the Tx pin on the master with the TDC/RDC clock and the TE1 enable. The receive register of the slave is unloaded when TE1 is high and by CLK.

Figure 2 shows how an LM339 quad comparator chip can be used to extract the necessary information from the coupling transformer. In this scheme a step-up winding is used to help the overall sensitivity of the receiver. The 51 kilohm and 10 kilohm resistors present an impedance to the line of about 3.8 kilohms so that the receiver presents a minimal impedance change to the line. These two resistors provide an over/under voltage protection network in conjunction with the two clamp diodes. Near end coupling of the transmit along with the voltage boost due to the transformer windings can create excessive voltage swings that will damage the LM339, the network prevents this from happening. When in a clamp condition, the 10 kilohm resistor prevents the receiver from reflecting a low impedance to the line through the transformer. From this point the signal is now fed into the comparator circuits. The comparator that outputs to DI is strictly a limiter and is used to square the signal so that it is easily demodulated. The other three comparators provide

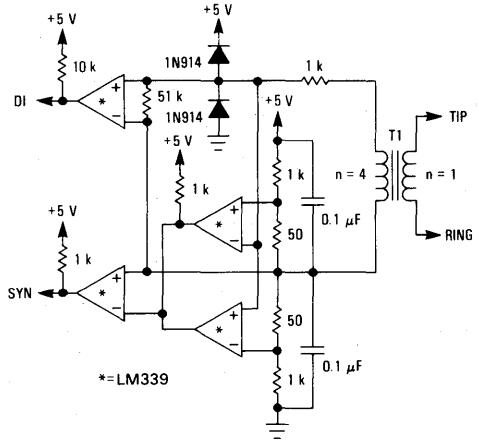


Figure 2. Receive Interface

a window detector that helps define the burst envelope to SYN. The four-resistor network provides a midpoint voltage between the supply voltages to use as a reference for the window detector and to provide a midpoint voltage for the transformer. The two capacitors are decoupling capacitors used to stabilize the reference. Each 1 kilohm and 50 ohm resistor network set a threshold voltage with respect to the midpoint voltage for the window comparator. One comparator checks for a valid indication above the midpoint and the second comparator checks for a valid indication below the midpoint. The outputs are then wire "ored" into the last comparator which feeds the results to SYN. Note that the window detector will have drop-outs near the zero crossings due to the thresholds. The SYN pin determines if the signal being input is valid based on the percentage of time the signal remains high and the percentage of time in which drop-outs are present. For more detail on the operation of the SYN pin consult the MC145418/MC145419 data sheet. The thresholds can be adjusted by changing the 50 ohm resistors. Larger resistors will help to de-sensitize the detector for noisy environments with some degradation in attenuation performance. Smaller resistors can be used in quiet environments where attenuation may be larger (such as extremely small gauge wire).

TRANSFORMER

Care must be taken in transformer design to guarantee proper operation and maximum performance. Figure 3 shows a diagram of the optimized transformer. In using the transformer one will see that the line side has split windings. If there is a need for a dc power feed to a remote DLT circuit, battery feed can be injected at B + and B –. In this case a 1.0 microfarad capacitor should be placed between B + and B – to preserve ac coupling. If battery feed is not used, B + and B – may be connected together directly. For best performance the Tx winding should present no more than 1.75 millihenrys in inductance to the transmitter. An optional 1000 picofarad capacitor can be added across the Tx winding to roll off the unused harmonics that exist above one megahertz. Care should also be taken to guarantee that all of the signal above 40 kilohertz (20 kilohertz is even better) is preserved so that the maximum amount of signal energy and information is available at the receiver. A final note in transformer design is in remote powering where dc current is present in the line loop, the transformer must be designed to not saturate. This means larger currents will probably demand larger cores so power must be kept to a minimum.

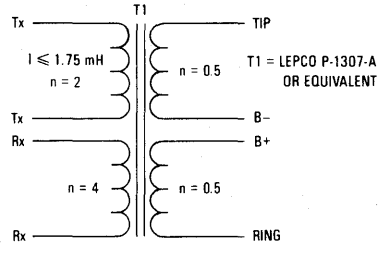


Figure 3. DLT Coupling Transformer

OPERATION WITH THE UDLT

While this circuit is intended to provide a means of implementing a DLT system, the signals presented at the line by the DLT, with this interface, are compatible with the UDLT. The signals from the UDLT can be demodulated by the DLT.

LSI for Telecommunications

a one-chip telephone

W. DAVID PACE
Motorola, Inc.
Tempe, Arizona

3

In recent years, a number of integrated circuits — such as DTMF dialers, speech networks, and tone ringers — have been developed for telephone applications. These products have replaced electromagnetic elements of the telephone because of performance and cost improvements achievable with integrated systems. In addition, the use of integrated circuits in telephones provides considerable freedom in the external design of telephone sets from both the practical and aesthetic points of view.

With these objectives in mind, a single-chip telephone circuit has been developed. The MC34010 Electronic Telephone Circuit (ETC) provides all the functions of a standard tone-dialing telephone. In addition, a microprocessor interface port facilitates automatic dialing features. An important characteristic of the ETC is its ability to operate with instantaneous input voltages as low as 1.4 V. Low-voltage operation is a key requirement in North American telephone networks, where parallel connections are common.

FUNCTIONAL BLOCKS OF THE MC34010 ETC

Figure 1 shows the elements of the ETC:

- **Line Voltage Regulator:** provides the dc termination of the subscriber loop and a bias voltage for the DTMF dialer and speech network.
- **DTMF Dialer:** generates the appropriate dual-tone multi-frequency (DTMF) signals for dialing.
- **MPU Interface:** allows the DTMF generator to be controlled by a separate microprocessor, which may be programmed to provide automatic dialing features.
- **Speech Network:** provides the two-wire to four-wire interface between the telephone line and the receiver and microphone of the handset.
- **Tone Ringer:** converts the ac ringing signals from the exchange into a warbled tone emitted through a piezo sound element.

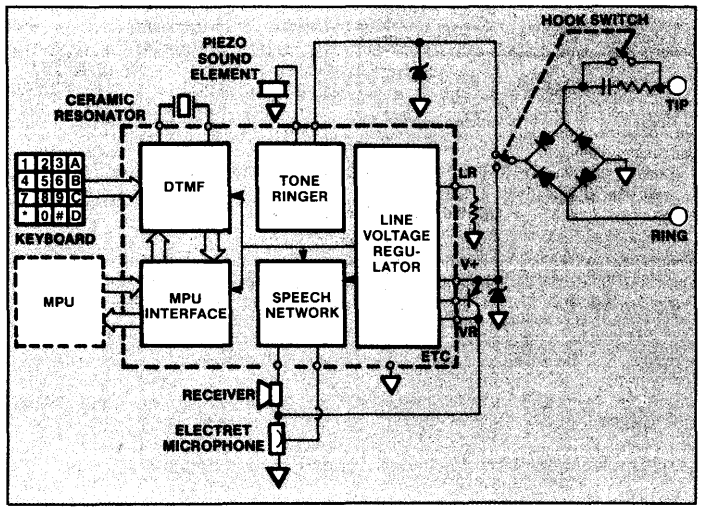


Fig. 1 Major elements of the MC34010 ETC.

Line Voltage Regulator

The line voltage regulator provides a regulated bias voltage at the VR terminal of 1.1 V to other sections of the ETC. The low saturation voltage of an external PNP pass transistor allows the line input voltage to fall within 300 mV of VR voltage without clipping signals on the line. Thus, the DTMF and speech circuits maintain specified performance with instantaneous line voltages as low as 1.4 V.

The circuit associated with the LR terminal determines the dc resistance of the telephone. At low line voltages (corresponding to operation in parallel with nonelectronic telephones), the ETC draws only 5 mA of bias current for the speech network and keypad interface circuits. When the V+ terminal voltage exceeds 3 V, excess line current flows through an external resistor at terminal LR. The 3-kV level shift from V+ to LR prevents saturation of the dc termination circuit with signals up to 2 V peak (+5 dBm) on the line.

An internal constant current sink nominally equal to the bias current of the DTMF dialer also flows through the dc termination circuit. When the DTMF dialer is activated, this current sink is disabled to reduce the line current transient and dialer clicks.

DTMF Dialer

Inexpensive telephone keypads have switches of the single pole/single throw (SPST) type that connect the row and column terminals corresponding to the selected digit. A keypad interface circuit within the ETC, consisting of input resis-

tors, comparators, and decoding logic, activates the DTMF tone generators whenever two keypad input terminals are connected.

When the keypad interface activates the DTMF generator, it also produces a mute signal for the speech network. This mute signal disables the transmit amplifier and reduces the DTMF sidetone in the receiver. Muting the receiver also suppresses clicks associated with DTMF turn-on and turn-off transients.

The row and column tone generators include a programmable counter, an encoder, and a digital-to-analog (D/A) converter. The output of the D/A converter is a stair-step approximation of a sine wave with 16-step intervals per period. Fourier analysis of such a waveform reveals that the time intervals corresponding to the positive and negative peaks (first and ninth intervals) can be shortened or lengthened with little impact on distortion. By modifying the division ratio of the programmable counter during these peak intervals, output frequency errors are reduced. The periods of the DTMF tones are adjusted to the desired value within the resolution afforded by the 500-kHz oscillator frequency.

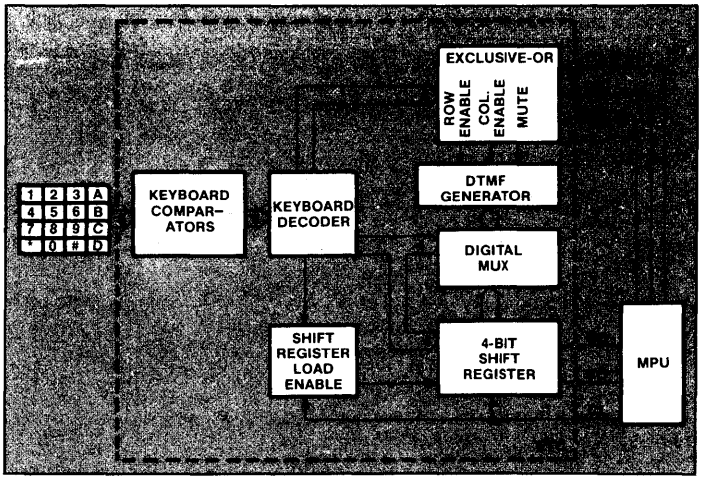


Fig. 3 The MPU interface circuit.

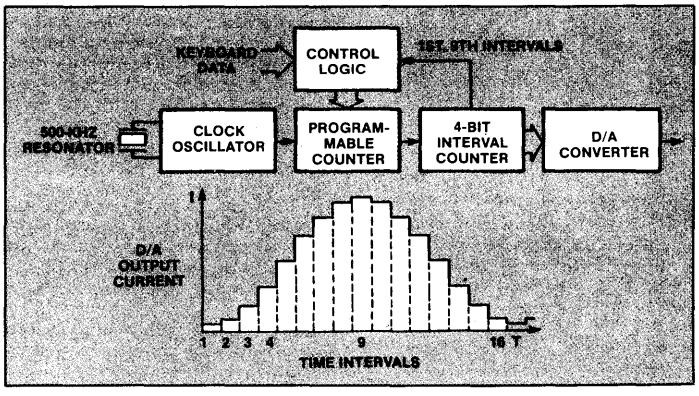


Fig. 2 The DTMF frequency synthesis technique.

Figure 2 depicts the implementation of this error reduction technique. The programmable counter divides the 500-kHz clock frequency by a number N that is loaded by the control logic at the beginning of each step. The output frequency of the programmable counter is further divided by the 4-bit interval counter. It is this counter which distinguishes the 16 waveform intervals. The output of the 4-bit counter drives the D/A converter through an encoder (not shown in **Figure 2** for simplicity).

Consider, for example, the generation of the 697-Hz Row 1 tone. For 14 of the 16 waveform intervals the control logic loads the programmable counter with a divisor of 45. For the first and the ninth intervals, however, feedback from the 4-bit interval counter causes the control logic to program the counter to divide by 44. This combination of divisors reduces the 500-kHz clock frequency to 11.14 kHz at the output of the programmable counter. The interval counter divides this signal by 16, producing a 696.4-Hz Row 1 tone. The desired frequency of 697 Hz, therefore, is synthesized with an error of only 0.09 percent.

Other DTMF tones are generated by loading the programmable counters with appropriate pairs of divisors. The worst-case frequency-division error for the eight dialing tones is 0.16 percent. Reducing the divider errors permits an inexpensive 500-kHz ceramic resonator to be used for DTMF clock generation instead of a more precise quartz crystal. In addition, the lower clock frequency allows the counter to be fabricated in a linear-compatible integrated injection logic (I^2L) technology which enhances the performance of the analog sections of the ETC.

The outputs of the row and column D/A converters are summed in the proper proportion (with a 2-dB twist) and amplified to drive the telephone line. The amplitude of the line's signal is determined by an external resistor. Feedback around the DTMF output amplifier reduces the dialing-mode output impedance to 2 kΩ to satisfy return-loss specifications.

MPU Interface

The MPU interface permits communication between the telephone keypad, the DTMF dialer, and a microprocessor. Through this port, telephone numbers may be stored in the microprocessor and later retrieved for automatic dialing. **Figure 3** shows the major blocks of the MPU interface section and the connections between the keypad, DTMF dialer, and microprocessor.

Each button of a 12- or 16-number keypad is represented by a 4-bit code. This same code controls the programmable counters to generate

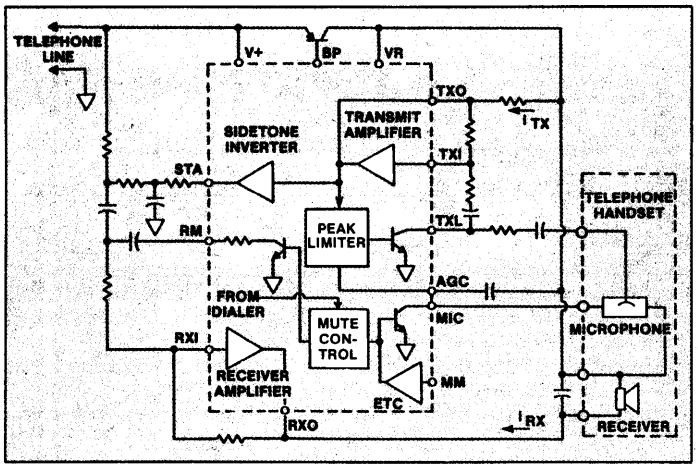


Fig. 4 Speech network block diagram.

3

the appropriate row and column tones. Binary words corresponding to keypad digits are transmitted serially to or from the microprocessor via the 4-bit shift register. The direction of data flow is determined by the state of the DD terminal input.

In the manual dialing mode, DD is a logic "0"; the 4-bit code from the keypad is fed to the DTMF generator and also loaded into the shift register. The microprocessor-controlled clock shifts the data through the I/O terminal on negative clock transitions. The shift register load-enable circuit cycles the register between the load and shift modes such that multiple read cycles may be provided to the microprocessor for a single key closure. Six complete clock cycles will output a 4-bit word from the ETC and reload the shift register for a second look.

In the automatic dialing mode, DD is a logic "1" and a 4-bit code is entered from the microprocessor into the ETC. The shift register load-enable circuit is disabled in this mode. Only four clock cycles are required to transfer a digit to be dialed into the ETC. A logic "1" on the TO terminal disables the DTMF output until valid data from the microprocessor is in place. Subsequently, TO is switched to a logic "0" to generate a DTMF tone pair on the line.

An exclusive OR circuit in the keypad interface logic determines if more than one key is depressed. Single tones may be initiated by depressing two keys in the same row or column. The exclusive OR circuit also generates the DP and MLS output signals. DP indicates when one and only one key is depressed, thereby signaling the microprocessor that valid data are available. MS indicates when the DTMF generator is enabled and the speech network is muted.

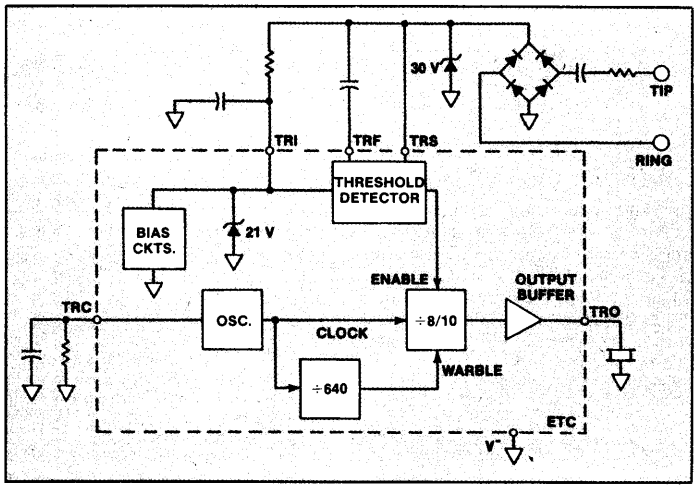


Fig. 5 Tone ringer block diagram.

Speech Network

The speech network illustrated in **Figure 4** provides the two- to four-wire interface between the telephone line and the transmit and receive transducers. The key feature of this circuit is its ability to operate with instantaneous line voltages as low as 1.4 V. Satisfactory operation has been demonstrated in parallel with a carbon microphone telephone for loop resistances of up to 2200 Ω. This corresponds to 27,000 ft of 26 AWG cable between the subscriber terminal and the local exchange.

An electret microphone biased by the VR regulator drives the transmit amplifier. The microphone is muted internally by the dialer during DTMF signaling and may be muted by the control signal on the MM terminal.

For very loud talkers, the peak limiter reduces the transmit amplifier input level to maintain low harmonic distortion. Transmit gain control is achieved by varying the saturation resistance of the transistor which drives the TXL terminal. This transistor operates as a variable resistance because its collector terminal is unbiased. The peak limiter circuit determines when the transmit amplifier output approaches the clipping level and drives the transistor at TXL to attenuate the amplifier input. The peak limiter typically provides 30-dB additional dynamic range with approximately 1 percent total distortion.

As shown in **Figure 4,** the transmit amplifier output signal is inverted at the STA terminal to provide sidetone cancellation at the receiver. The signals from the telephone line and the STA terminal are summed at the input at the receive amplifier. When transmitting, these signals are nominally 180° out of phase and the proper choice of external components will nullify the

transmitted signal in the receiver. In practice, phase shift from the transmit amplifier output to the line due to reactive line impedances limits the degree of sidetone cancellation achieved.

The receive amplifier output produces a signal current in the receive transducer that also flows through the VR regulator to the telephone line. This ac current determines the impedance of the telephone at the interface with the line. The input impedance is set by the proper choice of receive amplifier gain and receiver impedance. A 300-Ω receiver driven with a gain of one-half results in a 600-Ω input impedance and satisfactory receive sensitivity.

Tone Ringer

The tone ringer responds to large signal ac input voltages with a warbled two-tone output signal which may drive a piezo transducer or speaker. This warbled tone is produced by dividing the tone ringer oscillator frequency alternately by 8 or 10 as shown in **Figure 5.** The warble rate is the oscillator frequency divided by 640. In a typical application, an 8-kHz oscillator produces 800-Hz and 1000-Hz tones warbling at 12.5 Hz.

The tone ringer output is enabled by the threshold detector when a ringing signal greater than 35 Vrms is applied at tip and ring. The ringing signal level is measured by monitoring the voltage across the external resistor at the TRI terminal. When the average voltage across this resistor exceeds a threshold level, the output buffer commences driving the piezo element at the TRO terminal. The additional current drawn from the line to drive the piezo also flows through the external resistor at TRI. Therefore, the voltage across this resistor increases when the output is enabled. Increasing the voltage applied to the threshold detector creates hysteresis between the turn-on and turn-off levels that ensures clean on/off transitions.

DESCRIPTION

The MC34010 ETC incorporates 300 bipolar transistors and 520 I^2L gates on a 125 x 146 mil die. The chip is fabricated using a two-layer metal, Linear/I^2L process and packaged in a 40-pin plastic package. Combining a dialer, speech network, and tone ringer on a single chip represents a major step forward in the modernization and cost reduction of analog telephones. □

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MOTOROLA

Interfacing The Speakerphone To The MC34010/11/13 Speech Networks

Prepared by
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Bipolar Analog IC Division

INTRODUCTION

Interfacing the MC34018 speakerphone circuit to the MC34010 series of telephone circuits is described in this application note. The series includes the MC34010, MC34011, MC34013, and the newer "A" version of each of those. The interface is applicable to existing designs, as well as to new designs.

FUNCTIONAL REQUIREMENTS

Figure 1 shows the basic MC34010 telephone circuit as described in the data sheet. It is a completely functional telephone meant for use with a handset, and provides the additional function of a microprocessor interface for the DTMF dialing function. The MC34011 does not have the microprocessor interface, but otherwise is identical, including the pin numbers. The MC34013 has the same speech network, dialer, and line interface circuit as the MC34010, but does not have the microprocessor interface or the tone ringer. Except for a minor difference between the speech networks of the "A" version parts and the "non-A" parts, the interface to the speakerphone circuit is virtually the same for all 6 parts.

Figure 2 shows the basic MC34018 speakerphone circuit as described in the data sheet. It is NOT a complete telephone, but provides only the speakerphone functions. It requires a speech network, such as the MC34010, to transfer the speech signals to/from the Tip & Ring lines, and to provide the required supply voltage. The four external connections — transmit output, receive input, dc line input, and chip select — are the points which must be interfaced to the speech network.

In the following text, only the MC34010 interface will be described. The interface to the other parts is the same except where noted.

When combining a speech network which operates a handset, with a speakerphone circuit, certain changes are required in the circuit operation when switching between the handset mode and the speakerphone mode, and additionally when the dialing mode is in effect. The four modes to be considered are: 1) using the handset for speech, 2) using the speakerphone for speech, 3) dialing in the handset mode, and 4) dialing in the speakerphone mode. The requirements are summarized in the following table:

Mode	MC34018	Vlr	Handset Mike	Speaker-phone Mike
Handset-Speech	Unpowered	Low	Live	N/A
Spkrphone Speech	Powered	High	Dead	Live
Handset-Dialing	Unpowered	Low	Dead	N/A
Spkrphone Dialing	Powered	High	Dead	Dead

Since the entire circuit is to be powered by the phone line, the speakerphone circuit is powered up only when it is to be used since it uses a portion of the loop current, (a significant portion on long loops). The MC34010, however, must be powered all the time since it is the interface to the phone line. The Vlr voltage mentioned in the table is the voltage across the resistor at the LR pin of the MC34010, which sets the dc characteristics of the circuit. By increasing that resistor, the dc supply voltage (and the voltage at Tip & Ring) will be increased in the speakerphone modes, where additional power is required.

The handset mike is to be functional only in the handset-speech mode. If it were functional in the speakerphone-speech mode, system oscillations and/or additional echoes could occur. Disabling the microphone is accomplished by activating the MM (Mike Mute) pin on the MC34010. On the MC34010A, activating the MM pin results in disabling the transmit amplifier, so in that case, a transistor is added to the microphone circuit as the means to disable it. In both dialing modes, muting is automatic whenever the dialer is activated, so the DTMF tones are not distorted by sounds entering the microphone.

The speakerphone mike is listed as N/A in the handset modes since the MC34018 circuit is unpowered, effectively disabling the mike. In the speakerphone dialing mode it must be non-functional for the same reason as mentioned above. That is accomplished by the fact that the MC34010 (and MC34010A) transmit amplifier is inoperative when its DTMF dialer is activated.

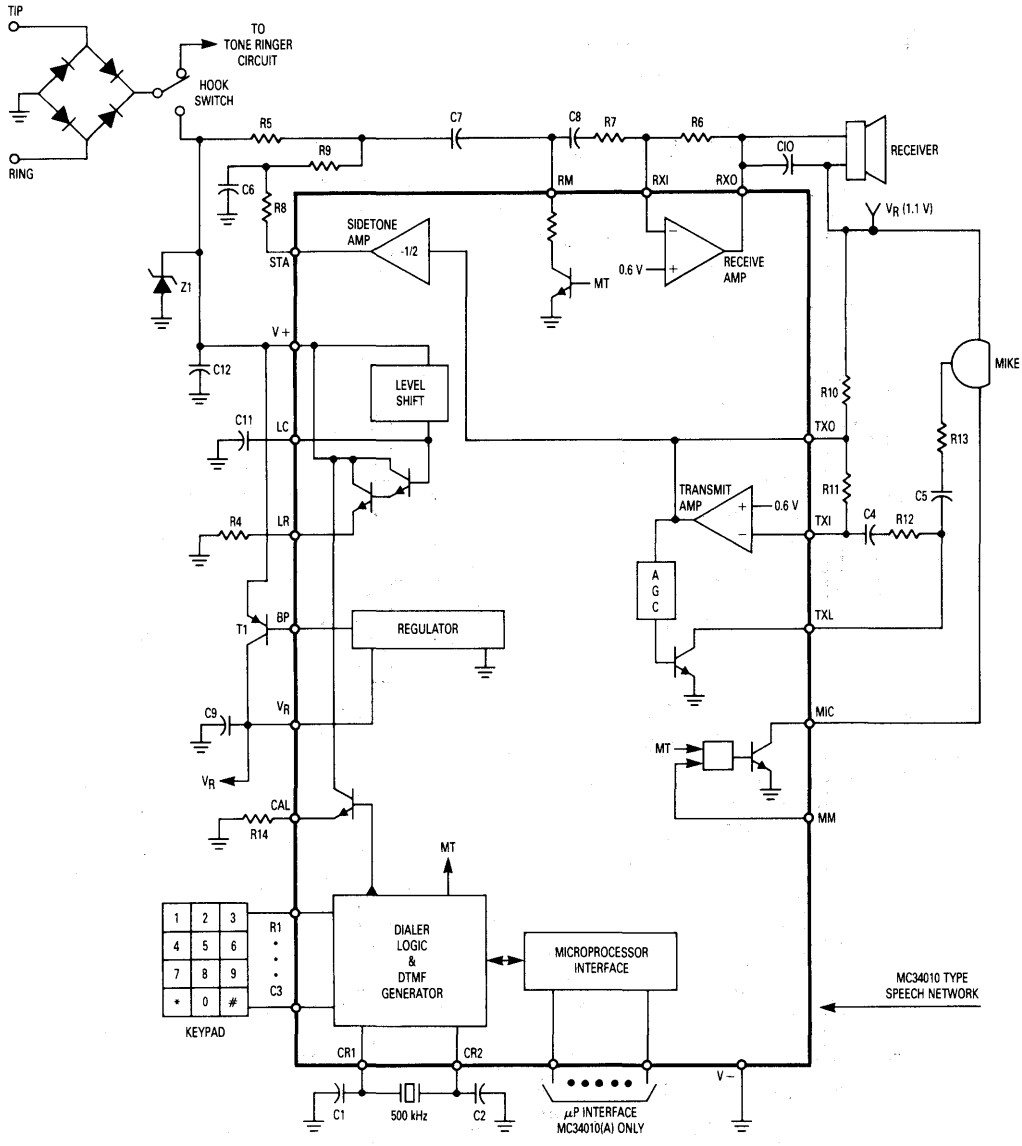


Figure 1. Basic MC34010 Type Telephone

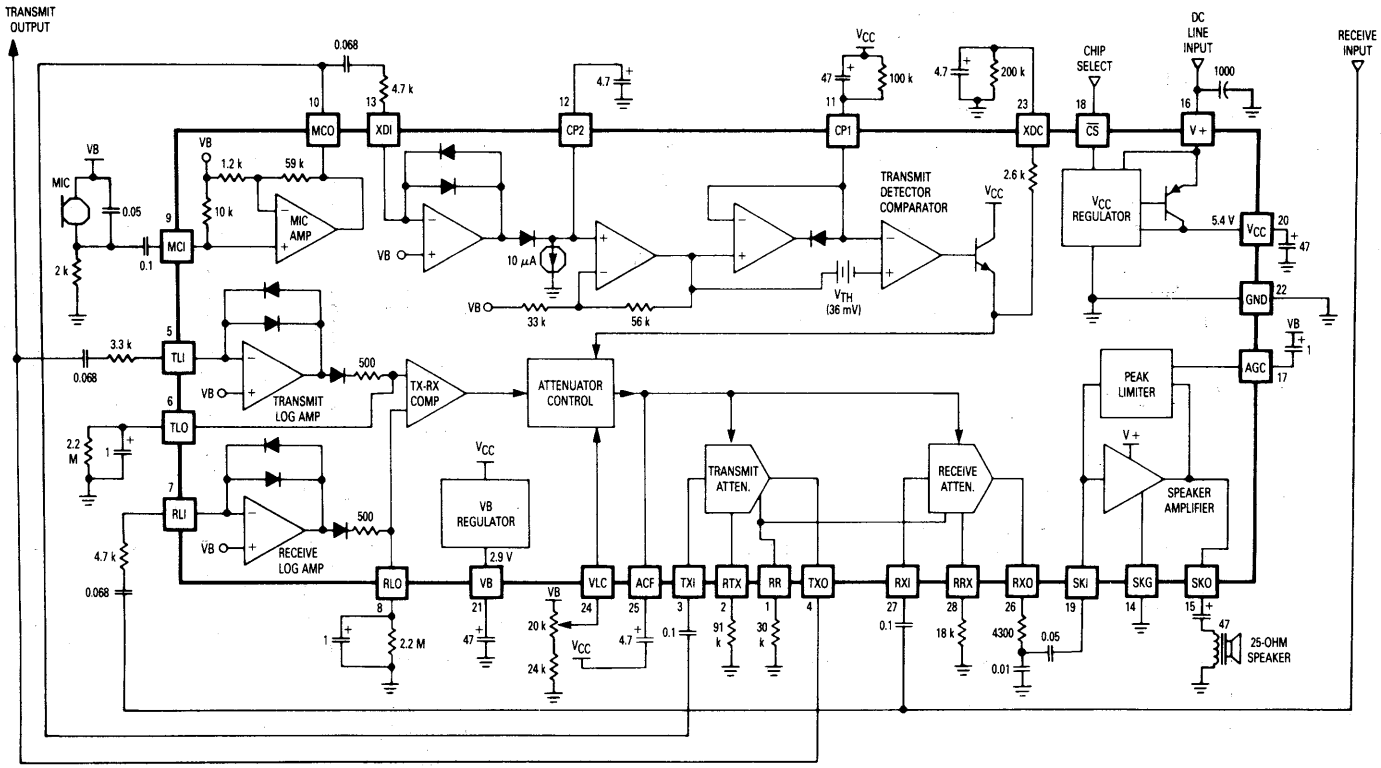


Figure 2. MC34018 Speakerphone Circuit

CIRCUIT DESCRIPTION

SWITCHING ARRANGEMENT

Figure 3 indicates the switching arrangement for going off-hook in either the handset mode or speakerphone mode, and for switching between them. S1 (a two pole switch) is the normal hook switch activated by lifting the handset. S2 (a two pole switch) is a manually operated switch which activates the speakerphone.

Whenever the handset is off-hook, and S2 is in the off position, power from Tip & Ring is applied to the MC34010 through the diode bridge and S1A. S1B's position is of no consequence in this mode. Should S2 be switched on while the handset is off-hook, power is then applied to the speakerphone IC through S2B. However, since S1B is open, the MC34018's $\overline{CS}$ pin (Chip Select) is taken high through R33, disabling the IC.

Anytime the handset is on-hook, and S2 is on (both poles closed), power is applied to both the MC34010 and the MC34018. Since S1B is closed, $\overline{CS}$ is taken low, enabling the speakerphone circuit. Anytime the handset is taken off-hook the circuit will revert back to the handset mode.

The 1.0 Henry inductor isolates the speech signals at Tip & Ring from the V+ pin of the MC34018, preventing an oscillatory loop from forming. The diode bridge, B2, is added for the tone ringer circuit of the MC34010(A), or MC34011(A), to keep the switches S1 and S2 from requiring 3 poles each.

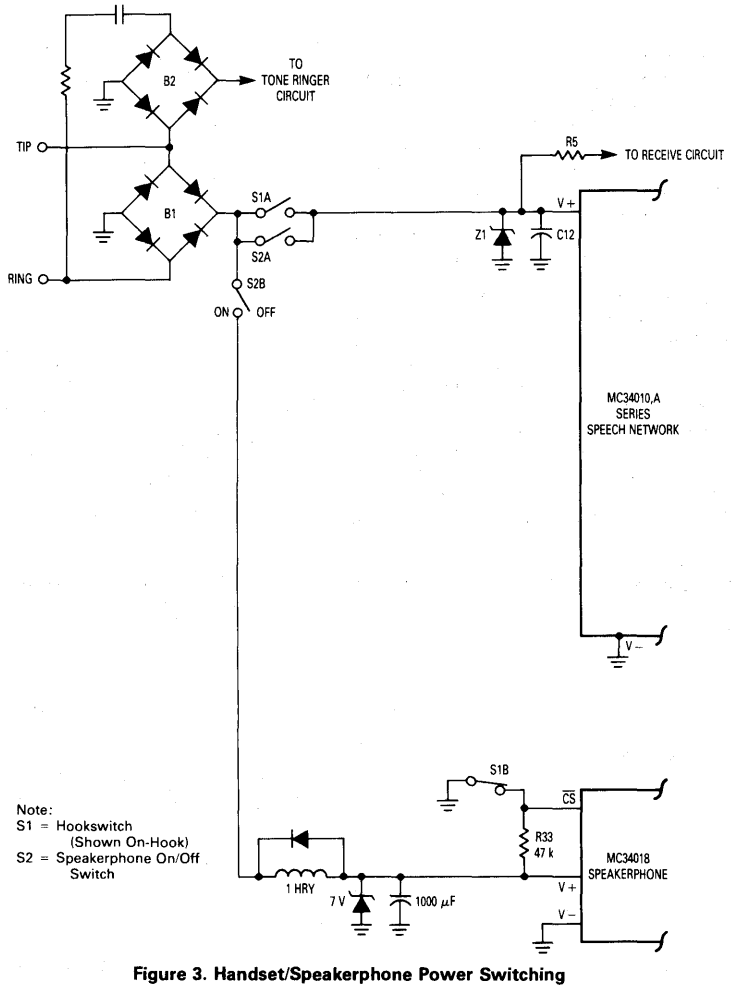


Figure 3. Handset/Speakerphone Power Switching

Vlr SHIFT

Since a speakerphone requires more power than a handset, it is necessary, particularly on long loops, to increase the Tip-Ring voltage. Since on long loops the Tip & Ring lines act more like a current source than a voltage source, increasing the voltage does not significantly decrease the available loop current. In order to shift the dc voltage, the additional components shown in Figure 4 are used. The voltage at the output of the diode bridge (B1) is equal to the voltage across the LR resistor, plus an internal level shift of approximately 3 volts between V+ and LR.

In the handset mode, the transistor T2 is on, and the equivalent LR resistance is approximately 80 ohms. The majority of the loop current (all except about 10 mA) flows through the LR resistor. In the speakerphone mode, the transistor is off, and the dc voltage is determined by the 390 ohm resistor, the internal 3 volt level shift, the resistance of the 1 Henry inductor, the 7 volt zener diode, the current draw of the two ICs, and the loop current. Figure 5 indicates the Tip-Ring voltage versus loop current for the two modes (the inductor resistance is 38 ohms).

To facilitate the design of the base drive to T2, diode D1 is added to the collector of T1, providing approximately 1.8 volts at that point. At the cathode of D1, the voltage is still regulated at 1.1 volts.

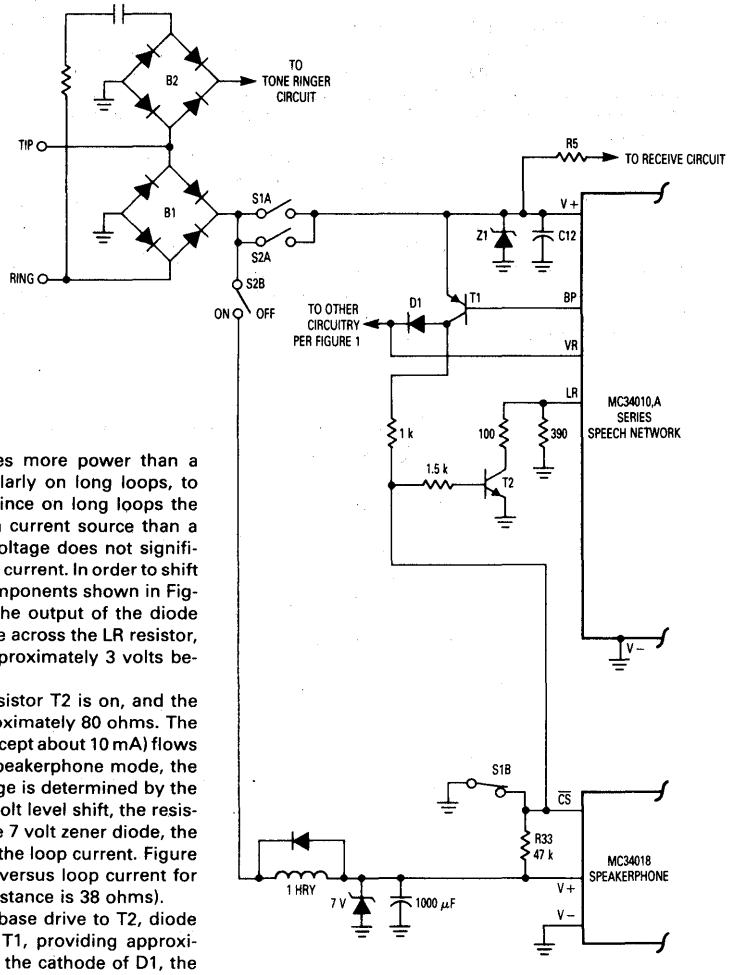


Figure 4. DC Level Shift

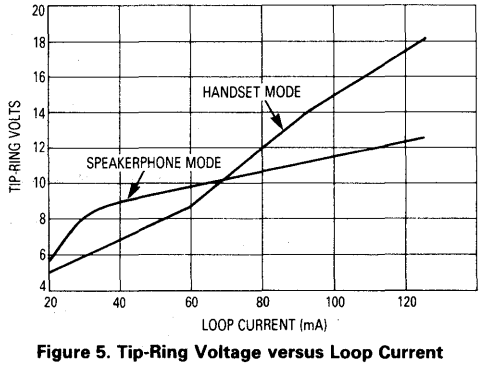


Figure 5. Tip-Ring Voltage versus Loop Current

MICROPHONE CONTROLS

To mute the handset microphone when the speakerphone speech mode is in effect, the circuit of Figure 6 is used for the MC34010 (MC34011, MC34013), and the circuit of Figure 7 is used for the MC34010A (MC34011A, MC34013A).

In Figure 6, when the handset mode is in effect, S1B takes the MM pin low, enabling the handset microphone by turning on the MIC pin (to ground). When the speakerphone mode is in effect, MM is taken high through R32, disabling the handset microphone (MIC pin is open).

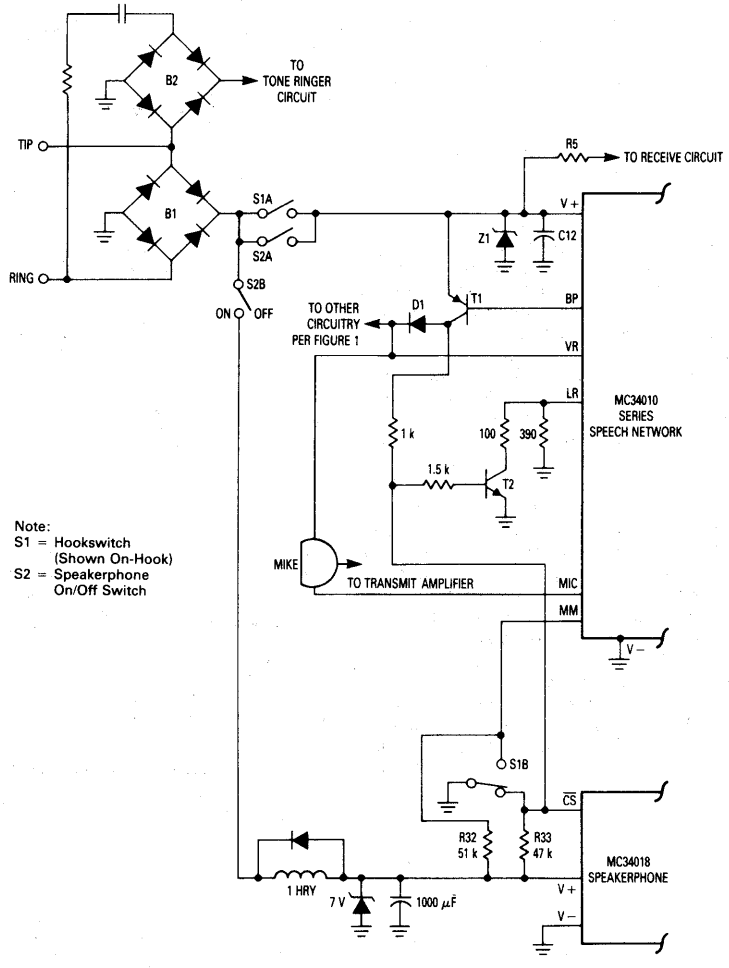


Figure 6. Microphone Muting — MC34010 Series

In Figure 7, in the handset mode, S1B is open, T3 is on, and the microphone bias current flows through the MIC pin. In the speakerphone mode, S1B is closed, turning off T3, disabling the microphone. T3 is required for disabling the microphone with the "A" series speech networks since the transmit amplifier is disabled when the MM pin is taken high.

In both the "non-A" and the "A" version circuits, the handset microphones are muted during dialing due to the fact that the MIC pin is opened by the dialer circuit.

SPEECH SIGNALS

Referring to the complete schematics (Figures 8, 9, 10, and 11) the receive signals coming in on Tip & Ring are sent to the handset receiver (at RXO) and to the speakerphone circuit's "receive input" path by the MC34010's hybrid function. It is not necessary to mute the handset receiver during speakerphone operation.

The transmit signals from the handset microphone are put onto the Tip & Ring lines through the MC34010's hybrid function, with a gain determined by resistors R27–R30. In the speakerphone mode, the transmit output signals (at TXO of the MC34018) are attenuated by R35 before being applied to the MC34010's transmit amplifier. The level of the speakerphone transmit signals at Tip & Ring can be adjusted by varying R35.

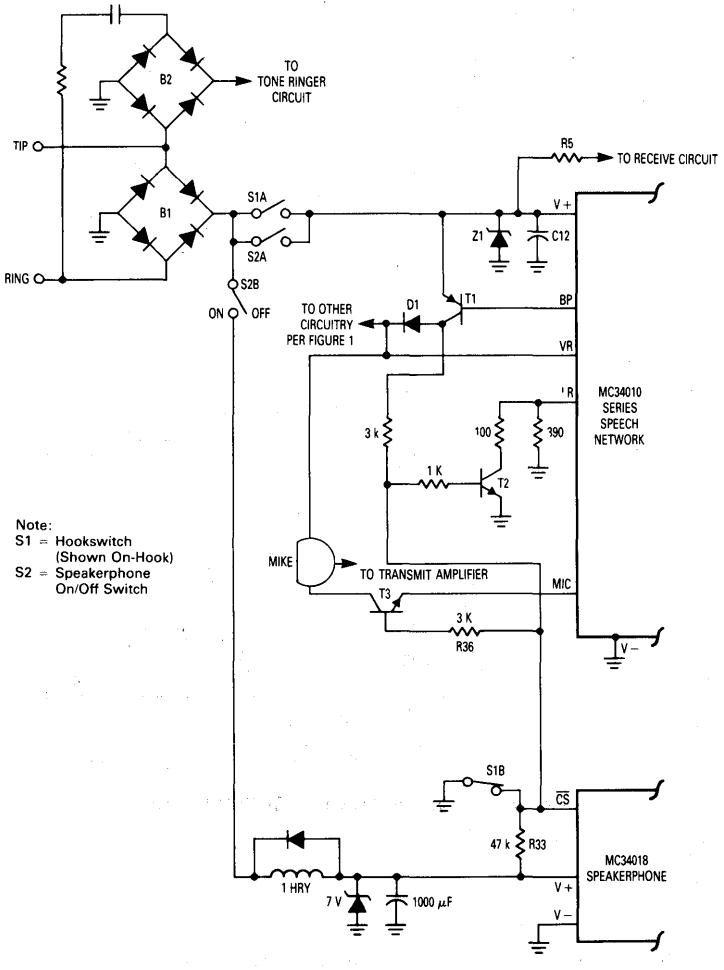
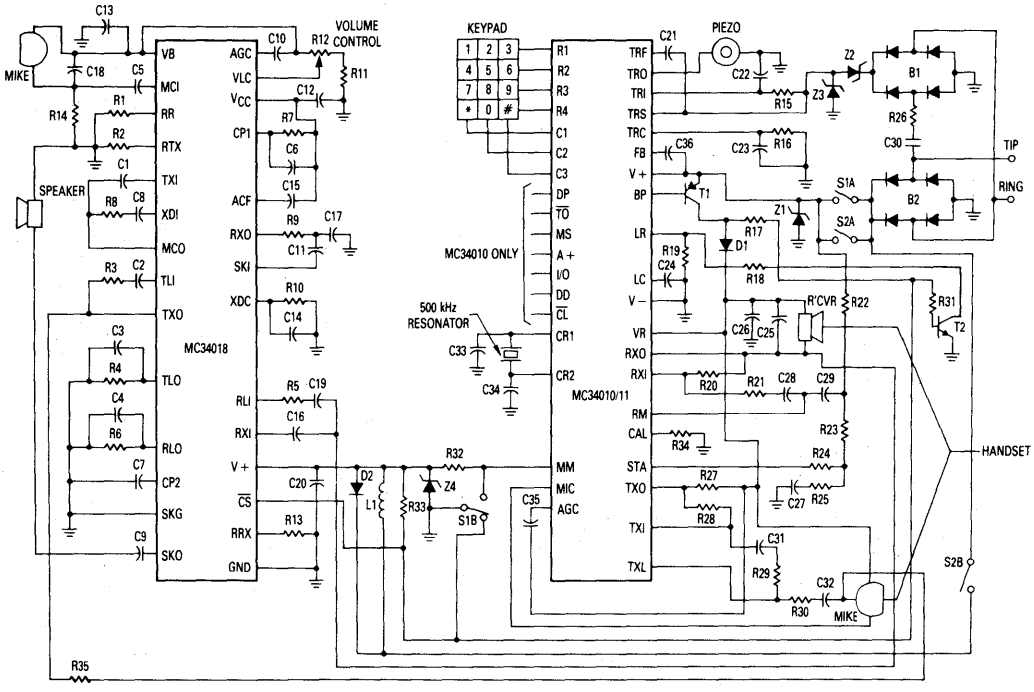


Figure 7. Microphone Muting — MC34010A Series



MC34010/11 and MC34018
COMPONENT VALUES

R1 — 30 k
R2 — 91 k
R3 — 3.3 k
R4 — 1 M
R5 — 4.7 k
R6 — 1 M
R7 — 100 k
R8 — 4.7 k
R9 — 4.3 k
R10 — 200 k
R11 — 24 k
R12 — 20 k
R13 — 18 k
R14 — 2 k
R15 — 1.8 k
R16 — 200 k
R17 — 1 k
R18 — 100
R19 — 390
R20 — 200 k
R21 — 56 k
R22 — 150 k
R23 — 56 k
R24 — 1.5 k
R25 — 1.5 k
R26 — 6.8 k
R27 — 270
R28 — 200 k
R29 — 4.7 k
R30 — 4.7 k
R31 — 1.5 k
R32 — 51 k
R33 — 47 k
R34 — 36
R35 — 33 k

C1 — 0.1
C2 — 0.068
C3 — 2.2 μF
C4 — 2.2 μF
C5 — 0.1
C6 — 47 μF
C7 — 4.7 μF
C8 — 0.068
C9 — 47 μF
C10 — 1 μF
C11 — 0.05
C12 — 47 μF
C13 — 47 μF
C14 — 4.7 μF
C15 — 4.7 μF
C16 — 0.05
C17 — 0.01
C18 — 0.05
C19 — 0.1
C20 — 1000 μF
C21 — 1 μF
C22 — 4.7 μF
C23 — 620 pF
C24 — 0.01
C25 — 0.01 μF
C26 — 2.2 μF
C27 — 0.1
C28 — 0.05
C29 — 0.05
C30 — 1 μF, NP
C31 — 0.1
C32 — 0.1
C33 — 100 pF
C34 — 100 pF
C35 — 1 μF
C36 — 0.1

L1 — 1 Hry, < 100 Ω

Z1 — 18 V
Z2 — 4.7 V
Z3 — 30 V
Z4 — 7 V
D1, D2 — 1N4001

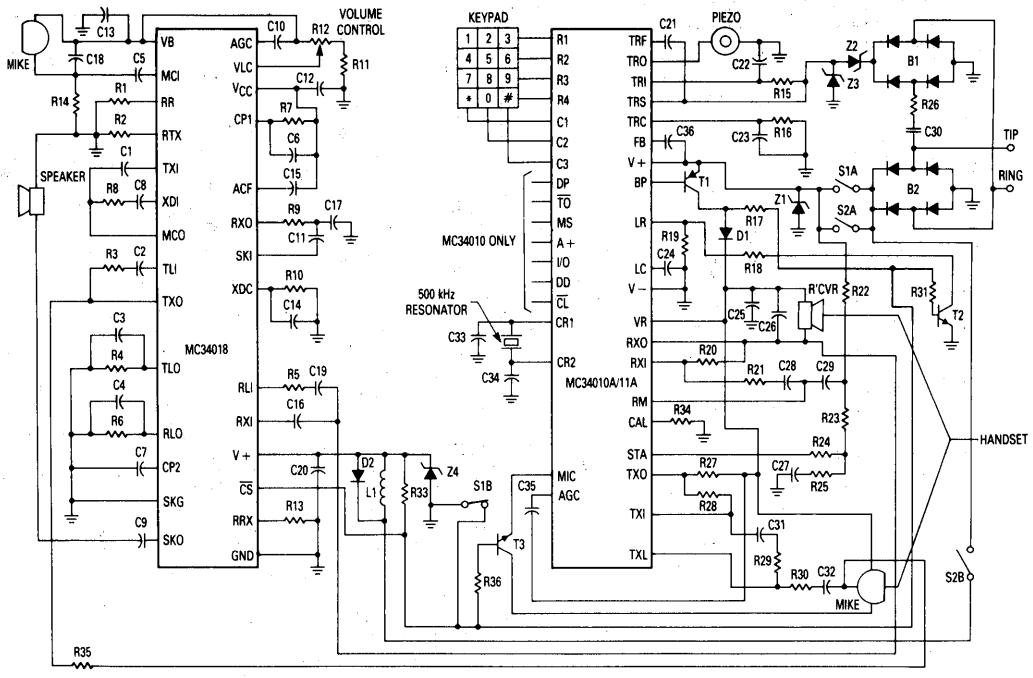
T1 — 2N4126
T2 — 2N2222A

B1 — 1N4004's
B2 — 1N4004's

S1 — DPDT (Hookswitch)
S2 — DPST (Speakerphone switch)

Handset R'cvr — 300 Ω
Handset Mike — Electret
Spkr'phone Speaker — 25 Ω, 0.3 W
Spkr'phone Mike — Electret

Figure 8. Handset/Handsfree System Using the MC34010/11 and MC34018



MC34010A/11A and MC34018 COMPONENT VALUES

R1 — 30 k
R2 — 91 k
R3 — 3.3 k
R4 — 1 M
R5 — 4.7 k
R6 — 1 M
R7 — 100 k
R8 — 4.7 k
R9 — 4.3 k
R10 — 200 k
R11 — 24 k
R12 — 20 k
R13 — 18 k
R14 — 2 k
R15 — 1.8 k
R16 — 200 k
R17 — 3 k
R18 — 100
R19 — 390
R20 — 200 k
R21 — 56 k
R22 — 150 k
R23 — 56 k
R24 — 1.5 k
R25 — 1.5 k
R26 — 6.8 k
R27 — 270
R28 — 200 k
R29 — 4.7 k
R30 — 4.7 k
R31 — 1 k
R33 — 47 k
R34 — 36
R35 — 33 k
R36 — 3 k

C1 — 0.1
C2 — 0.068
C3 — 2.2 μF
C4 — 2.2 μF
C5 — 0.1
C6 — 47 μF
C7 — 4.7 μF
C8 — 0.068
C9 — 47 μF
C10 — 1 μF
C11 — 0.05
C12 — 47 μF
C13 — 47 μF
C14 — 4.7 μF
C15 — 4.7 μF
C16 — 0.05
C17 — 0.01
C18 — 0.05
C19 — 0.1
C20 — 1000 μF
C21 — 1 μF
C22 — 4.7 μF
C23 — 620 pF
C24 — 0.1
C25 — 2.2 μF
C26 — 0.01
C27 — 0.1
C28 — 0.05
C29 — 0.05
C30 — 1 μF, NP
C31 — 0.1
C32 — 0.1
C33 — 100 pF
C34 — 100 pF
C35 — 1 μF
C36 — 0.1

L1 — 1 Hry, < 100 Ω

Z1 — 18 V
Z2 — 4.7 V
Z3 — 30 V
Z4 — 7 V

D1, D2 — 1N4001

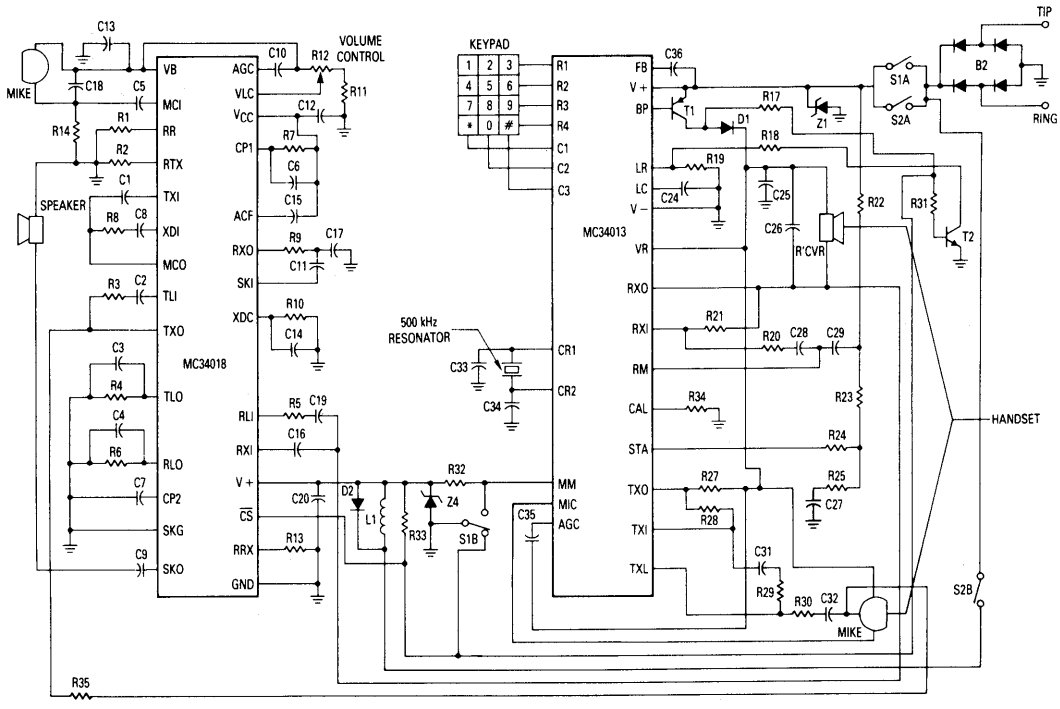
T1 — 2N4126
T2, T3 — 2N2222A

B1 — 1N4004's
B2 — 1N4004's

S1 — DPDT (Hookswitch)
S2 — DPST (Speakerphone switch)

Handset R'cvr — 300 Ω
Handset Mike — Electret
Spkr'phone Speaker — 25 Ω, 0.3 W
Spkr'phone Mike — Electret

Figure 9. Handset/Handsfree System Using the MC34010A/11A and MC34018



MC34013 and MC34018 COMPONENT VALUES

R1 — 30 k
R2 — 91 k
R3 — 3.3 k
R4 — 1 M
R5 — 4.7 k
R6 — 1 M
R7 — 100 k
R8 — 4.7 k
R9 — 4.3 k
R10 — 200 k
R11 — 24 k
R12 — 20 k
R13 — 18 k
R14 — 2 k
R17 — 1 k
R18 — 100
R19 — 390
R20 — 56 k
R21 — 200 k
R22 — 150 k
R23 — 56 k
R24 — 1.5 k
R25 — 1.5 k
R27 — 270
R28 — 200 k
R29 — 4.7 k
R30 — 4.7 k
R31 — 1.5 k
R32 — 51 k
R33 — 47 k
R34 — 36
R35 — 33 k

C1 — 0.1
C2 — 0.068
C3 — 2.2 μF
C4 — 2.2 μF
C5 — 0.1
C6 — 47 μF
C7 — 4.7 μF
C8 — 0.068
C9 — 47 μF
C10 — 1 μF
C11 — 0.05
C12 — 47 μF
C13 — 47 μF
C14 — 4.7 μF
C15 — 4.7 μF
C16 — 0.05
C17 — 0.01
C18 — 0.05
C19 — 0.1
C20 — 1000 μF
C24 — 0.1
C25 — 2.2 μF
C26 — 0.01
C27 — 0.1
C28 — 0.05
C29 — 0.05
C31 — 0.1
C32 — 0.1
C33 — 100 pF
C34 — 100 pF
C35 — 1 μF
C36 — 0.1

L1 — 1 Hry, < 100 Ω

Z1 — 18 V
Z4 — 7 V

D1, D2 — 1N4001

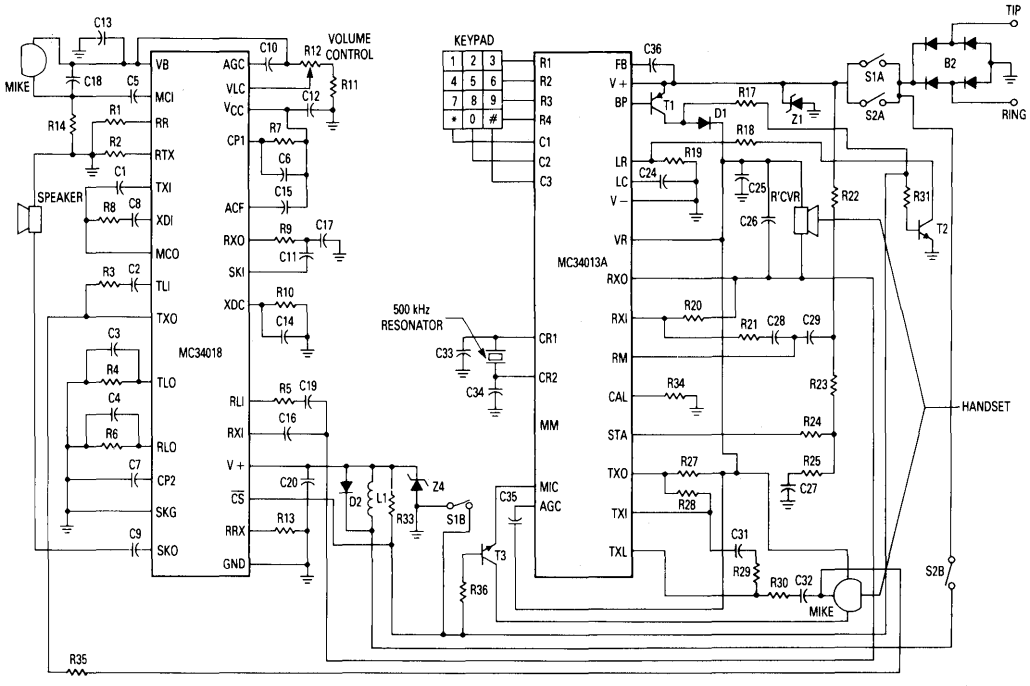
T1 — 2N4126
T2 — 2N2222A

B2 — 1N4004's

S1 — DPDT (Hookswitch)
S2 — DPST (Speakerphone switch)

Handset R'cvr — 300 Ω
Handset Mike — Electret
Spkr'phone Speaker — 25 Ω, 0.3 W
Spkr'phone Mike — Electret

Figure 10. Handset/Handsfree System Using the MC34013 and MC34018



MC34013A and MC34018 COMPONENT VALUES

R1 — 30 k
R2 — 91 k
R3 — 3.3 k
R4 — 1 M
R5 — 4.7 k
R6 — 1 M
R7 — 100 k
R8 — 4.7 k
R9 — 4.3 k
R10 — 200 k
R11 — 24 k
R12 — 20 k
R13 — 18 k
R14 — 2 k
R17 — 3 k
R18 — 100
R19 — 390
R20 — 56 k
R21 — 200 k
R22 — 150 k
R23 — 56 k
R24 — 1.5 k
R25 — 1.5 k
R27 — 270
R28 — 200 k
R29 — 4.7 k
R30 — 4.7 k
R31 — 1 k
R33 — 4.7 k
R34 — 36
R35 — 33 k
R36 — 3 k

C1 — 0.1
C2 — 0.068
C3 — 2.2 μF
C4 — 2.2 μF
C5 — 0.1
C6 — 47 μF
C7 — 4.7 μF
C8 — 0.068
C9 — 47 μF
C10 — 1 μF
C11 — 0.05
C12 — 47 μF
C13 — 47 μF
C14 — 4.7 μF
C15 — 4.7 μF
C16 — 0.05
C17 — 0.01
C18 — 0.05
C19 — 0.1
C20 — 1000 μF
C24 — 0.1
C25 — 2.2 μF
C26 — 0.01
C27 — 0.1
C28 — 0.05
C29 — 0.05
C31 — 0.1
C32 — 0.1
C33 — 100 pF
C34 — 100 pF
C35 — 1 μF
C36 — 0.1

L1 — 1 Hry, < 100 Ω

Z1 — 18 V
Z4 — 7 V

D1, D2 — 1N4001

T1 — 2N4126
T2, T3 — 2N2222A

B2 — 1N4004's

S1 — DPDT (Hookswitch)
S2 — DPST (Speakerphone switch)

Handset R'cvr — 300 Ω
Handset Mike — Electret
Spkr'phone Speaker — 25 Ω, 0.3 W
Spkr'phone Mike — Electret

Figure 11. Handset/Handsfree System Using the MC34013A and MC34018

CONCLUSION

Interfacing the MC34018 speakerphone circuit to the MC34010 series of speech networks has been shown to be simple and straightforward. The interface requires the addition of 2 diodes, 5 resistors, either 1 or 2 transistors (depending on the speech network), and one diode bridge for the tone ringer circuit in the MC34010(A) and the MC34011(A). Any existing MC34010 type circuit can be easily modified to accept the speakerphone circuit.

REFERENCES

MC34010 Data Sheet, Dec. 1983, Motorola, Inc.
MC34010A Data Sheet, May, 1985, Motorola, Inc.
MC34013 Data Sheet, Nov. 1983, Motorola, Inc.
MC34013A Data Sheet, Feb. 1985, Motorola, Inc.
MC34018 Data Sheet, Apr. 1985, Motorola, Inc.

MOTOROLA

Transmit Gain Adjustments For The MC34014 Speech Network

By
Scott Bader and Dennis Morgan
Bipolar Analog IC Division

INTRODUCTION

The MC34014 telephone speech network provides for direct connection to an electret microphone and to Tip and Ring. In between, the circuit provides gain, drive capability, and determination of the ac impedance for compatability with the telephone lines. Since different microphones have different sensitivity levels, different gain levels are required from the microphone to the Tip and Ring lines. This application note will discuss how to change the gain level to suit a particular microphone while not affecting the other circuit parameters.

CIRCUIT DESCRIPTION

Refer to Figure 1. The microphone is assumed to be an electret type, characterized by a high dynamic impedance. It is therefore considered to be an ac current source rather than a voltage source. If the microphone used has a dynamic impedance which is not high (compared to R_8), then the microphone must be modeled as a current source paralleled by its dynamic impedance. That impedance value must then be considered to be in parallel with R_8 in the following equations. The T_X amplifier has a fixed gain of -20, and the EQ amplifier gain varies from 0.25 to 0.75, depending on the loop current. Z_L is the line impedance. The transmit gain is defined as $V+/I_{mic}$ and is equal to:

$$\frac{V+}{I_{mic}} = \frac{R_6 \times Z_L \times A_{TX}}{(1 + R_6/R_A)R_9 + (A_{TX})\ (A_{EQ})\ (Z_L)}$$

where A_{TX} = gain of the transmit amplifier (20 V/V)
A_{EQ} = gain of the equalization amp. (0.25 to 0.75 V/V)
R_A = R_8//10 kΩ (10 kΩ = input impedance of Tx amp.)

The ac impedance of the circuit is defined as:

$$Zac = \frac{R_9\ (1 + R_6/R_A)}{(A_{TX})\ (A_{EQ})}$$

The receive gain (see data sheet for the equivalent circuit) is defined as:

$$Grx = \frac{R_4}{R_1} + \frac{(X_C//R_2)\ (A_{EQ})\ (A_{TXO})\ (A_{STA}) \times R_4}{((X_C//R_2) + R_3)\ (1 + R_6/R_A) \times R_2}$$

As can be seen from the above equations, changing R_6 while maintaining the R_6/R_A ratio constant will result in a transmit gain change (proportional to R_6) but will not affect the other parameters. For example, increasing R_8 and R_6 by a factor of 3 will increase the transmit gain by ≈10 dB.

Using the above procedure to increase the transmit gain results in increasing R_8, which supplies the bias current to the microphone. If the higher value of R_8 results in insufficient bias voltage at the microphone, then the alternate biasing scheme of Figure 2 should be used.

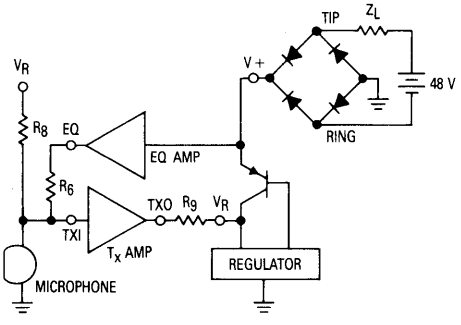


Figure 1. MC34014 Transmit Section

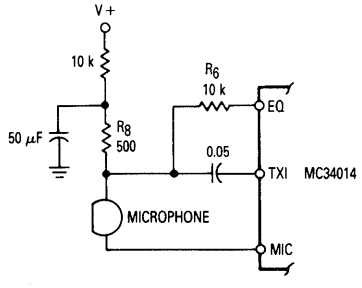


Figure 2. Alternate Biasing Scheme for Higher Voltage Microphones

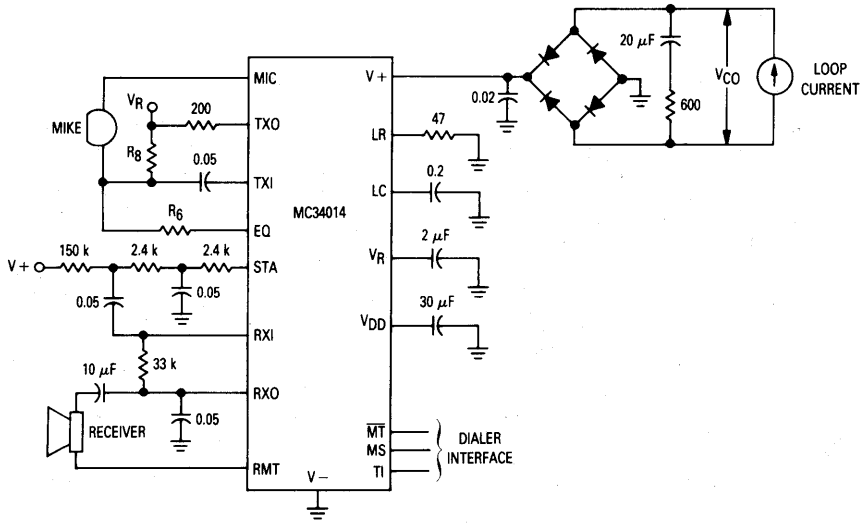
TEST RESULTS

Tests were conducted with a Primo EM-95A microphone, having a sensitivity of −53 dB ±3 dB (0 dB = 1 V/μbar), and a Hosiden KUC2123 microphone which has a sensitivity of −60 dB ±3 dB. The test circuit is shown in Figure 3. The tests consisted of applying a constant sound level to the microphones, and measuring the output at V_{CO}, while simulating line lengths of 0–21 Kfeet. The outputs of the two circuits were nearly identical at all line lengths.

CONCLUSION

Although the designs of the various parameters (transmit gain, receive gain, ac impedance, etc.) of the MC34014 speech network are not mutually exclusive due to the commonality of various components, it is possible to adjust the transmit gain independently to suit a particular microphone.

For further information on the MC34014 speech network, refer to the data sheet.



For Primo EM-95A microphone R_8 = 500 Ω, R_6 = 10 k
For Hosiden KUC2123 microphone R_8 = 1.5 k, R_6 = 30 k

Figure 3. Microphone Gain Test Circuit

MOTOROLA

A Speakerphone With Receive Idle Mode

By
Dennis Welty and Dennis Morgan
Bipolar Analog IC Division

INTRODUCTION

The MC34018 speakerphone system operates on the principle of comparing the transmit and receive signals to determine which is stronger, and then switching the circuit into that mode. Under conditions where noise from the telephone line (in the receive path) exceeds the background noise in the transmit path, the speakerphone will switch easily, or even lock, into the receive mode. Under these conditions the conversation will sound "dead" to the party at the far-end. It will also be more difficult for the near-end party to activate the transmit channel since the transmit detection is at the output of the transmit attenuator, which will be at maximum attenuation during this time. The addition of a receive idle mode can alleviate this problem by ensuring that the transmit and receive gains will be approximately equal when no voice signals are present. This allows the far-end party to hear ambient noises, and also increases the sensitivity to transmit signals.

CIRCUIT DESCRIPTION

The additional circuitry is shown in Figure 1. The receive signal normally applied to RXI also drives XDI through a 2.7 kΩ resistor and a 0.1 μF capacitor. XDC is connected to VLC through the NPN and PNP emitter followers. When voice signals in the receive channel exceed the background noise by 4.6 dB, XDC switches high and turns off the PNP transistor (the 4.6 dB threshold is built into the MC34018). The voltage at VLC is then determined by the volume control potentiometer. When voice signals are no longer present, XDC decays to 0.5 VB and turns on the emitter followers. The voltage at VLC is now determined by the voltage at XDC. By decreasing the VLC voltage with the emitter followers the transmit and receive gains are adjusted to produce a receive-idle mode.

A peak detector using an external voltage comparator and diode is required to hold the receive attenuator fully on (out of the idle mode) when constant level signals, such as dial tone, are intentionally presented to the re-

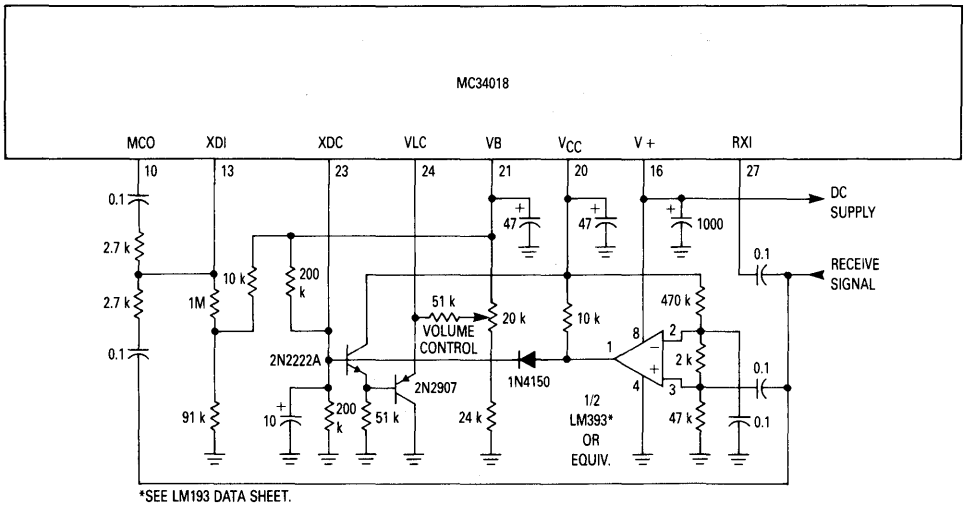


Figure 1. Receive-Idle Circuit

ceive channel. When the receive signal at the receive input exceeds the threshold on the comparator (typically 20 mV) the peak detector charges the capacitor at XDC which prevents the speakerphone from relaxing to the idle mode. The PNP transistor is turned off and the voltage at VLC is then determined by the volume control potentiometer. Under these conditions the speakerphone will be in the receive mode.

The sensitivity threshold of the voice detector circuitry can be changed by applying a dc current to XDI. The threshold current (nominally 250 nA) also prevents XDC from switching sporadically in quiet signal conditions. The threshold current is determined by the 1 Megohm resistor between XDI and the 10 kΩ/91 kΩ divider referenced to VB. Whenever receive signal currents exceed the threshold current by 4.6 dB, the voice detector will respond and allow XDC to switch high.

CONCLUSION

The receive-idle mode is simple to implement, and improves the performance of the speakerphone system by allowing noise rejection in both the receive and transmit channels. The voice-switching function operates only on valid speech, and ignores background noises.

REFERENCES

MC34018 data sheet, Motorola, 1985
LM193 data sheet, Motorola

MOTOROLA

Equalization of DTMF Signals Using the MC34014

by
Scott Bader and Dennis Morgan
Bipolar Analog IC Division

INTRODUCTION

This application note will describe how to obtain equalization (line length compensation) of the DTMF dialing tones using the MC34014 speech network. While the MC34014 does not have an internal dialer, it has the interface for a dialer so as to provide the means for putting the DTMF tones onto the Tip & Ring lines. The Equalization amplifier, whose gain varies with loop current, was meant primarily to equalize the speech signals. However, by adding one resistor, it can be used to equalize the DTMF signals as well.

CIRCUIT DESCRIPTION

Referring to Figure 1, the gain of the equalization amplifier varies with loop current as it is a function of the voltage at the LR pin (Pin 13). The gain varies from a minimum of −12 dB at low loop currents (long line), to −2.5 dB at high loop currents (short line). The output at EQ (Pin 6) is in phase with the signals going out onto Tip & Ring, but is out of phase with the DTMF input signals from the dialer at R7 (see Figure 2). Because of the out-of-phase relationship, the signal at EQ can be used to partially cancel the signals at the Tone Input (Pin 16). The addition of resistor R10 provides the path for this function, with the result that the DTMF gain increases as loop current decreases.

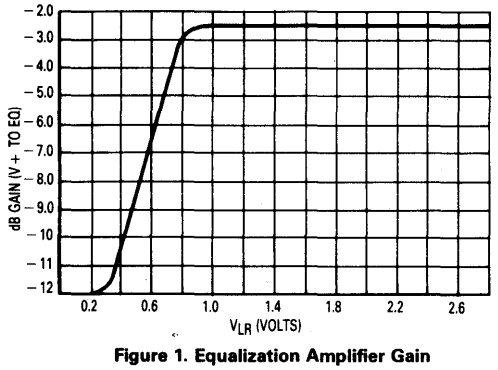


Figure 1. Equalization Amplifier Gain

Because the addition of R10 cancels some of the signal going into Pin 16, resistor R7 must be decreased in order to restore the overall gain from the dialer to Tip & Ring.

The DTMF gain values indicated in Figures 3 and 4 is the gain from the tone dialer (input at R7) to the Tip & Ring lines terminated with a 600 ohm resistor. Figure 3 indicates the gain CHANGE (as the loop current is varied from 60 to 20 mA) versus different values of R10. The gain change is a function of R10, and independent of R7. Figure 4 indicates the DTMF gain versus R7 for different values of R10 at a loop current of 20 mA.

Because the typical telephone line is not purely resistive, there will be a phase shift of other than 180° from the DTMF dialer to Tip & Ring in most applications. For this reason, the values of R10 and R7 will have to be adjusted slightly from those in the graphs to compensate for the phase shift.

The MC34014 data sheet mentions that a dc bias current of 20–50 μA is required into Pin 16 in order to bias the DTMF amplifier. The addition of R10 will provide the bias current from the EQ output for most applications, in which case it may be desirable to ac couple the dialer to R7 with a 0.5 μF capacitor. Excessive bias current will result in clipping of the signals at Tip & Ring. If just the addition of R10 results in excessive bias current, then the EQ output should be ac coupled to R10 with a 0.5 μF capacitor, and the bias current supplied either from the dialer or from an additional resistor as shown in Figure 5.

For further information on the MC34014, refer to its' data sheet.

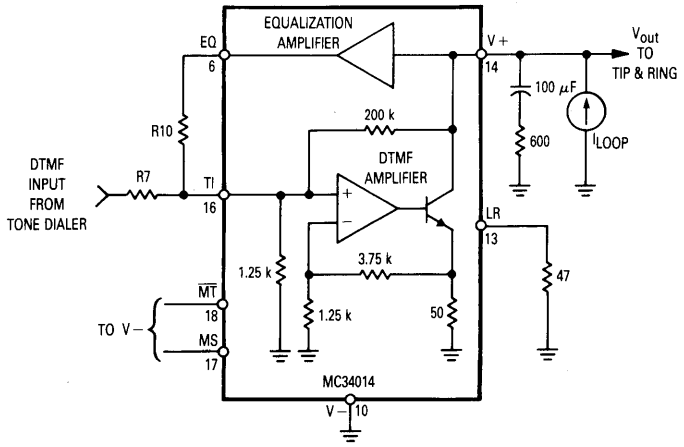


Figure 2. DTMF Driver

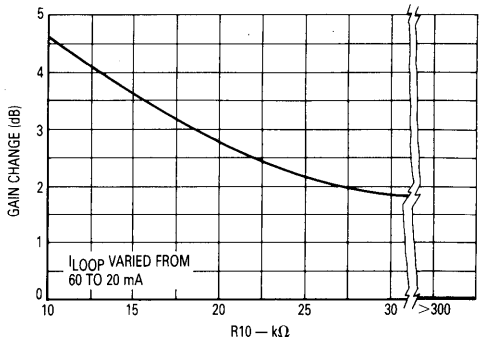


Figure 3. Gain Change

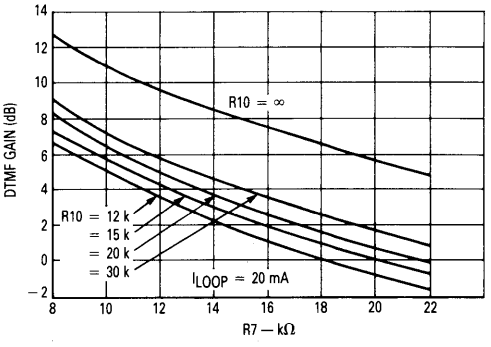


Figure 4. DTMF Gain

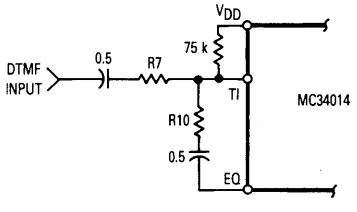


Figure 5. Alternate Biasing

MOTOROLA

THE APPLICATION OF A TELEPHONE TONE RINGER AS A RING DETECTOR

By Tanya Tussing and Glen Zoerner
Telecommunication Applications
Austin, Texas

Telephone ringers are driven by high voltage, low frequency ac signals which are superimposed on the 48 volt dc tip-ring feed voltage. An electronic ring detector must sense the presence of an ac signal on the line and produce a dielectrically isolated logic level to the system processor. To isolate the line from the system, an on-chip piezoelectric driver drives the LED of an optocoupler. A 1 μF capacitor filters the transistor output of the optocoupler, creating a solid logic 0 when a ring signal is present. Figure 1 depicts the schematic of the ring detector. The peripheral components around the MC34012 set trigger levels and the ringing impedance signature for FCC Part 68 compliance.

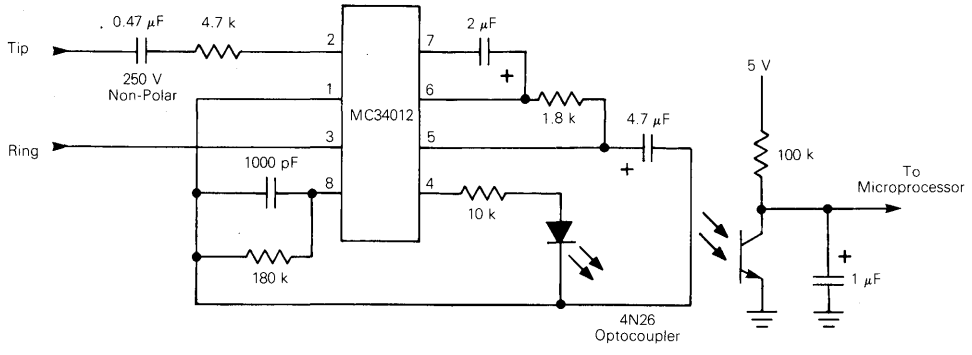


FIGURE 1 — Ring Detector Schematic

MOTOROLA

THE MC145409 PULSE DIALER APPLICATION CIRCUIT

by Roger Taylor
Telecommunication Applications
Austin, Texas

The purpose of this document is to describe a circuit for interfacing the MC145409 pulse dialer with a telephone system. The MC145409 is a monolithic CMOS integrated circuit which converts 2 of 7 keyboard inputs into pulse signals that simulate a rotary telephone dialer. It uses an inexpensive RC oscillator, operates directly off of telephone line supply, and consumes only microamperes of current when not outpulsing.

When off-hook, power is supplied through a constant current source consisting of Q1, R1, D5, D6, and R9. To keep the circuit's power consumption low, D5 and D6 are partially forward biased. As line voltage increases, voltage applied to the MC145409 increases as D5 and D6 become more forward biased necessitating zener diode, Z2, to provide adequate regulation. On-hook power for memory retention is supplied through R10. Diode, D7, is required to keep the on-hook current below the Bell specification of five microamperes maximum.

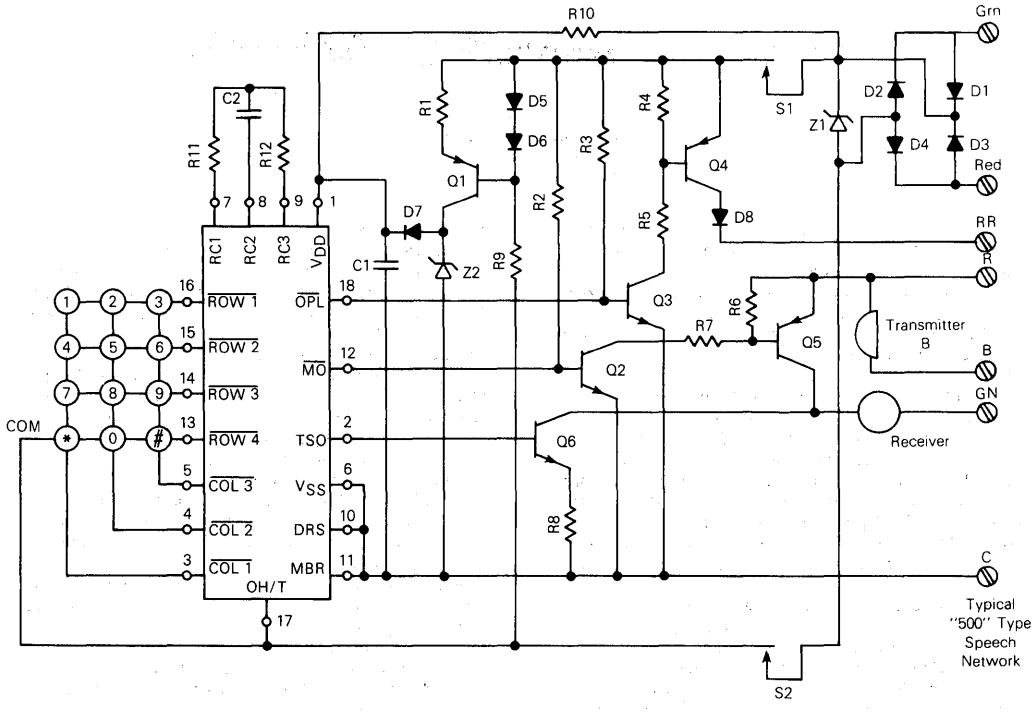
When off-hook, the oscillator is enabled when a valid key input is detected. The MC145409 senses key depressions, verifies that a single key is depressed, and stores the key's code in on-chip memory. If the first key depressed is a * or #, memory redial is initiated (provided the receiver has been on-hook for the minimum time). Otherwise, memory is cleared during a predigital pause, after which outpulsing commences. The receiver is muted during outpulsing.

The mute and outpulsing functions are accomplished through the circuitry containing transistors Q2 through Q5. The mute and outpulsing pins (12 and 18 respectively) are in an open drain configuration, so transistors Q2 and Q3 are forward biased by connecting their bases to the supply through pull-up resistors R2 and R3. Muting occurs when pin 12 pulls to V_{SS}. Transistor Q2 turns off, terminating current flow through R7. Transistor Q5 turns off as the base and emitter voltages equalize, muting the receiver.

Outpulsing is accomplished in a similar manner. A pulse is created when pin 18 pulls to V_{SS}. Transistor Q3 turns off, stopping current flow through R5. The base and emitter voltages of Q4 equalize through R4, shutting the transistor off, interrupting current flow through the speech network, thereby creating a pulse on the phone line.

During a key depression, the MC145409 outputs a tone signal at Pin 2. This signal drives the base of Q6, which in turn modulates the voltage at the receiver, creating an audible tone at 1 kilohertz for 10 pulse per second or 2 kilohertz for 20 pulse per second. The volume of this tone is controlled by R8. An increase in R8 corresponds to a decrease in tone level at the receiver.

TELEPHONE DIALER APPLICATION CIRCUIT



R1 = 1.4 k
R2 = 470 k
R3 = 330 k
R4 = 100 k
R5 = 3 k
R6 = 100 k
R7 = 3 k
R8 = 20 k

R9 = 560 k
R10 = 10 M
R11 = 2 M
R12 = 220 k

C1 = 68 μF low leakage
C2 = 390 pF

D1-D4 = IN4004
D5-D7 = IN914
D8 = IN4004

Z1 = 120 V, IW
Z2 = 5 V, 500 mW

Q1 = 2N5401
Q2 = 2N5550
Q3 = 2N5550
Q4 = 2N5401
Q5 = 2N5401
Q6 = 2N5550

LOW-SPEED MODEM FUNDAMENTALS

Prepared by:
Garth Nash
Computer Systems Engineering

GENERAL

The MC6860 low-speed Modem can be used in many different configurations. These include full duplex, half duplex, simplex, automatic answering, automatic disconnect, originate only, answer only, answer/originate, and others. Figure 1 illustrates the basic modem configuration used to evaluate the MC6860. An originate only and an answer only modem design is used for evaluation, and each section of the interface circuitry is dealt with in this article.

The originate modem transmits on the low-frequency channel (Mark 1270 Hz and Space 1070 Hz) and receives on the high-frequency channel (Mark 2225 Hz and Space 2025 Hz). The answer modem transmits on the upper channel and receives on the lower.

A buffer and duplexer as shown in Figure 1 provide the modem interface to the transmission network while the bandpass filter allows only the desired receive signals to be seen by the limiter and demodulator.

MODULATOR – BUFFER

Mark/Space information that is presented to the Transmit Data input of the modem is converted to an FSK signal for transmission. The modulator output is an approximated sinewave derived from a digital-to-analog converter within the MC6860. There are eight amplitude levels per cycle. Each step has been optimized such that the composite waveform has a maximum amount of signal energy at the fundamental. Figure 2 shows the 1270 Hz transmit carrier and Figure 3 gives its spectral distribution. A nominal signal has the second harmonic attenuated to -30 dB.

The modulator output impedance is typically 2 k ohms. Loading this output with an impedance less than 100 k ohms can produce harmonic distortion. Therefore, a buffer amplifier is required to match impedances to the duplexer and the telephone line. This buffer amplifier may be designed to also provide filtering if additional clean-up of the transmitted signal is required.

The modulation spectrum for 300 bits per second using an alternate Mark/Space data format is shown in Figure 4. The amount of modulation or sideband energy that falls in the adjacent channel is an item of concern in full duplex operation. Under this condition both channels are operating simultaneously and all the adjacent channel energy that is not balanced out in the duplexer feeds directly through the bandpass filter and to the limiter. Excessive phase jitter results if the received signal level is low enough to approach that of the interference level at the limiter input. For this reason, additional filtering of the modulator output may be required before it feeds to the duplexer on those modem designs desiring wide dynamic ranges of input signal levels.

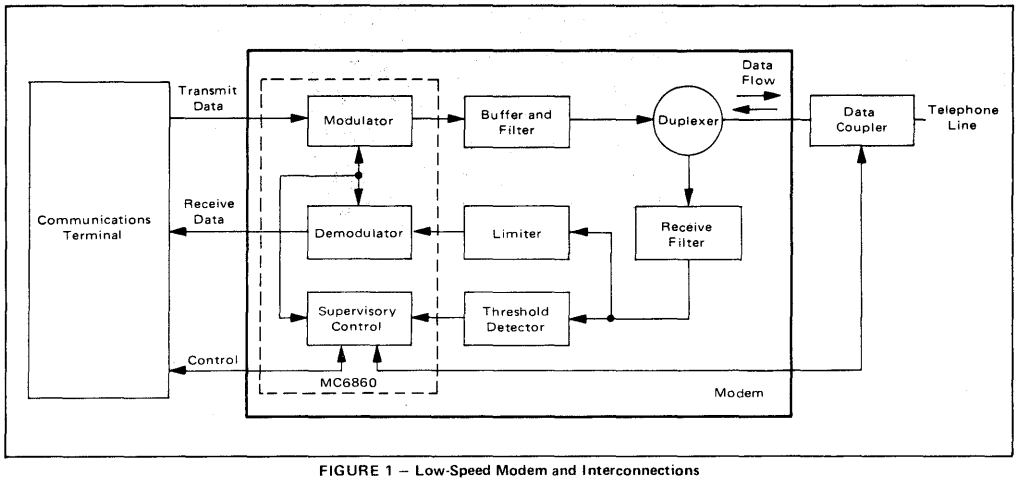


FIGURE 1 – Low-Speed Modem and Interconnections

Interference by the second harmonic is of concern in the originate mode only. In this mode, the transmit signal is in the low band and its second harmonic falls in or near the passband of the return channel. In half duplex operation, the transmit carrier is held at a constant Mark (1270 Hz) while data is being received. The second harmonic (2540 Hz), which is typically -30 dB or more below the fundamental in amplitude, falls just outside the passband of the receive filter and is further attenuated. In full duplex operation, the second harmonic and the modulation sidebands have about the same amount of energy. If this undesired energy must be reduced, the filter used to reduce the modulation sidebands will also reduce the second harmonic. Phase jitter and bias distortion inherent in the modulator is less than 3 μs.

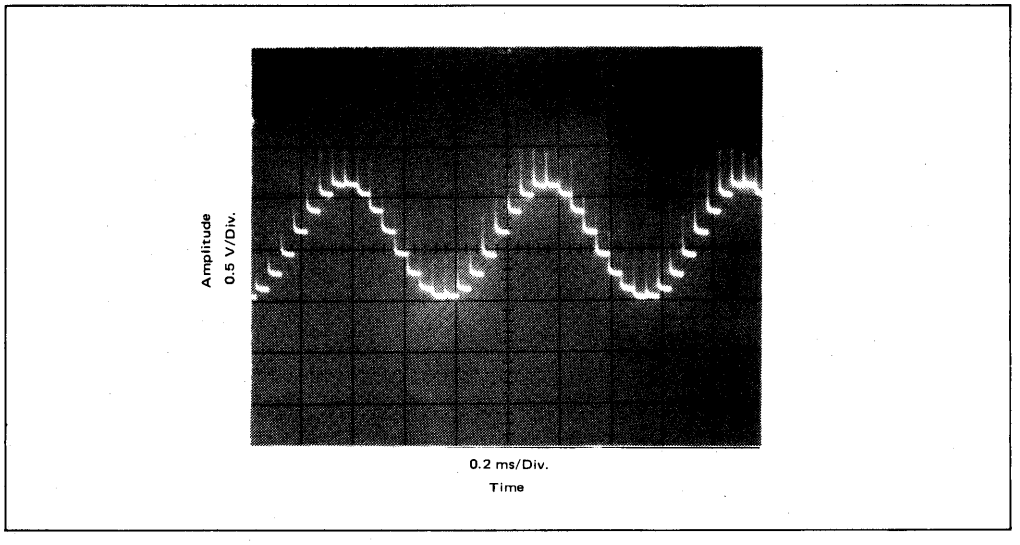


FIGURE 2 – MOS Synthesized 1270-Hz Sine Wave

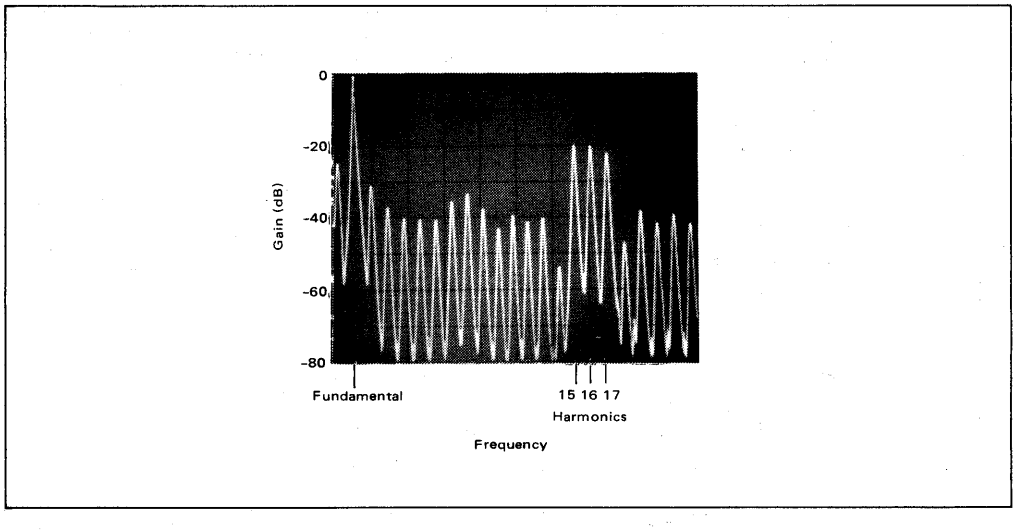


FIGURE 3 – Frequency Spectrum of MOS Sine Wave

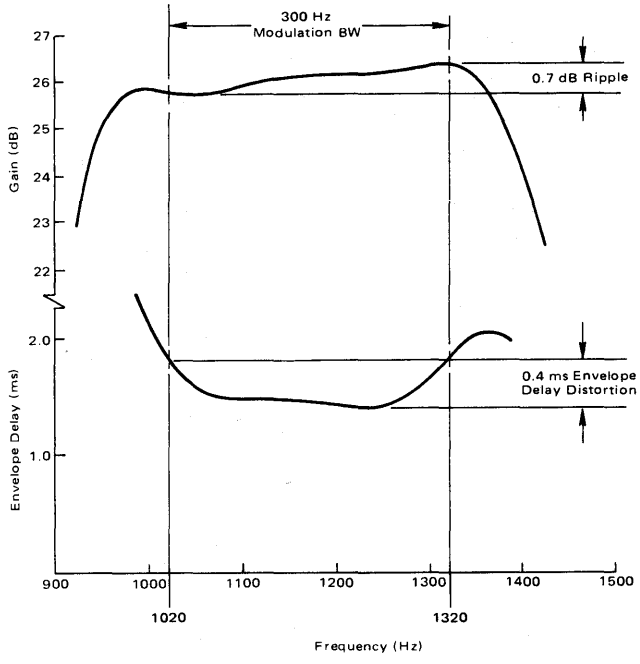


FIGURE 8 – Answer Bandpass Filter Characteristics

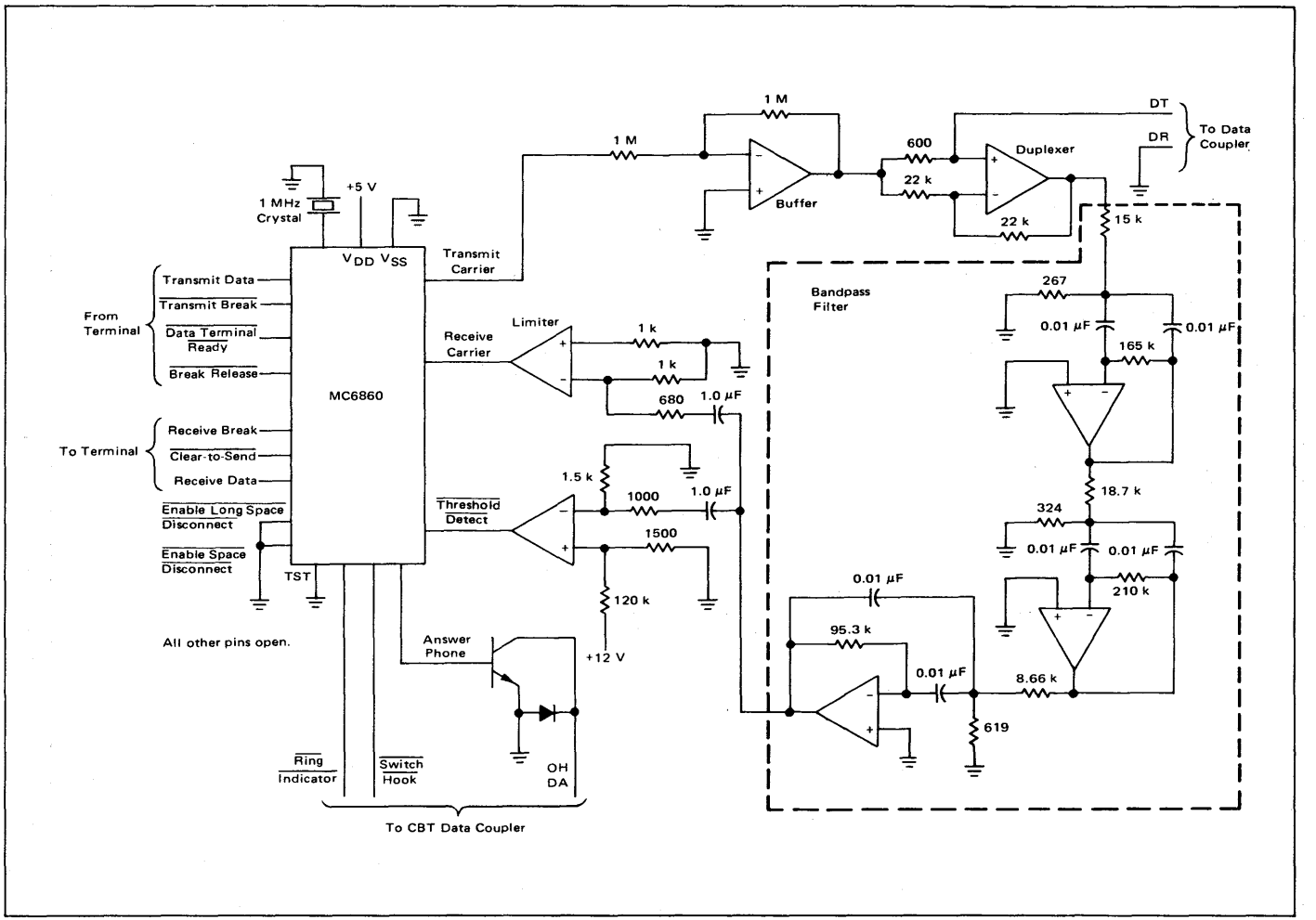


FIGURE 9 – Originate Modem

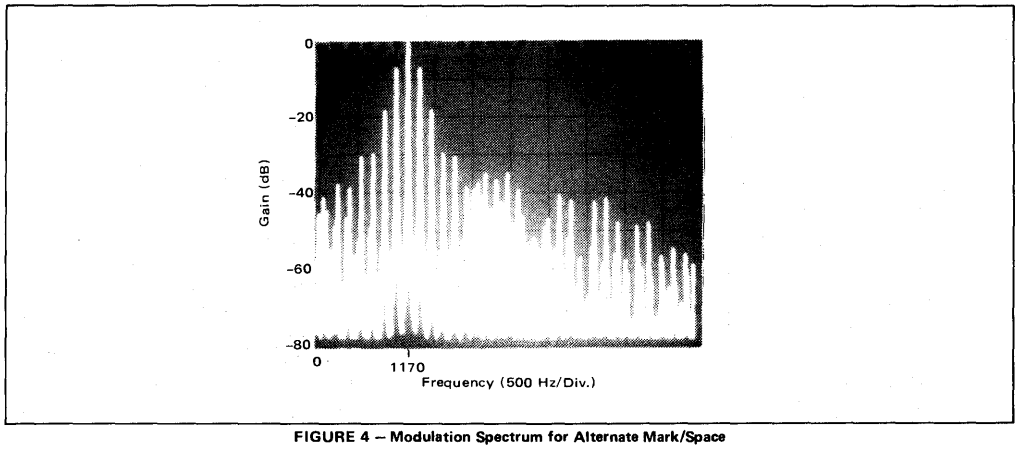


FIGURE 4 – Modulation Spectrum for Alternate Mark/Space

DUPLEXER

The duplexer is used to interface the modem with the transmission media which is a telephone system in most cases, through a data coupler. Since signal flow is bi-directional on the telephone line, the duplexer must allow the received signal to pass on to the bandpass filters, properly couple the transmitted signal onto the line, minimize the local transmit level at the bandpass filter input, and properly terminate the transmission line. The diagram of Figure 5 shows the various components of the duplexer with A1, A2, and A3 being the gain expressions of importance.

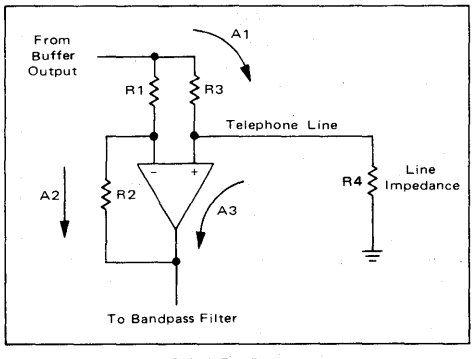


FIGURE 5 – Duplexer

The gain from the modulator output to the telephone line is

$$A1 = \frac{R4}{R3 + R4}$$

where R4 is the line impedance and is considered to be nominally 600 ohms resistive. Since the line must be properly terminated, R3 must equal R4. Therefore:

$$R3 = R4 = 600 \text{ ohms}$$

and $A1 = 0.5$

The gain from the buffer output to the bandpass filter input is

$$A2 = -\frac{R2}{R1} + \left(1 + \frac{R2}{R1}\right)\left(\frac{R4}{R3 + R4}\right)$$

It is desired that A2 = 0, thus reducing the intermodulation effects from the local modulator. With R3 = R4:

$$A2 = 0 = -\frac{R2}{R1} + \left(1 + \frac{R2}{R1}\right)\frac{1}{2}$$

$$2\frac{R2}{R1} = 1 + \frac{R2}{R1}$$

$$2R2 = R1 + R2$$

$$R2 = R1$$

With R1 = R2, the common mode characteristic of the operational amplifier is used to balance out the local modulator at the bandpass filter input, i.e., A2 = 0.

Since all impedances except the line impedance can be accurately controlled, the degree of nulling A2 becomes a function of the line impedance. The duplexer gain, A2, is plotted versus line impedance variation from 200 ohms to 1000 ohms in Figure 6. A well-defined notch exists when the line appears a purely resistive 600 ohms (the ideal case). In practice the line impedance can have reactive as well as resistive component variation, therefore the duplexer should be considered as providing approximately -10 dB even though in many connections greater attenuation will be achieved.

The gain from the telephone line to the bandpass filter input is given by

$$A3 = 1 + \frac{R2}{R1} = 2$$

when R1 = R2.

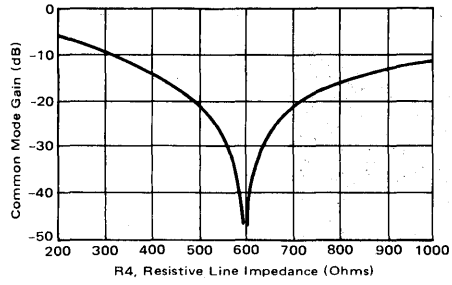


FIGURE 6 – Common Mode Gain versus Line Impedance

BANDPASS FILTER

The purpose of the bandpass filter is to amplify the received signal from the remote modem while rejecting all other signals that may be present in the local modem or on the telephone line. Interference which must be filtered out has several possible sources. Each of these must be considered and dealt with individually. Noise which is coupled in through the transmission media is either impulsive or band limited (gaussian) white noise. Both of these must be analyzed on a statistical basis. Discrete interfering signals may also be coupled in through the transmission media. However, the interfering signal of prime importance comes from the local modulator and will always exist in the half or full duplex modes.

Since the transmission media is lossy, the local transmit carrier level will exceed the level of the received signal. For this reason, the bandpass filter must have enough selectivity to reject the local carrier to an acceptable level. Modems that are designed for a wide dynamic range of input signal levels (-15 dBm to -55 dBm) require better than 70 dB rejection of interfering signals. Most of this rejection must come from the selectivity in the bandpass filter.

Reducing the effects of band limited white noise is accomplished by decreasing the bandwidth of the filter. Determining the minimum bandwidth comes by investigating the received signal characteristics. The transmitted data can be recovered from binary FSK by properly detecting the carrier and the first sidebands (first Bessel function)[1]. With a data rate of 300 bits per second and a data format of alternate Marks and Spaces, the first Bessel function occurs at ±150 Hz from the carrier. All other data formats have sidebands within the ±150 Hz limit. A minimum bandwidth of 300 Hz is then required in the bandpass filter.

The bandpass filter output is fed into an amplitude limiter, therefore the amount of passband ripple is not a critical parameter. An item of serious concern, however, is the phase linearity over the passband. All frequency components that pass through the filter must be equally delayed in time or jumbling and smearing of the data occurs. This is known as intersymbol or interbit interference. Performance of the communication system is degraded under these conditions with bias distortion and excessive phase jitter at the demodulator output resulting. Intersymbol interference can be reduced by linearizing the phase versus frequency transfer function. The slope of this transfer function is termed envelope delay and is determined by:

$$T_d = \frac{\Delta\phi}{\Delta f} \frac{1}{360 \text{ deg/cycle}}$$

where $\Delta\phi$ = change of phase in degrees
Δf = change of frequency in Hz

Minimizing the distortion of the envelope delay curve then minimizes the intersymbol interference. This is relatively easy over the center 2/3 of the passband. However, keeping constant delay near the band edges is quite difficult, if not impossible. For this reason, the optimum bandwidth is not determined according to the data rate but rather according to achievable linear phase characteristics. Bias distortion of one tenth of the bit period at 300 bps typically requires a -3 dB bandwidth of 450 Hz to 500 Hz.

Bandpass filters for evaluating the MC6860 were designed to have approximately a 450 Hz, -3 dB bandwidth with a Chebyschev response. The schematic for the answer filter is found in Figure 7 and is outlined for identification. The analytical response of this filter using standard valued components is tabulated in Table 1. The -3 dB bandwidth is calculated as 486 Hz and measured as 448 Hz. There is approximately 0.7 dB ripple over the center 300 Hz of the passband, with 0.4 ms envelope delay distortion, as shown in Figure 8. This filter attenuates the local transmit carrier of 2225 Hz by -35 dB relative to the passband gain.

A similar schematic for the originate bandpass filter is given in Figure 9. Its response approximates that of the originate filter as seen in Table 2 and Figure 10. Attenuation of the 1270 Hz local transmit carrier is -43 dB relative to the passband gain.

The envelope delay distortion for both of these filters can be reduced by widening the passband, thus flattening the envelope delay curve.

LIMITER-THRESHOLD DETECTOR

The demodulator in the MC6860 requires symmetrical limiting of the received signal in order to produce equal half-cycle periods. Each half-cycle period is measured in reference to an accurate time base to determine if the received frequency is a Mark or a Space. Non-symmetrical limiting produces errors in the demodulation process, thus degrading the system performance. Accurate limiting must be achievable over the expected input dynamic range. Such items as maximum input level and input offset voltage of the limiting device must be carefully considered.

Figure 11 shows the schematic for the limiter. The effect of the input offset is reduced by placing equal terminating resistors on both the inverting and non-inverting outputs. An input coupling capacitor is used to block any dc bias coming from the output of the last amplifier of the bandpass filter. The desired ac signal is now properly centered about the input bias level of the

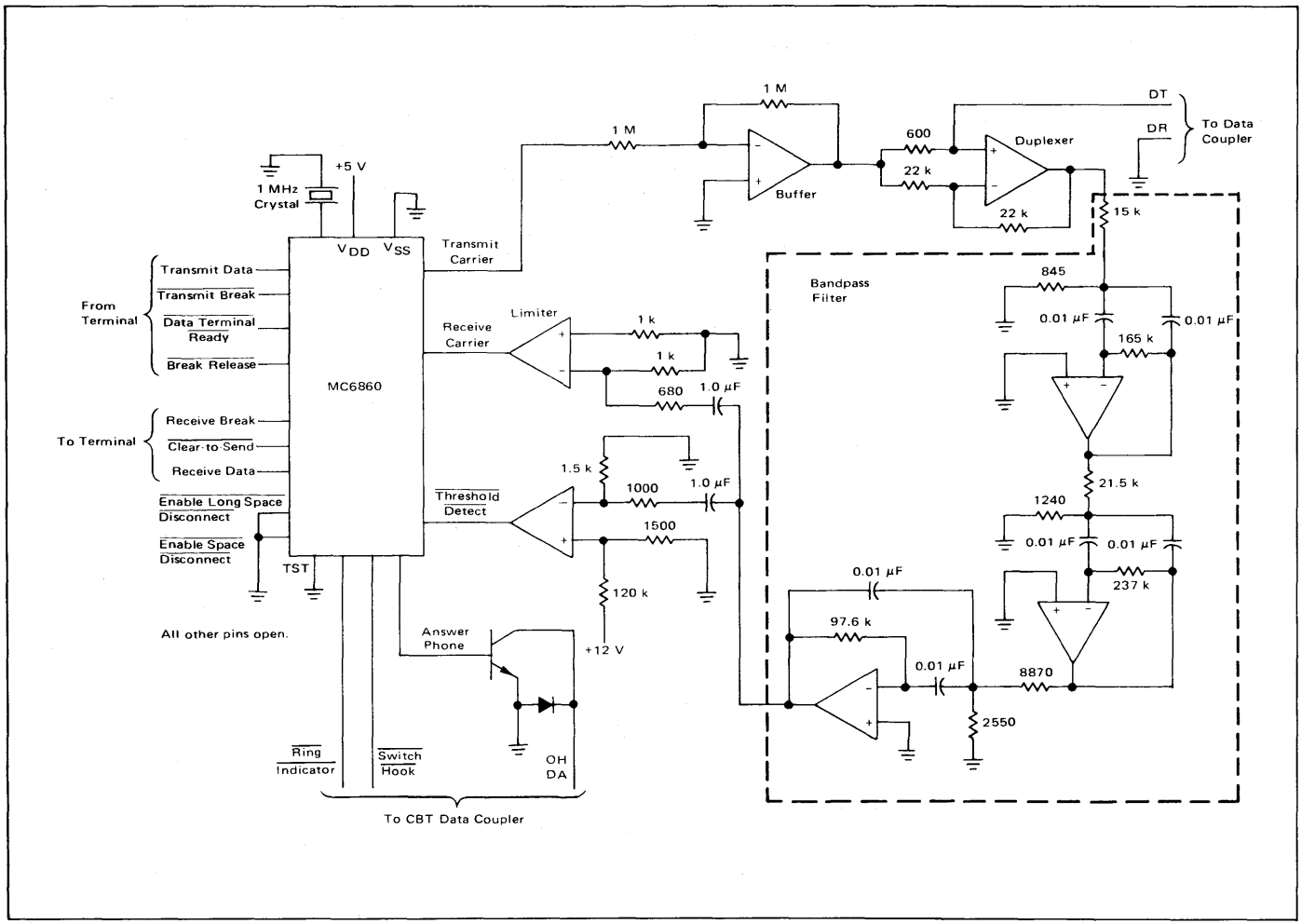


FIGURE 7 – Answer Modem

limiter and the maximum input dynamic range can now be achieved. A 40 dB dynamic range can be achieved with the limiter of Figure 11. Caution must be exercised in the amount of loading placed upon the bandpass filter output for distortion can result with large signal levels. An isolation resistor placed in series with the limiter input decreases the loading on the bandpass filter. Under maximum signal level conditions the limiter should be operating close to its upper input limit.

The output of the limiter is fed into the demodulator.

The threshold detector is used to determine if the input signal to the limiter is above the maximum detectable signal level of the modem. This is an amplitude measurement only, thus the period of the output is not critical. A comparator is used with one side biased to the peak amplitude of the desired minimum detectable signal level at the bandpass filter output. When the signal level exceeds the bias point, the comparator output goes low indicating an acceptable signal level.

TABLE 1 – Answer Filter Tabulated Response

Frequency	Node Voltage	dB Voltage	Phase Shift	Envelope Delay (ms)
0.3000E+03	0.202E-01	-33.883	80.83	
0.4000E+03	0.576E-01	-24.796	76.99	.11
0.5000E+03	0.145E+00	-16.770	72.24	.13
0.6000E+03	0.354E+00	-9.008	65.93	.18
0.7000E+03	0.906E+00	-.856	56.62	.26
0.8000E+03	0.267E+01	8.523	40.26	.45
0.9000E+03	0.101E+02	20.158	-1.03	1.15
0.9250E+03	0.141E+02	22.968	-21.78	2.31
0.9500E+03	0.176E+02	24.927	-47.11	2.81
0.9750E+03	0.194E+02	25.746	-72.41	2.81
0.1000E+04	0.196E+02	25.847	-93.83	2.38
0.1025E+04	0.194E+02	25.761	-111.32	1.94
0.1050E+04	0.193E+02	25.728	-126.37	1.67
0.1075E+04	0.195E+02	25.790	-140.24	1.54
0.1100E+04	0.198E+02	25.914	-153.70	1.50
0.1125E+04	0.201E+02	26.045	-167.08	1.49
0.1150E+04	0.203E+02	26.142	179.59	1.48
0.1175E+04	0.204E+02	26.190	166.42	1.46
0.1200E+04	0.204E+02	26.203	153.50	1.44
0.1225E+04	0.204E+02	26.210	140.79	1.41
0.1250E+04	0.205E+02	26.246	128.07	1.41
0.1275E+04	0.207E+02	26.321	114.90	1.46
0.1300E+04	0.209E+02	26.410	100.71	1.58
0.1325E+04	0.209E+02	26.417	84.93	1.75
0.1350E+04	0.203E+02	26.166	67.39	1.95
0.1375E+04	0.187E+02	25.459	48.87	2.06
0.1400E+04	0.163E+02	24.219	31.05	1.98
0.1425E+04	0.134E+02	22.568	15.50	1.73
0.1450E+04	0.108E+02	20.713	2.78	1.41
0.1500E+04	0.707E+01	16.984	-15.46	1.01
0.1600E+04	0.340E+01	10.635	-35.62	.56
0.1700E+04	0.193E+01	5.693	-46.41	.30
0.1800E+04	0.121E+01	1.703	-53.24	.19
0.1900E+04	0.829E+00	-1.634	-58.02	.13
0.2000E+04	0.596E+00	-4.501	-61.59	.10
0.2100E+04	0.446E+00	-7.016	-64.36	.08
0.2200E+04	0.345E+00	-9.255	-66.60	.06
0.2300E+04	0.273E+00	-11.275	-68.45	.05
0.2400E+04	0.221E+00	-13.115	-70.00	.04
0.2500E+04	0.182E+00	-14.807	-71.34	.04
0.2600E+04	0.152E+00	-16.372	-72.49	.03
0.2700E+04	0.128E+00	-17.830	-73.51	.03
0.2800E+04	0.109E+00	-19.194	-74.41	.03
0.2900E+04	0.947E-01	-20.476	-75.21	.02
0.3000E+04	0.824E-01	-21.687	-75.94	.02

TABLE 2 – Originate Filter Tabulated Response

Frequency	Node Voltage	dB Voltage	Phase Shift	Envelope Delay (ms)
0.3000E+03	0.467E-03	-66.607	87.38	
0.4000E+03	0.116E-02	-58.686	86.45	.03
0.5000E+03	0.242E-02	-52.315	85.47	.03
0.6000E+03	0.454E-02	-46.867	84.42	.03
0.7000E+03	0.794E-02	-42.001	83.28	.03
0.8000E+03	0.133E-01	-37.505	82.01	.04
0.9000E+03	0.218E-01	-33.233	80.59	.04
0.1000E+04	0.352E-01	-29.071	78.97	.05
0.1100E+04	0.567E-01	-24.925	77.07	.05
0.1200E+04	0.923E-01	-20.700	74.79	.06
0.1300E+04	0.153E+00	-16.298	71.98	.08
0.1400E+04	0.263E+00	-11.595	68.37	.10
0.1500E+04	0.477E+00	-6.425	63.50	.14
0.1600E+04	0.941E+00	-.531	56.43	.20
0.1700E+04	0.212E+01	6.534	44.84	.32
0.1800E+04	0.601E+01	15.574	20.75	.67
0.1825E+04	0.814E+01	18.210	9.86	1.21
0.1850E+04	0.110E+02	20.874	-4.80	1.63
0.1875E+04	0.146E+02	23.268	-24.14	2.15
0.1900E+04	0.176E+02	24.935	-47.21	2.56
0.1925E+04	0.192E+02	25.654	-70.39	2.57
0.1950E+04	0.194E+02	25.738	-90.48	2.23
0.1975E+04	0.191E+02	25.618	-107.18	1.86
0.2000E+04	0.189E+02	25.529	-121.58	1.60
0.2025E+04	0.189E+02	25.532	-134.82	1.47
0.2050E+04	0.191E+02	25.609	-147.63	1.42
0.2075E+04	0.193E+02	25.713	-160.44	1.42
0.2100E+04	0.195E+02	25.795	-173.34	1.43
0.2125E+04	0.196E+02	25.824	173.77	1.43
0.2150E+03	0.195E+02	25.798	161.04	1.41
0.2175E+04	0.194E+02	25.743	148.60	1.38
0.2200E+04	0.193E+02	25.696	136.37	1.36
0.2225E+04	0.193E+02	25.696	124.09	1.36
0.2250E+04	0.194E+02	25.756	111.29	1.42
0.2275E+04	0.196E+02	25.851	97.31	1.55
0.2300E+04	0.197E+02	25.876	81.50	1.76
0.2325E+04	0.191E+02	25.634	63.59	1.99
0.2350E+04	0.176E+02	24.888	44.47	2.13
0.2375E+04	0.150E+02	23.549	26.10	2.04
0.2400E+04	0.122E+02	21.768	10.27	1.76
0.2425E+04	0.976E+01	19.786	-2.47	1.42
0.2450E+04	0.775E+01	17.786	-12.48	1.11
0.2475E+04	0.621E+01	15.858	-20.37	.88
0.2500E+04	0.503E+01	14.039	-26.70	.70
0.2600E+04	0.247E+01	7.860	-42.90	.45
0.2700E+04	0.142E+01	3.031	-51.95	.25
0.2800E+04	0.901E+00	-.904	-57.83	.16
0.2900E+04	0.615E+00	-4.218	-62.00	.12
0.3000E+04	0.443E+00	-7.079	-65.14	.09

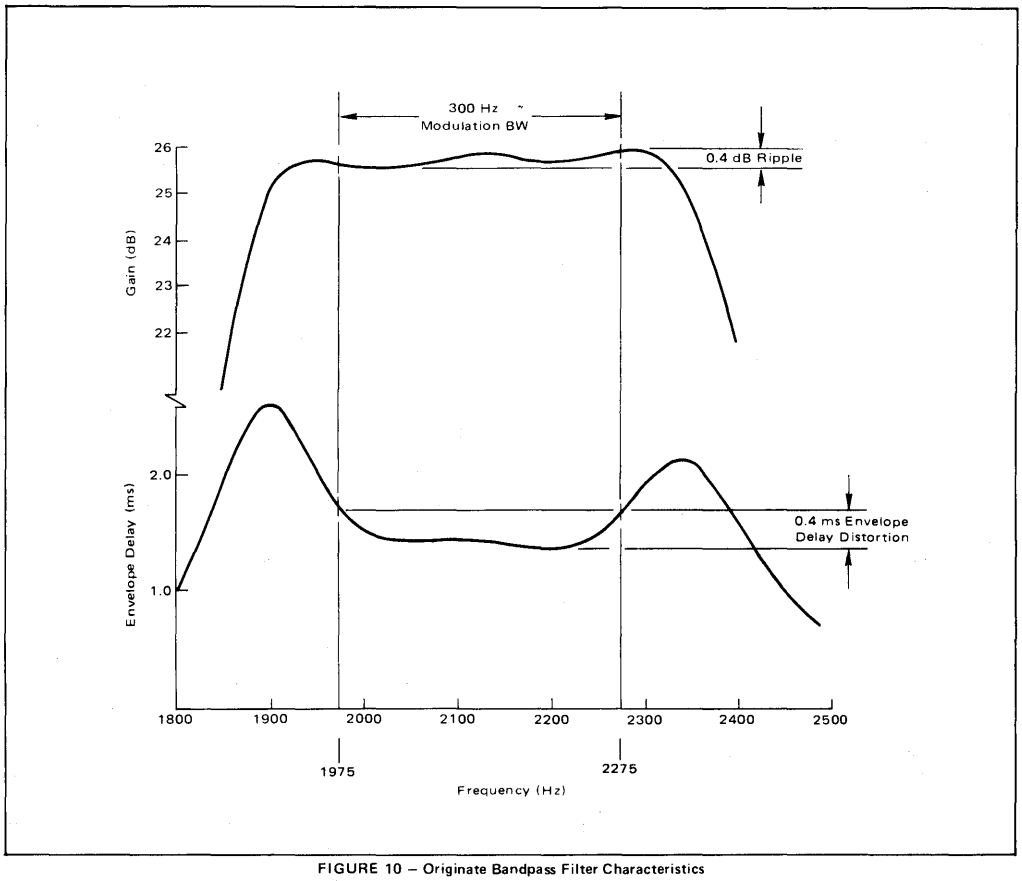


FIGURE 10 – Originate Bandpass Filter Characteristics

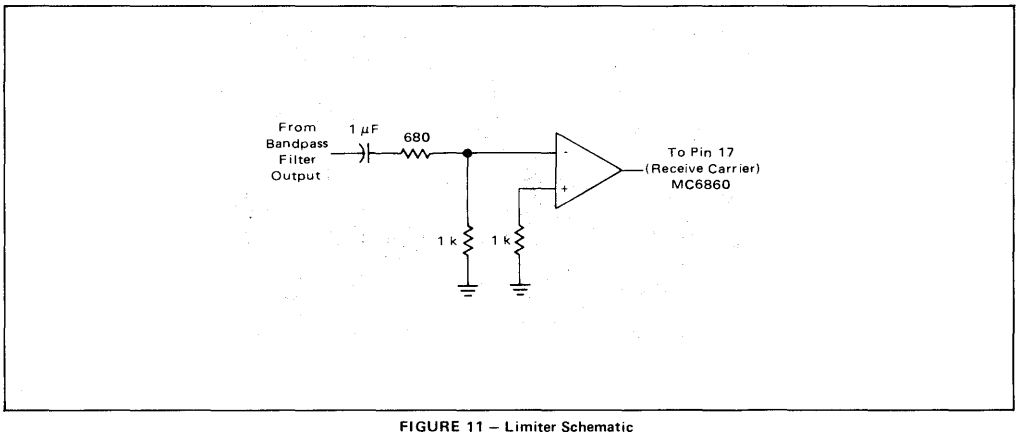


FIGURE 11 – Limiter Schematic

DEMODULATOR

The demodulator utilizes half-cycle detection for determining the presence of Mark or Space frequencies. Therefore, the Mark/Space information is quantized to half-cycle increments of the received carrier. Digitizing a linear signal produces a quantization error. This error appears in the form of phase jitter and bias distortion at the demodulator output of the MC6860.

The phase jitter of the demodulator output is shown in Figure 12. The upper trace is the alternate Mark/Space transmit data into the originate modulator. The lower trace shows the recovered data out of the demodulator of the answer modem. The inherent phase jitter of the demodulation process is approximated by

$$\%\phi_{j}\text{peak} \approx \frac{\text{Data Rate}}{4 \text{ Space Frequency}} \times 100$$

The receive Space frequency for the answer modem is 1070 Hz and the data rate is 300 bps, giving a peak phase jitter of 7%. This corresponds to 0.233 ms, as shown in Figure 12. The output Mark/Space transition will occur within 0.233 ms of the actual data transitions, neglecting bias distortion.

The receive Space frequency for the originate modem is 2025 Hz. The peak phase jitter is 3.7% (0.123 ms) at a data rate of 300 bps.

Bias distortion inherent in the demodulation process can be found according to:

$$\%\text{ Bias Distortion} \approx \frac{1}{2T}\left(\frac{1}{f_s} - \frac{1}{f_m}\right) 100$$

where T = Data bit period in seconds
f_s = Space frequency in Hz
f_m = Mark frequency in Hz

Thus the originate modem has a bias distortion of 0.67% and the answer modem has 2.2%. This is a marking bias (period of a Mark greater than period of a Space) for both modems.

Total distortion equals percent peak jitter plus percent bias distortion.

Careful inspection of Figure 12 reveals less than 0.2 ms marking bias. This is the accumulative bias distortion from the modulator input through the system to the demodulator output. The majority of this distortion results from the non-linear envelope delay through the bandpass filter in the answer modem. It is for this reason that special consideration must be given to delay distortion.

DATA COUPLERS

The two data couplers commonly used with low-speed modems are the CBS and CBT[2]. Each contains a data access arrangement (DAA) and the necessary telephone network control signaling functions. Figures 13 and 14 show the block diagrams of the CBS and CBT data couplers respectively. The supervisory control signals from the CBS comply with the RS-232 interface specifications, whereas the CBT control signals are contact closures and relay drive currents.

Table 3 identifies the various data coupler input/output signals.

SYSTEM PERFORMANCE

The MC6860 was evaluated in a typical system configuration. The tests utilized an originate only and an answer only design as outlined in Figure 15. The relative gains for both the answer and originate modems are given. A 600-ohm termination was provided to simulate the characteristic impedance of the transmission line, and to provide an input for the gaussian noise generator.

The test equipment was connected according to Figure 16. A word generator producing a 255-bit pseudo-random pattern at 300 bits per second was used as a transmit data input to the originate modem. The return channel was held at a constant Mark condition. The received data from the answer modem was compared for errors on a bit-by-bit basis with the transmitted data.

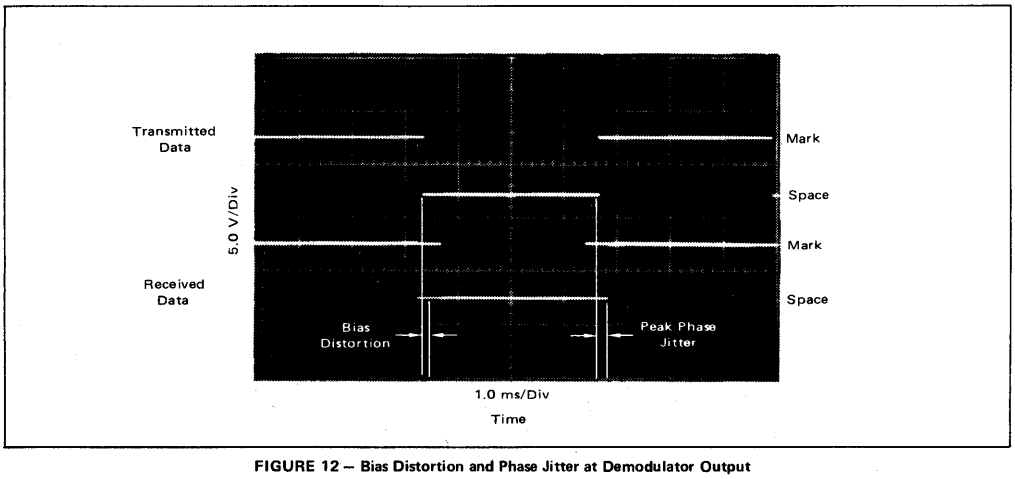


FIGURE 12 – Bias Distortion and Phase Jitter at Demodulator Output

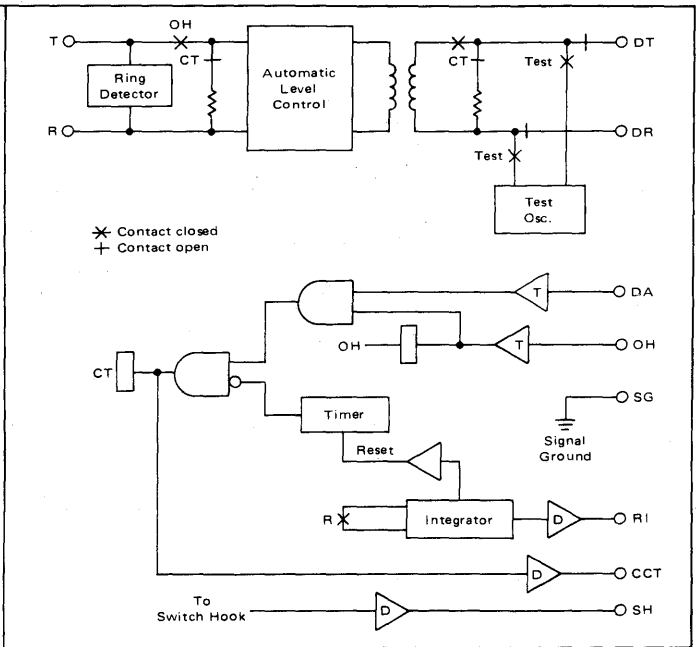


FIGURE 13 – Block Diagram of CBS Data Coupler

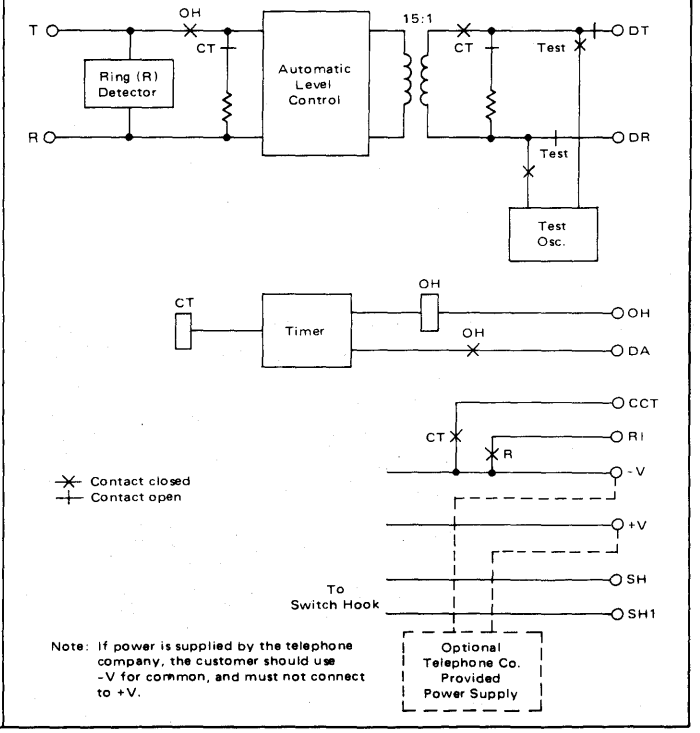


FIGURE 14 – Block Diagram of CBT Data Coupler

TABLE 3 – Data Coupler Interface Signals

Lead Designation		Direction	Function
Voltage (CBS)	Contact (CBT)		
DT DR	DT DR	Both	600-ohm transmission leads for data signals
OH	OH	To coupler	Control of OFF-HOOK relay
DA	DA	To coupler	To request data transmission path cut through
RI	RI	To customer	Ringing signal present
SG	*	Both	Signal ground in coupler (CBS)
CCT	CCT	To customer	Coupler transmission path cut through
SH	SH	To customer	Status of telephone set switch hook
*	SH1	To customer	Return for SH lead in coupler (CBT)
*	+V	To coupler	Positive dc power to coupler (CBT)
*	-V	Both	Return for dc power and common for all contact closures except the SH, SH1 pair in coupler (CBT)

*Not used in this unit.

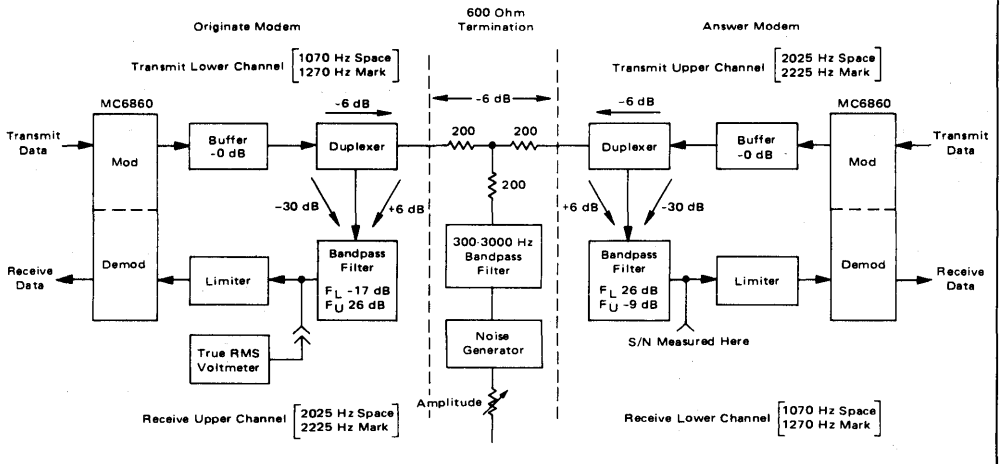


FIGURE 15 – Modem Evaluation

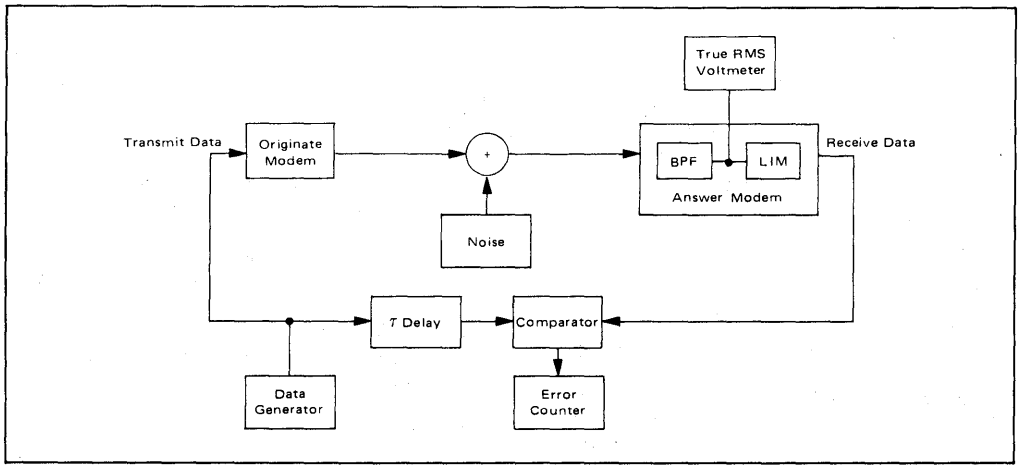


FIGURE 16 – Modem Test Equipment Configuration

Since the received data was delayed in time due to the time delay of the bandpass filter and the demodulator, the transmit data also had to be delayed an equal time before a meaningful bit-by-bit comparison could be made. This is accomplished by the τ delay between the data generator and the comparator. Sampling by the comparator was done at the center of the data bit. The number of bits used to determine the probability of error (P_e) was

$$\text{Number of bits} \geq \frac{100}{P_e}$$

A wideband gaussian noise generator was fed into a 300 Hz to 3000 Hz bandpass filter simulating band-limited white noise over a telephone channel. The signal-to-noise ratio for determining the probability of error was measured at the output of the bandpass filter in the modem just prior to the limiter. This ratio is a function of the noise bandwidth, and for proper evaluation of the system the rectangular noise bandwidth of the bandpass filters must be used. (The rectangular bandwidth for a sixth or higher order filter is approximately equal to the -3 dB bandwidth).

The signal and noise spectrum on the simulated transmission line is shown in Figure 17. Both the lower channel, F_L, and the upper channel, F_U, are present, along with the additive noise. When these signals are fed to the bandpass filter centered about F_L, all signals outside the passband are attenuated as shown.

The total amount of noise and F_U energy relative to the energy of F_L has now been reduced, thus improving the signal-to-noise ratio. The improvement of F_L to noise can be found according to the following formula:

$$\Delta(S/N) = 20 \log \sqrt{\frac{BW1}{BW2}} = 10 \log \frac{BW1}{BW2}$$

where BW1 = bandwidth of input noise
BW2 = filter bandwidth.
For the system in Figure 17
BW1 = (3000-300) Hz = 2700 Hz
BW2 = 448 Hz

$$\Delta(S/N) = 10 \log \frac{2700}{448} = 7.8 \text{ dB}$$

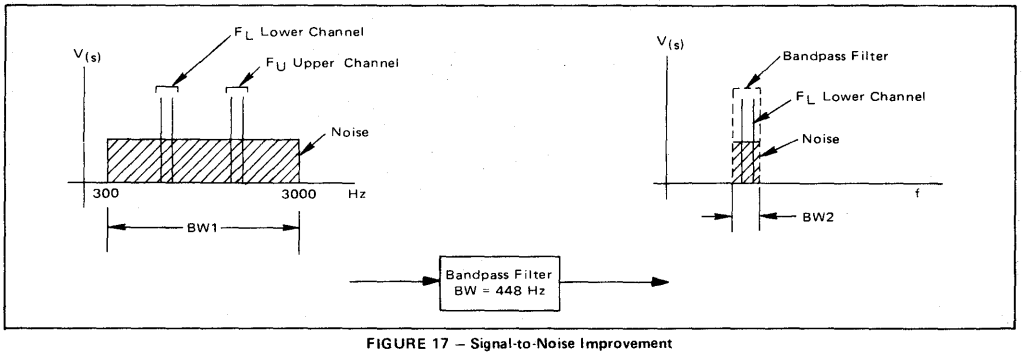


FIGURE 17 – Signal-to-Noise Improvement

Thus a signal-to-noise ratio of 12 dB at the filter output corresponds to 4.2 dB at the filter input.

$$(S/N)_{BW2} = (S/N)_{BW1} + \Delta(S/N)$$

The result of the performance tests is given in Figure 18. The theoretical probability of error $(P_e)^1$ curve for non-coherent FSK is determined according to:

$$P_e = \tfrac{1}{2}e^{-\frac{1}{2}\left(\frac{V_s}{V_n}\right)^2\left(\frac{BW_n}{BW_s}\right)}$$

where V_s = signal level
V_n = noise level (true rms)
BW_n = rectangular noise bandwidth
BW_s = signal bandwidth = 1/bit time = 1/T

The dashed curve in Figure 18 is based on the signal bandwidth and rectangular noise bandwidth being equal. Since the signal bandwidth is 300 Hz (300 bits per second) and the bandpass filter of the test circuit has a measured bandwidth of 448 Hz, the theoretical P_e curve now shifts to the left by the amount of

$$\Delta(S/N) = 10 \log \frac{448}{300} = 1.74 \text{ dB}$$

The measured P_e curve deviates from the theoretical by approximately 0.5 dB. In order to maintain a $P_e \leq 1 \times 10^{-5}$, a signal-to-noise ratio at the limiter input must be greater than 12.2 dB. This corresponds to a signal-to-noise ratio on the telephone line of 4.4 dB in a 2700 Hz bandwidth or a signal-to-noise ratio of 3.94 dB in a 4000 Hz bandwidth.

SUMMARY

This application note describes the basic functions of a low speed FSK modem using the MC6860. The criteria for design of each function are presented. A typical test configuration is illustrated and the results are documented. The interface to standard data couplers is also included.

ACKNOWLEDGEMENT

Appreciation is expressed to Don Kesner for his assistance in the design of the active filters.

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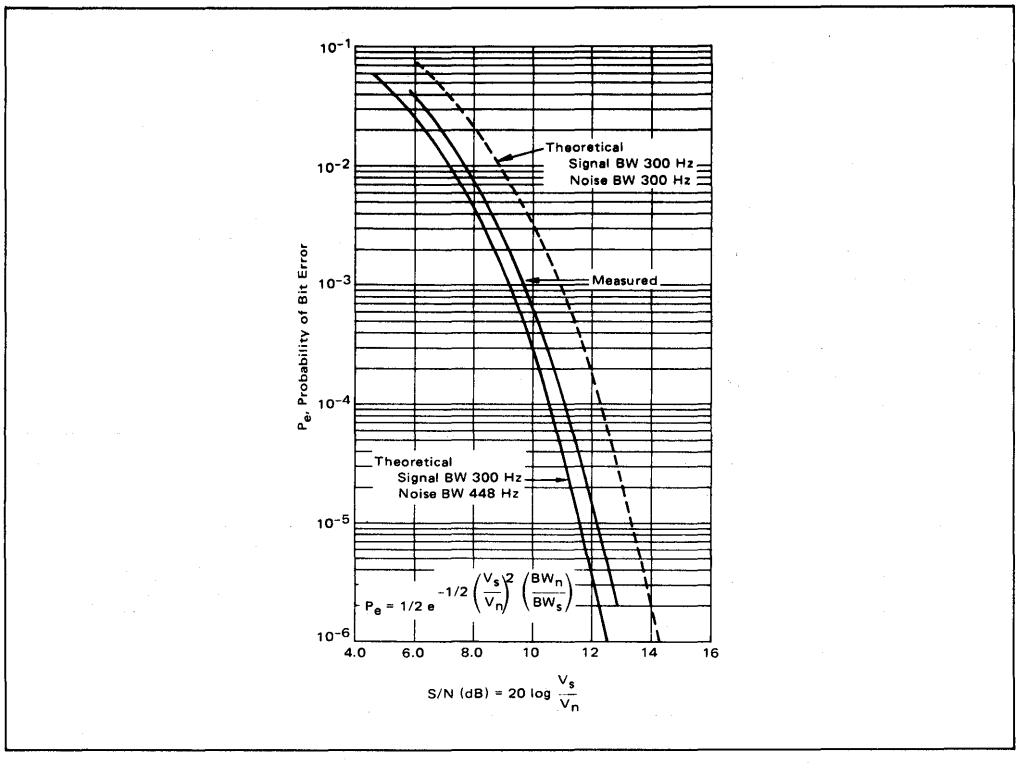


FIGURE 18 – System Performance with Gaussian Noise

LOW-SPEED MODEM SYSTEM DESIGN USING THE MC6860

Prepared by:
Jon M. DeLaune
Computer Applications

GENERAL

Low-speed modem designers will find that the MC6860 MOS LSI Modem with its built-in modulator, demodulator, and supervisory control will allow the design of a high performance, low cost 100 Series type modem. The designer, by selecting from different filter configurations and some surrounding support circuitry, may design either an originate only, answer only, or automatic answer/originate modem system.

It is the purpose of this note to cover in some detail these surrounding building blocks that comprise the total system. To familiarize the reader with the MC6860 chip operation, a general overview will be included with a more detailed description to be obtained from the MC6860 data sheet.

BASIC MC6860 CIRCUIT OPERATION

As illustrated in Figure 1, the MC6860 Modem contains a digital modulator, demodulator, and a supervisory control section to handle line disciplines for full duplex originate, auto-answer, and auto-disconnect operations.

Modulator

The modulator section converts serial digital data into analog frequencies for output to the telephone network. The analog output from the modem is a digital synthesized sinewave having one of four possible frequencies as listed in Figure 2. The modulation scheme used is frequency shift keying (FSK), where a logic "0" (space) is the lower frequency and a logic "1" (mark) is the upper or higher

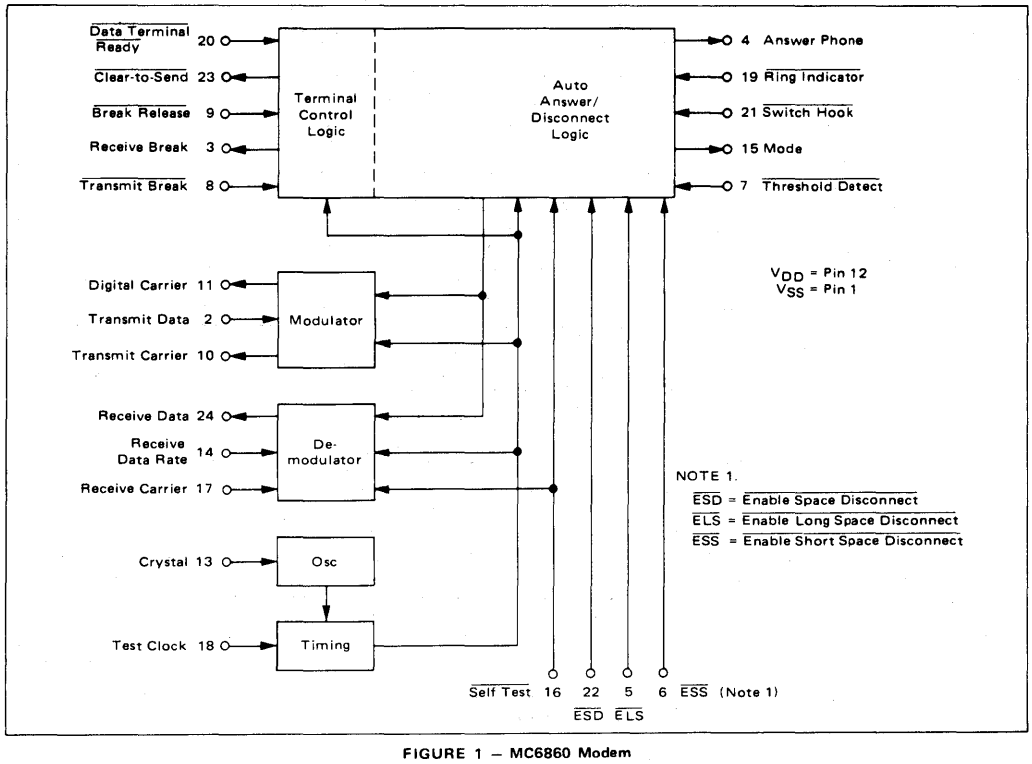


FIGURE 1 – MC6860 Modem

Output	Originate	Answer
Mark	1270 Hz	2225 Hz
Space	1070 Hz	2025 Hz

FIGURE 2 – Output Frequency Shift Keying Pairs

frequency of either the originate or answer frequency pairs. The analog signal output level from the modulator is typically 350 millivolts (rms) into a load of 100 k ohms; therefore, for the MC6860 to interface into a 600 ohm line system such as the telephone network with the necessary signal magnitude, an external transmit buffer will be required.

Demodulator

The demodulator section receives either the lower or upper (answer or originate modem) frequency tone pairs, and by a technique of digital half-cycle detection determines the presence of a mark or a space frequency and will output at the Receive Data pin either a digital logic "1" or "0" to the terminal or computer equipment. The incoming analog signal from the line should be bandlimited (filtered) and limited (amplified/clipped) prior to the demodulator carrier input to remove interfering signals and system noise. The limited input signal presented to the demodulator input should be at 50% duty cycle (±4%) over the full input signal dynamic range and be at a TTL compatible input level in order to maintain low bit-error-rate performance.

Supervisory Control

The supervisory control section of the MC6860 contains the necessary logic to provide initial inter-modem handshaking as well as operational protocol, such as automatic answer, originate only, initiate disconnect, and automatic disconnect. A graphical illustration of these control operations provided by the MC6860 is shown in Figures 3, 4, 5, and 6. Signals provided by the MC6860 for interfacing between a data terminal and either a CBS or a CBT telephone network data coupler are shown at the top right of Figure 1. Switch Hook (SH), Ring Indicator ($\overline{RI}$), and Answer Phone (An Ph) signals will interface directly with a CBT data coupler, or with a CBS data coupler when RS-232 interface circuits are used. Both of these data coupler interface methods will be illustrated in later system implementation examples.

Additional control signals that are provided for data terminal control are: Data Terminal Ready (DTR), Clear-to-Send (CTS), Receive Break (Rx Brk), Transmit Break (Tx Brk), and Break Release ($\overline{Brk\ R}$). The Mode output is a control function that is system oriented for the surrounding filter block. This output can be used to control switchable filters to provide a full automatic answer/originate modem system. A logic low level at the Mode output pin indicates the demodulator is in the answer mode of operation and will demodulate 1070 Hz and 1270 Hz incoming signals. When the Mode output is in a high state, the frequencies demodulated will be 2025 Hz and 2225 Hz. A design example using switchable filters will be illustrated in a later section.

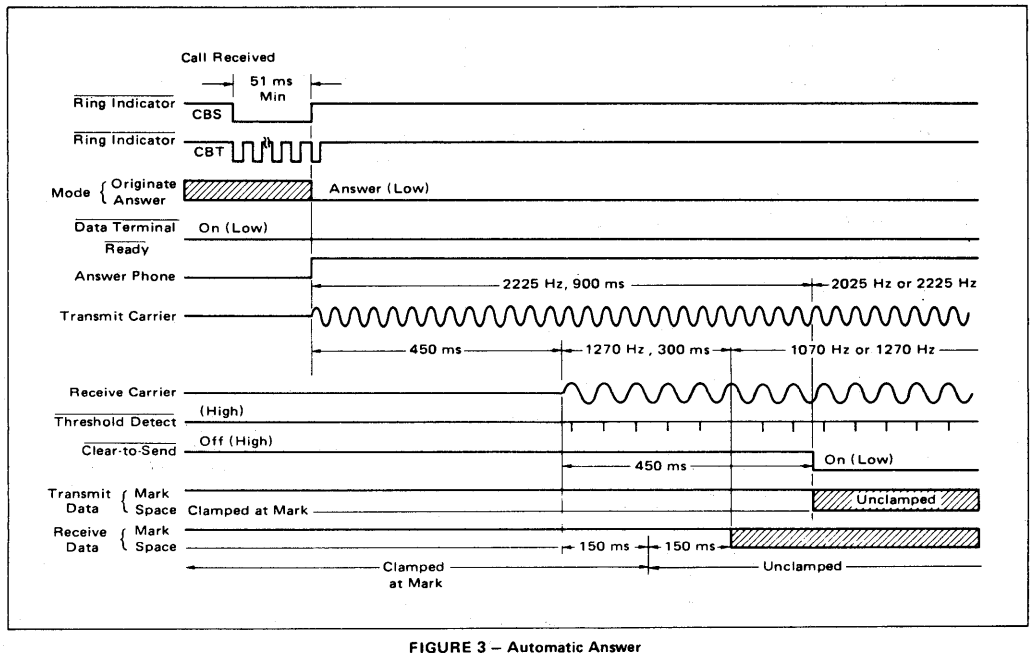


FIGURE 3 – Automatic Answer

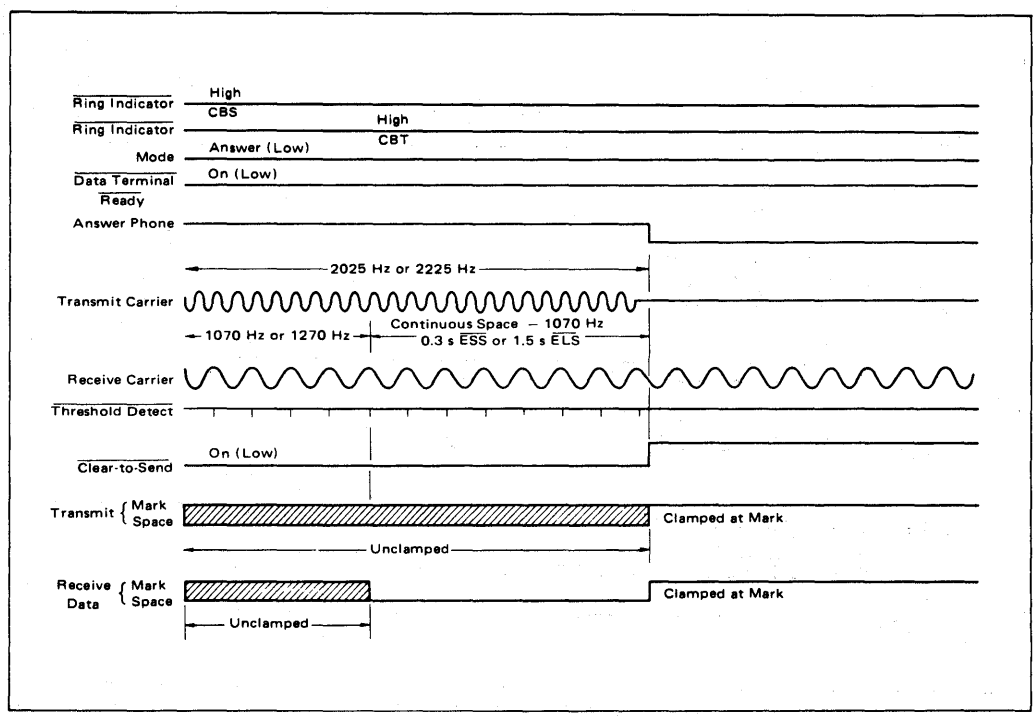


FIGURE 4 – Automatic Disconnect – Long or Short Space

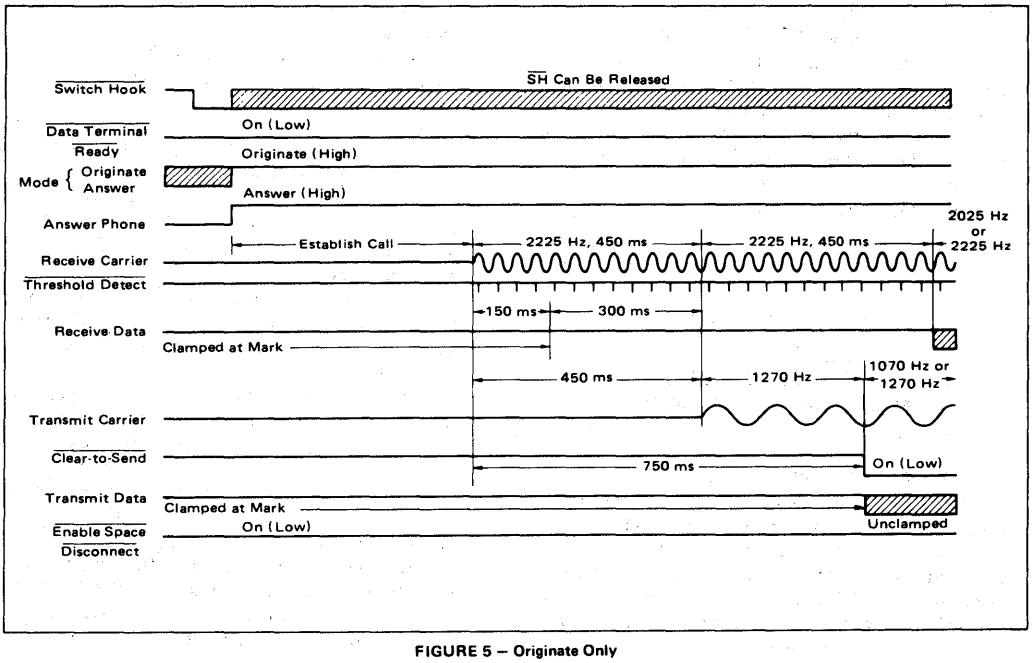


FIGURE 5 – Originate Only

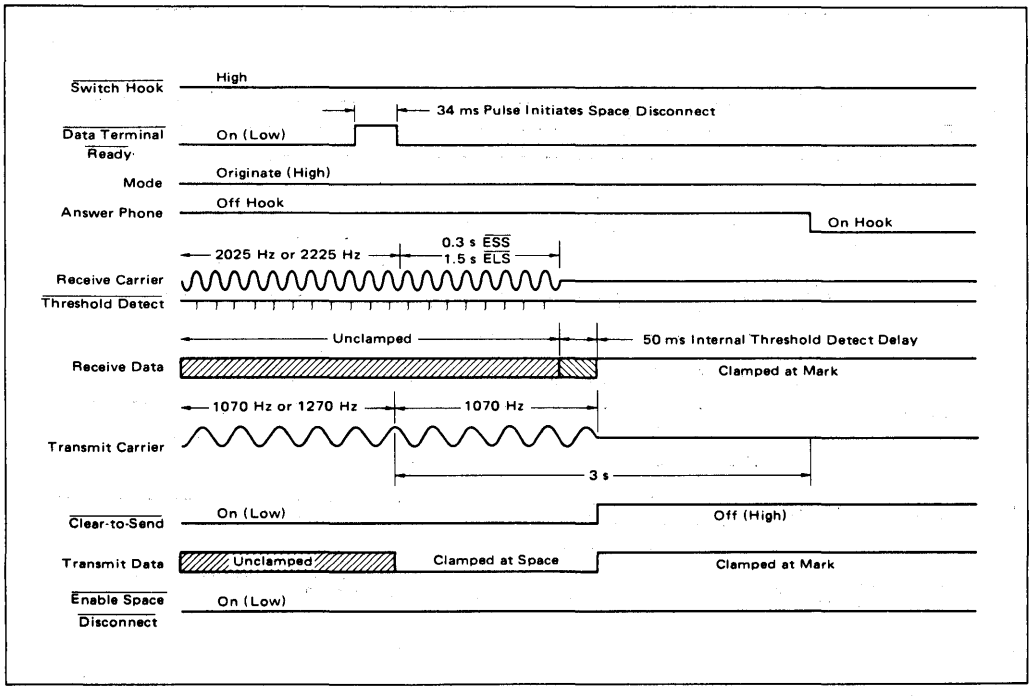


FIGURE 6 – Initiate Disconnect

A self test feature is included in the MC6860 for testing the modulator/demodulator sections. When a low logic level is applied to the Self Test ($\overline{ST}$) input pin, the demodulator is switched to detect the modulator transmitted frequency pair. Channel establishment obtained during initial handshaking is not lost, with only the Mode output changing state during initiation of self test as shown in Figure 7. This test feature allows the modulator, demodulator, and interval timer circuitry to be checked for proper operation during diagnostic system test.

$\overline{ST}$	$\overline{SH}$	$\overline{RI}$	Mode
H	L	H	H
H	H	L	L
L	L	H	L
L	H	L	H

FIGURE 7 – Mode Control Truth Table

MODEM FILTER DESIGN

Filter networks are among the most important surrounding element blocks in a modem system. As shown in Figure 8, a filter block is used in the receive carrier signal path and another filter block is used in the transmit carrier signal path. The transmit carrier filter may not be required in answer only modem designs but is required for originate mode operation.

The receive filter must provide sufficient adjacent channel rejection to provide good bit-error performance. During answer only operation, the filter must pass the receive frequencies of 1070 and 1270 Hz, but reject the adjacent channel local transmit frequencies of 2025 and 2225 Hz.

Typically, the receive carrier bandpass filter should provide greater than 35 dB attenuation to the adjacent channel. During full duplex originate operation, the local transmit signal produces second harmonic energy within the receive filter bandpass (2 x 1070 Hz = 2140 Hz). To reduce this frequency component in the receive filter passband, a transmit carrier filter must be included. This transmit filter may be either a low pass, a high pass, or a bandpass filter dependent upon the designed mode of operation of the modem: originate only, answer only, or auto answer/originate.

The filter design example presented is a bandpass configuration which could be used in either the transmit or receive signal paths with only component value changes. The transmit filter must have a pass frequency of 2025-2225 Hz when the modem is used as an answer only modem (receiving frequencies of 1070-1270 Hz). The opposite configuration is true when the modem is in the originate only mode of operation (transmit frequencies of 1070-1270 Hz and receive frequencies of 2025-2225 Hz).

A design example is presented, with design tables and equations to solve for the modem system bandpass filter

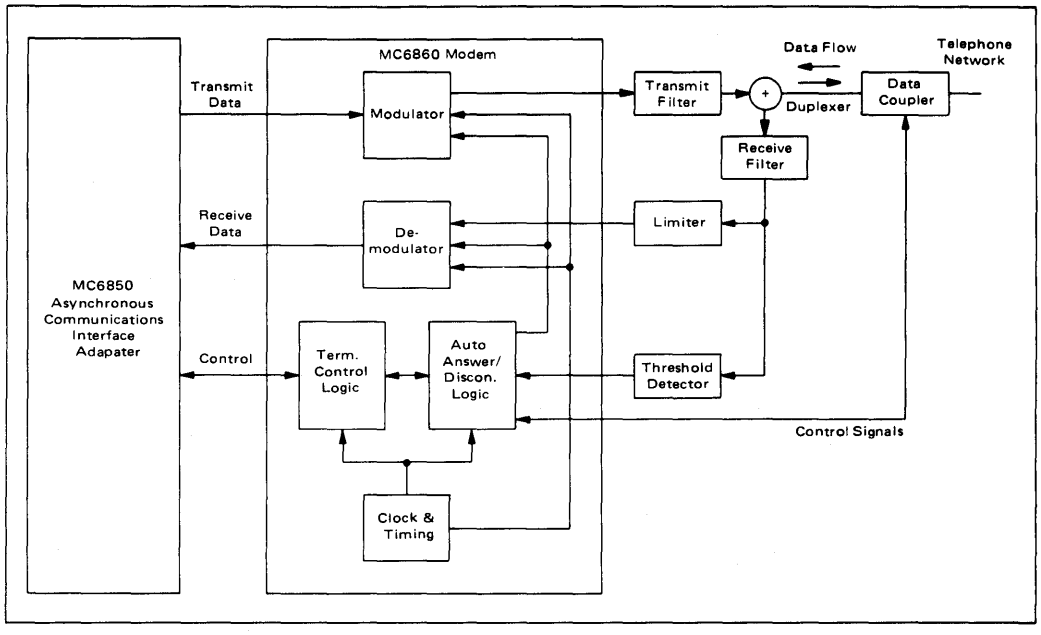


FIGURE 8 – Typical MC6860 Modem System

component values. A 6-pole answer filter is developed in detail in this application note, whereas a 6-pole originate filter has values tabulated only. Also tabulated are component values for 8-pole, 50-dB receive filters and 4-pole, 25-dB transmit filters.

A filter design may take one of many forms. The included design examples use a 0.5 dB ripple Chebyshev approximation. The filter element configuration used is a multiple feedback bandpass as shown in Figure 9. As indicated in Figure 10, the Chebyshev filter will provide a high degree of attenuation in the stop band, but with less phase linearity than a Butterworth or Bessel filter. Linear phase or group delay in the passband is an important design consideration for modem filter design. Error performance and demodulator phase/bias distortion of the modem system is affected by unequal delay of data frequencies within the filter passband. Therefore, it is important to provide filters that not only provide sharp stopband attenuation, but also provide some degree of phase linearity in the passband. By designing the Chebyshev filter to have a wider bandwidth than required for FSK (frequency shift keyed) data recovery, the designer can maximize phase linearity within the required passband.

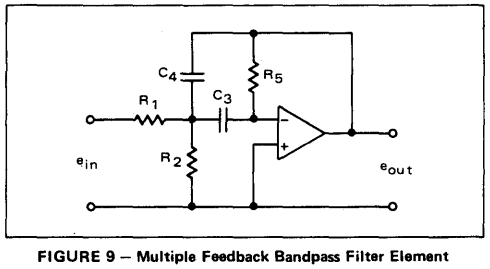


FIGURE 9 – Multiple Feedback Bandpass Filter Element

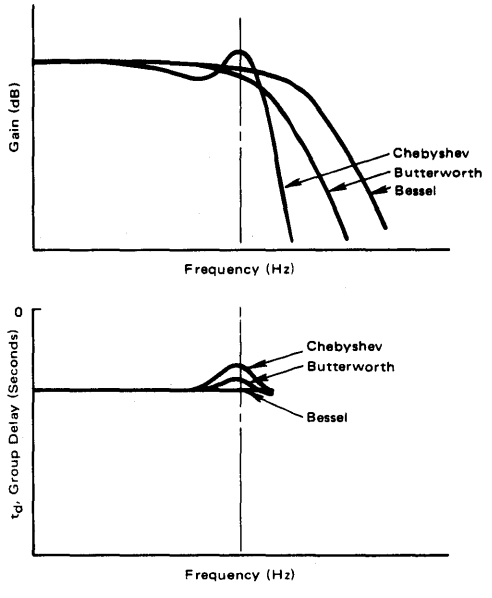


FIGURE 10 – Filter Approximation Characteristics

Determining the minimum filter bandwidth comes by investigating the received signal characteristics. Data communication theory states that data transmitted by FSK can be recovered by detecting the data carrier and the first sidebands. At a data rate of 300 bits per second and a data format of alternate mark and space, the first sidebands occur ±150 Hz from the carrier which is located halfway between the mark and space frequencies. Therefore, the minimum bandwidth for the receive bandpass filter is 300 Hz. Typically, frequencies within this 300 Hz bandwidth should undergo no greater than 0.8 millisecond change in group delay. Group delay is defined by:

$$t_d = \frac{\triangle\phi}{\triangle F} \frac{1}{360^o/\text{cycle}}$$

where $\triangle\phi$ = change in phase in degrees
$\triangle F$ = change in frequency in Hz

3

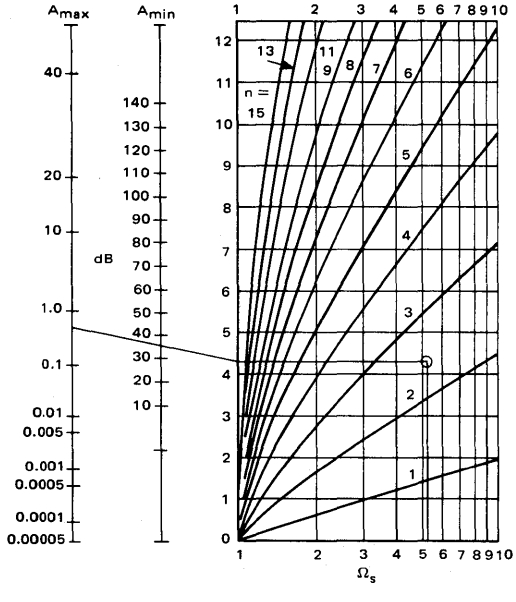
To maintain less than 0.8 millisecond group delay at a data rate of 300 bits per second requires an overall filter bandpass of 400 Hz. This results in the low frequency pair (answer) filter passband being between 970 Hz and 1370 Hz (6-pole, 0.5 dB ripple Chebyshev).

Filter Design Steps

The modem bandpass filter examples will be designed using the following procedural steps:

(1) Determine the required prototype low pass filter shape factor from the passband width and stopband attenuation.
(2) Enter Table 1 with the shape factor, passband ripple (A_{max}), and stopband attenuation (A_{min}), to determine the order of the prototype lowpass filter.
(3) From Table 2, determine the location of the prototype low pass filter poles opposite the determined filter order.
(4) From the low pass filter poles, determine their natural frequency (ω) and damping factor (ξ).
(5) Transform the low pass filter section parameters to cascaded second order bandpass filter design section Q and center frequency values.
(6) Determine the active element operational amplifier gain by solving for center frequency loss and system filter passband gain (A_{VO}).
(7) Use each section Q, frequency, and gain to solve for the bandpass filter passive component values.

TABLE 1 – Complexity Nomograph for Chebyshev Filters (Zverev)



Step (1) – Filter Shape Factor

Figure 11 shows a design example for a typical 6-pole answer modem receive filter design. From this data, it is possible to calculate the filter shape factor (Ω_s) for the prototype filter.

$$\Omega_s = \frac{F_4 - F_3}{F_2 - F_1} = \frac{2225 - 115}{1370 - 970} \quad (1)$$

$$\Omega_s = \frac{2110}{400} = 5.28$$

TABLE 2 – Pole Locations and Quadratic Factors ($s^2 + a_1 s + a_0$) for Chebyshev 0.5 dB Ripple Filter

Order	0.5 dB Ripple Poles	a_0	a_1
2	-0.71281 ± j 1.00404	1.51620	1.42562
3	-0.31323 ± j 1.02193	1.14245	0.62646
	-0.62646		
4	-0.17535 ± j 1.01625	1.06352	0.35071
	-0.42334 ± j 0.42095	0.35641	0.84668
5	-0.11196 ± j 1.01156	1.03578	0.22393
	-0.29312 ± j 0.62518	0.47677	0.58625
	-0.36232		
6	-0.07765 ± j 1.00846	1.02302	0.15530
	-0.21214 ± j 0.73824	0.59001	0.42429
	-0.28979 ± j 0.27022	0.15700	0.57959
7	-0.05700 ± j 1.00641	1.01611	0.11401
	-0.15972 ± j 0.80708	0.67688	0.31944
	-0.23080 ± j 0.44789	0.25388	0.46160
	-0.25617		
8	-0.04362 ± j 1.00500	1.01193	0.08724
	-0.12422 ± j 0.85200	0.74133	0.24844
	-0.18591 ± j 0.56929	0.35865	0.37182
	-0.21929 ± j 0.19991	0.08805	0.43859
9	-0.03445 ± j 1.00400	1.00921	0.06891
	-0.09920 ± j 0.88291	0.78936	0.19841
	-0.15199 ± j 0.65532	0.45254	0.30397
	-0.18644 ± j 0.34869	0.15634	0.37288
	-0.19841		
10	-0.02790 ± j 1.00327	1.00734	0.05580
	-0.08097 ± j 0.90507	0.82570	0.16193
	-0.12611 ± j 0.71826	0.53181	0.25222
	-0.15891 ± j 0.46115	0.23791	0.31781
	-0.17615 ± j 0.15890	0.05628	0.35230

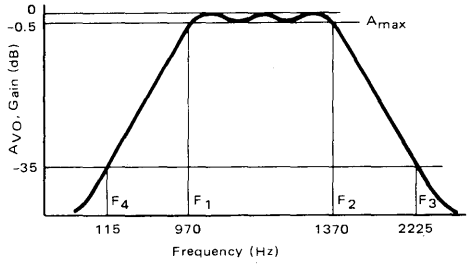


FIGURE 11 – Answer Filter Design Goals

where:

F_1 = lower passband frequency in Hz
F_2 = upper passband frequency in Hz
F_3 = lower stopband frequency in Hz
F_4 = upper stopband frequency in Hz

NOTE:

F_1 and F_2 are ripple bandwidth frequencies, i.e., gain down 0.5 dB.

Steps (2) and (3) – Filter Order and Pole Location

The second step of the filter design process was to determine the complexity of the filter. To determine this complexity, the following information is required:

1. The passband ripple, A_{max}.
2. The minimum stopband attenuation, A_{min}.
3. The ratio of the ripple bandwidth and the first frequency of minimum attenuation, shape factor Ω_S.

With A_{max} = 0.5 dB, A_{min} = -35 dB, and Ω_S = 5.28 enter the nomograph in Table 1 to determine the filter complexity or order.

The nomograph is used by locating the passband ripple A_{max} and the minimum stopband attenuation A_{min} and drawing a line from A_{max} through A_{min} to the left-hand side of the graph. From this point, a horizontal line is drawn to an intersection of the vertical line value of Ω_S. The minimum complexity or order, n, will be the n curve that passes through or above this intersection. In our example, the order n equals 3. This implies that the low pass prototype filter will have 3 poles and, consequently, the final bandpass filter will have 3 pole-pairs.

Table 2 gives the pole locations and quadratic factors for a third order 0.5 dB passband ripple Chebyshev low pass filter.

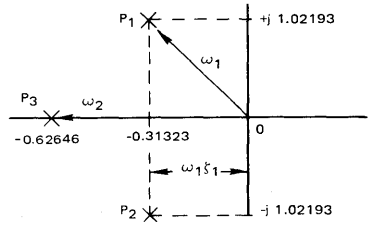
The values obtained from Table 2 are:

$-0.31323 \pm j1.02193$	Complex conjugate pole
$-0.62646 + j0$	Real pole
$a_0 = 1.14245$	Characteristic of non s term
$a_1 = 0.62646$	Characteristic of s term

where the s term equation = $(s^2 + a_1 s + a_0)$

Step (4) – Lowpass Prototype Filter Natural Frequencies and Damping Factors

Using the following relationships, solve for the natural frequencies (ω) and damping factors (ξ):



$$\omega_1^2 = (1.02193)^2 + (-0.31323)^2 \quad (2)$$
$$\omega_1 = 1.069$$

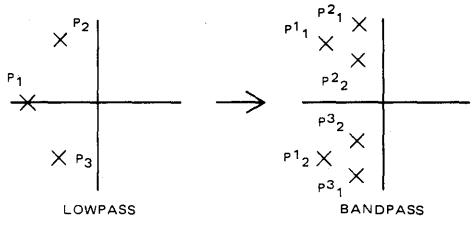
also, $\omega_1 \xi_1 = 0.31323$ (3)

$$\xi_1 = \frac{0.31323}{1.069}$$
$$\xi_1 = 0.293$$
$$\omega_2^2 = (0)^2 + (-0.62646)^2$$
$$\omega_2 = 0.62646$$

also, $\omega_2 \xi_2 = 0.62646$
$\xi_2 = 1$

Step (5) – Filter Section Q and Center Frequency

The complex conjugate pole of the low pass prototype is transformed into a pair of complex conjugate bandpass poles, whereas the real pole of the low pass prototype is transformed into a complex conjugate pair of bandpass poles.



The bandpass filter will take on a form of three 2-pole bandpass filter sections in cascade. When bandpass sections are cascaded, each section center frequency and Q must be determined from the low pass damping factors (ξ) and natural frequencies (ω).

Given:
$\omega_1 = 1.069, \xi_1 = 0.293$
$F_1 = 970$ Hz, $F_2 = 1370$ Hz
Then:

$$F_0 = \sqrt{F_1 F_2} = 1152.78 \text{ Hz (geometric center)} \quad (4)$$

$$Q_0 = \frac{F_0}{F_2 - F_1} = \frac{1152.78 \text{ Hz}}{400} \text{ (Filter Q)} \quad (5)$$

$$Q_0 = 2.8819$$

Section Q:

$$Q_1 = \left[\frac{\left[\left(\frac{\omega_1}{Q_0}\right)^2 + 2\right] + \sqrt{\left\{\left[\left(\frac{\omega_1}{Q_0}\right)^2 + 2\right] + 2\right\}^2 - 4\left(\frac{2\xi_1\omega_1}{Q_0}\right)^2 + 2}}{2\left(\frac{2\xi_1\omega_1}{Q_0}\right)^2}\right]^{1/2} \quad (6)$$

Yielding:

$Q_1 = 9.345$

Section 2 is a reflected image about F_0 of section 1 for a 3 section cascaded filter (odd order). Recall that a third order low pass when transformed to a bandpass results in two pairs of complex poles (sections 1 and 2) from the low pass complex pole and one pair of complex poles (section 3) from the low pass real pole.

$$Q_1 = Q_2 = 9.345$$

For section 3:

$$Q_3 = \frac{Q_0}{\xi_2\omega_2} = \frac{2.882}{(1)\ (0.627)} = 4.596 \quad (7)$$

Center Frequencies:

$$F_1 = MF_0 \quad (8)$$

where:

$$M = \frac{\xi_1\omega_1 Q_1}{Q_0} + \sqrt{\left(\frac{\xi_1\omega_1 Q_1}{Q_0}\right)^2 - 1} \quad (9)$$

$$M = \frac{(0.293)\ (1.069)\ (9.345)}{2.882} + \sqrt{\left[\frac{(0.293)\ (1.069)\ (9.345)}{2.882}\right]^2 - 1}$$

$M = 1.1932$

$F_1 = (1.1932)\ (1152.78) = 1375.52$ Hz

The image F_2 becomes:

$$F_2 = \frac{1}{M} F_0 = \frac{1152.78}{1.1932} = 966.1 \text{ Hz} \quad (10)$$

For section 3 the center frequency is:

$$F_3 = F_0 = 1152.78 \text{ Hz} \quad (11)$$

Step (6) – Center Frequency Loss and Filter Passband Gain

The gain produced by the active elements in the bandpass filter should overcome loss due to the stagger tuned filter sections. Each section of a cascade bandpass filter, except the section centered about ω_0, has a loss as represented by Equation 12. The overall filter center angular frequency ω_0 (Equation 13), section Q, and section center angular frequency ω_n (Equation 14) are required to determine each section's center frequency loss. Once the individual losses are determined, they are summed to arrive at the total cascaded filter loss $AVO(j\omega_0)$.

This value is used in determining filter section gain such that the designed bandpass filter meets design gain goals. The receive filter block must amplify the minimum input line signal to a minimum required limiter input signal.

$$AVO_n(j\omega_0)\ \text{dB loss} = 20 \log \frac{\frac{\omega_n\omega_0}{Q_n}}{\sqrt{(\omega_n^2 - \omega_0^2)^2 + \left(\frac{\omega_n\omega_0}{Q_n}\right)^2}} \quad (12)$$

$$\omega_0 = 2\pi\sqrt{F_1 F_2} \quad (13)$$

$$\omega_n = 2\pi F_n \quad (14)$$

The following will illustrate the use of Equation 12 to solve for the center frequency loss of the modem answer filter example.

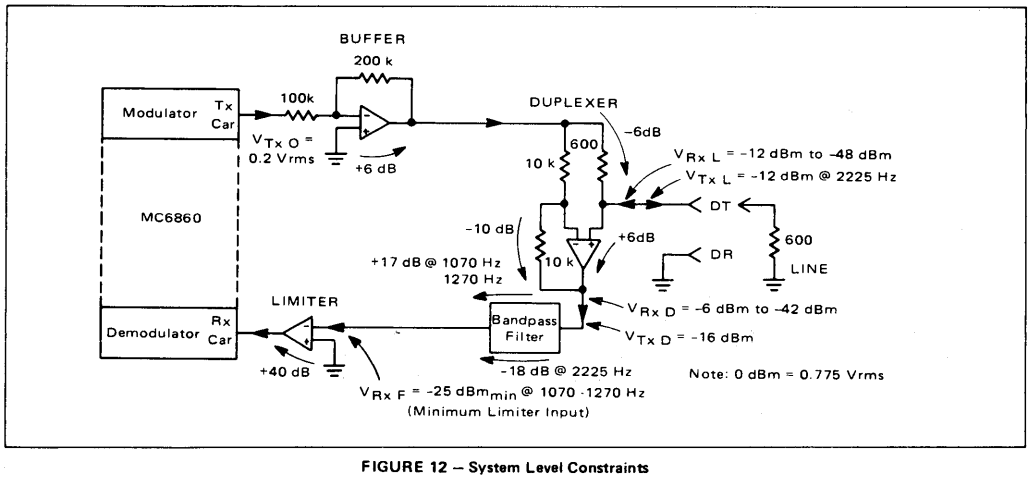


FIGURE 12 – System Level Constraints

Section 1

$$\omega_0 = 2\pi\sqrt{(970)(1370)} = 7.2431 \times 10^3 \text{ rad/s} \quad (15)$$

$$\omega_1 = 2\pi(1375.52) = 8.6426 \times 10^3 \text{ rad/s} \quad (16)$$

$$Q_1 = 9.345$$

$$|A_{VO1}(j\omega_0)|_{dB\ loss} = 20 \log \left[\frac{\frac{(8.6426 \times 10^3)(7.243 \times 10^3)}{9.345}}{\sqrt{\left[(8.642 \times 10^3)^2 - (7.243 \times 10^3)^2\right]^2 + \left[\frac{(8.642 \times 10^3)(7.243 \times 10^3)}{9.345}\right]^2}} \right] \quad (17)$$

$$|A_{VO1}(j\omega_0)|_{dB\ loss} = 20 \log (0.2886)$$

$$|A_{VO1}(j\omega_0)|_{dB\ loss} = -10.794 \text{ dB}$$

Section 2

$$\omega_0 = 7.243 \times 10^3 \text{ rad/s}$$

$$\omega_2 = 2\pi(966.1) = 6.07 \times 10^3 \text{ rad/s}$$

$$Q_2 = 9.345$$

$$|A_{VO2}(j\omega_0)|_{dB\ loss} = 20 \log (0.2886)$$

$$|A_{VO2}(j\omega_0)|_{dB\ loss} = -10.794 \text{ dB}$$

Section 3

$$\omega_0 = 7.243 \times 10^3 \text{ rad/s}$$

$$\omega_3 = 7.243 \times 10^3 \text{ rad/s}$$

$$Q_3 = 4.596$$

$$|A_{VO3}(j\omega_0)|_{dB\ loss} = 20 \log (1)$$

$$|A_{VO3}(j\omega_0)|_{dB\ loss} = 0 \text{ dB, due to } \omega_n = \omega_0$$

The total filter center frequency loss is equal to the sum of all sectional losses.

$$|A_{VO}(j\omega_0)|_{dB\ loss} = (-10.79 \text{ dB}) + (-10.79 \text{ dB}) + (0 \text{ dB}) \quad (18)$$

$$|A_{VO}(j\omega_0)|_{dB\ loss} = -21.58 \text{ dB}$$

Figure 12 illustrates the design goals that are used to determine the receive filter passband gain for the answer only modem system. The answer filter provides 35 dB of attenuation to 2225 Hz relative to the filter passband. This results in -34 dBm of unwanted signal level being present at the limiter input. To maintain a probability of error (P_e) $\leq 1 \times 10^{-5}$, a signal-to-noise ratio at the limiter input must be greater than +12.12 dB. The theoretical probability of error (P_e) curve for non-coherent FSK is determined by:

$$P_e = 1/2\, e^{-\left[\frac{\left(\frac{V_s}{V_n}\right)^2 \left(\frac{BW_n}{BW_s}\right)}{2}\right]} \quad (19)$$

where V_s = signal level
V_n = noise level
BW_n = noise bandwidth (400 Hz)
BW_s = signal bandwidth (300 Hz)

In calculating the voltage gain required by the receive active filter block, the following constraints should be considered:

(a) The signal to noise performance required by the modem system.
(b) The receive limiter minimum input level while providing less than ±4% deviation from a 50% output duty cycle.
(c) The worst case receive input line levels.

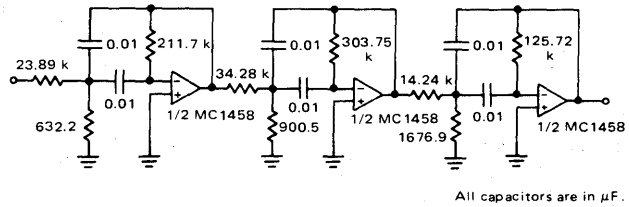


FIGURE 13a – Answer Filter Component Values

(d) At the maximum input line levels, the designed filter gain should not saturate any active stage of the filter.

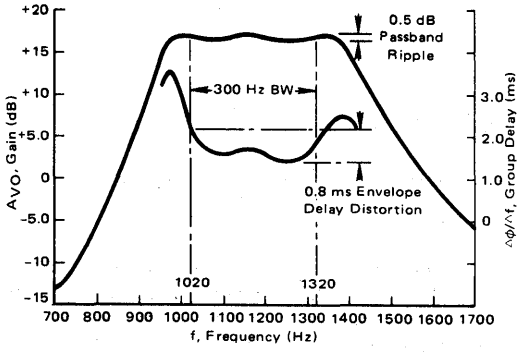


FIGURE 13b – Answer Filter Gain and Group Delay

The use of the MLM311 as a receive signal limiter provides 40 dB of signal gain while maintaining a limited output level having less than ±2% deviation from a 50% duty cycle with a -25 dBm applied input level ($V_{Rx\ F}$).

The telephone line receive level for the answer only example ranges between -12 dBm and -48 dBm. An active duplexer provides 6 dB of signal gain to these line levels resulting in filter input levels ($V_{Rx\ D}$) between -6 dBm and -42 dBm.

From the above information, the active filter must provide the following passband gain.

$$A_{VO} = |V_{Rx\ D\,min}| - |V_{Rx\ F\,max}| \quad (20)$$
$$A_{VO} = 42\ dB - 25\ dB = 17\ dB\ passband\ gain$$

The amount of operational amplifier gain used in the filter design is based on both the passband gain requirements and the filter center frequency loss.

$$A_{VO\,total} = |A_{VO}\ (passband)| + |A_{VO}\ (center\ frequency\ loss)| \quad (21)$$

$$A_{VO\,total} = 17\ dB + 21.58\ dB = +38.58\ dB$$

This requires that each of the three filter sections provide a gain of:

$$A_{VO} = \frac{+38.58\ dB}{3} = +12.86\ dB \text{ or } 4.41\ volts/volt. \quad (22)$$

Step (7) – Filter Component Values

Now that each section gain, center frequency, and design Q is known, the actual filter component values can be calculated (reference Figure 9).

Section 1:

$F_1 = 1375.52$ Hz
$\omega_1 = 8.6426 \times 10^3$ rad/s
$Q1 = 9.345$
$A_{VO1} = 4.41$ (gain of section)

$C_3 = C_4 = 0.01\ \mu F$ (using equal value capacitors)

$$R_5\ (uncorrected) = \frac{2Q_1}{\omega_1 C} = \frac{2(9.35)}{2\pi(1375.5)(1 \times 10^{-8})}$$
$$= 216.4\ k\Omega \quad (23)$$

$$R_1\ (uncorrected) = \frac{R_5}{2A_{VO1}} = \frac{216.4\ k}{2(4.41)}$$
$$= 24.5\ k\Omega \quad (24)$$

$$R_2\ (uncorrected) = \frac{R_1 R_5}{4Q_1^2 R_1 - R_5}$$
$$= \frac{(24.5\ k)(216.4\ k)}{4(9.35)^2(24.5\ k) - 216.4\ k}$$
$$= 634.9\ \Omega \quad (25)$$

These three resistor values, if used to initially implement the first bandpass section, would not produce exact design goals. Filter response will shift due to non-ideal operational amplifier parameters such as dc gain (A_{VOL}), gain bandwidth product (GBW), and input impedance (z_{in}).

To offset any shift in filter response, new values for selection Q, gain and frequency should be calculated taking into account the operational amplifier parameters. These corrected values will be used to obtain new values for R_5, R_1, and R_2, resulting in a filter response very near design goals.

Corrected values for ω_n, Q_n, and A_{VO_n} are calculated using the following MC1458 operational amplifier parameters.

$A_{VOL} = 1 \times 10^5$ volts/volt
$GBW = 1 \times 10^6$ Hz, 6.283×10^6 rad/s
$z_{in} = 1 \times 10^6$ ohms

$$\omega C_1 = \frac{\omega_1}{1 - Q_1\left(\frac{\omega_1}{GBW}\right)} \quad (26)$$

$$\omega C_1 = 8.755 \times 10^3\ rad/s,\ 1393.4\ Hz$$

$$Q C_1 = \frac{Q_1}{1 - Q_1\left[\frac{2Q_1}{A_{VOL}} + \left(\frac{R_5}{z_{in}} - 1\right)\frac{\omega_1}{GBW}\right]} \quad (27)$$

Plugging in values we obtain:

$Q C_1 = 9.27$

$$A_{VOC_1} = \frac{A_{VO1}}{1 - Q_1\left[\frac{2Q_1}{A_{VOL}} + \left(\frac{R_5}{z_{in}}\right)\frac{\omega_1}{GBW}\right]} \quad (28)$$

$A_{VOC_1} = 4.43$

Using these corrected values of section center frequency, Q, and section gain, solve for the corrected values of R_1, R_2, and R_5:

$$R_5 = \frac{2QC_1}{\omega C_1 C} \quad (29)$$

$$R_5 = \frac{2\,(9.27)}{(8.755 \times 10^3)\,(1 \times 10^{-8})} = 211.7\ k\Omega$$

$$R_1 = \frac{R_5}{2AVOC} \quad (30)$$

$$R_1 = \frac{2.117 \times 10^5}{2\,(4.43)} = 23.89\ k\Omega$$

$$R_2 = \frac{R_1 R_5}{4QC_1{}^2 R_1 - R_5} \quad (31)$$

$$R_2 = \frac{(2.389 \times 10^4)\,(2.117 \times 10^5)}{4(9.27)^2\,(2.389 \times 10^4) - 2.117 \times 10^5}$$

$$R_2 = 632.2\ \Omega$$

Section 2:

$F_2 = 966.1$ Hz
$\omega_2 = 6.07 \times 10^3$ rad/s
$Q_2 = 9.345$
$AVO_2 = 4.43$
$C_3 = C_4 = 1 \times 10^{-8}$ F

Solving as in Section 1 using Equations 23 through 31, we obtain:

$\omega C_2 = 6.1255 \times 10^3$ rad/s, 974.9 Hz
$QC_2 = 9.30$
$AVOC_2 = 4.43$
$R_5 = 303.75\ k\Omega$
$R_1 = 34.28\ k\Omega$
$R_2 = 900.5\ \Omega$

Section 3:

$F_3 = 1152.73$ Hz
$\omega_3 = 7.243 \times 10^3$ rad/s
$Q_3 = 4.596$
$AVO_3 = 4.41$
$C_3 = C_4 = 1 \times 10^{-8}$ F

Solving as in section 1 and 2, we obtain:

$\omega C_3 = 7.281 \times 10^3$ rad/s, 1158.87 Hz
$QC_3 = 4.58$
$AVOC_3 = 4.41$
$R_5 = 125.72\ k\Omega$
$R_1 = 14.24\ k\Omega$
$R_2 = 1676.9\ \Omega$

The complete answer filter is shown in Figure 13a with the filter response and envelope delay curves shown in Figure 13b. If the filter is not optimum after construction, it may be fine tuned by the following method.

In tuning filters, one of the most useful parameters is the sensitivity of the filter to element variations. Sensitivity is defined as a measure of the dependence of a network upon the change of some parameter of the network. The sensitivities of importance to the multiple-feedback bandpass filter must relate R_1, R_2, and R_5 to their effect upon ω_0 and Q. These sensitivities are:

$$S_{R_5}^{\omega_0} = -1/2 \text{ (ratio, no units)} \quad (32)$$

$$S_{R_1}^{\omega_0} = \frac{-1}{2(\omega_0)^2 R_1 R_5 C_3 C_4} \quad (33)$$

$$S_{R_2}^{\omega_0} = \frac{-1}{2(\omega_0)^2 R_2 R_5 C_3 C_4} \quad (34)$$

$$S_{R_1}^{Q} = \frac{R_1}{2(R_1 + R_2)} - 1/2 \quad (35)$$

$$S_{R_2}^{Q} = \frac{R_2}{2(R_1 + R_2)} - 1/2 \quad (36)$$

$$S_{R_5}^{Q} = +1/2 \quad (37)$$

In practice, $R_1 \gg R_2$ such that

$$S_{R_1}^{Q} \to 0$$

$$S_{R_2}^{Q} \to -1/2$$

These sensitivities imply that to change section Q, R_2 should be adjusted. If R_2 were increased, for example 20%, section Q will decrease 10%. Notice that the sensitivity of Q to changes in R_2 and R_5 is equal and opposite in magnitude. This implies that if R_2 and R_5 are changed by the same percentage, but in opposite directions, section Q will not change. Also, as R_5 is adjusted, it changes the section center frequency by a ratio of -1/2.

Filter Tuning Procedure

Section Center Frequency:

(a) Increase/decrease R_5 for a corresponding decrease/increase in section center frequency ω_0.
(b) Increase/decrease R_2 by the same percentage of increase/decrease applied to R_5 in step (a) to maintain constant sectionQ.

Section Q:

(a) Increase/decrease R_2 for a corresponding decrease/increase in section Q.

ORIGINATE FILTER DESIGN

Basically, the originate receiving filter design procedures are identical to the answer filter example. The one major difference is that the filter center frequency is shifted to accept 2025 – 2225 Hz signals. One might also note that the second harmonics of the local transmit signals in the originate mode (1070 – 1270 Hz) fall within and just

outside of the passband for the originate receive filter. For this reason, the originate only modem designer may want to provide a transmit bandpass filter to suppress harmonics produced by the local transmit carrier (see Figure 15).

The three section design parameters and component values for the 6-pole originate receive filter are:

Section 1:

F_1 = 2425.81 Hz
Q_1 = 16.56
A_{VO1} = 4.48
$C_3 = C_4 = 1 \times 10^{-8}$F
R_1 = 24.26 kΩ
R_2 = 199.76 Ω
R_5 = 217.258 kΩ

Section2:

F_2 = 1985.62 Hz
Q_2 = 16.67
A_{VO2} = 4.48
$C3 = C4 = 1 \times 10^{-8}$F
R_1 = 29.85 k
R_2 = 242.36 Ω
R_5 = 267.23 kΩ

Section 3:

F_3 = 2154.01 Hz
Q_3 = 8.32
A_{VO3} = 4.43
$C_3 = C_4 = 1 \times 10^{-8}$F
R_1 = 13.88 kΩ
R_2 = 458.85 Ω
R_5 = 122.913 kΩ

The complete 6-pole receive originate filter is shown in Figure 14a, with the response and envelope delay curves shown in Figure 14b.

8-POLE, -50 dB RECEIVE AND 4-POLE, -25 dB TRANSMIT FILTER DESIGN

A complete full duplex modem system will most likely require operation with input signals down to -50 dBm at the line input. This requires a receive filter network having at least 8 poles to provide the necessary attenuation to adjacent duplex channel interference and a local transmit filter having 4 poles to provide 25 dB local transmit signal harmonic rejection. The construction of an 8-pole or 4-pole filter takes on the same cascaded form as the illustrated 6-pole design example. Therefore, only the component values for the 8-pole and 4-pole filters are tabulated in Figure 15 without the individual circuit diagrams.

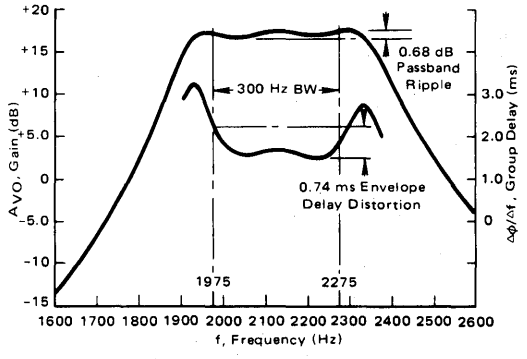


FIGURE 14b – Originate Filter Gain and Group Delay

RECEIVE ORIGINATE

Section	1	2	3	4
R_1 (Ω)	31.42 k	39.54 k	14.71 k	16.1 k
R_2 (Ω)	146.8	181.15	396.29	432.32
R_5 (Ω)	288.64 k	363.27 k	132.15 k	144.66 k

RECEIVE ANSWER

Section	1	2	3	4
R_1 (Ω)	31.08 k	46.34 k	14.51 k	17.1 k
R_2 (Ω)	468.48	690.57	1397.94	1643.88
R_5 (Ω)	283.33 k	422.31 k	131.38 k	154.8 k

TRANSMIT ORIGINATE

Section	1	2
R_1 (Ω)	15.73 k	20.56 k
R_2 (Ω)	1218.55	1586.55
R_5 (Ω)	130.47 k	170.47 k

TRANSMIT ANSWER

Section	1	2
R_1 (Ω)	16.17 k	18.78 k
R_2 (Ω)	366.95	423.79
R_5 (Ω)	133.25 k	154.81 k

Note: All Capacitors = 0.01 μF

FIGURE 15 – 8-Pole, -50 dB Receive and 4-Pole, -25 dB Transmit Filter Values

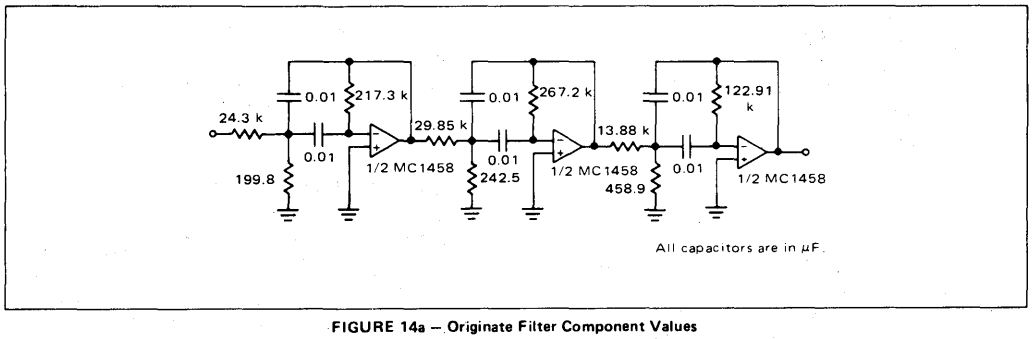


FIGURE 14a – Originate Filter Component Values

AUTOMATIC ANSWER/ORIGINATE MODEM SYSTEM

The filter design for a fully automatic answer/originate modem system must have switchable bandpass characteristics. By tabulating the previous component values for both the answer and originate filters, one can draw some conclusions on how to best switch the filter from one range to the other. The following example uses the previous derived values for the 6-pole receive filter. Figure 16 indicates that switching in different values of R_2 for all three sections and a different value for R_5 in the second section would provide the required switchable answer/originate filter. By adjusting the non-switched resistors to the average value between the answer and originate filter values, the more accurate the first switchable filter prototype will be. A semiconductor switch is used to switch values of R_2, and operates in shunt to ground. The best choice for the shunt switch is to use a low on-resistance bipolar device such as the 2N3904. For switching R_5 of section 2, a high off resistance device is required due to the high series resistance in the feedback path of the operational amplifier. An MFE2005 N-channel junction FET was selected to do this job. Figure 17a illustrates the fully automatic answer/originate switchable filter system. Also shown are the transmit buffer, duplexer, threshold detector, limiter, and mode control level translator sections. The level translator, which provides the correct on/off voltage levels to the bipolar FET switches, receives its answer/originate command from the MC6860 modem mode control output pin. The measured response and envelope delay for the switchable 6-pole receive filter design is shown in Figure 17b.

Figure 18 illustrates the complete modem system with the RS-232 interface to the CBS data coupler, and the direct interface to a CBT data coupler. Automatic disconnect option inputs are handled by PC board mounted switches. The complete automatic modem, less the power supply, may be easily constructed on a single 4 x 5 printed circuit board.

CONCLUSION

A low-speed modem design has been presented using the MC6860 LSI MOS digital Modem integrated circuit. Included has been a system design example using filter design tables and equations to develop a complete modem system. Also included have been component values for filter designs which may be used to develop full duplex modem systems.

The availability of this LSI modem circuit along with the presented filter designs should provide a very useful building block for the OEM modem and terminal designers by providing him precise digital modulation, demodulation, and supervisory control. The modem designer will find that a design approach using the MC6860 modem will also provide an impressive system size reduction as well as a better price-performance choice for his present and future low speed modem designs.

Resistor	Answer 1070-1270 Hz	Originate 2025-2225 Hz	Average or Δ Value	Answer Switched	Originate Switched
R_{11}	23.89 k	24.26 k	24.08 k	24.1 k	24.1 k
R_{21}	632.2	199.76	Δ 432.4	632	200
R_{51}	211.7 k	217.26 k	214.48 k	214.5 k	214.5 k
R_{12}	34.28 k	29.85 k	32.07 k	32.1 k	32.1 k
R_{22}	900.5	242.36	Δ 658.2	900	242
R_{52}	303.75 k	267.23 k	Δ 36.5 k	304 k	267 k
R_{13}	14.24 k	13.88 k	14.06 k	14.06 k	14.06 k
R_{23}	1676.9	458.85	1218.05	1677	459
R_{53}	125.72 k	122.91 k	124.32 k	124.3 k	124.3 k

FIGURE 16 – Switchable Modem Filter Values

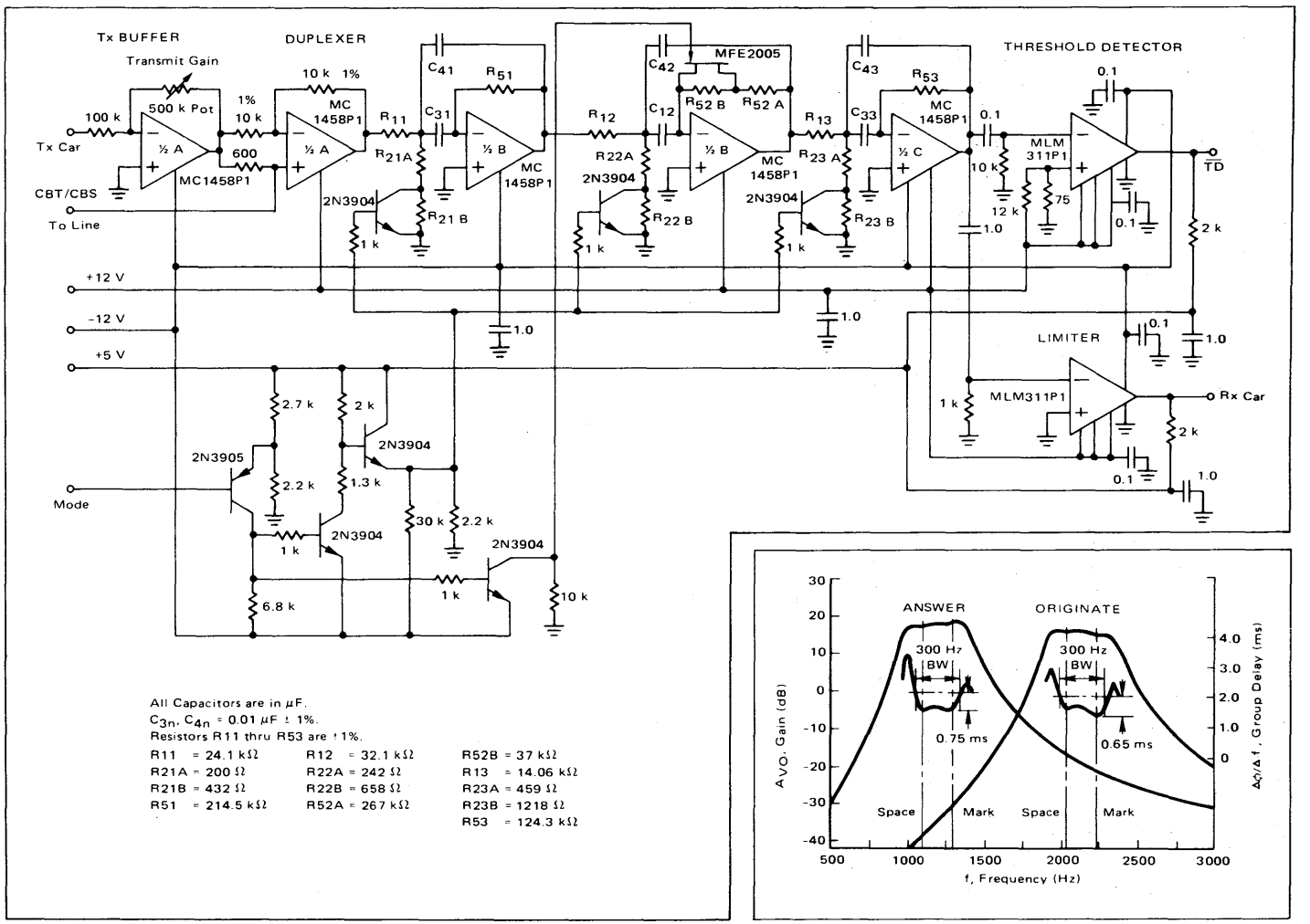


FIGURE 17a – Switchable Filter/Duplexer

FIGURE 17b – Switchable Filter Response

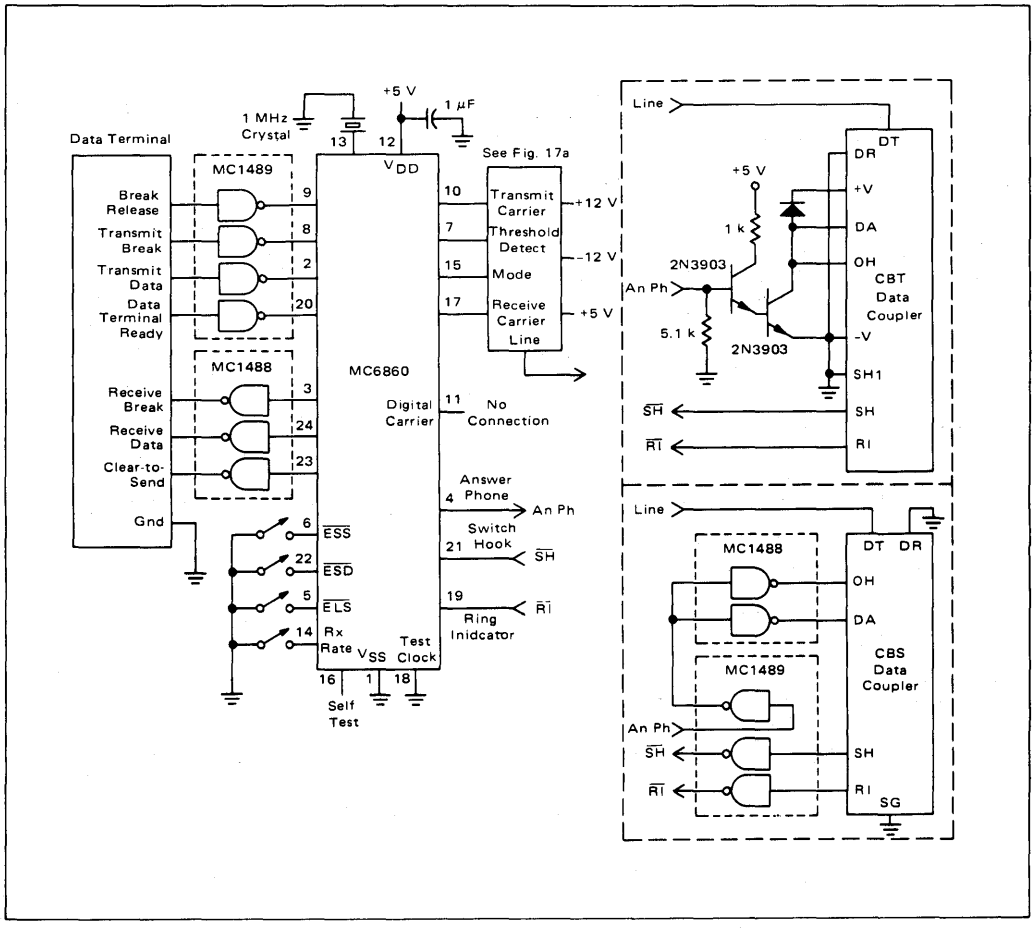


FIGURE 18 – Modem System

MOTOROLA

Application Performance of the MC6860 MODEM

A MODEM fills the need in a data communication network to provide interface between a telephone network, which carries analog information, and a computer system that operates on digital information. Figure 1 illustrates a typical MODEM application in which both transmitting (modulation) and receiving (demodulation) sections are contained within each MODEM system. Traditionally, these signal conversion operations are performed by analog methods whereas Motorola's recently introduced MC6860 MODEM modulates and demodulates using digital techniques.

3

MODEM Operation

Basically, a MODEM converts logical "1" and "0" levels into analog frequency tones and back again to "1"s and "0"s. These tones have the specific frequencies listed in figure 2. Two pairs of tones are listed for each modem, one set for transmitting and one set for receiving, so that two-way (full-duplex) operation is possible over a single transmission line. The computer terminal MODEM that places a call is referred to as the originate MODEM, (transmitting tones of 1070 Hz and 1270 Hz) whereas

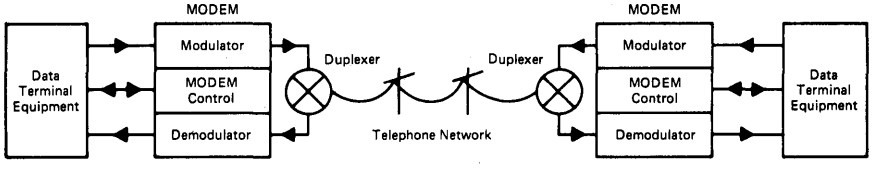
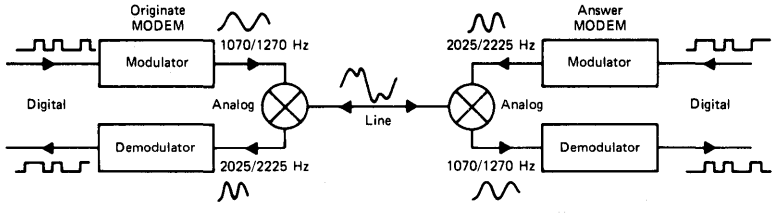


FIGURE 1. Typical MODEM System Application



Mode	Originate		Answer	
	Send	Receive	Send	Receive
Mark	1270 Hz	2225 Hz	2225 Hz	1270 Hz
Space	1070 Hz	2025 Hz	2025 Hz	1070 Hz

FIGURE 2. System Frequency Assignments

the data terminal receiving this call is the answer MODEM, (transmitting tones of 2025 Hz and 2225 Hz).

Modulation

In an analog MODEM, one constructed of linear devices, modulation is accomplished by shifting the frequency of a sinewave oscillator. This oscillator is usually constructed using tunable cup core inductors resonated with precision capacitors, a technique that can be expensive both in terms of components and the tuning necessary to meet frequency requirements. Temperature compensation of these oscillators is also necessary to maintain frequency tolerances across the operating temperature of the MODEM system.

In the MC6860 digital MODEM, a 1-MHz frequency is divided down by digital counters to obtain the desired modulation transmit frequencies. Outputs of this counter chain are used, with a resistor ladder network and decoder, to generate an eight-level analog output signal. Each of the eight levels of the digital sinewave output has been designed to provide the composite waveform with a maximum amount of signal energy at the fundamental frequency. This lowers second harmonic content; consequently, less interfering signal is generated which could cause problems during full-duplex operation. Output frequencies with an accuracy of 0.1% result from this digital modulation technique. The only external component necessary for MC6860 modulator operation is either a 1-MHz signal source or a 1-MHz crystal.

Demodulation

Demodulation in an analog MODEM depends on frequency discrimination obtained using narrow-bandwidth bandpass filters centered about each of the two possible received frequencies. When the received signal frequency is centered within one of these bandpass filters, a threshold comparator (slicer) is switched producing either a logic "1" or "0" output level dependent upon which frequency within either the originate or answer tone pairs was received. Analog demodulation deals directly with the continuously changing analog signal although periodic frequency changes occur. Recognition of these frequency changes is normally within 2% of the actual change in relationship to the total received signal time interval. By adjusting the threshold of the slicer, the output interval distortion (jitter) can be reduced to values of 1% or less.

Digital demodulation in the MC6860 takes place in the following manner. The received analog frequency is first shaped into a square wave by the use of an external symmetrical limiter. Once shaped, the signal's half-cycle period is measured and this information is used to determine if a space or a mark frequency is being received. For example, the frequencies of 1070 Hz and 1270 Hz have half-cycle periods of 467 μs and 393 μs, respectively. The optimum period for discriminating between a mark (1270 Hz) or a space (1070 Hz) frequency is the mean of these two half-cycle periods, or 429 μs, which may be easily measured by a counter circuit.

Using this half-cycle measurement technique, a quantization error results as is depicted in figure 3. When transition is made between a mark and space condition, the interval for that particular half-cycle depends on the phase of the half-cycle in which the change in frequency occurs. Thus, if the frequency changes early in the half-cycle period, this measured interval will closely approximate that of the new frequency period. However, if the frequency changes later in the half-cycle period, determination of change will be based on the previous condition. Because counter techniques are used, a discrimination point exists in the half-cycle interval such that the new information (i.e., the change from space to mark or vice versa) will be detected at the end of the interval if the frequency change occurs prior to the discrimination point. If the frequency change is made after the discrimination point, the new information will not be effectively detected until the end of the next interval, at which time this measured half-cycle interval will be totally determined by the new frequency period. The net result of this detection scheme is that new data is effectively detected within regions either half an interval prior to the discrimination point or half an interval after the discrimination point.

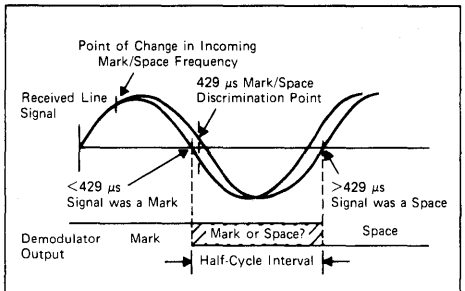


FIGURE 3. Mark/Space Uncertainty Region

The quantization error associated with this half-cycle technique leads to an output distortion condition called jitter. As defined in EIA Standard, RS-404, "Standard for Start-Stop Signal Quality Between Data Terminal Equipment and Non-Synchronous Data Communication Equipment" and generally accepted in the industry, jitter is a measure of the time displacement of the detected transistions between signal states from their ideal instants. This is normally expressed as a percentage of the unit bit interval. From previous discussion then,

the peak jitter associated with the demodulation scheme used in the MC6860 can be expressed in equation form as

$$\phi_J \approx \frac{1/4 \text{ Frequency Cycle Interval}}{\text{Bit Period Interval}} \text{ X } 100\%$$

Since jitter is maximized by using the largest frequency cycle interval which occurs during a space logic condition, phase jitter can be expressed as

$$\phi_J \approx \frac{\text{Bit Rate}}{4\text{X Space Frequency}} \text{ X } 100\%$$

Tabulated in figure 4 are peak values of phase jitter that can be expected at the demodulator output of the MC6860 MODEM.

FIGURE 4. MC6860 Demodulator Output Peak Phase Jitter (ϕ_J)

Data Rate Bits per Sec.	Answer Mode ϕ_J (Peak %)	Originate Mode ϕ_J (Peak %)
300	7.0	3.7
200	4.7	2.5
150	3.5	1.8
110	2.6	1.4

Although the demodulation technique used in the MC6860 leads to a somewhat larger amount of jitter than that from demodulators using linear devices, the overall jitter in a system is dependent on other factors including filter characteristics, transmission line characteristics, and system noise. These generally have about the same effect whether linear or digital techniques are used in the demodulation process; however, their contribution to system jitter may well be more significant than those of the demodulation process itself.

Why is Jitter a Concern to the MODEM User?

The effects of jitter can be thought of as a noise impingement on the data itself and since the complete bit interval may not be present, more errors may result. A look at many applications shows that at higher data rates the MODEM will interface with terminal transmitter/receiver devices, or asynchronous communication interface adapters. Such interface units sample the bit interval very close to the mid-point as indicated in figure 5. Consequently, a very large amount of phase jitter must be present before any errors occur. At slower data rates where mechanical MODEMS may be used, the system jitter is appreciably less than that of the MC6860 demodulator indicated in figure 4 and has little effect on device operation. Thus the jitter associated with the digital demodulation technique can be tolerated in a wide range of applications and provide acceptable MODEM system performance.

Bit Error Rate Performance

MODEM system performance is best shown by documenting the MODEM'S back-to-back error rate performance when the system is subjected to noise. Back-to-back operation is where MODEM A transmits to MODEM B over a connecting line and both the transmitting and receiving ports are locally available to a test instrument. The test setup shown in figure 6 uses a Bowmar 251A error rate test set to measure the MODEM system performance. A 511-bit pseudo random data pattern is supplied to MODEM A's modulator for transmission over the line to MODEM B's demodulator. The modulator's analog output is combined with noise at a line mixer unit and a signal of measured signal-to-noise ratio is delivered to the line input of MODEM B. MODEM B, operating in the originate mode (receiving 2025/2225 Hz tones), demodulates the received analog data into digital data in the presence of noise and delivers this data stream to the Bowmar test set.

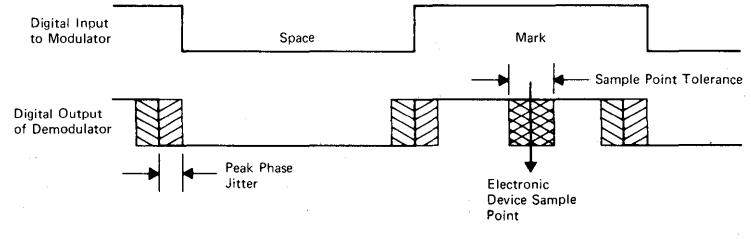


FIGURE 5. Demodulator Data Bit Output

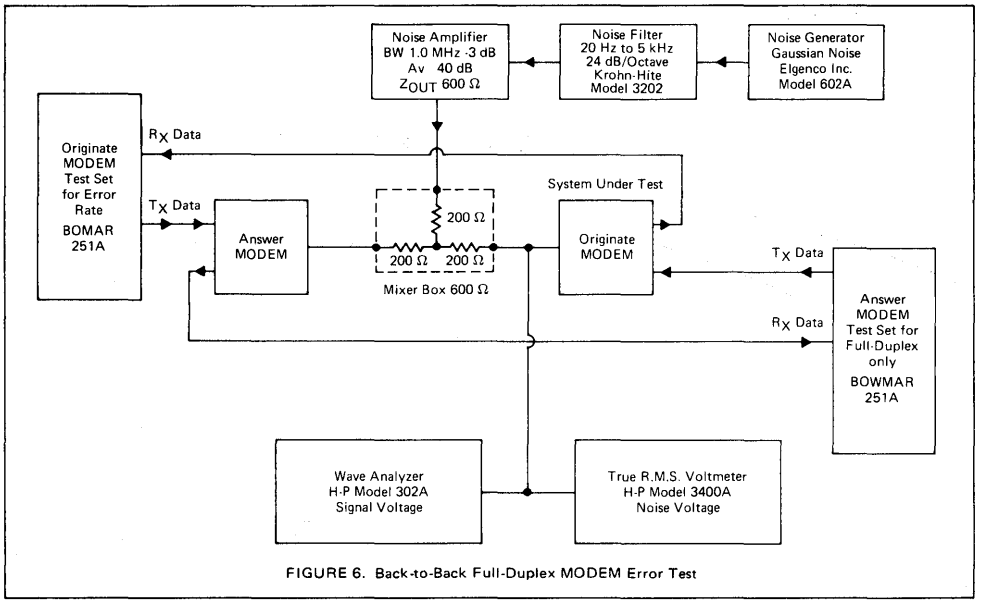


FIGURE 6. Back-to-Back Full-Duplex MODEM Error Test

The test set will compare the received data bit-for-bit with the transmitted data and each difference will be recorded as a bit error. Errors are recorded for a specified number of transmitted bits and the ratio of the number of bit errors to the number of bits sent is defined as the probability of bit error. This ratio is plotted against the measured line signal-to-noise ratio, figure 7, which then represents a MODEM'S system performance. Figure 7 has included for comparison a plot for a Bell 113A MODEM, an industry standard. Curves are shown for a MC6860 MODEM system operating in a full-duplex mode. These curves indicate that the MC6860 subjected to system noise provides excellent bit-error rate performance.

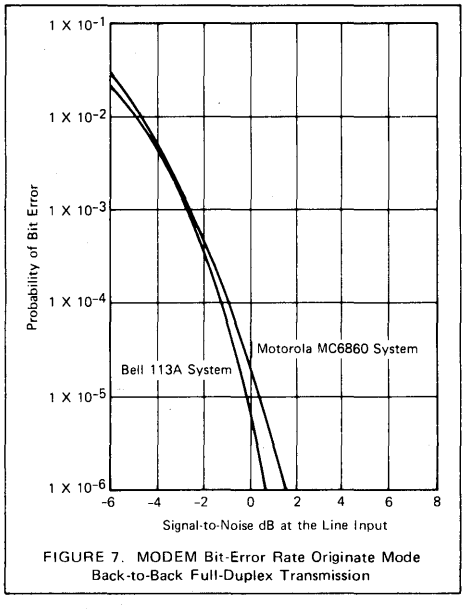


FIGURE 7. MODEM Bit-Error Rate Originate Mode Back-to-Back Full-Duplex Transmission

Summary

Although the jitter resulting from the digital demodulation technique used in the MC6860 MODEM is somewhat larger than that obtained using linear techniques, performance data shows that the MC6860 provides excellent performance in data communication systems. Advantages of small size, low-system expense, and good performance make the MC6860 MODEM a very cost-effective device worthy of serious consideration for your data communication applications.

MC14412/MC145440 CHIP SET SETS NEW STANDARD IN 300 BAUD MODEM DESIGNS

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The advent of the MC14412/MC145440 modem chip set offers a dramatic reduction in the cost and in the complexity of 300 baud modem designs. The MC14412 is a CMOS device that performs the modulate/demodulate functions of a basic 300 baud modem. The MC145440 is a CMOS switched-capacitor filter that provides the necessary upper- and lower-band separation for full-duplex operation at 300 baud. By adding a small number of components, a complete Bell 103-compatible modem can be built.

HOW DOES A 300 BAUD MODEM WORK?

A 300 baud modem is perhaps the most common type of modem encountered in data communications. Its advantages are many: low cost and complexity, full-duplex operation over a two-wire connection, and reliable operation over the normal dial-up telephone network. It has found a home in banks, offices, laboratories, and computing centers; and now with the increasing popularity of personal computers, it is even in our own homes.

These 300 baud modems (based overwhelmingly on Bell 103 operation) employ a modulation scheme called Frequency Shift Keying (FSK), a slightly intimidating term for a simple technique of using different frequencies to encode digital data for analog transmission over the telephone lines. In other words, a logic one causes the modem to transmit one frequency while a logic zero causes another frequency to be transmitted. Full-duplex transmission over a two-wire telephone line is achieved by separating the bandwidth of the line (300-3,000 Hz) into a low band and high band, each containing two frequencies for a logic one or zero. These two frequencies are referred to as mark and space, with mark representing the higher of the two frequencies. The frequency designations for Bell 103 operation are shown in Figure 1.

To avoid two modems trying to transmit data on the same band, a simple protocol usually exists. Whenever one modem calls another modem, the calling or **originate** modem transmits on the low band and receives on the high band. The modem you are calling will operate in the **answer** mode, transmitting on the high band and receiving on the low band. Variations on this theme are answer-only and originate-only modems that only transmit or receive on one particular band.

Communication theory predicts that the signal bandwidth of binary (that is, two frequencies in each band) FSK operating at 300 baud, with mark and space 200 Hz apart, is approximately 300 Hz.[1] This bandwidth is centered about the apparent carrier frequency halfway between the mark and space frequencies. In order to properly demodulate the FSK signal and attenuate out-of-band noise, the filter should have a similar bandwidth of 300-400 Hz for each band. Another concern is that the filter minimize envelope delay distortion (EDD), which is a measure of the linearity of a filter's phase response. Excessive EDD can distort the signal enough such that baud transitions smear and ultimately produce an error (this problem is usually called intersymbol interference). The MC145440 filter meets these requirements, as is shown in Figure 2.

300 BAUD MODEM EVALUATION BOARD

The schematic for a simple 300 baud modem that we have designed for an evaluation board is shown in Figure 3. This board allows the user to evaluate the performance of the MC14412/MC145440 system over a telephone line. An RS-232C connector permits testing with a terminal or any other RS-232C compatible equipment. A TTL compatible interface is also provided through the coaxial connectors TTL data in and TTL data out. The user can program this board to accommodate either single or dual power supplies. Switches and solderable straps allow selection of originate/answer, loop-back, different crystal frequencies, and other options, as are described in Figure 4.

To set up the board for a particular power supply configuration, it is important to understand the operation of the single/dual strap and how it relates to the power input jacks — V_{DD}, V_{SS}, and V_{AG}. When connecting a single supply of +5 to +6 V, the board must be strapped to use the internal V_{ref} generated by the MC145440 (E4-E5). Therefore, the +V would be connected to V_{DD} and ground to the V_{SS} terminal. The single strap (E13-E14) serves to

define the RS-232C signaling ground and the data in/out connectors' ground at the + V ground. To provide a negative supply below the + V ground for the RS-232C interface, the RS-232 V_{SS} jack provides access to the MC1488 drivers' negative supply input ($-V_{RS}$). When wanting to run the board from a ± supply, the V_{ref} strap (E4-E5) would be open and the single/dual point would be strapped for dual operation (E13-E15). + V would be connected to V_{DD}, − V to V_{SS}, and the common or ground of the supply would be connected to V_{AG}. This procedure is illustrated in Figure 5. **An important note for use of the RS-232C port is that the board must be run at either ±6 V or at +6 V with $-V_{RS}$ connected to −6 V for proper operation of the MC1488 RS-232C drivers.**

Data \ Band	Low Band	High Band
Mark	1270 Hz	2225 Hz
Space	1070 Hz	2025 Hz

Orig = Transmit On Low Band
Receive On High Band
Ans = Transmit On High Band
Receive On Low Band

FIGURE 1 — Bell 103 Frequency Designations

THEORY OF OPERATION

Asynchronous digital data is input from the RS-232C port or from the data in coaxial connector (TTL logic levels) by proper selection of S1. The MC14412 then transmits either a mark or space frequency in the form of a digitally-stepped waveform (the output of the resistor-string D/A). This waveform is ac-coupled to remove any dc offset. R3 sets the input level to the transmit filter and subsequently sets the output level to the line.

The signal at U2 pin 3 is then filtered and amplified by 10 dB and output at TxO, pin 2. This output will supply ± 5 mA at 4 V peak when the part is running on ± 5 V. This signal is then routed to the input of the active duplexer as well as to transformer T1 and on to the line.* The purpose of the duplexer is to help reject transmit signal energy while amplifying the receive signal at TP1 by 6 dB. Balancing the duplexer is an important procedure that minimizes transmit signal interference, and is shown in Figure 6. T1 is a typical 600:600 ohm telephone coupling transformer whose primary is rated to handle the 20-80 mA of dc loop current possible when seizing the telephone line. ZN1 is a transient-suppressor device designed to absorb any voltage spike above a certain clamp level. R8 provides surge current limiting to help protect the ZN1.

The receive signal at TP1 is routed to the non-inverting terminal of the duplexer op amp (pin 17). After being amplified by 6 dB, it is input to the receive filter at RxI (pin 13). The filter output is at RxO (pin 14) and this is fed to the limiter and carrier detect circuits. Between the actual input to the limiter and RxO is an optional gain of two stage (U4) which allows receive sensitivity down to − 45 dBm without having to trim the offset of the limiter comparator (U5A). The output of the gain stage is then filtered by a simple RC low pass that attenuates the high frequency switching noise inherent in a switched-capacitor filter. The signal at TP4 is ac-coupled into the limiter which converts the sinusoidal waveform into a symmetrical square wave which is then input to the MC14412 (pin 1) for demodulation. Careful layout of the limiter is important since extraneous high frequency noise can create jitter in the square wave output, degrading bit-error-rate performance. Selection of a low-offset comparator for the limiter is also critical since a higher offset will produce

*Before actual connection to the telephone line, the FCC requires that either a DAA be placed between the modem and the line or that the entire modem be certified and registered under the provisions of Part 68.

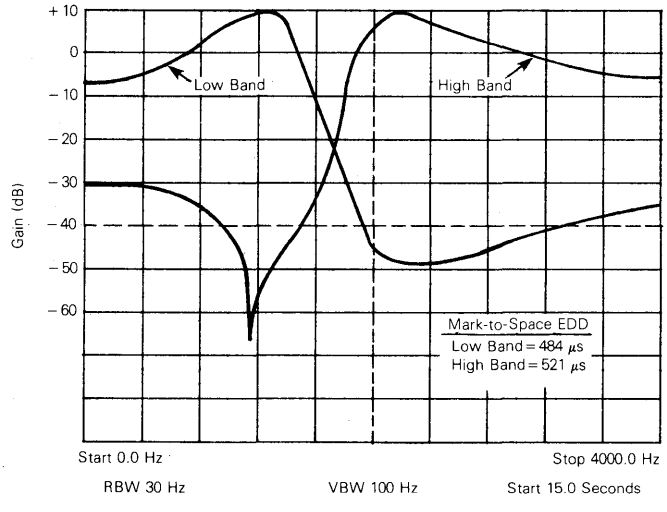
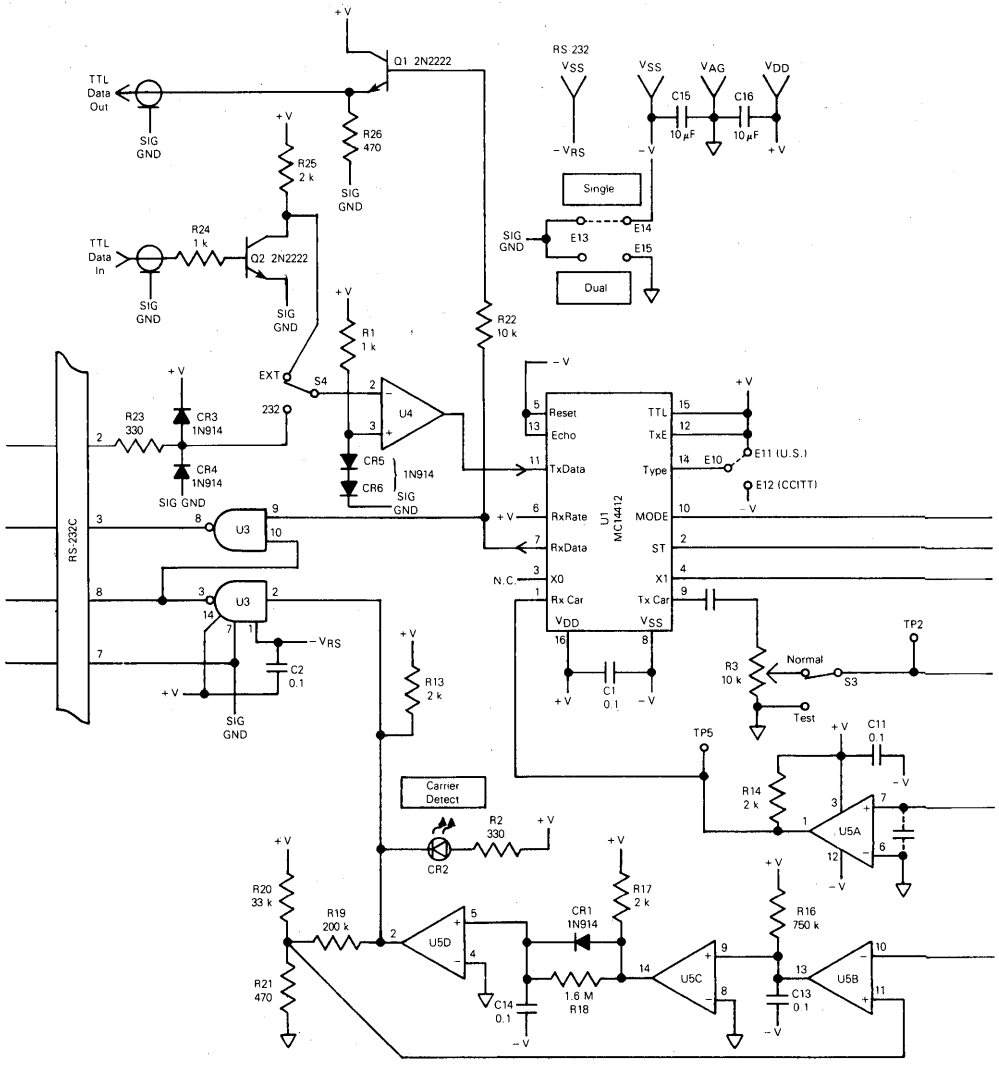


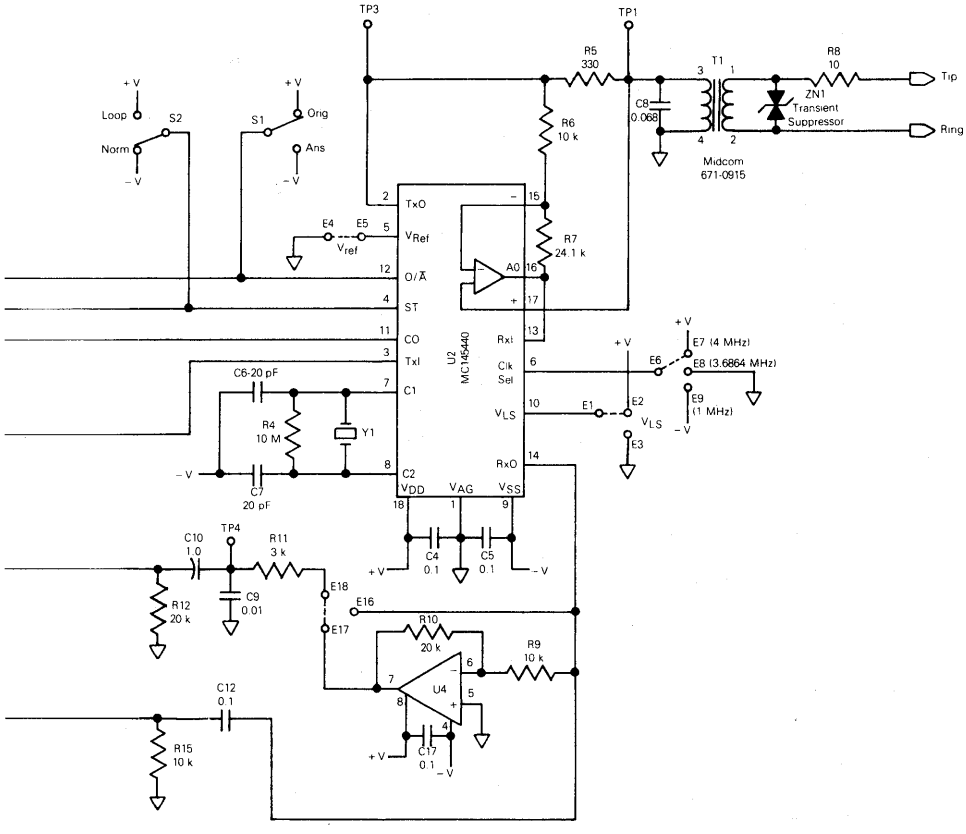
FIGURE 2 — Frequency Response of
High Band and Low Band of MC145440

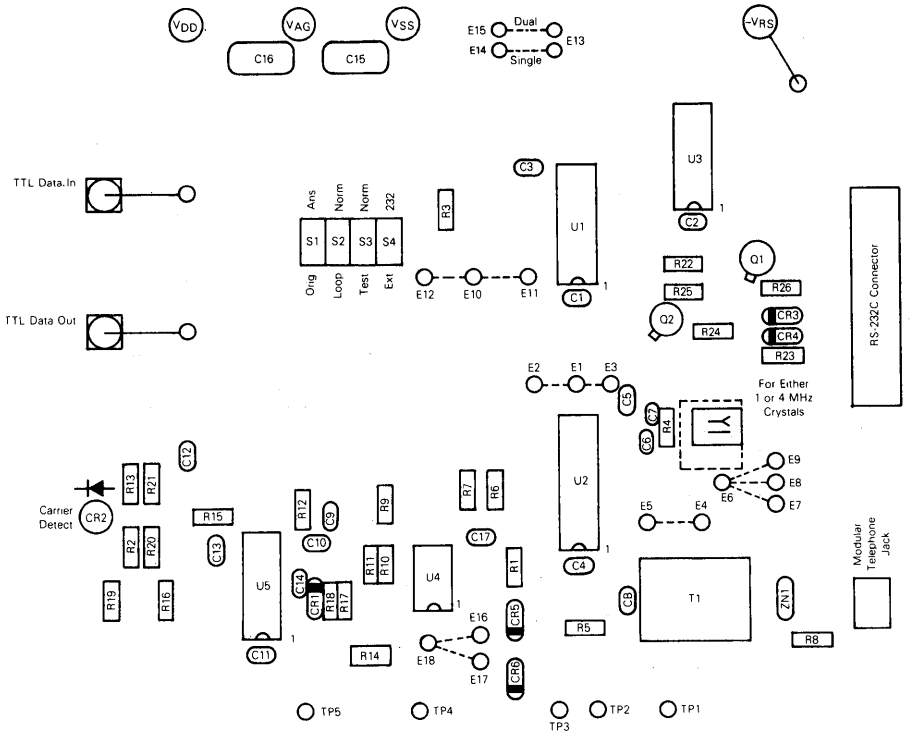


*May be needed for noisy environments. Should be ≈500-1000 pF.

FIGURE 3 - MC14412/MC145440 Modem Evaluation Board Schematic

U1 MC14412
U2 MC145440
U3 MC1488
U4 MC4558
U5 LM339A





Strapping and Switch Information

E1, E2, E3	Selects logic input/output levels. E1-E2 for CMOS swinging V_{DD} to V_{SS}. E1-E3 for TTL swinging from V_{AG} up.
E4, E5	Provides mid-supply reference voltage for use in single-supply operation; left open in dual supply.
E6, E7, E8, E9	Selects crystal frequency. E6-E7 4.0 MHz operation E6-E8 3.6864 MHz E6-E9 1.0 MHz
E10, E11, E12	Selects U.S. or CCITT operation. E10-E11 U.S. E10-E12 CCITT
E13, E14, E15	Selects signaling ground. E13-E14 SIG GND = V_{SS} (singly supply) E13-E15 SIG GND = V_{AG} (dual supply)
E16, E17, E18	Gain strap in. E18-E17 Gain in E18-E16 Gain out

Switches

S1	Selects originate or answer mode of operation.
S2	Selects normal operation or loop test in which the MC14412 and MC145440 will modulate and demodulate on the same band. Data input to the MC14412 will then be looped and available at MC14412 output.
S3	Selects normal operation or a test mode where TxI input is connected to V_{AG}. This allows measurement of receive level.
S4	Selects RS-232C data or external TTL data.

FIGURE 4

more duty-cycle distortion and perhaps exceed the 50 ±2% duty-cycle requirement of the MC14412.

The carrier detect circuit consists of U5B through U5D. The output of the first comparator (pin 13) goes into a decay control network formed by R16 and C13. When carrier is detected, pin 13 goes low, discharging C13. As the waveform passes below its peak, C13 begins to charge through R16 and therefore controls the decay response of carrier detect. The network on the output of U5C pin 14 controls the attack time and consists of R17, R18, CR1, and C14. When carrier is present, pin 14 goes low, discharging C14 through R18. Therefore, carrier must be present for a certain amount of time before it is recognized and causes pin 2 to switch low. The time responses for the attack and decay networks are:

Attack time = R18C14 ln(½) = 111 ms

Decay time = R16C13 ln(½) = 52 ms.

Three dB of hysteresis is accomplished by the resistor network of R19-R21. The whole carrier detect circuit will turn on at a received signal level of −40 dBm at TP1 and turn off at −43 dBm when operating at ±5 V.

Several features of the MC145440 merit special consideration because of the flexibility they allow the designer. One is the clock output pin (pin 11), which provides a 1 MHz clock to the MC14412 when operating the MC145440 at either 1 or 4 MHz. The clock select pin (pin 6) controls the selection of which external crystal to use — 4, 1, or 3.6864 MHz. The big advantage here is that a 4 MHz crystal is much cheaper than a 1 MHz crystal, although power consumption of the MC145440 increases slightly. Output levels are defined by the voltage at the V_{LS} pin (pin 10) for use of either CMOS or TTL logic. The V_{ref} output (pin 5) generates a mid-supply voltage between V_{DD} and V_{SS} for use in single-supply applications. As you can see, the design of the MC145440 was geared to making the modem designer's task much easier.

RECEIVE SENSITIVITY TESTING

The test set-up for evaluating receive sensitivity in the originate and answer modes is shown in Figure 7. The procedure for determining the receive level at the line side of T1 (A and B) is to first adjust the transmit signal level at A and B to about −9 dBm (via R3 and with the line side of the transformer terminated in 600 ohms), which is the maximum signal level allowed on the line. Then connect the receive signal and decrease its level until the bit error rate (BER) exceeds 1×10^{-5}. Next, close S3 to the test position and measure the signal level at A and B with a bandlimited voltmeter, such as the HP 3551 with 3 kHz flat filtering. This is then the receive sensitivity — the lowest level at which the demodulator begins to make significant errors on a back-to-back set-up. Measured performance on the evaluation board was −45 dBm in both the originate and answer modes.

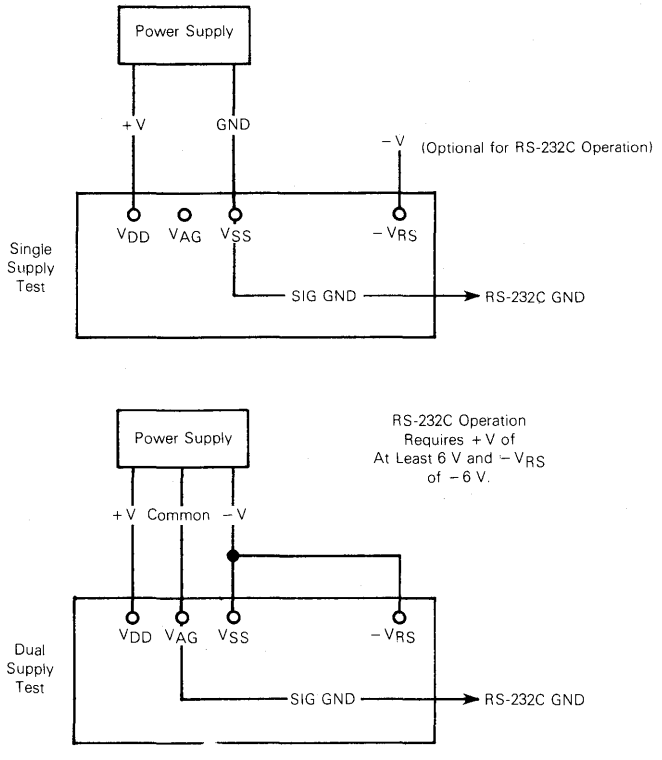


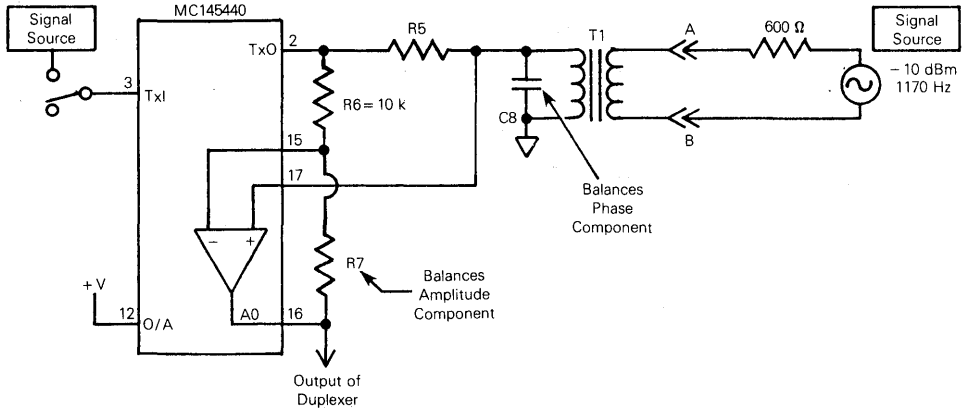
FIGURE 5 — Power Supply Set-Up

CONCLUSIONS

A simplified method of designing a basic 300 baud modem with the MC14412/MC145440 has been presented which offers very good performance and ease of implementation. The attention to detail which is reflected in the options and features of the MC145440 help the design engineer meet the variety of modem criteria that might otherwise exclude other parts. One common design requirement might be for a line-powered modem in which power consumption would be important. Since both the MC14412 and MC145440 can work at 5 V, a very-low-power system can be designed that operates on only +5 V. A possible circuit for this application that stresses minimum cost and power consumption is shown in Figure 8 with the component layout shown in Figure 9.

Reference

1. K. Sam Shanmugan: *Digital and Analog Communication Systems*, Wiley, New York, 1979.



The purpose of the duplexer is to help reject transmit signal energy from the receive signal. Theoretically, a duplexer can be "tuned" to achieve infinite rejection — where the phase and amplitude of the inverting and non-inverting signals cancel through the duplexer op-amp. In practice however, telephone line impedances vary enough such that only about 10-15 dB of rejection can be expected. To attain this rejection, it is recommended that the duplexer components (R5, R6, R7, and C8 in the schematic) be tuned for the impedance and loss characteristics of the particular type of transformer being used. This will minimize the impedance variation of the line. Once these component values have been determined for a particular transformer type, further trimming is usually unnecessary on a board-to-board basis. A recommended procedure for balancing the duplexer, which was used in finding the values in the schematic, is as follows:

1. First, put the TxI input to V_{AG}. Next, connect a 600 ohm signal source to points A and B (nominally – 10 dBm @ 1170 Hz). Tweak R5 until the loss at point A and B is exactly 6 dB. This allows maximum power transfer through the transformer.
2. With R5 at this new value, replace the signal source with a 600 ohm resistor at points A and B. Now feed the TxI input with the signal source at the same level and frequency.
3. Now tune R7 until the signal out of TxO reaches a minimum at A0. Then tune C8 until a new, lower minimum is reached which should be around 30 dB. The phase and amplitude of the two signal components have now been matched for the best rejection over the spread of telephone lines.

FIGURE 6 — Duplexer Considerations

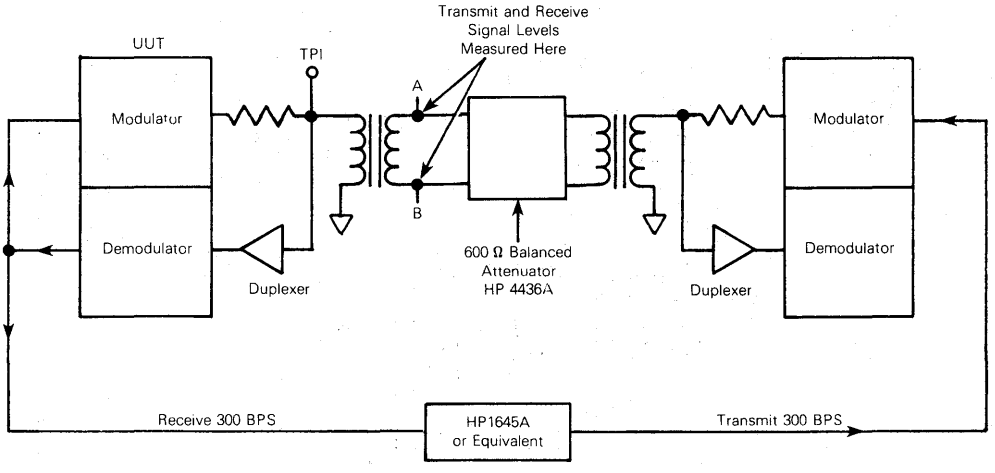
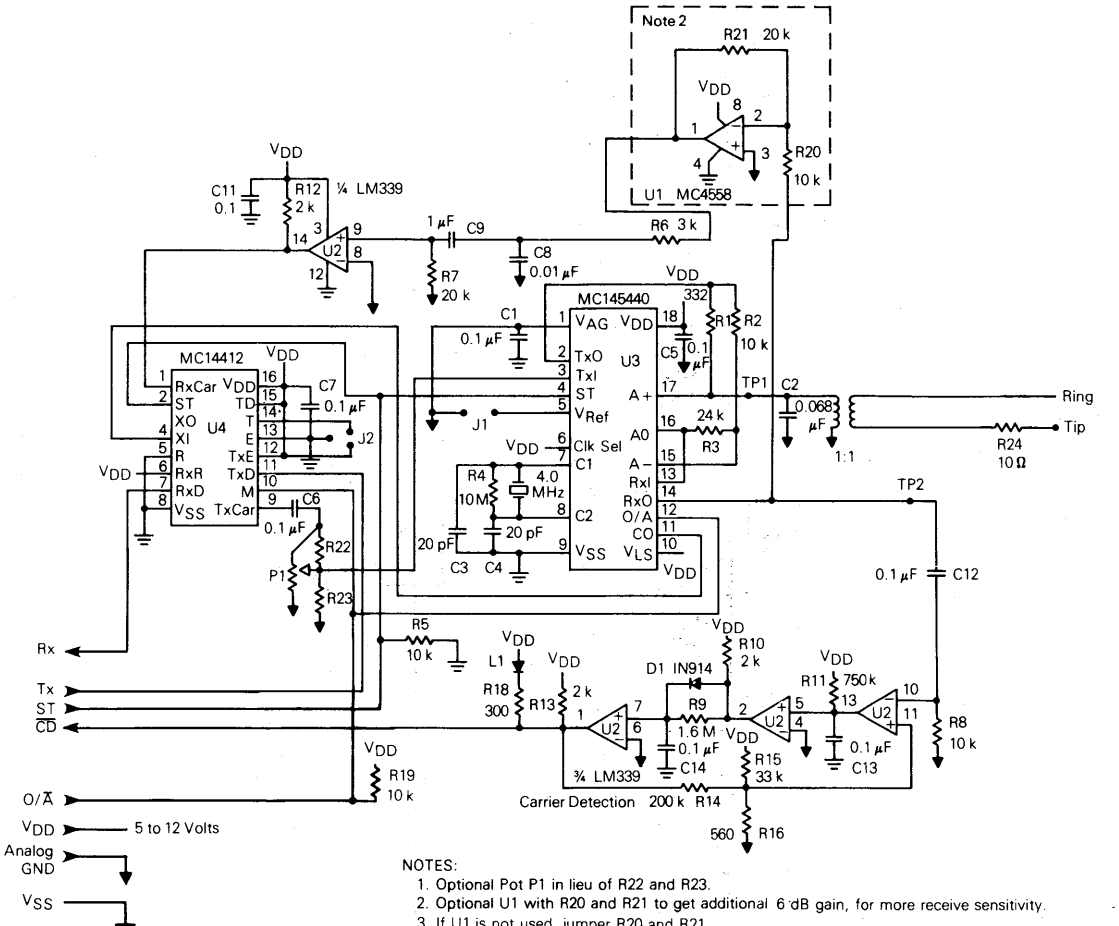


FIGURE 7 — Test Set-Up



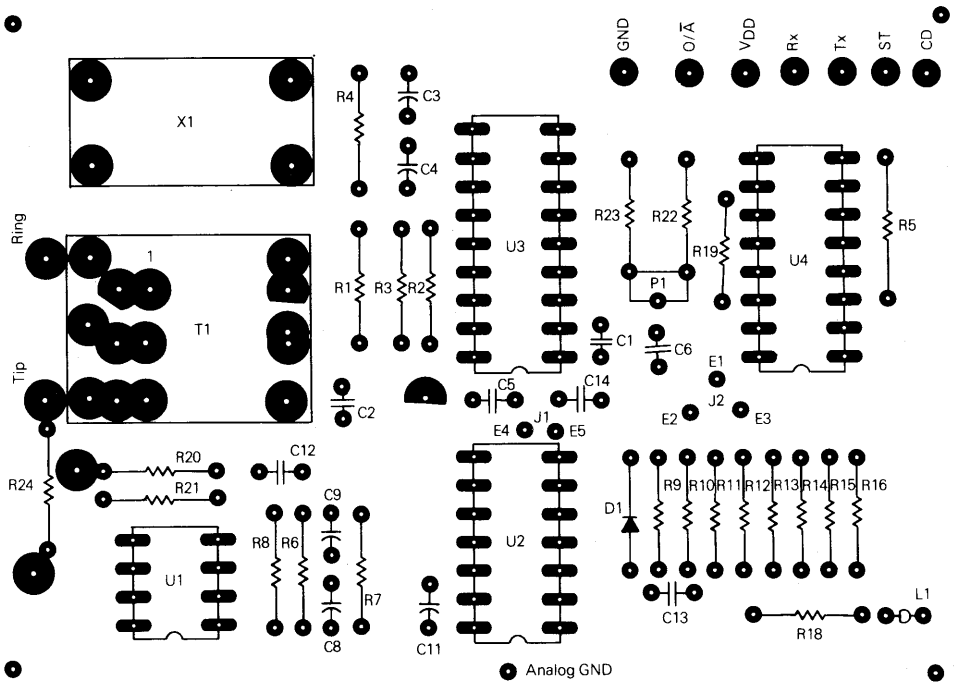
NOTES:
1. Optional Pot P1 in lieu of R22 and R23.
2. Optional U1 with R20 and R21 to get additional 6 dB gain, for more receive sensitivity.
3. If U1 is not used, jumper R20 and R21.

FIGURE 8 — Modem 1 Board MC145440/MC14412

R1 – 332
R2 – 10 k
R3 – 24 k
R4 – 10 M
R5 – 10 k
R6 – 3 k
R7 – 20 k
R8 – 10 k
R9 – 1.6 M
R10 – 2 k
R11 – 750 k
R12 – 2 k
R13 – 2 k
R14 – 200 k
R15 – 33 k
R16 – 560
R17 – N/A
R18 – 300
R19 – 10 k
R20 – 10 k
R21 – 20 k
R22 –
R23 –
R24 – 10

C1 – 0.1
C2 – 0.068
C3 – 20 pF
C4 – 20 pF
C5 – 0.1
C6 – 0.1
C7 – N/A
C8 – 0.01
C9 – 1 μF
C10 – N/A
C11 – 0.1
C12 – 0.1
C13 – 0.1
C14 – 0.1

U1 – MC4558P1
U2 – LM339A
U3 – MC145440P
U4 – MC14412FP
X1 – 4 MHz Crystal
P1 – 10 kΩ Pot
D1 – IN914
L1 – LED
T1 – Midcom 671-0915



NOTE:
1. Use P1 or resistors R23 and R22 to set output signal level.
2. Jumper J1 connects internal voltage reforance to analog ground.
3. Jumper J2 – for MC145440 Bell 103 connect E1 to E3
   for MC145441 CCITT V.23 connect E1 to E2

FIGURE 9 – Modem 1 Board MC145440/MC14412

2400 BPS DPSK MODEM SYSTEM USING THE MC6172/6173

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MOS Telecommunications Applications

INTRODUCTION

The tremendous growth in data communications has spurred the development of many diverse modems for use on the normal dial-up telephone network and on private leased lines. One of the more prominent ones is the type 201, 2400 bps (bits per second) system such as the Bell 201B/C data set or the system described in CCITT specification V.26/V.26 bis. This type of modem uses a technique of modulation called differential phase-shift keying (DPSK) in which a carrier frequency is phase modulated to represent different information states. The Motorola MC6172/6173 chip set is an NMOS LSI subsystem designed to perform the modulate/demodulate and control functions for implementing a DPSK modem. Pin-selectable options permit compliance with either U.S. (Bell) or European (CCITT) requirements and also allow selection of the standard data rate of 2400 bps or a secondary rate of 1200 bps. By using the MC6172/6173 chip set as a core, a complete modem system can be easily built that offers high performance at a surprisingly reasonable cost.

BACKGROUND

As mentioned, DPSK employs periodic phase shifting to transmit information through a communication medium. The primary advantage of this method of modulation is its efficient use of the narrow bandwidth of a telephone channel (typically 300-3000 Hz). This efficiency comes about through the use of multiple phase states which allow higher data rates within the same channel bandwidth. As a specific example, let us consider how DPSK is done in the MC6172/6173 system. The basic signal spectra for MC6172 modulator is from 600 to 3,000 Hz because it modulates an 1800 Hz carrier at a 1200 Hz rate ($f_{carrier} \pm f_{mod}$). In the 1200 bps mode, only two phase-shift states are used to encode each bit of data per baud transition (The baud rate is the actual signaling rate of the carrier). By using four phase states, two bits of data can be encoded at each baud transition which results in twice the data rate within the same channel bandwidth. Each two bits of data in the 2400 bps mode is called a *dibit* and the time that modulation begins to encode each new dibit is called dibit clock. The coding scheme of the U.S. and European options for 1200/2400 bps is as follows:

1200 bps

	Option C	Option D
Data	CCITT	U.S.
0	+90°	+45°
1	+270°	+225°

2400 bps

Dibit Data	Option A CCITT	Option B U.S.
00	0°	+45°
01	+90°	+135°
11	+180°	+225°
10	+270°	+315°

The term "differential" in DPSK refers to the fact that each time a phase shift occurs, it is in reference to the previous phase. This process is shown in Figure 1. Differential modulation eliminates the need for a synchronized reference at the transmitter and receiver. In our system, the MC6173 demodulator derives its timing synchronization from the incoming signal, although it does require an external clock for internal sequencing and to provide a reference input to the internal phase-locked loop (PLL) used to derive the carrier frequency and the 1200 Hz modulation component (dibit clock).

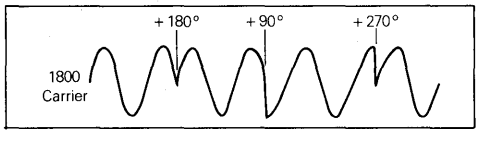


FIGURE 1—DPSK Format

Detection of DPSK signals occurs in one of two ways: differential coherent or differential comparative. Differential *coherent* uses a local noise-free reference in phase lock with the incoming signal for demodulation. This is the method used in the MC6173. Differential *comparative* delays the in-

coming signal one symbol transition time (or baud time) and compares this information with the next symbol change. Although differential coherent detection is more complex, it offers a significant signal-to-noise-ratio improvement of 2.3 dB over comparative detection for a 4-phase system in the presence of white noise.

To allow for detection of the 1200 Hz modulation component or dibit clock, an AM envelope is superimposed upon the output signal of the MC6172 modulator. This envelope also serves to define the waveform shape during the transition from one phase to another which occurs at the positive-going edge of dibit clock. As shown in Figure 2, the AM envelope of bordering dibit intervals are summed together to provide a smoother waveform with less spectral content than one with instantaneous phase shifts. The demodulator system uses a full-wave rectifier and a narrow band-pass filter to recover this envelope information for internal synchronization.

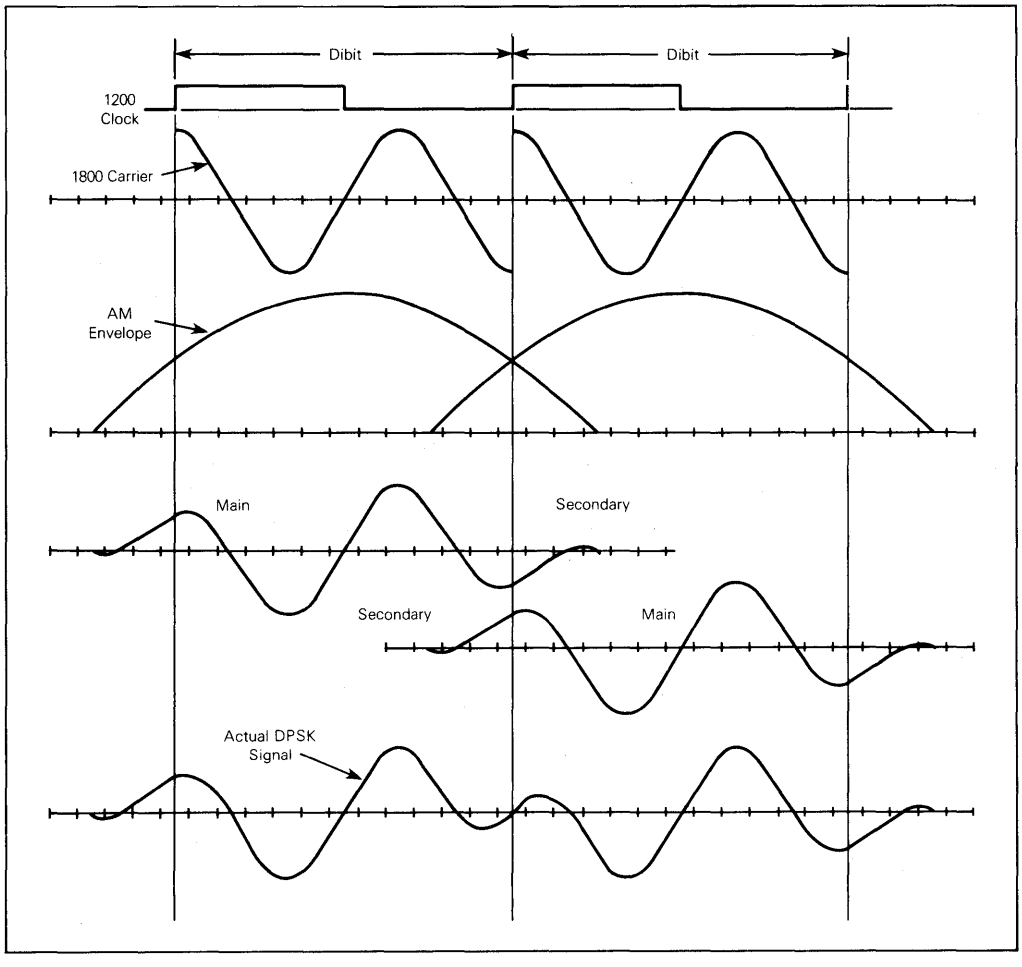


FIGURE 2—DPSK Waveforms

THE REAL WORLD

After the MC6172 modulator has received the input serial data, grouped it into dibits (2400 bps operation), and modulated the 1800 Hz carrier accordingly, the output DPSK signal is thrust into the real world of the switched telephone network. This environment typically contains such line impairments as noise, phase jitter, crosstalk, frequency translation and high voltage spikes. Of these, noise and phase jitter are the most important to consider in a DPSK system like the MC6172/6173. General background noise is usually treated statistically as a guassian distribution. In subsequent performance tests, the noise mentioned will be of the white guassian type. Phase jitter is a measure of the phase modulation the communication environment is imposing upon the line signal and is usually measured in degrees peak-to-peak at some frequency of modulation (°p-p/Hz).

To overcome some of the impairments in the normal dial-up telephone network, Bell and others can offer the modem user a variety of private leased lines which do not pass through any switching apparatus. These lines typically have special conditioning for higher quality transmission. A very popular choice is the 3002 voice-grade line which comes in five different levels of quality; C1, C2, C4, C5 and the basic unconditioned line. It is characterized by a higher SNR, flatter amplitude response, better phase linearity and less transient interference than dial-up lines. With appropriate equalization as will be described later, the MC6172/6173 modem can be used on any of the 3002 lines in addition to its dial-up line capability.

SYSTEM OVERVIEW

A block diagram of the MC6172/6173 modem system is shown in Figure 3. Serial data is output from the business machine or DTE (Data Terminal Equipment) as it is usually referred to, and transferred to the MC6172 modulator via an RS-232C interface (optional). Under the control of the DTE, the modulator produces a DPSK signal which is in the form of 6-bit digital words. The D/A converter then constructs a PAM waveform from the digital words. A low-pass filter limits the output frequency spectrum before transmission to the line. After propagating through the communication medium, the signal appears at the input to the demodulator system containing the MC6173 demodulator. The signal is then amplified, filtered by a band-pass filter and phase equalized. (The need for equalization would depend upon the quality of the line.) At this point, the signal splits into two paths: one through an automatic gain control (AGC) circuit and the other through the carrier detect circuit which merely indicates to the demodulator that sufficient signal energy is on the line. The AGC stabilizes the level of the signal before feeding the 1200 Hz envelope filter and the A/D converter. The 1200 Hz filter recovers the dibit clock from signal for synchronization with the internal dibit clock of the MC6173. The A/D converter uses successive approximation to transform the analog signal into a digital bit stream that is input to the demodulator. The MC6173 decodes the digital DPSK data into the original data which is then transmitted through another RS-232C interface to the receiving DTE.

The system as shown in the block diagram is only in a *simplex* mode of operation in which data flows in only one direction all the time. For *half-duplex* operation, where data flows bidirectionally but not simultaneously, a MC6172 and MC6173 would be needed at both ends of a 2-wire connection. In order to realize *full-duplex* operation where data flows bidirectionally and simultaneously, a 4-wire connection would be required.

Modulator System Design

The modulator design procedure is relatively straightforward and does not affect overall modem performance a great deal. The complete circuit schematic for the modulator system is shown in Figure 4. A thorough pinout description of the MC6172 will not be presented here; therefore the

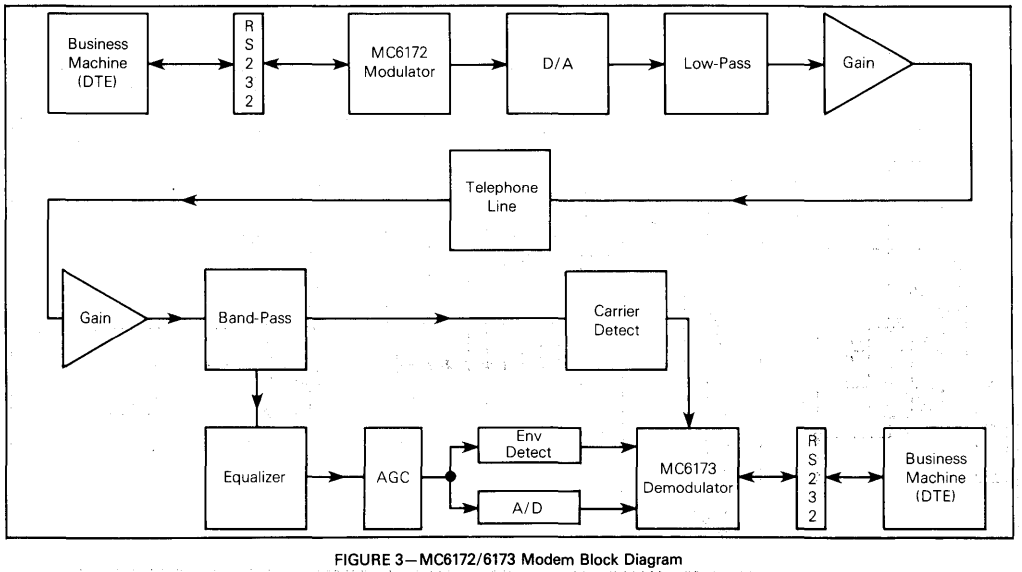


FIGURE 3—MC6172/6173 Modem Block Diagram

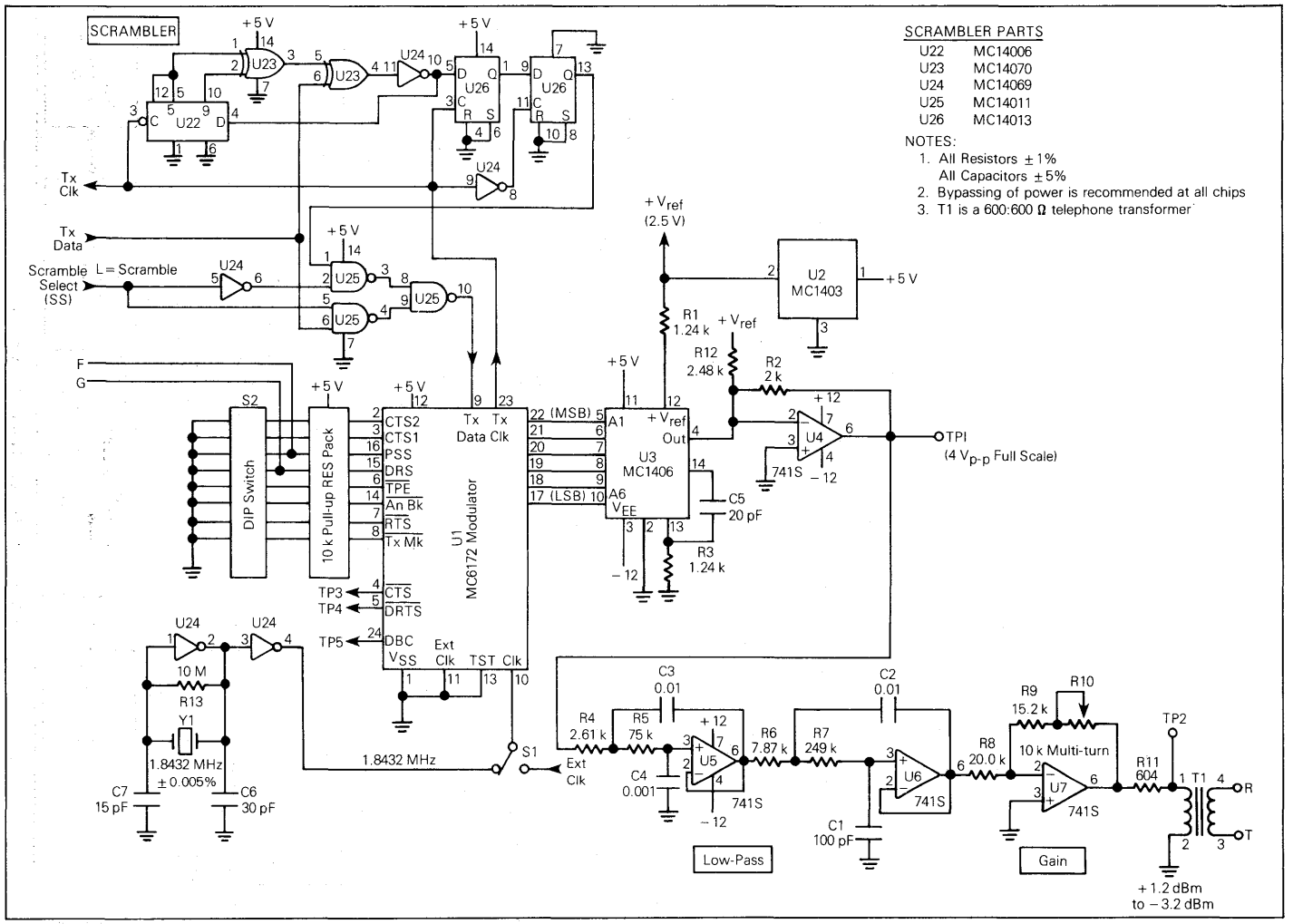


FIGURE 4 — 2400 BPS DPSK Modulator System

reader should consult both a MC6172 and MC6173 data sheet for full details. The clock source for the MC6172 is a simple CMOS inverter oscillator using a 1.8432 MHz ± 0.005% crystal as a time base. The MC6172 uses this reference frequency to derive the 1200/2400 Hz transmit clock, the 1800 Hz carrier and the dibit clock. The External Clock input (pin 11) can be used to supply the modulator with an external transmit data clock.

Control of the modulator by the DTE is established through the RS-232C interface and consists of these signals: $\overline{CTS}$, $\overline{RTS}$, Tx Data and Tx Clk. Tx Data is the input line for the serial digital data and Tx Clk is the clock provided by the modulator for clocking in the data. $\overline{RTS}$ stands for Request-To-Send and essentially is the output enable of the modulator. A high-to-low transition on $\overline{RTS}$ initiates a training sequence of constant marks (a mark is a logic one; a space is a logic zero) to be sent for a duration determined by $\overline{RTS}$-to-$\overline{CTS}$ delay selected by CTS1 and CTS2 (pins 3 and 2, respectively). When this delay has timed out, the $\overline{CTS}$ (Clear-To-Send) function, pin 4, falls low indicating to the DTE that normal data transmission can now begin. To terminate transmission, the DTE would take $\overline{RTS}$ high. A secondary output, $\overline{DRTS}$ (Delayed-Request-To-Send, pin 5) indicates the exact time the modulator actually ceases transmission. The small delay from the rising edge of $\overline{RTS}$ and the rising edge of $\overline{DRTS}$ is required to allow the residual data in the MC6172 to be sent after $\overline{RTS}$ goes high. An important note is that signals from RS-232C are inverted from the true logic of the MC6172; consequently, a mark to the interface is the most negative voltage level while in the MC6172 it is the most positive logic level. The Motorola MC1488/89 RS-232C interface chips provide the necessary inversion and logic shifting for compatibility between RS-232C and the MC6172/6173 modem system.

DPSK data is presented at U3, an MC1406 D/A converter, in the form of a 6-bit digital word. A reference current is supplied by an MC1403 +2.5 V_{ref} through R1. This current (about 2 mA) flows into pin 12 of the 1406 and is used as a reference to supply an output current at pin 4 proportional to the input digital word (pins 5 through 10). U4 is a simple current-to-voltage converter which establishes 4 volt peak-to-peak signal at TP1. Because the signal at TP1 is a PAM waveform with excessive high-frequency content, a low-pass filter is required. A fourth-order 0.01 dB ripple Chebyshev was chosen and its design equations are given in Appendix I. This filter provides excellent amplitude response and has a small envelope delay distortion (EDD) of 61 μs (referenced to delay at 1800 Hz). The output of the filter, pin 6 of U6, passes through an adjustable gain buffer (U7) that establishes a signal level range of +1 to −3 dBm/600 ohms at TP2.

Before actually connecting the output of the modem to a dial-up switched telephone line, Bell requires that a DAA or Data Access Arrangement be placed in series between the modem and the line. The purpose of the DAA is to protect the line from faulty operation of the modem, such as improper ground isolation or excessive power transmission. A DAA can be leased from various suppliers or can be built by the user and then certified by FCC under specification Part 68.

DEMODULATOR SYSTEM DESIGN

The demodulator system is shown in Figure 5. The signal voltage occurs across Tip (T) and Ring (R) of transformer T2. The signal is then amplified by 8 dB via U9 and then fed into the receive band-pass filter (400-3600 Hz pass-band). This filter is constructed by cascading a 2nd-order Chebyshev high-pass with the 4th-order low-pass used in the modulator system. The design equations for the high-pass are also given in Appendix I.

After filtering, the signal can be equalized if required to minimize the EDD of a typical 3002 voice-grade line. The EDD is usually worst about the channel band edges because that is where band-pass poles begin to accumulate phase. The schematic for the equalizer and its EDD response is shown in Figures 6 and 7, respectively.

The conditioned DPSK signal is then output at TP7. From there it goes to the carrier detect circuit and the AGC. The carrier detect consists of a 20 dB gain stage (U9D) and a comparator formed by U18 and U19 (MLM311) that will provide at least 3 dB of hysteresis. As shown, the circuit will turn on with an input level of −43 dBm or greater and will stay on until the signal falls to −48 dBm. These trip points can be adjusted by changing the divider network of R43-R45. The output of the carrier detect circuit is at U34 pin 6 which is connected to $\overline{FCar}$ (pin 2) of the MC6173. A negative transition at this point indicates to the demodulator that sufficient signal energy has been detected. If there is noise greater than −43 dBm on the line, then the trip points must be raised to prevent false triggering. The AGC consists chiefly of a Signectics NE571 compandor chip. This is a bipolar device that combines an integrated rectifier and variable gain amplifier in one package. The signal at TP7 is ac coupled into pins 2 and 6 of the NE571, the rectifier and signal inputs, respectively. C6 is the rectifier capacitor used to filter the signal at pin 2 and it directly affects the time constant of the circuit. After rectification and filtering, a dc level is obtained to control the gain of the signal at pin 6. The output of the AGC is taken from pin 7 of the NE571 and ac coupled to TP9. As shown, the AGC will maintain an output level at TP9 of 0 dBm ± 1.5 dB from −48 to 0 dBm at the input to the demodulator system (pins 1 and 2 of T2).

The signal at TP9 is routed to the 1200 Hz envelope detect circuit and the A/D converter. The envelope detect consists of a precision full-wave rectifier and a 1200 Hz band-pass filter. The output of the band-pass is ac coupled into U13, which is a comparator used to square the waveform before going into the Env input (pin 10) of the MC6173. The envelope signal is essentially the dibit clock of the incoming signal and is used by the MC6173 for synchronization with its internal dibit clock during the initial training sequence of all marks.

The A/D subsystem consists of an LF398 sample-and-hold chip (U12), an MC14559 successive approximation register (U17), an MC1408 D/A (U16), a current-to-voltage converter (U21) and a comparator (U14). Operation of this circuit is initiated by a negative transition of U12 for it to "hold" a voltage sample of the signal at TP9. U17 begins to construct a digital word by setting successive bits and comparing the subsequent output voltage at U21 pin 6 with the held voltage sample at U12 pin 5. If the voltage sample is less than the output voltage of the D/A, then that particular bit of U17 is set; otherwise it is reset low. This process continues at a 460 kHz rate until a 7-bit word has been constructed and shipped serially to the MC6173 from U17 pin 5. The clocking for the A/D is provided by the MC6173 through the ADS and ADC outputs (pins 8 and 6).

To summarize the operation of the demodulator system, assume that there is no data being sent by the modulator and the demodulator is in an idle condition. $\overline{FCar}$ is then at a high state which has effectively disabled the MC6173. The modulator initiates transmission at some point which, for the

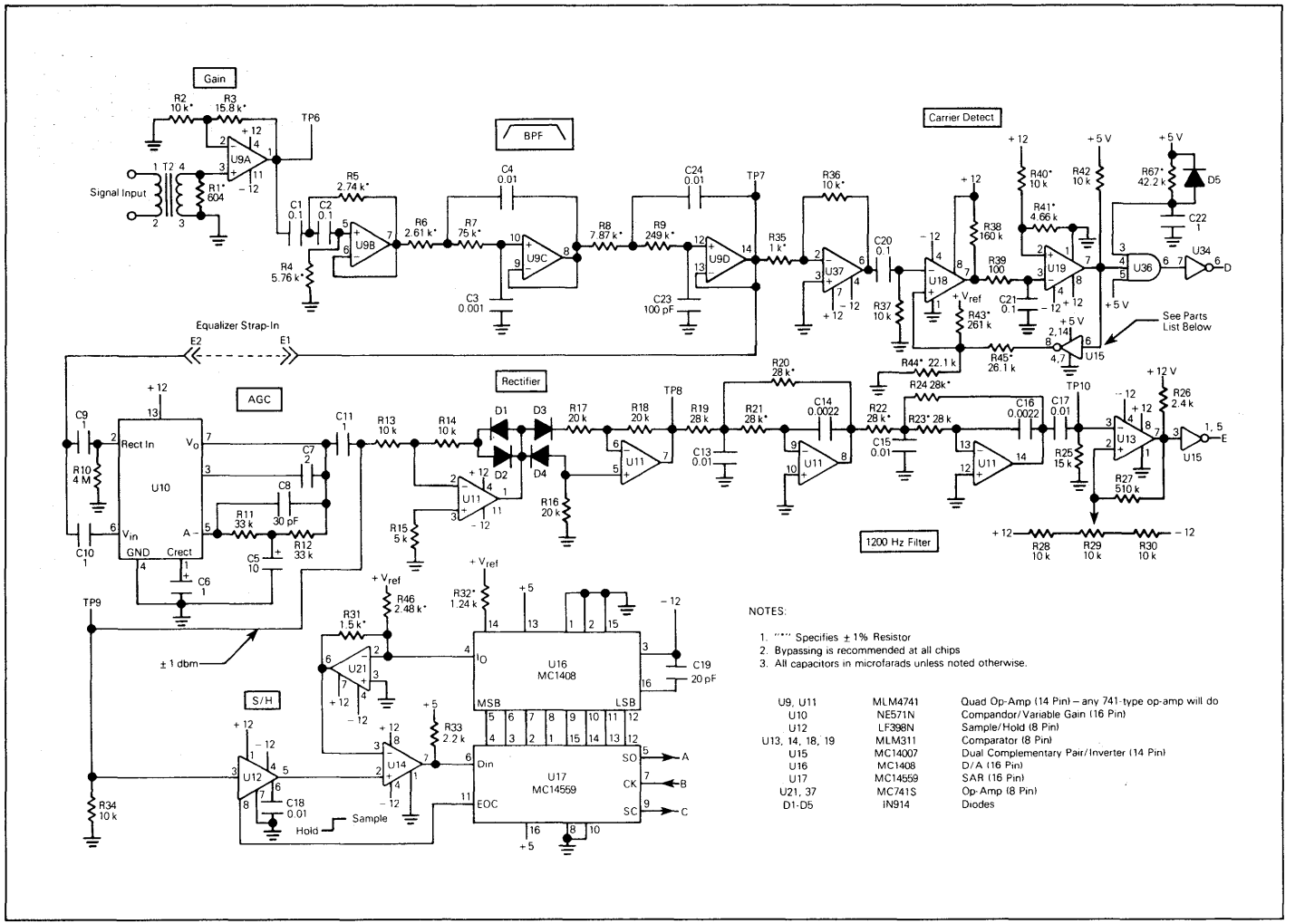


FIGURE 5 — 2400 BPS DPSK Demodulator (1 of 2)

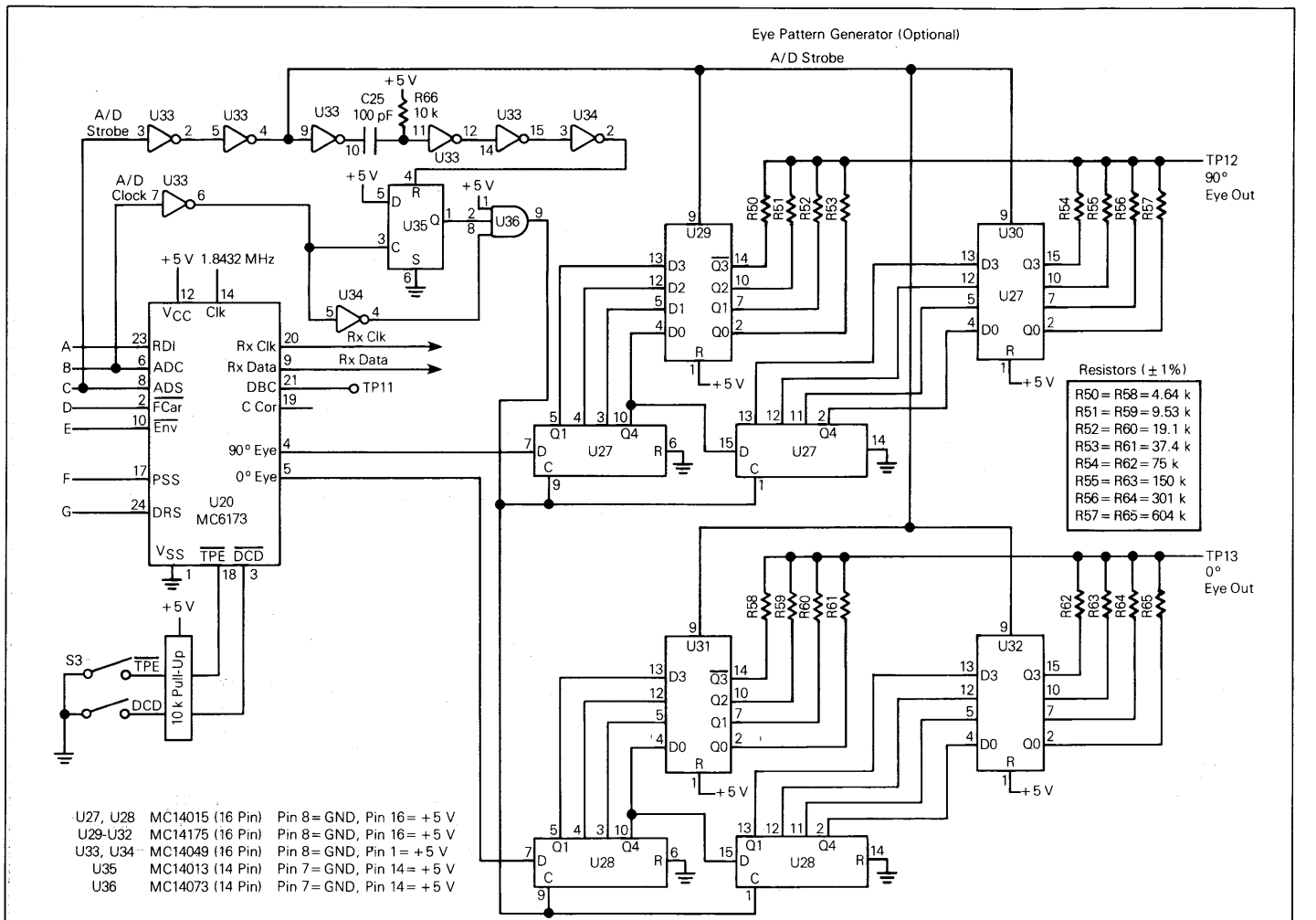


FIGURE 5 — 2400 BPS DPSK Demodulator System (2 of 2)

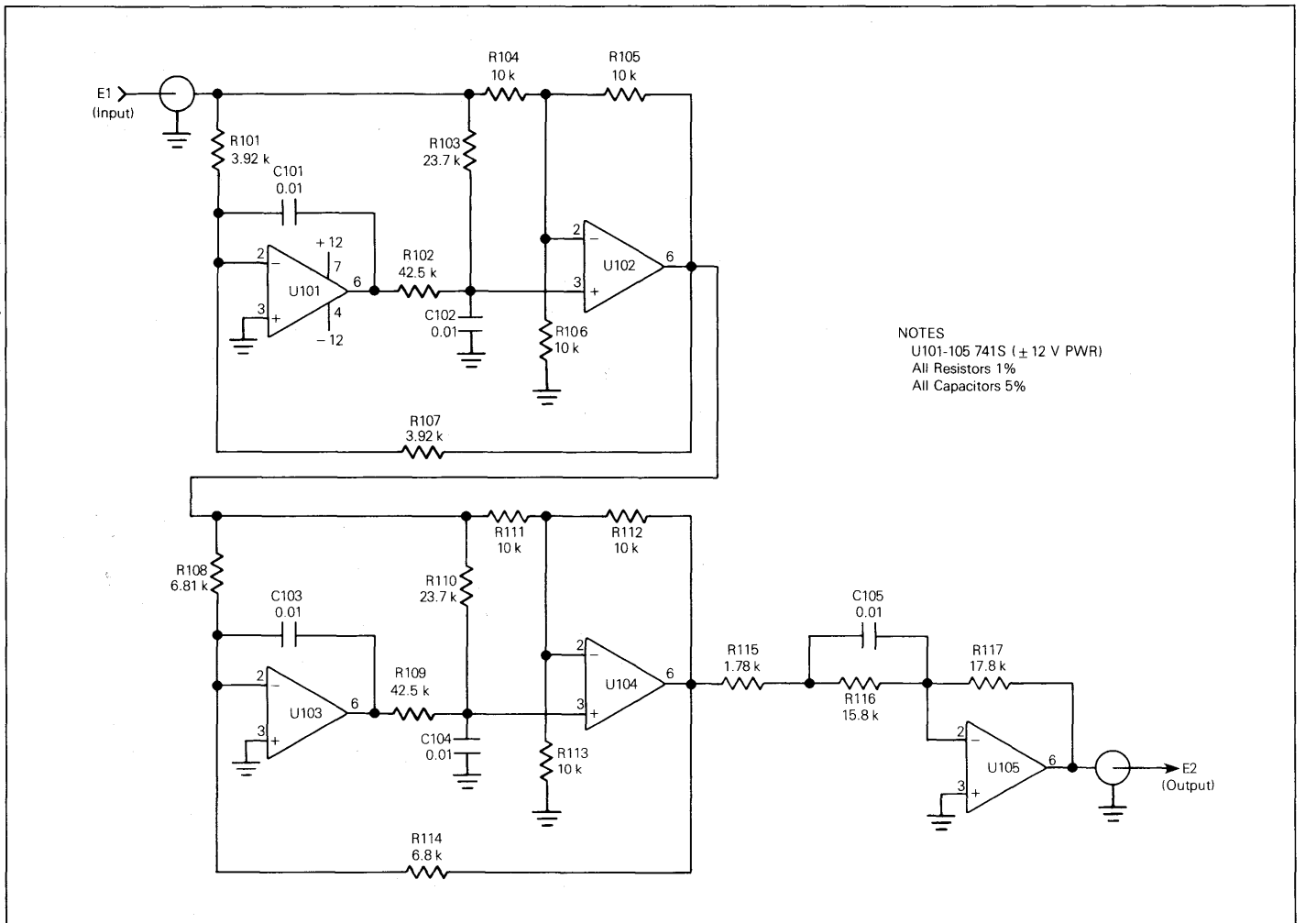


FIGURE 6 — 2400 BPS Modem System Equalizer Sub-Board

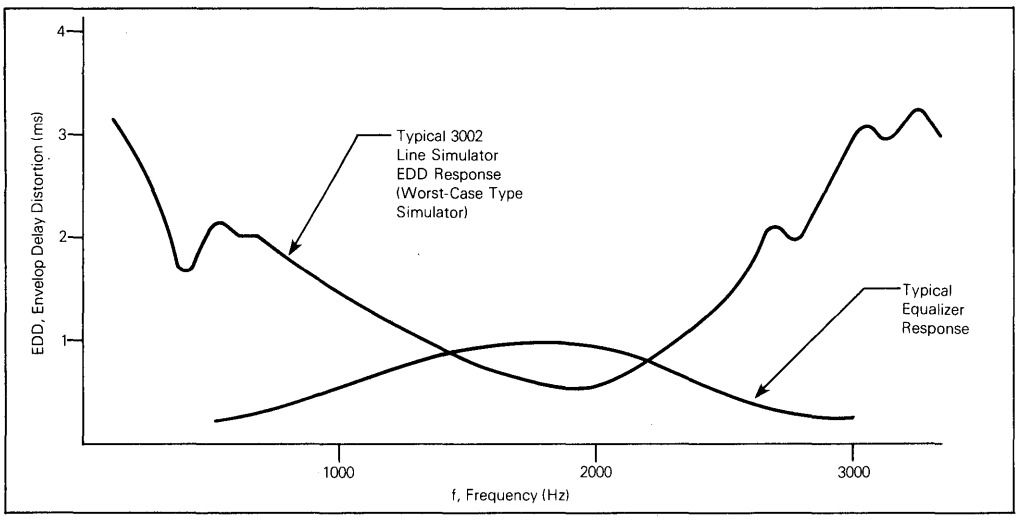


FIGURE 7 – EDD Response

specified training period, consists of all marks. The carrier detect circuit is turned on, taking $\overline{FCar}$ low and enabling the MC6173 to widen its PLL to lock onto the incoming signal. The envelope detect presents the recovered dibit clock at Env for internal synchronization during this time. After the training period times out, normal data transmission occurs and the Env input is ignored. All subsequent timing for this data message is derived directly from the DPSK signal. To lengthen the training period at the MC6173 in which envelope information is taken from Env, the Cars input (pin 15) should be taken low for the amount of the extended period.

Scrambler

A scrambler circuit is shown in the upper-left corner of Figure 4. This circuit will scramble the serial data with a 511-bit psuedo-random pattern as called for in specification V.52. The scrambling of data is done in an attempt to minimize demodulator sensitivity to long strings of spaces. When the scrambler is enabled (Scramble Select = 0), the Test Pattern Enable pin (TPE) should be left high. The MC6173 demodulator has a built-in descrambler that is enabled by taking its TPE input (pin 18) low.

Eye Pattern Generator

The MC6173 demodulator has the capability of producing an "eye" pattern through the use of the 90° Eye and 0° Eye outputs (pins 4 and 5). An eye pattern is a graphic indication of the incoming signal quality. The circuit for generating an oscilloscope picture from the 90° and 0° Eye pins is shown, surrounding the MC6173, in the second page of Figure 5. U27 and U28 are serial-to-parallel data registers that allow the eye information to be clocked out. The A/D Strobe output of the MC6173 is used to clock out the eye information to a resistor-scaling network that produces an equivalent discrete voltage level. As more data is clocked out, a PAM staircase waveform is constructed which illustrates the 0° and 90° carrier shifts. To see the waveform on an oscilloscope, attach probes from two channels to TP12 and TP13 and overlap the patterns on the scope while triggering on Dibit Clock (pin 21). The round spaces in the pattern are the eyes and if they are clearly defined the signal quality is high. As more noise and jitter perturb the signal, the eyes tend to become fuzzy and close up. Pictures of actual eye patterns for both phase options are shown in Figure 8.

PERFORMANCE TESTS

Performance data on modems is usually a nebulous area of comparison. One modem manufacturer may specify his modem using C-message weighted noise while another may use 3 kHz-flat weighting. Test equipment will vary and line simulators will have different characteristics. To validly compare modems, one must use the same equipment setup and test procedure. In the following tests, the equipment and procedure will be clearly stated.

The equipment setup is shown in Figure 9. The Bradley 2A/2B disturbence generator is designed to simulate such line perturbations such as phase jitter, frequency translation, AM interference and white noise. The Comstrom-S.E.G. FA-1445 simulates a worst-case 3002 unconditioned line. The HP 3551 is an ac voltmeter that can measure noise using different weighting schemes. In all cases, noise measurements were made using the *3 kHz-flat* filter while modem signals were measured in the Receive Tone mode (0-60 kHz bandwidth). The HP 1645A data error analyzer provided the serial test data and bit error rate (BER) figures. In all cases, the data pattern was the 511-bit psuedo-random sequence.

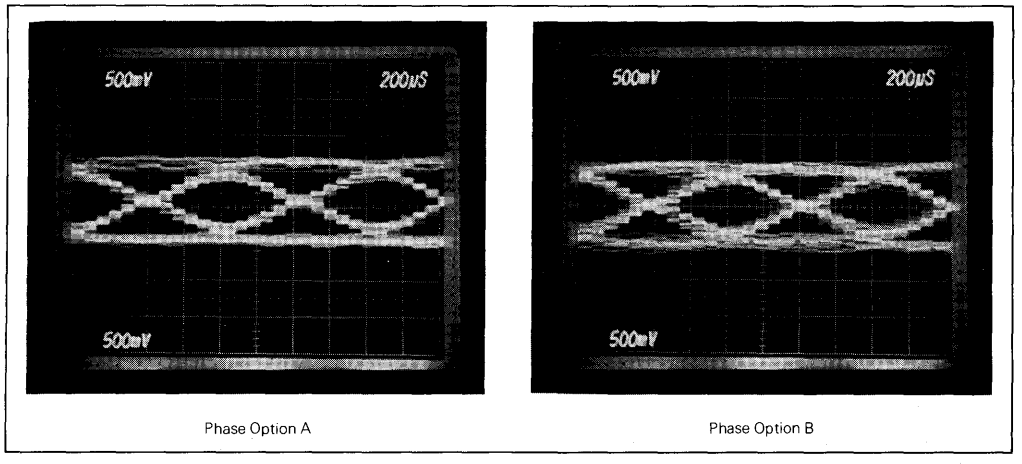
The performance tests, shown in Figures 10 through 13 are:

Figure 10—This is a test of back-to-back performance with white noise and phase jitter added for phase option B. Degradation in SNR is about 2.1 dB at 1×10^{-4} bit error rate.

Figure 11—Same test as in Figure 10 with option A selected.

Figure 12—Frequency translation effect on option B performance.

Figure 13—Performance when an S.E.G. 3002 Line Simulator is placed in the signal path. The equalizer used is the one described in Figure 6. The curve shows the worst-case performance that can occur with a worst-case 3002 line and the equalizer strapped in. On a typical 3002 line, the equalizer will improve performance considerably.



Phase Option A

Phase Option B

FIGURE 8 — Eye Patterns

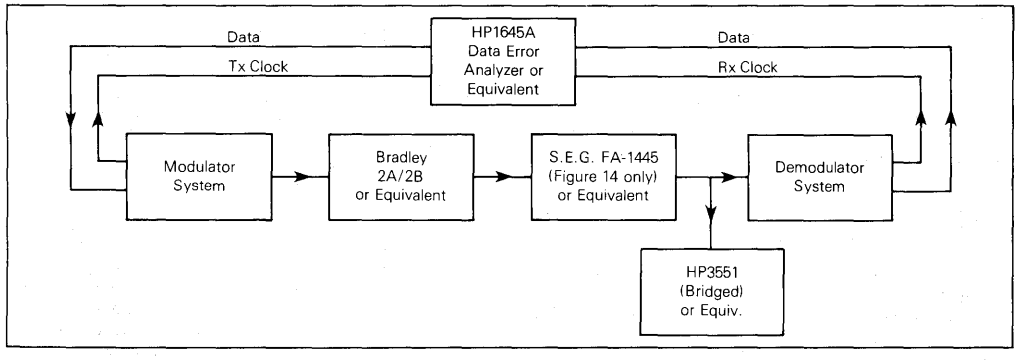


FIGURE 9 — Equipment Setup

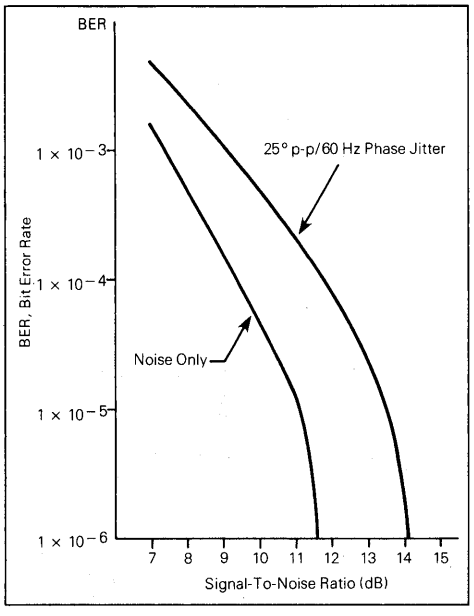


FIGURE 10 — B Mod 2400 BPS Back-To-Back 511 Test Pattern

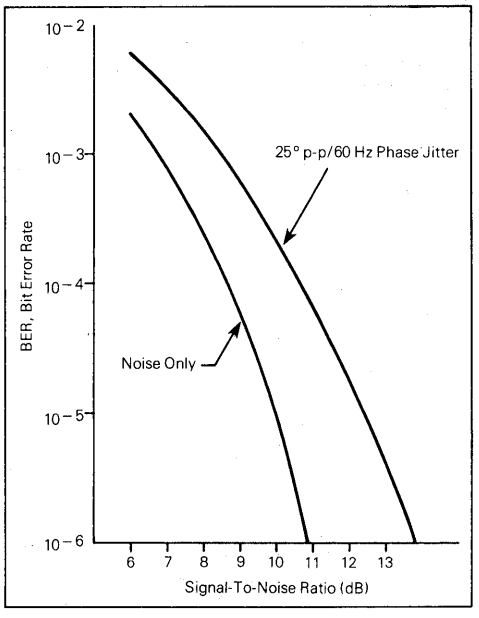


FIGURE 11 — A Mod 2400 BPS Back-To-Back 511 Test Pattern

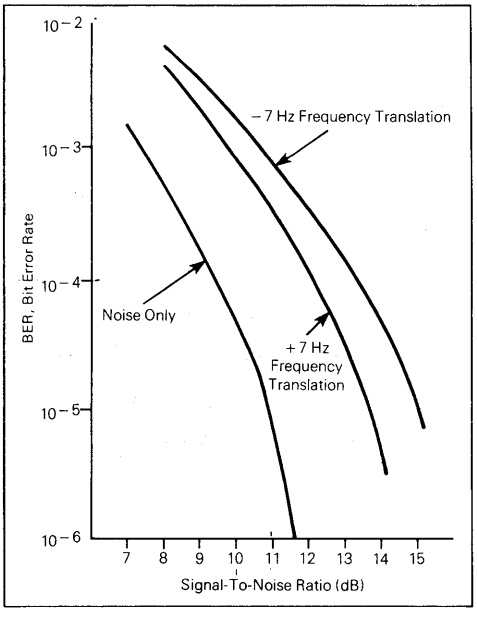


FIGURE 12 — B Mod 2400 BPS Frequency Translation 511 Test Pattern

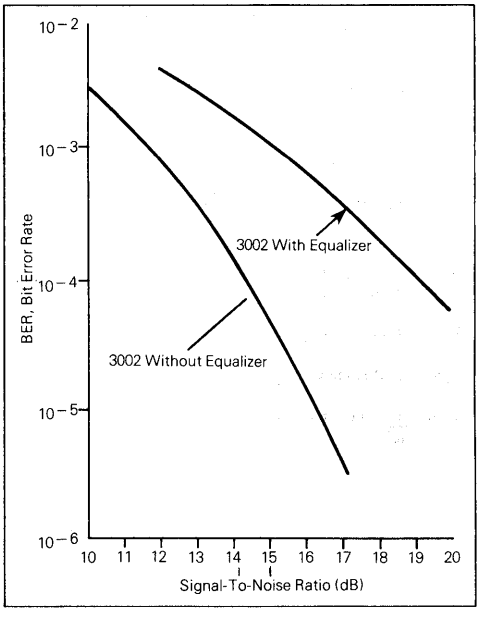


FIGURE 13 — B Mod 2400 BPS 3002 Simulator 511 Test Pattern

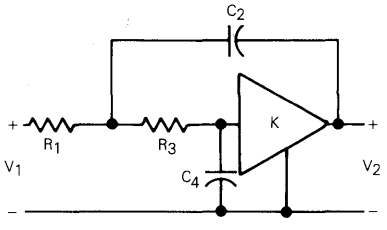
CONCLUSIONS

The MC6172/6173 modem system has been shown to be very effective over differing line conditions. The general design procedure for implementing this system has been presented so that easy modification is possible. The ability of the MC6172/6173 modem to operate synchronously over the dial-up telephone network without complex automatic equalization offers the user an attractive choice for medium-speed data links.

APPENDIX I

4th-Order Chebyshev Low-Pass Filter Design

This filter was realized by cascading two second-order Salen and Key filter sections. The design equations were taken from *INTRODUCTION TO THE THEORY AND DESIGN OF ACTIVE FILTERS* by Huelsman and Allen, pages 157-158. The general circuit realization for a Salen and Key is shown below.



Specifications:

Pass-band ripple = 0.01 dB f_c = 3600 Hz
Op-amp gain = K = 1

Pole Locations (normalized):

a	b	
−0.6762	± j.3828	first stage
−0.2801	± j.9241	second stage

$$Q = \text{Quality Factor} = \frac{(a^2 + b^2)^{1/2}}{2a}$$

where a = real pole coordinate
b = imaginary pole coordinate

Q_1 = first stage $Q = \underline{0.5746}$

Q_2 = second stage $Q = \underline{1.7237}$

Let $n = \frac{R3}{R1}$ and $m = \frac{C4}{C2}$

For this design procedure it is necessary that $m \leq \frac{1.}{4Q^2}$

Therefore $m_1 \leq \frac{1}{4(0.5746)^2} = 0.7573$ Choose m = 0.1

$$n = \frac{1}{2mQ^2} - 1 \pm \frac{(1 - 4mQ^2)^{1/2}}{2mQ^2}$$

either value obtained is valid

n = 28.25675 for first stage

$$R1C2 = \frac{1}{2(pi)(f_c)(mn)^{1/2}} = 2.63 \times 10^{-5}$$

Let C2 = 0.01 μF

Then R1 = 2.63 kΩ----------> 2.61 kΩ
R3 = nR1 = 74.315 kΩ----> 75 kΩ
C4 = mC2 = 0.001 μF

The second stage was designed using the same equations and resulted in the following values for Q_2 = 1.7237 and f_c = 3600:

C2 = 0.01 μF
C4 = 100 pF

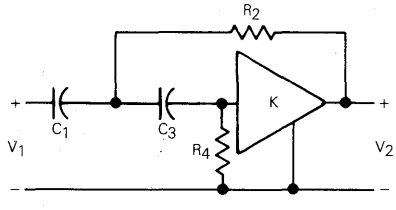
R1 = 7.87 kΩ
R3 = 249 kΩ

2nd-Order Chebyshev High-Pass Filter

Specifications:

Pass-band ripple = 0.01 dB f_c = 400 Hz
Op-amp gain = K = 1

The general Salen and Key high-pass realization is shown below:



Pole Locations (normalized low-pass values) =

$$\frac{a}{-0.6743} \pm \frac{b}{j.7075}$$

To transform the low-pass poles into high-pass poles,

$$a_{HP} = \frac{a}{a^2+b^2} = -0.7059 \qquad b_{HP} = \frac{b}{a^2+b^2} = 0.740654$$

$Q = 0.7247$ $\qquad \frac{1}{Q} = \frac{m+1}{(mn)^{1/2}}$ from page 165.

For minimum Q, m should equal 1 which reduces the above equation to:

$$Q = \frac{(n)^{1/2}}{2} \quad \text{or} \quad n = 4Q^2 = 2.101$$

$$R2C1 = \frac{1}{2(pi)(f_C)(n)^{1/2}} = 2.745 \times 10^{-4}$$

Letting C1 = C2 = 0.1 μF, we obtain

R2 = 2.745 kΩ-----> 2.74 kΩ
R4 = 5.767 kΩ-----> 5.76 kΩ

A FOUR-WIRE FULL DUPLEX 1200 BAUD MODEM IMPLEMENTATION USING THE MC145450 AND THE MC145415

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THE APPLICATION

The 1200 baud four-wire modem is intended for dedicated-wire type applications where there is a need for reliable and economical data transmission. This very design may be used as a basis for a Bell 202T modem where four dedicated wires are available from the phone company for long distance communications. Another possible use for this design is for transmitting data between computers or between a computer and a terminal where the distances exceed the ability of normal transmission methods. This is a very common problem when one computer is required to serve users at a site where an RS-232 link can only work locally (such as 200 feet from the computer), and some of the users may be as far away as a mile or more from the computer. Applications where data is transferred, but recovery of pure digital signals is impossible due to line conditions, is a possible candidate for the 1200 baud 4-wire modem link.

THE SYSTEM

The application circuit is comprised of six major functions which are delineated by the dashed lines in Figure 1. The 3.6864 MHz oscillator provides the master clock used throughout the complete modem circuit. The 153.6 kHz clock generator derives the 153.6 kHz clock, which is used by the filter, from the oscillator output. The filter provides all transmit and receive filtering to provide the optimum signal-to-noise ratio for the best possible performance. The limiter takes the received signal and squares it up into a digital signal. This is necessary for the mod/demod as it is a digital circuit that provides the actual conversion between tones and data.

The heart of the system is the MC145450 modem chip. This chip is capable of modulating and demodulating data at rates of up to 1800 bits per second. A detailed description of this part, as well as all the other parts, exists in the corresponding data sheet. Since no real features of the MC145450 are used in this design, only two inputs and two outputs are needed. The transmit input receives digital data to be modulated and the receive output is the digital representation of the demodulated data. The transmit carrier output is typically 490 mV peak-to-peak, and the filter gain is 18 dB, causing the output of the filter to clip, so a voltage divider is used to control the level of the modulated signal going to the filter. The receive carrier input expects a squared-up or digital representation of the receive modulated data. This is provided by the limiter.

The limiter section is based on the LM339A comparator. This particular device was selected for its low offset. The offset determines the minimum signal level detected, so a large offset will limit the modem's sensitivity. Two passive filters are used to remove low frequency signals such as 60 Hz noise and high frequency signals such as the 153.6 kHz clock ripple on the filter output. This ripple is characteristic of switched-capacitor filters that do not have on-board real-time smoothing filters. The extra three devices on the LM339A chip can be used in the optional carrier detect circuit shown in Figure 2. The limiter components should be located as close together as possible to help promote circuit stability.

The filter section utilizes the MC145415 switched-capacitor filter. This is actually a pair of low-pass filters based on a Bessel representation. The "A" filter has an in-band gain of 18 dB and the "B" filter has a 0 dB gain. In this design the "A" filter is used as the transmit filter. This would be the best choice when there is no specified maximum output level such as in non-telecom short haul modem designs. In this case the signal-to-noise ratio is optimized at the receiver. If the application had a level limitation of −12 dBm or less, the "B" filter should be used as the transmit filter so the "A" filter's gain can be used to extend the floor of the dynamic range. The 2.2 kilohm resistor network is used to provide a mid-supply reference for the analog circuitry. If the mid-supply level is not held fairly close to $V_{CC}/2$, then the headroom for large signals will be impacted with the signals clipping at the nearest rail. The filter requires a 153.6 kHz clock to guarantee a 2.4 kHz break frequency.

The clock generator circuit used to derive the filter clock is a very straightforward design. The 3.6864 MHz master clock is divided by 12 with U3. The resulting output is halved by U5 to give the 153.6 kHz signal. There is an added bonus in this direct divide down in that the filter's sample rate will be synchronous with the modem switching rate causing aliasing to be mimimized.

The master oscillator is a simple CMOS inverter design. The oscillator on U1 would suffice, but since there are already some spare inverters available, a buffered oscillator is created by adding 2 inexpensive capacitors. This is much more capable in terms of drive characteristics.

The line interface is set up for a 600 ohm balanced line. By exchanging the resistors, the lines can be used at other impedances, however, if the resistors are less than 300 ohms, the filter may have problems driving the line. The interface may also be redesigned with a duplexer to provide the basis for a two-wire system such as a Bell 202S modem.

ALTERNATE CLOCK CIRCUITS

The clock circuit made up of the 3.6864 MHz oscillator and the 153.6 kHz clock generator may be reconfigured into a number of different designs. Two other possible configurations are shown in Figure 3. The main criteria in all cases is that a 3.6864 MHz square wave is available to drive the MC145450 and a 153.6 kHz square wave is available to drive the MC145415. Since the 153.6 kHz is 3.6864 MHz divided by 24, the basic generator need only be a divide-by-24. The 3.6864 MHz clock and the 153.6 kHz clock should be synchronous to help minimize aliasing between the MC145450 and the MC145415.

CARRIER DETECTION

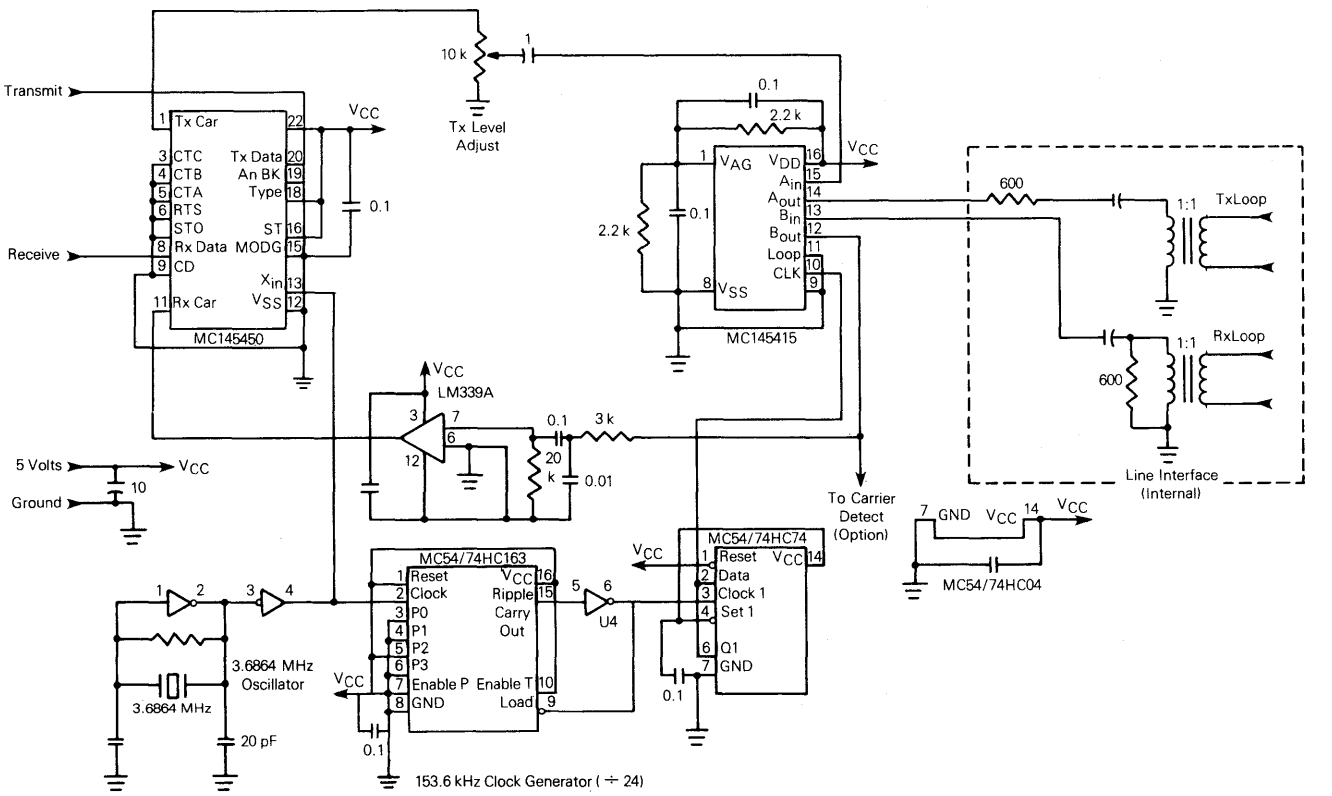
The optional carrier detect circuit utilizes the three remaining comparators on the LM339A. The output of the first comparator (Pin 2) goes into a decay control network formed by R3 and C2. When carrier is detected, Pin 2 goes low, discharging C2. As the waveform passes below its peak, C2 begins to charge through R3 and therefore controls the decay response of the carrier detect. The network at the output of the second comparator (Pin 14) controls the attack time and consists of R4, R5, C3 and the 1N914 diode. When carrier is present, Pin 14 goes low, discharging C3 through R5. Therefore, carrier must be present for a certain amount of time before it is recognized and causes Pin 13 to switch low. The time responses for the attack and decay network are:

$$\text{Attack time} = R5C3\ \ln(0.5) = 111\ \text{ms}$$

$$\text{Decay time} = R3C2\ \ln(0.5) = 52\ \text{ms}$$

Three dB of hysteresis is accomplished by the resistor network R7, R8 and R2. The whole carrier detect circuit will turn on at a received signal level of -29 dBm at the filter input and turn off at -31 dBm.

FIGURE 1 — TYPICAL 1200 BAUD 4 WIRE MODEM APPLICATION



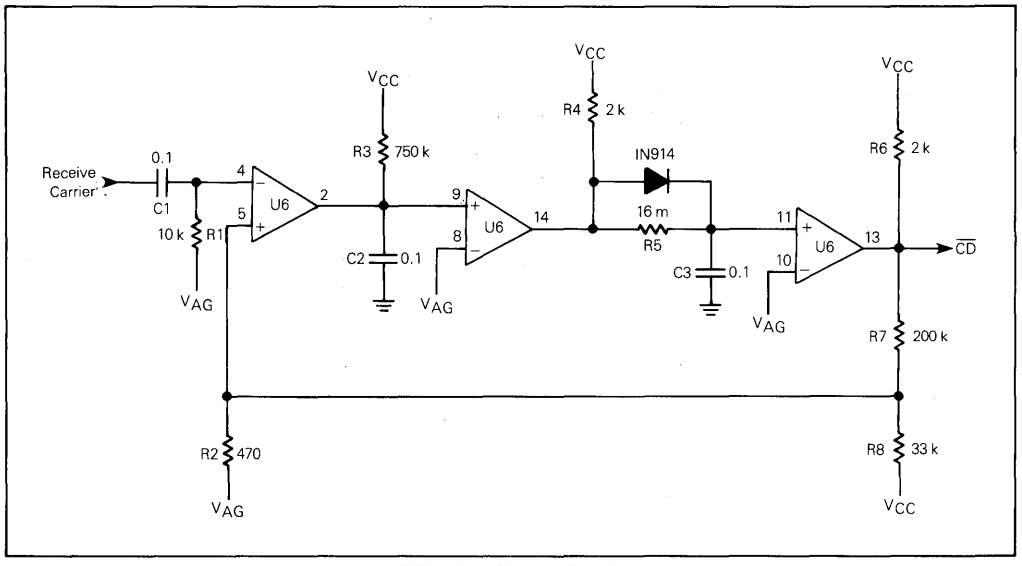


FIGURE 2 — CARRIER DETECT

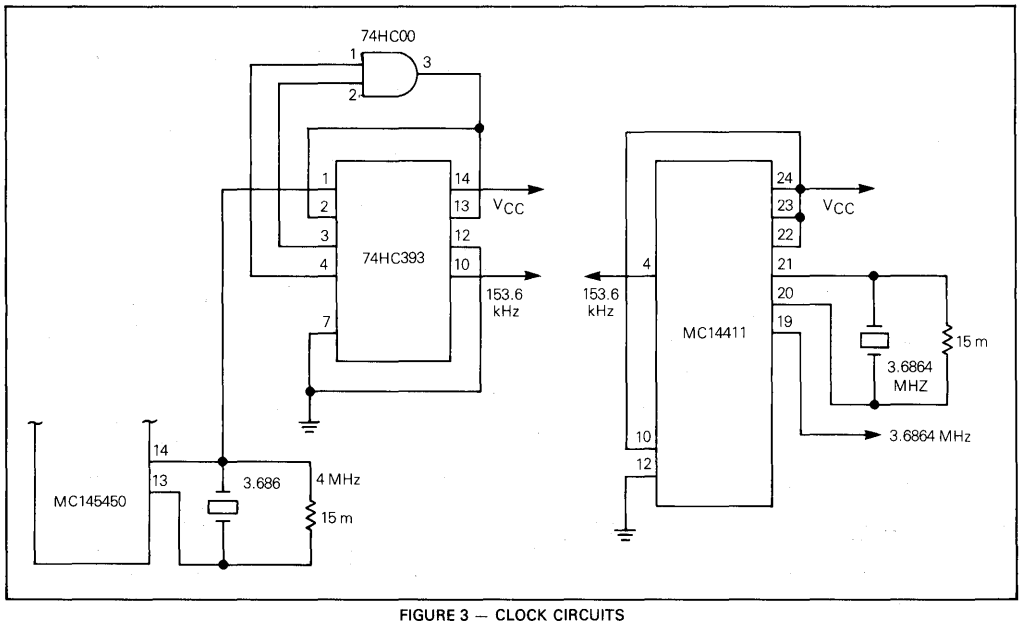


FIGURE 3 — CLOCK CIRCUITS

MOTOROLA

Limited Distance Modem
Using the Universal Digital Loop Transceiver Chip Family

OVERVIEW

The introduction of the Universal Digital Loop Transceiver (UDLT) family of integrated circuits aids the design of a high speed Limited Distance Modem (LDM). With an external clock, the LDM will transmit asynchronous data at rates up to 80 kbps. As shown here with an internal clock, the LDM can send as much as 38.4 kbps of asynchronous full duplex data up to two kilometers on 26 AWG twisted pair wire. The data transfer is controlled by the following RS-232C handshake signals: Request to Send (RTS), Clear to Send (CTS), Data Set Ready (DSR) and Carrier Detect (CD). If the data link is operating, CTS goes active in response to RTS going active. DSR is active if the LDM is powered up. If synchronization is lost, the CD signal goes inactive. Figure 1 shows a block diagram of the LDM. Figure 10 is a photostat of the LDM Demonstration Board - front, and Figure 11 is a photostat of the LDM Demonstration Board - back. Table 1 is a parts list for the slave and master LDM.

UNIVERSAL DIGITAL LOOP TRANSCEIVER

The heart of the LDM is the UDLT master/slave chip set. This chip set transmits data at a 256 kbps burst rate using a "ping pong" approach. As shown in Figure 2, a Modified Differential Phase Shift Keyed (MDPSK) data burst is transmitted from the master to the slave. Then after a slight delay, a burst is transmitted from the slave to the master. Since an eight kHz clock is typically applied to the Master Sync Input (MSI) pin, and ten bits are sent to the master and the slave every MSI period (every 125 μs), the transceiver is effectively transmitting 80 kbps of full duplex synchronous data.

The burst's ten bits of digital data are input on three different pins of the UDLT master. The first eight bits are serially received from the Receive Data Input (Rx) pin. The ninth bit is from the Signaling Bit Input (SI1) and the tenth bit is from the SI2 pin. These ten bits are formatted together and shipped out from the chip on the LO1 and the LO2 pins (Line Driver Outputs). After being transmitted across the line and received on the LI pin of the slave UDLT, eight bits of data are serially output through the slave's Transmit Data Output (Tx) pin, one bit on the SO1 and one bit on the SO2 (Signaling Bit Output). Then the slave UDLT sends a similar burst to the master UDLT.

DLT VS. UDLT

Since the MC145418/19 Digital Loop Transceiver (DLT) chip set is very similar to the UDLT, it is not difficult to adapt

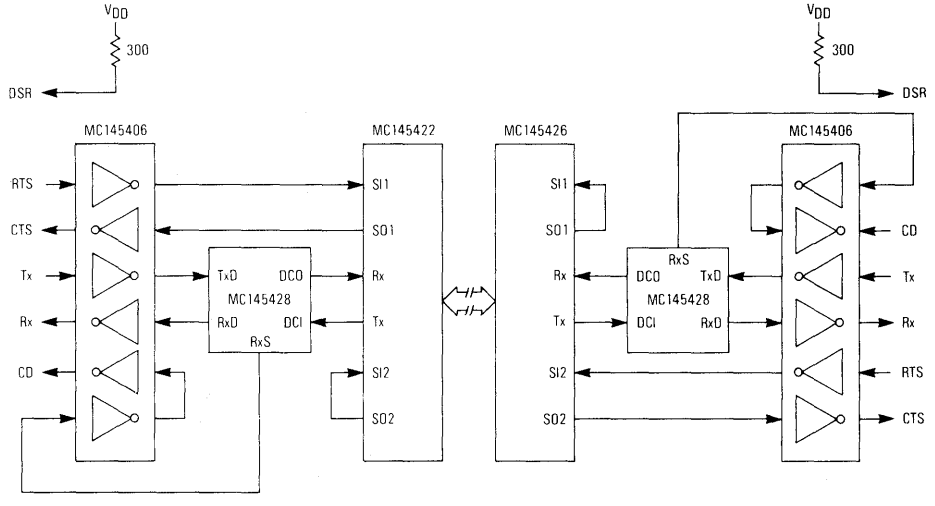


Figure 1. Limited Distance Modem Block Diagram

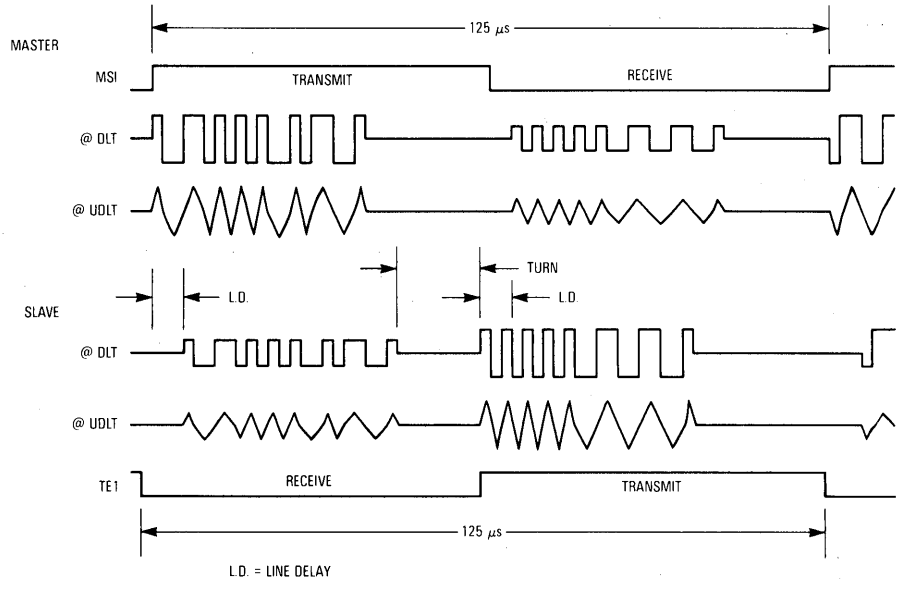


Figure 2. 80 kbps MDPSK Timing Diagram

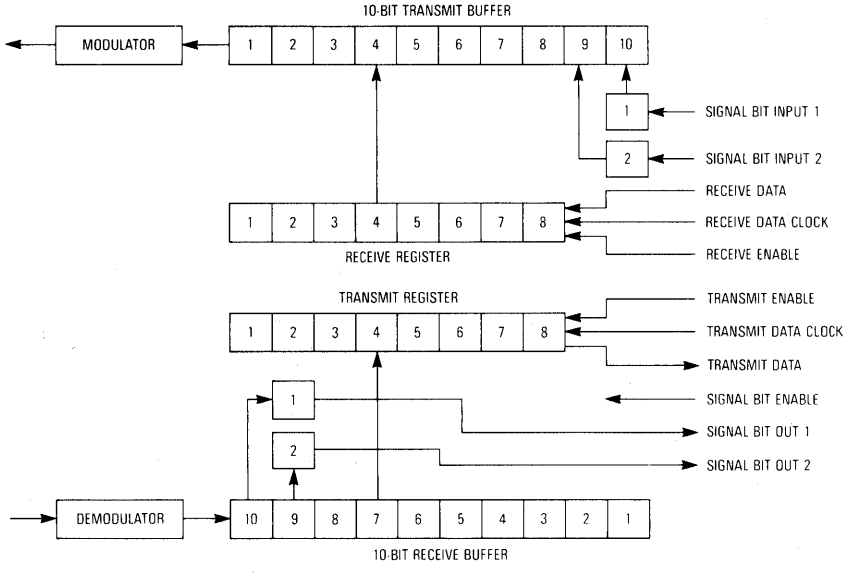


Figure 3. UDLT Receive and Transmit Registers

this LDM to use the DLT. There are three main differences between the UDLT and the DLT chips. The most important difference between the chips is that the UDLT automatically adjusts the thresholds on the receive circuitry. This allows the UDLT to optimize its reception to a particular line's attenuation level. The DLTs threshold is externally set , so typically this receive optimization will not be achieved, unless some rather complex circuitry is implemented. Also, the DLT requires external drivers and transmits square waves instead of triangular waves. In conclusion, the UDLT has on board driver and threshold adjust circuitry, but the DLTs basic approach allows driver and threshold design flexibility.

SIGNALING PINS FOR RTS/CTS HANDSHAKE

This LDM uses the SI1, SI2, SO1 and SO2 pins of the master and slave for a RTS/CTS handshake. To perform this task, the signaling channels are used for transmitting the RTS/CTS handshake. The input at SI1 of the master UDLT is the RTS signal. This information is transmitted to the SO1 of the slave UDLT chip. At this point, the signal is looped around into SI1 of the slave UDLT, and it is transmitted to SO1 of the master UDLT. This signal at SO1 is the master's CTS signal. A similar configuration is used for the slave's RTS/CTS handshake on the SI2/SO2 channel. This allows the RTS/CTS handshake to verify that the communication link is operating.

DATA SET INTERFACE

Since most data from a terminal is an asynchronous format, the Data Set Interface (DSI) is needed to convert data from an asynchronous to a synchronous format and vice versa. At TxD of the DSI, the asynchronous signal should begin with a start bit (logic 0). After following with an eight or nine bit data word, the format ends with one or more stop bits (logic 1). The rate that the data is loaded into the DSI is determined by the internal bit rate generator, whose rate, if 38.4 kbps or less, is selected by BR1, BR2 and BR3 (Baud Rate Select Pins). An external bit rate generator can be used for data rates higher than 38.4 kbps.

Once in the DSI, the data is stripped of its start and stop bits and loaded in a register. Next, the data is checked for a break condition, and one of three types of words is sent, under the timing control of the DC, CM and DOE pins. If a break condition is recognized, the break flag (11111110) is transmitted. If data is in the register, it is dispatched. Finally, if no data is in the register, a synchronizing flag (01111110) is sent. However, regardless of data being in the transmit register, a synchronizing flag is also transmitted on a regular basis to verify that synchronization is intact. Furthermore, the transmit circuitry inserts a binary 0 after five continuous 1's of data, so neither pattern, (11111110) or (01111110), can be sent as data.

At DCI, DC, CM and DIE control the synchronous data's receive loading into the DSI. Once loaded, the DSI's receiver determines if the data is break or synchronizing information. If it is a break or synchronizing flag, the appropriate action is taken. If it is not, the data is loaded into a receive register. From this register, data words are taken, start and stop bits are added and the asynchronous word is output on RxD (Receive Data) at the baud rate selected by BR1, BR2 and BR3. Figure 4 is a block diagram of the DSI.

MC145428
DATA SET INTERFACE

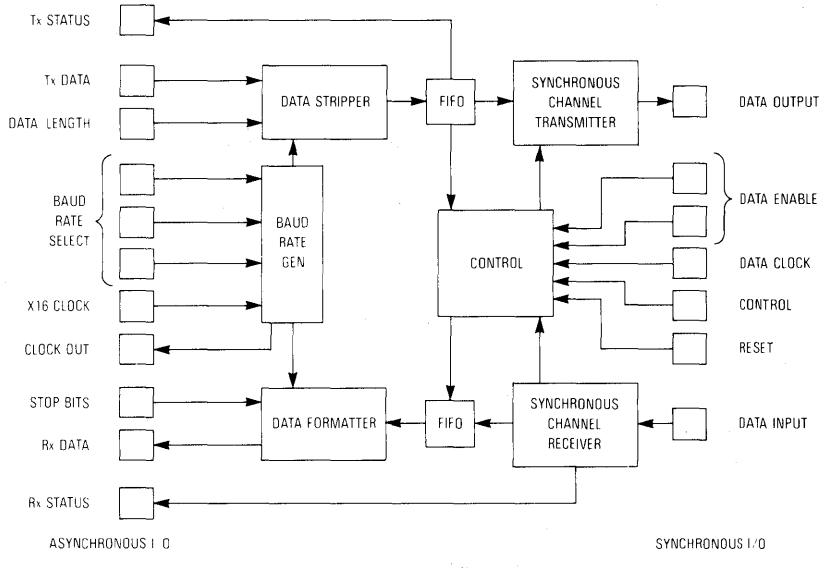


Figure 4. DSI Block Diagram

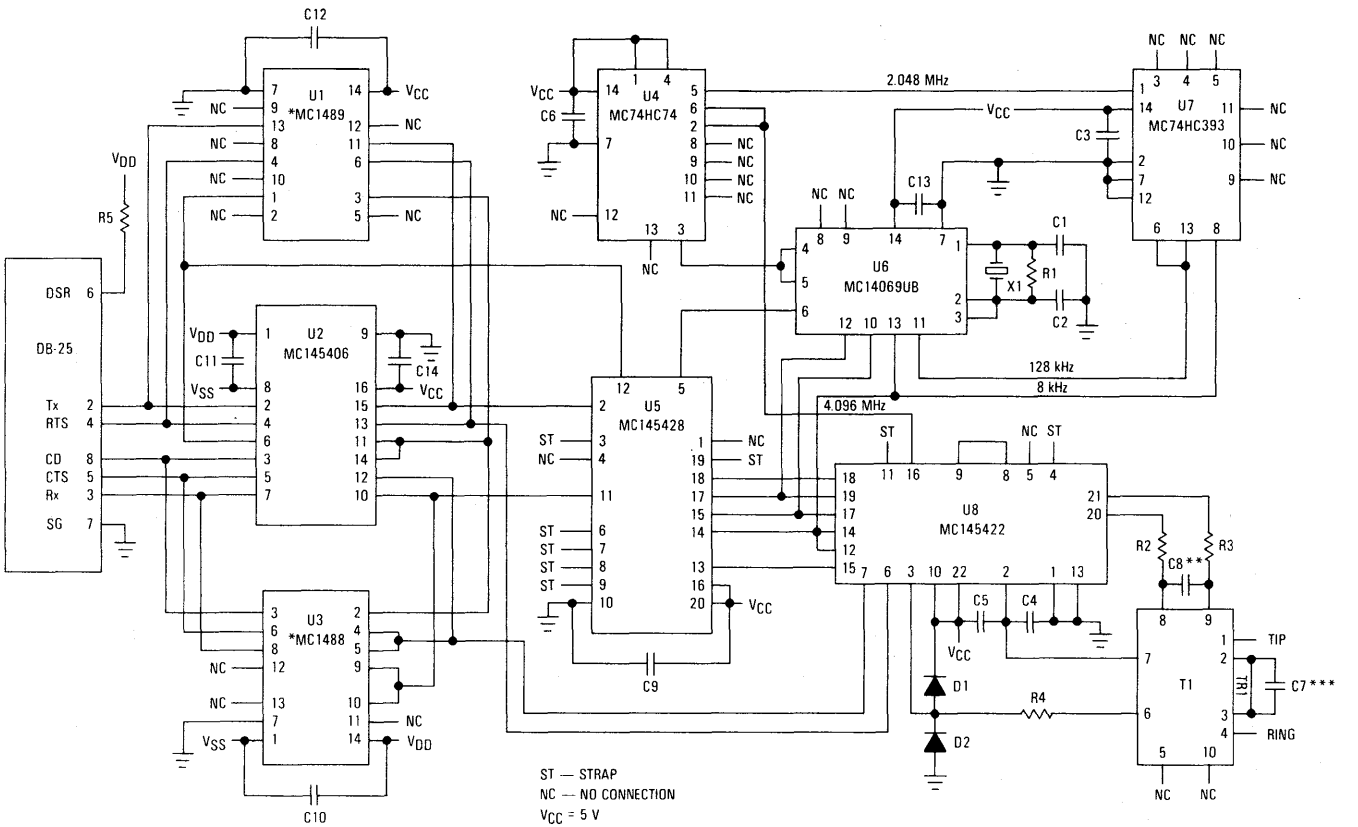
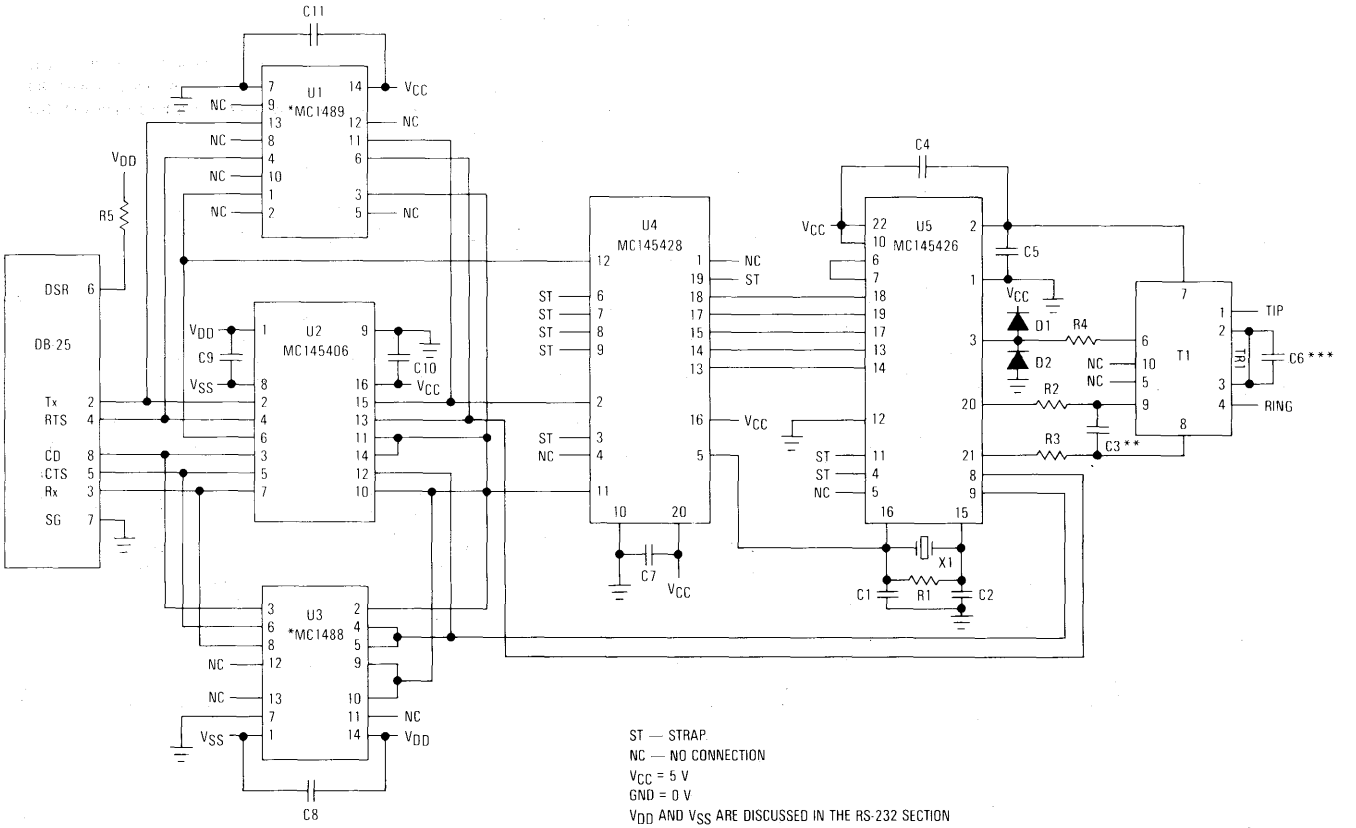


Figure 5. Master Limited Distance Modem



*MC1489 and MC1488 used when MC145406 not used
**C3 is optional filtering.
***TR1 should be cut when C6 is used

Figure 6. Slave Limited Distance Modem

RS-232C DRIVER/RECEIVER

The last integrated circuit discussed is the RS-232C interface. Either the MC145406 or the MC1488/MC1489 Driver/Receiver, which both fulfill the electrical specifications of EIA Standard RS-232C and CCITT Recommendation V.28, can be used. The receivers invert the signal and convert the RS-232 signals to standard five volt logic levels, and the drivers invert the signal and convert five volt logic levels to RS-232 voltage levels.

The MC145406 is a CMOS RS-232 chip with three drivers and three receivers. This chip operates with a five volt supply and ±5 to ±12 volt supplies. Although the MC145406 chip will work with ±5 volt supplies in most systems, the voltage supplies should be at least ±7 volts to meet the RS-232 driver specification. For full RS-232 compliance, the driver's output must be between 5 volts and 15 volts for a logical 0, and it must be between -5 volts to -15 volts for a logical 1.

The MC1488 is a quad line driver. For the MC1488 to comply with the RS-232 driver requirements, a minimum power supply of ±8 volts must be used. However, the chip will operate effectively in most systems with the positive supply voltage varying from +7 to +15 volts. The MC1489 is a five volt quad line receiver.

RS-232C CONTROL AND SIGNALS

As seen in Figure 5, the master LDM schematic, and Figure 6, the slave LDM schematic, asynchronous control and data signals enter the LDM at RS-232 voltage levels through a DB-25 connector. Figure 7 shows a DB-25 connector which is the standard computer terminal connector. Pins 2,3,4,5,6,7,8 transmit the following information:

Pin 2: Transmit Data (Tx)
Pin 3: Receive Data (Rx)
Pin 4: Request to Send (RTS)
Pin 5: Clear to Send (CTS)
Pin 6: Data Set Ready (DSR)
Pin 7: Signal Ground (GND)
Pin 8: Carrier Detect (CD)

The Tx and RTS signals are fed into the receivers, and the Rx, CTS and CD signals are outputs of the driver. For the CD signal, one of the receivers inverts the signal from the RxS pin of the DSI. When the DSI is in asynchronous status, this inversion gives the CD a logic 0. The output of that receiver is then put into a driver to obtain RS-232 voltage levels. The DSR pin is connected to the RS-232 positive power supply through a 300 ohm resistor. Therefore, DSR will go active whenever the power supply is on. The GND pin is connected to the system's ground. The remaining pins used of the DB-25 connector are routed to the RS-232 Driver/Receiver.

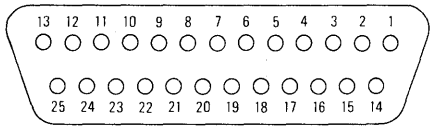


Figure 7. DB-25 Connector

TRANSFORMER INTERFACE

The transformer interface greatly affects the UDLTs capabilities. It performs the functions of impedance matching, bandwidth limiting, increasing receive voltages to required threshold levels and input protection. At 256 kHz, 26 AWG wire's characteristic impedance is 110 ohms. The source resistors from the LO1 and LO2 pins are chosen to be 220 ohms. With a transformer turns ratio of 2:1, the line side's characteristic impedance is 110 ohms. This configuration impedance matches the twisted pair.

The UDLTs minimum output voltage from the LO1 and the LO2 pins is 2.25 volts peak. Half of the voltage is lost across the 220 ohm source resistor. That voltage of 1.12 volt peak is halved again by the 2:1 turns ratio of the transformer to 0.56 volts peak. At 256 kHz, 26 AWG wire attenuates a signal level of 18 decibels-per-kilometer. After traveling a distance of two kilometers the signal will have attenuated 36 decibels. At the line side of the transformer, the minimum signal level is 8.9 millivolts peak. A turns ratio of 1:4 in the transformer windings brings the signal level up to 35.6 millivolt peak. This voltage is divided between a resistor from the transformer to the LI pin and an internal resistance. At worst case, 29 millivolt peak are at the LI pin — within the 25 millivolts peak minimum allowed signal.

The UDLTs maximum voltage output is 3.0 volts peak. Because of the voltage being halved by the source resistors and the transformer windings, the transmit signal level at the line side is 0.75 volt peak. With a short loop, the signal level drop is negligible, so the signal level at the receiving transformer is about 0.75 volts peak. With the 1:4 turns ratio at the receiving transformer, the signal level at LI will be 3.0 volts peak, which exceeds the 2.5 volt peak maximum input at LI. A signal level greater than 2.5 volts peak will inject current into the UDLTs substrate. This action will distort the modulator's output, thus creating bit errors. Consequently, protection diodes and resistors are needed to clamp the input at LI. The demonstration board's transformer configuration is shown in Figure 8. The LI pin's protection includes a 1 kilohm resistor between the LI pin and the diodes. This resistor is not on the

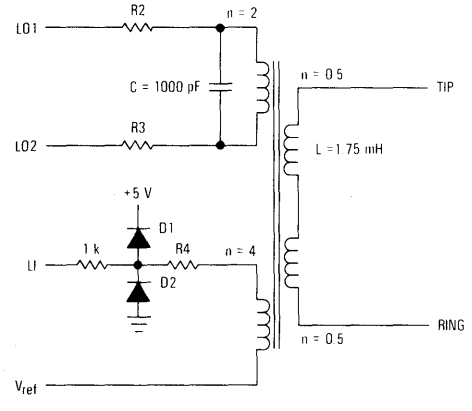


Figure 8. Transformer Configuration Used in LDM Schematic

demonstration board. Typically, the external diodes will turn on before the chip's internal diodes, so the external diodes will shunt most of the current. However, the 1 kilohm resistor will further ensure that the external diodes turn on first.

The maximum power bandwidth of the UDLT is 8 to 512 kHz, but to improve line settling, it is desirable to use a 20 to 512 kHz bandwidth. To make the lower corner of the bandwidth 20 kHz, the inductance of the transformer windings is chosen to be 1.75 millihenries. To make the upper corner of the bandwidth 512 kHz, a 0.001 microfarad capacitor is placed in parallel with the transmit tap. If battery feed is used, further input protection is advised. Figure 9 shows a more durable transformer configuration. Transformers fulfilling these specification can be obtained from:

Leonard Electric Products Company
85 Industrial Drive
Brownsville, Texas 78521
Part Number: P/N P-1358-A

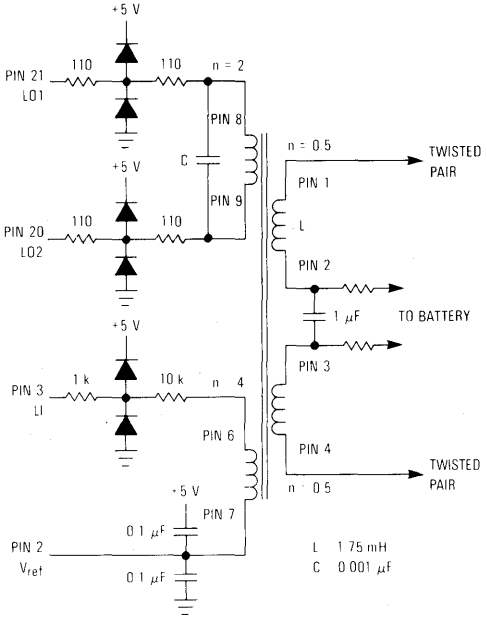


Figure 9. Battery Feed Transformer Configuration

LDM BOARD OPTIONS

A picture of the LDM demonstration board is shown in Figure 10 and 11. Many of the UDLT and DSI features are made available on the demonstration board using straps. These UDLT features include:

$\overline{LB}$: In the master, a low disconnects the LI pin from the internal circuitry, drives LO1, LO2 to V_{ref} and internally ties the modulator to the demodulator. In the slave, a low on the $\overline{LB}$ pin makes the incoming demodulated data going to Tx replace the incoming data on Rx.

$\overline{PD}$: A low powers down the UDLT, except for the receive circuitry.

The DSI features that can be controlled using the straps include:

SB: A low selects outputting one stop bit per data word, and a high selects outputting two stop bits.

DL: A low selects operating with eight bit data words, and a high selects operating with nine bit data words.

Reset: A low clears the internal FIFO, disables TxD, and forces TxS and RxS low.

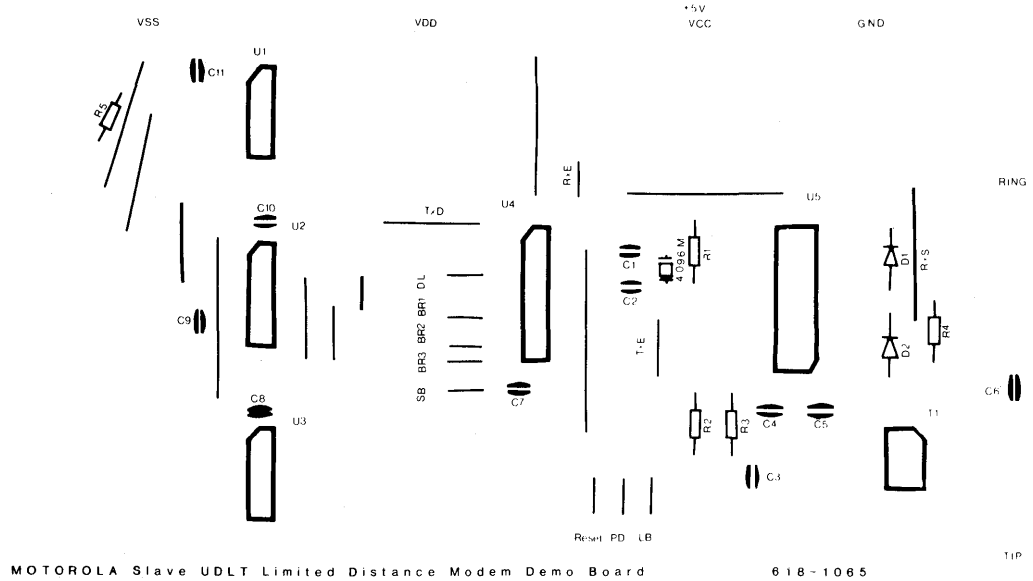
BR1, BR2, BR3: These pins select the asynchronous data rate.

For more information, refer to the individual data sheets. The top of the LDM board shows suggested straps for these functions. These straps select one stop bit, an eight data word, an inactive Reset, a 9600 baud asynchronous data rate, an inactive loop-back and an inactive power-down.

For battery feed applications, C6 of the slave LDM and C7 of the master LDM can be inserted, and the trace between these pins should be broken. This capacitor allows ac signals to pass through the transformer, but keeps dc power across the capacitor to be fed into the system's power supply. C3 of the slave LDM and C8 of master LDM provide filtering for the upper corner of the bandwidth. If this filtering is not desired, these capacitors may be omitted, but their insertion is recommended.

CONNECTORS

On the demonstration board, V_{SS} and V_{DD} are only used to power the RS-232 circuitry. V_{SS} is the most negative power supply, and V_{DD} is the most positive power supply. The RS-232C Driver/Receiver section explains the appropriate voltage ranges for using either the MC145406 or the MC1488/MC1489. V_{CC} is the board's five volt supply, and GND is the board's digital ground. Tip and Ring are the connections for the twisted pair wire. The 25 pins on the left side of both the slave and the master board is for the DB-25 connector.



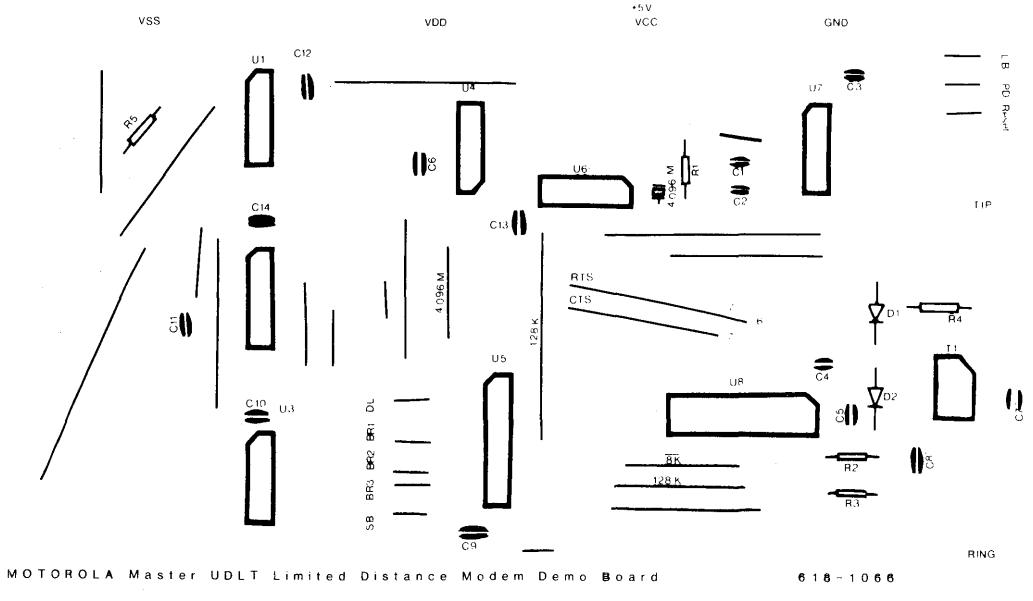
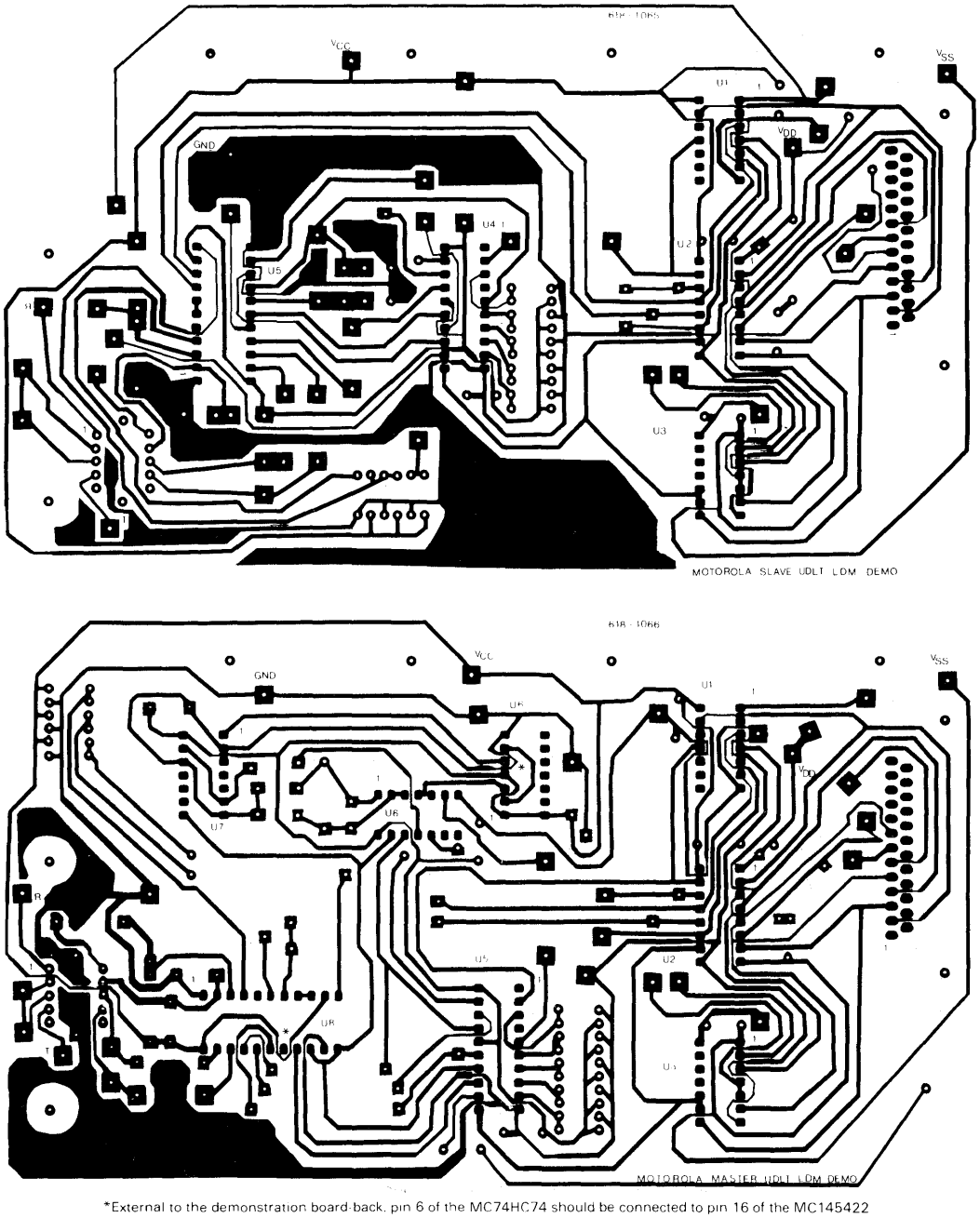


Figure 10. Photostat of LDM Demonstration Board - Front



*External to the demonstration board-back, pin 6 of the MC74HC74 should be connected to pin 16 of the MC145422

Figure 11. Photostat of LDM Demonstration Board - Back

Table 1. Limited Distance Modem Parts List

Master LDM		Slave LDM	
R1: 10 MΩ	R4: 10 kΩ	R1: 10 MΩ	R4: 10 kΩ
R2: 220 Ω	R5: 300 Ω	R2: 220 Ω	R5: 300 Ω
R3: 220 Ω		R3: 220 Ω	
C1: 20 pF	C8: 1000 pF	C1: 20 pF	C7: 0.1 μF
C2: 20 pF	C9: 0.1 μF	C2: 20 pF	C8: 0.1 μF
C3: 0.1 μF	C10: 0.1 μF	C3: 0.001 μF	C9: 0.1 μF
C4: 0.1 μF	C11: 0.1 μF	C4: 0.1 μF	C10: 0.1 μF
C5: 0.1 μF	C12: 0.1 μF	C5: 0.1 μF	C11: 0.1 μF
C6: 0.1 μF	C13: 0.1 μF	C6: 1.0 μF	
C7: 1.0 μF	C14: 0.1 μF		
D1: 1N914	D2: 1N914	D1: 1N914	D2: 1N914
X1: 4.096 MHz		X1: 4.096 MHz	
U1: MC1489		U1: MC1489	
U2: MC145406		U2: MC145406	
U3: MC1488		U3: MC1488	
U4: MC74HC74		U4: MC145428	
U5: MC145428		U5: MC145426	
U6: MC14069UB			
U7: MC74HC393			
U8: MC145422			
T1: Lepco P/N P-1358-A		T1: Lepco P N P-1358-A	

MOTOROLA

Data Multiplexing
Using the Universal Digital Loop Transceiver and the Data Set Interface

INTRODUCTION

Data multiplexers find applications where clusters of terminals are connected to a central computer and in systems where modems are pooled at a common location. Combining the signals from the various terminals onto one multiplexed data link simplifies wiring and reduces expenses. Sharing the cost of the multiplexer among the several terminals results in a lower net cost compared to installing and maintaining individual cables for each terminal. While present day multiplexers are economical, new ICs from Motorola make possible enhanced performance multiplexers for a fraction of the cost of existing devices.

This Application Note will describe the design of a short-haul multiplexer for asynchronous data at rates up to 9600 baud. The mux combines eight full-duplex data channels along with eight end-to-end RS-232 control signals onto a single pair of telephone wire for distances up to 2 km. Motorola's Universal Digital Loop Transceivers (MC145422/26 UDLTs) master/slave high-speed synchronous data transceivers and Data Set Interface (MC145428 DSI) full-duplex asynchronous to synchronous converter form the heart of this multiplexer. A few MSI CMOS ICs complete the design.

Figure 1 illustrates a typical system with the terminals in a departmental situation multiplexed onto one high-speed data link. RS-232 control signals are passed transparently through the multiplexer so the terminals have direct access to the controls of the modems. This multiplexer system transports one control signal bidirectionally for each data channel. As will be described below, other configurations may easily be constructed with simple wiring changes.

CHARACTERISTICS OF THE UDLTs

The UDLTs are synchronous data transceivers capable of transporting 80 kbps of full-duplex data over ordinary twisted pair 26 to 19 gauge telephone wire at distances of up to 2 km. These devices utilize a 256 kilobaud MDPSK ping-pong burst modulation technique for transmission. Three logical data channels, one of 64 kbps and two of 8 kbps each are exchanged in bursts of 10 bits every 125 μs frame. MDPSK timing is shown in Figure 2. The master initiates a ping-pong frame by bursting 10 bits of data to the slave beginning on the rising edge of an externally generated Master Sync Input (MSI). The modulator's analog output signal (LO1, LO2) is shown referenced to MSI. Upon receiving the last bit from the master, the slave responds with a 10 bit burst of its own after a four baud delay. The slave's modulator output (LO1, LO2) is shown referenced to its own Transmit Enable 1 (TE1). Depending on the transmission line characteristics and length, the actual time of arrival of the slave's return burst at the master will vary due to the propagation time of the signal

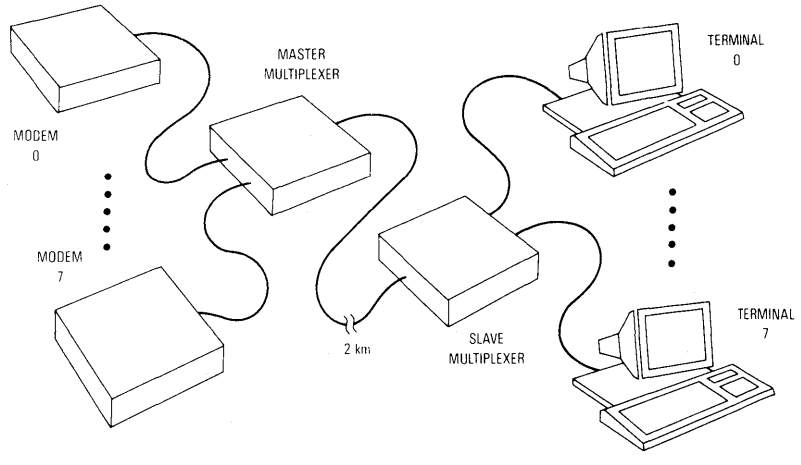


Figure 1. Typical Multiplexer Application

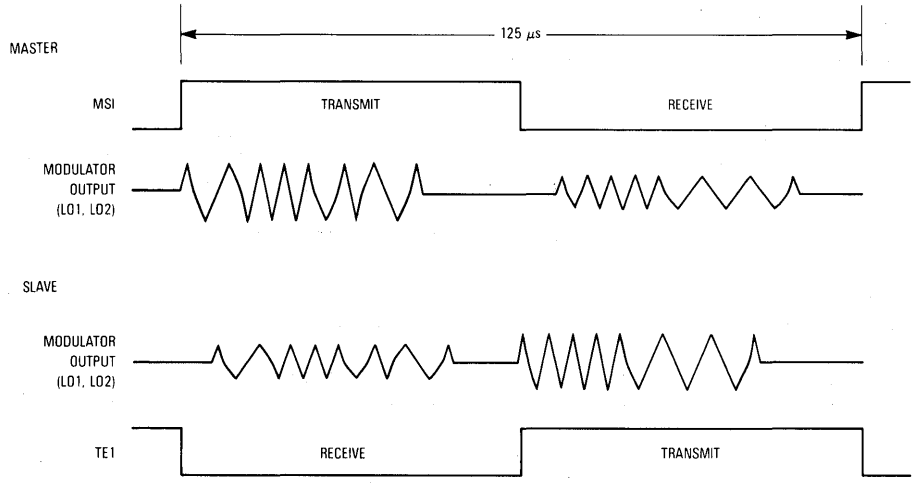


Figure 2. UDLT Timing

between UDLTs. On excessively long lines, propagation time down the transmission line results in collisions between the master and slave bursts so maximum line length is limited to 2 km with 26 gauge wire. The slave's TE1 is generated internally upon completion of demodulation of the burst from the master. TE1 remains high for eight data clock (128 kHz) periods and returns low until another burst is received. This process is repeated every 125 μs. Since both master and slave devices exchange data every frame in a half-duplex manner at a 256 kilobaud rate, an effective full-duplex rate of 80 kilobaud is accessible to the user.

The bursts of data on the transmission line use Modified DPSK signals to reduce EMI and susceptibility to crosstalk from other signals in telephone cables. The frequency spectrum consists of peaks at 128 kHz and 256 kHz and their odd harmonics. Only a small amount of energy is present in the frequency bands used by analog telephone service, so UDLT signals may be placed on adjacent pairs in cables with ordinary telephone signals with no degradation of performance. The power spectral density at 76 kHz is approximately 18 dBm and at 28 kHz the level is less than -30 dBm. Because there is no signal energy at very low frequencies, dc energy may be transported on the transmission line to power the remote multiplexer unit. Details of this feature will be described later.

The UDLTs have internal buffers to store and prepare synchronous data for transmission. Eight bits for the 64 kbps channel are serially input and output every 125 μs frame. The two 8 kbps channels each have one bit input and output every frame. The master and slave UDLTs synchronous timing is shown in Figures 3 and 4 respectively. Both figures illustrate the transmit and receive timing for the eight bit words on Tx and Rx, and the timing for the two signalling bits, both inputs (SI1, SI2) and outputs (SO1, SO2).

The master UDLT timing shown in Figure 3 requires external timing signals of 8 kHz for MSI, TE1, RE1, and 64 kHz up to 2.56 MHz may be used for the TDC/RDC pin. This application uses 128 kHz. Eight bits of the 64 kbps data channel received from the slave are output on the Tx pin on the first eight rising edges of TDC/RDC while TE1 is high. Data to be sent to the slave is input on the Rx pin on the first eight falling edges of TDC/RDC while RE1 is high. In this application TE1 and RE1 are connected together so data is input and output simultaneously. Data on the 8 kHz signalling channels are input on SI1 and SI2 pins and output on SO1 and SO2 pins on MSI's rising edge.

The slave UDLT timing (shown in Figure 4) is similar to the master except that the slave synchronizes to the master's bursts and generates its own clocks and enables. The eight bits of the 64 kbps data channel received from the master are presented on the Tx pin on the rising edges of CLK while TE1 is high. Data to be transmitted to the master is loaded in on the Rx pin on the falling edges of CLK while RE1 is high. Signalling bits on the 8 kbps channels to and from the master are input at SI1, SI2 and output at SO1, SO2 on TE1's rising edge.

The master UDLT has pin controlled Power-Down ($\overline{PD}$) and Loop-Back ($\overline{LB}$) features which can be used for system testing. Also available on the master is Signal Insert Enable (SIE) which enables the insertion and extraction of an 8 kbps channel into the LSB of the 64 kbps channel. In this application SIE is unused and held low. The signal enable pin ($\overline{SE}$) is a three-state control pin which when held high enables $\overline{PD}$, $\overline{LB}$, and the two signalling bits (SO1 and SO2) allowing these signals to be bussed to a microprocessor.

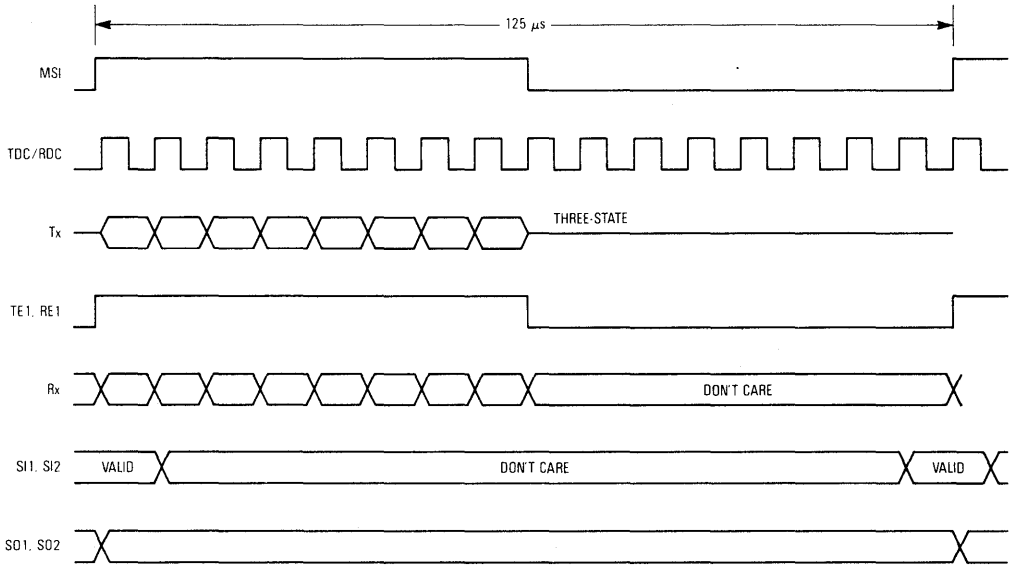


Figure 3. Master Timing

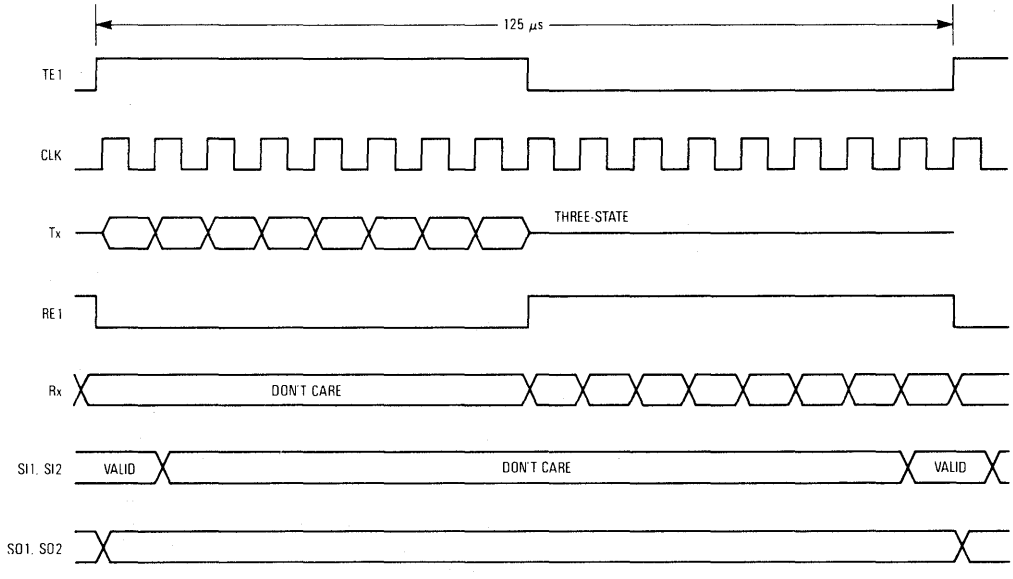
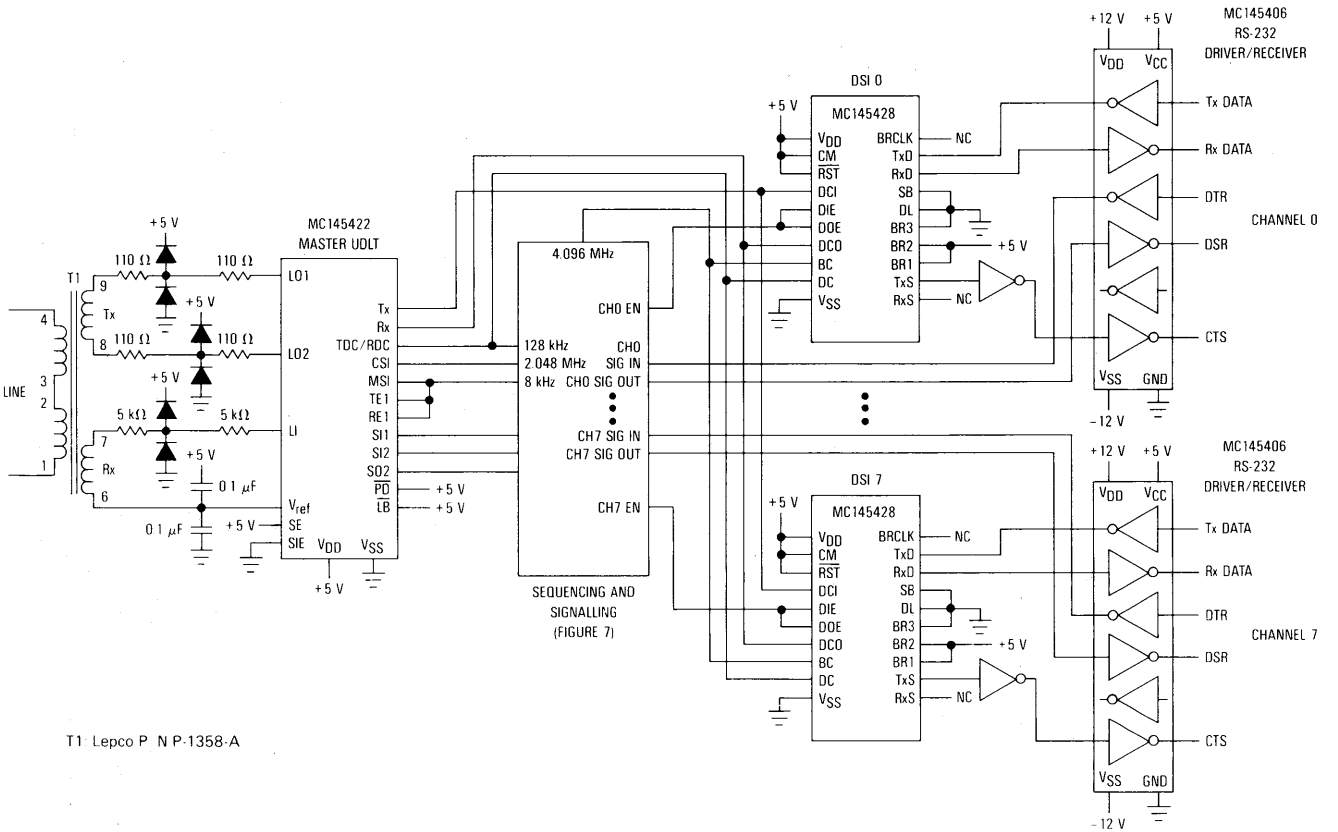


Figure 4. Slave Timing



T1: Lepco P N P-1358-A

Figure 5. Master Unit Interconnect

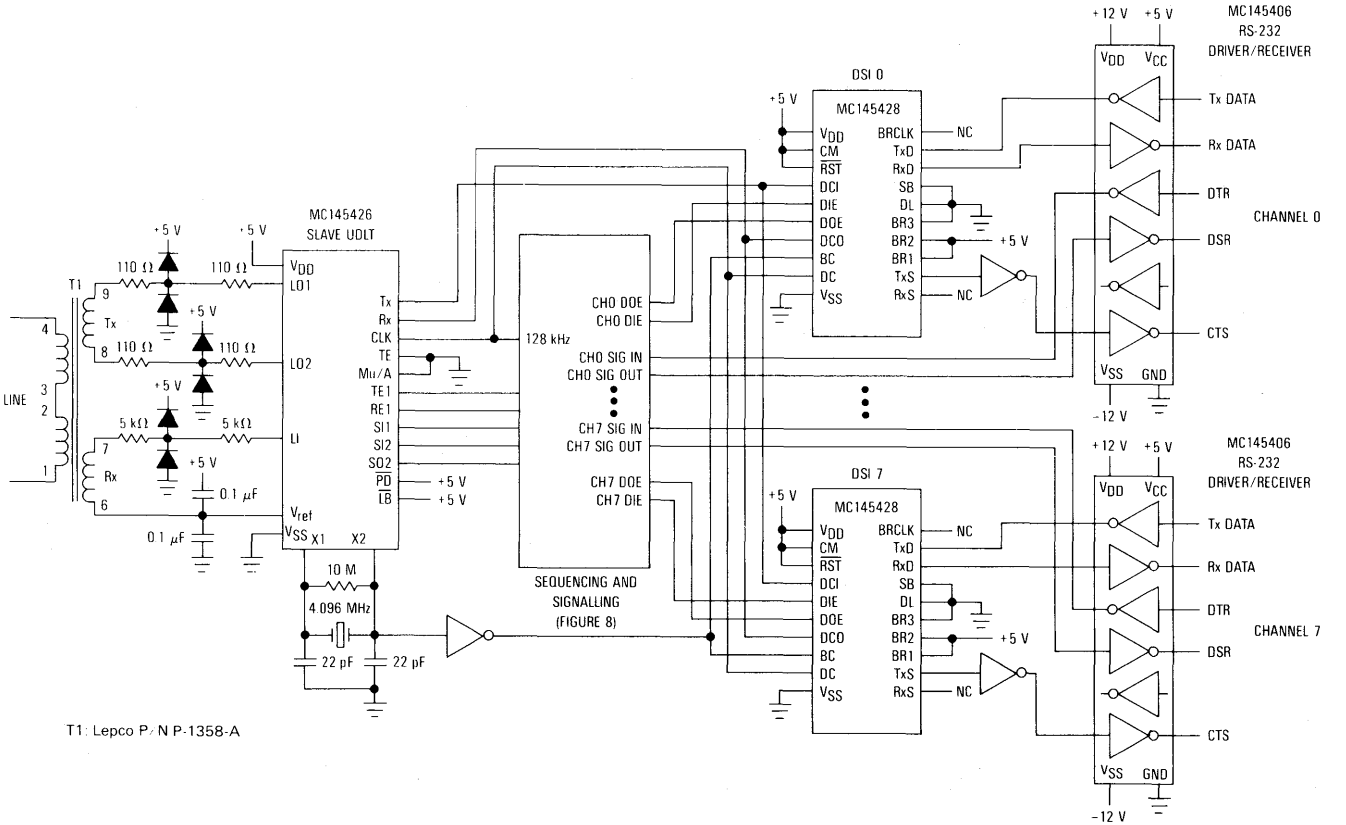


Figure 6. Slave Unit Interconnect

TRANSFORMER INTERFACE

The duplexer function, separating transmit and receive bursts on a single twisted pair wire is automatic with UDLTs. The receiver input is blanked while the transmitter is active so the transmitted signal is ignored by the demodulator circuits. The receiver unblanks when the transmitter finishes its burst to search for the return burst from the other end. Automatic duplexer action allows a simple transformer to be used for the interface between the transmission media and UDLTs shown in Figures 5 and 6. The transformer Tx winding and the associated padding network match the transmitter output to the impedance of the transmission line. The Rx winding steps up the signal from the far end to compensate for the loss in the matching network. The characteristic impedance of twisted pair telephone wire in the frequency range used by the UDLTs is approximately 110 ohms. Matching this impedance requires resistors of 220 ohms in each leg of the Tx winding. The impedance of 440 ohms when transformed through a 2:1 turns ratio results in a match to 110 ohms. 12 dB of loss is also introduced. The 12 dB is made up in the Rx winding which has a 4:1 step-up from line to receiver input.

Protection of the UDLTs against transients induced onto the transmission line is accomplished by adding clamp diodes to the padding networks. It is convenient to split the 220 ohm resistors into two 110 ohm resistors and place the clamps at the junction of the resistors. The same technique is used at the receiver inputs.

CHARACTERISTICS OF THE DSI

The DSI is a device which provides full-duplex asynchronous to synchronous conversion. It allows the user to select asynchronous data formats and baud rates. The synchronous port has selectable timing for easy interfacing to a variety of systems. The asynchronous port characteristics are controlled by the Stop Bit select (SB), Data Length select (DL), Baud Rate select (BR1-BR3) pins. Synchronous data is under the control of the Data Output Enable (DOE), Data Input Enable (DIE), Data Clock (DC), and Clock Mode (CM) pins. Asynchronous data is sampled at 16 times the selected baud rate. Logic circuits search the asynchronous data for a start bit, eight or nine data bits and one or two stop bits. When valid start and stop bits are found, they are removed from the character and the remaining eight or nine data bits are loaded into the transmit FIFO for transmission on the synchronous port. The Tx Status pin goes low when the transmit FIFO is more than half full. This signal may be used for a local Clear-To-Send indication to the data device on the asynchronous port. Special characters are generated and transmitted on the synchronous port to synchronize the receiver of the remote DSI to the character boundaries. At the remote DSI synchronous data is reassembled into eight or nine bit characters, start and stop bits are added and the data is transmitted out on the asynchronous port.

Since start and stop bits are removed from the asynchronous data before transmission on the synchronous port, some data compression is achieved. For example, asynchronous data at 9600 baud with eight data bits and one stop bit is compressed to 7680 baud on the synchronous channel. This makes possible the use of an 8 kbps synchronous channel to transport 9600 baud data. However, since sync and break characters consisting of data patterns 01111110 and 11111110 respectively are exchanged between DSIs every so often, the effective data compression is somewhat reduced. Zero bit insertion on the synchronous data between DSIs is used to eliminate the possibility of data imitating either of these characters (the inserted zeros are removed by the synchronous receiver). The multiplexer allocates the UDLTs 64 kbps synchronous channel to each DSI for one 125 μs ping-pong frame out of every 1 ms data frame. This results in an 8 kbps synchronous channel for each DSI. Under certain circumstances, with binary data, zero insertion may cause the transmit FIFO to overrun. If hex 'FF' characters are input to the DSI on the asynchronous port at 9600 baud with minimum time between characters, inserted zeros and sync characters cause the effective data rate to increase from 7680 baud to approximately 9400 baud. Since the synchronous channel supports only 8 kilobaud, an overrun of the Tx FIFO will occur. The TxS pin will go low approximately 5 ms before an overrun occurs and this indication may be used to stop the flow of new asynchronous data until the FIFO clears out. When ASCII data is used, only 6 characters (>(3E hex), ?(3F hex), |(7C hex), ~(7E hex), DEL(7F hex), and Blank(7D hex)) generate stuffed zeros. Fortunately, it is unlikely that these characters will be sent in large enough groups to cause FIFO overruns. In applications where ASCII data is transported, eight 9600 baud channels may be multiplexed onto this system's 64 kbps synchronous channel. If binary data is transported, a 16 kbps synchronous channel must be allocated for each DSI, resulting in a four channel multiplexer. This guarantees that even with maximum zero insertions, FIFO overruns will not occur.

OCTAL MULTIPLEXER SYSTEM DESCRIPTION

This multiplexer system fully exploits the DSI chips and the UDLT transceiver pair. The UDLTs 64 kbps channel transports the synchronous data from the DSIs. One of the UDLTs 8 kbps channels is used to synchronize the multiplexing of the eight data channels, and the other 8 kbps channel is used to transport eight RS-232 control signals.

The multiplexer system consists of two units, a master and a slave. Figure 5 illustrates the interconnection of the various devices within the master unit. The transformer interface to the twisted pair is shown with the previously described impedance matching and protection circuitry. The master UDLT is shown with the Tx, Rx lines along with the 128 kHz and the 4.096 MHz clocks bussed to the eight DSIs. The data channel enables and signalling lines are shown connecting the DSIs and the RS-232 driver/receivers to the sequencing and signalling block. Each DSI is shown configured for 9600 baud with eight bit character lengths and one stop bit which may be made switch selectable, if desired.

Figure 6 shows the complementing slave unit. Protection circuitry and the transformer interface are the same as the master unit. The slave UDLT generates its own clocks derived from an on-chip crystal oscillator circuit. An inverter is used to drive the eight clock inputs to the DSIs. Also shown is the sequencing and signalling interconnect to the DSIs and the RS-232 driver/receivers.

Circuitry in the sequencing and signalling blocks is shown in Figures 7 and 8 for the master and slave units respectively. All pertinent timing of the multiplexer system is shown in Figure 9. Master timing is shown in the top section, master and slave bursts on the twisted pair are shown on the line

labeled 'Transmission Line'. Slave timing is illustrated on the bottom half of the figure.

Clocks for the master UDLT are created by a 12-stage ripple counter (MC74HC4040) which is driven by a 4.096 MHz crystal oscillator. Taps at Q1, Q5, and Q9 create the 2.048 MHz (CCI), 128 kHz (TDC/RDC) and 8 kHz (MSI,TE1,RE1) clocks respectively. Inverters are needed on each line so the rising edges coincide. A pulse which synchronizes the master and slave data channel sequencing circuitry is generated when a count of 0 is reached by Q10, Q11, and Q12 of the ripple counter. This pulse is shifted through the enable shift register (MC14015B) to create eight non-overlapping enables for the DSIs. A latch (MC14013B) is used to delay the pulse so that it can be properly input into SI1 of the UDLT on the next rising edge of MSI. The delayed pulse on SI1 and the data channel enables (CH0-CH7 DOE, DIE) are shown on the timing diagram. RS-232 control data is routed to a latch by an addressable data selector (MC14051B). RS-232 control data received from the slave unit is written into an addressable latch (MC14051B). Notice that the first Q0 of the shift register is the enable to the DSI of data channel 1. Since the sync pulse arrives at the input of the shift register slightly after the clock, a one-channel offset is used to address the proper channel. This offset is transparent to the system.

Data input on the Rx pin of the UDLT is buffered until the next rising edge of MSI, when it is burst out on the transmission line. Data on SI1 and SI2 are latched in on the rising edge of MSI and transmitted in the burst which was initiated by that MSI edge. The bursts from the master (boxes with M) and the return bursts from the slave (boxes with S) on the twisted pair wire are illustrated on the 'Transmission Line'. The numbers indicate which channel's data is transported in that burst.

The system sync pulse arrives at the slave unit on the SO1 pin of the UDLT (Figure 8). It is shifted through a shift register (MC14015B) which is clocked by the RE1 pin. The Q's from this shift register enable the transmission of data from the DSIs to the UDLT. The sync pulse is delayed and shifted through another shift register clocked by TE1. The Q's from this shift register enable the DSIs to accept data from the UDLT. RS-232 control data is handled in the slave unit in a similar manner as the master with a data selector and an addressable latch. Simply offsetting the connections to the RS-232 driver/receivers realigns the data to the proper

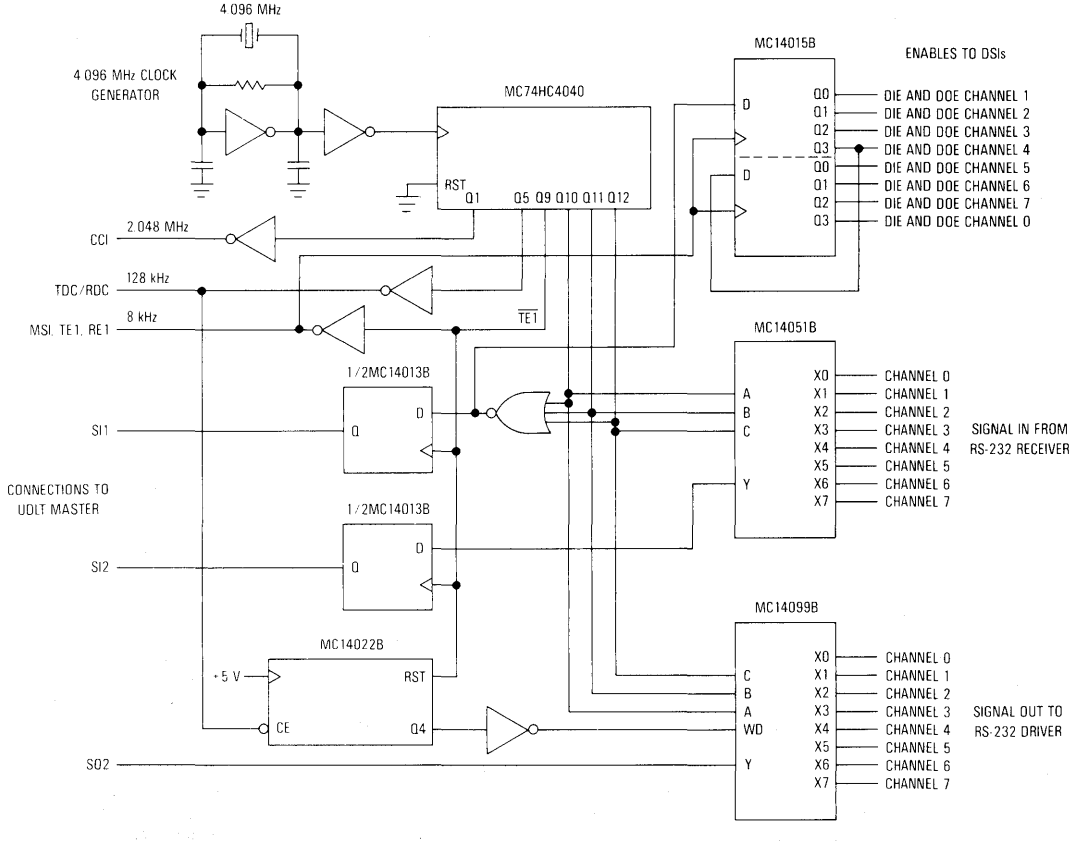


Figure 7. Master Sequencing and Signalling

channels eliminating any superfluous circuitry. Offsetting the connections to the data selector (MC14051B) similarly aligns the channels so that the data arrives at the master in the correct time slot. Following the channels on the timing diagram illustrates the concept.

ADDITIONAL CONSIDERATIONS

This multiplexer design is quite modular. If RS-232 control signalling is not desired then the circuitry can be simplified by removing the write pulse generator (MC14022B), addressable latches (MC14099B) and data selectors (MC14051B) from both units. The address generator (MC14163B) on the slave unit may also be removed. In applications where data rates of less than 9600 baud are used, the Baud Rate select pins on the DSIs need simply be reconfigured. A DIP switch can be conveniently used to set the Baud Rate, Data Length and Stop Bit pins on the DSIs. Note that the DSIs must not be set for 19.2 or 38.4 kilobaud when eight channels are multiplexed. If data rates higher than 9600 baud are desired, the individual data channels must be serviced more often by the UDLT. Because the high-speed synchronous channel between UDLTs is 64 kbps, the total bandwidth required by all of the channels must be at or below 64 kbps. The multiplexer may also be converted into a single channel limited-distance modem where data rates of up to 56 kbps can be attained.

This multiplexer, because it is all CMOS, consumes only about 175 mW per unit. One of the units may be powered by dc energy transported on the transmission line itself eliminating a power cord. The line interface transformer is designed to pass dc energy by separating the two line windings and installing a 1 μF capacitor between pins 2 and 3. Now, dc current may be passed to the twisted pair. A switching power supply may be installed in the remote unit to convert the line power to voltage levels useable by the digital circuitry. Recall that the dc resistance of 2 km of 26 AWG wire is approximately 575 ohms. This necessitates a relatively high voltage on the sending side to keep the I^2R losses in the twisted pair to a tolerable level. Usually 36 to 40 volts is satisfactory to furnish enough voltage to the remote unit. Since the transmission line is balanced, there is no ground reference between master and slave units. dc power to the twisted pair must be fed from an isolated winding on the mains transformer, so that a ground reference may be established at the remote unit. Connecting the ground references of the two units through the twisted pair will result in poor data performance due to longitudinal currents in the line.

References

Motorola Telecommunications Device Data Book DL136, 1984.

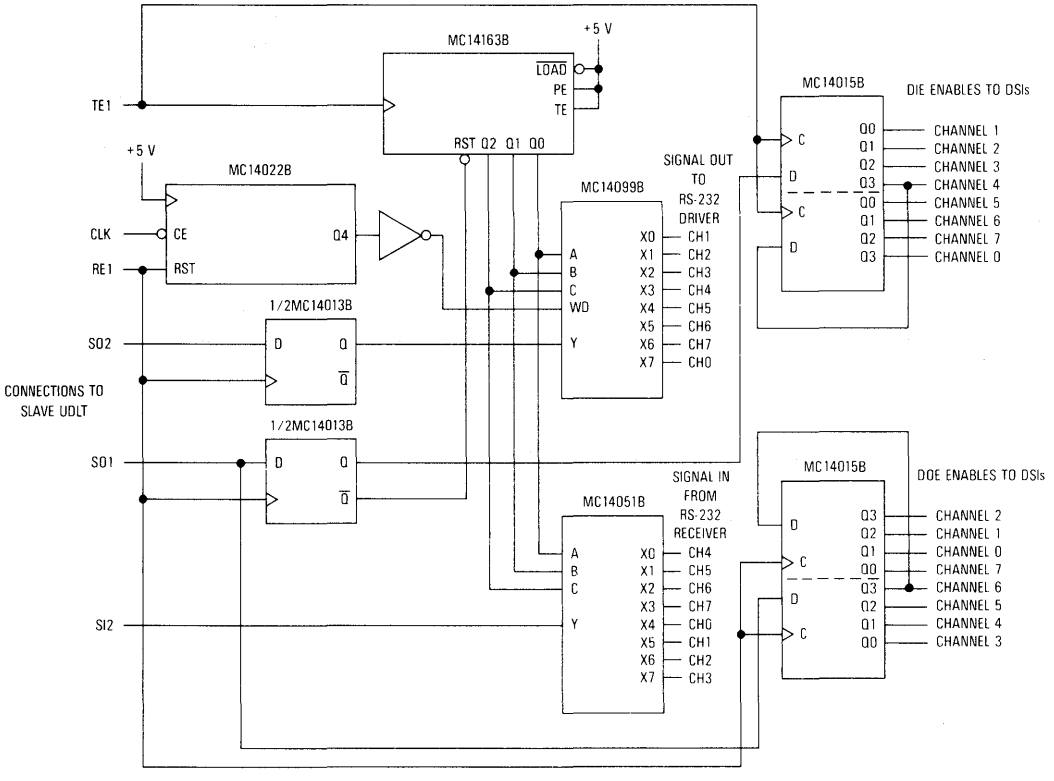


Figure 8. Slave Sequencing and Signalling

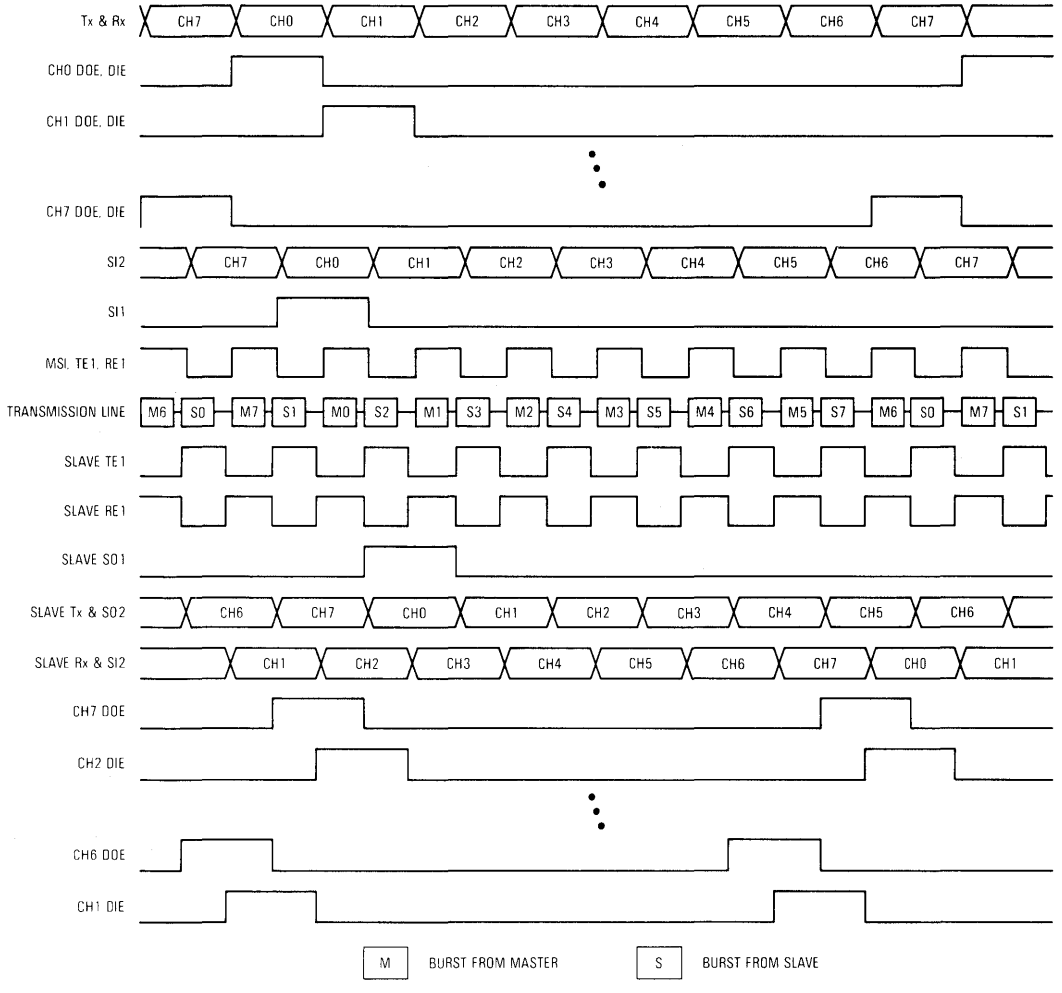


Figure 9. System Timing

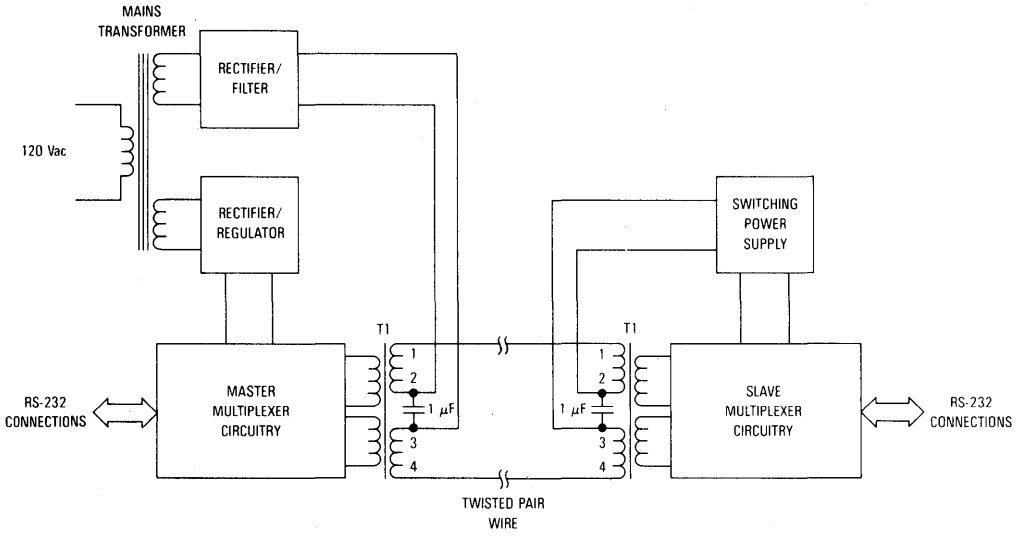


Figure 10. Powering Slave Unit From the Twisted Pair

MOTOROLA

THE APPLICATION OF A DUPLEXER

By Vince Deems
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Austin, Texas

The purpose of this document is to explain the application and operation of a duplexer circuit, to show how to balance a duplexer, and to discuss the duplexer's operation analysis when used with two different transformers and with variable components.

The duplexer circuit shown in Figure 1 is a fundamental circuit that is used to help reject the transmit energy from the receive signal. The circuit in Figure 1 is set up for a standard 600 ohm system.

This circuit eliminates the transmit signal from the receiving point by sending a combination of both signals into the inputs of a differential amplifier. This tends to cancel out the transmit signal leaving only the receive signal. A signal is transmitted into Pin 3, the noninverting input, while a signal is being received across Pins 5 and 8 of the transformer, from the same line. There is a 600 ohm impedance when looking into Pins 1 and 4 of the transformer. With R1 tweaked to approximately 600 ohms, a voltage divider network is established with the 600 ohm impedance of the transformer. Thus, the signal at the noninverting input, Pin 5, is Rx + (Tx/2). The signal at the inverting input, Pin 6, is Tx/2 due to the virtual ground concept. When these inputs are added together, the transmit signal cancels leaving Rx, the receive signal, at the output Pin 7.

There are several ways of balancing or tuning duplexers but only one technique will be explained for this application. The transmit Pin 3 is grounded while a 600 ohm signal source with a predetermined level and frequency is connected to Pins 5 and 8 of the transformer. A signal with a level of − 10 dBm (0.6938 Vp-p) and a frequency of 1700 Hz was used in this circuit. R1 is then tweaked such that the voltage across Pins 5 and 8 of the transformer is half the signal voltage or until there is exactly a 6 dB loss across Pins 5 and 8, (i.e., − 16 dBm at Pins 5 and 8). Next, the 600 ohm signal source set at the same level and frequency is connected to Tx (Pin 3) across a 10 kilohm resistor. A 600 ohm resistor is connected to Pins 5 and 8 of the transformer. Then, R2 is tweaked until there is a minimum signal at Rx. Next, several different values of capacitance are tried for C1 until the smallest null is found at Rx. Once the best value of capacitance has been found, the duplexer has been balanced for that particular input signal and the best possible rejection of the transmission signal to the receive signal has been found. This is called the Transhybrid Rejection and is shown with different values of capacitance in Figure 2.

There are several noisy signals that this duplexer can not eliminate at the receive Pin 7. For instance, deflection of the transmit signal off of the transformer returns out of phase and tends to leak through onto the receive signal. For this particular circuit, curve 1 shows the best rejection over the spectrum.

It is worth noting the difference in performance of this duplexer with respect to the type of transformer used. The rejection versus frequency plot shown in Figure 2 was the result obtained when the Midcom 671-0018 was incorporated. This transformer has winding resistances of 14 ohms on the primary coil and 18 ohms on the secondary. The same test was run with a different transformer (Midcom 671-0915) and the results are shown in Figure 3. This transformer has winding resistances of 178 ohms on the primary coil and 67 ohms on the secondary coil giving it a much larger insertion loss than the Midcom 671-0018. This difference is displayed in Figure 3 as there is not as much rejection with the Midcom 671-0915 over the spectrum as with the Midcom 671-0018 (Figure 2).

It can be seen from Figures 2 and 3 that changing the capacitance changes the amount of rejection. This is due to the fact that the coil (Pins 1 and 4) not only has a resistance but also has an inductive reactance. If there is not a proper sized capacitance in parallel with this inductance, then the overall impedance of the coil increases. This impedance changes the voltage divider with R1 which in turn allows a larger Tx at Pin 5 which is slightly out of phase with the Rx + Tx/2 at Pin 6. This allows more leakage of the transmission onto the receive signal thus decreasing the rejection. This difference between the size of the capacitance and the type of transformer to use is a tradeoff which is left to the designer's judgement.

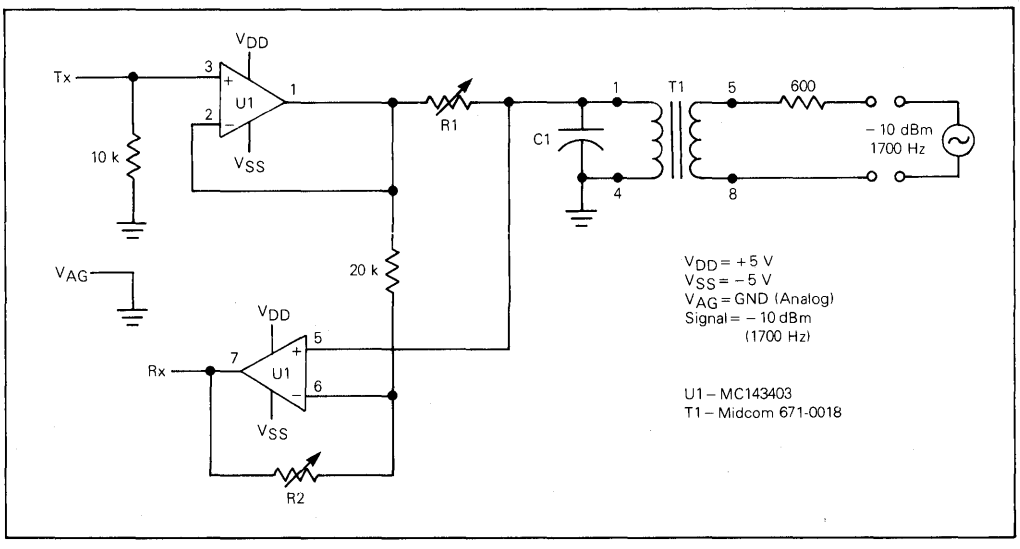

FIGURE 1 — Duplexer Circuit

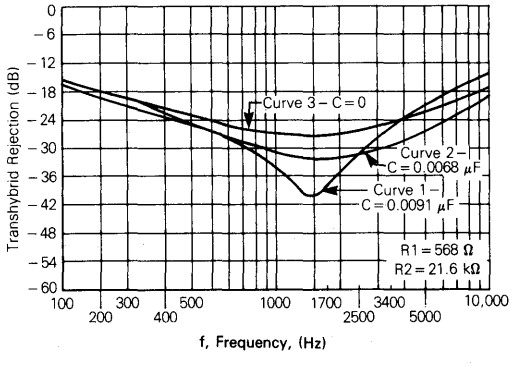

FIGURE 2 — Transhybrid Loss with Midcom 671-0018

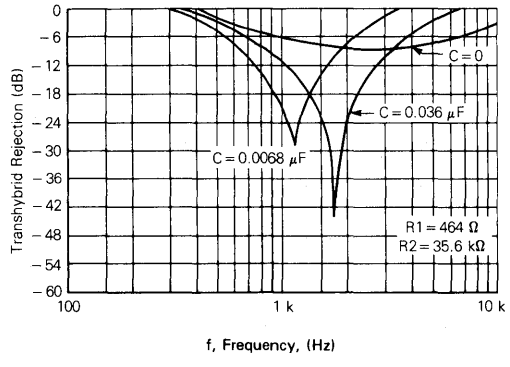

FIGURE 3 — Transhybrid Loss with Midcom 671-0915

Adjustable clock tunes notch filter

by Steve Bramblett
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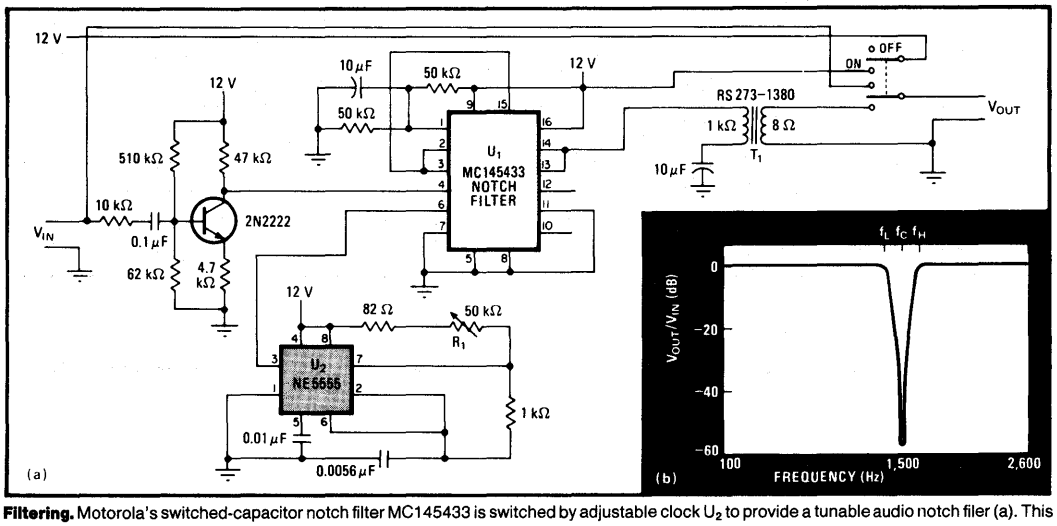
Radio transceivers often require notch filters to suppress interference from nearby broadcast stations. Unfortunately, most notch filters can handle only one frequency. This design employs a switched-capacitor notch filter to form an audio notch filter whose center frequency is externally tuned by varying the circuit's clock frequency. The changing clock frequency alters the filter's poles and zeros, resulting in a tunable notch filter.

A frequency generated by clock U_2 is used as the switching frequency for the tunable notch filter (a) whose notch frequency is $f_c = f_s/49.23$ hertz, where f_s is the switching frequency input. In addition, the filter's low and high 3-decibel points can be calculated, respectively, from equations $f_l = f_s/58.2$ Hz and $f_h = f_s/45.71$ Hz. Since tunable filter U_1 is not capable of driving less than 600 ohms directly, 1,000-Ω-to-8-Ω transformer T_1 is used at the output to increase the load impedance.

In order to compensate for the transformer loss and improve the circuit's signal-to-noise ratio, the filter uses an input amplifier that employs transistor Q_1 to provide a gain of 20 dB. Because U_2 can generate switching frequencies between 5 kilohertz and 128 kHz, the filter may be tuned between 100 Hz and 2.6 kHz. This circuit is designed to operate on +12 volts dc but will function with voltages between +10 to +15 V dc. In addition, when the circuit is switched off, the input is shunted directly to the output. The filter may be used by attaching the input to the receiver's headphone output jack and connecting the filter's output to the headphones. Interfering heterodyne frequencies may be suppressed by adjusting potentiometer R_1. □



Filtering. Motorola's switched-capacitor notch filter MC145433 is switched by adjustable clock U_2 to provide a tunable audio notch filer (a). This notch filter has a frequency response of about 100 Hz to 2.6 kHz (b) and can operate with voltages from +10 to +15 V dc. Transistor Q_1 improves the circuit's signal-to-noise ratio, while audio transformer T_1 drives an 8-ohm load.

MOTOROLA

THE MC145432 APPLICATION CIRCUIT

The purpose of this document is to provide a circuit capable of detecting 2600 Hz tone pulses on a telephone line as defined by the Bell System specification for type-F single-frequency signalling equipment.

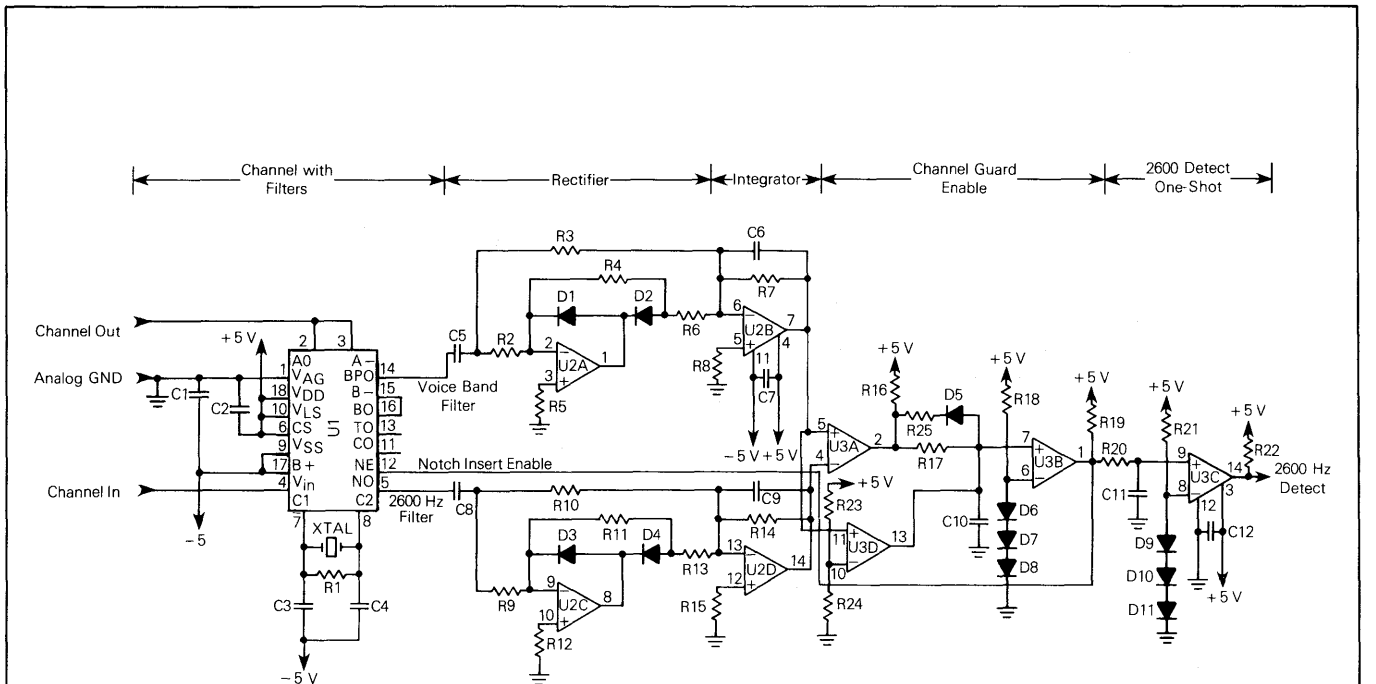
The circuit in Figure 1 is designed to provide a 0 dB gain on the channel, and the overall circuit is set up for a 600 ohm system. The signals presented to the channel are driven through the band-pass filter and out pin 14 of U1 (the MC145432). The signals are also driven through the notch filter and output to pin 5. Both outputs are AC coupled to precision full-wave rectifiers and then averaged by integrators to produce a voltage level that is proportional to in-band energies of each filter.

A three-step decision process is used in determining if a valid 2600 Hz signal is present. The comparator U3A compares the two levels to determine which band has the most energy. If the band-passed signal has the most energy, the first step has been met. The second decision criteria requires the signal level to be at least -26.5 dBm $\pm$ 1.5 dB. This is measured by the comparator U3D by selecting R23 and R24 so that the voltage drop across R24 equals the peak voltage level presented at the input by a -26.5 dBm signal multiplied by the gain of the averaging circuit, which is 0.64. The circuit is presently set up for 600 ohms, so a -26.5 dBm signal is 0.0518 volts peak and the desired voltage drop must be 0.0518×0.64, which is 0.0332 volts. If gain is added at the channel input or the circuit is used in a 900 ohm system, R23 and R24 must be modified to provide the proper comparison level. The final requirement is the signal must be present for 38 milliseconds. This requirement is measured against the averager's speed and the two time constants, R17-C10 and R20-C11.

Bell requires that a notch filter be inserted into the channel if the 2600 Hz tone is present in excess of 13 milliseconds with a 6 millisecond margin. This requirement is met by the R17-C10 time constant. It takes about 7.5 milliseconds for C10 to charge past the 2.1 volt threshold presented by D6-D8. Since the averager takes between 0.5 and 11.5 milliseconds (dependent on input tone level) to provide levels usable to make the decision, the overall delay is within 5 milliseconds of 13 milliseconds, which is within specification. When the threshold is met, the comparator U3B goes high and drives U1 pin 12 high, which inserts the notch filter into the channel. Should the signal be lost at anytime during the charge cycle, C10 is discharged through R25, which represents a maximum discharge time of 0.5 milliseconds.

The output signal of U3B represents a delay of about 13 milliseconds and 38 milliseconds are required to meet the Bell standard, so the R20-C11 time-constant provides another 25 millisecond delay. The comparator U3C will go high if the 2600 Hz signal is present in excess of 38 milliseconds, thus the final decision criteria is met at this point.

There are several other factors that must be taken into account. The circuit must be able to respond to a signal in the $+8.5$ dBm to -26.6 dBm range ± 1.5 dB variation in the presence of no more than 65 dBrnC noise. The circuit will detect a -25 dBm signal under these conditions, which is within the 1.5 dB spec. Another requirement is the ability to detect a tone that is as much as 15 Hz off frequency; however, this poses no real problem. There is one more factor known as talk-off. Although the Bell specifications does not directly address this problem, it can be difficult to deal with. Talk-off basically is caused by speech energy on an active phone line exceeding the tone energy and thus prematurely terminating the signal. There presently is enough protection to avert talk-off when voice signals reach 10 dB higher than the tone levels, but this can be augmented by varying R25. Increasing the discharge time means the excess energy in the notch band must remain for a longer period of time and this gives a better margin. However, if too long of a delay is introduced, another phonemena, know as talk-on, becomes a problem. This is when the circuit is energized by the voice energy caused by C10 not bleeding off fast enough. This is a qualitative trade-off left to the designer's judgement. Bell also specifies the detect signal's pulse length based on the length of the input burst but this is beyond the purpose of the circuit and can be easily implemented with some simple logic.



200 Ω	R24	39 kΩ	R17	1 μF	C11
1 kΩ	R4	47 kΩ	R20	4.7 μF	C5, C6, C8, C9
2 kΩ	R3, R7	62 kΩ	R25	IN914	D1-D11
5.1 kΩ	R8, R15, R16, R19, R22	10 MΩ	R1	U1	MC145432
10 kΩ	R5, R6, R12, R13, R18, R21	20 pF	C3, C4	U2	MC3403
20 kΩ	R2, R9, R10, R11, R14	0.01 μF	C1, C2, C7, C12	U3	LM339A
30 kΩ	R23	0.47 μF	C10	XTAL	3.579 MHz

FIGURE 1 — 2600 Hz Guard and Channel Circuit

FIGURE 2 — MC145432 Block Diagram

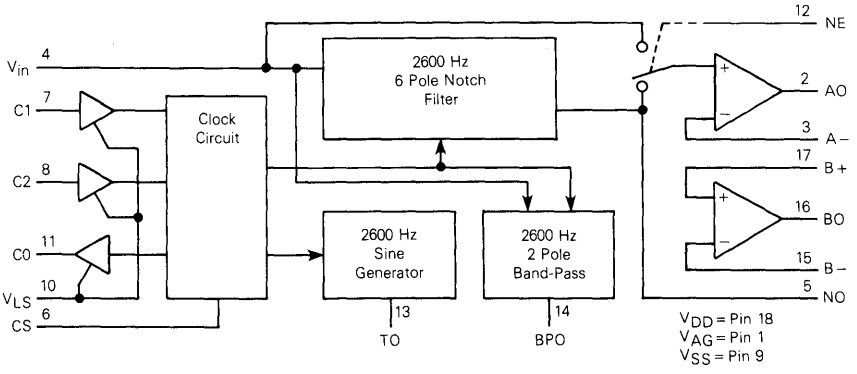


FIGURE 3 — Band-Pass Frequency Response

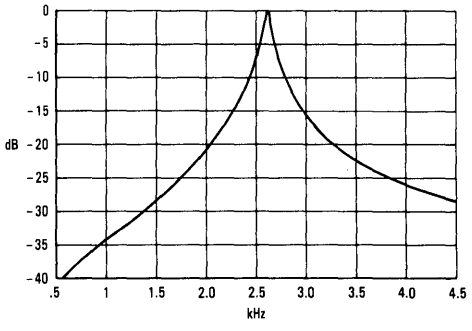
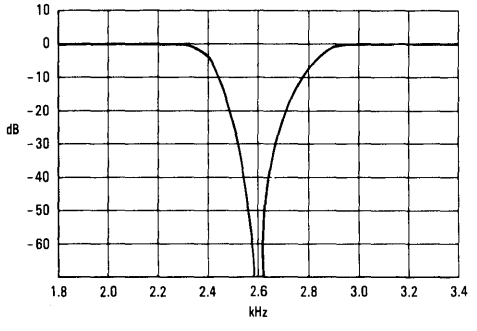


FIGURE 4 — Notch Frequency Response



Digitally control filter gain, cutoff

Earle West and **Henry Wurzburg**
Motorola Inc, Austin, TX

In addition to its intended application as a PCM channel filter, you can use the MC14414-2 dual switched-capacitor filter as a digitally controlled, 10th-order elliptic low-pass filter. Connected as shown in the **figure,** this device exhibits a passband ripple less than 0.6 dB p-p, a pass/stopband transition ratio of 1.5:1 and a stopband rejection level of more than 60 dB.

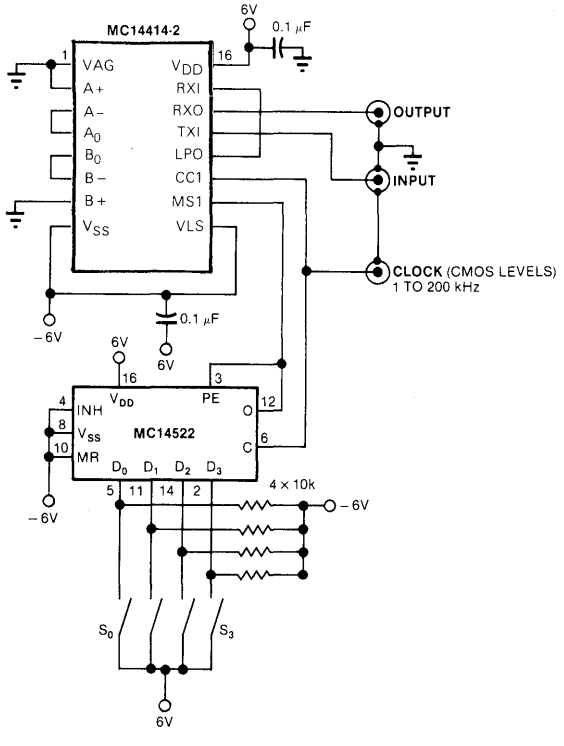
You set the filter's gain between 0 and 18 dB via switches S_0 through S_3. This action controls a divide-by-N counter's output frequency and therefore the switched-capacitor filter's sampling rate by changing the ratio between the filter's CCI and MSI inputs. (Note that the MC14522 is a BCD-controlled counter; if your application requires straight-binary control, use the MC14526B.)

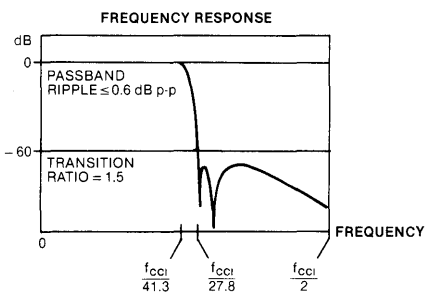
The filter's break (cutoff) frequency is also a function of the input clock's frequency. Set this characteristic by calculating

$$f_{BREAK}=f_{CCI}/41.3.$$

Thus, for the spec'd 1- to 200-kHz f_{CCI} span, you can achieve a break-frequency range of 21 Hz to 4.842 kHz. But keep in mind that because this is a switching filter, you must band-limit the input's spectrum to $0.97f_{CCI}$ to preclude signal aliasing. **EDN**

3





S_3	S_2	S_1	S_0	÷N	GAIN
0	0	0	0	*	18 dB
0	0	0	1	1	18 dB
0	0	1	0	2	18 dB
0	0	1	1	3	14.5 dB
0	1	0	0	4	12.0 dB
0	1	0	1	5	10.1 dB
0	1	1	0	6	8.5 dB
0	1	1	1	7	7.18 dB
1	0	0	0	8	6 dB
1	0	0	1	9	5.0 dB
1	0	1	0	10	4.1 dB
1	0	1	1	11	3.25 dB
1	1	0	0	12	2.5 dB
1	1	0	1	13	1.8 dB
1	1	1	0	14	1.16 dB
1	1	1	1	15	0.56 dB

*INVALID ÷N INPUT

A switched-capacitor filter provides *a gain- and frequency-adjustable 10th-order elliptic low-pass characteristic when its sampling and clock rates are varied. Switches S_0 through S_3 set the gain—via a counter—by controlling the sampling rate. The filter's cutoff frequency is related to the clock's frequency.*

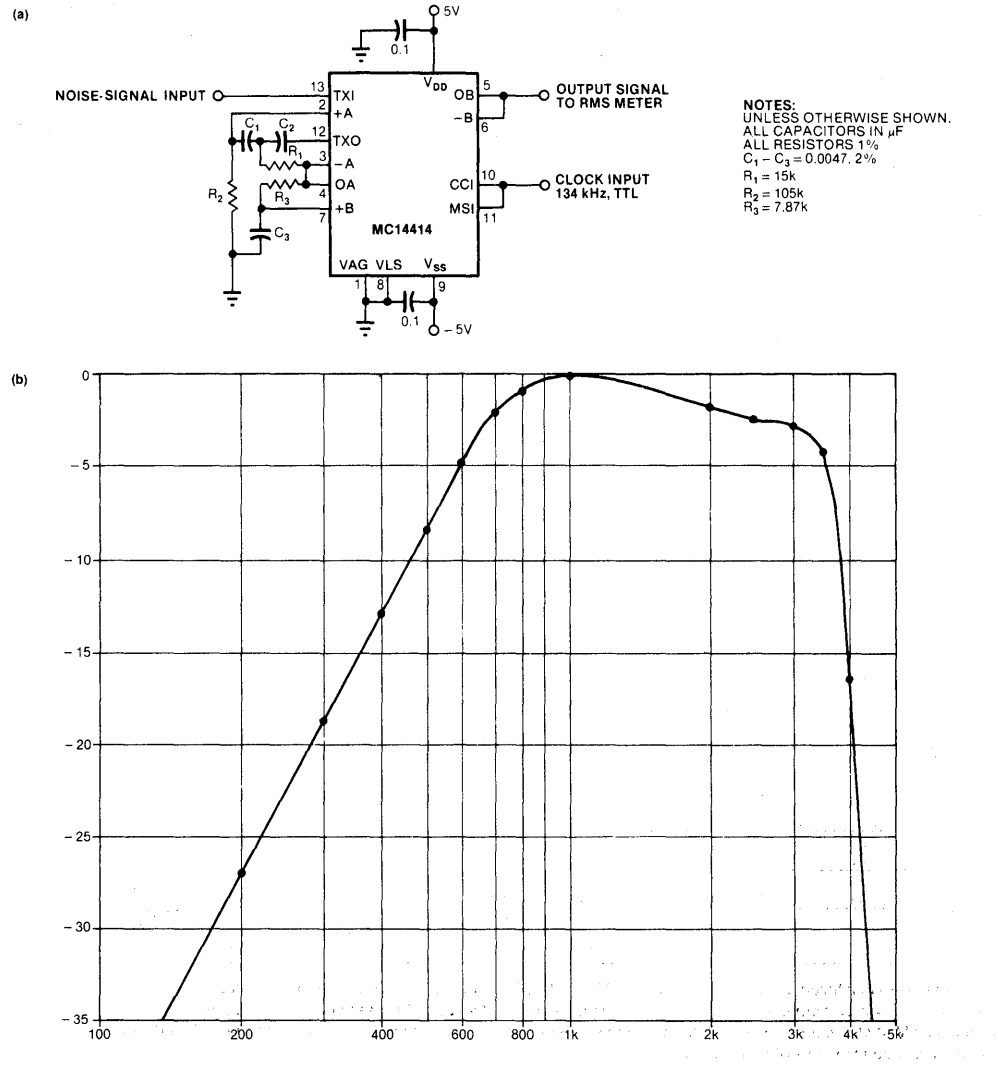
One IC conditions signals

Steve Kelley and **Henry Wurzburg**
Motorola Inc, Austin, TX

When making signal-to-noise-ratio, harmonic-distortion and idle-channel-noise measurements on a telephone voice channel, you can use a filter to weigh the noise spectrum before measuring its value. In US systems, such an arrangement is commonly termed a C Message filter.

You can closely approximate this filter's characteristics by employing the circuit shown in the **figure.** The MC14414—a switched-capacitor filter IC—provides the 5-pole elliptic low-pass function that meets a C Message filter's sharp high-frequency-rolloff requirements. One of the IC's two uncommitted op amps serves as a Sallen Key active filter, the other as the output filter's (R_3C_3) buffer.

The filter's output can directly drive a 1-kΩ load. Output noise equals 11 dBrn$_c$. **EDN**



Telephony signal conditioning *is a snap with this switched-capacitor filter IC* ***(a).*** *Meeting C Message standards, the circuit allows you to measure a voice channel's signal-to-noise ratio, harmonic distortion and idle-channel noise. A 5-pole elliptic characteristic* ***(b)*** *rolls off sharply above 4 kHz.*

IC trio simplifies speech synthesis

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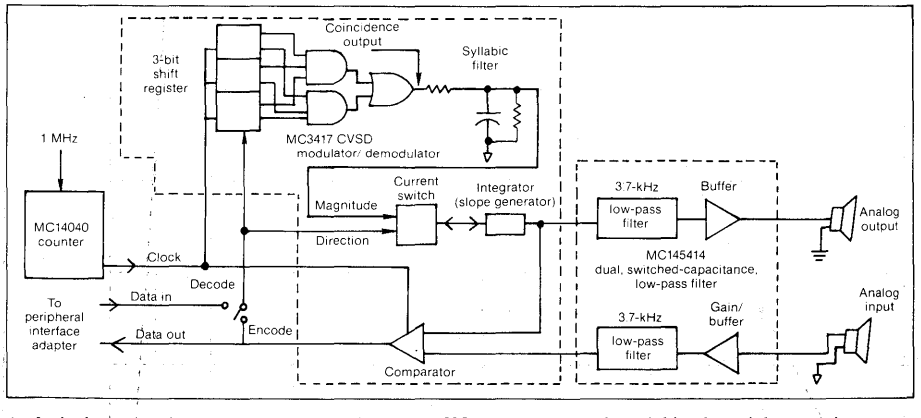
Despite the emergence of special-purpose speech chips, the details of adding voice output to a system are still foreign to most designers. However, they should be happy to learn that highly intelligible speech is possible using a low-cost microprocessor and three readily available integrated circuits.

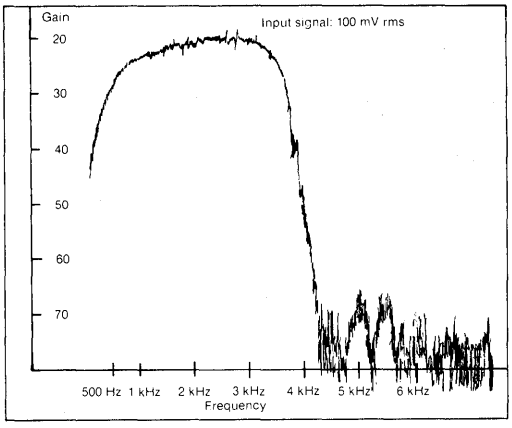
The speech peripheral, which contains an MC3417 continuously variable-slope delta modulator-demodulator, an MC145414 tunable, dual switched-capacitor, low-pass filter, and an MC14040 counter, encodes analog signals into a serial bit stream at a rate of 15,625 bits/s (Fig. 1). The bit stream is then stored in CPU memory. On demand, the peripheral will reproduce an analog signal well enough to be understood easily by an untrained listener.

Such a speech peripheral will enhance the I/O capability of industrial systems, consumer service systems, and games tremendously. Although more CPU memory is required than for linear predictive coding, stored words are easily changed than with LPC. Furthermore, no special memories or complicated calculations are required and no special-purpose synthesizer chips are needed. The encoded speech signals are simply recorded into and played out of CPU memory as any other data. Even the software is simple: words can be packed into ROM or a disk and need only be selected by the microprocessor software for output.

Since the three-IC circuit is designed for speech applications, the bandwidth ranges from 500 Hz to 3.7 kHz (Fig. 2). However, different filter time constants, data rates, and integrator designs can change the frequency range and with it the circuit's



1. At the heart of a three-chip speech peripheral is an MC3417 continuously variable-slope delta modulator-demodulator, which converts an audio waveform into a serial bit stream. The second and newest of the three is an MC145414 dual switched-capacitor low-pass filter with on-board operational amplifiers. An MC14040 12-bit binary counter completes the trio.

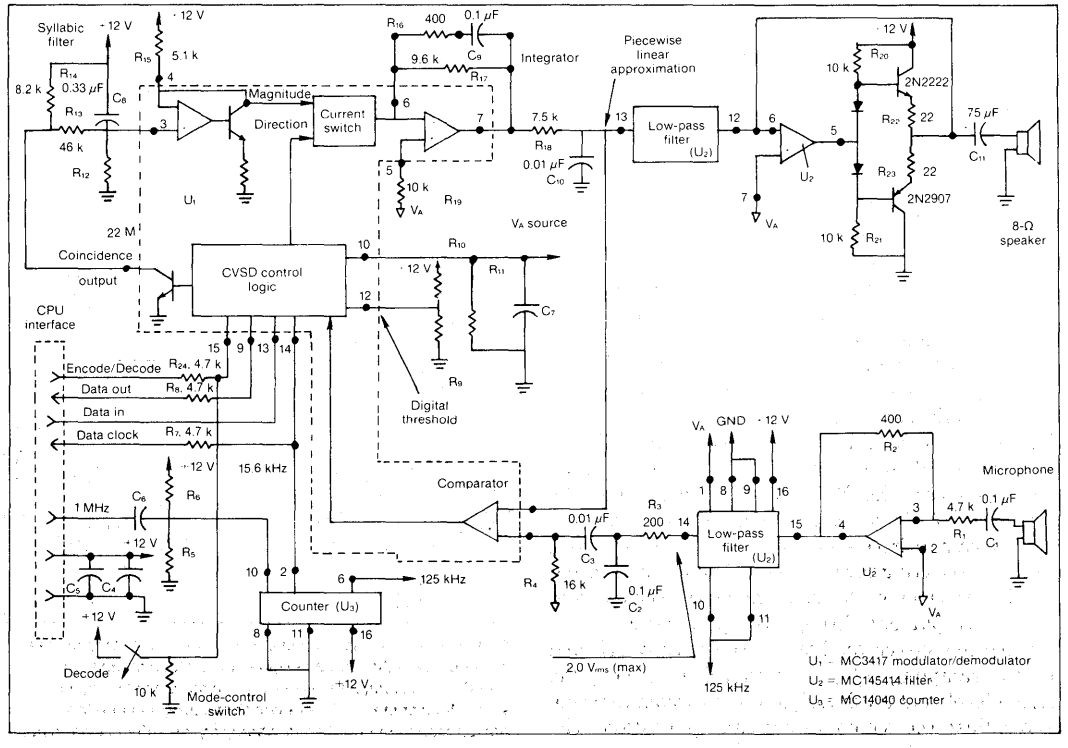


2. The switched-capacitor low-pass filter limits both input and output frequencies to about 3.7 kHz, as reflected by the system frequency response curve. Input frequencies are limited to prevent aliasing; filtering the output smooths it out. Bandwidth for the circuit ranges from 500 Hz to 3.7 kHz.

application. The tradeoffs made for this circuit make it suitable for many industrial applications as well.

About the key chip

Of the three ICs, the key one is the CVSD modulator-demodulator. On board, a current-controlled integrator generates a ramped voltage to linearly approximate the encoded analog waveform in piecewise fashion. Whenever the ramped voltage becomes greater than the input voltage, an on-board comparator switches the direction of the ramp. Digitally, an increasing slope is represented by a 1; a decreasing slope, by a 0. This process is called delta modulation because the slopes change, or delta, is detected. However, the MC3417 does more than simple delta modulation; it performs what is called continuously variable-slope delta modulation (and demodulation). Thus the slope of the ramp voltage —that is, the gain of the chip's integrator—is infinitely variable. This way, in tracking the analog input voltage, the output slope can change more quickly when changes in the analog input demand it. As a result, tracking is more accurate than with any constant-slope delta modulation scheme.



3. A continuously variable slope gives the MC3417 the accuracy to reproduce analog signals. When necessary, the syllabic filter changes the rate of integration and with it the slope. The three basic chips, a simple audio amplifier, and a microprocessor interface complete the speech peripheral circuit.

The MC145414 contains two filters and two operational amplifiers. One filter provides anti-aliasing by cutting off input frequencies above 3.7 kHz. It has a gain of 18 dB. The other filter smooths output noise, but has no inherent gain. One of the chip's on-board operational amplifiers augments the signal from a microphone to about 1 V rms to drive the MC3417's comparator input. At the output, a second op amp and several discrete components drive an 8-Ω speaker.

The MC145414 uses switched-capacitor filters, which need no precise external components for accurate, low-pass analog filtering. Both filters are five-pole, elliptic, low-pass types whose cutoff frequency depends on the sampling clock frequency.

For producing speech, the break frequency (3.7 kHz) requires a 125-kHz clock. The clock is generated by the third IC, a CMOS MC14040 divider, and a 1-MHz master clock derived from the CPU. The three ICs interface with a CPU system, in this case, through an MC6821 peripheral interface adapter (PIA).

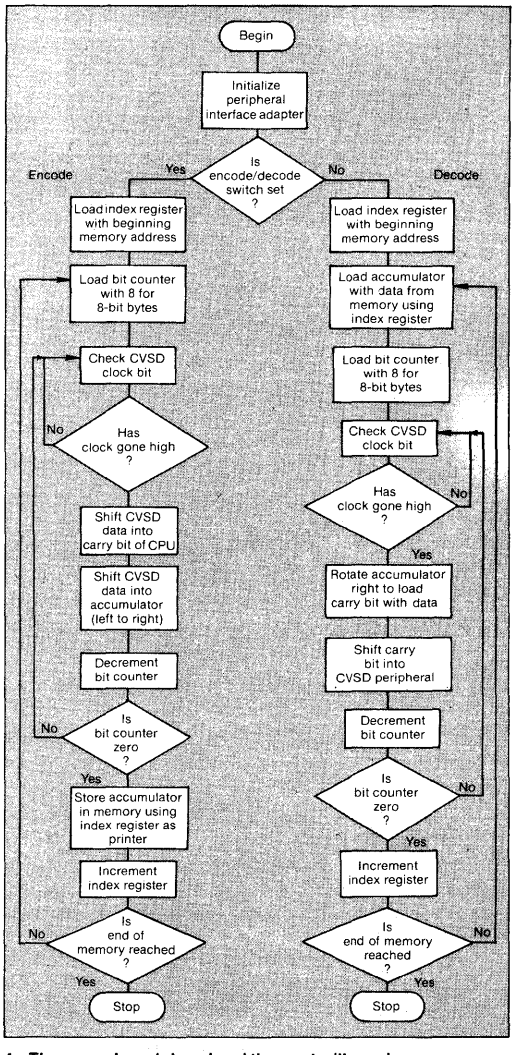
Figure 3 details the entire speech circuit and its two functions: encoding the analog signal into a serial bit stream for the CPU to record and decoding the bit stream into a reconstructed analog waveform. Switch S_1 determines which function to perform by supplying a corresponding level to both the CPU and the CVSD chip.

When switched to encode, analog signals from the microphone are amplified and filtered by one of the op amps and a low-pass filter on board the MC145414. The filtered audio is then fed to the MC3417, where the analog-to-digital conversion produces the serial bit stream. Each high bit means the integrator slope is positive, and each low signals a negative slope. Later, the stored bits are used to control the integrator, whose output approximates the audio signal. In this way, the integrator uses straight lines to reconstruct the original analog waveform.

Thus, when the circuit is set to decode—that is, to output speech—the sequence of bits that translates the serial bit stream into a linear approximation of the original audio is fed to the MC3417, which sends it to the second low-pass filter and op amp on board the MC145414 to smooth out the sequence of linear approximations and provide enough gain to drive a loud-speaker. As a result, with the CPU selecting the sequence of bits (representing words) previously stored in memory, spoken sentences are put out through the peripheral.

Since the speech quality is dramatically affected by the sampling rate, the feedback loop gain, the signal level, and the filtering, there is room to tweak and adjust the sound to suit an application. The circuit represents several tradeoffs to produce highly intelligible speech using a reasonable amount of CPU memory for speech storage, yet requires reasonably few readily available parts.

For example, the transfer function in this application has two poles—one at 160 Hz and one at 280 Hz—and a zero at 4.0 kHz. The pole at 160 Hz provides the long time constant necessary for following relatively linear portions of the original analog



4. The speech peripheral and the controlling microprocessor communicate through a peripheral interface adapter. In addition, clocking and serializing are software tasks, but since the transfer of data between the program and the peripheral is asynchronous, changing the software does not create a timing problem.

```
00001                   ********** MC6800 SPEECH PERIPHERAL DRIVER **********
00002                   *         FOR MC145414 / MC3417 PERIPHERAL CIRCUIT.
00003                   *
00004                   * A PROGRAM TO RECORD AND PLAY SERIAL CVSD DATA.
00005                   *
00006                   * ENTER STARTING MEMORY LOCATION FOR DATA STORAGE
00007                   *  AT LOCATIONS $A000 - $A001.
00008                   *
00009                   * ENTER ENDING MEMORY LOCATIONS FOR DATA STORAGE
00010                   *  AT LOCATIONS $A002 - $A003.
00011                   *
00012                   * PIA IS LOCATED AT ADDRESSES $8004 - $8007.
00013                   *   PIA PB7, PIN 17 IS DATA FROM MC3417 PIN 9.
00014                   *   PIA PB4, PIN 14 IS LEVEL FROM ENCODE/DECODE
00015                   *              SWITCH (ENCODE = "1").
00016                   *   PIA PB0, PIN 10 IS DATA TO MC3417 PIN 13.
00017                   *   PIA PB1, PIN 18 IS DATA CLOCK FROM MC14040 PIN 2
00018                   *   PIA PIN 25 IS 1.0000 MHZ CLOCK TO MC14040 PIN 10
00019                   *   PIA PIN 20 IS +5.0 VOLTS.
00020                   *   PIA PIN 1 IS GROUND.
00021                   *
00022                   *
00023  8004     PIAA    EQU   $8004
00024  8005     PIACRA  EQU   $8005
00025  8006     PIAB    EQU   $8006
00026  8007     PIACRB  EQU   $8007
00027                   *
00028  A000     DATSRT  EQU   $A000
00029  A002     DATEND  EQU   $A002
00030  A004     COUNTR  EQU   $A004
00031                   *
00032                   *
00033                   ***************************************INITIALIZE PIA
C000                    ORG   $C000
C000 C600       LDA B   #$00            ACCESS DATA DIRECTION REG.
C002 F78007     STA B   PIACRB
C005 C601       LDA B   #$01            BIT FOR OUTPUT.
C007 F78006     STA B   PIAB
C00A C637       LDA B   #$37            CB1 INTERRUPT ACTIVE GOING HI
C00C F78007     STA B   PIACRB
00041                   *
00042                   *
00043                   ***************************DETERMINE WHICH FUNCTION FROM SWITCH
C00F C610       LDA B   #$10            SET MASK FOR ENCODE.
C011 F58006     AND A   PIAB            LOOKS FOR ENCODE SWITCH SET.
C014 2703       BEQ     DECODE          BRANCH TO APPROPRIATE ROUTINE
00047                   *
00048                   ***************************************ENCODE ROUTINE
00049                   *
C017 FEA000     ENCODE LDX    DATSRT    SET STARTING ADDRESS.
C01A C608       BYTLP1 LDA B  #$08      SET UP BIT COUNTER.
C01C F78004     STA B  COUNTR
C01F F68004     BITGR1 LDA B  PIACRB     CHECK FOR CLOCK TRANSITION.
C022 5909               ROL B
C024 24F9               BCC   BITLP1    GO BACK FOR CLOCK.
C026 7980 04            ROL   PIAB      SHIFT CODE TO CARRY.
C029 46                 ROR A           SHIFT CARRY TO ACCUMULATOR.
C02A 7A8004             DEC   COUNTR     DECREMENT BIT COUNTER.
C02D 26F1               BNE   BITLP1
C02F A700               STA A 0,X       PUT BYTE IN MEMORY.
C031 08                 INX             POINT TO NEXT BYTE.
C032 FCA002             CPX   DATEND    CHECK FOR END OF MEMORY BLOCK
C035 26E4               BNE   BYTLP1
C037 3F                 SWI
00062                   *
00063                   *
00064                   ***************************************DECODE ROUTINE
00065                   *
C038 FEA000     DECODE LDX    DATSRT    GET STARTING ADDRESS.
C03B C608       BYTLP2 LDA B  #$08      SET UP BIT COUNTER.
C03D F78004            STA B  COUNTR
C040 A600              LDA A  0,X       GET A BYTE FROM MEMORY.
C042 F68007     BITLP2 LDA B  PIACRB     CHECK FOR CLOCK TRANSITION.
C045 5909              ROL B
C047 24F9              BCC    BITLP2
C049 46                ROR A            ROLL DATA INTO CARRY BIT.
C04A 7980 06           ROL    PIAB      ROLL CARRY BIT OUT
C04D 7A8004            DEC    COUNTR
C050 26F1              BNE    BITLP2
C052 08                INX              POINT TO NEXT BYTE.
C053 FCA002            CPX    DATEND    CHECK FOR END OF MEMORY BLOCK
C056 26E4              BNE    BYTLP2
C058 3F                SWI
0000                    END

TOTAL ERRORS 00000
```

5. Conspicuous by its small size, the program for running the speech peripheral circuit performs both encoding and decoding functions in 84 lines, including comments. The routine "reads" the encoding-decoding switch position and branches to the corresponding routine.

waveform; the pole at 280 Hz prevents instantaneous reversals of the integrator's output voltage. The latter action avoids a sawtoothlike peak at extreme values of the audio sine wave, which enables the output to follow rapid changes in the audio waveform more closely.

Finally, the zero at 4.0 kHz improves the phase margin of the MC3417's feedback loop. In a simple delta modulation-demodulation system, the slope of the output signal used to approximate the input is constant. Acceptable speech quality, however, calls for a continuously variable slope—one that increases or decreases with the input. The MC3417 performs continuously variable slope modulation and demodulation so that the slope of the approximating line segments depends on the last three bits clocked into the decoder.

To do that, the MC3417's internal 3-bit shift register monitors the serial bit stream of the comparator. If the comparator detects a series of three or more 1s or three or more 0s in a row, its coincidence pin will go active and the slope of the integrator's output line segments will be made slightly steeper. If three or more consecutive 1s or 0s are detected, a capacitor off the chip will charge up, and the control current of the integrator will be increased continuously.

When the stream of all 1s or all 0s ends, the capacitor is discharged by an external resistor (R_{17}), which, with capacitor C_9, forms a so-called syllabic filter. (Incidentally, the values of R and C are not critical and in this application, the time constant provided by the pair is 50 ms.)

Simple software

As Fig. 4 indicates, the software to record and play speech using this peripheral is simple. The assembly listing for an MC6800 system is given in Fig. 5. In this case, a switch on the CPU board selects the encoding or decoding by setting a high or low level, respectively, at pin 14 of the PIA and pin 15 of the CVSD chip. The encoding routine reads bits serially from the peripheral, performs serial-to-parallel conversion, and saves the encoded data in memory. The program operates asynchronously with the peripheral, allowing different clock rates without changing the software. The CPU simply waits for a data clock edge, then reads the data. The decoding routine works in the same way. The CPU waits for a data clock edge, then sends a bit from memory to the peripheral, which converts it into speech.□

Turn I/O data port into speech port

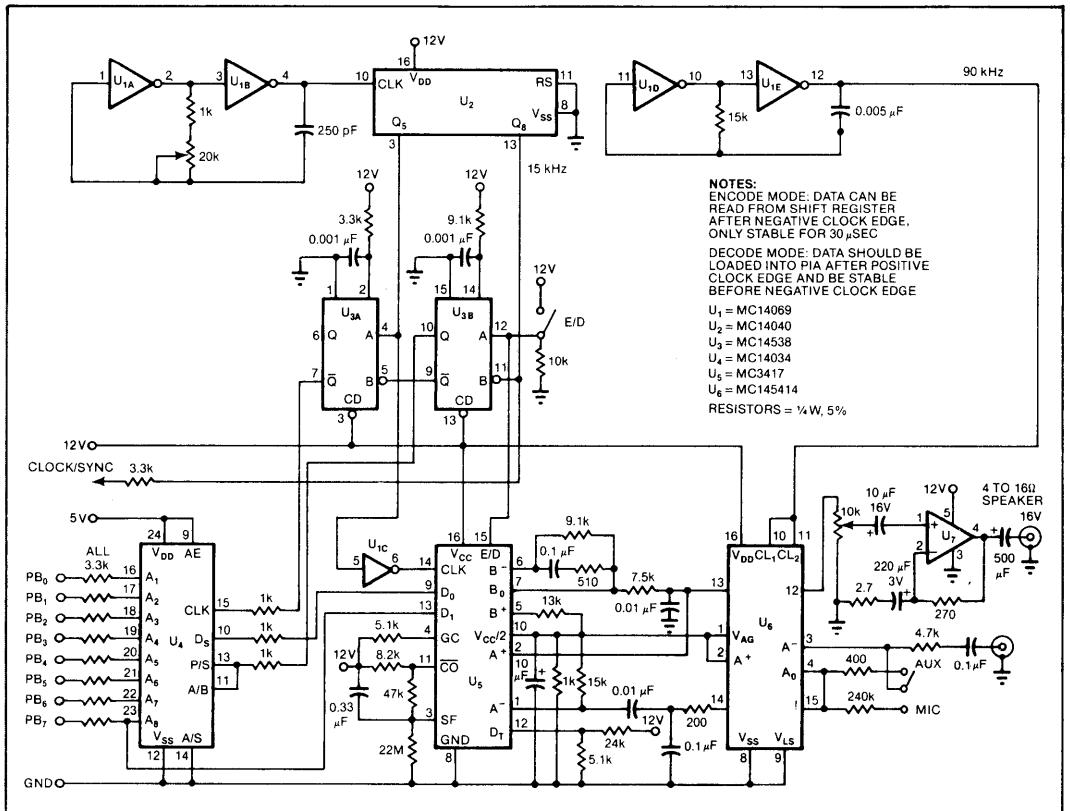
Earle West and **Al Mouton**
Motorola Inc, Austin, TX

This low-cost, low-power μP peripheral circuit (**figure**) converts an 8-bit I/O data port into a high-quality speech port, using continuously variable slope-delta (CVSD) modulation to encode and decode waveforms per μP direction. The μP can play back any segment of recorded speech; 1 sec of intelligible speech requires ~1.5k bytes of memory. You can trade off between voice quality and memory-storage requirements by adjusting the data-clock rate for the CVSD chip.

To encode speech, an MC145414 CMOS dual switched-capacitor filter/dual op amp (U_6) buffers the signal and band-limits the input to ~2.9 kHz. U_5, an MC3417 linear CVSD modulator/demodulator, encodes the CVSD word and creates a bit stream at ~12k bps. This serial bit stream loads into U_4, where the μP reads it in parallel.

For decoding and outputting speech, the μP loads the MC14014 8-bit shift register (U_4) with parallel data. U_4 shifts the data to U_5 for CVSD decoding. U_6 performs low-pass filtering and buffers the resultant voice waveform.

CMOS ICs U_1, U_2 and U_3 clock the filter and CVSD chips, and U_7 drives a loudspeaker. Four control lines connect with the μP to control data direction and synchronize data clocking. **EDN**



This 8-bit speech circuit *encodes and decodes analog waveforms. Adjust the data-clock rate to trade off between voice quality and memory overhead.*

Glossary 4

Glossary of Terms and Abbreviations

The list reproduced here refers to terms found in this and other Motorola publications concerned with Motorola Semiconductor products for Telecommunications.

A law — An European companding/encoding law commonly used in PCM systems.

A/B signaling — A special case of 8th-bit (LSB) signaling in a μ-law system that allows four logic states to be multiplexed with voice on PCM channels.

A/D (analog-to-digital) converter (ADC) — A converter that uniquely represents all analog input values within a specified total input range by a limited number of digital output codes, each of them exclusively representing a fractional part of the total analog input range.

Aliasing noise — A distortion component that is created when frequencies present in a sampled signal are greater than one-half the sample rate.

Answer back — A signal sent by receiving data-processing device in response to a request from a transmitting device, indicating that the receiver is ready to accept or has received data.

Anti-aliasing filter — A filter (normally low pass) that band limits an input signal *before* sampling to prevent aliasing noise.

Asynchronous — A mode of data transmission in which the time occurrence of the bits within each character or block of characters relates to a fixed time frame, but the start of each character or block of characters is not related to this fixed time frame.

Attenuation — A decrease in magnitude of a communication signal.

Bandwidth — The information-carrying frequencies between the limiting frequencies of a communication line or channel.

Baseband — The frequency band occupied by information-bearing signals before combining with a carrier in the modulation process.

Baud — A unit of signaling speed equal to the number of discrete signal conditions or events per second. This refers to the physical symbols/second used within a transmission channel.

Bit rate — The speed at which data bits are transmitted over a communication path, usually expressed in bits per second. A 9600 bps terminal is a 2400 baud system with 4 bits/baud.

Blocking — A condition in a switching system in which no paths or circuits are available to establish a connection to the called party even though it is not busy, resulting in a busy tone to the calling party.

BORS(C)HT — Battery, Overvoltage, Ringing, Supervision, (Codec), Hybrid, Test; the functions performed by a subscriber line card in a telephone exchange.

Broadband — A transmission facility whose bandwidth is greater than that available on voice-grade facilities. (Also called wide band.)

C message — A frequency weighting that evaluates the effects of noise based on its annoyance to the "typical" subscriber of standard telephone service or the effects of noise (background and impulse) on voice-grade data service.

Carrier — An analog signal of fixed amplitude and frequency that combines with an information-bearing signal by modulation to produce an output signal suitable for transmission.

CCITT — Consultative Committee for International Telephone and Telegraph; an international standards group of the European International Telecommunications Union.

Central Office (CO) — A main telephone office, usually within a few miles of a subscriber, that houses switching gear; commonly capable of handling about 10,000 subscribers.

Channel bank — Communication equipment commonly used for multiplexing voice-grade channels into a digital transmission signal (typically 24 channels in the U.S. and 30 channels in Europe).

Circuit, two-wire — A circuit with two conductors providing a "go" and "return" channels.

Circuit, four-wire — A circuit with two pairs of conductors, one pair for the "go" channel and one pair for the "return" channel.

CODEC — COder-DECoder; the A/D and D/A function on a subscriber line card in a telephone exchange.

COFIDEC — COder-FIlter-DECoder; the combination of a codec, the associated filtering, and voltage references required to code and decode voice in a subscriber line card.

Common mode rejection — The ability of a device having a balanced input to reject a voltage applied simultaneously to both differential-input terminals.

Companding — The process in which dynamic range compression of a signal is followed by expansion in accordance with a given transfer characteristic (companding law) which is usually logarithmic.

Compandor — A combination of a compressor at one point in a communication path for reducing the amplitude range of signals, followed by an expander at another point for restoring the original amplitude range, usually to improve the signal-to-noise ratio.

Conference call — A call between three or more stations, in which each station can carry on a conversation simultaneously.

Crosspoint — The operating contacts or other low-impedance-path connection over which conversations can be routed.

Crosstalk — The undesired transfer of energy from one signal path to another.

CTS — Clear to send; a control signal between a modem and a controller used to initiate data transmission over a communication line.

CVSD — Continuous Variable Slope Delta (modulation); a simple technique for converting an analog signal (like voice) into a serial bit stream.

D3 — D3 channel bank; a specific generation of AT&T 24-channel PCM terminal that multiplexes 24 voice channels into a 1.544 MHz digital bit stream. The specifications associated with D3 channel banks are the basis for all PCM device specifications.

D/A (digital-to-analog) converter (DAC) — A converter that represents a limited number of different digital input codes by a corresponding number of discrete analog output values.

Data compression — A technique that provides for the transmission of fewer data bits than originally required without information loss. The receiving location expands the received data bits into the original bit sequence.

dB (decibel) — A power or voltage-level measurement unit.

dBm — The decibel signal level level referred to one milliwatt, i.e., 0 dBm = 1 mW.

dBmO — Signal power measured at a point in a standard test tone level at the same point.

i.e., dBmO = dBm − dBr

where dBr is the relative transmission level, or level relative to the point in the system defined as the zero transmission level point.

dBmOp — Relative power expressed in dBmp. (See dBmO and dBmp.)

dBmp — Indicates dBm measurement made with a psophometric weighting filter.

dBrn — Relative signal level expressed in decibels above reference noise, where reference noise is 1 pW. Hence, 0 dBrn = 1 pW = −90 dBm.

dBrnC – Indicates dBrn measurement made with a C-message weighting filter. (These units are most commonly used in the U.S., where psophometric weighting is rarely used.)

dBrnc0 – Noise measured in dBrnc referenced to zero transmission level.

Decoding – A process in which one of a set of reconstructed analog samples is generated from the digital character signal representing a sample.

Delay distortion – Distortion that occurs on communication lines due to the different propagation speeds of signals at different frequencies, measured in microseconds of delay relative to the delay at 1700 Hz. (This type of distortion does not affect voice communication, but can seriously impair data transmission.)

Delta modulation – A simple digital coding technique that produces a serial bit stream corresponding to changes in analog input levels; usually utilized in devices employing continuously variable-slope delta (CVSD) modulation.

Demodulator – A functional section of a modem that converts received analog line signals to digital form.

Digital telephone – A telephone terminal that digitizes a voice signal for transmission and decodes a received digital signal back to a voice signal. (It will usually multiplex 64 kbps voice and separate data inputs at multiples of 8 kbps.)

Distortion – The failure to reproduce an original signal's amplitude, phase, delay, etc. characteristics accurately.

DPSK – Differential Phase Shift Keying; a modulation technique for transmission where the frequency remains constant but phase changes will occur from 90°, 180° and 290° to define the digital information.

DTMF – Dual Tone Multi Frequency (dialing).

Duplex – A mode of operation permitting the simultaneous two-way independent transmission of telegraph or data signals.

Echo – A signal that has been reflected or returned as a result of impedance mismatches, hybrid unbalance, or time delay. Depending upon the location of impedance irregularities and the propagation characteristics of a facility, echo may interfere with the speaker/listener or both.

Echo suppressor – A device used to minimize the effect of echo by blocking the echo return currents; typically a voice-operated gate that allows communication one way at a time.

Encoder (PCM) – A device that performs repeated sampling, compression, and A/D conversion to change an analog signal to a serial stream of PCM samples representing the analog signal.

Equalizer – An electrical network in which phase delay or gain varies with frequency to compensate for an undesired amplitude or phase characteristic in a frequency-dependent transmission line.

FDM – Frequency-Division Multiplex; a process that permits the transmission of two or more signals over a common path by using a different frequency band for each signal.

Frame – A set of consecutive digit time slots in which the position of each digit slot can be identified by reference to a frame alignment. The frame alignment signal does not necessarily occur, in whole or in part, in each frame.

Full duplex – A mode of operation permitting simultaneous transmission of information between two locations in both directions.

Gain – The increase in signal amplitude realized when a signal passes through an amplifier or repeater (normally measured in decibels).

Gain tracking error – The variation of gain from a constant level (determined at 0 dBm input level) when measuring the dependence of gain on signal level by comparing the output signal to the input signal over a range of input signals.

HDLC – High-Level Data Link Control; a CCITT standard data communication line protocol.

Half duplex – A mode of operation permitting transmission of information between two locations in only one direction at a time.

Handset – A rigid assembly providing both telephone transmitter and receiver in a form convenient for holding simultaneously to mouth and ear.

Hookswitch – The switch on a telephone set that is operated by the removal or replacement of the receiver on the hook (defined as off-hook and on-hook conditions, and corresponding to busy and idle circuits).

Idle channel noise (ICN) – The total signal energy measured at the output of a device or channel under test when the input of the device or channel is grounded (often a wideband noise measurement using a C-message weighting filter to band-limit the output noise).

Intermodulation – The modulation of the components of a complex wave by each other (in a nonlinear system).

Intermodulation distortion – An analog line impairment when two frequencies interact to create an erroneous frequency, in turn distorting the data signal repreentation.

ISDN – Integrated Services Digital Network; A future communication network intended to carry digitized voice and data multiplexed onto the public network.

Jitter – A type of analog communication line distortion caused by abrupt, spurious signal variation from a reference timing position, and capable of causing data transmission errors, particularly at high speeds. (The variation can be in amplitude, time, frequency or phase.)

Key system – A miniature PABX that accepts 4 to 10 lines and can direct them to as many as 30 telsets.

μ-law – A companding law accepted as the North American standard for PCM based systems.

LAN – Local Area Network; a data-only communication network between data terminals using a standard interface to the network.

Line – The portion of a circuit external to an apparatus that consists of the conductors connecting the apparatus to the exchange or connecting two exchanges.

Longitudinal balance – The common-mode rejection of a telephone circuit.

Loopback – Directing signals back toward the source at some point along a communication path.

MCU – MicroComputer Unit (also MicroController Unit).

MPU – MicroProcessor Unit.

Mu law – A companding/encoding law commonly used in U.S. (same as μ-law).

MUX – Multiplex or multiplexer.

Modem – MOdulator-DEModulator; a unit that modulates and demodulates digital information from a terminal or computer port to an analog carrier signal for passage over an analog line.

Multiplex – To simultaneously transmit two or more messages on a single channel.

Off hook – The circuit condition resulting when the handset is lifted from the hook switch of the telephone set; i.e., a low dc impedance is placed across the line causing loop current flow that is recognized by a relay at the central office as a request for service.

On hook – The circuit condition resulting when the handset of a telephone is replaced on its cradle (approximately an open circuit).

PABX – Private Automatic Branch Exchange; a customer-owned, switchable telephone system providing internal and/or external station-to-station dialing.

Pair – The two associated conductors that form part of a communication channel.

Pass-band filter – A filter used in communications systems that allows only the frequencies within a communication channel to pass, and rejects all frequencies outside the channel.

PBX – Private Branch Exchange; a class of service in standard Bell System terminology that typically provides the same service as PABX.

PCM – Pulse Code Modulation; a method of transmitting data in which signals are sampled and converted to digital words that are then transmitted serially, typically as 8-bit words.

Phase jitter – Abrupt, spurious variations in an analog line, generally caused by power and communication equipment along the line that shifts the signal phase relationship back and forth.

Propagation delay – The time interval between specified reference points on the input and output voltage waveforms.

Psophometric weighting – A frequency weighting similar to C-Message weighting that is used as the standard for European telephone system testing.

Pulse dialer – A device that generates pulse trains corresponding to digits or characters used in impulse or loop-disconnect dialing.

Quantizing noise – Signal-correlated noise generally associated with the quantizing error introduced by A/D and D/A conversions in digital transmission systems.

RTS – Request to send; an RS-232 control signal between a modem and user's digital equipment that initiates the data transmission sequence on a communication line.

Repeater – An amplifier and associated equipment used in a telephone circuit to process a signal and retransmit it.

Repertory dialer – A dialer that stores a repertory of telephone numbers and dials any one of them automatically on request.

Sampling rate – The frequency at which the amplitude of an analog signal is gated into a coder circuit. The Nyquist sampling theorem states that if a band-limited signal is sampled at regular intervals and at a rate equal to or greater than twice the highest frequency of interest, the sample contains all the information of the original signal. The frequency band of interest in telephony ranges from 300 to 3400 Hz, so a sampling rate of 8 kHz provides dc to 4000 Hz reproduction.

SCU – Subscriber Channel Unit; the circuitry at a telephone exchange associated with an individual subscriber line or channel.

Signaling – The transmission of control or status information between switching systems in the form of dedicated bits or channels of information inserted on trunks with voice data.

Signal-to-distortion ratio (S/D) – The ratio of the input signal level to the level of all components that are present when the input signal (usually a 1.020 kHz sinusoid) is eliminated from the output signal (e.g., by filtering).

SLIC – Subscriber Line Interface Circuit; a device that performs the 2-4 wire conversion, battery feed and other line interface functions on a subscriber telephone line.

Speech network – An electric circuit that connects a transmitter and a receiver to a telephone line or telephone test loop and to each other.

Subscriber line – The permanent connection between a station and the switching center that serves it.

Switchhook – A synonym for hookswitch.

Syn (Sync) – (1) A bit of character used to synchronize a time frame in a time-division multiplexer. (2) A sequence used by a synchronous modem to perform bit synchronization or by a line controller for character synchronization.

Synchronous modem – A modem that uses a derived clocking signal to perform bit synchronization with incoming data.

T1 carrier – A PCM system operating at 1.544 MHz and carrying 24 individual voice-frequency channels.

Tandem trunk – See trunk.

Telephone exchange – A switching center for interconnecting the lines that service a specific area.

TELETEX – A text communication service between entirely electronic work stations that will gradually replace TELEX with the introduction of the digital network. (Not to be confused with teletext.)

TELETEXT – The name usually used for broadcast text (and graphics) for domestic television reception. (Not to be confused with teletex.)

Time-division multiplex – A process that permits the transmission of two or more signals over a common paty by using a different time interval for each signal.

Tip (T) and ring (R) – Terms used to identify the two conductors of a circuit. (These terms originate from switchboard terminology for cord circuits, in which a four-wire circuit is designated T1, T2, and R1 and R2.)

Trunk – A telephone circuit or channel between two central offices or switching entities.

TSAC – Time Slot Assigner Circuit; a circuit that determines when a CODEC will put its 8 bits of data on a PCM bit stream.

TSIC – Time Slot Interchange Circuit; a device that switches digital highways in PCM based switching systems; a "digital" cross-point switch.

Twist – The amplitude ratio of a pair of DTMF tones. (Because of transmission and equipment variations, a pair of tones that originated equal in amplitude may arrive with a considerable difference in amplitude.)

UDLT – Universal Digital Loop Transceiver; a Motorola originated name for a voice/data transceiver circuit.

Voice frequency – A frequency within that part of the audio range that is used for the transmission of speech of commercial quality, i.e. 300-3400 Hz.

Weighting network – A network whose loss varies with frequency in a predetermined manner.

Handling and Design Guidelines

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MOTOROLA

HANDLING AND DESIGN GUIDELINES

HANDLING PRECAUTIONS

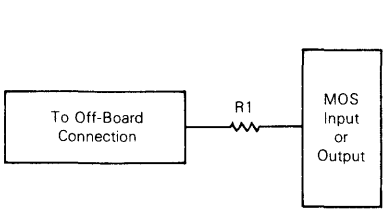
All MOS devices have an insulated gate that is subject to voltage breakdown. The gate oxide for Motorola's devices is about 800 Å thick and breaks down at a gate-source potential of about 100 V. The high-impedance gates on the devices are protected by resistor-diode networks. However, these on-chip networks do not make the IC immune to electrostatic damage (ESD). Laboratory tests show that devices may fail after one very high voltage discharge. They may also fail due to the cumulative effect of several discharges of lower potential.

Static-damaged devices behave in various ways, depending on the severity of the damage. The most severely damaged are the easiest to detect because the input or output has been completely destroyed and is either shorted to V_{DD}, shorted to V_{SS}, or open-circuited. The effect is that the device is no longer functional. Less severe cases are more difficult to detect because they appear as intermittent failures or degraded performance. Another effect of static damage is, often, increased leakage currents.

CMOS and NMOS devices are not immune to large static voltage discharges that can be generated while handling. For example, static voltages generated by a person walking across a waxed floor have been measured in the 4-15 kV range (depending on humidity, surface conditions, etc.). Therefore, the following precautions should be observed.

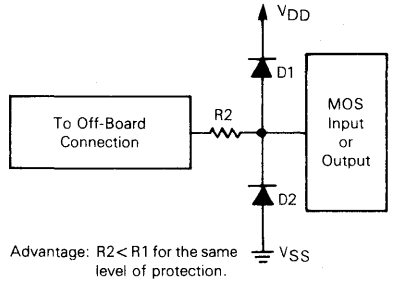
1. Do not exceed the Maximum Ratings specified by the data sheet.
2. All unused device inputs should be connected to V_{DD} or V_{SS}.
3. All low-impedance equipment (pulse generators, etc.) should be connected to CMOS or NMOS inputs only after the device is powered up. Similarly, this type of equipment should be disconnected before power is turned off.
4. A circuit board containing CMOS or NMOS devices is merely an extension of the device and the same handling precautions apply. Contacting edge connectors wired directly to devices can cause damage. Plastic wrapping should be avoided. When external connections to a PC board address pins of CMOS or NMOS integrated circuits, a resistor should be used in series with the inputs or outputs. The limiting factor for the series resistor is the added delay caused by the time constant formed by the series resistor and input capacitance. This resistor will help limit accidental damage if the PC board is removed and brought into contact with static generating materials. For convenience, equations for added propagation delay and rise time effects due to series resistance size are given in Figure 1.
5. All CMOS or NMOS devices should be stored or

FIGURE 1 — NETWORKS FOR MINIMIZING ESD AND REDUCING CMOS LATCH UP SUSCEPTIBILITY



Advantage: Requires minimal board area

Disadvantage: R1 > R2 for the same level of protection, therefore rise and fall times, propagation delays, and output drives are severely affected.



Advantage: R2 < R1 for the same level of protection. Impact on ac and dc characteristics is minimized.

Disadvantage: More board area, higher initial cost

Note: These networks are useful for protecting the following:
A. digital inputs and outputs
B. analog inputs and outputs
C. 3-state outputs
D. bidirectional (I/O) ports

EQUATION 1 — PROPAGATION DELAY vs. SERIES RESISTANCE

$$R \approx \frac{t}{C \cdot k}$$

where:
R = the maximum allowable series resistance in ohms
t = the maximum tolerable propagation delay in seconds
C = the board capacitance plus the driven device's input capacitance in farads
k = 0.33 for the MC145040/1
k = 0.7 for other devices

EQUATION 2 — RISE TIME vs. SERIES RESISTANCE

$$R \approx \frac{t}{C \cdot k}$$

where:
R = the maximum allowable series resistance in ohms
t = the maximum rise time per data sheet in seconds
C = the board capacitance plus the driven device's input capacitance in farads
k = 0.7 for the MC145040/1
k = 2.3 for other devices

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transported in materials that are antistatic. Devices must not be inserted into conventional plastic "snow", styrofoam or plastic trays, but should be left in their original container until ready for use.

6. All CMOS or NMOS devices should be placed on a grounded bench surface and operators should ground themselves prior to handling devices, since a worker can be statically charged with respect to the bench surface. Wrist straps in contact with skin are strongly recommended. See Figure 2.
7. Nylon or other static generating materials should not come in contact with CMOS or NMOS circuits.
8. If automatic handling is being used, high levels of static electricity may be generated by the movement of devices, belts, or boards. Reduce static build-up by using ionized air blowers or room humidifiers. All parts of machines which come into contact with the top, bottom, and sides of IC packages must be grounded metal or other conductive material.
9. Cold chambers using CO_2 for cooling should be equipped with baffles, and devices must be contained on or in conductive material.
10. When lead-straightening or hand-soldering is necessary, provide ground straps for the apparatus used and be sure that soldering ties are grounded.
11. The following steps should be observed during wave solder operations.
    a. The solder pot and conductive conveyor system of the wave soldering machine must be grounded to an earth ground.
    b. The loading and unloading work benches should have conductive tops which are grounded to an earth ground.
    c. Operators must comply with precautions previously explained.
    d. Completed assemblies should be placed in antistatic containers prior to being moved to subsequent stations.
12. The following steps should be observed during board cleaning operation.
    a. Vapor degreasers and baskets must be grounded to an earth ground. Operators must likewise be grounded.
    b. Brush or spray cleaning should not be used.
    c. Assemblies should be placed into the vapor degreaser immediately upon removal from the antistatic container.
    d. Cleaned assemblies should be placed in antistatic containers immediately after removal from the cleaning basket.
    e. High velocity air movement or application of solvents and coatings should be employed only when module circuits are grounded and a static eliminator is directed at the module.
13. The use of static detection meters for line surveillance is highly recommended.
14. Equipment specifications should alert users to the presence of CMOS or NMOS devices and require familiarization with this specification prior to performing any kind of maintenance or replacement of devices or modules.
15. Do not insert or remove CMOS or NMOS devices from test sockets with power applied. Check all power supplies to be used for testing devices to be certain there are no voltage transients present.
16. Double check test equipment setup for proper polarity of voltage before conducting parametric or functional testing.
17. Do not recycle shipping rails. Continuous use causes deterioration of their antistatic coating.

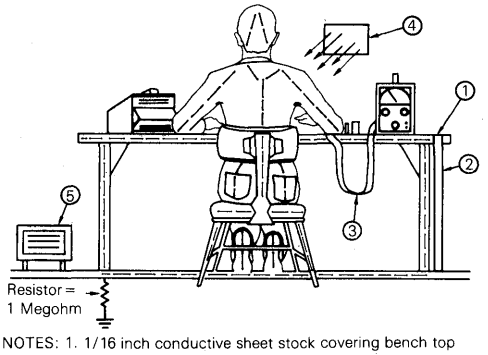
RECOMMENDED FOR READING

"Total Control of the Static in Your Business"

Available by writing to:
Static Control Systems Div.
Box ELB-3, 225-4S
3M Center
St. Paul, MN 55144

Or calling:
1-800-328-1368
1-612-733-9420 (in Minnesota)

FIGURE 2 — TYPICAL MANUFACTURING WORK STATION



NOTES: 1. 1/16 inch conductive sheet stock covering bench top work area.
2. Ground strap.
3. Wrist strap in contact with skin.
4. Static neutralizer. (Ionized air blower directed at work.) Primarily for use in areas where direct grounding is impractical.
5. Room humidifier. Primarily for use in areas where the relative humidity is less than 45%. Caution: building heating and cooling systems usually dry the air causing the relative humidity inside of buildings to be less than outside humidity.

CMOS LATCH UP

Latch up will not be a problem for most designs, but the designer should be aware of it, what causes it, and how to prevent it.

Figure 3 shows the layout of a typical CMOS inverter and Figure 4 shows the parasitic bipolar devices that are formed. The circuit formed by the parasitic transistors and resistors is the basic configuration of a silicon controlled rectifier, or SCR. In the latch-up condition, transistors Q1 and Q2 are turned on, each providing the base current necessary for the other to remain in saturation, thereby latching the devices on. Unlike a conventional SCR, where the device is turned on by applying a voltage to the base of the NPN transistor, the parasitic SCR is turned on by applying a voltage to the emitter of either transistor. The two emitters that trigger the SCR are the same point, the CMOS output. Therefore, to latch up the CMOS device, the output voltage must be greater than V_{DD} + 0.5 Vdc or less than − 0.5 Vdc and have sufficient current to trigger the SCR. The latch-up mechanism is similar for the inputs.

Once a CMOS device is latched up, if the supply current is not limited, the device will be destroyed. Ways to prevent such occurrences are listed below.

1. Insure that inputs and outputs are limited to the maximum rated values, as follows:
   $-0.5 \le V_{in} \le V_{DD} + 0.5$ Vdc referenced to V_{SS}
   $-0.5 \le V_{out} \le V_{DD} + 0.5$ Vdc referenced to V_{SS}
   $|I_{in}| \le 10$ mA
   $|I_{out}| \le 10$ mA when transients or dc levels exceed the supply voltages.
2. If voltage transients of sufficient energy to latch up the device are expected on the outputs, external protection diodes can be used to clamp the voltage. Another method of protection is to use a series resistor to limit the expected worst case current to the Maximum Ratings values. See Figure 1.
3. If voltage transients are expected on the inputs, protection diodes may be used to clamp the voltage or a series resistor may be used to limit the current to a level less than the maximum rating of $I_{in} = 10$ mA. See Figure 1.
4. Sequence power supplies so that the inputs or outputs of CMOS devices are not powered up first (e.g., recessed edge connectors may be used in plug-in board applications and/or series resistors).
5. Power supply lines should be free of excessive noise. Care in board layout and filtering should be used.
6. Limit the available power supply current to the devices that are subject to latch-up conditions. This can be accomplished with the power supply filtering network or with a current-limiting regulator.

FIGURE 3 — CMOS WAFER CROSS SECTION

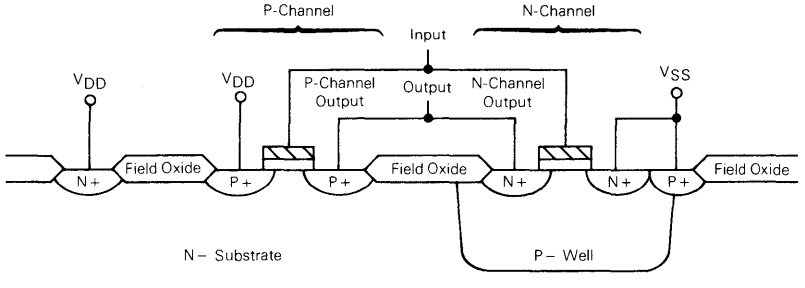
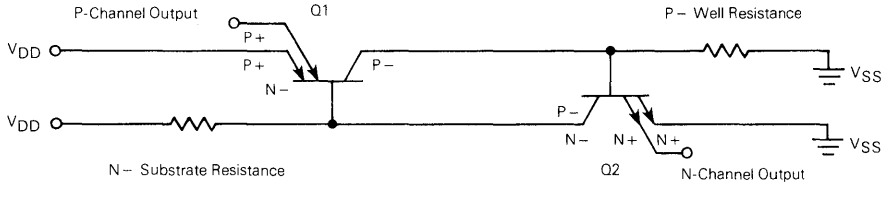


FIGURE 4 — LATCH UP CIRCUIT SCHEMATIC



5

Quality and Reliability 6

MOTOROLA

Introduction

This chapter is intended to demonstrate the quality and reliability aspects of the semiconductor products supplied by Motorola.

Quality in Manufacturing

QUALITY IN DESIGN

Motorola's quality activity starts at the product design stage. It is its philosophy to "design in" reliability. At all development points of any new design reliability orientated guidelines are continuously used to ensure that a thoroughly reliable part is ultimately produced. This is demonstrated by the excellent in-house reliability testing results obtained for all Motorola's semiconductor products and, more importantly, by our numerous customers.

MATERIAL INCOMING CONTROLS

Each vendor is supplied with a copy of the Motorola Procurement Specification which must be agreed in detail between both parties before any purchasing agreement is made. This is followed by a vendor appraisal report whereby each vendor's manufacturing facility is visited by Motorola Quality Engineers responsible for ensuring that the vendor has a well organized and adequately controlled manufacturing process capable of supplying the high quality material required to meet the Motorola Incoming Inspection Specification. Large investments have and are continuously being made and Quality Improvement programs developed with our main suppliers concerning:

Masks – Silicon – Piece-parts – Chemical products – Industrial gas, etc.

Each batch of material delivered to Motorola is quarantined at Goods-in until the Incoming Quality Organization has subjected adequate samples to the incoming detailed inspection specification. In the case of masks, this will include mask inspection for:

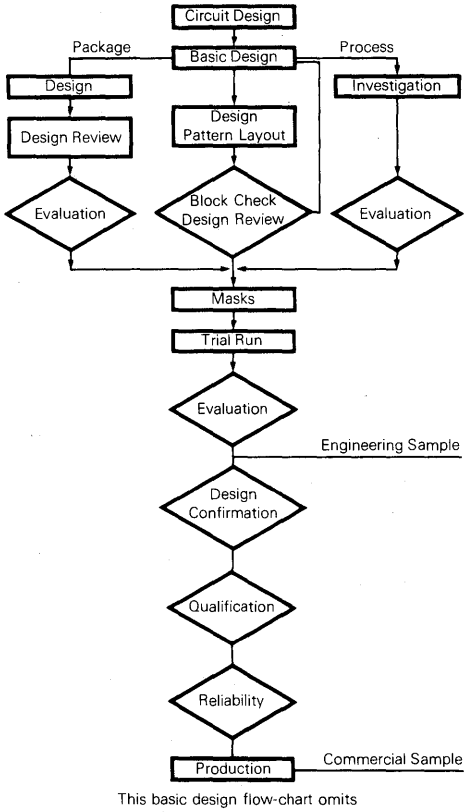
1. Defect Density
2. Intermask Alignment
3. Mask Revision
4. Device to Device Alignment
5. Mask Type

Silicon will undergo the following inspections:

1. Type "N" or "P"
2. Resistivity
3. Resistivity Gradient
4. Defects
5. Physical Dimensions
6. Dislocation Density

Incoming chemicals are also controlled to very rigorous standards. Many are submitted to in-house chemical analysis where the supplier's conformance to specification is meticulously checked. In many cases, line tests are performed before final acceptance. A major issue and responsibility for the Incoming Quality Department is to ensure that the most disciplined safety factors have been employed with regard to chemicals. Chemicals can and are often rejected because safety standards have not been deemed acceptable.

NEW PRODUCT TYPICAL DESIGN FLOW



This basic design flow-chart omits some feedback loops for simplicity

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WAFER FABRICATION

All processing stages of Motorola products are subjected to demanding manufacturing and quality control standards. A philosophy of "Do it Right the First Time" is instrumental in assuring that Motorola has a reliability record second to none.

The Bipolar and MOS Wafer Fabrication flow charts are examples which highlight the various in process control points audited by both Manufacturing and Quality people. The majority of these inspections are control audit points with inspection gates at critical points of the process; this is in line with Motorola policy of all personnel being responsible for quality at each manufacturing stage.

Diffusion and ion implantation processing is subject to oxide thickness controls penetration evaluations. Controls are also performed on resistivity and defect density. Diffusion furnaces, metallization, and passivation equipment are subjected to daily qualification requirements by using C-V plotting techniques. C-V techniques are also used to ensure ongoing stability as they do provide a very sensitive measurement of ionic species concentration.

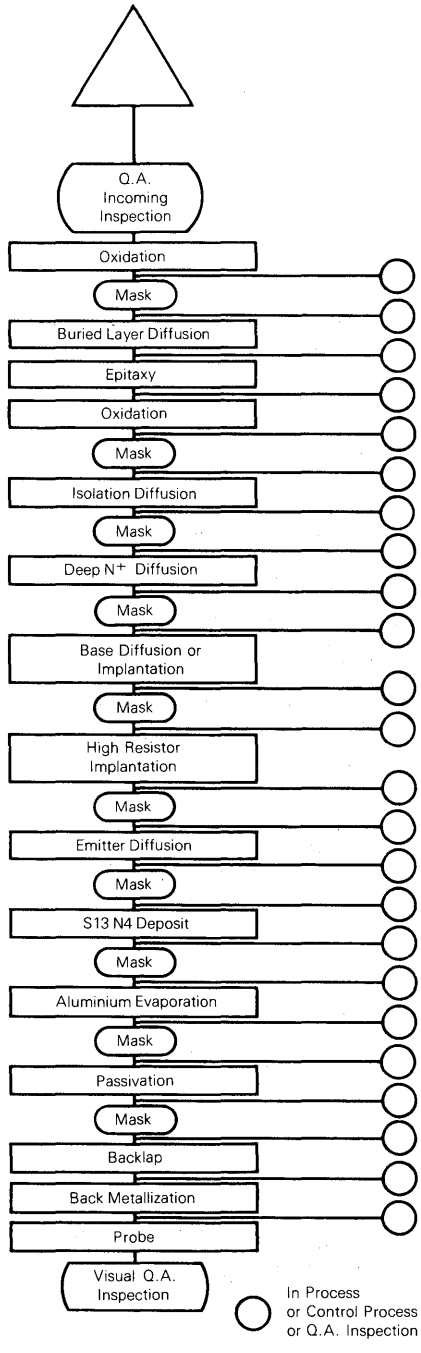
In addition many other specific controls are used as a means to ensure built-in reliability and provide statistical trend data, which include:

- Environmental monitoring for humidity, temperature and particles
- Deionized water resistivity, particles and bacteria checks in water
- Epitaxial material: resistivity — thickness — crystal defects
- Oxide: thickness — charges — pinhole density
- Metallization: thickness — adherence — metal composition — ohmic contacts
- Doping profiles
- Pre and post etch inspections
- In process SEM analysis for step coverage: metallization — grain size — phosphorous concentration
- Passivation integrity checks
- Calibration
- Final visual inspection gate.

After all processing stages are completed, every wafer lot is subject to a detailed electrical parameter check. Parameters such as threshold voltage, junction breakdown voltages, resistivity, field inversion voltages, etc., are measured and each batch is sentenced accordingly. The data generated at this point is treated statistically as a control on the distribution of each key electrical parameter thus allowing corrective action adjustments to be implemented in a timely manner.

Every wafer lot is submitted to an electrical probe test during which every individual die is tested to its electrical specification. Chips which fail are individually inked.

BIPOLAR WAFER FABRICATION



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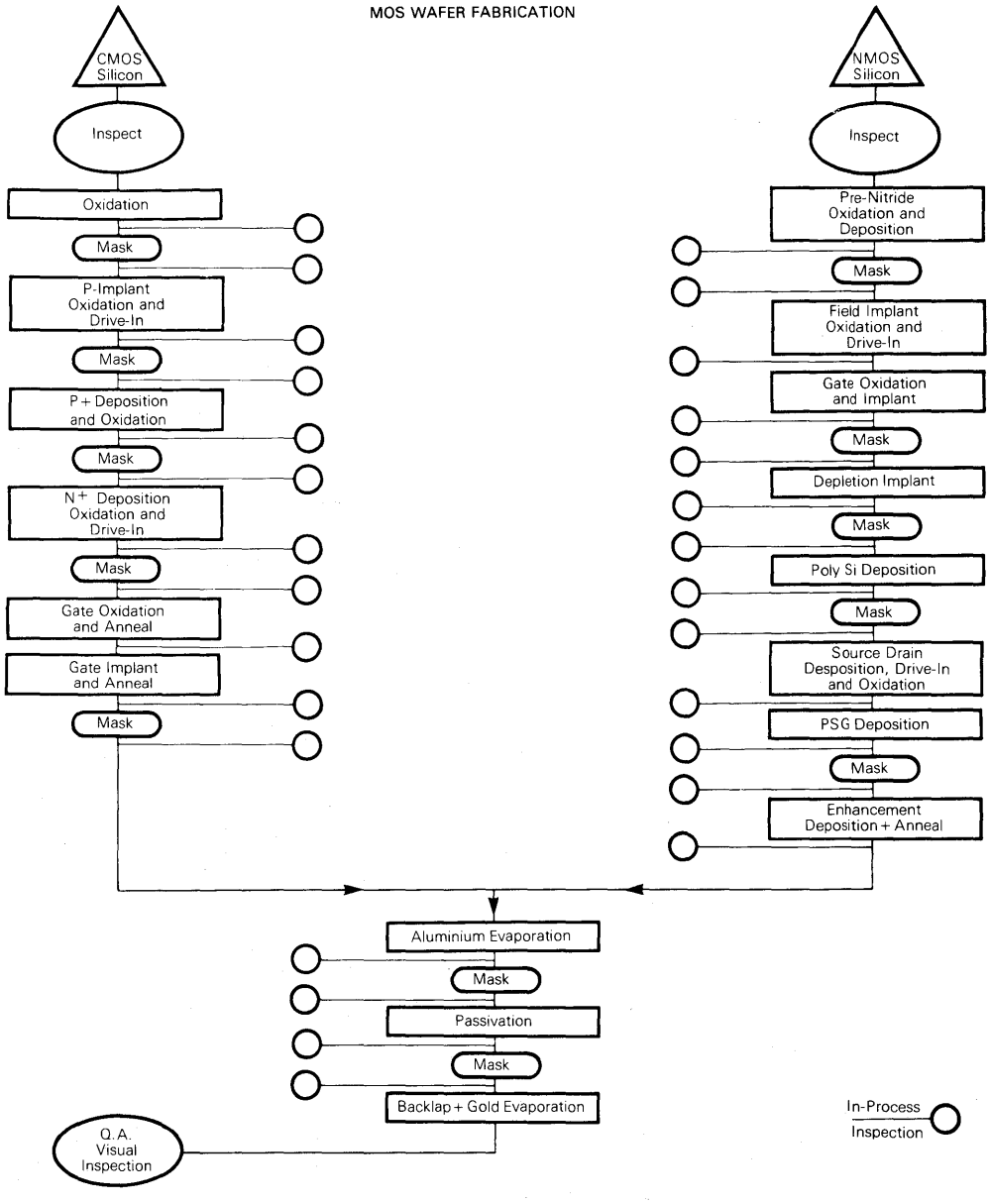


ASSEMBLY

The assembly operation is of equal importance to the wafer fabrication process as a manufacturing activity which will effect the reliability of the finished product. Motorola continuously makes major investments in specialized assembly areas located in Malaysia, the Philippines and Korea. These assembly plants employ the latest technologies available to ensure that all Motorola semiconductors are produced to the highest standards of Quality and Reliability. In addition, each wafer fabrication facility has in-house assembly capability which allows some production, specific engineering activity and qualification of piece-parts suppliers. The major production volumes of Motorola's Integrated Circuits are assembled offshore in the Far East.

identical Quality and Reliability philosophies are practiced in the assembly areas as within the wafer fabrication facilities. Quality Assurance Audits for immediate corrective actions are performed after major process steps as demonstrated in the flow-chart. In addition, screening options are available. The statistical data obtained from quality audits are reported to the appropriate business centers either daily, weekly or monthly for review.

Motorola is particularly aware of the major impact moisture can have on the reliability performance of either plastic or ceramic parts. With this in mind several major new innovations have been introduced to safeguard Motorola products and thus enhance their overall reliability performance, these include:

- Faraday shield vacuum packed wafer shipping system
- Temperature and humidity controlled wafer inventory stores
- Inert atmosphere for metal can packages encapsulation
- New design lead frames (plastic assembly)
- New molding compounds
- Low moisture content glass
- Moisture content audit procedures
- Super dry piece-part controls

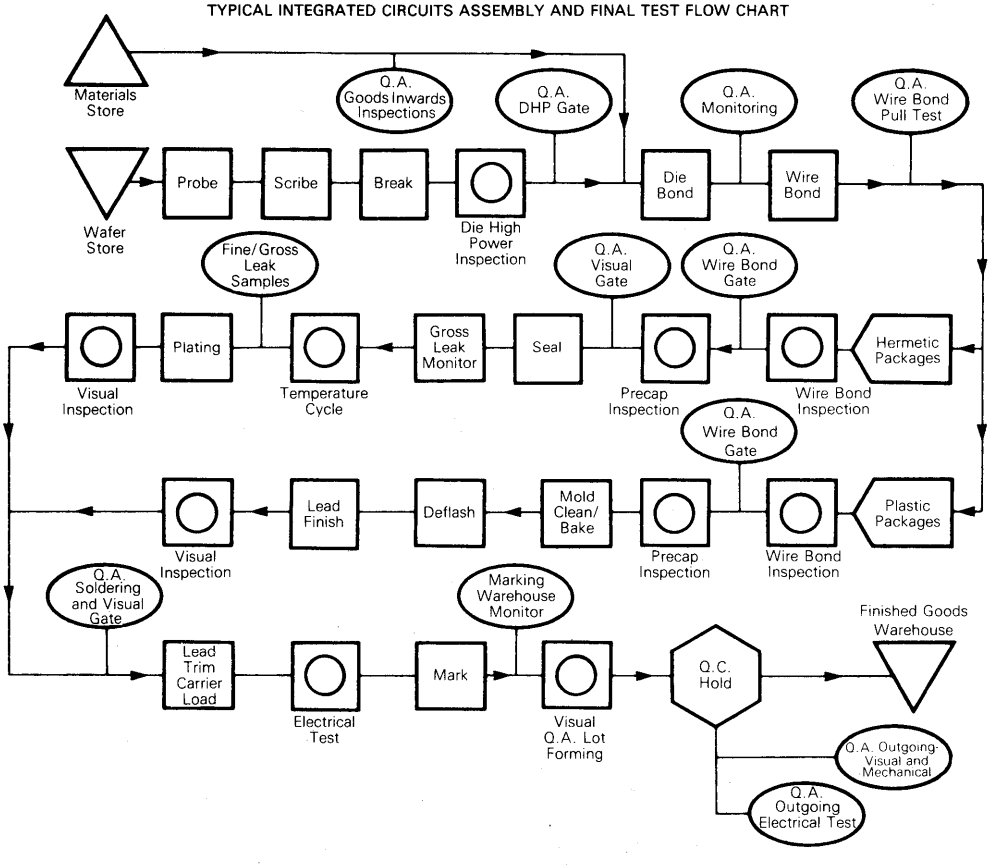
FINAL TESTING

Each of Motorola's facilties has a complete Final Test capability for all of the products fabricated and assembled. The majority of products, after assembly, are tested and Q.A. released at the facility responsible for that product. Some product is tested in the offshore assembly site; however, this is always returned to the facility for Q.A. release prior to final shipment to customer.

Final Test is a comprehensive series of dc, functional and speed orientated electrical tests as well as adapted forced tests. These tests are normally more stringent than data sheet requirements and are finally sampled by Outgoing Quality Assurance.

In practice, the test flow philosophies vary according to product. For instance, most of the Discrete devices are double tested as part of a zero defect quality improvement program. As well, many Integrated Circuits are tested at various temperatures. There are also many burn-in options available.

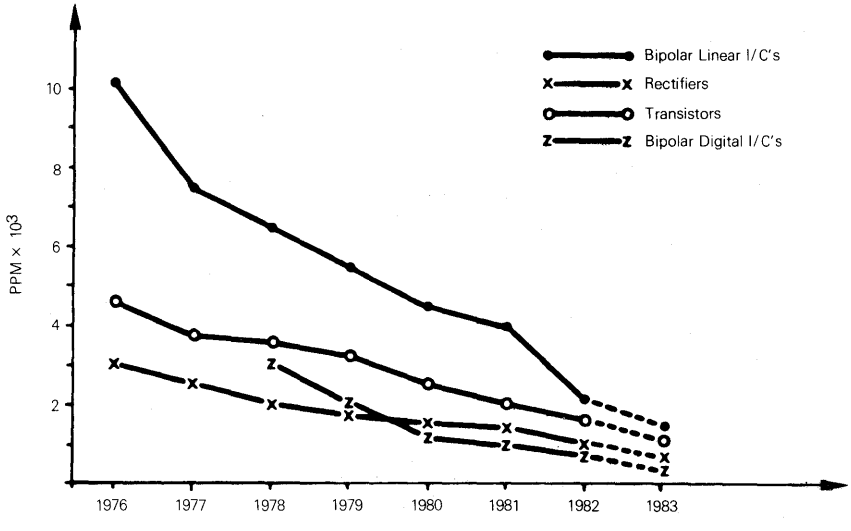
TYPICAL INTEGRATED CIRCUITS ASSEMBLY AND FINAL TEST FLOW CHART



OUTGOING QUALITY SAMPLING PLAN

		A.Q.L. 1979	1980	1981	1982	1983
Rectifiers	Electrical Inoperative	0.10	0.10	0.065	0.065	0.065
	Parametric	0.40	0.40	0.25	0.25	0.25
	Visual/Mechanical	0.25	0.25	0.15	0.15	0.10
Linear	Electrical Inoperative	0.25	0.15	0.15	0.15	0.10
	Parametric	0.65	0.40	0.40	0.40	0.25
	Visual/Mechanical	0.15	0.15	0.15	0.15	0.15
Power Transistors	Electrical Inoperative	0.10	0.10	0.10	0.10	0.10
	Parametric	0.40	0.40	0.40	0.40	0.25
	Visual/Mechanical	0.25	0.25	0.25	0.15	0.15
Small Signal Transistors	Electrical Inoperative	0.15	0.15	0.10	0.10	0.10
	Parametric	0.65	0.65	0.40	0.40	0.40
	Visual/Mechanical	0.40	0.40	0.25	0.15	0.15
CMOS	Function/Parametric	LTPD	LTPD	0.15	0.10	0.10
	Visual/Mechanical	(5.0)	(5.0)	0.15	0.15	0.15
MOS Microprocessors	Function/Parametric	LTPD	LTPD	0.15	0.10	0.10
	Visual/Mechanical	(5.0)	(5.0)	0.15	0.15	0.15
NMOS Memories	Function/Parametric	LTPD	LTPD	0.15	0.10	0.10
	Visual/Mechanical	(5.0)	(5.0)	0.15	0.15	0.15
LS TTL ECL	Function/Parametric	0.15	0.15	0.065	0.065	0.065
Bipolar Memory/LSI	Visual/Mechanical	0.65	0.15	0.065	0.065	0.065
ALS/FAST	Function/Parametric	–	–	–	0.065	0.065
	Visual/Mechanical					

EVOLUTION OF AVERAGE OUTGOING QUALITY – A.O.Q.
(TOTAL A.O.Q. INCLUDING VISUAL, MECHANICAL AND ELECTRICAL)



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OUTGOING QUALITY

Although test procedures may vary from product to product within Motorola, the same philosophy applies when considering quality objectives. Motorola's mission is to be a Quality and Reliability leader worldwide.

HIGHLIGHTS:

Motorola recognizes that you, our customers, are truly concerned about improving your own quality image. You are, therefore, concerned about the quality of the product Motorola supplies you.

Our customers measure us by the level of defects in the products we supply at incoming inspection, during assembly and, most important, field reliability.

During the past years, Motorola has achieved impressive reductions in defect rates known as A.O.Q. or Average Outgoing Quality. Instrumental in this success has been the planned continuous reduction in outgoing A.Q.L. to a point where Motorola believes that over all products it can demonstrate the most aggressive A.Q.L.'s in the industry.

This aggressive program has been designed to help eliminate expensive incoming inspection at our customers.

All of the facilities also practice an extremely demanding parts per million program program (PPM).

The PPM performance of all Motorola products is calculated in each location using the same method; they are, therefore, directly comparable. Motorola is well aware that when discussing PPM with existing or potential customers, it is of paramount importance to explain exactly which failure categories are included in the stated PPM figures. Motorola's PPM figures will include:

- Electrical Inoperative Failure
- Electrical Parametric Failures (dc and ac)
- Visual and Mechanical criteria.

In many published cases, stated PPM values refer to Electrical Inoperative failures only.

At Motorola, the Electrical Inoperative, the Electrical Parametric and the Visual Mechanical failure rates are calculated separately and then combined to reach an overall total. In this way Motorola believes that is giving its customers a true and accurate assessment of the quality of the product. Unqualified PPM statements can be misleading and cause the customer to expect quality levels which cannot be achieved. For example, Motorola CMOS A.O.Q. is quoted at 1,250 PPM overall Electrical parameters and including Visual/Mechanical categories. However, the function failure level is less than 200 PPM. Other product families such as Small Signal Plastic Transistors are already reaching 50 PPM in Electrical Inoperative failure rate.

The Motorola PPM graphs are excellent examples of what has been achieved over the last years with regard to quality improvements.

Reductions between 50% and 300% in average outgoing quality are typical across the broad range of Motorola products.

Throughout the semiconductor industry there have been, and there still are, examples of manufacturers offering higher quality standards at a premium. This is **not** a Motorola strategy, we believe that our customers should expect high quality products at no extra cost. This is Motorola's aim and we will continue to aggressively pursue Quality and Reliability improvements which will be passed on to our customers as an obligation on our part.

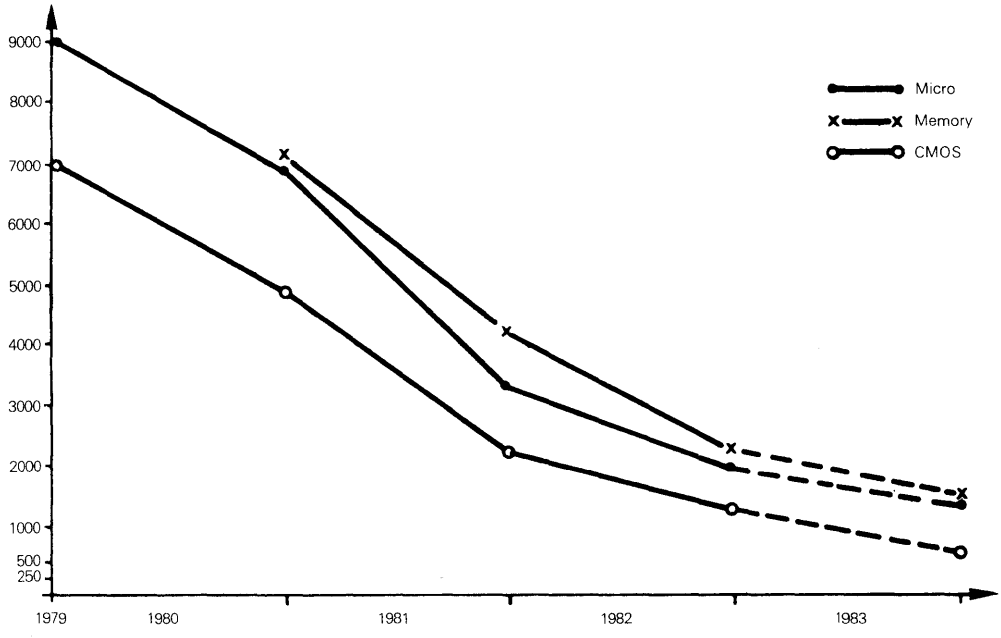
Also, we actively encourage our customers to provide their quality results at their Incoming Inspection, during their manufacturing process and from the field in order to better correlate and further improve our quality performance.

MOTOROLA A.O.Q. PLAN

	1980	History Average 1981	1982	Dec 1982	Goal 1983
Power Transistors	3400	1400	1100	950	700
Rectifiers	1750	1100	1000	950	700
Small Signal Metal	4100	2200	1400	1100	800
Small Signal Plastic	1500	1200	1030	800	600
Linear I/C's	4300	2800	1900	2000	1000
L. and S.F.	5000	2370	1380	1150	500
Memory	7000	4360	2400	2900	1300
Microprocessor	7000	3860	2450	2900	1300
Bipolar Digital Logic	1260	802	975	800	500
Bipolar Memory/LSI	1620	1200	1000	151	700

A.O.Q. Includes all Defects: Visual, Mechanical, Electrical Inoperative and Parametric.

AVERAGE A.O.Q. IN P.P.M. FOR MOS PRODUCTS FIGURES
INCLUDE FUNCTIONAL/PARAMETRIC/VISUAL/MECHANICAL



RELIABILITY

Paramount in the mind of every semiconductor user is the question of device performance versus time. After the applicability of a particular device has been established, its effectiveness depends on the length of troublefree service it can offer. The reliability of a device is exactly that — an expression of how well it will serve the customer. The following discussion will attempt to present an overview of Motorola's reliability efforts.

BASIC CONCEPTS

It is essential to begin with an explanation of the various parameters of Reliability. These are probably summarized best in the Bathtub Curve (Figure 1). The reliability performance of a device is characterized by three phases: infant mortality, useful life and wearout. When a device is produced, there is often a small distribution of failure mechanisms which will exhibit themselves under relatively moderate stress levels and therefore appear early. This period of early failures, termed infant mortality, are reduced significantly through proper manufacturing controls and screening techniques. The most effective period is that in which only occasional random failure mechanisms appear; the useful life typically spans a long period of time with a very low failure rate. The final period is that in which the devices literally wear out due to continuous phenomena which existed at the time of manufacture. Using strictly controlled design techniques and selectivity in applications, this period is shifted well beyond the lifetime required by the user.

FIGURE 1

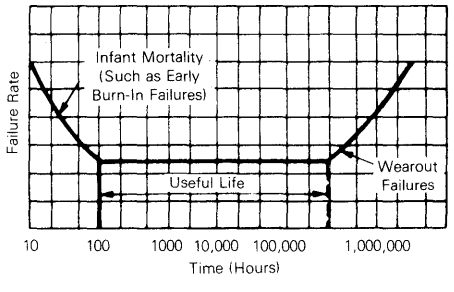
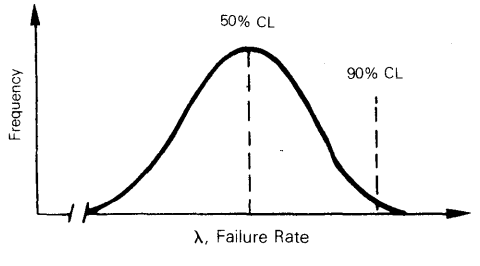


FIGURE 2



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Both the infant mortality and random failure rate regions can be described through the same types of calculations. During this time the probability of having no failures to a specific point in time can be expressed by the equation:

$$P_O = e^{-\lambda t}$$

where λ is the failure rate and t is time. Since λ is changing rapidly during infant mortality, the expression does not become useful until the random period, where λ is relatively constant. In this equation λ is failures per unit of time. It is usually expressed in percent failures per thousand hours. Other forms include FIT (Failures In Time= $(\%/10^3$ hrs) $\times 10^{-4} = 10^{-9}$ failures per hour) and MTTF (Mean Time To Failure) or MTBF (Mean Time Between Failures), both being equal to $1/\lambda$ and having units of hours.

Since reliability evaluations usually involve only samples of an entire population of devices, the concepts of the Central Limit Theorem apply and λ is calculated using x^2 distribution through the equation:

$$\lambda \leq \frac{x^2\,(x,\ 2r+2)}{2nt}$$

$$\text{where } x = \frac{100 - CL}{100}$$

CL = Confidence Limit in percent
r = Number of rejects
n = Number of devices
t = Duration of test

The confidence limit is the degree of conservatism desired in the calculation. The Central Limit Theorem states that the values of any sample of units out of a large population will produce a normal distribution. A 50% confidence limit is termed the best estimate and is the mean of this distribution. A 90% confidence limit is a very conservative value and results in a higher λ which represents the point at which 90% of the area of the distribution is to the left of that value (Figure 2). The term (2r+ 2) is called the degrees of freedom and is an expression of the number of rejects in a form suitable to x^2 tables.

The number of rejects is a critical factor since the definition of rejects often differs between manufacturers. While Motorola uses data sheet limits to determine failures, sometimes rejects are counted only if they are catastrophic. Due to the increasing chance of a test not being representative of the entire population as sample size and test time are decreased, the x^2 calculation produces surprisingly high values of λ for short test durations even though the true long term failure rate may be quite low. For this reason relatively large amounts of data must be gathered to demonstrate the real long term failure rate.

Since this would require years of testing on thousands of devices, methods of accelerated testing have been developed.

Years of semiconductor device testing has shown that temperature will accelerate failures and that this behaviour fits the form of the Arrhenius equation:

$$R(t) = R_O(t)e^{-\Theta/kT}$$

where R(t) = Reaction rate as a function of time and temperature

R_O = A constant
t = Time
Θ = Activation energy in electron volts
k = Boltzman's constant
T = Temperature in degrees Kelvin

To provide time-temperature equivalents this equation is applied to failure rate calculations in the form:

$$t = t_O e^{\Theta/kT}$$

where t = time

t_O = A constant

The Arrhenius equation essentially states that reaction rate increases exponentially with temperature. This produces a straight line when plotted on log-linear paper with a slope expressed by Θ. Θ may be physically interpreted as the energy threshold of a particular reaction or failure mechanism. The activation energy exhibited by semiconductors varies from about 0.3 eV. Although the relationships do not prohibit devices from having poor failure rates and high activation energies, good performance usually does imply a high Θ. Studies by Bell Telephone Laboratories have indicated that an overall Θ for semiconductors is 1.0 eV. This value has been accepted by the Rome Air Development Command for time-temperature acceleration in powered burn-in as specified in Method 1015 of MIL-STD-883. Data taken by Motorola on Integrated Circuits have verified this number and it is therefore applied as our standard time-temperature regression for extrapolation of high temperature failure rates to temperatures at which the devices will be used (Figure 3). For Discrete products, 0.7 eV is generally applied.

To accomplish this, the time in device hours (t1) and temperature (T1) of the test are plotted as point P1. A vertical line is drawn at the temperature of interest (T2) and a line with a 1.0 eV slope is drawn through point P1.

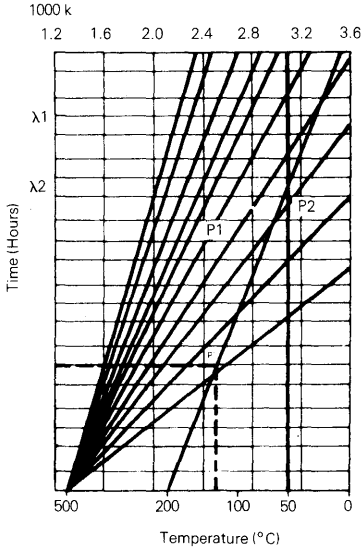
Its intersection with the vertical line defines point P2, and determines the number of equivalent device hours (t2). This number may then be used with the x^2 formula to determine the failure rate at the temperature of interest. Assuming T1 of 125°C at t1 of 10,000 hours, a t2 of 7.8 million hours results at a T2 of 50°C. If one reject results in the 10,000 device hours of testing at 125°C, the failure rate at that temperature will be 20%/1,000 hours using a 60% confidence level. One reject at the equivalent 7.8 million device hours at 50°C will result in a 0.026%/1,000 hour failure rate, as illustrated in Figure 4.

Three parameters determine the failure rate quoted by the manufacturer: the failure rate at the test temperature, the activation energy employed, and the difference between the test temperature and the temperature of the quoted λ. A term often used in this manipulation is the "acceleration factor" which is simply the equivalent device hours at the lower temperature divided by the actual test device hours.

Every device will eventually fail, but with the present techniques in Semiconductor design and applications, the wearout phase is extended far beyond the lifetime required. During wearout, as in infant mortality, the failure rate is changing rapidly and therefore loses its value. The parameter

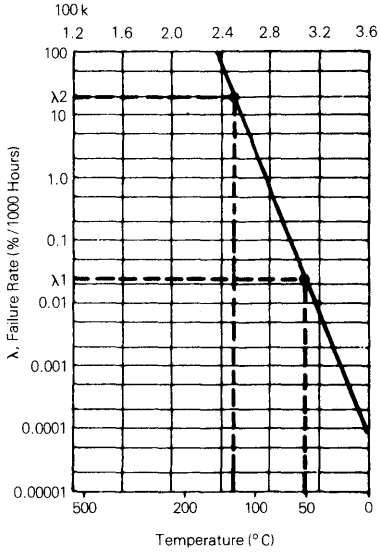
used to describe performance in this area is "Median Life" and is the point at which 50% of the devices have failed. There are currently only few significant wearout mechanisms: electromigration of circuit metallization, electrolytic corrosion in plastic devices and metal fatigue for Power devices.

FIGURE 3
NORMALIZED TIME-TEMPERATURE REGRESSIONS FOR VARIOUS ACTIVATION ENERGY VALUES



For increased flexibility in working with a broad range of device hours, the time-temperature regression lines have been normalized to 500°C and the time scale omitted, permitting the user to define the scale based on his own requirements.

FIGURE 4
FAILURE RATE



Reliability

RELIABILITY TESTS: DEFINITION, PURPOSE AND PROCEDURES

These definitions are intended to give the reader a brief understanding of the test currently used at Motorola for reliability checking. They also state which main failure mechanisms are accelerated by the test.

HIGH TEMPERATURE STORAGE LIFE

An environmental test where only temperature is the stress. Temperature and test duration must be specified. Usually temperature is the maximum storage temperature of the devices under test. Main failure mechanisms are metallization, bulk silicon, corrosion.

HIGH TEMPERATURE REVERSE BIAS (HTRB)

An environmental stress combined with an electrical stress whereby devices are subjected to an elevated temperature and simultaneously reverse biased. To be effective, voltage must be applied to the devices until they reach room temperature at the completion of the test. Temperature, time and voltage levels must be specified. Accelerated failure mechanisms are inversion, channeling, surface contamination, design.

HIGH HUMIDITY, HIGH TEMPERATURE REVERSE BIAS (H^3TRB)

A combined environmental/electrical stress whereby devices are subjected to an elevated ambient temperature and high humidity, simultaneously reverse biased for a period of time. Normally performed on a sample basis (qualification) on non-hermetic devices. The most common conditions is 85°C and 85% relative humidity. More extreme conditions generally are very destructive to the chambers used. Time, temperature, humidity and voltage must be specified. This accelerated test mainly detects corrosion risks.

STEADY STATE OPERATING LIFE

An electrical stress whereby devices are forward (reverse for zeners) biased at full rated power for prolonged duration. Test is normally 25°C ambient and power is 100% of full rated. (For power devices the I/C's maximum operating Ti is used.) Duration, power and ambient, if other than 25°C, must be specified. Accelerated failure mechanisms mainly are metallization, bulk silicon, oxide, inversion and channeling.

DYNAMIC OPERATING LIFE

An electrical stress whereby devices are alternately subjected to forward bias at full rated power or current and reverse bias.

Duration, power, duty cycle, reverse voltage ambient and frequency must be specified. Used normally for rectifiers and silicon controlled rectifiers. Failure mechanisms are essentially the same as steady state operating life.

INTERMITTENT OPERATING LIFE (POWER CYCLING)

An electrical stress whereby devices are turned on and off for a period of time. During the "on" time the devices are turned on at a power such that the junction temperature reaches its maximum rating. During "off" cycle the devices return to 25°C ambient. Duration, power, or duty cycle must be individually specified. Accelerated failures mechanisms are mainly die bonds, wire bond, metallization, bulk silicon, and oxide.

THERMAL SHOCK (TEMPERATURE CYCLING)

An environmental stress whereby devices are alternately subjected to a low and high temperature with or without a dwell time in between to stabilize the devices to 25°C ambient — the medium is usually air. Temperatures, dwell times and cycles must be specified. Failure mechanisms are essentially die bonds, wire bonds, and package.

THERMAL SHOCK (GLASS STRAIN)

An environmental stress whereby the devices are subjected to a low temperature, stabilized and immediately transferred to a high temperature. The medium is usually liquid. Failures mechanisms essentially are the same as temperature cycling.

EXAMPLE OF NEW PROCESS QUALIFICATION TESTS

Test	Condition	Duration	MIL-STD-883 Reference Test Method
Operating Life	125°C, 5 V or 15 V	1,000 Hours	1005
Temperature Humidity Bias	85°C, 85% R.H. 5 V or 15 V	1,000 Hours	
Autoclave	121°C, 100% R.H. 15P.S.I.G.	144 Hours	
High Temperature Storage	150°C	1,000 Hours	
Thermal Cycle (Air to Air)	− 65°C to 150°C 5 Min Dwell	1,000 Cycles	1010
Thermal Shock (Liquid to Liquid)	− 65°C to 150°C 5 Min Dwell	1,000 Cycles	1011
Shock, Vibration, and Constant Acceleration	1,500G, 3 per Axis 150− 2,000 Hz, 20 g 30 kg	0.5 MS 2 Hours	2002 2007 2001
Data Retention Bake (Non Volation Memories)	200/250°C	1,000 Hours	

MECHANICAL SHOCK

A mechanical stress whereby the devices are subjected to high impact forces normally in two or more of the six orientations X1, Y1, Z1, X2, Y2, Z2. Tests are to verify the physical integrity of the devices. G forces, pulse duration, and number of shocks and axes must be specified.

VIBRATION VARIABLE FREQUENCY

Same as Vibration Fatigue except that frequency is logarithmically varied from 100 Hz to 1 kHz and back. Number of cycles is normally four. Cycle time, amplitude and total duration must be specified. Failure mechanisms are mainly package, wire bond – this test is not applicable to molded devices.

EXAMPLE OF NEW PACKAGE QUALIFICATION TESTS

Test	Condition	Duration	MIL-STD-883 Reference Test Method
Operating Life	125°C, 5 V or 15 V	1,000 Hours	1005
Temperature Humidity Bias	85°C, 85% R.H. 5 V or 15 V	1,000 Hours	
Autoclave	121°C, 100% R.H. 15 P.S.I.G.	144 Hours	
High Temperature Storage	150°C	1,000 Hours	
Thermal Cycle (Air to Air)	−65°C to 150°C 5 Min Dwell	1,000 Cycles	1010
Thermal Shock (Liquid to Liquid)	−65°C to 150°C 5 Min Dwell	1,000 Cycles	1011
Shock, Vibration, and Constant Acceleration	1,500 G, 3 per Axis 150 – 2,000 Hz, 20 g 30 kg	0.5 ms 2 Hours	2002 2007 2001
Hermeticity	1.85, 10^{-8} atm cc/sec		1014
Visual Inspection			2008
Dimensions	Outline Dwg.		2016
Marking Permanency			2015
Solderability	230°C	3 Seconds	2003
Wire Bond Strength (Post Seal)	1.5 Gram		2011
Die Shear			2027

EXAMPLE OF STANDARD RELIABILITY PROGRAM

Reliability Engineering Department	Motorola Reliability Program For:			
Test Group	**Test**	**SS**	**Frequency**	**Test Methods/Conditions**
Reliability Audit	Thermal Shock	25	1 Product Line Per Week	MIL-STD-883, Method 1011 −25°C, +125°C. Dwell Time 5 mn, 100 Cycles
	High Temperature Reverse Bias	40		TA = 150°C, VCB = .8 VCB max. 168 hours
Life Tests	High Temperature Reverse Bias	25 (+2)	3 Product Lines Per Month	TA = 150°C, VCB = .8 VCB max. 1,000 hours
	High Temperature Storage	25 (+2)		TA = 150°C, 1,000 hours
	Steady State Life	25 (+2)		MIL-STD-883, Method 1005 TA = 125°C, 1,000 hours
	High Humidity	25		TA = 85°C, 85% Humidity
	High Temperature Reverse Bias	(+2)		VCB = .8 VCB max. 1,000 hours
(+2) devices for correlation purpose				

Product Family	Test Conditions	Device Hours	No. Of Failures	Activation Energy	Derated Temperature	% Per 1,000 Hours At 60% Confidence
Non Hermetic Interface I/C's	Operating T_j = 155°C	591,552	64	1 eV	70°C	0.014
Consumer I/C's	Operating T_j = 125°C	13,082,000	39	1 eV	70°C	0.0029
DO4/DO5 Rectifier	T_j = 150°C VR = .8 BVR	798,000	5	.7 eV	70°C	0.009
Plastic Axial Diodes	T_j = 100°C VR = .8 BVR	295,000	3	.7 eV	70°C	0.21
Button Diodes	T_j = 150°C VR = .8 BVR	520,000	5	.7 eV	70°C	0.014
Small Signal Plastic Transistor	T_j = 150°C VCB = .8 BVCO	579,000	6	.7 eV	70°C	0.014
Small Signal Metal Transistor	T_j = 150°C VCB = .8 BVCBO	3,944,000	12	.7 eV	70°C	0.0039
Case 77 Power Plastic Transistor	T_j = 150°C VBC = .8 BVCBO	364,416	2	.7 eV	70°C	0.0097
TO220 Power Plastic Transistor	T_j = 150°C VCB = .8 BVCBO	366,080	0	.7 eV	70°C	0.0028
TO3P Power Plastic Transistor	T_j = 150°C VCB = .8 BVCBO	297,024	3	.7 eV	70°C	0.016
TO3 Power Metal Transistor	T_j = 150°C VCB = .8 BVCBO	247,104	3	.7 eV	70°C	0.019

6

Product Family	Test Conditions	Device Hours	No. of Failures	Activation Energy	Derated Temperature	% Per 1,000 Hours At 60% Confidence
CMOS Ceramic	125°C Static Bias 15 V	2.04×10^6	6	1 EV	50°C 75°C 85°C	0.0004 0.003 0.014
CMOS Plastic	125°C Static Bias 15 V	1.13×10^6	4	1 EV	85°C	0.018
6800 Series Plastic	125°C Dynamic Bias 5 V	2.88×10^6	47	1 EV	70°C	0.039
U.V. EPROM Life Test	125°C Dynamic Bias 5 V	434,456	3	1 EV	70°C	0.009
Data Retention	250°C Bake	519,120	3	0.7 EV	70°C	0.0075
EEPROM Life Test	125°C Dynamic Bias 5 V	917,280	25	1 EV	70°C	0.027
Data Retention	250°C	966,672	19	0.7 EV	70°C	0.020
64K DRAM	125°C Dynamic Bias 5.5 V	1.05×10^6	6	0.7 EV	70°C	0.028

Product Family	Test Conditions	Device Hours	No. of Failures	Activation Energy	Derated Temperature	% Per 1,000 Hours At 90% Confidence
LS-TTL	125°C Static Basis −5.2 V			1.0 eV	70°C	0.0029
ECL	125°C Static Bias 5 V	61.74×10^6	7	1.0 eV	85°C	0.0189

Product Family	Test Conditions	Device Hours	No. of Failures	Activation Energy	Derated Temperature	% Per 1,000 Hours At 60% Confidence
Operational Amplifier	Operating $T_j = 135°C$	437,472	2	1 eV	70°C	0.0026
Hermetic Interface I/C's	Operating $T_j = 135°C$	718,848	4	1 eV	70°C	0.0033

The reliability approach at Motorola Semiconductors is based on designing in reliability rather than testing for reliability only. This concept is reflected by Motorola's mandatory procedures which require product, process and packaging qualification on three independently produced lots before any product is released to volume production. Reliability engineering approval supported by an officially documented report is required before any product is released to manufacturing. Tests at both maximum rated and accelerated stress levels are performed. Acceleration is important to determine how and at what stress level a new design, product process or package would fail. This information provides an indication of what design changes can be implemented to ensure a wider and safer margin between the maximum rated stress condition and the devices stress limitation.

As well as qualifying all new products, processes and piece-parts, each Motorola manufacturing facility operates an ongoing reliability monitor which covers all process and packaging options. This program provides a continuous up-to-date data base which is summarized in periodical reports.

Reliability statistics supporting all Motorola Semiconductor devices can be obtained from any of the Motorola Sales Offices upon request. The present operating life test results demonstrates Motorola's reputation for producing semiconductors with reliability second to none.

The Quality organization in each facility is responsible for preparing and maintaining a Quality Manual which describes in detail the quality systems and associated Reliability and Quality Assurance organization, policies, and procedures. This manual must be appraised and ultimately approved by the appropriate approval authority.

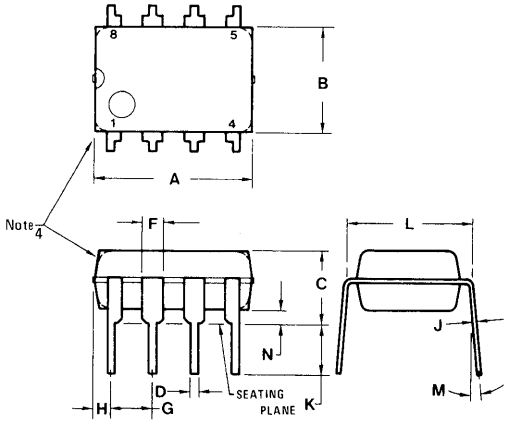
Mechanical Data 7

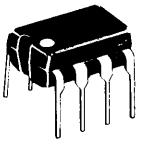
MECHANICAL DATA

The package availability for each device is indicated on the front page of the individual data sheets. Dimensions for the packages are given in this chapter.

8-PIN PACKAGE

P SUFFIX
PLASTIC PACKAGE
CASE 626-04





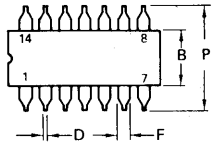
NOTES:
1. LEAD POSITIONAL TOLERANCE:
   ⌖ ⌀ 0.13 (0.005) Ⓜ | T | A Ⓜ | B Ⓜ
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS).
4. DIMENSIONS A AND B ARE DATUMS.
5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

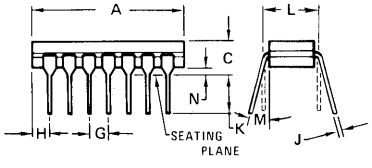
STYLE 1:
PIN 1. AC IN
2. DC + IN
3. DC - IN
4. AC IN
5. GROUND
6. OUTPUT
7. AUXILIARY
8. VCC

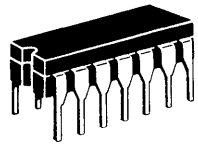
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.40	10.16	0.370	0.400
B	6.10	6.60	0.240	0.260
C	3.94	4.45	0.155	0.175
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	0.76	1.27	0.030	0.050
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	–	10^0	–	10^0
N	0.51	0.76	0.020	0.030

14-PIN PACKAGES

L SUFFIX
CERAMIC PACKAGE
CASE 632-07



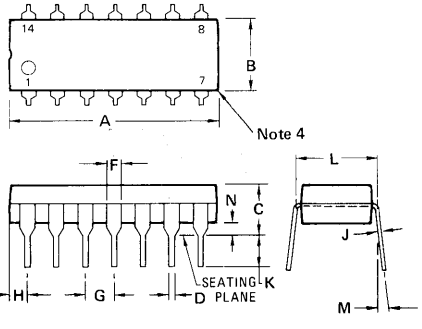


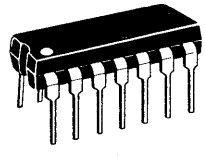


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	19.05	19.94	0.750	0.785
B	6.10	7.49	0.240	0.295
C	–	5.08	–	0.200
D	0.38	0.58	0.015	0.023
F	1.40	1.77	0.055	0.070
G	2.54 BSC		0.100 BSC	
H	1.91	2.29	0.075	0.090
J	0.20	0.38	0.008	0.015
K	3.18	4.32	0.125	0.170
L	7.62 BSC		0.300 BSC	
M	–	15°	–	15°
N	0.51	1.02	0.020	0.040

NOTES:
1. ALL RULES AND NOTES ASSOCIATED WITH MO-001 AA OUTLINE SHALL APPLY.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION "A" AND "B" (632-07) DO NOT INCLUDE GLASS RUN-OUT.
4. LEADS WITHIN 0.25 mm (0.010) DIA OF TRUE POSITION AT SEATING PLANE AND MAXIMUM MATERIAL CONDITION.

P SUFFIX
PLASTIC PACKAGE
CASE 646-05



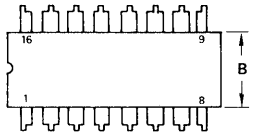


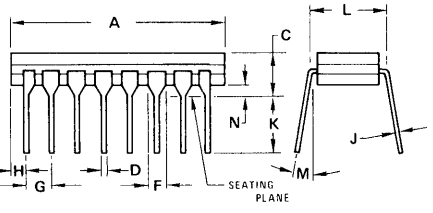
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	18.16	19.56	0.715	0.770
B	6.10	6.60	0.240	0.260
C	4.06	5.08	0.160	0.200
D	0.38	0.53	0.015	0.021
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	1.32	2.41	0.052	0.095
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	10°	0°	10°
N	0.51	1.02	0.020	0.040

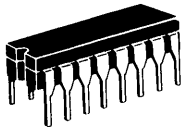
NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
4. ROUNDED CORNERS OPTIONAL.

16-PIN PACKAGES

L SUFFIX
CERAMIC PACKAGE
CASE 620-08



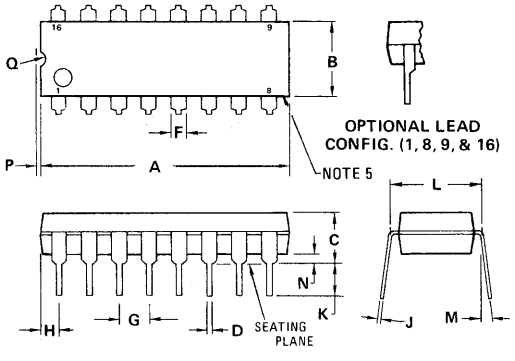


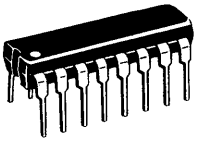


1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. PACKAGE INDEX: NOTCH IN LEAD NOTCH IN CERAMIC OR INK DOT.
3. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIM "A" AND "B" DO NOT INCLUDE GLASS RUN-OUT.
5. DIM "F" MAY NARROW TO 0.76 mm (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	19.05	19.94	0.750	0.785
B	6.10	7.49	0.240	0.295
C	–	5.08	–	0.200
D	0.38	0.53	0.015	0.021
F	1.40	1.78	0.055	0.070
G	2.54 BSC		0.100 BSC	
H	0.51	1.14	0.020	0.045
J	0.20	0.30	0.008	0.012
K	3.18	4.32	0.125	0.170
L	7.62 BSC		0.300 BSC	
M	–	15°	–	15°
N	0.51	1.02	0.020	0.040

P SUFFIX
PLASTIC PACKAGE
CASE 648-05



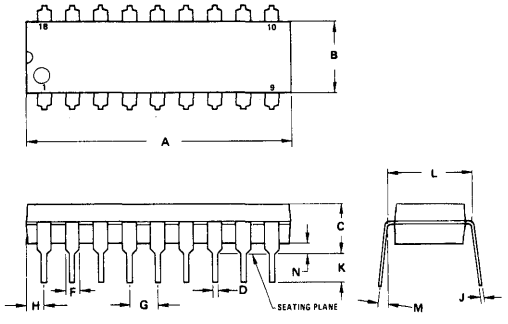


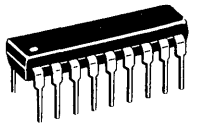
NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
4. "F" DIMENSION IS FOR FULL LEADS. "HALF" LEADS ARE OPTIONAL AT LEAD POSITIONS 1, 8, 9, and 16).
5. ROUNDED CORNERS OPTIONAL.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	18.80	21.34	0.740	0.840
B	6.10	6.60	0.240	0.260
C	4.06	5.08	0.160	0.200
D	0.38	0.53	0.015	0.021
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	0.38	2.41	0.015	0.095
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	10°	0°	10°
N	0.51	1.02	0.020	0.040

18-PIN PACKAGES

P SUFFIX
PLASTIC PACKAGE
CASE 707-02

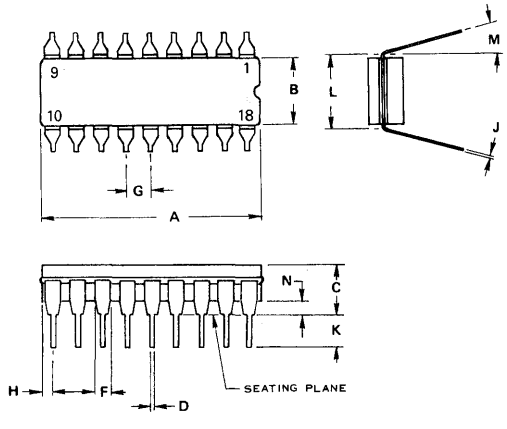


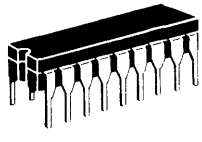


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	22.22	23.24	0.875	0.915
B	6.10	6.60	0.240	0.260
C	3.56	4.57	0.140	0.180
D	0.36	0.56	0.014	0.022
F	1.27	1.78	0.050	0.070
G	2.54 BSC		0.100 BSC	
H	1.02	1.52	0.040	0.060
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25mm(0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

L SUFFIX
CERAMIC PACKAGE
CASE 726-04



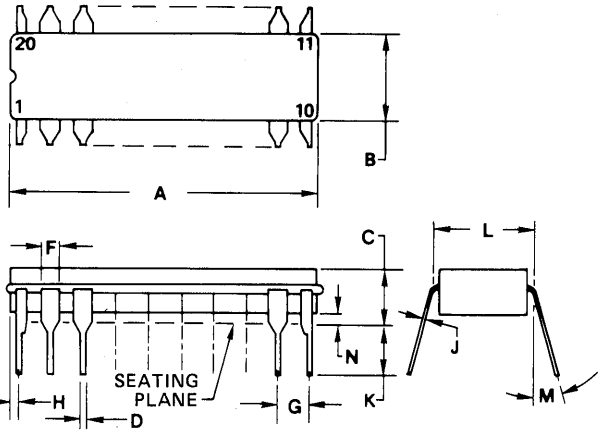


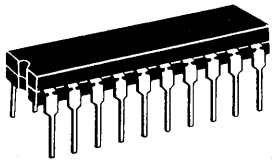
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	22.35	23.11	0.880	0.910
B	6.10	7.49	0.240	0.295
C	–	5.08	–	0.200
D	0.38	0.53	0.015	0.021
F	1.40	1.78	0.055	0.070
G	2.54 BSC		0.100 BSC	
H	0.51	1.14	0.020	0.045
J	0.20	0.30	0.008	0.012
K	3.18	4.32	0.125	0.170
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

NOTES:
1. LEADS, TRUE POSITIONED WITHIN 0.25 mm (0.010) DIA. AT SEATING PLANE, AT MAXIMUM MATERIAL CONDITION.
2. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIM "A" & "B" INCLUDES MENISCUS.

20-PIN PACKAGES

L SUFFIX
CERAMIC PACKAGE
CASE 732-03

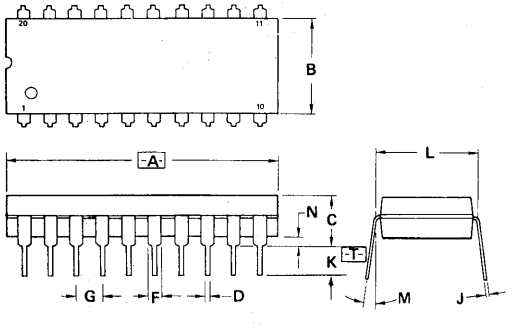


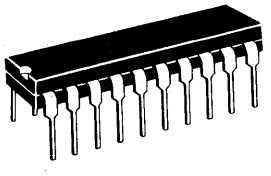


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	23.88	25.15	0.940	0.990
B	6.60	7.49	0.260	0.295
C	3.81	5.08	0.150	0.200
D	0.38	0.56	0.015	0.022
F	1.40	1.65	0.055	0.065
G	2.54 BSC		0.100 BSC	
H	0.51	1.27	0.020	0.050
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.25	1.02	0.010	0.040

NOTES:
1. LEADS WITHIN 0.25 mm (0.010) DIA, TRUE POSITION AT SEATING PLANE, AT MAXIMUM MATERIAL CONDITION.
2. DIM L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIM A AND B INCLUDES MENISCUS.

P SUFFIX
PLASTIC PACKAGE
CASE 738-02





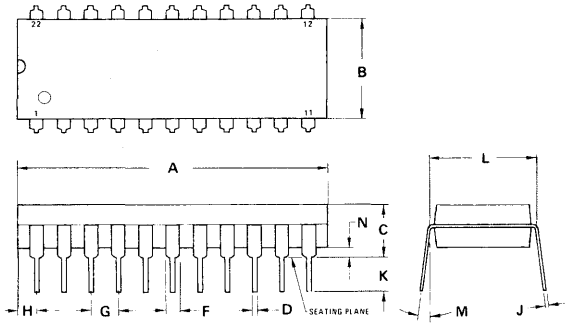
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	25.65	27.18	1.010	1.070
B	6.10	6.60	0.240	0.260
C	3.94	4.57	0.155	0.180
D	0.38	0.56	0.015	0.022
F	1.27	1.78	0.050	0.070
G	2.54 BSC		0.100 BSC	
J	0.20	0.38	0.008	0.015
K	2.79	3.56	0.110	0.140
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

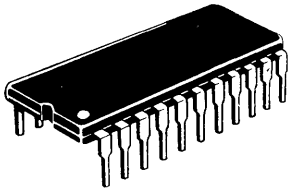
NOTES:
1. DIM -A- IS DATUM.
2. POSITIONAL TOL FOR LEADS;
   ⌖ Ø 0.25 (0.010)Ⓜ T A Ⓜ
3. -T- IS SEATING PLANE.
4. DIM "B" DOES NOT INCLUDE MOLD FLASH.
5. DIM -L- TO CENTER OF LEADS WHEN FORMED PARALLEL.
6. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

7

22-PIN PACKAGES

P SUFFIX
PLASTIC PACKAGE
CASE 708-04

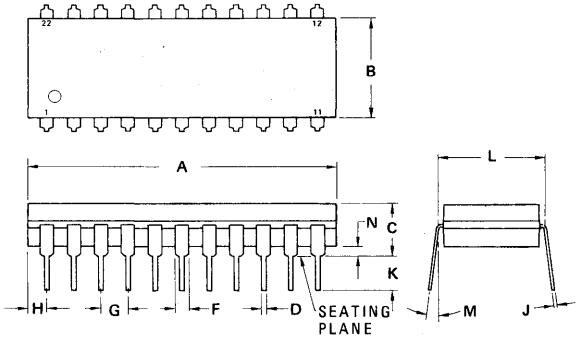


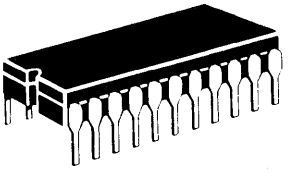


NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25mm(0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	27.56	28.32	1.085	1.115
B	8.64	9.14	0.340	0.360
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.27	1.78	0.050	0.070
G	2.54 BSC		0.100 BSC	
H	1.02	1.52	0.040	0.060
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	10.16 BSC		0.400 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

L SUFFIX
CERAMIC PACKAGE
CASE 736-03



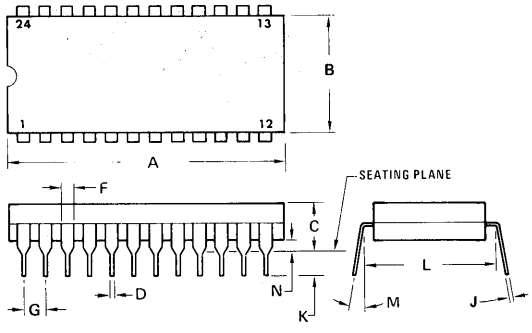


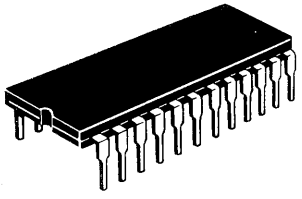
NOTES:
1. LEADS TRUE POSITIONED WITHIN 0.25 mm (0.010) DIA AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION (DIM "D").
2. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	26.80	27.81	1.055	1.095
B	9.14	9.91	0.360	0.390
C	3.81	5.46	0.150	0.215
D	0.38	0.53	0.015	0.021
F	1.27	1.65	0.050	0.065
G	2.54 BSC		0.100 BSC	
H	0.51	1.27	0.020	0.050
J	0.20	0.30	0.008	0.012
K	3.18	4.32	0.125	0.170
L	9.91	10.41	0.390	0.410
M	–	15°	–	15°
N	0.25	0.89	0.010	0.035

24-PIN PACKAGES

L SUFFIX
CERAMIC PACKAGE
CASE 623-05

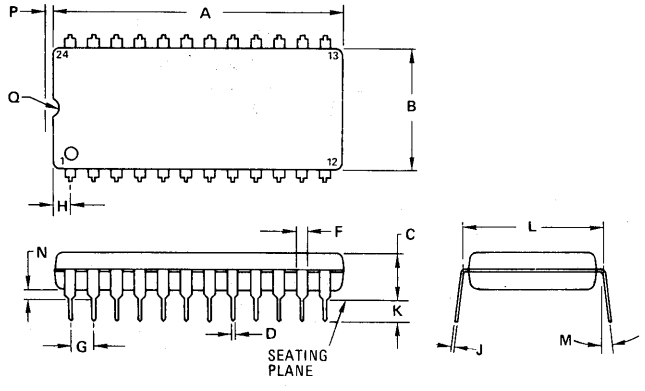


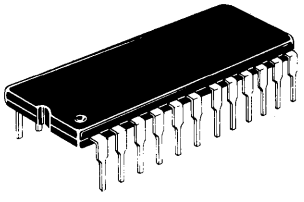


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	31.24	32.77	1.230	1.290
B	12.70	15.49	0.500	0.610
C	4.06	5.59	0.160	0.220
D	0.41	0.51	0.016	0.020
F	1.27	1.52	0.050	0.060
G	2.54 BSC		0.100 BSC	
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.27	0.020	0.050

NOTES:
1. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
2. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION. (WHEN FORMED PARALLEL).

P SUFFIX
PLASTIC PACKAGE
CASE 649-03



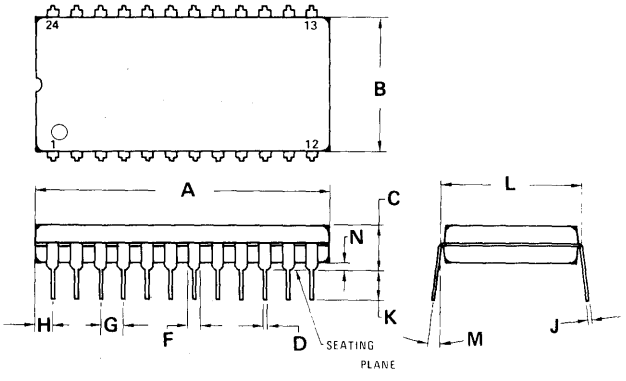


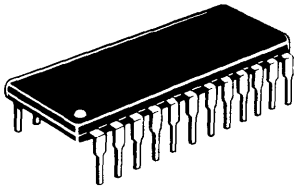
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	31.50	32.13	1.240	1.265
B	13.21	13.72	0.520	0.540
C	4.70	5.21	0.185	0.205
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	14.99	15.49	0.590	0.610
M	–	10°	–	10°
N	0.51	1.02	0.020	0.040
P	0.13	0.38	0.005	0.015
Q	0.51	0.76	0.020	0.030

NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

24-PIN PACKAGES (Continued)

P SUFFIX
PLASTIC PACKAGE
CASE 709-02



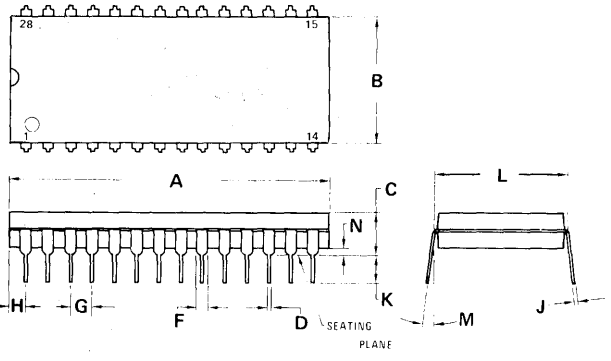


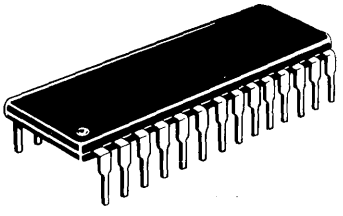
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	31.37	32.13	1.235	1.265
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.03	0.065	0.080
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0^0	15^0	0^0	15^0
N	0.51	1.02	0.020	0.040

NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 mm (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

28-PIN PACKAGES

P SUFFIX
PLASTIC PACKAGE
CASE 710-02

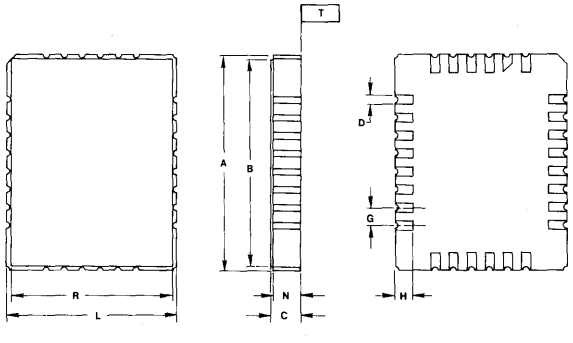


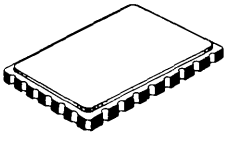


DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	36.45	37.21	1.435	1.465
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25mm(0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

Z SUFFIX
CHIP CARRIER
CASE 763-01





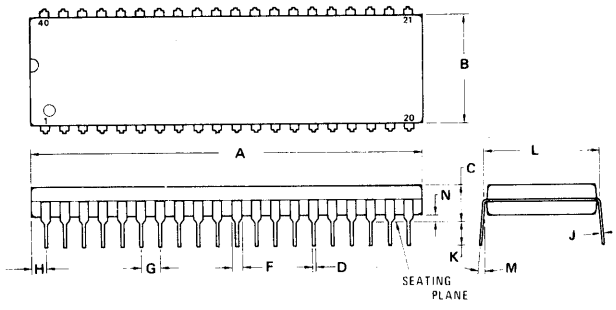
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	12.01	12.49	0.473	0.492
B	11.48	11.88	0.452	0.468
C	1.32	1.72	0.052	0.068
D	0.43	0.58	0.017	0.023
G	1.27 BSC		0.050 BSC	
H	0.83	1.19	0.033	0.047
L	9.47	9.95	0.373	0.392
N	1.52	2.03	0.060	0.080
R	8.94	9.34	0.352	0.368

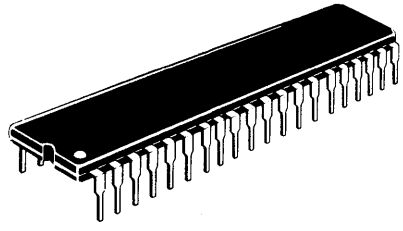
NOTES:
1. DIMENSIONS A AND L ARE DATUMS.
2. T IS A GAUGE PLANE.
3. POSITIONAL TOLERANCE FOR TERMINALS (D): 28 PLACES.
   ⌖ | 0.15 (0.006) Ⓜ | T | A Ⓢ | L Ⓢ
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

7

40-PIN PACKAGES

P SUFFIX
PLASTIC PACKAGE
CASE 711-03





DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	51.69	52.45	2.035	2.065
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0^0	15^0	0^0	15^0
N	0.51	1.02	0.020	0.040

NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 mm (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.