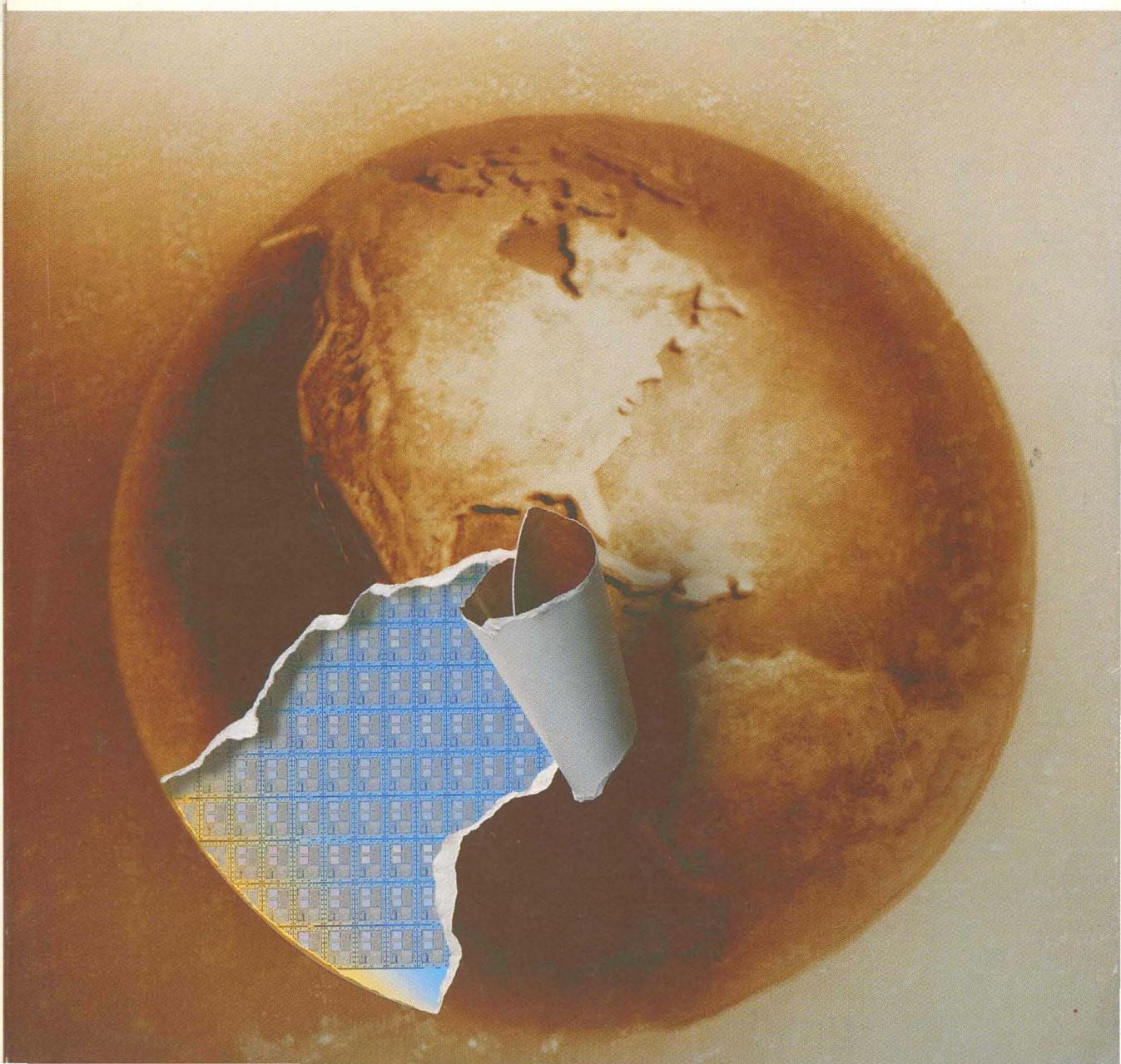
MOTOROLA

DL136/D
REV 4

Communications

Device Data



MOTOROLA COMMUNICATIONS DEVICE DATA

Q1/96
DL136
REV 4

DATA CLASSIFICATION

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MOTOROLA

Communications
Device Data

Motorola offers a broad range of semiconductor communications products for a wide variety of applications. The *Motorola Communications Device Data Book* contains specifications on these parts as well as information on Evaluation Kits, a selection of Application Notes and Product Literature, a Glossary of related terms, Handling and Design Guidelines, and Reliability and Quality information. Functional and Technical Selection Guides are also included to help you select the appropriate part for your application.

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TABLE OF CONTENTS

Chapter 1 — Selection Guides

Chapter 2 — Data Sheets

Selection Guides

1

1

Functional Selection Guide

This selection guide includes all Motorola devices characterized in this book, as well as other devices also used in communications applications, but associated with other product families. This guide references the page numbers for devices that appear in this book, or the appropriate reference document for the devices that do not appear in this book. The reference documents include the following:

Document No.	Title
DL110/D	Volume 1 and 2, RF Device Data
DL111/D	Bipolar Power Transistor Data
DL118/D	Optoelectronics Device Data
DL122/D	MECL Data
DL126/D	Small–Signal Transistors, FETs, and Diodes
DL128/D	Linear/Interface ICs Device Data
DL150/D	TVS/Zener Device Data
SG73/D	Master Selection Guide
SG96/D	Linear/Interface ICs Selector Guide and Cross Reference
SG169/D	MOS Digital–Analog IC Quarterly Update
BR . . .	Brochures
DSP . . .	Individual Device Data Sheets
MC . . .	Individual Device Data Sheets

AMPLIFIERS/COMPARATORS/REGULATORS

Device No.	Function	Page No. or Reference
MC33102	Dual Sleep–Mode Operational Amplifier	MC33102/D
MC33129	High Performance Current Mode Controller	2–537
MC33171	Low Power, Single Supply Operational Amplifier	MC33171/D
MC33178	High Output Current, Low Power, Low Noise Operational Amplifiers	MC33178/D
MC33179	High Output Current, Low Power, Low Noise Operational Amplifiers	MC33178/D
MC33201	Rail–To–Rail Operational Amplifier	MC33201/D
MC33304	Rail–To–Rail, Sleepmode Two–State Operational Amplifier	MC33304/D
MC34119	Low Power Audio Amplifier	2–536
MC34129	High Performance Current Mode Controller	2–537

ANALOG TELEPHONE

Device No.	Function	Page No. or Reference
MC34010	Electronic Telephone Circuit	2–416
MC34012–1	Telephone Tone Ringer	2–440
MC34012–2	Telephone Tone Ringer	2–440
MC34012–3	Telephone Tone Ringer	2–440
MC34014	Telephone Speech Network with Dialer Interface	2–448
MC34016	Cordless Universal Telephone Interface	2–465
MC34017	Telephone Tone Ringer	2–478
MC34114	Telephone Speech Network with Dialer Interface	2–497
MC145436A	Low–Power Dual Tone Multiple Frequency (DTMF) Decoder	2–982
TCA3385	Telephone Ring Signal Converter	2–1264
TCA3388	Speech Circuit	2–1272

DATA COMMUNICATION DEVICES

Device No.	Function	Page No. or Reference
MC145488	Dual Data Link Controller (DDLC) (ISDN LAPD/LAPB)	2–1090
MC68681	Universal Asynchronous Receiver/Transmitter	MC68681/D

DIGITAL–TO–ANALOG CONVERTERS

Device No.	Function	Page No. or Reference
MC144110	6–Bit D/A Converter with Serial Interface	2–565
MC144111	6–Bit D/A Converter with Serial Interface	2–565

DIGITAL SIGNAL PROCESSING

Device No.	Function	Page No. or Reference
DSP56ADC16	Analog–to–Digital Converter	DSP56ADC16/D
DSP56000	24–bit Digital Signal Processor	DSP56000/D
DSP56001	24–bit Digital Signal Processor	DSP56001/D
DSP56002	24–bit Digital Signal Processor	DSP56002/D
DSP56156	16–bit Digital Signal Processor	DSP56156/D
DSP56200	Cascadable Adaptive Finite Impulse Response Digital Filter	DSP56200/D

DMA CONTROLLERS

Device No.	Function	Page No. or Reference
MC68440	Dual DMAC	MC68440/D
MC68450	DMA Controller (DMAC)	MC68450/D

EVALUATION KITS

Device No.	Function	Page No. or Reference
LK45162EVB	Universal Programmable Dual PLL Demonstration Board	3–3
LK45165EVB	Low–Voltage Universal Programmable Dual PLL Demonstration Board	3–5
MC145190EVK	1.1 GHz PLL Frequency Synthesizer Evaluation Kit	3–7
MC145191EVK	1.1 GHz PLL Frequency Synthesizer Evaluation Kit	3–7
MC145192EVK	2.0 GHz PLL Frequency Synthesizer Evaluation Kit	3–16
MC145200EVK	1.1 GHz PLL Frequency Synthesizer Evaluation Kit	3–7
MC145201EVK	1.1 GHz PLL Frequency Synthesizer Evaluation Kit	3–7
MC145202EVK	2.0 GHz PLL Frequency Synthesizer Evaluation Kit	3–16
MC145460EVK	Calling Line ID (CLID) Receiver Evaluation Kit	3–17
MC145536EVK	Codec–Filter/ADPCM Transcoder Evaluation Kit	3–19
MC145537EVK	MC145540 ADPCM Codec Evaluation Kit	3–21
MC145572EVK	ISDN U–Interface Transceiver II Evaluation Kit	3–21

FIBER DISTRIBUTED DATA INTERFACE (FDDI)

Device No.	Function	Page No. or Reference
MC68836	FDDI Clock Generator	MC68800/D
MC68837	Elasticity Buffer and Link Manager	MC68800/D
MC68838	Media Access Controller	MC68800/D
MC68839	FDDI System Interface	MC68800/D
MC68840	Integrated FDDI	MC68840UMAD/AD

INTEGRATED PROCESSORS

Device No.	Function	Page No. or Reference
MC68LC302	Integrated Multiprotocol Processor	MC68LC302RM/AD
MC68PM302	Integrated Multiprotocol Processor	MC68PM302RM/AD
MC68EN302	Integrated Multiprotocol Processor	MC68EN302/D
MC68MH360	Quad Integrated Communication Controller (QUICC)	MC68MH360RM/AD
MPC860ADI–PC	IF Kit for IBM–PC	MPC860/D

INTEGRATED SERVICES DIGITAL NETWORK (ISDN)

Device No.	Function	Page No. or Reference
MC145472	ISDN (2B1Q) U–Interface Transceiver	2–1019
MC1454LC72	ISDN (2B1Q) U–Interface Transceiver	2–1019
MC145474	ISDN S/T–Interface Transceiver	2–1045
MC145475	ISDN S/T–Interface Transceiver	2–1045
MC145572	ISDN U–Interface Transceiver II	2–1173
MC145574	ISDN S/T–Interface Transceiver II	2–1195

INTERFACE

Device No.	Function	Page No. or Reference
MC14C88B	Quad Low Power Line Driver	MC14C88B/D
MC14C89B	Quad Low Power Line Receivers	MC14C89B/D
MC1488	Quad MDTL Line Driver	MC1488/D

INTERFACE (CONTINUED)

Device No.	Function	Page No. or Reference
MC1489	Quad MDTL Line Receivers	MC1489/D
MC26C31	Quad EIA–422–A Line Driver	2–3
MC26C32	Quad EIA–422–A Line Receiver	2–6
MC34C86	Quad EIA–422–A Line Receiver	2–79
MC34C87	Quad EIA–422–A Line Driver	2–82
MC145403	Drivers/Receivers (3/5)	2–927
MC145404	Drivers/Receivers (4/4)	2–927
MC145405	Drivers/Receivers (5/3)	2–927
MC145406	EIA–232–E/V.28 Driver/Receiver	2–933
MC145407	5–Volt Only Driver/Receiver	2–942
MC145408	Drivers/Receivers (5/5)	2–927
MC145583	3.3 Volt to 5 Volt EIA–232–E V.28 Driver/Receiver	2–1217
MC145705	5 V Only Driver/Receiver w/Integrated Standby Mode (2–Driver/3–Receiver)	2–1223
MC145706	5 V Only Driver/Receiver w/Integrated Standby Mode (3–Driver/2–Receiver)	2–1223
MC145707	5 V Only Driver/Receiver w/Integrated Standby Mode (3–Driver/3–Receiver)	2–1223

MODEMS

Device No.	Function	Page No. or Reference
MC145442	Single Chip 300–Baud Modem (CCITT V.21)	2–988
MC145443	Single Chip 300–Baud Modem (Bell 103)	2–988
MC145444	Single Chip 300–Baud Modem with DTMF Generator (CCITT V.21)	2–998
MC145446A	Single Chip 300–Baud Modem	2–1008
MC145447	Calling Line ID (CLID) Receiver with Ring Detector	2–1009

NETWORK DEVICES

Device No.	Function	Page No. or Reference
MC68184	Broadband Interface Controller	MC68184/D
MC68185	Twisted Pair Modem	MC68185/D
MC68194	Carrierband Modem	Order via Mfax
MC68195	LocalTalk Adaptor	MC68195/D
MC68605	X.25 Protocol Controller	BR272/D
MC68606	Multi–Link LAPD Controller CCITT Q.920/Q.921	BR520/D
MC68824	Token Bus Controller	MC58824UM/AD

PHASE–LOCKED LOOP (PLL) FREQUENCY SYNTHESIZERS

Device No.	Function	Page No. or Reference
MC145106	PLL Frequency Synthesizer	2–589
MC145145–2	4–Bit Data Bus Input PLL Frequency Synthesizer	2–596
MC145146–2	4–Bit Data Bus Input PLL Frequency Synthesizer	2–607
MC145149	Dual PLL Frequency Synthesizer	2–618
MC145151–2	Parallel–Input PLL Frequency Synthesizer (Single–Modulus Prescalers)	2–628
MC145152–2	Parallel–Input PLL Frequency Synthesizer (Dual–Modulus Prescalers)	2–628
MC145155–2	Serial–Input PLL Frequency Synthesizer (Single–Modulus Prescalers)	2–628
MC145156–2	Serial–Input PLL Frequency Synthesizer (Dual–Modulus Prescalers)	2–628
MC145157–2	Serial–Input PLL Frequency Synthesizer (Single–Modulus Prescalers)	2–628
MC145158–2	Serial–Input PLL Frequency Synthesizer (Dual–Modulus Prescalers)	2–628
MC145159–1	Serial–Input PLL Frequency Synthesizer with Analog Phase Detector	2–659
MC145162	60 MHz Universal Programmable Dual PLL Frequency Synthesizer	2–668
MC145162–1	85 MHz Universal Programmable Dual PLL Frequency Synthesizer	2–668
MC145165	Low–Voltage 60 MHz Universal Programmable Dual PLL Frequency Synthesizer	2–690
MC145166	4–Bit Parallel Dual PLL for 46/49 MHz Cordless Telephones	2–712
MC145167	Serial–Input Dual PLL for 46/49 MHz Cordless Telephones	2–712
MC145168	4–Bit Input Dual PLL for 46/49 MHz Cordless Telephones	2–721
MC145169	Serial–Input Dual PLL for 46/49 MHz Cordless Telephones	2–721
MC145170	PLL Frequency Synthesizer with Serial Interface (160 MHz)	2–730
MC145170–1	PLL Frequency Synthesizer with Serial Interface (160 MHz)	2–748
MC145173	Dual Band PLL Frequency Synthesizer	2–772
MC145190	1.1 GHz PLL Frequency Synthesizer (30/130 MHz)	2–802

PHASE–LOCKED LOOP (PLL) FREQUENCY SYNTHESIZERS (CONTINUED)

Device No.	Function	Page No. or Reference
MC145191	1.1 GHz PLL Frequency Synthesizer	2–802
MC145192	Low Voltage 1.1 GHz PLL Frequency Synthesizer	2–824
MC145200	2.0 GHz PLL Frequency Synthesizer	2–846
MC145201	2.0 GHz PLL Frequency Synthesizer	2–846
MC145202	Low–Voltage 2.0 GHz PLL Frequency Synthesizer	2–867
MC145220	Dual 1.1 GHz PLL Frequency Synthesizer	2–889

REMOTE CONTROL FUNCTIONS

Device No.	Function	Page No. or Reference
MC14469	Addressable Asynchronous Receiver/Transmitter	2–241
MC14489	Multi–Character LED Display	2–249
MC14497	PCM Remote Control Transmitter	2–268
MC14499	7–Segment LED Display Decoder/Driver with Serial Interface	2–274
MC44107	IR Remote Control Transmitter	2–557
MC145026	Encoder	2–571
MC145027	Decoder	2–571
MC145028	Decoder	2–571
MC145750	QPSK Encoder	2–1230
SC41343	Encoder	2–571
SC41344	Encoder	2–571

RF COMMUNICATIONS

Device No.	Function	Page No. or Reference
MC2833	Low Power FM Transmitter System	2–9
MC3356	Wideband FSK Receiver	2–16
MC3357	Low Power FM IF	2–22
MC3359	High Gain Low Power FM IF	2–26
MC3361C	Low Power FM IF	2–32
MC3362	Low Power Dual Conversion FM Receiver	2–38
MC3363	Low Power Dual Conversion FM Receiver	2–46
MC3371	Low Power Narrowband FM IF	2–54
MC3372	Low Power Narrowband FM IF	2–54
MC3374	Low Voltage Single Conversion FM Receiver	2–71
MC13055	Wideband FSK Receiver	2–104
MC13109	Universal Cordless Telephone Subsystem IC	2–111
MC13110	Universal Cordless Telephone Subsystem IC with Scrambler	2–149
MC13135	Dual Conversion Narrowband FM Receiver	2–166
MC13136	Dual Conversion Narrowband FM Receiver	2–166
MC13141	Low Power DC — 1.8 GHz LNA and Mixer	2–178
MC13142	Low Power DC — 1.8 GHz LNA, Mixer and VCO	2–180
MC13143	Ultra Low Power DC — 2.4 GHz Linear Mixer	2–182
MC13150	Narrowband FM Coilless Detector IF Subsystem	2–184
MC13155	Wideband FSK Receiver	2–186
MC13156	Wideband FM IF System	2–201
MC13158	Wideband FM IF Subsystem	2–220
MC13173	Infrared Integrated Transceiver IC	MC13173/D
MC13175	UHF FM/AM Transmitter	MC13175/D
MC13176	UHF FM/AM Transmitter	MC13175/D
MRFIC2001	900 MHz Downconverter LNA/Mixer	MRFIC2001/D
MRFIC2002	900 MHz Transmit Mixer	MRFIC2002/D
MRFIC2003	900 MHz GaAs Antenna Switch	MRFIC2003/D
MRFIC2004	900 MHz Driver and Ramp	MRFIC2004/D
MRFIC2006	900 MHz Two Stage Power Amplifier	MRFIC2006/D

SPEAKERPHONES

Device No.	Function	Page No. or Reference
MC33218A	Voice Switched Speakerphone with Microprocessor Interface	2–363
MC33219A	Voice Switched Speakerphone	2–390
MC34018	Voice Switched Speakerphone Circuit	2–483
MC34118	Voice Switched Speakerphone Circuit	2–516

SPEECH NETWORKS

MC34216	Programmable Telephone Line Interface Circuit with Loudspeaker Amplifier	2–552
MC145421	Universal Digital Loop Transceiver II (UDLT II)	2–949
MC145422	Universal Digital Loop Transceiver (UDLT)	2–963
MC145425	Universal Digital Loop Transceiver II (UDLT II)	2–949
MC145426	Universal Digital Loop Transceiver (UDLT)	2–963

SUBSCRIBER LOOP INTERFACE CIRCUITS (SLICS)

Device No.	Function	Page No. or Reference
MC33120	Subscriber Loop Interface Circuit	2–303
MC33121	Low Voltage Subscriber Loop Interface Circuit	2–333

VOICE CODING

Device No.	Function	Page No. or Reference
MC3418	CVSD Modulator/Demodulator (4–Bit Algorithm)	2–85
MC33110	Low–Voltage Compander	2–280
MC33111	Low–Voltage Compander	2–292
MC34115	CVSD Modulator/Demodulators	2–515
MC145402	Serial 13–Bit Linear Codec (A/D and D/A)	2–914
MC145480	5 V PCM Codec–Filter	2–1067
MC145481	3 V PCM Codec–Filter	2–1081
MC145500	Codec–Filter (Mono–Circuit; 16–Pin)	2–1101
MC145501	Codec–Filter (Mono–Circuit; 18–Pin)	2–1101
MC145502	Codec–Filter (Mono–Circuit; 22–Pin)	2–1101
MC145503	Codec–Filter (Mono–Circuit; 16–Pin)	2–1101
MC145505	Codec–Filter (Mono–Circuit; 16–Pin)	2–1101
MC145532	ADPCM Transcoder	2–1124
MC145540	ADPCM Codec	2–1139
MC14LC5540	ADPCM Codec	2–1140
MC145541	ADPCM Codec	2–1156
MC145554	PCM Codec–Filter (16–Pin)	2–1157
MC145557	PCM Codec–Filter (16–Pin)	2–1157
MC145564	PCM Codec–Filter (20–Pin)	2–1157
MC145567	PCM Codec–Filter (20–Pin)	2–1157

OTHER FUNCTIONS

Device No.	Function	Page No. or Reference
MC68HC68T1	Real Time Clock with RAM plus Serial Interface	2–1240
MJD243	4–A Silicon Power Transistor	MJD243/D
MJD253	4–A Silicon Power Transistor	MJD243/D
MPS6717	NPN One Watt Amplifier Transistors	MPS6717/D
4N35/36/37	Optoisolators	4N35/D

NOT RECOMMENDED FOR NEW DESIGN

The following devices are Not Recommended For New Design. Replacement parts are listed if available.

Device No.	Function	Replacement Part
MC14411	Bit Rate Generator	
MC142103	Encoder	
MC145030	Encoder/Decoder	
MC145031	Encoder	
MC145032	Decoder	
MC145033	Encoder/Decoder	
MC145034	Encoder	
MC145035	Decoder	
MC145160	4–Bit Parallel Dual PLL for 46/49 MHz Cordless Telephones	
MC145161	Dual PLL for 30/39 MHz Cordless Telephones	
MC145411	Bit Rate Generator	
MC145414	Dual Tunable Low–Pass Sampled Filter	
MC145428	Data Set Interface	
MC145412	Pulse/Tone Repertory Dialer	

NOT RECOMMENDED FOR NEW DESIGN (CONTINUED)

Device No.	Function	Replacement Part
MC145413	Pulse/Tone Repertory Dialer	
MC145416	Tone/Pulse Dialer with 10 Number Memory Plus 3 Emergency Numbers	
MC145436	Dual Tone Multiple Frequency (DTMF) Decoder	MC145436A
MC145540	ADPCM Codec	MC14LC5540
MC145512	Pulse/Tone Repertory Dialer	
MC14LC5494EVK	ISDN U–Interface Transceiver Evaluation Kit	

DISCONTINUED

The following devices are Discontinued. Replacement parts are listed if available.

Device No.	Function	Replacement Part
MC14400	Single–Chip Codec–Filter (Mono–Circuit)	
MC14401	Single–Chip Codec–Filter (Mono–Circuit)	
MC14402	Single–Chip Codec–Filter (Mono–Circuit)	
MC14403	Single–Chip Codec–Filter (Mono–Circuit)	
MC14405	Single–Chip Codec–Filter (Mono–Circuit)	
MC14413–1, –2	PCM Band–Pass/Low–Pass Filter	
MC14414–1, –2	PCM Dual Low–Pass Filter	
MC142100	4 × 4 Crosspoint Switch with Control Memory	
MC143403	Quad Line Driver	
MC143404	Quad Line Driver	
MC145100	4 × 4 Crosspoint Switch with Control Memory	
MC145418	80 kbps Digital Loop Transceiver (Master)	
MC145419	80 kbps Digital Loop Transceiver (Slave)	
MC145433	Tunable Notch/Band–Pass Filter	
MC145439	Encoder/Decoder	
MC145440	300 Baud Modem Filter (Bell 103)	
MC145441	300 Baud Modem Filter (CCITT V.21)	
MC145445	300 Baud Modem (Bell 103/CCITT V.21)	
MC145542	CT2 Speech and Framing IC	MC14LC5542
MC145610	Pulse Tone Dialer with Last Number Redial	

CANCELLED

The following devices are Cancelled. Replacement parts are listed if available.

Device No.	Function	Replacement Part
MC145415	Dual Tunable Linear Phase Low–Pass Sampled Data Filter	
MC145429	Teleset Audio Interface Circuit (TAIC)	
MC145432	2600 Hz Signaling Filter	
MC145611	PCM 8–Channel Conference Circuit	

Technical Selection Guide

This selection guide includes all Motorola devices characterized in this book, as well as other devices that can be found in Linear/Interface ICs Device Data (DL128/D).

RF COMMUNICATIONS

AM and Wideband FM Transmitters

Device	V_{CC}	I_{CC}	Output Power	Max RF Input Freq.	Max Mod. Freq.	Data Rate (Baud)	Notes	Suffix/ Case	Page
MC13173	3 – 5 V	6. mA	—	10.7 MHz	—	200 kb	Includes Single Frequency PLL for Tx Carrier and Rx L_O.	FTB/873	DL128
MC13175	2 – 5 V	40 mA	8.0 dBm	500 MHz	5 MHz	10 M	AM/FM Transmitter; Single Frequency PLL, $f_{OUT} = 8 \times f_{REF}$	P/648 D/751B	DL128
MC13176	2 – 5 V	40 mA	8.0 dBm	1 GHz	5 MHz	10 M	AM/FM Transmitter; Single Frequency PLL, $f_{OUT} = 32 \times f_{REF}$	P/648 D/751B	DL128

CT–1 Subsystem ICs

Device	Notes	Suffix/ Case	Page
MC13109	Integrates many functions required for cordless telephone: dual conversion FM receiver with RSSI, detector, compander, dual programmable PLL, and low battery detect.	FTA/932 FB/848B	2–111
MC13110	Integrates many functions required for cordless telephone into a single integrated circuit: dual conversion FM receiver, scrambler, detector, RSSI, compander, dual programmable PLL, and low battery detect.	FB/848B	2–149

RF/Mixers

Device	Notes	Suffix/ Case	Page
MC13141	Low drain current (7.5 mA/14 mA), IIP3 – 5 dBm LNA, + 20 dBm Mixer w/linearity control, Ton/off < 1 µs, VCO buffer to drive prescaler. VCO has emitter, base, collector pinned out.	D/751 D/751B	2–178
MC13142			2–180
MC13143			2–182

Single Conversion Receivers

Device	Notes	Suffix/ Case	Page
MC13150	Linear coilless detector, 2.3 to 6.0 Vdc, < 2.0 mA, 0 dBm IIP3, Adjustable demodulator bandwidth.	FTB/873	2–184
MC13158	1.8 to 6.0 Vdc, > 600 kHz detector bandwidth, data slicer w/special off function, > 80 dB RSSI, low power consumption in active/standby modes.	FTB/873	2–220

Wideband Single Conversion Receivers

Device	V_{CC}	I_{CC}	12 dB SINAD Sensitivity (Typ)	Input RF Freq.	IF	Mute	RSSI	Data Rate (Baud)	Notes	Suffix/ Case	Page
MC3356	3 – 9 V	25 mA	30 µV	200 MHz	10.7 MHz	Yes	Yes	50k	Includes squelch and data shaper	P/738 DW/751D	2–16
MC13156	2 – 7 V	3 mA	2 µV	500 MHz	21.4 MHz	No	Yes	1 M	CT–2 FM demodulator split IF	DW/751E	2–201

RF COMMUNICATIONS (continued)

Wideband IFs

Device	V_{CC}	I_{CC}	12 dB SINAD Sensitivity (Typ)	IF	Mute	RSSI	Data Rate (Baud)	Notes	Suffix/ Case	Page
MC13055	3 – 12 V	25 mA	20 µV	40 MHz	Yes	Yes	2 M	Wideband, includes data shaper	P/648 D/751B	2–104
MC13155	3 – 6 V	10 mA	100 µV	250 MHz	No	Yes	10 M	Video speed	D/751B	2–186

Narrowband FM Transmitters

Device	V_{CC}	I_{CC}	Output Power	Max RF Input Freq.	Max Mod. Freq.	Data Rate (Baud)	Notes	Suffix/ Case	Page
MC2833	3 – 8 V	10 mA	– 30 dBm to + 10 dBm	150 MHz	50 kHz	4.8k	FM Transmitter — Includes two frequency multiplier/amplifier transistors	P/648 D/751B	2–9

Narrowband Single Conversion Receivers

Device	V_{CC}	I_{CC}	12 dB SINAD Sensitivity (Typ)	Input RF Freq.	IF	Mute	RSSI	Data Rate (Baud)	Notes	Suffix/ Case	Page
MC3357	4 – 8 V	5 mA	5 µV	45 MHz	455 kHz	Yes	No	> 4.8k	Ceramic Quad Detector/Resonator	P/648	2–22
MC3359	4 – 9 V	7 mA	2 µV	45 MHz	455 kHz	Yes	No	> 4.8k	Scan Output Option	P/707 DW/751D	2–26
MC3361C	2 – 8 V	6 mA	2 µV	60 MHz	455 kHz	Yes	No	> 4.8k	Lowest Cost Receiver	P/648 D/751B	2–32
MC3371	2 – 8 V	6 mA	2 µV	60 MHz	455 kHz	Yes	No	> 4.8k	RSSI	P/648 D/751B	2–54
MC3372	2 – 8 V	6 mA	2 µV	60 MHz	455 kHz	Yes	No	> 4.8k	RSSI, Ceramic Quad Detector/Resonator	P/648 D/751B	DL128
MC3374	1 – 5 V	1 mA	1 µV	75 MHz	455 kHz	Yes	No	> 4.8k	1 Cell Operation	DW/751F	2–71

Narrowband Dual Conversion Receivers

Device	V_{CC}	I_{CC}	12 dB SINAD Sensitivity (Typ)	Input RF Freq.	IF1	IF2	Mute	RSSI	Data Rate (Baud)	Notes	Suffix/ Case	Page
MC3362	2 – 7 V	3 mA	0.7 µV	180 MHz	10.7 MHz	455 kHz	No	Yes	> 4.8k	Includes buffered VCO output	DW/751E	2–38
MC3363	2 – 7 V	4 mA	0.4 µV	180 MHz	10.7 MHz	455 kHz	Yes	Yes	> 4.8k	Includes RF Preamp and Mute	DW/751F	2–46
MC13135	2 – 7 V	4 mA	1 µV	180 MHz	10.7 MHz	455 kHz	No	Yes	> 4.8k	Voltage buffered RSSI, LC Quad Detector	DW/751E	2–166
MC13136	2 – 7 V	4 mA	1 µV	180 MHz	10.7 MHz	455 kHz	No	Yes	> 4.8k	Voltage buffered RSSI, Ceramic Quad Detector	DW/751E	2–166

LOW–POWER OPERATIONAL AMPLIFIER

Device	SR V/μs (Typ)	GBW MHz (Typ)	V_{IO} mV (Max)	I_{IB} μA (Max)	I_D mA (Max/ amp)	I_{SC} mA (Typ)	e_n nV/√Hz (Typ)	Temp Range °C	Notes	Suffix/ Case	Page
MC33102 (Awake) (Sleep)	 1.0 0.1	 4.0 0.3	 2.0 2.0	 500 nA 50 nA	 — —	 6.0 6.0	 50 25	– 40 to 85	Dual	P/626 D/751	DL128
MC33171	2.1	—	4.5	0.1	—	—	—	– 40 to 85	Low Power, Single Supply	P/626 D/751	DL128
MC33178 MC33179	2.0	5.0	3.0	0.5	0.7	80	7.5	– 40 to 85	Dual/Quad	P/626	DL128
MC33201	1.0	2.2	6.0	200 nA	—	—	—	– 40 to 85	Low V Rail–to–Rail	P/626 D/751	DL128
MC33304	1.0	3.0	13.0	250 nA	—	—	—	– 40 to 85	Rail–to–Rail, Sleepmode Two–State Op Amp	P/646 D/751A	DL128

REMOTE CONTROL

Function	Number of Address Lines	Maximum Number of Address Codes	Number of Data Bits	Operation	Device	Suffix/Case	Page
Addressable VART	7	128	7/8	Full Duplex	MC14469	P/711, FN/777	2–241
Transmitter	0	0	6	Simplex	MC14497	P/707	2–268
Transmitter	0	0	9	Simplex	MC44107	P/738	2–557
Encoder	Depends on Decoder(1)	Depends on Decoder(1)	Depends on Decoder(1)	Simplex	MC145026	P/648 D/751B	2–571
Decoder	5	243	4	Simplex	MC145027	P/648 DW/751G	2–571
	9	19,683	0		MC145028		
	5	243	4		SC41343	P/648, DW/751B	2–571
	9	19,683	4		SC41344	P/648	2–571

(1)See MC145027, MC145028

DECODERS/DISPLAY DRIVERS

Display Type	Input Format	Drive Capability Per Package	On–Chip Latch	Display Control Inputs	Segment Drive Current	Device	Suffix/Case	Page
LED — 1/5 Mux	Serial Binary	5 Characters + Decimals or 25 Lamps	Yes	Blank, Dim	0 to 35 mA (Peak) Adjustable Current Source	MC14489	P/738, DW/751D	2–249
LED — 1/4 Mux	Serial Binary	4 Digits + Decimals	Yes	—	50 mA (Peak)	MC14499	P/707, DW/751D	2–274

SWITCH MODE CONTROLLER

I_O (mA) Max	Minimum Operating Voltage Range (V)	Operating Mode	Reference (V)	Maximum Useful Oscillator Frequency (kHz)	Device	T_A (°C)	Suffix/ Case	Page
1000 (Totem Pole MOSFET Driver Output)	4.2 to 12	Current	1.25 ± 2.0%	300	MC34129	0 to + 70	P/646 D/751A	2–537
					MC33129	– 40 to + 85	P/646 D/751A	2–537

DIGITAL–TO–ANALOG CONVERTERS

Function	I/O Format	Resolution	Number of Analog Channels	Other Features	Device	Suffix/ Package	Page
DAC	Serial	6 Bits	6	Emitter–Follower Outputs	MC144110	P/707, DW/751D	2–565
			4		MC144111	P/646, DW/751G	2–565

EIA–232/562/V.28 DRIVERS/RECEIVERS

Drivers	Receivers	Power Supplies (V)	Features	Device	Suffix/ Package	Page
—	4	+ 5.0	EIA–232/EIA–562 V.28	MC14C89B	P/646, D/751A	DL128
—	4	+ 5.0	EIA–232/V.28	MC1489	P/646, D/751A	DL128
4	—	± 7.0 to ± 12	EIA–232/EIA–562 V.28	MC14C88B	P/646, D/751A	DL128
4	—	± 9.0 to ± 12	EIA–232/V.28	MC1488	P/646, D/751A	DL128
3	5	± 5.0 to ± 12	EIA–232/V.28	MC145403	P/738 DW/751D	2–927
4	4			MC145404		
5	3			MC145405		
3	3			MC145406	P/648, DW/751G, SD/940B	2–933
3	3	+ 5.0	EIA–232/V.28; Charge Pump	MC145407	P/738, DW/751D	2–942
5	5	± 5.0 to ± 12	EIA–232/V.28	MC145408	P/724, DW/751E	2–927
3	5	+ 3.3 to + 5.0	EIA–232/V.28; Onboard Ring Monitor Circuit; Charge Pump Power Down	MC145583	SD/940J	2–1217
2	3	+ 5.0	EIA–232/V.28; Charge Pump, Power Down	MC145705	P/738 DW/751D	2–1223
3	2			MC145706		
3	3			MC145707	P/724, DW/751E	

EIA–422 DRIVERS/RECEIVERS

Drivers	Receivers	Power Supplies (V)	Features	Device	Suffix/ Package	Page
4	—	+ 5.0	Pin compatible with AM26LS31. Enable and disable common to all four drivers. Typical ESD protection of 2 kV.	MC26C31	P/648, D/751B	2–3
—	4	+ 5.0	Pin compatible with AM26LS32. Enable and disable common to all four receivers. Typical ESD protection of 2 kV.	MC26C32	P/648, D/751B	2–6
—	4	+ 5.0	Pin compatible with MC3486. Typical ESD protection of 2 kV.	MC34C86	P/648, D/751B	2–79
4	—	+ 5.0	Pin compatible with MC3487. Typical ESD protection of 2 kV.	MC34C87	P/648, D/751B	2–82

PHASE–LOCKED LOOP FREQUENCY SYNTHESIZERS

Frequency (MHz)	Supply Voltage (V)	Nominal Supply Current (mA)	Phase Detector	Standby	Interface	Device	Suffix/ Case	Page
4 @ 5 V	4.5 to 12	6 @ 5 V	Single–ended three–state	No	Parallel	MC145106	P/707 DW/751D	2–589
15 @ 5 V	3.0 to 9.0	—	Two single–ended three–state		Serial	MC145149*	P/738 DW/751D	2–618
		7.5 @ 5 V	Analog			MC145159–1	P/738 DW/751D	2–659
20 @ 5 V	3.0 to 9.0	7.5 @ 5 V	Single–ended three–state, double–ended	No	4–Bit	MC145145–2	P/707 DW/751D	2–596
						MC145146–2	P/738 DW/751D	2–607
					Parallel	MC145151–2	P/710 DW/751F	2–628
			Double–ended			MC145152–2	P/710 DW/751F	2–628
			Single–ended three–state, double–ended		Serial	MC145155–2	P/707 DW/751D	2–628
						MC145156–2	P/707 DW/751D	2–628
						MC145157–2	P/648 DW/751G	2–628
						MC145158–2	P/648 DW/751G	2–628
60 @ 3 V	2.5 to 5.5	3.0 @ 3 V	Two single–ended three–state	Yes	Serial	MC145162*	P/648 DW/751G	2–668
						MC145162–1*	P/648, DW/751G	2–668
						MC145165*	P/648, DW751B	2–690
					Parallel	MC145166*	P/648 DW/751G	2–712
					Serial	MC145167*	P/648 DW/751G	2–712
					Parallel	MC145168*		2–721
					Serial	MC145169*		2–721
100 @ 3 V 160 @ 5 V	2.5 to 6.0	3.0 @ 3 V 7.0 @ 5 V	Single–ended three–state, double–ended	No	Serial	MC145170	P/648 D/751B	2–730

PHASE–LOCKED LOOP FREQUENCY SYNTHESIZERS (continued)

Frequency (MHz)	Supply Voltage (V)	Nominal Supply Current (mA)	Phase Detector	Standby	Interface	Device	Suffix/ Case	Page
100 @ 3 V 180 @ 5 V	2.5 to 5.5	TBD	Single–ended three–state, double–ended	No	Serial	MC145170–1	P/648 D/751B	2–748
40/130 @ 5 V	4.5 to 5.5	25 @ 5 V	Single–ended three–state, Current source/sink	Yes	Serial	MC145173	DW/751E	2–772
1100 @ 5 V	4.5 to 5.5	7.0 @ 5 V	Current source/sink, double–ended	Yes	Serial	MC145190	F/751J DT/948D	2–802
						MC145191	F/751J DT/948D	2–802
1100 @ 3 V	2.7 to 5.0	6.0 @ 2.7 V				MC145192	F/751J DT/948D	2–824
2000 @ 5 V	4.5 to 5.5	12 @ 5 V	Current source/sink, double–ended			MC145200	F/751J DT/948D	2–846
2000 @ 5 V	4.5 to 5.5	12 @ 5 V				MC145201	F/751J DT/948D	2–846
2000 @ 3 V	2.7 to 5.5					MC145202	F/751J DT/948D	2–867
1100 @ 3 V	2.7 to 5.5	12	Two current source/sink, double–ended	Yes	Serial	MC145220*	F/803C DT/948D	2–889

* Dual PLL.

TELECOM CIRCUITS

Audio Amplifiers

Function	Features	Device	Suffix/ Case	Page
Low Voltage Audio Amp	400 mW, 8.0 to 100 Ω, 2.0 to 16 V, differential outputs, chip–disable input pin	MC34119	P/626 D/751	2–536

Complete Telephone Circuit

Function	Features	Device	Suffix/Case	Page
POTS circuit + MPU Dialing	Speech network, tone ringer, DC loop current interface, DTMF dialer with serial port control	MC34010	P/711 FN/777	2–416

Companders

Function	Features	Device	Suffix/Case	Page
Basic Compander	2.7 to 7 V, no precision externals, 80 dB range, –40 to +85°C, independent compressor and expander	MC33110	P/646 D/751A	2–280
Compander with features	3.0 to 7.0 V, no precision externals, 80 dB range, – 40 to + 85°C, independent compressor and expander, pass through and mute functions, two op amps	MC33111	P/648 DW/751B	2–292

Dialers

Function	Features	Device	Suffix/Case	Page
Dual Tone Multiple Frequency Receiver	Pin compatible with SSI204. Single + 5 V supply. Detects all 16 tones. Provides guard time controls for improved speech immunity. Output in 4–bit hexadecimal code.	MC145436A	P/646 DW/751G	2–982

Integrated Services Digital Network (ISDN)

Function	Features	Device	Suffix/Case	Page
Line Cards, NT1s, Pair Gain, ISDN Compatible Bridge Routers, ISDN Terminals	ANSI T1.601 compliant, pin selectable LT or NT operation, industry standard IDL interface, slave–slave timing mode, control and status provided through four–wire serial control port	MC145472	FE/847B	2–1019
	500 mW die shrink version of the MC145472	MC14LC5472	FE/847B FU847	2–1019
Network Termination (NT1), PC Based and Standalone ISDN Terminal Adaptors, ISDN Telephone, ISDN Video Phones	Conforms to CCITT I.430 and ANSI T1.605, pin selectable NT and TE modes, Interchip Digital Link (IDL), serial control port (SCP), full multiframing capabilities, NT1 star mode, S/T and IDL loopbacks	MC145474	L/736B	2–1045
		MC145475	DW/751D	2–1045
Line Cards, NT1s, Pair Gain, ISDN Compatible Bridge Routers, ISDN Terminals	Enhanced version of the MC14LC5472, low power; 300 mW, ANSI T1.601 compliant, pin selectable LT or NT operation, IDL and GCI interfaces, timeslot assigner, parallel or serial control ports	MC145572	FN/777 FE/824A	2–1173
Network Termination (NT1), PC Based and Standalone ISDN Terminal Adaptors, ISDN Telephone, ISDN Video Phones, PBX Applications, Combination Network Termination/Terminal Adaptor (NT1/TA)	Conforms to CCITT I.430 and ANSI T1.605, pin selectable NT and TE modes, Interchip Digital Link (IDL), serial control port (SCP), full multiframing capabilities, NT1 star mode, S/T and IDL loopbacks, backwards software compatible with the MC145474/75, low power consumption, general circuit interface (GCI), timeslot assigner, NT terminal mode, slave/slave mode	MC145574	DW/751F	2–1195

Modems

Function	Features	Device	Suffix/Case	Page
Single Chip 300 Baud Modem	CCITT V.21 compatible. Capable of driving – 9 dBm into 600 Ω. Internal mid–supply generator. Uses color burst XTAL. Adjustable transmit level and CD delay timing.	MC145442	P/738 DW/751D	2–988
Single Chip 300 Baud Modem	Bell 103 compatible. Capable of driving – 9 dBm into 600 Ω. Internal mid–supply generator. Uses color burst XTAL. Adjustable transmit level and CD delay timing.	MC145443	P/738 DW/751D	2–988
Single Chip 300 Baud Modem	CCITT V.21 compatible. Capable of driving 0 dBm into 600 Ω. Uses color burst XTAL. Adjustable transmit level and CD delay timing. On–chip DTMF generator and imprecise call progress detection. 3–wire serial interface.	MC145444	H/804 DW/751D	2–998
Multi–Function 300 Baud Modem	CCITT V.21 compatible. Capable of driving 0 dBm into 600 Ω. Uses color burst XTAL. Adjustable transmit level and CD delay timing. On–chip DTMF Transceiver and imprecise call progress detection. 3–wire serial interface.	MC145446A	FW/751M	2–1008
Adjust Box, Telephones, Fax Machines, Answering Machines, Key Systems, Transaction Terminals	Low–power mode, 3.5 V to 6.5 V operating range, high–performance Bell 202/V.23 demodulator, on–chip ring detector, pin selectable oscillator frequencies: 3.68 MHz, 3.58 MHz, or 455 kHz.	MC145447	P/648 DW/751G	2–1009

Subscriber Loop Interface Circuits (SLICs)

Function	Features	Device	Suffix/Case	Page
Central Office, Remote Terminals, PBX Applications	All gains externally programmable, most BORSHT functions, current limit adjustable to 50 mA, 58 dB Longitudinal Balance, –42 to –58 V	MC33120	P/738 FN/776	2–303
Central Office, Remote Terminals, PBX Applications	All gains externally programmable, most BORSHT functions, current limit adjustable to 50 mA, 58 dB Longitudinal Balance, –21.6 to –42 V	MC33121	P/738 FN/776	2–333

TELECOM CIRCUITS (continued)

Speakerphone Circuits

Function	Features	Device	Suffix/Case	Page
Complete Speakerphone with MPU Interface	All level detection, attenuators, and switching controls, mike amp, MPU interface for: volume control, mode selection, mike mute	MC33218A	P/724 DW/751E	2–363
Complete Basic Speakerphone	All level detection, attenuators, and switching controls for basic half–duplex operation. Adjustable gain on mike amp and receive amp. Volume and mute control inputs. + 2.7 to 6.5 volt @ 3.2 mA	MC33219A	P/724 DW/751E	2–390
Complete Speakerphone with Speaker Amplifier	All level detection (2 pt.), attenuators, and switching controls, mike, and speaker amp	MC34018	P/710 DW/751F	2–483
Complete Speakerphone with Hybrid, Filter	All level detection (4 pt.), attenuators, and switching controls, mike amp with mute, hybrid, and filter	MC34118	P/710 DW/751F	2–516

Universal Digital Loop Transceivers

Function	Device	Features	Suffix/Case	Page
Universal Digital Loop Transceivers	MC145421	Provides synchronous full duplex 160 kbps voice and data communication in a 2B+2D format for ISDN compatibility on a single twisted pair up to 1 km. Single 5 V power supply, protocol independent.	P/709, DW/751E	2–949
	MC145425			2–949
Universal Digital Loop Transceivers II	MC145422	Provides synchronous full duplex 80 kbps voice and data communication in a 1B+1D format on a single twisted pair up to 2 km. Single 5 V power supply, protocol independent.	P/708, DW/751E	2–963
	MC145426			2–963

Speech Networks

Function	Features	Device	Suffix/Case	Page
Basic Phone Line Interface	Loop current interface, speech network, line length compensation, speech/dialing modes, Bell system compliant.	MC34014	P/707 D/751D	2–448
Cordless Universal Telephone Interface	For cordless telephone base for CT0, CT1, CT2, and DECT. European DC masks, double wheatstone bridge sidetone circuit, SPI port for masks, AGC, hookswitch, and mute and gain settings. Requires + 5 V and µP.	MC34016	P738 DW/751D	2–465
Basic Phone Line Interface	Loop current interface, speech network, line length compensation, speech/dialing modes, Bell system and foreign countries.	MC34114	P/707 D/751D	2–497
European Speech Network, Programmable Speaker Amplifier	Line powered, European DC masks, DTMF and pilot tone generator, listening–in mode with anti–howling. 2–wire bus to control masks, DTMF tones, speaker gain, pulse dialing, mute, AGC. Requires µP.	MC34216	DW/751F	2–552
European Speech Network	Loop current interface, speech network, line length compensation, speech/dialing modes, programmable masks for French, UK, low voltage, and PABX systems.	TCA3388	DP/738 FP/751	2–1272

Tone Ringers

Function	Features	Device	Suffix/Case	Page
Adjustable Tone Ringer	Single–ended output, meets FCC requirements, adjustable REN, different warble rates	MC34012 –1, –2, –3	P/626 D/751	2–440
Adjustable Tone Ringer	Differential output, meets FCC requirements, adjustable REN, different warble rates	MC34017 –1, –2, –3	P/626 D/751	2–478
Adjustable Tone Ringer	Differential output, meets FCC requirements, adjustable REN, different warble rates	MC34217	P/626 D/751	2–362
Ring Signal Converter	Switching regulator to convert ringing voltage to regulated DC output. Provides ring detect output	TCA3385	P/626 FP/751	2–1264

TELECOM CIRCUITS (continued)

Voice Coding

Function	Features	Device	Suffix/Case	Page
13–Bit Linear ADC and DAC	60 dB typ signal–to–distortion, serial data port, sample rate from 100 Hz to 16 Hz, ± 5 V power supply. 2's complement data coding.	MC145402	L/620, DW/751G	2–914
5 V PCM Codec–Filter	23 mW typ power dissipation, Mu–/A–Law pin selectable	MC145480	P/738, DW/751D, SD/940C	2–1067
3 V PCM Codec–Filter	10 mW typ power dissipation, Mu–/A–Law pin selectable	MC145481	P/738, DW/751D, SD/940C	2–1089
Dual Data Link Controller	Two–channel ISDN LAPD controller with on–chip direct memory access (DMA) controller. Two independent full–duplex bit–oriented protocol controllers, and compatible with 68000 and 80186 bus structures.	MC145488	FN/779	2–1090
PCM Codec–Filter	± 5 V or single 10 to 12 V, pin selectable Mu–/A–Law, serial PCM port	MC145502	P/708, FN/776	2–1101
		MC145503	P/648 DW/751G	
		MC145505		
Digital Cordless Telephone/ Base Station, T1 Multiplier	5 V ADPCM transcoder that is CCITT G.721, G.723, and G.726 compliant for 24 and 32 kbps with proprietary 16 kbps mode. Mu–Law and A–Law compatible.	MC145532	L/620, DW/751G	2–1124
3 V ADPCM Codec Replaces MC145540	PCM Codec–Filter with ADPCM transcoder, 64 kbps Mu–/A–Law. 32, 24, or 16 G.726 ADPCM encoder and decoder, 43 mW typ power at 3V, includes high–gain mic amp, receiver power driver, auxiliary driver, sidetone and gain controls	MC14LC5540	P/710, DW/751F, FU873	2–1140
2 V ADPCM Codec	PCM Codec–Filter with ADPCM transcoder, 64 kbps Mu–/A–Law. 32, 24, or 16 G.726 ADPCM encoder and decoder, 20 mW typ power at 3V, access to PCM and ADPCM, includes high–gain mic amp, receiver power driver, auxiliary driver, encoder VOX, decoder comfort noise generator, sidetone and gain controls	MC145541	TBD	2–1156
± 5 V PCM Codec–FIlter	Dual power supply PCM Codec–Filter. Industry pinout with serial PCM interface	MC145554	P/648, DW/751G	2–1157
		MC155557		
		MC145564	P/738, DW/751D	
		MC145567		

Voice Encoders/Decoders

Function	Features	Device	Suffix/Case	Page
Continuously Variable Slope Delta (CVSD) Modulator/Demodulator	Telephone quality voice encoding/decoding, variable clock rate, 3–bit coding for secure communications, voice storage/retrieval, answering machines, 0 – 70°C	MC34115	P/738 DW/751G	2–515
	Same as MC34115, except 4–bit coding	MC3418	P/738 DW/751G	2–85

Data Sheets

2

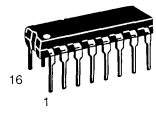
2

MC26C31

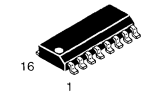
Product Preview

Quad EIA-422-A Line Driver

CMOS



P SUFFIX
PLASTIC DIP
CASE 648



D SUFFIX
SOG PACKAGE
CASE 751B

ORDERING INFORMATION

MC26C31P	Plastic DIP
MC26C31D	SOG Package

2

The MC26C31 is a quad differential line driver designed for digital data transmission over balanced lines. The MC26C31 meets all the requirements of standard EIA–422–A while retaining the low–power characteristics of CMOS.

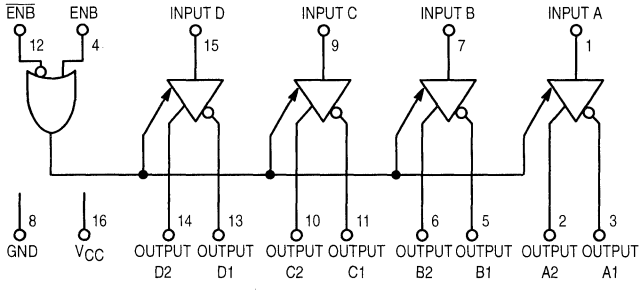
The MC26C31 accepts TTL or CMOS input levels and translates these to EIA–422–A output level. This part uses special output circuitry that enables the individual drivers to power down without loading down the bus. The MC26C31 also includes special circuitry which will set the outputs to a high impedance mode during power up or down, preventing spurious glitches. This device has enable and disable circuitry common for all four drivers.

The MC26C31 is pin compatible with the AM26LS31.

All pins are protected against damage due to electrostatic discharges.

- Maximum Supply Current: 3 mA
- 2000 V ESD Protection on the Inputs and Outputs
- TTL/CMOS Input Compatible
- Typical Propagation Delay: 6 ns
- Typical Output Skew: 1 ns
- Meets V_O = 6.0 V (and V_O = 0.25 V), V_{CC} = 0 V, I_O < 100 μA Requirement
- Meets the Requirements of Standard EIA–422–A
- Operation from Single 5 V Supply
- High Impedance Mode for Outputs Connected to System Buses

BLOCK DIAGRAM



This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

REV 3
1993

TRUTH TABLE

Control Inputs E/$\overline{E}$	Input	Non–Inverting Output	Inverting Output
L/H	X	Z	Z
All other combinations of enable inputs	H	H	L
	L	L	H

X = Don't Care
Z = High Impedance
H = High Logic State
L = Low Logic State

2

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	7	V
DC Input Voltage	V_{in}	– 1.5 to V_{CC} + 1.5	V
DC Output Voltage*	V_{out}	– 0.5 to V_{CC} + 0.5	V
DC Output Current, per Pin	I_{out}	150	mA
DC V_{CC} or GND Current, per Pin	I_{DD}	150	mA
Storage Temperature	T_{stg}	– 65 to + 150	°C
Power Dissipation	P_D	500	mW
ESD (Human Body Model)		2000	V

* Power–on conditions.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than the maximum rated voltages to this high impedance circuit.

For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$. Reliability of operation is enhanced if unused inputs are tied to and appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

OPERATING CONDITIONS

Rating	Symbol	Min	Max	Unit
Power Supply Voltage	V_{CC}	4.5	5.5	V
DC Input Voltage	V_{in}	0	V_{CC}	V
Operating Temperature Range	T_A	– 40	+ 85	°C
Input Rise and Fall Time	t_r, t_f	—	500	ns

DC CHARACTERISTICS (V_{CC} = 4.5 to 5.5 V, T_A = – 40 to + 85°C, unless otherwise stated)

Parameter	Symbol	Min	Typ	Max	Unit
Input Voltage (Low Logic State)	V_{IL}	—	—	0.8	V
Input Voltage (High Logic State)	V_{IH}	2.0	—	—	V
Output Voltage (Low Logic State) I_{sink} = 20 mA	V_{OL}	—	0.3	0.5	V
Output Voltage (High Logic State) I_{source} = 20 mA	V_{OH}	2.5	2.8	—	V
Output Differential Voltage R_L = 100 Ω (Note 1)	V_{OD}	2.0	—	—	V
Output Differential Voltage Difference R_L = 100 Ω (Note 1)	$D(V_{OD})$	—	—	± 0.4	V
Output Offset Voltage R_L = 100 Ω (Note 1)	V_{OS}	—	—	3.0	V
Output Offset Voltage Difference R_L = 100 Ω (Note 1)	$D(V_{OS})$	—	—	± 0.4	V
Input Current V_{IH} = V_{CC}, GND, V_{IH} or V_{IL}	I_{in}	—	—	± 1.0	μA
Quiescent Supply Current I_{out} = 0 μA	I_{CC}	—	—	3.0	mA
Output Short Circuit Current (Note 2)	I_{OS}	– 30	– 100	– 150	mA
Output Leakage Current (High–Z State) V_{out} = V_{CC} or GND	$I_{O(Z)}$	—	—	± 1.0	μA
Input Leakage Current (Power Off) V_{out} = 6 V	I_{oxh}	—	—	100	μA
V_{out} = – 0.25 V	I_{oxl}	—	—	– 100	

NOTES:
1. See EIA–422–A for exact test conditions.
2. Only one output may be shorted at a time.

AC CHARACTERISTICS (V_{CC} = 4.5 to 5.5 V, T_A = – 40 to + 85°C, unless otherwise stated)

Parameter	Symbol	Min	Typ	Max	Unit
Propagation Delay Input to Output (S1 Open)	t_{PLH} t_{PHL}	—	6	12	ns
Output Skew (S1 Open)*	Skew	—	1.0	4	ns
Differential Output Rise Time Fall Time (S1 Open)	$t_{(TLH)}$ $t_{(THL)}$	—	4	8	ns
Output Enable Time (S1 Closed)	t_{PZH} t_{PZL}	— —	16 15	— —	ns
Output Disable Time (S1 Closed)	t_{PHZ} t_{PLZ}	— —	6 9	— —	ns

* Skew: difference in propagation delays between complementary outputs.

2

AC TEST CIRCUIT AND SWITCHING TIME WAVEFORMS

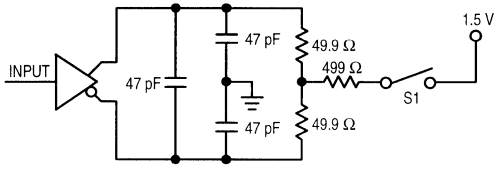


Figure 1. AC Test Circuit

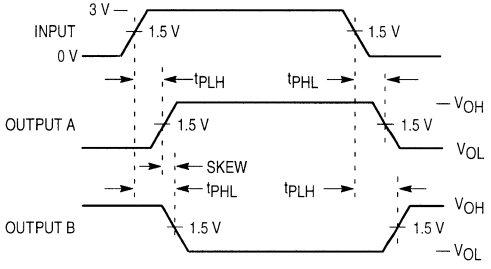


Figure 2. Propagation Delays and Skew Waveforms

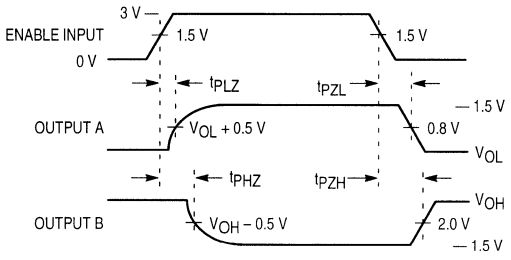


Figure 3. Enable and Disable Times

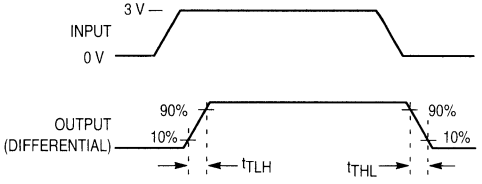


Figure 4. Differential Rise and Fall Times

TYPICAL APPLICATIONS

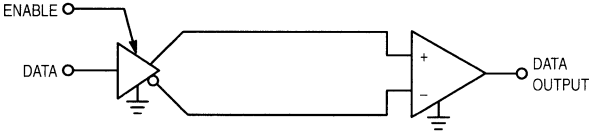


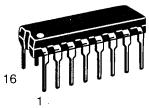
Figure 5. Two–Wire Balanced Systems (EIA–422–A)

MC26C32

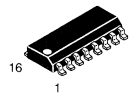
2

Product Preview

Quad EIA-422-A Line Receiver
CMOS



P SUFFIX
PLASTIC DIP
CASE 648



D SUFFIX
SOG PACKAGE
CASE 751B

ORDERING INFORMATION

MC26C32P	Plastic DIP
MC26C32D	SOG Package

The MC26C32 is a quad differential line receiver designed for digital data transmission over balanced lines. The MC26C32 meets all the requirements of standard EIA–422–A while retaining the low–power characteristics of CMOS.

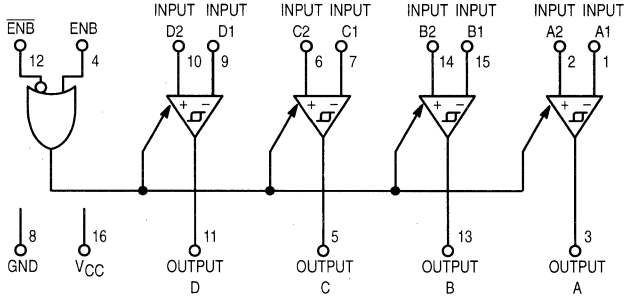
The MC26C32 has an input sensitivity of 200 mV over the common mode input voltage range of ± 7 V. In addition, each receiver chain has internal hysteresis circuitry to improve noise margin and discourage output instability for slowly changing input waveforms.

The MC26C32 is pin compatible with the AM26LS32.

All pins are protected against damage due to electrostatic discharges.

- Typical Power Supply Current: 6 mA
- 2000 V ESD Protection on the Inputs and Outputs
- Typical Propagation Delay: 18 ns
- Typical Input Hysteresis: 75 mV
- Meets the Requirements of Standard EIA–422–A
- Operation from Single 5 V Supply
- High Impedance Mode for Outputs Connected to System Buses
- TTL/CMOS Compatible Outputs

BLOCK DIAGRAM



REV 4
10/95

TRUTH TABLE

Control Inputs E/$\overline{E}$	Input	Output
L/H	X	Z
All other combinations of enable inputs	$V_{ID} \geq V_{TH}$ (max)	1
	$V_{ID} \geq V_{TH}$ (min)	0
	Open	1

X = Don't Care
Z = High Impedance
H = High Logic State
L = Low Logic State

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	7	V
Input Voltage	V_I	± 10	V
Input Differential Voltage	V_{ID}	± 14	V
Enable Control Input Voltage	V_{in}	V_{CC} + 0.5	V
Storage Temperature	T_{stg}	– 65 to + 150	°C
Maximum Current per Output	I_O	± 25	mA
ESD (Human Body Model)		2000	V

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than the maximum rated voltages to this high impedance circuit.

For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$. Reliability of operation is enhanced if unused inputs are tied to and appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

OPERATING CONDITIONS

Rating	Symbol	Min	Max	Unit
Power Supply Voltage	V_{CC}	4.5	5.5	V
Operating Temperature Range	T_A	– 40	+ 85	°C
Input Rise and Fall Time	t_r, t_f	—	500	ns

DC CHARACTERISTICS (V_{CC} = 4.5 to 5.5 V, T_A = – 40 to + 85°C, unless otherwise stated) (See Note 1)

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply Current, $V_{CC} \geq$ Max	I_{CC}	—	6	12	mA
Enable Input Current, $V_{in} = V_{CC}$ or GND	I_I	—	—	± 1.0	µA
Input Voltage — Low Logic State (Enable Control)	V_{IL}	—	—	0.8	V
Input Voltage — High Logic State (Enable Control)	V_{IH}	2	—	—	V
Differential Input Voltage, – 7 V < V_{LCM} < 7 V $V_{out} = V_{OH}$ $V_{out} = V_{OL}$	V_{TH}	0.2 —	— —	— – 0.2	V
Input Hysteresis, V_{LCM} = 0 V	V_{hys}	—	75	—	mV
Comparator Input Current V_{in} = + 10 V, Other Input = GND V_{in} = – 10 V, Other Input = GND	I_{in}	— —	1.4 – 2.5	— —	mA
Comparator Input Resistance, – 10 V < V_{LCM} < + 10 V	R_{in}	4	4.8	—	kΩ
Output Voltage (Low Logic State) V_{ID} = – 1 V, I_{out} = 6 mA (Note 2)	V_{OL}	—	0.13	0.33	V
Output Voltage (High Logic State) V_{ID} = + 1 V, I_{out} = – 6 mA (Note 2)	V_{OH}	3.8	4.8	—	V
Output Leakage Current (High Logic State) $V_{out} = V_{CC}$ or GND	I_{OZ}	– 5	—	5	µA

NOTES:
1. All currents into device pins are shown as positive, out of device pins are negative. All voltages referenced to ground unless otherwise noted.
2. See EIA specifications EIA–422–A for exact test conditions.

AC CHARACTERISTICS (V_{CC} = 4.5 to 5.5 V, T_A = – 40 to + 85°C, unless otherwise stated)

Parameter	Symbol	Min	Typ	Max	Unit
Propagation Delay Input to Output, C_L = 50 pF, V_{DIFF} = 2.5 V	t_{PLH} t_{PHL}	—	18	30	ns
Skew = $\lvert t_{PHL} - t_{PLH} \rvert$	Skew	—	1	—	ns
Propagation Delay Enable to Output C_L = 50 pF, R_L = 1000 Ω, V_{DIFF} = 2.5 V	t_{PLZ} t_{PHZ}	—	12	—	ns
Propagation Delay Enable to Output C_L = 50 pF, R_L = 1000 Ω, V_{DIFF} = 2.5 V	t_{PZL} t_{PZH}	—	14	—	ns

* Skew: difference in propagation delays between complementary outputs.

2

AC TEST CIRCUIT AND SWITCHING TIME WAVEFORMS

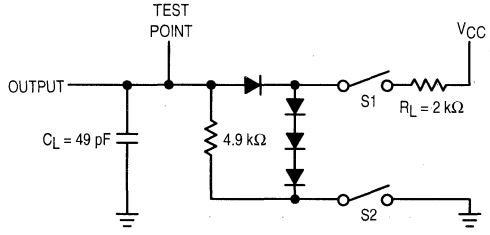


Figure 1. Test Circuit

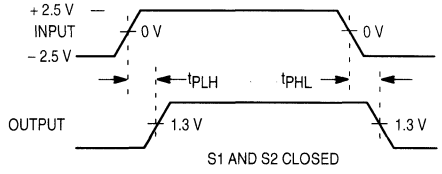


Figure 2. Propagation Delays

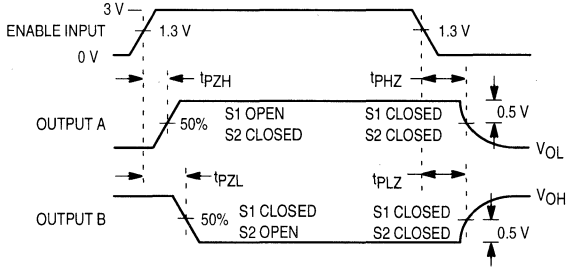


Figure 3. Enable and Disable Times

TYPICAL APPLICATIONS

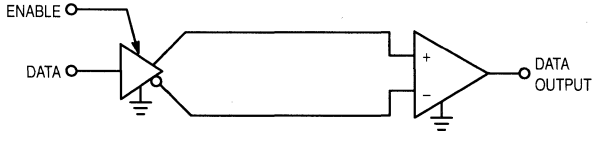


Figure 4. Two–Wire Balanced Systems (EIA–422–A)

MOTOROLA

MC2833

Low Power FM Transmitter System

MC2833 is a one–chip FM transmitter subsystem designed for cordless telephone and FM communication equipment. It includes a microphone amplifier, voltage controlled oscillator and two auxiliary transistors.

- Wide Range of Operating Supply Voltage (2.8–9.0 V)
- Low Drain Current (I_{CC} = 2.9 mA Typ)
- Low Number of External Parts Required
- – 30 dBm Power Output to 60 MHz Using Direct RF Output
- +10 dBm Power Output Attainable Using On–Chip Transistor Amplifiers
- Users Must Comply with Local Regulations on R.F. Transmission (FCC, DOT, P.T.T., etc)

LOW POWER FM TRANSMITTER SYSTEM

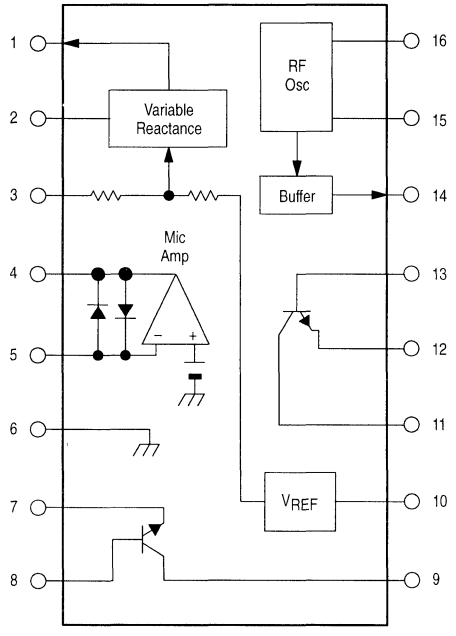
SEMICONDUCTOR TECHNICAL DATA

2

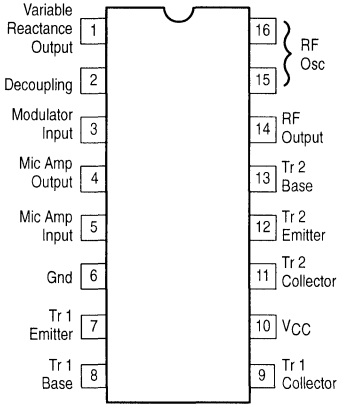
P SUFFIX
PLASTIC PACKAGE
CASE 648

D SUFFIX
PLASTIC PACKAGE
CASE 751B
(SO–16)

Representative Block Diagram



PIN CONNECTIONS



ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC2833D	T_A = – 30 to +75°C	SO–16
MC2833P		Plastic DIP

MAXIMUM RATINGS

Ratings	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	10 (max)	V
Operating Supply Voltage Range	V_{CC}	2.8–9.0	V
Junction Temperature	T_J	+ 150	°C
Operating Ambient Temperature	T_A	– 30 to + 75	°C
Storage Temperature Range	T_{stg}	– 65 to + 150	°C

2

ELECTRICAL CHARACTERISTICS (V_{CC} = 4.0 V, T_A = 25°C, unless otherwise noted)

Characteristics	Symbol	Pin	Min	Typ	Max	Unit
Drain Current (No input signal)	I_{CC}	10	1.7	2.9	4.3	mA
FM MODULATOR						
Output RF Voltage (f_o = 16.6 MHz)	V_{out} RF	14	60	90	130	mVrms
Output DC Voltage (No input signal)	Vdc	14	2.2	2.5	2.8	V
Modulation Sensitivity (f_o = 16.6 MHz) (V_{in} = 0.8 V to 1.2 V)	SEN	3 14	7.0 –	10 –	15 –	Hz/mVdc
Maximum Deviation (f_o = 16.6 MHz) (V_{in} = 0 V to 2.0 V)	Fdev	3 14	3.0 –	5.0 –	10 –	kHz
MIC AMPLIFIER						
Closed Loop Voltage Gain (V_{in} = 3.0 mVrms) (f_{in} = 1.0 kHz)	A_v	4 5	27 –	30 –	33 –	dB
Output DC Voltage (No input signal)	V_{out} dc	4	1.1	1.4	1.7	V
Output Swing Voltage (V_{in} = 30 mVrms) (f_{in} = 1.0 kHz)	V_{out} p–p	4	0.8	1.2	1.6	Vp–p
Total Harmonic Distortion (V_{in} = 3.0 mVrms) (f_{in} = 1.0 kHz)	THD	4	–	0.15	2.0	%

AUXILIARY TRANSISTOR STATIC CHARACTERISTICS

Characteristics	Symbol	Min	Typ	Max	Unit
Collector Base Breakdown Voltage (I_C = 5.0 μA)	$V_{(BR)CBO}$	15	45	–	V
Collector Emitter Breakdown Voltage (I_C = 200 μA)	$V_{(BR)CEO}$	10	15	–	V
Collector Substrate Breakdown Voltage (I_C = 50 μA)	$V_{(BR)CSO}$	–	70	–	V
Emitter Base Breakdown Voltage (I_E = 50 μA)	$V_{(BR)EBO}$	–	6.2	–	V
Collector Base Cut Off Current (V_{CB} = 10 V) (I_E = 0)	I_{CBO}	–	–	200	nA
DC Current Gain (I_C = 3.0 mA) (V_{CE} = 3.0 V)	h_{FE}	40	150	–	–

AUXILIARY TRANSISTOR DYNAMIC CHARACTERISTICS

Current Gain Bandwidth Product (V_{CE} = 3.0 V) (I_C = 3.0 mA)	f_T	–	500	–	MHz
Collector Base Capacitance (V_{CE} = 3.0 V) (I_C = 0)	C_{CB}	–	2.0	–	pF
Collector Substrate Capacitance (V_{CS} = 3.0 V) (I_C = 0)	C_{CS}	–	3.3	–	pF

Figure 1. Test Circuit

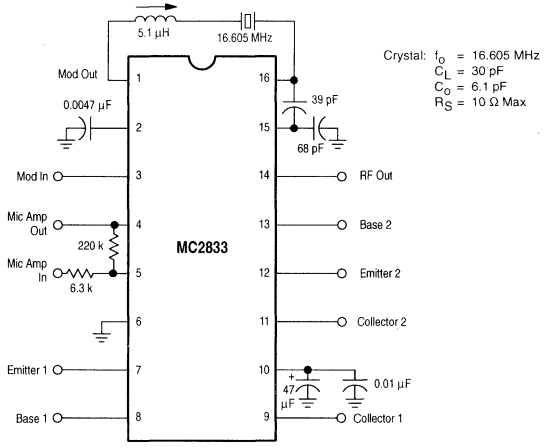
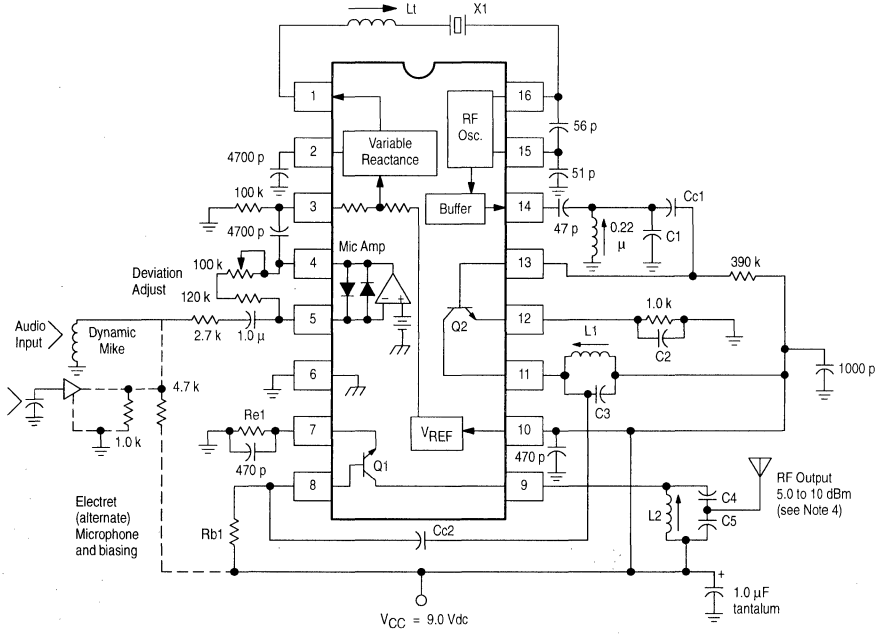


Figure 2. Single Chip VHF Narrowband FM Transmitter



NOTES:

1. Components versus output frequency:

Output RF	X1 (MHz)	Lt (µH)	L1 (µH)	L2 (µH)	Re1	Rb1	Cc1	Cc2	C1	C2	C3	C4	C5
50 MHz	16.6667	3.3–4.7	0.22	0.22	330	390 k	33 p	33 p	33 p	470 p	33 p	47 p	220 p
76 MHz	12.6000	5.1	0.22	0.22	150	300 k	68 p	10 p	68 p	470 p	12 p	20 p	120 p
144 MHz	12	5.6	0.15	0.10	150	220 k	47 p	10 p	68 p	1000 p	18 p	12 p	33 p

2. Crystal X1 is fundamental mode, calibrated for parallel resonance with a 32 pF load. The final output frequency is generated by frequency multiplication within the MC2833 IC. The RF output buffer (Pin 14) and Q2 transistor are used as a frequency tripler and doubler, respectively, in the 76 and 144 MHz transmitters. The Q1 output transistor is a linear amplifier in the 49.7 MHz and 76 MHz transmitters, and a frequency doubler in the 144 MHz transmitter.
3. All coils used are 7 mm shielded inductors, CoilCraft series M1175A, M1282A–M1289A, M1312A or equivalent.
4. Power output is ≈ + 10 dBm for 50 MHz and 76 MHz transmitters, and ≈ + 5.0 dBm for the 144 MHz transmitter at V_{CC} = 8.0 V. Power output drops with lower V_{CC}.
5. All capacitors in microfarads, inductors in Henries and resistors in Ohms unless otherwise specified.
6. Other frequency combinations may be set–up by simple scaling of the 3 examples shown.

Figure 3. Buffer/Multiplier (x3, Pin 14)
(16 MHz Fundamental)

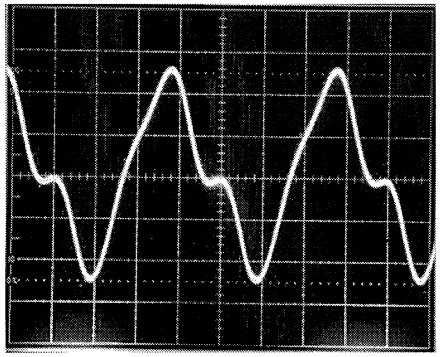


Figure 4. Input to Doubler (Pin 13)
(50 MHz x 3 Component)

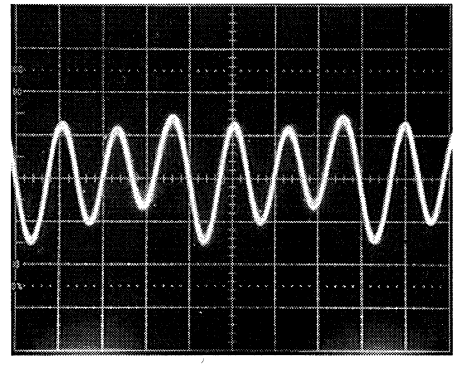


Figure 5. Doubler Output 76 MHz (Pin 11)

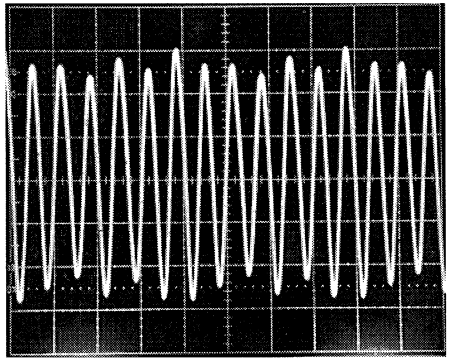


Figure 6. Spectrum

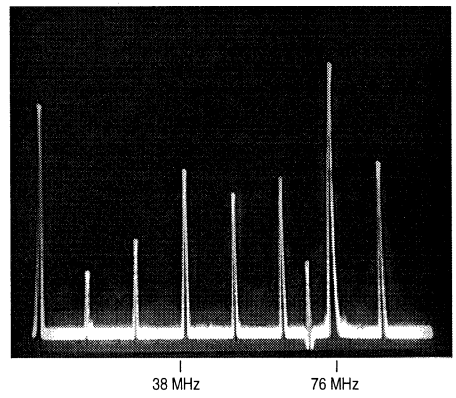


Figure 7. Output Spectrum (50 MHz)

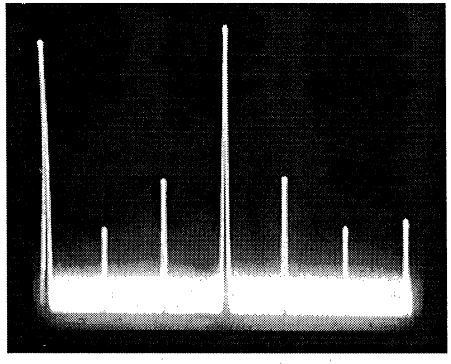


Figure 8. Modulation Spectrum
(1.0 kHz Showing Carrier Null)

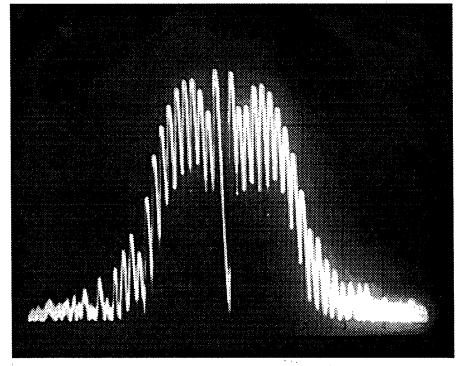


Figure 9. 144 MHz/x12 Multiplier

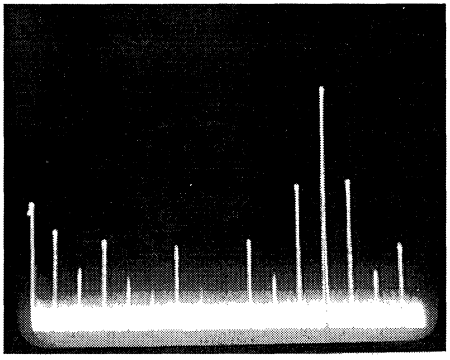


Figure 10. Circuit Side View

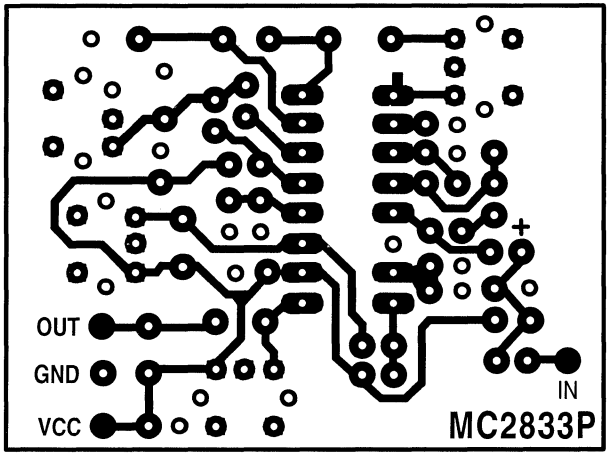


Figure 11. Ground Plane on Component Side

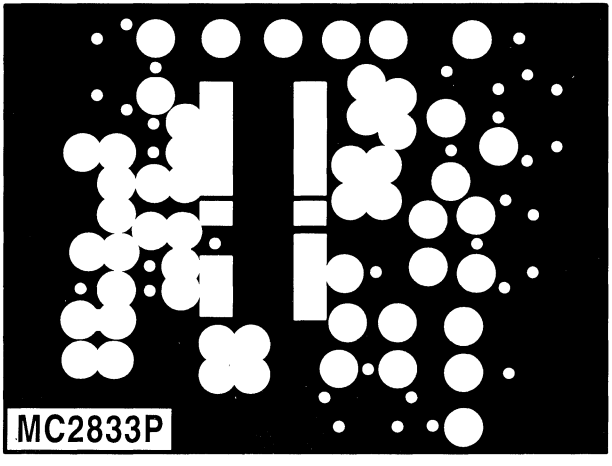
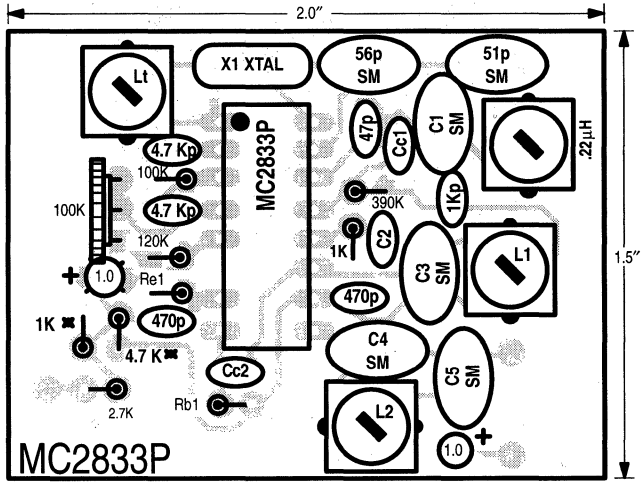
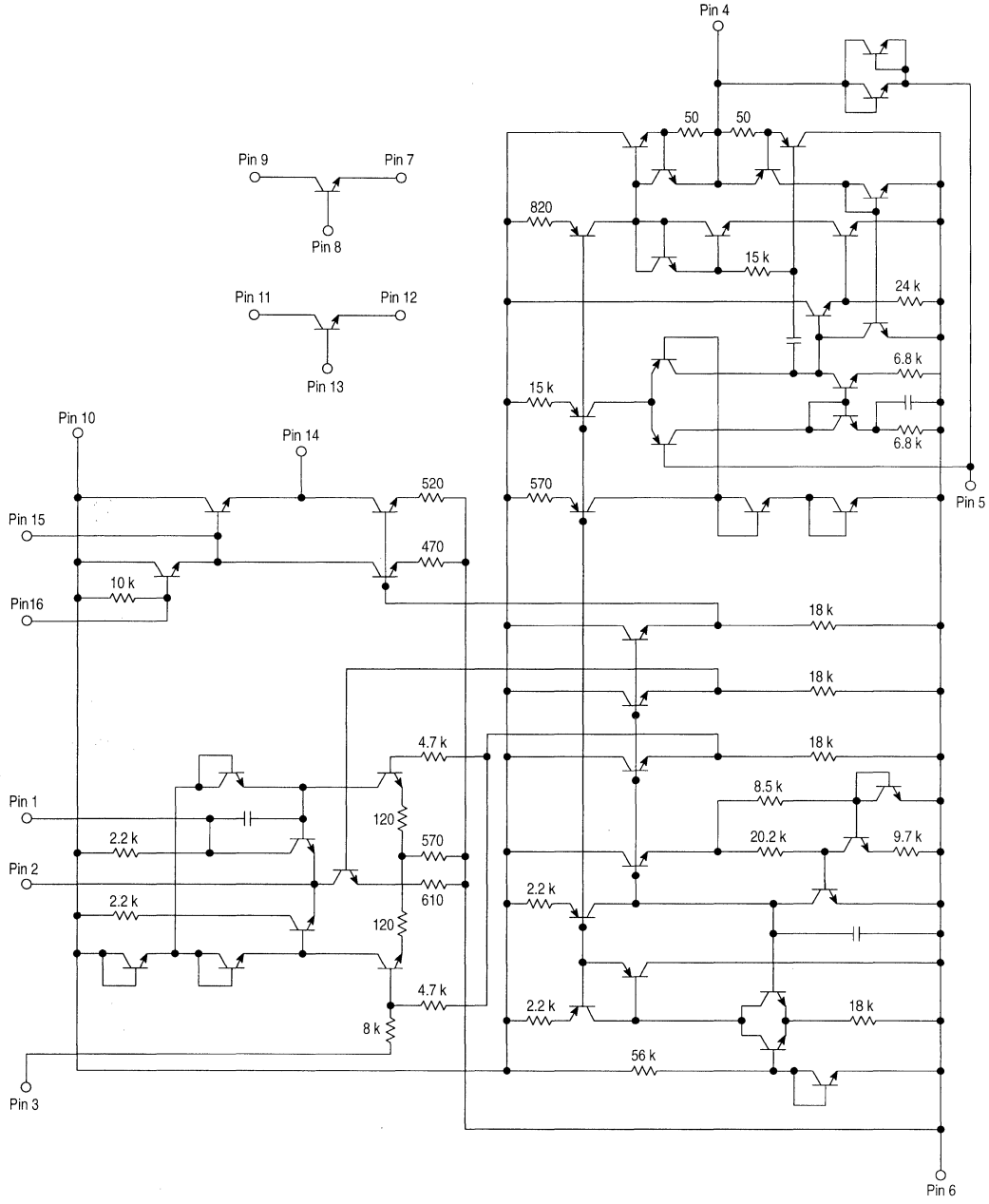


Figure 12. Component View



NOTES:
- Positive artwork provided.
- Drill holes must be plated to ensure making all ground (V_{EE}) connections!
- Resistors labelled * are used for biasing of electret microphone if used.
- Capacitors labelled "SM" are silver mica.
- Final board size 1.5″ × 2.0″.

Figure 13. Circuit Schematic



MOTOROLA

MC3356

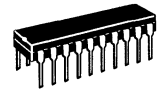
Wideband FSK Receiver

The MC3356 includes Oscillator, Mixer, Limiting IF Amplifier, Quadrature Detector, Audio Buffer, Squelch, Meter Drive, Squelch Status output, and Data Shaper comparator. The MC3356 is designed for use in digital data communciations equipment.

- Data Rates up to 500 kilobaud
- Excellent Sensitivity: – 3 dB Limiting Sensitivity
  30 μVrms @ 100 MHz
- Highly Versatile, Full Function Device, yet Few External Parts are Required
- Down Converter Can be Used Independently — Similar to NE602

WIDEBAND FSK RECEIVER

SEMICONDUCTOR TECHNICAL DATA



P SUFFIX
PLASTIC PACKAGE
CASE 738

DW SUFFIX
PLASTIC PACKAGE
CASE 751D
(SO–20L)

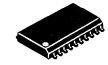
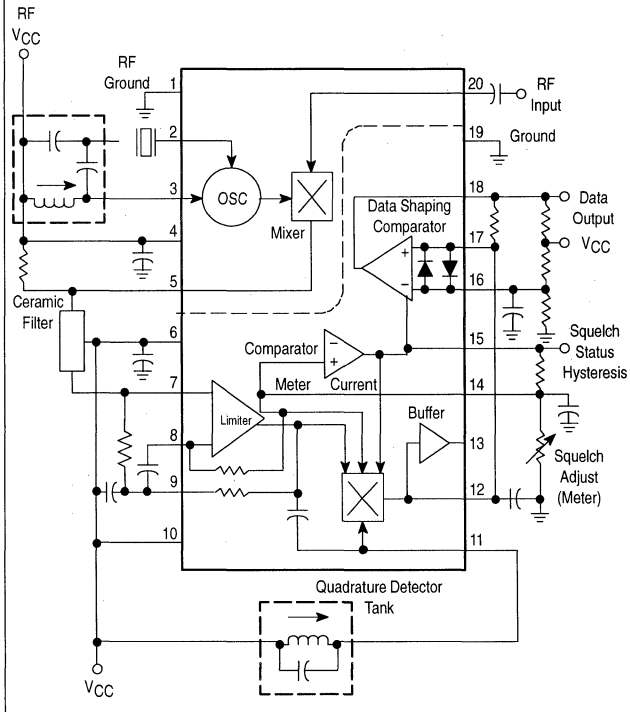
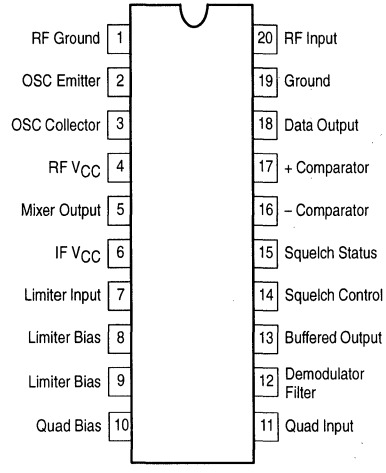


Figure 1. Representative Block Diagram



PIN CONNECTIONS



ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC3356DW	T_A = – 40 to +85°C	SO–20L
MC3356P		Plastic DIP

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	$V_{CC(max)}$	15	Vdc
Operating Power Supply Voltage Range (Pins 6, 10)	V_{CC}	3.0 to 9.0	Vdc
Operating RF Supply Voltage Range (Pin 4)	RF V_{CC}	3.0 to 12.0	Vdc
Junction Temperature	T_J	150	°C
Operating Ambient Temperature Range	T_A	– 40 to + 85	°C
Storage Temperature Range	T_{stg}	– 65 to + 150	°C
Power Dissipation, Package Rating	P_D	1.25	W

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 Vdc, f_o = 100 MHz, f_{osc} = 110.7 MHz, Δf = ±75 kHz, f_{mod} = 1.0 kHz, 50 Ω source, T_A = 25°C, test circuit of Figure 2, unless otherwise noted.)

Characteristics	Min	Typ	Max	Unit
Drain Current Total, RF V_{CC} and V_{CC}	–	20	25	mAdc
Input for – 3 dB limiting	–	30	–	µVrms
Input for 50 dB quieting $\left(\frac{S+N}{N}\right)$	–	60	–	µVrms
Mixer Voltage Gain, Pin 20 to Pin 5	2.5	–	–	
Mixer Input Resistance, 100 MHz	–	260	–	Ω
Mixer Input Capacitance, 100 MHz	–	5.0	–	pF
Mixer/Oscillator Frequency Range (Note 1)	–	0.2 to 150	–	MHz
IF/Quadrature Detector Frequency Range (Note 1)	–	0.2 to 50	–	MHz
AM Rejection (30% AM, RF V_{in} = 1.0 mVrms)	–	50	–	dB
Demodulator Output, Pin 13	–	0.5	–	Vrms
Meter Drive	–	7.0	–	µA/dB
Squelch Threshold	–	0.8	–	Vdc

NOTE: 1. Not taken in Test Circuit of Figure 2; new component values required.

Figure 2. Test Circuit

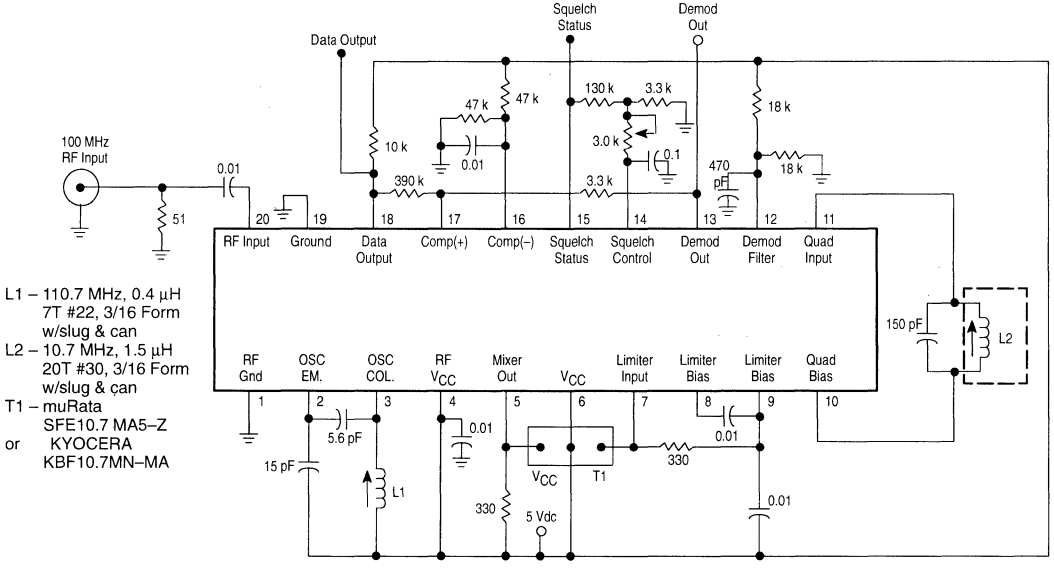


Figure 3. Output Components of Signal, Noise, and Distortion

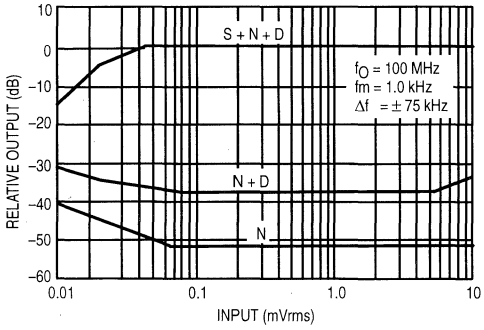
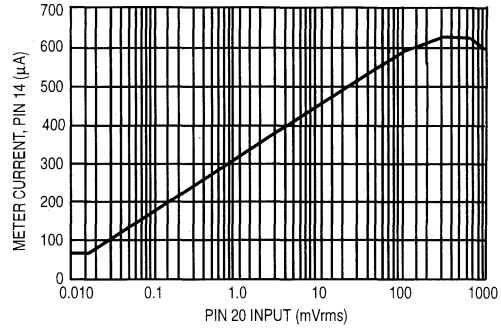


Figure 4. Meter Current versus Signal Input



GENERAL DESCRIPTION

This device is intended for single and double conversion VHF receiver systems, primarily for FSK data transmission up to 500 K baud (250 kHz). It contains an oscillator, mixer, limiting IF, quadrature detector, signal strength meter drive, and data shaping amplifier.

The oscillator is a common base Colpitts type which can be crystal controlled, as shown in Figure 1, or L–C controlled as shown in the other figures. At higher V_{CC}, it has been operated as high as 200 MHz. A mixer/oscillator voltage gain of 2 up to approximately 150 MHz, is readily achievable.

The mixer functions well from an input signal of 10 μVrms, below which the squelch is unpredictable, up to about 10 mVrms, before any evidence of overload. Operation up to 1.0 Vrms input is permitted, but non–linearity of the meter output is incurred, and some oscillator pulling is suspected. The AM rejection above 10 mVrms is degraded.

The limiting IF is a high frequency type, capable of being operated up to 50 MHz. It is expected to be used at 10.7 MHz in most cases, due to the availability of standard ceramic resonators. The quadrature detector is internally coupled to the IF, and a 5.0 pF quadrature capacitor is internally provided. The –3dB limiting sensitivity of the IF itself is approximately 50 μV (at Pin 7), and the IF can accept signals up to 1.0 Vrms without distortion or change of detector quiescent dc level.

The IF is unusual in that each of the last 5 stages of the 6 state limiter contains a signal strength sensitive, current sinking device. These are parallel connected and buffered to produce a signal strength meter drive which is fairly linear for IF input signals of 10 μV to 100 mVrms (see Figure 4).

A simple squelch arrangement is provided whereby the meter current flowing through the meter load resistance flips a comparator at about 0.8 Vdc above ground. The signal strength at which this occurs can be adjusted by changing the meter load resistor. The comparator (+) input and output are available to permit control of hysteresis. Good positive action can be obtained for IF input signals of above 30 μVrms. The 130 kΩ resistor shown in the test circuit provides a small amount of hysteresis. Its connection between the 3.3 k resistor to ground and the 3.0 k pot, permits adjustment of squelch level without changing the amount of hysteresis.

The squelch is internally connected to both the quadrature detector and the data shaper. The quadrature detector output, when squelched, goes to a dc level approximately equal to the zero signal level unsquelched. The squelch causes the data shaper to produce a high (V_{CC}) output.

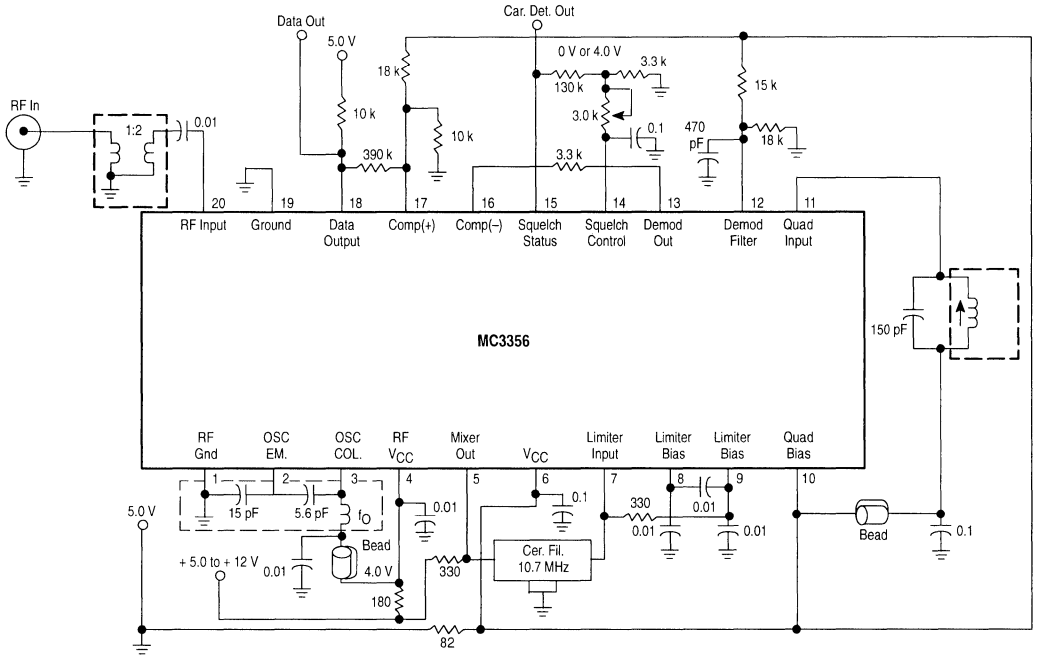
The data shaper is a complete "floating" comparator, with back to back diodes across its inputs. The output of the quadrature detector can be fed directly to either input of this amplifier to produce an output that is either at V_{CC} or V_{EE}, depending upon the received frequency. The impedance of the biasing can be varied to produce an amplifier which "follows" frequency detuning to some degree, to prevent data pulse width changes.

When the data shaper is driven directly from the demodulator output, Pin 13, there may be distortion at Pin 13 due to the diodes, but this is not important in the data application. A useful note in relating high/low input frequency to logic state: low IF frequency corresponds to low demodulator output. If the oscillator is above the incoming RF frequency, then high RF frequency will produce a logic low (input to (+) input of Data Shaper as shown in Figures 1 and 2).

APPLICATION NOTES

The MC3356 is a high frequency/high gain receiver that requires following certain layout techniques in designing a stable circuit configuration. The objective is to minimize or eliminate, if possible, any unwanted feedback.

Figure 5. Application with Fixed Bias on Data Shaper



APPLICATION NOTES (continued)

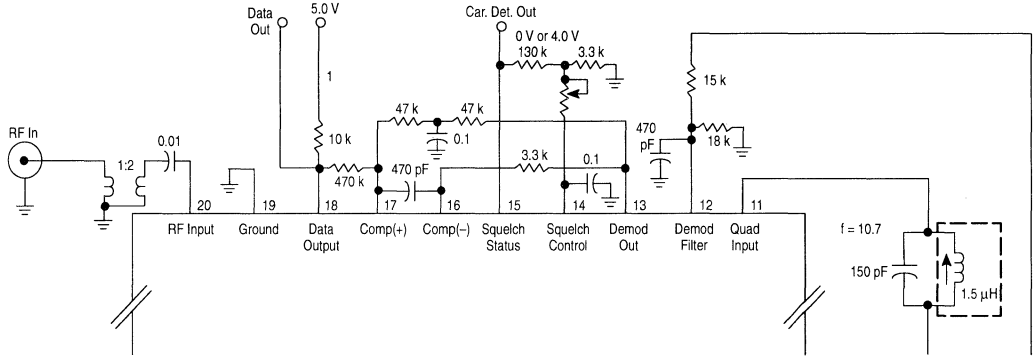
Shielding, which includes the placement of input and output components, is important in minimizing electrostatic or electromagnetic coupling. The MC3356 has its pin connections such that the circuit designer can place the critical input and output circuits on opposite ends of the chip. Shielding is normally required for inductors in tuned circuits.

The MC3356 has a separate V_{CC} and ground for the RF and IF sections which allows good external circuit isolation by minimizing common ground paths.

Note that the circuits of Figures 1 and 2 have RF, Oscillator, and IF circuits predominantly referenced to the plus supply rails. Figure 5, on the other hand, shows a suitable means of ground referencing. The two methods produce identical results when carefully executed. It is important to treat Pin 19 as a ground node for either approach. The RF input should be "grounded" to Pin 1 and then the input and the mixer/oscillator grounds (or RF V_{CC} bypasses) should be connected by a low inductance path to Pin 19. IF and detector sections should also have their bypasses returned by a **separate** path to Pin 19. V_{CC} and RF V_{CC} can be decoupled to minimize feedback, although the configuration of Figure 2 shows a successful implementation on a common 5.0 V supply. Once again, the message is: define a supply node and a ground node and return each section to those nodes by separate, low impedance paths.

The test circuit of Figure 2 has a 3 dB limiting level of 30 μV which can be lowered 6 db by a 1:2 untuned transformer at the input as shown in Figures 5 and 6. For applications that require additional sensitivity, an RF amplifier can be added, but with no greater than 20 db gain. This will give a 2.0 to 2.5 μV sensitivity and any additional gain will reduce receiver dynamic range without improving its sensitivity. Although the test circuit operates at 5.0 V, the mixer/oscillator optimum performance is at 8.0 V to 12 V. A minimum of 8.0 V is recommended in high frequency applications (above 150 MHz), or in PLL applications where the oscillator drives a prescaler.

Figure 6. Application with Self–Adjusting Bias on Data Shaper



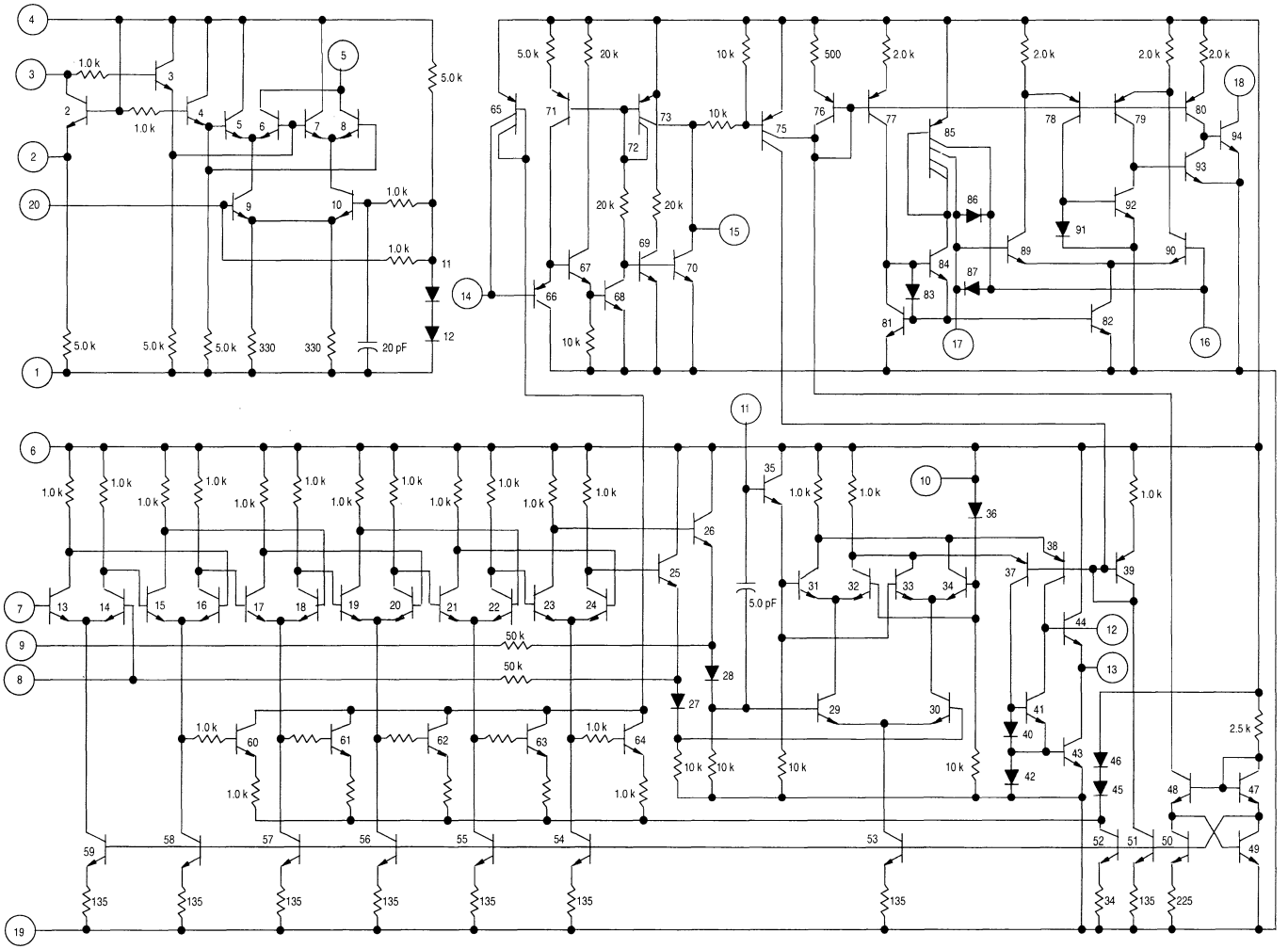
2

APPLICATION NOTES (continued)

Depending on the external circuit, inverted or noninverted data is available at Pin 18. Inverted data makes the higher frequency in the FSK signal a "one" when the local oscillator is above the incoming RF. Figure 5 schematic shows the comparator with hysteresis. In this circuit the dc reference voltage at Pin 17 is about the same as the demodulated output voltage (Pin 13) when no signal is present. This type circuit is preferred for systems where the data rates can drop to zero. Some systems have a low frequency limit on the data rate, such as systems using the MC3850 ACIA that has a start or stop bit. This defines the low frequency limit that can appear in the data stream. Figure 5 circuit can then be changed to a circuit configuration as shown in Figure 6. In Figure 6 the reference voltage for the comparator is derived from the demodulator output through a low pass circuit where τ is much lower than the lowest frequency data rate. This and similar circuits will compensate for small tuning changes (or drift) in the quadrature detector.

Squelch status (Pin 15) goes high (squelch off) when the input signal becomes greater than some preset level set by the resistance between Pin 14 and ground. Hysteresis is added to the circuit externally by the resistance from Pin 14 to Pin 15.

Figure 7. Internal Schematic



2

MOTOROLA

MC3357

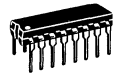
Low Power Narrowband FM IF

. . . includes Oscillator, Mixer, Limiting Amplifier, Quadrature Discriminator, Active Filter, Squelch, Scan Control, and Mute Switch. The MC3357 is designed for use in FM dual conversion communications equipment.

- Low Drain Current (3.0 mA (Typical) @ V_{CC} = 6.0 Vdc)
- Excellent Sensitivity: Input Limiting Voltage – (– 3.0 dB) = 5.0 μV (Typical)
- Low Number of External Parts Required
- Recommend MC3372 for Replacement/Upgrade

LOW POWER FM IF

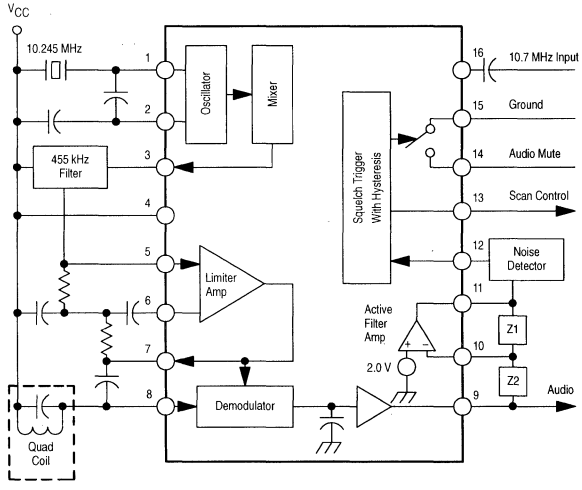
SEMICONDUCTOR TECHNICAL DATA



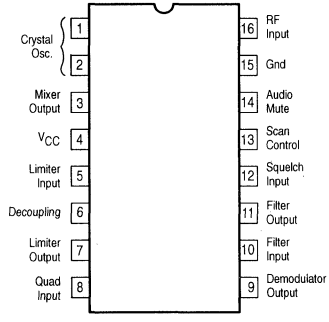
P SUFFIX
PLASTIC PACKAGE
CASE 648

D SUFFIX
PLASTIC PACKAGE
CASE 751B
(SO–16)

Figure 1. Representative Block Diagram



PIN CONNECTIONS



ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC3357D	T_A = – 30 to +70°C	SO–16
MC3357P		Plastic DIP

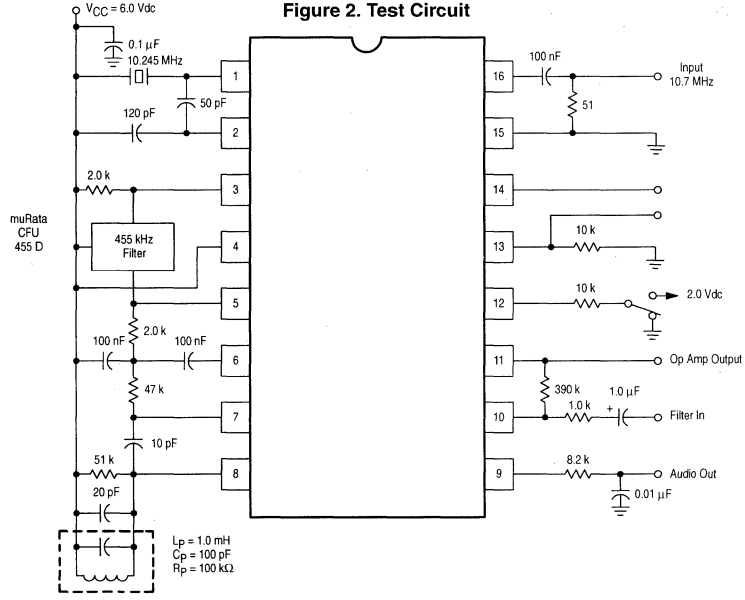
MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted)

Rating	Pin	Symbol	Value	Unit
Power Supply Voltage	4	V_{CC}(max)	12	Vdc
Operating Supply Voltage Range	4	V_{CC}	4 to 8	Vdc
Detector Input Voltage	8	–	1.0	Vp–p
Input Voltage ($V_{CC} \geq$ 6.0 Volts)	16	V_{16}	1.0	V_{RMS}
Mute Function	14	V_{14}	–0.5 to 5.0	V_{pk}
Junction Temperature	–	T_J	150	°C
Operating Ambient Temperature Range	–	T_A	– 30 to + 70	°C
Storage Temperature Range	–	T_{stg}	– 65 to + 150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 6.0 Vdc, fo = 10.7 MHz, $\Delta f = \pm$ 3.0 kHz, f_{mod} = 1.0 kHz, T_A = 25°C, unless otherwise noted.)

Characteristic	Pin	Min	Typ	Max	Unit
Drain Current Squelch Off Squelch On	4	– –	2.0 3.0	– 5.0	mA
Input Limiting Voltage (– 3 dB Limiting)	16	–	5.0	10	μV
Detector Output Voltage	9	–	3.0	–	Vdc
Detector Output Impedance	–	–	400	–	Ω
Recovered Audio Output Voltage (V_{in} = 10 mV)	9	200	350	–	mVrms
Filter Gain (10 kHz) (V_{in} = 5 mV)	–	40	46	–	dB
Filter Output Voltage	11	1.8	2.0	2.5	Vdc
Trigger Hysteresis	–	–	100	–	mV
Mute Function Low	14	–	15	50	Ω
Mute Function High	14	1.0	10	–	MΩ
Scan Function Low (Mute Off) (V_{12} = 2 Vdc)	13	–	0	0.5	Vdc
Scan Function High (Mute On) (V_{12} = Gnd)	13	5.0	–	–	Vdc
Mixer Conversion Gain	3	–	20	–	dB
Mixer Input Resistance	16	–	3.3	–	kΩ
Mixer Input Capacitance	16	–	2.2	–	pF

Figure 2. Test Circuit



CIRCUIT DESCRIPTION

The MC3357 is a low power FM IF circuit designed primarily for use in voice communication scanning receivers.

The mixer–oscillator combination converts the input frequency (e.g., 10.7 MHz) down to 455 kHz, where, after external bandpass filtering, most of the amplification is done. The audio is recovered using a conventional quadrature FM detector. The absence of an input signal is indicated by the presence of noise above the desired audio frequencies. This "noise band" is monitored by an active filter and a detector. A squelch trigger circuit indicates the presence of a noise (or a tone) by an output which can be used to control scanning. At the same time, an internal switch is operated which can be used to mute the audio.

The oscillator is an internally–biased Colpitts type with the collector, base, and emitter connections at Pins 4, 1, and 2 respectively. A crystal can be used in place of the usual coil.

The mixer is doubly–balanced to reduce spurious responses. The input impedance at Pin 16 is set by a 3.0 kΩ internal biasing resistor and has low capacitance, allowing the circuit to be preceded by a crystal filter. The collector output at Pin 3 must be dc connected to B +, below which it can swing 0.5 V.

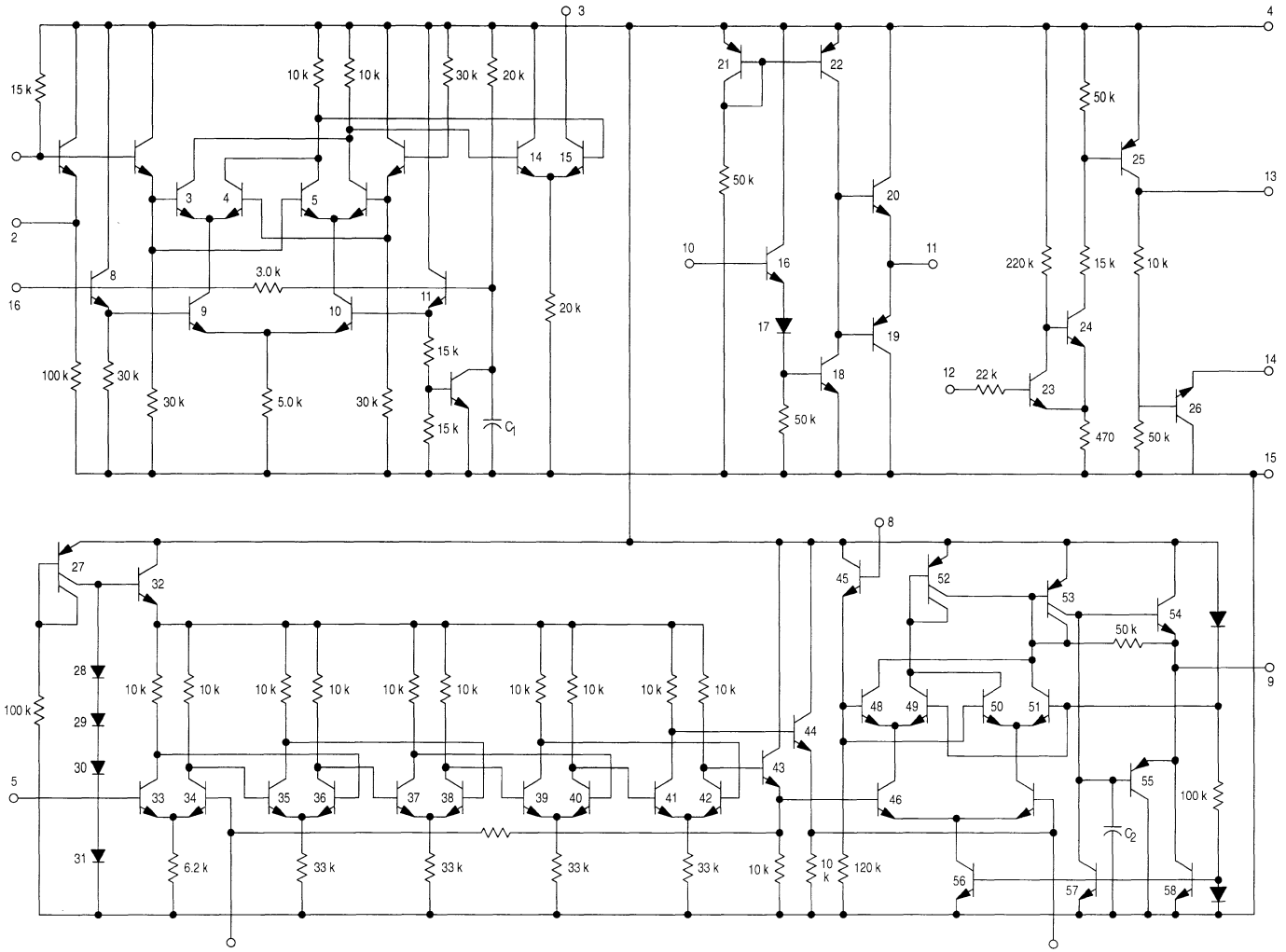
After suitable bandpass filtering (ceramic or LC), the signal goes to the input of a five–stage limiter at Pin 5. The output of the limiter at Pin 7 drives a multiplier, both internally directly, and externally through a quadrature coil, to detect the FM. The output at Pin 7 is also used to supply dc feedback to Pin 5. The other side of the first limiter stage is decoupled at Pin 6.

The recovered audio is partially filtered, then buffered, giving an impedance of around 400 Ω at Pin 9. The signal still requires de–emphasis, volume control and further amplification before driving a loudspeaker.

A simple inverting op amp is provided with an output at Pin 11 providing dc bias (externally) to the input at Pin 10 which is referred internally to 2.0 V. A filter can be made with external impedance elements to discriminate between frequencies. With an external AM detector, the filtered audio signal can be checked for the presence of noise above the normal audio band, or a tone signal. This information is applied to Pin 12.

An external positive bias to Pin 12 sets up the squelch trigger circuit such that Pin 13 is low at an impedance level of around 60 kΩ, and the audio mute (Pin 14) is open circuit. If Pin 12 is pulled down to 0.7 V by the noise or tone detector, Pin 13 will rise to approximately 0.5 Vdc below supply where it can support a load current of around 500 µA and Pin 14 is internally short–circuited to ground. There is 100 mV of hysteresis at Pin 12 to prevent jitter. Audio muting is accomplished by connecting Pin 14 to a high–impedance ground–reference point in the audio path between Pin 9 and the audio amplifier.

Figure 3. Circuit Schematic



MC3359

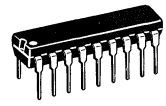
Low Power Narrowband FM IF

. . . includes oscillator, mixer, limiting amplifier, AFC, quadrature discriminator, op/amp, squelch, scan control, and mute switch. The MC3359 is designed to detect narrowband FM signals using a 455 kHz ceramic filter for use in FM dual conversion communications equipment. The MC3359 is similar to the MC3357 except that the MC3359 has an additional limiting IF stage, an AFC output, and an opposite polarity Broadcast Detector. The MC3359 also requires fewer external parts. For low cost applications requiring V_{CC} below 6.0 V, the MC3361BP,BD are recommended. For applications requiring a fixed, tuned, ceramic quadrature resonator, use the MC3357. For applications requiring dual conversion and RSSI, refer to these devices; MC3335, MC3362 and MC3363.

- Low Drain Current: 3.6 mA (Typical) @ V_{CC} = 6.0 Vdc
- Excellent Sensitivity: Input Limiting Voltage – – 3.0 dB = 2.0 μV (Typical)
- Low Number of External Parts Required
- For Low Voltage and RSSI, use the MC3371

HIGH GAIN LOW POWER FM IF

SEMICONDUCTOR TECHNICAL DATA



P SUFFIX
PLASTIC PACKAGE
CASE 707

DW SUFFIX
PLASTIC PACKAGE
CASE 751D
(SO–20L)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC3359DW	T_A = –30 to +70°C	SO–20L
MC3359P		Plastic DIP

Figure 1. Simplified Application in a Scanner Receiver

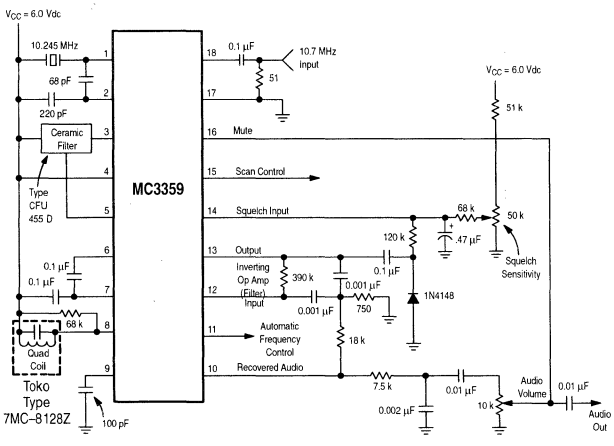
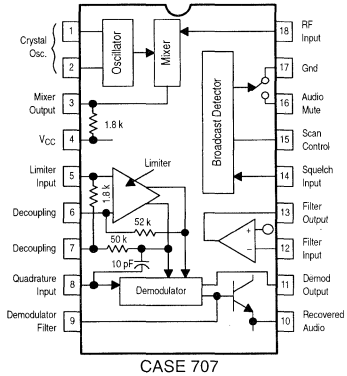
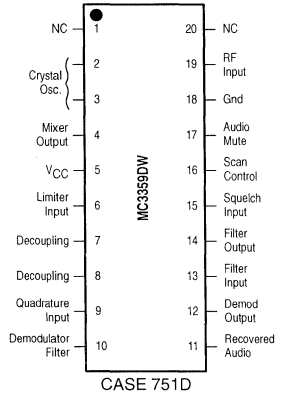


Figure 2. Pin Connections and Functional Block Diagram



CASE 707



CASE 751D

MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted)

Rating	Pin	Symbol	Value	Unit
Power Supply Voltage	4	V_{CC}(max)	12	Vdc
Operating Supply Voltage Range	4	V_{CC}	6 to 9	Vdc
Input Voltage ($V_{CC} \geq$ 6.0 Volts)	18	V_{18}	1.0	V_{rms}
Mute Function	16	V_{16}	– 0.7 to 12	V_{pk}
Junction Temperature	–	T_J	150	°C
Operating Ambient Temperature Range	–	T_A	– 30 to + 70	°C
Storage Temperature Range	–	T_{stg}	– 65 to + 150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 6.0 Vdc, f_o = 10.7 MHz, $\Delta f = \pm 3.0$ kHz, f_{mod} = 1.0 kHz, 50 Ω source, T_A = 25°C test circuit of Figure 3, unless otherwise noted)

Characteristics		Min	Typ	Max	Units
Drain Current (Pins 4 and 8)	Squelch Off Squelch On	– –	3.6 5.4	6.0 7.0	mA
Input for 20 dB Quieting		–	8.0	–	μVrms
Input for – 3.0 dB Limiting		–	2.0	–	μVrms
Mixer Voltage Gain (Pin 18 to Pin 3, Open)		–	46	–	
Mixer Third Order Intercept, 50 Ω Input		–	– 1.0	–	dBm
Mixer Input Resistance		–	3.6	–	kΩ
Mixer Input Capacitance		–	2.2	–	pF
Recovered Audio, Pin 10 (Input Signal 1.0 mVrms)		450	700	–	mVrms
Detector Center Frequency Slope, Pin 10		–	0.3	–	V/kHz
AFC Center Slope, Pin 11, Unloaded		–	12	–	V/kHz
Filter Gain (test circuit of Figure 3)		40	51	–	dB
Squelch Threshold, Through 10K to Pin 14		–	0.62	–	Vdc
Scan Control Current, Pin 15	Pin 14 – High – Low	– 2.0	0.01 2.4	1.0 –	μA mA
Mute Switch Impedance Pin 16 to Ground	Pin 14 – High – Low	–	5.0 1.5	10 –	Ω MΩ

Figure 3. Test Circuit

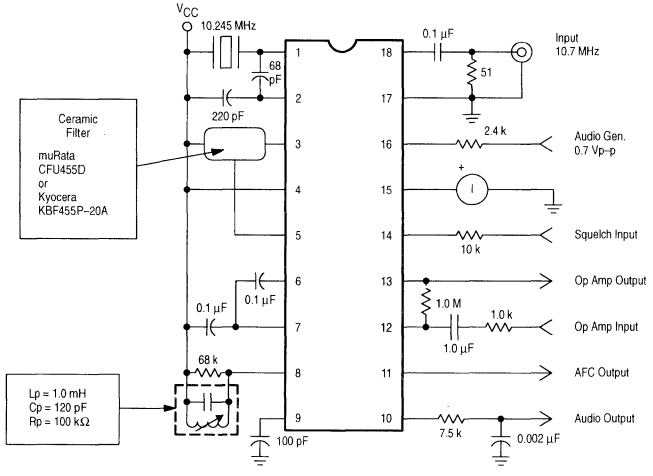


Figure 4. Mixer Voltage Gain

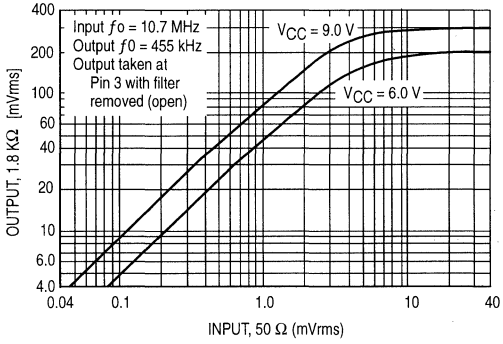


Figure 5. Limiting IF Frequency Response

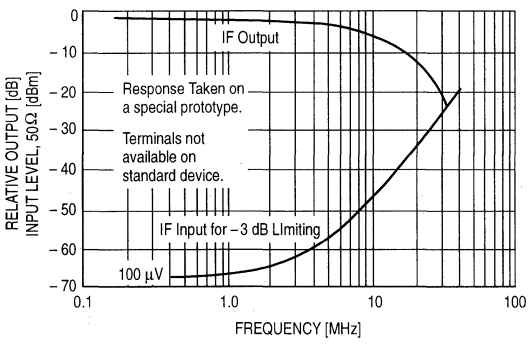


Figure 6. Mixer Third Order Intermodulation Performance

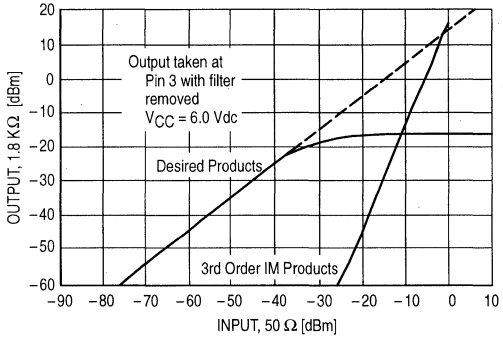


Figure 7. Detector and AFC Responses

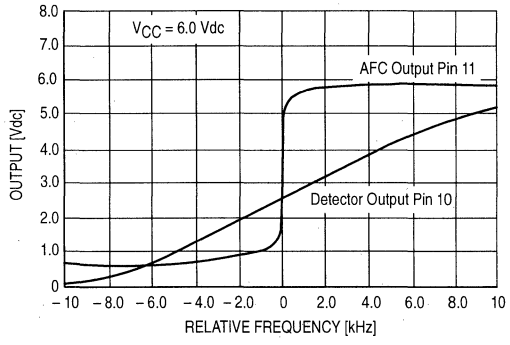


Figure 8. Relative Mixer Gain

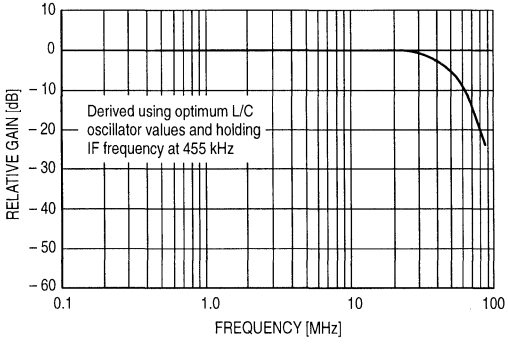


Figure 9. Overall Gain, Noise, and AM Rejection

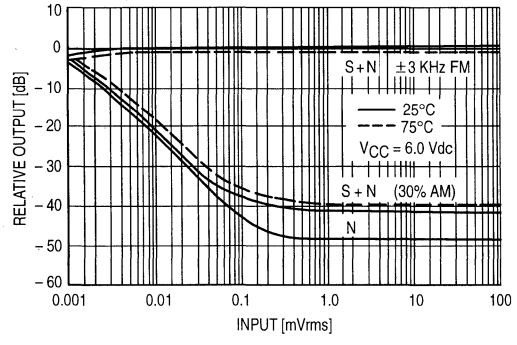


Figure 10. Output Components of Signal, Noise, and Distortion

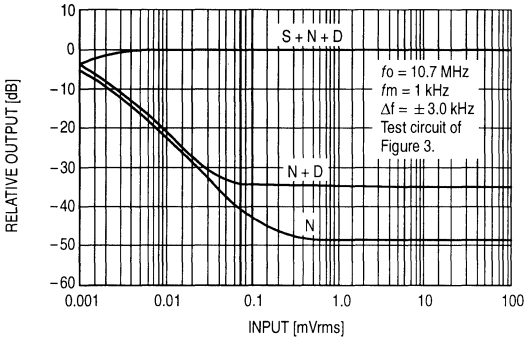


Figure 11. Audio Output and Total Current Drain versus Supply Voltage

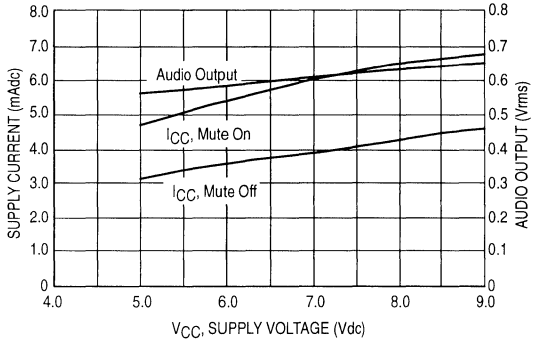


Figure 12. L/C Oscillator, Temperature and Power Supply Sensitivity

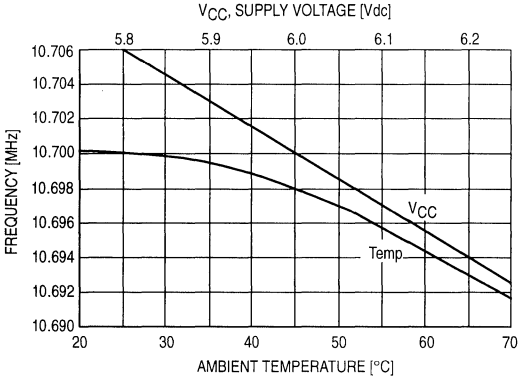


Figure 13. Op Amp Gain and Phase Response

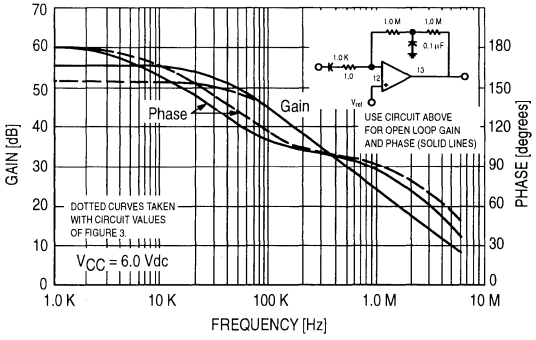


Figure 14. L/C Oscillator Recommended Component Values

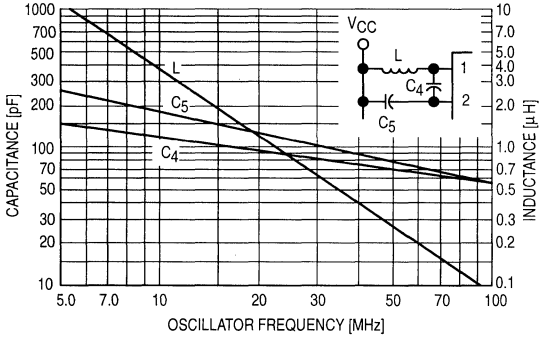


Figure 15. The Op Amp as a Bandpass Filter

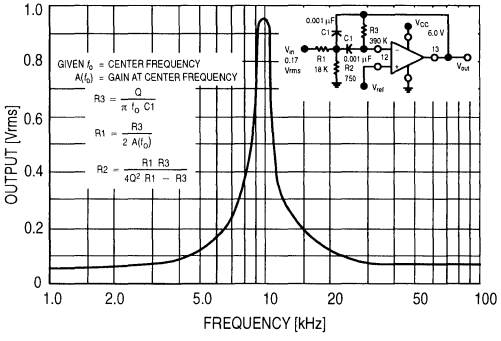
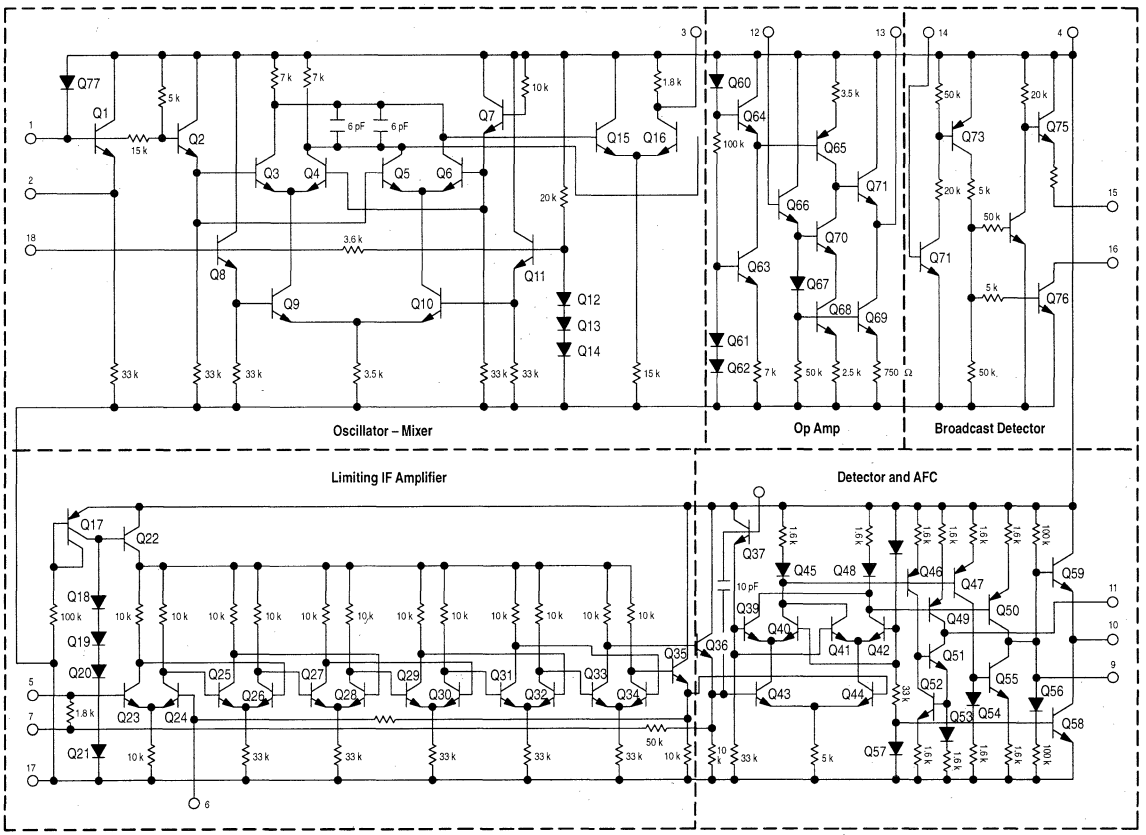


Figure 16. Representative Schematic Diagram



CIRCUIT DESCRIPTION

The MC3359 is a low–power FM IF circuit designed primarily for use in voice–communication scanning receivers. It is also finding a place in narrowband data links.

In the typical application (Figure 1), the mixer–oscillator combination converts the input frequency (10.7 MHz) down to 455 kHz, where, after external bandpass filtering, most of the amplification is done. The audio is recovered using a conventional quadrature FM detector. The absence of an input signal is indicated by the presence of noise above the desired audio frequencies. This "noise band" is monitored by an active filter and a detector. A squelch–trigger circuit indicates the presence of noise (or a tone) by an output which can be used to control scanning. At the same time, an internal switch is operated which can be used to mute the audio.

APPLICATIONS INFORMATION

The oscillator is an internally biased Colpitts type with the collector, base, and emitter connections at Pin 4, 1 and 2, respectively. The crystal is used in fundamental mode, calibrated for parallel resonance at 32 pF load capacitance. In theory this means that the two capacitors in series should be 32 pF, but in fact much larger values do not significantly affect the oscillator frequency, and provide higher oscillator output.

The oscillator can also be used in the conventional L/C Colpitts configuration without loss of mixer conversion gain. This oscillator is, of course, much more sensitive to voltage and temperature as shown in Figure 12. Guidelines for choosing L and C values are given in Figure 14.

The mixer is doubly balanced to reduce spurious responses. The mixer measurements of Figure 4 and 6 were made using an external 50 Ω source and the internal 1.8 k at Pin 3. Voltage gain curves at several V_{CC} voltages are shown in Figure 4. The Third Order Intercept curves of Figure 6 are shown using the conventional dBm scales. Measured power gain (with the 50 Ω input) is approximately 18 dB but the useful gain is much higher because the mixer input impedance is over 3 kΩ. Most applications will use a 330 Ω 10.7 MHz crystal filter ahead of the mixer. For higher frequencies, the relative mixer gain is given in Figure 8.

Following the mixer, a ceramic bandpass filter is recommended. The 455 kHz types come in bandwidths from ± 2 kHz to ± 15 kHz and have input and output impedances of 1.5 k to 2.0 k. For this reason, the Pin 5 input to the 6 stage limiting IF has an internal 1.8 k resistor. The IF has a 3 dB limiting sensitivity of approximately 100 μV at Pin 5 and a useful frequency range of about 5 MHz as shown in Figure 5. The frequency limitation is due to the high resistance values in the IF, which were necessary to meet the low power requirement. The output of the limiter is internally connected to the quadrature detector, including the 10 pF quadrature capacitor. Only a parallel L/C is needed externally from Pin 8 to V_{CC}. A shunt resistance can be added to widen the peak separation of the quadrature detector.

The detector output is amplified and buffered to the audio output, Pin 10, which has an output impedance of approximately 300 Ω. Pin 9 provides a high impedance (50 k) point in the output amplifier for application of a filter or de–emphasis capacitor. Pin 11 is the AFC output, with high gain and high output impedance (1 M). If not needed, it should be grounded, or it can be connected to Pin 9 to double the recovered audio. The detector and AFC responses are shown in Figure 7.

Overall performance of the MC3359 from mixer input to audio output is shown in Figure 9 and 10. The MC3359 can also be operated in "single conversion" equipment; i.e., the mixer can be used as a 455 kHz amplifier. The oscillator is disabled by connecting Pin 1 to Pin 2. In this mode, the overall performance is identical to the 10.7 MHz results of Figure 9.

A simple inverting op amp is provided with an output at Pin 13 providing dc bias (externally) to the input at Pin 12, which is referred internally to 2.0 V. A filter can be made with external impedance elements to discriminate between frequencies. With an external AM detector, the filtered audio signal can be checked for the presence of either noise above the normal audio, or a tone signal.

The open loop response of this op amp is given in Figure13. Bandpass filter design information is provided in Figure 15.

A low bias to Pin 14 sets up the squelch–trigger circuit so that Pin 15 is high, a source of at least 2.0 mA, and the audio mute (Pin 16) is open–circuit. If Pin 14 is raised to 0.7 V by the noise or tone detector, Pin 15 becomes open circuit and Pin 16 is internally short circuited to ground. There is no hysteresis. Audio muting is accomplished by connecting Pin 16 to a high–impedance ground–reference point in the audio path between Pin 10 and the audio amplifier. No dc voltage is needed, in fact it is not desirable because audio "thump" would result during the muting function. Signal swing greater than 0.7 V below ground on Pin 16 should be avoided.

MC3361C

Low Power Narrowband FM IF

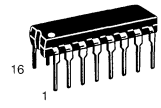
2

The MC3361C includes an Oscillator, Mixer, Limiting Amplifier, Quadrature Discriminator, Active Filter, Squelch, Scan Control and Mute Switch. This device is designed for use in FM dual conversion communications equipment.

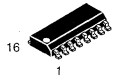
- Operates from 2.0 to 8.0 V Supply
- Low Drain Current 2.8 mA Typical @ V_{CC} = 4.0 Vdc
- Excellent Sensitivity: Input Limiting Voltage – – 3.0 dB = 2.6 μV Typical
- Low Number of External Parts Required
- Operating Frequency Up to 60 MHz
- Full ESD Protection

LOW POWER NARROWBAND FM IF

SEMICONDUCTOR TECHNICAL DATA

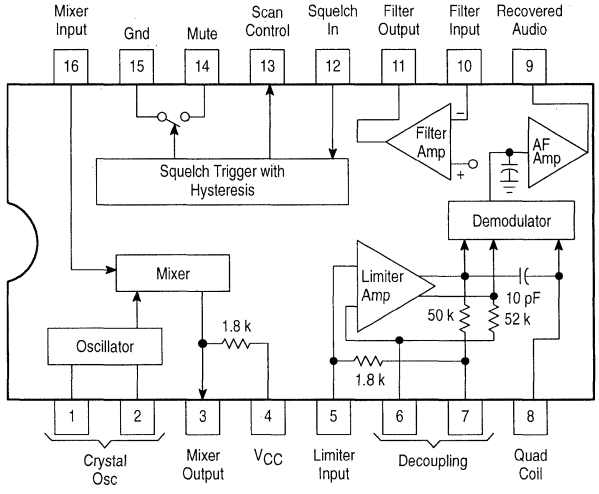


P SUFFIX
PLASTIC PACKAGE
CASE 648



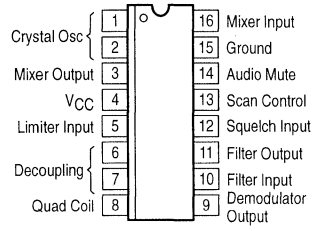
D SUFFIX
PLASTIC PACKAGE
CASE 751B
(SO–16)

Representative Block Diagram



This device contains 92 active transistors.

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC3361CD	T_A = – 30 to +70°C	SO–16
MC3361CP		Plastic DIP

MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted.)

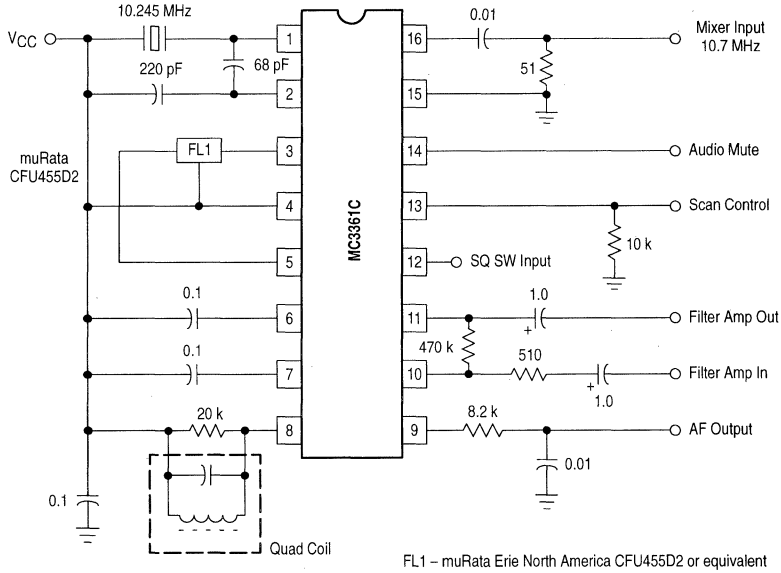
Rating	Pin	Symbol	Value	Unit
Power Supply Voltage	4	V_{CC}(max)	10	Vdc
Operating Supply Voltage Range	4	V_{CC}	2.0 to 8.0	Vdc
Detector Input Voltage	8	–	1.0	Vp–p
Input Voltage ($V_{CC} \geq$ 4.0 V)	16	V_{16}	1.0	V_{RMS}
Mute Function	14	V_{14}	–0.5 to +5.0	V_{pk}
Junction Temperature	–	T_J	150	°C
Operating Ambient Temperature Range	–	T_A	–30 to +70	°C
Storage Temperature Range	–	T_{stg}	–65 to +150	°C

2

ELECTRICAL CHARACTERISTICS (V_{CC} = 4.0 Vdc, f_o = 10.7 MHz, $\Delta f = \pm$ 3.0 kHz, f_{mod} = 1.0 kHz, T_A = 25°C, unless otherwise noted.)

Characteristic	Pin	Min	Typ	Max	Unit
Drain Current (No Signal) Squelch "Off" Squelch "On"	4	 2.0 3.7	 2.8 5.2	 3.5 6.3	mA
Recovered Audio Output Voltage (V_{in} = 10 mVrms)	9	130	170	210	mVrms
Input Limiting Voltage (–3.0 dB Limiting)	16	–	2.6	6.0	µV
Total Harmonic Distortion	9	–	0.86	–	%
Recovered Output Voltage (No Input Signal)	9	60	190	350	mVrms
Drop Voltage AF Gain Loss	9	– 3.0	– 0.6	–	dB
Detector Output Impedance	–	–	450	–	Ω
Filter Gain (10 kHz) (V_{in} = 0.3 mVrms)	–	40	50	–	dB
Filter Output Voltage	11	0.5	0.7	0.9	Vdc
Mute Function Low	14	–	30	50	Ω
Mute Function High	14	1.0	11	–	MΩ
Scan Function Low (Mute "Off") (V_{12} = 1.0 Vdc)	13	–	0	0.4	Vdc
Scan Function High (Mute "On") (V_{12} = Gnd)	13	3.0	3.9	–	Vdc
Trigger Hysteresis	–	–	45	100	mV
Mixer Conversion Gain	3	–	28	–	dB
Mixer Input Resistance	16	–	3.3	–	kΩ
Mixer Input Capacitance	16	–	9.0	–	pF

Figure 1. Test Circuit



FL1 – muRata Erie North America CFU455D2 or equivalent

Quadrature Coil – Toko America Type 7MC–8128Z or equivalent

C – μF, unless noted

Figure 2. Audio Output, Distortion versus Supply Voltage

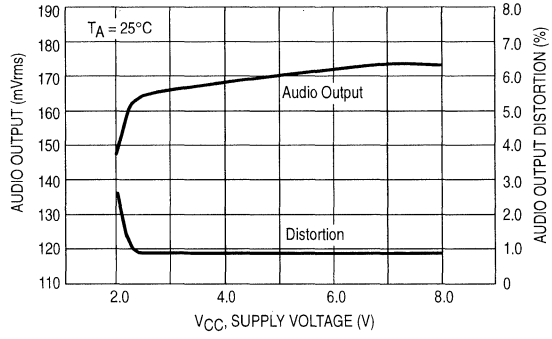


Figure 3. Audio Output, Distortion versus Temperature

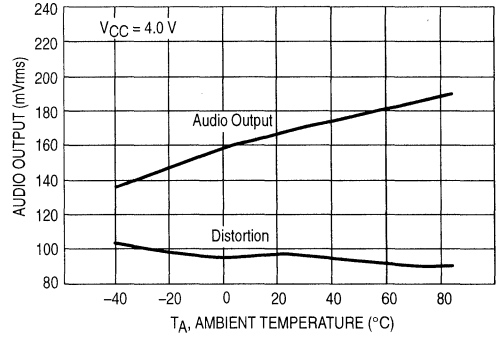


Figure 4. Low Voltage Low Power Narrowband FM IF

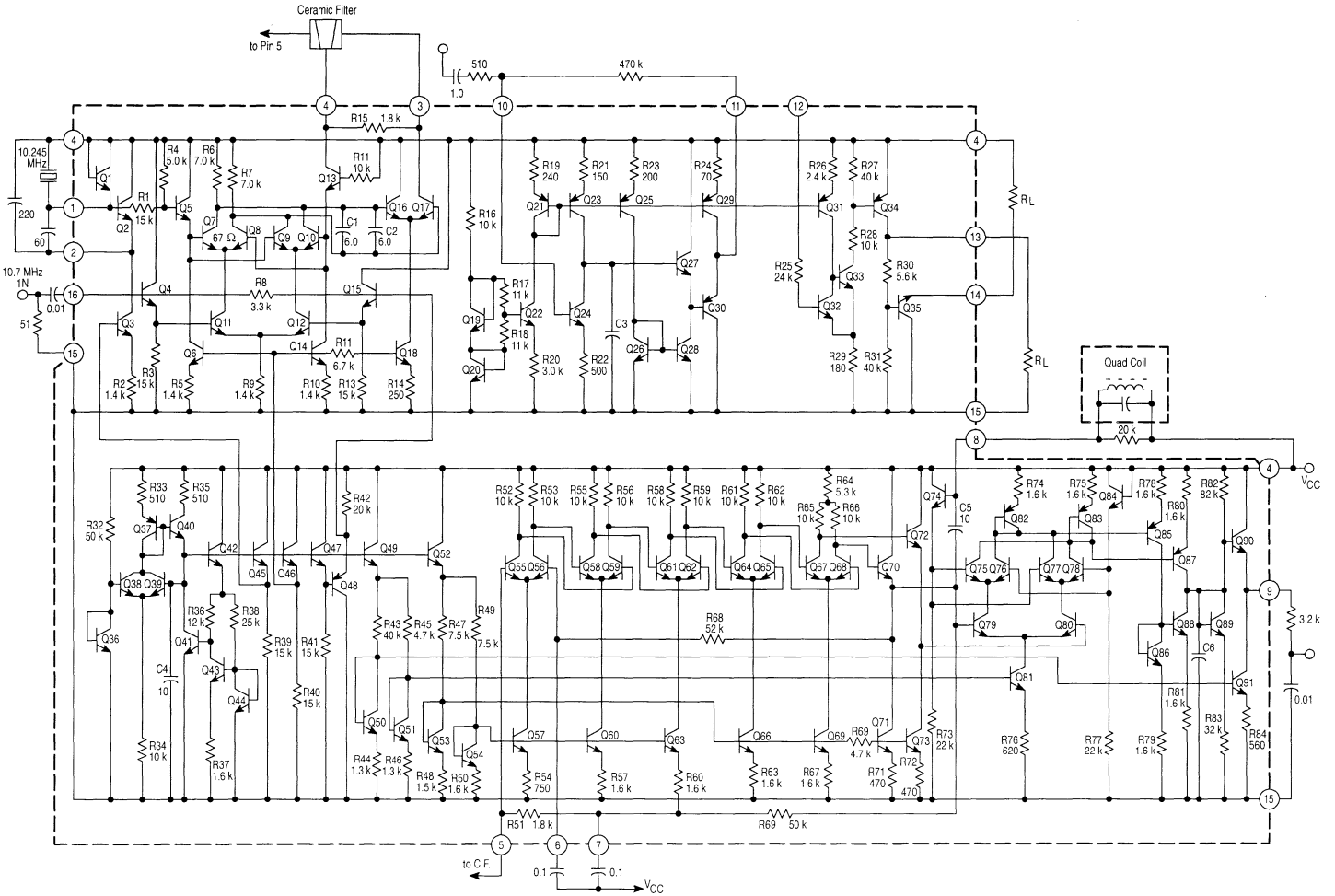


Figure 5. Input Limiting Voltage

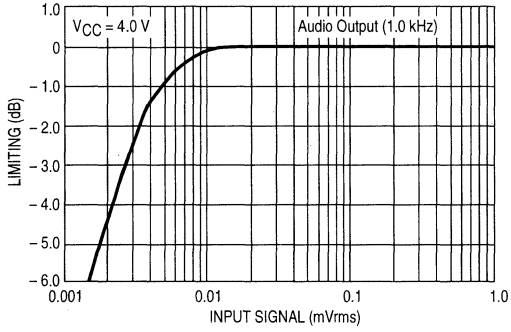


Figure 6. Overall Gain, Noise and AM Rejection

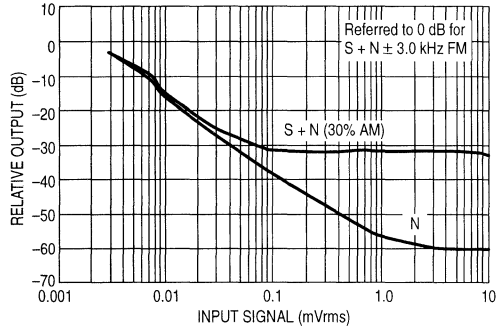


Figure 7. Filter Amp Response

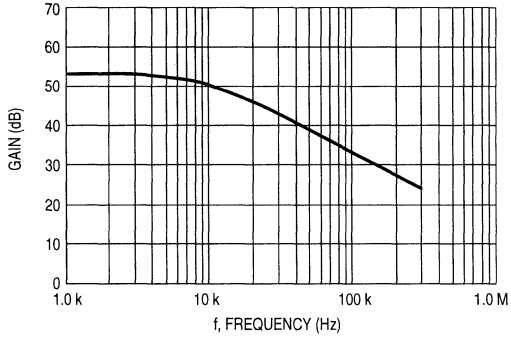


Figure 8. Filter Amp Gain

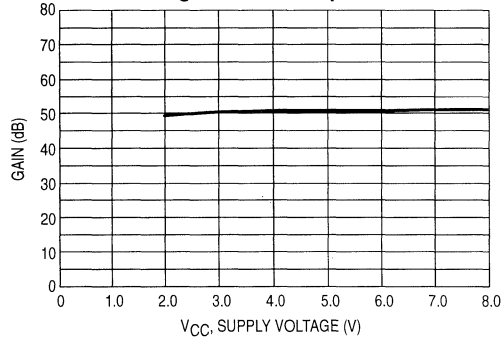


Figure 9. Supply Current

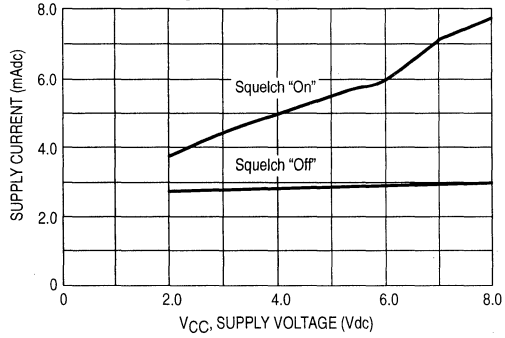
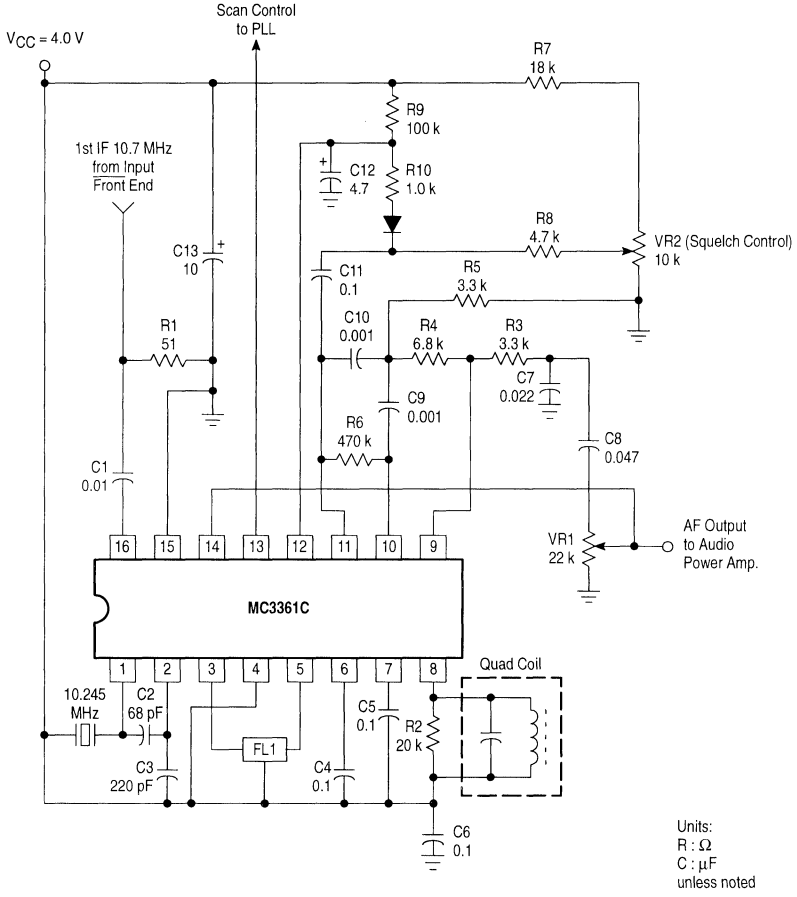


Figure 10. Simplified Application



FL1 – muRata Erie North America Type CFU455D2 or equivalent

Quadrature Coil – Toko America Type 7MC–8128Z or equivalent

MOTOROLA

MC3362

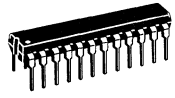
Low-Power Narrowband FM Receiver

. . . includes dual FM conversion with oscillators, mixers, quadrature discriminator, and meter drive/carrier detect circuitry. The MC3362 also has buffered first and second local oscillator outputs and a comparator circuit for FSK detection.

- Complete Dual Conversion Circuitry
- Low Voltage: V_{CC} = 2.0 to 6.0 Vdc
- Low Drain Current (3.6 mA (Typical) @ V_{CC} = 3.0 Vdc)
- Excellent Sensitivity: Input Voltage 0.6 μVrms (Typical) for 12 dB SINAD
- Externally Adjustable Carrier Detect Function
- Low Number of External Parts Required
- Manufactured Using Motorola's MOSAIC® Process Technology
- MC13135 is Preferred for New Designs

LOW–POWER DUAL CONVERSION FM RECEIVER

SEMICONDUCTOR TECHNICAL DATA



P SUFFIX
PLASTIC PACKAGE
CASE 724

DW SUFFIX
PLASTIC PACKAGE
CASE 751E
(SO-24L)

Figure 1. Simplified Application in a PLL Frequency Synthesized Receiver

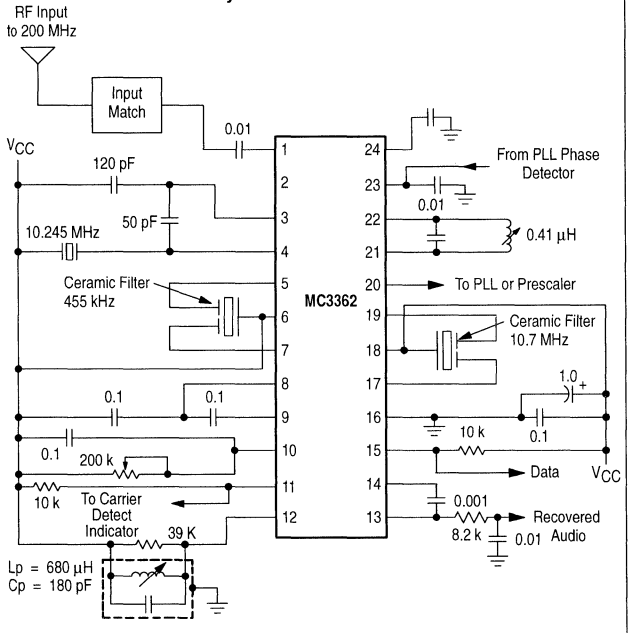
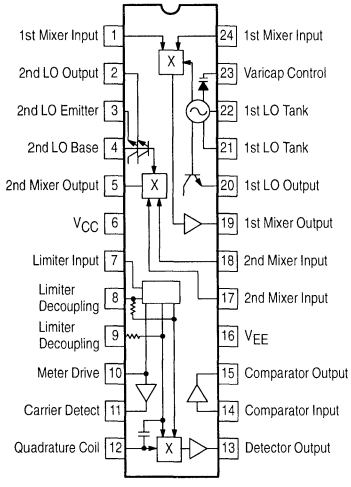


Figure 2. Pin Connections and Representative Block Diagram



ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC3362DW	T_A = – 40 to +85°C	SO–24L
MC3362P		Plastic DIP

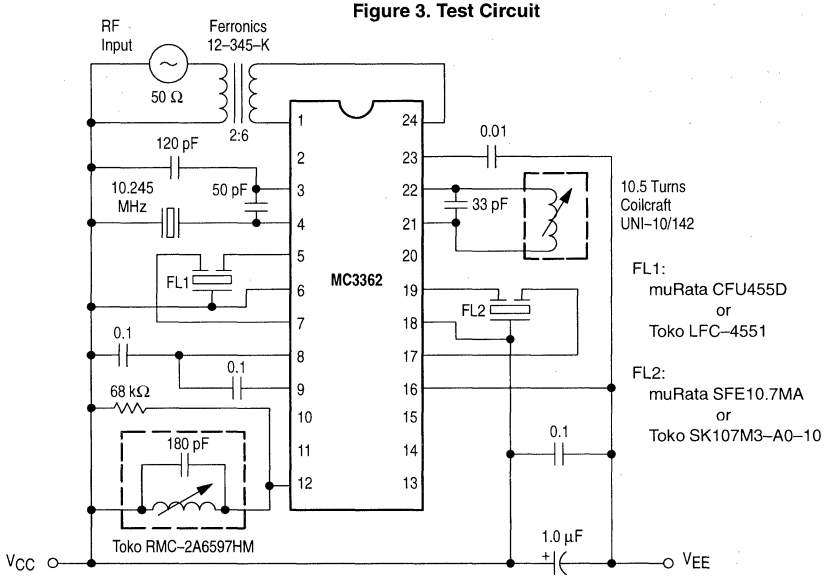
MAXIMUM RATING (T_A = 25°C, unless otherwise noted)

Rating	Pin	Symbol	Value	Unit
Power Supply Voltage (See Figure 2)	6	$V_{CC(max)}$	7.0	Vdc
Operating Supply Voltage Range (Recommended)	6	V_{CC}	2.0 to 6.0	Vdc
Input Voltage ($V_{CC} \geq$ 5.0 Vdc)	1, 24	V_{1-24}	1.0	Vrms
Junction Temperature	–	T_J	150	°C
Operating Ambient Temperature Range	–	T_A	– 40 to + 85	°C
Storage Temperature Range	–	T_{stg}	– 65 to + 150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 Vdc, f_o = 49.7 MHz, Deviation = 3.0 kHz, T_A = 25°C, Test Circuit of Figure 3, unless otherwise noted)

Characteristic	Pin	Min	Typ	Max	Units
Drain Current (Carrier Detect Low – See Figure 5)	6	–	4.5	7.0	mA
Input for –3.0 dB Limiting		–	0.7	2.0	μVrms
Input for 12 dB SINAD (See Figure 9)		–	0.6	–	μVrms
Series Equivalent Input Impedence		–	450–j350	–	Ω
Recovered Audio (RF signal level = 10 mV)	13	–	350	–	mVrms
Noise Output (RF signal level = 0 mV)	13	–	250	–	mVrms
Carrier Detect Threshold (below V_{CC})	10	–	0.64	–	Vdc
Meter Drive Slope	10	–	100	–	nA/dB
Input for 20 dB (S + N)/N (See Figure 7)		–	0.7	–	μVrms
First Mixer 3rd Order Intercept (Input)		–	–22	–	dBm
First Mixer Input Resistance (Rp)		–	690	–	Ω
First Mixer Input Capacitance (Cp)		–	7.2	–	pF
Conversion Voltage Gain, First Mixer		–	18	–	dB
Conversion Voltage Gain, Second Mixer		–	21	–	
Dector Output Resistance	13	–	1.4	–	kΩ

Figure 3. Test Circuit



NOTE: See AN980 for Additional Design Information.

Figure 4. I_{Meter} versus Input

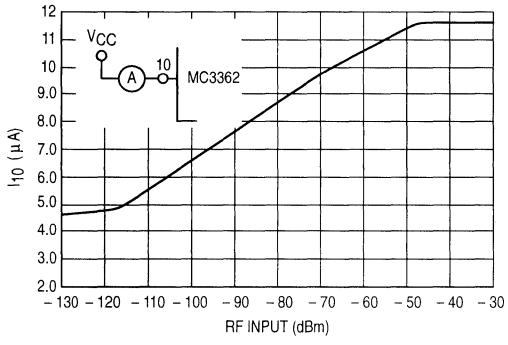


Figure 5. Drain Current, Recovered Audio versus Supply

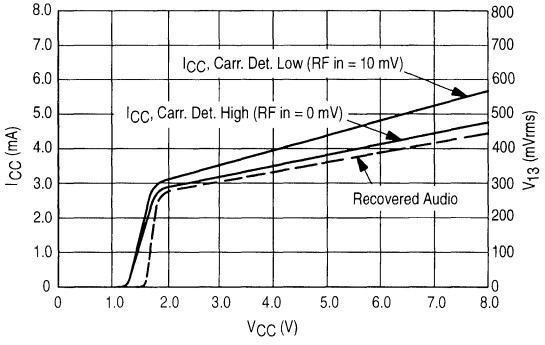


Figure 6. Signal Levels

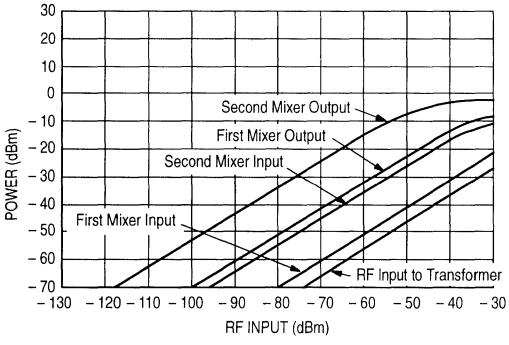


Figure 7. S + N, N, AMR versus Input

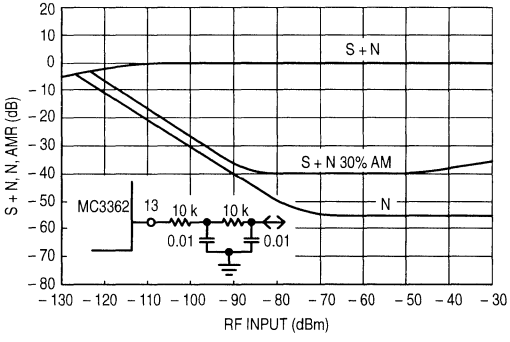


Figure 8. 1st Mixer 3rd Order Intermodulation

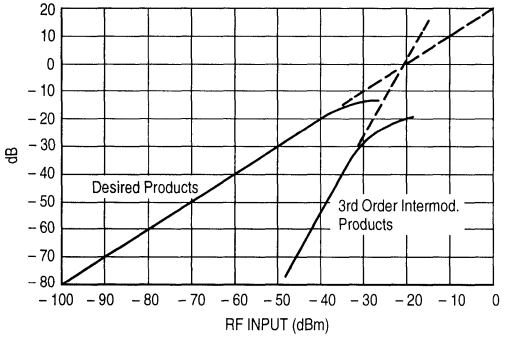


Figure 9. Detector Output versus Frequency

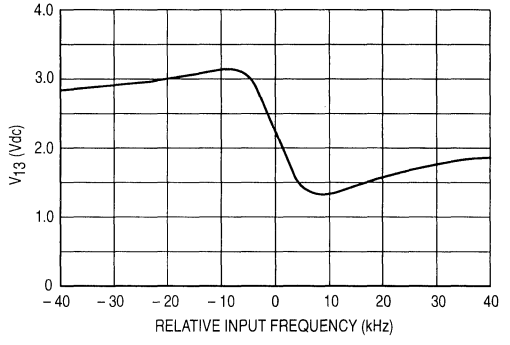
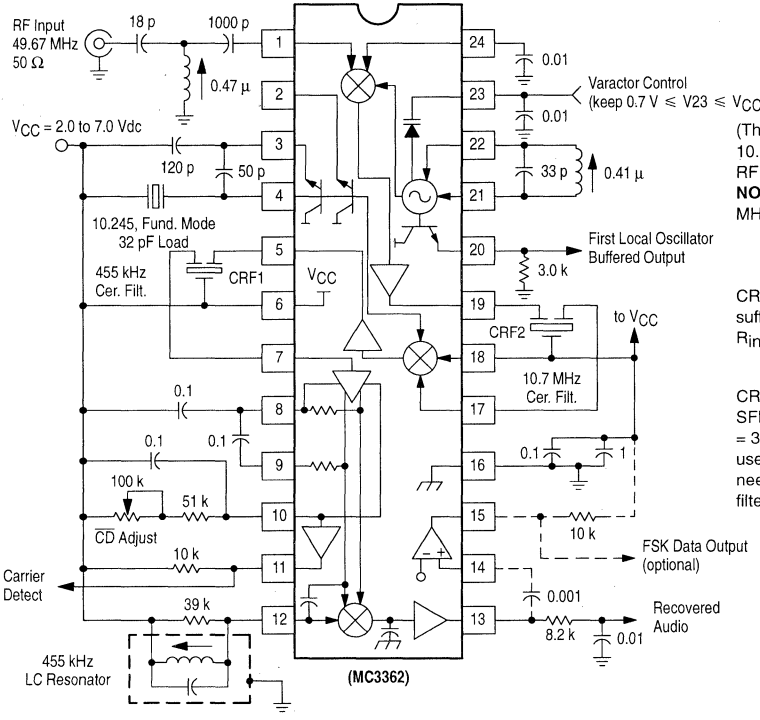


Figure 10. PC Board Test Circuit
(LC Oscillator Configuration Used in PLL Synthesized Receiver)

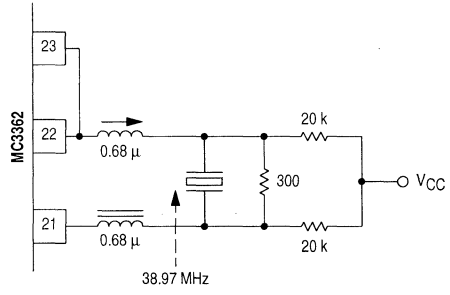


(This network must be tuned to exactly 10.7 MHz above or below the incoming RF signal.
NOTE: The IF is rolled off above 10.7 MHz to reduce L.O. feedthrough.)

CRF1 = muRata CFU 455X – the X suffix denotes 6.0 dB bandwidth. $R_{in} = R_{out}$ = 1.5 to 2.0 kΩ.

CRF2 = muRata SFA10.7 MF5 or SFE10.7 or equivalent. $R_{in} = R_{out}$ = 330 Ω. Crystal filters can be used but impedance matching will need to be added to ensure proper filter characteristics are realized.

Figure 10A. Crystal Oscillator Configuration for Single Channel Application



Crystal used is series mode resonant (no load capacity specified), 3rd overtone. This method has not proven adequate for fundamental mode, 5th or 7th overtone crystals. The inductor and capacitor will need to be changed for other frequency crystals. See AN980 for further information.

Figure 11. Component Placement View Showing Crystal Oscillator Circuit

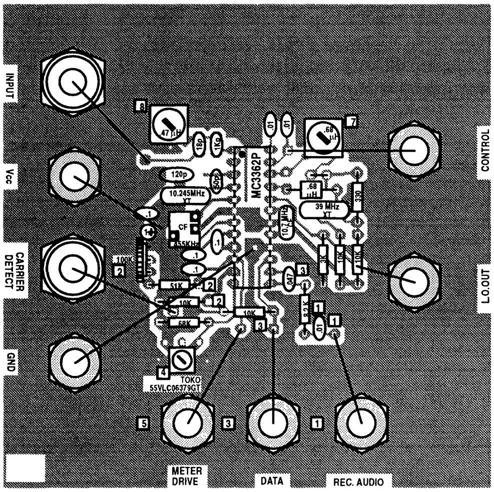
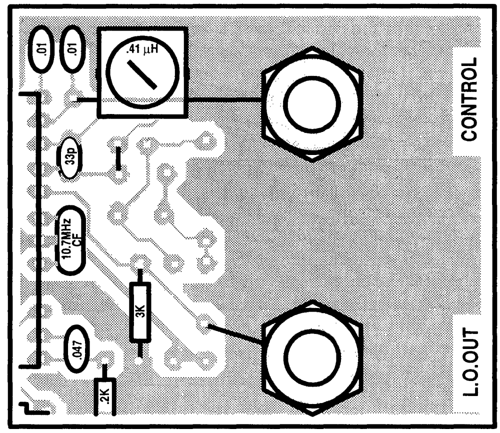


Figure 11A. LC Oscillator Component View



NOTES: 1. Recovered Audio components may be deleted when using data output.
2. Carrier Detect components must be deleted in order to obtain linear Meter Drive output. With these components in place the Meter Drive outputs serve only to trip the Carrier Detect indicator.
3. Data Output components should be deleted in applications where only audio modulation is used. For combined audio/data applications, the 0.047 µF coupling capacitor will add distortion to the audio, so a pull–down resistor at pin 13 may be required.
4. Use Toko 7MC81282 Quadrature coil.
5. Meter Drive cannot be used simultaneously with Carrier Detect output. For analog meter drive, remove components labelled "2" and measure meter current (4–12 µA) through ammeter to V_{CC}.
6. Either type of oscillator circuit may be used with any output circuit configuration.
7. LC Oscillator Coil: Coilcraft UNI 10/42 10.5 turns, 0.41 µH Crystal Oscillator circuit: trim coil, 0.68 µH. Coilcraft M1287–A.
8. 0.47 H, Coilcraft M1286–A. Input LC network used to match first mixer input impedance to 50 Ω.

CIRCUIT DESCRIPTION

The MC3362 is a complete FM narrowband receiver from antenna input to audio preamp output. The low voltage dual conversion design yields low power drain, excellent sensitivity and good image rejection in narrowband voice and data link applications.

In the typical application (Figure 1), the first mixer amplifies the signal and converts the RF input to 10.7 MHz. This IF signal is filtered externally and fed into the second mixer, which further amplifies the signal and converts it to a 455 kHz IF signal. After external bandpass filtering, the low IF is fed into the limiting amplifier and detection circuitry. The audio is recovered using a conventional quadrature detector. Twice–IF filtering is provided internally.

The input signal level is monitored by meter drive circuitry which detects the amount of limiting in the limiting amplifier. The voltage at the meter drive pin determines the state of the carrier detect output, which is active low.

APPLICATIONS INFORMATION

The first local oscillator can be run using a free–running LC tank, as a VCO using PLL synthesis, or driven from an external crystal oscillator. It has been run to 190 MHz.* A buffered output is available at Pin 20. The second local oscillator is a common base Colpitts type which is typically run at 10.245 MHz under crystal control. A buffered output is available at Pin 2. Pins 2 and 3 are interchangeable.

The mixers are doubly balanced to reduce spurious responses. The first and second mixers have conversion gains of 18 dB and 22 dB (typical), respectively, as seen in Figure 6. Mixer gain is stable with respect to supply voltage. For both conversions, the mixer impedances and pin layout are designed to allow the user to employ low cost, readily available ceramic filters. Overall sensitivity and AM rejection are shown in Figure 7. The input level for 20 dB (S + N)/N is 0.7 µV using the two–pole post–detection filter pictured.

* If the first local oscillator (Pins 21 and/or 22) is driven from a strong external source (100 mVrms), the mixer can be used to over 450 MHz.

Following the first mixer, a 10.7 MHz ceramic band–pass filter is recommended. The 10.7 MHz filtered signal is then fed into one second mixer input pin, the other input pin being connected to V_{CC}. Pin 6 (V_{CC}) is treated as a common point for emitter–driven signals.

The 455 kHz IF is typically filtered using a ceramic band-pass filter then fed into the limiter input pin. The limiter has 10 μV sensitivity for – 3.0 dB limiting, flat to 1.0 MHz.

The output of the limiter is internally connected to the quadrature detector, including a quadrature capacitor. A parallel LC tank is needed externally from Pin 12 to V_{CC}. A 39 kΩ shunt resistance is included which determines the peak separation of the quadrature detector; a smaller value will increase the spacing and linearity but decrease recovered audio and sensitivity.

A data shaping circuit is available and can be coupled to the recovered audio output of Pin 13. The circuit is a comparator which is designed to detect zero crossings of FSK modulation. Data rates are typically limited to 1200 baud to ensure data integrity and avoid adjacent channel "splatter." Hysteresis is available by connecting a high valued resistor from Pin 15 to Pin 14. Values below 120 kΩ are not recommended as the input signal cannot overcome the hysteresis.

The meter drive circuitry detects input signal level by monitoring the limiting amplifier stages. Figure 4 shows the unloaded current at Pin 10 versus input power. The meter drive current can be used directly (RSSI) or can be used to trip the carrier detect circuit at a specified input power. To do this, pick an RF trip level in dBm. Read the corresponding current from Figure 4 and pick a resistor such that:

$$R_{10} \simeq 0.64\ \text{Vdc} / I_{10}$$

Hysteresis is available by connecting a high valued resistor R_H between Pins 10 and 11. The formula is:

$$\text{Hysteresis} = V_{CC}/(R_H \times 10^{-7})\ \text{dB}$$

Figure 12. Circuit Side View

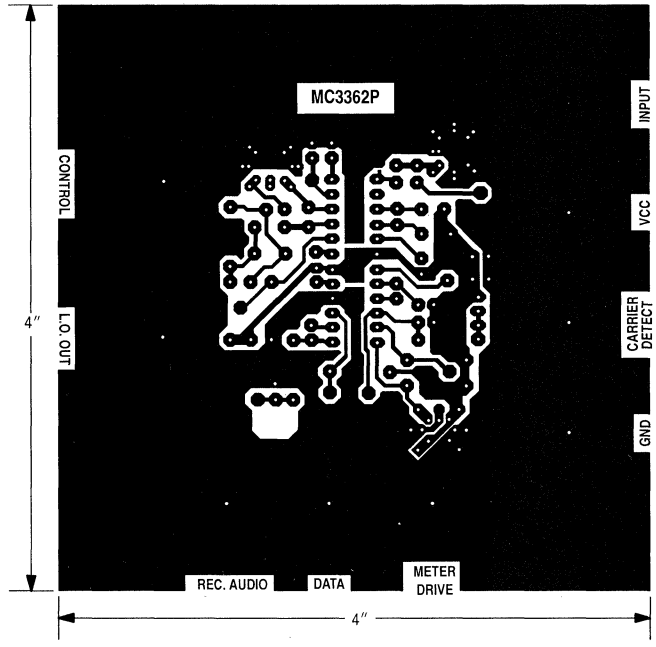
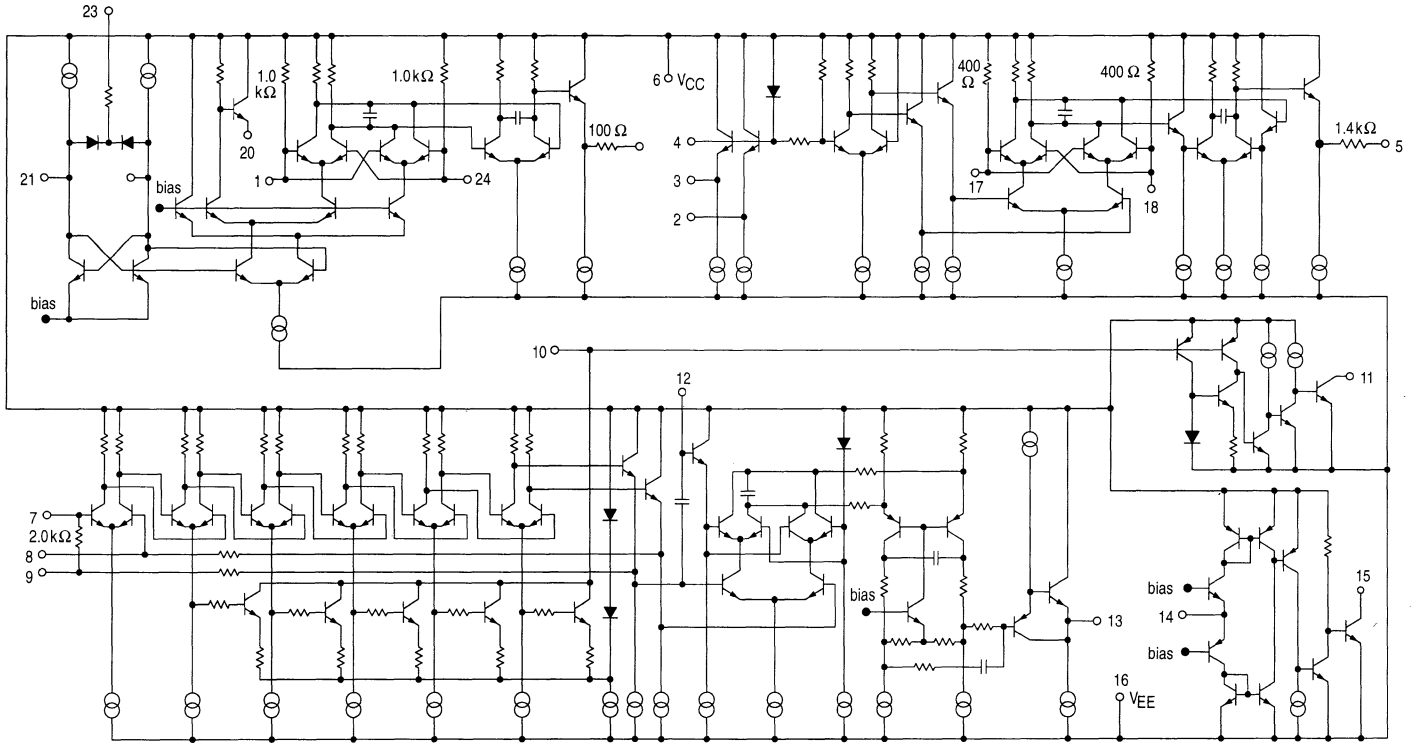


Figure 13. Representative Schematic Diagram



MOTOROLA

MC3363

Low Power Dual Conversion FM Receiver

The MC3363 is a single chip narrowband VHF FM radio receiver. It is a dual conversion receiver with RF amplifier transistor, oscillators, mixers, quadrature detector, meter drive/carrier detect and mute circuitry. The MC3363 also has a buffered first local oscillator output for use with frequency synthesizers, and a data slicing comparator for FSK detection.

- Wide Input Bandwidth – 200 MHz Using Internal Local Oscillator
  – 450 MHz Using External Local Oscillator
- RF Amplifier Transistor
- Muting Operational Amplifier
- Complete Dual Conversion
- Low Voltage: V_{CC} = 2.0 V to 6.0 Vdc
- Low Drain Current: I_{CC} = 3.6 mA (Typical) at V_{CC} = 3.0 V, Excluding RF Amplifier Transistor
- Excellent Sensitivity: Input 0.3 μV (Typical) for 12 dB SINAD Using Internal RF Amplifier Transistor
- Data Shaping Comparator
- Received Signal Strength Indicator (RSSI) with 60 dB Dynamic Range
- Low Number of External Parts Required
- Manufactured in Motorola's MOSAIC® Process Technology

LOW POWER DUAL CONVERSION FM RECEIVER

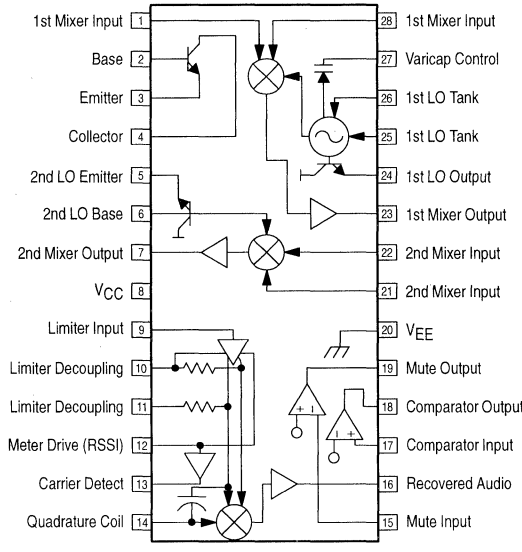
SEMICONDUCTOR TECHNICAL DATA

DW SUFFIX
PLASTIC PACKAGE
CASE 751F
(SO-28L)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC3363DW	T_A = – 40 to +85°C	SO–28L

Figure 1. Pin Connections and Representative Block Diagram



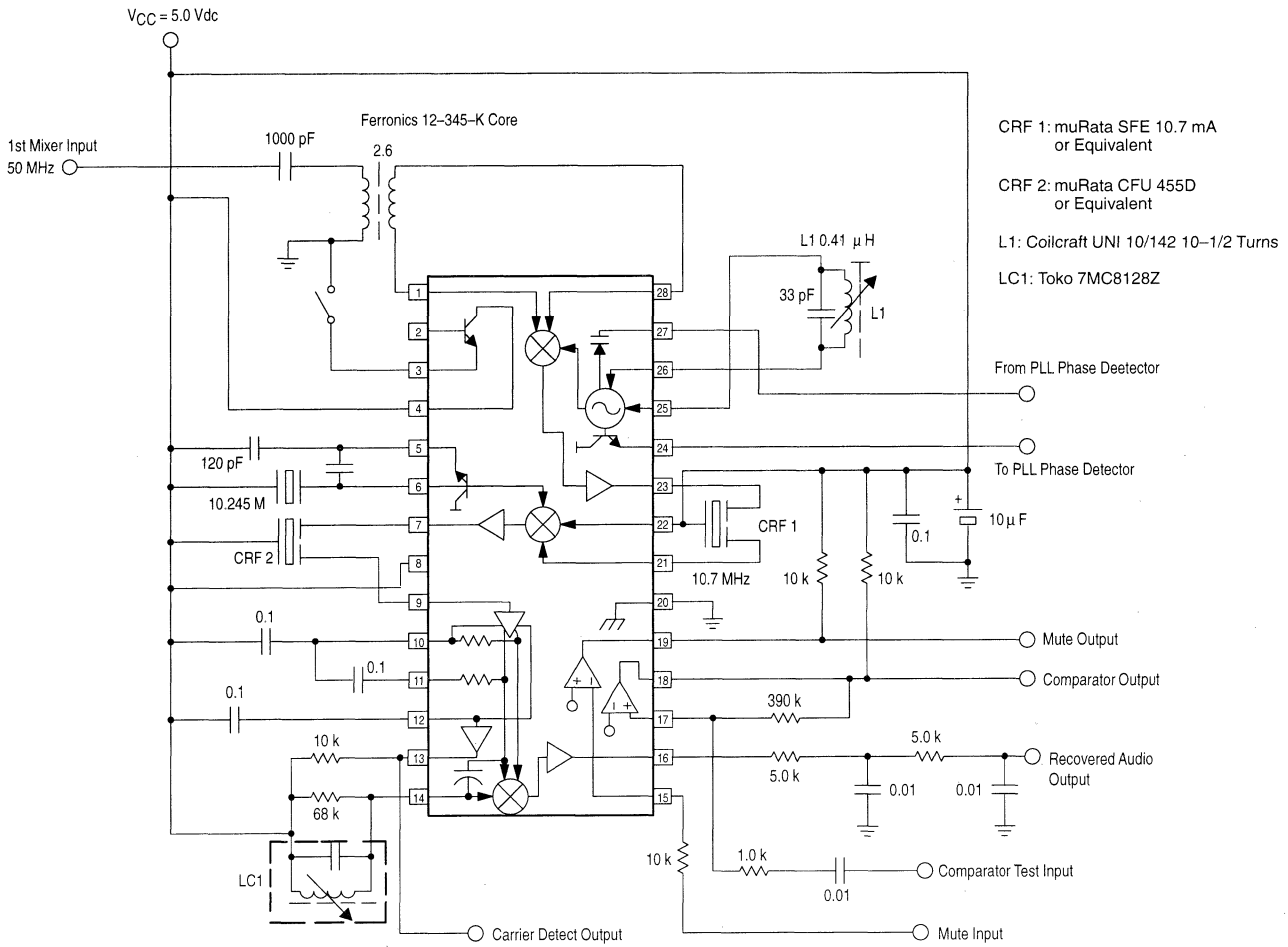
MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Pin	Symbol	Value	Unit
Power Supply Voltage	8	$V_{CC(max)}$	7.0	Vdc
Operating Supply Voltage Range (Recommended)	8	V_{CC}	2.0 to 6.0	Vdc
Input Voltage (V_{CC} = 5.0 Vdc)	1, 28	V_{1-28}	1.0	Vrms
Mute Output Voltage	19	V_{19}	– 0.7 to 8.0	Vpk
Junction Temperature	–	T_J	150	°C
Operating Ambient Temperature Range	–	T_A	– 40 to +85	°C
Storage Temperature Range	–	T_{stg}	– 65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 Vdc, f_O = 49.7 MHz, Deviation = ±3.0 kHz, T_A = 25°C, Mod 1.0 kHz, test circuit of Figure 2 unless otherwise noted)

Characteristic	Pin	Min	Typ	Max	Units
Drain Current (Carrier Detect Low)	8	–	4.5	8.0	mA
–3.0 dB Limiting Sensitivity (RF Amplifier Not Used)		–	0.7	2.0	µVrms
Input For 12 dB SINAD		–	0.3	–	
20 dB S/N Sensitivity (RF Amplifier Not Used)		–	1.0	–	
1st Mixer Input Resistance (Parallel – Rp)	1, 28	–	690	–	Ω
1st Mixer Input Capacitance (Parallel – Cp)	1, 28	–	7.2	–	pF
1st Mixer Conversion Voltage Gain (A_{vc1}, Open Circuit)		–	18	–	dB
2nd Mixer Conversion Voltage Gain)A_{vc2}, Open Circuit)		–	21	–	
2nd Mixer Input Sensitivity (20 dB S/N) (10.7 MHz i/p)	21	–	10	–	µVrms
Limiter Input Sensitivity (20 dB S/N) (455 kHz i/p)	9	–	100	–	
RF Transistor DC Current Drain	4	1.0	1.5	2.5	mAdc
Noise Output Level (RF Signal = 0 mV)	16	–	70	–	mVrms
Recovered Audio (RF Signal Level = 1.0 mV)	16	120	200	–	mVrms
THD of Recovered Aduio (RF Signal = 1.0 mV)	16	–	2%	–	%
Detector Output Impedance	16	–	400	–	Ω
Series Equivalent Input Impedance	1	–	450–j350	–	
Data (Comparator) Output Voltage – High – Low	18	– 0.1	– 0.1	V_{CC} –	Vdc
Data (Comparator) Threshold Voltage Difference	17	70	110	150	mV
Meter Drive Slope	12	70	100	135	nA/dB
Carrier Detect Threshold (Below V_{CC})	12	0.53	0.64	0.77	Vdc
Mute Output Impedance – High – Low	19	– –	10 25	– –	MΩ

Figure 2. Test Circuit



CIRCUIT DESCRIPTION

The MC3363 is a complete FM narrowband receiver from RF amplifier to audio preamp output. The low voltage dual conversion design yields low power drain, excellent sensitivity and good image rejection in narrowband voice and data link applications.

In the typical application, the input RF signal is amplified by the RF transistor and then the first mixer amplifies the signal and converts the RF input to 10.7 MHz. This IF signal is filtered externally and fed into the second mixer, which further amplifies the signal and converts it to a 455 kHz IF signal. After external bandpass filtering, the low IF is fed into the limiting amplifier and detection circuitry. The audio is recovered using a conventional quadrature detector. Twice-IF filtering is provided internally.

The input signal level is monitored by meter drive circuitry which detects the amount of limiting in the limiting amplifier. The voltage at the meter drive pin determines the state of the carrier detect output, which is active low.

APPLICATIONS INFORMATION

The first local oscillator is designed to serve as the VCO in a PLL frequency synthesized receiver. The MC3363 can operate together with the MC145166/7 to provide a two-chip ten–channel frequency synthesized receiver in the 46/49 cordless telephone band. The MC3363 can also be used with the MC14515X series of CMOS PLL synthesizers and MC120XX series of ECL prescalers in VHF frequency synthesized applications to 200 MHz.

For single channel applications the first local oscillator can be crystal controlled. The circuit of Figure 4 has been used successfully up to 60 MHz. For higher frequencies an external oscillator signal can be injected into Pins 25 and/or 26 — a level of approximately 100 mVrms is recommended. The first mixer's transfer characteristic is essentially flat to 450 MHz when this approach is used (keeping a constant 10.7 MHz IF frequency). The second local oscillator is a Colpitts type which is typically run at 10.245 MHz under crystal control.

The mixers are doubly balanced to reduce spurious responses. The first and second mixers have conversion gains of 18 dB and 21 dB (typical), respectively. Mixer gain is stable with respect to supply voltage. For both conversions, the mixer impedances and pin layout are designed to allow the user to employ low cost, readily available ceramic filters.

Following the first mixer, a 10.7 MHz ceramic bandpass filter is recommended. The 10.7 MHz filtered signal is then fed into the second mixer input Pin 21, the other input Pin 22 being connected to V_{CC}.

The 455 kHz IF is filtered by a ceramic narrow bandpass filter then fed into the limiter input Pin 9. The limiter has 10 μV sensitivity for −3.0 dB limiting, flat to 1.0 MHz.

NOTE: For further application and design information, refer to AN980.

The output of the limiter is internally connected to the quadrature detector, including a quadrature capacitor. A parallel LC tank is needed externally from Pin 14 to V_{CC}. A 68 kΩ shunt resistance is included which determines the peak separation of the quadrature detector; a smaller value will lower the Q and expand the deviation range and linearity, but decrease recovered audio and sensitivity.

A data shaping circuit is available and can be coupled to the recovered audio output of Pin 16. The circuit is a comparator which is designed to detect zero crossings of FSK modulation. Data rates of up to 35000 baud are detectable using the comparator. Best sensitivity is obtained when data rates are limited to 1200 baud maximum. Hysteresis is available by connecting a high-valued resistor from Pin 17 to Pin 18. Values below 120 kΩ are not recommended as the input signal cannot overcome the hysteresis.

The meter drive circuitry detects input signal level by monitoring the limiting of the limiting amplifier stages. Figure 5 shows the unloaded current at Pin 12 versus input power. The meter drive current can used directly (RSSI) or can be used to trip the carrier detect circuit at a specified input power.

A muting op amp is provided and can be triggered by the carrier detect output (Pin 13). This provides a carrier level triggered squelch circuit which is activated when the RF input at the desired input frequency falls below a present level. The level at which this occurs is determined by the resistor placed between the meter drive output (Pin 12) and V_{CC}. Values between 80–130 kΩ are recommended. This type of squelch is pictured in Figures 3 and 4.

Hysteresis is available by connecting a high-valued resistor Rh between Pins 12 and 13. The formula is:

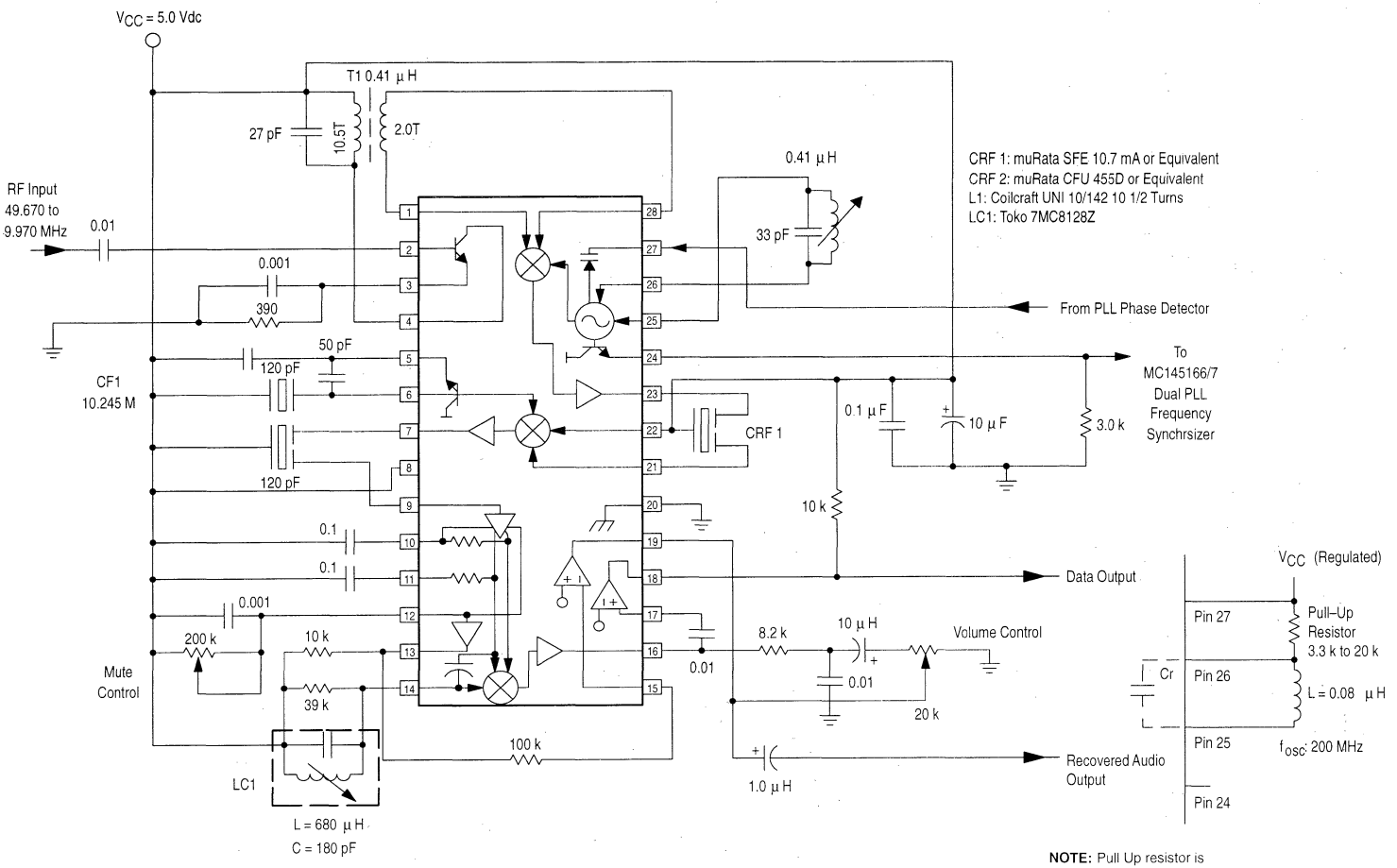
$$\text{Hyst} = V_{CC} / (\text{Rh} \times 10^{-7}) \text{ dB}$$

The meter drive can also be used directly to drive a meter or to provide AGC. A current to voltage converter or other linear buffer will be needed for this application.

A second possible application of the op amp would be in a noise triggered squelch circuit, similar to that used with the MC3357/MC3359/MC3361B FM IFs. In this case the op amp would serve as an active noise filter, the output of which would be rectified and compared to a reference on a squelch gate. The MC3363 does not have a dedicated squelch gate, but the NPN RF input stage or data shaping comparator might be used to provide this function if available. The op amp is a basic type with the inverting input and the output available. This application frees the meter drive to allow it to be used as a linear signal strength monitor.

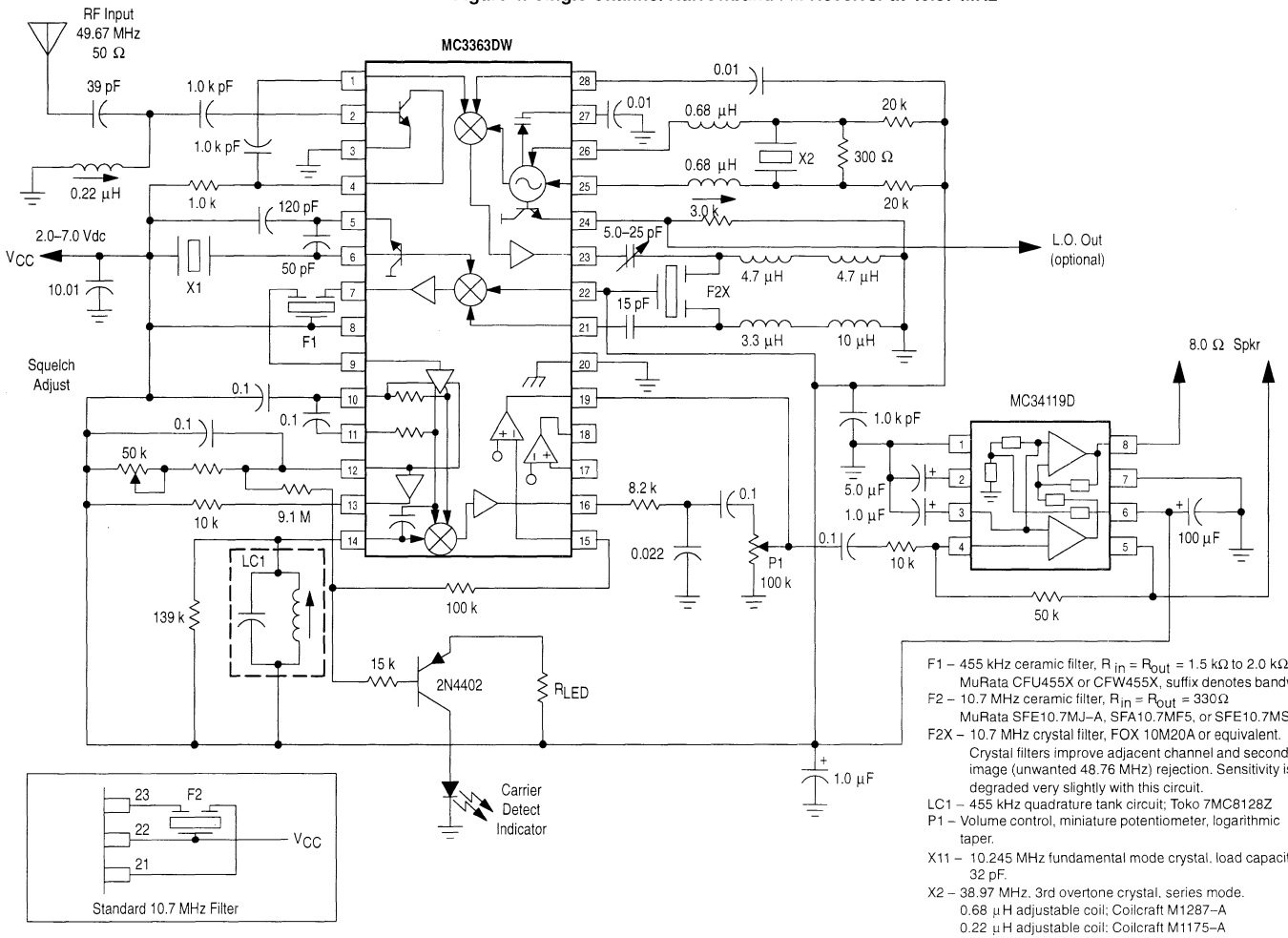
The circuit of Figure 4 is a complete 50 MHz receiver from antenna input to audio preamp output. It uses few components and has good performance. The receiver operates on a single channel and has input sensitivity of < 0.3 μV for 12 dB SINAD.

Figure 3. Typical Application in a PLL Frequency Synthesized Receiver



NOTE: Pull Up resistor is used to run the oscillator above 50 MHz.

Figure 4. Single Channel Narrowband FM Receiver at 49.67 MHz



F1 – 455 kHz ceramic filter, $R_{in} = R_{out}$ = 1.5 kΩ to 2.0 kΩ
MuRata CFU455X or CFW455X, suffix denotes bandwidth
F2 – 10.7 MHz ceramic filter, $R_{in} = R_{out}$ = 330Ω
MuRata SFE10.7MJ–A, SFA10.7MF5, or SFE10.7MS2A.
F2X – 10.7 MHz crystal filter, FOX 10M20A or equivalent.
Crystal filters improve adjacent channel and second image (unwanted 48.76 MHz) rejection. Sensitivity is degraded very slightly with this circuit.
LC1 – 455 kHz quadrature tank circuit; Toko 7MC8128Z
P1 – Volume control, miniature potentiometer, logarithmic taper.
X11 – 10.245 MHz fundamental mode crystal, load capacity 32 pF.
X2 – 38.97 MHz, 3rd overtone crystal, series mode.
0.68 µH adjustable coil; Coilcraft M1287–A
0.22 µH adjustable coil: Coilcraft M1175–A

R_{LED} is used to adjust LED current: $I_{LED} = \frac{V_{CC} - V_{LED}}{R_{LED}}$

Figure 5. Circuit Schematic

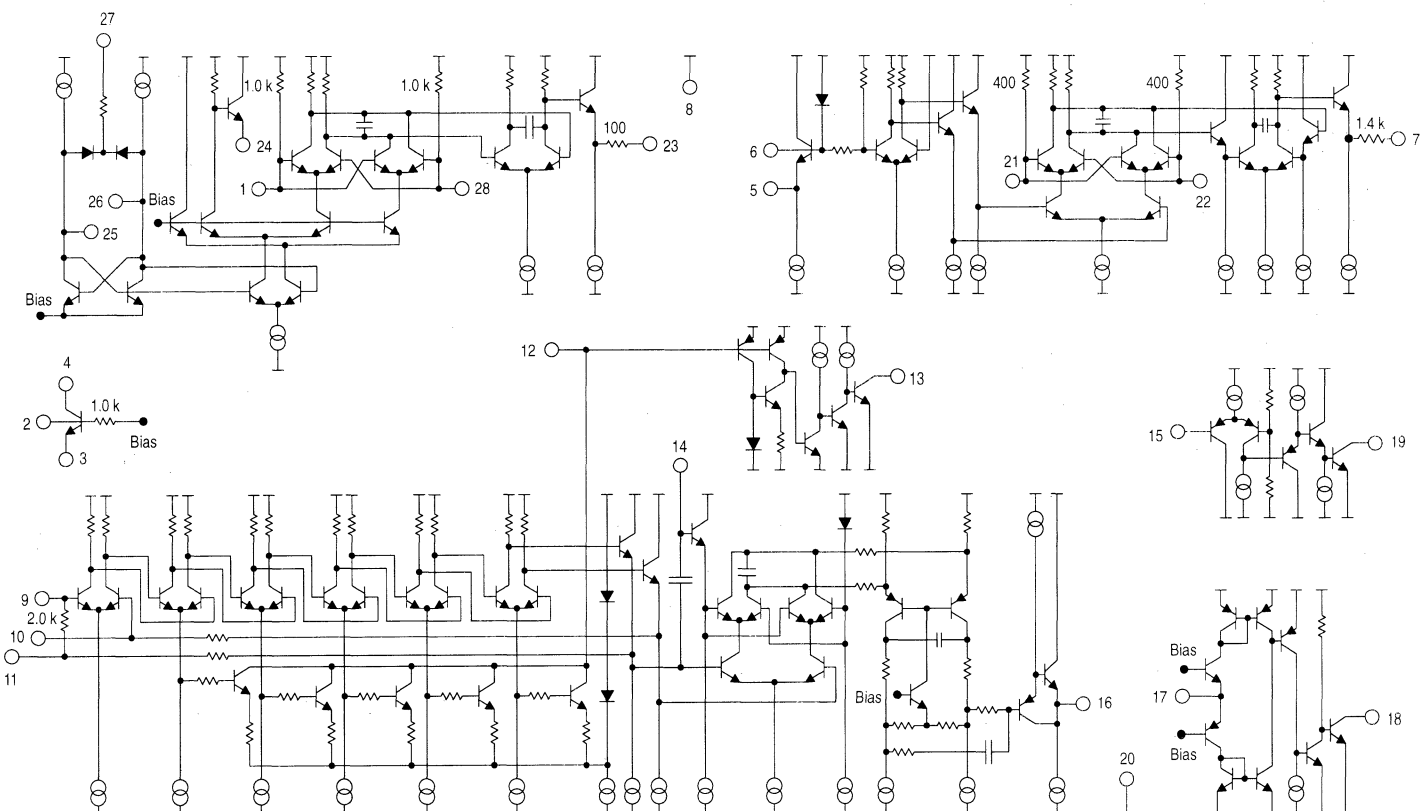


Figure 6. PC Board Component View with High Performance Crystal Filter

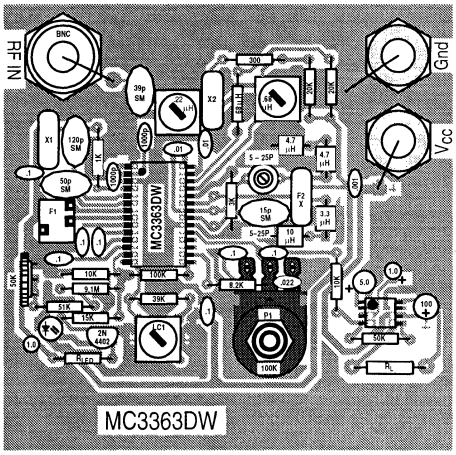


Figure 7. PC Board Circuit Side View

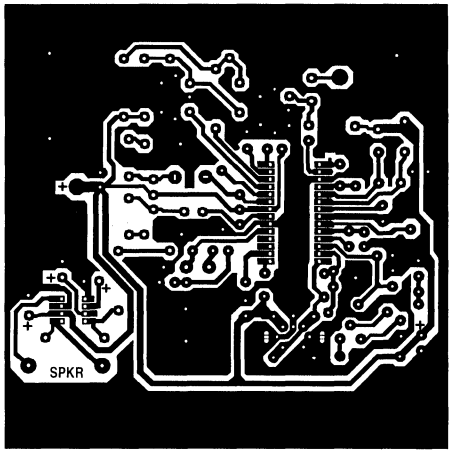
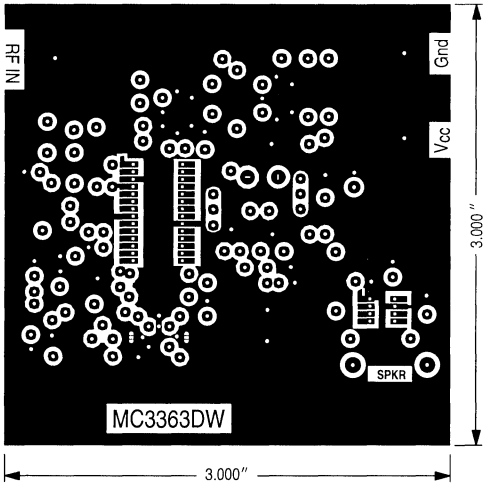


Figure 8. PC Board Component Side Ground Plane



MOTOROLA

MC3371
MC3372, A

Advance Information

Low Power Narrowband FM IF

LOW POWER FM IF

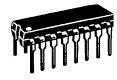
SEMICONDUCTOR TECHNICAL DATA

2

The MC3371 and MC3372 perform single conversion FM reception and consist of an oscillator, mixer, limiting IF amplifier, quadrature discriminator, active filter, squelch switch, and meter drive circuitry. These devices are designed for use in FM dual conversion communication equipment. The MC3371/MC3372 are similar to the MC3361/MC3357 FM IFs, except that a signal strength indicator replaces the scan function controlling driver which is in the MC3361/MC3357. The MC3371 is designed for the use of parallel LC components, while the MC3372 is designed for use with either a 455 kHz ceramic discriminator, or parallel LC components.

These devices also require fewer external parts than earlier products. The MC3371 and MC3372 are available in dual–in–line and surface mount packaging.

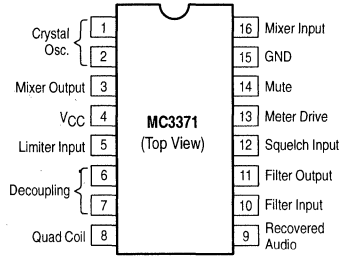
- Wide Operating Supply Voltage Range: V_{CC} = 2.0 to 9.0 V
- Input Limiting Voltage Sensitivity of – 3.0 dB
- Low Drain Current: I_{CC} = 3.2 mA, @ V_{CC} = 4.0 V, Squelch Off
- Minimal Drain Current Increase When Squelched
- Signal Strength Indicator: 60 dB Dynamic Range
- Mixer Operating Frequency Up to 100 MHz
- Fewer External Parts Required than Earlier Devices

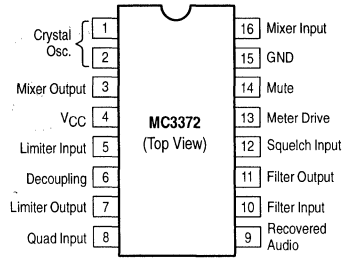


P SUFFIX
PLASTIC PACKAGE
CASE 648

D SUFFIX
PLASTIC PACKAGE
CASE 751B
(SO–16)

PIN CONNECTIONS





MAXIMUM RATINGS

Rating	Pin	Symbol	Value	Unit
Power Supply Voltage	4	V_{CC}(max)	10	Vdc
RF Input Voltage (V_{CC} ≥ 4.0 Vdc)	16	V_{16}	1.0	Vrms
Detector Input Voltage	8	V_8	1.0	V_{p-p}
Squelch Input Voltage (V_{CC} ≥ 4.0 Vdc)	12	V_{12}	6.0	Vdc
Mute Function	14	V_{14}	– 0.7 to 10	V_{pk}
Mute Sink Current	14	I_{14}	50	mA
Junction Temperature	–	T_J	150	°C
Storage Temperature Range	–	T_{stg}	– 65 to + 150	°C

Devices should not be operated at these values. The "Recommended Operating Conditions" table provides conditions for actual device operation.

RECOMMENDED OPERATING CONDITIONS

Rating	Pin	Symbol	Value	Unit
Supply Voltage (@ T_A = 25°C) ($-30°C \leq T_A \leq +75°C$)	4	V_{CC}	2.0 to 9.0 2.4 to 9.0	Vdc
RF Input Voltage	16	V_{rf}	0.0005 to 10	mVrms
RF Input Frequency	16	f_{rf}	0.1 to 100	MHz
Oscillator Input Voltage	1	V_{local}	80 to 400	mVrms
Intermediate Frequency	–	f_{if}	455	kHz
Limiter Amp Input Voltage	5	V_{if}	0 to 400	mVrms
Filter Amp Input Voltage	10	V_{fa}	0.1 to 300	mVrms
Squelch Input Voltage	12	V_{sq}	0 or 2	Vdc
Mute Sink Current	14	I_{sq}	0.1 to 30	mA
Ambient Temperature Range	–	T_A	– 30 to + 70	°C

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC3371D	T_A = – 30° to +70°C	SO–16
MC3371P		Plastic DIP
MC3372D, AD		SO–16
MC3372P, AP		Plastic DIP

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 4.0 Vdc, f_o = 58.1125 MHz, df = ± 3.0 kHz, f_{mod} = 1.0 kHz, 50 Ω source, f_{local} = 57.6575 MHz, V_{local} = 0 dBm, T_A = 25°C, unless otherwise noted)

Characteristic	Pin	Symbol	Min	Typ	Max	Unit
Input for 12 dB SINAD Matched Input – (See Figures 10, 11 & 12) Unmatched Input – (See Figures 7A & 7B)	–	V_{SIN}	 – –	 1.0 5.0	 – 15	µVrms
Input for 20 dB NQS	–	V_{NQS}	–	3.5	–	µVrms
Recovered Audio Output Voltage V_{rf} = – 30 dBm	–	AF_O	 120	 200	 320	mVrms
Recovered Audio Drop Voltage Loss Vrf = – 30 dBm, V_{CC} = 4.0 V to 2.0 V	–	AF_{loss}	 – 8.0	 – 1.5	 –	dB
Meter Drive Output Voltage (No Modulation) V_{rf} = – 100 dBm V_{rf} = – 70 dBm V_{rf} = – 40 dBm	13	M_{Drv} MV1 MV2 MV3	 – 1.1 2.0	 0.3 1.5 2.5	 0.5 1.9 3.1	Vdc
Filter Amp Gain R_S = 600 Ω , f_S = 10 kHz, V_{fa} = 1.0 mVrms	–	$A_{V(Amp)}$	 47	 50	 –	dB
Mixer Conversion Gain V_{rf} = – 40 dBm, R_L = 1.8 kΩ	–	$A_{V(Mix)}$	 14	 20	 –	dB
Signal to Noise Ratio V_{rf} = – 30 dBm	–	s/n	 36	 67	 –	dB
Total Harmonic Distortion V_{rf} = – 30 dBm, BW = 400 Hz to 30 kHz	–	THD	 –	 0.6	 3.4	%
Detector Output Impedance	9	Z_O	–	450	–	Ω
Detector Output Voltage (No Modulation) V_{rf} = – 30 dBm	9	DV_O	 –	 1.45	 –	Vdc
Meter Drive V_{rf} = – 100 to – 40 dBm	13	M_O	 –	 0.8	 –	µA/dB
Meter Drive Dynamic Range RF_{In} IF_{In} (455 kHz)	13	MVD	 – –	 60 80	 – –	dB
Mixer Third Order Input Intercept Point f1 = 58.125 MHz f2 = 58.1375 MHz	–	ITO_{Mix}	 –	 – 22	 –	dBm
Mixer Input Resistance	16	R_{in}	–	3.3	–	kΩ
Mixer Input Capacitance	16	C_{in}	–	2.2	–	pF

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 4.0 Vdc, T_A = 25°C, unless otherwise noted)

Characteristic	Pin	Symbol	Min	Typ	Max	Unit
Drain Current (No Input Signal) Squelch Off, V_{sq} = 2.0 Vdc Squelch On, V_{sq} = 0 Vdc Squelch Off, V_{CC} = 2.0 to 9.0 V	4	 Icc1 Icc2 dIcc1	 – – –	 3.2 3.6 1.0	 4.2 4.8 2.0	mA
Detector Output (No Input Signal) DC Voltage, V8 = V_{CC}	9	V_9	 0.9	 1.6	 2.3	Vdc
Filter Output (No Input Signal) DC Voltage Voltage Change, V_{CC} = 2.0 to 9.0 V	11	 V_{11} dV_{11}	 1.5 2.0	 2.5 5.0	 3.5 8.0	Vdc
Trigger Hysteresis	–	Hys	34	57	80	mV

TYPICAL CURVES (UNMATCHED INPUT)

Figure 1. Total Harmonic Distortion versus Temeprature

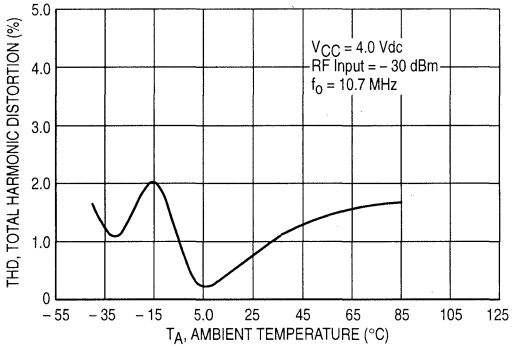


Figure 2. RSSI versus RF Input

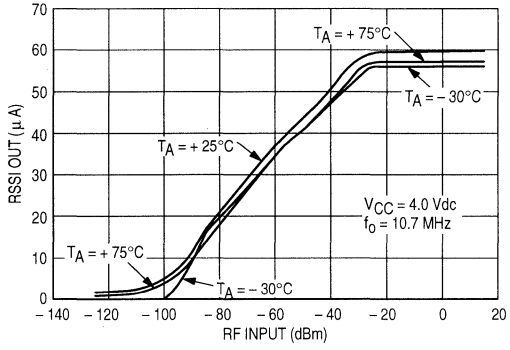


Figure 3. RSSI Output versus Temperature

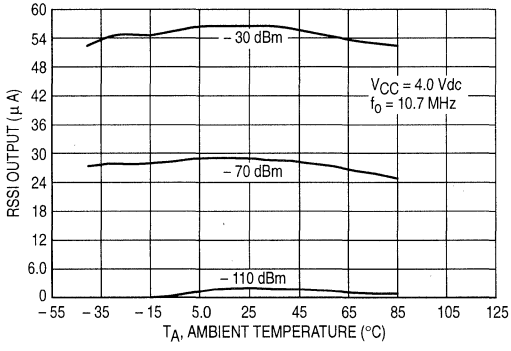


Figure 4. Mixer Output versus RF Input

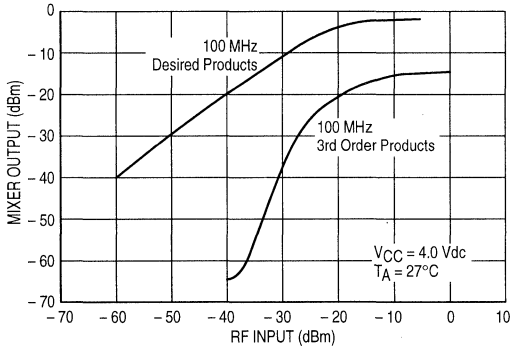


Figure 5. Mixer Gain versus Supply Voltage

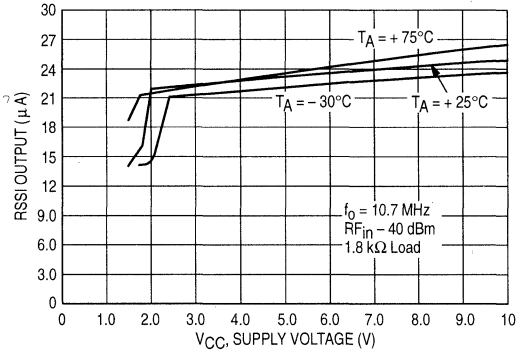


Figure 6. Mixer Gain versus Frequency

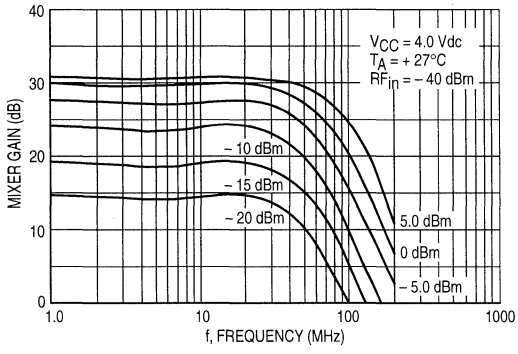


Figure 7A. MC3371 Functional Block Diagram and Test Fixture Schematic

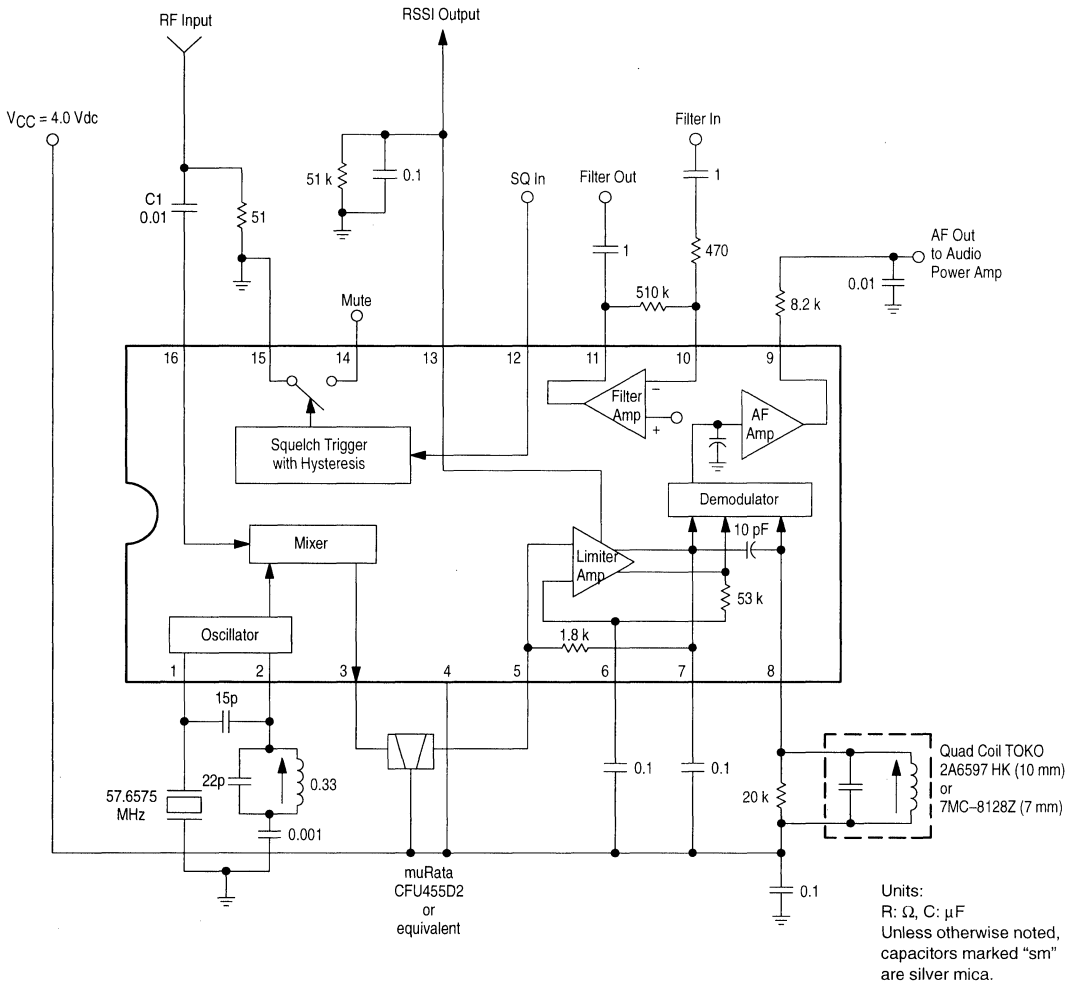
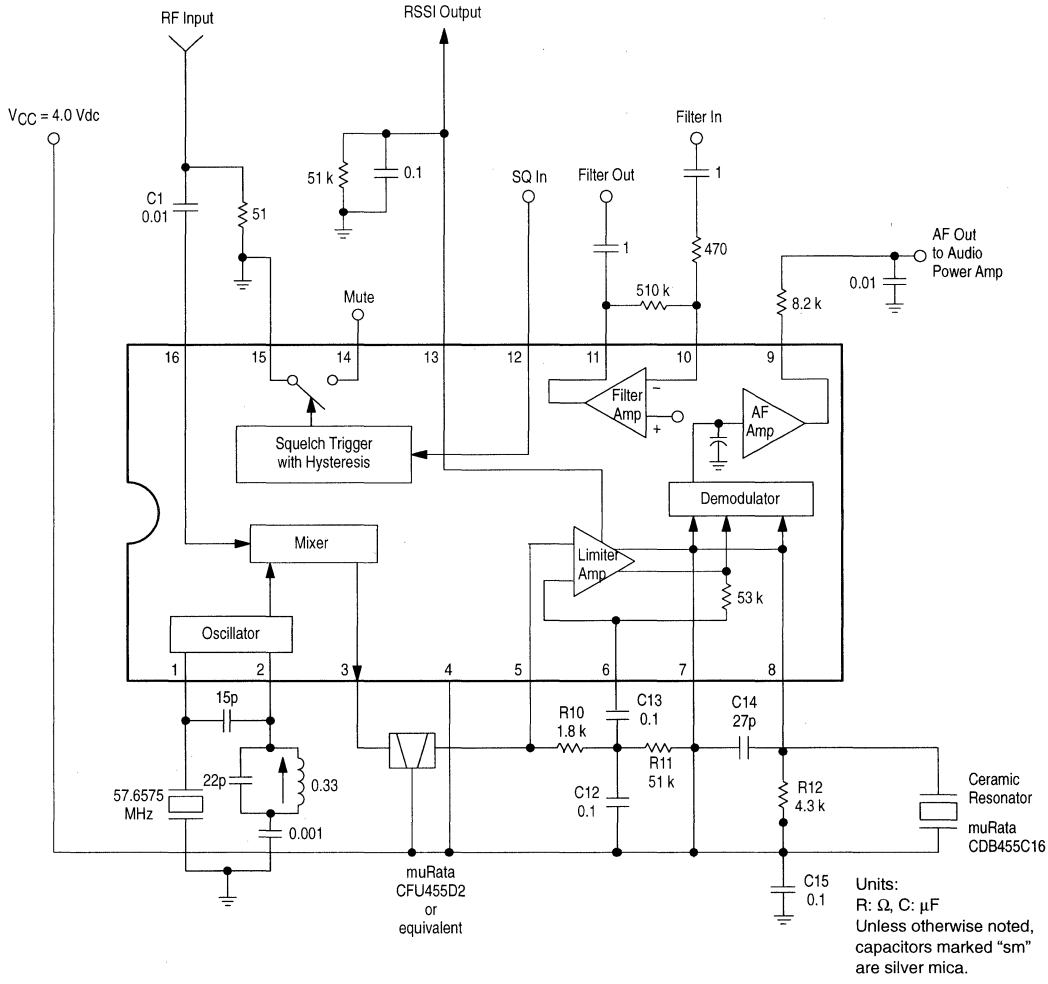
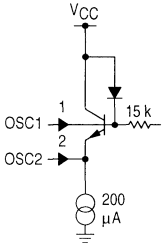
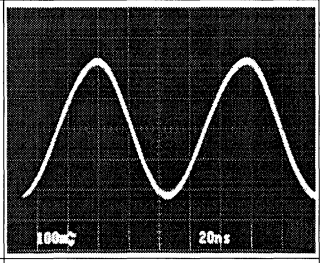
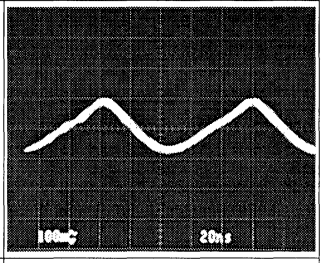
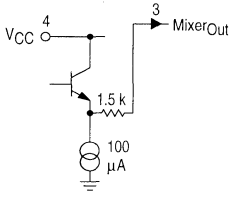
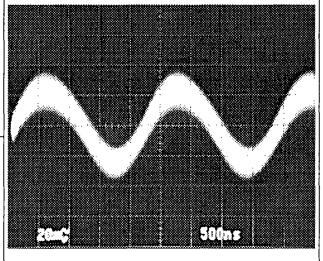
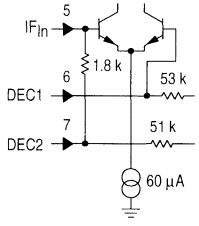
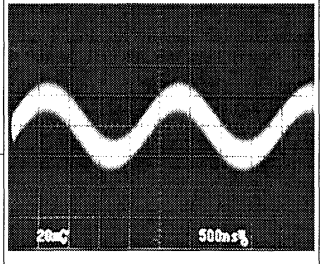


Figure 7B. MC3372 Functional Block Diagram and Test Fixture Schematic



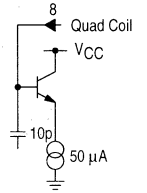
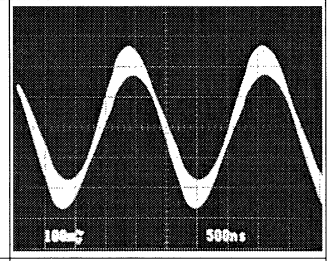
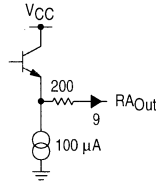
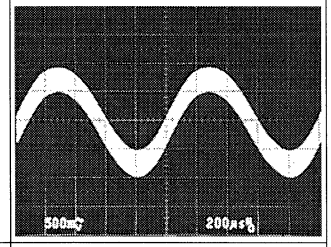
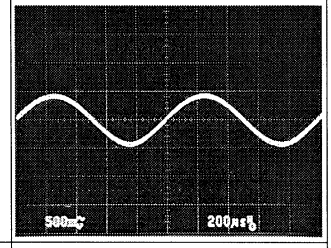
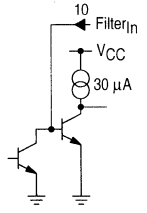
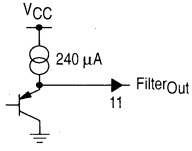
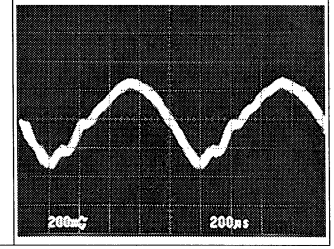
MC3371 PIN FUNCTION DESCRIPTION

OPERATING CONDITIONS V_{CC} = 4.0 Vdc, RF_{In} = 100 µV, f_{mod} = 1.0 kHz, f_{dev} = 3.0 kHz. MC3371 at f_{RF} = 10.7 MHz (see Figure 10).

Pin	Symbol	Internal Equivalent Circuit	Description	Waveform
1	OSC1		The base of the Colpitts oscillator. Use a high impedance and low capacitance probe or a "sniffer" to view the waveform without altering the frequency. Typical level is 450 mVp–p.	
2	OSC2		The emitter of the Colpitts oscillator. Typical signal level is 200 mVp–p. Note that the signal is somewhat distorted compared to that on pin 1.	
3	MX_{Out}		Output of the Mixer. Riding on the 455 kHz is the RF carrier component. The typical level is approximately 60 mVp–p.	
4	V_{CC}		Supply Voltage – 2.0 to 9.0 Vdc is the operating range. V_{CC} is decoupled to ground.	
5	IF_{In}		Input to the IF amplifier after passing through the 455 kHz ceramic filter. The signal is attenuated by the filter. The typical level is approximately 50 mVp–p.	
6 7	DEC1 DEC2		IF Decoupling. External 0.1 µF capacitors connected to V_{CC}.	

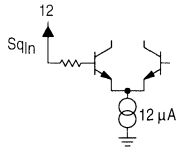
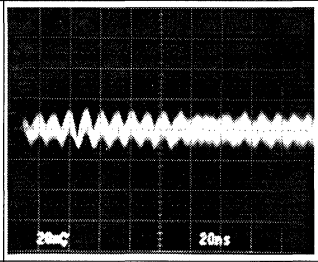
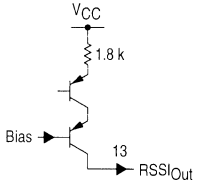
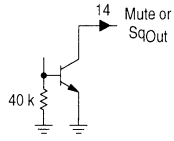
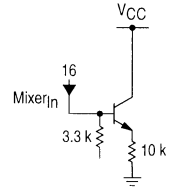
MC3371 PIN FUNCTION DESCRIPTION

OPERATING CONDITIONS V_{CC} = 4.0 Vdc, RF_{In} = 100 µV, f_{mod} = 1.0 kHz, f_{dev} = 3.0 kHz. MC3371 at f_{RF} = 10.7 MHz (see Figure 10).

Pin	Symbol	Internal Equivalent Circuit	Description	Waveform
8	Quad Coil		Quadrature Tuning Coil. Composite (not yet demodulated) 455 kHz IF signal is present. The typical level is 500 mVp–p.	
9	RA		Recovered Audio. This is a composite FM demodulated output having signal and carrier component. The typical level is 1.4 Vp–p.	
			The filtered recovered audio has the carrier component removed and is typically 800 mVp–p.	
10	Fil_{In}		Filter Amplifier Input	
11	Fil_{Out}		Filter Amplifier Output. The typical signal level is 400 mVp–p.	

MC3371 PIN FUNCTION DESCRIPTION

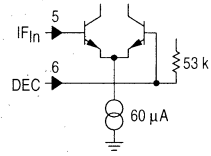
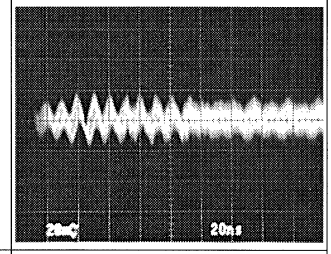
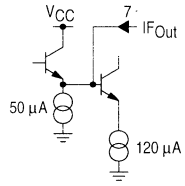
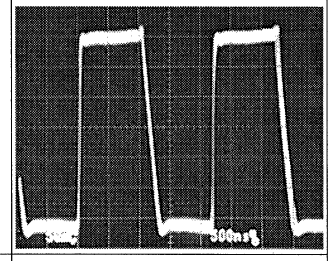
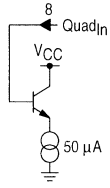
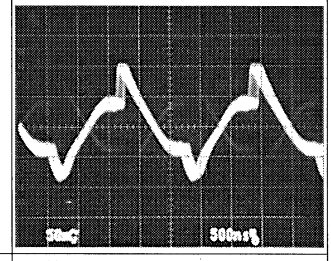
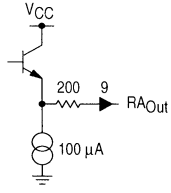
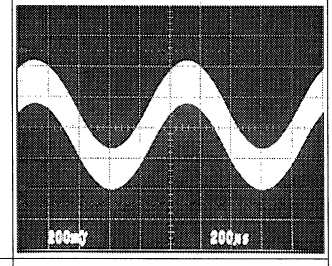
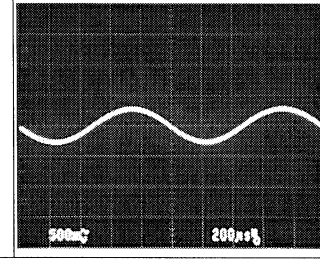
OPERATING CONDITIONS V_{CC} = 4.0 Vdc, RF_{In} = 100 µV, f_{mod} = 1.0 kHz, f_{dev} = 3.0 kHz. MC3371 at f_{RF} = 10.7 MHz (see Figure 10).

Pin	Symbol	Internal Equivalent Circuit	Description	Waveform
12	Sq_{In}		Squelch Input. See discussion in application text.	
13	RSSI		RSSI Output. Referred to as the Received Signal Strength Indicator or RSSI. The chip sources up to 60 µA over the linear 60 dB range. This pin may be used many ways. such as: AGC, meter drive and carrier triggered squelch circuit.	
14	MUTE		Mute Output. See discussion in application text.	
15	GND		Ground. The ground area should be continuous and unbroken. In a two–sided layout, the component side has the ground plane. In a one–sided layout, the ground plane fills around the traces on the circuit side of the board and is not interrupted.	
16	MIX_{In}		Mixer Input – Series Input Impedance: @ 10 MHz: 309 – j33 Ω @ 45 MHz: 200 – j13 Ω	

2

MC3372 PIN FUNCTION DESCRIPTION

OPERATING CONDITIONS V_{CC} = 4.0 Vdc, RF_{In} = 100 µV, f_{mod} = 1.0 kHz, f_{dev} = 3.0 kHz. MC3372 at f_{RF} = 45 MHz (see Figure 12).

Pin	Symbol	Internal Equivalent Circuit	Description	Waveform
5	IF_{In}		IF Amplifier Input	
6	DEC1		IF Decoupling. External 0.1 µF capacitors connected to V_{CC}.	
7	IF_{Out}		IF Amplifier Output Signal level is typically 300 mVp–p.	
8	$Quad_{In}$		Quadrature Detector Input. Signal level is typically 150 mVp–p.	
9	RA		Recovered Audio. This is a composite FM demodulated output having signal and carrier components. Typical level is 800 mVp–p.	
			The filtered recovered audio has the carrier signal removed and is typically 500 mVp–p.	

*Other pins are the same as pins in MC3371.

Figure 8. MC3371 Circuit Schematic

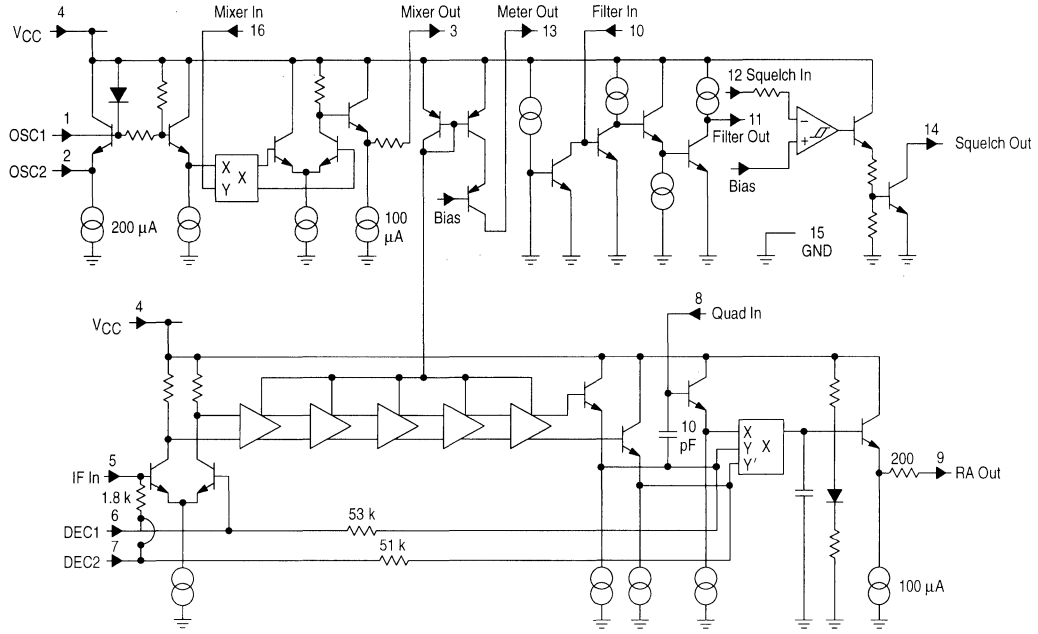
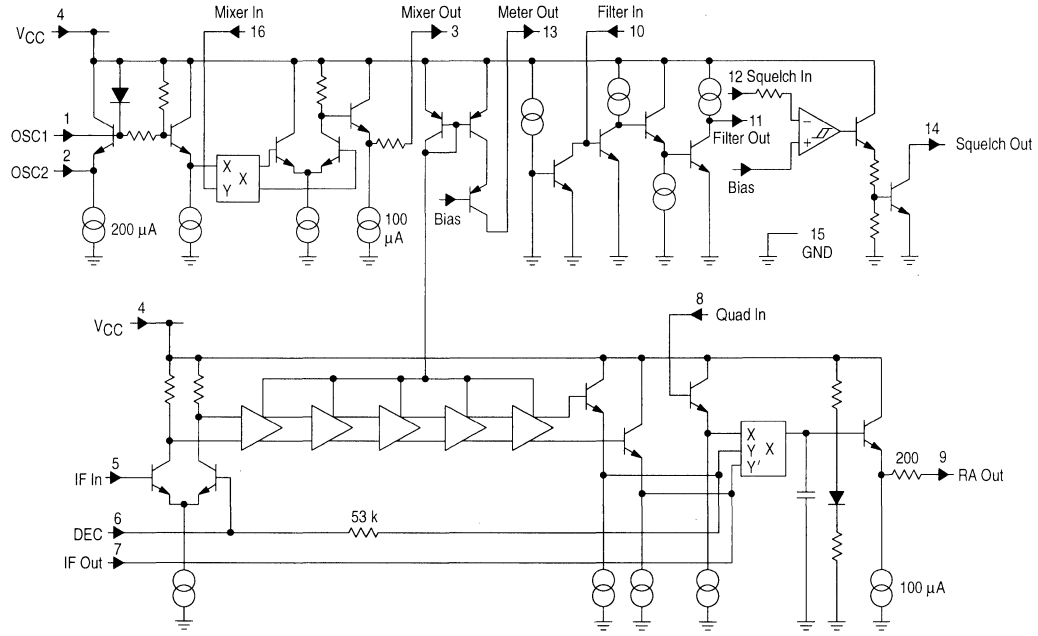


Figure 9. MC3372 Circuit Schematic



CIRCUIT DESCRIPTION

The MC3371 and MC3372 are low power narrowband FM receivers with an operating frequency of up to 60 MHz. Its low voltage design provides low power drain, excellent sensitivity, and good image rejection in narrowband voice and data link applications.

This part combines a mixer, an IF (intermediate frequency) limiter with a logarithmic response signal strength indicator, a quadrature detector, an active filter and a squelch trigger circuit. In a typical application, the mixer amplifier converts an RF input signal to a 455 kHz IF signal. Passing through an external bandpass filter, the IF signal is fed into a limiting amplifier and detection circuit where the audio signal is recovered. A conventional quadrature detector is used.

The absence of an input signal is indicated by the presence of noise above the desired audio frequencies. This "noise band" is monitored by an active filter and a detector. A squelch switch is used to mute the audio when noise or a tone is present. The input signal level is monitored by a meter drive circuit which detects the amount of IF signal in the limiting amplifier.

APPLICATIONS INFORMATION

The oscillator is an internally biased Colpitts type with the collector, base, and emitter connections at Pins 4, 1 and 2 respectively. This oscillator can be run under crystal control. For fundamental mode crystals use crystal characterized parallel resonant for 32 pF load. For higher frequencies, use 3rd overtone series mode type crystals. The coil (L2) and resistor RD (R13) are needed to ensure proper and stable operation at the LO frequency (see Figure 12, 45 MHz application circuit).

The mixer is doubly balanced to reduce spurious radiation. Conversion gain stated in the AC Electrical Characteristics table is typically 20 dB. This power gain measurement was made under stable conditions using a 50 Ω source at the input and an external load provided by a 455 kHz ceramic filter at the mixer output which is connected to the V_{CC} (Pin 4) and IF input (Pin 5). The filter impedance closely matches the 1.8 kΩ internal load resistance at Pin 3 (mixer output). Since the input impedance at Pin 16 is strongly influenced by a 3.3 kΩ internal biasing resistor and has a low capacitance, the useful gain is actually much higher than shown by the standard power gain measurement. The Smith Chart plot in Figure 16 shows the measured mixer input impedance versus input frequency with the mixer input matched to a 50 Ω source impedance at the given frequencies. In order to assure stable operation under matched conditions, it is necessary to provide a shunt resistor to ground. Figures 10, 11 and 12 show the input networks used to derive the mixer input impedance data.

Following the mixer, a ceramic bandpass filter is recommended for IF filtering (i.e. 455 kHz types having a bandwidth of ± 2.0 kHz to ± 15 kHz with an input and output impedance from 1.5 kΩ to 2.0 kΩ). The 6 stage limiting IF amplifier has approximately 92 dB of gain. The MC3371 and MC3372 are different in the limiter and quadrature detector circuits. The MC3371 has a 1.8 kΩ and a 51 kΩ resistor providing internal DC biasing and the output of the limiter is internally connected, both directly and through a 10 pF capacitor to the quadrature detector; whereas, in the MC3372 these components are not provided internally. Thus, in the MC3371, no external components are necessary to match the 455 kHz ceramic filter, while in the MC3372, external 1.8 kΩ and 51 kΩ biasing resistors are needed between Pins 5 and 7, respectively (see Figures 11 and 12).

In the MC3371, a parallel LCR quadrature tank circuit is connected externally from Pin 8 to V_{CC} (similar to the MC3361). In the MC3372, a quadrature capacitor is needed externally from Pin 7 to Pin 8 and a parallel LC or a ceramic discriminator with a damping resistor is also needed from Pin 8 to V_{CC} (similar to the MC3357). The above external quadrature circuitry provides 90° phase shift at the IF center frequency and enables recovered audio.

The damping resistor determines the peak separation of the detector and is somewhat critical. As the resistor is decreased, the separation and the bandwidth is increased but the recovered audio is decreased. Receiver sensitivity is dependent on the value of this resistor and the bandwidth of the 455 kHz ceramic filter.

On the chip the composite recovered audio, consisting of carrier component and modulating signal, is passed through a low pass filter amplifier to reduce the carrier component and then is fed to Pin 9 which has an output impedance of 450 Ω. The signal still requires further filtering to eliminate the carrier component, deemphasis, volume control, and further amplification before driving a loudspeaker. The relative level of the composite recovered audio signal at Pin 9 should be considered for proper interaction with an audio post amplifier and a given load element. The MC13060 is recommended as a low power audio amplifier.

The meter output indicates the strength of the IF level and the output current is proportional to the logarithm of the IF input signal amplitude. A maximum source current of 60 μA is available and can be used to drive a meter and to detect a carrier presence. This is referred to as a Received Strength Signal Indicator (RSSI). The output at Pin 13 provides a current source. Thus, a resistor to ground yields a voltage proportional to the input carrier signal level. The value of this resistor is estimated by (V_{CC}(Vdc) – 1.0 V)/60 μA; so for V_{CC} = 4.0 Vdc, the resistor is approximately 50 kΩ and provides a maximum voltage swing of about 3.0 V.

A simple inverting op amp has an output at Pin 11 and the inverting input at Pin 10. The noninverting input is connected to 2.5 V. The op amp may be used as a noise triggered squelch or as an active noise filter. The bandpass filter is designed with external impedance elements to discriminate between frequencies. With an external AM detector, the filtered audio signal is checked for a tone signal or for the presence of noise above the normal audio band. This information is applied to Pin 12.

An external positive bias to Pin 12 sets up the squelch trigger circuit such that the audio mute (Pin 14) is open or connected to ground. If Pin 12 is pulled down to 0.9 V or below by the noise or tone detector, Pin 14 is internally shorted to ground. There is about 57 mV of hyteresis at Pin 12 to prevent jitter. Audio muting is accomplished by connecting Pin 14 to the appropriate point in the audio path between Pin 9 and an audio amplifier. The voltage at Pin 14 should not be lower than – 0.7 V; this can be assured by connecting Pin 14 to the point that has no DC component.

Another possible application of the squelch switch may be as a carrier level triggered squelch circuit, similar to the MC3362/MC3363 FM receivers. In this case the meter output can be used directly to trigger the squelch switch when the RF input at the input frequency falls below the desired level. The level at which this occurs is determined by the resistor placed between the meter drive output (Pin 13) and ground (Pin 15).

Figure 10. Typical Application for MC3371 at 10.7 MHz

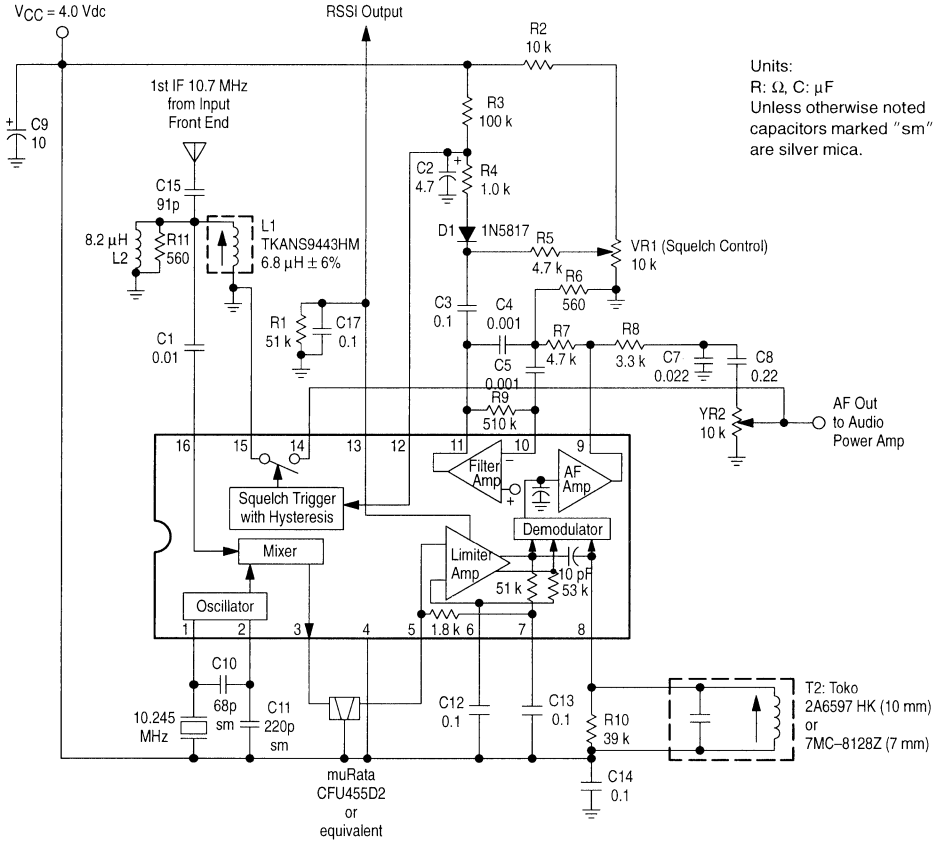


Figure 11. Typical Application for MC3372 at 10.7 MHz

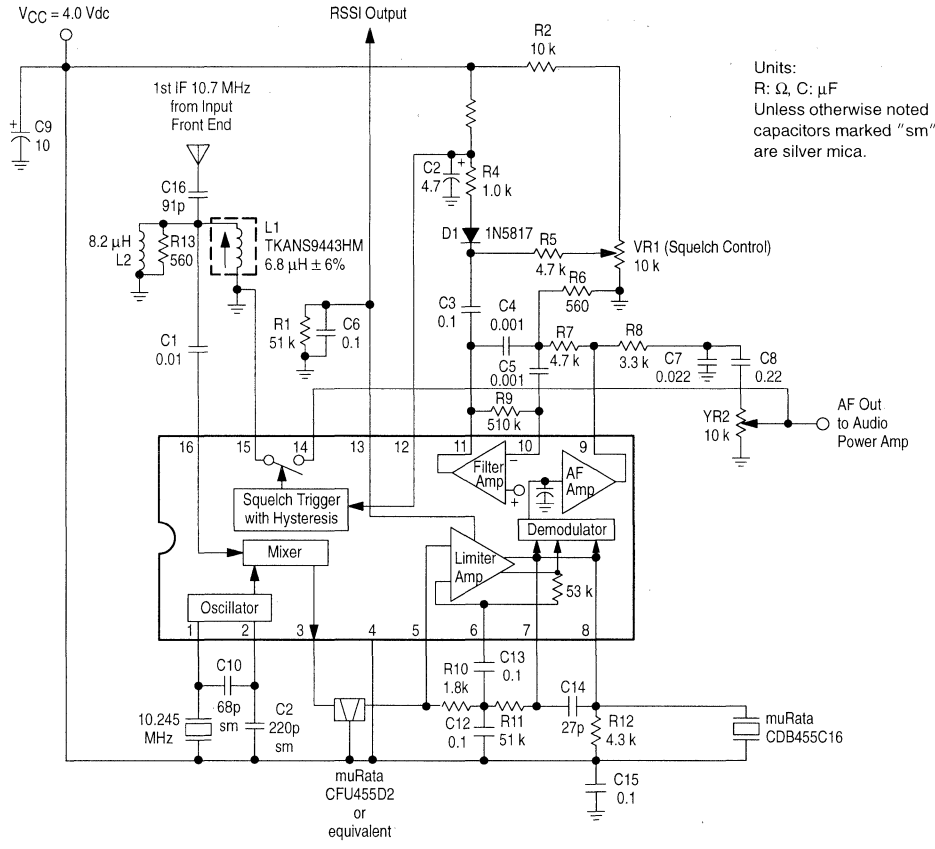


Figure 12. Typical Application for MC3372 at 45 MHz

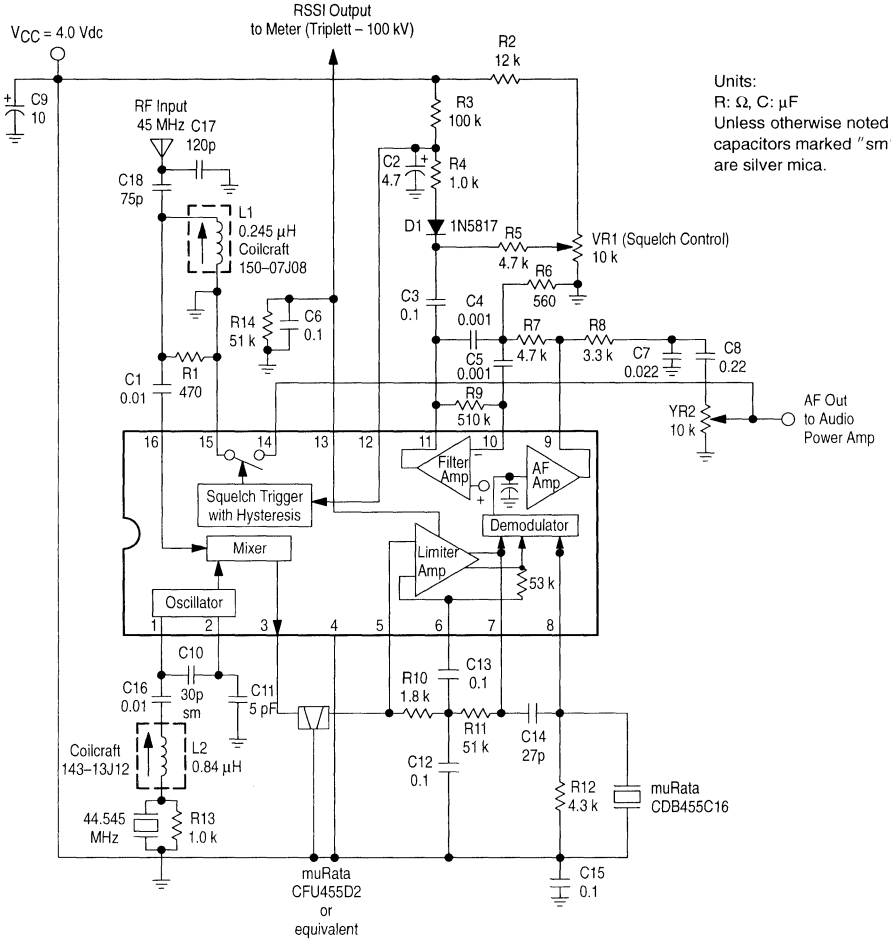


Figure 13. RSSI Output versus RF Input

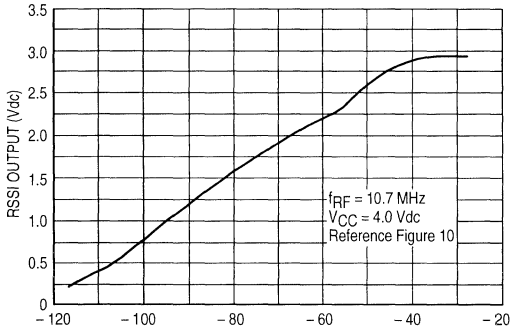


Figure 14. RSSI Output versus RF Input

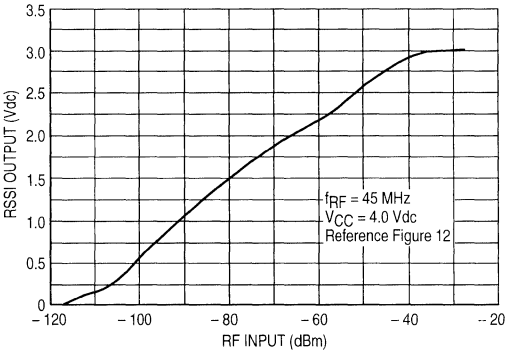
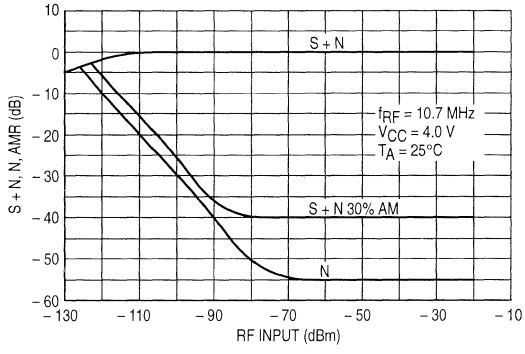


Figure 15. S + N, N, AMR versus Input



* REFERENCE FIGURES 10, 11 & 12

Figure 16. Mixer Input Impedance versus Frequency

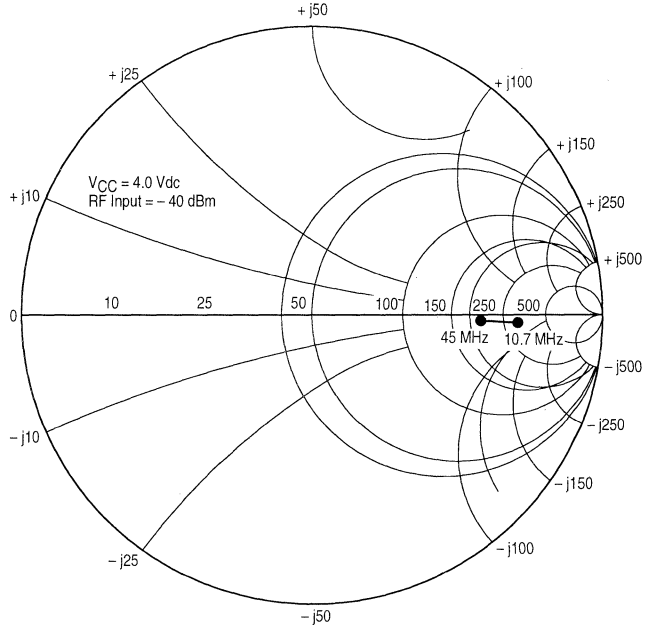


Figure 17. MC3371 PC Board Component View with Matched Input at 10.7 MHz

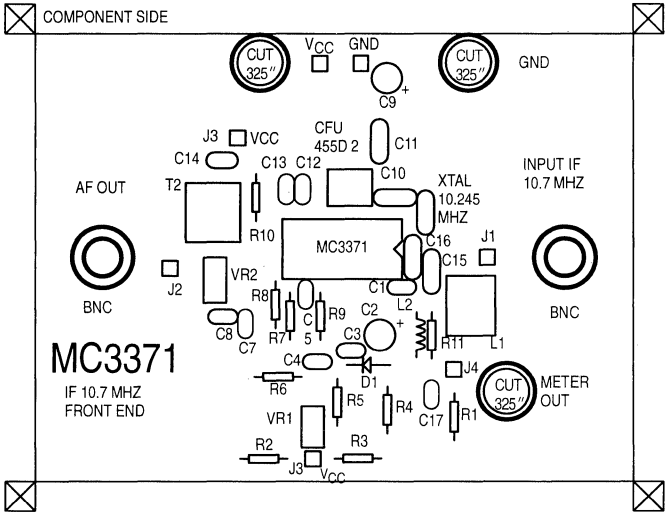
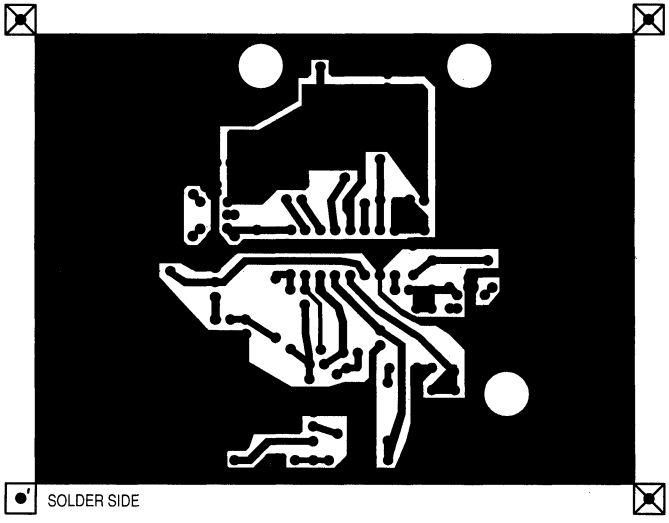


Figure 18. MC3371 PC Board Circuit or Solder Side as Viewed thru Component Side



Above PC Board is laid out for the circuit in Figure 10.

Figure 19. MC3372P PC Board Component View with Matched Input at 10.7 MHz

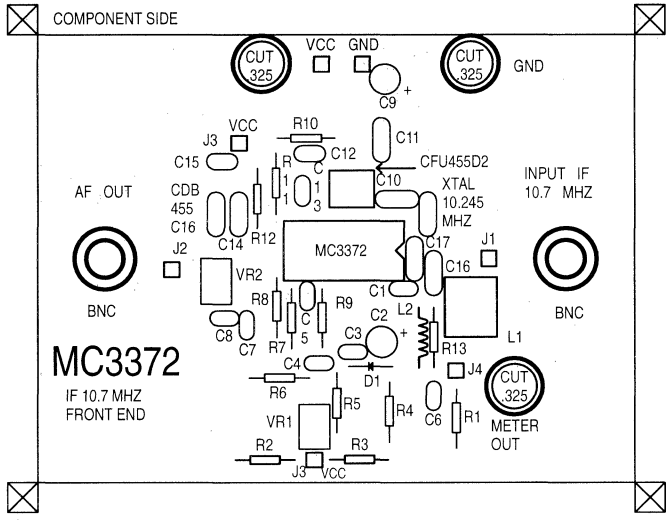
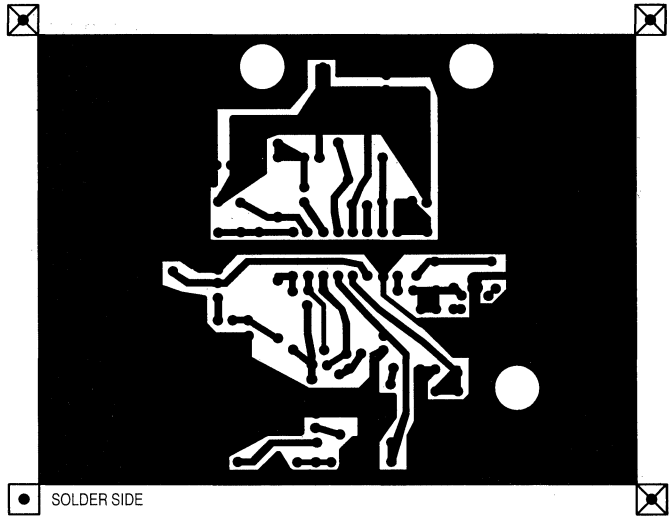


Figure 20. MC3372P PC Board Circuit or Solder Side as Viewed thru Component Side



Above PC Board is laid out for the circuit in Figure 11.

MOTOROLA

MC3374

Advance Information

Low Voltage FM Narrowband Receiver

. . . with single conversion circuitry including oscillator, mixer, IF amplifiers, limiting IF circuitry, and quadrature discriminator. The MC3374 is perfect for narrowband audio and data applications up to 75 MHz which require extremely low power consumption. Battery powered applications down to V_{CC} = 1.1 V are possible. The MC3374 also includes an on–board voltage regulator, low battery detection circuitry, a receiver enable allowing a power down SLEEPMODE™, two undedicated buffer amplifiers to allow simultaneous audio and data reception, and a comparator for enhancing FSK (Frequency Shift Keyed) data reception to 1200 baud.

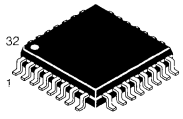
- Low Supply Voltage: V_{CC} = 1.1 to 3.0 Vdc
- Low Power Consumption: P_D = 1.5 to 5.0 mW
- Input Bandwidth 75 MHz
- Excellent Sensitivity: 0.5 μVrms for 12 dB SINAD
- Voltage Regulator Available (Source Capability 3.0 mA)
- Receiver Enable to Allow Active/Standby Operation
- Low Battery Detection Circuitry
- Self Biasing Audio Buffer
- Data Buffer
- FSK Data Shaping Comparator
- Standard 32–Lead QFP Surface Mount Package

SLEEPMODE is a trademark of Motorola, Inc.

LOW VOLTAGE SINGLE CONVERSION FM RECEIVER

SEMICONDUCTOR TECHNICAL DATA

2

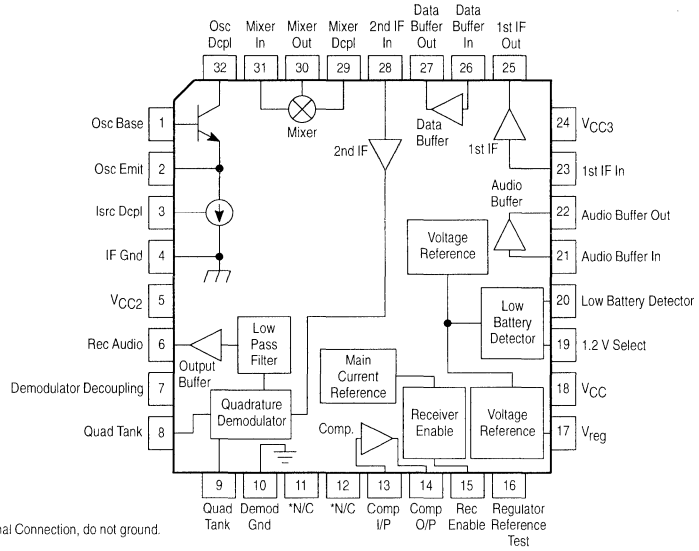


FTB SUFFIX
PLASTIC PACKAGE
CASE 873
(Thin QFP)

ORDERING INFORMATION

Device	Tested Operating Temperature Range	Package
MC3374FTB	T_A = –10° to +70°C	TQFP–32

Simplified Block Diagram



*Internal Connection, do not ground.

This device contains 87 active transistors

MAXIMUM RATINGS (Voltage with respect to Pins 4 and 10; T_A = 25°C.)

Rating	Pin	Value	Unit
Supply Voltage	18	5.0	Vdc
RF Input Signal	31	1.0	Vrms
Audio Buffer Input	21	1.0	Vrms
Data Buffer Input	26	1.0	Vrms
Comparator Input	13	1.0	Vrms
Junction Temperature	–	150	°C
Storage Temperature	–	−65 to +150	°C

Device should not be operated at or outside these values. The "Recommended Operating Limits" provide for actual device operation.

RECOMMENDED OPERATING CONDITIONS

Parameter	Pin	Value	Unit
Supply Voltage	18	1.1 to 3.0	Vdc
Receiver Enable Voltage	15	V_{CC}	Vdc
1.2 V Select Voltage	19	Open or V_{CC}	Vdc
RF Input Signal Level	31	0.001 to 100	mVrms
RF Input Frequency	31	0 to 75	MHz
Intermediate Frequency (IF)	–	455	kHz
Audio Buffer Input	21	0 to 75	mVrms
Data Buffer Input	26	0 to 75	mVrms
Comparator Input	13	10 to 300	mVrms
Ambient Temperature	–	−10 to 70	°C

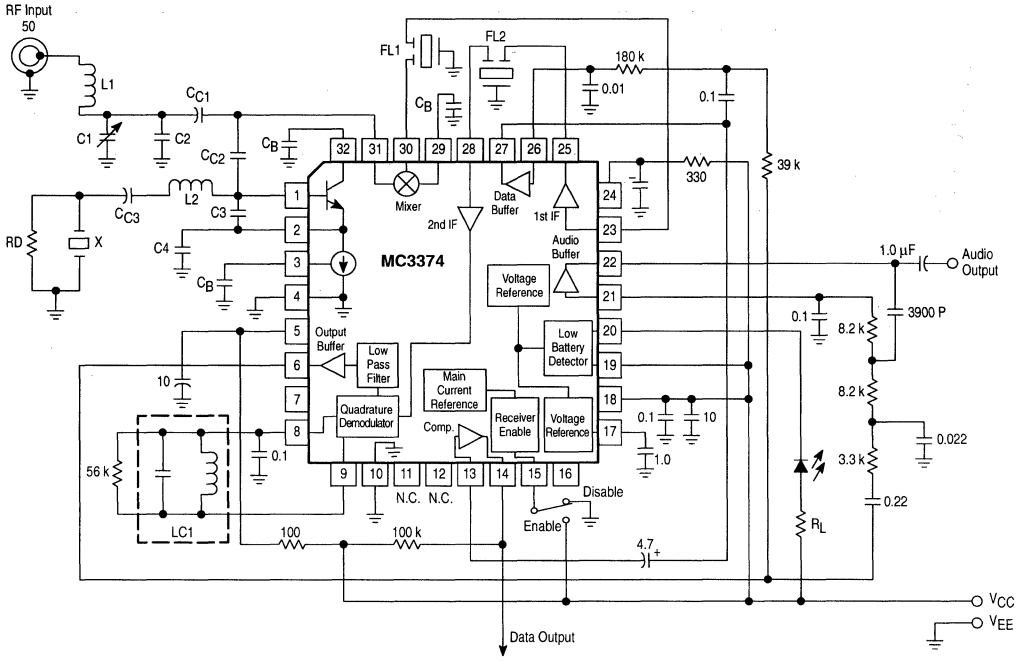
ELECTRICAL CHARACTERISTICS (V_{CC} = 1.3 V, f_o = 10.7 MHz, f_{mod} = 1.0 kHz, Deviation = 3.0 kHz, T_A = 25°C, Test Circuit of Figure 1, unless otherwise noted.)

Characteristic	Pin	Min	Typ	Max	Unit
OVERALL MC3374 PERFORMANCE					
Drain Current – Pin 15 = V_{CC} (Enabled) – Pin 15 = 0 Vdc (Disabled)	5 + 18 + 24 5 + 18 + 24	– –	1.6 0.5	3.0 –	mA μA
Recovered Audio (RF Input = 10 μV)	6	13	18	30	mVrms
Noise Output (RF Input = 0 mV, 300 Hz–5.0 kHz)	6	–	1.0	–	mVrms
Input for –3.0 dB Limiting	31	–	0.6	–	μVrms
MIXER					
Mixer Input Resistance (Rp)	31	–	1.5	–	kΩ
Mixer Input Capacitance (Cp)	31	–	9.0	–	pF
FIRST IF AMPLIFIER					
First IF Amp Voltage Gain	–	–	27	–	dB
AUDIO BUFFER					
Voltage Gain	–	3.0	4.0	4.7	V/V
Input Resistance	21	–	110	–	kΩ
Maximum Input for Undistorted Output (<5% THD)	21	–	64	–	mVrms
Maximum Output Swing (<5% THD)	22	–	690	–	mV_{pp}
Output Resistance	22	–	780	–	Ω
DATA BUFFER					
Voltage Gain	–	1.4	2.7	4.3	V/V
Input Resistance	26	–	9.8	–	MΩ
Maximum Input for Undistorted Output (<5% THD)	26	–	100	–	mVrms
Maximum Output Swing (<5% THD)	27	–	800	–	mV_{pp}
Output Resistance	27	–	690	–	Ω

ELECTRICAL CHARACTERISTICS (continued) (V_{CC} = 1.3 V, f_o = 10.7 MHz, f_{mod} = 1.0 kHz, Deviation = 3.0 kHz, T_A = 25°C, Test Circuit of Figure 1, unless otherwise noted.)

Characteristic	Pin	Min	Typ	Max	Unit
COMPARATOR					
Minimum Input for Triggering (R_L = 100 kΩ)	13	–	7.0	–	mVrms
Maximum Input Frequency (R_L = 100 kΩ)	13	–	25	–	kHz
Rise Time (10–90%; R_L = 100 kΩ)	14	–	5.0	–	µs
Fall Time (90–10%; R_L = 100 kΩ)	14	–	0.4	–	µs
LOW BATTERY DETECTOR					
Low Battery Trip Point	19	–	1.2	–	Vdc
Low Battery Output – V_{CC} = 0.9 V – V_{CC} = 1.3 V	20 20	– –	0.2 V_{CC}	– –	Vdc
VOLTAGE REGULATOR					
Regulated Output (see Figure 4)	17	0.95	1.07	1.15	Vdc
Source Capability	17	–	–	3.0	mA

Figure 1. MC3374 Pager IF Application Circuit



NOTES:

1. FL1 and FL2 are 455 kHz ceramic bandpass filters, which should have input and output impedances of 1.5 kΩ to 2.0 kΩ. Suggested part numbers are MuRata CFU455X or CFW455x – the 'X' suffix denotes bandwidth.
2. LC1 is a 455 kHz LC resonator. Recommended part numbers are Toko America RMC2A6597HM or 5SVLC–0637BGT (smaller). The evaluation board layout shown provides for use of either resonator. Ceramic discriminator elements cannot be used with the MC3374 due to their low input impedance. The damping resistor value can be raised to increase the recovered audio or lowered to increase the quadrature detector's bandwidth and linearity – practical limits are approximately 27 kΩ to 75 kΩ. Typically the quadrature detector's bandwidth should match the low IF filter's bandwidth.
3. The data buffer is set up as a low–pass filter with a corner frequency of approximately 200 Hz. The audio buffer is a bandpass filter with corner frequencies of 300 Hz and 3.0 kHz. The audio amplifier provides bass suppression.
4. C_{C1} and C_{C3} are RF coupling capacitors and should have ≤ 20 Ω impedance at the desired input and oscillator frequencies.
5. C_{C2} provides "light coupling" of the oscillator signal into the mixer, and should have a 3.0 kΩ to 5.0 kΩ impedance at the desired local oscillator frequency.
6. Capacitors labelled C_B are bypass capacitors and should have 20 Ω impedance at the desired RF and local oscillator frequencies.
7. The network of L1, C1 and C2 provides impedance matching of the mixer input (nominally 3.0 kΩ shunted by 9.0 pF) to 50 Ω at the desired RF/IF input frequency. This will allow for bench testing of the receiver from typical RF signal generators or radio service monitors, but additional or different matching will be required to maximize receiver sensitivity when used in conjunction with an antenna, RF preamplifier or mixer.

In. Freq.	L1	L2	C1	C2	C3	C4	C_{C1}/C_{C3}	C_{C2}	C_B	RD
10.7 MHz	6.8 µH	Short	2–82 pF	10 pF	120 pF	50 pF	1.0 nF	5.0 pF	0.1 µF	Open
45 MHz	0.68 µH	1.2 µH	5–25 pF	Open	30 pF	5.0 pF	1.0 nF	1.0 pF	1.0 nF	1.0 k
72 MHz	0.22 µH	0.22 µH	5–25 pF	Open	18 pF	3.0 pF	470 pF	1.0 pF	470 pF	1.0 k

Figure 2. Recovered Audio versus Supply

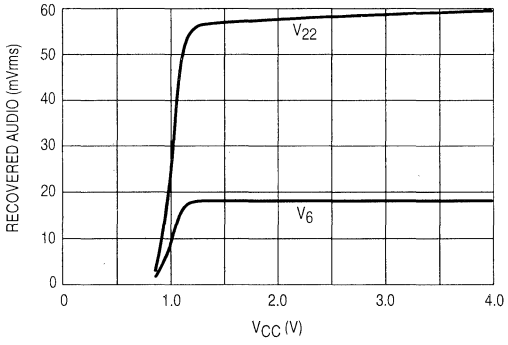


Figure 3. S+N, N versus Input

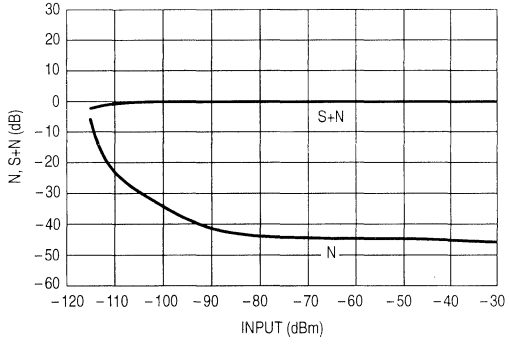


Figure 4. V_{REG} versus Supply

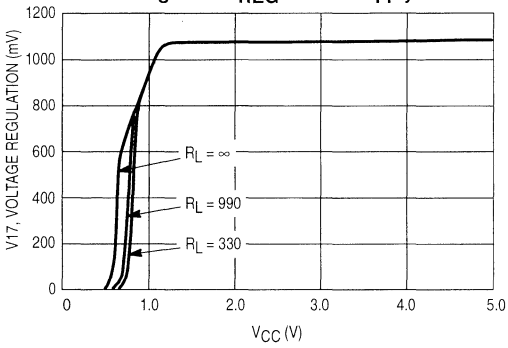


Figure 5. Regulated Output and Recovered Audio versus Temperature

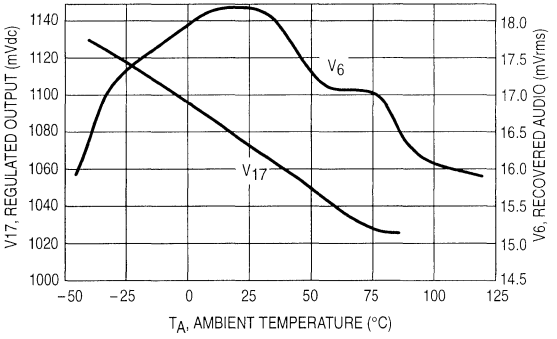
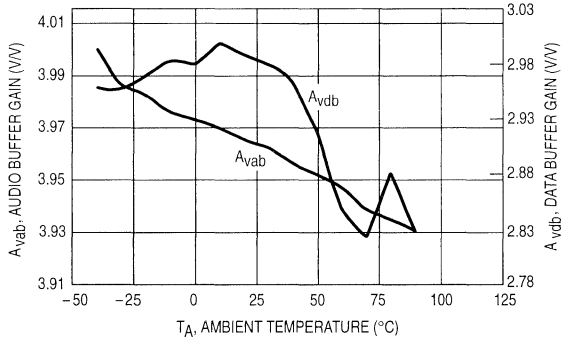


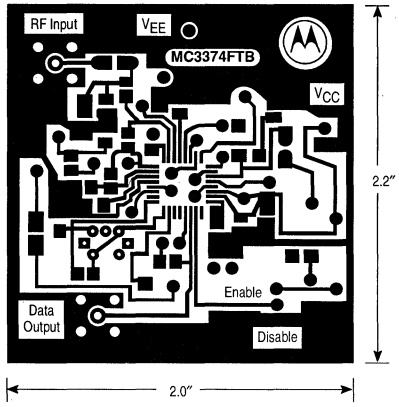
Figure 6. Buffer Amplifier Gains versus Temperature



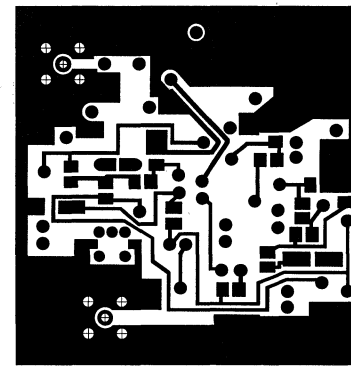
2

Figure 7. MC3374 Pager Receiver PCB Artwork

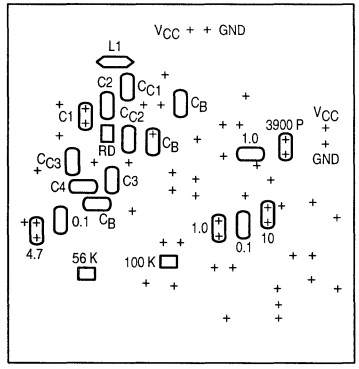
COPPER 1 LAYER
(Actual View of Surface Mount Side)



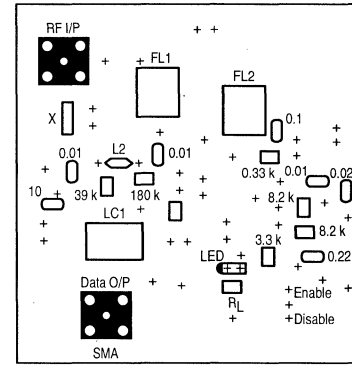
COPPER 2 LAYER
(Caution: Reversed View of Through–Hole Side)



COMPONENT 1 LAYER



COMPONENT 2 LAYER



NOTE: + = Through Hole

CIRCUIT DESCRIPTION

The MC3374 is an FM narrowband receiver capable of operation to 75 MHz. The low voltage design yields low power drain and excellent sensitivity in narrowband voice and data link applications. In the typical application the mixer amplifies the incoming RF or IF signal and converts this frequency to 455 kHz. The signal is then filtered by a 455 kHz ceramic filter and applied to the first intermediate frequency (IF) amplifier input, before passing through a second ceramic filter. The modulated IF signal is then applied to the limiting IF amplifier and detector circuitry. Modulation is recovered by a conventional quadrature detector. The typical modulation bandwidth available is 3.0 to 5.0 kHz.

Features available include buffers for audio/data amplification and active filtering, on board voltage regulator, low battery detection circuitry with programmable level, and receiver disable circuitry. The MC3374 is an FM utility receiver to be used for voice and/or narrowband data reception. It is especially suitable where extremely low power consumption and high design flexibility are required.

APPLICATION

The MC3374 can be used as a high performance FM IF for the use in low power dual conversion receivers. Because of the MC3374's extremely good sensitivity (0.6 μV for 20 dB (S+N/N, see Figure 3)), it can also be used as a stand alone single conversion narrowband receiver to 75 MHz for applications not sensitive to image frequency interference. An RF preamplifier will likely be needed to overcome preselector losses.

The oscillator is a Colpitts type which must be run under crystal control. For fundamental mode crystals choose resonators, parallel resonant, for a 32 pF load. For higher frequencies, use a 3rd overtone series mode type. The coil L2 and RD resistor are needed to ensure proper operation.

The best adjacent channel and sensitivity response occur when two 455 kHz ceramic filters are used, as shown in Figure 1. Either can be replaced by a 0.1 μF coupling capacitor to reduce cost, but some degradation in sensitivity and/or stability is suspected.

The detector is a quadrature type, with the connection from the limiter output to the detector input provided internally. A 455 kHz LC tank circuit must be provided externally. One of the tank pins (Pin 8) must be decoupled using a 0.1 μF capacitor. The 56 kΩ damping resistor (see Figure 1), determines the peak separation of the detector (and thus its bandwidth). Smaller values will increase the separation and bandwidth but decrease recovered audio and sensitivity.

The data buffer is a noninverting amplifier with a nominal voltage gain of 2.7 V/V. This buffer needs its dc bias (approximately 250 mV) provided externally or else debiasing will occur. A 2nd order Sallen–Key low pass filter, as shown in Figure 1, connecting the recovered audio output to the data buffer input provides the necessary dc bias and some post detection filtering. The buffer can also be used as an active filter.

The audio buffer is a noninverting amplifier with a nominal voltage gain of 4.0 V/V. This buffer is self–biasing so its input should be ac coupled. The two buffers, when applied as active filters, can be used together to allow simultaneous audio and very low speed data reception. Another possible configuration is to receive audio only and include a noise–triggered squelch.

The comparator is a noninverting type with an open collector output. Typically, the pull–up resistor used between Pin 14 and V_{CC} is 100 kΩ. With R_L = 100 kΩ the comparator is capable of operation up to 25 kHz. The circuit is self–biasing, so its input should be ac coupled.

The regulator is a 1.07 V reference capable of sourcing 3.0 mA. This pin (Pin 17) needs to be decoupled using a 1.0–10 μF capacitor to maintain stability of the MC3374.

All three V_{CC}s on the MC3374 (V_{CC}, V_{CC2}, V_{CC3}) run on the same supply voltage. V_{CC} is typically decoupled using capacitors only. V_{CC2} and V_{CC3} should be bypassed using the RC bypasses shown in Figure 1. Eliminating the resistors on the V_{CC2} and V_{CC3} bypasses may be possible in some applications, but a reduction in sensitivity and quieting will likely occur.

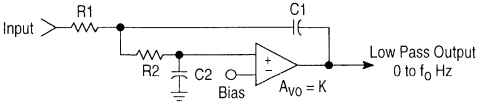
The low battery detection circuit gives an NPN open collector output at Pin 20 which drops low when the MC3374 supply voltage drops below 1.2 V. Typically it would be pulled up via a 100 kΩ resistor to supply.

The 1.2 V Select pin, when connected to the MC3374 supply, programs the low battery detector to trip at V_{CC} < 1.1 V. Leaving this pin open raises the trip voltage on the low battery detector.

Pin 15 is a receiver enable which is connected to V_{CC} for normal operation. Connecting this pin to ground shuts off receiver and reduces current drain to I_{CC} < 0.5 μA.

APPENDIX

Design of 2nd Order Sallen–Key Low Pass Filters



The audio and data buffers can easily be configured as active low pass filters using the circuit configuration shown above. The circuit has a center frequency (f_o) and quality factor (Q) given by the following:

$$f_o = \frac{1}{2\pi\sqrt{R1R2C1C2}}$$

$$Q = \frac{1}{\sqrt{\frac{R2C2}{R1C1}} + \sqrt{\frac{R1C2}{R2C1}} + (1-K)\sqrt{\frac{R1C1}{R2C2}}}$$

If possible, let R1 = R2 or C1 = C2 to simplify the above equations. Be sure to avoid a negative Q value to prevent instability. Setting $Q = 1/\sqrt{2} = 0.707$ yields a maximally flat filter response.

Data Buffer Design

The data buffer is designed as follows:

f_o = 200 Hz
C1 = C2 = 0.01 μF
Q = 0.707 (target)

K = 2.7 (data buffer open loop voltage gain)

Setting C1 = C2 yields:

$$fo = \frac{1}{2\pi C1\sqrt{R1R2}}$$

$$Q = \frac{1}{\sqrt{\frac{R2}{R1}} + (2-K)\sqrt{\frac{R1}{R2}}}$$

Iteration yields R2 = 4.2 (R1) to make Q = 0.707.
Substitution into the equation for f_o yields:
R1 = 38 kΩ (use 39 kΩ)
R2 = 4.2(R1) = 180 kΩ
C1 = C2 = 0.01 μF

Audio Buffer Design

The audio buffer is designed as follows:

f_o = 3000 Hz
R1 = R2 = 8.2 kΩ
Q = 0.707 (target)

K = 3.9 (audio buffer open loop voltage gain)

Setting C1 = C2 yields:

$$fo = \frac{1}{2\pi R1\sqrt{C1C2}}$$

$$Q = \frac{1}{\sqrt{\frac{C2}{C1}} + (1-K)\sqrt{\frac{C1}{C2}}}$$

Iteration yields C2 = 2.65 (C1) to make Q = 0.707.
Substitution into the equation for f_o yields:
C1 = 3900 pF
C2 = 2.65(C1) = 0.01 μF
R1 = R2 = 8.2 kΩ

MC34C86

Product Preview

Quad EIA-422-A Line Receiver

CMOS

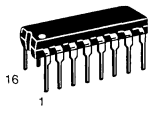
The MC34C86 is a quad differential line receiver designed for digital data transmission over balanced lines. The MC34C86 meets all the requirements of standard EIA–422–A while retaining the low–power characteristics of CMOS.

The MC34C86 has an input sensitivity of 200 mV over the common mode input voltage range of ± 7 V. In addition, each receiver chain has internal hysteresis circuitry to improve noise margin and discourage output instability for slowly changing input waveforms.

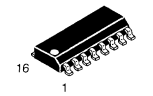
The MC34C86 is pin compatible with the MC3486.

All pins are protected against damage due to electrostatic discharges.

- Typical Power Supply Current: 6 mA
- 2000 V ESD Protection on the Inputs and Outputs
- Typical Propagation Delay: 18 ns
- Typical Input Hysteresis: 75 mV
- Meets the Requirements of Standard EIA–422–A
- Operation from Single 5 V Supply
- High Impedance Mode for Outputs Connected to System Buses
- TTL/CMOS Compatible Outputs



P SUFFIX
PLASTIC DIP
CASE 648



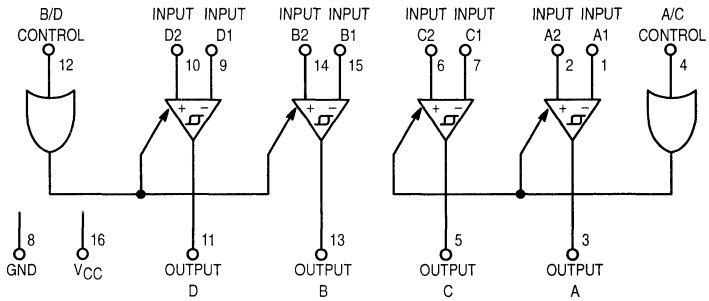
D SUFFIX
SOG PACKAGE
CASE 751B

ORDERING INFORMATION

MC34C86P	Plastic DIP
MC34C86D	SOG Package

2

BLOCK DIAGRAM



This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

REV 4
10/95

TRUTH TABLE

Control Input	Input	Output
L	X	Z
H	$V_{ID} \geq V_{TH}$ (Max)	1
H	$V_{ID} \leq V_{TH}$ (Min)	0
H	Open	1

X = Don't Care
Z = High Impedance
H = High Logic State
L = Low Logic State

2

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	7	V
Input Voltage	V_I	± 10	V
Input Differential Voltage	V_{ID}	± 14	V
Enable Control Input Voltage	V_{in}	V_{CC} + 0.5	V
Storage Temperature	T_{stg}	– 65 to + 150	°C
Maximum Current per Output	I_O	± 25	mA
ESD (Human Body Model)		2000	V

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than the maximum rated voltages to this high impedance circuit.

For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$. Reliability of operation is enhanced if unused inputs are tied to and appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

OPERATING CONDITIONS

Rating	Symbol	Min	Max	Unit
Power Supply Voltage	V_{CC}	4.5	5.5	V
Operating Temperature Range	T_A	– 40	+ 85	°C
Input Rise and Fall Time	t_r, t_f	—	500	ns

DC CHARACTERISTICS (V_{CC} = 4.5 to 5.5 V, T_A = – 40 to + 85°C, unless otherwise stated) (See Note 1)

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply Current, V_{CC} = Max	I_{CC}	—	6	12	mA
Enable Input Current, $V_{in} = V_{CC}$ or GND	I_L	—	—	± 1.0	µA
Input Voltage — Low Logic State (Enable Control)	V_{IL}	—	—	0.8	V
Input Voltage — High Logic State (Enable Control)	V_{IH}	2	—	—	V
Differential Input Voltage, – 7 V < V_{LCM} < 7 V $V_{out} = V_{OH}$ / $V_{out} = V_{OL}$	V_{TH}	0.2 —	— —	— – 0.2	V
Input Hysteresis, V_{LCM} = 0 V	V_{hys}	—	75	—	mV
Comparator Input Current V_{in} = + 10 V, Other Input = GND / V_{in} = – 10 V, Other Input = GND	I_{in}	— —	1.4 – 2.5	— —	mA
Comparator Input Resistance, – 10 V < V_{LCM} < + 10 V	R_{in}	4	4.8	—	kΩ
Output Voltage (Low Logic State) V_{ID} = – 1 V, I_{out} = 6 mA (Note 2)	V_{OL}	—	0.13	0.33	V
Output Voltage (High Logic State) V_{ID} = + 1 V, I_{out} = – 6 mA (Note 2)	V_{OH}	3.8	4.8	—	V
Output Leakage Current (High Logic State) $V_{out} = V_{CC}$ or GND	I_{OZ}	– 5	—	5	µA

NOTES:
1. All currents into device pins are shown as positive, out of device pins are negative. All voltages referenced to ground unless otherwise noted.
2. See EIA specifications EIA–422–A for exact test conditions.

AC CHARACTERISTICS (V_{CC} = 4.5 to 5.5 V, T_A = – 40 to + 85°C, unless otherwise stated)

Parameter	Symbol	Min	Typ	Max	Unit
Propagation Delay Input to Output, C_L = 50 pF, V_{DIFF} = 2.5 V	t_{PLH} t_{PHL}	—	18	30	ns
Skew = $\lvert t_{PHL} - t_{PLH} \rvert$	Skew	—	1	—	ns
Propagation Delay Enable to Output C_L = 50 pF, R_L = 1000 Ω, V_{DIFF} = 2.5 V	t_{PLZ} t_{PHZ}	—	12	—	ns
Propagation Delay Enable to Output C_L = 50 pF, R_L = 1000 Ω, V_{DIFF} = 2.5 V	t_{PZL} t_{PZH}	—	14	—	ns

2

AC TEST CIRCUIT AND SWITCHING TIME WAVEFORMS

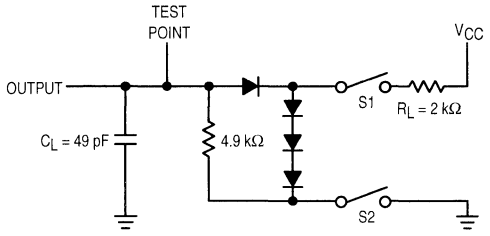


Figure 1. Test Circuit

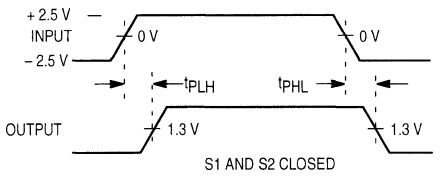


Figure 2. Propagation Delays

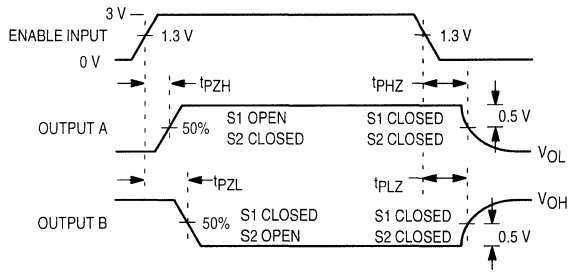


Figure 3. Enable and Disable Times

TYPICAL APPLICATIONS

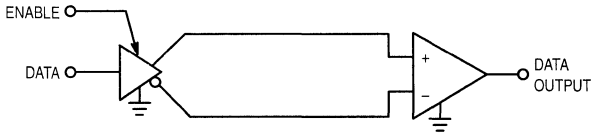
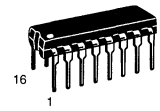


Figure 4. Two–Wire Balanced Systems (EIA–422–A)

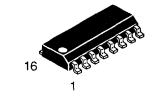
MC34C87

Product Preview

Quad EIA-422-A Line Driver
CMOS



P SUFFIX
PLASTIC DIP
CASE 648



D SUFFIX
SOG PACKAGE
CASE 751B

ORDERING INFORMATION

MC34C87P	Plastic DIP
MC34C87D	SOG Package

2

The MC34C87 is a quad differential line driver designed for digital data transmission over balanced lines. The MC34C87 meets all the requirements of standard EIA–422–A while retaining the low–power characteristics of CMOS.

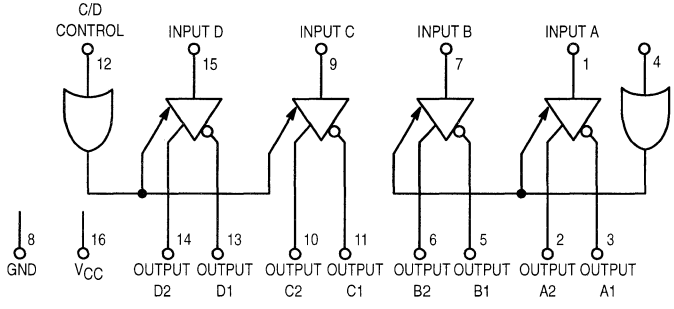
The MC34C87 accepts TTL or CMOS input levels and translates these to EIA–422–A output level. This part uses special output circuitry that enables the individual drivers to power down without loading down the bus. The MC34C87 also includes special circuitry which will set the outputs to a high impedance mode during power up or down, preventing spurious glitches. Each enable pin controls two drivers.

The MC34C87 is pin compatible with the MC3487.

All pins are protected against damage due to electrostatic discharges.

- Maximum Power Supply Current: 3 mA
- 2000 V ESD Protection on the Inputs and the Outputs
- TTL/CMOS Input Compatible
- Typical Propagation Delay: 6 ns
- Typical Output Skew: 1 ns
- Meets V_O = 6.0 V (and V_O = – 0.25 V), V_{CC} = 0 V, I_O < 100 µA Requirement
- Operation from Single 5 V Supply
- High Impedance Mode for Outputs Connected to System Buses

BLOCK DIAGRAM



This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

REV 3
1993

TRUTH TABLE

Control Input	Input	Non–Inverting Output	Inverting Output
L	X	Z	Z
H	H	H	L
H	L	L	H

X = Don't Care
Z = High Impedance
H = High Logic State
L = Low Logic State

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	7	V
DC Input Voltage	V_{in}	– 1.5 to V_{CC} + 1.5	V
DC Output Voltage*	V_{out}	– 0.5 to V_{CC} + 0.5	V
DC Output Current, per Pin	I_{out}	150	mA
DC V_{CC} or GND Current, per Pin	I_{DD}	150	mA
Storage Temperature	T_{stg}	– 65 to + 150	°C
Power Dissipation	P_D	500	mW
ESD (Human Body Model)		2000	V

* Power–on conditions.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than the maximum rated voltages to this high impedance circuit.

For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$. Reliability of operation is enhanced if unused inputs are tied to and appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

OPERATING CONDITIONS

Rating	Symbol	Min	Max	Unit
Power Supply Voltage	V_{CC}	4.5	5.5	V
DC Input Voltage	V_{in}	0	V_{CC}	V
Operating Temperature Range	T_A	– 40	+ 85	°C
Input Rise and Fall Time	t_r, t_f	—	500	ns

DC CHARACTERISTICS (V_{CC} = 4.5 to 5.5 V, T_A = – 40 to + 85°C, unless otherwise stated)

Parameter	Symbol	Min	Typ	Max	Unit
Input Voltage (Low Logic State)	V_{IL}	—	—	0.8	V
Input Voltage (High Logic State)	V_{IH}	2.0	—	—	V
Output Voltage (Low Logic State) I_{sink} = 20 mA	V_{OL}	—	0.3	0.5	V
Output Voltage (High Logic State) I_{source} = – 20 mA	V_{OH}	2.5	2.8	—	V
Output Differential Voltage R_L = 100 Ω (Note 1)	V_{OD}	2.0	—	—	V
Output Differential Voltage Difference R_L = 100 Ω (Note 1)	$D(V_{OD})$	—	—	± 0.4	V
Output Offset Voltage R_L = 100 Ω (Note 1)	V_{OS}	—	—	3.0	V
Output Offset Voltage Difference R_L = 100 Ω (Note 1)	$D(V_{OS})$	—	—	± 0.4	V
Input Current V_{in} = V_{CC}, GND, V_{IH} or V_{IL}	I_{in}	—	—	± 1.0	µA
Quiescent Supply Current I_{out} = 0 µA	I_{CC}	—	—	3.0	mA
Output Short Circuit Current (Note 2)	I_{OS}	– 30	– 100	– 150	mA
Output Leakage Current (High–Z State) V_{out} = V_{CC} or GND	$I_{O(Z)}$	—	—	± 1.0	µA
Output Leakage Current (Power Off) V_{out} = 6 V V_{out} = – 0.25 V	I_{oxh} I_{oxl}	— —	— —	100 – 100	µA

NOTES:
1. See EIA specifications EIA–422–A for exact test conditions.
2. Only one output may be shorted at a time.

AC CHARACTERISTICS (V_{CC} = 4.5 to 5.5 V, T_A = – 40 to + 85°C, unless otherwise stated)

Parameter	Symbol	Min	Typ	Max	Unit
Propagation Delay Input to Output (S1 Open)	t_{PLH} t_{PHL}	—	6	12	ns
Output Skew (S1 Open)*	Skew	—	1.0	4	ns
Differential Output Rise Time Fall Time (S1 Open)	t_{TLH} t_{THL}	—	4	8	ns
Output Enable Time (S1 Closed)	t_{PZH} t_{PZL}	— —	16 15	— —	ns
Output Disable Time (S1 Closed)	t_{PHZ} t_{PLZ}	— —	6 9	— —	ns

* Skew: difference in propagation delays between complementary outputs.

2

AC TEST CIRCUIT AND SWITCHING TIME WAVEFORMS

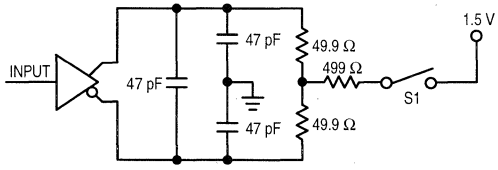


Figure 1. AC Test Circuit

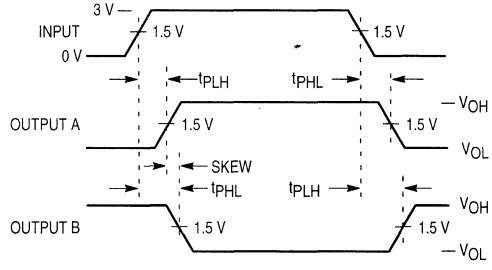


Figure 2. Propagation Delays and Skew Waveforms

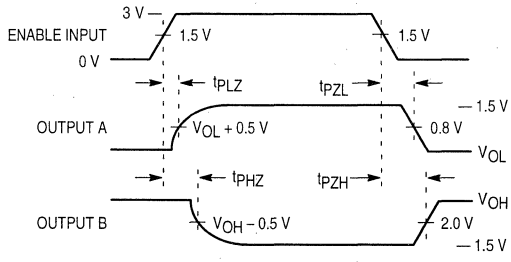


Figure 3. Enable and Disable Times

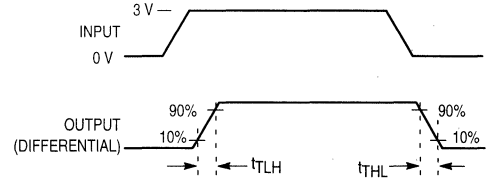


Figure 4. Differential Rise and Fall Times

TYPICAL APPLICATIONS

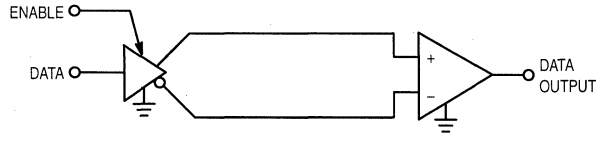


Figure 5. Two–Wire Balanced Systems (EIA–422–A)

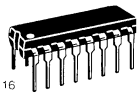
MC3418

Continuously Variable Slope Delta Modulator/Demodulator

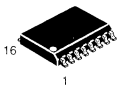
Laser–Trimmed Integrated Circuit

Providing a simplified approach to digital speech encoding/decoding, the MC3418 CVSD is designed for military secure communication and commercial telephone applications. A single IC provides both encoding and decoding functions.

- Encode and Decode Functions on the Same Chip with a Digital Input for Selection
- Utilization of Compatible I^2L — Linear Bipolar Technology
- CMOS Compatible Digital Output
- Digital Input Threshold Selectable ($V_{CC}/2$ Reference Provided On Chip)
- MC3418 has a 4–Bit Algorithm (Commercial Telephone)



P SUFFIX
PLASTIC DIP
CASE 648

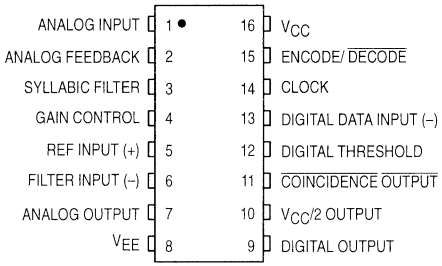


DW SUFFIX
PLASTIC SOIC
CASE 751G
SO–16L

ORDERING INFORMATION

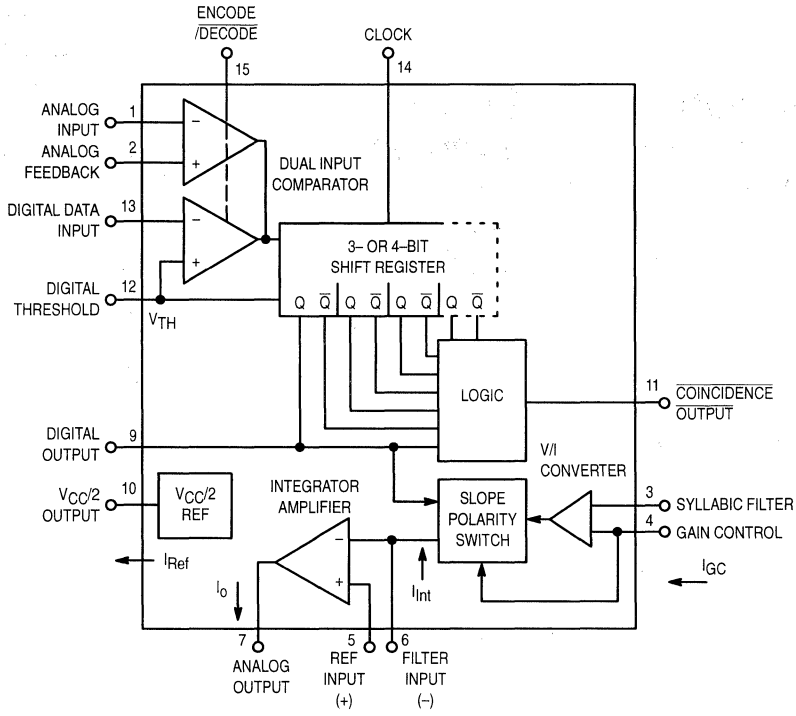
MC3418P	Plastic DIP
MC3418DW	Plastic SOIC

PIN ASSIGNMENT



REV
9/95

BLOCK DIAGRAM



MAXIMUM RATINGS

(All voltages referenced to V_{EE}, T_A = 25°C unless otherwise noted)

Parameter	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.4 to + 18	Vdc
Differential Analog Input Voltage	V_{ID}	± 5.0	Vdc
Digital Threshold Voltage	V_{TH}	– 0.4 to V_{CC}	Vdc
Logic Input Voltage (Clock, Digital Data, Encode/$\overline{\text{Decode}}$)	V_{Logic}	– 0.4 to +18	Vdc
Coincidence Output Voltage	$V_{O(Con)}$	– 0.4 to + 18	Vdc
Syllabic Filter Input Voltage	$V_{I(Syl)}$	– 0.4 to V_{CC}	Vdc
Gain Control Input Voltage	$V_{I(GC)}$	– 0.4 to V_{CC}	Vdc
Reference Input Voltage	$V_{I(Ref)}$	V_{CC}/2 – 1.0 to V_{CC}	Vdc
V_{CC}/2 Output Current	I_{Ref}	– 25	mA

ELECTRICAL CHARACTERISTICS (V_{CC} = 12 V, V_{EE} = Gnd, T_A = 0 to 70°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Power Supply Voltage Range (Figure 1)		V_{CCR}	4.75	12	16.5	Vdc
Power Supply Current (Figure 1) (@ Idle Channel)	V_{CC} = 5.0 V V_{CC} = 15 V	I_{CC}	— —	3.7 6.0	5.5 11	mA
Gain Control Current Range (Figure 2)		I_{GCR}	0.002	—	3.0	mA
Analog Comparator Input Range (Pins 1 and 2) (4.75 V ≤ V_{CC} ≤ 16.5 V)		V_I	1.3	—	V_{CC} – 1.3	Vdc
Analog Output Range (Pin 7) (4.75 V ≤ V_{CC} ≤ 16.5 V, I_O = ± 5.0 mA)		V_O	1.3	—	V_{CC} – 1.3	Vdc
Input Bias Currents (Figure 3) (Comparator in Active Region)	Analog Input (I1) Analog Feedback (I2) Syllabic Filter Input (I3) Reference Input (I5)	I_{IB}	— — — —	0.25 0.25 0.06 – 0.06	1.0 1.0 0.3 – 0.3	µA
Input Offset Current (Comparator in Active Region)	Analog Input/Analog Feedback |I1 – I2| (Figure 3) Analog Input/Analog Feedback |I5 – I6| (Figure 4)	I_{IO}	— —	0.05 0.01	0.4 0.1	µA
Input Offset Voltage V/I Converter (Pins 3 and 4) (Figure 5)		V_{IO}	—	2.0	6.0	mV
Transconductance	V/I Converter, 0 to 3.0 mA Integrator Amplifier, 0 to ± 5.0 mA Load	gm	0.1 1.0	0.3 10	— —	mA/mV
Propagation Delay Times (See Note)	Clock Trigger to Digital Output C_L = 25 pF to Gnd Clock Trigger to Coincidence Output C_L = 25 pF to Gnd, R_L = 4.0 kΩ to V_{CC}	t_{PLH} t_{PHL} t_{PLH} t_{PHL}	— — — —	1.0 0.8 1.0 0.8	2.5 2.5 3.0 2.0	µs
Coincidence Output Voltage — Low Logic Stage ($I_{OL(Con)}$ = 3.0 mA)		$V_{OL(Con)}$	—	0.12	0.25	Vdc
Coincidence Output Leakage Current — High Logic State (V_{OH} = 15 V, 0°C ≤ T_A ≤ 70°C)		$I_{OH(Con)}$	—	0.01	0.5	µA
Applied Digital Threshold Voltage Range (Pin 12)		V_{TH}	+ 1.2	—	V_{CC} – 2.0	Vdc
Digital Threshold Input Current (1.2 V ≤ V_{th} ≤ V_{CC} – 2.0 V) V_{IL} Applied to Pins 13, 14, and 15 V_{IH} Applied to Pins 13, 14, and 15		$I_{I(th)}$	 — —	 — – 10	 5.0 – 50	µA
Maximum Integrator Amplifier Output Current		I_O	± 5.0	—	—	mA
V_{CC}/2 Generator Maximum Output Current (Source Only)		I_{Ref}	+ 10	—	—	mA
V_{CC}/2 Generator Output Impedance (0 to + 10 mA)		z_{Ref}	—	3.0	6.0	Ω
V_{CC}/2 Generator Tolerance (4.75 V ≤ V_{CC} ≤ 16.5 V)		εr	—	—	± 3.5	%

NOTE: All propagation delay times measured 50% to 50% from the negative going (from V_{CC} to + 0.4 V) edge of the clock.

ELECTRICAL CHARACTERISTICS (continued)

Characteristic		Symbol	Min	Typ	Max	Unit
Logic Input Voltage (Pins 13, 14, and 15)	Low Logic State	V_{IL}	Gnd	—	V_{th} – 0.4	Vdc
	High Logic State	V_{IH}	V_{th} + 0.4	—	18	
Dynamic Total Loop Offset Voltage (See Note) (Figures 3, 4, and 5)		ΣV_{offset}				mV
I_{GC} = 12 µA, V_{CC} = 12 V	T_A = 25°C		—	± 0.5	± 3.0	
	0°C ≤ T_A ≤ + 70°C		—	± 0.75	± 3.8	
I_{GC} = 12 µA, V_{CC} = 5.0 V	T_A = 25°C		—	± 1.0	± 3.5	
	0°C ≤ T_A ≤ + 70°C		—	± 1.3	± 4.3	
Digital Output Voltage	I_{OH} = 3.6 mA	V_{OL}	—	0.1	0.4	Vdc
	I_{OH} = – 3.5 mA	V_{OH}	V_{CC} – 1.0	V_{CC} – 2.0	—	
Syllabic Filter Applied Voltage (Pin 3) (Figure 2)		$V_{I(Syl)}$	+ 3.2	—	V_{CC}	Vdc
Integrating Current (Figure 2)	I_{GC} = 12 µA	$\lvert I_{Int} \rvert$	8.0	10	12	µA
	I_{GC} = 1.5 mA		1.42	1.5	1.58	mA
	I_{GC} = 3.0 mA		2.75	3.0	3.25	mA
Dynamic Integrating Current Match (Figure 6)	I_{GC} = 1.5 mA	$V_{O(Ave)}$	—	± 100	± 280	mV
Input Current — High Logic State (V_{IH} = 18 V)	Digital Data Input	I_{IH}	—	—	+ 5.0	µA
	Clock Input		—	—	+ 5.0	
	Encode/$\overline{\text{Decode}}$ Input		—	—	+ 5.0	
Input Current — Low Logic State (V_{IL} = 0 V)	Digital Data Input	I_{IL}	—	—	– 10	µA
	Clock Input		—	—	– 360	
	Encode/$\overline{\text{Decode}}$ Input		—	—	– 36	
	Clock Input, V_{IL} = 0.4 V		—	—	– 72	

NOTE: Dynamic total loop offset (ΣV_{offset}) equals V_{IO} (comparator) (Figure 3) minus V_{IOX} (Figure 5). The input offset voltages of the analog comparator and of the integrator amplifier include the effects of input offset current through the input resistors. The slope polarity switch current mismatch appears as an average voltage across the 10 k integrator resistor. The clock frequency is 32 kHz. Idle channel performance is guaranteed if this dynamic total loop offset is less than one–half of the change in integrator output voltage during one clock cycle (ramp step size). Laser trimming is used to ensure good idle channel performance.

DEFINITION AND FUNCTION OF PINS

Pin 1 — Analog Input

This is the analog comparator inverting input where the voice signal is applied. It may be ac or dc coupled depending on the application. If the voice signal is to be level shifted to the internal reference voltage, then a bias resistor between Pins 1 and 10 is used. The resistor is used to establish the reference as the new dc average of the ac coupled signal. The analog comparator was designed for low hysteresis (typically less than 0.1 mV) and high gain (typically 70 dB).

Pin 2 — Analog Feedback

This is the noninverting input to the analog signal comparator within the IC. In an encoder application it should be connected to the analog output of the encoder circuit. This may be Pin 7 or a low pass filter output connected to Pin 7. In a decode circuit Pin 2 is not used and may be tied to $V_{CC}/2$ on Pin 10, ground, or left open.

The analog input comparator has bias currents of 1.5 µA max, thus the driving impedances of Pins 1 and 2 should be equal to avoid disturbing the idle channel characteristics of the encoder.

Pin 3 — Syllabic Filter

This is the point at which the syllabic filter voltage is returned to the IC in order to control the integrator step size. It is an NPN input to an op amp. The syllabic filter consists of an RC network between Pins 11 and 3. Typical time constant values of 6.0 ms to 50 ms are used in voice codecs.

Pin 4 — Gain Control Input

The syllabic filter voltage appears across C_S of the syllabic filter and is the voltage between V_{CC} and Pin 3. The active voltage to current (V – I) converter drives Pin 4 to the same voltage at a slew rate of typically 0.5 V/µs. Thus the current injected into Pin 4 (I_{GC}) is the syllabic filter voltage divided by the R_X resistance. Figure 7 shows the relationship between I_{GC} (x–axis) and the integrating current, I_{Int} (y–axis). The discrepancy, which is most significant at very low currents, is due to circuitry within the slope polarity switch which enables trimming to a low total loop offset. The R_X resistor is then varied to adjust the loop gain of the codec, but should be no larger than 5.0 kΩ to maintain stability.

Pin 5 — Reference Input

This pin is the noninverting input of the integrator amplifier. It is used to reference the dc level of the output signal. In an encoder circuit it must reference the same voltage as Pin 1 and is tied to Pin 10.

Pin 6 — Filter Input

This inverting op amp input is used to connect the integrator external components. The integrating current (I_{Int}) flows into Pin 6 when the analog input (Pin 1) is high with respect to the analog feedback (Pin 2) in the encode mode or when the digital data input (Pin 13) is high in the decode mode. For the opposite states, I_{Int} flows out of Pin 6. Single integration systems require a capacitor and resistor between Pins 6 and 7. Multipole configurations will have different circuitry. The re-

sistance between Pins 6 and 7 should always be between 8.0 kΩ and 13 kΩ to maintain good idle channel characteristics.

Pin 7 — Analog Output

This is the integrator op amp output. It is capable of driving a 600–ohm load referenced to $V_{CC}/2$ to + 6.0 dBm and can otherwise be treated as an op amp output. Pins 5, 6, and 7 provide full access to the integrator op amp for designing integration filter networks. The slew rate of the internally compensated integrator op amp is typically 0.5 V/μs. Pin 7 output is current limited for both polarities of current flow at typically 30 mA.

Pin 8 — V_{EE}

The circuit is designed to work in either single or dual power supply applications. Pin 8 is always connected to the most negative supply.

Pin 9 — Digital Output

The digital output provides the results of the delta modulator's conversion. It swings between V_{CC} and V_{EE} and is CMOS or TTL compatible. Pin 9 is inverting with respect to Pin 1 and noninverting with respect to Pin 2. It is clocked on the falling edge of Pin 14. The typical 10% to 90% rise and fall times are 250 ns and 50 ns respectively for V_{CC} = 12 V and C_L = 25 pF to ground.

Pin 10 — $V_{CC}/2$ Output

An internal low impedance mid–supply reference is provided for use in single supply applications. The internal regulator is a current source and must be loaded with a resistor to ensure its sinking capability. If a + 6.0 dBmo signal is expected across a 600 ohm input bias resistor, then Pin 10 must sink 2.2 V/600 Ω = 3.66 mA. This is only possible if Pin 10 sources 3.66 mA into a resistor normally and will source only the difference under peak load. The reference load resistor is chosen accordingly. A 0.1 μF bypass capacitor from Pin 10 to V_{EE} is also recommended. The $V_{CC}/2$ reference is capable of sourcing 10 mA and can be used as a reference elsewhere in the system circuitry.

Pin 11 — $\overline{\text{Coincidence Output}}$

The duty cycle of this pin is proportional to the voltage across C_S. The coincidence output will be low whenever the content of the internal shift register is all 1s or all 0s. The MC3418 contains a 4–bit register. Pin 11 is an open collector of an NPN device and requires a pull–up resistor. If the syllabic filter is to have equal charge and discharge time constants, the value of R_P should be much less than R_S. In systems requiring different charge and discharge constants, the charging constant is R_SC_S while the decaying constant is $(R_S + R_P)C_S$. Thus longer decays are easily achievable. The NPN device should not be required to sink more than 3.0 mA in any configuration. The typical 10% to 90% rise and fall times are 200 ns and 100 ns respectively for R_L = 4.0 kΩ to + 12 V and C_L = 25 pF to ground.

Pin 12 — Digital Threshold

This input sets the switching threshold for Pins 13, 14, and 15. It is intended to aid in interfacing different logic families without external parts. Often it is connected to the $V_{CC}/2$ reference for CMOS interface or can be biased two diode drops above V_{EE} for TTL interface.

Pin 13 — Digital Data Input

In a decode application, the digital data stream is applied to Pin 13. In an encoder it may be unused or may be used to transmit signaling message under the control of Pin 15. It is an inverting input with respect to Pin 9. When Pins 9 and 13 are connected, a toggle flip–flop is formed and a forced idle channel pattern can be transmitted. The digital data input level should be maintained for 0.5 μs before and after the clock trigger for proper clocking.

Pin 14 — Clock Input

The clock input determines the data rate of the codec circuit. A 32K bit rate requires a 32 kHz clock. The switching threshold of the clock input is set by Pin 12. The shift register circuit toggles on the falling edge of the clock input. The minimum width for a positive–going pulse on the clock input is 300 ns, whereas for a negative–going pulse, it is 900 ns.

Pin 15 — $\overline{\text{Encode/Decode}}$

This pin controls the connection of the analog input comparator and the digital input comparator to the internal shift register. If high, the result of the analog comparison will be clocked into the register on the falling edge at Pin 14. If low, the digital input state will be entered. This allows use of the IC as an encoder/decoder or simplex codec without external parts. Furthermore, it allows non–voice patterns to be forced onto the transmission line through Pin 13 in an encoder.

Pin 16 — V_{CC}

The power supply range is from 4.75 to 16.5 volts between Pin V_{CC} and V_{EE}.

CIRCUIT DESCRIPTION

The continuously variable slope delta modulator (CVSD) is a simple alternative to more complex conventional conversion techniques in systems requiring digital communication of analog signals. The human voice is analog, but digital transmission of any signal over great distance is attractive. Signal/noise ratios do not vary with distance in digital transmission and multiplexing, switching and repeating hardware is more economical and easier to design. However, instrumentation A to D converters do not meet the communications requirements. The CVSD A to D is well suited to the requirements of digital communications and is an economically efficient means of digitizing analog inputs for transmission.

The Delta Modulator

The innermost control loop of a CVSD converter is a simple delta modulator. A block diagram CVSD Encoder is shown in Figure 11. A delta modulator consists of a comparator in the forward path and an integrator in the feedback path of a simple control loop. The inputs to the comparator are the

input analog signal and the integrator output. The comparator output reflects the sign of the difference between the input voltage and the integrator output. That sign bit is the digital output and also controls the direction of ramp in the integrator. The comparator is normally clocked so as to produce a synchronous and band–limited digital bit stream.

If the clocked serial bit stream is transmitted, received, and delivered to a similar integrator at a remote point, the remote integrator output is a copy of the transmitting control loop integrator output. To the extent that the integrator at the transmitting locations tracks the input signal, the remote receiver reproduces the input signal. Low pass filtering at the receiver output will eliminate most of the quantizing noise, if the clock rate of the bit stream is an octave or more above the bandwidth of the input signal. Voice bandwidth is 4 kHz and clock rates from 8 k and up are possible. Thus the delta modulator digitizes and transmits the analog input to a remote receiver. The serial, unframed nature of the data is ideal for communications networks. With no input at the transmitter, a continuous one zero alternation is transmitted. If the two integrators are made leaky, then during any loss of contact the receiver output decays to zero and receive restart begins without framing when the receiver reacquires. Similarly, a delta modulator is tolerant of sporadic bit errors. Figure 12 shows the delta modulator waveforms while Figure 13 shows the corresponding CVSD decoder block diagram.

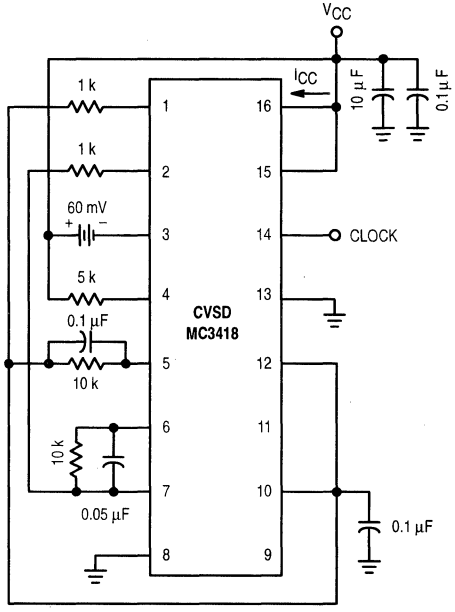
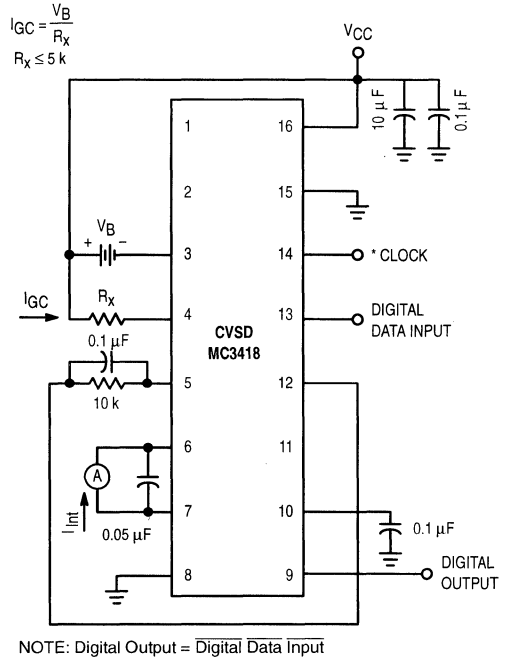


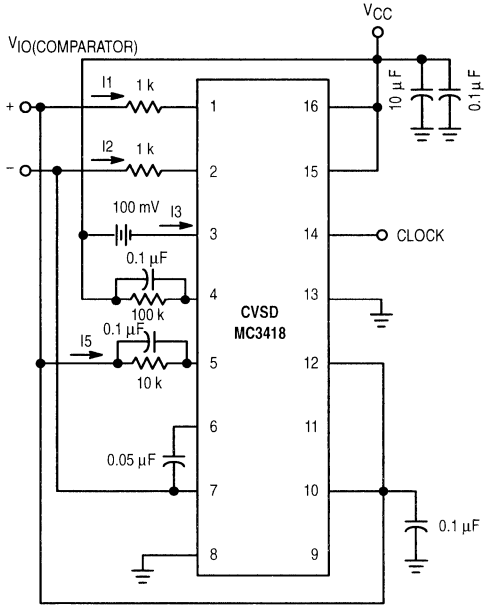
Figure 1. Power Supply Current



NOTE: Digital Output = $\overline{\text{Digital Data Input}}$

* For static testing, the clock is only necessary for preconditioning to obtain proper state for a given input.

Figure 2. I_{GCR} — Gain Control Range and I_{Int} — Integrating Current



NOTE: The analog comparator offset voltage is tested under dynamic conditions and therefore must be measured with appropriate filtering.

Figure 3. Input Bias Currents, Analog Comparator Offset Voltage and Current

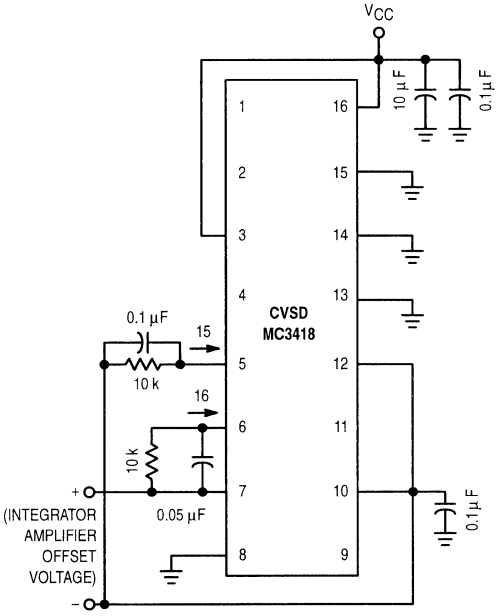
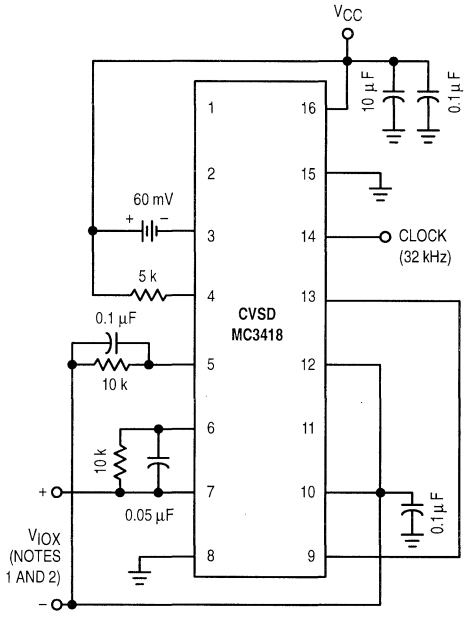
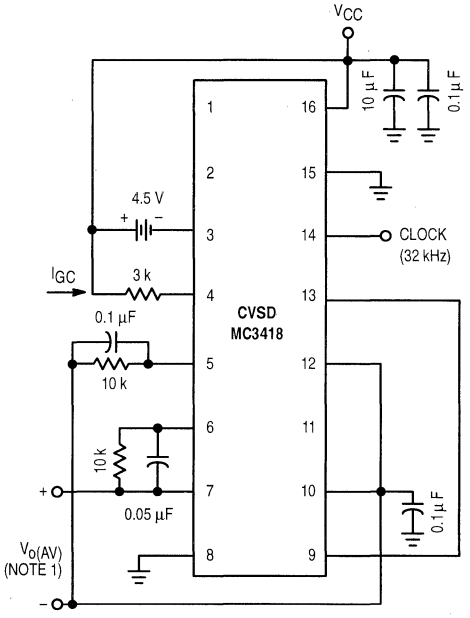


Figure 4. Integrator Amplifier Offset Voltage and Current



NOTES:
1. Integrator amplifier offset voltage plus slope polarity switch mismatch.
2. V_{IOX} is the average voltage of the triangular waveform observed at the measurement points.

Figure 5. V/I Converter Offset Voltage, V_{IO} and V_{IOX}



NOTES:
1. $V_{O(AV)}$, Dynamic Integrating Current Match, is the average voltage of the triangular waveform observed at the measurement points, across 10 kΩ resistor with I_{GC} = 1.5 mA.
2. See note in the Electrical Characteristics table.

Figure 6. Dynamic Integrating Current Match

TYPICAL PERFORMANCE CURVES

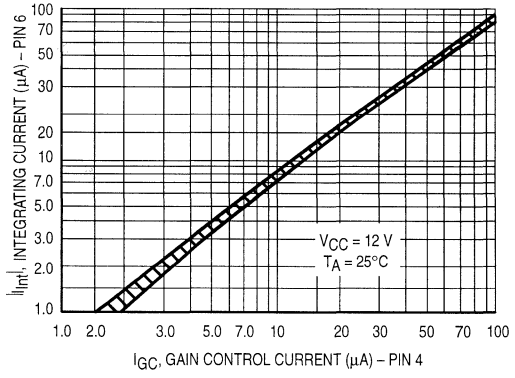


Figure 7. Typical I_{Int} versus I_{GC} (Mean ± 2 σ)

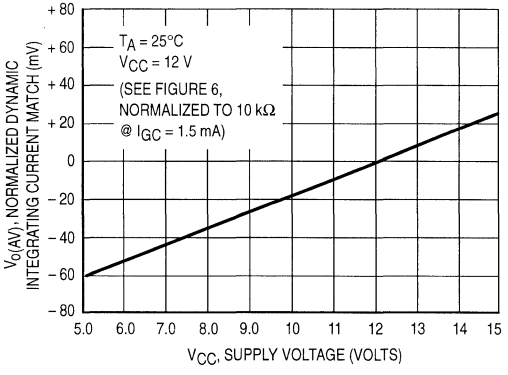


Figure 8. Normalized Dynamic Integrating Current Match versus V_{CC}

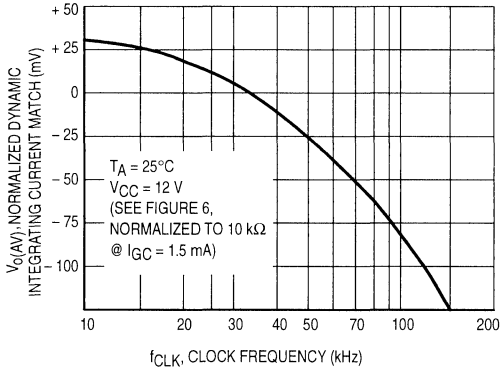


Figure 9. Normalized Dynamic Integrating Current Match versus Clock Frequency

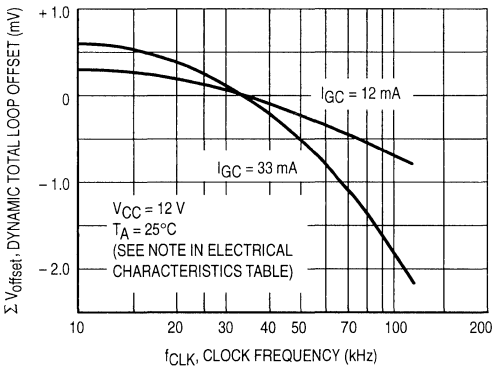


Figure 10. Dynamic Total Loop Offset versus Clock Frequency

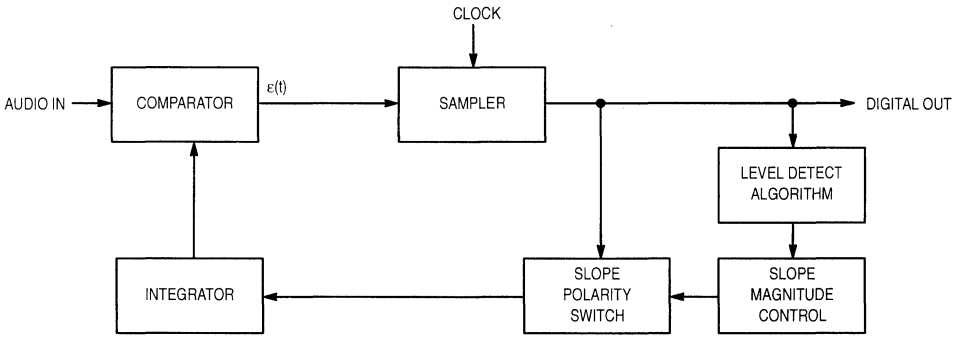


Figure 11. Block Diagram of the CVSD Encoder

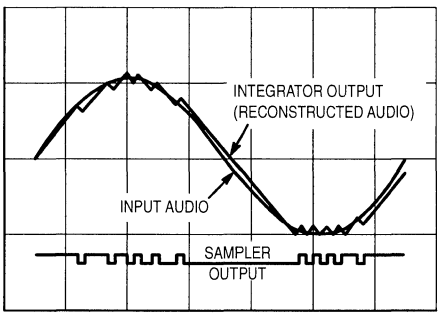


Figure 12. CVSD Waveforms

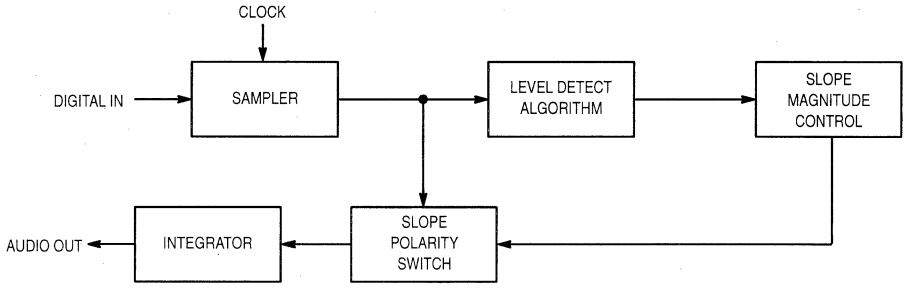


Figure 13. Block Diagram of the CVSD Decoder

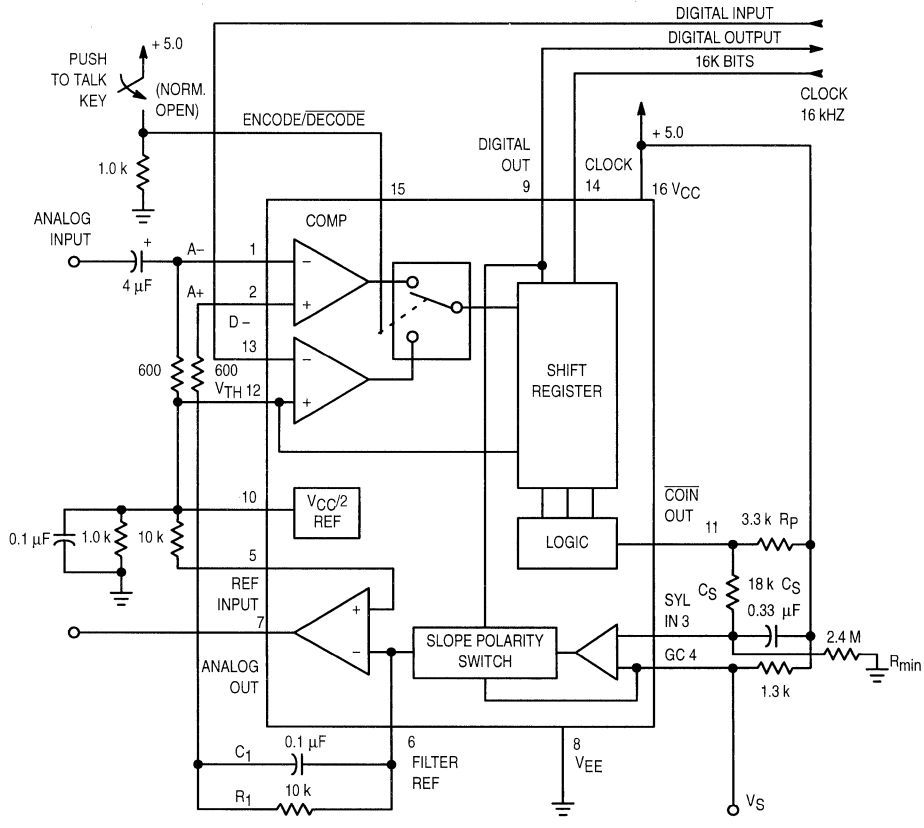


Figure 14. 16 kHz Simplex Voice Codec (Single Pole Companding and Single Integration)

The Companding Algorithm

The fundamental advantages of the delta modulator are its simplicity and the serial format of its output. Its limitations are its ability to accurately convert the input within a limited digital bit rate. The analog input must be band limited and amplitude limited. The frequency limitations are governed by the nyquist rate while the amplitude capabilities are set by the gain of the integrator.

The frequency limits are bounded on the upper end; that is, for any input bandwidth there exists a clock frequency larger than that bandwidth which will transmit the signal with a specific noise level. However, the amplitude limits are bounded on both upper and lower ends. For a signal level, one specific gain will achieve an optimum noise level. Unfortunately, the basic delta modulator has a small dynamic range over which the noise level is constant.

The continuously variable slope circuitry provides increased dynamic range by adjusting the gain of the integrator. For a given clock frequency and input bandwidth the additional circuitry increases the delta modulator's dynamic range. External to the basic delta modulator is an algorithm which monitors the past few outputs of the delta modulator in a simple shift register. The register is 4 bits long. The accepted CVSD algorithm simply monitors the contents of the shift register and indicates if it contains all 1s or 0s. This condition is called coincidence. When it occurs, it indicates that the gain of the integrator is too small. The coincidence output charges a single pole low pass filter. The voltage output of this syllabic filter controls the integrator gain through a pulse amplitude modulator whose other input is the sign bit or up/down control.

The simplicity of the all 1s, all 0s algorithm should not be taken lightly. Many other control algorithms using the shift register have been tried. The key to the accepted algorithm is that it provides a measure of the average power or level of the input signal. Other techniques provide more instantaneous information about the shape of the input curve. The purpose of the algorithm is to control the gain of the integrator and to increase the dynamic range. Thus a measure of the average input level is what is needed.

The algorithm is repeated in the receiver and thus the level data is recovered in the receiver. Because the algorithm only operates on the past serial data, it changes the nature of the bit stream without changing the channel bit rate.

The effect of the algorithm is to compand the input signal. If a CVSD encoder is played into a basic delta modulator, the output of the delta modulator will reflect the shape of the input signal but all of the output will be at an equal level. Thus the algorithm at the output is needed to restore the level variations. The bit stream in the channel is as if it were from a standard delta modulator with a constant level input.

The delta modulator encoder with the CVSD algorithm provides an efficient method for digitizing a voice input in a manner which is especially convenient for digital communications requirements.

APPLICATIONS INFORMATION

CVSD DESIGN CONSIDERATIONS

A simple CVSD encoder using the MC3418 is shown in Figure 14. This IC is a general purpose CVSD building block which allows the system designer to tailor the encoder's transmission characteristics to the application. Thus, the achievable transmission capabilities are constrained by the fundamental limitations of delta modulation and the design of encoder parameters. The performance is not dictated by the internal configuration of the MC3418. There are seven design considerations involved in designing these basic CVSD building blocks into a specific codec application, and they are as follows:

1. Selection of clock rate
2. Required number of shift register bits
3. Selection of loop gain
4. Selection of minimum step size
5. Design of integration filter transfer function
6. Design of syllabic filter transfer function
7. Design of low pass filter at the receiver

The circuit in Figure 14 is the most basic CVSD circuit possible. For many applications in secure radio or other intelligible voice channel requirements, it is entirely sufficient. In this circuit, items 5 and 6 are reduced to their simplest form. The syllabic and integration filters are both single pole networks. The selection of items 1 through 4 govern the codec performance.

Layout Considerations

Care should be exercised to isolate all digital signal paths (Pins 9, 11, 13, and 14) from analog signal paths (Pins 1 – 7 and 10) in order to achieve proper idle channel performance.

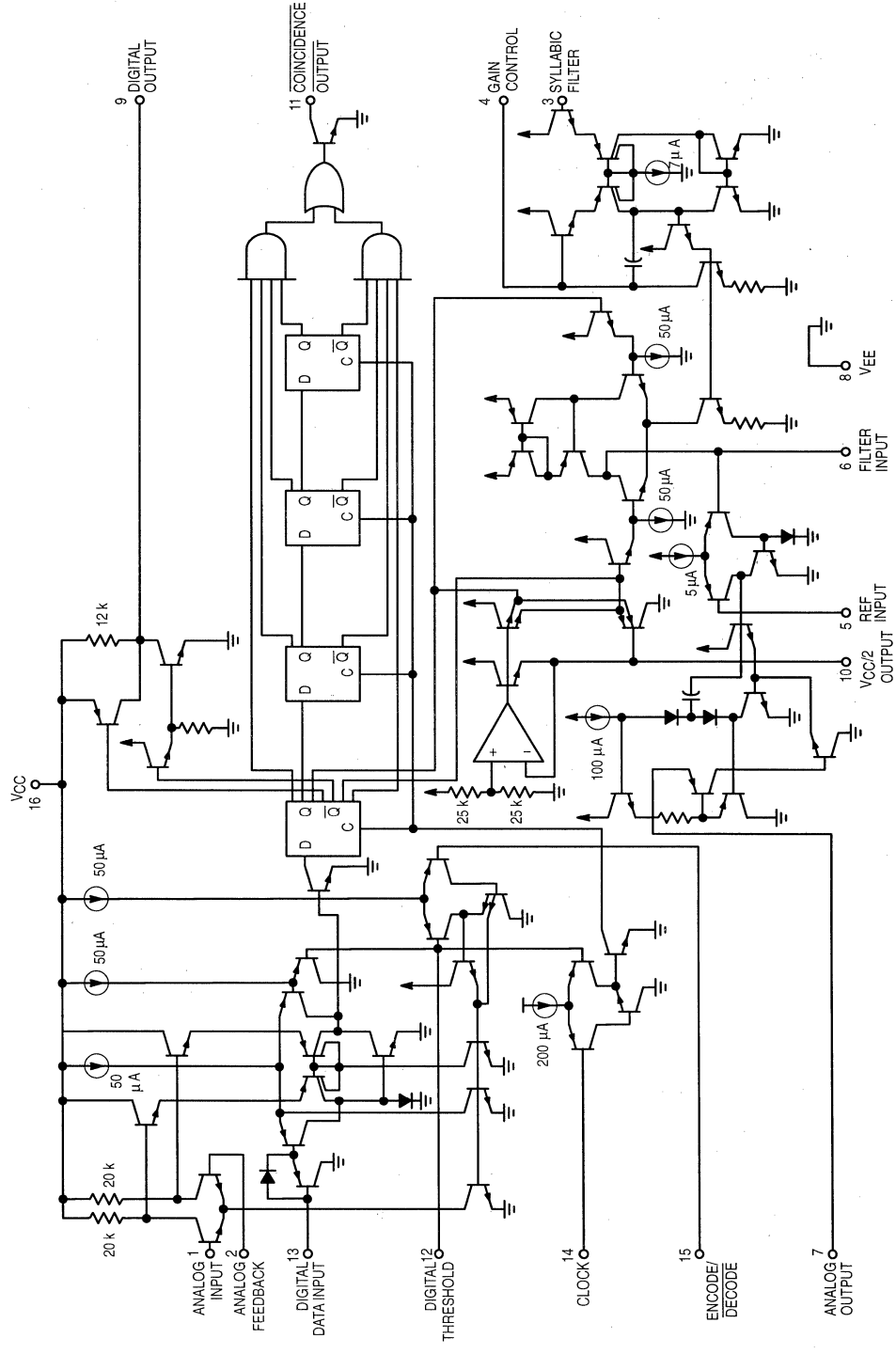
Clock Rate

With minor modifications, the circuit in Figure 14 may be operated anywhere from 9.6 kHz to 64 kHz clock rates. Obviously the higher the clock rate the higher the S/N performance. The circuit in Figure 14 typically produces the S/N performance shown in Figure 15. The selection of clock rate is usually dictated by the bandwidth of the transmission medium. Voice bandwidth systems will require no higher than 9600 Hz. Some radio systems will allow 12 kHz. Private 4–wire telephone systems are often operated at 16 kHz and commercial telephone performance can be achieved at 32K bits and above. Other codecs may use bit rates up to 200K bits/sec.

Shift Register Length (Algorithm)

The MC3418 has a four–bit algorithm well suited for 32 kHz and higher clock rates. Since the algorithm records a fixed past history of the input signal, a longer shift register is required to obtain the same internal history. At 16 bits and below, the four–bit algorithm will produce a slightly wider dynamic range at the expense of level change response. Basically the MC3418 is intended for high performance, high bit rate systems.

CVSD CIRCUIT SCHEMATIC



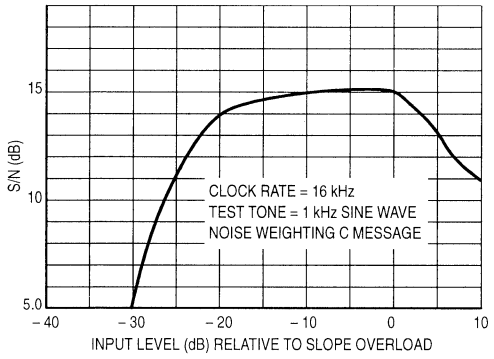


Figure 15. Signal–to–Noise Performance with Single Integration, Single–Pole and Companding at 16K Bits (Typical)

Selection of Loop Gain

The gain of the circuit in Figure 14 is set by resistor R_X. R_X must be selected to provide the proper integrator step size for high level signals such that the companding ratio does not exceed about 25%. The companding ratio is the active low duty cycle of the coincidence output on Pin 11 of the codec circuit. Thus the system gain is dependent on:

1. The maximum level and frequency of the input signal.
2. The transfer function of the integration filter.

For voice codecs the typical input signal is taken to be a sine wave at 1 kHz of 0 dBmo level. In practice, the useful dynamic range extends about 6 dB above the design level. In any system the companding ratio should not exceed 30%.

To calculate the required step size current, we must describe the transfer characteristics of the integration filter. In the basic circuit of Figure 14, a single pole of 160 Hz is used.

$$R_1 = 10\ k\Omega,\ C_1 = 0.1\ \mu F$$

$$\frac{V_o}{I_i} = \frac{1}{C(S + 1/RC)} \equiv \frac{K}{S + \omega_o}$$

$$\omega_o = 2\pi f$$

$$10^3\ \omega_o = 2\pi f$$

$$f = 159.2\ Hz$$

Note that the integration filter produces a single–pole response from 300 to 3 kHz. The current required to move the integrator output a specific voltage from zero is simply:

$$I_i = \frac{V_o}{R_1} + \left(C_1 \times \frac{dV_o}{dt}\right)$$

Now a 0 dBmo sine wave has a peak value of 1.0954 volts. In 1/8 of a cycle of a sine wave centered around the zero crossing, the sine wave changes by approximately its peak value. The CVSD step should trace that change. The required current for a 0 dBm 1 kHz sine wave is:

$$I_i = \frac{1.1\ V}{*2(10\ k\Omega)} + \frac{0.1\ \mu F\ (1.1)}{0.125\ ms} = 0.935\ mA$$

* The maximum voltage across R_1 when maximum slew is required is:

$$\frac{1.1\ V}{2}$$

Now the voltage range of the syllabic filter is the power supply voltage, thus:

$$R_X = 0.25(V_{CC})\ \frac{1}{0.935\ mA}$$

A similar procedure can be followed to establish the proper gain for any input level and integration filter type.

Minimum Step Size

The final parameter to be selected for the simple codec in Figure 14 is idle channel step size. With no input signal, the digital output becomes a one–zero alternating pattern and the analog output becomes a small triangle wave. Mismatches of internal currents and offsets limit the minimum step size which will produce a perfect idle channel pattern. The MC3418 is tested to ensure that a 20 mV p–p minimum step size at 16 kHz will attain a proper idle channel. The idle channel step size must be twice the specified total loop offset if a one–zero idle pattern is desired. In some applications a much smaller minimum step size (e.g., 0.1 mV) can produce quiet performance without providing a 1 – 0 pattern.

To set the idle channel step size, the value of R_{min} must be selected. With no input signal, the slope control algorithm is inactive. A long series of ones or zeros never occurs. Thus, the voltage across the syllabic filter capacitor (C_S) would decay to zero. However, the voltage divider of R_S and R_{min} (see Figure 14) sets the minimum allowed voltage across the syllabic filter capacitor. That voltage must produce the desired ramps at the analog output. Again we write the filter input current equation:

$$I_i = \frac{V_o}{R_1} + C\frac{dV_o}{dt}$$

For values of V_o near $V_{CC}/2$ the V_o/R term is negligible; thus:

$$I_i = C_S\frac{\Delta V_o}{\Delta T}$$

where ΔT is the clock period and ΔV_o is the desired peak–to–peak value of the idle output. For a 16K–bit system using the circuit in Figure 14:

$$I_i = \frac{0.1\ \mu F\ 20\ mV}{62.5\ \mu s} = 33\ \mu A$$

The voltage on C_S which produces a 33 μA current is determined by the value of R_X.

$$I_i R_X = V_S min;\ \text{for } 33\ \mu A,\ V_S min = 41.6\ mV$$

In Figure 14 R_S is 18 kΩ. That selection is discussed with the syllabic filter considerations. The voltage divider of R_S and R_{min} must produce an output of 41.6 mV.

$$V_{CC}\frac{R_S}{R_S + R_{min}} = V_{Smin} \qquad R_{min} \simeq 2.4\ M\Omega$$

Having established these four parameters — clock rate, number of shift register bits, loop gain, and minimum step

size — the encoder circuit in Figure 14 will function at near optimum performance for input levels around 0 dBm.

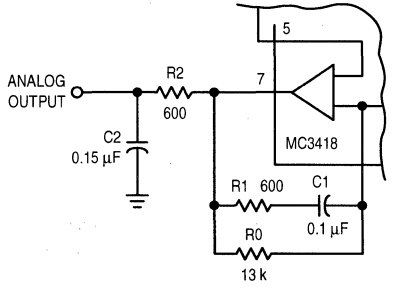
INCREASING CVSD PERFORMANCE

Integration Filter Design

The circuit in Figure 14 uses a single–pole integration network formed with a 0.1 μF capacitor and a 10 kΩ resistor. It is possible to improve the performance of the circuit in Figure 14 by 1 or 2 dB by using a two–pole integration network. The improved circuit is shown.

The first pole is still placed below 300 Hz to provide the 1/S voice content curve and a second pole is placed somewhere above the 1 kHz frequency. For telephony circuits, the second pole can be placed above 1.8 kHz to exceed the 1633 touchtone frequency. In other communication systems, values as low as 1 kHz may be selected. In general, the lower in frequency the second pole is placed, the greater the noise improvement. Then, to ensure the encoder loop stability, a zero is added to keep the phase shift less than 180°. This zero should be placed slightly above the low–pass output filter break frequency so as not to reduce the effectiveness of the second pole. A network of 235 Hz, 2 kHz, and 5.2 kHz is typical for telephone applications while 160 Hz, 1.2 kHz, and 2.8 kHz might be used in voice only channels. (Voice only channels can use an output low–pass filter which breaks at about 2.5 kHz.) The two–pole network in Figure 16 has a transfer function of:

$$\frac{V_o}{I_i} = \frac{R_0R_1\left(S+\frac{1}{R_1C_1}\right)}{R_2C_2(R_0+R_1)\left(S+\frac{1}{(R_0+R_1)C_1}\right)S+\left(\frac{1}{R_2C_2}\right)}$$



NOTE: These component values are for the telephone channel circuit poles described in the text. The R2, C2 product can be provided with different values of R and C. R2 should be chosen to be equal to the termination resistor on Pin 1.

Figure 16. Improved Filter Configuration

Thus the two poles and the zero can be selected arbitrarily as long as the zero is at a higher frequency than the first pole. The values in Figure 16 represent one implementation of the telephony filter requirement.

The selection of the two–pole filter network effects the selection of the loop gain value and the minimum step size resistor. The required integrator current for a given change in voltage now becomes:

$$I_i = \frac{V_o}{R_0} + \left(\frac{R_2C_2}{R_0} + \frac{R_1C_1}{R_0} + C_1\right)\frac{\Delta V_o}{\Delta T} +$$

$$\left(R_2C_2C_1 + \frac{R_1C_1R_2C_2}{R_0}\right)\frac{\Delta V_o^2}{\Delta T^2}$$

The calculation of desired gain resistor R_X then proceeds exactly as previously described.

Syllabic Filter Design

The syllabic filter in Figure 14 is a simple single–pole network of 18 kΩ and 0.33 μF. This produces a 6.0 ms time constant for the averaging of the coincidence output signal. The voltage across the capacitor determines the integrator current which in turn establishes the step size. The integrator current and the resulting step size determine the companding ratio and the S/N performance. The companding ratio is defined as the voltage across C_S/V_{CC}.

The S/N performance may be improved by modifying the voltage to current transformation produced by R_X. If different portions of the total R_X are shunted by diodes, the integrator current can be other than $(V_{CC} - V_S)/R_X$. These breakpoint curves must be designed experimentally for the particular system application. In general, one would wish that the current would double with input level. To design the desired curve, supply current to Pin 4 of the codec from an external source. Input a signal level and adjust the current until the S/N performance is optimum. Then record the syllabic filter voltage and the current. Repeat this for all desired signal levels. Then derive the resistor diode network which produces that curve on a curve tracer.

Once the network is designed with the curve tracer, it is then inserted in place of R_X in the circuit and the forced optimum noise performance will be achieved from the active syllabic algorithm.

Diode breakpoint networks may be very simple or moderately complex and can improve the usable dynamic range of any codec. In the past they have been used in high performance telephone codecs.

Typical resistor–diode networks are shown in Figure 17.

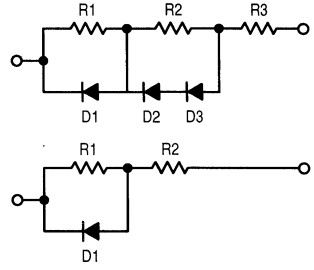


Figure 17. Resistor–Diode Networks

If the performance of more complex diode networks is desired, the circuit in Figure 18 should be used. It simulates the companding characteristics of nonlinear R_X elements in a different manner.

Output Low Pass Filter

A low pass filter is required at the receiving circuit output to eliminate quantizing noise. In general, the lower the bit rate, the better the filter must be. The filter in Figure 20 provides excellent performance for 12 kHz to 40 kHz systems.

TELEPHONE CARRIER QUALITY CODEC

Two specifications of the integrated circuit are specifically intended to meet the performance requirements of commercial telephone systems. First, slope polarity switch current matching is laser trimmed to guarantee proper idle channel performance with 5 mV minimum step size and a typical 1% current match from 15 μA to 3 mA. Thus a 300 to 1 range of step size variation is possible. Second, the MC3418 provides the four–bit algorithm currently used in subscriber loop telephone systems. With these specifications and the circuit of Figure 18, a telephone quality codec can be mass produced.

The circuit in Figure 18 provides a 30 dB S/Nc ratio over 50 dB of dynamic range for a 1 kHz test tone at a 37.7K bit rate. At 37.7K bits, 40 voice channels may be multiplexed on a standard 1.544 megabit T1 facility. This codec has also been tested for 10^{-7} error rates with asynchronous and synchronous data up to 2400 baud and for reliable performance with DTMF signaling. Thus, the design is applicable in telephone quality subscriber loop carrier systems, subscriber loop concentrators, and small PABX installations.

The Active Companding Network

The unique feature of the codec in Figure 18 is the step size control circuit which uses a companding ratio reference, the present step size, and the present syllabic filter output to establish the optimum companding ratios and step sizes for any given input level. The companding ratio of a CVSD codec is defined as the duty cycle of the coincidence output. It is the parameter measured by the syllabic filter and is the voltage across C_S divided by the voltage swing of the coincidence output. In Figure 18, the voltage swing of Pin 11 is 6.0 volts. The operating companding ratio is analoged by the voltage between Pins 10 and 4 by means of the virtual short across Pins 3 and 4 of the V to I op amp within the integrated circuit. Thus, the instantaneous companding ratio of the codec is always available at the negative input of A1.

The diode D1 and the gain of A1 and A2 provide a companding ratio reference for any input level. If the output of A2 is more than 0.7 volts below $V_{CC}/2$, then the positive input of A1 is ($V_{CC}/2$ – 0.7). The on diode drop at the input of A1 represents a 12% companding ratio (12% = 0.7 V/6.0 V).

The present step size of the operating codec is directly related to the voltage across R_X, which established the integrator current. In Figure 18, the voltage across R_X is amplified by the differential amplifier A2 whose output is single ended with respect to Pin 10 of the IC.

For large signal inputs, the step size is large and the output of A2 is lower than 0.7 volts. Thus D1 is fully on. The present step size is not a factor in the step size control. However, the difference between 12% companding ratio and the instantaneous companding ratio at Pin 4 is amplified by A1. The output of A1 changes the voltage across R_X in a direction which reduces the difference between the companding reference and the operating ratio by changing the step size. The ratio of R4 and R3 determines how closely the voltage at Pin 4 will be forced to 12%. The selection of R3 and R4 is initially experimental. However, the resulting companding control is dependent on R_X, R3, R4, and the full diode drop D1. These values are easy to reproduce from codec to codec.

For small input levels, the companding ratio reference becomes the output of A2 rather than the diode drop. The operating companding ratio on Pin 4 is then compared to a companding ratio smaller than 12% which is determined by the voltage drop across R_X and the gain of A2 and A1. The gain of A2 is also experimentally determined, but once determined, the circuitry is easily repeated.

With no input signal, the companding ratio at Pin 4 goes to zero and the voltage across R_X goes to zero. The voltage at the output of A2 becomes zero since there is no drop across R_X. With no signal input, the actively controlled step size vanished.

The minimum step size is established by the 500 k resistor between V_{CC} and $V_{CC}/2$ and is therefore independently selectable.

The signal to noise results of the active companding network are shown in Figure 19. A smooth 2 dB drop is realized from + 12 dBm to – 24 under the control of A1. At – 24 dBm, A2 begins to degenerate the companding reference and the resulting step size is reduced so as to extend the dynamic range of the codec by 20 dBm.

The slope overload characteristic is also shown. The active companding network produces improved performance with frequency. The 0 dBm slope overload point is raised to 4.8 kHz because of the gain available in controlling the voltage across R_X. The curves demonstrate that the level linearity has been maintained or improved.*

The codec in Figure 18 is designed specifically for 37.7K bit systems. However, the benefits of the active companding network are not limited to high bit rate systems. By modifying the crossover region (changing the gain of A2), the active technique may be used to improve the performance of lower bit rate systems.

The performance and repeatability of the codec in Figure 18 represents a significant step forward in the art and cost of CVSD codec designs.

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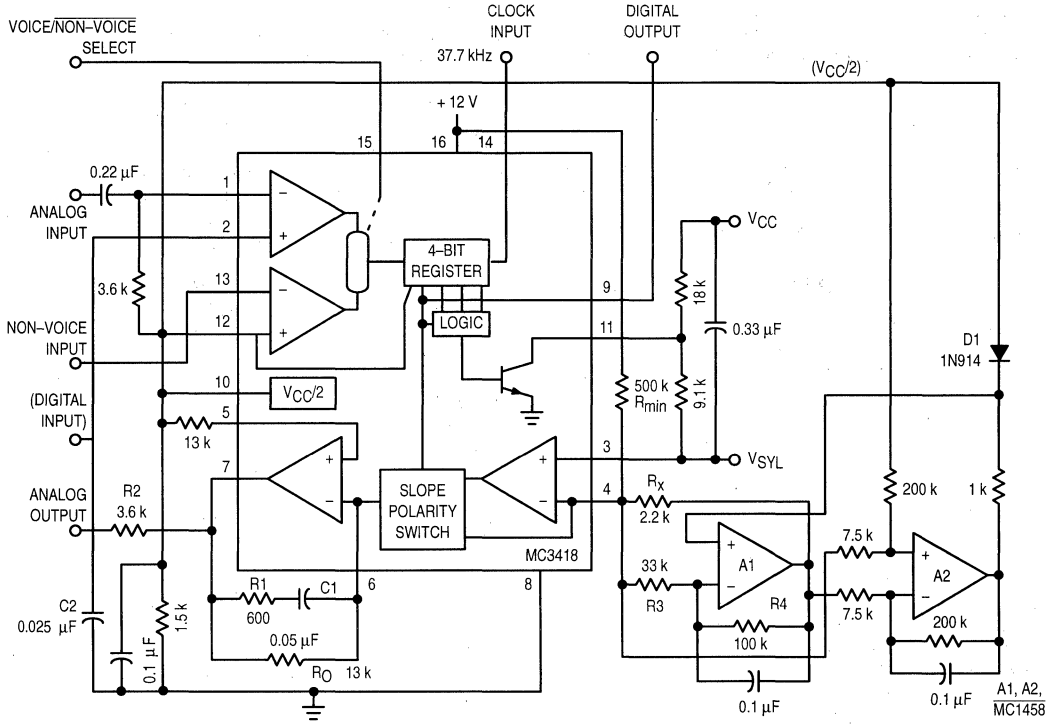
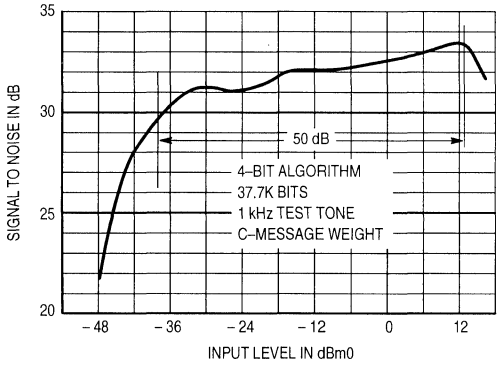
* A larger value for C2 is required in the decoder circuit than in the encoder to adjust the level linearity with frequency. In Figure 18, 0.050 μF would work well.

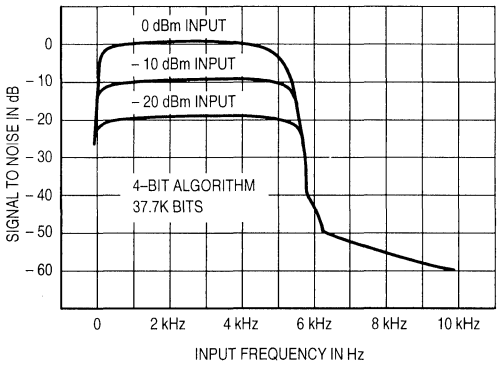


* Both double integration and active companding control are used to obtain improved CVSD performance. Laser trimming of the integrated circuit provides reliable idle channel and step size range characteristics.

Figure 18. Telephone Quality Delatmod Coder*



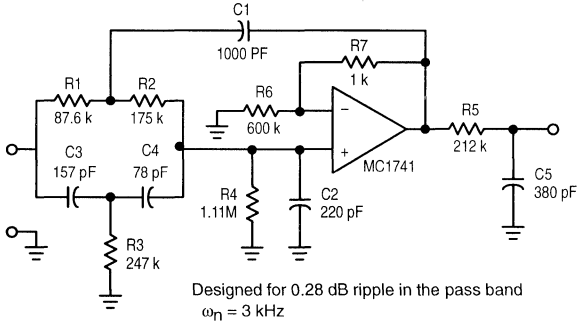
(a) Signal–to–Noise Performance of Telephony Quality Deltamodulator



(b) Frequency Response versus Input Level (Slope Overload Characteristic)

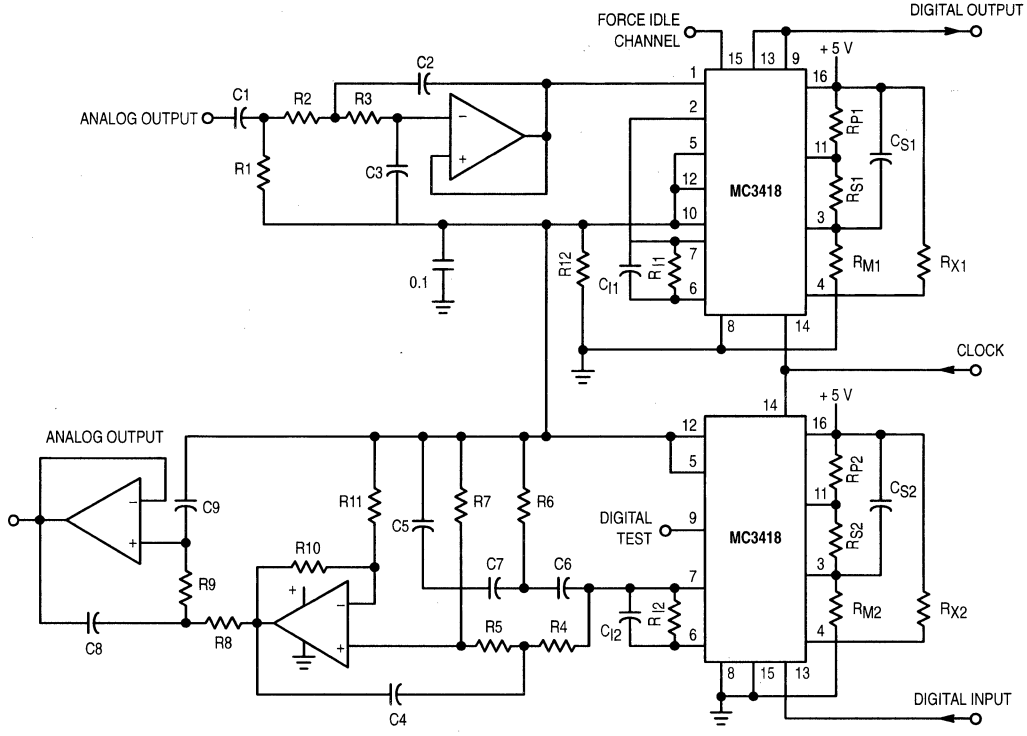
* Showing the improvement realized with the circuit in Figure 18.

Figure 19. Signal–to–Noise Performance and Frequency Response*



Designed for 0.28 dB ripple in the pass band
ω_n = 3 kHz
ω_S = ≅ 6 kHz
AdB at ω_S and above 29.5 dB

Figure 20. High Performance Elliptic Filter for CVSD Output



Codec Components

R_{X1}, R_{X2} – 3.3 kΩ
R_{P1}, R_{P2} – 3.3 kΩ
R_{S1}, R_{S2} – 100 kΩ
R_{I1}, R_{I2} – 20 kΩ
R_{12} – 1 kΩ

R_{M1}, R_{M2} – 15 MΩ
Minimum step size = 6 mV

C_{S1}, C_{S2} – 0.05 µF
C_{I1}, C_{I2} – 0.05 µF

2 MC3418
1 MC3403 (or MC3406)

NOTE: All Res. 5%
All Cap. 5%

Input Filter Specifications

12 dB/Octave Rolloff above 3.3 kHz
6 db/Octave Rolloff below 50 Hz

Output Filter Specifications

Break Frequency – 3.3 kHz
Stop Band – 9 kHz
Stop Band Atten. – 50 dB
Rolloff – > 40 dB/Octave

Filter Components

R1 – 965 Ω
R2 – 72 kΩ
R3 – 72 kΩ
R4 – 63.46 kΩ
R5 – 127 kΩ
R6 – 365.5 kΩ
R7 – 1.645 MΩ
R8 – 72 kΩ
R9 – 72 kΩ
R10 – 29.5 Ω
R11 – 72 kΩ

C1 – 3.3 µF
C2 – 837 pF
C3 – 536 pF
C4 – 1000 pF
C5 – 222 pF
C6 – 77 pF
C7 – 38 pF
C8 – 837 pF
C9 – 536 pF

NOTE: All Res. 0.1% to 1%
All Cap. 0.1%

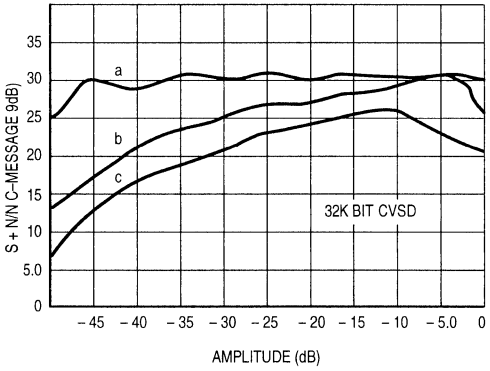
Figure 21. Full Duplex/32K Bit CVSD Voice Codec

COMPARATIVE CODEC PERFORMANCE

The salient feature of CVSD codecs is versatility. The range of codec complexity tradeoffs and bit rate is so wide that one cannot grasp the interdependency of parameters for voice applications in a few pages.

Design of a specific codec must be tailored to the digital channel bandwidth, the analog bandwidth, the quality of signal transmission required, and the cost objectives. To illustrate the choices available, the data in Figure 22 compares the signal–to–noise ratios and dynamic range of various codec design options at 32K bits. Generally, the relative merits of each design feature will remain intact in any application. Lowering the bit rate will reduce the dynamic range and noise performance of all techniques. As the bit rate is increased, the overall performance of each technique will improve and the need for more complex designs diminishes.

Non–voice applications of the MC3418 are also possible. In those cases, the signal bandwidth and amplitude characteristics must be defined before the specification of codec parameters can begin. However, in general, the design can proceed along the lines of the voice applications shown here, taking into account the different signal bandwidth requirements.



These curves demonstrate the improved performance obtained with several codec designs of varying complexity.

Curve a — Complex companding and double integration (Figure 18)

Curve b — Double integration (Figure 14 using Figure 16)

Curve c — Single integration (Figure 14) with 6.0 mV step size

Figure 22. Comparative Codec Performance — Signal–to–Noise Ratio for 1 kHz Test Tone

2

MOTOROLA

MC13055

Advance Information

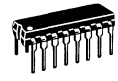
Wideband FSK Receiver

The MC13055 is intended fo RF data link systems using carrier frequencies up to 40 MHz and FSK (frequency shift keying) data rates up to 2.0 M Baud (1.0 MHz). This design is similar to the MC3356, except that it does not include the oscillator/mixer. The IF bandwidth has been increased and the detector output has been revised to a balanced configuration. The received signal strength metering circuit has been retained, as has the versatile data slicer/comparator.

- Input Sensitivity 20 μV @ 40 MHz
- Signal Strength Indicator Linear Over 3 Decades
- Available in Surface Mount Package
- Easy Application, Few Peripheral Components

WIDEBAND FSK RECEIVER

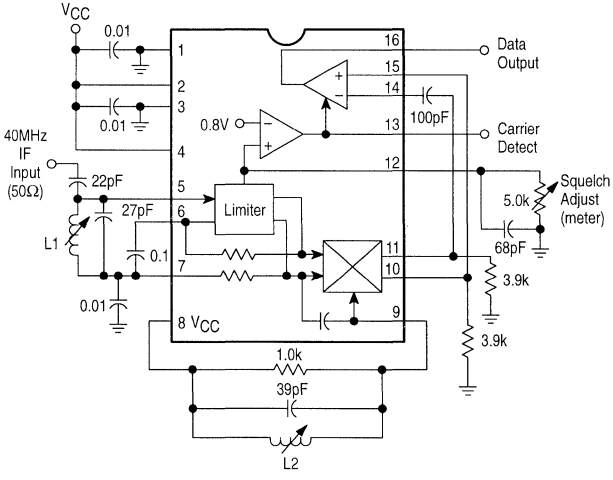
SEMICONDUCTOR TECHNICAL DATA



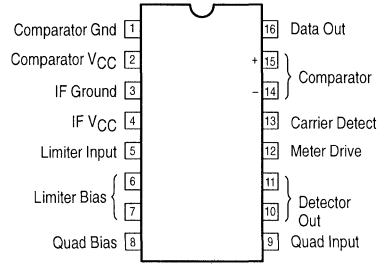
P SUFFIX
PLASTIC PACKAGE
CASE 648

D SUFFIX
PLASTIC PACKAGE
CASE 751B
(SO–16)

Figure 1. Block Diagram and Application Circuit



PIN CONNECTIONS



ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC13055D	T_A = – 40 to +85°C	SO–16
MC13055P		Plastic DIP

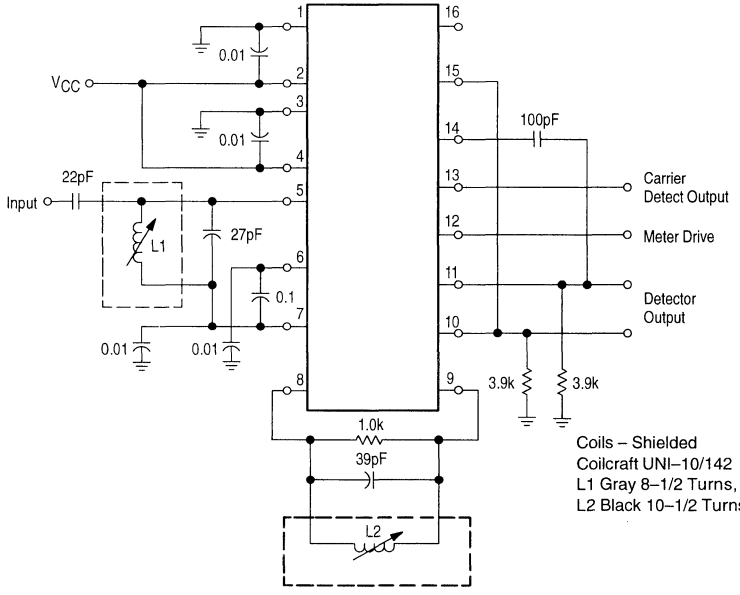
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	$V_{CC(max)}$	15	Vdc
Operating Supply Voltage Range	V2, V4	3.0 to 12	Vdc
Junction Temperature	T_J	150	°C
Operating Ambient Temperature Range	T_A	–40 to +85	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Power Dissipation, Package Rating	P_D	1.25	W

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 Vdc, f_o = 40 MHz, f_{mod} = 1.0 MHz, Δf = ±1.0 MHz, T_A = 25°C, test circuit of Figure 2.)

Characteristics		Measure	Min	Typ	Max	Unit
Total Drain Current		12 + 14	–	20	25	mA
Data Comparator Pull–Down Current		I16	–	10	–	mA
Meter Drive Slope versus Input		I12	4.5	7.0	9.0	µA/dB
Carrier Detect Pull–Down Current		I13	–	1.3	–	mA
Carrier Detect Pull–Up Current		I13	–	500	–	µA
Carrier Detect Threshold Voltage		V12	700	800	900	mV
DC Output Current		I10, I11	–	430	–	µA
Recovered Signal		V10 – V11	–	350	–	mVrms
Sensitivity for 20 dB S + N/N, BW = 5.0 MHz		VIN	–	20	–	µVrms
S + N/N at V_{in} = 50 µV		V10 – V11	–	30	–	dB
Input Impedance @ 40 MHz	R_{in} C_{in}	Pin 5, Ground	– –	4.2 4.5	– –	kΩ pF
Quadrature Coil Loading	R_{in} C_{in}	Pin 9 to 8	– –	7.6 5.2	– –	kΩ pF

Figure 2. Test Circuit



Coils – Shielded
Coilcraft UNI–10/142
L1 Gray 8–1/2 Turns, nominal 300 nH
L2 Black 10–1/2 Turns, nominal 380 nH

Figure 3. Overall Gain, Noise, AM Rejection

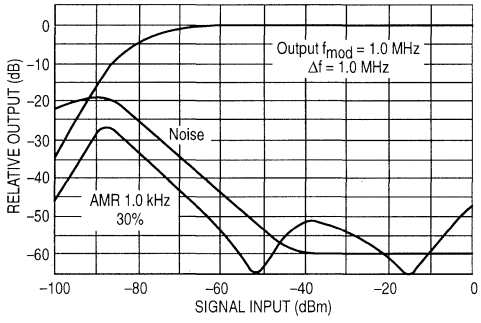


Figure 4. Meter Current versus Signal

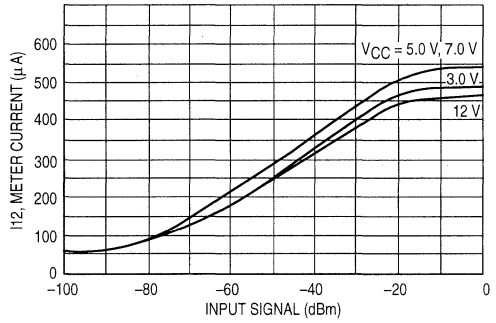


Figure 5. Untuned Input: Limiting Sensitivity versus Frequency

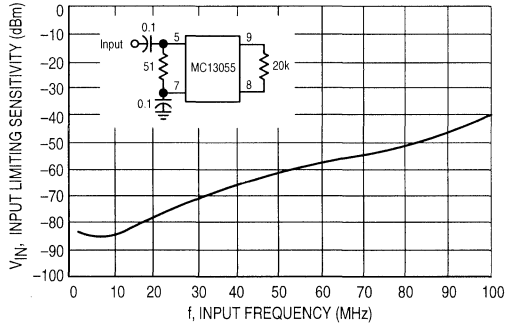


Figure 6. Untuned Input: Meter Current versus Frequency

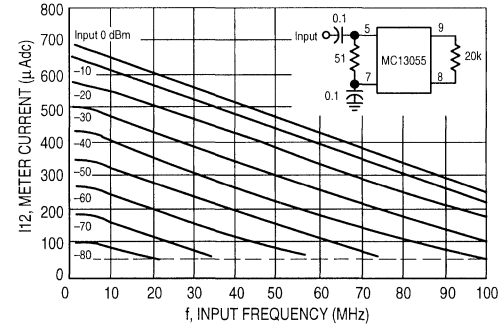


Figure 7. Limiting Sensitivity and Detuning versus Supply Voltage

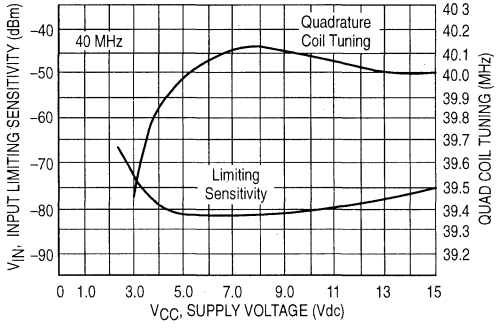


Figure 8. Detector Current and Power Supply Current versus Supply Voltage

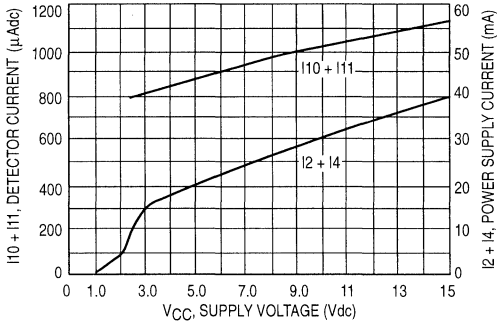


Figure 9. Recovered Audio versus Temperature

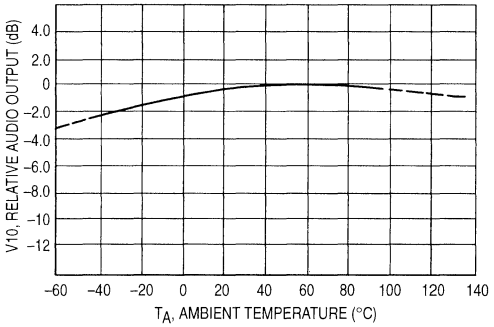


Figure 10. Carrier Detect Threshold versus Temperature

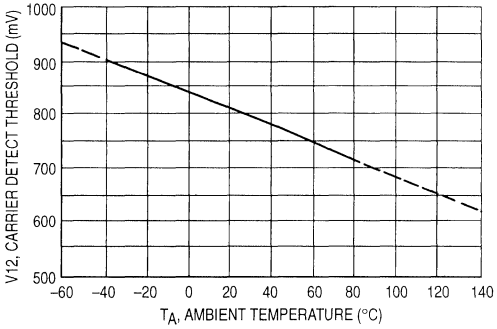


Figure 11. Meter Current versus Temperature

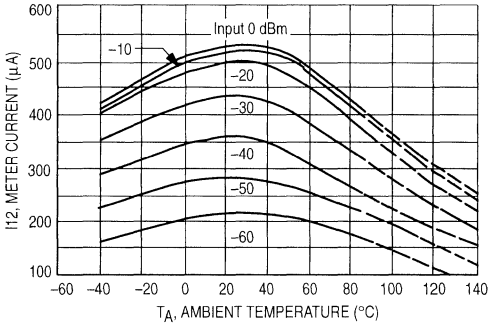


Figure 12. Input Limiting versus Temperature

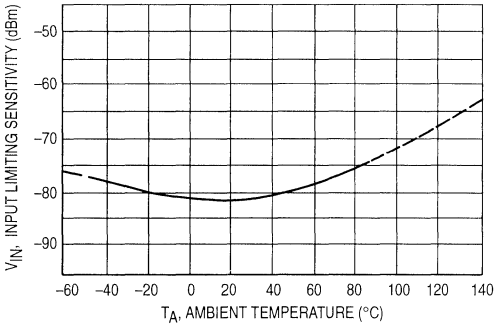


Figure 13. Input Impedance, Pin 5

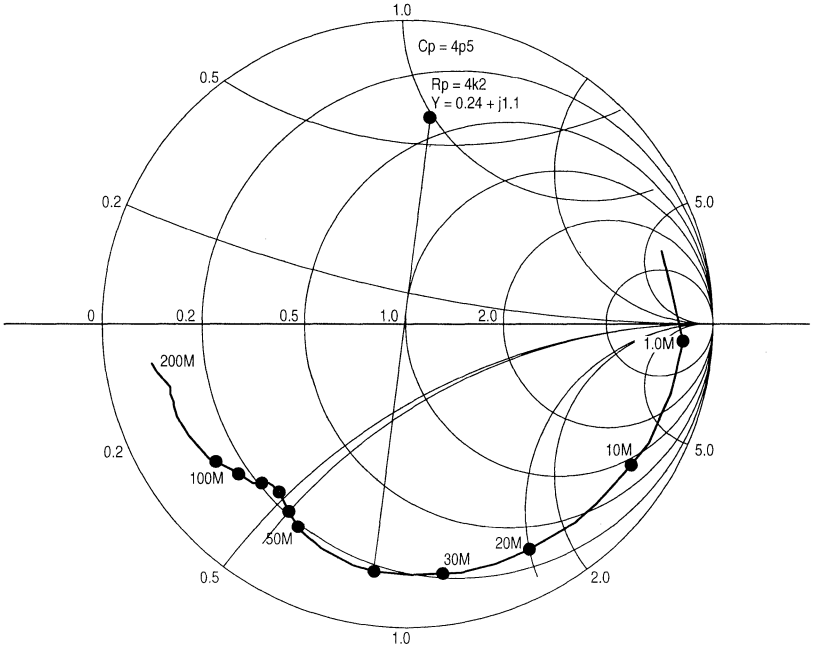
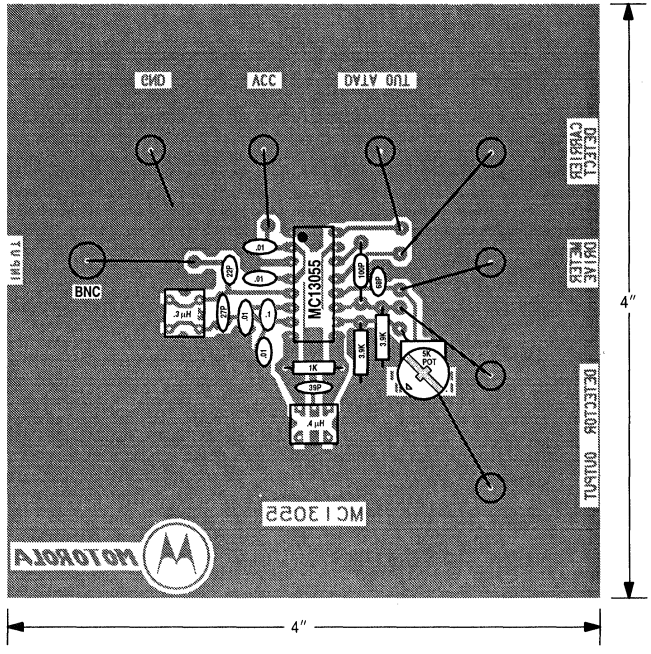


Figure 14. Test Fixture
(Component Layout)



(Circuit Side View)

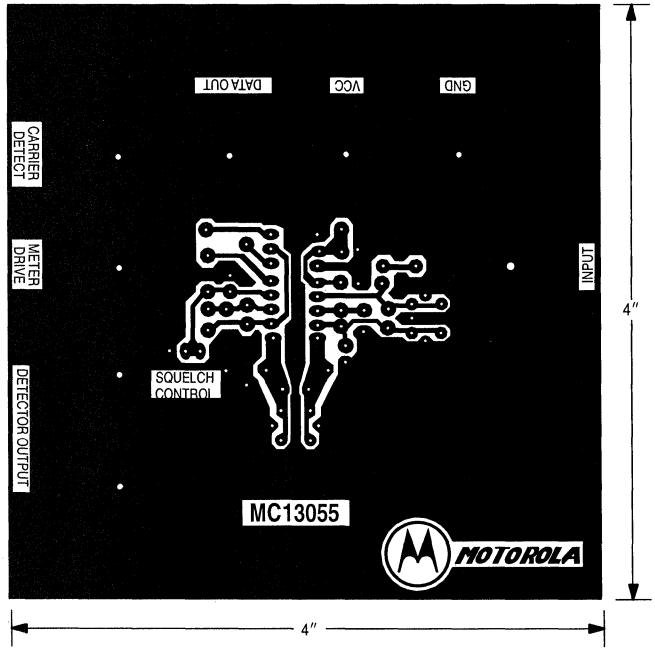
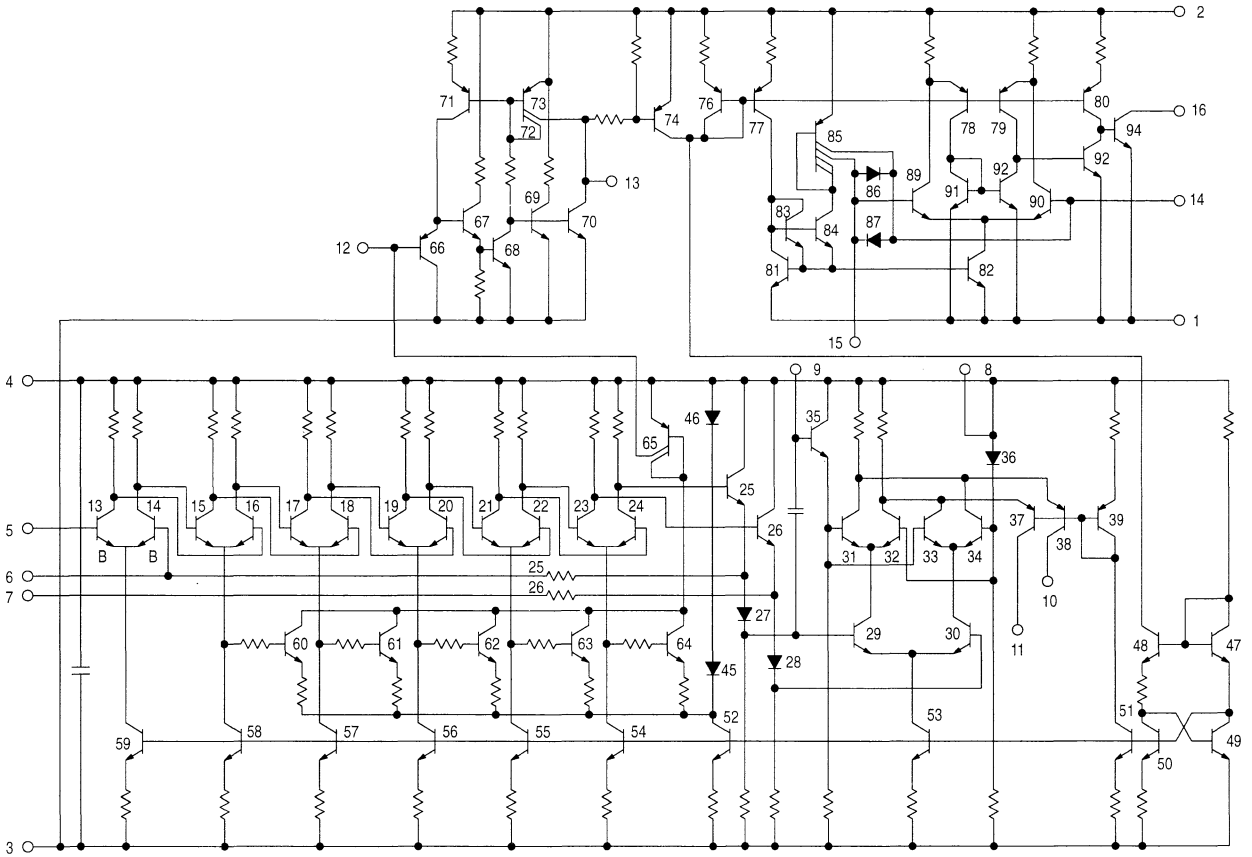


Figure 15. Internal Schematic



GENERAL DESCRIPTION

The MC13055 is an extended frequency range FM IF, quadrature detector, signal strength detector and data shaper. It is intended primarily for FSK data systems. The design is very similar to MC3356 except that the oscillator/mixer has been removed, and the frequency capability of the IF has been raised about 2:1. The detector output configuration has been changed to a balanced, open–collector type to permit symmetrical drive of the data shaper (comparator). Meter drive and squelch features have been retained.

The limiting IF is a high frequency type, capable of being operated up to 100 MHz. It is expected to be used at 40 MHz in most cases. The quadrature detector is internally coupled to the IF, and a 2.0 pF quadrature capacitor is internally provided. The 20 dB quieting sensitivity is approximately 20 μV, tuned input, and the IF can accept signals up to 220 mVrms without distortion or change of detector quiescent DC level.

The IF is unusual in that each of the last 5 stages of the 6 stage limiter contains a signal strength sensitive, current sinking device. These are parallel connected and buffered to produce a signal strength meter drive which is fairly linear for IF input signals of 20 μV to 20 mVrms (see Figure 4).

A simple squelch arrangement is provided whereby the meter current flowing through the meter load resistance flips a comparator at about 0.8 Vdc above ground. The signal strength at which this occurs can be adjusted by changing the meter load resistor. The comparator (+) input and output are available to permit control of hysteresis. Good positive action can be obtained for IF input signals of above 20 μVrms. A resistor (R) from Pin 13 to Pin 12 will provide V_{CC}/R of feedback current. This current can be correlated to an amount of signal strength hysteresis by using Figure 4.

The squelch is internally connected to the data shaper. Squelch causes the data shaper to produce a high (V_{CC}) output.

The data shaper is a complete "floating" comparator, with diodes across its inputs. The outputs of the quadrature detector can be fed directly to either or preferably both inputs of the comparator to produce a squared output swinging from V_{CC} to ground in inverted or noninverted form.

MC13109

Advance Information

Universal Cordless Telephone Subsystem IC

UNIVERSAL CT–1 SUBSYSTEM INTEGRATED CIRCUIT

The MC13109 integrates several of the functions required for a cordless telephone into a single integrated circuit. This significantly reduces component count, board space requirements, and external adjustments. It is designed for use in both the handset and the base.

- Dual Conversion FM Receiver
  - Complete Dual Conversion Receiver – Antenna Input to Audio Output 80 MHz Maximum Carrier Frequency
  - RSSI Output
  - Carrier Detect Output with Programmable Threshold
  - Comparator for Data Recovery
  - Operates with Either a Quad Coil or Ceramic Discriminator
- Compander
  - Expandor Includes Mute, Digital Volume Control and Speaker Driver
  - Compressor Includes Mute, ALC and Limiter
- Dual Universal Programmable PLL
  - Supports New 25 Channel U.S. Standard with No External Switches
  - Universal Design for Domestic and Foreign CT–1 Standards
  - Digitally Controlled Via a Serial Interface Port
  - Receive Side Includes 1st LO VCO, Phase Detector, and 14–Bit Programmable Counter and 2nd LO with 12–Bit Counter
  - Transmit Section Contains Phase Detector and 14–Bit Counter
  - MPU Clock Output Eliminates Need for MPU Crystal
- Supply Voltage Monitor
  - Externally Adjustable Trip Point
- 2.0 to 5.5 V Operation with One–Third the Power Consumption of Competing Devices

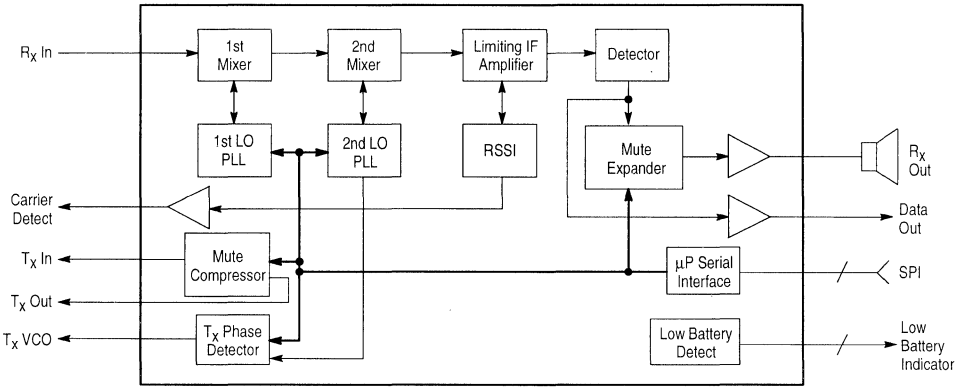
FB SUFFIX
PLASTIC PACKAGE
CASE 848B
(QFP–52)

FTA SUFFIX
PLASTIC PACKAGE
CASE 932
(Thin QFP)

ORDERING INFORMATION

Device	Tested Operating Temperature Range	Package
MC13109FB	T_A = – 40° to +85°C	QFP–52
MC13109FTA		TQFP–48

Simplified Block Diagram



This device contains 6,609 active transistors.

Figure 1. MC13109FB Test Circuit

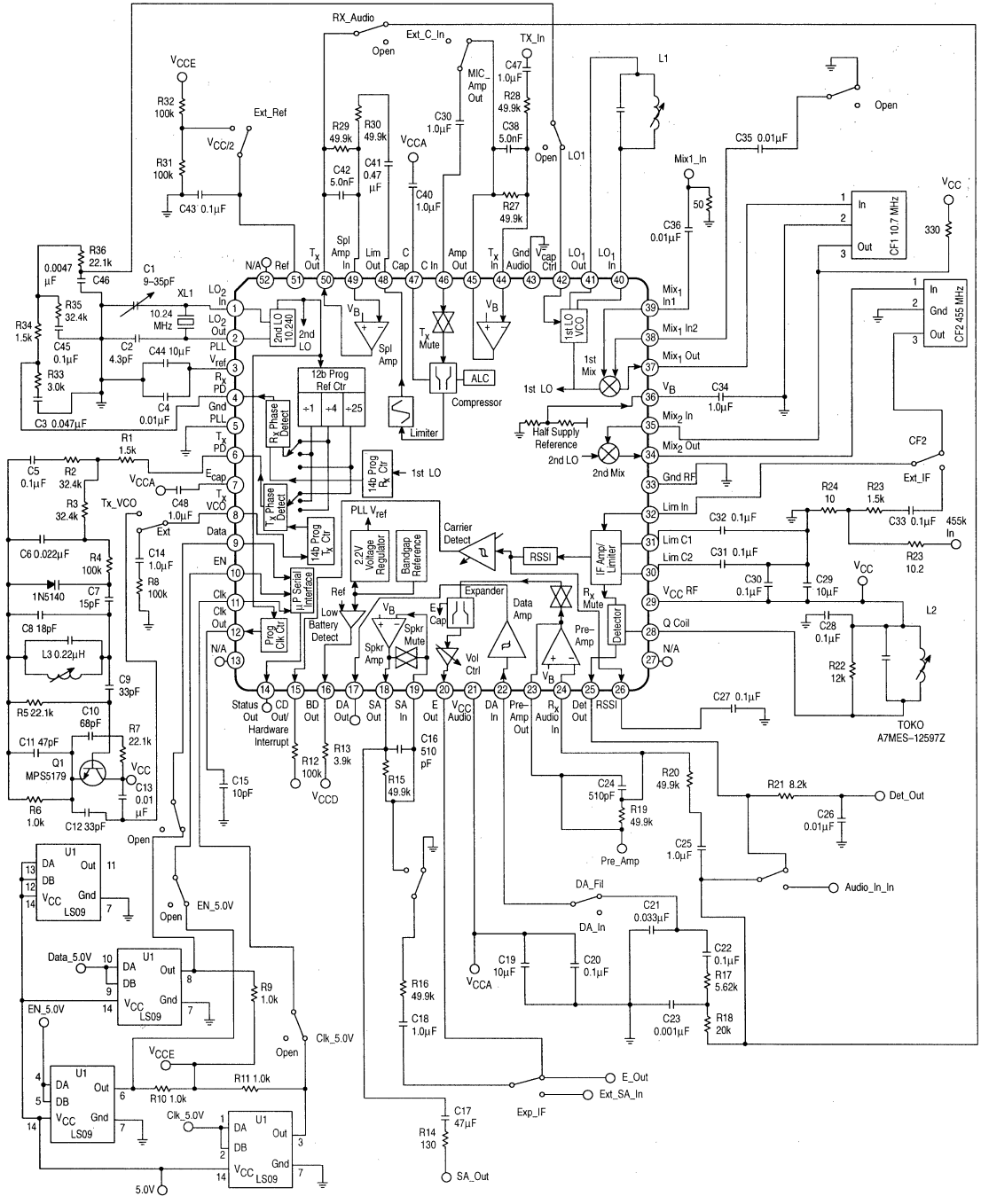
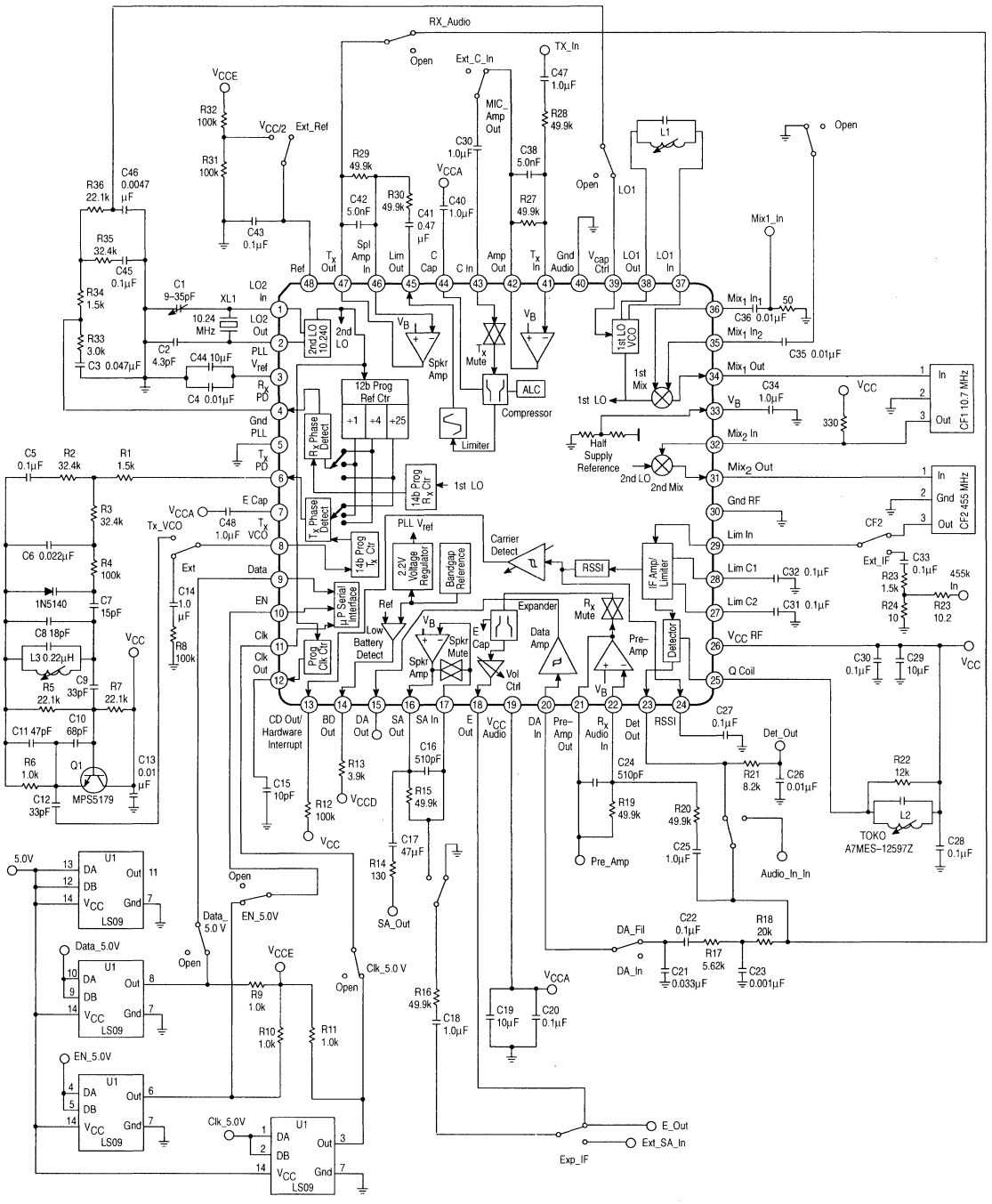


Figure 2. MC13109FTA Test Circuit



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.5 to +5.5	Vdc
Junction Temperature	T_J	−65 to +150	°C

NOTE: Devices should not be operated at these limits. The "Recommended Operating Conditions" provide for actual device operation.

RECOMMENDED OPERATING CONDITIONS

Characteristic	Min	Typ	Max	Unit
V_{CC}	2.0	–	5.5	Vdc
Operating Ambient Temperature	−40	–	85	°C

NOTE: All limits are not necessarily functional concurrently.

ELECTRICAL CHARACTERISTICS (V_{CC} = 2.6 V, T_A = 25°C, RF In = 46.61 MHz, f_{DEV} = ±3.0 kHz, f_{mod} = 1.0 kHz; Test Circuit Figure 1.)

Characteristic	Min	Typ	Max	Unit
POWER SUPPLY				
Static Current				
Active Mode (V_{CC} = 2.6 V)	–	6.7	12	mA
Active Mode (V_{CC} = 3.6 V)	–	7.1	–	mA
Receive Mode (V_{CC} = 2.6 V)	–	4.3	7.0	mA
Receive Mode (V_{CC} = 3.6 V)	–	4.5	–	mA
Standby Mode (V_{CC} = 2.6 V)	–	300	600	µA
Standby Mode (V_{CC} = 3.6 V)	–	600	–	µA
Inactive Mode (V_{CC} = 2.6 V)	–	40	80	µA
Inactive Mode (V_{CC} = 3.6 V)	–	56	–	µA

ELECTRICAL CHARACTERISTICS (continued)

FM Receiver

The FM receivers can be used with either a quad coil or a ceramic resonator. The FM receiver and 1st LO have been designed to work for all country channels, including 25 channel U.S., without the need for any external switching circuitry (see Figure 29).

(Test Conditions: V_{CC} = 2.6 V, T_A = 25°C, f_O = 46.61 MHz, f_{DEV} = ±3.0 kHz, f_{mod} = 1.0 kHz.)

Characteristic	Condition	Input Pin	Measure Pin	Symbol	Min	Typ	Max	Unit
Sensitivity (Input for 12 dB SINAD)	Matched Impedance Differential Input	Mix_1 $In_{1/2}$	Det Out	V_{SIN}	–	0.7	–	µVrms
1st Mixer Conversion Gain	V_{in} = 1.0 mVrms, with CF_1 Load	Mix_1 $In_{1/2}$	CF_1	MX_{gain1}	–	10	–	dB
2nd Mixer Conversion Gain	V_{in} = 3.0 mVrms, with CF_2 Load	Mix_2 In	CF_2	MX_{gain2}	–	20	–	dB
1st and 2nd Mixer Gain Total	V_{in} = 1.0 mVrms, with CF_1 and CF_2 Load	Mix_1 $In_{1/2}$	CF_2	MX_{gainT}	24	30	–	dB
1st Mixer Input Impedance	–	–	Mix_1 In_1 Mix_1 In_2	Z_{in1}	–	1.0	–	kΩ
2nd Mixer Input Impedance	–	–	Mix_2 In	Z_{in2}	–	3.0	–	kΩ
1st Mixer Output Impedance	–	–	Mix_1 Out	Z_{out1}	–	330	–	Ω
2nd Mixer Output Impedance	–	–	Mix_2 Out	Z_{out2}	–	1.5	–	kΩ
IF –3.0 dB Limiting Sensitivity	f_{in} = 455 kHz	Lim In	Det Out	IF Sens	–	55	–	µVrms
Total Harmonic Distortion (CCITT Filter)	With R_C = 8.2 kΩ/ 0.01 µF Filter at Det Out	Mix_1 $In_{1/2}$	Det Out	THD	–	0.7	–	%
Recovered Audio	With R_C = 8.2 kΩ/ 0.01 µF Filter at Det Out	Mix_1 $In_{1/2}$	Det Out	AFO	80	100	154	mVrms
Demodulator Bandwidth	–	Lim In	Det Out	BW	–	20	–	kHz
Signal to Noise Ratio	V_{in} = 10 mVrms, R_C = 8.2 kΩ/0.01 µF	Mix_1 $In_{1/2}$	Det Out	SN	–	49	–	dB
AM Rejection Ratio	30% AM, V_{in} = 10 mVrms, R_C = 8.2 kΩ/0.001 µF	Mix_1 $In_{1/2}$	Det Out	AMR	–	37	–	dB
First Mixer 3rd Order Intercept (Input Referred)	Matched Impedance Input	Mix_1 $In_{1/2}$	Mix_1 Out	TOI_{mix1}	–	–10	–	dBm
Second Mixer 3rd Order Intercept (Input Referred)	Matched Impedance Input	Mix_2 In	Mix_2 Out	TOI_{mix2}	–	–27	–	dBm
Detector Output Impedance	–	–	Det Out	Z_O	–	870	–	Ω

ELECTRICAL CHARACTERISTICS (continued)

RSSI/Carrier Detect

Connect 0.01 µF to Gnd from "RSSI" output pin to form the carrier detect filter. "CD Out" is an open collector output which requires an external 100 kΩ pull–up resistor to V_{CC}. The carrier detect threshold is programmable through the MPU interface.

(R_L = 100 kΩ, V_{CC} = 2.6 V, T_A = 25°C.)

Characteristic	Condition	Input Pin	Measure Pin	Symbol	Min	Typ	Max	Unit
RSSI Output Current Dynamic Range	–	Mix_1 In	RSSI	RSSI	–	65	–	dB
Carrier Sense Threshold	CD Threshold Adjust = (10100)	Mix_1 In	CD Out	V_T	–	22.5	–	µVrms
Hysteresis	–	Mix1 In	CD Out	Hys	–	2.0	–	dB
Output High Voltage	V_{in} = 0 µVrms, R_L = 100 kΩ, CD = (10100)	Mix_1 In	CD Out	V_{OH}	V_{CC} – 0.1	2.6	–	V
Output Low Voltage	V_{in} = 100 µVrms, R_L = 100 kΩ, CD = (10100)	Mix_1 In	CD Out	V_{OL}	–	0.01	0.4	V
Carrier Sense Threshold Adjustment Range	Programmable through MPU Interface	–	–	V_{Trange}	–20	–	11	dB
Carrier Sense Threshold – Number of Steps	Programmable through MPU Interface	–	–	V_{Tn}	–	32	–	–

Data Amp Comparator (see Figure 4)

Inverting hysteresis comparator. Open collector output with internal 100 kΩ pull–up resistor. A band pass filter is connected between the "Det Out" pin and the "DA In" pin with component values as shown in the attached block diagram. The "DA In" input signal is ac coupled.

(V_{CC} = 2.6 V, T_A = 25°C)

Characteristic	Condition	Input Pin	Measure Pin	Symbol	Min	Typ	Max	Unit
Hysteresis	–	DA In	DA Out	Hys	30	40	50	mV
Threshold Voltage	–	DA In	DA Out	V_T	V_{CC} – 0.9	V_{CC} – 0.7	V_{CC} – 0.5	V
Input Impedance	–	–	DA In	Z_I	–	11	–	kΩ
Output Impedance	–	–	DA Out	Z_O	–	100	–	kΩ
Output High Voltage	V_{in} = V_{CC} – 1.0 V, I_{OH} = 0 mA	DA In	DA Out	V_{OH}	V_{CC} – 0.1	2.6	–	V
Output Low Voltage	V_{in} = V_{CC} – 0.4 V, I_{OL} = 0 mA	DA In	DA Out	V_{OL}	–	0.03	0.4	V

ELECTRICAL CHARACTERISTICS (continued)

Pre–Amplifier/Expander/R_x Mute/Volume Control (See Figure 5)

The Pre–Amplifier is an inverting rail–to–rail output swing operational amplifier with the non–inverting input terminal connected to the internal V_B half supply reference. External resistors and capacitors can be connected to set the gain and frequency response. The expander analog ground is set to the half supply reference so the input and output swing capability will increase as the supply voltage increases. The volume control can be adjusted through the MPU interface. The "R_x Audio In" input signal is ac coupled.

(Test Conditions: V_{CC} = 2.6 V, T_A = 25°C, f_{in} = 1.0 kHz, Set External Pre–Amplifier R's for Gain of 1, Volume Control = (0111).)

Characteristic	Condition	Input Pin	Measure Pin	Symbol	Min	Typ	Max	Unit
Pre–Amp Open Loop Gain	–	R_x Audio In	Pre–Amp	A_{VOL}	–	60	–	dB
Pre–Amp Gain Bandwidth	–	R_x Audio In	Pre–Amp	GBW	–	100	–	kHz
Pre–Amp Maximum Output Swing	R_L = 10 kΩ	R_x Audio In	Pre–Amp	V_{Omax}	–	V_{CC} – 0.3	–	V_{pp}
Expander 0 dB Gain Level	V_{in} = –10 dBV	R_x Audio In	E Out	G	–3.0	–0.11	3.0	dB
Expander Gain Tracking	V_{in} = –20 dBV, Output Relative to G V_{in} = –30 dBV, Output Relative to G	R_x Audio In	E Out	G_t	–21 –42	–19.65 –39.42	–19 –37	dB
Total Harmonic Distortion	V_{in} = –10 dBV	R_x Audio In	E Out	THD	–	0.5	–	%
Maximum Output Voltage	Increase input voltage until output voltage THD = 5%, then measure output voltage. R_L = 10 kΩ	R_x Audio In	E Out	V_{Omax}	–	–5.0	–	dBV
Attack Time	E_{cap} = 1.0 µF, R_{filt} = 20 kΩ (See Appendix B)	R_x Audio In	E Out	t_a	–	3.0	–	ms
Release Time	E_{cap} = 1.0 µF, R_{filt} = 20 kΩ (See Appendix B)	R_x Audio In	E Out	t_r	–	13.5	–	ms
Compressor to Expander Crosstalk	V (R_x Audio In) = 0 Vrms, V_{in} = –10 dBV	C In	E Out	C_T	–	–	–70	dB
R_x Mute	V_{in} = –10 dBV No popping detectable during R_x Mute transitions	R_x Audio In	E Out	M_e	–	–70	–	dB
Volume Control Range	Programmable through MPU Interface	–	–	V_{Crange}	–14	–	16	dB
Volume Control Steps	Programmable through MPU Interface	–	–	V_{Cn}	–	16	–	–

ELECTRICAL CHARACTERISTICS (continued)

Speaker Amplifier/SP Mute

The Speaker Amplifier is an inverting rail–to–rail operational amplifier. The non–inverting input terminal is connected to the internal V_B half supply reference. External resistors and capacitors are used to set the gain and frequency response. The "SA In" input is ac coupled.

(Test Conditions: V_{CC} = 2.6 V, T_A = 25°C, f_{in} = 1.0 kHz, External Resistors Set for Gain of 1.)

Characteristic	Condition	Input Pin	Measure Pin	Symbol	Min	Typ	Max	Unit
Maximum Output Swing	V_{CC} = 2.3 V, R_L = 130 Ω	SA In	SA Out	V_{Omax}	–	0.8	–	V_{pp}
	V_{CC} = 2.3 V, R_L = 600 Ω				–	2.0	–	
	V_{CC} = 3.4 V, R_L = 600 Ω				–	3.0	–	
SP Mute	V_{in} = –20 dBV R_L = 130 Ω No popping detectable during SP Mute transitions	SA In	SA Out	M_{sp}	–	–70	–	dB

Mic Amplifier (See Figure 7)

The Mic Amplifier is an inverting rail–to–rail output operational amplifier with the non–inverting input terminal connected to the internal V_B half supply reference. External resistors and capacitors are connected to set the gain and frequency response. The "T_X In" input is ac coupled.

(Test Conditions: V_{CC} = 2.6 V, T_A = 25°C, f_{in} = 1.0 kHz, External Resistors Set for Gain of 1.)

Characteristic	Condition	Input Pin	Measure Pin	Symbol	Min	Typ	Max	Unit
Open Loop Gain	–	T_X In	Amp Out	A_{VOL}	–	60	–	dB
Gain Bandwidth	–	T_X In	Amp Out	G_{BW}	–	100	–	kHz
Maximum Output Swing	R_L = 10 kΩ	T_X In	Amp Out	V_{Omax}	–	V_{CC} – 0.3	–	V_{pp}

ELECTRICAL CHARACTERISTICS (continued)

Compressor/ALC/T_X Mute/Limiter (See Figure 6)

The compressor analog gound is set to the half supply reference so the input and output swing capability will increase as the supply voltage increases. The "C In" input is ac coupled. The ALC (Automatic Level Control) provides a soft limit to the output signal swing as the input voltage increases slowly (i.e., a sine wave is maintained). The Limiter circuit limits rapidly changing signal levels by clipping the signal peaks. The ALC and/or Limiter can be disabled through the MPU serial interface.

(Test Conditions: V_{CC} = 2.6 V, f_{in} = 1.0 kHz, T_A = 25°C.)

Characteristic	Condition	Input Pin	Measure Pin	Symbol	Min	Typ	Max	Unit
Compressor 0 dB Gain Level	V_{in} = –10 dBV, ALC disabled, Limiter disabled	C In	Lim Out	G	–3.0	–0.17	3.0	dB
Compressor Gain Tracking	V_{in} = –30 dBV, Output Relative to G	C In	Lim Out	G_t	–11	–10.23	–9.0	dB
	V_{in} = –50 dBV, Output Relative to G				–23	–20.23	–17	
Maximum Compressor Gain	V_{in} –70 dBV	C In	Lim Out	A_{Vmax}	–	30	–	dB
Total Harmonic Distortion	V_{in} –10 dBV, ALC disabled, Limiter disabled	C In	Lim Out	THD	–	0.5	–	%
Input Impedance	–	C In	Lim Out	Z_{in}	–	16	–	kΩ
Attack Time	C_{cap} = 1.0 µF, R_{filt} = 20 kΩ (see Appendix B)	C In	Lim Out	t_a	–	3.0	–	ms
Release Time	C_{cap} = 1.0 µF, R_{filt} = 20 kΩ (see Appendix B)	C In	Lim Out	t_r	–	13.5	–	ms
Expander to Compressor Crosstalk	V (C In) = 0 Vrms, V_{in} = –10 dBV	R_X Audio In	Lim Out	C_T	–	–	–40	dB
T_X Data Mute	V_{in} = –10 dBV, ALC disabled No popping detectable during R_X Mute transitions	C In	Lim Out	M_e	–	–70	–	dB
ALC Dynamic Range	–	C In	Lim Out	DR	–24	–	–2.5	dBV
ALC Output Level	V_{in} = –18 dBV	C In	Lim Out	ALC_{out}	–	–16	–	dBV
	V_{in} = –2.5 dBV				–	–12	–	
Limiter Output Level	ALC disabled	C In	T_X Out	V_{lim}	–	0.8	–	V_{pp}

Splatter Amplifier (see Figure 7)

The Splatter Amplifier is an inverting rail–to–rail output operational amplifier with the non–inverting input terminal connected to the internal V_B half supply reference. External resistors and capacitors can be connected to set the gain and frequency response. The "Spl Amp In" input is ac coupled.

(Test Conditions: V_{CC} = 2.6 V, T_A = 25°C, f_{in} = 1.0 kHz, External resistors Set for Gain of 1.)

Characteristic	Condition	Input Pin	Measure Pin	Symbol	Min	Typ	Max	Unit
Open Loop Gain	–	Spl Amp In	T_X Out	A_{VOL}	–	60	–	dB
Gain Bandwidth	–	Spl Amp In	T_X Out	GBW	–	100	–	kHz
Maximum Output Swing	R_L = 10 kΩ	Spl Amp In	T_X Out	V_{Omax}	–	V_{CC} – 0.3	–	V_{pp}

T_X Audio Path Recommendation

The recommended configuration for the T_X Audio path includes setting the Microphone Amplifier gain to 16 dB using the external gain setting resistors and setting the Splatter Amplifier gain to 9.0 dB using the external gain setting resistors. With these gain values, the total T_X Path transfer characteristic is shown in Figure 7.

PLL Voltage Regulator

The PLL supply voltage is regulated to a nominal of 2.2 V. The "V_{CC} Audio" pin is the supply voltage for the internal voltage regulator. The "PLL V_{ref}" pin is the 2.2 V regulated output voltage. Two capacitors with 10 µF and 0.01 µF values must be connected to the "PLL V_{ref}" pin to filter and stabilize this regulated voltage. The voltage regulator provides power for the 2nd LO, R_X and T_X PLL's, and MPU Interface. The voltage regulator can also be used to provide a regulated supply voltage for external IC's. R_X and T_X PLL loop performance are independent of the power supply voltage when the voltage regulator is used. The voltage regulator requires about 200 mV of "headroom". When the power supply decreases to within about 200 mV of the output voltage, the regulator will go out of regulation but the output voltage will not turn off. Instead, the output voltage will maintain about a 200 mV delta to the power supply voltage as the power supply voltage continues to decrease. The "PLL V_{ref}" pin can be connected to "V_{CC} Audio" by the external wiring if voltage higher than 2.2 V is required. But it should not be connected to other supply except "V_{CC} Audio". The voltage regulator is "on" in the Active and R_X modes. In the Standby and Inactive modes, the voltage regulator is turned off to reduce current drain and the "PLL V_{ref}" pin is internally connected to "V_{CC} Audio" (i.e., the supply voltage is maintained but is now unregulated).

(Test Conditions: V_{CC} = 2.6 V, T_A = 25°C.)

Characteristic	Condition	Input Pin	Measure Pin	Symbol	Min	Typ	Max	Unit
Output Voltge Level	V_{CC} = 2.6 V, O_L= 0 mA	–	V_{CC} PLL	V_{out}	1.9	2.2	2.5	V
Line Regulation	I_L = 0 mA, V_{CC} = 2.6 to 5.5 V	V_{CC}	V_{CC} PLL	Reg_{line}	–	1.43	40	mV
Load Regulation	V_{CC} = 2.6 V, I_L = 0 to 1.0 mA	V_{CC}	V_{CC} PLL	Reg_{load}	–	–1.86	40	mV
Drop–Out Voltage	I_L = 0 mA	–	–	DO	–	–	V_{out} + 200	mV

ELECTRICAL CHARACTERISTICS (continued)

Low Battery Detect

An external resistor divider is connected to the "Ref" input pin to set the threshold for the low battery detect. The voltage at the "Ref" input pin is compared to an internal 1.23 V Band-gap reference voltage. The "BD Out" pin is open collector and requires and external pull–up resistor to V_{CC}.

(Test Conditions: V_{CC} = 2.6 V, T_A = 25°C.)

Characteristic	Condition	Input Pin	Measure Pin	Symbol	Min	Typ	Max	Unit
Average Threshold Voltage	Take average of rising and falling threshold	Ref	Ref/ BD Out	Threshold	–	1.23	–	V
Hysteresis	–	Ref	Ref/ BD Out	Hys	–	4.0	–	mV
Input Current	V_{in} = 1.6 V	–	Ref	I_{in}	–50	5.71	+50	nA
Output High Voltage	V_{ref} = 1.6, R_L = 3.9 kΩ	Ref	BD Out	V_{OH}	V_{CC} – 0.1	2.6	–	V
Output Low Voltage	V_{ref} = 0.9, R_L = 3.9 kΩ	Ref	BD Out	V_{OL}	–	0.12	0.4	V

Figure 3. Data Amp Operation

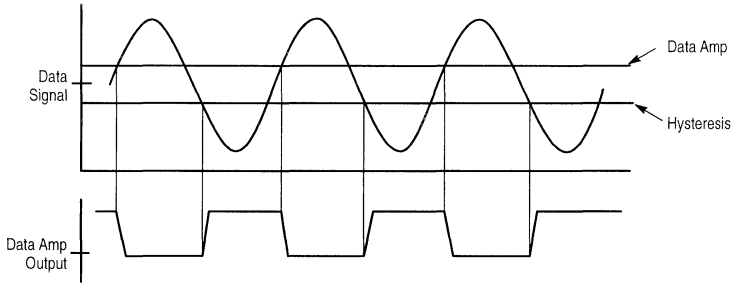


Figure 4. Typical Expander Response

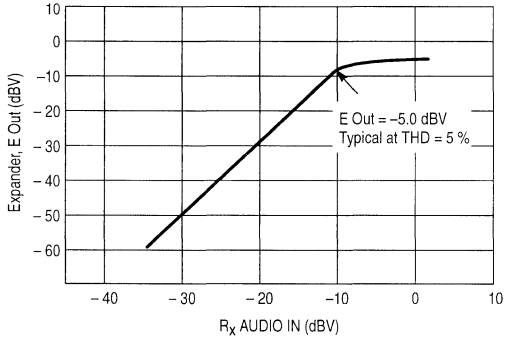


Figure 5. Typical Compressor/ALC/Limiter Response

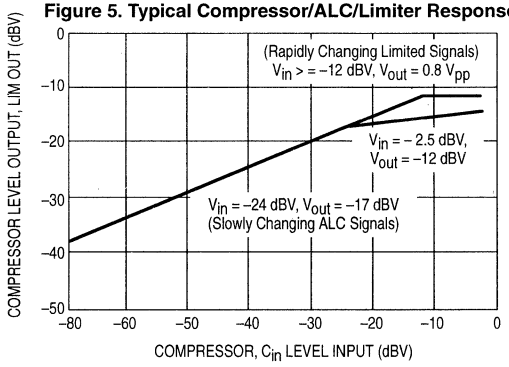


Figure 6. Total T_X Path, Mic Amp Gain = 16 dB, Splatter Amp Gain = 9.0 dB

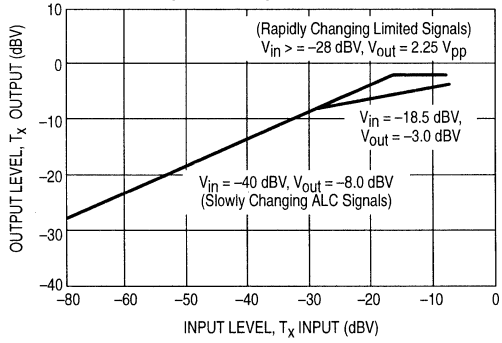
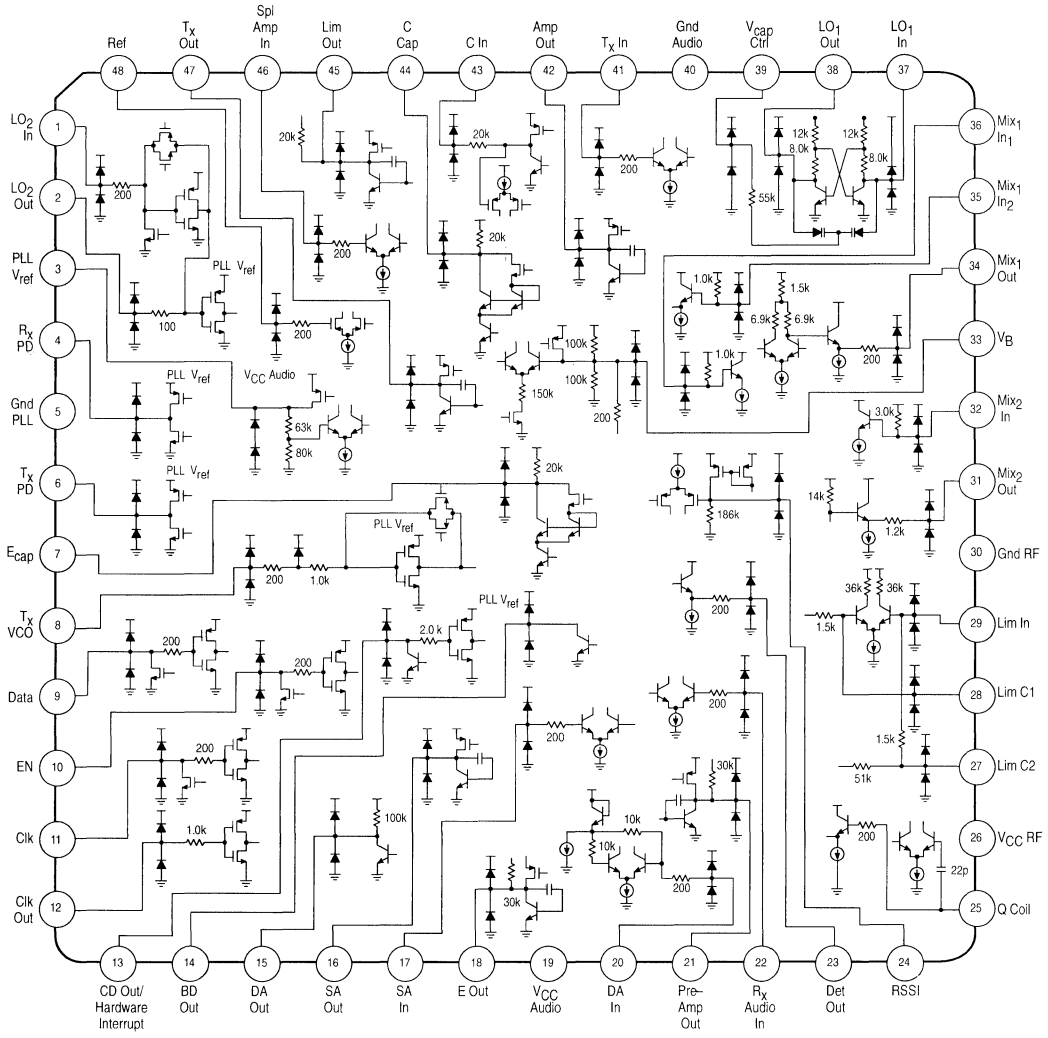


Figure 7. MC13109FTA Internal I/O Block Diagram



PIN FUNCTION DESCRIPTION

48–TQFP Pin	52–QFP Pin	Symbol	Type	Description
1 2	1 2	LO_2 In LO2 Out	–	These pins form the PLL reference oscillator when connected to an external parallel–resonant crystal (10.24 MHz typical). The reference oscillator is also the second Local Oscillator (LO_2) for the RF receiver.
3	3	PLL V_{ref}	Supply	Voltage Regulator output pin. The internal voltage regulator provides a stable power supply voltage for the R_X and T_X PLL's and can also be used as a regulated supply voltage for the other IC's.
4	4	R_X PD	Output	Three state voltage output of the R_X Phase Detector. This pin is either "high", "low", or "high impedance" depending on the phase difference of the phase detector input signals. During lock, very narrow pulses with a frequency equal to the reference frequency are present. This pin drives the external R_X PLL loop filter. It is important to minimize the line length and capacitance of this pin.
5	5	Gnd PLL	Gnd	Ground pin for PLL section of IC.
6	6	T_X PD	Output	Three state voltage output of the T_X Phase Detector. This pin is either "high", "low", or "high impedance" depending on the phase difference of the phase detector input signals. During lock, very narrow pulses with a frequency equal to the reference frequency are present. This pin drives the external T_X PLL loop filter. It is important to minimize the line length and capacitance on this pin.
7	7	E Cap	–	Expander rectifier filter capacitor pin. Connect capacitor to V_{CC}.
8	8	T_X VCO	Input	Transmit divide counter input which is driven by an ac coupled external transmit loop VCO. The minimum signal level is 200 mV_{pp} @ 80.0 MHz. This pin also functions as the test mode input for the counter tests.
9 10 11	9 10 11	Data EN Clk	Input	Microprocessor serial interface input pins for programming various counters and control functions.
12	12	Clk Out	Output	Microprocesor Clock Output which is derived from the 2nd LO crystal oscillator and a programmable divider. It can be used to drive a microprocessor and thereby reduce the number of crystals required in the system design. The driver has an internal resistor in series with the output whch can be combined with an external capacitor to form a low pass filter to reduce radiated noise on the PCB. This output also functions as the output for the counter test modes.
N/A	14	Status Out	Output	This pin indicates when the internal latches may have lost memory due to a power glitch.
13	15	CD Out/ Hardware Interrupt	Output/ Input	Dual function pin; 1) Carrier detect output (open collector with external 100 kΩ pull–up resistor. 2) Hardware interrupt input which can be used to "wake–up" from Inactive Mode.
14	16	BD Out	Output	Low battery detect output (open collector with external pull–up resistor).
15	17	DA Out	Output	Data amplifier output (open collector with internal 100 kΩ pull–up resistor).
16	18	SA Out	Output	Speaker amplifier output.
17	19	SA In	Input	Speaker amplifier input (ac coupled).
18	20	E Out	Output	Expander output.
19	21	V_{CC} Audio	Supply	V_{CC} supply for audio section.
20	22	DA In	Input	Data amplifier input (ac coupled).
21	23	Pre–Amp Out	Output	Pre–amplifier output for connection of pre–amplifier feedback resistor.
22	24	R_X Audio In	Input	R_X audio input to pre–amplifier (ac coupled).
23	25	Det Out	Output	Audio output from FM detector.
24	26	RSSI	–	Receive signal strength indicator filter capacitor.
N/A	27	N/A	–	Note used.
25	28	Q Coil	–	A quad coil or ceramic discriminator are connected to this pin.
26	29	V_{CC} RF	Supply	V_{CC} supply for RF receiver section.
27 28	30 31	Lim C2 Lim C1	–	IF amplifier/limiter capacitor pins.

PIN FUNCTION DESCRIPTION (continued)

48–TQFP Pin	52–QFP Pin	Symbol	Type	Description
29	32	Lim In	Input	Signal input for IF amplifier/limiter.
30	33	Gnd RF	Gnd	Ground pin for RF section of the IC.
31	34	Mix_2 Out	Output	Second mixer output.
32	35	Mix_2 In	Input	Second mixer input.
33	36	V_B	–	Internal half supply analog ground reference.
34	37	Mix_1 Out	Output	First mixer output.
35	38	Mix_1 In_2	Input	Negative polarity first mixer input.
36	39	Mix_1 In_1	Input	Positive polarity first mixer input.
37 38	40 41	LO_1 In LO_1 Out	–	Tank elements for 1st LO multivibrator oscillator are connected to these pins.
39	42	V_{cap} Ctrl	–	1st LO varactor control pin.
40	43	Gnd Audio	Gnd	Ground for audio section of the IC.
41	44	T_X In	Input	T_X path input to Microphone Amplifier (ac coupled).
42	45	Amp Out	Output	Microphone amplifier output.
43	46	C In	Input	Compressor input (ac coupled).
44	47	C Cap	–	Compressor rectifier filter capacitor pin. Connect capacitor to V_{CC}.
45	48	Lim Out	Output	T_X path limiter output.
46	49	Spl Amp In	Input	Splatter amplifier input (ac coupled).
47	50	T_X Out	Output	T_X path audio output.
48	51	Ref	Input	Reference voltage input for low battery detect.
N/A	52	N/A	–	Not used.

Power Supply Voltage

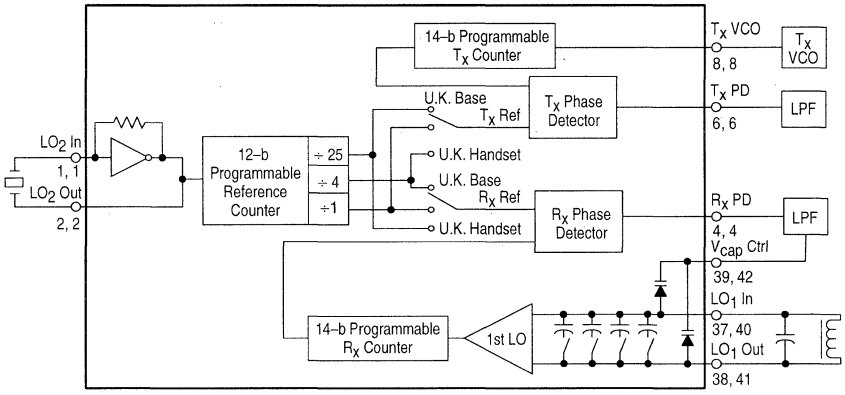
This circuit is used in a cordless telephone handset and base unit. The handset is battery powered and can operate on two ro three NiCad cells or on 5.0 V power.

PLL Frequency Synthesizer General Description

Figure 8 shows a simplified block diagram of the programmable universal dual phase locked loop (PLL). This dual PLL is fully programmable thorugh the MCU serial interface and supports most country channel frequencies including USA (25 ch), France, Spain, Australia, Korea, New Zealand, U.K., Netherlands and China (see channel frequency tables in Appendix A).

The 2nd local oscillator and reference divider provide the reference frequency for the R_X and T_X PLL loops. The programmed divider value for the reference divider is selected based on the crystal frequency and the desired R_X and T_X reference frequency values. Additional divide by 25 and divide by 4 blocks are provided to allow for generation of the 1.0 kHz and 6.25 kHz reference frequencies required for the U.K. The 14–bit T_X counter is programmed for the desired transmit channel frequency. The 14–bit R_X counter is programmed for the desired first local oscillator frequency. All counters power up in the proper default state for USA channel #6 and for a 10.24 MHz reference frequency crystal. Internal fixed capacitors can be connected to the tank circuit of the 1st LO through microprocessor control to extend the sensitivity of the 1st LO for U.S. 25 channel operation.

Figure 8. Dual PLL Simplified Block Diagram



ELECTRICAL CHARACTERISTICS (V_{CC} = 2.6 V, T_A = 25°C)

Characteristic	Condition	Measure Pin	Symbol	Min	Max	Unit
PLL PIN DC						
Input Voltage Low	–	Data Clk EN Hardware Int.	V_{IL}	–	0.3	V
Input Voltage High	–	Data Clk EN	V_{IH}	"PLL V_{ref}" – 0.3	"V_{CC} Audio"	V
Input Current Low	V_{in} = 0.3 V	Data Clk EN	I_{IL}	–5.0	–	µA
Input Current High	V_{in} = (V_{CC} Audio) – 0.3	Data Clk EN	I_{IH}	–	5.0	µA
Hysteresis Voltage	–	Data Clk EN	V_{hys}	1.0	–	V
Output Current High	–	R_X PD T_X PD	I_{OH}	–	–0.7	mA
Output Current Low	–	R_X PD T_X PD	I_{OL}	0.7	–	mA
Output Voltage Low	I_{IL} = 0.7 mA	R_X PD T_X PD	V_{OL}	–	(PLL V_{ref})* 0.2	V
Output Voltage High	I_{IH} = –0. 7mA	R_X PD T_X PD	V_{OH}	(PLL V_{ref})* 0.8	–	V
Tri–State Leakage Current	V = 1.2 V	R_X PD T_X PD	I_{OZ}	–50	50	nA
Input Capacitance	–	Data Clk EN	C_{in}	–	8.0	pF
Output Capacitance	–	R_X PD T_X PD	C_{out}	–	8.0	pF

ELECTRICAL CHARACTERISTICS (continued) (V_{CC} = 2.6 V, T_A = 25°C)

Characteristic	Condition	Measure Pin	Symbol	Min	Max	Unit
PLL PIN INTERFACE						
EN to Clk Setup Time	–	EN, Clk	t_{suEC}	200	–	ns
Data to Clk Setup Time	–	Data, Clk	t_{suDC}	100	–	ns
Hold Time	–	Data, Clk	t_h	90	–	ns
Recovery Time	–	EN, Clk	t_{rec}	90	–	ns
Input Pulse Width	–	EN, Clk	t_w	100	–	ns
Input Rise and Fall Time	–	Data Clk EN	t_r, t_f	– – –	9.0 – –	µs
MPU Interface Power–Up Delay	90% of PLL V_{ref} to Data, Clk, EN	–	t_{puMPU}	–	100	µs

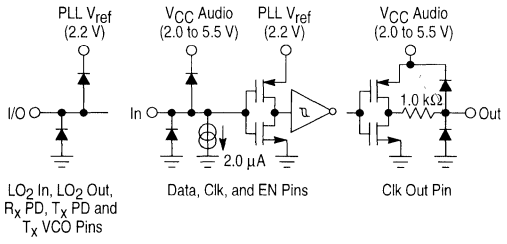
PLL LOOP

Characteristic	Condition	Measure Pin	Symbol	Min	Max	Unit
2nd LO Frequency	–	LO_2 In LO_2 Out	f_{LO}	–	12	MHz
"T_X VCO" Input Frequency	V_{in} = 200 mV_{pp}	T_X VCO	f_{txmax}	–	80	MHz

PLL I/O Pin Specifications

The 2nd LO, R_X and T_X PLL's and MPU serial interface are normally powered by the internal voltage regulator at the "PLL V_{ref}" pin. The "PLL V_{ref}" pin is the output of a voltage regulator which is powered from the "V_{CC} Audio" power supply pin. Therefore, the maximum input and output levels for most PLL I/O pins (LO_2 In, LO_2 Out, R_X PD, T_X PD, T_X VCO) is the regulated voltage at the "PLL V_{ref}" pin. The ESD protection diodes on these pins are also connected to "PLL V_{ref}". Internal level shift buffers are provided for the pins (Data, Clk, EN, Clk Out) which connect directly to the microprocessor. The maximum input and output levels for these pins is V_{CC}. Figure 9 shows a simplified schematic of the PLL I/O pins.

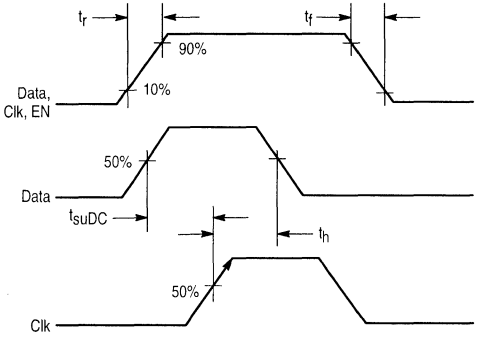
Figure 9. PLL I/O Pin Simplified Schematics



Microprocessor Serial Interface

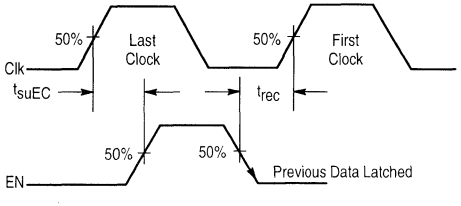
The "Data", "Clk", and "EN" pins provide an MPU serial interface for programming the reference counters, the transmit and receive channel divider counter and various control functions. The "Data" and "Clk" pins are used to load data into the shift register. Figure 10 shows "Data" and "Clk" pin timing. Data is clocked on positive clock transitions.

Figure 10. Data and Clock Timing Requirement



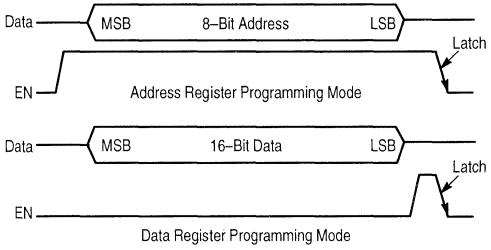
After data is loaded into the shift register, the data is latched into the appropriate latch register using the "EN" pin. This is done in two steps. First, an 8–bit address is loaded into the shift register and latched into the 8–bit address latch register. Then, up to 16–bits of data is loaded into the shift register and latched into the data latch register specified by the address that was previously loaded. Figure 11 shows the timing required on the EN pin. Latching occurs on the negative EN transition.

Figure 11. Enable Timing Requirement



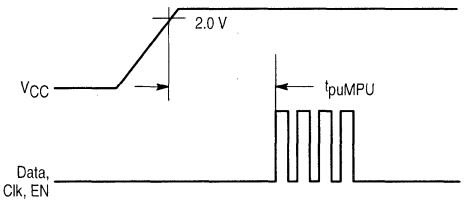
The state of the EN pin when clocking data into the shift register determines whether the data is latched into the address register or a data register. Figure 12 shows the address and data programming diagrams. In the data programming mode, there must not be any clock transitions when "EN" is high. The clock can be in a high state (default high) or a low state (default low) but must not have any transitions during the "EN" high state. The convention in these figures is that latch bits to the left are loaded into the shift register first.

Figure 12. Microprocessor Interface Programming Mode Diagrams



The MPU serial interface is fully operational within 100 μs after the power supply has reached its minimum level during power–up (See Figure 13). The MPU Interface shift registers and data latches are operational in all four power saving modes; Inactive, Standby, R_X, and Active Modes. Data can be loaded into the shift registers and latched into the latch registers in any of the operating modes.

Figure 13. Microprocessor Serial Interface Power–Up Delay



Status Out

This is a digital output which indicates whether the latch registers have been reset to their power–up default values. Latch power–up default values are given in Figure 32. If there is a power glitch or ESD event which causes the latch registers to be reset to their default values, the "Status Out" pin will indicate this to the MPU so it can reload the correct information into the latch registers.

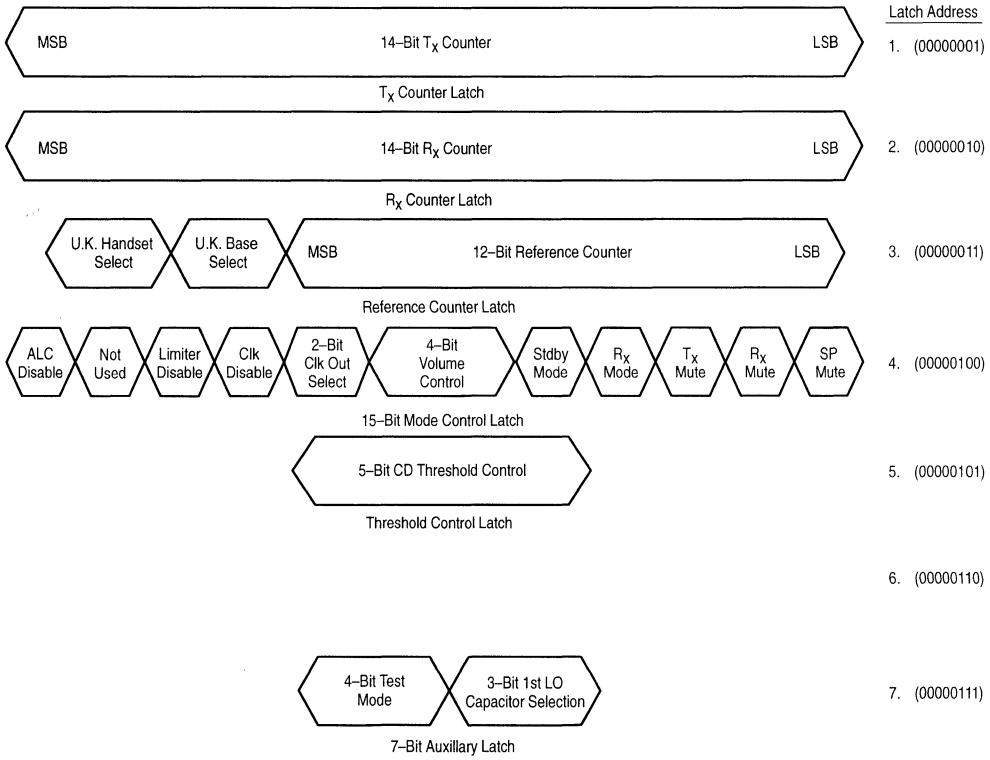
Figure 14. Status Out Operation

Status Latch Register Bits	Status Out Logic Level
Latch bits not at power–up default value	0
Latch bits at power–up default value	1

Data Registers

Figure 15 shows the data latch registers and addresses which are used to select each of these registers. Latch bits to the left (MSB) are loaded into the shift register first. The LSB bit must always be the last bit loaded into the shift register. "Don't care" bits can be loaded into the shift register first if 8–bit bytes of data are loaded.

Figure 15. Microprocessor Interface Data Latch Registers



2

Reference Frequency Selection

The "LO_2 In" and "LO_2 Out" pins form a reference oscillator when connected to an external parallel–resonant crystal. The reference oscillator is also the second local oscillator for the RF Receiver. Figure 16 shows the relationship between different crystal frequencies and reference frequencies for cordless phone applications in various countries.

Figure 16. Reference Frequency and Reference Divider Values

Crystal Frequency	Reference Divider Value	U.K. Base/ Handset Divider	Reference Frequency
10.24 MHz	2048	1	5.0 kHz
10.24 MHz	1024	4	2.5 kHz
11.15 MHz	2230	1	5.0 kHz
12.00 MHz	2400	1	5.0 kHz
11.15 MHz	1784	1	6.25 kHz
11.15 MHz	446	4	6.25 kHz
11.15 MHz	446	25	1.0 kHz

Reference Counter

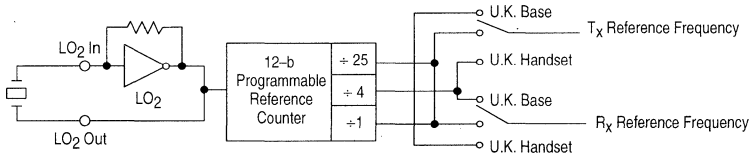
Figure 17 shows how the reference frequencies for the R_X and T_X loops are generated. All countries except U.K. require that the T_X and R_X reference frequencies be identical. In this case, set "U.K. Base Select" and "U.K. Handset Select" bits to "0". Then the fixed divider is set to "1" and the T_X and R_X reference frequencies will be equal to the crystal oscillator frequency divided by the programmable reference counter value. The U.K. is a special case which requires a different reference frequency value fo T_X and R_X.

For U.K. base operation, set "U.K. Base Select" to "1". For U.K. handset operation, set "U.K. Handset Select" to "1". The Netherlands is also a special case since a 2.5 kHz reference frequency is used for both the T_X and R_X reference and the total divider value required is 4096 which is larger than the maximum divide value available from the 12–bit reference divider (4095). In this case, set "U.K. Base Select" to "1" and set "U.K. Handset Select" to "1". This will give a fixed divide by 4 for both the T_X and R_X reference. Then set the reference divider to 1024 to get a total divider of 4096.

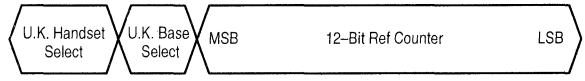
Mode Control Register

Power saving modes, mutes, disables, volume control, and microprocessor clock output frequency are all set by the Control Register. Operation of the Control Register is explained in Figures 18 through 25.

Figure 17. Reference Register Programming Mode



U.K. Handset Select	U.K. Base Select	T_X Divider Value	R_X Divider Value	Application
0	0	1	1	All but U.K. and Netherlands
0	1	25	4	U.K. Base Set
1	0	4	25	U.K. Hand Set
1	1	4	4	Netherlands Base and Hand Set



14–Bit Reference Counter Latch

Figure 18. Control Register Bits

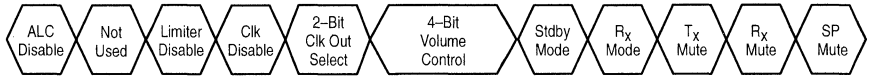


Figure 19. Mute and Disable Control Bit Descriptions

ALC Disable	1 0	Automatic Level Control Disabled Normal Operation
Limiter Disable	1 0	Limiter Disabled Normal Operation
Clock Disable	1 0	MPU Clock Output Disabled Normal Operation
T_X Mute	1 0	Transmit Channel Muted Normal Operation
R_X Mute	1 0	Receive Channel Muted Normal Operation
SP Mute	1 0	Speaker Amp Muted Normal Operation

Power Saving Operating Modes

When the MC13109 is used in a handset, it is important to conserve power in order to prolong battery life. There are five modes of operation; Active, R_X, Standby, Interrupt and Inactive. In Active Mode, all circuit blocks are powered. In R_X mode, all circuitry is powered down exept for those circuit sections needed to receive a transmission from the base. In the Standby and Interrupt Modes, all circuitry is powered down except for the circuitry needed to provide the clock output for the microprocessor. In Inactive Mode, all circuitry is powered down except the MPU interface. Latch memory is maintained in all modes. Figure 20 shows the control register bit values for selection of each power saving mode and Figure 21 show the circuit blocks which are powered in each of these operating mode.

Figure 20. Power Saving Mode Selection

Stdby Mode Bit	R_X Mode Bit	"CD Out/Hardware Interrupt" Pin	Power Saving Mode
0	0	X	Active
0	1	X	R_X
1	0	X	Standby
1	1	1 or High Impedance	Inactive
1	1	0	Inactive

Figure 21. Circuit Blocks Powered During Power Saving Modes

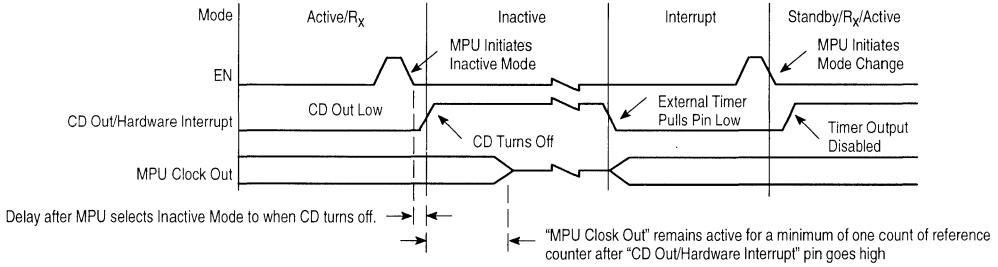
Circuit Blocks	Active	R_X	Standby	Inactive
"PLL V_{ref}" Regulated Voltage	X	X	X[1]	X[1]
MPU Interface	X	X	X	X
2nd LO Oscillator	X	X	X	
MPU Clock Output	X	X	X	
RF Receiver	X	X		
1st LO VCO	X	X		
R_X PLL	X	X		
Carrier Detect	X	X		
Data Amp	X	X		
Low Battery Detect	X	X		
T_X PLL	X			
R_X Audio Path	X			
T_X Audio Path	X			

NOTE: 1. In Standby and Inactive Modes, "PLL V_{ref}" remains powered but is not regulated. It will fluctuate with V_{CC}.

Inactive Mode Operation and Hardware Interrupt

In some handset applications it may be desirable to power down all circuitry including the microprocessor (MPU). First put the MC13109 into the Inactive mode, which turns off the MPU Clock Output (see Figure 22), and then disable the microprocessor. In order to give the MPU adequate time to power down, the MPU Clock output remains active for a minimum of one reference counter cycle (about 200 µs) after the command is given to switch into the "Inactive" mode. An external timing circuit should be used to initiate the turn–on sequence. The "CD Out" pin has a dual function. In the Active and R_X modes it performs the carrier detect function. In the Standby and Inactive modes the carrier detect circuit is disabled and the "CD Out" pin is in a "High" state due to the external pull–up resistor. In the Inactive mode the "CD Out" pin is the input for the hardware interrupt function. When the "CD Out" pin is pulled "low" by the external timing circuit, the MC13109 swtiches from the Inactive to the Interrupt mode thereby turning on the MPU Clock Output. The MPU can then resume control of the combo IC. The "CD Out" pin must remain low until the MPU changes the operating mode from Interrupt to Standby, Active or R_X modes.

Figure 22. Hardware Interrupt Operation



"Clk Out" Divider Programming

The "Clk Out" pin is derived from the 2nd local oscillator and can be used to drive a microprocessor, thereby reducing the number of crystals required. Figure 23 shows the relationship between the crystal frequency and the clock output for different divider values. Figure 24 shows the "Clk Out" register bit values.

Figure 23. Clock Output Values

Crystal Frequency	Clock Output Divider			
	2	3	4	5
10.24 MHz	5.120 MHz	3.413 MHz	2.560 MHz	2.048 MHz
11.15 MHz	5.575 MHz	3.717 MHz	2.788 MHz	2.230 MHz
12.00 MHz	6.000 MHz	4.000 MHz	3.000 MHz	2.400 MHz

Figure 24. Clock Output Divider

Clk Out Bit #1	Clk Out Bit #0	Clk Out Divider Value
0	0	2
0	1	3
1	0	4
1	1	5

MPU "Clk Out" Power–Up Default Divider Value

The power–up default divider value is "divide by 10". This provides an MPU clock of about 1.0 MHz after initial power–up. The reason for choosing this relatively low clock frequency after intial power–up is that some microprocessors that operate down to a 2.0 V power supply have a maximum clock frequency fo 1.0 MHz. After initial power–up, the MPU can change the clock divider value to set the clock to the desired operating frequency. Special care has been taken in the design of the clock divider to ensure that the transition between one clock divider value and another is "smooth" (i.e., there will be no narrow clock pulses to disturb the MPU).

MPU "Clk Out" Radiated Noise on Circuit Board

The clock line running between the MC13109 and the microprocessor has the potential to radiate noise which can cause problems in the system especially if the clock is a square wave digital signal with large high frequency harmonics. In order to minimize radiated noise, a 1.0 kΩ resistor is included on–chip in–series with the "Clk Out" output driver. A small capacitor can be connected to the "Clk Out" line on the PCB to form a single pole low pass filter. This filter will significantly reduce noise radiated from the "Clk Out" line.

Volume Control

The volume control can be programmed in 2.0 dB gain steps from –14 dB to +16 dB. The power–up default value is 0 dB.

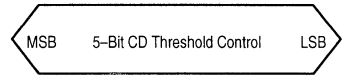
Figure 25. Volume Control

Volume Control Bit #3	Volume Control Bit #2	Volume Control Bit #1	Volume Control Bit #0	Volume Control #	Gain/Attenuation Amount
0	0	0	0	0	–14 dB
0	0	0	1	1	–12 dB
0	0	1	0	2	–10 dB
0	0	1	1	3	–8.0 dB
0	1	0	0	4	–6.0 dB
0	1	0	1	5	–4.0 dB
0	1	1	0	6	–2.0 dB
0	1	1	1	7	0 dB
1	0	0	0	8	2.0 dB
1	0	0	1	9	4.0 dB
1	0	1	0	10	6.0 dB
1	0	1	1	11	8.0 dB
1	1	0	0	12	10 dB
1	1	0	1	13	12 dB
1	1	1	0	14	14 dB
1	1	1	1	15	16 dB

Gain Control Register

The gain control register contains bits which control the Carrier Detect threshold. Operation of these latch bits are explained in Figures 26 and 27.

Figure 26. Gain Control Latch Bits



Carrier Detect Threshold Programming

Th "CD Out" pin will give an indication to the microprocessor if a carier signal is present on the selected channel. The nominal value and tolerance of the carrier detect threshold is given in the carrier detect specification section of this document. If a different carrier detect threshold value is desired, it can be set through the MPU interface as shown in Figure 27 below.

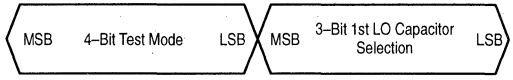
Figure 27. Carrier Detect Threshold Control

CD Bit #4	CD Bit #3	CD Bit #2	CD Bit #1	CD Bit #0	CD Control #	Carrier Detect Threshold
0	0	0	0	0	0	−20 dB
0	0	0	0	1	1	−19 dB
0	0	0	1	0	2	−18 dB
0	0	0	1	1	3	−17 dB
0	0	1	0	0	4	−16 dB
0	0	1	0	1	5	−15 dB
0	0	1	1	0	6	−14 dB
0	0	1	1	1	7	−13 dB
0	1	0	0	0	8	−12 dB
0	1	0	0	1	9	−11 dB
0	1	0	1	0	10	−10 dB
0	1	0	1	1	11	−9.0 dB
0	1	1	0	0	12	−8.0 dB
0	1	1	0	1	13	−7.0 dB
0	1	1	1	0	14	−6.0 dB
0	1	1	1	1	15	−5.0 dB
1	0	0	0	0	16	−4.0 dB
1	0	0	0	1	17	−3.0 dB
1	0	0	1	0	18	−2.0 dB
1	0	0	1	1	19	−1.0 dB
1	0	1	0	0	20	0 dB
1	0	1	0	1	21	1.0 dB
1	0	1	1	0	22	2.0 dB
1	0	1	1	1	23	3.0 dB
1	1	0	0	0	24	4.0 dB
1	1	0	0	1	25	5.0 dB
1	1	0	1	0	26	6.0 dB
1	1	0	1	1	27	7.0 dB
1	1	1	0	0	28	8.0 dB
1	1	1	0	1	29	9.0 dB
1	1	1	1	0	30	10 dB
1	1	1	1	1	31	11 dB

Auxiliary Register

The auxiliary register contains a 3–bit 1st LO Capacitor Selection latch and a 4–bit Test Mode latch. Operation of these latch bits are explained in Figures 28, 29 and 30.

Figure 28. Auxiliary Register Latch Bits



First Local Oscillator Capacitor Selection for 25 Channel U.S. Operation

There is a very large frequency difference between the minimum and maximum channel frequencies in the proposed 25 Channel U.S. standard. The sensitivity of the 1st LO is not large enough to accommodate this large frequency variation. Fixed capacitors can be connected across the 1st LO tank circuit to change the 1st LO sensitivity. Internal switches and capacitors are provided to enable microprocessor control over internal fixed capacitor values. Figure 29 shows the schematic of the 1st LO tank circuit. Figure 30 shows the latch control bit values.

The internal varactor temperature coefficient is 1800 ppm (C_O = 8.9 pF at 25°C, V_{cap} control voltage = 1.2 V, F_{req} = 36 MHz). Customer is suggested to use a negative temperature coefficient capacitor in 1st LO tank circuit when the whole operating temperature range of –40 to +85°C is considered.

Figure 29. 1st LO Schematic

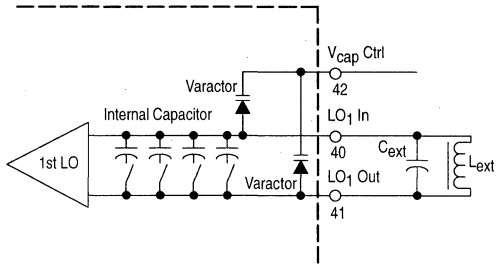


Figure 30. 1st LO Capacitor Select for U.S. 25 Channels

1st LO Cap. Bit 2	1st LO Cap. Bit 1	1st LO Cap Bit 0	1st LO Cap. Select	U.S. Base Channels	U.S. Handset Channels	Internal Cap. Value (Excluding Varactor)	Varactor Value over 0.5 to 2.2 V Range	External Capacitor Value	External Inductor Value
0	0	0	0	16 – 25	–	0.92 pF	10 – 6.4 pF	27 pF	0.47 µH
0	0	0	0	–	16 – 25	0.92 pF	10 – 6.4 pF	33 pF	0.47 µH
0	0	1	1	1 – 66	–	2.61 pF	10 – 6.4 pF	27 pF	0.47 µH
0	1	0	2	7 – 15	–	1.82 pF	10 – 6.4 pF	27 pF	0.47 µH
0	1	1	3	–	1 – 6	8.69 pF	10 – 6.4 pF	33 pF	0.47 µH
1	0	0	4	–	7 – 15	7.19 pF	10 – 6.4 pF	33 pF	0.47 µH

Figure 31. Test Mode Description

TM #	TM 3	TM 2	TM 1	TM 0	Counter Under Test or Test Mode Option	"T_X V_{CO}" Input Signal	"Clk Out" Output Expected
0	0	0	0	0	Normal Operation	>200 mV_{pp}	–
1	0	0	0	1	R_X Counter, upper 6	0 to 2.2 V	Input Frequency/64
2	0	0	1	0	R_X Counter, lower 8	0 to 2.2 V	See Note Below
3	0	0	1	1	R_X Prescaler	0 to 2.2 V	Input Frequency/4
4	0	1	0	0	T_X Counter, upper 6	0 to 2.2 V	Input Frequency/64
5	0	1	0	1	T_X Counter, lower 8	0 to 2.2 V	See Note Below
6	0	1	1	0	T_X Prescaler	>200 mV_{pp}	Input Frequency/4
7	0	1	1	1	Reference Counter	0 to 2.2 V	Input Frequency/Reference Counter Value
8	1	0	0	0	Divide by 4, 25	0 to 2.2 V	Input Frequency/100
9	1	0	0	1	AGC Gain = 10 Option	N/A	–
10	1	0	1	0	AGC Gain = 25 Option	N/A	–

NOTE: To determine the correct output, look at the lower 8 bits in the R_X or T_X register (Divisor (7;0). If the value of the divisor is > 16, then the output divisor value is Divisor (7;2) (the upper 6 bits of the divisor). If Divisor (7;0) < 16 and Divisor (3;2) > = 2, then output divisor value is Divisor (3;2) (bits 2 and 3 of the divisor). If Divisor (7;0) < 16 and Divisor (3;2) < 2, then output divisor value is (Divisor (3;2) + 60).

Test Modes

Test Mode Control latch bits enable independent testing of internal counters and set AGC Gain Options. In test mode, the "T_X VCO" input pin is multiplexed to the input of the counter under test and the output of the counter under test is multiplexed to the "Clk Out" output pin so that each counter can be individually tested. Make sure test mode bits are set to "0" for normal operation. Test mode operation is described in Figure 31. During normal operation and when testing the T_X Prescaler, the "T_X VCO" input can be a minimum of 200 mV_{pp} at 80 MHz and should be ac coupled. For other test modes, input signals should be standard logic levels of 0 to 2.2 V and a maximum frequency of 16 MHz.

Power–Up Defaults for Control and Counter Registers

When the IC is first powered up, all latch registers are initialized to a defined state. The MC13109 is initially placed in the Rx mode with all mutes active and nothing disabled. The reference counter is set to generate a 5.0 kHz reference frequency from a 10.24 MHz crystal. The MPU clock output divider is set to 10 to give the minimum clock output frequency. The T_X and R_X latch registers are set for USA Channel Frequency #21. Figure 32 shows the initial power–up states for all latch registers.

Figure 32. Latch Register Power–Up Defaults

		MSB								LSB							
Register	Count	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
T_X	9966	–	–	1	0	0	1	1	0	1	1	1	0	1	1	1	0
R_X	7215	–	–	0	1	1	1	0	0	0	0	1	0	1	1	1	1
Ref	2048	–	–	0	0	1	0	0	0	0	0	0	0	0	0	0	0
Mode	N/A	–	0	0	0	0	1	1	0	1	1	1	0	1	1	1	1
Gain	N/A	–	–	–	–	–	–	–	–	–	–	–	1	0	1	0	0
TM	N/A	–	–	–	–	–	–	–	–	–	0	0	0	0	0	0	0

Figure 33. I_{CC} versus V_{CC} at Active Mode

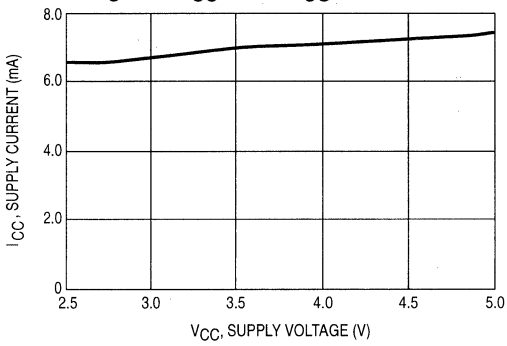


Figure 34. I_{CC} versus V_{CC} at Receive Mode

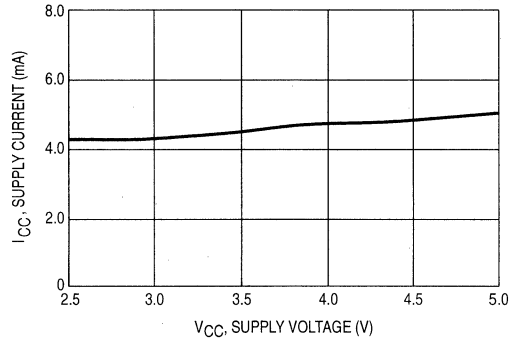


Figure 35. I_{CC} versus V_{CC} at Standby Mode

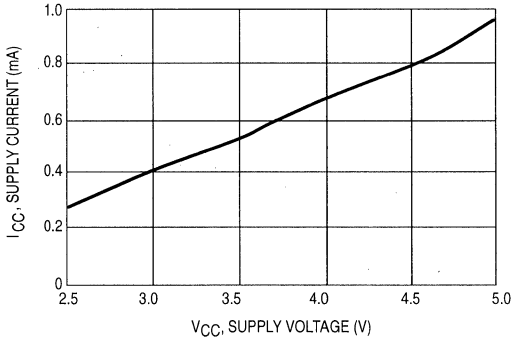


Figure 36. I_{CC} versus V_{CC} at Inactive Mode

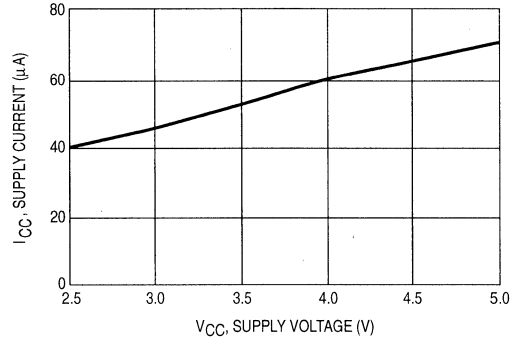


Figure 37. RF_{in} versus AF_{out}, N+D, N, AMR

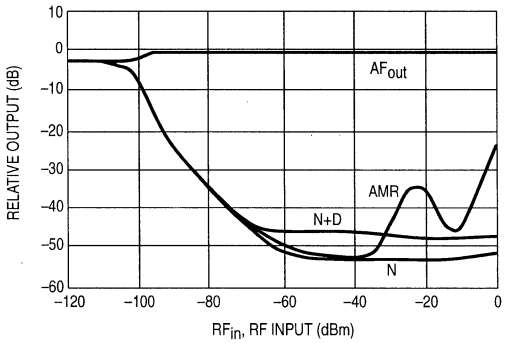


Figure 38. Recovered Audio/THD versus f_{DEV}

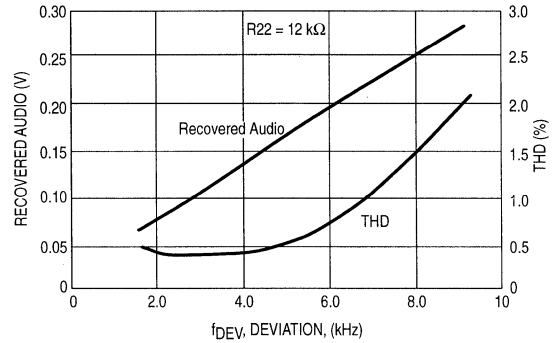


Figure 39. RSSI Output versus RF_{in}

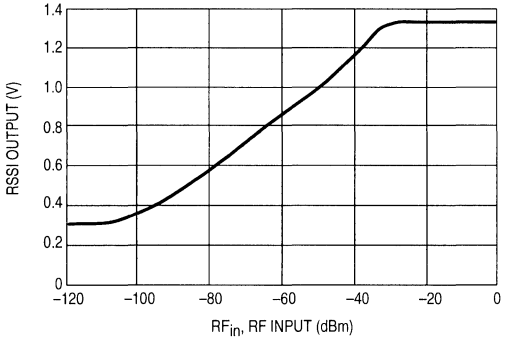
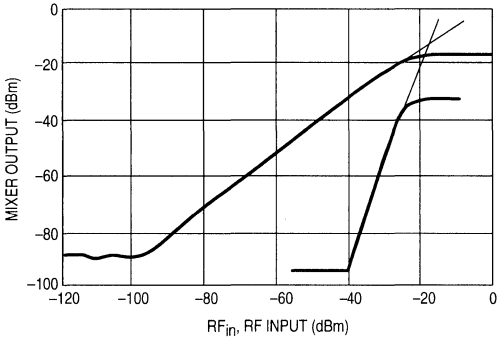


Figure 40. First Mixer Third Order Intercept Performance



2

APPENDIX A – CHANNEL FREQUENCIES

USA CT–1 BASE SET CHANNEL FREQUENCIES (2nd LO = 10.240 MHz, Ref Divider = 2048)

Channel Number	T_X Channel Frequency (MHz)	T_X Divider (5.0 kHz Ref)	1st LO Frequency (MHz) 1st IF = 10.695 MHz	R_X Divider (5.0 kHz Ref)
1	43.720	8744	38.065	7613
2	43.740	8748	38.145	7629
3	43.820	8764	38.165	7633
4	43.840	8768	38.225	7645
5	43.920	8784	38.325	7665
6	43.960	8792	38.385	7677
7	44.120	8824	38.405	7681
8	44.160	8832	38.465	7693
9	44.180	8836	38.505	7701
10	44.200	8840	38.545	7709
11	44.320	8864	38.585	7717
12	44,360	8872	38.665	7733
13	44.400	8880	38.705	7741
14	44.460	8892	38.765	7753
15	44.480	8896	38.805	7761
16	46.610	9322	38.975	7795
17	46.630	9326	39.150	7830
18	46.670	9334	39.165	7833
19	46.710	9342	39.075	7815
20	46.730	9346	39.180	7836
21	46.770	9354	39.135	7827
22	46.830	9366	39.195	7839
23	46.870	9374	39.235	7847
24	46.930	9386	39.295	7859
25	46.970	9394	39.275	7855

USA CT–1 HANDSET CHANNEL FREQUENCIES (2nd LO = 10.240 MHz, Ref Divider = 2048)

Channel Number	T_X Channel Frequency (MHz)	T_X Divider (5.0 kHz Ref)	1st LO Frequency (MHz) 1st IF = 10.695 MHz	R_X Divider (5.0 kHz Ref)
1	48.760	9752	33.025	6605
2	48.840	9768	33.045	6609
3	48.860	9772	33.125	6625
4	48.920	9784	33.145	6629
5	49.020	9804	33.225	6645
6	49.080	9816	33.265	6653
7	49.100	9820	33.425	6685
8	49.160	9832	33.465	6693
9	49.200	9840	33.485	6697
10	49.240	9848	33.505	6701
11	49.280	9856	33.625	6725
12	49.360	9872	33.665	6733
13	49.400	9880	33.705	6741
14	49.460	9892	33.765	6753
15	49.500	9900	33.785	6757
16	49.670	9934	35.915	7183
17	49.845	9969	35.935	7187
18	49.860	9972	35.975	7195
19	49.770	9954	36.015	7203
20	49.875	9975	36.035	7207
21	49.830	9966	36.075	7215
22	49.890	9978	36.135	7227
23	49.930	9986	36.175	7235
24	49.990	9998	36.235	7247
25	49.970	9994	36.275	7255

SPAIN CT–1 BASE SET CHANNEL FREQUENCIES (2nd LO = 10.240 MHz, Ref Divider = 2048)

Channel Number	T_X Channel Frequency (MHz)	T_X Divider (5.0 kHz Ref)	1st LO Frequency (MHz) 1st IF = 10.695 MHz	R_X Divider (5.0 kHz Ref)
1	31.025	6205	29.230	5846
2	31.050	6210	29.255	5851
3	31.075	6215	29.280	5856
4	31.100	6220	29.305	5861
5	31.125	6225	29.330	5866
6	31.150	6230	29.355	5871
7	31.175	6235	29.380	5876
8	31.200	6240	29.405	5881
9	31.250	6250	29.455	5891
10	31.275	6255	29.480	5896
11	31.300	6260	29.505	5901
12	31.325	6295	29.530	5906

SPAIN CT–1 HANDSET CHANNEL FREQUENCIES (2nd LO = 10.240 MHz, Ref Divider = 2048)

Channel Number	T_X Channel Frequency (MHz)	T_X Divider (5.0 kHz Ref)	1st LO Frequency (MHz) 1st IF = 10.695 MHz	R_X Divider (5.0 kHz Ref)
1	39.925	7985	20.330	4066
2	39.950	7990	20.355	4071
3	39.975	7995	20.380	4076
4	40.000	8000	20.405	4081
5	40.025	8005	20.430	4086
6	40.050	8010	20.455	4091
7	40.075	8015	20.480	4096
8	40.100	8020	20.505	4101
9	40.150	8030	20.555	4111
10	40.175	8035	20.580	4116
11	40.200	8040	20.605	4121
12	40.225	8045	20.630	4126

AUSTRALIA CT–1 BASE SET CHANNEL FREQUENCIES (2nd LO = 10.240 MHz, Ref Divider = 2048)

Channel Number	T_X Channel Frequency (MHz)	T_X Divider (5.0 kHz Ref)	1st LO Frequency (MHz) 1st IF = 10.695 MHz	R_X Divider (5.0 kHz Ref)
1	30.075	6015	29.080	5816
2	30.125	6025	29.130	5826
3	30.175	6035	29.180	5836
4	30.225	6045	29.230	5846
5	30.275	6055	29.280	5856
6	30.100	6020	29.105	5821
7	30.150	6030	29.155	5831
8	30.200	6040	29.205	5841
9	30.250	6050	29.255	5851
10	30.300	6060	29.305	5861

AUSTRALIA CT–1 HANDSET CHANNEL FREQUENCIES (2nd LO = 10.240 MHz, Ref Divider = 2048)

Channel Number	T_X Channel Frequency (MHz)	T_X Divider (5.0 kHz Ref)	1st LO Frequency (MHz) 1st IF = 10.695 MHz	R_X Divider (5.0 kHz Ref)
1	39.775	7955	19.380	3876
2	39.825	7965	19.430	3886
3	39.875	7975	19.480	3896
4	39.925	7985	19.530	3906
5	39.975	7995	19.580	3916
6	39.800	7960	19.405	3881
7	39.850	7970	19.455	3891
8	39.900	7980	19.505	3901
9	39.950	7990	19.555	3911
10	40.000	8000	19.605	3921

KOREA CT–1 BASE SET CHANNEL FREQUENCIES (2nd LO = 10.240 MHz, Ref Divider = 2048)

Channel Number	T_X Channel Frequency (MHz)	T_X Divider (5.0 kHz Ref)	1st LO Frequency (MHz) 1st IF = 10.695 MHz	R_X Divider (5.0 kHz Ref)
1	46.610	9322	38.975	7795
2	46.630	9326	39.150	7830
3	46.670	9334	39.165	7833
4	46.710	9342	39.075	7815
5	46.730	9346	39.180	7836
6	46.770	9354	39.135	7827
7	46.830	9366	39.195	7839
8	46.870	9374	39.235	7847
9	46.930	9386	39.295	7859
10	46.970	9394	39.275	7855
11	46.510	9302	39.000	7800
12	46.530	9306	39.015	7803
13	46.550	9310	39.030	7806
14	46.570	9314	39.045	7809
15	46.590	9318	39.060	7812

KOREA CT–1 HANDSET CHANNEL FREQUENCIES (2nd LO = 10.240 MHz, Ref Divider = 2048)

Channel Number	T_X Channel Frequency (MHz)	T_X Divider (5.0 kHz Ref)	1st LO Frequency (MHz) 1st IF = 10.695 MHz	R_X Divider (5.0 kHz Ref)
1	49.670	9934	35.915	7183
2	49.845	9969	35.935	7187
3	49.860	9972	35.975	7195
4	49.770	9954	36.015	7203
5	49.875	9975	36.035	7207
6	49.830	9966	36.075	7215
7	49.890	9978	36.135	7227
8	49.930	9986	36.175	7235
9	49.990	9998	36.235	7247
10	49.970	9994	36.275	7255
11	49.695	9939	35.815	7163
12	49.710	9942	35.835	7167
13	49.725	9945	35.855	7171
14	49.740	9948	35.875	7175
15	49.755	9951	35.895	7179

NEW ZEALAND CT–1 BASE SET CHANNEL FREQUENCIES (2nd LO = 10.240 MHz, Ref Divider = 2048)

Channel Number	T_X Channel Frequency (MHz)	T_X Divider (5.0 kHz Ref)	1st LO Frequency (MHz) 1st IF = 10.695 MHz	R_X Divider (5.0 kHz Ref)
11	34.250	6850	29.555	5911
12	34.275	6855	29.580	5916
13	34.300	6860	29.605	5921
14	34.325	6865	29.630	5926
15	34.350	6870	29.655	5931
16	34.375	6875	29.680	5936
17	34.400	6880	29.705	5941
18	34.425	6885	29.730	5946
19	34.450	6890	29.755	5951
20	34.475	6895	29.780	5956

NEW ZEALAND CT–1 HANDSET CHANNEL FREQUENCIES (2nd LO = 10.240 MHz, Ref Divider = 2048)

Channel Number	T_X Channel Frequency (MHz)	T_X Divider (5.0 kHz Ref)	1st LO Frequency (MHz) 1st IF = 10.695 MHz	R_X Divider (5.0 kHz Ref)
11	40.250	8050	23.555	4711
12	40.275	8055	23.580	4716
13	40.300	8060	23.605	4721
14	40.325	8065	23.630	4726
15	40.350	8070	23.655	4731
16	40.375	8075	23.680	4736
17	40.400	8080	23.705	4741
18	40.425	8085	23.730	4746
19	40.450	8090	23.755	4751
20	40.475	8095	23.780	4756

U.K. BASE SET CHANNEL FREQUENCIES (2nd LO = 11.150 MHz, Ref Divider = 446 + divide by 4/25)

Channel Number	T_X Channel Frequency (MHz)	T_X Divider (1.0 kHz Ref)	1st LO Frequency (MHz) 1st IF = 10.7 MHz	R_X Divider (6.25 kHz Ref)
1	1.642	1642	36.75625	5881
2	1.662	1662	36.76875	5883
3	1.682	1682	36.78125	5885
4	1.702	1702	36.79375	5887
5	1.722	1722	36.80625	5889
6	1.742	1742	36.81875	5891
7	1.762	1762	36.83125	5893
8	1.782	1782	36.84375	5895

U.K. HANDSET CHANNEL FREQUENCIES (2nd LO = 11.150 MHz, Ref Divider = 446 + divide by 4/25)

Channel Number	T_X Channel Frequency (MHz)	T_X Divider (6.25 kHz Ref)	1st LO Frequency (MHz) 1st IF = 10.7 MHz	R_X Divider (1.0 kHz Ref)
1	47.45625	7593	12.342	12342
2	47.46875	7595	12.362	12362
3	47.48125	7597	12.382	12382
4	47.49375	7599	12.402	12402
5	47.50625	7601	12.422	12422
6	47.51875	7603	12.442	12442
7	47.53125	7605	12.462	12462
8	47.54375	7607	12.482	12482

FRANCE BASE SET CHANNEL FREQUENCIES (2nd LO = 11.150 MHz, Ref Divider = 1784)

Channel Number	T_X Channel Frequency (MHz)	T_X Divider (6.25 kHz Ref)	1st LO Frequency (MHz) 1st IF = 10.7 MHz	R_X Divider (6.25 kHz Ref)
1	26.3125	4210	30.6125	4898
2	26.3250	4212	30.6250	4900
3	26.3375	4214	30.6375	4902
4	26.3500	4216	30.6500	4904
5	26.3625	4218	30.6625	4906
6	26.3750	4220	30.6750	4908
7	26.3875	4222	30.6875	4910
8	26.4000	4224	30.7000	4912
9	26.4125	4226	30.7125	4914
10	26.4250	4228	30.7250	4916
11	26.4375	4230	30.7375	4918
12	26.4500	4232	30.7500	4920
13	26.4625	4234	30.7625	4922
14	26.4750	4236	30.7750	4924
15	26.4875	4238	30.7875	4926

FRANCE HANDSET CHANNEL FREQUENCIES (2nd LO = 11.150 MHz, Ref Divider = 1784)

Channel Number	T_X Channel Frequency (MHz)	T_X Divider (6.25 kHz Ref)	1st LO Frequency (MHz) 1st IF = 10.7 MHz	R_X Divider (6.25 kHz Ref)
1	41.3125	6610	37.0125	5922
2	41.3250	6612	37.0250	5924
3	41.3375	6614	37.0375	5926
4	41.3500	6616	37.0500	5928
5	41.3625	6618	37.0625	5930
6	41.3750	6620	37.0750	5932
7	41.3875	6622	37.0875	5934
8	41.4000	6624	37.1000	5936
9	41.4125	6626	37.1125	5938
10	41.4250	6628	37.1250	5940
11	41.4375	6630	37.1375	5942
12	41.4500	6632	37.1500	5944
13	41.4625	6634	37.1625	5946
14	41.4750	6636	37.1750	5948
15	41.4875	6638	37.1875	5950

CHINA BASE SET CHANNEL FREQUENCIES (2nd LO = 10.240 MHz, Ref Divider = 2048)

Channel Number	T_X Channel Frequency (MHz)	T_X Divider (5.0 kHz Ref)	1st LO Frequency (MHz) 1st IF = 10.695 MHz	R_X Divider (5.0 kHz Ref)
1	45.250	9050	37.555	7511
2	45.275	9055	37.580	7516
3	45.300	9060	37.605	7521
4	45.325	9065	37.630	7526
5	45.350	9070	37.655	7531
6	45.375	9075	37.680	7536
7	45.400	9080	37.705	7541
8	45.425	9085	37.730	7546
9	45.450	9090	37.755	7551
10	45.475	9095	37.780	7556

CHINA HANDSET CHANNEL FREQUENCIES (2nd LO = 10.240 MHz, Ref Divider = 2048)

Channel Number	T_X Channel Frequency (MHz)	T_X Divider (5.0 kHz Ref)	1st LO Frequency (MHz) 1st IF = 10.695 MHz	R_X Divider (5.0 kHz Ref)
1	48.250	9650	34.555	6911
2	48.275	9655	34.580	6916
3	48.300	9660	34.605	6921
4	48.325	9665	34.630	6926
5	48.350	9670	34.655	6931
6	48.375	9675	34.680	6936
7	48.400	9680	34.705	6941
8	48.425	9685	34.730	6946
9	48.450	9690	34.755	6951
10	48.475	9695	34.780	6956

NETHERLANDS CT–1 BASE SET CHANNEL FREQUENCIES

(2nd LO = 10.240 MHz, Ref Divider = 1024 + divide by 4, 2nd IF = 455 Hz)

Channel Number	T_X Channel Frequency (MHz)	T_X Divider (2.5 kHz Ref)	1st LO Frequency (MHz) 1st IF = 10.695 MHz	R_X Divider (2.5 kHz Ref)
1	31.0375	12415	29.2425	11697
2	31.0625	12425	29.2675	11707
3	31.0875	12435	29.2925	11717
4	31.1125	12445	29.3175	11727
5	31.1375	12455	29.3425	11737
6	31.1625	12465	29.3675	11747
7	31.1875	12475	29.3925	11757
8	31.2125	12485	29.4175	11767
9	31.2375	12495	29.4425	11777
10	31.2625	12505	29.4675	11787
11	31.2875	12515	29.4925	11797
12	31.3125	12525	29.5175	11807

NETHERLANDS CT–1 HANDSET CHANNEL FREQUENCIES

(2nd LO = 10.240 MHz, Ref Divider = 1024 + divide by 4, 2nd IF = 455 Hz)

Channel Number	T_X Channel Frequency (MHz)	T_X Divider (2.5 kHz Ref)	1st LO Frequency (MHz) 1st IF = 10.695 MHz	R_X Divider (2.5 kHz Ref)
1	39.9375	15975	20.3425	8137
2	39.9625	15985	20.3675	8147
3	39.9875	15995	20.3925	8157
4	40.0125	16005	20.4175	8167
5	40.0375	16015	20.4425	8177
6	40.0625	16025	20.4675	8187
7	40.0875	16035	20.4925	8197
8	40.1125	16045	20.5175	8207
9	40.1375	16055	20.5425	8217
10	40.1625	16065	20.5675	8227
11	40.1875	16075	20.5925	8237
12	40.2125	16085	20.6175	8247

APPENDIX B – MEASUREMENT OF COMPANDOR ATTACK/DECAY TIME

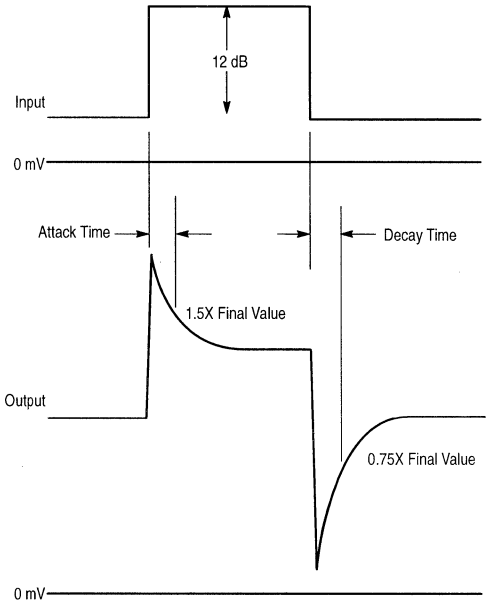
This measurement definition is based on EIA/CCITT recommendations.

Compressor Attack Time

For a 12 dB step up at the input, attack time is defined as the time for the output to settle to 1.5X of the final steady state value.

Compressor Decay Time

For a 12 dB step down at the input, decay time is defined as the time for the input to settle to 0.75X of the final steady state value.

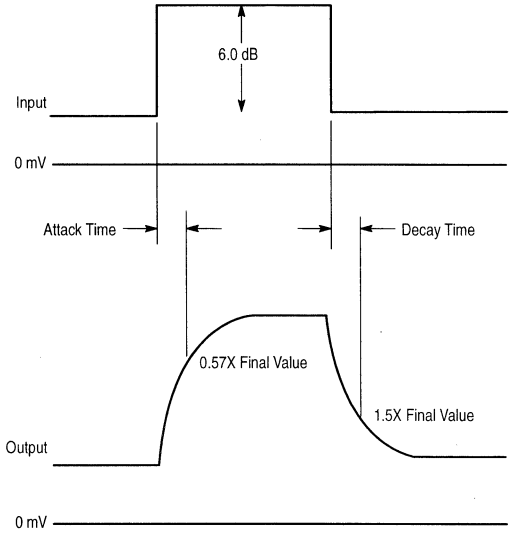


Expander Attack

For a 6.0 dB step up at the input, attack time is defined as the time for the output to settle to 0.57X of the final steady state value.

Expander Decay

For a 6.0 dB step down at the input, decay time is defined as the time for the output to settle to 1.5X of the final steady state value.



MOTOROLA

Product Preview

Universal Cordless Telephone Subsystem IC with Scrambler

MC13110

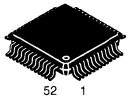
UNIVERSAL CT–1 SUBSYSTEM INTEGRATED CIRCUIT

SEMICONDUCTOR TECHNICAL DATA

2

The MC13110 integrates several of the functions required for a cordless telephone into a single integrated circuit. This significantly reduces component count, board space requirements, and external adjustments. It is designed for use in both the handset and the base.

- Dual Conversion FM Receiver
  - Complete Dual Conversion Receiver – Antenna In to Audio Out 80 MHz Maximum Carrier Frequency
  - RSSI Output
  - Carrier Detect Output with Programmable Threshold
  - Comparator for Data Recovery
  - Operates with Either a Quad Coil or Ceramic Discriminator
- Compander
  - Expandor Includes Mute, Digital Volume Control, Speaker Driver, 3.5 kHz Low Pass Filter, and Programmable Gain Block
  - Compressor Includes Mute, 3.5 kHz Low Pass Filter, Limiter, and Programmable Gain Block
- Dual Universal Programmable PLL
  - Supports New 25 Channel U.S. Standard with New External Switches
  - Universal Design for Domestic and Foreign CT–1 Standards
  - Digitally Controlled Via a Serial Interface Port
  - Receive Side Includes 1st LO VCO, Phase Detector, and 14–Bit Programmable Counter and 2nd LO with 12–Bit Counter
  - Transmit Section Contains Phase Detector and 14–Bit Counter
  - MPU Clock Outputs Eliminates Need for MPU Crystal
- Supply Voltage Monitor
  - Provides Two Levels of Monitoring with Separate Outputs
  - Separate, Adjustable Trip Points
- Frequency Inversion Scrambler/Descrambler
  - Can Be Enabled/Disabled Via MPU Interface
  - Programmable Carrier Modulation Frequency
- 2.7 to 5.5 V Operation with One–Third the Power Consumption of Competing Devices

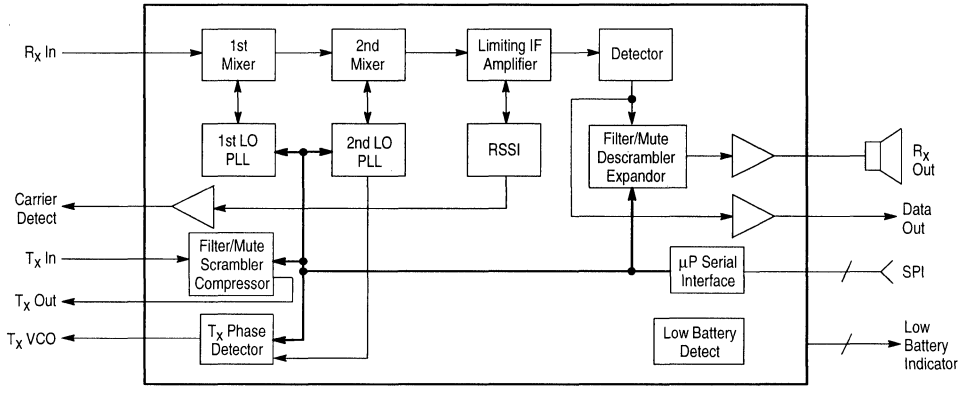


FB SUFFIX
PLASTIC QFP PACKAGE
CASE 848B

ORDERING INFORMATION

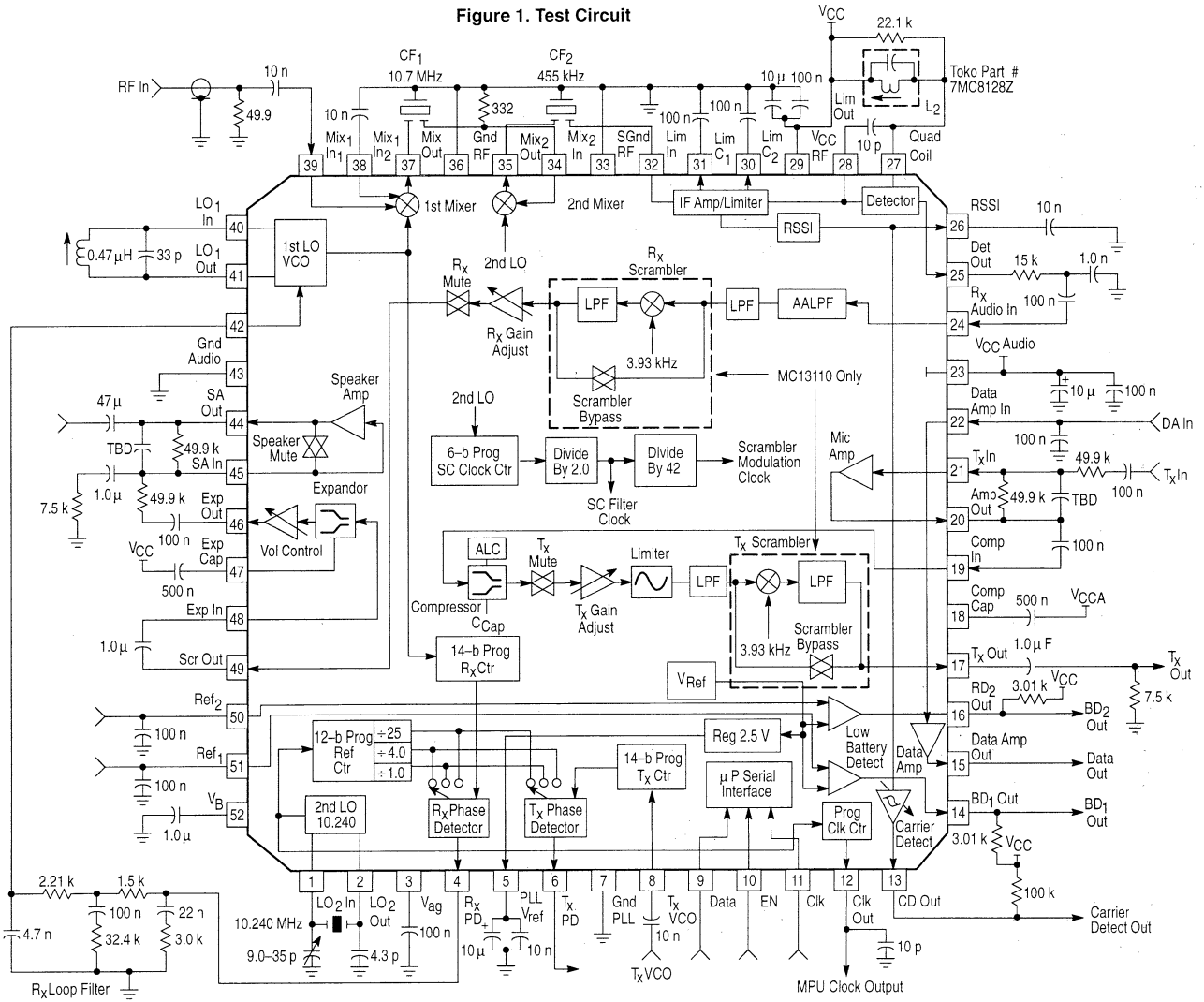
Device	Tested Operating Temperature Range	Package
MC13110FB	T_A = – 40° to +85°C	QFP–52

Simplified Application



This device contains 8,262 active transistors.

Figure 1. Test Circuit



MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.5 to +5.5	Vdc
Junction Temperature	T_J	−65 to +150	°C

NOTE: Devices should not be operated at these limits. The "Recommended Operating Conditions" provide for actual device operation.

RECOMMENDED OPERATING CONDITIONS

Characteristic	Min	Typ	Max	Unit
V_{CC}	2.7	3.6	5.5	Vdc
Operating Ambient Temperature	−40	–	85	°C

NOTE: All limits are not necessarily functional concurrently.

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 3.6 V, T_A = 25°C, unless otherwise specified; Test Circuit Figure 1.)

Characteristic	Min	Typ	Max	Unit
Static Current				
Active Mode	–	8.2	12	mA
Receive Mode	–	4.1	5.5	mA
Standby Mode	–	350	750	µA
Inactive Mode	–	60	100	µA

PIN FUNCTION DESCRIPTION

Pin	Symbol	Type	Description
1 2	LO_2 In LO2 Out	–	These pins form the PLL reference oscillator when connected to an external parallel–resonant crystal (10.24 MHz typical). The reference oscillator is also the second Local Oscillator (LO_2) for the RF receiver. "LO_2 In" may also serve as an input for an externally generated reference signal which is typically ac–coupled.
3	V_{ag}	–	Internal reference voltage for switched capacitor filter section.
4	R_X PD	Output	Three state voltage output of the R_X Phase Detector. This pin is either "high", "low", or "high impedance" depending on the phase difference of the phase detector input signals. During lock, very narrow pulses with a frequency equal to the reference frequency are present. This pin drives the external R_X PLL loop filter.
5	PLL V_{ref}	–	PLL voltage regulator output pin. An internal voltage regulator provides a stable power supply voltage for the R_X and T_X PLL's.
6	T_X PD	Output	Three state voltage output of the T_X Phase Detector. This pin is either "high", "low", or "high impedance" depending on the phase difference of the phase detector input signals. During lock, very narrow pulses with a frequency equal to the reference frequency are present. This pin drives the external T_X PLL loop filter.
7	Gnd PLL	Gnd	Ground pin for PLL section of IC.
8	T_X VCO	Input	Transmit divide counter input which is driven by an ac–coupled external transmit loop VCO. The minimum signal level is 200 mV_{pp} @ 60.0 MHz. This pin also functions as the test mode input for the counter tests.
9 10 11	Data EN Clk	Input	Microprocessor serial interface input pins for programming various counters and control functions.
12	Clk Out	Output	Microprocessor Clock Output which is derived from the 2nd LO crystal oscillator and a programmable divider with divide ratios of 2.0 to 5.0. It can be used to drive a microprocessor and thereby reduce the number of crystals required in the system design.
13	CD Out HWI	I/O	Carrier Detect open collector output and hardware interrupt.
14	BD_1 Out	Output	Open collector output of Battery Detect #1.
15	DA Out	Output	Data Amp output (open collector with internal 100 kΩ pull–up resistor).
16	BD_2 Out	Output	Open collector output of Battery Detect #2.
17	T_X Out	Output	T_X path audio output.
18	C Cap	–	Compressor rectifier filter capacitor pin.

PIN FUNCTION DESCRIPTION (continued)

Pin	Symbol	Type	Description
19	C In	Input	Compressor input (ac–coupled).
20	Amp Out	Output	Mic Amp Output.
21	T_X In	Input	T_X path input to Mic Amp (ac–coupled).
22	DA In	Input	Data Amp input (ac–coupled).
23	V_{CC} Audio	Supply	V_{CC} supply for audio section.
24	R_X Audio In	Input	R_X audio input (ac–coupled).
25	Det Out	Output	Audio output from FM detector.
26	RSSI	Output	Receive Signal Strength Indicator filter capacitor.
27 28	Q Coil Lim Out	–	A quad coil or ceramic discriminator are connected to these pins as part of the FM demodulator circuit.
29	V_{CC} RF	Supply	V_{CC} supply for RF receiver section.
30 31	Lim C_2 Lim C_1	–	IF amplifier/limiter capacitor pins.
32	Lim In	Input	Signal input for IF amplifier/limiter.
33	SGND RF	Gnd	Substrate ground pin for RF section of the IC.
34	Mix_2 In	Input	Second mixer input.
35	Mix_2 Out	Output	Second mixer output.
36	Gnd RF	Gnd	Ground pin for RF section of the IC.
37	Mix_1 Out	Output	First mixer output.
38	Mix_1 In_2	Input	Negative phase first mixer input.
39	Mix_1 In_1	Input	Positive phase first mixer input.
40 41	LO_1 In LO_1 Out	–	Tank Elements for 1st LO Multivibrator Oscillator are connected to these pints.
42	V_{cap} Ctrl	–	1st LO Varactor Control Pin.
43	Gnd Audio	Gnd	Ground for audio section of the IC.
44	SA Out_1	Output	Speaker amp positive phase output.
45	SA In	Input	Speaker amp input.
46	E Out	Output	Expandor output.
47	E_{cap}	–	Expandor rectifier filter capacitor pin.
48	E In	Input	Expandor Input.
49	Scr Out	Output	R_X Scrambler Output.
50	Ref_2	–	Reference voltage input for Battery Detect #2.
51	Ref_1	–	Reference voltage input for Battery Detect #1.
52	V_B	–	Internal reference voltage.

Power Supply Voltage

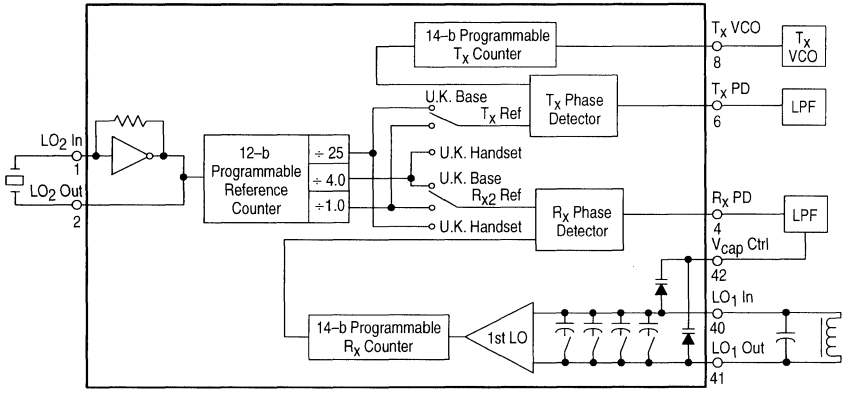
This circuit is used in a cordless telephone handset and base unit. The handset is battery powered and can operate on three NiCad cells.

PLL Frequency Synthesizer General Description

Figure 2 shows a simplified block diagram of the programmable universal dual phase locked loop (PLL). This dual PLL is fully programmable through the MCU serial interface and supports most country channel frequencies including USA (25 ch), Spain, Australia, Korea, New Zealand, U. K., Netherlands, France, and China.

The 2nd local oscillator and reference divider provide the reference frequency for the receive (R_X) and transmit (T_X) PLL loops. The programmed divider value for the reference divider is selected based on the crystal frequency and the desired R_X and T_X reference frequency values. Additional divide by 25 and divide by 4 blocks are provided to allow for generation of the 1.0 kHz and 6.25 kHz reference frequencies required for the U. K. The 14–bit T_X counter is programmed for the desired transmit channel frequency. The 14–bit R_X counter is programmed for the desired first local oscillator frequency. All counters power up in the proper default state for USA channel #6 and for a 10.24 MHz reference frequency crystal. Internal fixed capacitors can be connected to the tank circuit of the 1st LO through microprocessor control to extend the sensitivity of the 1st LO for U.S. 25 channel operation.

Figure 2. Dual PLL Simplified Block Diagram

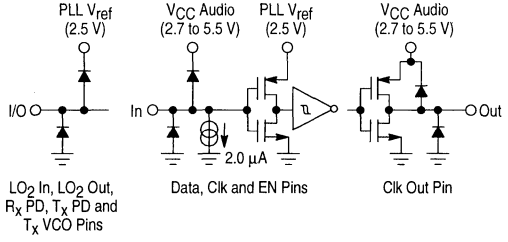


2

PLL I/O Pin Specifications

The 2nd LO, R_X and T_X PLL's, and MPU serial interface are powered by the internal voltage regulator at the "PLL V_{ref}" pin. The "PLL V_{ref}" pin is the output of a voltage regulator which is powered from the "V_{CC} Audio" power supply pin and is regulated by an internal bandgap voltage reference. Therefore, the maximum input and output levels for most PLL I/O pins (LO_2 In, LO_2 Out, R_X PD, T_X PD, T_X VCO) is the regulated voltage at the "PLL V_{ref}" pin. The ESD protection diodes on these pins are also connected to "PLL V_{ref}". Internal level shift buffers are provided for the pins (Data, Clk, EN, Clk Out) which connect directly to the microprocessor. The maximum input and output levels for these pins is V_{CC}. Figure 3 shows a simplified schematic of the I/O pins.

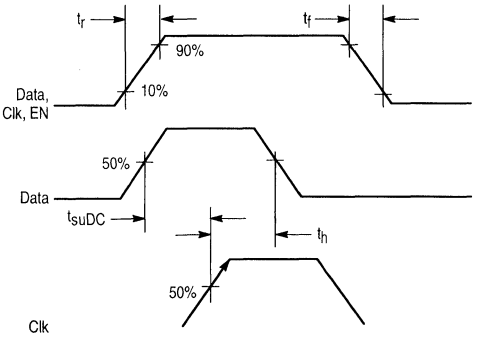
Figure 3. PLL I/O Pin Simplified Schematics



Microprocessor Serial Interface

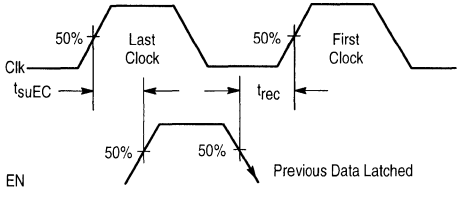
The "Data", "Clk", and "EN" pins provide an MPU serial interface for programming the reference counters, the transmit and receive channel divider counters, the switched capacitor filter clock counter, and various control functions. The "Data" and "Clk" pins are used to load data into the shift register. Figure 4 shows the timing required on the "Data" and "Clk" pins. Data is clocked into the shift register on positive clock transitions.

Figure 4. Data and Clock Timing Requirement



After data is loaded into the shift register, the data is latched into the appropriate latch register using the "EN" pin. This is done in two steps. First, an 8–bit address is loaded into the shift register and latched into the 8–bit address latch register. Then, up to 16–bits of data is loaded into the shift register and latched into the data latch register specified by the address that was previously loaded. Figure 5 shows the timing required on the EN pin. Latching occurs on the negative EN transition.

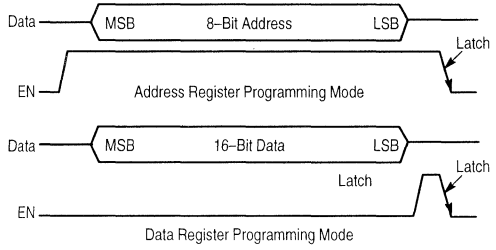
Figure 5. Enable Timing Requirement



The state of the EN pin when clocking data into the shift register determines whether the data is latched into the address register or a data register. Figure 6 shows the

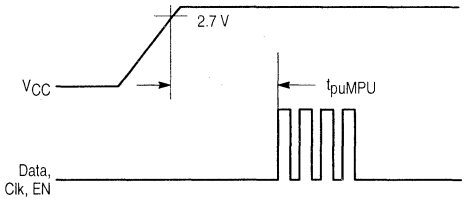
address and data programming diagrams. In the data programming mode, there must not be any clock transitions when "EN" is high. The clock can be in a high state (default high) or a low state (default low) but must not have any transitions during the "EN" high state. The convention in these figures is that latch bits to the left are loaded into the shift register first.

Figure 6. Microprocessor Interface Programming Mode Diagrams



The MPU serial interface is fully operational within 100 µs after the power supply has reached its minimum level during power–up (See Figure 7). The MPU Interface shift registers and data latches are operational in all four power saving modes; Inactive, Standby, R_X, and Active Modes. Data can be loaded into the shift registers and latched into the latch registers in any of the operating modes.

Figure 7. Microprocessor Serial Interface Power–Up Delay



Data Registers

Figure 8 shows shows the data latch registers and addresses which are used to select each of these registers. Latch bits to the left (MSB) are loaded into the shift register first. The LSB bit must always be the last bit loaded into the shift register. Bits preceeding the register must be "0's" as shown in Figure 8.

Figure 8. Microprocessor Interface Data Latch Registers

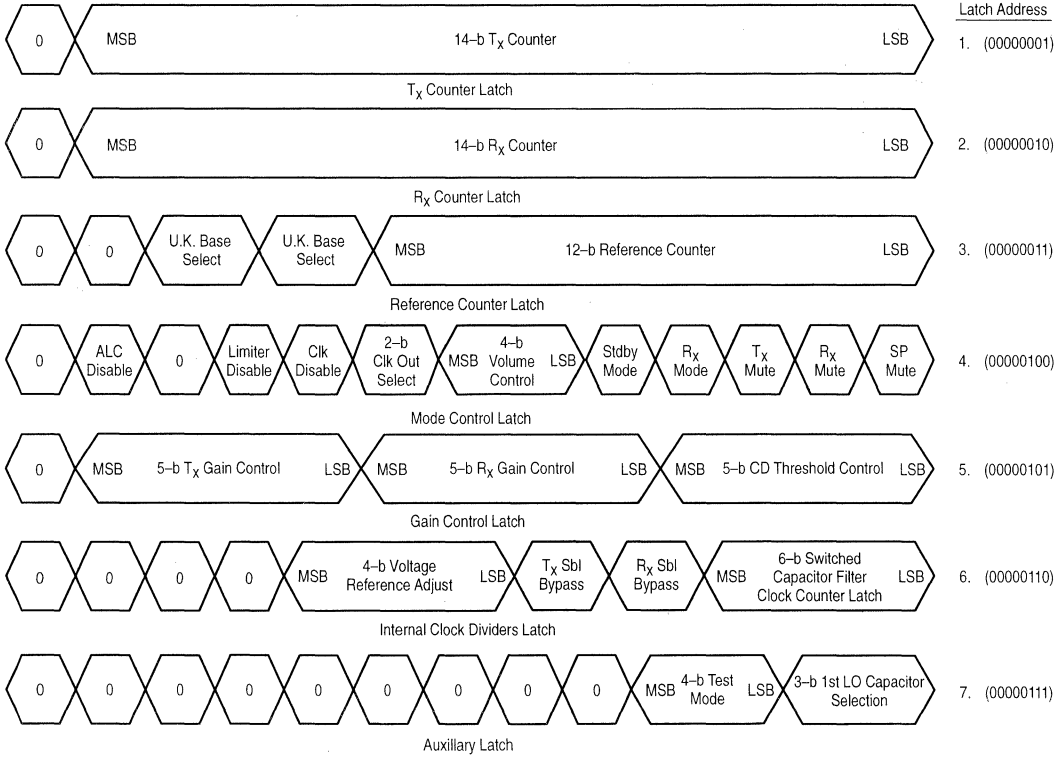


Figure 9. Reference Frequency and Reference Divider Values

Crystal Frequency	Reference Divider Value	U.K. Base/ Handset Divider	Reference Frequency	SC Filter Clock Divider	SC Filter Clock Frequency	Scrambler Modulation Divider	Scrambler Modulation Frequency
10.24 MHz	2048	1.0	5.0 kHz	31	165.16 kHz	40	4.129 kHz
10.24 MHz	1024	4.0	2.5 kHz	31	165.16 kHz	40	4.129 kHz
11.15 MHz	2230	1.0	5.0 kHz	34	163.97 kHz	40	4.099 kHz
12.00 MHz	2400	1.0	5.0 kHz	36	166.67 kHz	40	4.167 kHz
11.15 MHz	1784	1.0	6.25 kHz	34	163.97 kHz	40	4.099 kHz
11.15 MHz	446	4.0	6.25 kHz	34	163.97 kHz	40	4.099 kHz
11.15 MHz	446	25	1.0 kHz	34	163.97 kHz	40	4.099 kHz

2

Reference Frequency Selection

The "LO_2 In" and "LO_2 Out" pins form a reference oscillator when connected to an external parallel–resonant crystal. The reference oscillator is also the second local oscillator for the RF Receiver. Figure 9 shows the relationship between different crystal frequencies and reference frequencies for cordless phone applications in various countries. "LO_2 In" may also serve as an input for an externally generated reference signal which is ac–coupled. The switched capacitor filter 6–bit programmable counter must be programmed for the crystal frequency that is selected since this clock is derived from the crystal frequency and must be held constant regardless of the crystal that is selected. The actual switched capacitor clock divider ratio is twice the programmed divider ratio since there is a fixed divide by 2.0 after the programmable counter. The scrambler mixer modulation frequency is the switched capacitor clock divided by 40.

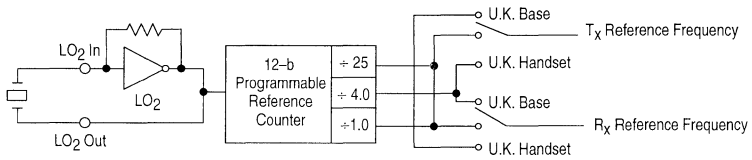
Reference Counter

Figure 10 shows how the reference frequencies for the R_X and T_X loops are generated. All countries except the U.K. require that the T_X and R_X reference frequencies be identical. In this case, set "U.K. Base Select" and "U.K. Handset Select" bits to "0". Then the fixed divider is set to "1" and the T_X and R_X reference frequencies will be equal to the crystal oscillator frequency divided by the programmable reference counter value. The U.K. is a special case which requires a different reference frequency value for T_X and R_X. For U.K. base operation, set "U.K. Base Select" to "1". For U.K. handset operation, set "U.K. Handset Select" to "1".The Netherlands is also a special case since a 2.5 kHz reference frequency is used for both the T_X and R_X reference and the total divider value required is 4096 which is larger than the maximum divide value available from the 12–bit reference divider (4095). In this case, set "U.K. Base Select" to "1" and set "U.K. Handset Select" to "1". This will give a fixed divide by 4 for both the T_X and R_X reference. Then set the reference divider to 1024 to get a total divider of 4096.

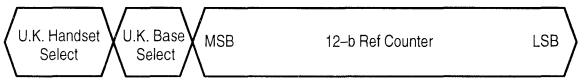
Mode Control Register

Power saving modes, mutes, disables, volume control, and microprocessor clock output frequency are all set by the Control Register. Operation of the Control Register is explained in Figures 11 through 18.

Figure 10. Reference Register Programming Mode



U.K. Handset Select	U.K. Base Select	T_X Divider Value	R_X Divider Value	Application
0	0	1.0	1.0	All but U.K. and Netherlands
0	1	25	4.0	U.K. Base Set
1	0	4.0	25	U.K. Hand Set
1	1	4.0	4.0	Netherlands Base and Hand Set



14–Bit Reference Counter Latch

Figure 11. Control Register Bits

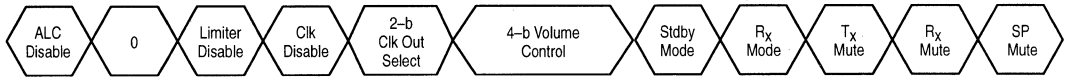


Figure 12. Mute and Disable Control Bit Descriptions

ALC Disable	1 0	Automatic Level Control Disabled Normal Operation
Limiter Disable	1 0	Limiter Disabled Normal Operation
Clock Disable	1 0	MPU Clock Output Disabled Normal Operation
T_X Mute	1 0	Transmit Channel Muted Normal Operation
R_X Mute	1 0	Receive Channel Muted Normal Operation
SP Mute	1 0	Speaker Amp Muted Normal Operation

Power Saving Operating Modes

When the MC13110 is used in a handset, it is important to conserve power in order to prolong battery life. There are five modes of operation; Active, R_X, Standby, Interrupt, and Inactive. In Active mode, all circuit blocks are powered. In R_X mode, all circuitry is powered down except for those circuit sections needed to receive a transmission from the base. In the Standby and Interrupt Modes, all circuitry is powered down except for the circuitry needed to provide the clock output for the microprocessor. In Inactive Mode, all circuitry is powered down except the MPU interface. Latch memory is maintained in all modes. Figure 13 shows the control register bit values for selection of each power saving mode and Figure 14 shows the circuit blocks which are powered in each of these operating modes.

Figure 13. Power Saving Mode Selection

Stdby Mode Bit	R_X Mode Bit	"CD Out/ Hardware Interrupt" Pin	Mode
0	0	X	Active
0	1	X	R_X
1	0	X	Standby
1	1	1 or High Impedance	Inactive
1	1	0	Interrupt

Figure 14. Power Saving Modes

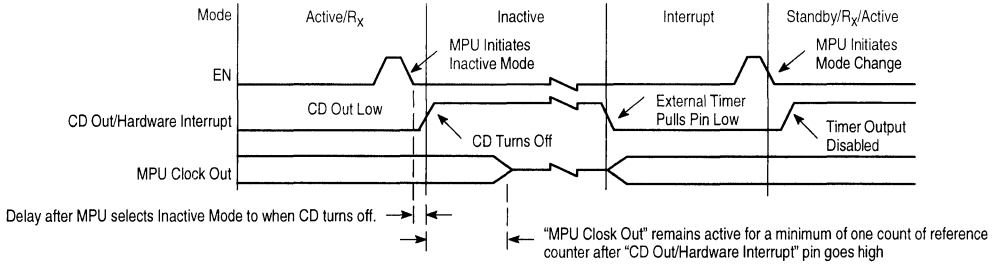
Circuit Blocks	Active	R_X	Standby	Inactive
"PLL V_{ref}" Regulated Voltage	X	X	X[1]	X[1]
MPU Interface	X	X	X	X
2nd LO Oscillator	X	X	X	
MPU Clock Output	X	X	X	
RF Receiver and 1st LO VCO	X	X		
R_X PLL	X	X		
Carrier Detect	X	X		
Data Amp	X	X		
Low Battery Detect	X	X		
T_X PLL	X			
R_X and T_X Audio Paths	X			

NOTE: In Standby and Inactive Modes, "PLL V_{ref}" remains powered but is not regulated. It will fluctuate with V_{CC}.

Inactive Mode Operation and Hardware Interrupt

In some handset applications it may be desirable to power down all circuitry including the microprocessor (MPU). First put the combo IC into the Inactive mode, which turns off the MPU Clock Output (See Figure 15), and then disable the microprocessor. In order to give the MPU adequate time to power down, the MPU Clock output remains active for a minimum of one reference counter cycle (about 200 μs) after the command is given to switch into the "Inactive" mode. An external timing circuit should be used to initiate the turn–on sequence. The "CD Out" pin has a dual function. In the Active and R_X modes it performs the carrier detect function. In the Standby and Inactive modes the carrier detect circuit is disabled and the "CD Out" pin is in a "High" state due to the external pull–up resistor. In the Inactive mode, the "CD Out" pin is the input for the hardware interrupt function. When the "CD Out" pin is pulled "low" by the external timing circuit, the combo IC switches from the Inactive to the Interrupt mode thereby turning on the MPU Clock Output. The MPU can then resume control of the combo IC. The "CD Out" pin must remain low until the MPU changes the operating mode from Interrupt to Standby, Active or R_X modes.

Figure 15. Hardware Interrupt Operation



2

MPU "Clk Out" Divider Programming

This pin is a clock output which is derived from the crystal oscillator (2nd local oscillator). It can be used to drive a microprocessor and thereby reduce the number of crystals required. Figure 15 shows the relationship between the crystal frequency and the clock output for different divider values. Figure 16 shows the "Clk Out" register bit values.

Figure 16. Clock Output Values

Crystal Frequency	Clock Output Divider			
	2	3	4	5
10.24 MHz	5.120 MHz	3.413 MHz	2.560 MHz	2.048 MHz
11.15 MHz	5.575 MHz	3.717 MHz	2.788 MHz	2.230 MHz
12.00 MHz	6.000 MHz	4.000 MHz	3.000 MHz	2.400 MHz

MPU "Clk Out" Radiated Noise on Circuit Board

The clock line running between the MC13110 and the microprocessor has the potential to radiate noise which can cause problems in the system especially if the clock is a square wave digital signal with large high frequency harmonics. In order to minimize radiated noise, a 1.0 kΩ resistor is included on–chip in series with the "Clk Out" output driver. A small capacitor can be connected to the "Clk Out" line on the PCB to form a single pole low pass filter. This filter will significantly reduce noise radiated from the "Clk Out" line.

Volume Control Programming

The volume control adjustable gain block can be programmed in 2.0 dB gain steps from –14 dB to +16 dB. The power–up default value is 0 dB.

Figure 17. Clock Output Divider

Clk Out Bit #1	Clk Out Bit #0	Clk Out Divider Value
0	0	2
0	1	3
1	0	4
1	1	5

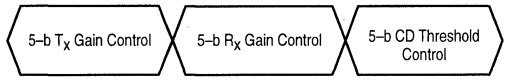
Figure 18. Volume Control

Volume Control Bit #3	Volume Control Bit #2	Volume Control Bit #1	Volume Control Bit #0	Volume Control #	Gain/Attenuation Amount
0	0	0	0	0	–14 dB
0	0	0	1	1	–12 dB
0	0	1	0	2	–10 dB
0	0	1	1	3	–8.0 dB
0	1	0	0	4	–6.0 dB
0	1	0	1	5	–4.0 dB
0	1	1	0	6	–2.0 dB
0	1	1	1	7	0 dB
1	0	0	0	8	2.0 dB
1	0	0	1	9	4.0 dB
1	0	1	0	10	6.0 dB
1	0	1	1	11	8.0 dB
1	1	0	0	12	10 dB
1	1	0	1	13	12 dB
1	1	1	0	14	14 dB
1	1	1	1	15	16 dB

Gain Control Register

The gain control register contains bits which control the T_X Voltage Gain, R_X Voltage Gain, and Carrier Detect threshold. Operation of these latch bits are explained in Figures 19, 20, and 21.

Figure 19. Gain Control Latch Bits



T_X and R_X Gain Programming

The T_X and R_X audio signal paths each have a programmable gain block. If a T_X or R_X voltage gain other than the nominal power–up default is desired, it can be programmed through the MPU interface. Alternately, these programmable gain blocks can be used during final test of the telephone to electronically adjust for gain tolerances in the telephone system as shown in Figure 20. In this case, the T_X and R_X gain register values should be stored in ROM during final test so that they can be reloaded each time the combo IC is powered up.

Figure 20. T_X and R_X Gain Control

Gain Control Bit #4	Gain Control Bit #3	Gain Control Bit #2	Gain Control Bit #1	Gain Control Bit #0	Gain Control #	Gain/Attenuation Amount
0	0	0	0	0	0	–15 dB
0	0	0	0	1	1	–14 dB
0	0	0	1	0	2	–13 dB
0	0	0	1	1	3	–12 dB
0	0	1	0	0	4	–11 dB
0	0	1	0	1	5	–10 dB
0	0	1	1	0	6	–9.0 dB
0	0	1	1	1	7	–8.0 dB
0	1	0	0	0	8	–7.0 dB
0	1	0	0	1	9	–6.0 dB
0	1	0	1	0	10	–5.0 dB
0	1	0	1	1	11	–4.0 dB
0	1	1	0	0	12	–3.0 dB
0	1	1	0	1	13	–2.0 dB
0	1	1	1	0	14	–1.0 dB
0	1	1	1	1	15	0 dB
1	0	0	0	0	16	1.0 dB
1	0	0	0	1	17	2.0 dB
1	0	0	1	0	18	3.0 dB
1	0	0	1	1	19	4.0 dB
1	0	1	0	0	20	5.0 dB
1	0	1	0	1	21	6.0 dB
1	0	1	1	0	22	7.0 dB
1	0	1	1	1	23	8.0 dB
1	1	0	0	0	24	9.0 dB
1	1	0	0	1	25	10 dB
1	1	0	1	0	26	11 dB
1	1	0	1	1	27	12 dB
1	1	1	0	0	28	13 dB
1	1	1	0	1	29	14 dB
1	1	1	1	0	30	15 dB
1	1	1	1	1	31	16 dB

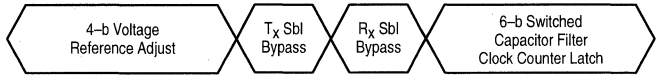
Carrier Detect Threshold Programming

The "CD Out" pin gives an indication to the microprocessor if a carrier signal is present on the selected channel. The nominal value and tolerance of the carrier detect threshold is given in the carrier detect specification section of this document. If a different carrier detect threshold value is desired, it can be programmed through the MPU interface as shown in Figure 21. Alternately, the carrier detect threshold can be electronically adjusted during final test of the telephone to reduce the tolerance of the carrier detect threshold. This is done by measuring the threshold and then by adjusting the threshold through the MPU interface. In this case, it is necessary to store the carrier detect register value in ROM so that the CD register can be reloaded each time the combo IC is powered up.

Figure 21. Carrier Detect Threshold Control

CD Bit #4	CD Bit #3	CD Bit #2	CD Bit #1	CD Bit #0	CD Control #	Carrier Detect Threshold
0	0	0	0	0	0	−20 dB
0	0	0	0	1	1	−19 dB
0	0	0	1	0	2	−18 dB
0	0	0	1	1	3	−17 dB
0	0	1	0	0	4	−16 dB
0	0	1	0	1	5	−15 dB
0	0	1	1	0	6	−14 dB
0	0	1	1	1	7	−13 dB
0	1	0	0	0	8	−12 dB
0	1	0	0	1	9	−11 dB
0	1	0	1	0	10	−10 dB
0	1	0	1	1	11	−9.0 dB
0	1	1	0	0	12	−8.0 dB
0	1	1	0	1	13	−7.0 dB
0	1	1	1	0	14	−6.0 dB
0	1	1	1	1	15	−5.0 dB
1	0	0	0	0	16	−4.0 dB
1	0	0	0	1	17	−3.0 dB
1	0	0	1	0	18	−2.0 dB
1	0	0	1	1	19	−1.0 dB
1	0	1	0	0	20	0 dB
1	0	1	0	1	21	1.0 dB
1	0	1	1	0	22	2.0 dB
1	0	1	1	1	23	3.0 dB
1	1	0	0	0	24	4.0 dB
1	1	0	0	1	25	5.0 dB
1	1	0	1	0	26	6.0 dB
1	1	0	1	1	27	7.0 dB
1	1	1	0	0	28	8.0 dB
1	1	1	0	1	29	9.0 dB
1	1	1	1	0	30	10 dB
1	1	1	1	1	31	11 dB

Figure 22. Switched Capacitor Filter Clock Divider/Voltage Reference Adjust Latch Bits



2

Switched Capacitor Filter Clock Divider/Voltage Reference Adjust Register

This register controls the scrambler bypass mode, the divider value for the programmable switched capacitor filter clock divider, and the voltage reference adjust. Operation is explained in Figures 22 through 27.

Figure 23. Bypass Mode Bit Description

T_X Scrambler Bypass	1	T_X Scrambler Pre–Mixer LPF and Mixer Bypassed
	0	Normal Operation with T_X Scrambler
R_X Scrambler Bypass	1	R_X Scrambler Pre–Mixer LPF and Mixer Bypassed
	0	Normal Operation R_X Scrambler

Switched Capacitor Filter Clock Programming

A block diagram of the switched capacitor filter and scrambler modulation clock dividers is shown in Figure 24. There is a fixed divide by 2 after the programmable divider. The switched capacitor filter clock value is given by the following equation;

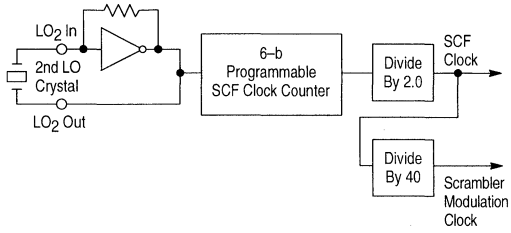
$$(\text{SCF Clock}) = F(\text{2nd LO})/(\text{SCF Divider Value} * 2)$$

The scrambler modulation clock frequency (SMCF) is proportional to the SCF clock and is given by the following equation;

$$\text{SMCF} = (\text{SCF Clock Frequency})/40$$

The SCF divider should be set to a value which gives a SCF Clock as close to 165.16 kHz as possible based on the 2nd LO frequency which is chosen (see Figure 9).

Figure 24. SCF Clock and Scrambler Carrier Circuit



Scrambler Modulation Frequency Programming

Four different scrambler modulation frequencies may be selected by programming the SCF Clock divider as shown in Figures 25 and 26. Note that all filter corner frequencies will change proportionately with the SCF Clock and Scrambler Modulation Frequency. The power–up default SCF Clock divider value is 31.

Figure 25. Scrambler Modulation Frequency Programming for a 10.240 MHz 2nd LO

SCF Clock Divider	Total Divide Value	SCF Clock Freq. (kHz)	Scrambler Modulation Frequency (Clk/40) (kHz)	Scrambler Lower Corner Frequency (Hz)	Scrambler Upper Corner Frequency (kHz)
29	58	176.55	4.414	267.2	3.902
30	60	170.67	4.267	258.3	3.772
31	62	165.16	4.129	250.0	3.650
32	64	160.00	4.000	242.2	3.536

NOTE: All filter corner frequencies have a tolerance of ±3%.

Figure 26. Scrambler Modulation Frequency Programming for a 11.15 MHz 2nd LO

SCF Clock Divider	Total Divide Value	SCF Clock Freq. (kHz)	Scrambler Modulation Frequency (Clk/40) (kHz)	Scrambler Lower Corner Frequency (Hz)	Scrambler Upper Corner Frequency (kHz)
32	64	174.22	4.355	263.7	3.850
33	66	168.94	4.223	255.7	3.733
34	68	163.97	4.099	248.2	3.624
35	70	159.29	3.982	241.1	3.520

NOTE: All filter corner frequencies have a tolerance of ±3%.

Voltage Reference Adjustment

The internal 1.5 V Bandgap voltage reference provides the voltage reference for the "BD1 Out" and "BD2 Out" low battery detect circuits, the "PLL V_{ref}" voltage regulator, the "V_B" reference, and all internal analog ground references. The initial tolerance of the Bandgap voltage reference is ±6%. The tolerance of the internal reference voltage can be improved to ±1.5% through MPU serial interface programming.

During final test of the telephone, the battery detect threshold is measured. Then, the internal reference voltage value is adjusted electronically through the MPU serial interface to achieve the desired accuracy level. The voltage reference register value should be stored in ROM during final test so that it can be reloaded each time the MC13110 is powered up (see Figure 27).

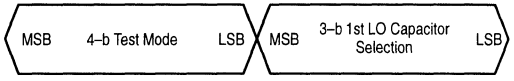
Figure 27. Bandgap Voltage Reference Adjustment

V_{ref} Adj. Bit #3	V_{ref} Adj. Bit #2	V_{ref} Adj. Bit #1	V_{ref} Adj. Bit #0	V_{ref} Adj. #	V_{ref} Adj. Amount
0	0	0	0	0	–9.0%
0	0	0	1	1	–7.8%
0	0	1	0	2	–6.6%
0	0	1	1	3	–5.4%
0	1	0	0	4	–4.2%
0	1	0	1	5	–3.0%
0	1	1	0	6	–1.8%
0	1	1	1	7	–0.6%
1	0	0	0	8	+0.6 %
1	0	0	1	9	+1.8 %
1	0	1	0	10	+3.0 %
1	0	1	1	11	+4.2 %
1	1	0	0	12	+5.4 %
1	1	0	1	13	+6.6 %
1	1	1	0	14	+7.8 %
1	1	1	1	15	+9.0 %

Auxiliary Register

The auxiliary register contains a 3 bit 1st LO Capacitor Selection latch and a 4 bit Test Mode latch. Operation of these latch bits are explained in Figures 28, 29 and 30.

Figure 28. Auxiliary Register Latch Bits



First Local Oscillator Capacitor Selection for 25 Channel U.S. Operation

There is a very large frequency difference between the minimum and maximum channel frequencies in the 25 Channel U.S. standard. The sensitivity of the 1st LO is not large enough to accommodate this large frequency variation. Fixed capacitors can be connected across the 1st LO tank circuit to change the 1st LO sensitivity. Internal switches and capacitors are provided to enable microprocessor control over internal fixed capacitor values. Figure 29 shows the schematic of the 1st LO tank circuit. Figure 30 shows the latch control bit values.

Figure 29. 1st LO Schematic

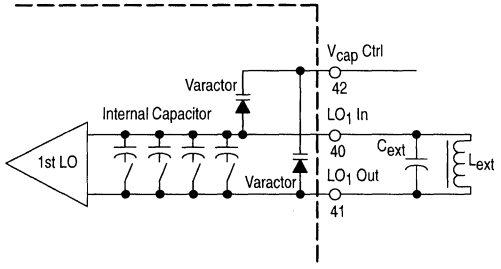


Figure 30. 1st LO Capacitor Select for U.S. 25 Channels

1st LO Cap. Bit 2	1st LO Cap. Bit 1	1st LO Cap Bit 0	1st LO Cap. Select	U.S. Base Channels	U.S. Handset Channels	Internal Capacitor Value	Varactor Value over 0.5 to 2.5 V	External Capacitor Value	External Inductor Value
0	0	0	0	1 – 10	–	0.76 pF	10 – 6.4 pF	27 pF	0.47 µH
0	0	0	0	–	1 – 10	0.76 pF	10 – 6.4 pF	33 pF	0.47 µH
0	0	1	1	11 – 16	–	1.64 pF	10 – 6.4 pF	27 pF	0.47 µH
0	1	0	2	17 – 25	–	0.86 pF	10 – 6.4 pF	27 pF	0.47 µH
0	1	1	3	–	11 – 16	7.63 pF	10 – 6.4 pF	33 pF	0.47 µH
1	0	0	4	–	17 – 25	6.01 pF	10 – 6.4 pF	33 pF	0.47 µH

Figure 31. Digital Test Mode Description

TM #	TM 3	TM 2	TM 1	TM 0	Counter Under Test or Test Mode Option	"T_X V_{CO}" Input Signal	"Clk Out" Output Expected
0	0	0	0	0	Normal Operation	>200 mV_{pp}	–
1	0	0	0	1	R_X Counter, upper 6	0 to 2.5 V	Input Frequency/64
2	0	0	1	0	R_X Counter, lower 8	0 to 2.5 V	See Note Below
3	0	0	1	1	R_X Prescaler	0 to 2.5 V	Input Frequency/4
4	0	1	0	0	T_X Counter, upper 6	0 to 2.5 V	Input Frequency/64
5	0	1	0	1	T_X Counter, lower 8	0 to 2.5 V	See Note Below
6	0	1	1	0	T_X Prescaler	>200 mV_{pp}	Input Frequency/4
7	0	1	1	1	Reference Counter	0 to 2.5 V	Input Frequency/Reference Counter Value
8	1	0	0	0	Divide by 4, 25	0 to 2.5 V	Input Frequency/100
9	1	0	0	1	SC Counter	0 to 2.5 V	Input Frequency/SC Counter Value
10	1	0	1	0	Scrambler Modulation Counter	0 to 2.5 V	Input Frequency/40

NOTE: To determine the correct output, look at the lower 8 bits in the R_X or T_X register (Divisor (7;0). If the value of the divisor is > 16, then the output divisor value is Divisor (7;2) (the upper 6 bits of the divisor). If Divisor (7;0) < 16 and Divisor (3;2) > = 2, then output divisor value is Divisor (3;2) (bits 2 and 3 of the divisor). If Divisor (7;0) < 16 and Divisor (3;2) < 2, then output divisor value is (Divisor (3;2) + 60).

Figure 32. Analog Test Mode Description

TM #	TM 3	TM 2	TM 1	TM 0	Circuit Blocks Under Test	Input Pin	Output Pin
11	1	0	1	1	Compresser	C In	T_X In
12	1	1	0	0	T_X Scrambler	T_X In	T_X Out
13	1	1	0	1	ALC Gain = 10 Option	N/A	N/A
14	1	1	1	0	ALC Gain = 25 Option	N/A	N/A
15	1	1	1	1	Not Used	N/A	N/A

Test Modes

Digital and analog test modes can be selected through the 4–bit Test Mode Register. In digital test mode, the "T_X V_{CO}" input pin is multiplexed to the input of the counter under test and the output of the counter under test is multiplexed to the "Clk Out" output pin so that each counter can be individually tested. Make sure test mode bits are set to "0's" for normal operation. Digital test mode operation is described in Figure 31. During normal operation and when testing the T_X Prescaler, the "T_X VCO" input can be a minimum of 200 mV_{pp} at 80 MHz and should be ac–coupled. For other test modes, input signals should be standard logic levels of 0 to 2.5 V and a maximum frequency of 16 MHz.

The analog test modes enable separate testing of the Compresser and T_X Scrambler blocks as shown in Figure 32. Also, ALC Gain options can be selected through analog test modes.

Power–Up Defaults for Control and Counter Registers

When the IC is first powered up, all latch registers are initialized to a defined state. The device is initially placed in the Rx mode with all mutes active. The reference counter is set to generate a 5.0 kHz reference frequency from a 10.24 MHz crystal. The switched capacitor filter clock counter is set properly for operation with a 10.24 MHz crystal. The scrambler bypass mode control are set for normal operation of scrambler. The T_X and R_X latch registers are set for USA Channel Frequency #6. Figure 33 shows the initial power–up states for all latch registers.

Figure 33. Latch Register Power–Up Defaults

		MSB								LSB							
Register	Count	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
T_X	9966	–	–	1	0	0	1	1	0	1	1	1	0	1	1	1	0
R_X	7215	–	–	0	1	1	1	0	0	0	0	1	0	1	1	1	1
Ref	2048	–	–	0	0	1	0	0	0	0	0	0	0	0	0	0	0
Mode	N/A	–	0	X	0	0	1	1	0	1	1	1	0	1	1	1	1
Gain	N/A	–	0	1	1	1	1	0	1	1	1	1	1	0	1	0	0
SC	31	–	–	–	–	0	1	1	1	0	0	0	1	1	1	1	1
TM	N/A	–	–	–	–	–	–	–	–	–	0	0	0	0	0	0	0

APPLICATIONS INFORMATION

Evaluation PC Board

The PCB should be double sided with a full ground plane on one side; any leaded components are inserted on the ground plane side. This affords shielding and isolation from the circuit side of the PCB. The other side is the circuit side which has the interconnect traces and the surface mount components. In cases where cost allows, it may be benificial to use multi layer boards.

The placement of certain components specified in the application circuits is very critical. These components should be placed first and the other less critical components are fitted in last. In general, all RF paths should be kept as short as possible, ground pins should be grounded at the pins and V_{CC} pins should have adequate decoupling to ground at the pins. In mixed mode systems where digital and RF/Analog circuitry are present, the V_{EE} and V_{CC} busses are isolated ac –wise from each other.

Component Selection

The evaluation PC board is designed to accommodate specific components, while in some cases it is versatile enough to use components from various manufacturers and coil types. The application circuit schematics specify particular components that were used to achieve the results shown in the typical curves and tables, but alternate components should give similar results.

The MC13110 "Combo" is capable of matching the sensitivity, IMD, adjacent channel rejection, and other performance criteria of a multi–chip analog cordless telephone system. For the most part, the same external components are used as in the multi–chip solution. In the following discussion, various parts of the system are analyzed for best peformance and cost tradeoffs. Specific recommendations are made where certain components or circuit designs offer superior performance. The system analyzed is the USA "CT–1" cordless phone.

Input Matching/Sensitivity

The sensitivity of the "Combo" is typically 1.0 μVrms matched with no preamp. To achieve suitable system performance, a preamp and passive duplexer must be used. In production final test, each section of the IC is separately tested to guarantee its system performance in the specific application. The preamp and duplexer yields typically –116 dBm 12 dB SINAD sensitivity performance under full duplex operation.

The duplexer is important to achieve full duplex operation without significant "desensing" of the receiver by the transmitter. The combination of the duplexer and preamp circuit have to attenuate the transmitter power to the receiver by over 60 dB to be effective. They do this while improving the receiver system noise figure and without giving up too much IMD performance.

The duplexer may be a single piece unit offered by Shimida and Sansui products (designed for 10 channel CT–1 cordless phone) or a two piece solution offered by Toko (designed for 25 channel operation). The duplexer frequency response at the receiver port has a notch at the transmitter frequency band of about 35 to 40 dB with a 2.0 to 3.0 dB insertion loss at the receiver frequency band.

The preamp circuit utilizes a tuned transformer at the output side of the amplifier; this transformer is designed to bandpass filter the receiver input frequency while rejecting the transmitter frequency. The tuned preamp also improves the noise performance by reducing the bandwidth of the pass band and reducing the second stage contribution of the 1st mixer. The preamp is biased at about 1.0 mA and 3.0 Vdc which yields suitable noise figure and gain.

Mixers

The 1st and 2nd mixers are similar in design. Both are double balanced to suppress the LO and the input frequencies to give only the sum and difference frequencies out. Typically the LO is suppressed about 40 to 60 dB. The 1st mixer may be driven either differentially or single ended. The gain of the 1st mixer has a 3.0 dB corner at 20 MHz and is used at a 10.7 MHz IF. It has an output impedance of 330 Ω and matches to a typical 10.7 MHz ceramic filter with a source and load impedance of 330 Ω. A series resistor may be used to raise the impedance for use with crystal filters which typically have an input impedance much greater than 330 Ω. The 2nd mixer input impedance is typically 3.0 kΩ; it requires an external 360 Ω parallel resistor for use with a standard 330 Ω 10.7 MHz ceramic filter. The second mixer output impedance is 1.5 kΩ making it suitable to match 455 kHz ceramic filters.

1st Local Oscillators

The 1st local oscillator is a multi–vibrator oscillator that takes an external capacitance and inductance. It is voltage controlled to an internal varactor from an external loop filter and on–board PLL.

The 2nd LO is a CMOS oscillator similar to that used in the MC145162. The 2nd LO is also used as the PLL reference oscillator. It is designed to utilize an external parallel resonant crystal.

PLL Design

The 1st LO level is important, as well as the choice of the crystal for the PLL clock reference and 2nd LO. A fundamental, parallel resonant crystal specified with 7.0 to 12 pF load calibration capacitance is recommended. With load calibration capacitance too high, the crystal locks up very slowly. If the LO power is less than –10 dBm, a pull–down resistor at the 1st LO emitter (Pin 41) will increase its drive level. The LO level is primarily a function of the Colpitts capacitive voltage divider formed by the capacitors between the base to emitter and the emitter to ground.

The VCO gain factor expressed in MHz/V is indeed critical to the phase noise performance. If this curve is too steep or too sensitive to changes in control voltage, it may degrade the phase noise performance. The external VCO circuit design needs to consider the typical swing of the control voltage and the corresponding linearity of the transfer function, $\Delta f_{osc}/\Delta V_{control}$. In general, the higher the Q of the VCO circuit inductor, the better phase noise performance.

Adjacent channel rejection and isolation between the 1st and 2nd mixers may be adversely affected due to layout problems and difficulty in getting close to the package pins with the grounds and decoupling capacitors on the RF V_{CC}. These system parameters must be evaluated for sensitivity to layout and external component placement.

Intermodulation and adjacent channel performance problems may also result from spurs around the 1st LO which may be caused by harmonics from the switched capacitor clock driver and too low 1st LO drive level. The clock driver

operates at a frequency which is f(2nd LO)/(2 * (SCF Divider)). The harmonics are n * (f(2nd LO)), where n can be any positive integer. The current spikes of the SCF on the supply lines cause the disturbance of the 1st LO. This may be verified by observing the spurs on a spectrum analyzer while changing the clock divider value. The spur frequencies will change when the divider value is changed. The spurious sideband problem may be avoided by changing the clock divider value via software for each channel where it is a problem. Certain channels are worse than others.

The PLL alignment procedure for the application circuit is detailed in Appendix C. Refer to the MC145162 data sheet for PLL design example.

2

Limiting IF Amplifiers

The limiting IF amplifier typically has about 110 dB of gain; the frequency response starts rolling off at 1.0 MHz. Decoupling capacitors should be placed close to the decoupling Pins 31 and 32 to ensure low noise and stable operation. The IF input impedance is 1.5 kΩ for a suitable match to 455 kHz ceramic filters.

RSSI/Carrier Detect

The Received Signal Strength Indicator (RSSI) indicates the strength of the IF level and the output is proportional to the logarithm of the IF input signal magnitude. The RSSI dynamic range is typically 70 dB. Connect 0.01 µF to GND from "RSSI" output pin to form the carrier detect filter. A resistor needed to convert the RSSI current to voltage is included in the internal circuit. A temperature compensated reference current also improves the RSSI accuracy over temperature.

"CD Out" is an open collector output; thus, an external 100 kΩ pull–up resistor to V_{CC} is recommended. The carrier detect threshold is programmable through the MPU interface.

Quadrature Detector

The quadrature detector is coupled to the IF with an external capacitor between Pins 27 and 28; thus, the recovered signal level output is increased for a given bandwidth by increasing the capacitor. The external quadrature component may be either a LCR resonant circuit, which may be adjustable, or a ceramic resonator which is usually fixed tuned.

The bandwidth performance of the detector is controlled by the loaded Q of the LC tank circuit. The following equation defines the components which set the detector circuit's bandwidth:

$$(1)\quad R_T = Q\,X_L$$

where R_T is the equivalent shunt resistance across the LC Tank. X_L is the reactance of the quadrature inductor at the IF frequency ($X_L = 2\pi fL$).

Specific 455 kHz quadrature LC components are manufactured by Toko in various 5 mm, 7 mm and 10 mm shielded cans in surface mount or leaded packages. Recommended components such as, the 7 mm Toko, is used in the application circuit. When minaturization is a key constraint, a surface mount inductor and capacitor may be chosen to form a resonant LC tank with the PCB and parasitic device capacitance. The 455 kHz IF center frequency is calculated by

$$(2)\quad f_c = \left[2\pi\,(LC_p)^{1/2}\right] - 1$$

where L is the parallel tank inductor. C_p is the equivalent parallel capacitance of the parallel resonant tank circuit.

The following is a design example for a detector at 455 kHz and a specific loaded Q. The loaded Q of the quadrature detector is chosen somewhat less than the Q of the IF bandpass. For an IF frequency of 455 kHz and an IF bandpass of 20 kHz, the IF bandpass Q is approximately 23; the loaded Q of the quadrature tank is chosen at 15.

Example:

Let the total external C = 180 pF. Note: the capacitance may be split between a 150 pF chip capacitor and a 5.0 to 25 pF variable capacitor; this allows for tuning to compensate for component tolerance. Since the external capacitance is much greater than the internal device and PCB parasitic capacitance, the parasitic capacitance may be neglected.

Rewrite equation (2) and solve for L:

$$L = (0.159)^2/(C\,fc^2)$$
$$L = 678\ \mu H\ ;\ \text{Thus, a standard value is chosen:}$$
$$L = 680\ \mu H\ \text{(surface mount inductor)}$$

The value of the total damping resistor to obtain the required loaded Q of 15 can be calculated from equation (1):

$$R_T = Q(2\pi fL)$$
$$R_T = 15\,(2\pi)(0.455)(680) = 29.5\ k\Omega$$

The internal resistance, R_{int} at the quadrature tank Pin 27 is approximately 100 kΩ and is considered in determining the external resistance, R_{ext} which is calculated from

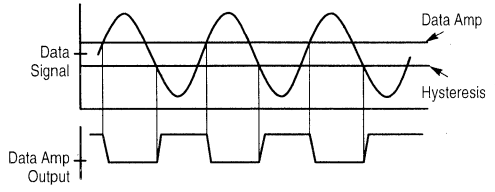
$$R_{ext} = ((R_T)(R_{int}))/(R_{int} - R_T)$$
$$R_{ext} = 41.8\ k\Omega;\ \text{Thus, choose the standard value:}$$
$$R_{ext} = 39\ k\Omega$$

A ceramic discriminator is recommended for the quadrature circuit in applications where fixed tuning is desired. The ceramic discriminator and a 22 k resistor are placed from Pin 27 to V_{CC}. A 10 pF capacitor is placed from Pin 28 to 27 to properly drive the discriminator.

Data Amp Comparator

The data amp comparator is an inverting hysteresis comparator. Its open collector output has an internal 100 kΩ pull–up resistor. A band pass filter is connected between the "Det Out" pin and the "DA In" pin with component values as shown in the circuit block diagram. The "DA In" input signal is ac–coupled.

Figure 34. Data Amp Operation



Expandor/ Compressor

In Appendix B, the EIA/CCITT recommendations for measurement of the attack and decay times are defined. The curves in Figures 35 and 36 show the typical expandor and compressor E Out versus E In responses.

Figure 35. Expandor Typical Response

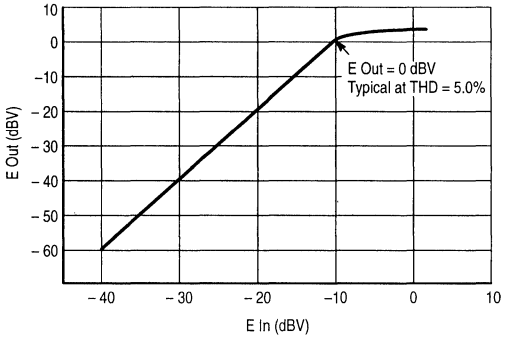
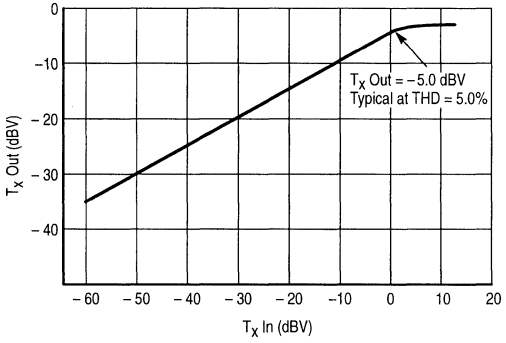


Figure 36. Compressor Typical Response



T_X and R_X Scrambler

The T_X and R_X signal paths each contain a frequency inversion scrambler in the MC13110. Each scrambler contains a pre–mixer low pass switched capacitor filter, a double balanced mixer, and a post–mixer low pass switched capacitor filter. The scrambler function can be defeated by setting the Scramble Bypass bit in the control register to "1" through the MPU interface. In this mode, the mixer and the post–mixer LPF are bypassed and only the pre–mixer LPF remains in the signal path. The switched capacitor filter corner frequencies are proportional to the switched capacitor filter clock. The SCF Clock Divider is programmable through the MPU interface. The (SCF Clock) = F(2nd LO)/(SCF Divider Value*2). The scrambler modulation frequency is (SCF Clock)/40. Four scrambler modulation frequencies may be selected (see Figures 25 and 26).

PLL Voltage Regulator

The "PLL V_{ref}" pin is the internal supply voltage for the R_X and T_X PLL's. It is regulated to a nominal of 2.5 V. The "V_{CC} Audio" pin is the supply voltage for the internal voltage regulator. Two capacitors with 10 μF and 0.01 μF values must be connected to the "PLL Vref" pin to filter and stabilize this regulated voltage. The "PLL V_{ref}" pin may be used to power other IC's as long as the total external load current does not exceed 3.0 mA. The tolerance of the regulated voltage is initially ±8% but is improved to ±4% after the internal Bandgap voltage reference is adjusted electronically through the MPU serial interface.

Low Battery Detect

Two external precision resistor dividers are used to set independent thresholds for two battery detect hysteresis comparators. The voltages on "Ref_1" and "Ref_2" are compared to an internally generated 1.5 V reference voltage. The tolerance of the internal reference voltage is initially ±6%. The tolerance of the internal reference voltage can be improved to ±1.5% through MPU serial interface programming. The internal reference can be measured directly at the "V_B" pin. During final test of the telephone, the V_B internal reference voltage is measured. Then, the internal reference voltage value is adjusted electronically through the MPU serial interface to achieve the desired accuracy level. The voltage reference register value should be stored in ROM during final test so that it can be reloaded each time the MC13110 is powered up. Low Battery Detect outputs are open collector.

MOTOROLA

MC13135
MC13136

FM Communications Receivers

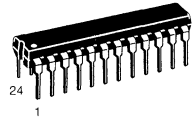
DUAL CONVERSION NARROWBAND FM RECEIVERS

The MC13135/MC13136 are the second generation of single chip, dual conversion FM communications receivers developed by Motorola. Major improvements in signal handling, RSSI and first oscillator operation have been made. In addition, recovered audio distortion and audio drive have improved. Using Motorola's MOSAIC™ 1.5 process, these receivers offer low noise, high gain and stability over a wide operating voltage range.

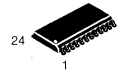
Both the MC13135 and MC13136 include a Colpitts oscillator, VCO tuning diode, low noise first and second mixer and LO, high gain limiting IF, and RSSI. The MC13135 is designed for use with an LC quadrature detector and has an uncommitted op amp that can be used either for an RSSI buffer or as a data comparator. The MC13136 can be used with either a ceramic discriminator or an LC quad coil and the op amp is internally connected for a voltage buffered RSSI output.

These devices can be used as stand–alone VHF receivers or as the lower IF of a triple conversion system. Applications include cordless telephones, short range data links, walkie–talkies, low cost land mobile, amateur radio receivers, baby monitors and scanners.

- Complete Dual Conversion FM Receiver – Antenna to Audio Output
- Input Frequency Range – 200 MHz
- Voltage Buffered RSSI with 70 dB of Usable Range
- Low Voltage Operation – 2.0 to 6.0 Vdc (2 Cell NiCad Supply)
- Low Current Drain – 3.5 mA Typ
- Low Impedance Audio Output < 25 Ω
- VHF Colpitts First LO for Crystal or VCO Operation
- Isolated Tuning Diode
- Buffered First LO Output to Drive CMOS PLL Synthesizer



P SUFFIX
PLASTIC PACKAGE
CASE 724



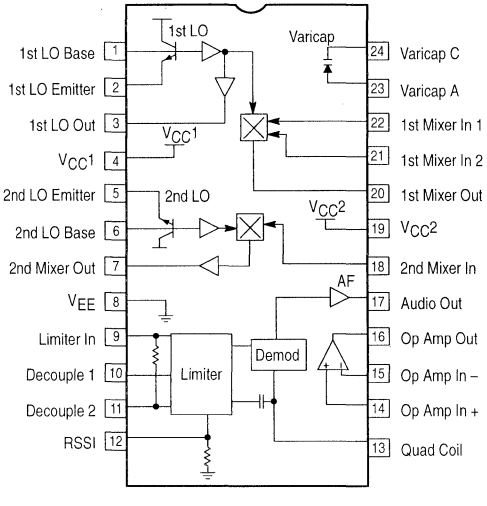
DW SUFFIX
PLASTIC PACKAGE
CASE 751E
(SO–24L)

ORDERING INFORMATION

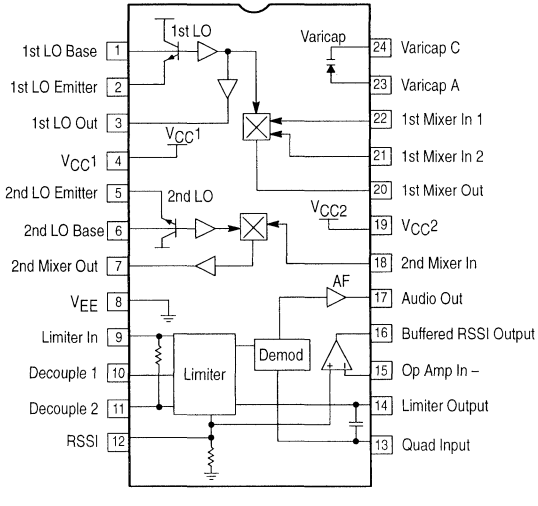
Device	Operating Temperature Range	Package
MC13135P	$T_A = -40°$ to $+85°C$	Plastic DIP
MC13135DW		SO–24L
MC13136P		Plastic DIP
MC13136DW		SO–24L

PIN CONNECTIONS

MC13135



MC13136



Each device contains 142 active transistors.

Rev 2

MAXIMUM RATINGS

Rating	Pin	Symbol	Value	Unit
Power Supply Voltage	4, 19	V_{CC} (max)	6.5	Vdc
RF Input Voltage	22	RF_{in}	1.0	Vrms
Junction Temperature	–	T_J	+150	°C
Storage Temperature Range	–	T_{stg}	– 65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

Rating	Pin	Symbol	Value	Unit
Power Supply Voltage	4, 19	V_{CC}	2.0 to 6.0	Vdc
Maximum 1st IF	–	f_{IF1}	21	MHz
Maximum 2nd IF	–	f_{IF2}	3.0	MHz
Ambient Temperature Range	–	T_A	– 40 to + 85	°C

ELECTRICAL CHARACTERISTICS (T_A=25°C, V_{CC}=4.0 Vdc, f_o=49.7 MHz, f_{MOD}=1.0 kHz, Deviation=±3.0 kHz, f_{1stLO}=39 MHz, f_{2nd} LO=10.245 MHz, IF1=10.7 MHz, IF2=455 kHz, unless otherwise noted. *All measurements performed in the test circuit of Figure 1.*)

Characteristic	Condition	Symbol	Min	Typ	Max	Unit
Total Drain Current	No Input Signal	I_{CC}	–	4.0	6.0	mAdc
Sensitivity (Input for 12 dB SINAD)	Matched Input	V_{SIN}	–	1.0	–	µVrms
Recovered Audio MC13135 MC13136	V_{RF} = 1.0 mV	AF_O	 170 215	 220 265	 300 365	mVrms
Limiter Output Level (Pin 14, MC13136)		V_{LIM}	 –	 130	 –	mVrms
1st Mixer Conversion Gain	V_{RF} = – 40 dBm	MX_{gain1}	–	12	–	dB
2nd Mixer Conversion Gain	V_{RF} = – 40 dBm	MX_{gain2}	–	13	–	dB
First LO Buffered Output	–	V_{LO}	–	100	–	mVrms
Total Harmonic Distortion	V_{RF} = – 30 dBm	THD	–	1.2	3.0	%
Demodulator Bandwidth	–	BW	–	50	–	kHz
RSSI Dynamic Range	–	RSSI	–	70	–	dB
First Mixer 3rd Order Intercept (Input)	 Matched Unmatched	TOI_{Mix1}	 – –	 –17 –11	 – –	dBm
Second Mixer 3rd Order Intercept (RF Input)	Matched Input	TOI_{Mix2}	 –	 – 27	 –	dBm
First LO Buffer Output Resistance	–	R_{LO}	–	–	–	Ω
First Mixer Parallel Input Resistance	–	R	–	722	–	Ω
First Mixer Parallel Input Capacitance	–	C	–	3.3	–	pF
First Mixer Output Impedance	–	ZO	–	330	–	Ω
Second Mixer Input Impedance	–	Z_I	–	40	–	kΩ
Second Mixer Output Impedance	–	ZO	–	1.8	–	kΩ
Detector Output Impedance	–	ZO	–	25	–	Ω

TEST CIRCUIT INFORMATION

Although the MC13136 can be operated with a ceramic discriminator, the recovered audio measurements for both the MC13135 and MC13136 are made with an LC quadrature detector. The typical recovered audio will depend on the external circuit; either the Q of the quad coil, or the RC matching network for the ceramic discriminator. On the MC13136, an external capacitor between Pins 13 and 14 can be used with a quad coil for slightly higher recovered audio. See Figures 10 through 13 for additional information.

Since adding a matching circuit to the RF input increases the signal level to the mixer, the third order intercept (TOI) point is better with an unmatched input (50 Ω from Pin 21 to Pin 22). Typical values for both have been included in the Electrical Characterization Table. TOI measurements were taken at the pins with a high impedance probe/spectrum analyzer system. The first mixer input impedance was measured at the pin with a network analyzer.

2

Figure 1a. MC13135 Test Circuit

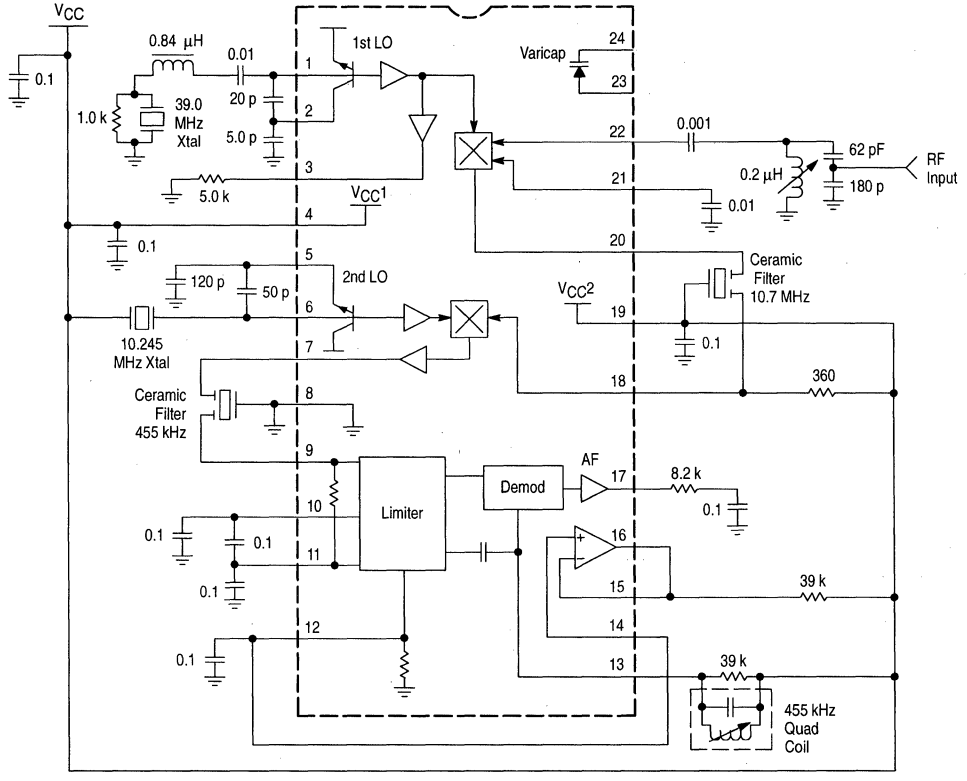


Figure 1b. MC13136 Quad Detector Test Circuit

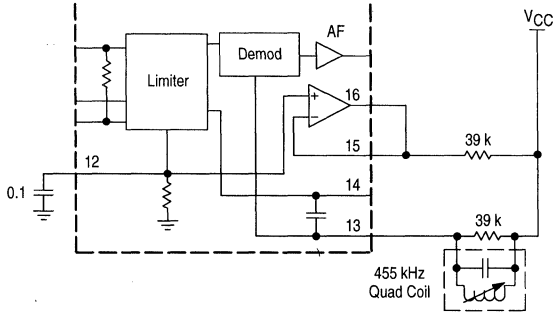


Figure 2. Supply Current versus Supply Voltage

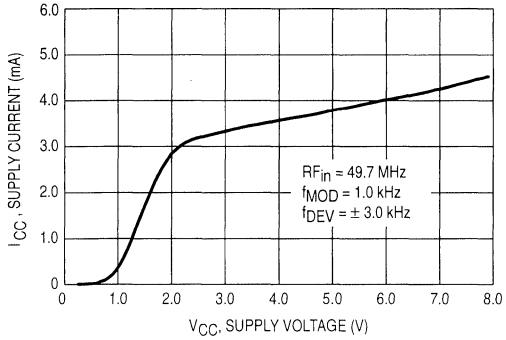


Figure 3. RSSI Output versus RF Input

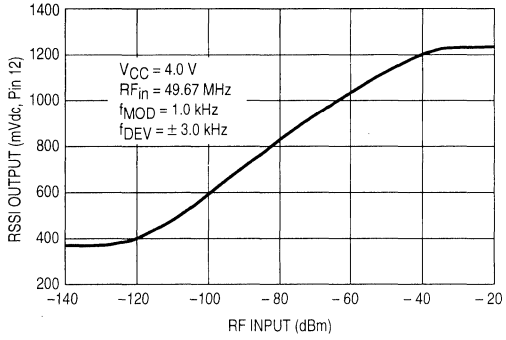


Figure 4. Varactor Capacitance, Resistance versus Bias Voltage

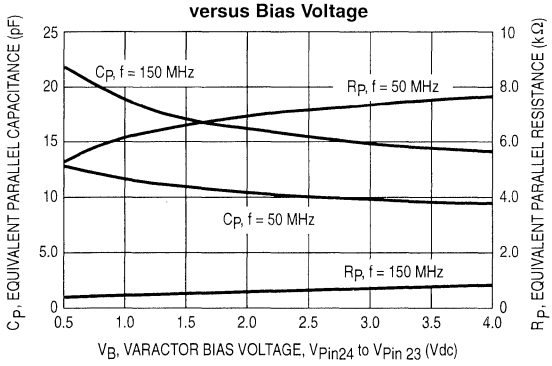


Figure 5. Oscillator Frequency versus Varactor Bias

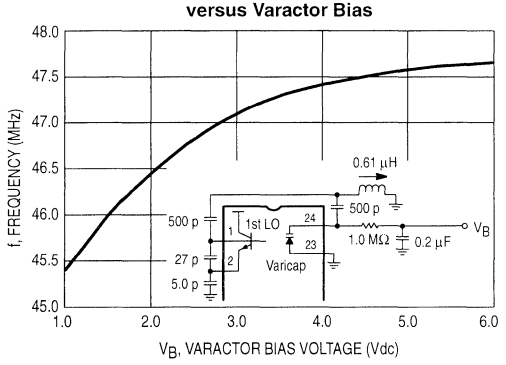


Figure 6. Signal Levels versus RF Input

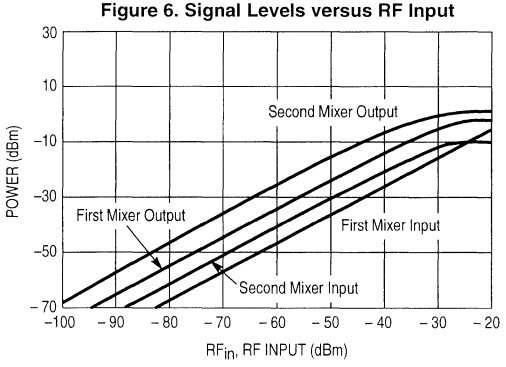


Figure 7. Signal + Noise, Noise, and AM Rejection versus Input Power

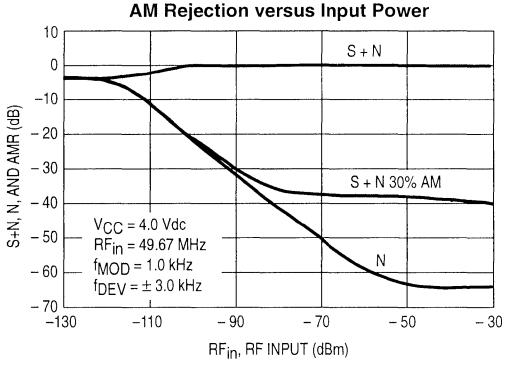


Figure 8. Op Amp Gain and Phase versus Frequency

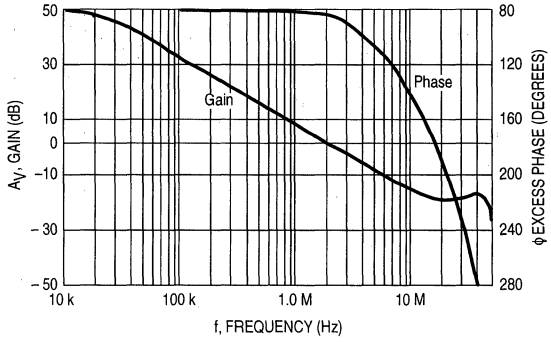


Figure 9. First Mixer Third Order Intermodulation (Unmatched Input)

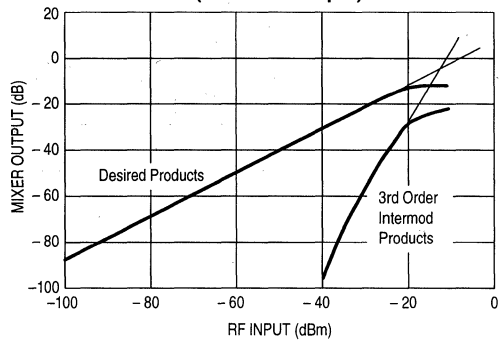


Figure 10. Recovered Audio versus Deviation for MC13135

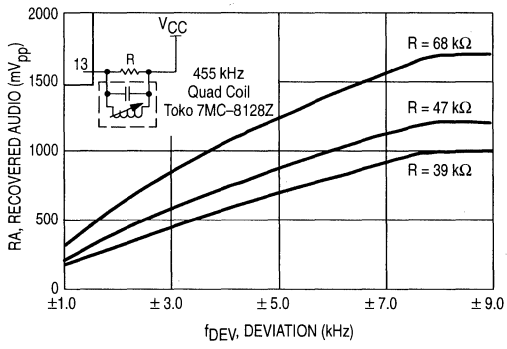


Figure 11. Distortion versus Deviation for MC13135

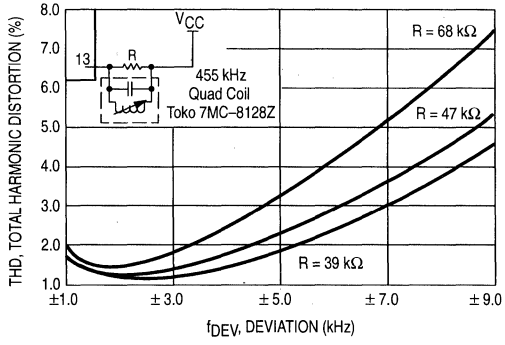


Figure 12. Recovered Audio versus Deviation for MC13136

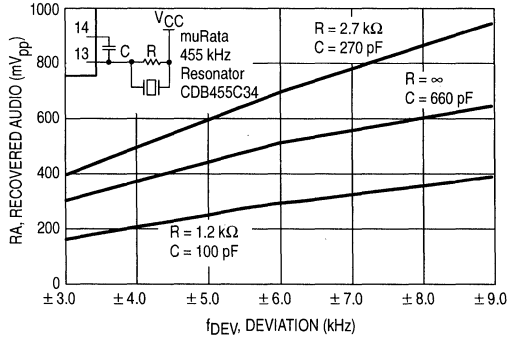
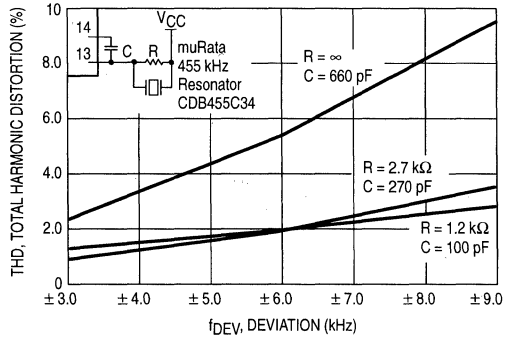


Figure 13. Distortion versus Deviation for MC13136



CIRCUIT DESCRIPTION

The MC13135/13136 are complete dual conversion receivers. They include two local oscillators, two mixers, a limiting IF amplifier and detector, and an op amp. Both provide a voltage buffered RSSI with 70 dB of usable range, isolated tuning diode and buffered LO output for PLL operation, and a separate V_{CC} pin for the first mixer and LO. Improvements have been made in the temperature performance of both the recovered audio and the RSSI.

V_{CC}

Two separate V_{CC} lines enable the first LO and mixer to continue running while the rest of the circuit is powered down. They also isolate the RF from the rest of the internal circuit.

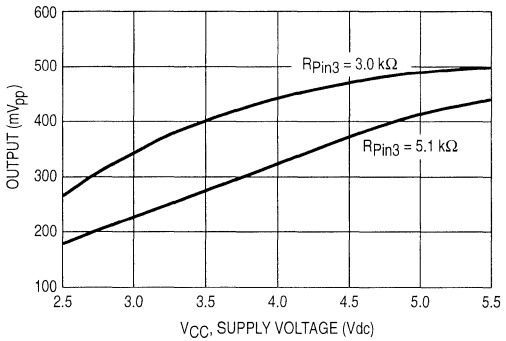
Local Oscillators

The local oscillators are grounded collector Colpitts, which can be easily crystal–controlled or VCO controlled with the on–board varactor and external PLL. The first LO transistor is internally biased, but the emitter is pinned–out and I_Q can be increased for high frequency or VCO operation. The collector is not pinned out, so for crystal operation, the LO is generally limited to 3rd overtone crystal frequencies; typically around 60 MHz. For higher frequency operation, the LO can be provided externally as shown in Figure 16.

Buffer

An amplifier on the 1st LO output converts the single–ended LO output to a differential signal to drive the mixer. Capacitive coupling between the LO and the amplifier minimizes the effects of the change in oscillator current on the mixer. Buffered LO output is pinned–out at Pin 3 for use with a PLL, with a typical output voltage of 320 mV_{pp} at V_{CC} = 4.0 V and with a 5.1 k resistor from Pin 3 to ground. As seen in Figure 14, the buffered LO output varies with the supply voltage and a smaller external resistor may be needed for low voltage operation. The LO buffer operates up to 60 MHz, typically. Above 60 MHz, the output at Pin 3 rolls off at approximately 6.0 dB per octave. Since most PLLs require about 200 mV_{pp} drive, an external amplifier may be required.

Figure 14. Buffered LO Output Voltage versus Supply Voltage



Mixers

The first and second mixer are of similar design. Both are double balanced to suppress the LO and input frequencies to give only the sum and difference frequencies out. This configuration typically provides 40 to 60 dB of LO suppression. New design techniques provide improved mixer linearity and third order intercept without increased noise. The gain on the output of the 1st mixer starts to roll off at about 20 MHz, so this receiver could be used with a 21 MHz first IF. It is designed for use with a ceramic filter, with an output impedance of 330 Ω. A series resistor can be used to raise the impedance for use with a crystal filter, which typically has an input impedance of 4.0 kΩ. The second mixer input impedance is approximately 4.0 kΩ; it requires an external 360 Ω parallel resistor for use with a standard ceramic filter.

Limiting IF Amplifier and Detector

The limiter has approximately 110 dB of gain, which starts rolling off at 2.0 MHz. Although not designed for wideband operation, the bandwidth of the audio frequency amplifier has been widened to 50 kHz, which gives less phase shift and enables the receiver to run at higher data rates. However, care should be taken not to exceed the bandwidth allowed by local regulations.

The MC13135 is designed for use with an LC quadrature detector, and does not have sufficient drive to be used with a ceramic discriminator. The MC13136 was designed to use a ceramic discriminator, but can also be run with an LC quad coil, as mentioned in the Test Circuit Information section. The data shown in Figures 12 and 13 was taken using a muRata CDB455C34 ceramic discriminator which has been specially matched to the MC13136. Both the choice of discriminators and the external matching circuit will affect the distortion and recovered audio.

RSSI/Op Amp

The Received Signal Strength Indicator (RSSI) on the MC13135/13136 has about 70 dB of range. The resistor needed to translate the RSSI current to a voltage output has been included on the internal circuit, which gives it a tighter tolerance. A temperature compensated reference current also improves the RSSI accuracy over temperature. On the MC13136, the op amp on board is connected to the output to provide a voltage buffered RSSI. On the MC13135, the op amp is not connected internally and can be used for the RSSI or as a data slicer (see Figure 17c).

Figure 15. PLL Controlled Narrowband FM Receiver at 46/49 MHz

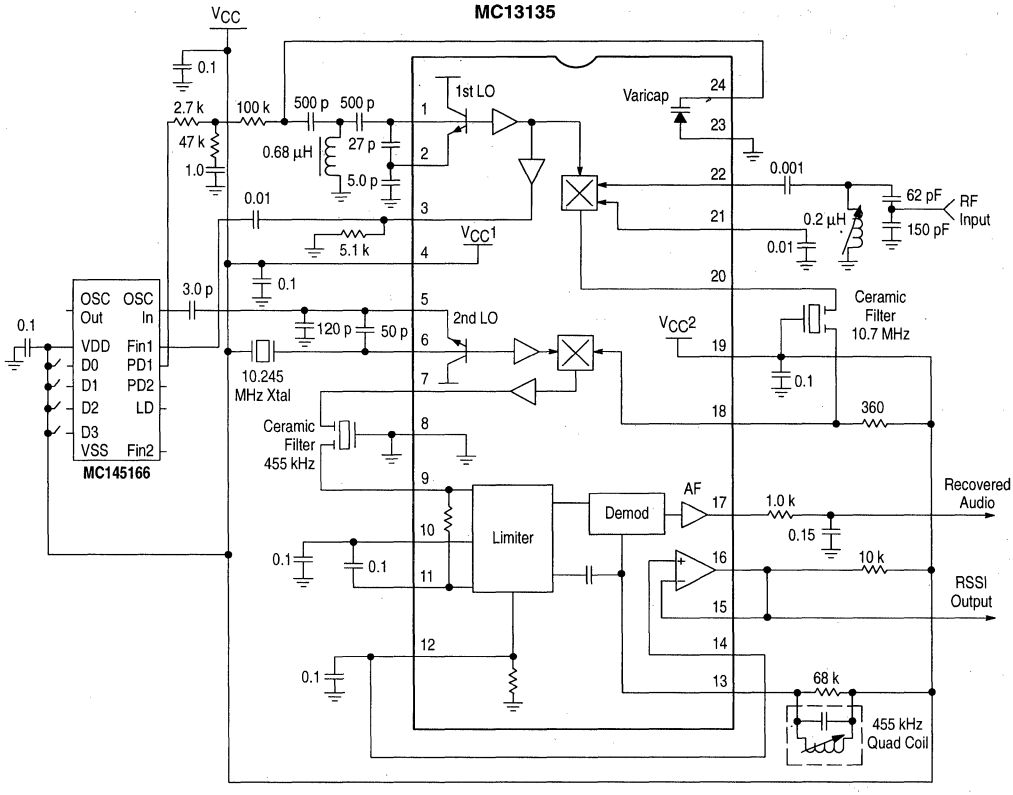
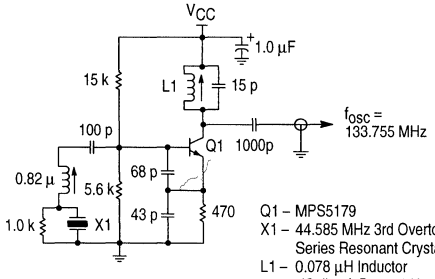


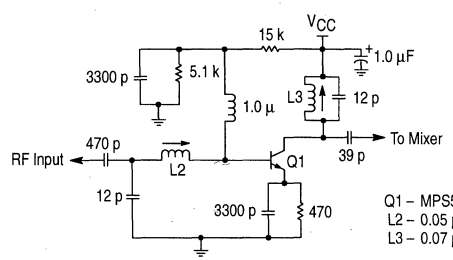
Figure 16. 144 MHz Single Channel Application Circuit

1st LO External Oscillator Circuit



Q1 – MPS5179
X1 – 44.585 MHz 3rd Overtone Series Resonant Crystal
L1 – 0.078 µH Inductor (Coilcraft Part # 146–02J08)

Preamp for MC13135 at 144.455 MHz



Q1 – MPS5179
L2 – 0.05 µH
L3 – 0.07 µH

Figure 17a. Single Channel Narrowband FM Receiver at 49.7 MHz

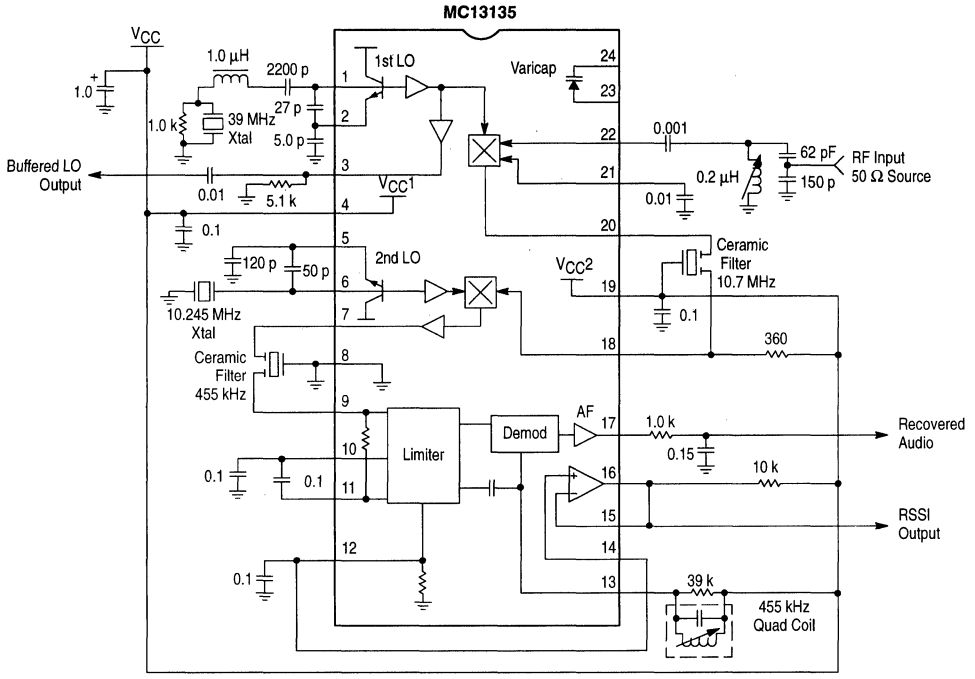
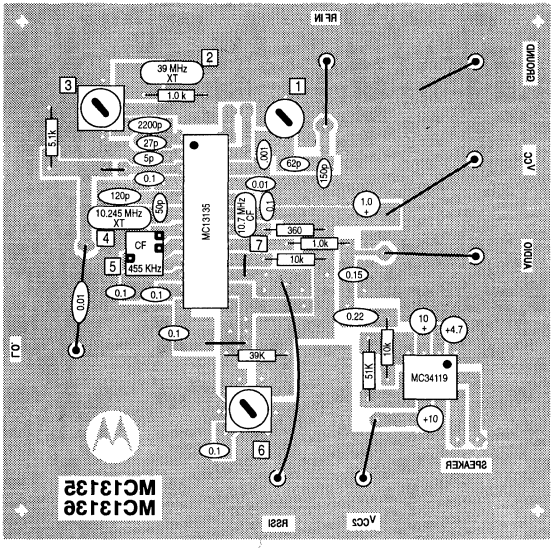


Figure 17b. PC Board Component View



NOTES: 1. 0.2 µH tunable (unshielded) inductor
2. 39 MHz Series mode resonant 3rd Overtone Crystal
3. 1.5 µH tunable (shielded) inductor
4. 10.245 MHz Fundamental mode crystal, 32 pF load
5. 455 kHz ceramic filter, muRata CFU 455B or equivalent
6. Quadrature coil, Toko 7MC–8128Z (7mm) or Toko RMC–2A6597HM (10mm)
7. 10.7 MHz ceramic filter, muRata SFE10.7MJ–A or equivalent

Figure 17c. Optional Data Slicer Circuit
(Using Internal Op Amp)

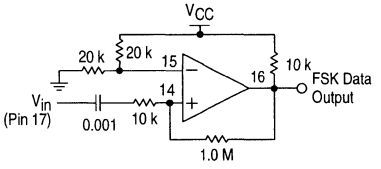
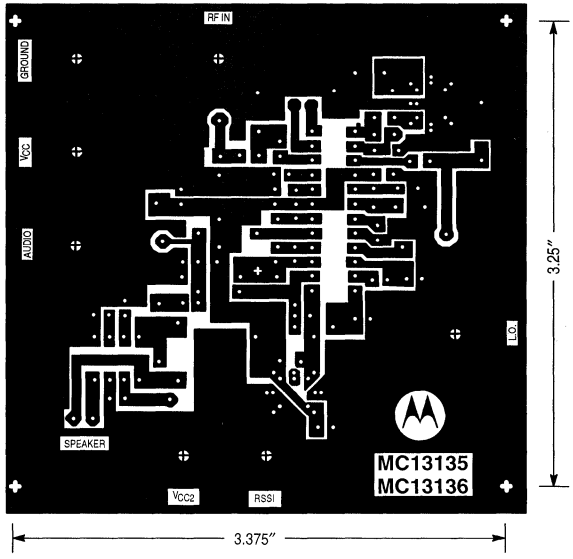
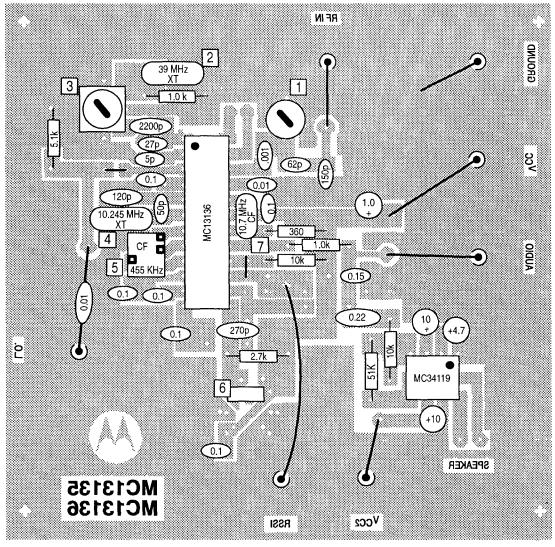


Figure 18. PC Board Solder Side View



(Circuit Side View)

Figure 19. PC Board Component View



NOTES: 1. 0.2 µH tunable (unshielded) inductor
2. 39 MHz Series mode resonant 3rd Overtone Crystal
3. 1.5 µH tunable (shielded) inductor
4. 10.245 MHz Fundamental mode crystal, 32 pF load
5. 455 kHz ceramic filter, muRata CFU 455B or equivalent
6. Ceramic discriminator, muRata CDB455C34 or equivalent
7. 10.7 MHz ceramic filter, muRata SFE10.7MJ–A or equivalent

Figure 20a. Single Channel Narrowband FM Receiver at 49.7 MHz

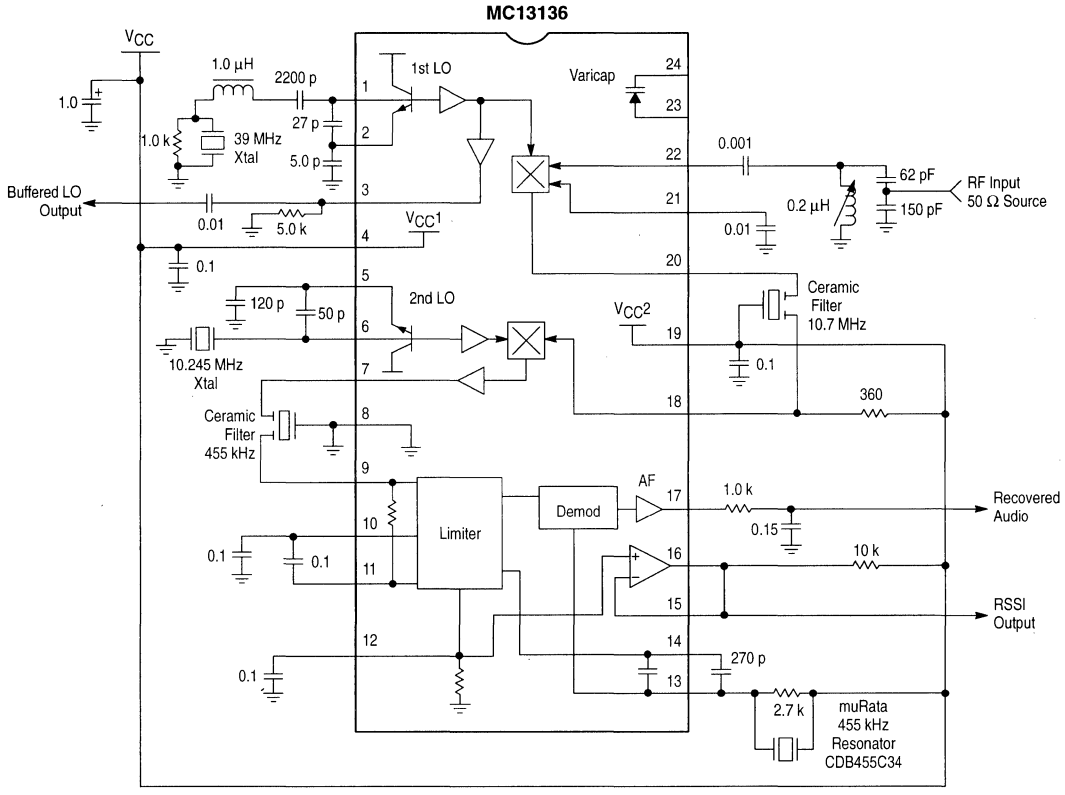


Figure 20b. Optional Audio Amplifier Circuit

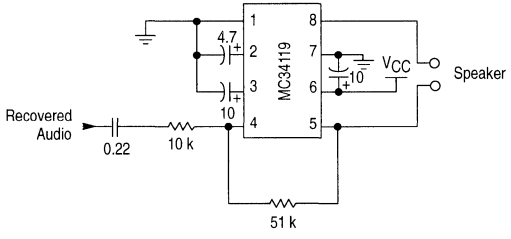
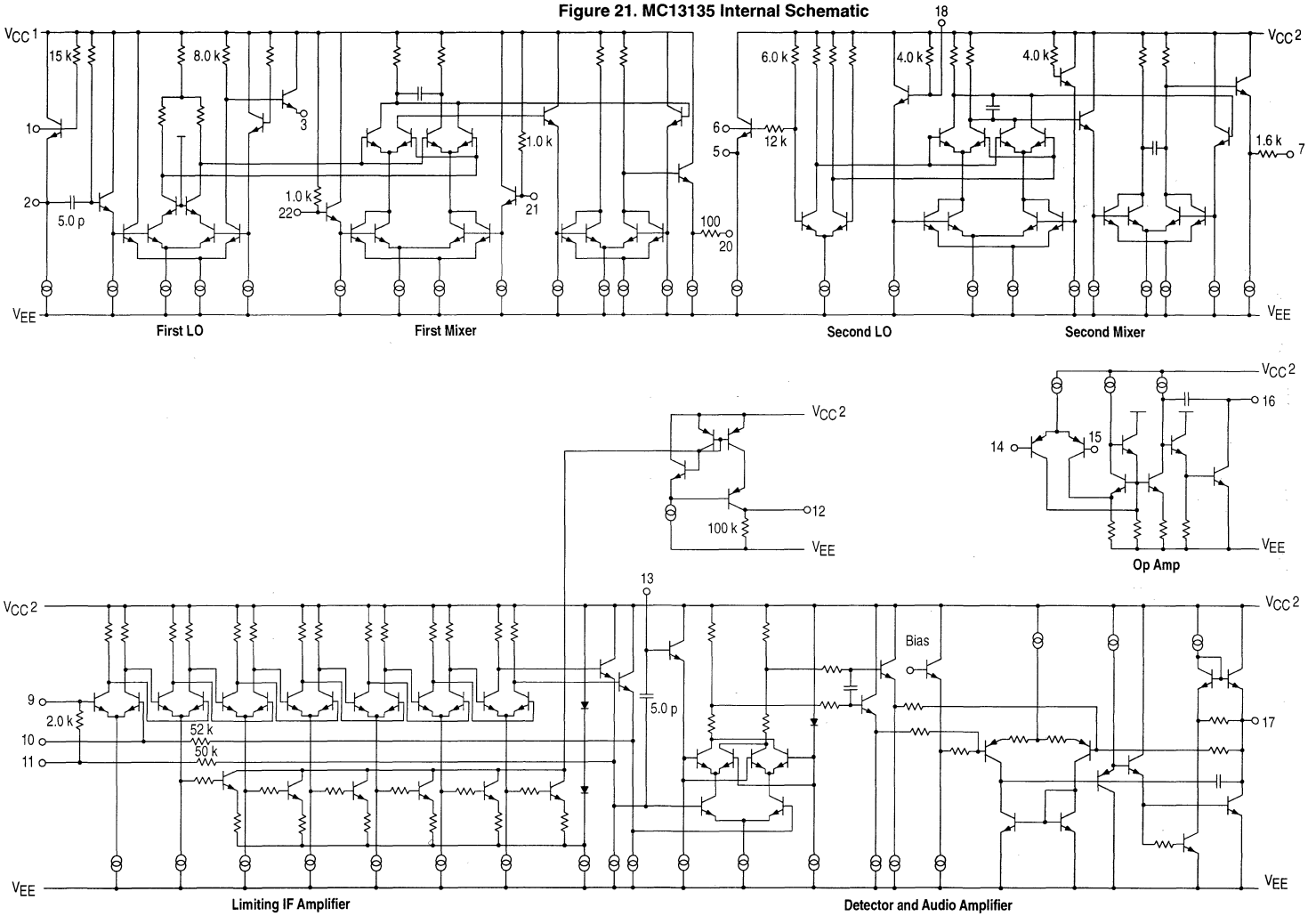
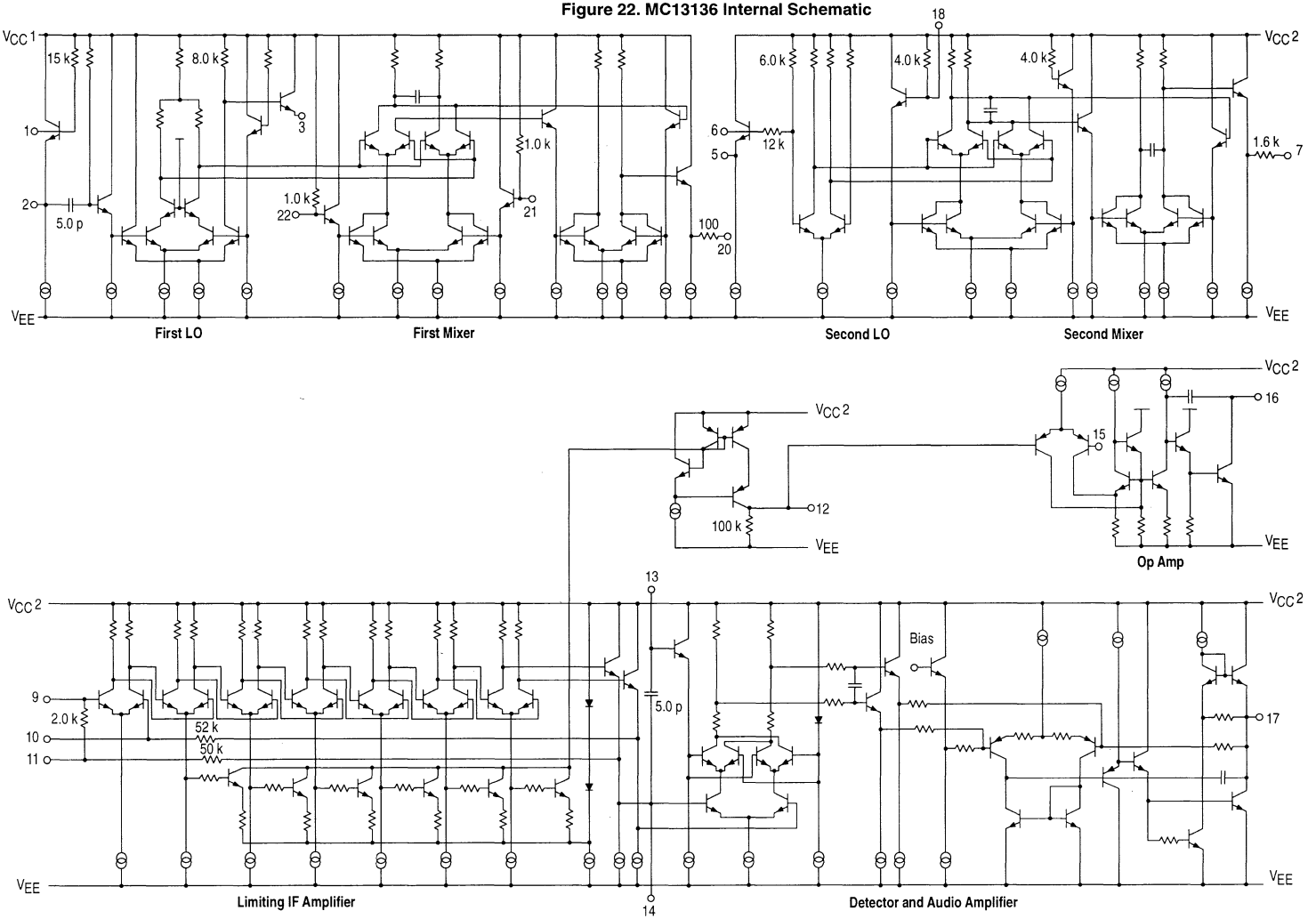


Figure 21. MC13135 Internal Schematic



This device contains 142 active transistors.

Figure 22. MC13136 Internal Schematic



This device contains 142 active transistors.

MC13141

Product Preview

Low Power DC - 1.8 GHz LNA and Mixer

LOW POWER DC – 1.8 GHz LNA AND MIXER

SEMICONDUCTOR TECHNICAL DATA

2

The MC13141 is intended to be used as a first amplifier and down converter for RF applications. It features wide band operation, low noise, high gain and high linearity while maintaining low current consumption. The circuit consists of a Low Noise Amplifier (LNA), a Local Oscillator amplifier (LO_{amp}), a mixer, an Intermediate Frequency amplifier (IF_{amp}) and a dc control section.

- Wide RF Bandwidth: DC–1.8 GHz
- Wide Mixer Bandwidth: DC–1.8 GHz
- Wide IF Bandwidth: DC–150 MHz
- Low Power: 7.0 mA @ V_{CC} = 2.7–6.5 V
- High Mixer Linearity: $Pi_{1.0\ dB}$ = – 2.0 dBm, IP_{3in} = + 3.0 dBm
- Linearity Adjustment Increases IP_{3in} (Not Available in SOIC8)
- Single–Ended 50 Ω Mixer Input
- Double Balanced Mixer Operation
- Single Ended 800 Ω Mixer Output

D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO–14)

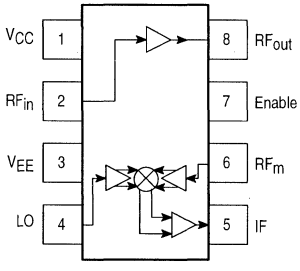
FTB SUFFIX
PLASTIC PACKAGE
CASE 976
(Thin QFP)

ORDERING INFORMATION

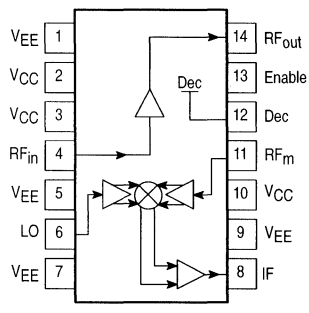
Device	Operating Temperature Range	Package
MC13141D	T_A = – 40 ° to +85°C	SO–8
MC13141D		SO–14
MC13141FTB		TQFP–20

PIN CONNECTIONS

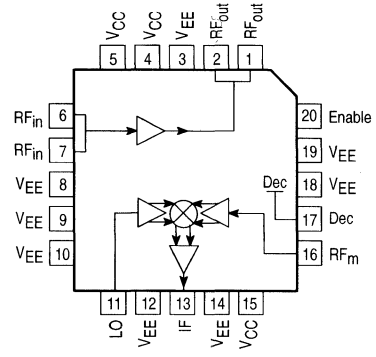
SO–8



SO–14



TQFP–20



MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	7.0 (max)	Vdc
Operating Supply Voltage Range	V_{CC}	2.7–6.5	Vdc

ELECTRICAL CHARACTERISTICS (SOIC8 Package, V_{CC} = 3.0 V, T_A = 25°C, LO_{in} = –10 dBm @ 950 MHz, IF @ 50 MHz.)

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Current (Power Down)	I_{CC}	–	100	–	pA
Supply Current (Power Up)	I_{CC}	–	5.5–8.5	–	mA
Amplifier Gain	S_{21}	–	17	–	dB
Amplifier Reverse Isolation	S_{12}	–	– 25	–	dB
Amplifier Input Match	$\Gamma_{in\ amp}$	–	–10	–	dB
Amplifier Output Match	$\Gamma_{out\ amp}$	–	–15	–	dB
Amplifier 1.0 dB Gain Compression	$Pin_{-1.0\ dB}$	–	–15	–	dBm
Amplifier Input Third Order Intercept	$IP3_{in}$	–	– 5.0	–	dBm
Amplifier Noise Figure (50 Ω)	NF	–	2.5	–	dB
Mixer Voltage Conversion Gain ($R_P = R_L$ = 800 Ω)	VG_C	–	15	–	dB
Mixer Power Conversion Gain ($R_P = R_L$ = 800 Ω)	PG_C	–	3.0	–	dB
Mixer Input Match	$\Gamma_{in\ M}$	–	– 20	–	dB
Mixer SSB Noise Figure	NF_{SSBM}	–	17.0	–	dB
Mixer 1.0 dB Gain Compression	$Pin_{-1.0\ dBM}$	–	– 2.0	–	dBm
Mixer Input Third Order Intercept	$IP3_{inM}$	–	3.0	–	dBm
LO Drive Level	LO_{In}	–	–10	–	dBm
RF_{in} Feedthrough to RF_m	$P_{RFin–Rin}$	–	– 25	–	dB
RF_{out} Feedthrough to RF_m	$P_{RFout–RFm}$	–	– 25	–	dB
LO Feedthrough to IF	$P_{LO–IF}$	–	– 25	–	dB
LO Feedthrough to RF_{in}	$P_{LO–RFin}$	–	– 25	–	dB
LO Feedthrough to RF_m	$P_{LO–RFm}$	–	– 25	–	dB
Mixer RF Feedthrough to IF	$P_{RFm–IF}$	–	– 25	–	dB
Mixer RF Feedthrough to RF_{in}	$P_{RFm–RFin}$	–	– 25	–	dB

MOTOROLA

MC13142

Product Preview

Low Power DC - 1.8 GHz LNA, Mixer and VCO

2

The MC13142 is intended to be used as a first amplifier, voltage controlled oscillator and down converter for RF applications. It features wide band operation, low noise, high gain and high linearity while maintaining low current consumption. The circuit consists of a Low Noise Amplifier (LNA), a Voltage Controlled Oscillator (VCO), a buffered oscillator output, a mixer, an Intermediate Frequency amplifier (IF_{amp}) and a dc control section. The wide mixer IF bandwidth allows this part also to be used as an up converter and exciter amplifier.

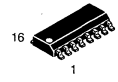
- Wide RF Bandwidth: DC–1.8 GHz
- Wide LO Bandwidth: DC–1.8 GHz
- Wide IF Bandwidth: DC–1.8 GHz
- Low Power: 13 mA @ V_{CC} = 2.7–6.5 V
- High Mixer Linearity: $P_{i1.0\ dB}$ = + 3.0 dBm
- Linearity Adjustment Increases IP_{3in} (TQFP–20 Package Only)
- Single–Ended 50 Ω Mixer Input
- Double Balanced Mixer Operation
- Open Collector Mixer Output
- Single Transistor Oscillator with Collector, Base and Emitter Pinned Out
- Buffered Oscillator Output
- Mixer and Oscillator Can be Enabled Independently

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC13142D	T_A = –40 ° to +85°C	SO–16
MC13142FTB		TQFP–20

LOW POWER DC – 1.8 GHz LNA, MIXER and VCO

SEMICONDUCTOR TECHNICAL DATA

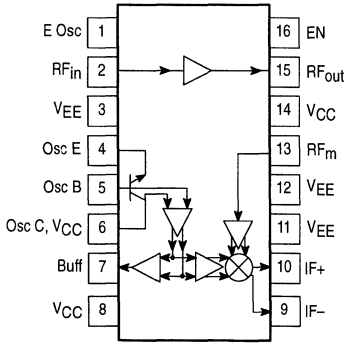


D SUFFIX
PLASTIC PACKAGE
CASE 751B
(SO–16)

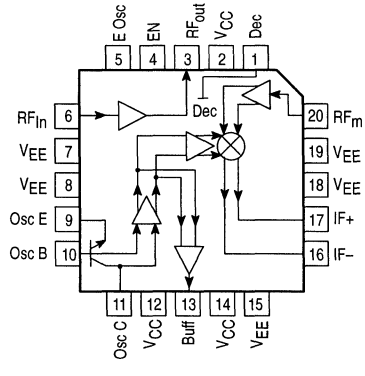
FTB SUFFIX
PLASTIC PACKAGE
CASE 976
(Thin QFP)

PIN CONNECTIONS

SO–16



TQFP–20



MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	7.0 (max)	Vdc
Operating Supply Voltage Range	V_{CC}	2.7–6.5	Vdc

ELECTRICAL CHARACTERISTICS (V_{CC} = 3.0 V, T_A = 25°C, LO_{in} = –10 dBm @ 950 MHz, IF @ 50 MHz.)

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Current (Power Down)	I_{CC}	–	100	–	pA
Supply Current (Power Up)	I_{CC}	–	10–16	–	mA
Amplifier Gain	S_{21}	–	17	–	dB
Amplifier Reverse Isolation	S_{12}	–	– 25	–	dB
Amplifier Input Match	$\Gamma_{in\ amp}$	–	–10	–	dB
Amplifier Output Match	$\Gamma_{out\ amp}$	–	–15	–	dB
Amplifier 1.0 dB Gain Compression	$Pin_{-1.0\ dB}$	–	–15	–	dBm
Amplifier Input Third Order Intercept	$IP3_{in}$	–	– 5.0	–	dBm
Amplifier Noise Figure (50 Ω)	NF	–	2.5	–	dB
Mixer Voltage Conversion Gain (R_P = R_L = 800 Ω)	VG_C	–	9.0	–	dB
Mixer Power Conversion Gain (R_P = R_L = 800 Ω)	PG_C	–	– 3.0	–	dB
Mixer Input Match	$\Gamma_{in\ M}$	–	– 20	–	dB
Mixer SSB Noise Figure	NF_{SSBM}	–	12	–	dB
Mixer 1.0 dB Gain Compression	$Pin_{-1.0\ dBM}$	–	3.0	–	dBm
Mixer Input Third Order Intercept	$IP3_{InM}$	–	– 2.0	–	dBm
Oscillator Buffer Drive (50 Ω)	P_{VCO}	–	–16	–	dBm
Oscillator Phase Noise @ 25 kHz Offset	N_Φ	–	– 90	–	dBc/Hz
RF_{in} Feedthrough to RF_m	$P_{RFin–RFm}$	–	– 35	–	dB
RF_{out} Feedthrough to RF_m	$P_{RFout–RFm}$	–	– 35	–	dB
LO Feedthrough to IF	$P_{LO–IF}$	–	– 35	–	dBm
LO Feedthrough to RF_{in}	$P_{LO–RFin}$	–	– 35	–	dBm
LO Feedthrough to RF_m	$P_{LO–RFm}$	–	– 35	–	dBm
Mixer RF Feedthrough to IF	$P_{RFm–IF}$	–	– 25	–	dB
Mixer RF Feedthrough to RF_{in}	$P_{RFm–RFin}$	–	– 25	–	dB

MOTOROLA

MC13143

Product Preview

Ultra Low Power DC - 2.4 GHz Linear Mixer

The MC13143 is a high compression linear mixer with single–ended RF input, differential IF output and differential LO inputs which consumes as little as 1.8 mW. A new circuit topology is used to achieve a high third order intermodulation intercept point, high linearity and high 1.0 dB output compression point while maintaining a linear 50 Ω input impedance. It is designed for Up or Down conversion anywhere from dc to 2.4 GHz.

Ultra Low Power: 1.0 mA @ V_{CC} = 1.8–6.5 V

- Wide Input Bandwidth: DC–2.4 GHz
- Wide Output Bandwidth: DC–2.4 GHz
- Wide LO Bandwidth: DC–2.4 GHz
- High Mixer Linearity: $P_{i1.0\ dB}$ = + 3.0 dBm

Linearity Adjustment of up to IP_{3in} = +20 dBm

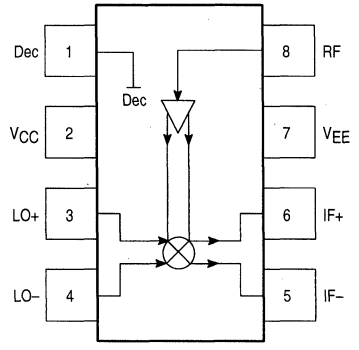
- 50 Ω Mixer Input
- Single–Ended Mixer Input
- Double Balanced Mixer Operation
- Differential Open Collector Mixer Output

ULTRA LOW POWER DC – 2.4 GHz LINEAR MIXER

SEMICONDUCTOR TECHNICAL DATA

D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC13143D	T_A = –40 ° to +85°C	SO–8

MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	7.0 (max)	Vdc
Operating Supply Voltage Range	V_{CC}	1.8–6.5	Vdc

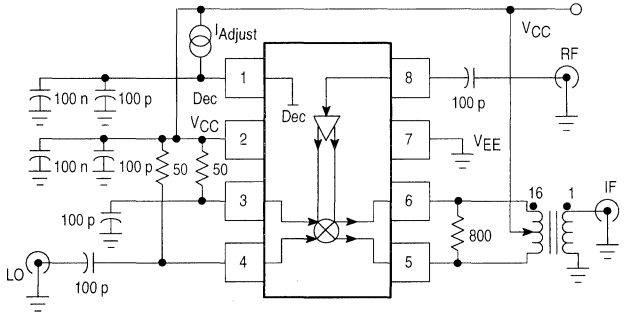
This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

ELECTRICAL CHARACTERISTICS (V_{CC} = 2.0 V, T_A = 25°C, RF = – 30 dBm @ 900 MHz, LO = 0 dBm @ 950 MHz, IF @ 50 MHz.)

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Current	I_{CC}	–	0.7–1.3	–	mA
Mixer Voltage Conversion Gain (R_P = R_L = 800 Ω)	VG_C	–	9.0	–	dB
Mixer Power Conversion Gain (R_P = R_L = 800 Ω)	PG_C	–	– 3.0	–	dB
Mixer Input Match	Γ_{in}	–	– 20	–	dB
Mixer SSB Noise Figure	NF_{SSB}	–	12	–	dB
Mixer 1.0 dB Gain Compression	$PIn_{-1.0\ dB}$	–	3.0	–	dBm
Mixer Input Third Order Intercept	$IP3_{in}$	–	– 3.0	–	dBm
LO Drive Level	LO_{in}	–	– 5.0	–	dBm
LO Feedthrough to Mixer Out	P_{LO-IF}	–	– 25	–	dB
Mixer Input Feedthrough Output	P_{RFm-IF}	–	– 25	–	dB
Mixer Input Feedthrough to LO	P_{RFm-LO}	–	– 25	–	dB

2

Test Circuit



MOTOROLA

MC13150

Product Preview

Narrowband FM Coilless Detector IF Subsystem

NARROWBAND FM COILLESS DETECTOR IF SUBSYSTEM FOR CELLULAR AND ANALOG APPLICATIONS

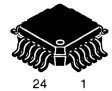
SEMICONDUCTOR TECHNICAL DATA

2

The MC13150 is a narrowband FM IF subsystem targeted at cellular and other analog applications. Excellent high frequency performance is achieved, with low cost, through use of Motorola's MOSAIC 1.5™ RF bipolar process. The MC13150 has an onboard Colpitts VCO for Crystal controlled second LO in dual conversion receivers. The mixer is a double balanced configuration with excellent third order intercept. It is useful to beyond 200 MHz. The IF amplifier is split to accommodate two low cost cascaded filters. RSSI output is derived by summing the output of both IF sections. The quadrature detector is a unique design eliminating the conventional tunable quadrature coil.

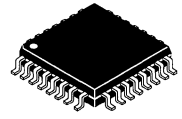
Applications for the MC13150 include cellular, CT–1 900 MHz cordless telephone, data links and other radio systems utilizing narrowband FM modulation.

- Linear Coilless Detector
- Adjustable Demodulator Bandwidth
- 2.5 to 6.0 Vdc Operation
- Low Drain Current: < 2.0 mA
- Typical Sensitivity of 2.0 μV for 12 dB SINAD
- IIP3, Input Third Order Intercept Point of 0 dBm
- RSSI Range of Greater Than 100 dB
- Internal 1.4 kΩ Terminations for 455 kHz Filters
- Split IF for Improved Filtering and Extended RSSI Range



24 1

FTA SUFFIX
PLASTIC PACKAGE
CASE 977
(Thin QFP)



32 1

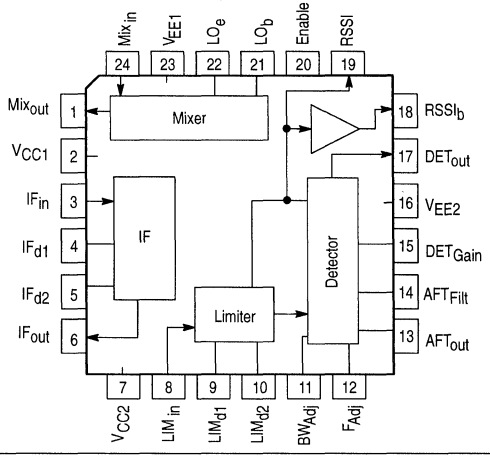
FTB SUFFIX
PLASTIC PACKAGE
CASE 873
(Thin QFP)

ORDERING INFORMATION

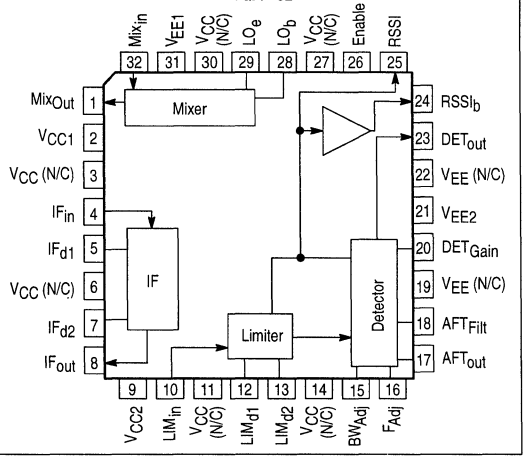
Device	Tested Operating Temperature Range	Package
MC13150FTA	T_A = –40 ° to +85°C	TQFP–24
MC13150FTB		TQFP–32

PIN CONNECTIONS

TQFP-24



TQFP-32



This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

MAXIMUM RATINGS

Rating	Pin	Symbol	Value	Unit
Power Supply Voltage	2, 9	V_{CC}(max)	65	Vdc
Junction Temperature	–	T_{Jmax}	+150	°C
Storage Temperature Range	–	T_{stg}	– 65 to +150	°C

NOTE: Devices should not be operated at or outside these values. The "Recommended Operating Limits" provide for actual device operation.

RECOMMENDED OPERATING CONDITIONS

Rating	Pin	Symbol	Value	Unit
Power Supply Voltage T_A = 25°C – 40°C ≤ T_A ≤ 85°C	2, 9 21, 31	V_{CC} V_{EE}	2.5 to 6.0 0	Vdc
Input Frequency	32	f_{in}	10 to 500	MHz
Ambient Temperature Range	-	T_A	– 40 to + 85	°C
Input Signal Level	32	V_{in}	0	dBm

2

DC ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC1} = V_{CC2} = 3.0 Vdc, No Input Signal.)

Characteristics	Condition	Pin	Symbol	Min	Typ	Max	Unit
Total Drain Current	V_S = 3.0 Vdc	2 + 9	I_{TOTAL}	–	1.7	3.0	mA
Supply Current, Power Down	–	2 + 9	–	–	40	–	nA

AC ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC} = 3.0 Vdc, f_{RF} = 50 MHz, f_{LO} = 50.455 MHz, LO Level = –10 dBm, Unless Otherwise Specified.)

Characteristics	Condition	Pin	Symbol	Min	Typ	Max	Unit
12 dB SINAD Sensitivity	f_{mod} = 1.0 kHz; f_{DEV} = ± 5.0 kHz	32	–	–	–100	–	dBm
RSSI Dynamic Range	–	25	–	–	100	–	dB
Input 1.0 dB Compression Point Input 3rd Order Intercept Point	– –	– –	1.0 dB C. Pt. IIP3	– –	–11 –1.0	– –	dBm
Coilless Detector Bandwidth Adjust	Measured with No IF Filters	–	ΔBW adj	–	26	–	kHz/μA
MIXER							
Conversion Voltage Gain	P_{in} = – 30 dBm; PLO = –10 dBm	32	– –	– –	10 –	– –	dB
Mixer Input Impedance	Single–Ended	32	–	–	200	–	Ω
Mixer Output Impedance	–	1	–	–	1.5	–	kΩ
LO Emitter Current	–	29	–	30	63	100	μA
IF & LIMITING AMPLIFIERS SECTION							
IF and Limiter RSSI Slope	–	25	–	–	0.4	–	μA/dB
IF Gain	–	4, 8	–	–	42	–	dB
IF Input & Output Impedance	–	4, 8	–	–	1.5	–	kΩ
Limiter Input Impedance	–	10	–	–	1.5	–	kΩ
Limiter Gain	–	–	–	–	96	–	dB
DETECTOR							
Frequency Adjust Current	f_{IF} = 455 kHz	16	–	41	49	56	μA
Frequency Adjust Voltage	f_{IF} = 455 kHz	16	–	600	650	700	mVdc
Bandwidth Adjust Voltage	I_{15} = 1.0 μA	15	–	–	570	–	mVdc
Detector DC Output Voltage	–	23	–	–	1.36	–	Vdc
Recovered Audio Voltage	f_{DEV} = ±3.0 kHz	23	–	85	122	175	mVrms

MOTOROLA

MC13155

Advance Information

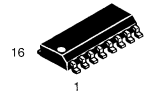
Wideband FM IF

The MC13155 is a complete wideband FM detector designed for satellite TV and other wideband data and analog FM applications. This device may be cascaded for higher IF gain and extended Receive Signal Strength Indicator (RSSI) range.

- 12 MHz Video/Baseband Demodulator
- Ideal for Wideband Data and Analog FM Systems
- Limiter Output for Cascade Operation
- Low Drain Current: 7.0 mA
- Low Supply Voltage: 3.0 to 6.0 V
- Operates to 300 MHz

WIDEBAND FM IF

SEMICONDUCTOR TECHNICAL DATA



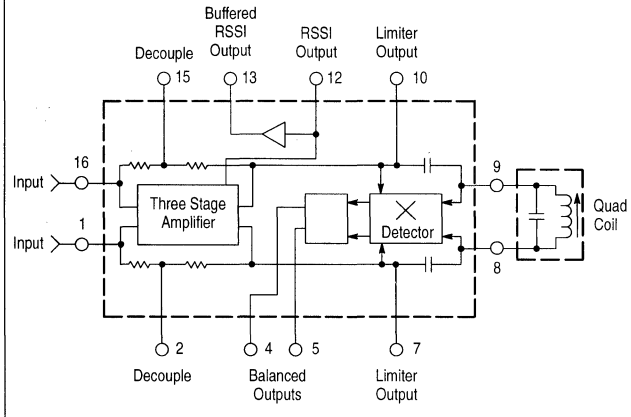
D SUFFIX
PLASTIC PACKAGE
CASE 751B
(SO–16)

MAXIMUM RATINGS

Rating	Pin	Symbol	Value	Unit
Power Supply Voltage	11, 14	V_{EE} (max)	6.5	Vdc
Input Voltage	1, 16	V_{in}	1.0	Vrms
Junction Temperature	–	T_J	+150	°C
Storage Temperature Range	–	T_{stg}	– 65 to +150	°C

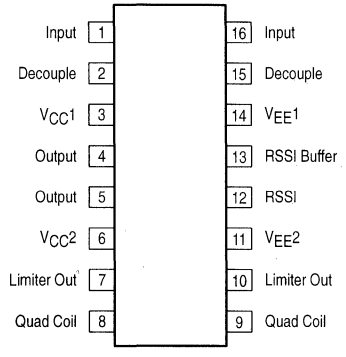
NOTE: Devices should not be operated at or outside these values. The "Recommended Operating Conditions" provide for actual device operation.

Figure 1. Representative Block Diagram



NOTE: This device requires careful layout and decoupling to ensure stable operation.

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC13155D	T_A = – 40 to +85°C	SO–16

RECOMMENDED OPERATING CONDITIONS

Rating	Pin	Symbol	Value	Unit
Power Supply Voltage (T_A= 25°C) – 40°C ≤ T_A ≤ 85°C	11, 14 3, 6	V_{EE} V_{CC}	– 3.0 to – 6.0 Grounded	Vdc
Maximum Input Frequency	1, 16	f_{in}	300	MHz
Ambient Temperature Range	–	T_J	– 40 to + 85	°C

DC ELECTRICAL CHARACTERISTICS (T_A = 25°C, no input signal.)

Characteristic	Pin	Symbol	Min	Typ	Max	Unit
Drain Current (V_{EE} = – 5.0 Vdc) (V_{EE} = – 5.0 Vdc)	11 14 14	I_{11} I_{14} I_{14}	2.0 3.0 3.0	2.8 4.3 4.3	4.0 6.0 6.0	mA
Drain Current Total (see Figure 3) (V_{EE} = – 5.0 Vdc) (V_{EE} = – 6.0 Vdc) (V_{EE} = – 3.0 Vdc)	11, 14	I_{Total}	5.0 5.0 5.0 4.7	7.1 7.5 7.5 6.6	10 10.5 10.5 9.5	mA

AC ELECTRICAL CHARACTERISTICS (T_A = 25°C, f_{IF} = 70 MHz, V_{EE} = – 5.0 Vdc Figure 2, unless otherwise noted.)

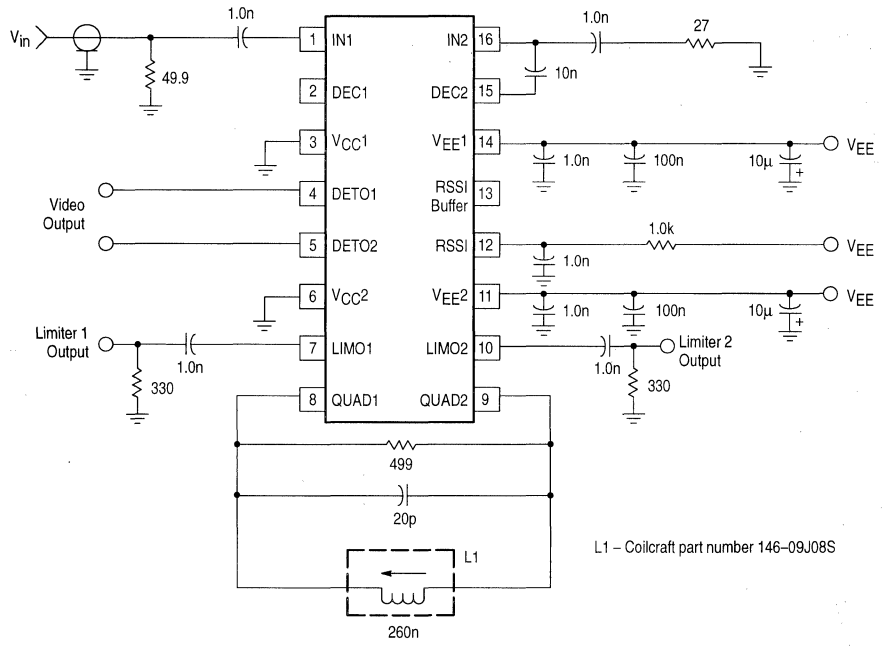
Characteristic	Pin	Min	Typ	Max	Unit
Input for – 3 dB Limiting Sensitivity	1, 16	–	1.0	2.0	mVrms
Differential Detector Output Voltage (V_{in} = 10 mVrms) (f_{dev} = ± 3.0 MHz) (V_{EE} = – 6.0 Vdc) (V_{EE} = – 5.0 Vdc) (V_{EE} = – 3.0 Vdc)	4, 5	 470 450 380	 590 570 500	 700 680 620	mV_{p-p}
Detector DC Offset Voltage	4, 5	– 250	–	250	mVdc
RSSI Slope	13	1.4	2.1	2.8	µA/dB
RSSI Dynamic Range	13	31	35	39	dB
RSSI Output (V_{in} = 100 µVrms) (V_{in} = 1.0 mVrms) (V_{in} = 10 mVrms) (V_{in} = 100 mVrms) (V_{in} = 500 mVrms)	12	 – – 16 – –	 2.1 2.4 24 65 75	 – – 36 – –	µA
RSSI Buffer Maximum Output Current (V_{in} = 10 mVrms)	13	–	2.3	–	mAdc
Differential Limiter Output (V_{in} = 1.0 mVrms) (V_{in} = 10 mVrms)	7, 10	100 –	140 180	– –	mVrms
Demodulator Video 3.0 dB Bandwidth	4, 5	–	12	–	MHz
Input Impedance (Figure 14) @ 70 MHz Rp (V_{EE} = – 5.0 Vdc) Cp (C_2=C_{15} = 100 p)	1, 16	 – –	 450 4.8	 – –	 Ω pF
Differential IF Power Gain	1, 7, 10, 16	–	46	–	dB

NOTE: Positive currents are out of the pins of the device.

CIRCUIT DESCRIPTION

The MC13155 consists of a wideband three–stage limiting amplifier, a wideband quadrature detector which may be operated up to 200 MHz, and a received signal strength indicator (RSSI) circuit which provides a current output linearly proportional to the IF input signal level for approximately 35 dB range of input level.

Figure 2. Test Circuit



APPLICATIONS INFORMATION

Evaluation PC Board

The evaluation PCB shown in Figures 19 and 20 is very versatile and is designed to cascade two ICs. The center section of the board provides an area for attaching all surface mount components to the circuit side and radial leaded components to the component ground side of the PCB (see Figures 17 and 18). Additionally, the peripheral area surrounding the RF core provides pads to add supporting and interface circuitry as a particular application dictates. This evaluation board will be discussed and referenced in this section.

Limiting Amplifier

Differential input and output ports interfacing the three stage limiting amplifier provide a differential power gain of typically 46 dB and useable frequency range of 300 MHz. The IF gain flatness may be controlled by decoupling of the internal feedback network at Pins 2 and 15.

Scattering parameter (S–parameter) characterization of the IF as a two port linear amplifier is useful to implement maximum stable power gain, input matching, and stability over a desired bandpass response and to ensure stable operation outside the bandpass as well. The MC13155 is unconditionally stable over most of its useful operating frequency range; however, it can be made unconditionally stable over its entire operating range with the proper decoupling of Pins 2 and 15. Relatively small decoupling capacitors of about 100 pF have a significant effect on the wideband response and stability. This is shown in the scattering parameter tables where S–parameters are shown for various values of C2 and C15 and at V_{EE} of – 3.0 and – 5.0 Vdc.

TYPICAL PERFORMANCE AT TEMPERATURE
(See Figure 2. Test Circuit)

Figure 3. Drain Current versus Supply Voltage

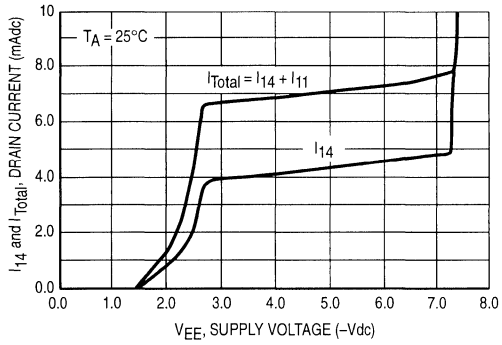


Figure 4. RSSI Output versus Frequency and Input Signal Level

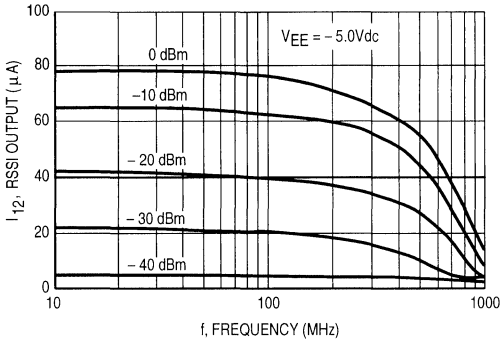


Figure 5. Total Drain Current versus Ambient Temperature and Supply Voltage

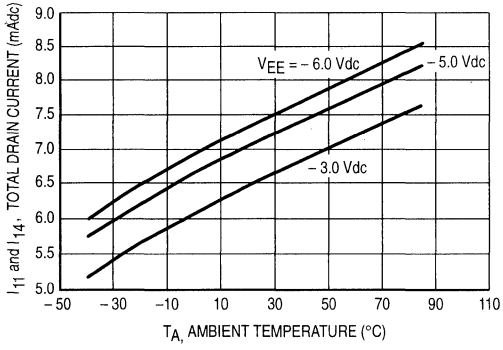


Figure 6. Detector Drain Current and Limiter Drain Current versus Ambient Temperature

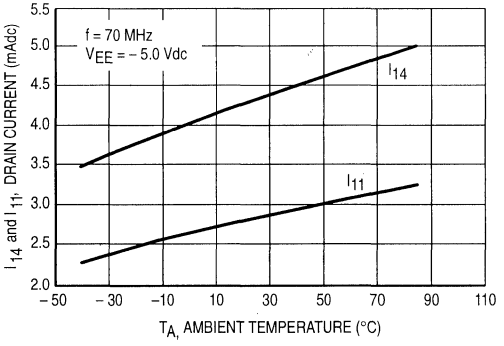


Figure 7. RSSI Output versus Ambient Temperature and Supply Voltage

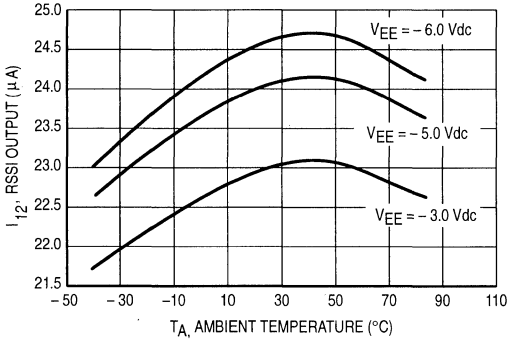


Figure 8. RSSI Output versus Input Signal Voltage (V_{in} at Temperature)

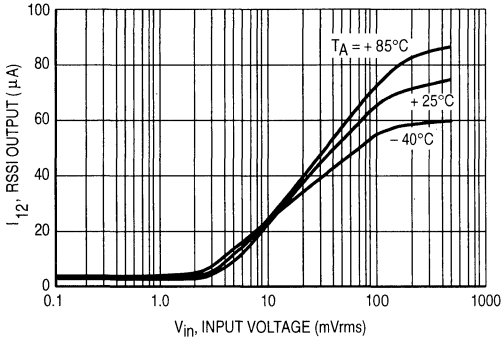


Figure 9. Differential Detector Output Voltage versus Ambient Temperature and Supply Voltage

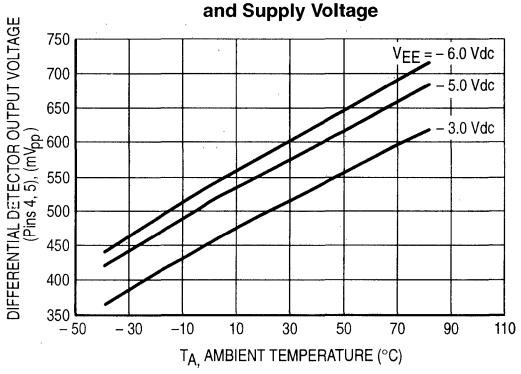


Figure 10. Differential Limiter Output Voltage versus Ambient Temperature (V_{in} = 1 and 10 mVrms)

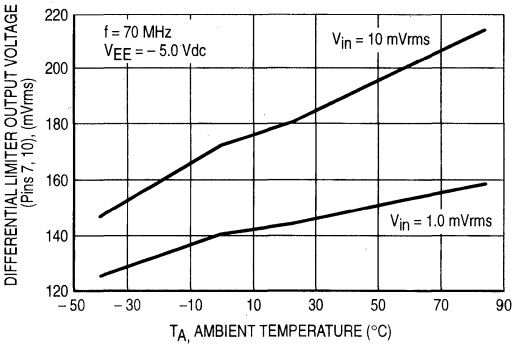


Figure 11A. Differential Detector Output Voltage versus Q of Quadrature LC Tank

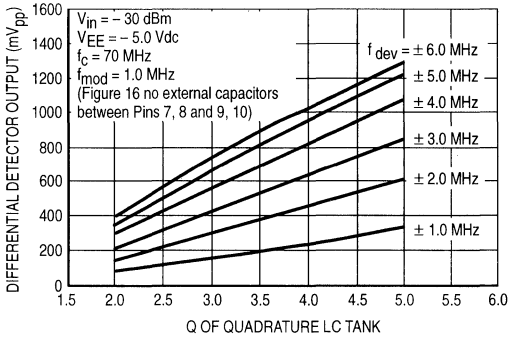


Figure 11B. Differential Detector Output Voltage versus Q of Quadrature LC Tank

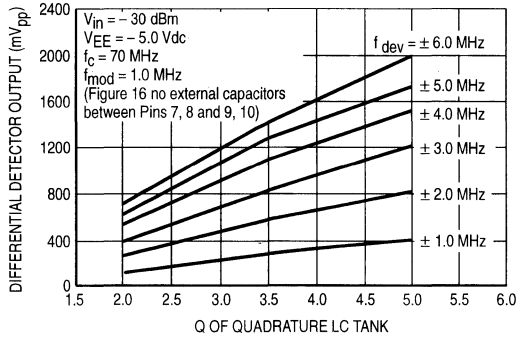


Figure 12. RSSI Output Voltage versus IF Input

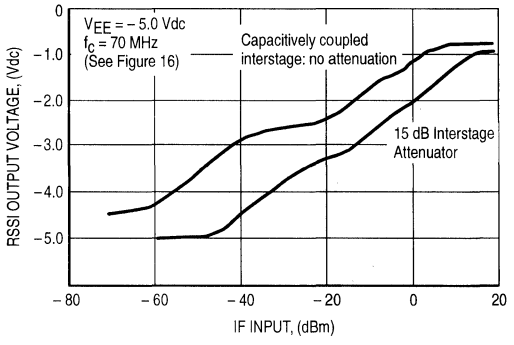
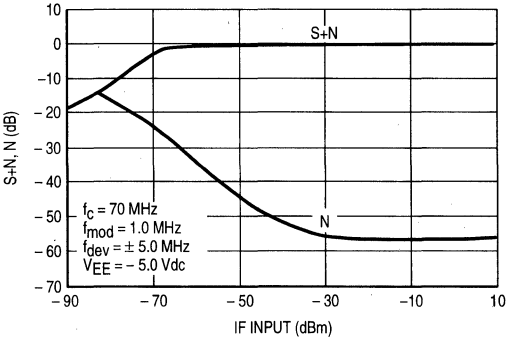


Figure 13. – S+N, N versus IF Input



In the S–parameters measurements, the IF is treated as a two–port linear class A amplifier. The IF amplifier is measured with a single–ended input and output configuration in which the Pins 16 and 7 are terminated in the series combination of a 47 Ω resistor and a 10 nF capacitor to V_{CC} ground (see Figure 14. S–Parameter Test Circuit).

The S–parameters are in polar form as the magnitude (MAG) and angle (ANG). Also listed in the tables are the calculated values for the stability factor (K) and the Maximum Available Gain (MAG). These terms are related in the following equations:

$$K = (1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2) / (2 |S_{12} S_{21}|)$$

where: $|\Delta| = |S_{11} S_{22} - S_{12} S_{21}|$.

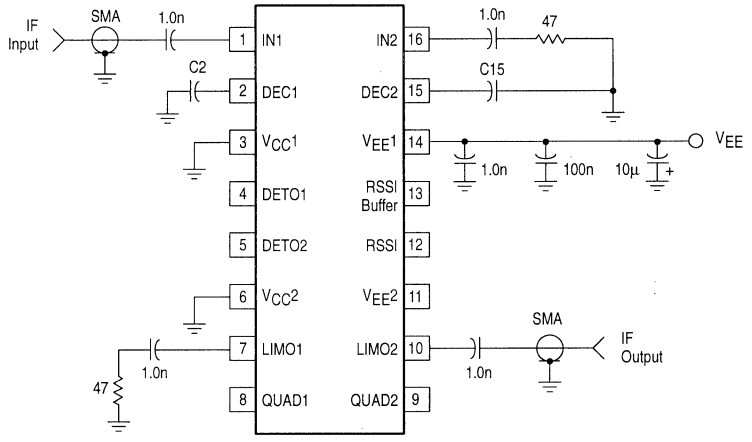
$$MAG = 10 \log |S_{21}| / |S_{12}| + 10 \log |K - (K^2 - 1)^{1/2}|$$

where: K > 1. The necessary and sufficient conditions for unconditional stability are given as K > 1:

$$B1 = 1 + |S_{11}|^2 - |S_{22}|^2 - |\Delta|^2 > 0$$

2

Figure 14. S–Parameter Test Circuit



S–Parameters (V_{EE} = – 5.0 Vdc, T_A = 25°C, C_2 and C_{15} = 0 pF)

Frequency	Input S11		Forward S21		Rev S12		Output S22		K	MAG
MHz	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG	MAG	dB
1.0	0.94	–13	8.2	143	0.001	7.0	0.87	– 22	2.2	32
2.0	0.78	– 23	23.5	109	0.001	– 40	0.64	– 31	4.2	33.5
5.0	0.48	1.0	39.2	51	0.001	– 97	0.34	–17	8.7	33.7
7.0	0.59	15	40.3	34	0.001	– 41	0.33	–13	10.6	34.6
10	0.75	17	40.9	19	0.001	– 82	0.41	–1.0	5.7	36.7
20	0.95	7.0	42.9	– 6.0	0.001	– 42	0.45	0	1.05	46.4
50	0.98	–10	42.2	– 48	0.001	– 9.0	0.52	– 3.0	0.29	–
70	0.95	–16	39.8	– 68	0.001	112	0.54	–16	1.05	46.4
100	0.93	– 23	44.2	– 93	0.001	80	0.53	– 22	0.76	–
150	0.91	– 34	39.5	–139	0.001	106	0.50	– 34	0.94	–
200	0.87	– 47	34.9	–179	0.002	77	0.42	– 44	0.97	–
500	0.89	–103	11.1	– 58	0.022	57	0.40	–117	0.75	–
700	0.61	–156	3.5	–164	0.03	0	0.52	179	2.6	13.7
900	0.56	162	1.2	92	0.048	– 44	0.47	112	4.7	4.5
1000	0.54	131	0.8	42	0.072	– 48	0.44	76	5.1	0.4

S–Parameters (V_{EE} = – 5.0 Vdc, T_A = 25°C, C_2 and C_{15} = 100 pF)

Frequency	Input S11		Forward S21		Rev S12		Output S22		K	MAG
MHz	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG	MAG	dB
1.0	0.98	–15	11.7	174	0.001	–14	0.84	– 27	1.2	37.4
2.0	0.50	– 2.0	39.2	85.5	0.001	–108	0.62	– 35	6.0	35.5
5.0	0.87	8.0	39.9	19	0.001	100	0.47	– 9.0	4.2	39.2
7.0	0.90	5.0	40.4	9.0	0.001	– 40	0.45	– 8.0	3.1	40.3
10	0.92	3.0	41	1.0	0.001	– 40	0.44	– 5.0	2.4	41.8
20	0.92	– 2.0	42.4	–14	0.001	– 87	0.49	– 6.0	2.4	41.9
50	0.91	– 8.0	41.2	– 45	0.001	85	0.50	– 5.0	2.3	42
70	0.91	–11	39.1	– 63	0.001	76	0.52	– 4.0	2.2	41.6
100	0.91	–15	43.4	– 84	0.001	85	0.50	–11	1.3	43.6
150	0.90	– 22	38.2	–126	0.001	96	0.43	– 22	1.4	41.8
200	0.86	– 33	35.5	–160	0.002	78	0.43	– 21	1.3	39.4
500	0.80	– 66	8.3	– 9.0	0.012	75	0.57	– 63	1.7	23.5
700	0.62	– 96	2.9	– 95	0.013	50	0.49	–111	6.3	12.5
900	0.56	–120	1.0	–171	0.020	53	0.44	–150	13.3	2.8
1000	0.54	–136	0.69	154	0.034	65	0.44	–179	12.5	– 0.8

S–Parameters (V_{EE} = – 5.0 Vdc, T_A = 25°C, C_2 and C_{15} = 680 pF)

Frequency	Input S11		Forward S21		Rev S12		Output S22		K	MAG
MHz	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG	MAG	dB
1.0	0.74	4.0	53.6	110	0.001	101	0.97	– 35	0.58	–
2.0	0.90	3.0	70.8	55	0.001	60	0.68	– 34	1.4	45.6
5.0	0.91	0	87.1	21	0.001	–121	0.33	– 60	1.1	49
7.0	0.91	0	90.3	11	0.001	–18	0.25	– 67	1.2	48.4
10	0.91	– 2.0	92.4	2.0	0.001	33	0.14	– 67	1.5	47.5
20	0.91	– 4.0	95.5	–16	0.001	63	0.12	–15	1.3	48.2
50	0.90	– 8.0	89.7	– 50	0.001	– 43	0.24	26	1.8	46.5
70	0.90	–10	82.6	–70	0.001	92	0.33	21	1.4	47.4
100	0.91	–14	77.12	–93	0.001	23	0.42	–1.0	1.05	49
150	0.94	– 20	62.0	–122	0.001	96	0.42	– 22	0.54	–
200	0.95	– 33	56.9	–148	0.003	146	0.33	– 62	0.75	–
500	0.82	– 63	12.3	–12	0.007	79	0.44	– 67	1.8	26.9
700	0.66	– 98	3.8	–107	0.014	84	0.40	–115	4.8	14.6
900	0.56	–122	1.3	177	0.028	78	0.39	–166	8.0	4.7
1000	0.54	–139	0.87	141	0.048	76	0.41	165	7.4	0.96

S–Parameters (V_{EE} = – 3.0 Vdc, T_A = 25°C, C_2 and C_{15} = 0 pF)

Frequency	Input S11		Forward S21		Rev S12		Output S22		K	MAG
MHz	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG	MAG	dB
1.0	0.89	–14	9.3	136	0.001	2.0	0.84	– 27	3.2	30.7
2.0	0.76	– 22	24.2	105	0.001	– 90	0.67	– 37	3.5	34.3
5.0	0.52	5.0	35.7	46	0.001	– 32	0.40	–13	10.6	33.3
7.0	0.59	12	38.1	34	0.001	– 41	0.40	–10	9.1	34.6
10	0.78	15	37.2	16	0.001	– 92	0.40	–1.0	5.7	36.3
20	0.95	5.0	38.2	– 9.0	0.001	47	0.51	– 4.0	0.94	–
50	0.96	–11	39.1	– 50	0.001	–103	0.48	– 6.0	1.4	43.7
70	0.93	–17	36.8	– 71	0.001	– 76	0.52	–13	2.2	41.4
100	0.91	– 25	34.7	– 99	0.001	–152	0.51	–19	3.0	39.0
150	0.86	– 37	33.8	–143	0.001	53	0.49	– 34	1.7	39.1
200	0.81	– 49	27.8	86	0.003	76	0.55	– 56	2.4	35.1
500	0.70	– 93	6.2	– 41	0.015	93	0.40	–110	2.4	19.5
700	0.62	–144	1.9	–133	0.049	56	0.40	–150	3.0	8.25
900	0.39	–176	0.72	125	0.11	–18	0.25	163	5.1	–1.9
1000	0.44	166	0.49	80	0.10	– 52	0.33	127	7.5	– 4.8

S–Parameters (V_{EE} = – 3.0 Vdc, T_A = 25°C, C_2 and C_{15} = 100 pF)

Frequency	Input S11		Forward S21		Rev S12		Output S22		K	MAG
MHz	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG	MAG	dB
1.0	0.97	–15	11.7	171	0.001	– 4.0	0.84	– 27	1.4	36.8
2.0	0.53	2.0	37.1	80	0.001	– 91	0.57	– 31	6.0	34.8
5.0	0.88	7.0	37.7	18	0.001	– 9.0	0.48	– 7.0	3.4	39.7
7.0	0.90	5.0	37.7	8.0	0.001	–11	0.49	– 7.0	2.3	41
10	0.92	2.0	38.3	1.0	0.001	– 59	0.51	– 9.0	2.0	41.8
20	0.92	– 2.0	39.6	–15	0.001	29	0.48	– 3.0	1.9	42.5
50	0.91	– 8.0	38.5	– 46	0.001	– 21	0.51	– 7.0	2.3	41.4
70	0.91	–11	36.1	– 64	0.001	49	0.50	– 8.0	2.3	40.8
100	0.91	–15	39.6	– 85	0.001	114	0.52	–13	1.7	37.8
150	0.89	– 22	34.4	–128	0.001	120	0.48	– 23	1.6	40.1
200	0.86	– 33	32	–163	0.002	86	0.40	– 26	1.7	37.8
500	0.78	– 64	7.6	–12	0.013	94	0.46	– 71	1.9	22.1
700	0.64	– 98	2.3	–102	0.027	58	0.42	–109	4.1	10.1
900	0.54	–122	0.78	179	0.040	38.6	0.35	–147	10.0	– 0.14
1000	0.53	–136	0.47	144	0.043	23	0.38	–171	15.4	– 4.52

S–Parameters (V_{EE} = – 3.0 Vdc, T_A = 25°C, C_2 and C_{15} = 680 pF)

Frequency	Input S11		Forward S21		Rev S12		Output S22		K	MAG
MHz	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG	MAG	dB
1.0	0.81	3.0	37	101	0.001	–19	0.90	– 32	1.1	43.5
2.0	0.90	2.0	47.8	52.7	0.001	– 82	0.66	– 39	0.72	–
5.0	0.91	0	58.9	20	0.001	104	0.37	– 56	2.3	44
7.0	0.90	–1	60.3	11	0.001	– 76	0.26	– 55	2.04	44
10	0.91	– 2.0	61.8	3.0	0.001	105	0.18	– 52	2.2	43.9
20	0.91	– 4.0	63.8	– 15	0.001	59	0.11	–13	2.0	44.1
50	0.90	– 8.0	60.0	– 48	0.001	96	0.22	33	2.3	43.7
70	0.90	–11	56.5	– 67	0.001	113	0.29	15	2.3	43.2
100	0.91	–14	52.7	– 91	0.001	177	0.36	5.0	2.0	43
150	0.93	– 21	44.5	–126	0.001	155	0.35	–17	1.8	42.7
200	0.90	– 43	41.2	–162	0.003	144	0.17	– 31	1.6	34.1
500	0.79	– 65	7.3	–13	0.008	80	0.44	– 75	3.0	22
700	0.65	– 97	2.3	–107	0.016	86	0.38	–124	7.1	10.2
900	0.56	–122	0.80	174	0.031	73	0.38	–174	12	0.37
1000	0.55	–139	0.52	137	0.50	71	0.41	157	11.3	– 3.4

DC Biasing Considerations

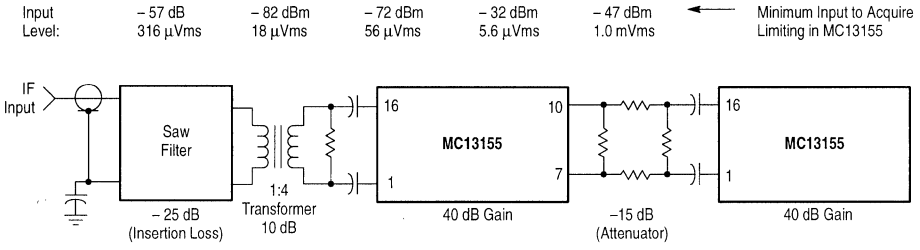
The DC biasing scheme utilizes two V_{CC} connections (Pins 3 and 6) and two V_{EE} connections (Pins 14 and 11). $V_{EE}1$ (Pin 14) is connected internally to the IF and RSSI circuits' negative supply bus while $V_{EE}2$ (Pin 11) is connected internally to the quadrature detector's negative bus. Under positive ground operation, this unique configuration offers the ability to bias the RSSI and IF separately from the quadrature detector. When two ICs are cascaded as shown in the 70 MHz application circuit and provided by the PCB (see Figures 17 and 18), the first MC13155 is used without biasing its quadrature detector, thereby saving approximately 3.0 mA. A total current of 7.0 mA is used to fully bias each IC, thus the total current in the application circuit is approximately 11 mA. Both V_{CC} pins are biased by the same supply. $V_{CC}1$ (Pin 3) is connected internally to the positive bus of the first half of the IF limiting amplifier, while $V_{CC}2$ is internally connected to the positive bus of the RSSI, the quadrature detector circuit, and the second half of the IF limiting amplifier (see Figure 15). This distribution of the V_{CC} enhances the stability of the IC.

RSSI Circuitry

The RSSI circuitry provides typically 35 dB of linear dynamic range and its output voltage swing is adjusted by selection of the resistor from Pin 12 to V_{EE}. The RSSI slope is typically 2.1 μA/dB ; thus, for a dynamic range of 35 dB, the current output is approximately 74 μA. A 47 k resistor will yield an RSSI output voltage swing of 3.5 Vdc. The RSSI buffer output at Pin 13 is an emitter–follower and needs an external emitter resistor of 10 k to V_{EE}.

In a cascaded configuration (see circuit application in Figure 16), only one of the RSSI Buffer outputs (Pin 13) is used; the RSSI outputs (Pin 12 of each IC) are tied together and the one closest to the V_{EE} supply trace is decoupled to V_{CC} ground. The two pins are connected to V_{EE} through a 47 k resistor. This resistor sources a RSSI current which is proportional to the signal level at the IF input; typically, 1.0 mVrms (– 47 dBm) is required to place the MC13155 into limiting. The measured RSSI output voltage response of the application circuit is shown in Figure 12. Since the RSSI current output is dependent upon the input signal level at the IF input, a careful accounting of filter losses, matching and other losses and gains must be made in the entire receiver system. In the block diagram of the application circuit shown below, an accounting of the signal levels at points throughout the system shows how the RSSI response in Figure 12 is justified.

Block Diagram of 70 MHz Video Receiver Application Circuit

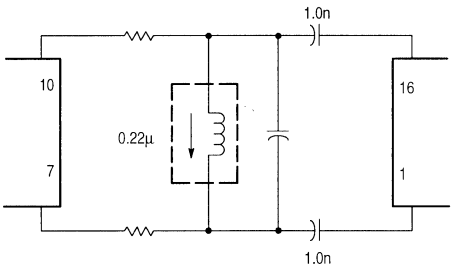


Cascading Stages

The limiting IF output is pinned–out differentially, cascading is easily achieved by AC coupling stage to stage. In the evaluation PCB, AC coupling is shown, however, interstage filtering may be desirable in some applications. In which case, the S–parameters provide a means to implement a low loss interstage match and better receiver sensitivity.

Where a linear response of the RSSI output is desired when cascading the ICs, it is necessary to provide at least 10 dB of interstage loss. Figure 12 shows the RSSI response with and without interstage loss. A 15 dB resistive attenuator is an inexpensive way to linearize the RSSI response. This has its drawbacks since it is a wideband noise source that is dependent upon the source and load impedance and the amount of attenuation that it provides. A better, although more costly, solution would be a bandpass filter designed to the desired center frequency and bandpass response while carefully selecting the insertion loss. A network topology shown below may be used to provide a bandpass response with the desired insertion loss.

Network Topology



Quadrature Detector

The quadrature detector is coupled to the IF with internal 2.0 pF capacitors between Pins 7 and 8 and Pins 9 and 10. For wideband data applications, such as FM video and satellite receivers, the drive to the detector can be increased with additional external capacitors between these pins, thus, the recovered video signal level output is increased for a given bandwidth (see Figure 11A and Figure 11B).

The wideband performance of the detector is controlled by the loaded Q of the LC tank circuit. The following equation defines the components which set the detector circuit's bandwidth:

$$Q = R_T/X_L \quad (1)$$

where: R_T is the equivalent shunt resistance across the LC Tank and X_L is the reactance of the quadrature inductor at the IF frequency ($X_L = 2\pi fL$).

The inductor and capacitor are chosen to form a resonant LC Tank with the PCB and parasitic device capacitance at the desired IF center frequency as predicted by:

$$fc = (2\pi \sqrt{(LC_p)})^{-1} \quad (2)$$

where: L is the parallel tank inductor and C_p is the equivalent parallel capacitance of the parallel resonant tank circuit.

The following is a design example for a wideband detector at 70 MHz and a loaded Q of 5. The loaded Q of the quadrature detector is chosen somewhat less than the Q of the IF bandpass. For an IF frequency of 70 MHz and an IF bandpass of 10.9 MHz, the IF bandpass Q is approximately 6.4.

Example:

Let the external Cext = 20 pF. (The minimum value here should be greater than 15 pF making it greater than the internal device and PCB parasitic capacitance, Cint ≈ 3.0 pF).

$$C_p = Cint + Cext = 23\ pF$$

Rewrite Equation 2 and solve for L:

$L = (0.159)^2 / (C_p\ fc^2)$

L = 198 nH, thus, a standard value is chosen.

L = 0.22 μH (tunable shielded inductor).

The value of the total damping resistor to obtain the required loaded Q of 5 can be calculated by rearranging Equation 1:

$$R_T = Q(2\pi fL)$$

$R_T = 5\ (2\pi)(70)(0.22) = 483.8\ \Omega.$

The internal resistance, Rint between the quadrature tank Pins 8 and 9 is approximately 3200 Ω and is considered in determining the external resistance, Rext which is calculated from:

Rext = $((R_T)(Rint))/ (Rint - R_T)$

Rext = 570, thus, choose the standard value.

Rext = 560 Ω.

SAW Filter

In wideband video data applications, the IF occupied bandwidth may be several MHz wide. A good rule of thumb is to choose the IF frequency about 10 or more times greater than the IF occupied bandwidth. The IF bandpass filter is a SAW filter in video data applications where a very selective response is needed (i.e., very sharp bandpass response). The evaluation PCB is laid out to accommodate two SAW filter package types: 1) A five–leaded plastic SIP package. Recommended part numbers are Siemens X6950M which operates at 70 MHz; 10.4 MHz 3 dB passband, X6951M (X252.8) which operates at 70 MHz; 9.2 MHz 3 dB passband; and X6958M which operates at 70 MHz, 6.3 MHz 3 dB passband, and 2) A four–leaded TO–39 metal can package. Typical insertion loss in a wide bandpass SAW filter is 25 dB.

The above SAW filters require source and load impedances of 50 Ω to assure stable operation. On the PC board layout, space is provided to add a matching network, such as a 1:4 surface mount transformer between the SAW filter output and the input to the MC13155. A 1:4 transformer, made by Coilcraft and Mini Circuits, provides a suitable interface (see Figures 16, 17 and 18). In the circuit and layout, the SAW filter and the MC13155 are differentially configured with interconnect traces which are equal in length and symmetrical. This balanced feed enhances RF stability, phase linearity, and noise performance.

Figure 15. Simplified Internal Circuit Schematic

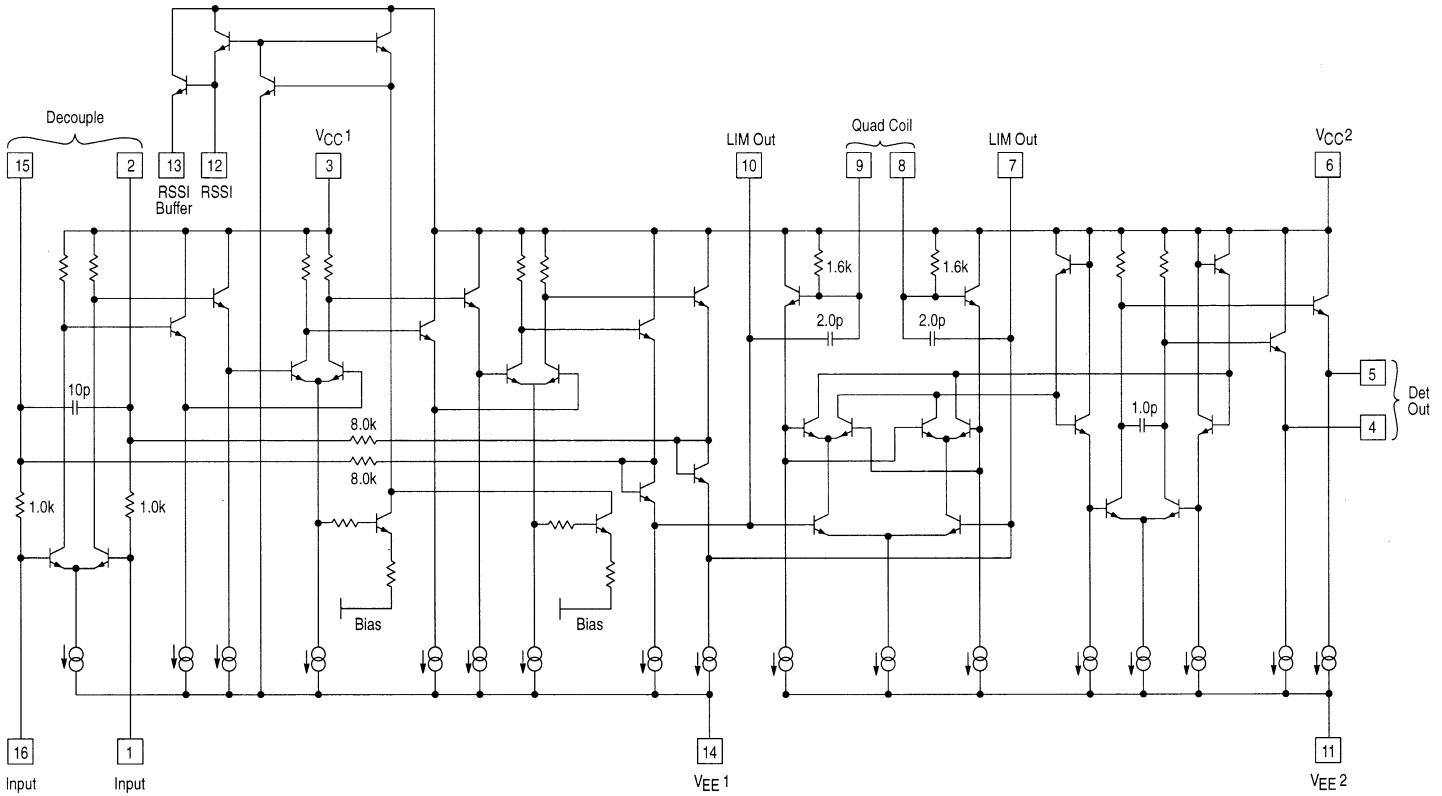


Figure 16. 70 MHz Video Receiver Application Circuit

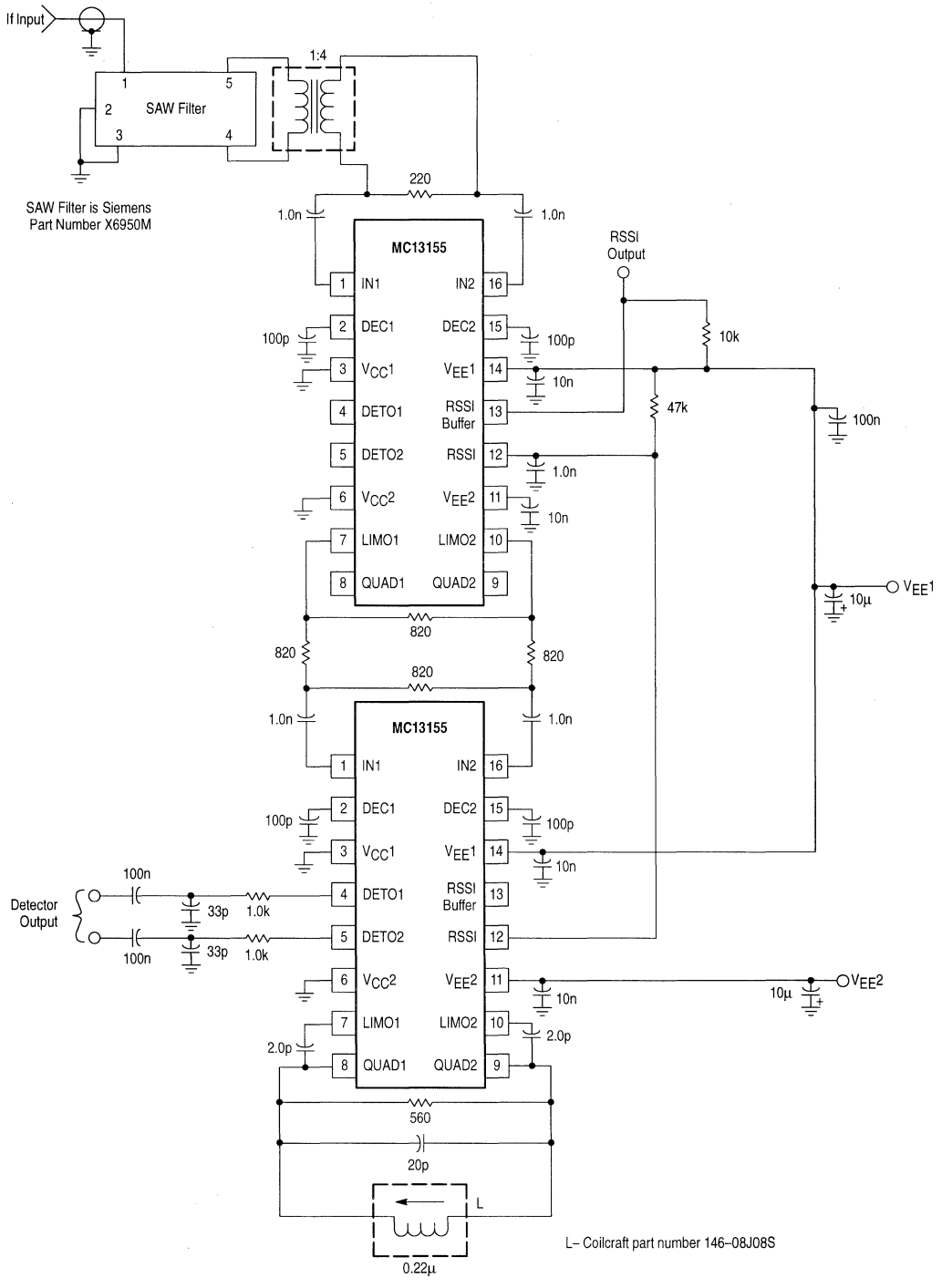


Figure 17. Component Placement (Circuit Side)

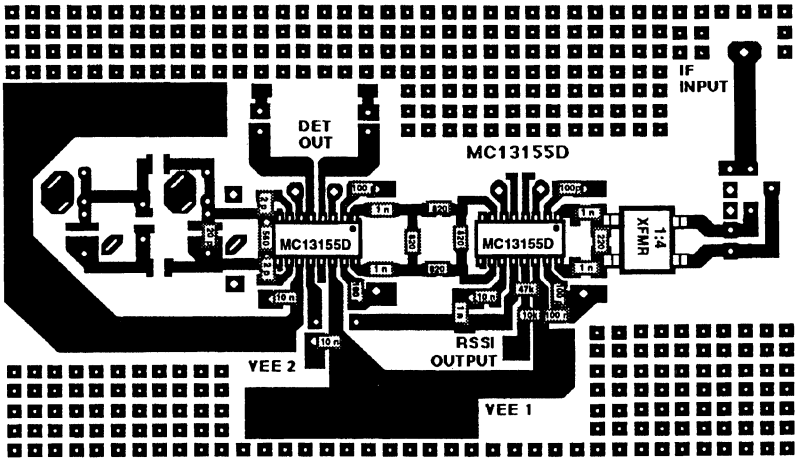


Figure 18. Component Placement (Ground Side)

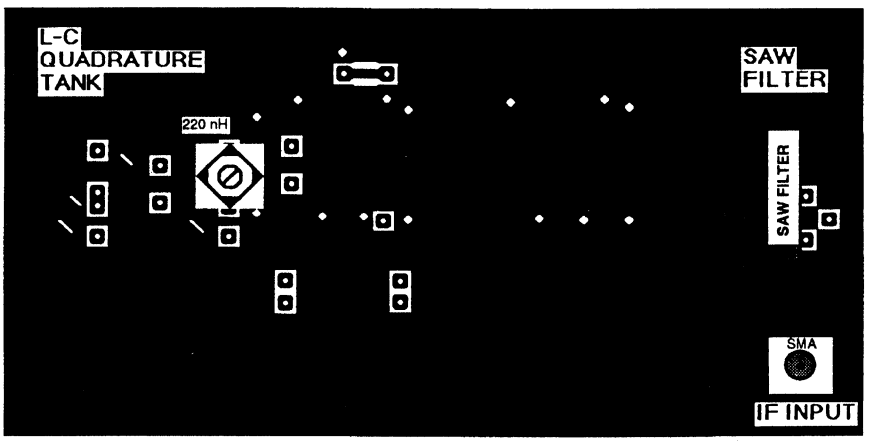


Figure 19. Circuit Side View

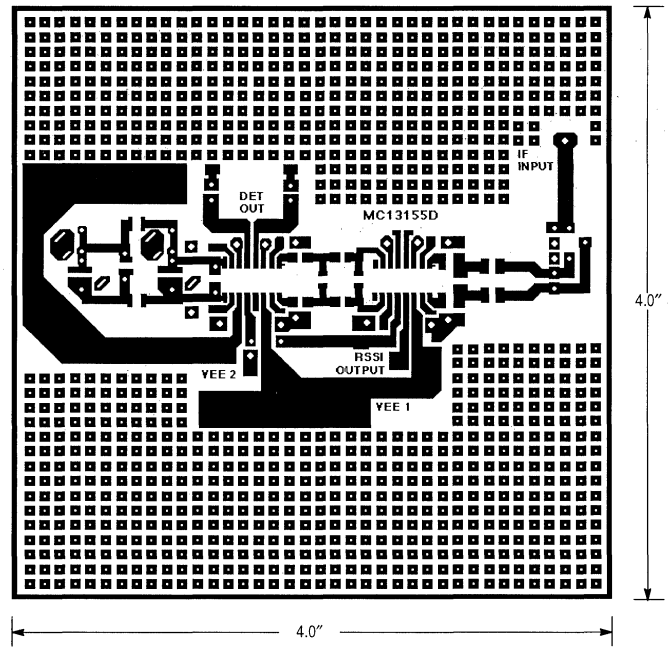
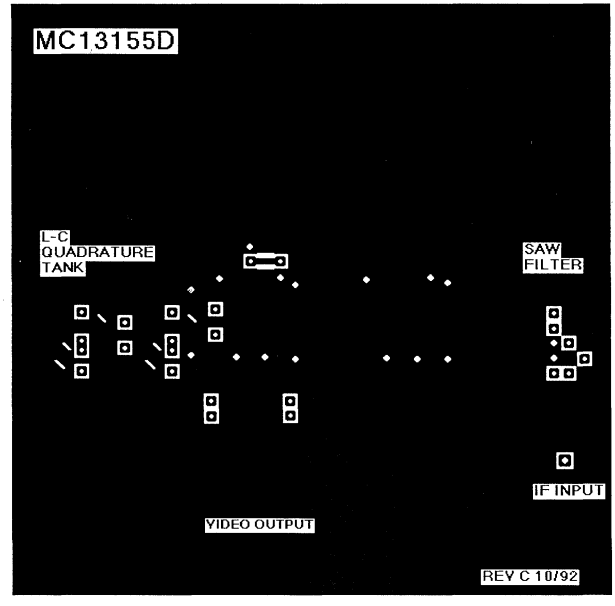


Figure 20. Ground Side View



MOTOROLA

MC13156

Advance Information

Wideband FM IF System

The MC13156 is a wideband FM IF subsystem targeted at high performance data and analog applications. Excellent high frequency performance is achieved at low cost using Motorola's MOSAIC 1.5™ bipolar process. The MC13156 has an onboard grounded collector VCO transistor that may be used with a fundamental or overtone crystal in single channel operation or with a PLL in multichannel operation. The mixer is useful to 500 MHz and may be used in a balanced–differential, or single–ended configuration. The IF amplifier is split to accommodate two low cost cascaded filters. RSSI output is derived by summing the output of both IF sections. A precision data shaper has a hold function to preset the shaper for fast recovery of new data.

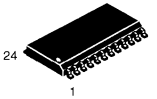
Applications for the MC13156 include CT–2, wideband data links, and other radio systems utilizing GMSK, FSK or FM modulation.

- 2.0 to 6.0 Vdc Operation
- Typical Sensitivity at 200 MHz of 2.0 μV for 12 dB SINAD
- RSSI Dynamic Range Typically 80 dB
- High Performance Data Shaper for Enhanced CT–2 Operation
- Internal 330 Ω and 1.4 kΩ Terminations for 10.7 MHz and 455 kHz Filters
- Split IF for Improved Filtering and Extended RSSI Range
- 3rd Order Intercept (Input) of – 25 dBm (Input Matched)

WIDEBAND FM IF SYSTEM FOR DIGITAL AND ANALOG APPLICATIONS

SEMICONDUCTOR TECHNICAL DATA

2



DW SUFFIX
PLASTIC PACKAGE
CASE 751E
(SO–24L)

FB SUFFIX
PLASTIC QFP PACKAGE
CASE 873

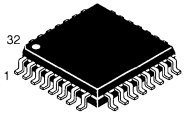
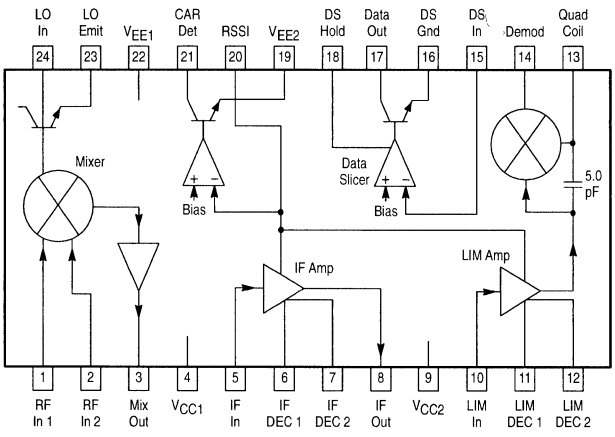


Figure 1. Simplified Block Diagram



NOTE: Pin Numbers shown for SOIC package only. Refer to Pin Assignments Table.

PIN CONNECTIONS

Function	SO–24L	QFP
RF Input 1	1	31
RF Input 2	2	32
Mixer Output	3	1
V_{CC1}	4	2
IF Amp Input	5	3
IF Amp Decoupling 1	6	4
IF Amp Decoupling 2	7	5
V_{CC} Connect (N/C Internal)	–	6
IF Amp Output	8	7
V_{CC2}	9	8
Limiter IF Input	10	9
Limiter Decoupling 1	11	10
Limiter Decoupling 2	12	11
V_{CC} Connect (N/C Internal)	–	12, 13, 14
Quad Coil	13	15
Demodulator Output	14	16
Data Slicer Input	15	17
V_{CC} Connect (N/C Internal)	–	18
Data Slicer Ground	16	19
Data Slicer Output	17	20
Data Slicer Hold	18	21
V_{EE2}	19	22
RSSI Output/Carrier Detect In	20	23
Carrier Detect Output	21	24
V_{EE1} and Substrate	22	25
LO Emitter	23	26
LO Base	24	27
V_{CC} Connect (N/C Internal)	–	28, 29, 30

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC13156DW	T_A = – 40 to +85°C	SO–24L
MC13156FB		QFP

 Rev 1

MAXIMUM RATINGS

Rating	Pin	Symbol	Value	Unit
Power Supply Voltage	16, 19, 22	$V_{EE(max)}$	– 6.5	Vdc
Junction Temperature	–	$T_{J(max)}$	+150	°C
Storage Temperature Range	–	T_{stg}	– 65 to +150	°C

Devices should not be operated at or outside these values. The "Recommended Operating Conditions" table provides for actual device operation.

RECOMMENDED OPERATING CONDITIONS

Rating	Pin	Symbol	Value	Unit
Power Supply Voltage @ T_A = 25°C – 40°C ≤ T_A ≤ + 85°C	4, 9 16, 19, 22	V_{CC} V_{EE}	0 (Ground) – 2.0 to – 6.0	Vdc
Input Frequency	1, 2	f_{in}	500	MHz
Ambient Temperature Range	–	T_A	– 40 to + 85	°C
Input Signal Level	1, 2	V_{in}	200	mVrms

DC ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC1} = V_{CC2} = 0, no input signal.)

Characteristic	Pin	Symbol	Min	Typ	Max	Unit
Total Drain Current (See Figure 3)	19, 22	I_{Total}				mA
V_{EE} = – 2.0 Vdc			–	4.8	–	
V_{EE} = – 3.0 Vdc			3.0	5.0	8.0	
V_{EE} = – 5.0 Vdc			–	5.2	–	
V_{EE} = – 6.0 Vdc			–	5.4	–	
Drain Current, I_{22} (See Figure 4)	22	I_{22}				mA
V_{EE} = – 2.0 Vdc			–	3.0	–	
V_{EE} = – 3.0 Vdc			–	3.1	–	
V_{EE} = – 5.0 Vdc			–	3.3	–	
V_{EE} = – 6.0 Vdc			–	3.4	–	
Drain Current, I_{19} (See Figure 4)	19	I_{19}				mA
V_{EE} = – 2.0 Vdc			–	1.8	–	
V_{EE} = – 3.0 Vdc			–	1.9	–	
V_{EE} = – 5.0 Vdc			–	1.9	–	
V_{EE} = – 6.0 Vdc			–	2.0	–	
DATA SLICER (Input Voltage Referenced to V_{EE} = – 3.0 Vdc, no input signal; See Figure 16.)						
Input Threshold Voltage (High V_{in})	15	V_{15}	1.0	1.1	1.2	Vdc
Output Current (Low V_{in}) Data Slicer Enabled (No Hold) V_{15} > 1.1 Vdc V_{18} = 0 Vdc	17	I_{17}	–	1.7	–	mA

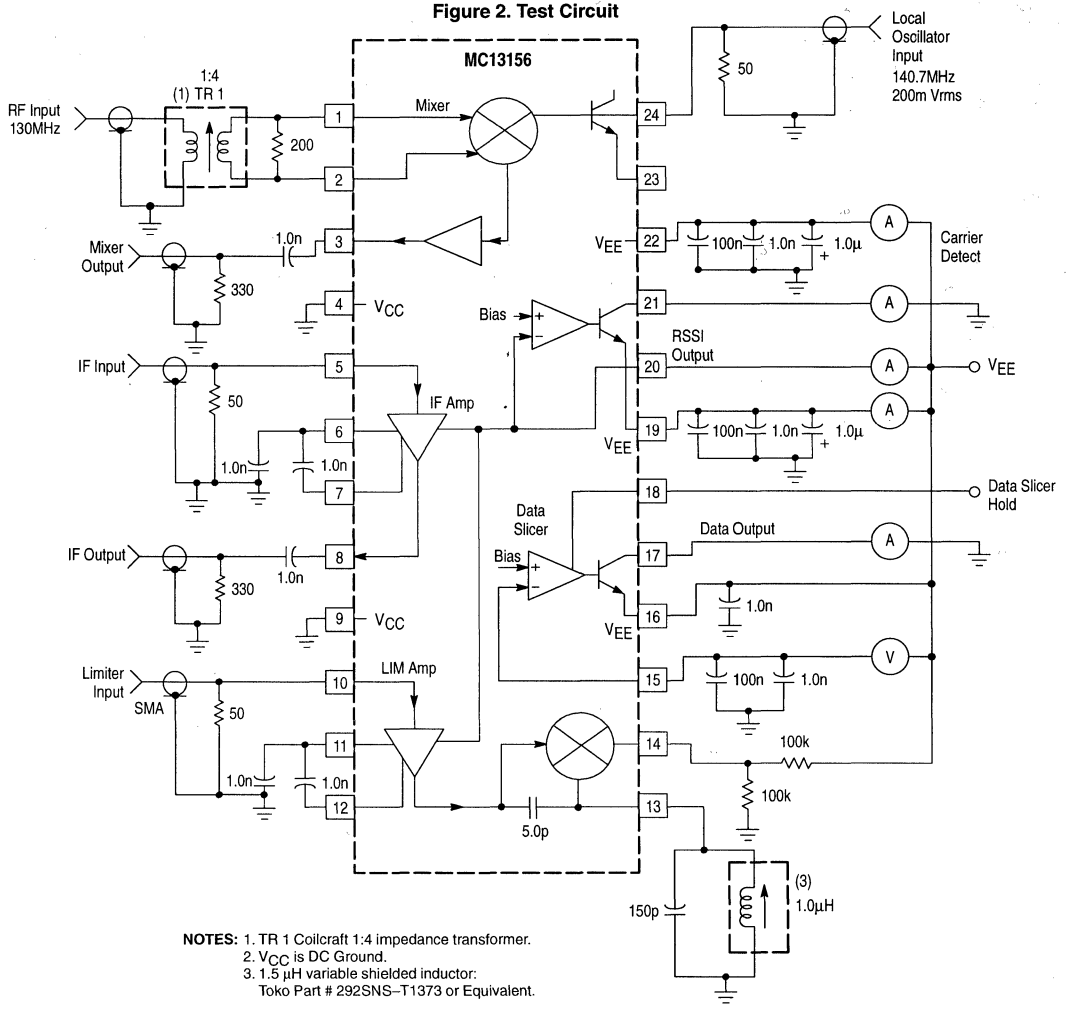
AC ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{EE} = – 3.0 Vdc, f_{RF} = 130 MHz, f_{LO} = 140.7 MHz, Figure 2 test circuit, unless otherwise specified.)

Characteristic	Pin	Symbol	Min	Typ	Max	Unit
12 dB SINAD Sensitivity (See Figures 18, 26) f_{in} = 144.45 MHz; f_{mod} = 1.0 kHz; f_{dev} = ± 75 kHz	1, 14		–	–100	–	dBm
MIXER						
Conversion Gain P_{in} = – 37 dBm (Figure 5)	1, 3		–	22	–	dB
Mixer Input Impedance Single–Ended (Table 1)	1, 2	R_p C_p	– –	1.0 4.0	– –	kΩ pF
Mixer Output Impedance	3		–	330	–	Ω
IF AMPLIFIER SECTION						
IF RSSI Slope (Figure 7)	20		0.2	0.4	0.6	μA/dB
IF Gain (Figure 6)	5, 8		–	39	–	dB

AC ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{EE} = – 3.0 Vdc, f_{RF} = 130 MHz, f_{LO} = 140.7 MHz, Figure 2 test circuit, unless otherwise specified.)

Characteristic	Pin	Symbol	Min	Typ	Max	Unit
IF AMPLIFIER SECTION						
Input Impedance	5		–	1.4	–	kΩ
Output Impedance	8		–	290	–	Ω
LIMITING AMPLIFIER SECTION						
Limiter RSSI Slope (Figure 8)	20		0.2	0.4	0.6	μA/dB
Limiter Gain	–		–	55	–	dB
Input Impedance	10		–	1.4	–	kΩ
CARRIER DETECT						
Output Current – Carrier Detect (High V_{in})	21		–	0	–	μA
Output Current – Carrier Detect (Low V_{in})	21		–	3.0	–	mA
Input Threshold Voltage – Carrier Detect Input Voltage Referenced to V_{EE} = – 3.0 Vdc	20		0.9	1.2	1.4	Vdc

Figure 2. Test Circuit



NOTES: 1. TR 1 Coilcraft 1:4 impedance transformer.
2. V_{CC} is DC Ground.
3. 1.5 µH variable shielded inductor:
Toko Part # 292SNS–T1373 or Equivalent.

Figure 3. Total Drain Current versus Supply Voltage and Temperature

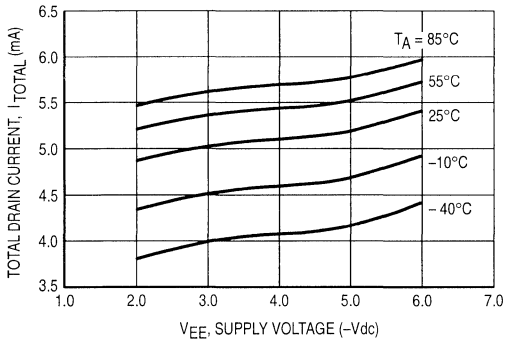


Figure 4. Drain Currents versus Supply Voltage

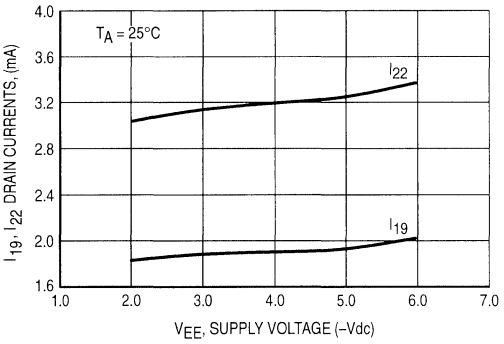


Figure 5. Mixer Gain versus Input Signal Level

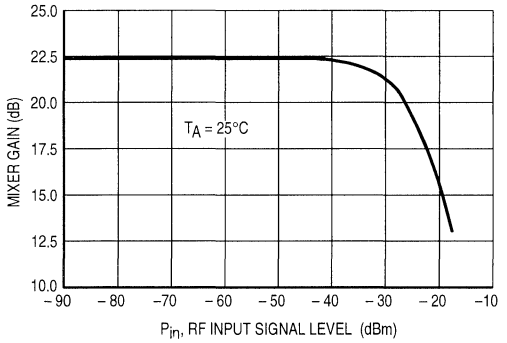


Figure 6. IF Amplifier Gain versus Input Signal Level and Ambient Temperature

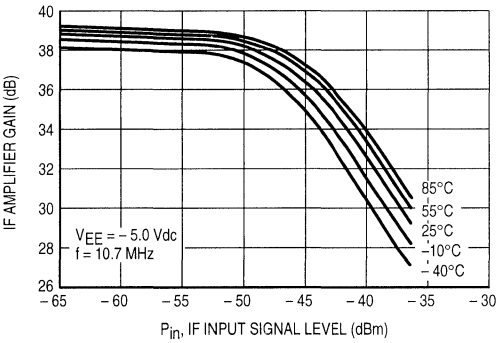


Figure 7. IF Amplifier RSSI Output Current versus Input Signal Level and Ambient Temperature

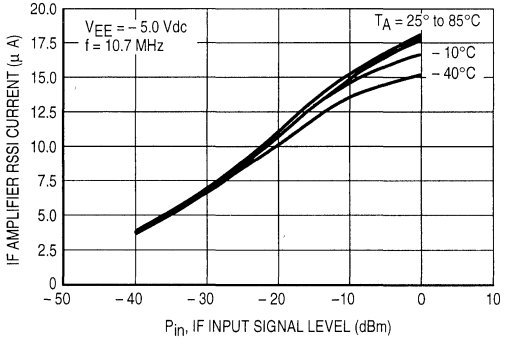


Figure 8. Limiter Amplifier RSSI Output Current versus Input Signal Level and Temperature

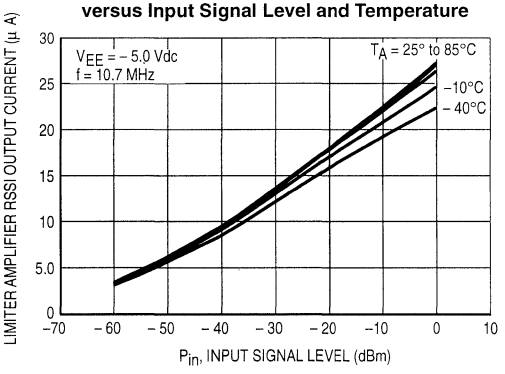
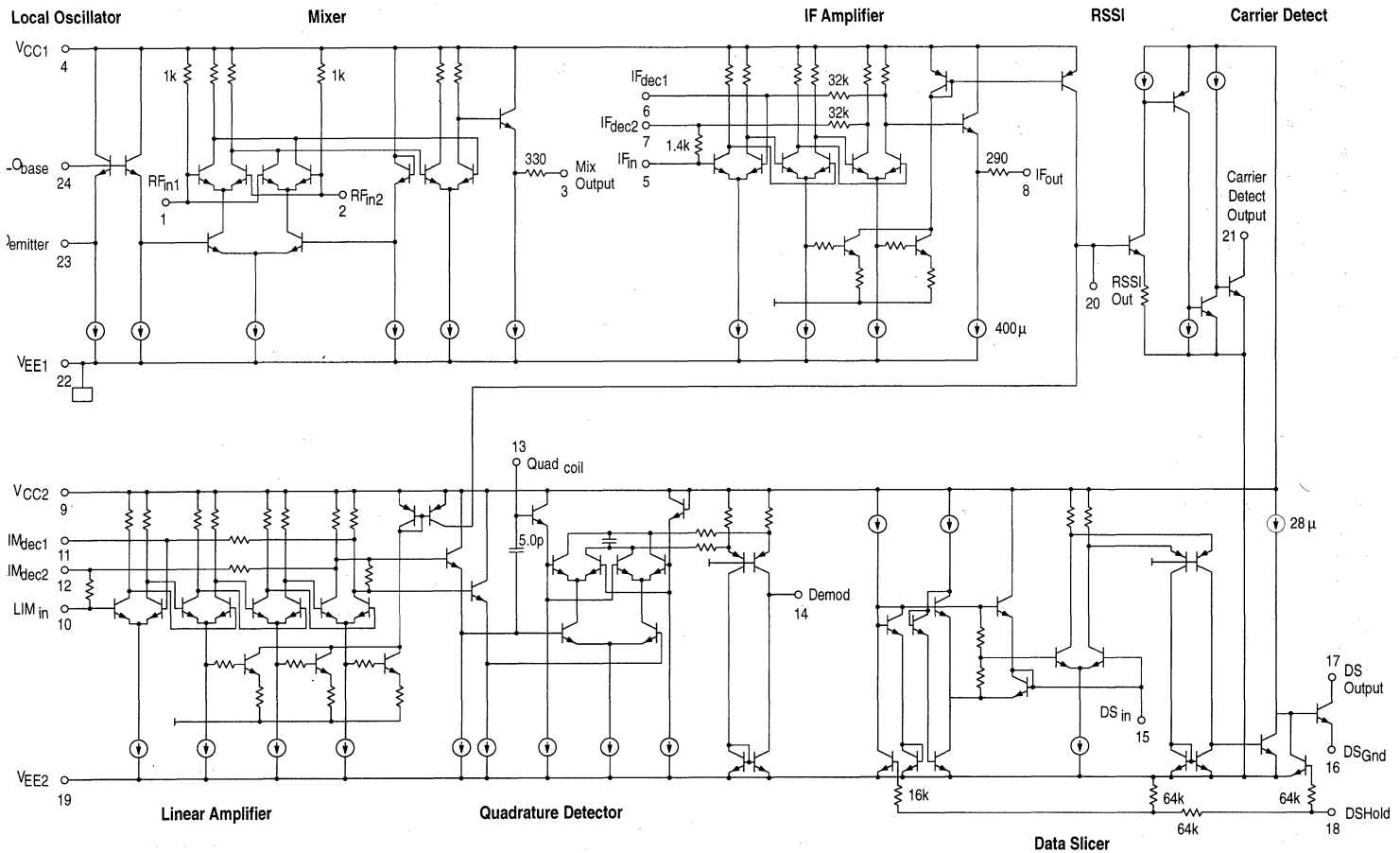


Figure 9. MC13156DW Internal Circuit Schematic



CIRCUIT DESCRIPTION

General

The MC13156 is a low power single conversion wideband FM receiver incorporating a split IF. This device is designated for use as the backend in digital FM systems such as CT–2 and wideband data links with data rates up to 500 kbaud. It contains a mixer, oscillator, signal strength meter drive, IF amplifier, limiting IF, quadrature detector and a data slicer with a hold function (refer to Figure 9, Simplified Internal Circuit Schematic).

Current Regulation

Temperature compensating voltage independent current regulators are used throughout.

Mixer

The mixer is a double–balanced four quadrant multiplier and is designed to work up to 500 MHz. It can be used in differential or in single–ended mode by connecting the other input to the positive supply rail.

Figure 5 shows the mixer gain and saturated output response as a function of input signal drive. The circuit used to measure this is shown in Figure 2. The linear gain of the mixer is approximately 22 dB. Figure 10 shows the mixer gain versus the IF output frequency with the local oscillator of 150 MHz at 100 mVrms LO drive level. The RF frequency is swept. The sensitivity of the IF output of the mixer is shown in Figure 11 for an RF input drive of 10 mVrms at 140 MHz and IF at 10 MHz.

The single–ended parallel equivalent input impedance of the mixer is Rp ~ 1.0 kΩ and Cp ~ 4.0 pF (see Table 1 for details). The buffered output of the mixer is internally loaded resulting in an output impedance of 330 Ω.

Local Oscillator

The on–chip transistor operates with crystal and LC resonant elements up to 220 MHz. Series resonant, overtone crystals are used to achieve excellent local oscillator stability. 3rd overtone crystals are used through about 65 to 70 MHz. Operation from 70 MHz up to 180 MHz is feasible using the on–chip transistor with a 5th or 7th overtone crystal. To enhance operation using an overtone crystal, the internal transistor's bias is increased by adding an external resistor from Pin 23 to V_{EE}. –10 dBm of local oscillator drive is needed to adequately drive the mixer (Figure 11).

The oscillator configurations specified above, and two others using an external transistor, are described in the application section:

1) A 133 MHz oscillator multiplier using a 3rd overtone crystal, and
2) A 307.8 to 309.3 MHz manually tuned, varactor controlled local oscillator.

RSSI

The Received Signal Strength Indicator (RSSI) output is a current proportional to the log of the received signal amplitude. The RSSI current output is derived by summing the currents from the IF and limiting amplifier stages. An external resistor at Pin 20 sets the voltage range or swing of the RSSI output voltage. Linearity of the RSSI is optimized by using external ceramic or crystal bandpass filters which have an insertion loss of 8.0 dB. The RSSI circuit is designed to provide 70+ dB of dynamic range with temperature compensation (see Figures 7 and 8 which show RSSI responses of the IF and Limiter amplifiers). Variation in the RSSI output current with supply voltage is small (see Figure 12).

Carrier Detect

When the meter current flowing through the meter load resistance reaches 1.2 Vdc above ground, the comparator flips, causing the carrier detect output to go high. Hysteresis can be accomplished by adding a very large resistor for positive feedback between the output and the input of the comparator.

IF Amplifier

The first IF amplifier section is composed of three differential stages with the second and third stages contributing to the RSSI. This section has internal DC feedback and external input decoupling for improved symmetry and stability. The total gain of the IF amplifier block is approximately 39 dB at 10.7 MHz. Figure 6 shows the gain and saturated output response of the IF amplifier over temperature, while Figure 13 shows the IF amplifier gain as a function of the IF frequency.

The fixed internal input impedance is 1.4 kΩ. It is designed for applications where a 455 kHz ceramic filter is used and no external output matching is necessary since the filter requires a 1.4 kΩ source and load impedance.

For 10.7 MHz ceramic filter applications, an external 430 Ω resistor must be added in parallel to provide the equivalent load impedance of 330 Ω that is required by the filter; however, no external matching is necessary at the input since the mixer output matches the 330 Ω source impedance of the filter. For 455 kHz applications, an external 1.1 kΩ resistor must be added in series with the mixer output to obtain the required matching impedance of 1.4 kΩ of the filter input resistance. Overall RSSI linearity is dependent on having total midband attenuation of 12 dB (6 dB insertion loss plus 6.0 dB impedance matching loss) for the filter. The output of the IF amplifier is buffered and the impedance is 290 Ω.

Limiter

The limiter section is similar to the IF amplifier section except that four stages are used with the last three contributing to the RSSI. The fixed internal input impedance is 1.4 kΩ. The total gain of the limiting amplifier section is approximately 55 dB. This IF limiting amplifier section internally drives the quadrature detector section.

Figure 10. Mixer Gain versus IF Frequency

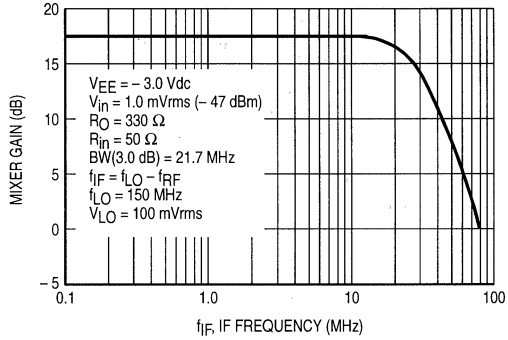


Figure 11. Mixer IF Output Level versus Local Oscillator Input Level

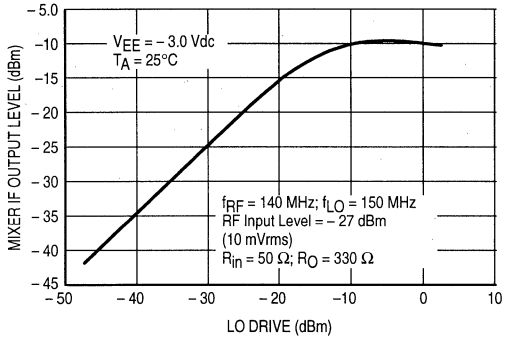


Figure 12. RSSI Output Current versus Supply Voltage and RF Input Signal Level

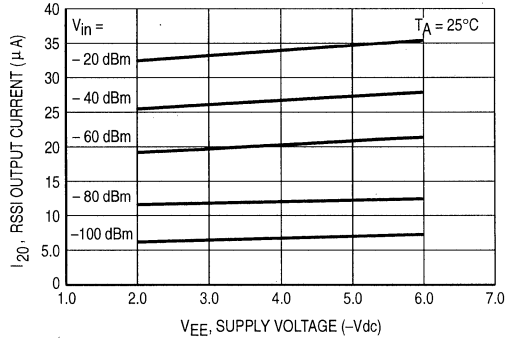


Figure 13. IF Amplifier Gain versus IF Frequency

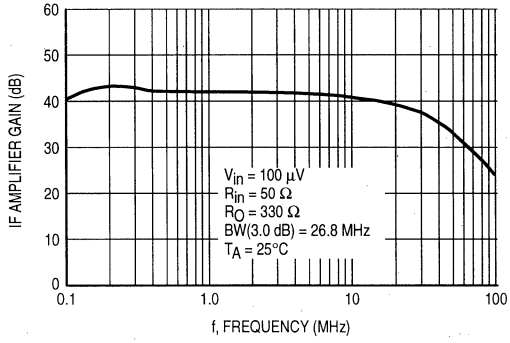
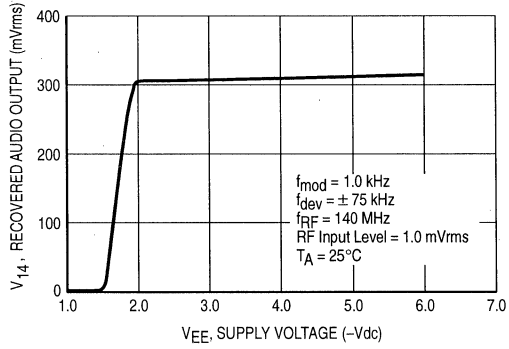


Figure 14. Recovered Audio Output Voltage versus Supply Voltage



Quadrature Detector

The quadrature detector is a doubly balanced four quadrant multiplier with an internal 5.0 pF quadrature capacitor to couple the IF signal to the external parallel RLC resonant circuit that provides the 90 degree phase shift and drives the quadrature detector. A single pin (Pin 13) provides for the external LC parallel resonant network and the internal connection to the quadrature detector.

The bandwidth of the detector allows for recovery of relatively high data rate modulation. The recovered signal is converted from differential to single ended through a push–pull NPN/PNP output stage. Variation in recovered audio output voltage with supply voltage is very small (see Figure 14). The output drive capability is approximately ± 9.0 μA for a frequency deviation of ± 75 kHz and 1.0 kHz modulating frequency (see Application Circuit).

Data Slicer

The data slicer input (Pin 15) is self centering around 1.1 V with clamping occurring at 1.1 ± 0.5 V_{be} Vdc. It is designed to square up the data signal. Figure 15 shows a detailed schematic of the data slicer.

The Voltage Regulator sets up 1.1 Vdc on the base of Q12, the Differential Input Amplifier. There is a potential of 1 V_{be} on the base–collector of transistor diode Q11 and 2 V_{be} on the base–collector of Q10. This sets up a 1.5 V_{be} (~ 1.1 Vdc) on the node between the 36 kΩ resistors which is connected to the base of Q12. The differential output of the data slicer Q12 and Q13 is converted to a single–ended output by the Driver Circuit. Additional circuitry, not shown in Figure 15, tends to keep the data slicer input centered at 1.1 Vdc as input signal levels vary.

The Input Diode Clamp Circuit provides the clamping at 1 V_{be} (0.75 Vdc) and 2 V_{be} (1.45 Vdc). Transistor diodes Q7 and Q8 are on, thus, providing a 2 V_{be} potential at the base of Q1. Also, the voltage regulator circuit provides a potential of 2 Vbe on the base of Q3 and 1 V_{be} on the emitter of Q3 and Q2. When the data slicer input (Pin 15) is pulled up, Q1 turns off; Q2 turns on, thereby clamping the input at 2 V_{be}. On the other hand, when Pin 15 is pulled down, Q1 turns on; Q2 turns off, thereby clamping the input at 1 V_{be}.

The recovered data signal from the quadrature detector is AC coupled to the data slicer via an input coupling capacitor. The size of this capacitor and the nature of the data signal determine how faithfully the data slicer shapes up the recovered signal. The time constant is short for large peak to peak voltage swings or when there is a change in DC level at the detector output. For small signal or for continuous bits of the same polarity which drift close to the threshold voltage, the time constant is longer. When centered there is no input current allowed, which is to say, that the input looks high in impedance.

Another unique feature of the data slicer is that it responds to various logic levels applied to the Data Slicer Hold Control pin (Pin 18). Figure 16 illustrates how the input and output currents under "no hold" condition relate to the input voltage. Figure 17 shows how the input current and input voltage relate for both the "no hold" and "hold" condition.

The hold control (Pin18) does three separate tasks:

1) With Pin 18 at 1 V_{be} or greater, the output is shut off (sets high). Q19 turns on which shunts the base drive from Q20, thereby turning the output off.

2) With Pin 18 at 2 V_{be} or greater, internal clamping diodes are open circuited and the comparator input is shut off and effectively open circuited. This is accomplished by turning off the current source to emitters of the input differential amplifier, thus, the input differential amplifier is shut off.

3) When the input is shut off, it allows the input capacitor to hold its charge during transmit to improve recovery at the beginning of the next receive period. When it is turned on, it allows for very fast charging of the input capacitor for quick recovery of new tuning or data average. The above features are very desirable in a TDD digital FM system.

Figure 15. Data Slicer Circuit

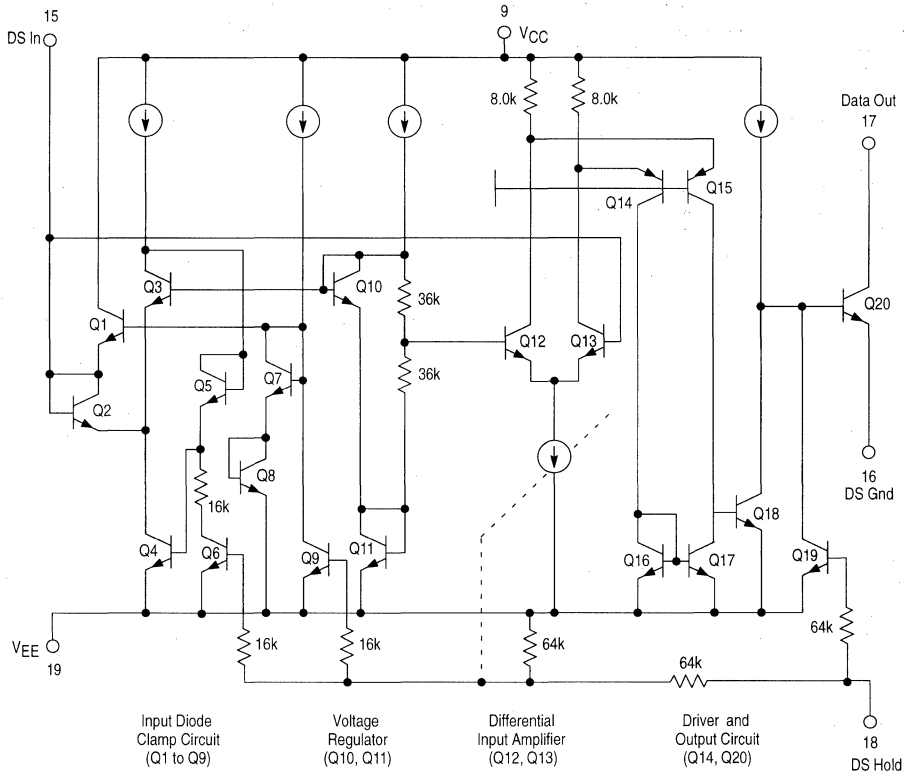


Figure 16. Data Slicer Input/Output Currents versus Input Voltage

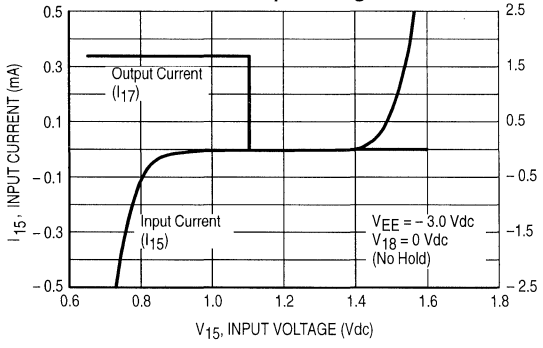


Figure 17. Data Slicer Input Current versus Input Voltage

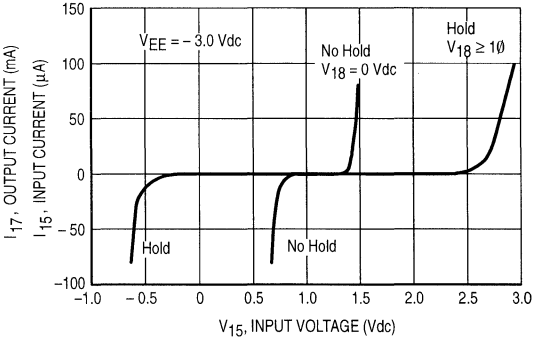
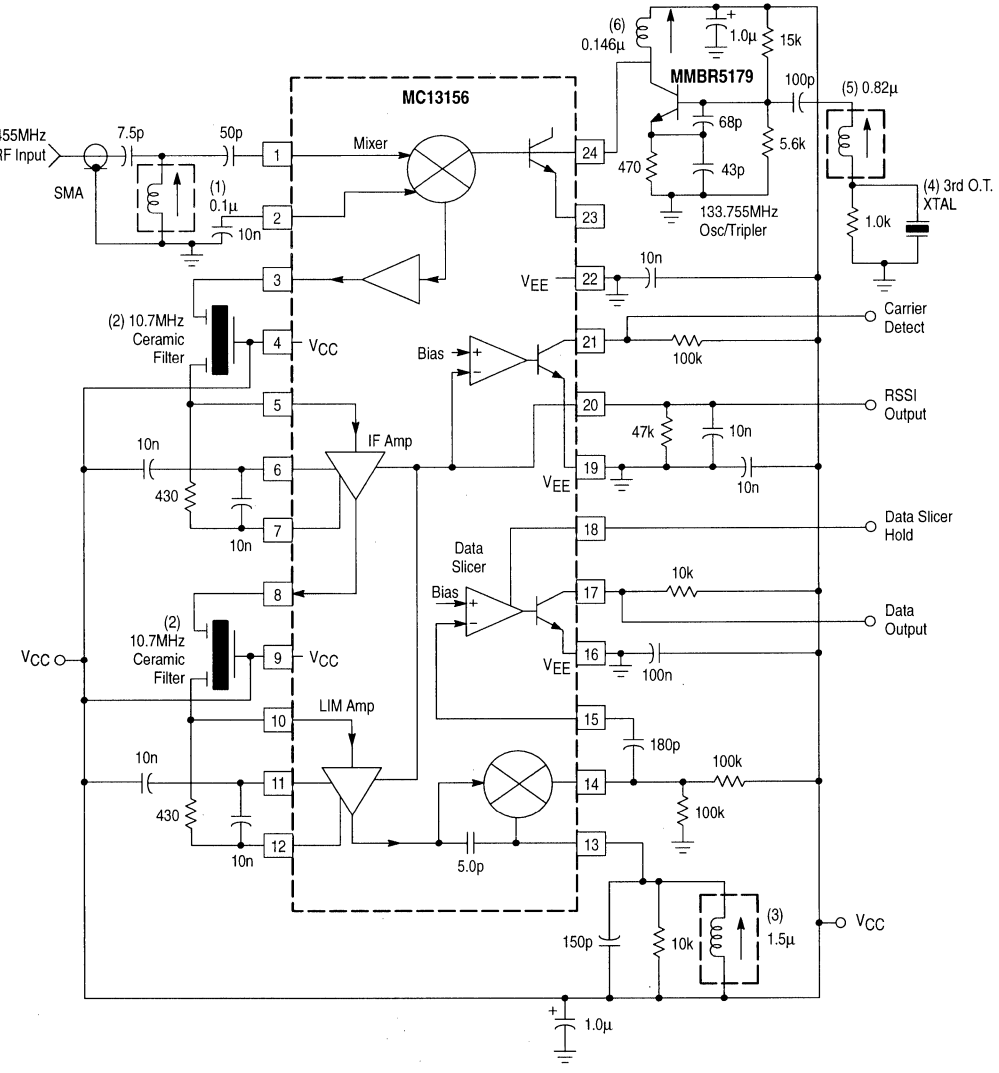


Figure 18. MC13156DW Application Circuit



NOTES: 1. 0.1 µH Variable Shielded Inductor: Coilcraft part # M1283–A or equivalent.
2. 10.7 MHz Ceramic Filter: Toko part # SK107M5–A0–10X or Murata Erie part # SFE10.7MHY–A.
3. 1.5 µH Variable Shielded Inductor: Toko part # 292SNS–T1373.
4. 3rd Overtone, Series Resonant, 25 PPM Crystal at 44.585 MHz.
5. 0.814 µH Variable Shielded Inductor: Coilcraft part # 143–18J12S.
6. 0.146 µH Variable Inductor: Coilcraft part # 146–04J08.

Figure 19. MC13156DW Circuit Side Component Placement

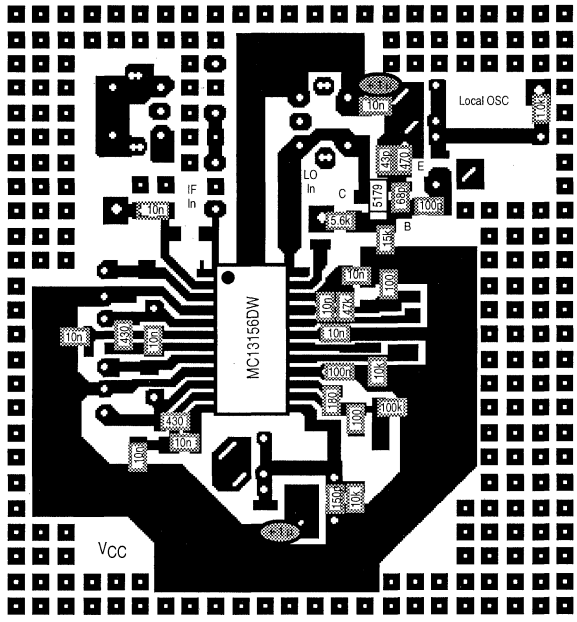
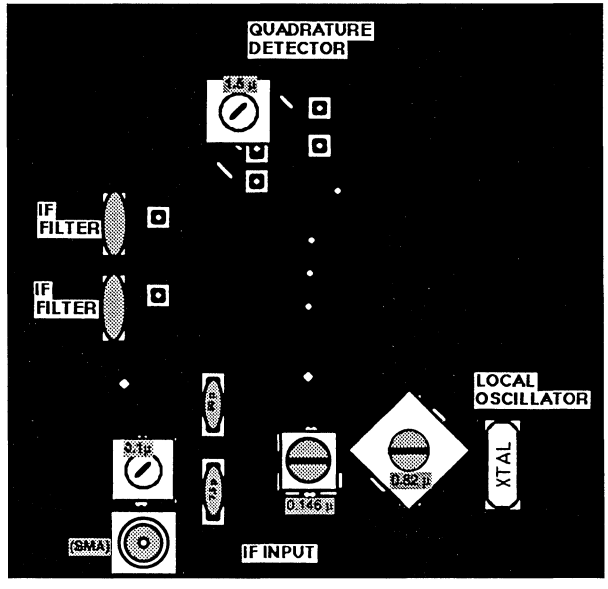


Figure 20. MC13156DW Ground Side Component Placement



APPLICATIONS INFORMATION

Component Selection

The evaluation PC board is designed to accommodate specific components, while also being versatile enough to use components from various manufacturers and coil types. Figures 19 and 20 show the placement for the components specified in the application circuit (Figure 18). The applications circuit schematic specifies particular components that were used to achieve the results shown in the typical curves and tables but equivalent components should give similar results.

Input Matching Networks/Components

The input matching circuit shown in the application circuit schematic is passive high pass network which offers effective image rejection when the local oscillator is below the RF input frequency. Silver mica capacitors are used for their high Q and tight tolerance. The PC board is not dedicated to any particular input matching network topology; space is provided for the designer to breadboard as desired.

Alternate matching networks using 4:1 surface mount transformers or BALUNs provide satisfactory performance. The 12 db SINAD sensitivity using the above matching networks is typically –100 dBm for f_{mod} = 1.0 kHz and f_{dev} = ±75 kHz at f_{IN} = 144.45 MHz and f_{OSC} = 133.75 MHz (see Figure 26).

It is desirable to use a SAW filter before the mixer to provide additional selectivity and adjacent channel rejection and improved sensitivity. The SAW filter should be designed to interface with the mixer input impedance of approximately 1.0 kΩ. Table 1 displays the series equivalent single–ended mixer input impedance.

Local Oscillators

VHF Applications – The local oscillator circuit shown in the application schematic utilizes a third overtone crystal and an RF transistor. Selecting a transistor having good phase noise performance is important; a mandatory criteria is for the device to have good linearity of beta over several decades of collector current. In other words, if the low current beta is suppressed, it will not offer good 1/f noise performance. A third overtone series resonant crystal having at least 25 ppm tolerance over the operating temperature is recommended. The local oscillator is an impedance inversion third overtone Colpitts network and harmonic generator. In this circuit a 560 to 1.0 kΩ resistor shunts the crystal to ensure that it operates in its overtone mode; thus, a blocking capacitor is needed to eliminate the dc path to ground. The resulting parallel LC network should "free–run" near the crystal frequency if a short to ground is placed across the crystal. To provide sufficient output loading at the collector, a high Q variable inductor is used that is tuned to self resonate at the 3rd harmonic of the overtone crystal frequency.

The on–chip grounded collector transistor may be used for HF and VHF local oscillator with higher order overtone crystals. Figure 21 shows a 5th overtone oscillator at 93.3 MHz and Figure 22 shows a 7th overtone oscillator at 148.3 MHz. Both circuits use a Butler overtone oscillator configuration. The amplifier is an emitter follower. The crystal is driven from the emitter and is coupled to the high impedance base through a capacitive tap network. Operation at the desired overtone frequency is ensured by the parallel resonant circuit formed by the variable inductor and the tap capacitors and parasitic capacitances of the on–chip transistor and PC board. The variable inductor specified in the schematic could be replaced with a high tolerance, high Q ceramic or air wound surface mount component if the other components have good tolerances. A variable inductor provides an adjustment for gain and frequency of the resonant tank ensuring lock up and start–up of the crystal oscillator. The overtone crystal is chosen with ESR of typically 80 Ω and 120 Ω maximum; if the resistive loss in the crystal is too high, the performance of the oscillator may be impacted by lower gain margins.

Table 1. Mixer Input Impedance Data
(Single–ended configuration, V_{CC}= 3.0 Vdc, local oscillator drive = 100 mVrms)

Frequency (MHz)	Series Equivalent Complex Impedance (R + jX) (Ω)	Parallel Resistance Rp (Ω)	Parallel Capacitance Cp (pF)
90	190 – j380	950	4.7
100	160 – j360	970	4.4
110	130 – j340	1020	4.2
120	110 – j320	1040	4.2
130	97 – j300	1030	4.0
140	82 – j280	1040	4.0
150	71 – j270	1100	4.0
160	59 – j260	1200	3.9
170	52 – j240	1160	3.9
180	44 – j230	1250	3.8
190	38 – j220	1300	3.8

A series LC network to ground (which is V_{CC}) is comprised of the inductance of the base lead of the on–chip transistor and PC board traces and tap capacitors. Parasitic oscillations often occur in the 200 to 800 MHz range. A small resistor is placed in series with the base (Pin 24) to cancel the negative resistance associated with this undesired mode of oscillation. Since the base input impedance is so large a small resistor in the range of 27 to 68 Ω has very little effect on the desired Butler mode of oscillation.

The crystal parallel capacitance, C_O, provides a feedback path that is low enough in reactance at frequencies of 5th overtone or higher to cause trouble. C_O has little effect near resonance because of the low impedance of the crystal motional arm (R_m–L_m–C_m). As the tunable inductor which forms the resonant tank with the tap capacitors is tuned off the crystal resonant frequency, it may be difficult to tell if the oscillation is under crystal control. Frequency jumps may occur as the inductor is tuned. In order to eliminate this behavior an inductor (L_O) is placed in parallel with the crystal. L_O is chosen to resonant with the crystal parallel capacitance (C_O) at the desired operation frequency. The inductor provides a feedback path at frequencies well below resonance; however, the parallel tank network of the tap capacitors and tunable inductor prevent oscillation at these frequencies.

UHF Application

Figure 23 shows a 318.5 to 320 MHz receiver which drives the mixer with an external varactor controlled (307.8 to 309.3 MHz) LC oscillator using an MPS901 (RF low power transistor in a TO–92 plastic package; also MMBR901 is available in a SOT–23 surface mount package). With the 50 kΩ 10 turn potentiometer this oscillator is tunable over a range of approximately 1.5 MHz. The MMBV909L is a low voltage varactor suitable for UHF applications; it is a dual back–to–back varactor in a SOT–23 package. The input matching network uses a 1:4 impedance matching transformer (Recommended sources are Mini–Circuits and Coilcraft).

Using the same IF ceramic filters and quadrature detector circuit as specified in the applications circuit in Figure 18, the 12 dB SINAD performance is – 95 dBm for a f_{mod} = 1.0 kHz sinusoidal waveform and f_{dev} ± 40 kHz.

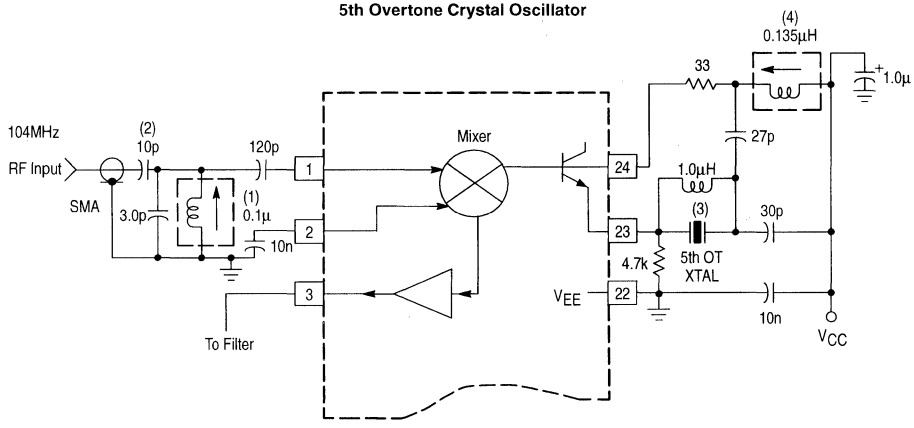
This circuit is breadboarded using the evaluation PC board shown in Figures 33 and 34. The RF ground is V_{CC} and path lengths are minimized. High quality surface mount components were used except where specified. The absolute values of the components used will vary with layout placement and component parasitics.

RSSI Response

Figure 27 shows the full RSSI response in the application circuit. The 10.7 MHz, 110 kHz wide bandpass ceramic filters (recommended sources are TOKO part # SK107M5–AO–10X or Murata Erie SFE10.7MHY–A) provide the correct bandpass insertion loss to linearize the curve between the limiter and IF portions of RSSI. Figure 26 shows that limiting occurs at an input of –100 dBm. As shown in Figure 27, the RSSI output linear from –100 dBm to – 30 dBm.

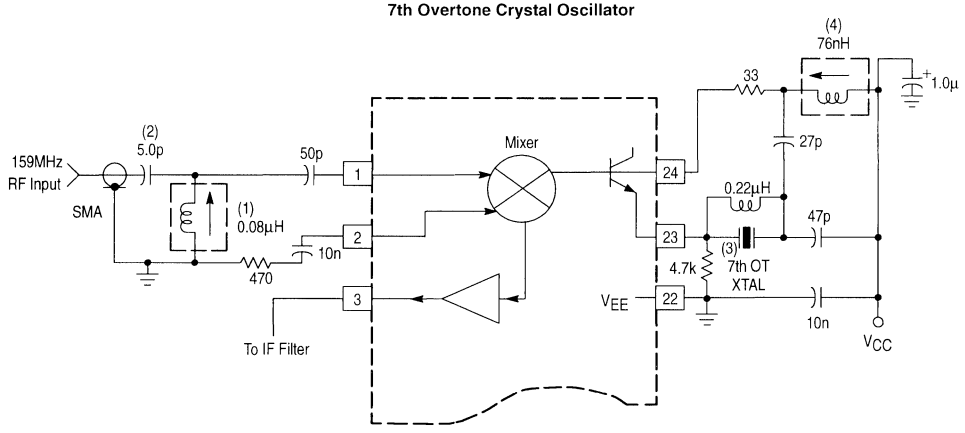
The RSSI rise and fall times for various RF input signal levels and R20 values are measured at Pin 20 without 10 nF filter capacitor. A 10 kHz square wave pulses the RF input signal on and off. Figure 28 shows that the rise and fall times are short enough to recover greater than 10 kHz ASK data; with a wider IF bandpass filters data rates up to 50 kHz may be achieved. The circuit used is the application circuit in Figure 18 with no RSSI output filter capacitor.

Figure 21. MC13156DW Application Circuit
f_{RF} = 104 MHz; f_{LO} = 93.30 MHz
5th Overtone Crystal Oscillator



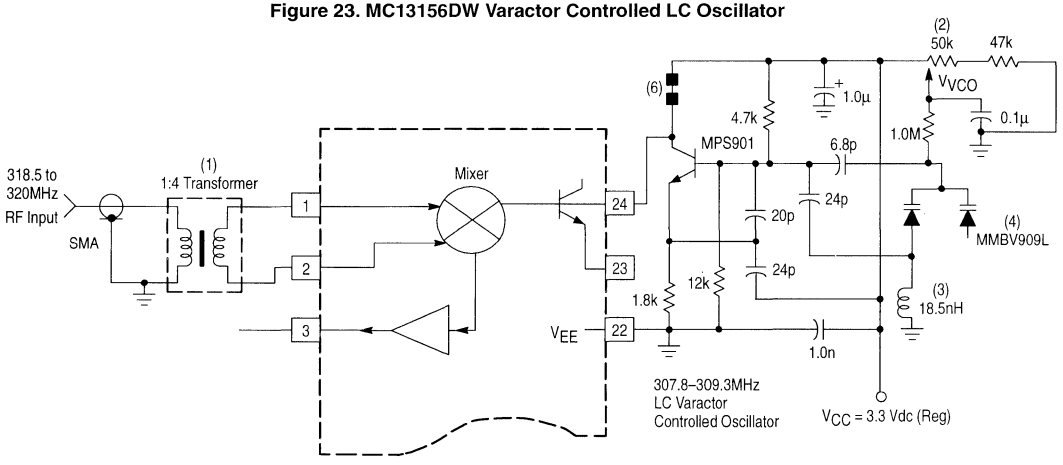
NOTES: 1. 0.1 µH Variable Shielded Inductor: Coilcraft part # M1283–A or equivalent.
2. Capacitors are Silver Mica.
3. 5th Overtone, Series Resonant, 25 PPM Crystal at 93.300 MHz.
4. 0.135 µH Variable Shielded Inductor: Coilcraft part # 146–05J08S or equivalent.

Figure 22. MC13156DW Application Circuit
f_{RF} = 159 MHz; f_{LO} = 148.30 MHz
7th Overtone Crystal Oscillator



NOTES: 1. 0.08 µH Variable Shielded Inductor: Toko part # 292SNS–T1365Z or equivalent.
2. Capacitors are Silver Mica.
3. 7th Overtone, Series Resonant, 25 PPM Crystal at 148.300 MHz.
4. 76 nH Variable Shielded Inductor: Coilcraft part # 150–03J08S or equivalent.

Figure 23. MC13156DW Varactor Controlled LC Oscillator



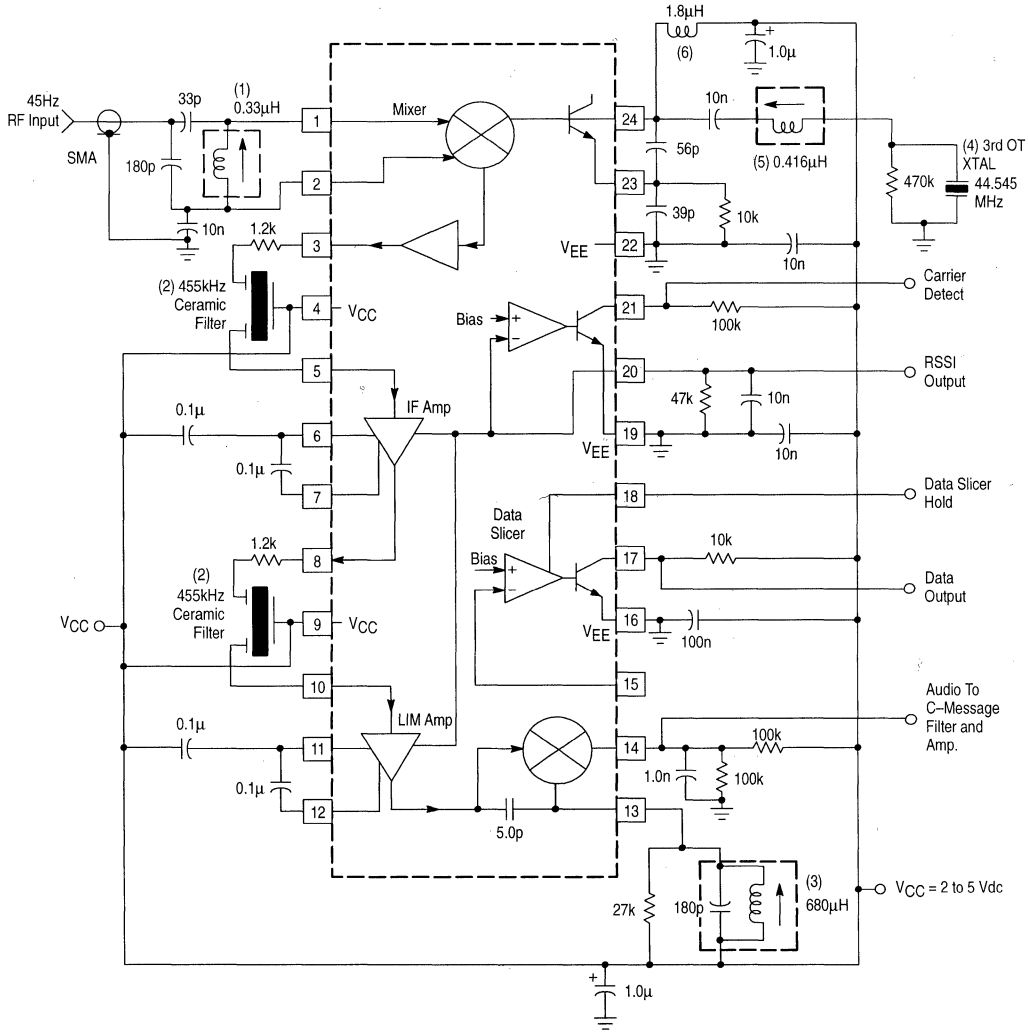
NOTES: 1. 1:4 Impedance Transformer: Mini–Circuits.
2. 50 k Potentiometer, 10 turns.
3. Spring Coil; Coilcraft A05T.
4. Dual Varactor in SOT–23 Package.
5. All other components are surface mount components.
6. Ferrite beads through loop of 24 AWG wire.

45 MHz Narrowband Receiver

The above application examples utilize a 10.7 MHz IF. In this section a narrowband receiver with a 455 kHz IF will be described. Figure 24 shows a full schematic of a 45 MHz receiver that uses a 3rd overtone crystal with the on–chip oscillator transistor. The oscillator configuration is similar to the one used in Figure 18; it is called an impedance inversion Colpitts. A 44.545 MHz 3rd overtone, series resonant crystal is used to achieve an IF frequency at 455 kHz. The ceramic IF filters selected are Murata Erie part # SFG455A3. 1.2 kΩ chip resistors are used in series with the filters to achieve the terminating resistance of 1.4 kΩ to the filter. The IF decoupling is very important; 0.1 μF chip capacitors are used at Pins 6, 7, 11, and 12. The quadrature detector tank circuit uses a 455 kHz quadrature tank from Toko.

The 12 dB SINAD performance is –109 dBm for a f_{mod} = 1.0 kHz and a f_{dev} = ± 4.0 kHz. The RSSI dynamic range is approximately 80 dB of linear range (see Figure 25).

Figure 24. MC13156DW Application Circuit at 45 MHz



NOTES: 1. 0.33 μH Variable Shielded Inductor: Coilcraft part # 7M3–331 or equivalent.
2. 455 kHz Ceramic Filter: Murata Erie part # SFG455A3.
3. 455 kHz Quadrature Tank: Toko part # 7MC8128Z.
4. 3rd Overtone, Series Resonant, 25 PPM Crystal at 44.540 MHz.
5. 0.416 μH Variable Shielded Inductor: Coilcraft part # 143–10J12S.
6. 1.8 μH Molded Inductor.

Figure 25. RSSI Output Voltage versus Input Signal Level

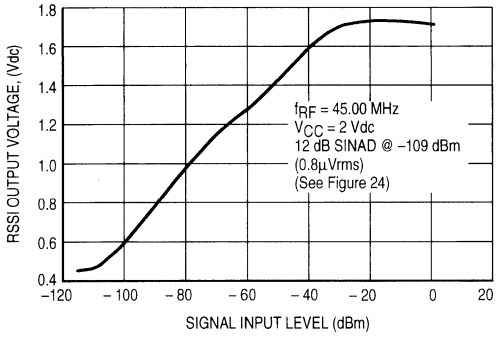


Figure 26. S + N/N versus RF Input Signal Level

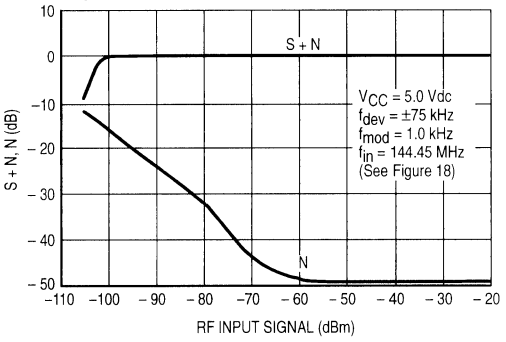


Figure 27. RSSI Output Voltage versus Input Signal Level

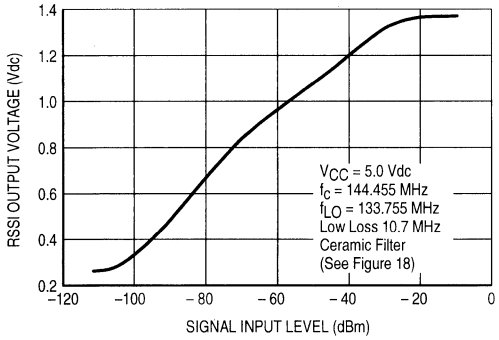
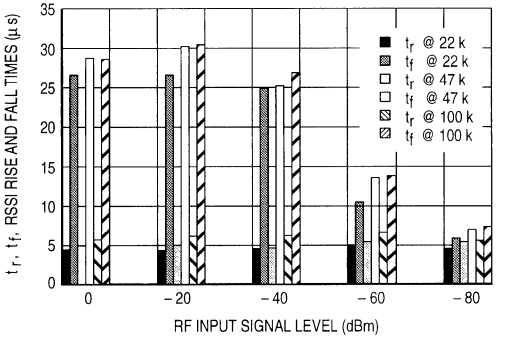


Figure 28. RSSI Output Rise and Fall Times versus RF Input Signal Level



Receiver Design Considerations

The curves of signal levels at various portions of the application receiver with respect to RF input level are shown in Figure 29. This information helps determine the network topology and gain blocks required ahead of the MC13156 to achieve the desired sensitivity and dynamic range of the receiver system. In the application circuit the input third order intercept (IP3) performance of the system is approximately – 25 dBm (see Figure 30).

Figure 29. Signal Levels versus RF Input Signal Level

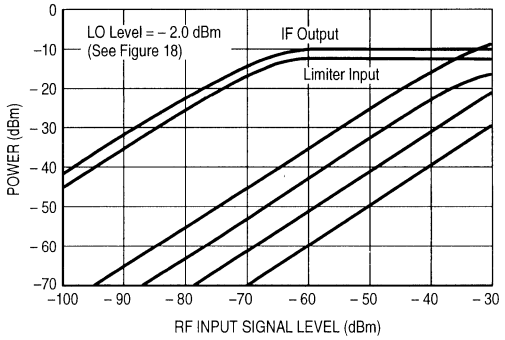
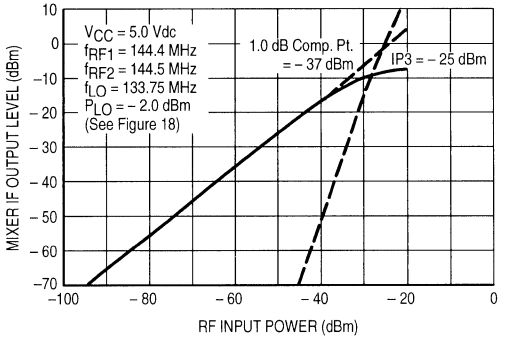


Figure 30. 1.0 dB Compression Pt. and Input Third Order Intercept Pt. versus Input Power



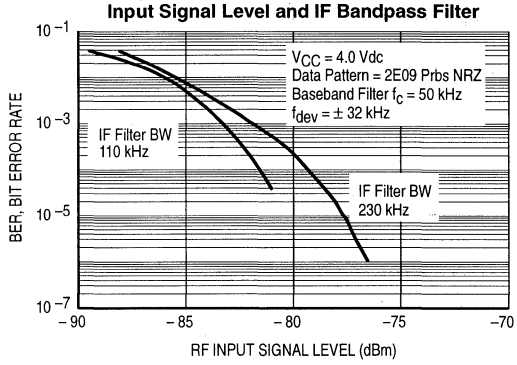
Description

The test setup shown in Figure 31 is configured so that the function generator supplies a 100 kHz clock source to the bit error rate tester. This device generates and receives a repeating data pattern and drives a 5 pole baseband data filter. The filter effectively reduces harmonic content of the baseband data which is used to modulate the RF generator which is running at 144.45 MHz. Following processing of the signal by the receiver (MC13156), the recovered baseband sinewave (data) is AC coupled to the data slicer. The data slicer is essentially an auto–threshold comparator which tracks the zero crossing of the incoming sinewave and provides logic level data at its ouput. Data errors associated with the recovered data are collected by the bit error rate receiver and displayed.

Bit error rate versus RF signal input level and IF filter bandwidth are shown in Figure 32. The bit error rate data was taken under the following test conditions:

- Data rate = 100 kbps
- Filter cutoff frequency set to 39% of the data rate or 39 kHz.
- Filter type is a 5 pole equal–ripple with 0.5° phase error.
- V_{CC} = 4.0 Vdc
- Frequency deviation = ± 32 kHz.

Figure 31. Bit Error Rate versus RF Input Signal Level and IF Bandpass Filter



Evaluation PC Board

The evaluation PCB is very versatile and is intended to be used across the entire useful frequency range of this device. The center section of the board provides an area for attaching all SMT components to the circuit side and radial leaded components to the component ground side (see Figures 33 and 34). Additionally, the peripheral area surrounding the RF core provides pads to add supporting and interface circuitry as a particular application dictates.

Figure 32. Bit Error Rate Test Setup

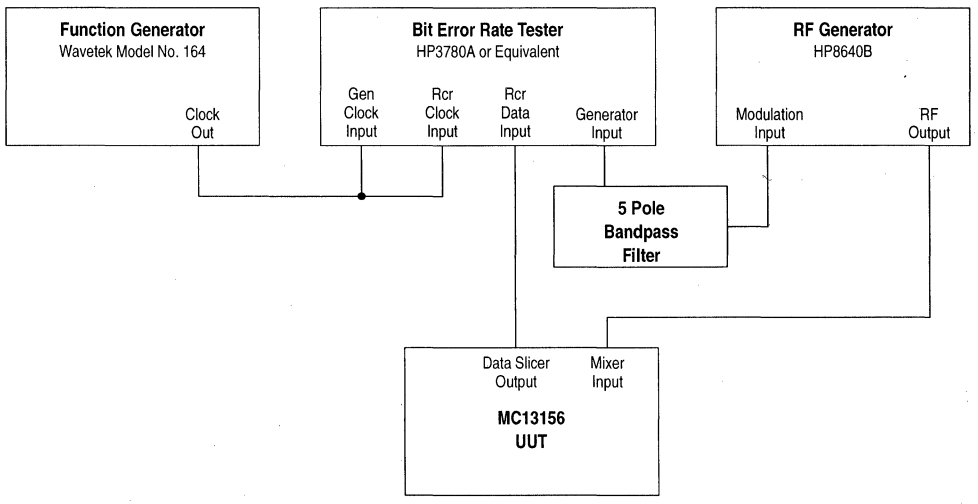


Figure 33. Circuit Side View

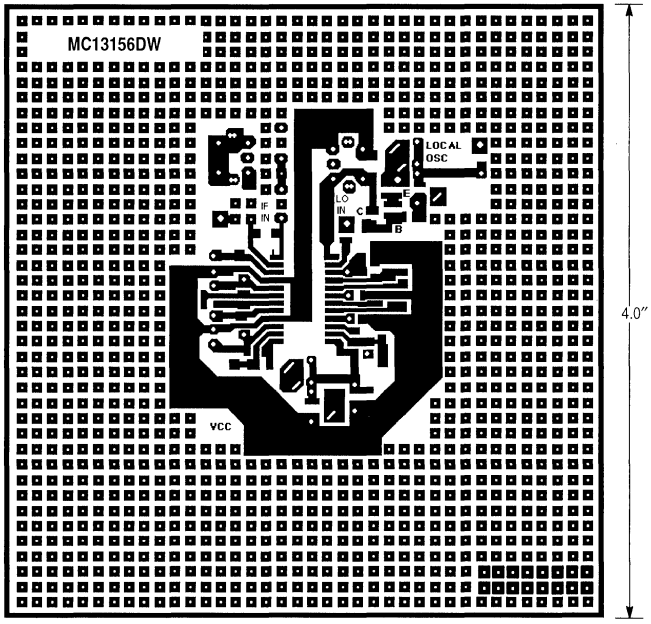
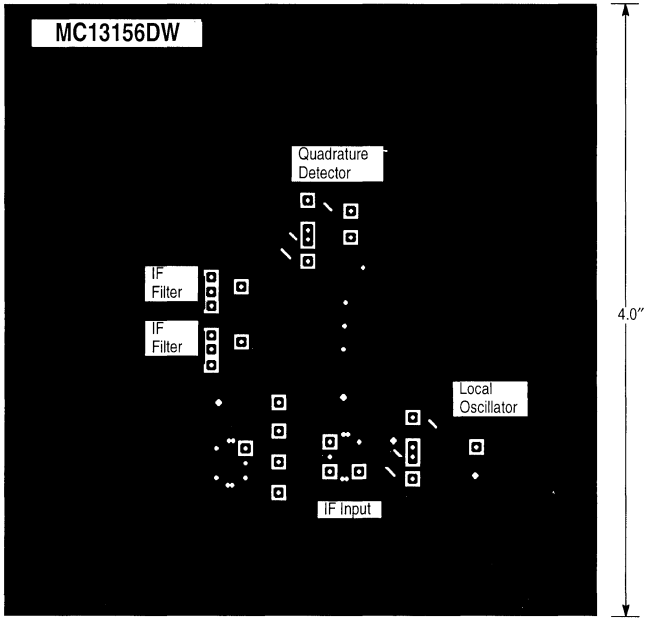


Figure 34. Ground Side View



MOTOROLA

MC13158

Advance Information

Wideband FM IF Subsystem

WIDEBAND FM IF SUBSYSTEM FOR DECT AND DIGITAL APPLICATIONS

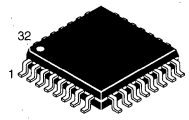
SEMICONDUCTOR TECHNICAL DATA

2

The MC13158 is a wideband IF subsystem that is designed for high performance data and analog applications. Excellent high frequency performance is achieved, with low cost, through the use of Motorola's MOSAIC 1.5™ RF bipolar process. The MC13158 has an on–board grounded collector VCO transistor that may be used with a fundamental or overtone crystal in single channel operation or with a PLL in multi–channel operation. The mixer is useful to 500 MHz and may be used in a balanced differential or single ended configuration. The IF amplifier is split to accommodate two low cost cascaded filters. RSSI output is derived by summing the output of both IF sections. A precision data shaper has an Off function to shut the output off to save current. An enable control is provided to power down the IC for power management in battery operated applications.

Applications include DECT, wideband wireless data links for personal and portable laptop computers and other battery operated radio systems which utilize GFSK, FSK or FM modulation.

- Designed for DECT Applications
- 1.8 to 6.0 Vdc Operating Voltage
- Low Power Consumption in Active and Standby Mode
- Greater than 600 kHz Detector Bandwidth
- Data Slicer with Special Off Function
- Enable Function for Power Down of Battery Operated Systems
- RSSI Dynamic Range of 80 dB Minimum
- Low External Component Count

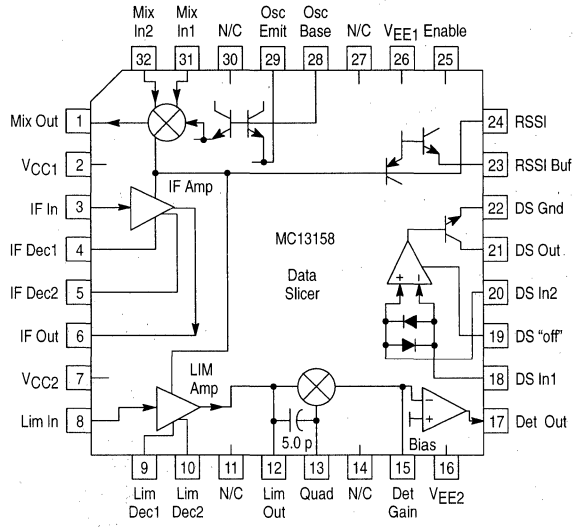


FTB SUFFIX
PLASTIC PACKAGE
CASE 873
(Thin QFP)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC13158FTB	T_A = – 40 to +85°C	TQFP–32

Representative Block Diagram



This device contains 234 active transistors.

Rev 1

MAXIMUM RATINGS

Rating	Pin	Symbol	Value	Unit
Power Supply Voltage	16, 26	$V_{S(max)}$	6.5	Vdc
Junction Temperature		T_{JMAX}	+150	°C
Storage Temperature Range		T_{stg}	−65 to +150	°C

NOTE: 1. Devices should not be operated at or outside these values. The "Recommended Operating Conditions" provide for actual device operation.

RECOMMENDED OPERATING CONDITIONS ($V_{CC} = V_2 = V_7$; $V_{EE} = V_{16} = V_{22} = V_{26}$; $V_S = V_{CC} - V_{EE}$)

Rating	Pin	Symbol	Value	Unit
Power Supply Voltage T_A = 25°C −40°C ≤ T_A ≤ 85°C	2, 7 16, 26	V_S	2.0 to 6.0	Vdc
Input Frequency	31, 32	F_{in}	10 to 500	MHz
Ambient Temperature Range		T_A	−40 to +85	°C
Input Signal Level	31, 32	V_{in}	200	mVrms

DC ELECTRICAL CHARACTERISTICS (T_A = 25°C; V_S = 3.0 Vdc; No Input Signal; See Figure 1.)

Characteristic	Condition	Pin	Symbol	Min	Typ	Max	Unit
Total Drain Current	V_S = 2.0 Vdc V_S = 3.0 Vdc V_S = 6.0 Vdc See Figure 2	16, 26	I_{TOTAL}	2.5 3.5 3.5	5.5 5.7 6.0	8.5 8.5 9.5	mA
DATA SLICER (Input Voltage Referenced to V_{EE}; V_S = 3.0 Vdc; No Input Signal)							
Output Current; V_{18} LO; Data Slicer Enabled (DS "on")	$V_{19} = V_{EE}$ $V_{18} < V_{20}$ $V_{20} = V_S/2$ See Figure 3	21	I_{21}	2.0	5.9	–	mA
Output Current; V_{18} HI; Data Slicer Enabled (DS "on")	$V_{19} = V_{EE}$ $V_{18} > V_{20}$ $V_{20} = V_S/2$ See Figure 4	21	I_{21}	–	0.1	1.0	µA
Output Current; Data Slicer Disabled (DS "off")	$V_{19} = V_{CC}$ $V_{20} = V_S/2$	21	I_{21}	–	0.1	1.0	µA

AC ELECTRICAL CHARACTERISTICS (T_A = 25°C; V_S = 3.0 Vdc; f_{RF} = 110.7 MHz; f_{LO} = 100 MHz; See Figure 1.)

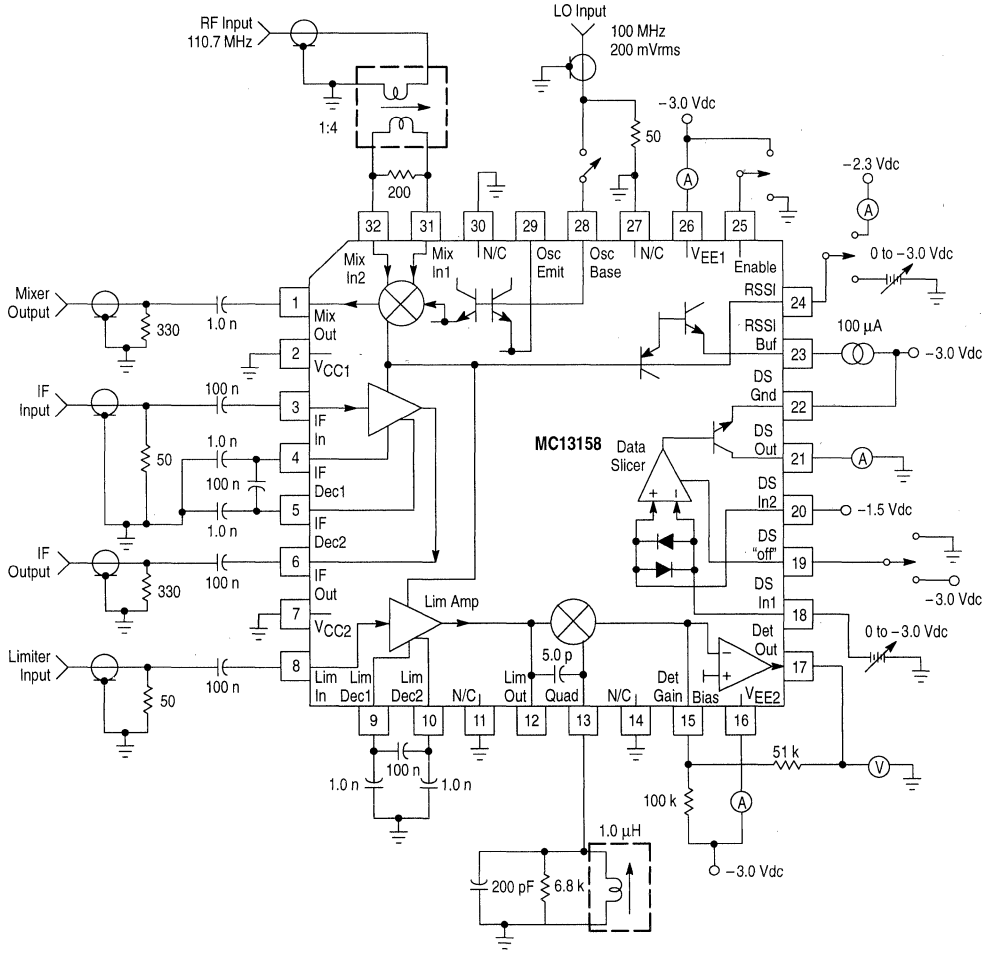
Characteristic	Condition	Pin	Symbol	Min	Typ	Max	Unit
MIXER							
Mixer Conversion Gain	V_{in} = 1.0 mVrms See Figure 5	31, 32, 1	–	–	22	–	dB
Noise Figure	Input Matched	31, 32, 1	NF	–	14	–	dB
Mixer Input Impedance	Single–Ended See Figure 15	31, 32	Rp Cp	– –	865 1.6	– –	Ω pF
Mixer Output Impedance		1	–	–	330	–	Ω

AC ELECTRICAL CHARACTERISTICS (continued) (T_A = 25°C; V_S = 3.0 Vdc; f_{RF} = 110.7 MHz; f_{LO} = 100 MHz; See Figure 1.)

Characteristic	Condition	Pin	Symbol	Min	Typ	Max	Unit
IF AMPLIFIER SECTION							
IF RSSI Slope	See Figure 8	23	–	0.15	0.3	0.4	µA/dB
IF Gain	f = 10.7 MHz See Figure 7	3, 6	–	–	36	–	dB
Input Impedance		3	–	–	330	–	Ω
Output Impedance		6	–	–	330	–	Ω
LIMITING AMPLIFIER SECTION							
Limiter RSSI Slope	See Figure 9	23	–	0.15	0.3	0.4	µA/dB
Limiter Gain	f = 10.7 MHz	8, 12	–	–	70	–	dB
Input Impedance		8	–	–	330	–	Ω

2

Figure 1. Test Circuit



Typical Performance Over Temperature

(per Figure 1)

Figure 2. Total Supply Current versus Ambient Temperature, Supply Voltage

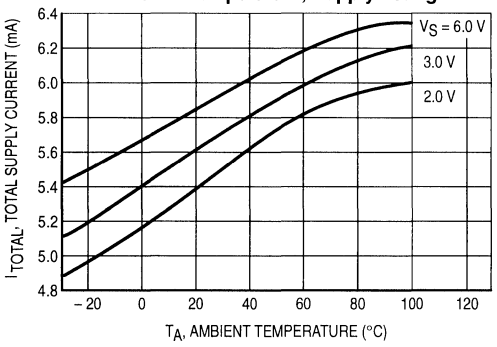


Figure 3. Data Slicer On Output Current versus Ambient Temperature

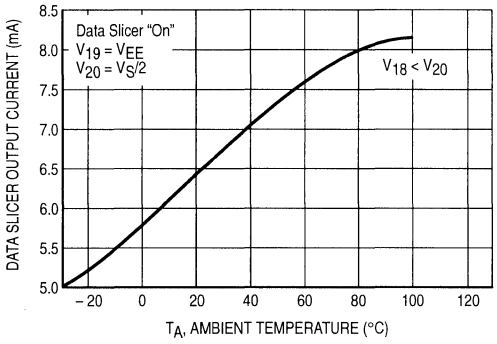


Figure 4. Data Slicer On Output Current versus Ambient Temperature

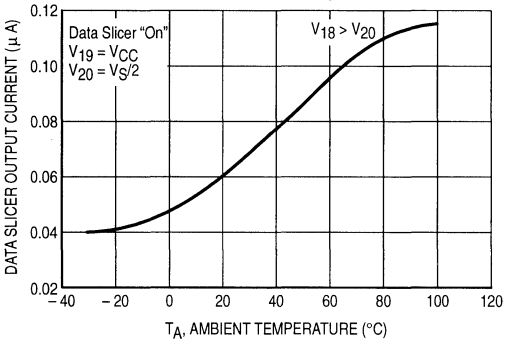


Figure 5. Normalized Mixer Gain versus Ambient Temperature

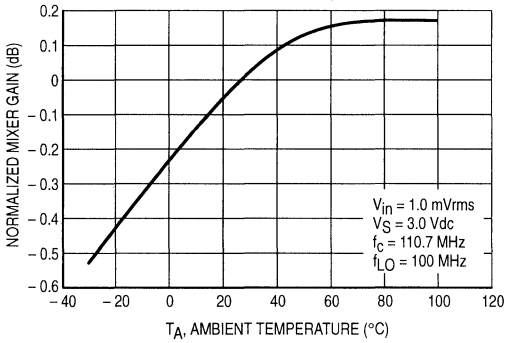


Figure 6. Mixer RSSI Output Current versus Ambient Temperature, Mixer Input Level

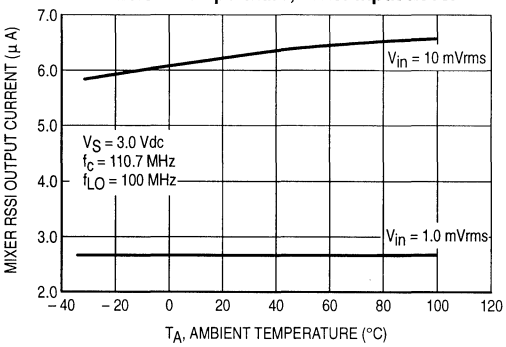
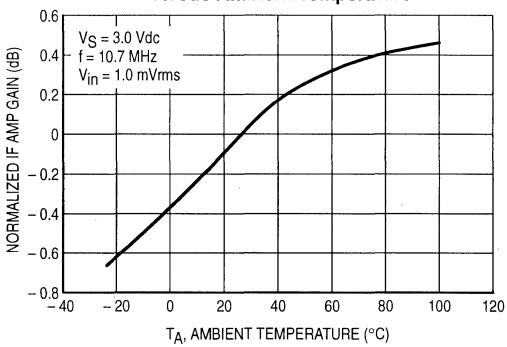


Figure 7. Normalized IF Amp Gain versus Ambient Temperature



Typical Performance Over Temperature

(per Figure 1)

Figure 8. IF Amp RSSI Output Current versus Ambient Temperature, IF Input Level

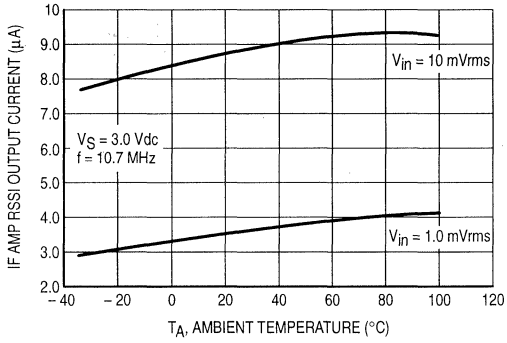


Figure 9. Limiter Amp RSSI Output Current versus Ambient Temperature, Input Signal Level

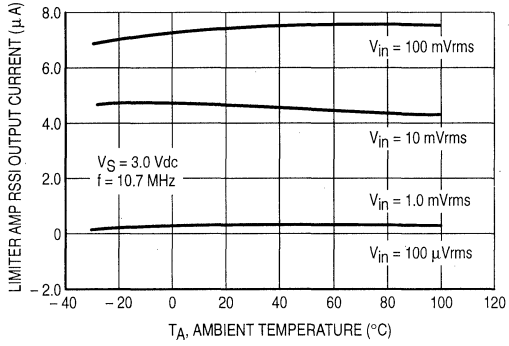


Figure 10. Total RSSI Output Current versus Ambient Temperature (No Signal)

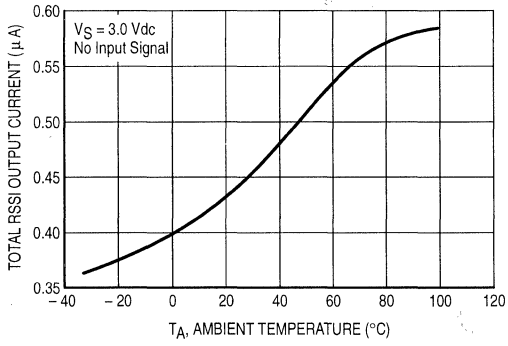
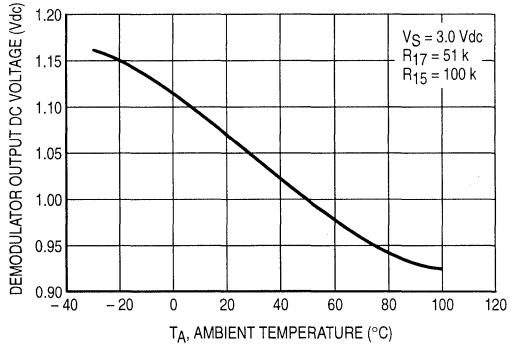


Figure 11. Demodulator DC Voltage versus Ambient Temperature



SYSTEM LEVEL AC ELECTRICAL CHARACTERISTICS (T_A = 25°C; V_S = 3.0 Vdc; f_{RF} = 112 MHz; f_{LO} = 122.7 MHz)

Characteristic	Condition	Notes	Symbol	Typ	Unit
12 dB SINAD Sensitivity: Narrowband Application	f_{RF} = 112 MHz f_{mod} = 1.0 kHz f_{dev} = ±125 kHz SINAD Curve	1	–		dBm
Without Preamp	Figure 25			−101	
With Preamp	Figure 26			−113	
Third Order Intercept Point	f_{RF1} = 112 MHz f_{RF2} = 112.1 MHz	2	IIP3	−32	dBm
1.0 dB Comp. Point	V_S = 3.5 Vdc Figure 28		1.0 dB C.Pt.	−39	

NOTES: 1. Test Circuit & Test Set per Figure 24.
2. Test Circuit & Test Set per Figure 27.

CIRCUIT DESCRIPTION

General

The MC13158 is a low power single conversion wideband FM receiver incorporating a split IF. This device is designated for use as the backend in digital FM systems such as Digital European Cordless Telephone (DECT) and wideband data links with data rates up to 2.0 Mbps. It contains a mixer, oscillator, Received Signal Strength Indicator (RSSI), IF amplifier, limiting IF, quadrature detector, power down or enable function, and a data slicer with output off function. Further details are covered in the Pin Function Description which shows the equivalent internal circuit and external circuit requirements.

Current Regulation/Enable

Temperature compensating voltage independent current regulators which are controlled by the enable pin (Pin 25) where "low" powers up and "high" powers down the entire circuit.

Mixer

The mixer is a double–balanced four quadrant multiplier and is designed to work up to 500 MHz. It can be used in differential or in single ended mode by connecting the other input to the positive supply rail. The linear gain of the mixer is approximately 22 dB at 100 mVrms LO drive level. The mixer gain and noise figure have been emphasized at the expense of intermodulation performance. RSSI measurements are added in the mixer to extend the range to higher signal levels. The single–ended parallel equivalent input impedance of the mixer is Rp ~ 1.0 kΩ and Cp ~ 2.0 pF. The buffered output of the mixer is internally loaded resulting in an output impedance of 330 Ω.

Local Oscillator

The on–chip transistor operates with crystal and LC resonant elements up to 220 MHz. Series resonant, overtone crystals are used to achieve excellent local oscillator stability. Third overtone crystals are used through about 65 to 70 MHz. Operation from 70 MHz up to 180 MHz is feasible using the on–chip transistor with a 5th or 7th overtone crystal. To enhance operation using an overtone crystal, the internal transistor bias is increased by adding an external resistor from Pin 29 to V_{EE}; however, with an external resistor the oscillator stays on during power down. Typically, –10 dBm of local oscillator drive is needed to adequately drive the mixer. With an external oscillator source, the IC can be operated up to 500 MHz.

RSSI

The received signal strength indicator (RSSI) output is a current proportional to the log of the received signal amplitude. The RSSI current output is derived by summing the currents from the mixer, IF and limiting amplifier stages. An increase in RSSI dynamic range, particularly at higher input signal levels is achieved. The RSSI circuit is designed to provide typically 85 dB of dynamic range with temperature compensation.

Linearity of the RSSI is optimized by using external ceramic bandpass filters which have an insertion loss of 4.0 dB and 330 Ω source and load impedance. For higher data rates used in DECT and related applications, LC bandpass filtering is necessary to acquire the desired bandpass response; however, the RSSI linearity will require the same insertion loss.

RSSI Buffer

The RSSI output current creates a voltage across an external resistor. A unity voltage–gain amplifier is used to buffer this voltage. The output of this buffer has an active pull–up but no pull–down, so it can also be used as a peak detector. The negative slew rate is determined by external capacitance and resistance to the negative supply.

IF Amplifier

The first IF amplifier section is composed of three differential stages with the second and third stages contributing to the RSSI. This section has internal DC feedback and external input decoupling for improved symmetry and stability. The total gain of the IF amplifier block is approximately 40 dB at 10.7 MHz.

The fixed internal input impedance is 330 Ω. When using ceramic filters requiring source and loss impedances of 330 Ω, no external matching is necessary. Overall RSSI linearity is dependent on having total midband attenuation of 10 dB (4.0 dB insertion loss plus 6.0 dB impedance matching loss) for the filter. The output of the IF amplifier is buffered and the impedance is 330 Ω.

Limiter

The limiter section is similar to the IF amplifier section except that five differential stages are used. The fixed internal input impedance is 330 Ω. The total gain of the limiting amplifier section is approximately 70 dB. This IF limiting amplifier section internally drives the quadrature detector section and it is also brought out on Pin 12.

Quadrature Detector

The quadrature detector is a doubly balanced four quadrant multiplier with an internal 5.0 pF quadrature capacitor between Pins 12 and 13. An external capacitor may be added between these pins to increase the IF signal to the external parallel RLC resonant circuit that provides the 90 degree phase shift and drives the quadrature detector. A single pin (Pin 13) provides for the external LC parallel resonant network and the internal connection to the quadrature detector.

Internal low pass filter capacitors have been selected to control the bandwidth of the detector. The recovered signal is brought out by the inverting amplifier buffer. An external feedback resistor from the output (Pin 17) to the input of the inverting amplifier (Pin 15) controls the output amplitude; it is combined with another external resistor from the input to the negative supply (Pin 16) to set the output dc level. For a resistor ratio of 1, the DC level at the detector output is 2.0 V_{BE} (see Figure 12). A small capacitor C_{17} across the first resistor (from Pin 17 to 15) can be used to reduce the bandwidth.

Data Slicer

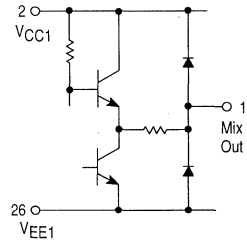
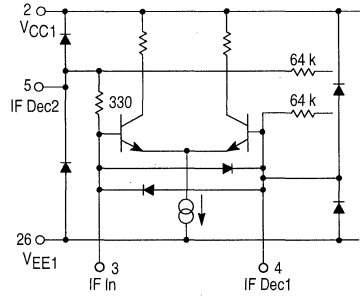
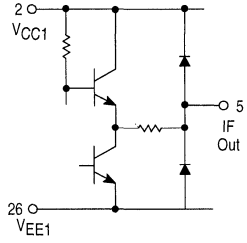
The data slicer is a comparator that is designed to square up the data signal. Across the data slicer inputs (Pins 18 and 20) are back to back diodes.

The recovered data signal from the quadrature detector can be DC coupled to the data slicer DS IN1 (Pin 18). In the application circuit shown in Figure 1 it will be centered at 2.0 V_{BE} and allowed to swing ± V_{BE}. A capacitor is placed from DS IN2 (Pin 20) to V_{EE}. The size of this capacitor and the nature of the data signal determine how faithfully the data slicer shapes up the recovered signal. The time constant is short for large peak to peak voltage swings or when there is a change in DC level at the detector output. For small signal or for continuous bits of the same polarity which drift close to the threshold voltage, the time constant is longer.

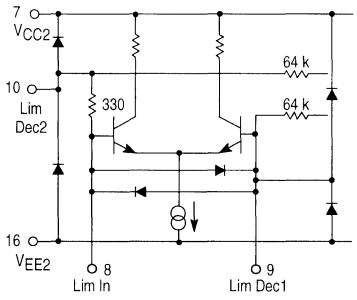
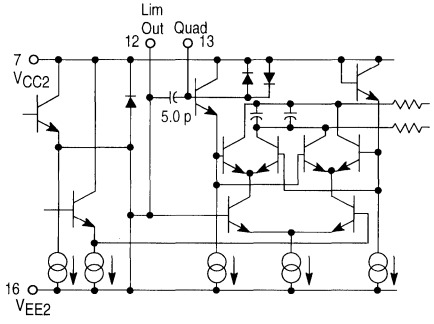
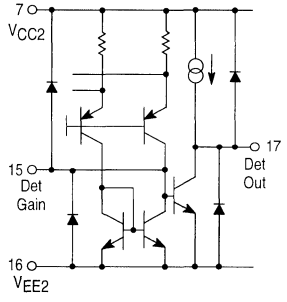
A unique feature of the data slicer is that the inverting switching stages in the comparator are supplied through the emitter pin of the output transistor (Pin 22 – DS Gnd) to V_{EE} rather than internally to V_{EE}. This is provided in order to reduce switching feedback to the front end. A control pin is provided to shut the data slicer output off (DS "off" – Pin 19). With DS "off" pin at V_{CC} the data slicer output is shut off by shutting down the base drive to the output transistor. When a channel is being monitored to make an RSSI measurement, but not to collect data, the data output may be shut off to save current.

2

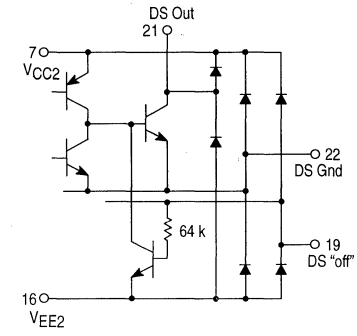
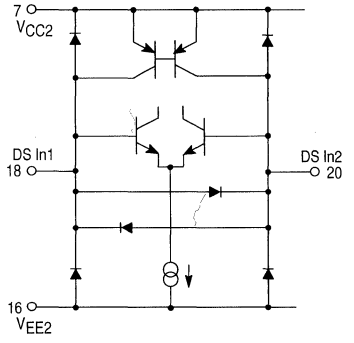
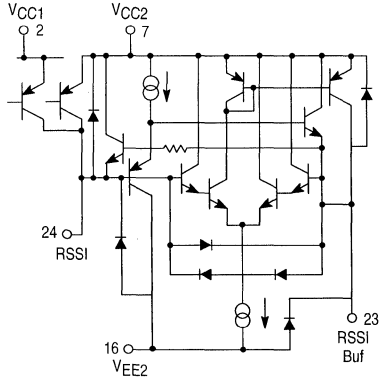
PIN FUNCTION DESCRIPTION

Pin	Symbol	Internal Equivalent Circuit	Description/External Circuit Requirements
1	Mix Out		**Mixer Output** The mixer output impedance is 330 Ω; it matches to 10.7 MHz ceramic filters with 330 Ω input impedance.
2	V_{CC1}		**Supply Voltage (V_{CC1})** This pin is the V_{CC} pin for the Mixer, Local Oscillator, and IF Amplifer. The operating supply voltage range is from 1.8 Vdc to 5.0 Vdc. In the PCB layout, the V_{CC} trace must be kept as wide as possible to minimize inductive reactances along the trace; it is best to have it completely fill around the surface mount components and traces on the circuit side of the PCB.
3	IF In		**IF Input** The input impedance at Pin 3 is 330 Ω. It matches the 330 Ω load impedance of a 10.7 MHz ceramic filter. Thus, no external matching is required.
4	IF Dec1		**IF DEC1 & DEC2** IF decoupling pins. Decoupling capacitors should be placed directly at the pins to enhance stability. Two capacitors are decoupled to the RF ground V_{CC1}; one is placed between DEC1 & DEC2.
5	IF Dec2		
6	IF Out		**IF Output** The output impedance is 330 Ω; it matches the 330 input resistance of a 10.7 MHz ceramic filter.

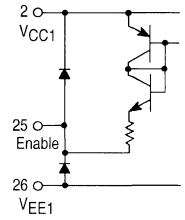
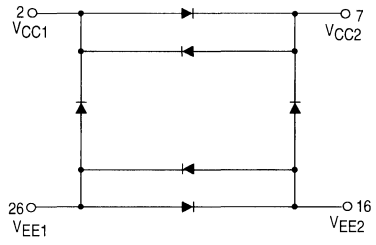
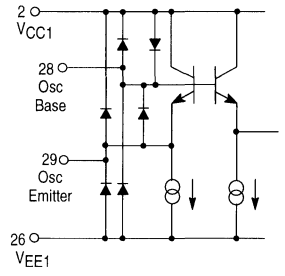
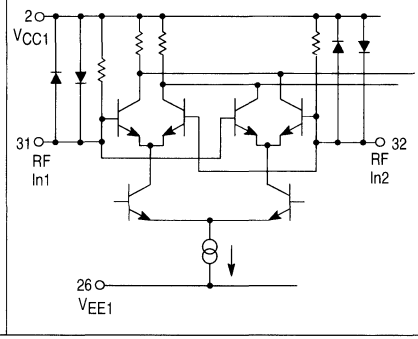
PIN FUNCTION DESCRIPTION (continued)

Pin	Symbol	Internal Equivalent Circuit	Description/External Circuit Requirements
7	V_{CC2}		**Supply Voltage (V_{CC2})** This pin is V_{CC} supply for the Limiter, Quadrature Detector, data slicer and RSSI buffer circuits. In the application PC board this pin is tied to a common V_{CC} trace with V_{CC1}. **Limiter Input** The limiter input impedance is 330 Ω. **Limiter Decoupling** Decoupling capacitors are placed directly at these pins and to V_{CC} (RF ground). Use the same procedure as in the IF decoupling.
8	Lim In		
9	Lim Dec1		
10	Lim Dec2		
11,14, 27 & 28	N/C		**No Connects** There is no internal connection to these pins; however it is recommended that these pins be connected externally to V_{CC} (RF ground).
12	Lim Out		**Limiter Output** The output impedance is low. The limiter drives a quadrature detector circuit with in–phase and quadrature phase signals. **Quadrature Detector Circuit** The quadrature detector is a doubly balanced four–quadrant multiplier with an internal 5.0 pF capacitor between Pins 12 and 13. An external capacitor may be added to increase the IF signal to Pin 13. The quadrature detector pin is provided to connect the external RLC parallel resonant network which provides the 90 degree phase shift and drives the quadrature detector.
13	Quad		
15	Det Gain		**Detector Buffer Amplifier** This is an inverting amplifier. An external feedback resistor from Pin 17 to 15, (the inverting input) controls the output amplitude; another resistor from Pin 15 to the negative supply (Pin 16) sets the DC output level. A 1:1 resistor ratio sets the output DC level at two V_{BE} with respect to V_{EE}. A small capacitor from Pin 17 to 15 can be used to set the bandwidth. **Supply Ground (V_{EE2})** In the PCB layout, the ground pins (also applies to Pin 26) should be connected directly to chassis ground. Decoupling capacitors to V_{CC} should be placed directly at the ground pins.
16	V_{EE2}		

PIN FUNCTION DESCRIPTION (continued)

Pin	Symbol	Internal Equivalent Circuit	Description/External Circuit Requirements
19 21 22	DS "off" DS Out DS Gnd		**Data Slicer Off** The data output may be shut off to save current by placing DS "off" (Pin 19) at V_{CC}. **Data Slicer Output** In the application example a 10 kΩ pull–up resistor is connected to the collector of the output transistor at Pin 21. **Data Slicer Ground** All the inverting switching stages in the comparator are supplied through the emitter pin of the output transistor (Pin 22) to ground rather than internally to V_{EE} in order to reduce switching feedback to the front end.
18 20	DS In1 DS In2		**Data Slicer Inputs** The data slicer has differential inputs with back to back diodes across them. The recovered signal is DC coupled to DS IN1 (Pin 18) at nominally V_{18} with respect to V_{EE}; thus, it will maintain $V_{18} \pm V_{BE}$ at Pin 18. DS IN2 (Pin 20) is AC coupled to V_{EE}. The choice of coupling capacitor is dependent on the nature of the data signal. For small signal or continuous bits of the same polarity, the response time is relatively large. On the other hand, for large peak to peak voltage swings or when the DC level at the detector output changes, the response time is short. See the discussion in the application section for external circuit design details.
23 24	RSSI Buf RSSI		**RSSI Buffer** A unity gain amplifier is used to buffer the voltage at Pin 24 to 23.The output of the unity gain buffer (Pin 23) has an active pull up but no pull down. An external resistor is placed from Pin 23 to V_{EE} to provide the pull down. **RSSI** The RSSI output current creates a voltage drop across an external resistor from Pin 24 to V_{EE}. The maximum RSSI current is 26 μA; thus, the maximum RSSI voltage using a 100 kΩ resistor is approximately 2.6 Vdc. Figure 22 shows the RSSI Output Voltage versus Input Signal Level in the application circuit. The negative slew rate is determined by an external capacitor and resistor to V_{EE} (negative supply). The RSSI rise and fall times for various RF input signal levels and R_{24} values without the capacitor, C_{24} are displayed in Figure 24. This is the maximum response time of the RSSI.

PIN FUNCTION DESCRIPTION (continued)

Pin	Symbol	Internal Equivalent Circuit	Description/External Circuit Requirements
25 26	Enable V_{EE1}		**Enable** The IC regulators are enabled by placing this pin at V_{EE}.
			**V_{CC} and V_{EE} ESD Protection** ESD protection diodes exist between the V_{CC} and V_{EE} pins. It is important to note that significant differences in potential (> 0.5 V_{BE}) between the two V_{CC} pins or between the V_{EE} pins can cause these structures to start to conduct, thus compromising isolation between the supply busses. V_{CC1} & V_{CC2} should be maintained at the same DC potential, as should V_{EE1} & V_{EE2}.
28 29	Osc Base Osc Emitter		**Oscillator Base** This pin is connected to the base lead of the common collector transistor. Since there is no internal bias resistor to the base, V_{CC} is applied through an external choke or coil. **Oscillator Emitter** This pin is connected to the emitter lead; the emitter is connected internally to a current source of about 200 μA. Additional emitter current may be obtained by connecting an external resistor to V_{EE}; $I_E = V_{29}/R_{29}$. Details of circuits using overtone crystal and LC varactor controlled oscillators are discussed in the application section.
31 32	Mix In1 Mix In2		**Mixer Inputs** The parallel equivalent differential input impedance of the mixer is approximately 2.0 kΩ in parallel with 1.0 pF. This equates to a single ended input impedance of 1.0 kΩ in parallel with 2.0 pF. The application circuit utilizes a SAW filter having a differential output that requires a 2.0 kΩ II 2.0 pF load. Therefore, little matching is required between the SAW filter and the mixer inputs. This and alternative circuits are discussed in more detail in the application section.

APPLICATIONS INFORMATION

Evaluation PC Board

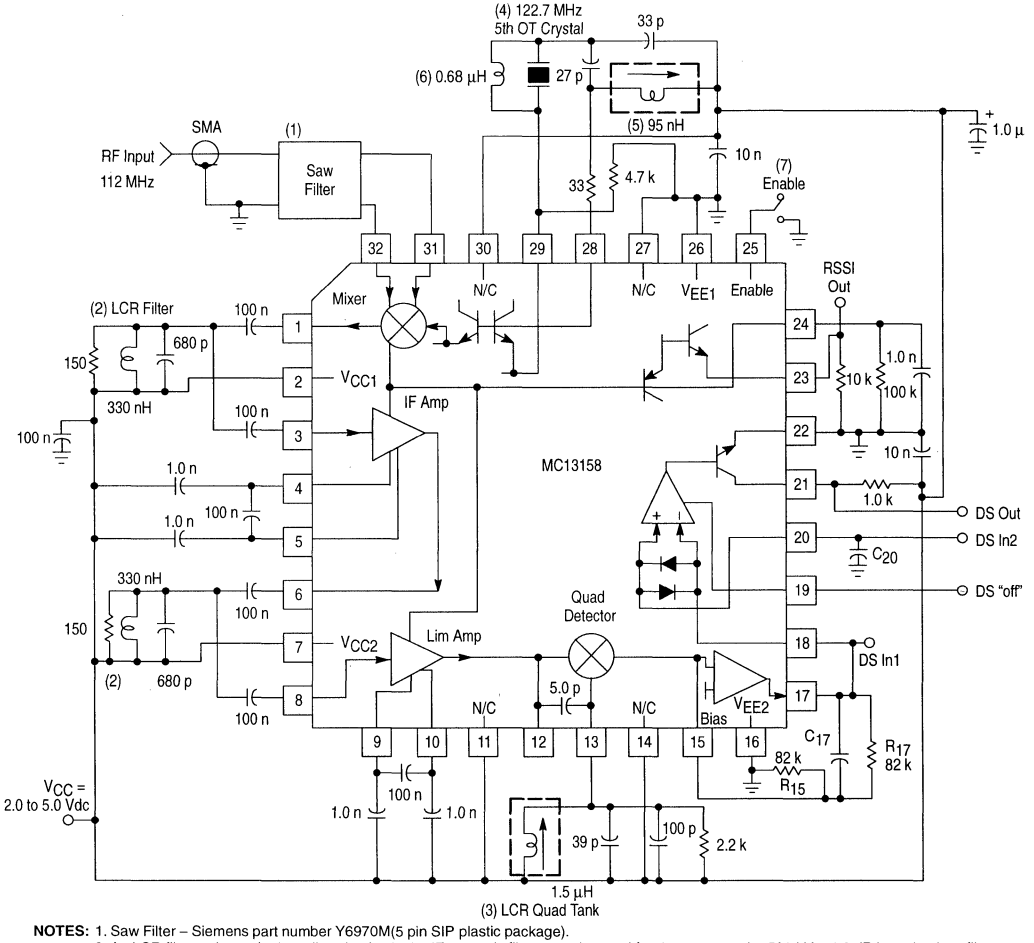
The evaluation PCB is very versatile and is intended to be used across the entire useful frequency range of this device. The center section of the board provides an area for attaching all SMT components to the circuit side and radial leaded components to the component ground side (see Figures 29 and 30). Additionally, the peripheral area surrounding the RF core provides pads to add supporting and interface circuitry as a particular application dictates. This evaluation board will be discussed and referenced in this section.

Component Selection

The evaluation PC board is designed to accommodate specific components, while also being versatile enough to use components from various manufacturers and coil types. Figures 13 and 14 show the placement for the components specified in the application circuit (Figure 12). The application circuit schematic specifies particular components that were used to achieve the results shown in the typical curves and tables but alternate components should give similar results.

2

Figure 12. Application Circuit



NOTES: 1. Saw Filter – Siemens part number Y6970M(5 pin SIP plastic package).
2. An LCR filter reduces the broadband noise in the IF; ceramic filters may be used for data rates under 500 kHz. 4.0 dB insertion loss filters optimize the linearity of RSSI.
3. The quadrature tank components are chosen to optimize linearity of the recovered signal while maintaining adequate recovered signal level. 1.5 µH 7.0 mm variable shielded inductor: Toko part # 292SNS–T1373Z. The shunt resistor is approximately equal to $Q(2\pi fL)$, where Q ~ 18 (3.0 dB BW = 600 kHz).
4. The local oscillator circuit utilizes a 122.7 MHz, 5th overtone, series resonant crystal specified with a frequency tolerance of 25 PPM, ESR of 120 Ω max. The oscillator configuration is an emitter coupled butler.
5. The 95 NH (Nominal) inductor is a 7.0 mm variable shielded inductor: Coilcraft part # 150–04J08S or equivalent.
6. 0.68 µH axial lead chokes (molded inductor): Coilcraft part # 90–11.
7. To enable the IC, Pin 25 is taken to V_{EE}. The external pull down resistor at Pin 29 could be linked to the enable function; otherwise if it is taken to V_{EE} as shown, it will keep the oscillator biased at about 500 µA depending on the V_{CC} level.
8. The other resistors and capacitors are surface mount components.

Figure 13. Circuit Side Component Placement

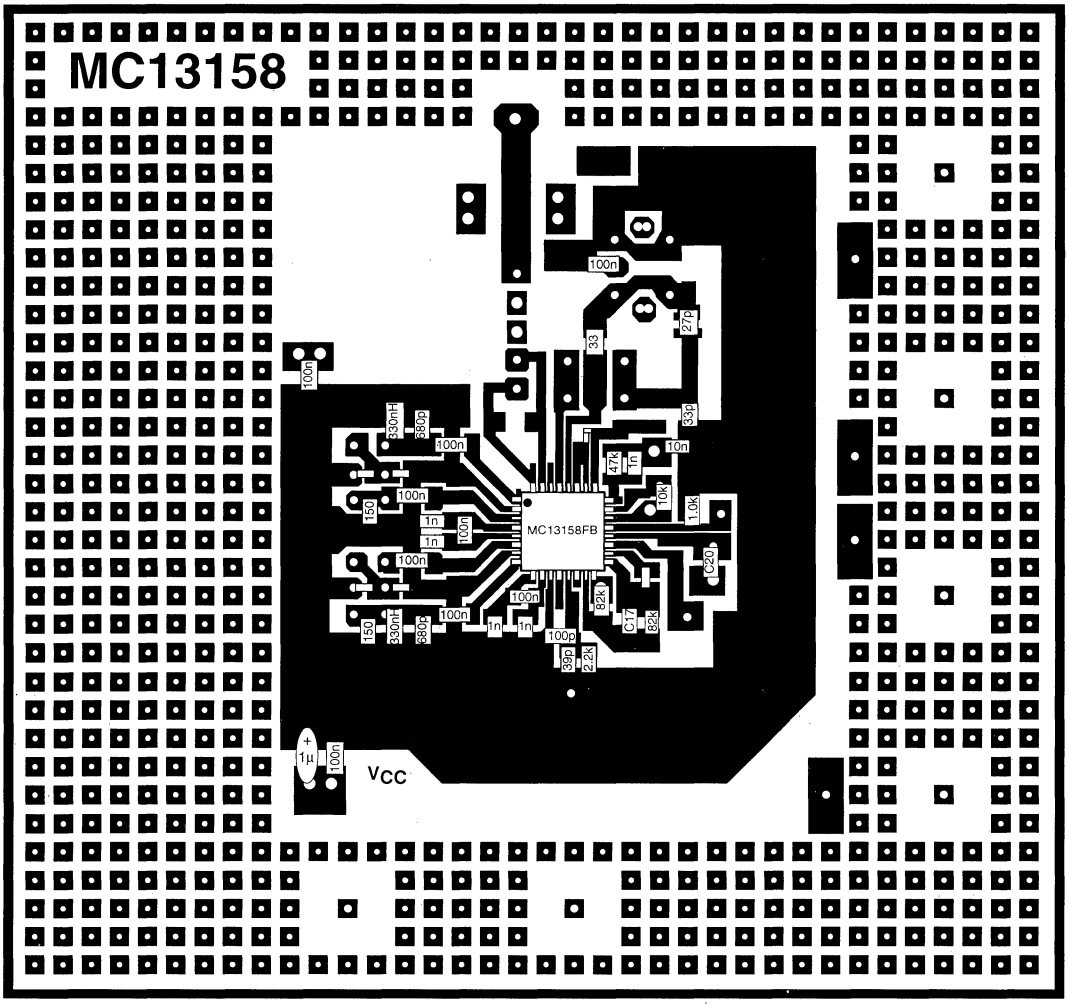


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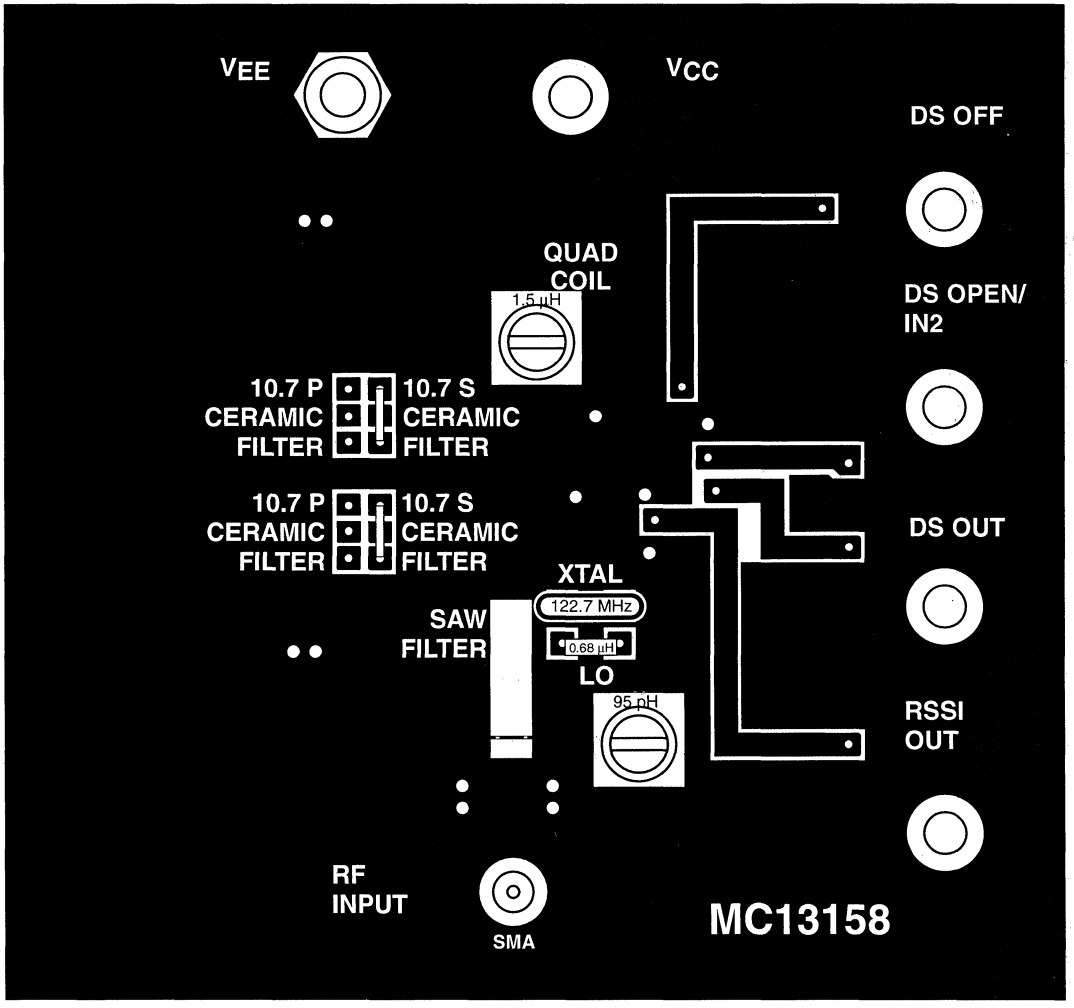
Figure 14. Ground Side Component Placement



Input Matching/Components

It is desirable to use a SAW filter before the mixer to provide additional selectivity and adjacent channel rejection. In a wideband system the primary sensitivity of the receiver backend may be achieved before the last mixer. Bandpass filtering in the limiting IF is costly and difficult to achieve for bandwidths greater than 280 kHz.

The SAW filter should be selected to easily interface with the mixer differential input impedance of approximately 2.0 kΩ in parallel with 1.0 pF. The PC board is dedicated to the Siemens SAW filter (part number Y6970M); the part is designed for DECT at 112 MHz 1st IF frequency. It is designed for a load impedance of 2.0 kΩ in parallel with 2.0 pF; thus, no or little input matching is required between the SAW filter and the mixer.

The Siemens SAW filter has an insertion loss of typically 10 dB and a 3.0 dB bandwidth of 1.0 MHz. The relatively high insertion loss significantly contributes to the system noise and a filter having lower insertion loss would be desirable. In existing low loss SAW filters, the required load impedance is 50 Ω; thus, interface matching between the filter and the mixer will be required. Figure 15 is a table of the single–ended mixer input impedance. A careful noise analysis is necessary to determine the secondary contribution to system noise.

2

Figure 15. Mixer Input Impedance

(Single–ended)

f (MHz)	Rs (Ω)	Xs (Ω)	Rp (Ω)	Xp (Ω)	Cp (pF)
50	930	−350	1060	−2820	1.1
100	480	−430	865	−966	1.6
150	270	−400	860	−580	1.8
200	170	−320	770	−410	1.9
250	130	−270	690	−330	1.85
300	110	−250	680	−300	1.8
400	71	−190	580	−220	1.8
500	63	−140	370	−170	1.9
600	49	−110	300	−130	2.0

System Noise Considerations

The system block diagram in Figure 16 shows the cascaded noise stages contributing to the system noise; it represents the application circuit in Figure 12 and a low noise preamp using a MRF941 transistor (see Figure 17). The preamp is designed for a conjugately matched input and output at 2.0 Vdc V_{CE} and 3.0 mAdc I_C. S–parameters at 2.0 V, 3.0 mA and 100 MHz are:

S11 = 0.86, –20
S21 = 9.0, 164
S12 = 0.02, 79
S22 = 0.96, –12

The bias network sets V_{CE} at 2.0 V and I_C at 3.0 mA for V_{CC} = 3.0 to 3.5 Vdc. The preamp operates with 18 dB gain and 2.7 dB noise figure.

In the cascaded noise analysis the system noise equation is:

$$Fsystem = F1 + [(F2–1)/G1] + [(F3–1)]/[(G1)(G2)]$$

where:

F1 = the Noise Factor of the Preamp
G1 = the Gain of the Preamp
F2 = the Noise factor of the SAW Filter
G2 = the Gain of the SAW Filter
F3 = the Noise factor of the Mixer

Note: the proceeding terms are defined as linear relationships and are related to the log form for gain and noise figure by the following:

$$F = \log^{-1}[(NF \text{ in dB})/10] \quad \text{and similarly}$$

$$G = \log^{-1}[(Gain \text{ in dB})/10]$$

The noise figure and gain measured in dB are shown in the system block diagram. The mixer noise figure is typically 14 dB and the SAW filter adds typically 10 dB insertion loss. Addition of a low noise preamp having a 18 dB gain and 2.7 dB noise figure not only improves the system noise figure but it increases the reverse isolation from the local oscillator to the antenna input at the receiver. Calculating in terms of gain and noise factor yields the following:

F1 = 1.86; G1 = 63.1
F2 = 10; G2 = 0.1
F3 = 25.12

Thus, substituting in the equation for system noise factor:

Fsystem = 5.82; NFsystem = 7.7 dB

Figure 16. System Block Diagram for Noise Analysis

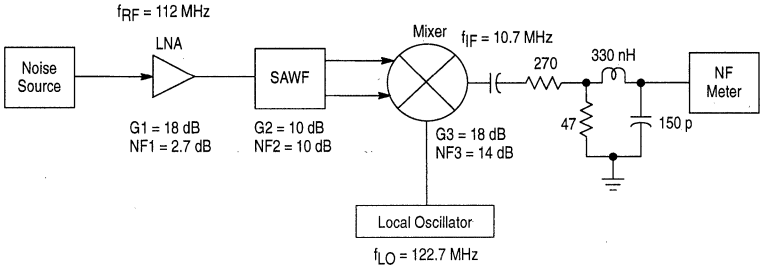
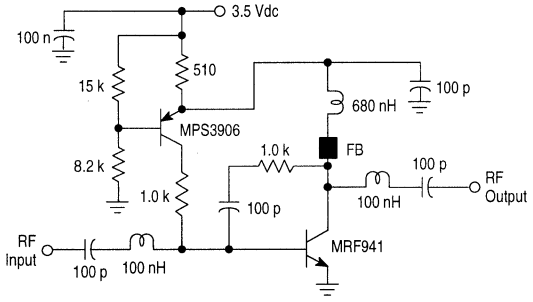


Figure 17. 112 MHz LNA



LOCAL OSCILLATORS

VHF Applications

The on–chip grounded collector transistor may be used for HF and VHF local oscillator with higher order overtone crystals. The local oscillator in the application circuit (Figure 12) shows a 5th overtone oscillator at 122.7 MHz. This circuit uses a Butler overtone oscillator configuration. The amplifier is an emitter follower. The crystal is driven from the emitter and is coupled to the high impedance base through a capacitive tap network. Operation at the desired overtone frequency is ensured by the parallel resonant circuit formed by the variable inductor and the tap capacitors and parasitic capacitances of the on–chip transistor and PC board. The variable inductor specified in the schematic could be replaced with a high tolerance, high Q ceramic or air wound surface mount component if the other components have tight enough tolerances. A variable inductor provides an adjustment for gain and frequency of the resonant tank ensuring lock up and start–up of the crystal oscillator. The overtone crystal is chosen with ESR of typically 80 Ω and 120 Ω maximum; if the resistive loss in the crystal is too high the performance of oscillator may be impacted by lower gain margins.

A series LC network to ground (which is V_{CC}) is comprised of the inductance of the base lead of the on–chip transistor and PC board traces and tap capacitors. Parasitic oscillations often occur in the 200 to 800 MHz range. A small resistor is placed in series with the base (Pin 28) to cancel the negative resistance associated with this undesired mode of oscillation. Since the base input impedance is so large a small resistor in the range of 27 to 68 Ω has very little effect on the desired Butler mode of oscillation.

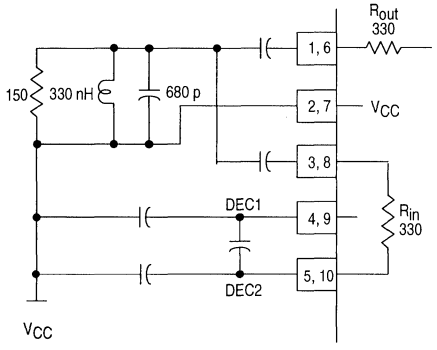
The crystal parallel capacitance, C_o, provides a feedback path that is low enough in reactance at frequencies of 5th overtones or higher to cause trouble. C_o has little effect near resonance because of the low impedance of the crystal motional arm (R_m–L_m–C_m). As the tunable inductor which forms the resonant tank with the tap capacitors is tuned "off" the crystal resonant frequency it may be difficult to tell if the oscillation is under crystal control. Frequency jumps may occur as the inductor is tuned. In order to eliminate this behavior an inductor, L_o, is placed in parallel with the crystal. L_o is chosen to be resonant with the crystal parallel capacitance, C_o, at the desired operation frequency. The inductor provides a feedback path at frequencies well below resonance; however, the parallel tank network of the tap capacitors and tunable inductor prevent oscillation at these frequencies.

IF Filtering/Matching

In wideband data systems the IF bandpass needed is greater than can be found in low cost ceramic filters operating at 10.7 MHz. It is necessary to bandpass limit with LC networks or series–parallel ceramic filter networks. Murata offers a series–parallel resonator pair (part number KMFC545) with a 3.0 dB bandwidth of ± 325 kHz and a maximum insertion loss of 5.0 dB. The application PC board is laid out to accommodate this filter pair (a filter pair is used at both locations of the split IF). However, even using a series parallel ceramic filter network yields only a maximum bandpass of 650 kHz. In some applications a wider band IF bandpass is necessary.

A simple LC network yields a bandpass wider than the SAW filter but it does reduce an appreciable amount of wideband IF noise. In the application circuit an LC network is specified using surface mount components. The parallel LC components are placed from the outputs of the mixer and IF amplifier to the V_{CC} trace; internal 330 loads are connected from the mixer and IF amplifier outputs to DEC2 (Pin 5 and 10 respectively).This loads the outputs with the optimal load impedance but creates a low insertion loss filter. An external shunt resistor may be used to widen the bandpass and to acquire the 10 dB composite loss necessary to linearize the RSSI output. The equivalent circuit is shown in Figure 18.

Figure 18. IF LCR Filter



The following equations satisfy the 12 dB loss (1:4 resistive ratio):

(Rext)(330)/(Rext + 330) = Requivalent
Requivalent/(Requivalent + 330) = 1/4

Solve for Requivalent:

4(Requivalent) = Requivalent + 330
3(Requivalent) = 330
Requivalent = 110

Substitute for Requivalent and solve for Rext:

330(Rext) = 110(Rext) + (330)(110)
Rext = (330)(110)/220
Rext = 165 Ω

The IF is 10.7 MHz although any IF between 10 to 20 MHz could be used. The value of the coil is lowered from that used in the quadrature circuit because the unloaded Q must be maintained in a surface mount component. A standard value component having an unloaded Q = 100 at 10.7 MHz is 330 nH; therefore the capacitor is 669 pF. Standard values have been chosen for these components;

Rext = 150 Ω
C = 680 pF
L = 330 nH

Computation of the loaded Q of this LCR network is

$Q = \text{Requivalent}/X_L$

where: $X_L = 2\pi fL$ and Requivalent is 103 Ω

Thus, Q = 4.65

The total system loss is

20 log (103/433) = –12.5 dB

Quadrature Detector

The quadrature detector is coupled to the IF with an internal 5.0 pF capacitor between Pins 12 and 13. For wideband data applications, the drive to the detector can be increased with an additional external capacitor between these pins; thus, the recovered signal level output is increased for a given bandwidth

The wideband performance of the detector is controlled by the loaded Q of the LC tank circuit. The following equation defines the components which set the detector circuit's bandwidth:

$$Q = R_T/X_L \quad [1]$$

where R_T is the equivalent shunt resistance across the LC Tank
X_L is the reactance of the quadrature inductor at the IF frequency ($X_L = 2\pi fL$).

The inductor and capacitor are chosen to form a resonant LC tank with the PCB and parasitic device capacitance at the desired IF center frequency as predicted by

$$f_c = [2\pi\ (LC_p)^{1/2}]^{-1} \quad [2]$$

where L is the parallel tank inductor C_p is the equivalent parallel capacitance of the parallel resonant tank circuit.

The following is a design example for a wideband detector at 10.7 MHz and a loaded Q of 18. The loaded Q of the quadrature detector is chosen somewhat less than the Q of the IF bandpass. For an IF frequency of 10.7 MHz and an IF bandpass of 600 kHz, the IF bandpass Q is approximately 6.4.

Example:

Let the external Cext = 139 pF. (The minimum value here should be much greater than the internal device and PCB parasitic capacitance, Cint ≈ 3.0 pF). Thus, C_p = Cint + Cext = 142 pF.

Rewrite equation (2) and solve for L:

$$L = (0.159)^2/(C_p f c^2)$$

$$L = 1.56\ \mu H;$$ Thus, a standard value is choosen:

$$L = 1.56\ \mu H \text{ (tunable shielded inductor)}$$

The value of the total damping resistor to obtain the required loaded Q of 18 can be calculated by rearranging equation (1):

$$R_T = Q(2\pi fL)$$

$$R_T = 18(2\pi)(10.7)(1.5) = 1815\ \Omega$$

The internal resistance, Rint at the quadrature tank Pin 13 is approximately 13 kΩ and is considered in determining the external resistance, Rext which is calculated from

$$Rext = ((R_T)(Rint))/(Rint - R_T)$$

Rext = 2110; Thus, choose the standard value:

Rext = 2.2 kΩ

It is important to set the DC level of the detector output at Pin 17 to center the peak to peak swing of the recovered signal. In the equivalent internal circuit shown in the Pin Function Description, the reference voltage at the positive terminal of the inverting op amp buffer amplifier is set at 1.0 V_{BE}. The detector DC level, V_{17} is determined by the following equation:

$$V_{17} = [((R_{15}/R_{17}) + 1)/(R_{15}/R_{17})]\ V_{BE}$$

Thus, for a 1:1 ratio of R_{15}/R_{17}, V_{17} = 2.0 V_{BE} = 1.4 Vdc. Similarly for a 2:1, V_{17} = 1.5 V_{BE} = 1.05 Vdc; and for 3:1, V_{17} = 1.33 V_{BE} = 0.93 Vdc.

Figure 19 shows the detector "S–Curves", in which the resistor ratio is varied while maintaining a constant gain (R_{17} is held at 62 k). R_{15} is 62 k for a 1:1 ratio; while R_{15} = 120 k and 180 k to produce the 2:1 and 3:1 ratios. The IF signal into the detector is swept ± 500 kHz about the 10.7 MHz IF center frequency. The resulting curve show how the resistor ratio and the supply voltage effects the symmetry of the "S–curve" (Figure 21 Test Setup). For the 3:1 and 2:1 ratio, symmetry is maintained with V_S from 2.0 to 5.0 Vdc; however, for the 1:1 ratio, symmetry is lost at 2.0 Vdc.

Figure 19. Detector Output Voltage versus Frequency Deviation

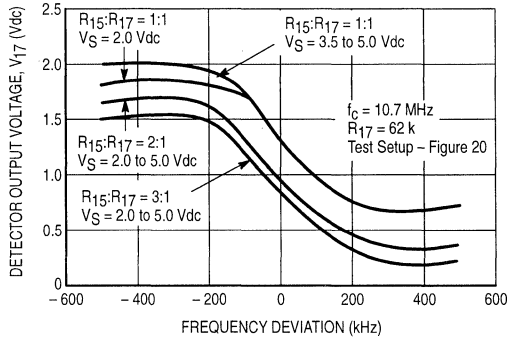
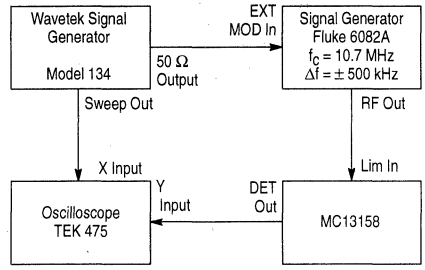


Figure 20. Demodulator "S–Curve" Test Setup



Data Slicer Circuit

C_{20} at the input of the data slicer is chosen to maintain a time constant long enough to hold the charge on the capacitor for the longest strings of bits at the same polarity. For a data rate at 576 kHz a bit stream of 15 bits at the same polarity would equate to an apparent data rate of approximately 77 kbps or 38 kHz. The time constant would be approximately 26 μs. The following expression equates the time constant, t, to the external components:

$$t = 2\pi\ (R_{18})(C_{20})$$

Solve for C_{20}:

$$C_{20} = t/2\pi\ (R_{18})$$

where the effective resistance R_{18} is a complex function of the demodulator feedback resistance and the data slicer input circuit. In the data input network the back to back diodes form a charge and discharge path for the capacitor at Pin 20; however, the diodes create a non–linear response. This resistance is loaded by the ß, beta of the detector output transistor; beta =100 is a typical value (see Figure 21). Thus, the apparent value of the resistance at Pin 18 (DS IN1) is approximately equal to:

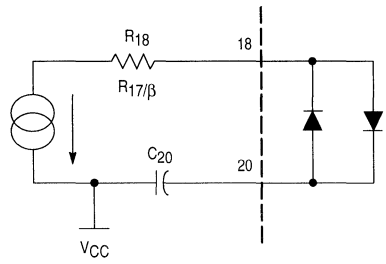
$$R_{18} \sim R_{17}/100$$

where R_{17} is 82 kΩ, the feedback resistor from Pin 17 to 15. Therefore, substituting for R_{18} and solving for C_{20}:

$$C_{20} = 15.9\ (t)/R_{17} = 5.04\ nF$$

The closest standard value is 4.7 nF.

Figure 21. Data Slicer Equivalent Input Circuit



SYSTEM PERFORMANCE DATA

RSSI

In Figure 22, the RSSI versus RF Input Level shows the linear response of RSSI over a 65 dB range but it has extended capability over 80 dB from –80 dBm to +10 dBm. The RSSI is measured in the application circuit (Figure 12) in which a SAW filter is used before the mixer; thus, the overall sensitivity is compromised for the sake of selectivity. The curves are shown for three filters having different bandwidths:

1) LCR Filter with 2.3 MHz 3.0 dB BW (Circuit and Component Placement is shown in Figure 12)
2) Series–Parallel Ceramic Filter with 650 kHz 3.0 dB BW (Murata Part # KMFC–545)
3) Ceramic Filter with 280 kHz 3.0 dB BW.

Figure 22. RSSI Output Voltage versus Signal Input Level

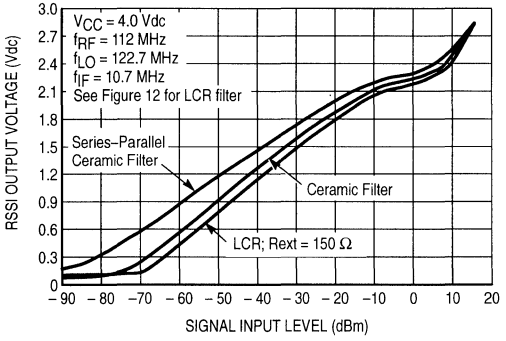
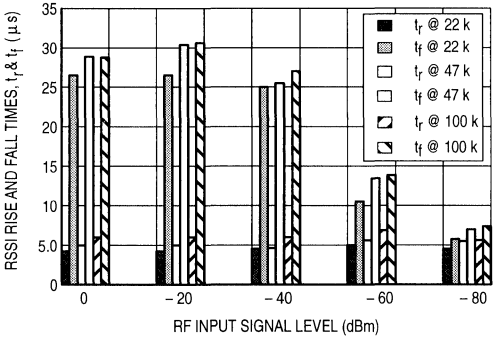


Figure 23. RSSI Output Rise and Fall Times versus RF Input Signal Level



SINAD Performance

Figure 24 shows a test setup for a narrowband demodulator output response in which a C–message filter and an active de–emphasis filter is used following the demodulator. The input is matched using a 1:4 impedance transformer. The SINAD performance is shown in Figure 25 with no preamp and in Figure 26 with a preamp (Preamp – Figure 16). The 12 dB SINAD sensitivity is –101 dBm with no preamp and –113 dBm with the preamp.

Figure 24. Test Setup for Narrowband SINAD

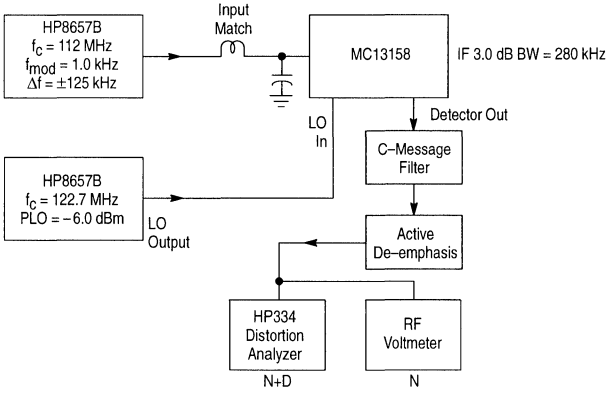


Figure 25. S+N+D, N+D, N versus Input Signal Level (without preamp)

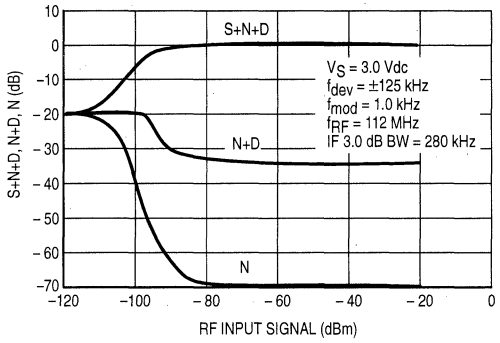


Figure 26. S+N+D, N+D, N versus Input Signal Level (with preamp)

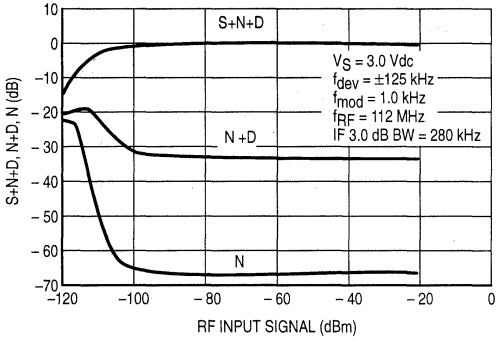


Figure 27. Input IP3, 1.0 dB Compression Pt. Test Setup

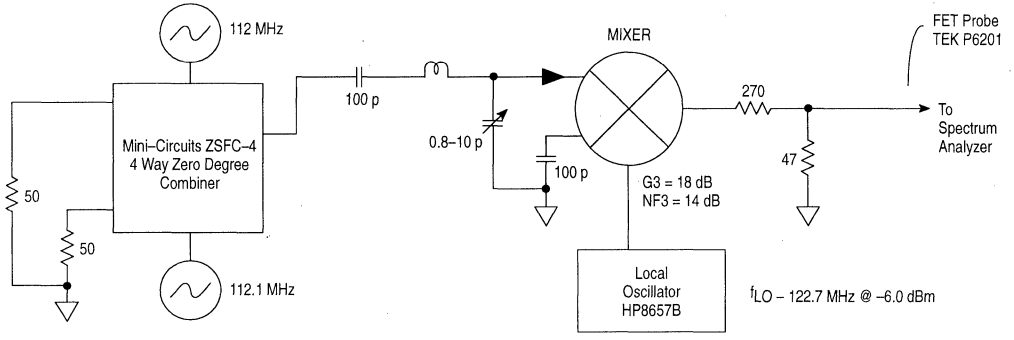


Figure 28. –1.0 dB Compression Pt. and Input Third Order Intercept

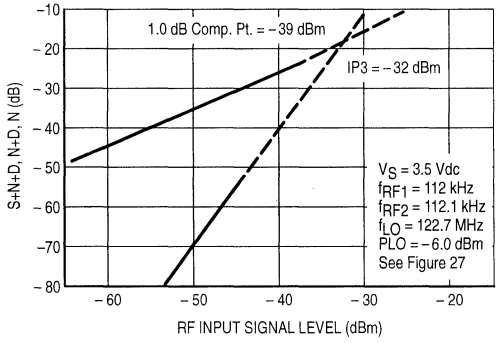


Figure 29. Circuit Side View

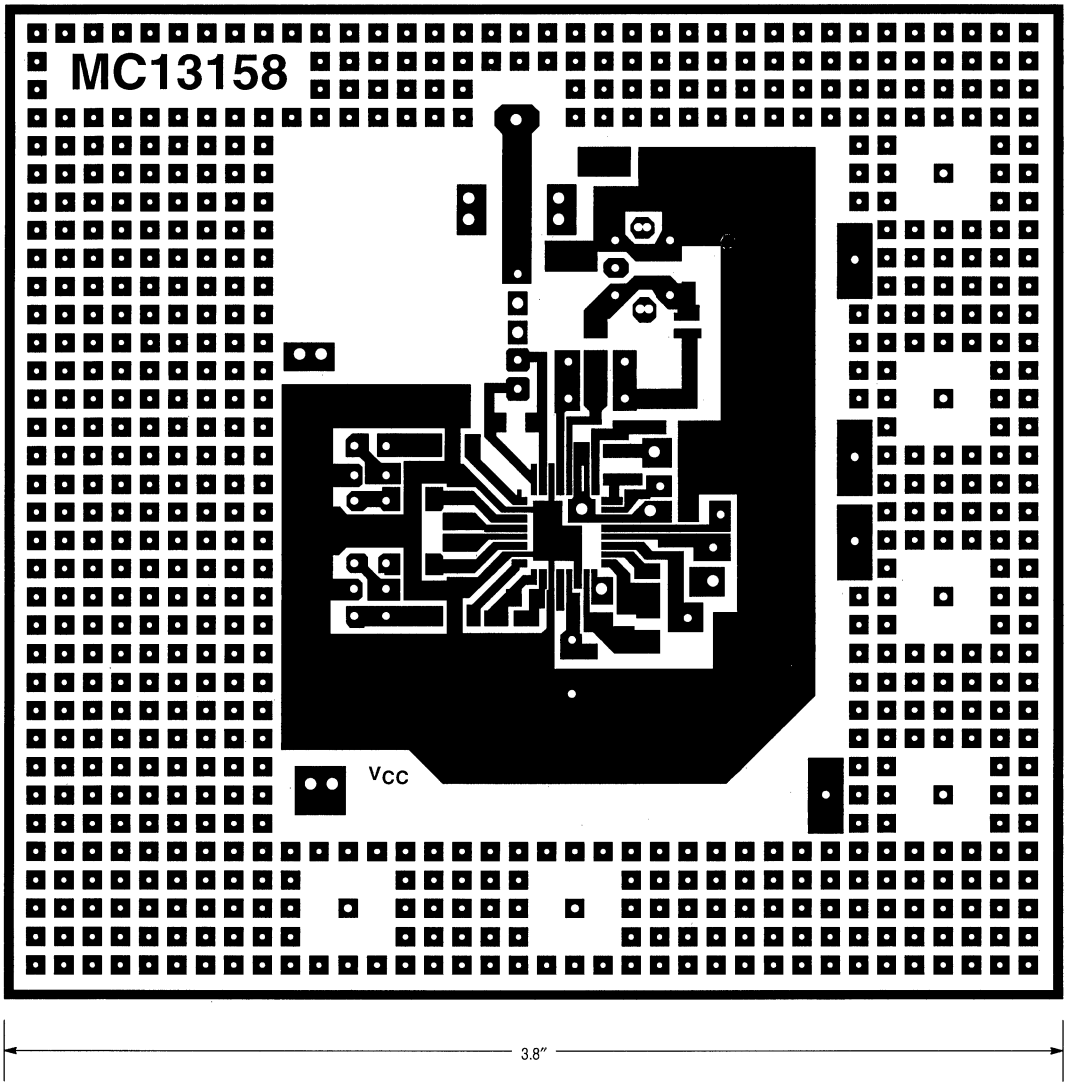
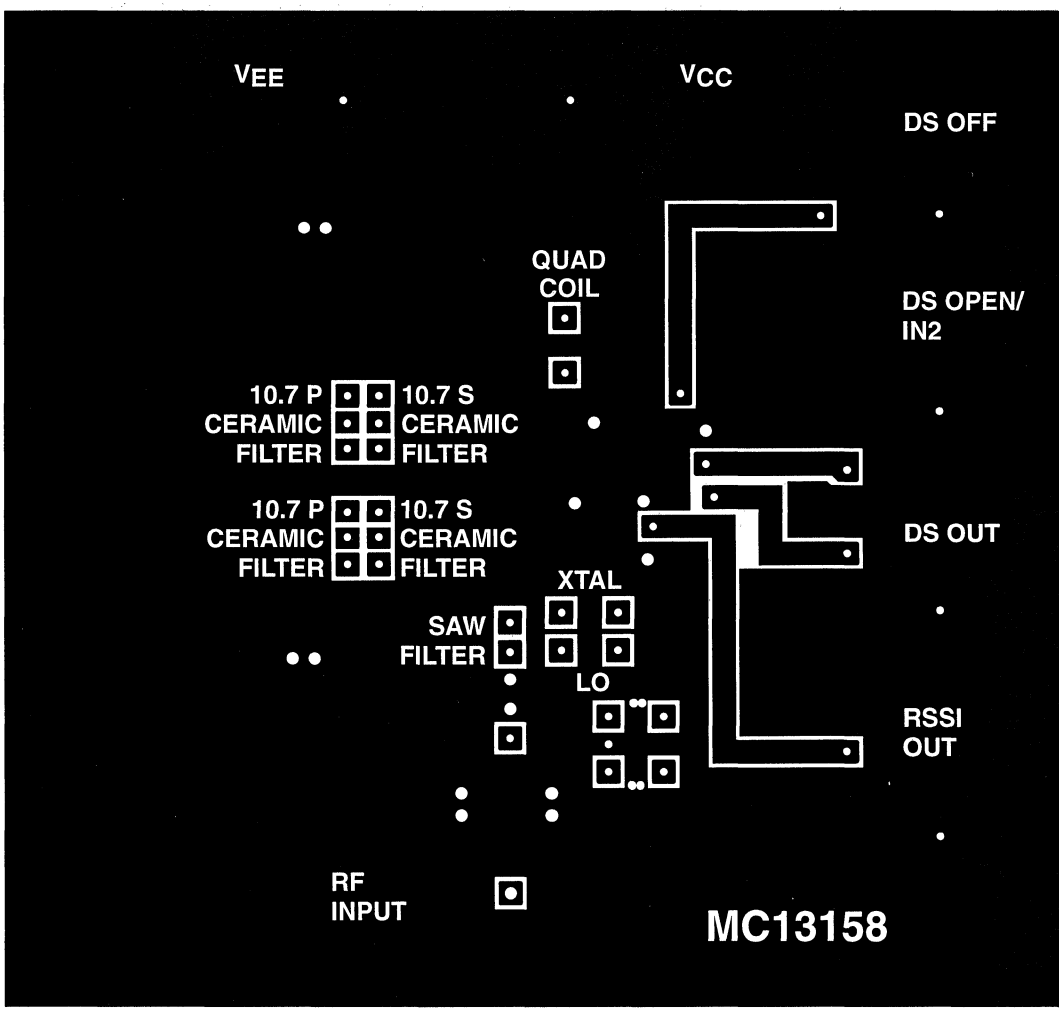
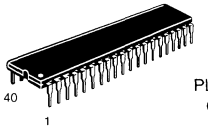


Figure 30. Ground Side View

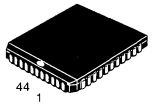


MC14469

Addressable Asynchronous Receiver/Transmitter
CMOS



P SUFFIX
PLASTIC DIP
CASE 711



FN SUFFIX
PLCC PACKAGE
CASE 777

ORDERING INFORMATION

MC14469P	Plastic DIP
MC14469FN	PLCC Package

The MC14469 receives one or two 11–bit words in a serial data stream. One of the incoming words contains the address and when the address matches, the MC14469 then transmits information in two 11–bit word data streams. Each of the transmitted words contains eight data bits, an even parity bit, and start and stop bits.

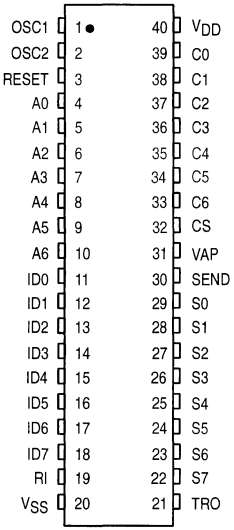
The received word contains seven address bits with the address of the MC14469 set on seven pins. Therefore, 2^7 or 128 units can be interconnected in simplex or full–duplex data transmission. In addition to the address received, seven command bits may be received for general–purpose data or control use.

The MC14469 finds application in transmitting data from remote analog–to–digital converters, remote MPUs, or remote digital transducers to the master computer or MPU.

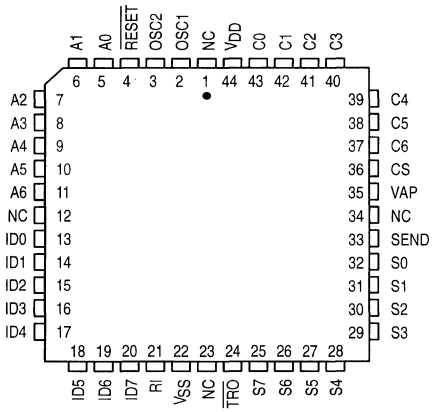
- Supply Voltage Range: 4.5 V to 18 V
- Low Quiescent Current: 75 μA Maximum @ 5 V, 25°C
- Guaranteed Data Rates to 4800 Baud @ 5 V, to 9600 Baud @ 12 V
- Receive — Serial to Parallel
  Transmit — Parallel to Parallel
- Transmit and Receive Simultaneously in Full Duplex
- Crystal or Resonator Operation for On–Chip Oscillator
- See Application Note AN806A
- Chip Complexity: 1200 FETs or 300 Equivalent Gates

PIN ASSIGNMENTS

P SUFFIX

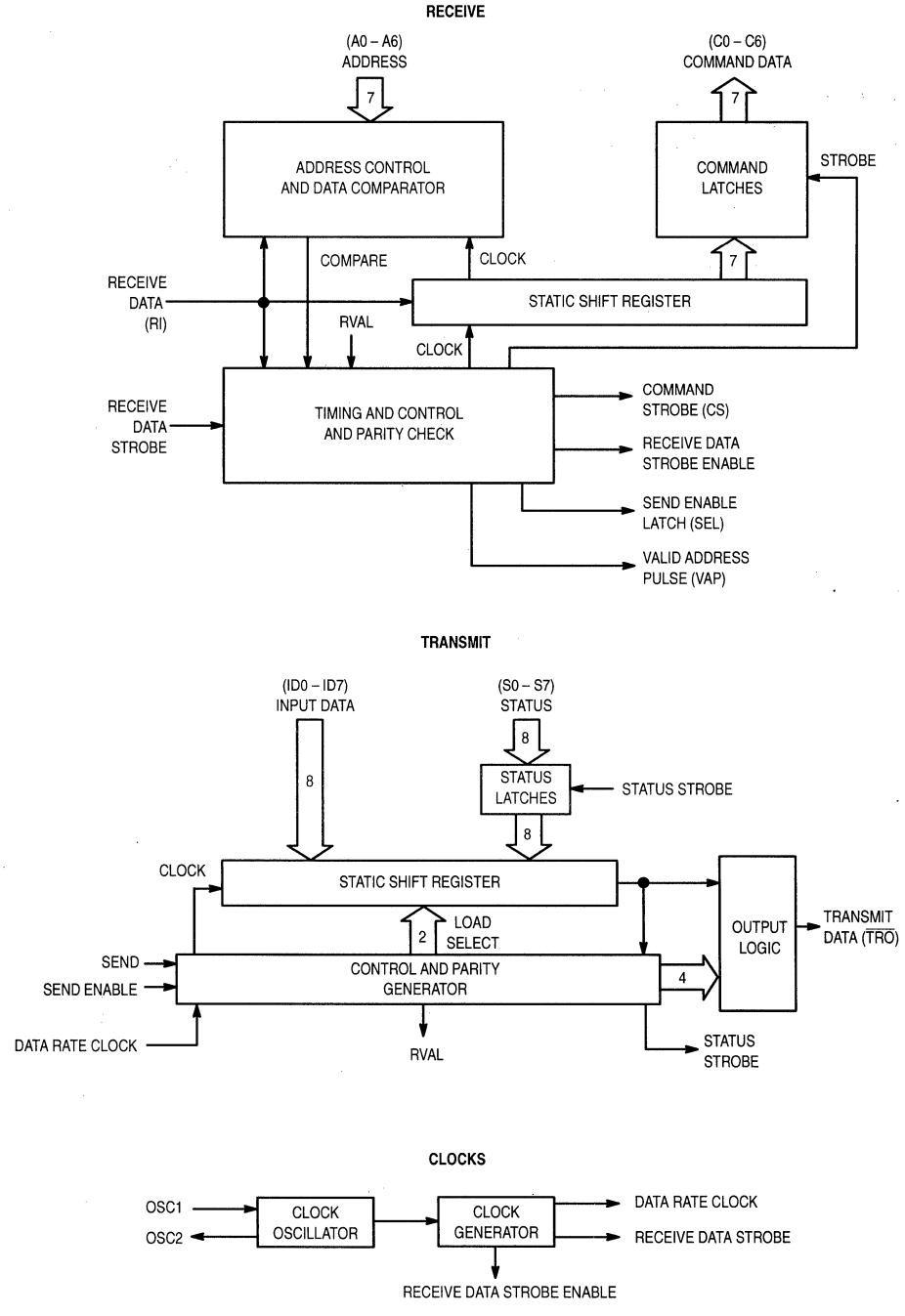


FN SUFFIX



NC = NO CONNECTION

BLOCK DIAGRAM



MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	− 0.5 to + 18	V
Input Voltage, All Inputs	V_{in}	− 0.5 to V_{DD} + 0.5	V
DC Current Drain per Pin	I	10	mA
Operating Temperature Range	T_A	− 40 to + 85	°C
Storage Temperature Range	T_{stg}	− 65 to + 150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

ELECTRICAL CHARACTERISTICS (Voltages referenced to V_{SS})

Characteristic	Symbol	V_{DD}	− 40°C Min	− 40°C Max	25°C Min	25°C Max	85°C Min	85°C Max	Unit
Output Voltage	V_{OL}								V
V_{in} = V_{DD} or 0 "0" Level		5.0	—	0.05	—	0.05	—	0.05	
		10	—	0.05	—	0.05	—	0.05	
		15	—	0.05	—	0.05	—	0.05	
V_{in} = 0 or V_{DD} "1" Level	V_{OH}	5.0	4.95	—	4.95	—	4.95	—	V
		10	9.95	—	9.95	—	9.95	—	
		15	14.95	—	14.95	—	14.95	—	
Input Voltage (Except OSC1)	V_{IL}								V
V_O = 4.5 or 0.5 V "0" Level		5.0	—	1.5	—	1.5	—	1.5	
V_O = 9.0 or 1.0 V		10	—	3.0	—	3.0	—	3.0	
V_O = 13.5 or 1.5 V		15	—	4.0	—	4.0	—	4.0	
V_O = 0.5 or 4.5 V "1" Level	V_{IH}	5.0	3.5	—	3.5	—	3.5	—	V
V_O = 1.0 or 9.0 V		10	7.0	—	7.0	—	7.0	—	
V_O = 1.5 or 13.5 V		15	11	—	11	—	11	—	
Output Drive Current (Except OSC2)	I_{OH}								mA
V_{OH} = 2.5 V Source		5.0	− 1.0	—	− 0.8	—	− 0.6	—	
V_{OH} = 4.6 V		5.0	− 0.2	—	− 0.16	—	− 0.12	—	
V_{OH} = 9.5 V		10	− 0.5	—	− 0.4	—	− 0.3	—	
V_{OH} = 13.5 V		15	− 1.4	—	− 1.2	—	− 1.0	—	
V_{OL} = 0.4 V Sink	I_{OL}	5.0	0.52	—	0.44	—	0.36	—	mA
V_{OL} = 0.5 V		10	1.3	—	1.1	—	0.9	—	
V_{OL} = 1.5 V		15	3.6	—	3.0	—	2.4	—	
Output Drive Current (OSC2 Only)	I_{OH}								mA
V_{OH} = 2.5 V Source		5.0	− 0.19	—	− 0.16	—	− 0.13	—	
V_{OH} = 4.6 V		5.0	− 0.04	—	− 0.035	—	− 0.03	—	
V_{OH} = 9.5 V		10	− 0.09	—	− 0.08	—	− 0.06	—	
V_{OH} = 13.5 V		15	− 0.29	—	− 0.27	—	− 0.2	—	
V_{OL} = 0.4 V Sink	I_{OL}	5.0	0.1	—	0.085	—	0.07	—	mA
V_{OL} = 0.5 V		10	0.17	—	0.14	—	0.1	—	
V_{OL} = 1.5 V		15	0.5	—	0.42	—	0.3	—	
OSC Frequency*	f_{OSC}	4.5	0	400	0	365	0	310	kHz
		12	0	800	0	730	0	620	
Input Current	I_{in}	15	—	± 0.3	—	± 0.3	—	± 1.0	µA
Pull–Up Current (A0 – A6, ID0 – ID7)	I_{UP}	15	12	120	10	100	8.0	85	µA
Input Capacitance (V_{in} = 0)	C_{in}	—	—	—	—	7.5	—	—	pF
Quiescent Current (Per Package)	I_{DD}	5.0	—	75	—	75	—	565	µA
		10	—	150	—	150	—	1125	
		15	—	300	—	300	—	2250	
Supply Voltage	V_{DD}	—	+ 4.5	+ 18	+ 4.5	+ 18	+ 4.5	+ 18	V

* 310 kHz at 85°C guarantees 4800 baud; 620 kHz at 85°C guarantees 9600 baud.

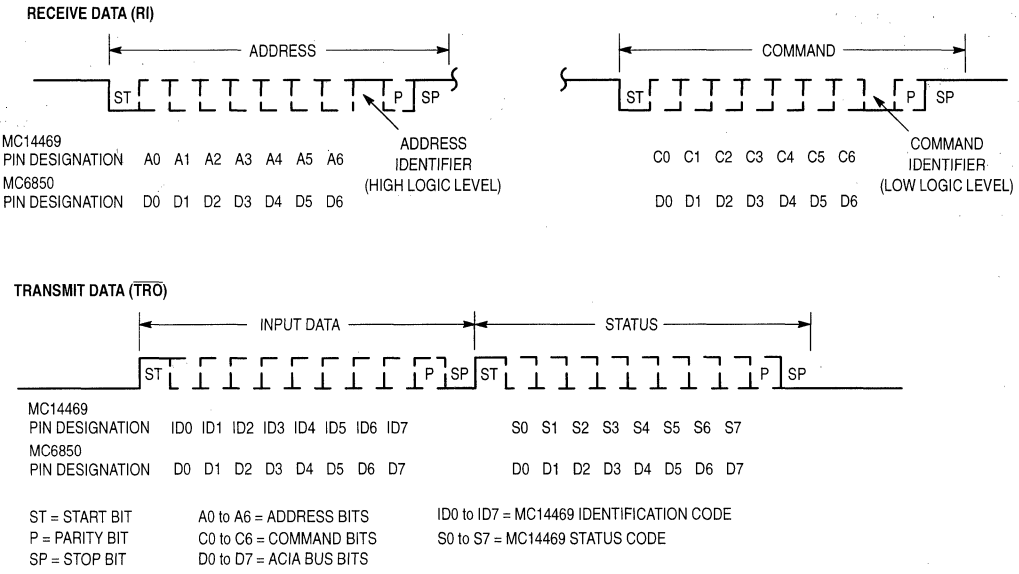


Figure 1. Data Format and Corresponding Data Position and Pins for MC14469 and MC6850

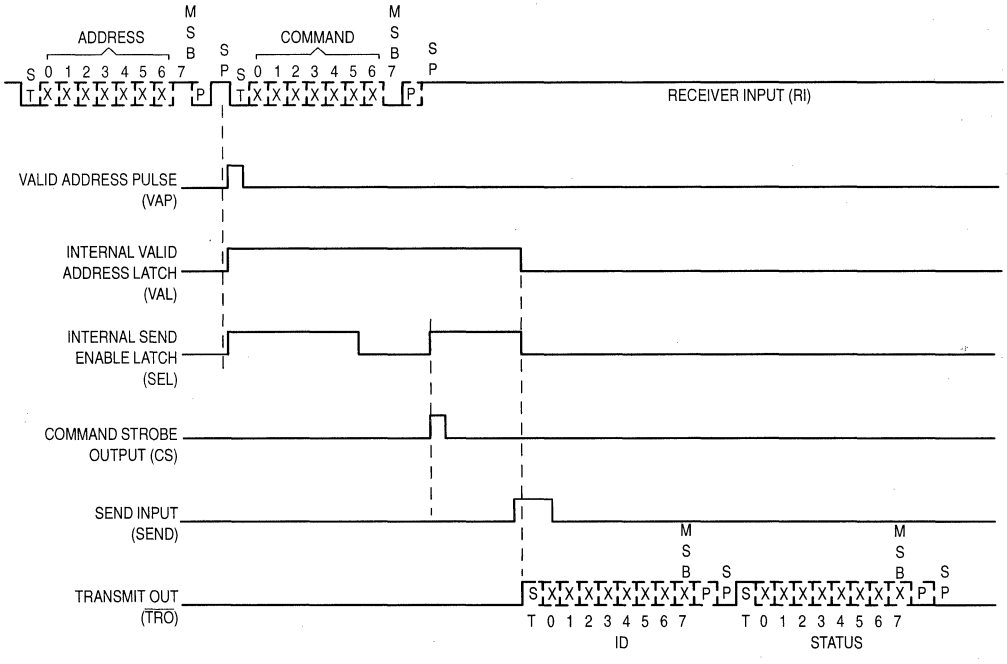


Figure 2. Typical Receive/Send Cycle

PIN DESCRIPTIONS

A0 – A6
Address Inputs

These inputs are the address setting pins which contain the address match for the received signal. Pins A0 – A6 have on–chip pull–up resistors.

C0 – C6
Command Word

These pins are the readout of the general–purpose command word which is the second word of the received signal.

CS
Command Strobe

This is the output for the command strobe signifying a valid set of command data (C0 – C6). The pulse width is one oscillator cycle. For example, when a 307.2 kHz ceramic resonator is used, the pulse width is approximately 3 μs.

ID0 – ID7
Input Data Pins

These pins contain the input data for the first eight bits of data to be transmitted. Pins ID0 – ID7 have on–chip pull–up resistors.

OSC1, OSC2
Oscillator Input and Oscillator Output

These pins are the oscillator input and output (see Figure 3).

$\overline{\text{RESET}}$
Reset

When this pin is pulled low for a minimum of 700 ns, the circuit is reset and ready for operation.

RI
Receive Input

This is the receive input pin.

S0 – S7
Second or Status Input Data

These pins contain the input data for the second eight bits of data to be transmitted.

SEND
Send

This pin accepts the send command after receipt of an address.

$\overline{\text{TRO}}$
Transmit Register Output Signal

This pin transmits the outgoing signal. Note that it is inverted from the incoming signal. It must go through one stage of inversion if it is to drive another MC14469.

VAP
Valid Address Pulse

This is the output for the valid address pulse upon receipt of a matched incoming address.

V_{DD}
Positive Power Supply

This pin is the package positive power supply connection. This pin may range from + 4.5 V to + 18 V with respect to V_{SS}.

V_{SS}
Negative Power Supply

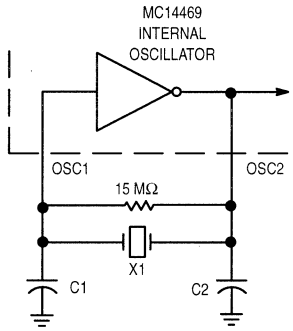
This pin is the negative power supply connection. Normally this pin is system ground.

OPERATING CHARACTERISTICS

The receipt of a start bit on the receive input (RI) line causes the receive clock to start at a frequency equal to that of the oscillator divided by 64. All received data is strobed in at the center of a receive clock period. The start bit is followed by eight data bits. Seven of the bits are compared against states of the address of the particular circuit (A0 – A6). Address is latched 31 clock cycles after the end of the start bit of the incoming address. The eighth bit signifies an address word "1" or a command word "0". Next, a parity bit is received and checked by the internal logic for even parity. Finally a stop bit is received. At the completion of the cycle if the address matches, a valid address pulse (VAP) occurs. Immediately following the address word, a command word is received. It also contains a start bit, eight data bits, even parity bit, and a stop bit. The eight data bits are composed of a seven–bit command, and a "0" which indicates a command word. At the end of the command word a command strobe pulse (CS) occurs.

A positive transition on the send input initiates the transmit sequence. Send must occur within seven bit times of CS. Again the transmitted data is made up of two eleven–bit words, i.e., address and command words. The data portion of the first word is made up from input data inputs (ID0 – ID7), and the data for the second word from second input data (S0 – S7) inputs. The data on inputs ID0 – ID7 is latched one clock before the falling edge of the start bit. The data on inputs S0 – S7 is latched on the rising edge of the start bit. The transmitted signal is the inversion of the received signal, which allows the use of an inverting amplifier to drive the lines. $\overline{\text{TRO}}$ begins either 1/2 or 1–1/2 bit times after send, depending where send occurs.

The oscillator can be crystal controlled or ceramic resonator controlled for required accuracy. OSC1 can be driven from an external oscillator (see Figure 3).



NOTE: For externally generated clock, drive OSC1, float OSC2.

X1 = Ceramic Resonator: 307.2 kHz ± 1 kHz for 4800 baud rate.
C1 and C2 are sized per the ceramic resonator supplier's recommendation.

Ceramic Resonator Suppliers:*
1. Morgan Matroc, Inc., Bedford, OH, 216/232–8600
2. Radio Materials Co., Attica, IN, 317/762–2491

* Motorola cannot recommend one supplier over another and in no way suggests that this is a complete listing of ceramic resonator suppliers.

Figure 3. Oscillator Circuit

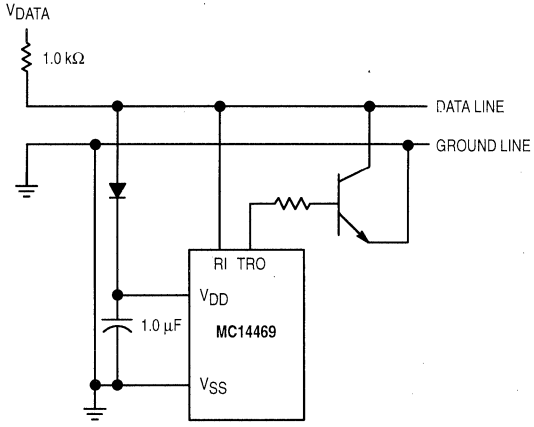


Figure 4. Rectified Power from Data Lines Circuit

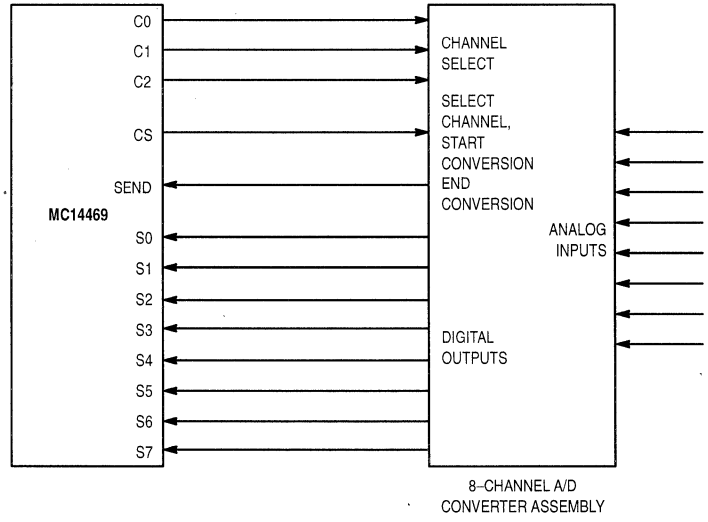


Figure 5. A–D Converter Interface

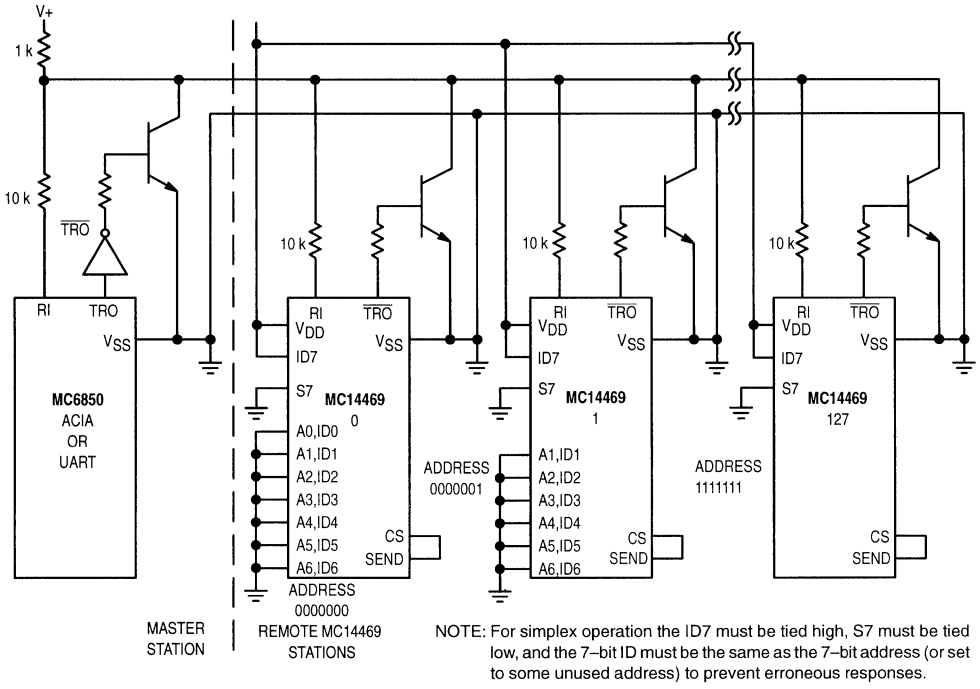


Figure 6. Single Line, Simplex Data Transmission

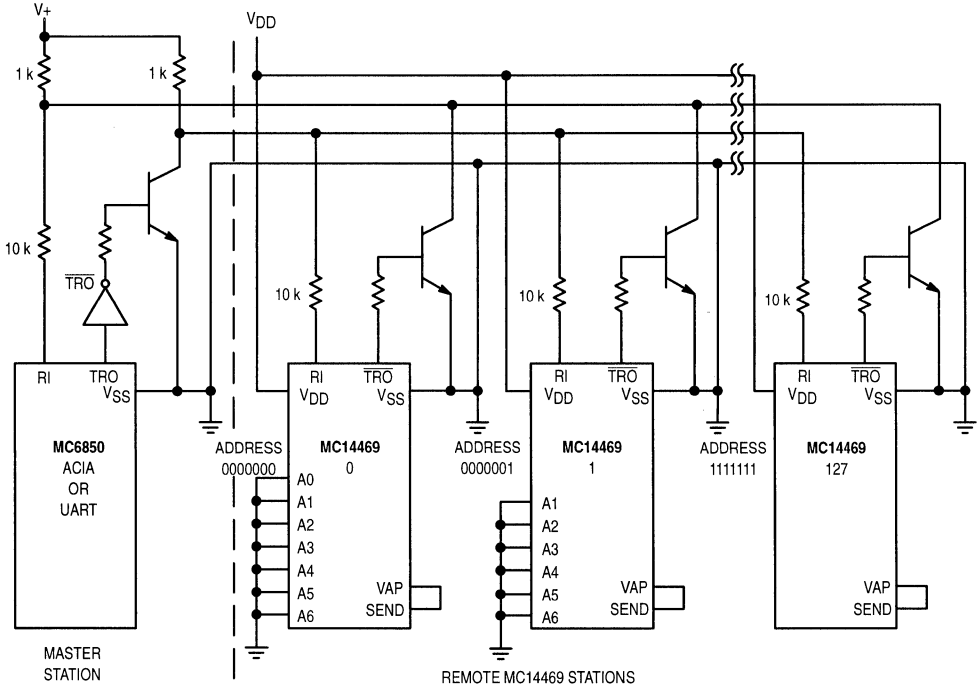


Figure 7. Double Line, Full Duplex Data Transmission

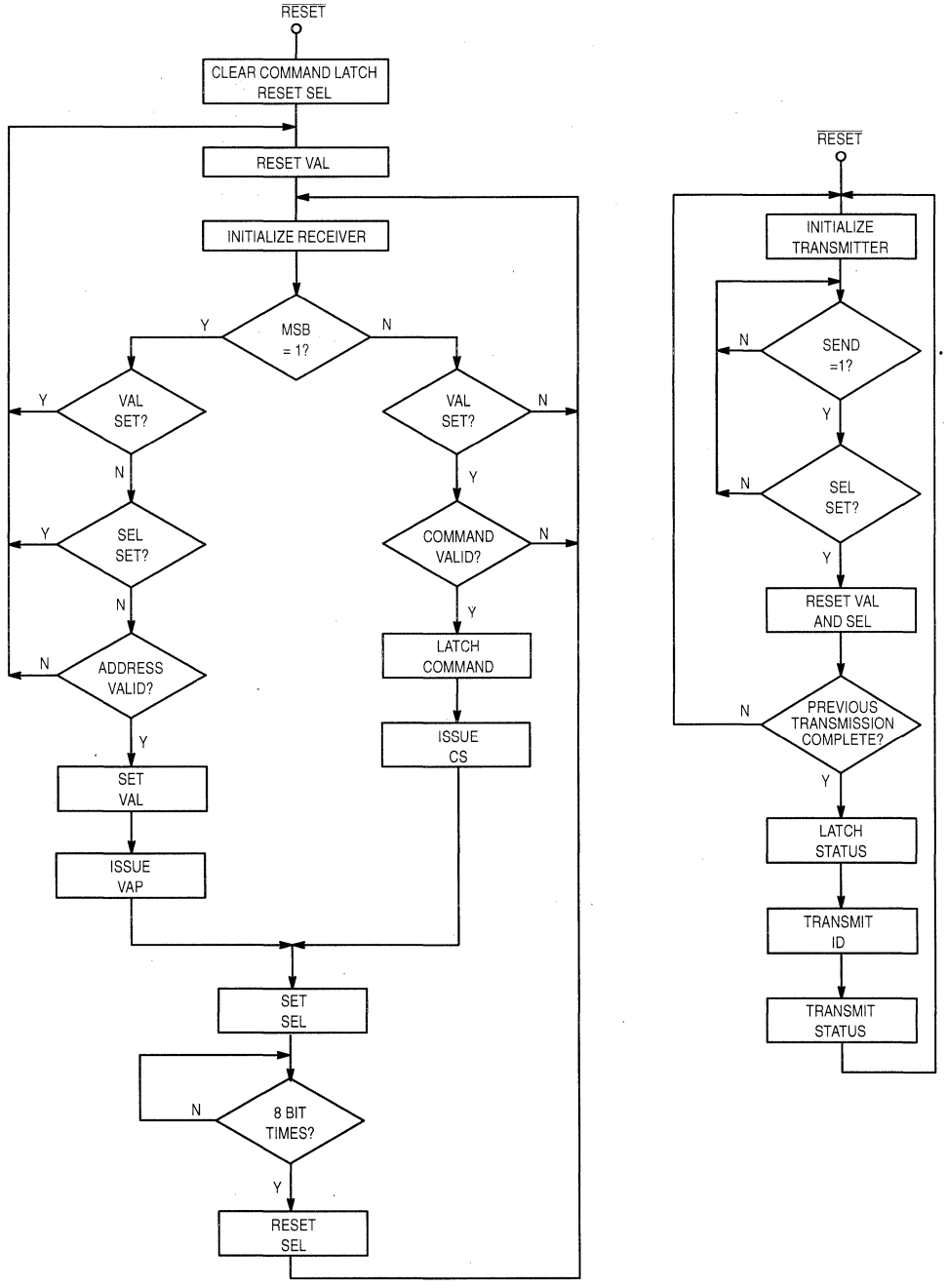
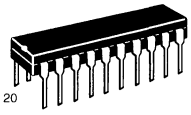


Figure 8. Flow Chart of MC14469 Operation

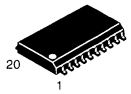
MC14489

Multi-Character LED Display/Lamp Driver

CMOS



P SUFFIX
PLASTIC DIP
CASE 738



DW SUFFIX
SOG PACKAGE
CASE 751D

ORDERING INFORMATION

MC14489P	Plastic DIP
MC14489DW	SOG Package

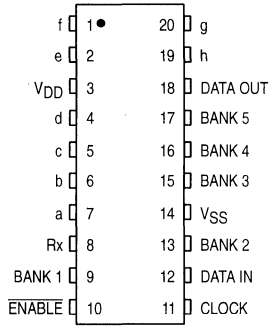
The MC14489 is a flexible light–emitting–diode driver which directly interfaces to individual lamps, 7–segment displays, or various combinations of both. LEDs wired with common cathodes are driven in a multiplexed–by–5 fashion. Communication with an MCU/MPU is established through a synchronous serial port. The MC14489 features data retention plus decode and scan circuitry, thus relieving processor overhead. A single, current–setting resistor is the only ancillary component required.

A single device can drive any one of the following: a 5–digit display plus decimals, a 4–1/2–digit display plus decimals and sign, or 25 lamps. A special technique allows driving 5 1/2 digits; see Figure 16. A configuration register allows the drive capability to be partitioned off to suit many additional applications. The on–chip decoder outputs 7–segment–format numerals 0 to 9, hexadecimal characters A to F, plus 15 letters and symbols.

The MC14489 is compatible with the Motorola SPI and National MICROWIRE™ serial data ports. The chip's patented BitGrabber™ registers augment the serial interface by allowing random access without steering or address bits. A 24–bit transfer updates the display register. Changing the configuration register requires an 8–bit transfer.

- Operating Voltage Range of Drive Circuitry: 4.5 to 6 V
- Operating Junction Temperature Range: – 40° to 130°C
- Current Sources Controlled by Single Resistor Provide Anode Drive
- Low–Resistance FET Switches Provide Direct Common Cathode Interface
- Low–Power Mode (Extinguishes the LEDs) and Brightness Controlled via Serial Port
- Special Circuitry Minimizes EMI when Display is Driven and Eliminates EMI in Low–Power Mode
- Power–On Reset (POR) Blanks the Display on Power–Up, Independent of Supply Ramp Up Time
- May Be Used with Double–Heterojunction LEDs for Optimum Efficiency
- Chip Complexity: 4300 Elements (FETs, Resistors, Capacitors, etc.)
- See Application Note AN431, *Temperature Measurement and Display Using the MC68HC05B4 and the MC14489* and Engineering Bulletin EB153, *Driving a Seven–Segment Display with the NEURON® CHIP*

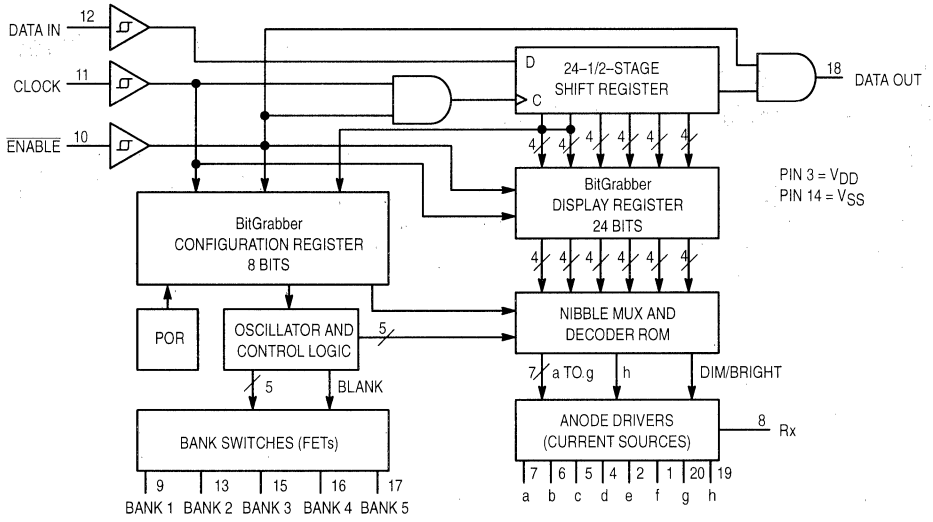
PIN ASSIGNMENT



BitGrabber is a trademark of Motorola Inc.
MICROWIRE is a trademark of National Semiconductor Corp.

REV 3
10/95

BLOCK DIAGRAM



MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	– 0.5 to + 6.0	V
V_{in}	DC Input Voltage	– 0.5 to V_{DD} + 0.5	V
V_{out}	DC Output Voltage	– 0.5 to V_{DD} + 0.5	V
I_{in}	DC Input Current — per Pin (Includes Pin 8)	± 15	mA
I_{out}	DC Output Current — Pins 1, 2, 4 – 7, 19, 20 Sourcing	– 40	mA
	Sinking	10	
	Pins 9, 13, 15, 16, 17 Sinking	320	
	Pin 18	± 15	
I_{DD}, I_{SS}	DC Supply Current, V_{DD} and V_{SS} Pins	± 350	mA
T_J	Chip Junction Temperature	– 40 to + 130	°C
$R_{\theta JA}$	Device Thermal Resistance, Junction–to–Ambient (see Thermal Considerations section) Plastic DIP	90	°C/W
	SOG Package	100	
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds	260	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Descriptions section.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS}, T_J = – 40° to 130°C* unless otherwise indicated)

Symbol	Parameter	Test Condition	V_{DD} V	Guaranteed Limit	Unit
V_{DD}	Power Supply Voltage Range of LED Drive Circuitry		—	4.5 to 6.0	V
V_{DD} (stby)	Minimum Standby Voltage	Bits Retained in Display and Configuration Registers, Data Port Fully Functional	—	3.0	V
V_{IL}	Maximum Low–Level Input Voltage (Data In, Clock, $\overline{Enable}$)		3.0 6.0	0.9 1.8	V
V_{IH}	Minimum High–Level Input Voltage (Data In, Clock, $\overline{Enable}$)		3.0 6.0	2.1 4.2	V
V_{Hys}	Minimum Hysteresis Voltage (Data In, Clock, $\overline{Enable}$)		3.0 6.0	0.2 0.4	V
V_{OL}	Maximum Low–Level Output Voltage (Data Out)	I_{out} = 20 µA	3.0 6.0	0.1 0.1	V
		I_{out} = 1.3 mA	4.5	0.4	
V_{OH}	Minimum High–Level Output Voltage (Data Out)	I_{out} = – 20 µA	3.0 6.0	2.9 5.9	V
		I_{out} = – 800 µA	4.5	4.1	
I_{in}	Maximum Input Leakage Current (Data In, Clock, $\overline{Enable}$)	V_{in} = V_{DD} or V_{SS}	6.0	± 2.0	µA
		V_{in} = V_{DD} or V_{SS}, T_J = 25°C only	6.0	± 0.1	
i_{OL}	Minimum Sinking Current (a, b, c, d, e, f, g, h)	V_{out} = 1.0 V	4.5	0.2	mA
i_{OH}	Peak Sourcing Current — See Figure 9 for currents up to 35 mA (a, b, c, d, e, f, g, h)	Rx = 2.0 kΩ, V_{out} = 3.0 V, Dimmer Bit = High	5.0	13 to 17.5	mA
		Rx = 2.0 kΩ, V_{out} = 3.0 V, Dimmer Bit = Low	5.0	6 to 9	
I_{OZ}	Maximum Output Leakage Current (Bank 1, Bank 2, Bank 3, Bank 4, Bank 5)	V_{out} = V_{DD} (FET Leakage)	6.0	50	µA
		V_{out} = V_{DD} (FET Leakage), T_J = 25°C only	6.0	1	
		V_{out} = V_{SS} (Protection Diode Leakage)	6.0	1	
R_{on}	Maximum ON Resistance (Bank 1, Bank 2, Bank 3, Bank 4, Bank 5)	I_{out} = 0 to 200 mA	5.0	10	Ω
I_{DD}, I_{SS}	Maximum Quiescent Supply Current	Device in Low–Power Mode, V_{in} = V_{SS} or V_{DD}, Rx in Place, Outputs Open	6.0	100	µA
		Same as Above, T_J = 25°C	6.0	20	
I_{ss}	Maximum RMS Operating Supply Current (The V_{SS} leg does not contain the Rx current component. See Pin Descriptions.)	Device NOT in Low–Power Mode, V_{in} = V_{SS} or V_{DD}, Outputs Open	6.0	1.5	mA

* See Thermal Considerations section.

AC ELECTRICAL CHARACTERISTICS (T_J = – 40° to 130°C*, C_L = 50 pF, Input $t_r = t_f$ = 10 ns)

Symbol	Parameter	V_{DD} V	Guaranteed Limit	Unit
f_{clk}	Serial Data Clock Frequency, Single Device or Cascaded Devices NOTE: Refer to Clock t_w below (Figure 1)	3.0 4.5 6.0	dc to 3.0 dc to 4.0 dc to 4.0	MHz
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Clock to Data Out (Figures 1 and 5)	3.0 4.5 6.0	140 80 80	ns
t_{TLH}, t_{THL}	Maximum Output Transistion Time, Data Out (Figures 1 and 5)	3.0 4.5 6.0	70 50 50	ns
f_R	Refresh Rate — Bank 1 through Bank 5 (Figures 2 and 6)	3.0 4.5 6.0	NA 700 to 1900 700 to 1900	Hz
C_{in}	Maximum Input Capacitance — Data In, Clock, $\overline{\text{Enable}}$	—	10	pF

* See Thermal Considerations section.

TIMING REQUIREMENTS (T_J = – 40° to 130°C*, Input $t_r = t_f$ = 10 ns unless otherwise indicated)

Symbol	Parameter	V_{DD} V	Guaranteed Limit	Unit
t_{su}, t_h	Minimum Setup and Hold Times, Data In versus Clock (Figure 3)	3.0 4.5 6.0	50 40 40	ns
t_{su}, t_h, t_{rec}	Minimum Setup, Hold, ** and Recovery Times, $\overline{\text{Enable}}$ versus Clock (Figure 4)	3.0 4.5 6.0	150 100 100	ns
$t_{w(L)}$	Minimum Active–Low Pulse Width, $\overline{\text{Enable}}$ (Figure 4)	3.0 4.5 6.0	4.5 3.4 3.4	µs
$t_{w(H)}$	Minimum Inactive–High Pulse Width, $\overline{\text{Enable}}$ (Figure 4)	3.0 4.5 6.0	300 150 150	ns
t_w	Minimum Pulse Width, Clock (Figure 1)	3.0 4.5 6.0	167 125 125	ns
t_r, t_f	Maximum Input Rise and Fall Times — Data In, Clock, $\overline{\text{Enable}}$ (Figure 1)	3.0 4.5 6.0	1 1 1	ms

* See Thermal Considerations section.

** For a high–speed 8–Clock access, t_h for $\overline{\text{Enable}}$ is determined as follows:
V_{DD} = 3 to 4.5 V, f_{clk} > 1.78 MHz: $t_h = 4350 - (7500/f_{clk})$
V_{DD} = 4.5 to 6 V, f_{clk} > 2.34 MHz: $t_h = 3300 - (7500/f_{clk})$
where t_h is in ns and f_{clk} is in MHz.

NOTES:
1. This restriction does NOT apply for f_{clk} rates less than those listed above. For "slow" f_{clk} rates, use the t_h limits in the above table.
2. This restriction does NOT apply for an access involving more than 8 Clocks. For > 8 Clocks, use the t_h limits in the above table.

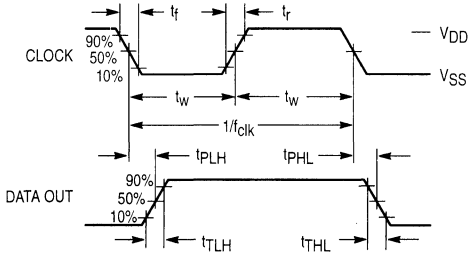


Figure 1.

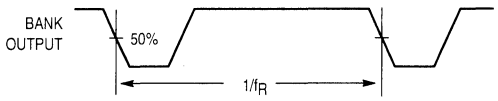


Figure 2.

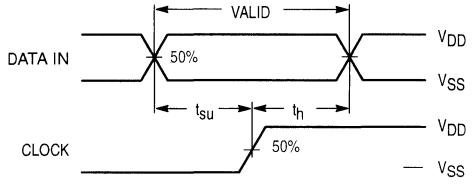


Figure 3.

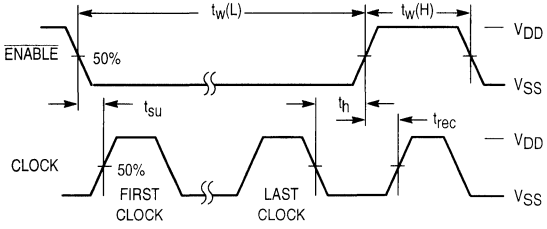
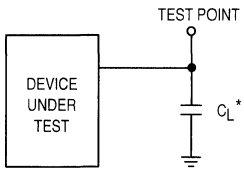
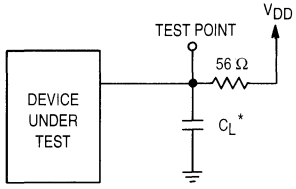


Figure 4.



*Includes all probe and fixture capacitance.

Figure 5.



*Includes all probe and fixture capacitance.

Figure 6.

PIN DESCRIPTIONS

DIGITAL INTERFACE

Data In (Pin 12)

Serial Data Input. The bit stream begins with the MSB and is shifted in on the low–to–high transition of Clock. When the device is not cascaded, the bit pattern is either 1 byte (8 bits) long to change the configuration register or 3 bytes (24 bits) long to update the display register. For two chips cascaded, the pattern is either 4 or 6 bytes, respectively. The display does not change during shifting (until $\overline{\text{Enable}}$ makes a low–to–high transition) which allows slow serial data rates, if desired.

The bit stream needs neither address nor steering bits due to the innovative BitGrabber registers. Therefore, all bits in the stream are available to be data for the two registers. Random access of either register is provided. That is, the registers may be accessed in any sequence. Data is retained in the registers over a supply range of 3 to 6 V. The format is shown in Figures 7 and 8. Information on the segment decoder is given in Table 1.

Data In typically switches near 50% of V_{DD} and has a Schmitt–triggered input buffer. These features combine to maximize noise immunity for use in harsh environments and bus applications. This input can be directly interfaced to CMOS devices with outputs guaranteed to switch near rail–to–rail. When interfacing to NMOS or TTL devices, either a level shifter (MC14504B, MC74HCT04A) or pullup resistor of 1 kΩ to 10 kΩ must be used. Parameters to be considered when sizing the resistor are the worst–case I_{OL} of the driving device, maximum tolerable power consumption, and maximum data rate.

Clock (Pin 11)

Serial Data Clock Input. Low–to–high transitions on Clock shift bits available at Data In, while high–to–low transitions shift bits from Data Out. The chip's 24–1/2–stage shift register is static, allowing clock rates down to dc in a continuous or intermittent mode. The Clock input does not need to be synchronous with the on–chip clock oscillator which drives the multiplexing circuit.

Eight clock cycles are required to access the configuration register, while 24 are needed for the display register when the MC14489 is not cascaded. See Figures 7 and 10.

As shown in Figure 11, two devices may be cascaded. In this case, 32 clock cycles access the configuration register and 48 access the display register, as depicted in Figure 8.

Cascading of 3, 4, and 5 devices is shown in Figures 12, 13, and 14, respectively.

Clock typically switches near 50% of V_{DD} and has a Schmitt–triggered input buffer. Slow Clock rise and fall times are tolerated. See the last paragraph of **Data In** for more information.

NOTE

To guarantee proper operation of the power–on reset (POR) circuit, the Clock pin must NOT be floated or toggled during power–up. That is, the Clock pin must be **stable** until the V_{DD} pin reaches at least 3 V.
If control of the Clock pin during power–up is not practical, then the MC14489 must be reset via bit C0 in the C register. To accomplish this, C0 is reset low, then set high.

$\overline{\text{Enable}}$ (Pin 10)

Active–Low Enable Input. This pin allows the MC14489 to be used on a serial bus, sharing Data In and Clock with other peripherals. When $\overline{\text{Enable}}$ is in an inactive high state, Data Out is forced to a known (low) state, shifting is inhibited, and the port is held in the initialized state. To transfer data to the device, $\overline{\text{Enable}}$ (which initially must be inactive high) is taken low, a serial transfer is made via Data In and Clock, and $\overline{\text{Enable}}$ is taken high. The low–to–high transition on $\overline{\text{Enable}}$ transfers data to either the configuration or display register, depending on the data stream length.

Every rising edge on $\overline{\text{Enable}}$ initiates a blanking interval while data is loaded. Thus, continually loading the device with the same data may cause the LEDs on some banks to appear dimmer than others.

NOTE

Transitions on $\overline{\text{Enable}}$ must not be attempted while Clock is high. This puts the device out of synchronization with the microcontroller. Resynchronization occurs when $\overline{\text{Enable}}$ is high and Clock is low.

This input is also Schmitt–triggered and switches near 50% of V_{DD}, thereby minimizing the chance of loading erroneous data in the registers. See the last paragraph of **Data In** for more information.

Data Out (Pin 18)

Serial Data Output. Data is transferred out of the shift register through Data Out on the high–to–low transition of Clock. This output is a no connect, unless used in one of the manners discussed below.

When cascading MC14489's, Data Out feeds Data In of the next device per Figures 11, 12, 13, and 14.

Data Out could be fed back to an MCU/MPU to perform a wrap–around test of serial data. This could be part of a system check conducted at power–up to test the integrity of the system's processor, pc board traces, solder joints, etc.

The pin could be monitored at an in–line Q.A. test during board manufacturing.

Finally, Data Out facilitates troubleshooting a system.

DISPLAY INTERFACE

Rx (Pin 8)

External Current–Setting Resistor. A resistor tied between this pin and ground (V_{SS}) determines the peak segment drive current delivered at pins a through h. Pin 8's resistor ties into a current mirror with an approximate current gain of 10 when bit D23 = high (brighten). With D23 = low, the peak current is reduced about 50%. Values for Rx range from 700 Ω to infinity. When Rx = ∞ (open circuit), the display is extinguished. For proper current control, resistors having ± 1% tolerance should be used. See Figure 9.

CAUTION

Small Rx values may cause the chip to overheat if precautions are not observed. See **Thermal Considerations.**

a through h (Pins 1, 2, 4 – 7, 19, 20)

Anode–Driver Current Sources. These outputs are closely–matched current sources which directly tie to the anodes of external discrete LEDs (lamps) or display segment LEDs. Each output is capable of sourcing up to 35 mA.

When used with lamps, outputs a, b, c, and d are used to independently control up to 20 lamps. Output h is used to control up to 5 lamps dependently. (See Figure 17.) For lamps, the *No Decode* mode is selected via the configuration register, forcing e, f, and g inactive (low).

When used with segmented displays, outputs a through g drive segments a through g, respectively. Output h is used to drive the decimals. If unused, h must be left open. Refer to Figure 10.

Bank 1 through Bank 5 (Pins 9, 13, 15, 16, 17)

Diode–Bank FET Switches. These outputs are low–resistance switches to ground (V_{SS}) capable of handling currents of up to 320 mA each. These pins directly tie to the common cathodes of segmented displays or the cathodes of lamps (wired with cathodes common).

The display is refreshed at a nominal 1 kHz rate to achieve optimum brightness from the LEDs. A 20% duty cycle is utilized.

Special design techniques are used on–chip to accommodate the high currents with low EMI (electromagnetic interference) and minimal spiking on the power lines.

POWER SUPPLY

V_{SS} (Pin 14)

Most–negative supply potential. This pin is usually ground.

Resistor Rx is externally tied to ground (V_{SS}). Therefore, the chip's V_{SS} pin does not contain the Rx current component.

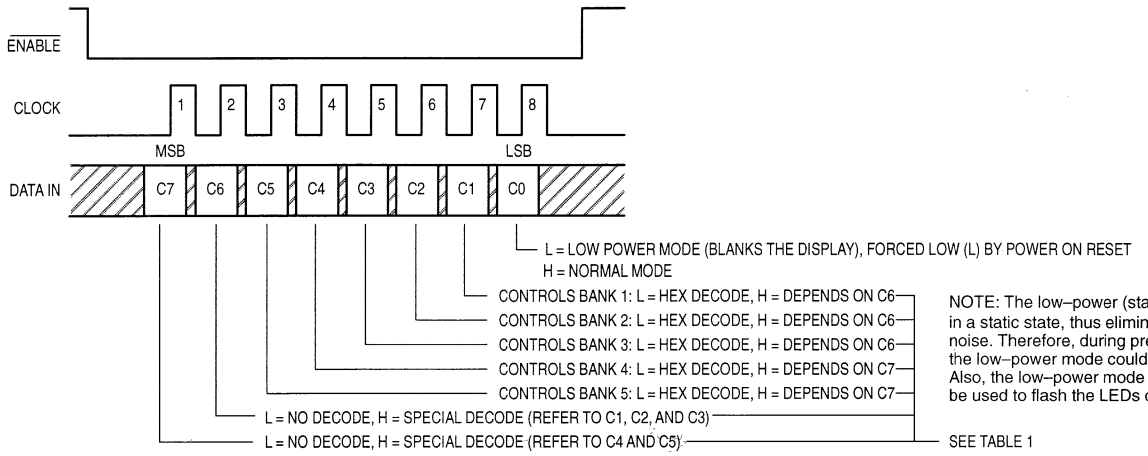
V_{DD} (Pin 13)

Most–positive supply potential.

To guarantee data integrity in the registers and to ensure the serial interface is functional, this voltage may range from 3 to 6 volts with respect to V_{SS}. For example, within this voltage range, the chip could be placed in and out of the low–power mode.

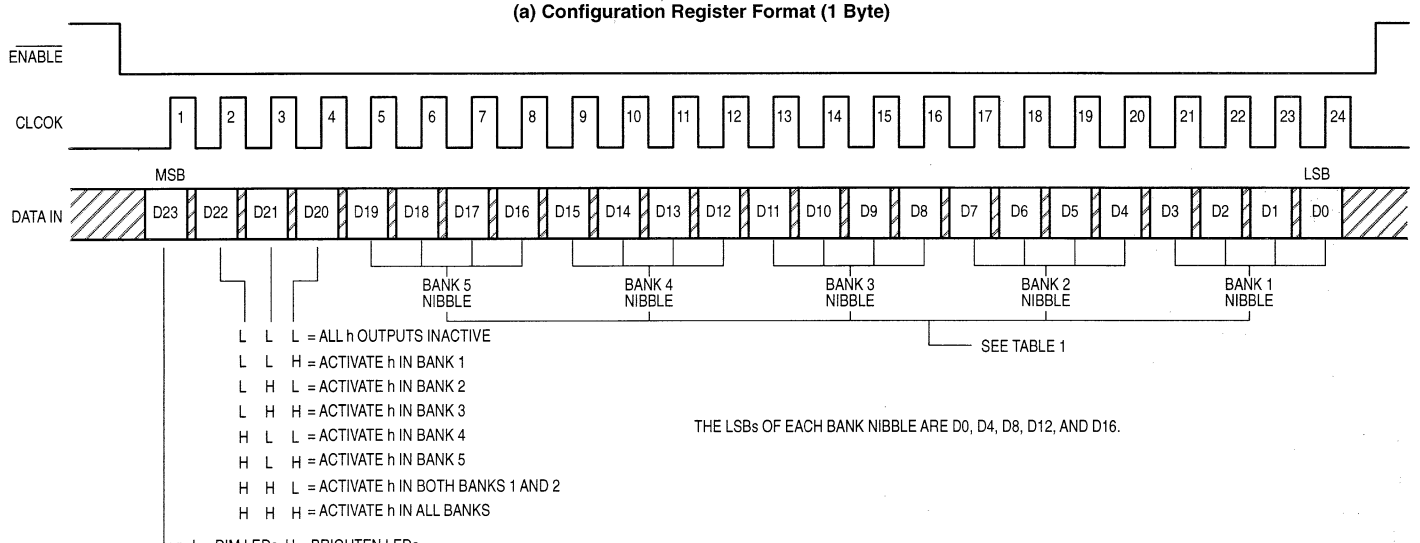
To adequately drive the LEDs, this voltage must be 4.5 to 6 volts with respect to V_{SS}.

The V_{DD} pin contains the Rx current component plus the chip's current drain. In the low–power mode, the current mirror and clock oscillator are turned off, thus significantly reducing the V_{DD} current, I_{DD}.



NOTE: The low–power (standby) mode places the device in a static state, thus eliminating EMI and mux switching noise. Therefore, during precision analog measurements, the low–power mode could be invoked by a system's MCU. Also, the low–power mode blanks the display, and could be used to flash the LEDs on and off.

(a) Configuration Register Format (1 Byte)



THE LSBs OF EACH BANK NIBBLE ARE D0, D4, D8, D12, AND D16.

(b) Display Register Format (3 Bytes)

NOTE: L = Low Voltage Level (Logic 0), H = High Voltage Level (Logic 1)

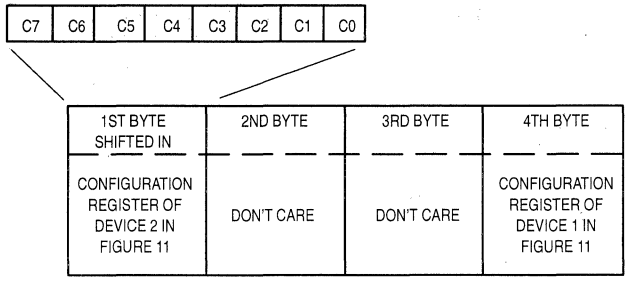
Figure 7. Timing Diagrams for Non–Cascaded Devices

Table 1. Triple–Mode Segment Decoder Function Table

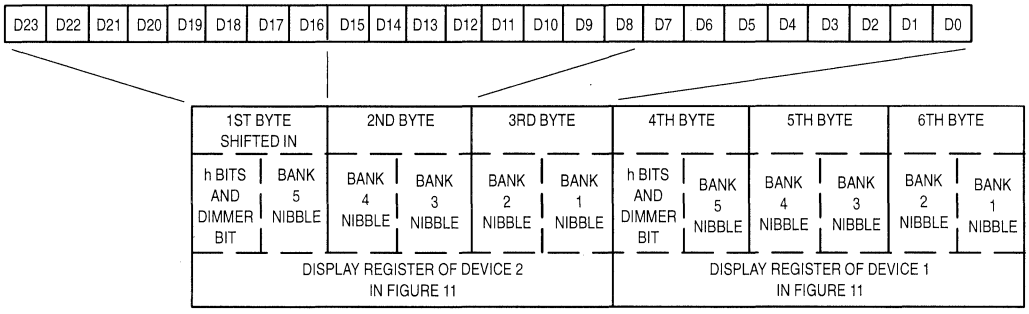
Bank Nibble Value		7–Segment Display Characters		Lamp Conditions			
				No Decode (1) (Invoked via Bits C1 to C7)			
Hexadecimal	Binary MSB LSB	Hex Decode (Invoked via Bits C1 to C5)	Special Decode (Invoked via Bits C1 to C7)	d	c	b	a
$0	L L L L	0					
$1	L L L H	1	c				on
$2	L L H L	2	H			on	
$3	L L H H	3	h			on	on
$4	L H L L	4	J		on		
$5	L H L H	5 (2)	L		on		on
$6	L H H L	6	n		on	on	
$7	L H H H	7	o		on	on	on
$8	H L L L	8 (3)	P	on			
$9	H L L H	9 (4)	r	on			on
$A	H L H L	A	U	on		on	
$B	H L H H	b	u	on		on	on
$C	H H L L	C	y	on	on		
$D	H H L H	d	-	on	on		on
$E	H H H L	E	_	on	on	on	
$F	H H H H	F	°	on	on	on	on

NOTES:

1. In the *No Decode* mode, outputs e, f, and g are unused and are all forced inactive (low). Output h decoding is unaffected, i.e., unchanged from the other modes. The *No Decode* mode is used for three purposes:
   a. Individually controlling lamps.
   b. Controlling a half digit with sign.
   c. Controlling annunciators - examples: AM, PM, UHF, kV, mm Hg.
2. Can be used as capital S.
3. Can be used as capital B.
4. Can be used as small g.



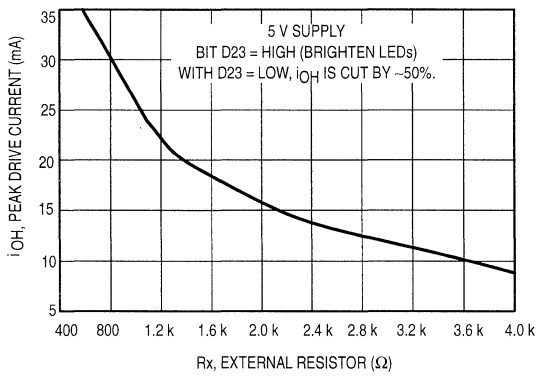
(a) Configuration Registers



(b) Display Registers

NOTE: $\overline{\text{ENABLE}}$ (which initially must be inactive high) is kept active–low during the entire 4–byte configuration transfer or 6–byte display transfer. When $\overline{\text{ENABLE}}$ is brought back high, either a 4– or 6–byte transfer occurs in the cascaded devices, depending on the number of bytes in the transfer.

Figure 8. Bit Stream Formats for Two Devices Cascaded



NOTE: Drive current tolerance is approximately ± 15%.

Figure 9. a through h Nominal Current per Output versus Rx

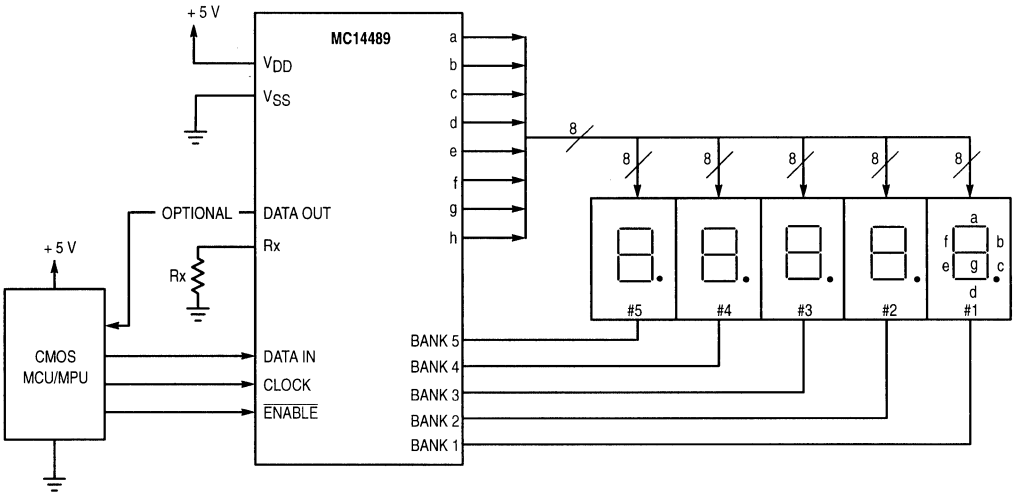


Figure 10. Non–Cascaded Application Example: 5 Character Common Cathode LED Display with Two Intensities as Controlled via Serial Port

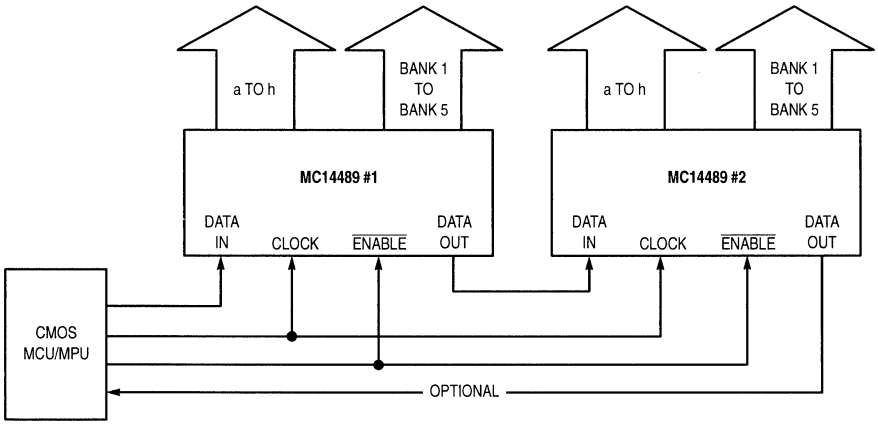
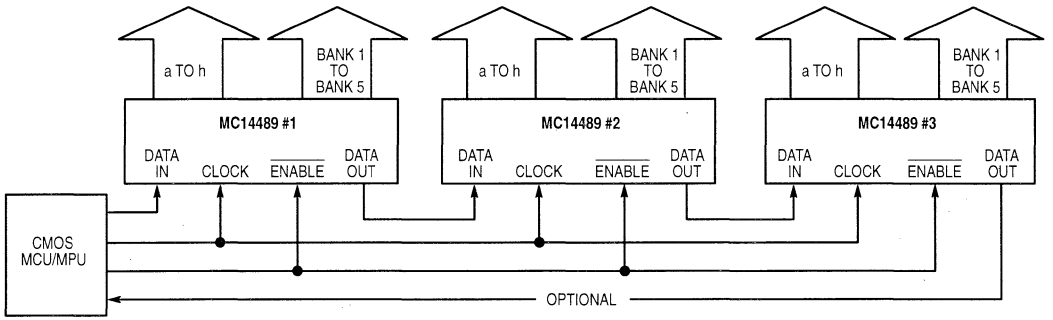
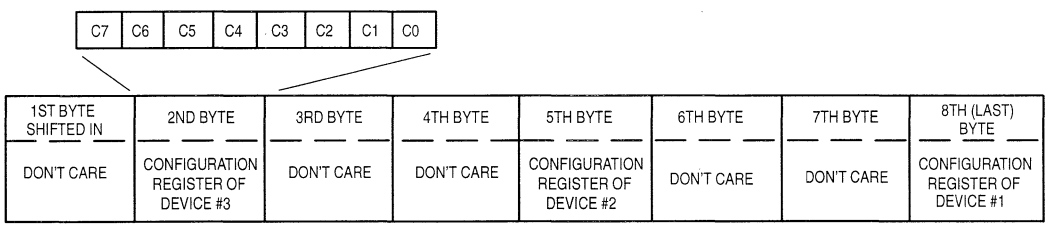


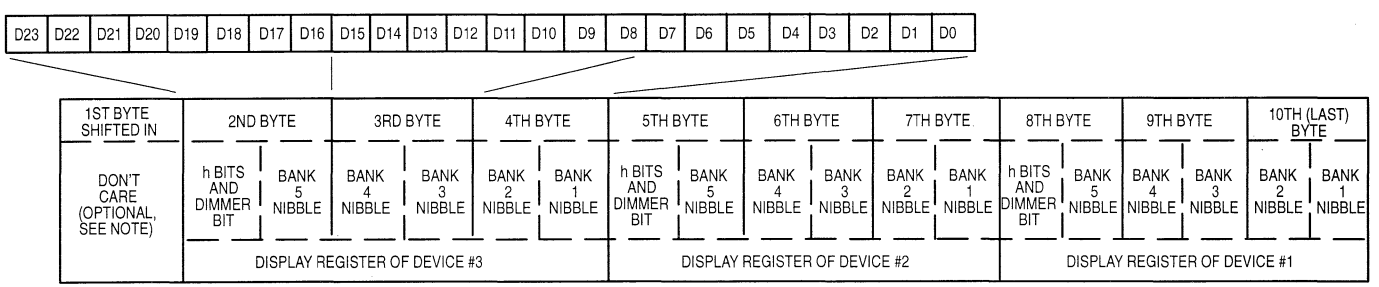
Figure 11. Cascading Two Devices



(a) Cascading Three Devices



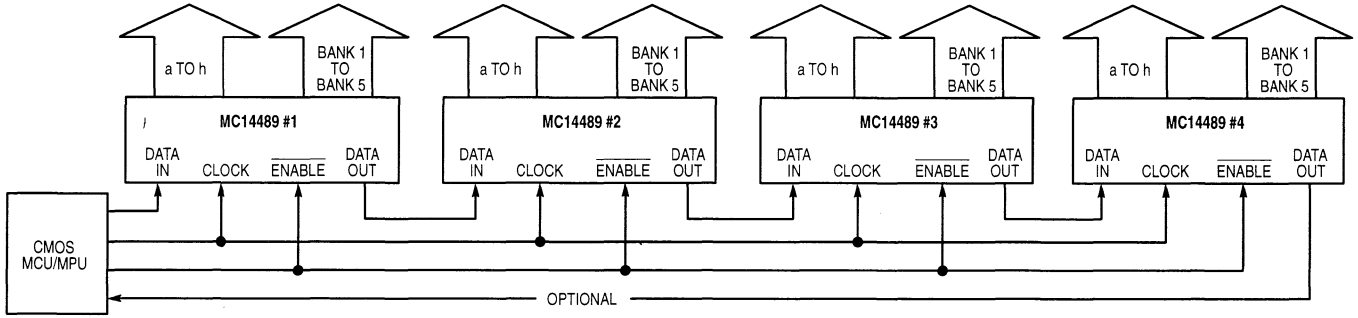
(b) Configuration Registers



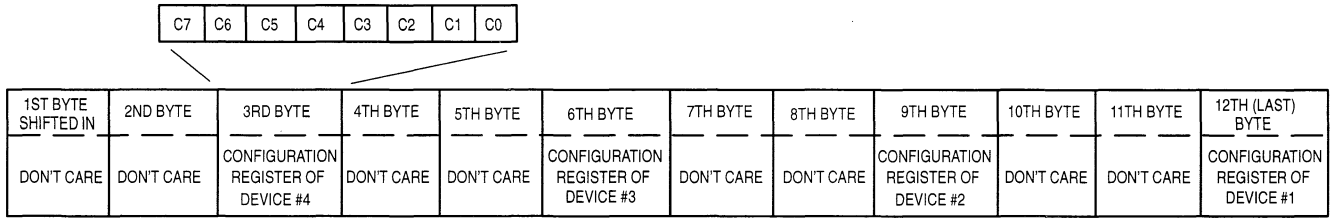
(c) Display Registers

Figure 12. Bit Stream Formats for Three Devices Cascaded

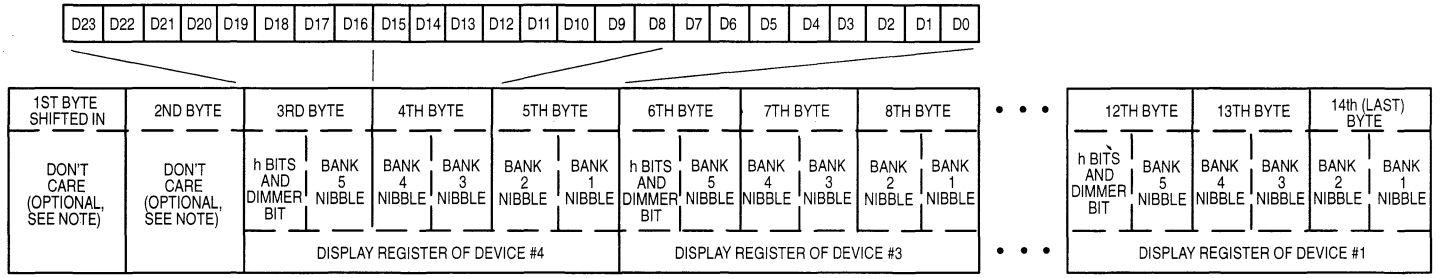
NOTE: When the leading "don't care" bytes are included, $\overline{\text{ENABLE}}$ (which initially must be inactive high) is kept active–low during the entire 8–byte configuration transfer or 10–byte display transfer. When ENABLE is brought back high, either an 8– or 10–byte transfer occurs in the cascaded devices. Alternatively, when updating the display registers, the one "don't care" byte can be eliminated as follows: (1) take $\overline{\text{ENABLE}}$ active low, (2) transfer 6 bytes, (3) pulse $\overline{\text{ENABLE}}$ inactive high, see t_w(H) spec, (4) transfer last 3 bytes, and (5) take $\overline{\text{ENABLE}}$ inactive high.



(a) Cascading Four Devices



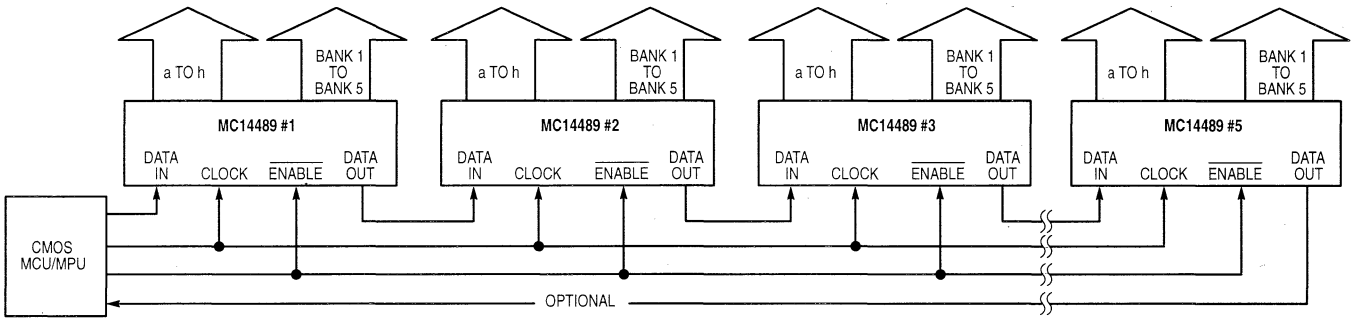
(b) Configuration Registers



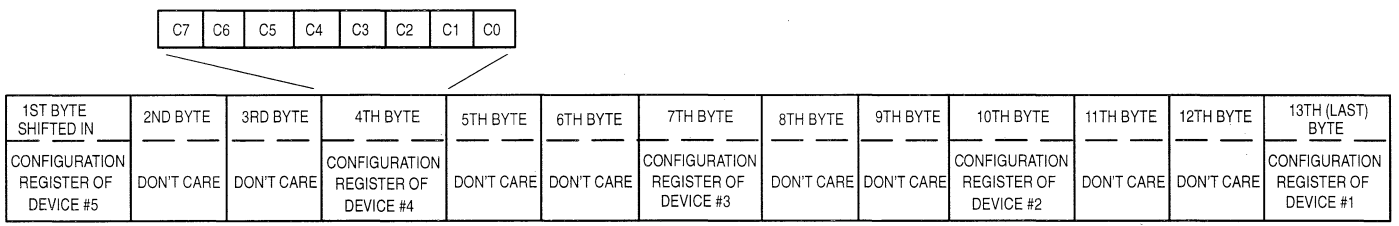
(c) Display Registers

Figure 13. Bit Stream Formats for Four Devices Cascaded

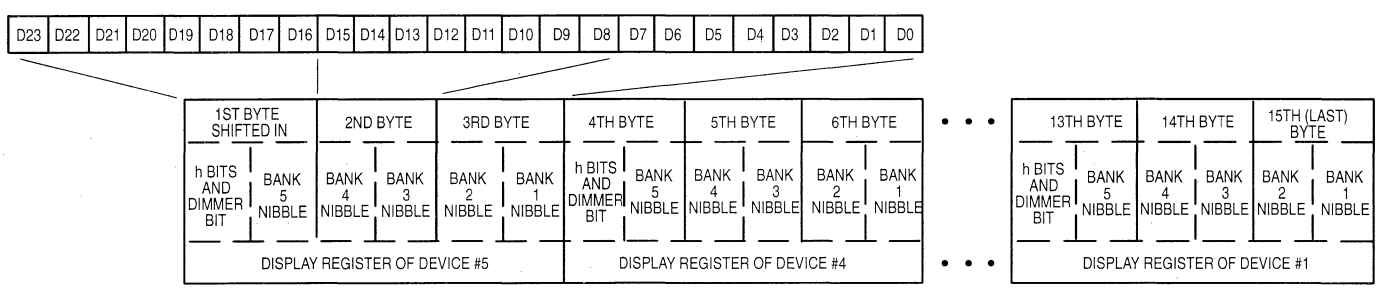
NOTE: When the leading "don't care" bytes are included, $\overline{\text{ENABLE}}$ (which initially must be inactive high) is kept active–low during the entire 12–byte configuration transfer or 14–byte display transfer. When ENABLE is brought back high, either a 12– or 14–byte transfer occurs in the cascaded devices. Alternatively, when updating the display registers, the two "don't care" bytes can be eliminated as follows: (1) take $\overline{\text{ENABLE}}$ active low, (2) transfer 6 bytes, (3) pulse $\overline{\text{ENABLE}}$ inactive high, see $t_W(H)$ spec, (4) transfer last 6 bytes, and (5) take $\overline{\text{ENABLE}}$ inactive high.



(a) Cascading Five Devices



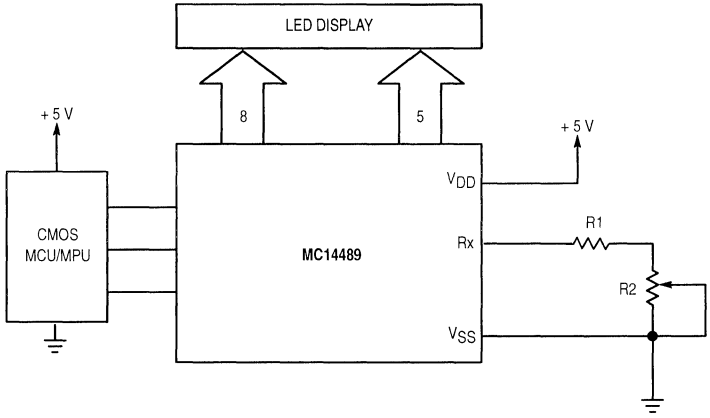
(b) Configuration Registers



(c) Display Registers

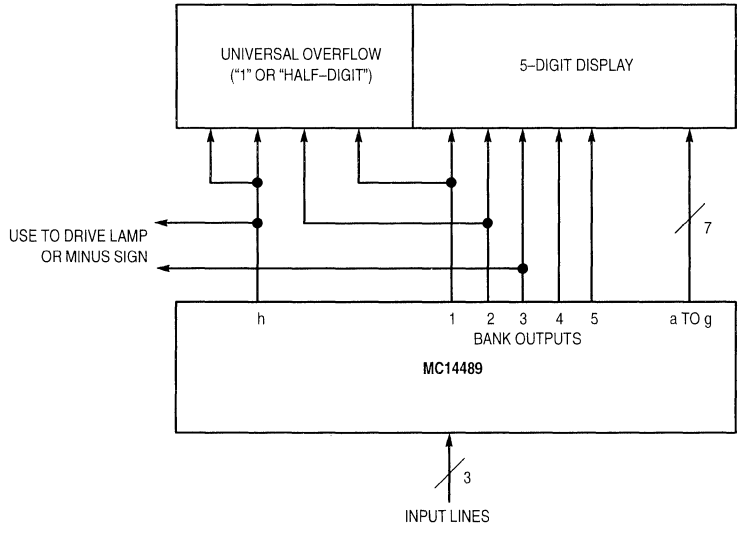
NOTE: $\overline{\text{ENABLE}}$ (which initially must be inactive high) is kept active–low during the entire 13–byte configuration transfer or 15–byte display transfer. When $\overline{\text{ENABLE}}$ is brought back high, either a 13– or 15–byte transfer occurs in the cascaded devices, depending on the number of bytes in the transfer.

Figure 14. Bit Stream Formats for Five Devices Cascaded



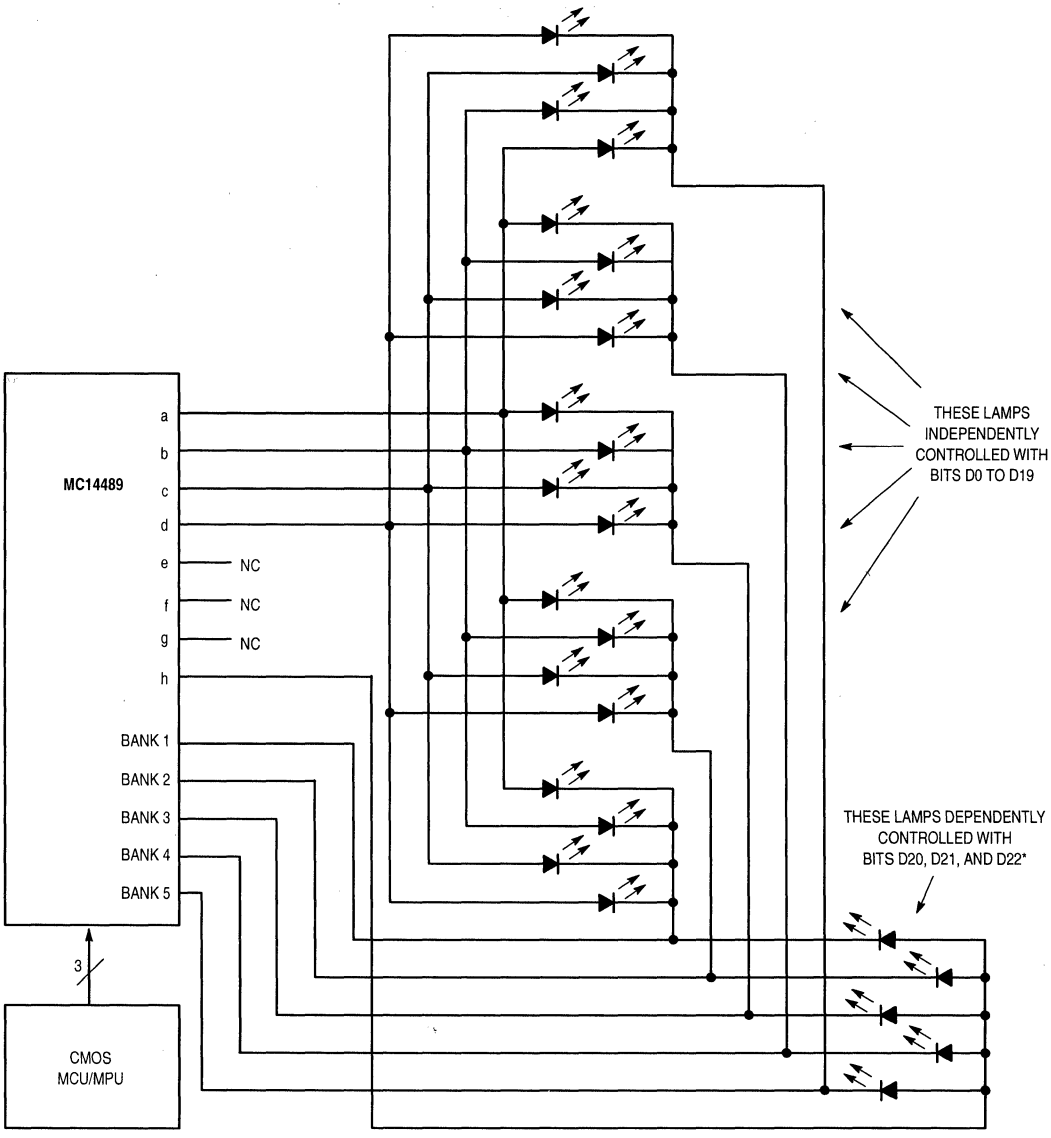
NOTE: R1 limits the maximum current to avoid damaging the display and/or the MC14489 due to overheating. See the Thermal Considerations section. An 1/8 watt resistor may be used for R1. R2 is a 1 kΩ or 5 kΩ potentiometer (≥ 1/8 watt). R2 may be a light–sensitive resistor.

Figure 15. Common–Cathode LED Display with Dial–Adjusted Brightness



NOTE: A Universal Overflow pins out all anodes and cathodes.

Figure 16. Driving 5 1/2 Digits



* If required, this group of lamps can be independently controlled. To accomplish independent control, only connect lamps to BANK 1 and BANK 2 for output h (two lamps). Then, use bits D20, D21, and D22 for control of these two lamps.

Figure 17. 25–Lamp Application

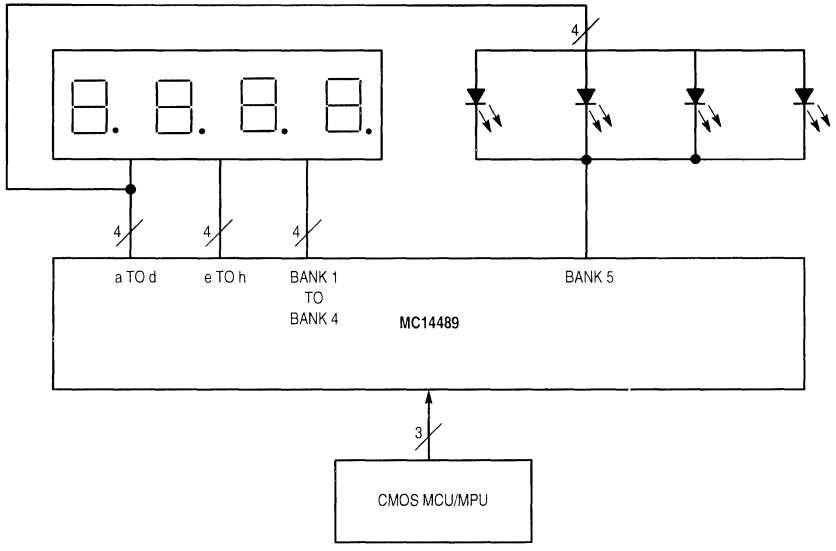


Figure 18. 4–Digit Display Plus Decimals with Four Annunciators or 4–1/2–Digit Display Plus Sign

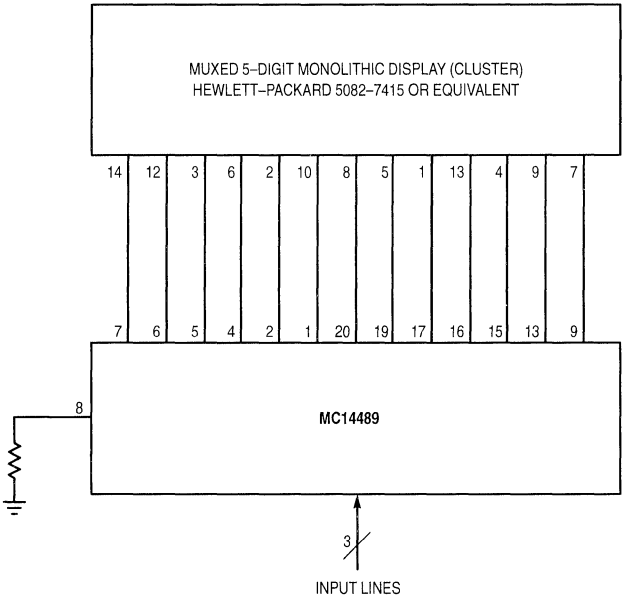


Figure 19. Compact Display System with Three Components

The MC14489 is designed to operate with a *chip–junction* temperature (T_J) ranging from – 40 to 130°C, as indicated in the electrical characteristics tables. The *ambient* operating temperature range (T_A) is dependent on $R_{\theta JA}$, the internal chip current, how many anode drivers are used, the number of bank drivers used, the drive current, and how the package is cooled. The maximum ratings table gives the thermal resistance, junction–to–ambient, of the MC14489 mounted on a pc board using natural convection to be 90°C per watt for the plastic DIP. The SOG thermal resistance is 100°C per watt.

The following general equation (1) is used to determine the power dissipated by the MC14489.

$$P_T = P_D + P_I \quad (1)$$

where

P_T = Total power dissipation of the MC14489
P_D = Power dissipated in the driver circuitry (mW)
P_I = Power dissipated by the internal chip circuitry (mW)

The equations for the two terms of the general equation are:

$$P_D = (i_{OH})\ (N)(V_{DD} - V_{LED})(B/5) \quad (2)$$

$$P_I = (1.5\ mA)(V_{DD}) + I_{Rx}(V_{DD} - I_{Rx}Rx) \quad (3)$$

where

i_{OH} = Peak anode driver current (mA)
I_{Rx} = i_{OH} /10, with i_{OH} = the peak anode driver current (mA) when the dimmer bit is high
N = Number of anode drivers used
B = Number of bank drivers used
Rx = External resistor value (kΩ)
V_{DD} = Maximum supply voltage, referenced to V_{SS} (volts)
V_{LED} = Minimum anticipated voltage drop across the LED
1.5 mA = Operating supply current of the MC14489

The following two examples show how to calculate the maximum allowable ambient temperature.

Worst–Case Analysis Example 1:

5–digit display with decimals (5 banks and 8 anode drivers)
DIP without heat sink on PC board
i_{OH} = 20 mA max
V_{LED} = 1.8 V min
V_{DD} = 5.25 max

$P_D = (20)(8)(5.25 - 1.8)(5/5) = 552$ mW Ref. (2)

$P_I = (1.5)(5.25) + 2[5.25 - 2(2)] = 10$ mW Ref. (3)

Therefore, $P_T = 552 + 10 = 562$ mW Ref. (1)

and $\Delta T_{chip} = R_{\theta JA}P_T = (90°C/W)(0.562) = 51°C$

Finally, the maximum allowable
$T_A = T_J max - \Delta T_{chip} = 130 - 51 = 79°C$

That is, if $T_A = 79°C$, the maximum junction temperature is 130°C. The chip's average temperature for this example is lower than 130°C because all segments are usually not illuminated simultaneously for an indefinite period.

Worst–Case Analysis Example 2:

16 lamps (4 banks and 4 anode drivers)
SOG without heat sink on PC board
i_{OH} = 30 mA max
V_{LED} = 1.8 V min
V_{DD} = 5.5 max

$P_D = (30)(4)(5.5 - 1.8)(4/5) = 355$ mW Ref. (2)

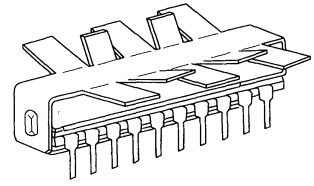
$P_I = (1.5)(5.5) + 3[5.5 - 3(1.0)] = 16$ mW Ref. (3)

Therefore, $P_T = 355 + 16 = 371$ mW Ref. (1)

and $\Delta T_{chip} = R_{\theta JA}P_T = (100°C/W)(0.371) = 37°C$

Finally, the maximum allowable
$T_A = T_J max - \Delta T_{chip} = 130 - 37 = 93°C$

To extend the allowable ambient temperature range or to reduce T_J, which extends chip life, a heat sink such as shown in Figure 20 can be used in high–current applications. Alternatively, heat–spreader techniques can be used on the PC board, such as running a wide trace under the MC14489 and using thermal paste. Wide, radial traces from the MC14489 leads also act as heat spreaders.



AAVID #5804 or equivalent
(Tel. 603/524–4443, FAX 603/528–1478)
Motorola cannot recommend one supplier over another and in no way suggests that this is the only heat sink supplier.

Figure 20. Heat Sink

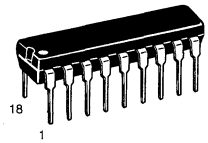
Table 2. LED Lamp and Common–Cathode Display Manufacturers

Supplier	Contact Information
QT Optoelectronics	Phone: (800) 533–6786 FAX: (214) 447–0784
Hewlett–Packard (HP), Components Group	Contact your local HP Components Sales Office
Industrial Electronic Engineers (IEE), Component Products Div.	Phone: (818) 787–0311 FAX: (818) 901–9046
Purdy Electronics Corp., AND Product Line	Phone: (408) 523–8210 FAX: (408) 733–1287

NOTE: Motorola cannot recommend one supplier over another and in no way suggests that this is a complete listing of LED suppliers.

MC14497

PCM Remote Control Transmitter



P SUFFIX
PLASTIC DIP
CASE 707

ORDERING INFORMATION

MC14497P	Plastic DIP

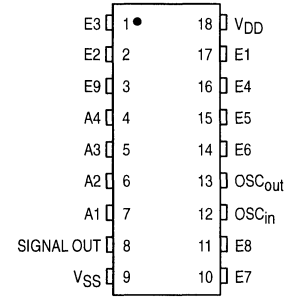
2

The MC14497 is a PCM remote control transmitter realized in CMOS technology. Using a dual–single (FSK/AM) frequency bi–phase modulation, the transmitter is designed to work with the MC3373 receiver. Information on the MC3373 can be found in the Motorola *Linear* and *Interface Integrated Circuits* book (DL128/D).

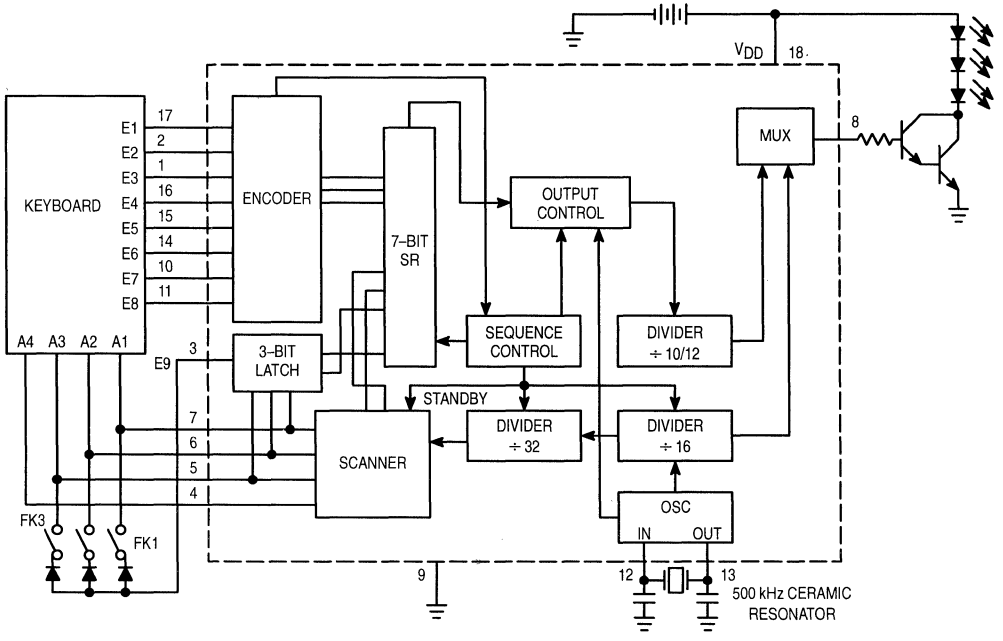
There is not a decoder device which is compatible with the MC14497. Typically, the decoding resides in MCU software.

- Both FSK/AM Modulation Selectable
- 62 Channels (Up to 62 Keys)
- Reference Oscillator Controlled by Inexpensive Ceramic Resonator: Maximum Frequency = 500 kHz
- Very Low Duty Cycle
- Very Low Standby Current: 50 μA Maximum
- Infrared Transmission
- Selectable Start–Bit Polarity (AM Only)
- Shifted Key Mode Available
- Wide Operating Voltage Range: 4 to 10 V
- See Application Notes AN1016 and AN1203

PIN ASSIGNMENT



BLOCK DIAGRAM



SAME AS IN DL136/D R3

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Parameter	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	− 0.5 to + 18	V
Input Voltage, All Inputs	V_{in}	− 0.5 to V_{DD} + 0.5	V
DC Current Drain per Pin	I	10	mA
Operating Temperature Range	T_A	− 40 to + 85	°C
Storage Temperature Range	T_{stg}	− 65 to + 150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

ELECTRICAL CHARACTERISTICS (T_A = 0 to 70°C; all Voltages Referenced to V_{SS})

Characteristic		Symbol	V_{DD}	Min	Max	Unit
Supply Voltage		V_{DD}	—	4.0	10.0	V
Supply Current		I_{DD}				
Idle			10	—	50	µA
Operation			10	—	5	mA
Output Current — Signal						µA
V_{OH} = 3.0 V	Source	I_{OH}	4	− 900	—	
V_{OL} = 0.5 V	Sink	I_{OL}	4	120	—	
Output Current — Scanner						µA
V_{OH} = 3.0 V	Source	I_{OH}	4	− 30	—	
V_{OL} = 0.5 V	Sink	I_{OL}	4	245	—	
Output Current — Oscillator						µA
V_{OH} = 3.0 V	Source	I_{OH}	4	− 300	—	
V_{OL} = 0.5 V	Sink	I_{OL}	4	245	—	
Input Current — Oscillator		I_{in}				µA
Operation			10	± 2	± 80	
Idle, V_{IL} = 0.5 V			4	30	—	
Input Current — Encoder		I_{in}				µA
V_{IH} = 9.0 V			10	− 15	—	
V_{IL} = 0.5 V			4	—	− 60	
Input Voltage — Encoder		V_{IH}	10	9	—	V
		V_{IL}	10	—	1.2	
		V_{IH}	4	3	—	
		V_{IL}	4	—	1.0	

CIRCUIT OPERATION

The transmitter sends a 6–bit, labelled A (LSB) to F (MSB), binary code giving a total of 64 possible combinations or code words. All of these channels are user selectable, except the last two (where channel 63 is not sent while channel 62 is automatically sent by the transmitter at the end of each transmission as an "End of Transmission" code).

In either mode, FSK or AM, the transmitted signal is in the form of a bi–phase pulse code modulation (PCM) signal. The AM coding is shown in Figure 1.

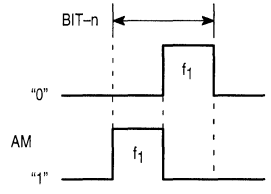


Figure 1. AM Coding

In the AM mode, f_1 is a train of pulses at the modulating frequency of 31.25 kHz for a reference frequency of 500 kHz.

In the FSK mode, two modulating frequencies are used as shown in Figure 2.

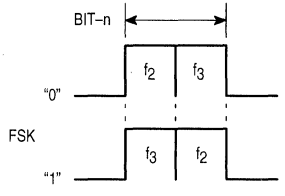


Figure 2. FSK Coding

In this mode, f_3 is 50 kHz and f_2 is 41.66 kHz for a reference frequency of 500 kHz.

The keyboard can be a simple switch matrix using no external diodes, connected to the four scanner inputs (A1 – A4) and the eight row input (E1 – E8). Under these conditions, only the first 32 code words are available since bit–F is always at logical 0. However, a simple 2–pole changeover switch, in the manner of a typewriter "shift" key (switch FK3 in the Block Diagram) can be used to change the polarity of bit–F to give access to the next full set of 32 instructions.

An alternative method of accessing more than 32 instructions is by the use of external diodes between the address inputs (see Figure 3). These have the effect of producing "phantom" address inputs by pulling two inputs low at the same time, which causes bit–F to go high (i.e., to logical 1). By interconnecting only certain address inputs it is possible to make an intermediate keyboard with between 32 and 64 keys.

The other two switches in the Block Diagram (FK1 and FK2) change the modulation mode. Closing FK1 changes the modulation from FSK to AM and the start–bit polarity. Closing FK2 changes the start–bit to a logical 0.

The full range of options available is illustrated in Table 1.

Table 1.

	Start Bit	Modulation	Bit–F	Channels
E9 = Open	1	FSK	0	0 – 31
E9 = A1 (FK1)	1	AM	0	0 – 31
E9 = A2 (FK2)	0	FSK	0	0 – 31*
E9 = A3 (FK3)	1	FSK	1	32 – 61
E9 = A1 • A2	0	AM	0	0 – 31
E9 = A1 • A3	1	AM	1	32 – 61
E9 = A2 • A3	0	FSK	1	32 – 61*
E9 = A1 • A2 • A3	0	AM	1	32 – 61

* Not allowed.

One of the transmitter's major features is its low power consumption (in the order of 10 μA in the idle state). For this reason, the battery is perpetually in circuit. It has in fact been found that a light discharge current is beneficial to battery life.

In its active state, the transmitter efficiency is increased by the use of a low duty cycle which is less than 2.5% for the modulating pulse trains.

While no key is pressed, the circuit is in its idle state and the reference oscillator is stopped. Also, the eight address input lines are held high through internal pull–up resistors.

As soon as a key is pressed, this takes the appropriate address line low, signaling to the circuit that a key has been selected. The oscillator is now enabled. If the key is released before the code word has been sent, the circuit returns to its idle state. To account for accidental activation of the transmitter, the circuit has a built–in reactive time of approximately 20 ms, which also overcomes contact bounce. After this delay, the code word will be sent and repeated at 90 ms intervals for as long as the key is pressed. As soon as the key is released, the circuit automatically sends channel 62, the "End of Transmission" (EOT) code. The transmitter then returns to its idle state.

The differences between the two modulation modes are illustrated in Figure 4. However, it should be noted that in the AM mode, each transmitted word is preceded by a burst of pulses lasting 512 μs. This is used to set up the AGC loop in the receiver's preamp. In the FSK mode, the first frequency of the first bit is extended by 1.5 ms and the AGC burst is suppressed. In either mode, it is assumed that the normal start–bit is present.

PIN DESCRIPTIONS

E1 – E8
Row Inputs (Pins 1, 2, 10, 11, 14, 15, 16, 17)

Under idle conditions, these inputs are held high by internal pull–up resistors. As soon as a key is pressed, a logical 0 on that particular line signals to the circuit that a key has been selected. After a delay of 20 ms, the internal register is loaded with the code word for the key selected.

E9
Row Input (Pin 3)

This is a special programming input and when connected to the appropriate scanner output via a diode, it will modify the transmitted output according to Table NO TAG.

In Table NO TAG, the figures in brackets (FK1, etc.) refer to the switches shown in the Block Diagram and Figure 3. If only one option is required, the diode may be omitted. The connections shown in Table NO TAG may be made in any combination.

Although E9 is a row input, forcing this line low will not activate the circuit.

A1 – A4
Scanner Outputs (Pins 4 – 7)

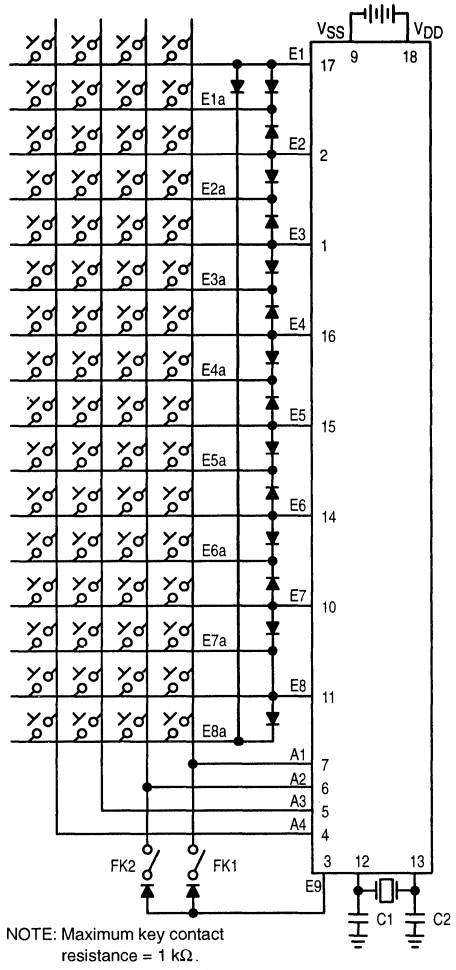
Under idle conditions, these outputs are held low, logical 0. When a key is pressed, the circuit is activated and the oscillator will start and release the outputs (see Figure 5).

OSC_{in}, OSC_{out}
Oscillator Input and Oscillator Output (Pins 12, 13)

These pins are designed to operate with a 500 kHz ceramic resonator or a tune LC circuit. It is important that a ceramic resonator and **not a filter** be used here, as the oscillator frequency cannot be guaranteed if a ceramic filter is used.

SIGNAL OUT
Signal Output (Pin 8)

This output provides the modulating signal ready to drive the modulation amplifier. If required, the transmitter can be used as a keyboard encoder for direct use with a receiver. In this case, the AM option is selected, the output inverted, and fed directly to the receiver's signal input pin.



NOTE: Maximum key contact resistance = 1 kΩ.

Figure 3. 64–Key Keyboard

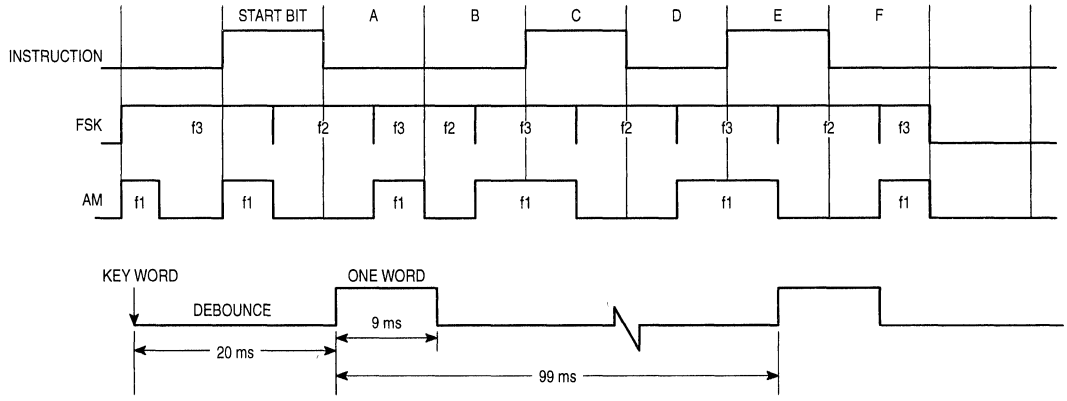


Figure 4. Transmitted Waveforms and Timing (Not Drawn to Scale)

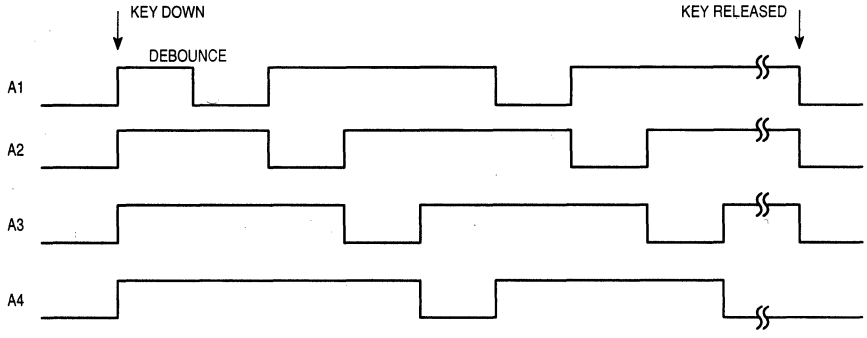
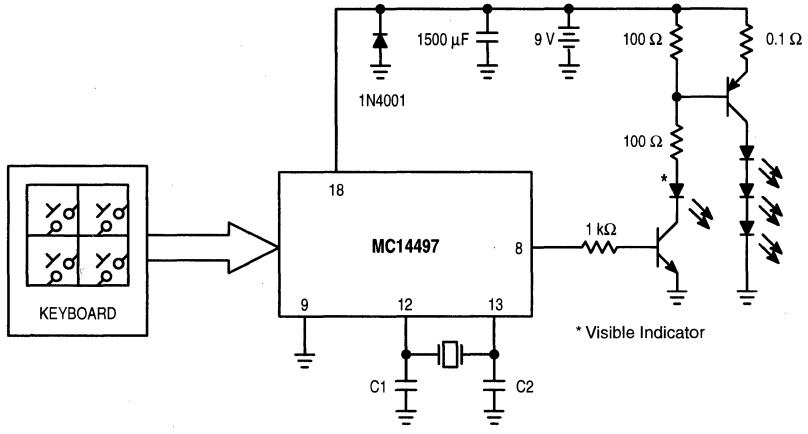


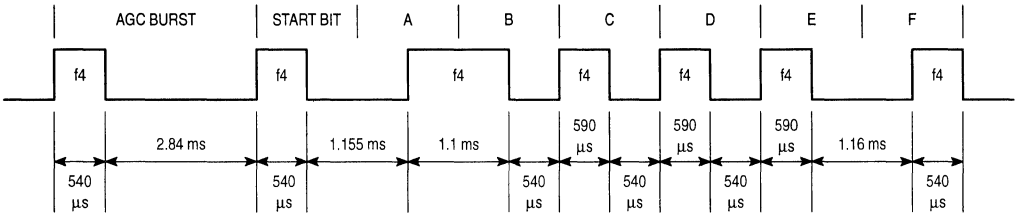
Figure 5. Scanner Output Timing Diagram



C1 and C2 are sized per the ceramic resonator supplier's recommendation.
Ceramic Resonator Suppliers:
1. Morgan Matrox, Inc., Bedford, OH, 216/232–8600
2. Radio Materials Co., Attica, IN, 317/762–2491

Motorola cannot recommend one supplier over another and in no way suggests that this is a complete listing of ceramic resonator suppliers.

Figure 6. Typical Application Circuit



NOTES:
1. f4 = 28.4 kHz.
2. Indicated time durations are approximated.

Figure 7. AM Mode Transmitted Wavetrain with 455 kHz Oscillator

Table 2. Transmitted Codes

	Code Word						Keyboard			Code Word							Keyboard	
Channel	F	E	D	C	B	A	In	Out	Channel	F	E	D	C	B	A	In	Out
0	0	0	0	0	0	0	E8	A4	32	1	0	0	0	0	0	E8a	A4
1				0	0	1	E1	A4	33				0	0	1	E1a	A4
2				0	1	0	E2	A4	34				0	1	0	E2a	A4
3				0	1	1	E3	A4	35				0	1	1	E3a	A4
4				1	0	0	E4	A4	36				1	0	0	E4a	A4
5				1	0	1	E5	A4	37				1	0	1	E5a	A4
6				1	1	0	E6	A4	38				1	1	0	E6a	A4
7				1	1	1	E7	A4	39				1	1	1	E7a	A4
8	0	0	1	0	0	0	E8	A1	40	1	0	1	0	0	0	E8a	A1
9				0	0	1	E1	A1	41				0	0	1	E1a	A1
10				0	1	0	E2	A1	42				0	1	0	E2a	A1
11				0	1	1	E3	A1	43				0	1	1	E3a	A1
12				1	0	0	E4	A1	44				1	0	0	E4a	A1
13				1	0	1	E5	A1	45				1	0	1	E5a	A1
14				1	1	0	E6	A1	46				1	1	0	E6a	A1
15				1	1	1	E7	A1	47				1	1	1	E7a	A1
16	0	1	0	0	0	0	E8	A3	48	1	1	0	0	0	0	E8a	A3
17				0	0	1	E1	A3	49				0	0	1	E1a	A3
18				0	1	0	E2	A3	50				0	1	0	E2a	A3
19				0	1	1	E3	A3	51				0	1	1	E3a	A3
20				1	0	0	E4	A3	52				1	0	0	E4a	A3
21				1	0	1	E5	A3	53				1	0	1	E5a	A3
22				1	1	0	E6	A3	54				1	1	0	E6a	A3
23				1	1	1	E7	A3	55				1	1	1	E7a	A3
24	0	1	1	0	0	0	E8	A2	56	1	1	1	0	0	0	E8a	A2
25				0	0	1	E1	A2	57				0	0	1	E1a	A2
26				0	1	0	E2	A2	58				0	1	0	E2a	A2
27				0	1	1	E3	A2	59				0	1	1	E3a	A2
28				1	0	0	E4	A2	60				1	0	0	E4a	A2
29				1	0	1	E5	A2	61				1	0	1	E5a	A2
30				1	1	0	E6	A2	62				1	1	0	E6a	A2
31	0	1	1	1	1	1	E7	A2	Not Transmitted	1	1	1	1	1	1	E7a	A2

NOTE: Although the "a" suffix applies to a phantom input when using a keyboard with up to 64 keys, the coding is identical with a 32–key keyboard when switch FK3 is closed.

MC14499

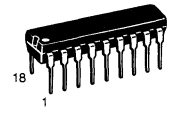
7-Segment LED Display Decoder/Driver with Serial Interface

CMOS

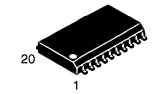
2

The MC14499 is a 7–segment alphanumeric LED decoder/driver with a serial interface port to provide communication with CMOS microprocessors and microcomputers. This device features NPN output drivers which allow interfacing to common cathode LED displays through external series resistors.

- High–Current Segment Drivers On–Chip
- CMOS MPU compatible Input Levels
- Wide Operating Voltage Range: 4.5 to 6.5 V
- Operating Temperature Range: 0 to 70°C
- Drives Four Characters with Decimal Points
- Also See MC14489



P SUFFIX
PLASTIC DIP
CASE 707

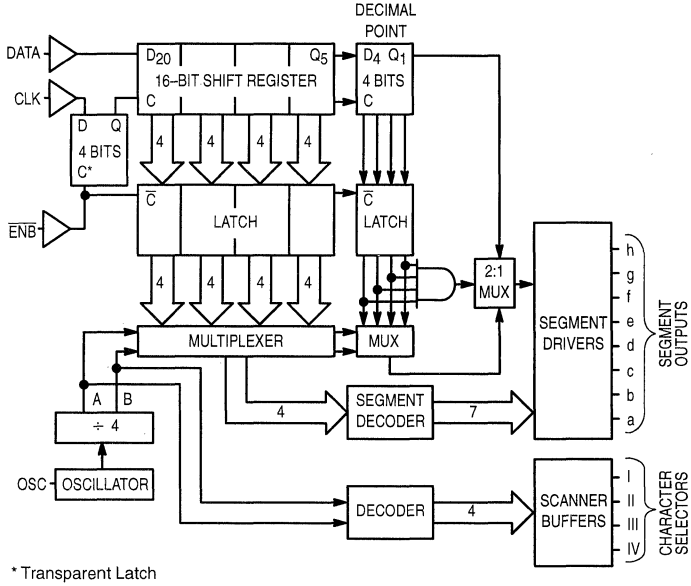


DW SUFFIX
SOG PACKAGE
CASE 751D

ORDERING INFORMATION

MC14499P	Plastic DIP
MC14499DW	SOG Package

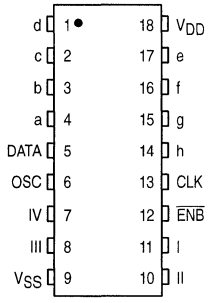
BLOCK DIAGRAM



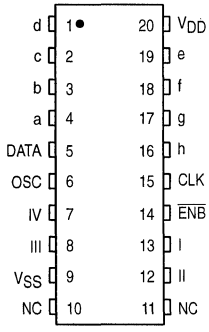
* Transparent Latch

PIN ASSIGNMENTS

PLASTIC DIP



SOG PACKAGE



NC = NO CONNECTION

SAME AS IN DL130/D R1

MAXIMUM RATINGS* (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	– 0.5 to + 7	V
Input Voltage, All Inputs	V_{in}	– 0.5 to V_{DD} + 0.5	V
Storage Temperature Range	T_{stg}	– 65 to + 150	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics table or Circuit Operation section.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation, it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

ELECTRICAL CHARACTERISTICS (V_{DD} = 4.5 to 6.5 V)

Characteristic	Symbol	0°C		25°C		70°C		Unit
		Min	Max	Min	Max	Min	Max	
Serial Port Input Voltage '0' Level	V_{IL}	—	0.3 x V_{DD}	—	0.3 x V_{DD}	—	0.3 x V_{DD}	V
'1' Level	V_{IH}	0.7 x V_{DD}	—	0.7 x V_{DD}	—	0.7 x V_{DD}	—	
Serial Port Input Current (V_{in} = 0 to V_{DD})	I_{in}	—	± 0.1	—	± 0.1	—	± 1.0	µA
Oscillator Input Voltage '0' Level	V_{IL}	—	0.25 x V_{DD}	—	0.25 x V_{DD}	—	0.2 x V_{DD}	V
'1' Level	V_{IH}	0.75 x V_{DD}	—	0.75 x V_{DD}	—	0.8 x V_{DD}	—	
Oscillator Input Current V_{OSC} = 0	I_{IL}	—	100	30	80	10	—	µA
V_{OSC} = V_{DD}	I_{IH}	—	– 100	– 30	– 80	– 10	—	
Segment Driver Voltage Below V_{DD}	ΔV_{OH}							V
I_{out} = 50 mA		—	1.1	—	1.0	—	1.1	
I_{out} = 10 mA		—	0.8	—	0.75	—	0.8	
Segment Driver Off Leakage V_{out} = 0	I_{OZ}	—	100	—	50	—	100	µA
Digit Drivers								mA
Source (On) V_{out} = 0.8 V	I_{OH}	6	—	5.5	—	4	—	
Sink (Off) V_{out} = 0.5 V	I_{OL}	– 0.2	—	– 0.2	—	– 0.1	—	
Supply Current (V_{in} = 0, I_{out} = 0, C_{OSC} = 0.015 µF	I_{DD}	—	1	—	1	—	1	mA
Maximum Power Dissipation	P_D	—	500	—	500	—	500	mW

SWITCHING CHARACTERISTICS (V_{DD} = 5 V ± 10%, T_A = 0 to 70°C)

Characteristic	Figure No.	Symbol	Min	Max	Unit
Clock High Time	2	t_{CH}	2	—	µs
Clock Low Time	2	t_{CL}	2	—	µs
Clock Rise Time	2	t_{CR}	—	2	µs
Clock Fall Time	2	t_{CF}	—	2	µs
Enable Lead Time	2	$t_{E\ LEAD}$	200	—	ns
Enable Lag Time	2	$t_{E\ LAG}$	200	—	ns
Data Set–Up Time	2	$t_{D\ SUP}$	200	—	ns
Data Hold Time	2	$t_{D\ HOLD}$	1	—	µs
Scanner Frequency*	4	$1/t_{SCAN}$	50	300	Hz
OSC/Digit Lead Time	4	t_{OD}	—	10	µs
OSC/Segment Lead Time	4	t_{OS}	—	10	µs
Digit Overlap	4	t_{OV}	—	5	µs

* Scanner Capacitance = 0.022 µF.

CIRCUIT OPERATION

The circuit accepts a 20–bit input, 16 bits for the four–digit display plus 4 bits for the decimal point — these latter four bits are optional.

The input sequence is the decimal point code followed by the four digits, as shown in Figure 1.

In order to enter data the enable input, $\overline{ENB}$, must be active low. The sample and shift are accomplished on the falling clock edge, see Figure 2. Data are loaded from the shift register to the latches when $\overline{ENB}$ goes high. While the shift register is being loaded, the previous data are stored in the latches.

If the decimal point is used, the system requires 20 clock pulses to load data; otherwise only 16 are required.

CASCADING

The circuit may be cascaded in the following manner.

If a 1111 word is loaded into the decimal point latch, the output of the shift register is switched to the decimal point driver, see Figure 3. Therefore, to cascade n four–digit display drivers, a set–up is used which loads the 1111 cascading word:

1. $\overline{ENB}$ = active low.
2. Load 20 bits, the first four bits being 1, with 20 clock pulses.
3. $\overline{ENB}$ = high, to load the latch.
4. Repeat steps 1 to 3 (n – 1) times.
5. (n x 20) bits can be loaded into n circuits, with 1111 as decimal point word to continue the cascading.

SCANNER

The scanner frequency is determined by an on–chip oscillator, which requires an external frequency–determining capacitor. The capacitor voltage varies between two trigger levels at the oscillator frequency.

An external oscillator signal can be used, within the recommended operating range of 200 to 800 Hz. For test purposes this frequency may be increased up to 10 kHz.

A divide by four counter provides four non–overlapping scanner waveforms corresponding to the four digits — see Figure 4.

SEGMENT DECODER

The code used in these matrix decoders is shown in Figure 5.

OUTPUT DRIVERS

There are two different drivers:

- The segment and decimal point drivers; these are NPN emitter followers with no current limiting devices.
- The digit output buffers; these are short–circuit protected CMOS devices.

A typical application circuit is shown in Figure 6.

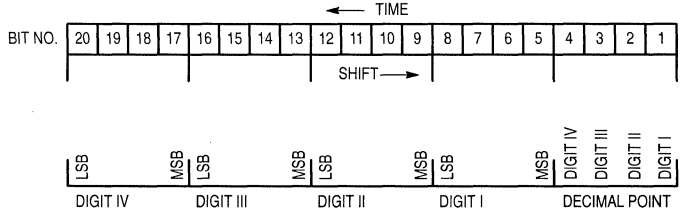


Figure 1. Input Sequence

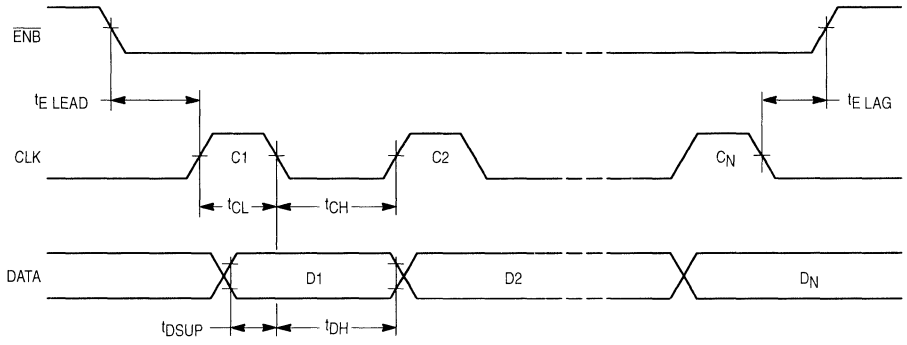


Figure 2a. Serial Input, Positive Clock

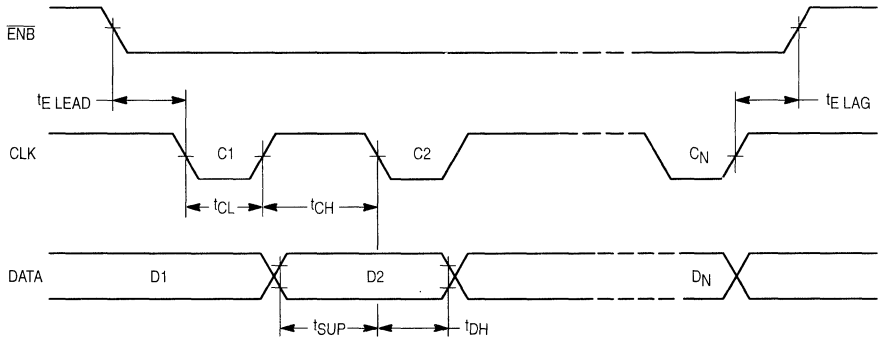


Figure 2b. Serial Input, Negative Clock

Figure 2. Serial Input

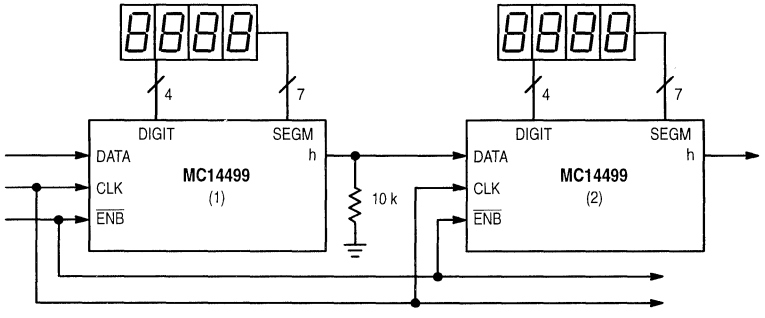


Figure 3. Cascading MC14499s

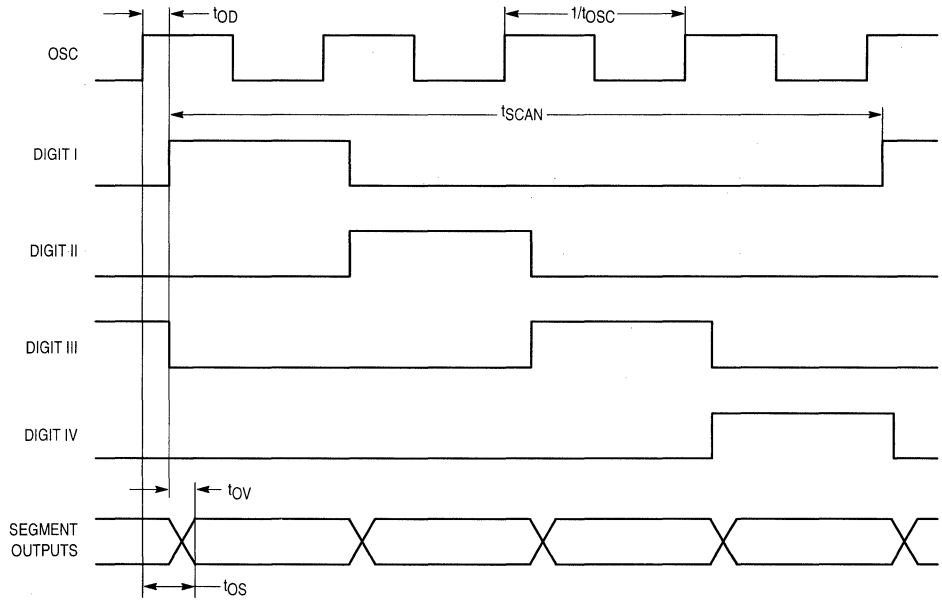


Figure 4. Scanner Waveforms

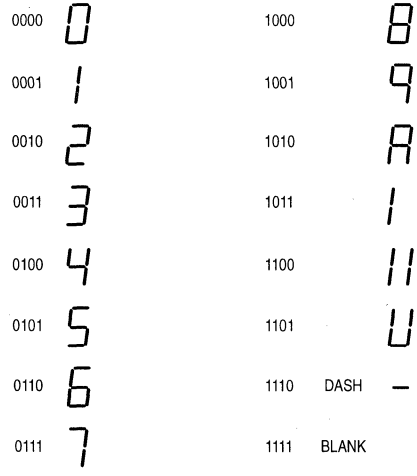


Figure 5. Segment Code

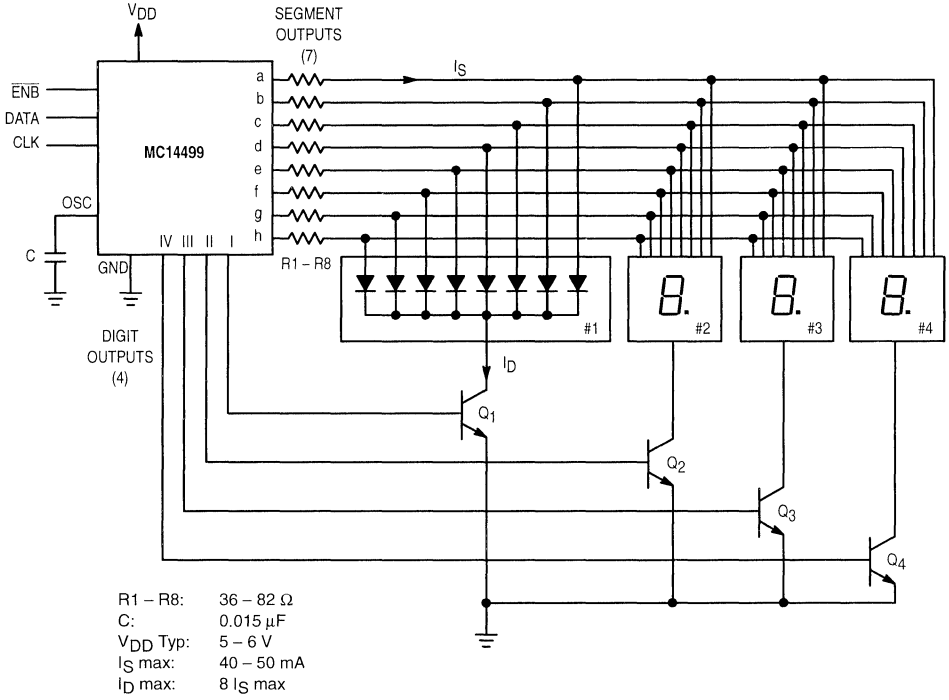


Figure 6. Application Example

MC33110

Low Voltage Compander

2

The MC33110 contains two variable gain circuits configured for compressing and expanding the dynamic range of an audio signal. One circuit is configured as an expander, while the other circuit can be configured as a compressor or expander. Each circuit has a full wave rectifier to provide average value information to a variable gain cell located in either the input stage or the feedback path. An internal, temperature stable bandgap reference provides the necessary precision voltages and currents required.

The MC33110 will operate from a supply voltage of 2.1 to 7.0 V, over a temperature range of −40° to +85°C. The device is designed to accommodate an 80 dB dynamic range from −60 dB to +20 dB, referenced to 100 mVrms.

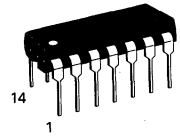
Applications include cordless telephone, CB, walkie-talkie, most voice RF links, and any application where the signal-to-noise ratio can be improved by reducing the transmitted dynamic range. Other applications include speakerphone and voice activated intercom, dictating machine, standard telephone, etc.

The MC33110 is packaged in a 14 pin DIP for through-the-hole applications and an SO-14 surface mount.

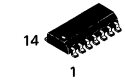
- Operating Supply Voltage: 2.1 to 7.0 V
- No Precision External Components Required
- 80 dB Dynamic Range Compressed to 40 dB, Re-expandable to 80 dB
- Unity Gain Level: 100 mVrms
- Adjustable Response Time
- Ambient Operating Temperature: −40° to +85°C
- Temperature Compensated Reference
- Applications Include Cordless Phone, CB Radio, Speakerphone, etc.

LOW VOLTAGE COMPANDER

SILICON MONOLITHIC INTEGRATED CIRCUIT

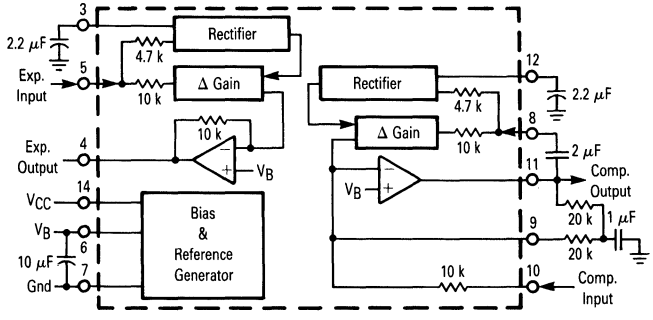


P SUFFIX
PLASTIC PACKAGE
CASE 646

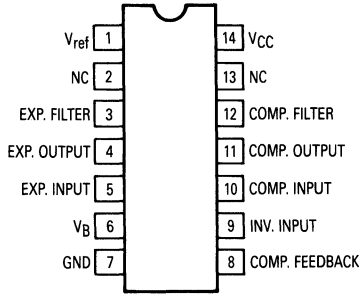


D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO-14)

SIMPLIFIED BLOCK DIAGRAM



PIN CONNECTIONS
(TOP VIEW)



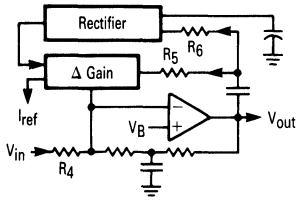
ORDERING INFORMATION

Device	Temperature Range	Package
MC33110D MC33110P	−40°C to +85°C	SO-14 Plastic DIP

PIN DESCRIPTION

Name	Pin	Description
V_{ref}	1	Normally this pin is not used and is left open. It can be used to make limited adjustments to the 0 dB level. Any noise or leakage at this pin will affect the 0 dB level and gain tracking.
NC	2, 13	No connection. These pins are not internally connected.
Expander Filter	3	Connect to an external capacitor to filter the full wave rectifier's output. This capacitor affects attack and decay times, as well as low frequency accuracy.
Expander Output	4	Output of the expander amplifier.
Expander Input	5	The input impedance is nominally 3.2 kΩ. Nominal signal range is 3.16 mVrms to 316 mVrms. Must be capacitor coupled to the signal source.
V_B	6	An internal reference voltage, nominally $V_{CC}/2$. This is an AC ground and must be well filtered to obtain high power supply rejection and low crosstalk.
Ground	7	Connect to a clean power supply ground.
Compressor Feedback	8	Input to the compressor variable gain stage and rectifier. Normally the signal is supplied by the compressor's output (Pin 11). Input impedance is nominally 3.2 kΩ.
Inverting Input	9	Inverting input to the compressor amplifier. Normally, this is connected to the compressor's output through a filtered DC feedback path.
Compressor Input	10	The input impedance is nominally 10 kΩ. Nominal signal range is 100 μVrms to 1.0 Vrms. Must be capacitor coupled to the signal source.
Compressor Output	11	Output of the compressor amplifier.
Compressor Filter	12	Connect to an external capacitor to filter the full wave rectifier's output. This capacitor affects attack & decay times, and low frequency accuracy.
V_{CC}	14	Power supply pin. Connect to a power supply providing between 2.1 V and 7.0 V. Nominal current consumption is 3.5 mA.

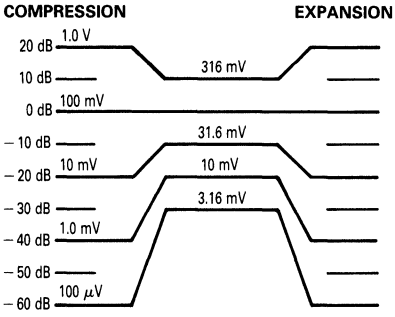
COMPRESSOR



$$V_{out} = \sqrt{\frac{R_5 \times R_6 \times I_{ref} \times V_{in}}{7.2 \times R_4}}$$

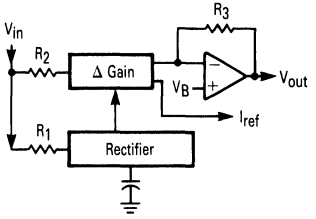
$$= 0.3162 \times \sqrt{V_{in}}$$

TRANSFER FUNCTIONS



(VOLTAGES ARE RMS)

EXPANDER



$$V_{out} = \frac{7.2 \times R_3 \times V_{in}^2}{R_1 \times R_2 \times I_{ref}}$$

$$= 10 \times V_{in}^2$$

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
V_{CC} Supply Voltage	V_{CC}	+12, −0.5	Vdc
High Input Voltage (Pin 5 & 10)	V_{IH}	V_{CC} + 0.5	Vdc
Low Input Voltage	V_{IL}	−0.5	Vdc
Output Source Current (Pin 4 & 11)	I_{O+}	Self-Limiting	
Output Sink Current	I_{O-}	20	mA
Junction Temperature	T_J	−65, +150	°C

Devices should not be operated at these values. The "Recommended Operating Conditions" table provides conditions for actual device operation.

2

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Min	Typ	Max	Unit
V_{CC} Supply Voltage	V_{CC}	2.1	—	7.0	Vdc
Input Voltage Range	V_{IR}				Vrms
Compressor, 2.1 V < V_{CC} < 7.0 V		0	—	1.0	
Expander, V_{CC} = 2.1 V		0	—	0.25	
Expander, 3.0 V < V_{CC} < 7.0 V		0	—	0.316	
Input Frequency	F_{in}	100	—	20 k	Hz
Output Load	R_L				Ω
Compressor (Pin 11, V_O = 100 mV)		300	—	∞	
Expander (Pin 4, V_O = 100 mV)		150	—	∞	
Ambient Temperature	T_A	−40	—	+85	°C

All limits are not necessarily functional concurrently.

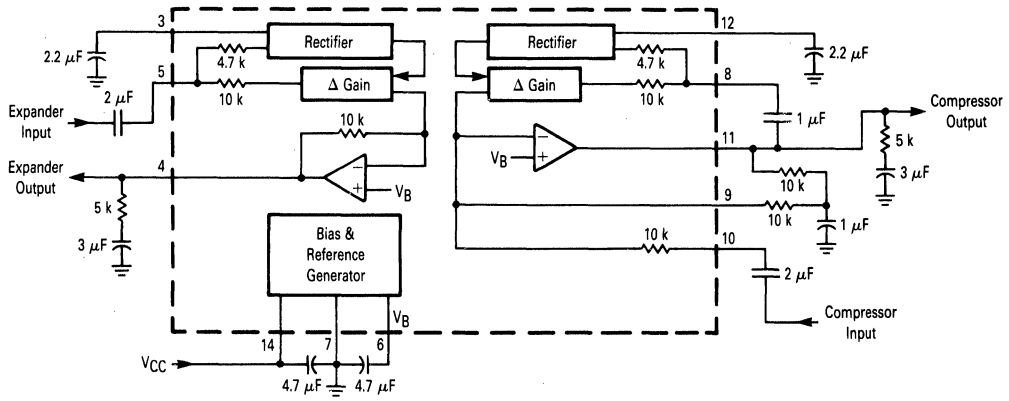
ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, f = 1.0 kHz, unless otherwise noted, T_A = 25°C, see Figure 1)

Characteristic		Symbol	Min	Typ	Max	Unit
POWER SUPPLY						
Power Supply Current		I_{CC}				mA
V_{CC} = +5.0 V			—	3.5	5.5	
V_{CC} = +2.1 V			—	3.3	—	
V_B Voltage		V_B				Vdc
V_{CC} = +5.0 V			2.4	2.5	2.6	
2.1 V < V_{CC} < 7.0 V			—	$V_{CC}/2$	—	
COMPRESSOR						
0 dB Gain		$G_{(CO)}$				dB
V_{in} = 100 mVrms, Pin 1 = Open			−1.5	0	1.5	
Gain Tracking		G_t				dB
@ V_{in} = 1.0 Vrms, output relative to $G_{(CO)}$			+9.0	+10	+11	
@ V_{in} = 10 mVrms, output relative to $G_{(CO)}$			—	−10	—	
@ V_{in} = 1.0 mVrms, output relative to $G_{(CO)}$			—	−20	—	
@ V_{in} = 100 μVrms, output relative to $G_{(CO)}$			−31	−30	−29	
Total Harmonic Distortion		THD				%
V_{in} = 100 mVrms, f = 1.0 kHz			0	0.1	1.5	
Power Supply Rejection		PSRR				dB
f = 1.0 kHz, C_{VB} = 10 μF, V_{in} = −20 dB			—	22	—	
Attack Time (Capacitor @ Pin 12 = 2.2 μF)		$t_{a(C)}$	—	6.0	—	ms
Decay Time (Capacitor @ Pin 12 = 2.2 μF)		$t_{d(C)}$	—	20	—	ms
Input Impedance	Pin 10	R_{in}	—	10	—	kΩ
	Pin 8		—	3.2	—	
Peak Output Current	Pin 11	I_{pk}	—	0.3	—	mA
Output Offset		V_{OO}				mVdc
Pin 11, with respect to Pin 6, NO SIGNAL			−150	0	+150	
Change from NO SIGNAL to 1.0 Vrms at Input			—	50	—	

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, f = 1.0 kHz, unless otherwise noted, T_A = 25°C, see Figure 1)

Characteristic		Symbol	Min	Typ	Max	Unit
EXPANDER						
0 dB Gain (V_{in} = 100 mVrms, Pin 1 = open)		$G_{(EO)}$	 −1.5	 0	 1.5	dB
Gain Tracking @ V_{in} = 316 mVrms, output relative to $G_{(EO)}$ @ V_{in} = 31.6 mVrms, output relative to $G_{(EO)}$ @ V_{in} = 10 mVrms, output relative to $G_{(EO)}$ @ V_{in} = 3.16 mVrms, output relative to $G_{(EO)}$		G_t	 +19 — — −61	 +20 −20 −40 −60	 +21 — — −59	dB
Total Harmonic Distortion V_{in} = 100 mVrms, f = 1.0 kHz		THD	 0	 0.06	 1.5	%
Power Supply Rejection (f = 1.0 kHz, C_{VB} = 10 μF)		PSRR	—	37	—	dB
Attack Time (Capacitor @ Pin 3 = 2.2 μF)		$t_{a(E)}$	—	19	—	ms
Decay Time (Capacitor @ Pin 3 = 2.2 μF)		$t_{d(E)}$	—	20	—	ms
Input Impedance	Pin 5	R_{in}	—	3.2	—	kΩ
Peak Output Current	Pin 4	I_{pk}	—	1.0	—	mA
Output Offset Pin 4, with respect to Pin 6, NO SIGNAL Change from NO SIGNAL to 316 mVrms at Input		V_{OO}	 −150 —	 0 25	 +150 —	mVdc
MISCELLANEOUS						
Gain (Pin 10 to Pin 4; Pin 11 capacitor coupled to Pin 5) V_{CC} = 7.0 V, V_{in} = 1.0 Vrms V_{CC} = 3.0 V, V_{in} = 1.0 Vrms V_{CC} = 2.1 V, V_{in} = 31.6 mVrms		A_V	 −2.5 −2.5 −2.5	 0 0 0	 +2.5 +2.5 +2.5	dB
Channel Separation Expander to Compressor, output measured at Pin 11 V_{in} @ Pin 5 = 316 mVrms, f = 1.0 kHz V_{in} @ Pin 5 = 316 mVrms, f = 10 kHz		CS	 43 —	 48 68	 — —	dB
Compressor to Expander, output measured at Pin 4 V_{in} @ Pin 10 = 1.0 Vrms, f = 1.0 kHz V_{in} @ Pin 10 = 1.0 Vrms, f = 10 kHz			 65 —	 107 114	 — —	

FIGURE 1 — TEST CIRCUIT



COMPRESSOR

FIGURE 2 — COMPRESSOR TRANSFER CHARACTERISTICS

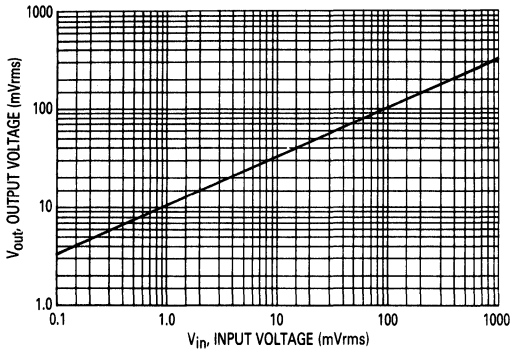


FIGURE 4 — COMPRESSOR TRANSFER CHARACTERISTICS

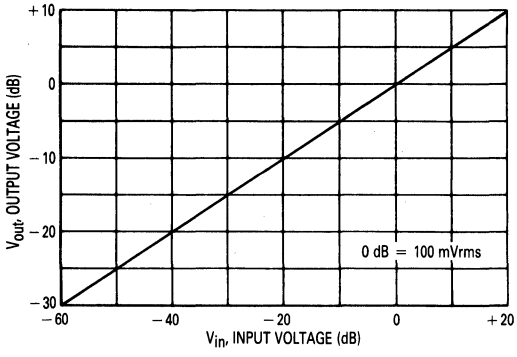
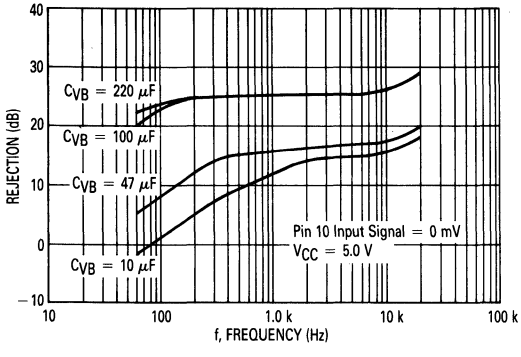


FIGURE 6 — POWER SUPPLY REJECTION (COMPRESSOR)



EXPANDER

FIGURE 3 — EXPANDER TRANSFER CHARACTERISTICS

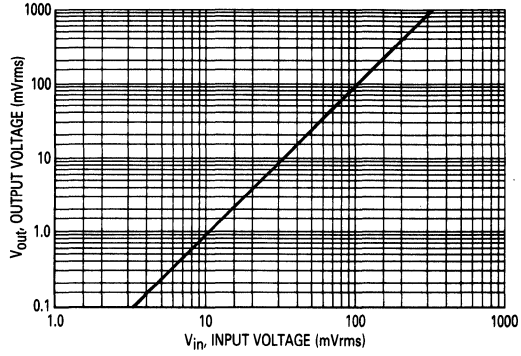


FIGURE 5 — EXPANDER TRANSFER CHARACTERISTICS

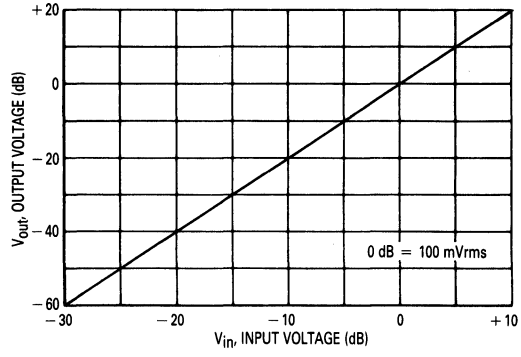
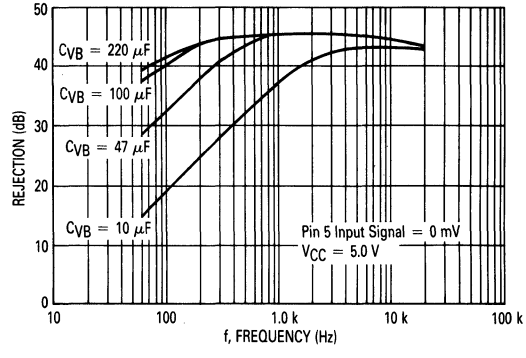


FIGURE 7 — POWER SUPPLY REJECTION (EXPANDER)



COMPRESSOR

EXPANDER

FIGURE 8 — POWER SUPPLY REJECTION (COMPRESSOR)

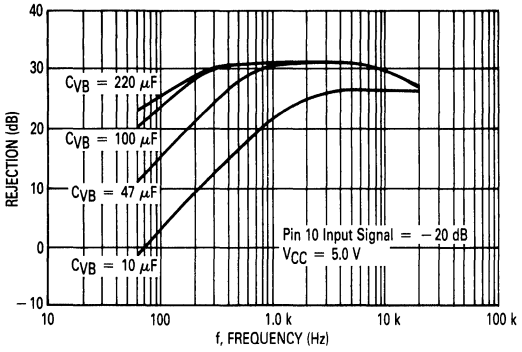


FIGURE 9 — POWER SUPPLY REJECTION (EXPANDER)

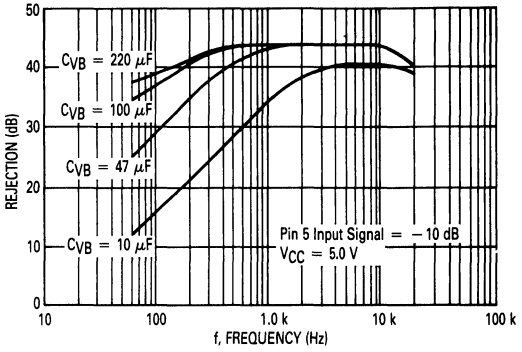


FIGURE 10 — FREQUENCY RESPONSE (COMPRESSOR)

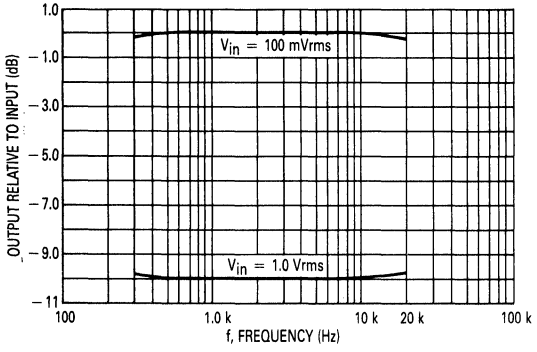


FIGURE 11 — FREQUENCY RESPONSE (EXPANDER)

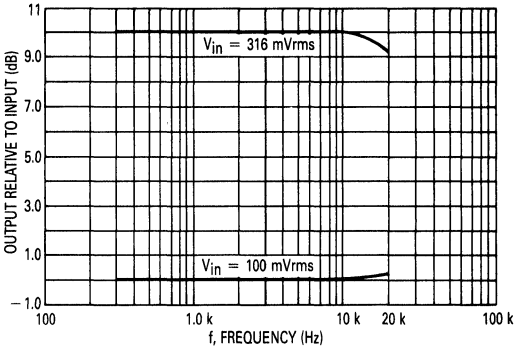


FIGURE 12 — FREQUENCY RESPONSE (COMPRESSOR)

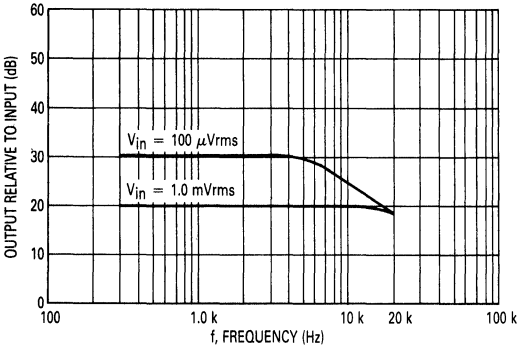


FIGURE 13 — FREQUENCY RESPONSE (EXPANDER)

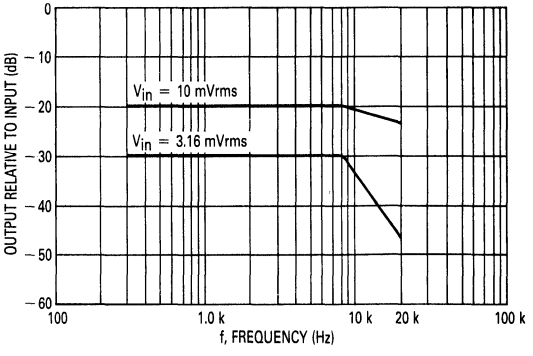


FIGURE 14 — ATTACK AND DECAY TIMES (COMPRESSOR)

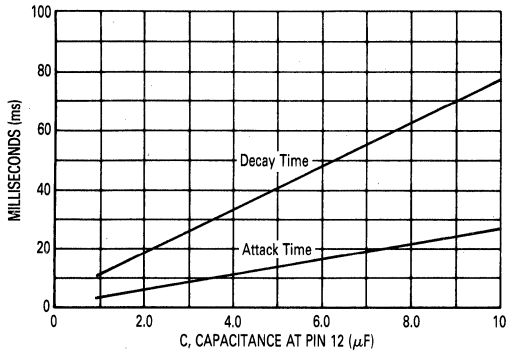


FIGURE 15 — ATTACK AND DECAY TIMES (EXPANDER)

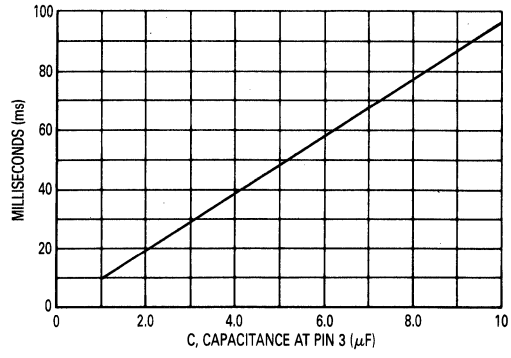
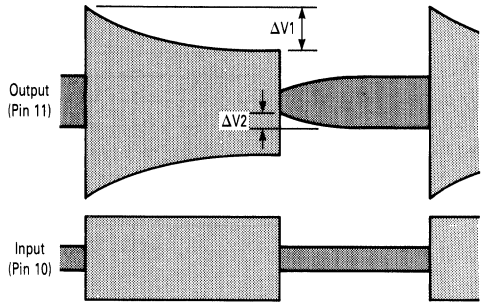
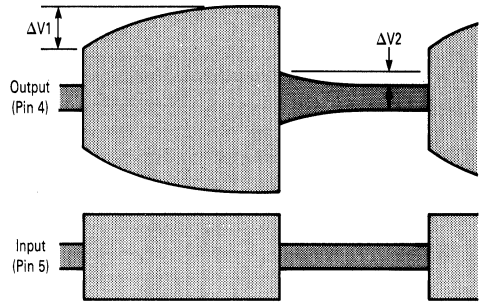


FIGURE 16 — ATTACK AND DECAY TIMES (COMPRESSOR)



Attack Time = Time to 63% of ΔV1.
Decay Time = Time to 63% of ΔV2.

FIGURE 17 — ATTACK AND DECAY TIMES (EXPANDER)



Attack Time = Time to 63% of ΔV1.
Decay Time = Time to 63% of ΔV2.

FIGURE 18 — MAXIMUM INPUT SIGNAL

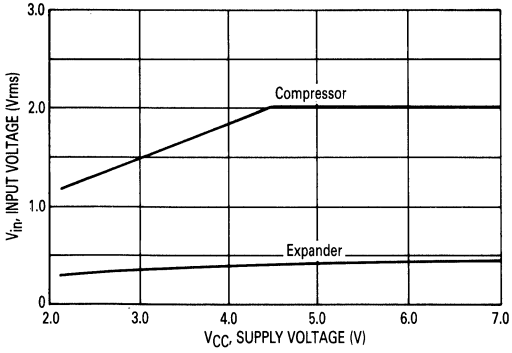
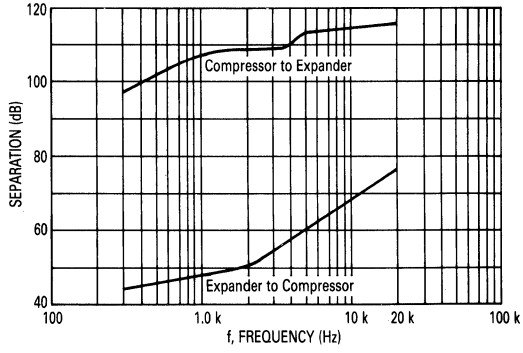
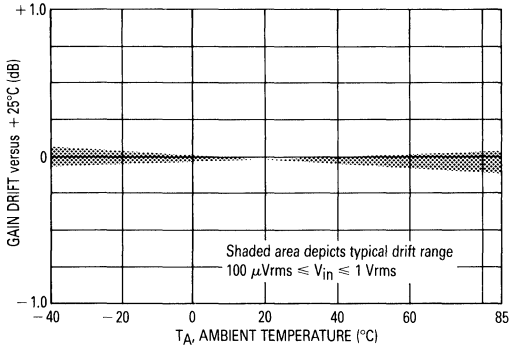


FIGURE 19 — CHANNEL SEPARATION



COMPRESSOR

FIGURE 20 — COMPRESSOR GAIN TRACKING versus TEMPERATURE



EXPANDER

FIGURE 21 — EXPANDER GAIN TRACKING versus TEMPERATURE

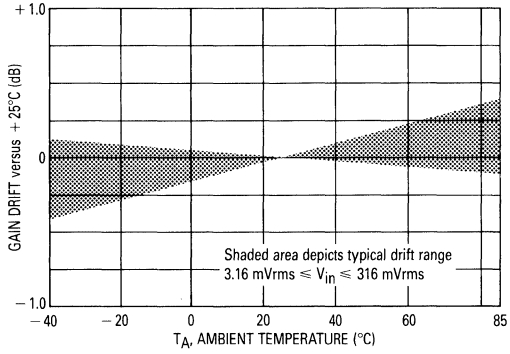


FIGURE 22 — COMPRESSOR THD versus TEMPERATURE

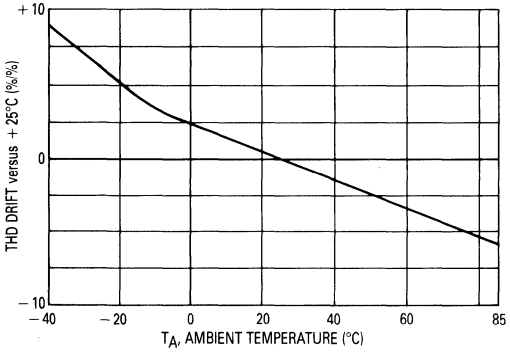
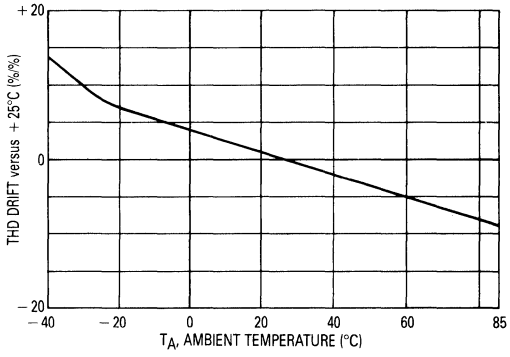


FIGURE 23 — EXPANDER THD versus TEMPERATURE



FUNCTIONAL DESCRIPTION

Introduction

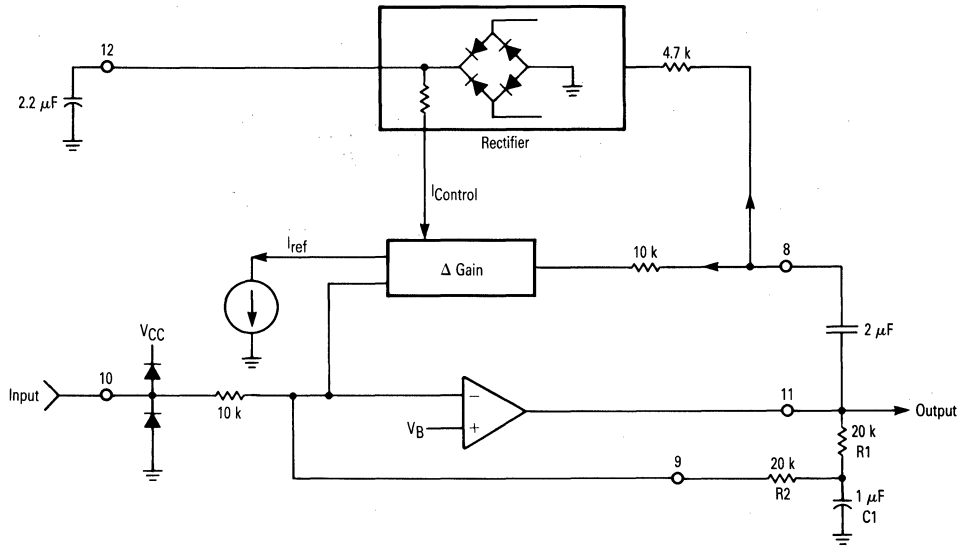
The MC33110 compander (COMpressor and exPANDER) is composed of two variable gain circuits which provide compression and expansion of the signal dynamic range. The compressor will take a signal with an 80 dB dynamic range (100 μV to 1.0 Vrms), and reduce that to a 40 dB dynamic range by attenuating strong signals, while amplifying low level signals. The expander does the opposite in that the 40 dB signal range is increased to a dynamic range of 80 dB by amplifying strong signals and attenuating low level signals. The 0 dB level is internally set at 100 mVrms — that is the signal level which is neither amplified nor attenuated. Both circuits contain the necessary precision full wave rectifier, variable gain cell, and temperature compensated references required for accurate and stable performance.

Note: All dB values mentioned in this data sheet, unless otherwise noted, are referred to 100 mVrms.

Compressor

The compressor is an operational amplifier with a fixed input resistor and a variable gain cell in its feedback path as shown in Figure 24.

FIGURE 24 — COMPRESSOR



The amplifier output is sampled by the precision rectifier which, in turn, supplies a DC signal ($I_{Control}$), representative of the rectifier's AC signal, to the variable gain cell. The reference current (I_{ref}) is an internally generated precision current. The effective impedance of the variable gain cell varies with the ratio of the two currents, and decreases as $I_{Control}$ increases, thereby providing compression. The output is related to the input by the following equation:

$$V_{out} = 0.3162 \times \sqrt{V_{in}} \qquad \text{(Equation 1)}$$

In terms of dB levels, the relationship is:

$$V_{out(dB)} = 0.5 \times V_{in(dB)} \qquad \text{(Equation 2)}$$

where 0 dB = 100 mVrms (see Figure 2 and 4).

The inputs and output are internally biased at V_B ($V_{CC}/2$), and must therefore be capacitor coupled to external circuitry. Pin 10 input impedance is nominally 10 kΩ (±20%), and the maximum functional input signal is shown in Figure 18. Bias currents required by the op amp and the variable gain cell are internally supplied. Due to clamp diodes at the input (to V_{CC} and ground), the input signal must be maintained between the supply rails. If the input signal goes more than 0.5 V above V_{CC} or below ground, excessive currents will flow and distortion will show up at the output.

When no AC signals are present at the input, the variable gain cell will attempt to set such a high gain that the circuit may become unstable. For this reason resistors R1 and R2, and capacitor C1 are added to provide DC stability. The pole formed by R1, R2 and C1 should have a pole frequency no more than 1/10th of the lowest frequency of interest. The pole frequency is calculated from:

$$f = \frac{R_1 + R_2}{2\pi \times R_1 R_2 C_1} \qquad \text{(Equation 3)}$$

for the component values shown, the pole frequency is ≈16 Hz.

Likewise, the capacitor between Pins 11 and 8 should be selected such that, in conjunction with the input impedance at Pin 8 (≈3200 Ω, ±20%), the resulting pole frequency is no more than 1/10 of the lowest frequency of interest. With the components shown, the pole frequency is <30 Hz. This pole frequency is calculated from:

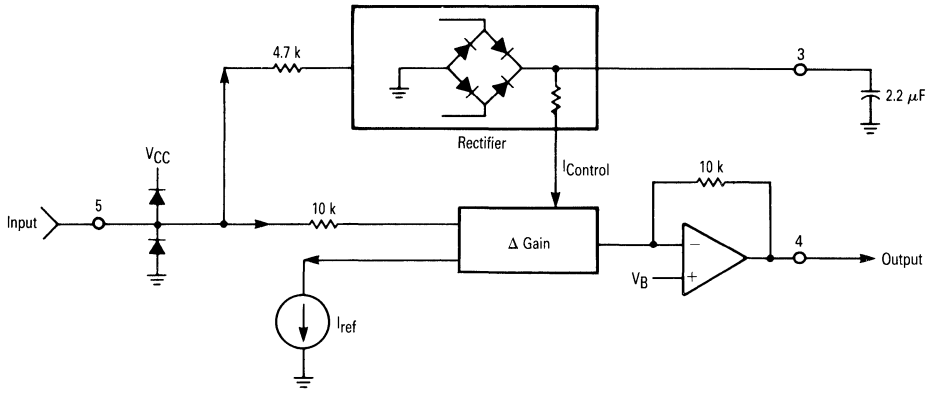
$$f = \frac{1}{2\pi \times 3.2\text{ k} \times C} \qquad \text{(Equation 4)}$$

The output of the rectifier is filtered by the capacitor at Pin 12, which, in conjunction with an internal 10 k resistor, provides the time constant for the attack and decay times. Figure 14 and 16 indicate how the times vary with the capacitor value. The attack time for the compressor is always faster than the decay time due to the fact that the rectifier is fed from the output rather than the input. Since the output is initially larger than expected (immediately after the input has increased), the external capacitor is charged more quickly during the initial part of the time constant. When the input is decreased, the time constant is closer to that calculated by t = RC. If the attack and decay times are decreased by using a smaller capacitor, performance at low frequencies will degrade.

Expander

The expander is an operational amplifier with a fixed feedback resistor and a variable gain cell in its input path as shown in Figure 25.

FIGURE 25 — EXPANDER



The input signal is sampled by the precision rectifier which, in turn, supplies a DC signal ($I_{Control}$), representative of the AC input signal, to the variable gain cell. The reference current (I_{ref}) is an internally generated precision current. The effective impedance of the variable gain cell varies with the ratio of the two currents, and decreases as $I_{Control}$ increases, thereby providing expansion. The output is related to the input by the following equation:

$$V_{out} = 10 \times (V_{in})^2 \qquad \text{(Equation 5)}$$

In terms of dB levels, the relationship is:

$$V_{out(dB)} = 2.0 \times V_{in(dB)} \qquad \text{(Equation 6)}$$

where 0 dB = 100 mVrms (see Figure 3 and 5).

The inputs and output are internally biased at V_B ($V_{CC/2}$), and must therefore be capacitor coupled to external circuitry. The input impedance at Pin 5 is nominally 3.2 kΩ (±20%), and the maximum functional input signal is shown in Figure 18. Bias currents required by the op amp and the variable gain cell are internally supplied. Due to clamp diodes at the input (to V_{CC} and ground), the input signal must be maintained between the supply rails. If the input signal goes more than 0.5 V above V_{CC} or below ground, excessive currents will flow, and distortion will show up at the output.

The output of the rectifier is filtered by the capacitor at Pin 3, which, in conjunction with an internal 10 k resistor, provides the time constant for the attack and decay times. Figure 15 and 17 indicate how the times vary with the capacitor value. If the attack and decay times are decreased by using a smaller capacitor, performance at low frequencies will degrade.

Power Supply

The MC33110 requires a power supply voltage between 2.1 V and 7.0 V, and a nominal current of 3.5 mA. The supply voltage should be well filtered and free of ripple. A minimum of 4.7 μF in parallel with a 0.01 μF capacitor is recommended for filtering and RF bypass.

V_B (Pin 6) is an internally generated mid supply reference, and is used internally as an AC ground. The external capacitor at Pin 6 filters this voltage, and its value affects the power supply noise rejection as shown in Figures 6 through 9. This reference voltage may be used to bias external circuitry as long as the current draw is limited to <10 μA.

Signal-to-Noise Improvement

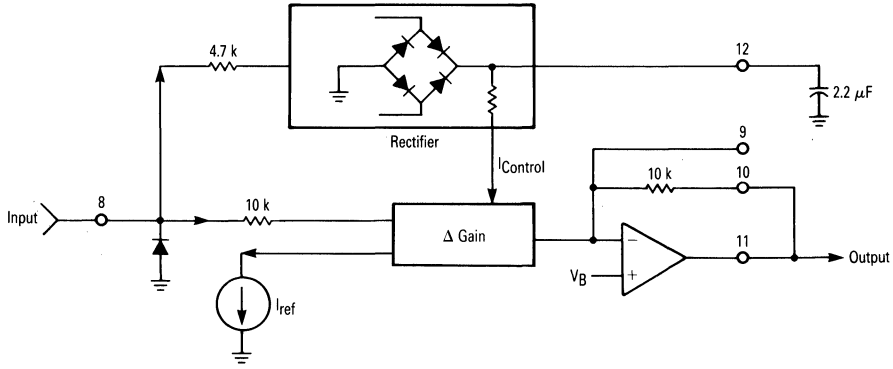
Among the basic reasons for the original development of compander type circuits was to improve the signal-to-noise ratio of long distance telecom circuits, and of voice circuits which are transmitted over RF links (CBs, walkie-talkies, cordless phones, etc.). Since much of the noise heard at the receiving end of a transmission is due to noise picked up, for example, in the airway portion of the RF link, the compressor was developed to increase the low-level signals at the transmitting end. Then any noise picked in the RF link would be a smaller percentage of the transmitted signal level. At the receiving end, the signal is then expanded back to its original level, retaining the same high signal-to-noise ratio. While the above explanation indicates it is not necessary to attenuate strong signals (at the transmitting end), a benefit of doing this is the reduced dynamic range which must be handled by the system transmitter and receiver. The MC33110 was designed for a two-to-one compression and expansion, i.e. an 80 dB dynamic signal is compressed to a 40 dB dynamic range, transmitted to the receiving end and then expanded back to an 80 dB dynamic range.

The MC33110 compander is not limited to RF or long distance telephony applications. It can be used in any system requiring an improved signal-to-noise ratio such as telephones, speakerphones, tape recorders, digital recording, and many others.

Second Expander

Should the application require it, the MC33110 can be configured as two expanders by reconfiguring the compressor side as shown in Figure 26.

FIGURE 26 — SECOND EXPANDER



This circuit will provide the same performance as the expander at Pins 3 through 5.

Power Supplies, Grounding

The PC board layout, the quality of the power supplies and the ground system **at the IC** are very important in order to obtain proper operation. Noise, from any source, coming into the device on V_{CC} or ground, can cause a distorted output, or incorrect gain level.

V_{CC} must be decoupled to the appropriate ground **at the IC** (within 1" max) with a 4.7 μF capacitor and a 0.01 μF ceramic. A tantalum capacitor is recommended for the larger value if very high frequency noise is present since electrolytic capacitors simply have too much inductance at those frequencies. The quality of the power supply voltage should be checked at the IC with a high frequency scope. Noise spikes (always present if digital circuits are near this IC) can easily exceed 400 mV, and if they get into the IC, the output can have noise or distortion. Noise can be reduced by inserting resistors and/or inductors between the supply and the IC.

If switching power supplies are used, there will usually be spikes of 0.5 V or greater at frequencies of 50 kHz to 1.0 MHz. These spikes are generally more difficult to reduce because of their greater energy content. In extreme cases, a three terminal regulator (MC78L05ACP), with appropriate high frequency filtering, should be used and dedicated to the analog portion of the circuit.

The ripple content of the supply should not allow its magnitude to exceed the values in the Recommended Operating Conditions table.

The PC board tracks supplying V_{CC} and ground to the MC33110 should preferably not be at the tail end of the bus distribution, after passing through a maze of digital circuitry. The analog circuitry containing the MC33110 should be close to the power supply, or the connector where the supply voltages enter the board. If V_{CC} is supplying considerable current to other parts of the board, then it is preferable to have dedicated lines from the supply or connector directly to the MC33110 and associated circuitry.

PC Board Layout

Although this device is intended for use in the audio frequency range, the amplifiers have a bandwidth of ≈300 kHz, and can therefore oscillate at frequencies outside the voiceband should there be excessive stray capacitance or other unintended feedback loops. A solid ground plane is strongly recommended to minimize coupling of any digital noise into the analog section. Use of wire wrapped boards should definitely be avoided.

Since many applications of the MC33110 compander involve voice transmission over RF links, care must be taken in the design of the product to keep RF signals out of the MC33110 and associated circuitry. This involves proper layout of the PC boards, the physical arrangement of the boards, shielding, proper RF ground, etc.

2

GLOSSARY

ATTACK TIME — The settling time for a circuit after its input signal has been increased.

ATTENUATION — A decrease in magnitude of a communication signal, usually expressed in dB.

BANDWIDTH — The range of information carrying frequencies of a communication system.

CHANNEL SEPARATION — The ability of one circuit to reject outputting signals which are being processed by another circuit. Also referred to as crosstalk, it is usually expressed in dB.

COMPANDER — A contraction of the words compressor and expander. A compander is composed of two circuits, one of each kind.

COMPRESSOR — A circuit which compresses or reduces the dynamic range of a signal by attenuating strong signals and amplifying low level signals.

dB — A power or voltage measurement unit, referred to another power or voltage. It is generally computed as:

$10 \times \log (P_1/P_2)$ for power measurements, and

$20 \times \log (V_1/V_2)$ for voltage measurements.

dBm — An indication of signal power. 1.0 mW across 600 Ω or 0.775 V rms, is typically defined as 0 dBm for telecom applications. Any voltage level is converted to dBm by:

$$dBm = 20 \times \log (Vrms/0.775), \text{ or}$$
$$dBm = [20 \times \log (Vrms)] + 2.22.$$

dBrn — Indicates a dBm measurement relative to 1.0 pW power level into 600 Ω. Generally used for noise measurements, 0 dBrn = −90 dBm.

dBrnC — Indicates a dBrn measurement using a C-message weighting filter.

DECAY TIME — The settling time for a circuit after its input signal has been decreased.

EXPANDER — A circuit which expands or increases the dynamic range of a signal by amplifying strong signals and attenuating low level signals.

GAIN — The change in signal amplitude (increase or decrease) after passing through an amplifier, or other circuit stage. Usually expressed in dB, an increase is a positive number and a decrease is a negative number.

POWER SUPPLY REJECTION RATIO — The ability of a circuit to reject outputting noise, or ripple, which is present on the power supply lines. PSRR is usually expressed in dB.

SIGNAL-TO-NOISE RATIO — The ratio of the desired signal to unwanted signals (noise) within a defined frequency range. The larger the number, the better.

VOICEBAND — That portion of the audio frequency range used for transmission across the telephone system. Typically, it is 300 to 3400 Hz.

MC33111

Advance Information

Low Voltage Compander

2

The MC33111 contains two variable gain circuits configured for compressing and expanding the dynamic range of an audio signal. One circuit is configured as an expander, and the other is configured as a compressor. Each circuit has a full wave rectifier to provide average value information to a variable gain cell located in either the input stage or the feedback path. An internal temperature stable bandgap reference provides the necessary precision voltages.

Included in the MC33111 are controls for muting each section independently, and for passthrough of both. Two uncommitted op amps are available for peripheral functions.

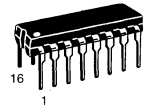
The MC33111 will operate from a supply voltage of 3.0 V to 7.0 V, and over a temperature range of – 40° to + 85°C. It is designed to accommodate a 60 dB dynamic range; from – 40 dB to + 20 dB referenced to 100 mVrms.

Applications include cordless telephone, CBs, walkie-talkies, and most voice RF links, and any application where an improvement in the signal to noise ratio is desired. Other applications include speakerphones and voice activated intercoms, dictating machines, etc.

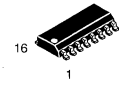
- Operating Supply Voltage: 3.0 V to 7.0 V
- Output Voltage Swing = 2.8 V_{p-p} with V_{CC} = 3.0 V
- No Precision External Components Required
- 60 dB Dynamic Range Compressed to 30 dB, Re-expandable to 60 dB
- Unity Gain Level set at 100 mVrms
- Attack and Decay Times Adjustable
- Mute and Passthrough Controls
- Two Uncommitted Op Amps
- Temperature Compensated Reference
- Available in Standard DIP and Surface Mount Packages

LOW VOLTAGE COMPANDER

SILICON MONOLITHIC INTEGRATED CIRCUIT

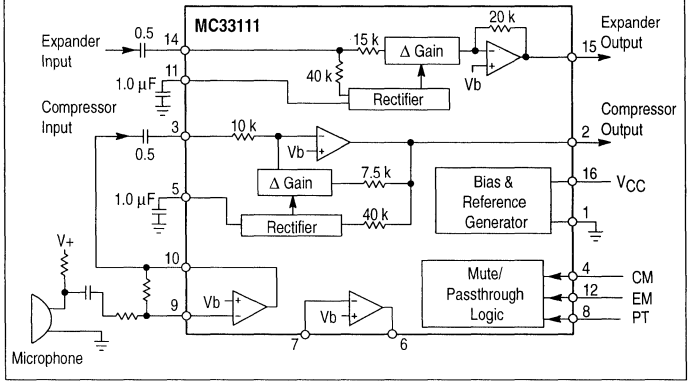


P SUFFIX
PLASTIC PACKAGE
CASE 648



D SUFFIX
PLASTIC PACKAGE
CASE 751B
(SO-16)

Simplified Block Diagram



This document contains information on a new product. Specifications and information herein are subject to change without notice. This device contains 329 active transistors.

TRUTH TABLE

CM	EM	PT	Function
0	0	0	Normal
1	X	X	Comp. Mute
X	1	X	Expander Mute
0	0	1	Passthrough

ORDERING INFORMATION

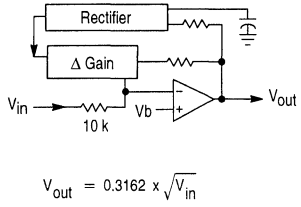
Device	Temperature Range	Package
MC33111D	– 40° to + 85°C	SO-16
MC33111P		Plastic DIP

PIN FUNCTION DESCRIPTION

Name	Pin	Description
Ground	1	Connect to a clean power supply ground.
Compressor Output	2	Output of the compressor section.
Compressor Input	3	Compressor input. The input impedance is nominally 10 kΩ. Nominal signal range is 1.0 mVrms to 1.0 Vrms in normal mode, and up to 0.8 Vrms in passthrough mode. Must be capacitor coupled to the signal source.
Compressor Mute	4	A logic high mutes the compressor. A logic low permits normal operation and passthrough.
Compressor Filter	5	Connect an external capacitor to filter the full wave rectifier's output. This capacitor affects attack and decay times, and low frequency accuracy.
Amplifier #1	6, 7	Inverting input (7) and output (6) of an op amp internally referenced to Vb.
Passthrough	8	A logic high sets the gain of both expander and compressor to ≈ 0 dB, independent of input level.
Amplifier #2	9, 10	Inverting input (9) and output (10) of an op amp internally referenced to Vb.
Expander Filter	11	Connect an external capacitor to filter the full wave rectifier's output. This capacitor affects attack and decay times, and low frequency accuracy.
Expander Mute	12	A logic high mutes the expander. A logic low permits normal operation and passthrough.
No Connect	13	This pin is not internally connected to anything.
Expander Input	14	Expander input. The input impedance is nominally 10.9 kΩ. Nominal signal range is 10 mVrms to 316 mVrms in normal mode, and up to 1.0 Vrms in passthrough mode. Must be capacitor coupled to the signal source.
Expander Output	15	Output of the expander section.
V_{CC}	16	Power supply. Connect to a power supply voltage in the range of 3.0 V to 7.0 V. Bypass capacitor should be provided at this pin.

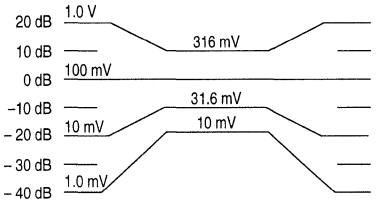
TRANSFER FUNCTIONS

Compressor



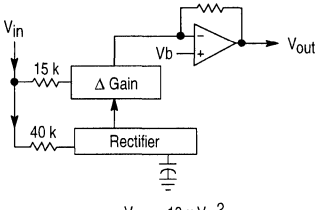
$V_{out} = 0.3162 \times \sqrt{V_{in}}$

Compression **Expansion**



(Voltages are rms)

Expander



$V_{out} = 10 \times V_{in}^2$

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
V_{CC} Supply Voltage (Pin 16 – Pin 1)	V_{CC}	−0.5, +12	Vdc
High Input Voltage (Pins 3, 4, 8, 12, 14)	V_{IH}	V_{CC} + 0.5	Vdc
Low Input Voltage (Pins 3, 4, 8, 12, 14)	V_{IL}	− 0.5	Vdc
Output Source Current (Pins 2, 6, 10, 15)	IO+	Self-limiting	mA
Output Sink Current (Pins 2, 6, 10, 15)	IO–	Self-limiting	mA
Storage Temperature	T_{stg}	− 65, +150	°C

NOTE: Devices should not be operated at these limits. The "Recommended Operating Conditions" provides for actual device operation.

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Min	Typ	Max	Unit
V_{CC} Supply Voltage	V_{CC}	3.0	—	7.0	Vdc
Input Signal Voltage Range (3.0 V < V_{CC} < 7.0 V)	V_{in}				
Compressor					
— Normal and Mute Mode		0	—	1.3	Vrms
— Passthrough Mode		0	—	0.8	
Expander		0	—	0.32	
— Normal Mode					
— Mute Mode		0	—	1.3	
— Passthrough Mode		0	—	1.0	
Frequency Range (± 1.0 dB accuracy)	Fin	0.300	—	10	kHz
Logic Input Voltage Range (Pins 4, 8, 12)	V_{in}	0	—	V_{CC}	Vdc
Operating Ambient Temperature	T_A	– 40	—	+ 85	°C

NOTE: All limits are not necessarily functional concurrently.

ELECTRICAL CHARACTERISTICS (V_{CC} = 3.6 V, f = 1.0 kHz, T_A = + 25°C, unless noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
COMPRESSOR (Pin 4 = Low unless noted)					
0 dB Gain (V_{in} = 100 mVrms)	G_{OC}	–1.5	0	1.5	dB
Gain tracking relative to G_{OC}	G_{TC}				dB
V_{in} = 1.0 Vrms		9.0	10	11	
V_{in} = 1.0 mVrms		– 21	– 20	–19	
Passthrough Gain (Pin 8 = High, Pin 4 = Low, V_{in} = 1.0 Vrms)	G_{PTC}	– 2.0	0	1.0	dB
Muting (Δ Gain) with Pin 4 = High (V_{in} = 1.0 Vrms)	G_{MTC}	55	67	—	dB
Max. Output Swing @ Pin 2 (3.0 V < V_{CC} < 7.0 V)	V_{out}				V_{p-p}
Normal Mode		—	1.1	—	
Passthrough Mode		—	2.3	—	
Peak Output Current (3.0 ≤ V_{CC} ≤ 7.0 V, Normal or Passthrough Modes, V_{in} = Max)	I_{PK}	—	± 4.0	—	mA
Total Harmonic Distoration (V_{in} = 100 mVrms)	THD	—	0.2	1.0	%
Power Supply Rejection @ 1.0 KHz	PSRR				dB
V_{in} (Pin 3) = 0		—	37	—	
V_{in} (Pin 3) = 10 mVrms		—	64	—	
V_{in} (Pin 3) = 1.0 Vrms		—	72	—	
Attack Time (Capacitor @ Pin 5 = 1.0 µF, per EIA-553)	$t_{AT(C)}$	—	3.0	—	ms
Decay Time (Capacitor @ Pin 5 = 1.0 µF, per EIA-553)	$t_{D(C)}$	—	14	—	
Input Impedance at Pin 3	Rin	8.0	10	14	kΩ
DC Bias Level (Pin 2)	V_{bIAS}	1.4	Vb	1.6	Vdc
Output DC Shift (V_{in} Changed from 0 to 100 mVrms)		– 20	1.6	2.0	mVdc
EXPANDER (Pin 12 = Low, unless noted)					
0 dB Gain (V_{in} = 100 mVrms)	G_{OE}	–1.5	0	1.5	dB
Gain Tracking Relative to G_{OE}	G_{TE}				dB
V_{in} = 316 mVrms		19	20	21	
V_{in} = 10 mVrms		– 41	– 40	– 39	
Passthrough Gain (Pin 8 = High, Pin 12 = Low, V_{in} = 1.0 Vrms)	G_{PTE}	–1.0	0	2.0	dB
Muting (Δ Gain) with Pin 12 = High (V_{in} = 0.316 Vrms)	G_{MTE}	60	76	—	dB
Max. Output Swing @ Pin 15 (3.0 V < V_{CC} , 7.0 V)	V_{out}				V_{p-p}
Normal Mode		—	2.8	—	
Passthrough Mode		—	2.8	—	
Peak Output Current	I_{PK}				mA
V_{CC} = 3.0 V, V_{out} ≤ 2.4 V_{p-p}		—	± 3.5	—	
V_{CC} = 3.0 V, V_{out} = 2.7 V_{p-p}		—	±1.0	—	
V_{CC} ≥ 3.6 V, V_{out} ≤ 2.8 V_{p-p}		—	± 4.0	—	
Total Harmonic Distoration (V_{in} = 100 mVrms)	THD	—	0.2	1.0	%

ELECTRICAL CHARACTERISTICS (V_{CC} = 3.6 V, f = 1.0 kHz, T_A = + 25°C, unless noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
EXPANDER (Pin 12 = Low, unless noted)					
Power Supply Rejection @ 1.0 kHz	PSRR				dB
V_{in} (Pin 14) = 0		—	74	—	
V_{in} (Pin 14) = 10 mVrms		—	76	—	
V_{in} (Pin 14) = 316 mVrms		—	62	—	
Attack Time (Capacitor @ Pin 11 = 1.0 µF, per EIA-553)	$t_{AT(E)}$	—	3.0	—	ms
Decay Time (Capacitor @ Pin 11 = 1.0 µF, per EIA-553)	$t_{D(E)}$	—	14	—	
Input Impedance at Pin 14	R_{in}	8.0	10.9	14	kΩ
DC Bias Level (Pin 15)	V_{bIAS}	1.4	Vb	1.6	Vdc
Output DC Shift (V_{in} changed from 0 to 100 mVrms)		– 20	1.0	20	mVdc
LOGIC INPUTS (Pins 4, 8, 12)					
Switching Threshold (3.0 < V_{CC} < 7.0 V)	V_{ST}	—	1.3	—	Vdc
Input Current	Rin				µA
@ V_{in} = 0 V		—	0	—	
@ V_{in} = 3.6 V		—	55	—	
Timing (V_{in} @ Pins 3 and 14 = 300 mVrms, See Figures 1, 2)					µs
Comp. Mute (Pin 4) to Comp. Output Low-to-High	t_{CMLH}	—	2.0	—	
High-to-Low	t_{CMHL}	—	3.0	—	
Exp. Mute (Pin 12) to Exp. Output Low-to-High	t_{EMLH}	—	2.0	—	
High-to-Low	t_{EMHL}	—	3.0	—	
Passthrough (Pin 8) to Comp. Output Low-to-High	t_{PCLH}	—	2.0	—	
High-to-Low	t_{PCHL}	—	5.0	—	
Passthrough (Pin 8) to Exp. Output Low-to-High	t_{PELH}	—	6.0	—	
High-to-Low	t_{PEHL}	—	7.0	—	
OP AMPS (Pins 6, 7, 9, 10)					
Open Loop Gain	A_{VOL}	—	100	—	dB
Gain Bandwidth	BW	—	300	—	kHz
Input Bias Current @ Pins 7, 9	I_{IB}	—	8.0	—	nA
Max Output Swing @ Pins 6, 10 (3.0 V < V_{CC} < 7.0 V)	V_{out}	—	2.8	—	V_{p-p}
Peak Output Current	I_{PK}				mA
V_{CC} = 3.0 V, $V_{out} \leq$ 2.4 V_{p-p}		—	± 3.0	—	
V_{CC} = 3.0 V, V_{out} = 2.6 V_{p-p}		—	± 2.0	—	
$V_{CC} \geq$ 3.6 V, $V_{out} \leq$ 2.8 V_{p-p}		—	± 3.7	—	
Total Harmonic Distoration (V_{out} = 1.0 Vrms, Unity Gain)	THD	—	0.02	0.2	%
MISCELLANEOUS					
Power Supply Current	I_{CC}				mA
@ V_{CC} = 3.6 V		—	1.5	2.0	
@ V_{CC} = 7.0 V		—	1.7	—	
Reference Voltage	Vb	—	1.5	—	Vdc
Channel Separation	CS				dB
Expander to Compressor					
(Pin 14 = 316 mVrms @ 1.0 kHz and Pin 3 = 0 mVrms)		40	70	—	
(Pin 14 = 100 mVrms (300 Hz < f < 20 kHz), Pin 3 = 100 mVrms @ 1.2 kHz)		—	96	—	
Compressor to Expander					
(Pin 3 = 1.0 Vrms @ 1.0 kHz and Pin 14 = 0 mVrms)		60	100	—	
(Pin 3 = 100 mVrms (300 Hz < f < 20 kHz), Pin 14 = 100 mVrms @ 1.2 kHz)		—	97	—	

TEMPERATURE PERFORMANCE (Typical performance based on device characterization, not guaranteed.)

Characteristic	– 40°C	+25°C	+ 85°C
Power Supply Current @ V_{CC} = 3.6 V @ V_{CC} = 7.0 V	 1.2 mA 1.4 mA	 1.5 mA 1.7 mA	 1.6 mA 1.9 mA
Reference Voltage (Vb)	1.495 V	1.5 V	1.505 V
0 dB Gain (V_{in} = 100 mVrms) — Compressor	0.08 dB	0 dB	– 0.04 dB
0 dB Gain (V_{in} = 100 mVrms) — Expander	0.04 dB	0 dB	– 0.03 dB
Total Harmonic Distortion (V_{in} = 100 mVrms) — Compressor	0.3%	0.2%	0.2%
Total Harmonic Distortion (V_{in} = 100 mVrms) — Expander	0.3%	0.2%	0.16%
Gain Tracking Relative to 0 dB Gain — Compressor V_{in} = 1.0 Vrms V_{in} = 1.0 mVrms	 10.8 dB –19.95 dB	 10 dB – 20 dB	 10 dB – 20.1 dB
Gain Tracking Relative to 0 dB Gain — Expander V_{in} = 316 mVrms V_{in} = 10 mVrms	 18.6 dB – 40.2 dB	 20 dB – 40 dB	 19.95 dB – 39.9 dB
Muting (Δ Gain) with Pin 4 = High (V_{in} = 1.0 Vrms) — Compressor	68 dB	67 dB	66 dB
Muting (Δ Gain) with Pin 12 = High (V_{in} = 0.316 Vrms) — Expander	76 dB	76 dB	75 dB

Figure 1. Mute Timing

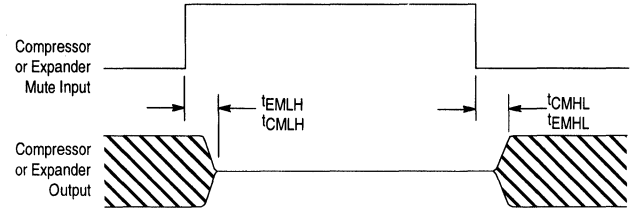


Figure 2. Passthrough Timing

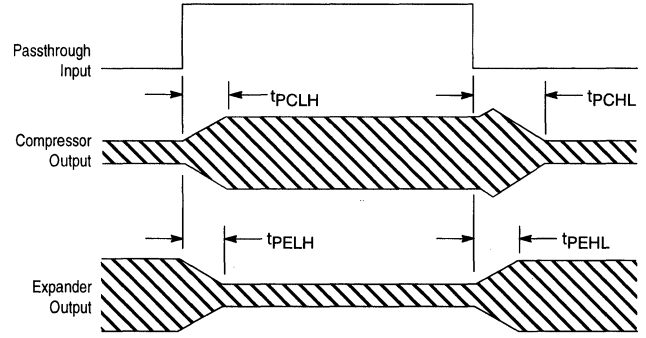


Figure 3. Transfer Characteristics

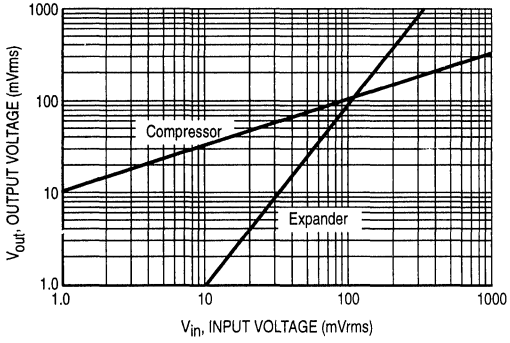


Figure 4. Transfer Characteristics

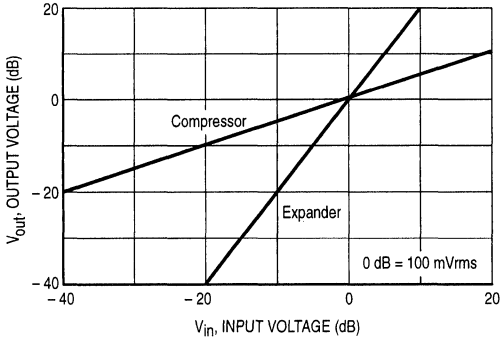


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Figure 5. Frequency Response (Compressor)

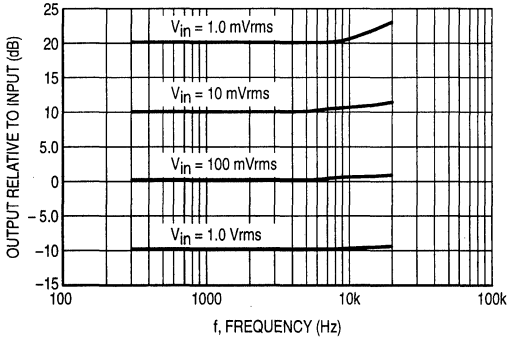


Figure 6. Frequency Response (Expander)

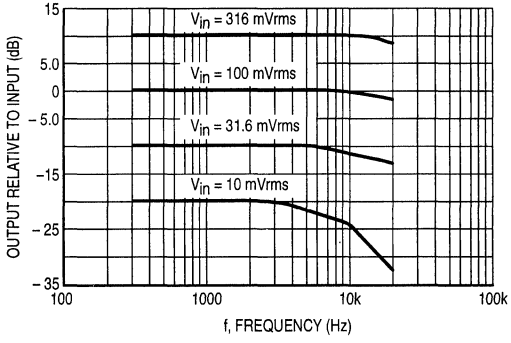
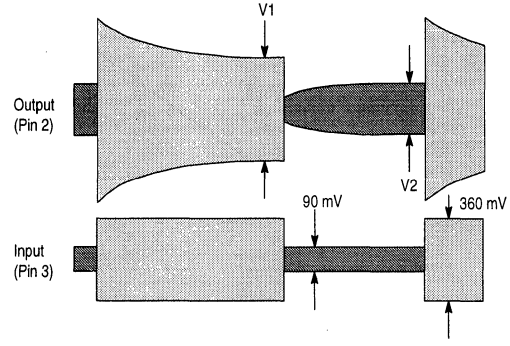
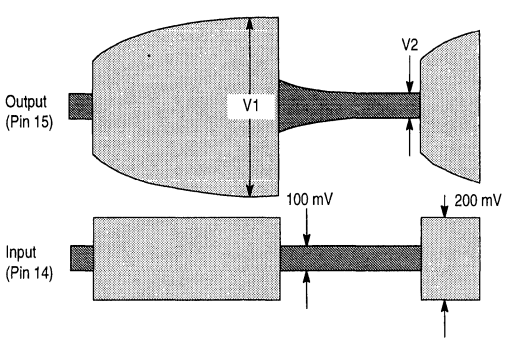


Figure 7. Attack and Decay Times (Compressor)



Attack Time = Time to 1.5 x V1 from input increase.
Decay Time = Time to 0.75 x V2 from input decrease.
Test per EIA-553.

Figure 8. Attack and Decay Times (Expander)



Attack Time = Time to 0.57 x V1 from input increase.
Decay Time = Time to 1.5 x V2 from input decrease.
Test per EIA-553.

Figure 9. Attack and Decay Times (Compressor)

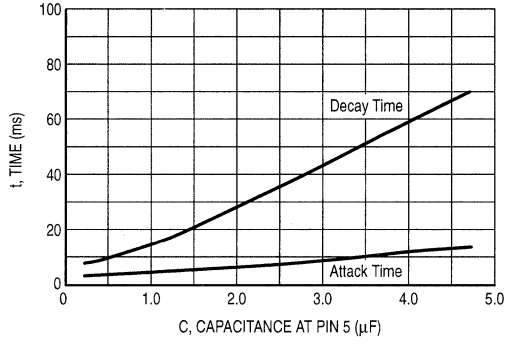


Figure 10. Attack and Decay Times (Expander)

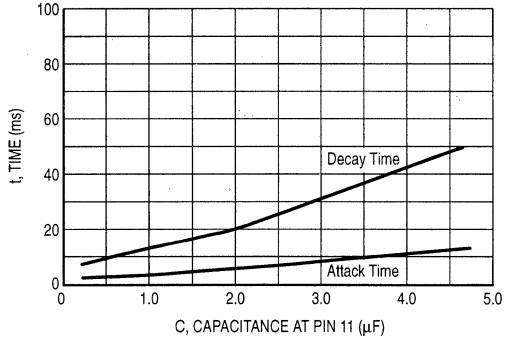


Figure 11. Compressor Gain Tracking versus Temperature

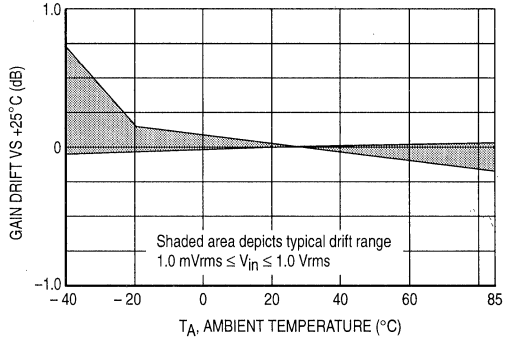


Figure 12. Expander Gain Tracking versus Temperature

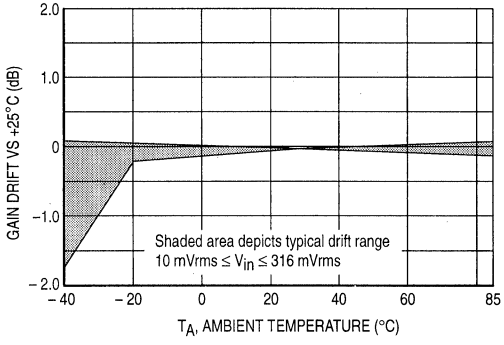


Figure 13. THD versus Temperature

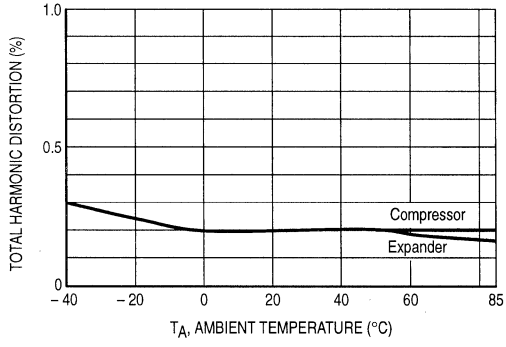
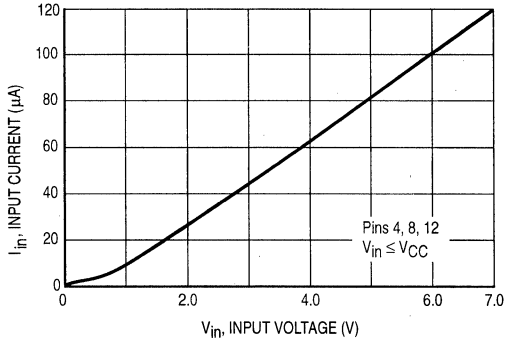


Figure 14. Logic Inputs' Current



FUNCTIONAL DESCRIPTION

Introduction

The MC33111 compander (COMpressor and exPANDER) is composed of two variable gain circuits which provide compression and expansion of a signal's dynamic range. The compressor will take a signal with a 60 dB dynamic range (1.0 mV to 1.0 Vrms), and reduce that to a 30 dB dynamic range (10 mV to 316 mV) by attenuating strong signals, while amplifying low level signals. The expander does the opposite in that the 30 dB signal range is increased to a dynamic range of 60 dB by amplifying strong signals and attenuating low level signals. The 0 dB level is internally set at 100 mVrms — that is the signal level which is neither amplified nor attenuated. Both circuits contain the necessary precision full wave rectifier, variable gain cell, and temperature compensated references required for accurate and stable performance.

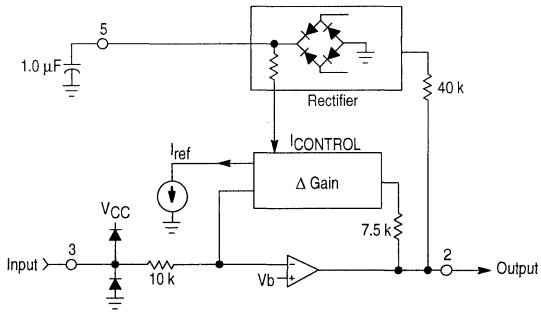
Both the compressor and expander can be muted independently by the use of Pins 4 and 12, respectively. A minimum of 55 dB of muting is guaranteed for the compressor, and 60 dB for the expander. A passthrough function (Pin 8) is provided which sets both sections to unity gain, regardless of input level.

Two uncommitted op amps are provided which can be used for perpherial functions. Each is internally biased at Vb (≈ +1.5 V), and has a bandwidth of ≈ 300 kHz.

NOTE: All dB values mentioned in this data sheet, unless otherwise noted, are referenced to 100 mVrms.

2

Figure 15. Compressor



Compressor

The compressor is a noninverting amplifier with a fixed input resistor and a variable gain cell in its feedback path as shown in Figure 15.

The amplifier output is sampled by the precision rectifier which, in turn, supplies a DC signal ($I_{CONTROL}$), representative of the rectifier's AC signal, to the variable gain cell. The reference current (I_{REF}) is an internally generated precision current. The effective impedance of the variable gain cell varies with the ratio of the two currents, and decreases as $I_{CONTROL}$ increases, thereby providing compression. The output is related to the input by the following equation (V_{in} and V_{out} are rms volts):

$$V_{out} = 0.3162 \times \sqrt{V_{in}} \quad (1)$$

In terms of dB levels, the relationship is:

$$Vo(dB) = 0.5 \times Vi(dB) \quad (2)$$

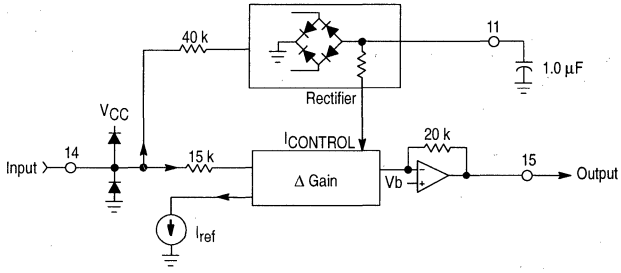
where 0 dB = 100 mVrms (See Figures 3 and 4).

The input and output are internally biased at Vb (≈ +1.5 V), and must therefore be capacitor coupled to external circuitry. Pin 3 input impedance is nominally 10 kΩ (± 20%), and the maximum functional input signal is listed in the Recommended Operating Conditions table. Bias currents required by the op amp and the variable gain cell are internally supplied. Due to clamp diodes at the input (to V_{CC} and ground), the input signal must be maintained between the supply rails. If the input signal goes more than 0.5 V above V_{CC} or below ground, excessive currents will flow, and distortion will show up at the output and possibly in other parts of the circuit.

When AC signals are not present at the input, the variable gain cell will attempt to set a very high gain to comply with Equation 2. An internal clamp limits the maximum gain to ≈ 26 dB to prevent instabilities.

The output of the rectifier is filtered by the capacitor at Pin 5, which, in conjunction with an internal 20 k resistor, provides the time constant for the attack and decay times. The attack and decay times listed in the Electrical Characteristics were determined using the test procedure defined in EIA-553. Figure 9 indicates how the times vary with the capacitor value. If the attack and decay times are decreased using a smaller capacitor, performance at low frequencies will degrade.

Figure 16. Expander



2

Expander

The expander is an noninverting amplifier with a fixed feedback resistor and a variable gain cell in its input path as shown in Figure 16.

The input signal is sampled by the precision rectifier which, in turn, supplies a DC signal ($I_{CONTROL}$), representative of the AC input signal, to the variable gain cell. The reference current (I_{REF}) is an internally generated precision current. The effective impedance of the variable gain cell varies with the ratio of the two currents, and decreases as $I_{CONTROL}$ increases, thereby providing expansion. The output is related to the input by the following equation (V_{in} and V_{out} are rms volts):

$$V_{out} = 10 \times (V_{in})^2 \quad (3)$$

In terms of dB levels, the relationship is:

$$Vo(dB) = 2.0 \times Vi(dB) \quad (4)$$

where 0 dB = 100 mVrms (See Figures 3 and 4).

The input and output are internally biased at Vb (≈ +1.5 V), and must therefore be capacitor coupled to external circuitry. The input impedance at Pin 14 is nominally 10.9 kΩ (± 20%), and the maximum functional input signal is listed in the Recommended Operating Conditions table. Bias currents required by the op amp and the variable gain cell are internally supplied. Due to clamp diodes at the input (to V_{CC} and ground), the input signal must be maintained between the supply rails. If the input signal goes more than 0.5 V above V_{CC} or below ground, excessive currents will flow, and distortion will show up at the output, and possibly in other parts of the circuit.

The output of the rectifier is filtered by the capacitor at Pin 11, which, in conjunction with an internal 20 k resistor, provides the time constant for the attack and decay times. The attack and decay times listed in the Electrical Characteristics were determined using the test procedure defined in EIA-553. Figure 10 indicates how the times vary with the capacitor value. If the attack and decay times are decreased by using a smaller capacitor, performance at low frequencies will degrade.

Op Amps

The two op amps (at Pins 6, 7, 9, and 10) are identical and can be used for peripheral functions, such as a microphone amplifier, buffer, filter, etc. They have an open loop gain of ≈100 dB, and a bandwidth of ≈ 300 kHz. The noninverting inputs are internally biased at Vb (≈ +1.5 V). The inverting inputs (Pins 7, 9) require a bias current of ≈ 8.0 nA, which flows **into** the pin. The outputs can typically supply a maximum of 3.7 mA load current (see Electrical Characteristics).

NOTE: If an op amp is unused, its output MUST be tied to its input (Pin 6 to 7 and/or 9 to 10). Leaving an input open can affect other portions of the IC.

Logic Inputs

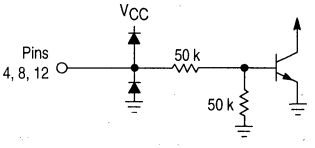
The three inputs (Pins 4, 8, 12) provide for muting and passthrough functions for the compressor and expander according to the following truth table:

CM (Pin 4)	EM (Pin 12)	PT (Pin 8)	Function
0	0	0	Normal Operation
1	X	X	Compressor Mute
X	1	X	Expander Mute
0	0	1	Passthrough

The logic section permits the compressor and expander to be muted independently. The Passthrough control affects both sections simultaneously, but only if the Mute inputs are at a logic level 0. If both the Passthrough and a Mute input are asserted, the Mute will override the Passthrough. The logic controls do not affect the two uncommitted op amps in any way.

Figure 17 depicts a typical logic input stage configuration, and Figure 14 indicates the typical input current. The inputs' threshold is ≈ +1.3 V, independent of V_{CC}. An open input is equivalent to a logic low, but good design practices dictate that inputs should never be left open. The inputs must be kept within the range of V_{CC} and GND. If an input is taken more than 0.5 V above V_{CC} or below GND excessive currents will flow, and the device's operation will be distorted.

Figure 17. Logic Input Stage



Power Supply

The MC33111 requires a supply voltage between 3.0 V and 7.0 V, and a nominal current of ≈ 1.6 mA. The supply voltage should be well filtered and free of ripple. A minimum of 4.7 μF in parallel with a 0.01 μF capacitor is recommended for filtering and RF bypass.

Vb is an internally generated reference set at ≈ +1.5 V, and is used internally as an AC ground. It is not available directly at any pins, but can be obtained as a buffered reference from either op amp by connecting the op amp as a follower.

APPLICATION INFORMATION

Typical Application Circuit

Figure 18 indicates a typical implementation of the MC33111 compander. The following points apply:

a) The values shown adjacent to some components are based on the expected use of the IC:
   — The input capacitors (Pins 3 and 14) provide a 3.0 dB rolloff of ≈ 30 Hz, a decade below the nominal voiceband.
   — The rectifier capacitors provide attack and decay times as indicated in the Electrical Tables.

b) The values for the unlabeled components are application dependent:
   — The components around the op amps depend on their use.
   — The value of the capacitors at the compressor and expander outputs depend on the circuit to which they are connected.

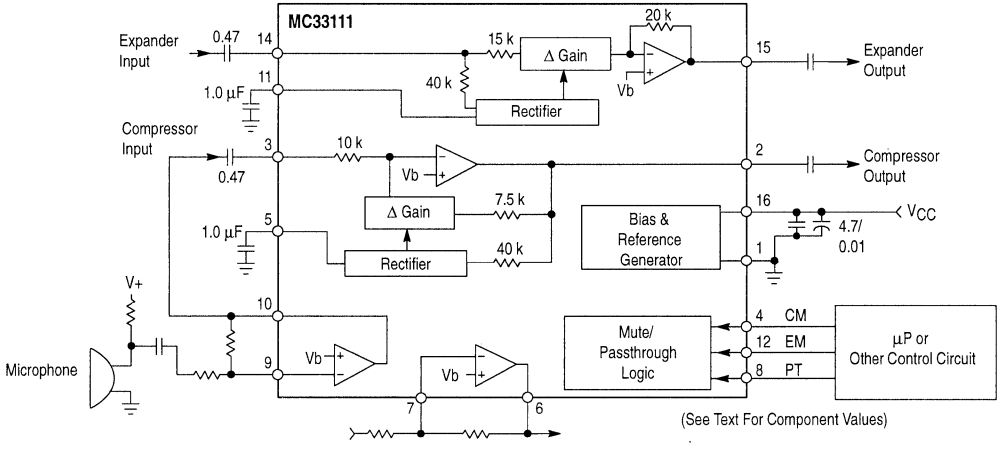
c) If either the compressor or expander is not used, its input **must** not be left open. It can be connected to ground either through a capacitor, or directly to ground.

d) The two op amps can be used for any purpose which suits the application. The indicated use of the one op amp as a microphone amplifier is only an example.

e) If an op amp is not used, its output and input **must** be connected together. Do not leave Pin 7 or Pin 9 open.

f) The logic inputs (Pins 4, 8, 12) are TTL/CMOS compatible. The logic high voltage must not exceed the V_{CC} voltage on the MC33111. Any unused input should be connected to ground and not left open.

Figure 18. Typical Application



Signal-To-Noise Improvement

Among the basic reasons for the original development of compander type circuits was to improve the signal-to-noise ratio of long distance communications circuits, and of voice circuits which are transmitted over RF links (CBs, walkie-talkies, cordless phones, etc.). Since much of the interfering noise heard at the receiving end of a transmission is due to noise picked up, for example, in the airway portion of the RF link, the compressor was developed to increase the low-level signals at the transmitting end. Then any noise picked up in the RF link would be a smaller percentage of the transmitted signal level. At the receiving end, the signal is then expanded back to is original level, retaining the same high signal-to-noise ratio. While the above explanation indicates it is not necessary to attenuate strong signals (at the transmitting end), a benefit of doing this is the reduced dynamic range which must be handled by the system transmitter and receiver. The MC33111 was designed for a two-to-one compression and expansion, i.e. a 60 dB dynamic signal is compressed to a 30 dB dynamic range, transmitted to the receiving end, and then expanded back to a 60 dB dynamic range.

The MC33111 compander is not limited to RF or long distance telephony applications. It can be used in any system requiring either an improved signal-to-noise ratio, or a reduced dynamic range. Such applications include telephones, speakerphones, tape recorders, wireless microphones, digital recording, and many others.

Power Supplies, Grounding

The PC board layout, and the quality of the power supplies and the ground system **at the IC** are very important in order to obtain proper operation. Noise, from any source, coming into the device on V_{CC} or ground, can cause a distorted output, or incorrect gain levels.

V_{CC} must be decoupled to the appropriate ground **at the IC** (within 1″ max.) with a 4.7 μF capacitor and a 0.01 μF ceramic. A tantalum capacitor is recommended for the larger value if very high frequency noise is present, since electrolytic capacitors simply have too much inductance at those frequencies. The quality of the power supply voltage should be checked at the IC with a high frequency scope. Noise spikes (always present if digital circuits are near this IC) can easily exceed 400 mV, and if they get into the IC, the output can have noise or distortion. Noise can be reduced by inserting resistors and/or inductors between the supply and the IC.

If switching power supplies are used, there will be spikes of 0.5 V or greater at frequencies of 50 kHz – 1.0 MHz. These spikes are generally more difficult to reduce because of their greater energy content. In extreme cases, a 3-terminal regulator (e.g., MC78L05ACP), with appropriate high frequency filtering, should be used and dedicated to the analog portion of the circuit.

The ripple content of the supply should not allow its magnitude to exceed the values in the Recommended Operating Conditions table.

The PC board tracks supplying V_{CC} and ground to the MC33111 should preferably not be at the tail end of the bus distribution, after passing through a maze of digital circuitry. The analog circuitry containing the MC33111 should be close to the power supply, or the connector where the supply voltages enter the board. If V_{CC} is supplying considerable current to other parts of the board, then it is preferable to have dedicated lines directly to the MC33111 and associated circuitry.

PC Board Layout

Although this device is intended for use in the audio frequency range, the various amplifiers have a bandwidth of ≈ 300 kHz, and can therefore oscillate at frequencies outside the voiceband should there be excessive stray capacitance or other unintended feedback loops. A solid ground plane is strongly recommended to minimize coupling of any digital noise into the analog section. Use of wire wrapped boards should definitely be avoided.

Since many applications of the MC33111 compander involve voice transmission over RF links, care must be taken in the design of the product to keep RF signals out of the MC33111 and associated circuitry. This involves proper layout of the PC boards and the physical arrangement of the boards, shielding, proper RF ground, etc.

DEFINITIONS

Attack Time — The settling time for a circuit after its input signal has been increased.

Attenuation — A decrease in magnitude of a communication signal, usually expressed in dB.

Bandwidth — The range of information carrying frequencies of a communication system.

Channel Separation — The ability of one circuit to reject outputting signals which are being processed by another circuit. Also referred to as crosstalk rejection, it is usually expressed in dB.

Compander — A contraction of the words compressor and expander. A compander is composed of two circuits, one of each kind.

Compressor — A circuit which compresses, or reduces, the dynamic range of a signal by attenuating strong signals and amplifying low level signals.

dB — A power or voltage measurement unit, referred to another power or voltage. It is generally computed as:

$10 \times \log (P_1/P_2)$ for power signals, and

$20 \times \log (V_1/V_2)$ for voltage signals.

dBm — An indication of signal power. 1.0 mW across 600 Ω, or 0.775 Vrms, is typically defined as 0 dBm for telecom applications. Any voltage level is converted to dBm by:

dBm = 20 x log (Vrms/0.775), or

dBm = [20 x log (Vrms)] + 2.22.

dBrn — Indicates a dBm measurement relative to 1.0 pW power level into 600 Ω. Generally used for noise measurements, 0 dBm = – 90 dBm.

dBrnC — Indicates a dBrn measurement using a C-message weighting filter.

Decay Time — The settling time for a circuit after its input signal has been decreased.

Expander — A circuit which expands, or increases the dynamic range of a signal by amplifying strong signals and attenuating low level signals.

Gain — The change in signal amplitude (increase or decrease) after passing through an amplifier, or other circuit stage. Usually expressed in dB, an increase is a positive number, and a decrease is a negative number.

Mute — Reducing the level of an audio signal, generally so that it is inaudible. Partial muting is used in some applications.

Passthrough — Bypassing the compression and/or expansion function by setting the gain to a fixed value (usually unity). This is usually employed when data, rather than voice, is to be transmitted without attenuation.

Power Supply Rejection Ratio — The ability of a circuit to reject outputting noise, or ripple, which is present on the power supply lines. PSRR is usually expressed in dB.

Signal to Noise Ratio — The ratio of the desired signal to unwanted signals (noise) within a defined frequency range. The larger the number, the better.

Voiceband — That portion of the audio frequency range used for transmission in the telephone system. Typically it is 300-3400 Hz.

Zero dB Point — The signal level which has its amplitude unchanged by a compressor or expander.

MC33120

Subscriber Loop Interface Circuit

SUBSCRIBER LOOP INTERFACE CIRCUIT (SLIC)

THIN FILM SILICON MONOLITHIC INTEGRATED CIRCUIT

2

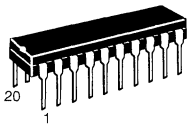
The MC33120 is designed to provide the interface between the 4-wire side of a central office, or PBX, and the 2-wire subscriber line. Interface functions include battery feed, proper loop termination AC impedance, hookswitch detection, adjustable transmit, receive, and transhybrid gains, and single/double fault indication. Additionally the MC33120 provides a minimum of 58 dB of longitudinal balance (4-wire and 2-wire).

The transmit and receive signals are referenced to analog ground, while digital signals are referenced to digital ground, easing the interface to codecs, filters, etc. The 2 status outputs (hookswitch and faults) and the Power Down Input are TTL/CMOS compatible. The Power Down Input permits local shutdown of the circuit.

Internal drivers allow the external loop current pass transistors to be standard bipolar transistors (non-Darlington).

The MC33120 is available in a 20 pin DIP and a 28 pin PLCC surface mount package.

- 58 dB Longitudinal Balance Guaranteed; 4-wire and 2-wire
- Transmit, Receive, and Transhybrid Gains Externally Adjustable
- Return Loss Externally Adjustable
- Proper Hookswitch Detection With 30 kΩ Leakage
- Single/Double Fault Indication With Shutdown for Thermal Protection
- Critical Sense Resistors Included Internally
- Standard Power Supplies: – 42 V to – 58 V, and +5.0 V, ±10%
- On-Hook Transmission
- Power Down Input (TTL and CMOS Compatible)
- Operating Ambient Temperature: – 40°C to +85°C
- Available in a 20 Pin DIP and 28 Pin PLCC Package



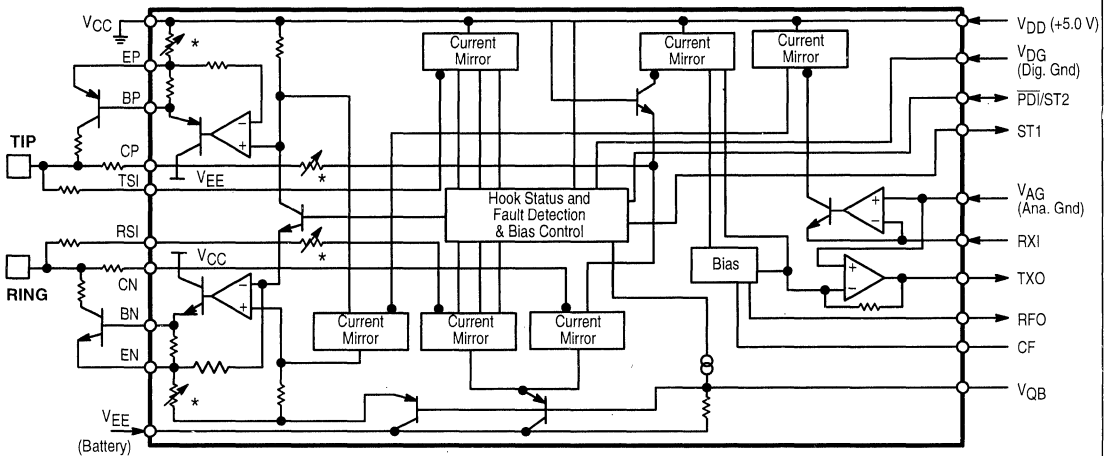
P SUFFIX
PLASTIC PACKAGE
CASE 738

FN SUFFIX
PLCC
CASE 776

ORDERING INFORMATION

Device	Temperature Range	Package
MC33120P	– 40° to +85°C	Plastic DIP
MC33120FN		PLCC

SIMPLIFIED BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Supply Voltage with respect to V_{CC} with respect to V_{DG}	 V_{EE} V_{DD}	 – 60, +0.5 – 0.5, +7.0	Vdc
Input Voltage @ PDI, with respect to V_{DG} @ Pins 1–5, 16–20	V_{in}	 – 0.5, +7.0 V_{EE} to V_{CC}	Vdc
Storage Temperature Range	T_{stg}	– 65 to +150	°C
Junction Temperature	T_J	150	°C

Devices should not be operated at these values. The "Recommended Operating Conditions" table provides conditions for actual device operation.

2

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Voltage (with respect to V_{CC}) (with respect to V_{DG})	 V_{EE} V_{DD}	 – 58 +4.5	 – 48 +5.0	 – 42 +5.5	Vdc
(with respect to V_{CC}) (with respect to V_{CC}) (with respect to V_{AG})	V_{AG} V_{DG}	– 3.0 – 3.0 – 3.0	0 0 0	+10 +7.0 +10	Vdc
(with respect to V_{EE}) (with respect to V_{CC} and V_{AG})	V_{DD}	— +3.5	— —	+63.5 —	Vdc
Loop Current	I_{LOOP}	15	—	50	mA
PDI Input Voltage	V_{PDI}	0	—	V_{DD}	Vdc
Sink Current ST1 ST2	 I_{ST1L} I_{ST2L}	 0 0	 — —	 1.0 1.0	mA
Transmit Signal Level at Tip & Ring Receive Signal Level at V_{RX}	S_{TX} S_{RX}	– 48 – 48	— —	+3.0 +3.0	dBm
Loop Resistance	R_L	0	—	2.0	kΩ
External Transistor Beta	H_{FE}	40	—	500	A/A
Operating Ambient Temperature (See text for derating)	T_A	– 40	—	+85	°C

All limits are not necessarily functional concurrently.

ELECTRICAL CHARACTERISTICS (V_{EE} = – 48 V, V_{DD} = +5.0 V, unless otherwise noted, V_{CC} = V_{AG} = V_{DG} = 0 V, T_A = 25°C, see Figure 1, unless otherwised noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
POWER SUPPLIES					
V_{EE} Current On Hook (R_L > 10 MΩ, V_{EE} = – 58 V) Off Hook (R_L = 0 Ω, V_{EE} = – 58 V)*	 I_{EEN} I_{EEF}	 – 2.7 – 75	 – 1.2 – 58	 — – 45	mA
V_{DD} Current On Hook (R_L > 10 MΩ, V_{DD} = +5.5 V) Off Hook (R_L = 0 Ω, V_{DD} = +5.5 V)	 I_{DDN} I_{DDF}	 — 5.5	 1.4 9.0	 2.7 15	
V_{EE} Ripple Rejection f = 1.0 kHz, at V_{TX} (4-wire) f = 1.0 kHz, at Tip/Ring (2-wire)	PSRR	 40 40	 62 52	 — —	dB
V_{DD} Ripple Rejection f = 1.0 kHz, at V_{TX} (4-wire) f = 1.0 kHz, at Tip/Ring (2-wire)		 37 37	 52 48	 — —	

*Includes loop current.

ELECTRICAL CHARACTERISTICS (V_{EE} = – 48 V, V_{DD} = +5.0 V, unless otherwise noted, V_{CC} = V_{AG} = V_{DG}, T_A = 25°C, see Figure 1)

Characteristic	Symbol	Min	Typ	Max	Unit
LOOP FUNCTIONS					
Loop Current					mA
Maximum (RRF = 4.7 k, R_L = 10 Ω)	I_{LMAX}	41	43	53	
Nominal (RRF = 4.7 k, R_L = 600 Ω)	I_{LOOP}	37	40	48	
Minimum (RRF = 4.7 k, R_L = 1800 Ω)	I_{LMN}	19	21	—	
Battery Feed Resistance (RRF = 4.7 k, R_L = 1800 Ω)*	R_{BF}	475	508	675	Ω
Hookswitch Threshold					kΩ
On-to-Off Hook	R_{NF}	2.0	3.1	—	
Off-to-On Hook	R_{FN}	—	7.0	10	
Fault Detection Threshold					Ω
Ring-to-Ground (R_L = 600 Ω)	R_{RG}	600	660	—	
Tip-to-Battery (R_L = 600 Ω)	R_{TB}	600	660	—	

*Calculated from [(48/I_{LMN}) – 1800]

GAIN LEVELS

Transmit Voltage Gain (CP, CN to TXO)	G_{TX1}	—	0.328	—	V/V
Transmit Voltage Gain (V_{TX}/V_L)	G_{TX2}				dB
V_L = 0 dBm, f = 1.0 kHz		– 0.3	0.0	+0.3	
V_L = 0 dBm, f = 3.4 kHz, with respect to G_{TX2}		– 0.1	0.0	+0.1	
V_L = +3.0 dBm, f = 1.0 kHz, with respect to G_{TX2}		– 0.15	0.0	+0.15	
V_L = – 48 dBm, f = 1.0 kHz, with respect to G_{TX2}		—	±0.1	—	
Transmit Distortion (at Pin 11)	THD_T				%
(f = 300 Hz to 4.0 kHz, – 40 dBm ≤ V_{T-R} ≤ +5.0 dBm)		—	0.05	—	
Receive Current Gain (I_{EP}/I_{RXI})	G_{RX1}	94	102	110	mA/mA
Receive Voltage Gain (V_L/V_{RXI}) (R_L = 600 Ω)	G_{RX2}				dB
V_{RXI} = 0 dBm, f = 1.0 kHz		– 0.3	0.0	+0.3	
V_{RXI} = 0 dBm, f = 3.4 kHz, with respect to G_{RX2}		– 0.1	0.0	+0.1	
V_{RXI} = +3.0 dBm, f = 1.0 kHz, with respect to G_{RX2}		– 0.15	0.0	+0.15	
V_{RXI} = – 48 dBm, f = 1.0 kHz, with respect to G_{RX2}		—	±0.1	—	
Receive Distortion	THD_R	—	0.05	—	%
(f = 300 Hz to 4.0 kHz, – 40 dBm ≤ V_{RXI} ≤ +5.0 dBm)					
Return Loss (Reference = 600 Ω resistive, f = 1.0 kHz)	RL	30	>40	—	dB
Transhybrid Rejection (R_L = 600 Ω, f = 1.0 kHz, Figure 4)	THR	—	44	—	dB

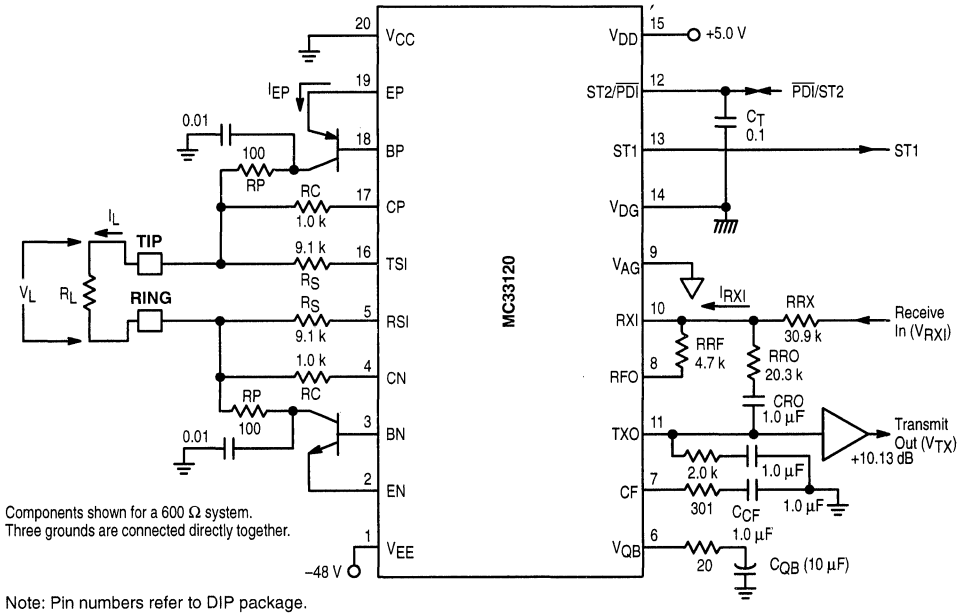
LONGITUDINAL SIGNALS (V_{CM} = 5.12 Vrms, see Figures 1 and 2)

2-Wire Balance, f = 1.0 kHz, Z_{ac} = 600 Ω (@ Tip/Ring)	LB	58	64	—	dB
4-Wire Balance, f = 1.0 kHz, Z_{ac} = 600 Ω (@ V_{TX})		58	64	—	
2-Wire Balance, f = 330 Hz, Z_{ac} = 600 Ω (@ Tip/Ring)		58	64	—	
4-Wire Balance, f = 330 Hz, Z_{ac} = 600 Ω (@ V_{TX})		58	64	—	
2-Wire Balance, f = 3.3 kHz, Z_{ac} = 600 Ω (@ Tip/Ring)		53	60	—	
4-Wire Balance, f = 3.3 kHz, Z_{ac} = 600 Ω (@ V_{TX})		53	60	—	
2-Wire Balance, f = 1.0 kHz, Z_{ac} = 900 Ω (@ Tip/Ring)		—	62	—	
4-Wire Balance, f = 1.0 kHz, Z_{ac} = 900 Ω (@ V_{TX})		—	62	—	
Signal Balance, f = 1.0 kHz (Figure 3)		40	55	—	
Longitudinal Impedance, RS = 9100 Ω	Z_{LONG}	150	180	210	Ω
Maximum Longitudinal Current per side	I_{LM}				mA
f = 1.0 kHz, I_{LOOP} = I_{LMN}, C_T = 0.1 μF		8.5	16	—	

ELECTRICAL CHARACTERISTICS (V_{EE} = – 48 V, V_{DD} = +5.0 V, unless otherwise noted, $V_{CC} = V_{AG} = V_{DG}$, T_A = 25°C, see Figure 1)

Characteristic	Symbol	Min	Typ	Max	Unit
LOGIC INTERFACE					
ST1 Output Voltage					Vdc
Low (I_{ST1} = 1.0 mA, V_{DD} = 5.5 V)	V_{OL}	V_{DG}	0.17	0.4	
High (I_{ST1} = – 100 µA, V_{DD} = 4.5 V)	V_{OH}	2.4	3.2	—	
ST2 Output Voltage					
Low (I_{ST2} = 1.0 mA, V_{DD} = 5.5 V)	V_{OL}	V_{DG}	0.17	0.4	
High (I_{ST2} = – 100 µA, V_{DD} = 4.5 V)	V_{OH}	2.4	4.3	—	
Time Delay					µs
Hookswitch Closure to ST1 Change	t_{ST11}	—	10	—	
Hookswitch Opening to ST1 Change	t_{ST12}	—	200	—	
Hookswitch Closure to 90% of Loop Current (C_T = 0.1 µF)	t_{HS}	—	19	—	ms
PDI Taken High-to-Low to 10% of Loop Current	t_{ST21}	—	18	—	ms
PDI Taken Low-to-High to 90% of Loop Current	t_{ST22}	—	10	—	µs
PDI Input Current	I_{IH}				µA
V_{PDI} = 3.0 V, R_L = 600 Ω, V_{DD} = 5.0 V		– 1250	– 800	– 300	
V_{PDI} = 0 V, R_L = 600 Ω, V_{DD} = 5.5 V		—	– 800	—	
PDI Input Voltage					V
Low	V_{IL}	V_{DG}	—	0.8	
High	V_{IH}	2.0	—	V_{DD}	
MISCELLANEOUS					
V_{QB} Voltage ($V_{QB} - V_{EE}$)	V_{QB}				Vdc
@ I_L = 20 mA		—	0.82	—	
@ I_L = 40 mA		—	0.95	—	
TXO Offset Voltage ($V_{TXO} - V_{AG}$) @ R_L = 600 Ω	V_{TXO}	– 400	+30	+400	mVdc
TXO Output Current	I_{TXO}	±275	±800	—	µA pk
RXI Offset Voltage ($V_{RXI} - V_{AG}$) @ R_L = 600 Ω	V_{RXOS}	—	0.8	—	mVdc
V_{AG} Input Current @ R_L = 600 Ω	I_{VAG}	—	0.2	—	µA
Idle Channel Noise (with C-message filter, R_L = 600 Ω)					dBrnc
@ TXO (Pin 11)	N_{IC4}	—	– 10	—	
@ Tip/Ring	N_{IC2}	—	– 5.0	—	
Thermal Resistance — Junction to Ambient	θ_{JA}				°C/W
(Either package, in still air, soldered to a PC board) (@ T_A = +25°C)		—	62	—	
(@ T_A = +85°C)		—	36	—	

FIGURE 1 — TEST CIRCUIT



Note: Pin numbers refer to DIP package.

FIGURE 2 — LONGITUDINAL BALANCE TEST

(Per IEEE-455)

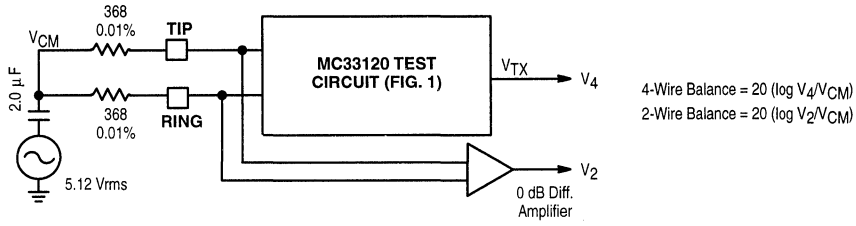


FIGURE 3 — SIGNAL BALANCE TEST

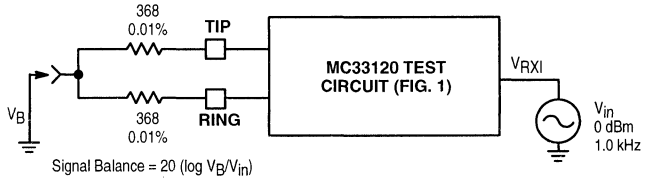
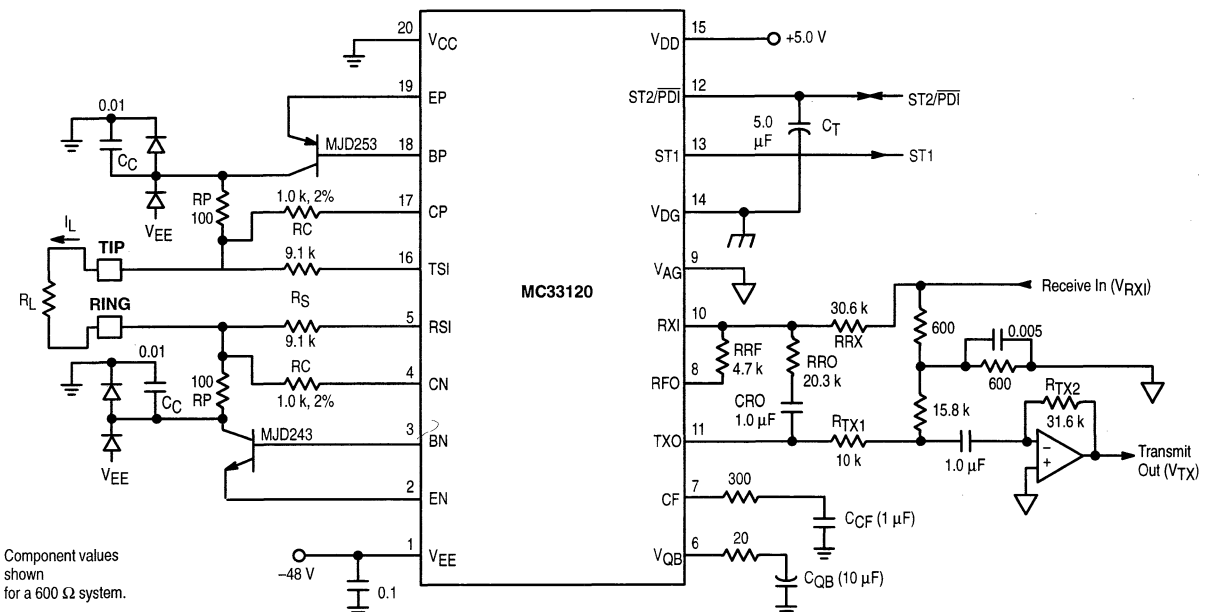


FIGURE 4 — APPLICATION CIRCUIT



Note: Pin numbers refer to DIP package.

PIN DESCRIPTION

Name	Pin		Description
	DIP	PLCC	
V_{CC}	20	28	Connect to noise-free Battery ground. Carries loop current and some bias currents.
EP	19	27	Connect to the emitter of the PNP pass transistor.
BP	18	26	Connect to the base of the PNP pass transistor.
CP	17	24	Connect to TIP through a current limiting protection resistor (R_C). CP is the noninverting input to the internal transmit amplifier (Figure 28). Input impedance is 31 kΩ.
TSI	16	23	Sense input. Connect to TIP through a current limiting protection resistor (R_S) which also sets the longitudinal impedance. Input impedance is ≈100 Ω to V_{CC}.
V_{DD}	15	22	Connect to a +5.0 V, ±10% supply, referenced to digital ground. Powers logic section and provides some bias currents for the loop current drivers.
V_{DG}	14	20	Digital Ground. Reference for ST1, ST2 and V_{DD}. Connect to system digital ground.
ST1	13	18	Status Output (TTL/CMOS). Indicates hook switch status — High when on-hook, low when off-hook, and pulse dialing information. Used with ST2 to indicate fault conditions.
ST2/PDI	12	17	Status output **and** an input (TTL/CMOS). As an output, ST2 can indicate hook status — Low when on-hook, high when off-hook. Used with ST1 to indicate fault conditions. As an input, it can be taken low (when off-hook) to deny subscriber loop current.
TXO	11	16	Transmit voltage output. Amplitude is ≈1/3 that across CP and CN. Nominally capable of 800 μA output current. DC referenced to V_{AG}.
RXI	10	14	Receive current input. Current at this pin is multiplied by 102 at EP and EN to generate loop current. RXI is a virtual ground at V_{AG} level. Current flow is **out** of this pin.
V_{AG}	9	13	Analog ground, reference for TXO and RXI. Connect to system analog ground.
RFO	8	12	A resistor between this pin and RXI sets the maximum loop current and DC feed resistance. Minimum resistor value is 3.3 k (see Figures 5–7).
CF	7	10	A low leakage capacitor between this pin and V_{AG} provides DC and AC signal separation. A series resistor is required for battery supply turn-on/off transient protection (Figure 4).
V_{QB}	6	8	Quiet Battery. A capacitor between V_{QB} and V_{CC} filters noise and ripple from V_{EE}, providing a quiet battery source for the speech amplifiers. A series resistor is required for battery supply turn-on/off transient protection (Figure 4).
RSI	5	7	Sense input. Connect to RING through a current limiting protection resistor which also sets the longitudinal impedance. Input impedance is ≈100 Ω to V_{QB}.
CN	4	6	Connect to RING through a current limiting protection resistor. CN is the inverting input to the internal transmit amplifier (Figure 28). Input impedance is 31 kΩ.
BN	3	4	Connect to the base of the NPN pass transistor.
EN	2	3	Connect to the emitter of the NPN pass transistor.
V_{EE}	1	2	Connect to battery voltage. Nominally – 48 V, it can range from – 42 to – 58 V.

(Pins 1, 5, 9, 11, 15, 19, 21, and 25 are not internally connected on the PLCC package).

FIGURE 5 — LOOP CURRENT versus LOOP RESISTANCE AND RRF

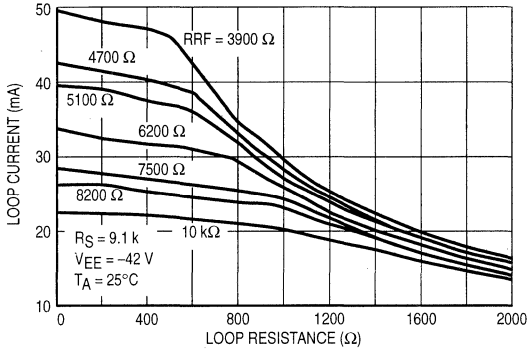


FIGURE 6 — LOOP CURRENT versus LOOP RESISTANCE AND RRF

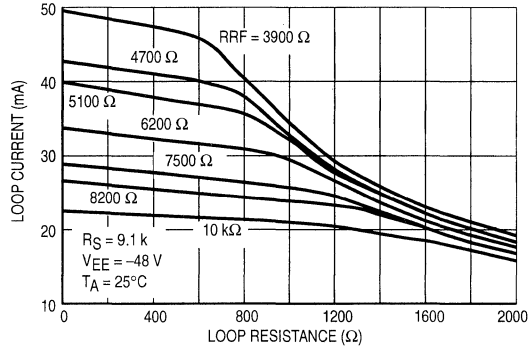


FIGURE 7 — LOOP CURRENT versus LOOP RESISTANCE AND RRF

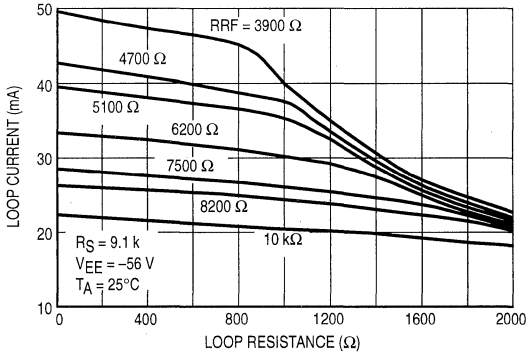


FIGURE 8 — OFF-HOOK TO ON-HOOK THRESHOLD versus RRF

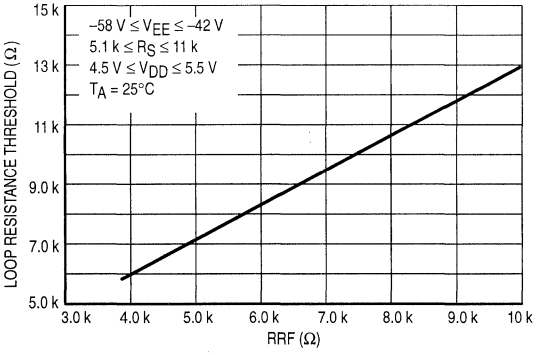


FIGURE 9 — ON-HOOK TO OFF-HOOK THRESHOLD versus R_S

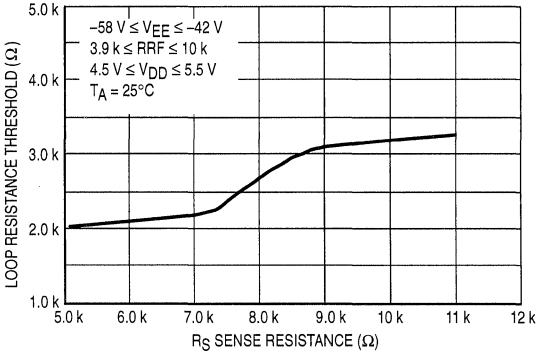


FIGURE 10 — I_{DD} versus LOOP CURRENT

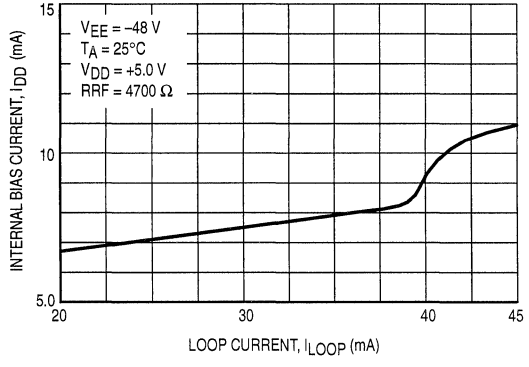


FIGURE 11 — FAULT THRESHOLD (ON-HOOK) versus R_S

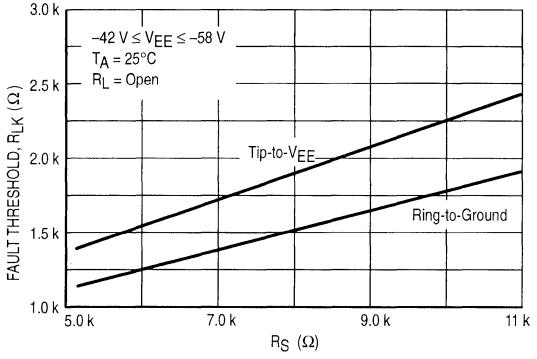


FIGURE 12 — FAULT THRESHOLD (OFF-HOOK) versus LOOP RESISTANCE

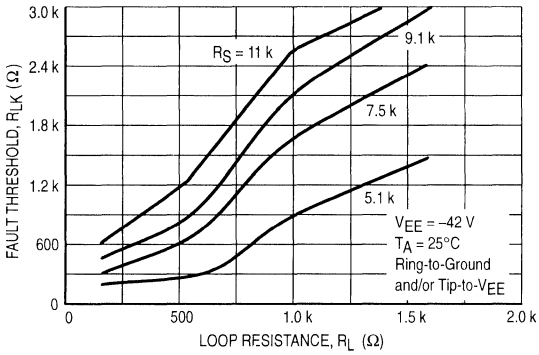


FIGURE 13 — FAULT THRESHOLD (OFF-HOOK) versus LOOP RESISTANCE

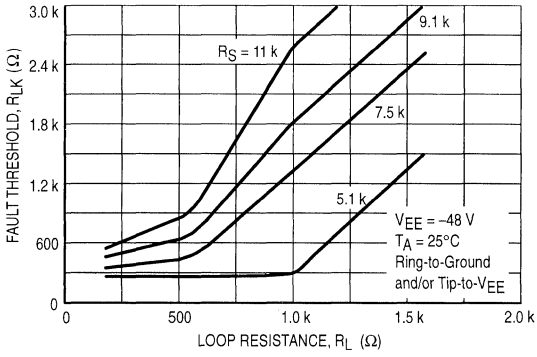


FIGURE 14 — FAULT THRESHOLD (OFF-HOOK) versus LOOP RESISTANCE

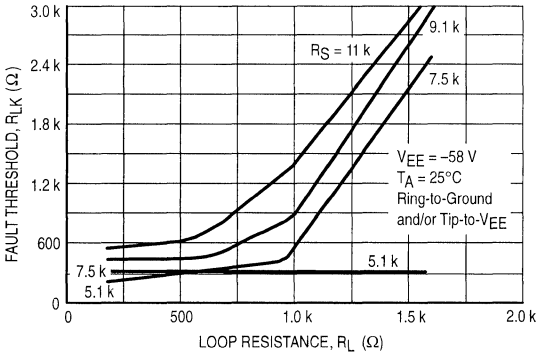


FIGURE 15 — FAULT THRESHOLD (OFF-HOOK) versus R_S

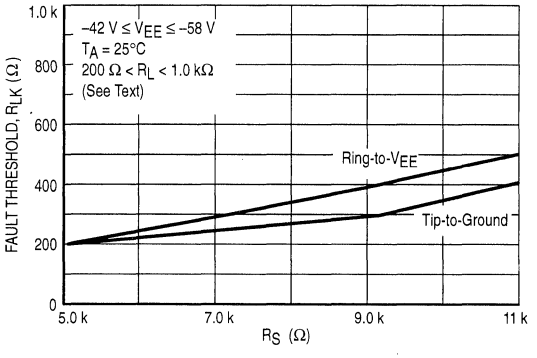


FIGURE 16 — V_{DD} RIPPLE REJECTION versus FREQUENCY

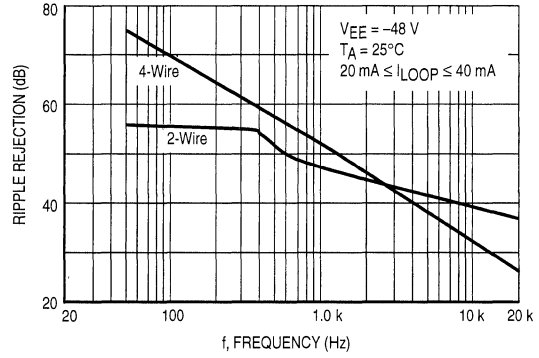


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FIGURE 17 — V_{EE} RIPPLE REJECTION versus FREQUENCY

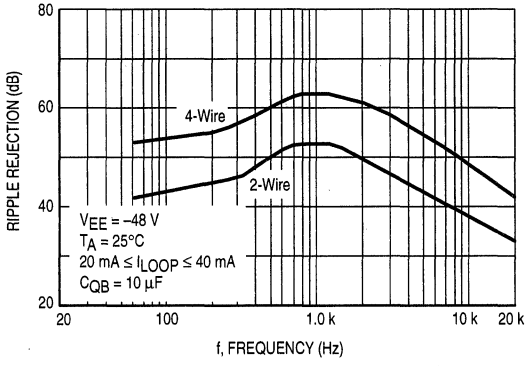


FIGURE 18 — V_{EE} RIPPLE REJECTION versus FREQUENCY AND C_{QB}

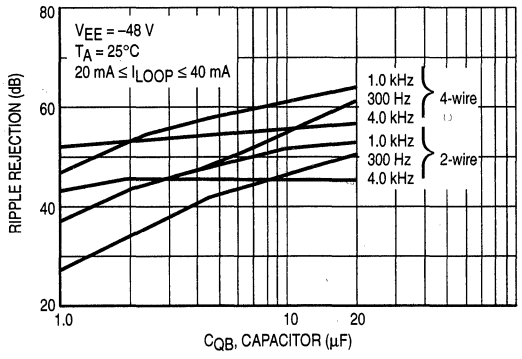


FIGURE 19 — ST1, V_{OL} versus I_{OL}

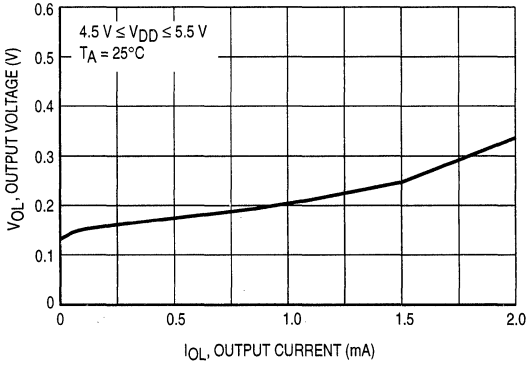


FIGURE 20 — ST1, V_{OH} versus I_{OH}

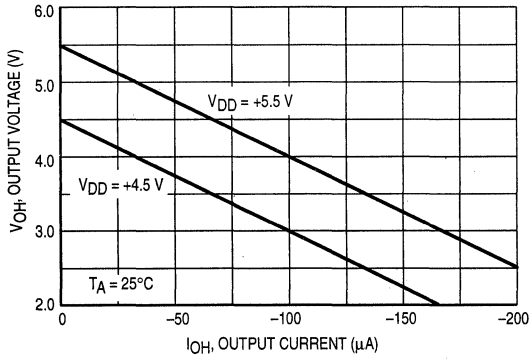


FIGURE 21 — ST2, V_{OL} versus I_{OL}

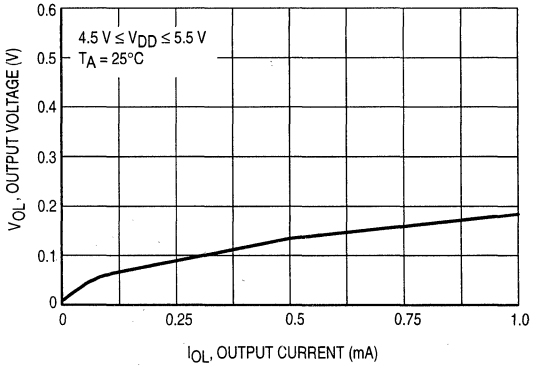


FIGURE 22 — ST2, V_{OH} versus I_{OH}

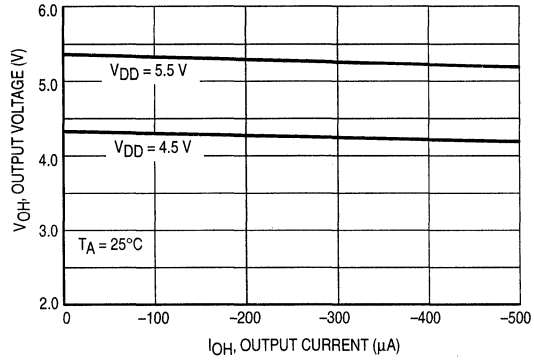


FIGURE 23 — IC POWER DISSIPATION versus LOOP RESISTANCE AND V_{EE}

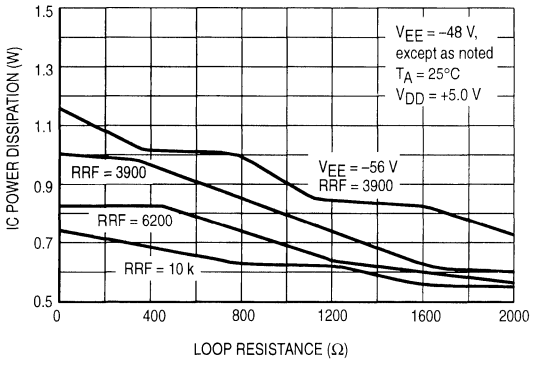


FIGURE 24 — TRANSISTOR POWER DISSIPATION versus LOOP RESISTANCE AND RRF

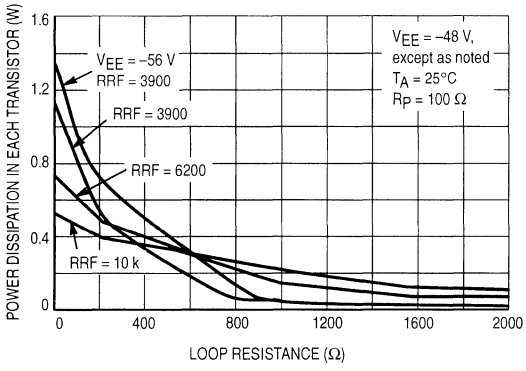


FIGURE 25 — MAXIMUM LONGITUDINAL CURRENT versus LOOP CURRENT

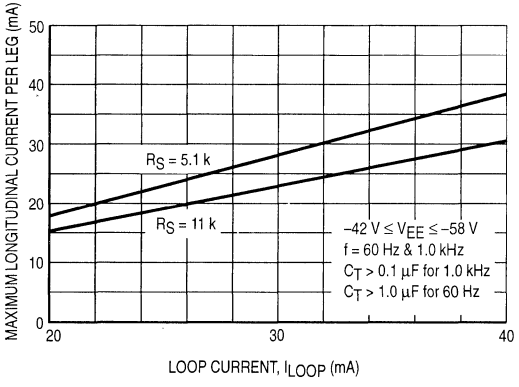
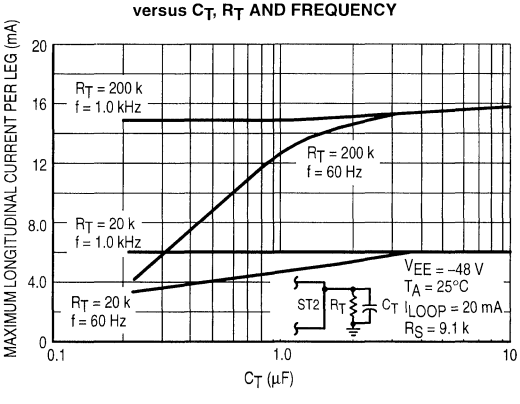


FIGURE 26 — MAXIMUM LONGITUDINAL CURRENT versus C_T, R_T AND FREQUENCY



2

FUNCTIONAL DESCRIPTION

Introduction

The MC33120 is a solid state SLIC (Subscriber Line Interface Circuit) which provides the interface between the two wire telephone line and the four wire side of a Central Office or PBX. Most of the BORSCHT functions are provided, specifically:

— **B**attery feed of the loop current to the line, with programmable maximum current for short lines and battery feed resistance for long lines.
— **O**vervoltage protection through internal clamp diodes and external resistors and diodes.
— **S**upervision, in that hook status is indicated in the presence of ≥30 kΩ leakage, and regardless of whether or not the circuit is powered down intentionally by the Central Office or PBX. Fault conditions are detected and indicated to the system. Dialing (pulse and DTMF) information is passed through the MC33120 to the 4-wire side.
— **H**ybrid function, in that the MC33120 is a 2-to-4 wire converter. Transmit, receive, return loss, and transhybrid gains are independently adjustable.

The MC33120 does not provide ring insertion, ring trip, digital coding/decoding of the speech signals, nor test functions. These must be provided external to this device.

The MC33120 controls two external transistors (one NPN and one PNP) through which the loop current flows. By appropriate circuit design, the power dissipation (which can exceed 3.0 watts under certain worst case conditions) is approximately equally distributed among the two transistors and the IC, thereby lowering junction temperatures and increasing long term reliability. In most situations, heatsinks will not be required.

The MC33120 incorporates critical sense resistors internally, which are trimmed for optimum performance. With this technique, the external resistors on the two wire side, which generally must be high wattage for transient protection reasons, can be non-precision.

Longitudinal balance is tested to a minimum of 58 dB @ 1.0 kHz (refer to Electrical Characteristics and Figure 1) for both the two wire and four wire side, and typically measures in the mid-60s. The longitudinal current capability is tested to a minimum of 8.5 mArms per side (refer to Electrical Characteristics and Figure 1) at a loop current of 20 mA.

Following is a description of the individual sections. Figure 4 is the reference schematic.

DC Loop Current

The DC loop current is determined by the battery voltage (V_{EE}), the load resistance across Tip and Ring, and the resistor at RFO. Varying the 4 resistors R_S and RC will influence the loop current a small amount (<5%). The curves of Figures 5–7 indicate the loop current versus loop resistance, different values of RRF, and for various values of V_{EE}. The graphs represent performance at T_A = 25°C and after the IC had reached a steady state temperature (>5 minutes).

FIGURE 27 — DC LOOP CURRENT PATH

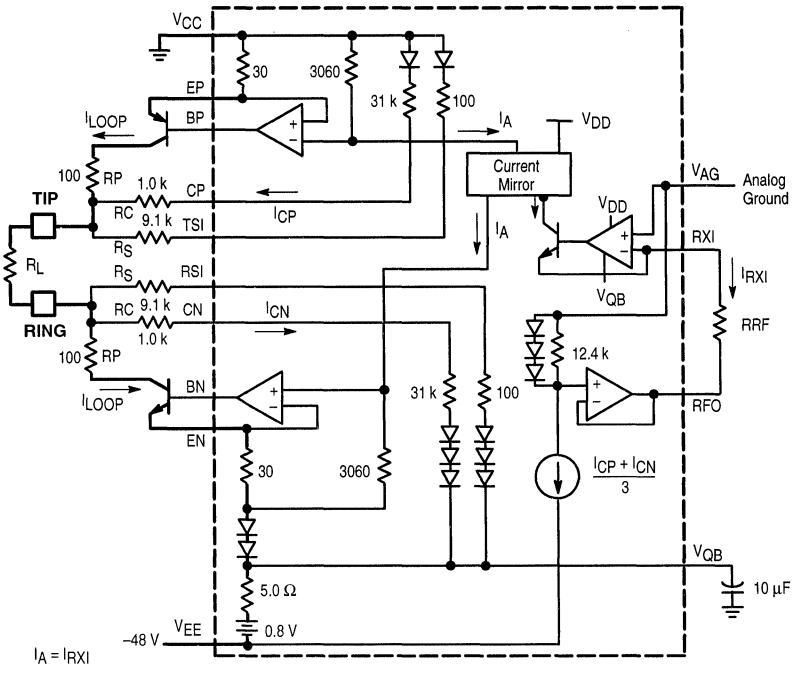


Figure 27 is representative of the DC loop current path (bold lines). On a long line (R_L > 1.0 kΩ), the loop current can be determined from the following equation:

$$I_{LOOP} = \frac{(|V_{EE}| - 3.6\ V) \bullet 13}{RRF + \{(R_L + 5) \bullet 13\}} \qquad \text{(Equation 1)}$$

On short lines (R_L < 1.0 kΩ), the three diodes across the 12.4 k resistor clamp the voltage at RFO, thereby preventing the RXI current from increasing as the load resistance is decreased. The maximum loop current is:

$$I_{LOOP\ (MAX)} = \frac{1.85\ V \bullet 102}{RRF} \quad (T_A = 25°C) \qquad \text{(Equation 2)}$$

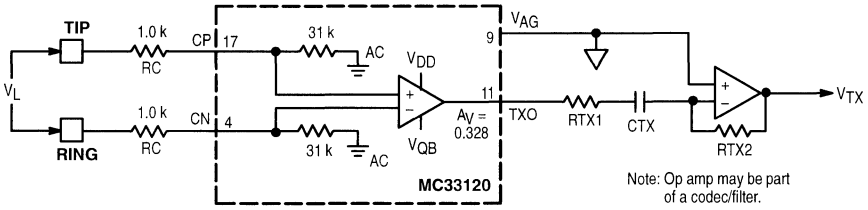
Due to the temperature dependence of a diode's forward voltage, the maximum loop current will change with temperature by ≈ –0.3%/°C.

The battery feed resistance ($\Delta V_{TIP}/\Delta I_L$) is ≈400 Ω, but depends on the loop current, V_{EE}, RRF, and is a valid parameter only on long lines where the current limit is not in effect. On short lines, the feed resistance is high since the loop current is clamped at a constant level. The AC impedance (Return Loss) however, is not determined nor affected by the DC parameters. See the Applications Section for Return Loss information.

Transmit Path

The transmit path, shown in Figure 28, consists of an internal amplifier which has inputs at CP and CN, and its output at TXO. The gain is internally fixed at 0.328 V/V (–9.7 dB). The output is in phase with the signal at CP (normally the same as TIP), and is out of phase with the signal at CN. The signal at TXO is also out of phase with that at V_{RX}, the receive signal input, described in another section.

FIGURE 28 — TRANSMIT PATH



The TXO output can swing ≈3.0 Vp-p, with a nominal current capability of ±800 µA peak (±275 µA minimum). The load on TXO is the parallel combination of RTX1 and the RRO network (described later). TXO is nominally internally biased at the V_{AG} DC level, but has an offset which varies with loop current.

In normal applications, the signal at CP/CN is reduced slightly from that at Tip/Ring by the voltage divider composed of the external RC resistors, and the internal 31 k resistors. The value of the RC resistors depends on the transient protection needed, described in another section, with 1.0 kΩ resistors being suitable for most applications. The resulting signal at TXO needs to be gained up to obtain 0 dB from Tip/Ring to V_{TX} (the 4-wire output). The common method involves an external op amp, as shown in Figure 28, with a gain of RTX2/RTX1. The gain from V_L to V_{TX} is:

$$\frac{V_{TX}}{V_L} = \frac{RTX2 \bullet 31\ k \bullet 0.328}{RTX1 \bullet (RC + 31\ k)} \qquad \text{(Equation 3)}$$

If a codec/filter is used, many of which include an internal op amp, a separate op amp is not needed. CTX is primarily for DC blocking (of the TXO offset), and is usually large (1.0 µF) so as to not affect the gain.

Receive Path

The receive path, shown in Figure 29, consists of the input at RXI, the transistor driver amplifiers, the external transistors, and the load at Tip/Ring.

RXI is a virtual ground (DC level = V_{AG}) and is a current input. Current flow is **out** of the pin. The RXI current is mirrored to the two transistor drivers which provide a gain of 102. The two external transistors are then two current sources, in series, operating at the same value. An additional internal circuit (not shown) balances the two current sources to maintain operation in their linear region.

The load current (through R_L) is slightly different from the transistor current due to the sense resistors RC and RS. The sense resistors add to the DC loop current, but subtract from the AC load current.

In normal operation, the current at RXI is composed of a DC current (from RFO), an AC current (from V_{RX}) which is the receive signal, and an AC current from TXO, which is the feedback signal to set the return loss (setting the return loss is discussed in the section on AC Terminating Impedance). The resulting AC signal at Tip is inverted from that at V_{RX}, while the signal at Ring is in phase with V_{RX}.

The resistors RP are for transient protection, and their value (defined in another section) depends on the amount of protection required. A nominal value of 100 Ω is suitable for most applications.

The system receive gain, from V_{RX} to Tip/Ring, is not described in this section since in normal applications, it involves the feedback which sets the AC terminating impedance. The Applications Section discusses these in detail.

Logic Interface (Hook status, pulse dialing, faults)

The logic interface section provides hookswitch status, fault information, and pulse dialing information to the 4-wire side of the system at the ST1 and ST2 outputs. Figure 30 is a representative diagram.

FIGURE 29 — RECEIVE PATH

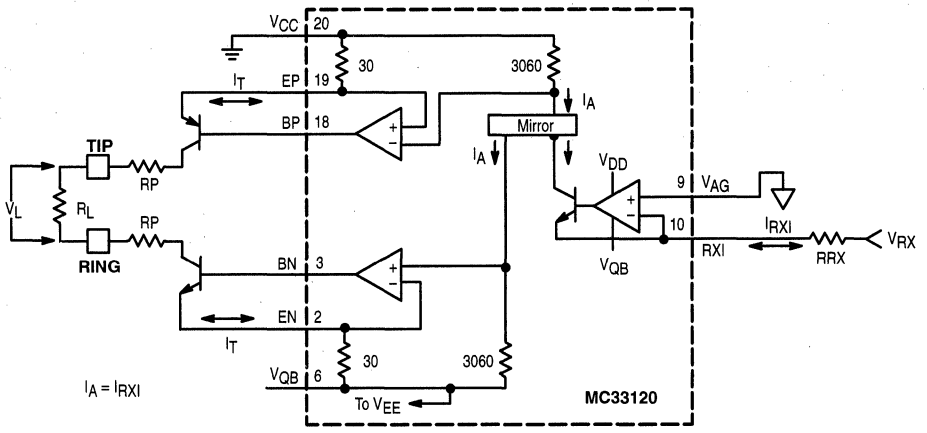
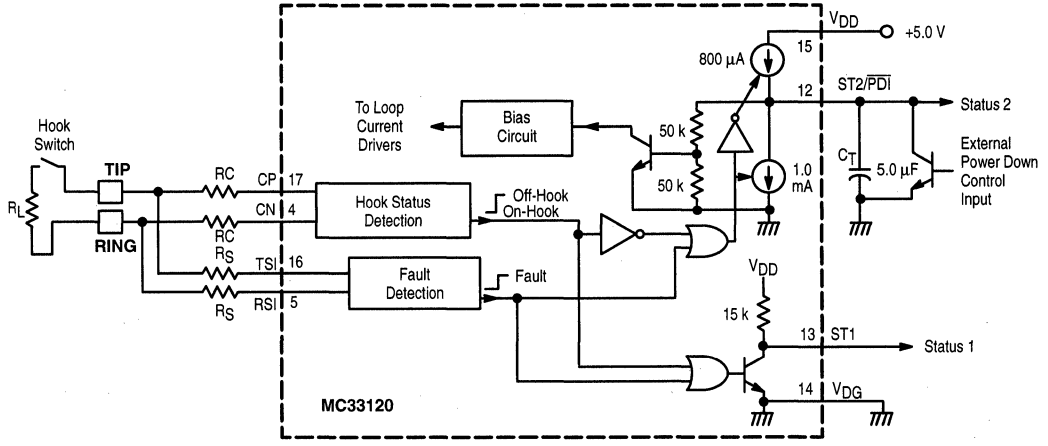


FIGURE 30 — LOGIC INTERFACE



The logic outputs operate according to the truth table in Table 1:

TABLE 1 — STATUS OUTPUT TRUTH TABLE

Hook Status	Fault Detection	Outputs ST1	Outputs ST2	Circuit Condition
On Hook	No Fault	Hi	Lo	Internally powered down
Off Hook	No Fault	Lo	Hi	Powered up
On Hook	Fault	Lo	Lo	Internally powered down
Off Hook	Fault	Lo	Lo	Internally powered down

Referring to Figure 30, ST1 is configured as an active NPN pulldown with a 15 kΩ pullup resistor. ST2 has a 800 µA current source pullup, and a 1.0 mA current source for a pulldown. Current limiting this output controls the discharge from the external capacitor when ST2 switches low.

The condition where both ST1 and ST2 are high is not valid, but may occur momentarily during an off-hook to on-hook transition. The condition where both ST1 and ST2 are low may occur momentarily during an on-hook to off-hook transition — this should not be interpreted as a fault condition. ST1 and ST2 are TTL/CMOS compatible and are powered by the +5.0 V supply (V_{DD}). Refer to the Applications Section for more details.

Power Supplies, Grounds

The MC33120 requires 2 power supplies: battery voltage between – 42 V and – 58 V (V_{EE}), and an auxiliary voltage between +4.5 V and +5.5 V (V_{DD}).

V_{EE} is nominally – 48 V, with a typical range of – 42 V to – 58 V, and must be referenced to V_{CC} (battery ground). A 0.1 µF bypass capacitor should be provided between V_{CC} and V_{EE}. The V_{EE} current (I_{EE}) is nominally 1.2 mA when on-hook, 10 to 14 mA more than the loop current when off-hook, and ≈8.0 mA when off-hook but powered down by using the PDI pin. Ripple and noise rejection from V_{EE} is a minimum of 40 dB (with a 10 µF capacitor at V_{QB}), and is dependent on the size and quality of the V_{QB} capacitor (C_{QB}) since V_{QB} is the actual internal supply voltage for the

speech amplifiers. The absolute maximum for V_{EE} is – 60 V, and should not be exceeded by the combination of the battery voltage, its tolerance, and its ripple.

V_{DD} is normally supplied from the line card's digital +5.0 V supply, and is referenced to V_{DG} (digital ground). A 0.1 μF capacitor should be provided between V_{DD} and V_{DG}. The V_{DD} current (I_{DD}) is nominally 1.7 mA when on-hook and between 6.0 and 11 mA when off-hook (see Figure 10). When the MC33120 is intentionally powered down using the PDI pin, I_{DD} changes by <1.0 mA from the normal off-hook value.

V_{AG} is the analog ground for the MC33120, and is the reference for the speech signals (RXI and TXO). Current flow is **into** the pin, and is typically <0.5 μA.

Normally, V_{CC}, V_{DG} and V_{AG} are to be at the same DC level. However, if strong transients are expected at Tip and Ring, as in a Central Office application, V_{CC} should not be connected directly to V_{DG} and V_{AG} in order to prevent possible damage to the +5.0 V system. The MC33120 is designed to tolerate as much as ±30 V between V_{CC} and the other two grounds **on a transient basis only.** This feature permits V_{CC} and the other grounds to be kept separate (on an AC basis) on the line card by transient suppressors, or to be connected together farther into the system (at the power supplies). See the Applications Section on ground arrangements and transient protection for further information on connecting the MC33120 to the system supplies.

For operation of the MC33120 at supply voltages other than – 42 to – 58 V (such as – 24 V or – 28 V), contact your local Motorola sales office.

2

APPLICATIONS INFORMATION

This section contains information on the following topics:

Design Procedure
Power Dissipation Calculations and Considerations
Selecting the Transistors
Longitudinal Current Capability
PC Board Layout Considerations
Alternate Circuit Configurations

Design Procedure

This section describes the step-by-step sequence for designing in the MC33120 SLIC into a typical line card application for either a PBX or Central Office. The sequence is important so that each new component value which is calculated does not affect components previously determined. Figure 4 (Typical Application Circuit) is the reference circuit for most of this discussion. The recommended sequence (detailed below), consists of establishing the DC aspects first, and then the AC aspects:

1) Determine the maximum loop current for the shortest line, select RRF. Power dissipation must be considered here.
2) Select the main protection resistors (RP), and diodes, based on the expected transient voltages. Transient protection configuration must also be considered here.
3) Select RC based on the expected transient voltages.
4) Select RS based on the desired longitudinal impedance at Tip and Ring. Transient voltages are also a factor here.
5) Calculate RRO based on the desired AC terminating impedance (return loss).
6) Calculate RRX based on the desired receive gain.
7) Calculate RTX2 and RTX1 based on the desired transmit gain.
8) Calculate the balance resistor (RB), or network, as appropriate for desired transhybrid rejection.
9) Logic Interface

Preliminary

There is a primary AC feedback loop which has its main sense points at CP and CN (see Figure 34). The loop extends from there to TXO, through RRO to RXI, through the internal amplifiers to the transistor drivers, through RP to Tip and Ring, and through the RCs to CP and CN. Components within this loop, such as RP, RC, the transistors, and the compensation capacitors need not be tightly matched to each other in order to maintain good longitudinal balance. The tolerance requirements on these components, and others, are described in subsequent sections. Any components, however, which are placed **outside** the loop for additional line card functions, such as test relay contacts, fuses, resistors in series with Tip and Ring, etc. will affect longitudinal balance, signal balance, and gains if their values and mismatch is not carefully considered. The MC33120 cannot compensate for mismatch among components outside the loop.

The compensation capacitors (0.01 μF) shown at the transistor collectors (Figure 4) compensate the transistor driver amplifiers, providing the required loop stability. The required tolerance on these capacitors can be determined from the following guidelines:

A 10% mismatch (±5% tolerance) will degrade the longitudinal balance by ≈1.0 dB on a 60 dB device, and by ≈3.0 dB on a 70 dB device.

A 20% mismatch (±10% tolerance) will degrade the longitudinal balance by ≈3.0 dB on a 60 dB device, and by ≈6.0 dB on a 70 dB device.

High quality ceramic capacitors are recommended since they serve the secondary function of providing a bleedoff path for RF signals picked up on the phone line. These capacitors should be connected to a good quality RF ground.

The capacitors used at C_{QB} and C_F must be low leakage to obtain proper performance. Leakage at the C_{QB} capacitor will affect the DC loop current characteristics, while leakage at the C_F capacitor will affect the AC gain parameters.

1) Maximum Loop Current and Battery Feed Resistance

The maximum loop current (at R_L = 0) is determined by the RRF resistor between RFO and RXI. The current limit is accomplished by three internal series diodes (see Figure 27) which clamp the voltage across RRF as the loop resistance decreases, thereby limiting the current at RXI. Since the loop current is 102 x I_{RXI}, the loop current is therefore clamped. The graphs of Figures 5–7 indicate the maximum loop current at an ambient temperature of +25°C, and after the IC has reached thermal equilibrium (approx. 10 minutes).

Although the maximum loop current is primarily a function of the RRF resistor, it is also affected by ambient tempera-

ture, and slightly by V_{EE}. The ambient temperature effects are due to the temperature dependence of the diodes' forward voltage drop, causing the maximum loop current to change by ≈ – 0.3%/°C. Changing V_{EE} affects the maximum current in that the power dissipation is changed, thereby changing the die temperature, which affects the diodes' voltage.

The maximum loop current is affected slightly (<5%) by the choice of the RS and RC resistors, since the sense currents through those resistors add to the current supplied by the transistors.

The battery feed resistance is determined by RRF, and is not adjustable independently of the current limit. Defined as $\Delta V_{TIP}/\Delta I_L$, it is ≈400 Ω, and is a valid parameter only on long lines where the current limit is not in effect. On short lines, the feed resistance is high since the loop current is clamped at a near constant level. The AC impedance (return loss) however, is not determined nor affected by these DC parameters. Return loss is discussed in another section.

If the application requires that the current limit value have a low temperature dependence, refer to the section following this design sequence which describes an alternate configuration.

2) Main Protection Resistors (RP) and Transient Currents

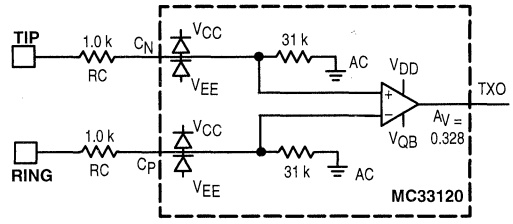
The purpose of the protection resistors (RP), along with the 4 clamp diodes shown in Figure 4, is to absorb the bulk of the transient energy when transient voltages come in from the phone line. The resistor value must be selected to limit the transient current to a value which can be tolerated by the diodes, while dissipating the energy. The recommended value shown (100 Ω) will limit the current from a 1500 V transient to 15 A, which can be carried by 1N4002 diodes under surge conditions. The resistors must be of a type which can tolerate the high instantaneous energy associated with transients. Resistor manufacturers should be consulted for this information.

Referring to Figure 4, a positive transient on either Tip or Ring, or both, will cause the transient current to be delivered to Ground. A negative transient will cause the transient current to come from the V_{EE} supply line. Therefore, the PC board track supplying V_{CC} and V_{EE} to the MC33120 must be designed to carry the transient currents as well as the normal operating currents. Additionally, since a negative transient will cause a current flow **out** of the power supply's negative output, which is opposite to the normal flow of current, provisions must be made for this reverse current flow. One suggested method is to place a zener transient suppressor (1N6290A) across the battery supply pins (V_{CC} to V_{EE}) **physically adjacent to the MC33120.** The inductance associated with PC board tracks and wiring will result in insufficient protection for the MC33120 if the suppressor is located at the opposite end of the line card, or at the power supplies.

Transient currents can be reduced by increasing the value of RP, with an upper limit determined by the DC conditions on the longest line (highest loop resistance) and minimum V_{EE} supply voltage. These conditions determine the minimum DC voltage across the transistors, which must be sufficient to handle the largest AC (transmit and receive) signals. If too large a value is selected for RP, the AC signals will be clipped. It is recommended that each transistor have no less than one volt (DC) across their collector to emitter. System AC specifications may require more than this.

Since the RP resistors are within the loop, their tolerance can be ±5% with no substantial degradation of longitudinal balance. A ±10% tolerance (20% mismatch) will degrade balance by ≈4.0 dB on a 65 dB device.

FIGURE 32 — RC PROTECTION RESISTORS



3) Selecting the RC Resistors

The primary purpose of the RC resistors is to protect the CP and CN pins from transient voltages and destructive currents. Internally, these pins have clamp diodes to V_{CC} and V_{EE} rated for a maximum of 1.0 A under surge conditions only (Figure 32). The 1.0 kΩ resistors shown in the figures, for example, will provide protection against surges up to 1.0 kV. Resistor manufacturers must be consulted for the proper type of resistor for this environment.

The RC resistors are in series with internal 31 kΩ resistors, and therefore form a voltage divider to the inputs of the transmit amplifier, as shown in Figure 32. This will affect the transmit gain, receive gain, return loss, and transhybrid rejection (described in subsequent sections). The tolerance of the RC resistors depends on the value selected for them, since any mismatch between them will create a differential voltage at CP and CN when longitudinal voltages are present on Tip and Ring. To ensure a minimum of 58 dB of longitudinal balance, the resistors' absolute value must not differ by more than 39 Ω. With a nominal value of 1.0 kΩ, their tolerance must be ±2%, or less. If their nominal value is 390 Ω or less, their tolerance can be ±5%.

4) Longitudinal Impedance (Z_{LONG}) — Selecting the RS Resistors

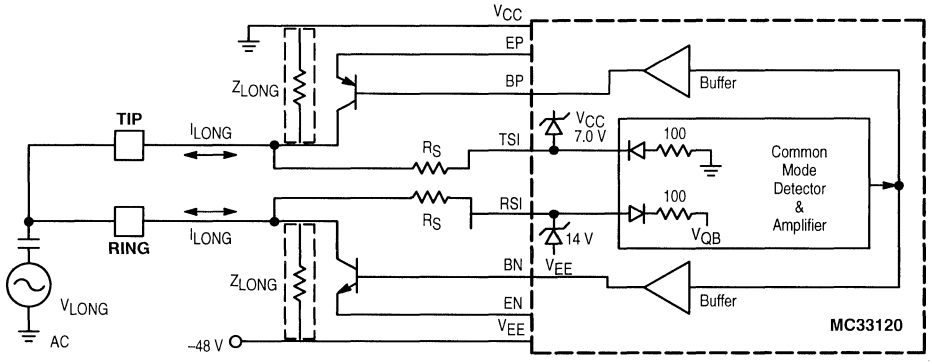
The longitudinal impedance is determined by the RS resistors at the TSI and RSI pins according to the following equation:

$$Z_{LONG} = \frac{RS + 100}{51} \qquad \text{(Equation 4)}$$

Z_{LONG} is defined as V_{LONG}/I_{LONG} as shown in Figure 33; for RS = 9.1 kΩ, Z_{LONG} = 180 Ω. The calculated value of Z_{LONG} includes the fact that the RS resistors are in parallel with the synthesized impedance. The tolerance of the RS resistors therefore depends on how much mismatch can be tolerated between the longitudinal impedances at Tip and at Ring. Calculations indicate the two RS resistors can have a ±5% tolerance, and still comfortably provide a minimum of 58 dB longitudinal balance.

The resistors must be able to withstand transient voltages expected at Tip and Ring. The TSI and RSI pins have internal clamp diodes rated for a maximum of 1.0 A under surge conditions only (Figure 33). Resistor manufacturers must be consulted for the proper type of resistor for this environment.

FIGURE 33 — LONGITUDINAL IMPEDANCE



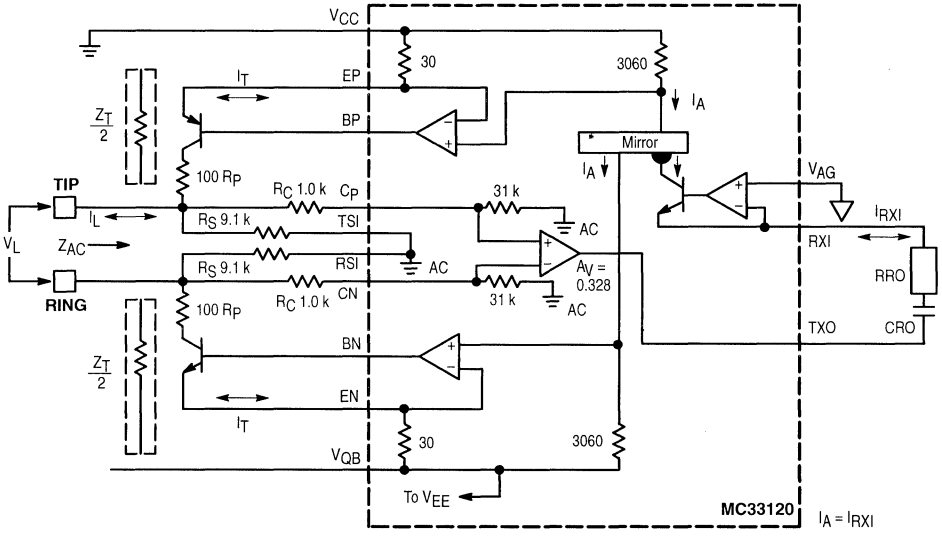
5) AC Terminating Impedance and Source Impedance (Z_{ac}) — Return Loss

The return loss measurement is a measure of how closely the AC impedance of the SLIC circuit matches the characteristic impedance of the phone line, or a reference impedance. The reference impedance can be, in some cases, a pure resistance (commonly 600 Ω or 900 Ω), a series resistor and capacitor (900 Ω + 2.16 μF), or a more complex network.

To achieve proper return loss with the MC33120, the RRO impedance shown in Figure 34 is to have the same configuration as the reference impedance, but with values scaled according to the equations mentioned below.

CRO, used primarily for DC blocking, is generally a large value (1.0 μF) so as to not affect the impedance of RRO. However, it can be included in the RRO network if a complex network is required.

FIGURE 34 — AC TERMINATING IMPEDANCE



Z_{ac} is the impedance looking into the circuit from Tip and Ring (set by RRO), and is defined as V_L/I_L. Half of Z_{ac} is from Tip to V_{CC}, and the other half is from Ring to V_{QB} (an AC ground). Each half is made up of a synthesized impedance ($Z_T/2$) in parallel with R_S and (RC + 31 k).

Therefore Z_{ac} is equal to:

$$Z_{ac} = [Z_T/2 \,//R_S//(RC + 31\ k)] \bullet 2 \qquad \text{(Equation 5)}$$

$$\text{and}\ \frac{Z_T}{2} = \frac{\{R_S//(RC + 31\ k)\} \bullet (Z_{ac}/2)}{\{R_S//(RC + 31\ k)\} - (Z_{ac}/2)} \qquad \text{(Equation 6)}$$

The synthesized impedance Z_T is created as follows:

An incoming signal V_L produces a differential voltage at CP and CN, and therefore at TXO equal to:

$$V_{TXO} = \frac{V_L \bullet 31\ k \bullet 0.328}{(RC + 31\ k)} \qquad \text{(Equation 7)}$$

The signal at TXO creates an AC current I_{RXI} through RRO. RXI is a virtual ground, and CRO is insignificant for first order calculations.

I_{RXI} is gained up by a factor of 102 to produce the current I_T through the transistors.

Z_T is therefore V_L/I_T. The relationship between Z_T and RRO is:

$$RRO = \frac{Z_T \bullet 1.037 \bullet 10^6}{(31\ k + RC)} \qquad \text{(Equation 8)}$$

While equation 8 gives the exact value for RRO, a first order approximation is $Z_{ac} \bullet 33.5$.

a) Resistive Loads (with RC = 1.0 k, R_S = 9.1 k):

For a 600 Ω resistive system, Z_T calculates to 626 Ω, and RRO calculates to 20.3 kΩ.

For a 900 Ω resistive system, Z_T calculates to 961 Ω, and RRO calculates to 31.14 kΩ.

b) Complex Loads

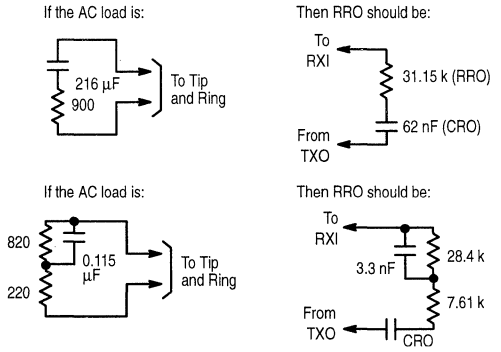
For complex (non-resistive) loads, the MC33120 must be made to look like a termination impedance equal to that complex load. This is accomplished by configuring RRO the same as the complex load, but with all impedance values increased according to the scaling factor of Equation 9.

$$SF = \frac{[(RC + 31\ k)//RS] \bullet 1.037 \bullet 10^6}{(RC + 31\ k) \bullet [(RC + 31\ k)//R_S - (Z_{ac}/2)]} \qquad \text{(Equation 9)}$$

Z_{ac} is computed at a nominal frequency of interest. A first order approximation of Equation 9 is:

$$SF = 1.037 \bullet 10^6/(RC + 31\ k) \qquad \text{(Equation 9a)}$$

For example:

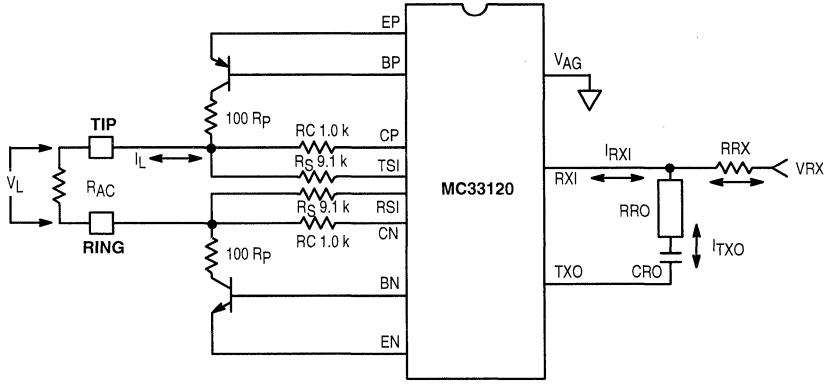


CRO must remain in series with the network to provide DC blocking. If the load network does not include a series capacitor (as in the second example above), CRO should be large (1.0 µF) so its impedance does not affect the RRO network. The above procedure will yield a return loss measurement which is constant with respect to frequency. The RRO resistor, or network, must have a tolerance equal to or better than the required system tolerance for return loss and receive gain.

6) Receive Gain (G_{RX})

The receive gain involves the same circuit as Figure 34, but with the addition of the RRX resistor (or network) which sets the receive gain. See Figure 35.

FIGURE 35 — RECEIVE GAIN



The receive gain (G_{RX}), defined as the voltage gain from V_{RX} to V_L, is calculated as follows:

RXI is a virtual ground, and R_{ac} is the AC impedance of the load (phone line).

The AC current generated in the transistors is 102 • I_{RXI}, which is equal to 102 • (I_R – I_{TXO}).

$I_R = V_{RX}/RRX$, and

$$I_{TXO} = \frac{V_{TXO}}{RRO} = \frac{V_L \bullet 31\ k \bullet 0.328}{RRO \bullet (31\ k + RC)} \qquad \text{(Equation 10)}$$

Using equations 5 and 8, involving Z_{ac}, RS and RC, and the above equations yields:

$$\frac{V_L}{V_{RX}} = G_{RX} = \frac{102 \bullet (R_{ac}//Z_{ac})}{RRX} \qquad \text{(Equation 11)}$$

$$\text{Therefore, } RRX = \frac{102 \bullet (R_{ac}//Z_{ac})}{G_{RX}} \qquad \text{(Equation 12)}$$

Equation 12 applies **only** for the case where R_{ac} and Z_{ac} have the same configuration. If they also have the same magnitude, then set RRX = 51 • R_{ac} to set a receive gain of 0 dB. The AC source impedance of the above circuit to Tip and Ring is Z_{ac}. For the case where $R_{ac} \neq Z_{ac}$, use the following equation:

$$\frac{V_L}{V_{RX}} = \frac{102}{RRX \bullet \left[\frac{1}{Z_L} + \frac{1.037 \bullet 10^6}{(31k + RC) \bullet RRO}\right]} \qquad \text{(Equation 13)}$$

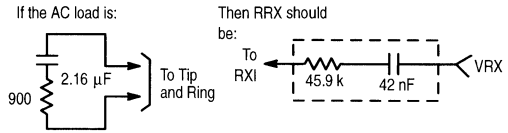
$$\text{where } Z_L = \left[\frac{R_{ac}}{2} // RS // (RC + 31\ k)\right] \bullet 2 \qquad \text{(Equation 14)}$$

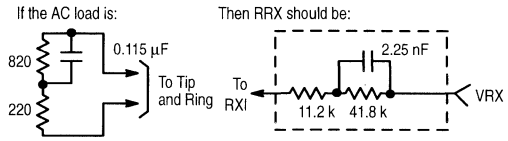
a) Resistive Loads

For a 600 Ω resistive system, set RRX = 30.6 kΩ, and for a 900 Ω resistive system, set RRX = 45.9 kΩ.

b) Complex Loads

For complex (non-resistive) loads, the RRX resistor needs to be replaced with a network having the same configuration as the complex load, but with all impedance values scaled up by a factor of 51 (for 0 dB gain). If a gain other than 0 dB is desired, the scaling factor is determined from Equation 12. This methods applies **only** if the RRO network has been made complex comparable to the load according to the procedure in the previous section (Equations 5–9a), such that $R_{ac} = Z_{ac}$. Using a scaling factor of 51, and the previous examples, yields:





The preceeding procedure will yield a receive gain which is constant with respect to frequency. The RRX resistor, or network, must have a tolerance equal to or better than the required system tolerance for receive gain.

7) Transmit Gain (G_{TX})

Setting the transmit gain involves selecting RTX1 and RTX2 in Figure 28. The voltage gain from V_L to V_{TX} is calculated from the following:

$$G_{TX} = \frac{V_{TX}}{V_L} = \frac{RTX2 \bullet 31\ k \bullet 0.328}{RTX1 \bullet (RC + 31\ k)} \qquad \text{(Equation 15)}$$

For 0 dB gain, set RTX2 = 3.15 x RTX1 (for RC = 1.0 k). The actual values of RTX2 and RTX1 are not critical — only their ratio so as to provide the proper gain at the op amp. Once the ratio is established, the two resistors can be selected from a set of standard resistor values. The minimum value for RTX1 is limited by the drive capability of TXO, which is a nominal ±800 µA peak (±275 µA minimum). As a general rule, RTX1 should be between 6.0 kΩ and 20 kΩ. The load on TXO is the parallel combination of RTX1 and RRO.

CTX is for DC blocking, and is typically a large value (1.0 µF) so as to not be a significant impedance. In general, it should **not** be used for low frequency rolloff as that will affect the transhybrid rejection (discussed in the next section). Low frequency rolloff should be done after the op amp. High frequency rolloff can be set by placing a capacitor across RTX2.

For complex loads (at Tip and Ring), if RRO and RRX have been made complex comparable to the load as described in the previous sections, neither RTX1 nor RTX2 needs to be complex since both the transmit and receive signals which appear at TXO will be flat with respect to frequency.

RTX1 and RTX2 must have a tolerance equal to or better than the required system tolerance for the transmit gain.

8) Balance Network (RB) — Transhybrid Rejection

When a receive signal is applied to V_{RX} to produce a signal at Tip and Ring, the two-to-four wire arrangement of a hybrid (the MC33120) results in a reflected signal at TXO. Transhybrid rejection involves canceling that reflected signal before it appears at V_{TX}. The method used is to insert the RB resistor (or network) as shown in Figure 36. The current I_B, supplied form V_{RX}, cancels the current I_{TX1} supplied from TXO (Node A is a virtual ground). Good transhybrid cancellation requires that the currents be equal in magnitude **and** 180° out of phase at node A.

Using the equations for transmit and receive gains, the current I_{TX1} is equal to:

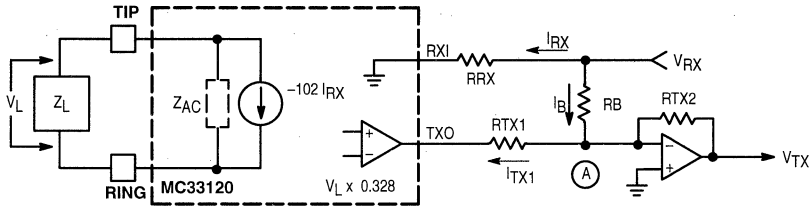
$$I_{TX1} = \frac{33.5 \bullet V_{RX} \bullet Z_{ac} \bullet Z_L \bullet 31\ k}{RRX \bullet [Z_{ac} + Z_L] \bullet RTX1 \bullet (RC + 31\ k)} \qquad \text{(Equation 16)}$$

a) For the case where RRO and RRX are comparable in configuration to Z_L:

Since $I_B = V_{RX}/RB$, then RB can be determined from:

$$RB = \frac{RRX \bullet RTX1 \bullet (RC + 31\ k)}{33.5 \bullet [Z_{ac}//Z_L] \bullet 31\ k} \qquad \text{(Equation 17)}$$

FIGURE 36 — BALANCE RESISTOR



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Equation 17 provides a value for an RB resistor which will provide the correct magnitude for I_B. The correct phase relationship is provided by the fact that the signal at TXO is out of phase with that at V_{RX}. The phase relationship will be 180° **only** if RRO and RRX are of a configuration identical to that of the load. This applies regardless of whether the load, Z_L, (and RRO and RRX) are purely resistive or of a complex nature. Equation 17 reduces to a non-complex resistance if RRX, Z_{ac}, and Z_L are all comparably complex.

For the case where $Z_{ac} = Z_L$, RRX = 51 • Z_{ac}, and RC = 1.0 k, Equation 17 reduces to:

$$RB = 3.15 \bullet RTX1 \qquad \text{(Equation 18)}$$

b) For the case where Z_{ac} and Z_L do not have the same frequency characteristics:

For the case where, for reasons of cost and/or simplicity, the load (R_L) is considered resistive (whereas in reality it is not a pure resistance) and therefore resistors, rather than networks, were selected for RRO and RRX, using a simple resistor for RB may not provide sufficient transhybrid rejection due to a phase angle difference between V_{RX} and TXO. The terminating impedance may therefore not necessarily be matched exactly to the line impedance, but the resulting circuit still provides sufficiently correct performance for receive gain, transmit gain, and return loss. The rejection can be improved in this case by replacing RB with the configuration shown in Figure 37. Even on a very short phone line there is a reactive component to the load due to the two compensation capacitors (C_C, Figure 4) at the transistor collectors. The two capacitors can be considered in series with each other, and across the load as shown in Figure 37. To simplify the explanation, the current source and Z_{ac} of Figure 36 are replaced with the Thevenin voltage source and series Z_{ac}. Since Z_L and Z_{ac} are not matched, there will be a phase shift from V_{RX} to the signal across Tip and Ring. This phase shift is also present at TXO. The same phase shift is generated at node B in the RB network by making RB1 equal to Z_{ac}, and Z_L equal to the load. RB2 is then calculated from:

$$RB2 = \frac{RRX \bullet RTX1 \bullet (RC + 31\ k)}{33.5 \bullet Z_{ac} \bullet 31\ k} \qquad \text{(Equation 19)}$$

For example, for a system where the load is considered a 600 Ω resistor (RRO = 20.3 kΩ, RRX = 30.6 kΩ, RTX1 = 10 kΩ, and RC = 1.0 kΩ), RB1 would be a 600 Ω resistor, Z_L (in the RB network) would be a 600 Ω resistor in parallel with a 0.005 µF capacitor, and RB2 calculates to 15.715 kΩ.

The RB resistor, or network, must have a tolerance equal to or better than the required system tolerance for transhybrid rejection.

9) Logic Interface

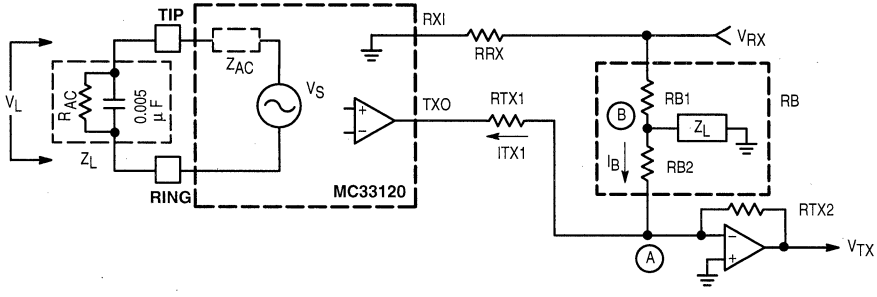
The logic circuit (output ST1, and the I/O labeled ST2/PDI) is depicted in Figure 30, and functions according to the truth table in Table 1.

a) Output Characteristics

ST1 is a traditional NPN pull-down with a 15 kΩ pull-up resistor. Figures 19 and 20 indicate its output characteristics.

ST2 is configured with the following items: a) a 1.0 mA current source for a pull-down which is active only when ST2 is internally set low; b) an 800 µA current source pull-up which is active only when ST2 is internally set high; c) a positive feedback aspect within this output circuit which provides considerable hysteresis for stability reasons. Its output characteristics are shown in Figures 21 and 22. Due to this configuration, any external pull-up resistance which is applied to this pin must be greater than 15 kΩ, or the output may not reliably switch from high to low. Any external pull-down resistance does not affect this output's ability to

FIGURE 37 — BALANCE NETWORK



switch from low-to-high, but **does** affect the maximum longitudinal currents which can be accepted by the circuit (see the section on Longitudinal Current capability). The capacitor (C_T) is required to provide a time delay, for stability reasons, during transitions between off-hook and on-hook. This capacitor additionally affects maximum longitudinal currents, as well as stability during pulse dialing (explained below).

b) Hook Status

The MC33120 uses the sense currents at CP and CN to activate the hook status circuit. The sensing is configured such that the circuit monitors the impedance across Tip/Ring, which results in the hookswitch thresholds being virtually independent of the battery voltage. The off-hook to on-hook threshold is affected by the choice of RRF according to the graph of Figure 8, but is not affected by the value of RS. The on-hook to off-hook threshold is affected by the value of RS according to the graph of Figure 9, but is not affected by RRF. Varying the RC resistors does not affect the thresholds significantly.

When the telephone is on-hook (ST1 = Hi, ST2 = Low), the MC33120 is internally powered down, the external transistors are shut off, and power consumption is at a minimum. Upon closure of the phone's hookswitch, ST1 will switch low within 10 µs. ST2 will then change state slowly due to the external capacitor (C_T = 5.0 µF). There is a ≈8.0 millisecond delay for ST2 to reach the threshold necessary to activate the internal bias circuit, which in turn activates the external drive transistors to supply loop current. This delay is necessary to prevent instabilities during the transition to off-hook.

Upon opening the telephone's hookswitch, ST1 will switch high within ≈200 µs. ST2 then requires ≈60 ms to reach the threshold to switch off the internal bias circuit, which in turn shuts down the external drive transistors.

c) Pulse Dialing

During pulse dialing, ST1 will change state concurrent with the hookswitch. ST2 is kept from switching during pulse dialing by the external capacitor (C_T), which keeps the MC33120 in a powered up condition and stable. If the C_T capacitor is too small, the voltage at ST2 could droop to the PDI threshold (see section e below) during each pulse. This could cause the MC33120 to create additional noise on the line as it would cycle between a power-up and power-down condition with each dialing pulse.

d) Fault Detection

Faults are defined as excessive leakage from Tip to V_{EE} and/or ground, and from Ring to V_{EE} and/or ground. A single fault is any one of the above conditions, while a double fault is defined as excessive leakage from Tip to V_{EE} **and** from Ring to V_{CC}, as depicted in Figure 38. Refer to Figures 11–15 for the resistance, R_{LK}, which will cause the MC33120 to switch to a power-down condition. If the leakage resistance is less than that indicated in the graphs, the MC33120 will power-down itself and the two external transistors, thereby protecting them from overheating. Both status outputs (ST1 and ST2) will be at a logic low, indicating a fault condition. A fault condition is detected by monitoring an imbalance in the magnitudes of the currents at TSI and RSI, and/or a polarity reversal at Tip and Ring.

The MC33120 will detect the following conditions:

1) When on-hook (see Figure 11):
   a) <2.0 kΩ between Ring and V_{CC}, with no hysteresis at this threshold, or
   b) <2.5 kΩ between Tip and V_{EE}, with no hysteresis at this threshold, or
   c) Both a and b simultaneously.

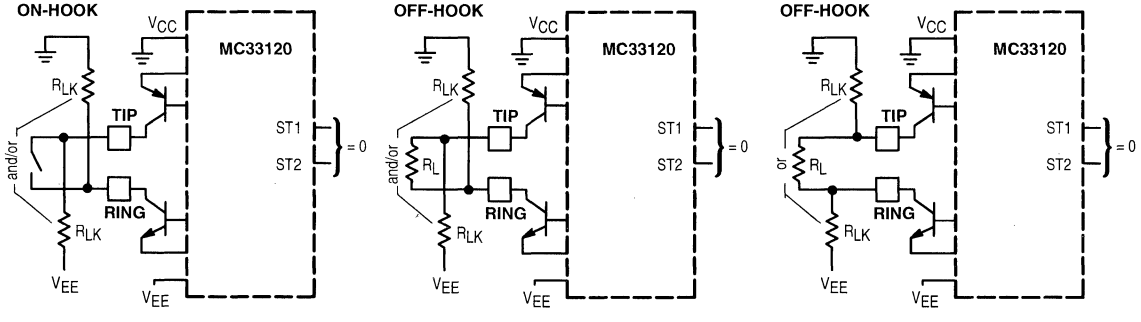
Leakage from Tip to V_{CC} and/or Ring to V_{EE} are not detected as faults while the MC33120 is on-hook.

2) When off-hook (600 Ω between Tip and Ring):
   a) <500 Ω between Tip and V_{CC}, or
   b) <600 Ω between Tip and V_{EE}, or
   c) <500 Ω between Ring and V_{EE}, or
   d) <600 Ω between Ring and V_{CC}, or
   e) Both b and d simultaneously

A simultaneous occurrence of conditions a) and c) is not detected as a fault. See Figures 12–15 for the threshold variation with R_L. Resetting of the fault detection circuit requires that the leakage resistance be increased to a value between 10 kΩ and 20 kΩ, depending on V_{EE}, R_L, and R_S. Both ST1 and ST2 should be monitored for hookswitch status to preclude not detecting a fault condition.

Figure 15 indicates the variation in fault thresholds for Tip-to-V_{CC} and Ring-to-Battery faults, and is valid only for loop resistances of 200 Ω to 1.0 kΩ. On loops larger than 1.0 kΩ, the MC33120 does not reliably indicate the fault

FIGURE 38 — FAULT DETECTION



condition at ST1 and ST2, but may indicate on-hook status instead. This does not apply to Tip-to-Battery and Ring-to-V_{CC} faults which are correctly detected for lines beyond 1.0 kΩ.

e) PDI Input

The ST2 output can also be used as an input (PDI input) to power down the circuit, denying loop current to the subscriber (by shutting off the external pass transistors), regardless of the hookswitch position. Powering down is accomplished by pulling PDI to a logic low with an open collector output, or an NPN transistor as shown in Figure 30. The switching threshold is ≈+1.5 V. The current out of PDI, when pulled low, is ≈800 μA. Releasing PDI allows the MC33120 to resume normal operation.

If the external telephone is off-hook while the MC33120 is powered down, sense currents at CP and TSI will result in some loop current flowing through the loop and back into CN and RSI. This current is generally on the order of 1.0 to 3.0 mA, determined primarily by the RS resistors, loop resistance, and V_{EE}. ST1 will continue to indicate the telephone's actual hook status while PDI is held low. The on-to-off hook threshold is the same as that during normal operation, but the off-to-on hook threshold is >250 kΩ.

When powered down with the PDI pin, the receive gain (V_{RXI} to Tip/Ring) is muted by >90 dB, and the transmit gain (Tip/Ring to TXO) is muted by >30 dB.

Power Dissipation, Calculation and Considerations

a) Reliability

The maximum power dissipated by the MC33120 must be considered, and managed, so as to not exceed the junction temperature listed in the Absolute Maximum Ratings. Exceeding this temperature on a recurring basis will reduce long term reliability, and possibly degrade performance. The junction temperature also affects the statistical lifetime of the device, due to long term thermal effects within the package. Today's plastic integrated circuit packages are as reliable as ceramic packages under most environmental conditions. However, when the ultimate in system reliability is required, thermal managements must be considered as a prime system design goal.

Modern plastic package assembly technology utilizes gold wire bonded to aluminum bonding pads throughout the electronics industry. When exposed to high temperatures for protracted periods of time an intermetallic compound can form in the bond area resulting in high impedance contacts and degradation of device performance. Since the formation of intermetallic compounds is directly related to device junction temperature, it is incumbent on the designer to determine that the device junction temperature is consistent with system reliability goals.

Based on the results of almost ten years of +125°C operating life testing, Table 2 has been derived indicating the relationship between junction temperature and time to 0.1% wire bond failure.

TABLE 2 — STATISTICAL LIFETIME

Junction Temperature (°C)	Time (Hours)	Time (Years)
80	1,032,200	117.8
90	419,300	47.9
100	178,700	20.4
110	79,600	9.4
120	37,000	4.2
130	17,800	2.0
140	8,900	1.0

Motorola MECL Device Data, DL122

The "time" in Table 2 refers to the time the device is operating at that junction temperature. Since the MC33120 is at a low power condition (nominally 68 mW) when on-hook, the duty cycle must be considered. For example, if a statistical duty cycle of 20% off-hook time is used, operation at 130°C junction temperature (when off-hook) would result in a statistical lifetime of ≈10 years.

b) Power and Junction Temperature Calculation

The power within the IC is calculated by subtracting the power dissipated in the two wire side (the transistors and the load) from the power delivered to the IC by the power supplies. Refer to Figure 4 and 27.

$$P_D = |V_{DD} \bullet I_{DD}| + |V_{EE} \bullet I_{EE}| - (I_{LOOP} \bullet |V_{EP} - V_{EN}|) \quad \text{(Equation 20)}$$

The terms V_{EP} and V_{EN} are the DC voltages, with respect to ground, at the EP and EN pins. These voltages can be measured, or can be approximated by:

$$V_{EP} \approx -(30\ \Omega \bullet I_{LOOP})$$
$$V_{EN} \approx V_{EE} + 2.1\ V + (I_{LOOP} \bullet 35\ \Omega)$$

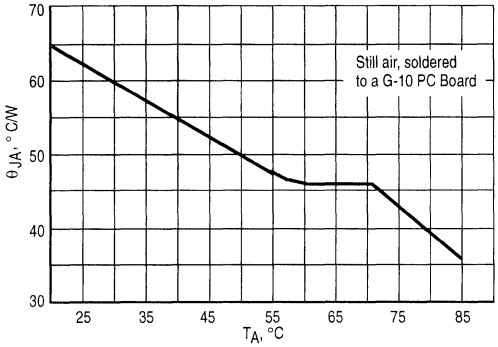
Refer to Figure 23. The junction temperature is then calculated from:

$$T_J = T_A + (P_D \bullet \theta_{JA}) \quad \text{(Equation 21)}$$

where T_A is the ambient air temperature at the IC package, and θ_{JA} is the junction-to-ambient thermal resistance shown in Figure 39. The highest junction temperature will occur at maximum V_{EE} and V_{DD}, maximum loop current, and maximum ambient temperature.

If the above calculations indicate the junction temperature will exceed the maximum specified, then it is necessary to reduce the maximum loop current, ambient temperature, and/or V_{EE} supply voltage. Air flow should not be restricted near the IC by tall components or other objects since even a small amount of air flow can substantially reduce junction temperature. For example, typically an air flow of 300 LFPM (3.5 mph) can reduce the effective θ_{JA} by 14 to 20% from that which occurs in still air. Additionally, providing as much copper area as possible at the IC pins will assist in drawing away heat from within the IC package. For additional information on this subject, refer to the "Thermal Considerations" section of *Motorola MECL System Design Handbook* (HB205), and the "System Design Considerations" section of *Motorola MECL Device Data* (DL122).

FIGURE 39 — THERMAL RESISTANCE (JUNCTION TO AMBIENT)



Selecting the Transistors

The specifications for the two loop current pass transistors involve their current gain, voltage rating, and power dissipation capabilities at the highest ambient temperatures. Power dissipation during both normal operation and faults must be considered when determining worst case situations. Generally, more power is dissipated during a fault condition than during normal operation.

The transistors' minimum beta is recommended to be 40 at the loop currents involved in the application. A lower beta could degrade gain and balance performance. Maximum beta should be less than 500 to prevent possible oscillations. Darlington type transistors should not be used. The voltage rating should be a minimum of 80 V, although the choice of protection scheme may require a higher rating.

Referring to Figure 27, during normal operation the loop current and the voltage across the transistors are both at a maximum when the load impedance (R_L) is at a minimum. The loop current is determined by RRF and the graphs of Figures 5–7. The voltage across each transistor is determined from the following:

$$V_T = \frac{|V_{EE}| - 2.1 - [(65 + 2RP + R_L) \bullet I_{LOOP}]}{2} \quad \text{(Equation 22)}$$

The power in each transistor is then ($V_T \bullet I_{LOOP}$). The voltage across the two transistors will always be nearly equal during normal operation, resulting in equal power dissipation. The graph of Figure 24 indicates the power dissipated in each transistor where RP = 100 Ω.

During a fault condition, depicted in Figure 38, if the leakage resistance from Tip to V_{EE} or from Ring to V_{CC} is less than that shown in Figures 12–14 (when off-hook), the MC33120 will power down the transistors to protect them from overheating. Should the leakage resistance be slightly higher than that shown in the graphs, however, and the fault detection has not been activated, the power in one transistor (in a single fault, both transistors in a double fault) will be higher than normal. The power will depend on V_{EE}, R_L, RP and the leakage resistance. Table 3 is a guide of the power in the transistor dissipating the higher power level.

TABLE 3 — TRANSISTOR POWER DURING A FAULT

V_{EE}	R_S	R_L	P_{PNP}	P_{NPN}
–58	9.1 k	200	1.64	1.34
–48	9.1 k	200	1.05	0.957
–58	9.1 k	600	1.37	1.11
–48	9.1 k	600	0.746	0.616
–58	9.1 k	1.0 k	0.897	0.68
–48	9.1 k	1.0 k	0.232	0.194
–58	5.1 k	200	1.8	1.55
–58	11 k	200	1.53	1.3

The power (in watts) in the two right columns indicates the power dissipated by that transistor if it is carrying the maximum fault current. The system designer should attempt to predict possible fault conditions for the system, and then measure the conditions on the transistors during the worse case fault(s).

For most applications involving a nominal V_{EE} of – 48 V (with a maximum of – 58 V), a maximum loop current of 30 to 40 mA, and a maximum T_A of +85°C, the MJD243 and MJD253 DPAK transistors are recommended. When mounted as described in their data sheet, they will handle both the normal loop current as well as most fault conditions. If faults are not expected to occur in a particular application, then smaller package transistors, such as MPS6717 and MPS6729, may be used. Each application must be evaluated individually when selecting the transistors.

Other possible transistors which can be considered:

PNP	NPN
MJD253-1	MJD243-1
MJE253	MJE243
MJD32	MJD31
MJD42	MJD41
MJD350	MJD340
TIP30A,B,C	TIP29A,B,C

Longitudinal Current Capability

The maximum longitudinal current which can be handled without distortion is a function of loop current, battery feed resistance, the longitudinal impedance, and the components on ST2.

Since the pass transistors cannot pass current in the reverse direction, the DC loop current provides one upper boundary for the peak longitudinal current plus peak speech signal current. The battery feed resistance determines, in effect, the DC voltage across the transistors, which is a measure of the headroom available for the circuit to handle the peak longitudinal voltage plus peak speech signal voltage. The longitudinal impedance, determined by the R_S resistors (equation 4), determines the longitudinal current for a given longitudinal voltage.

While analysis of the above items may yield one value of maximum longitudinal current, a different limit (which may be higher or lower) is imposed by the capacitor C_T, and any pulldown resistance R_T, on Pin 12 (ST2). This is due to the fact that the sense currents at TSI and RSI will be alternately mismatched as Tip and Ring move up and down together in the presence of longitudinal signals. When the longitudinals are strong, the internal fault detect circuit is activated with each 1/2 cycle, which attempts to switch ST2 low (see the section on Fault Detection). The speed at which ST2 can

switch low is a function of both the external capacitor, C_T and any pulldown resistance, R_T.

The graphs of Figures 25 and 26 indicate the maximum longitudinal current which can be handled (in Tip **and** in Ring) without distortion or causing ST2 to switch low.

PC Board Layout Considerations

PC board considerations include thermal, RFI/EMI, transient conditions, interconnection of the four wire side to the codec/filter, and others. Wirewrapped boards should be avoided — breadboarding should be done on a (at least) reasonably neat PC board.

2

a) Thermal

Power dissipated by the MC33120 and the two transistors must be removed to prevent excessively high junction temperatures. The equations for calculating junction temperatures are mentioned elsewhere in this data sheet. Heat is removed by both air flow and copper foil on the PC board. Since even a small amount of air flow substantially reduces junction temperatures compared to still air, tall components or other objects should not be placed such that they block air flow across the heat generating devices. Increasing, wherever possible, the area of the copper foil at the IC pins will provide additional heat removal capability. A ground plane can generally help here, while at the same time helping to reduces RFI problems.

b) RFI/EMI

While the MC33120 is intended for use at audio frequencies, the internal amplifiers have bandwidths in excess of 1.0 MHz, and can therefore respond to externally induced RFI and EMI. Interference signals can come in on the phone line, or be radiated on to the PC board from nearby radio stations or from high frequency circuitry (digital & microprocessor circuitry) in the vicinity of the line card.

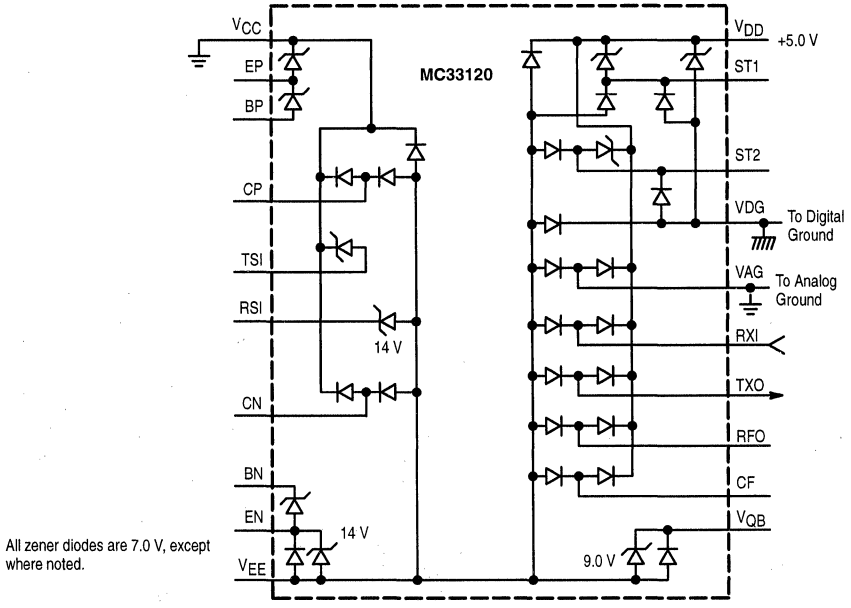
Usually RFI entering from the phone line at Tip and Ring can be removed by the compensation capacitors (C_C) provided they are connected to a good quality RF ground (generally the same ground which connects to V_{CC} on the MC33120). The ground track should be as wide and as direct as possible to minimize lead inductance. Generally better results can be obtained if an RF bleedoff to earth (or chassis) ground can be provided where the twisted pair phone line comes into the system.

To minimize problems due to noise radiating directly onto the PC board from nearby high frequency circuitry, all components associated with the MC33120 should be physically as close as possible to the IC. The most sensitive pins in this respect are the CP, CN, RSI, TSI, VAG and RXI pins. Keeping the tracks short minimizes their "antenna" effect.

c) Transient Conditions

When transient voltages come in to Tip and Ring, the transient currents, which can be several amperes, must be carried by the ground line (V_{CC}) and/or the V_{EE} line. These tracks, along with the protection and clamping devices, must be designed for these currents at the frequencies involved. If the tracks are narrow, not only may they be destroyed by the high currents, but their inductance can allow the voltage at the IC, and other nearby components, to rise to damaging levels.

FIGURE 40 — PROTECTION DIODES



The protection circuits shown in Figure 4, and in other figures in this data sheet, are such that the bulk of the transient energy is dissipated by **external** components (the protection resistors and the clamp diodes). The MC33120 has internal diodes to limit voltage excursions on the pins, and to pass a small amount of the transient current — typically less than 1.0 ampere peak. The arrangement of the diodes is shown in Figure 40.

d) Interconnection of the four-wire side

The connections on the four-wire side to the codec and other digital circuitry involves keeping digital noise out of the speech paths, and also ensuring that potentially destructive transients on Tip and Ring do not get through to the +5.0 V system.

Basically, digital connections to ST1 and ST2 should be referenced to the V_{DD} and V_{DG} pins, while the transmit and receive analog signals should be referenced to the analog ground (V_{AG}). V_{CC} should be connected to a clean battery ground, and generally should **not** be connected directly to V_{DG} and/or V_{AG} (on the line card) when strong transients are anticipated. Even with a good layout, V_{CC} can move several volts when a transient hits, possibly damaging components on the +5.0 V line **if** their grounds have a direct connection at the line card. The MC33120 is designed to allow V_{CC} to move as much as ±30 V with respect to V_{DG} and V_{AG} **on a transient basis only.** V_{CC} and the other grounds should preferably be connected together **at the power supply** rather than at the IC. Internally, the MC33120 has clamp diodes on the 4-wire side pins as shown in Figure 40.

If the codec has a single ground pin, as in Figure 41, it will be the reference for both the digital and analog signals, and must be connected to both V_{AG} and V_{DG} on the MC33120. If the codec has separate digital and analog grounds, as in Figure 42 (the MC145503 internally generates the analog ground), then each ground should be connected to the appropriate ground on the MC33120.

e) Other

A 0.1 µF capacitor should be provided across V_{CC} to V_{EE} on the MC33120 to help keep idle channel noise to a minimum.

The C_{QB} capacitor (on the V_{QB} pin) forms a pole with an internal 7.5 kΩ resistor to filter noise from the V_{EE} pin,

FIGURE 41 — CONNECTION TO A CODEC WITH A SINGLE GROUND

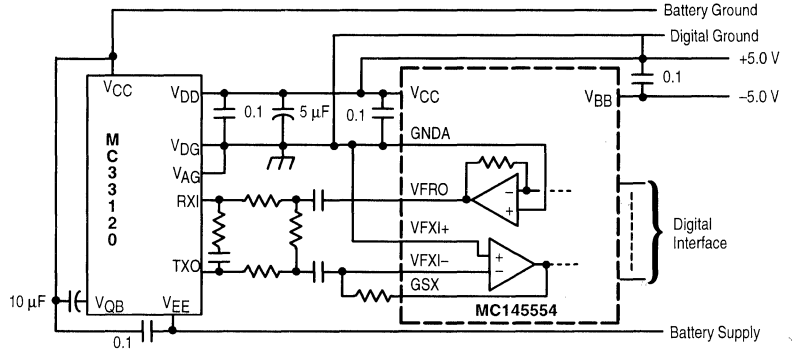
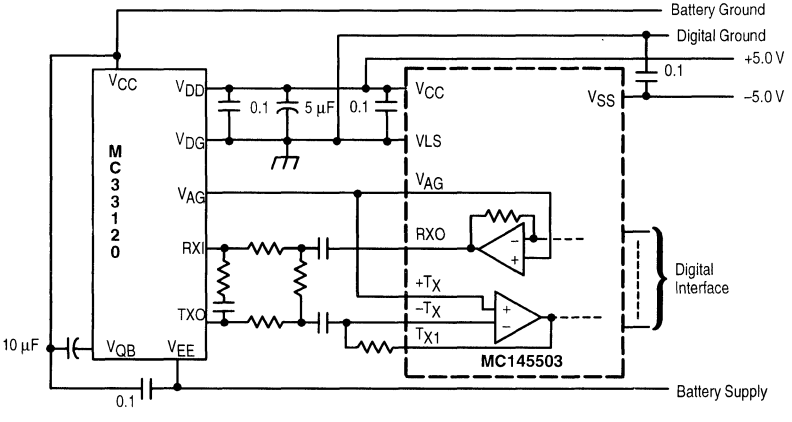


FIGURE 42 — CONNECTION TO A CODEC WITH SEPARATE GROUNDS



providing an internal quiet battery supply for the speech amplifiers. Power supply rejection will depend on the value and quality of this capacitor at the frequencies of concern. Tantalum capacitors generally have better high frequency characteristics then electrolytics. See Figure 17 and 18 for ripple rejection characteristics (the four-wire data was measured at pin 11 (TXO)). Figure 16 indicates ripple rejection from the +5.0 V supply (V_{DD}).

In general, PC board tracks carrying analog signals (on the four wire side and Tip/Ring) should not be routed through the digital section where they could pick up digital noise. Any tracks longer than a few inches should be considered an antenna and should be checked for potential noise or RFI pickup which could affect the circuit operation.

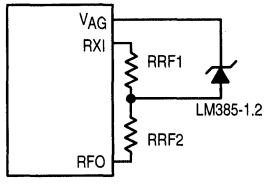
2

Alternate Circuit Configurations

a) Loop Current Limit

Replacing the RRF resistor with the circuit in Figure 43 will change the DC loop current characteristics in two ways from the graphs of Figures 5–7; a) the maximum loop current on a short line can be reduced while increasing the current on a long line, and b) the temperature dependence of the maximum current is reduced to the TC of the external reference diode.

FIGURE 43 — ALTERNATE CURRENT LIMIT CIRCUIT



The LM385-1.2 is a precision temperature stable zener diode. As the load impedance at Tip and Ring is reduced, the voltage at RFO goes increasingly negative. When the zener diode is turned on, the current into RXI is then clamped at a value determined by RRF1 and the zener diode. To calculate the two resistors, use the following procedure:

RRF1 must be >0.7 • (RRF1 + RRF2);

Determine RRF1 to set the current limit on a short line by using the following equation:

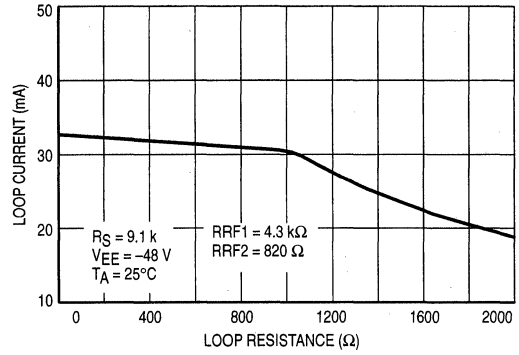
$$RRF1 = \frac{102 \bullet 1.23\ V}{I_{LOOP\ (MAX)} - 3.0\ mA} \qquad \text{(Equation 23)}$$

Then using Equation 1 calculate RRF for the long line current. RRF2 is then determined by;

$$RRF2 = RRF - RRF1 \qquad \text{(Equation 24)}$$

Figure 44 illustrates one example using the above circuit. Comparing this graph to the 5100 Ω curve of Figure 6 shows a substantial decrease in the current limit (at R_L = 0), resulting in reduced power consumption and dissipation. Use of this circuit does not affect the hookswitch or fault thresholds.

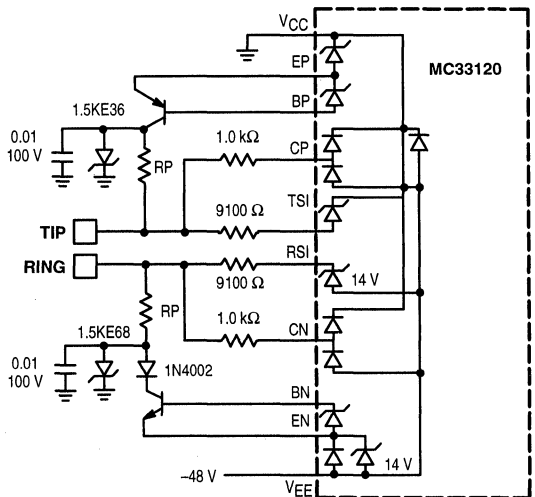
FIGURE 44 — LOOP CURRENT versus LOOP RESISTANCE ALTERNATE LOOP CURRENT LIMIT CONFIGURATION



b) Protection Scheme

The protection circuit shown in Figure 45 has the advantage of drawing ≈90% of the transient current from ground (V_{CC}) on a negative transient, rather than from the V_{EE} line as the circuit of Figure 4 does. The majority of the transient current flows through the RP resistors and the Mosorbs while a small amount (≈10%) flows through the sense resistors and the CP, CN, RSI pins. On a positive transient, all the current (except at RSI) is directed to ground. The diode in the NPN's collector prevents reverse current through the base-collector junction of the transistor during a negative transient.

FIGURE 45 — ALTERNATE PROTECTION SCHEME



All zener diodes are 7.0 V except as noted.

CIRCUIT PERFORMANCE

The following three circuits are presented as typical application examples, and the accompanying graphs indicate their measured performance. The first circuit (Figure 46) has a 600 Ω pure resistance as the AC load. The second circuit (Figures 47) has as an AC load a 900 Ω resistor in series with a 2.16 μF capacitor. The third circuit (Figure 48) has as an AC load, a complex network composed of an 820 Ω resistor in parallel with 0.115 μF, and those in series with a 220 Ω resistor. In the graphs of Figures 49–51, R_L = Return Loss, THR = Transhybrid Rejection, GTX = Transmit Gain, GRX = Receive Gain.

FIGURE 46 — 600 Ω SYSTEM

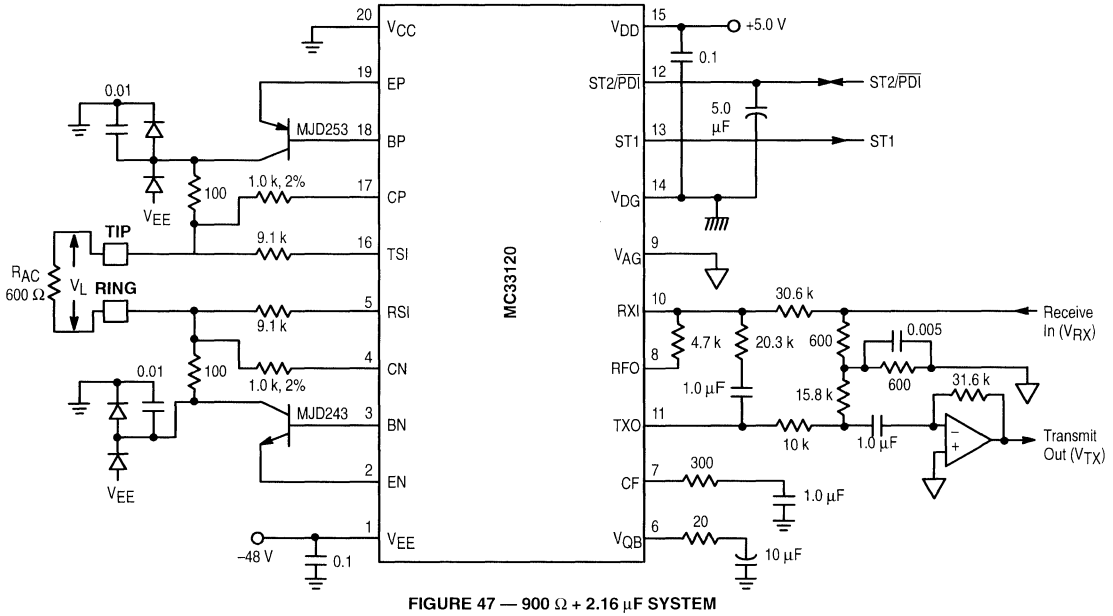


FIGURE 47 — 900 Ω + 2.16 μF SYSTEM

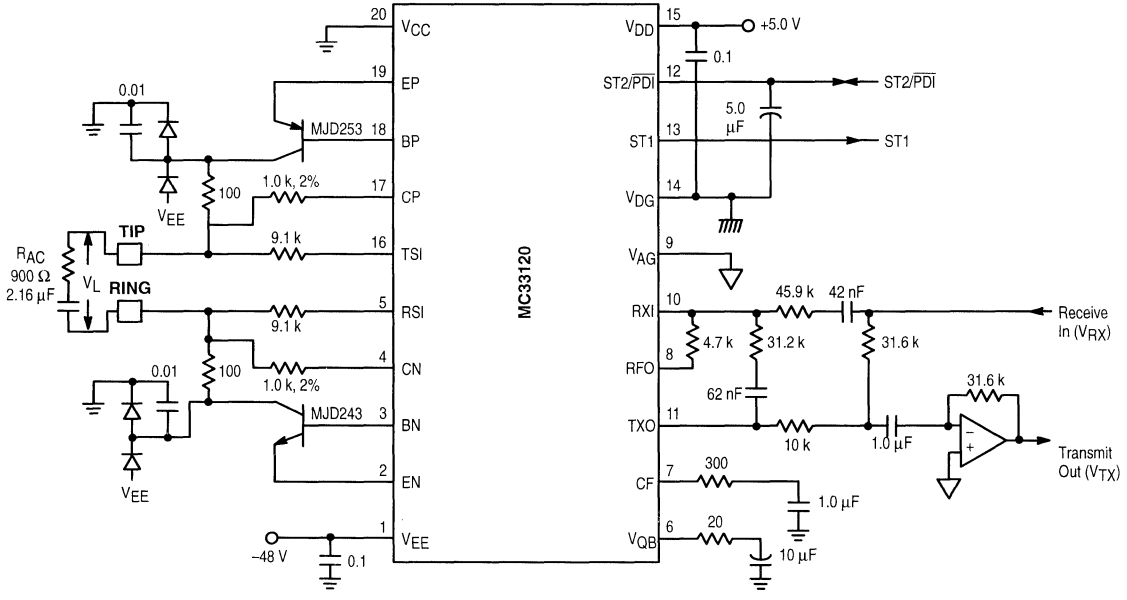


FIGURE 48 — 220 Ω + 820 Ω//0.115 μF SYSTEM

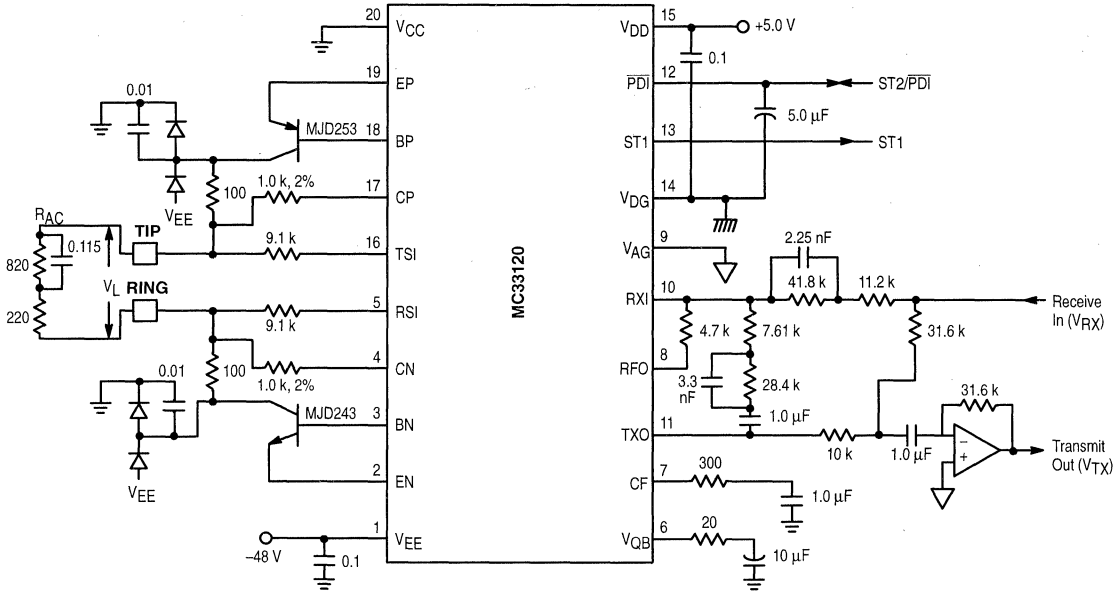


FIGURE 49 — CIRCUIT PERFORMANCE, 600 Ω SYSTEM

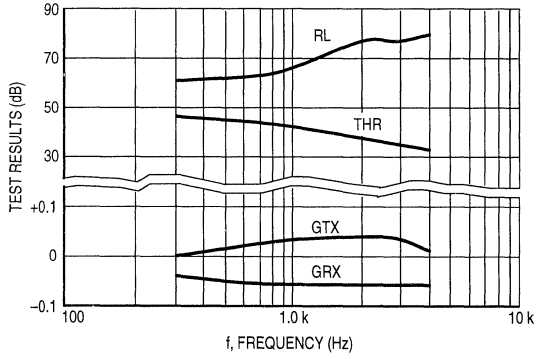


FIGURE 50 — CIRCUIT PERFORMANCE 900 Ω + 2.16 μF SYSTEM

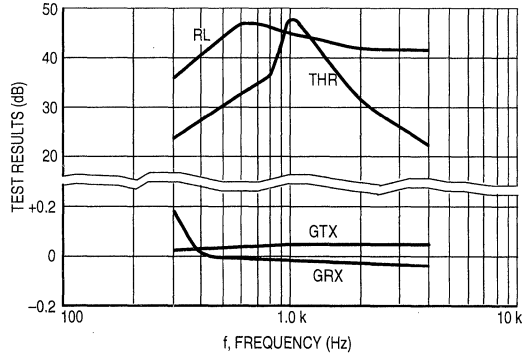


FIGURE 51 — CIRCUIT PERFORMANCE
820 Ω//0.115 μF + 220 Ω SYSTEM

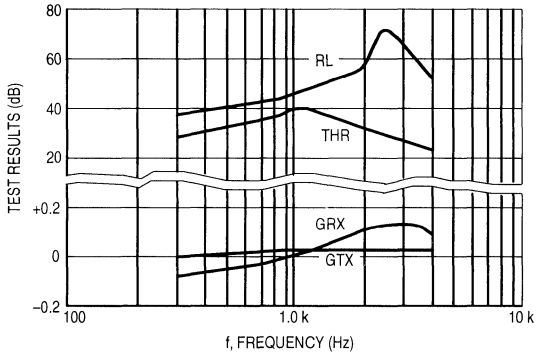
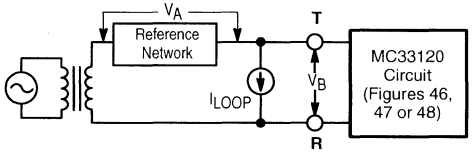


FIGURE 52 — RETURN LOSS TEST CIRCUIT
FOR FIGURES 46 TO 51



Reference Network = R_{AC} of Figures 46 to 48.
Return Loss = $20 \log \left| \frac{V_A + V_B}{V_A - V_B} \right|$

2

GLOSSARY

ATTENUATION — A decrease in magnitude of a communication signal, usually expressed in dB.

BALANCE NETWORK — That part of the SLIC circuit which provides transhybrid rejection.

BANDWIDTH — The range of information carrying frequencies of a communication system.

BATTERY — The voltage which provides the loop current, and in some cases powers the SLIC circuit. The name derives from the fact that COs have always used batteries, in conjunction with AC power, to provide this voltage.

BATTERY FEED RESISTANCE — The equivalent Thevenin DC resistance of the SLIC circuit for supplying loop current. Traditionally it is 400 Ω.

C-MESSAGE FILTER — A frequency weighting which evaluates the effects of noise on a typical subscriber's system.

CENTRAL OFFICE — Abbreviated CO, it is a main telephone office, usually within a few miles of its subscribers, that houses switching gear for interconnection within its exchange area, and to the rest of the telephone system. A typical CO can handle up to 10,000 subscriber numbers.

CODEC — Coder/Decoder — Interfacing between the SLIC and the digital switch, it converts the SLIC's transmit signal to digital, and converts the digital receive signal to analog.

dB — A power or voltage measurement unit, referred to another power or voltage. It is generally computed as:

$$10 \bullet \log (P_1 / P_2)$$

for power measurements, and

$$20 \bullet \log (V_1 / V_2)$$

for voltage measurements.

dBm — An indication of signal power. 1.0 mW across 600 Ω, or 0.775 V rms, is defined as 0 dBm. Any other voltage level is converted to dBm by:

dBm = 20 • log (Vrms/0.775), or
dBm = [20 • log (Vrms)] + 2.22.

dBmp — Indicates dBm measurement using a psophometric weighting filter.

dBrn — Indicates a dBm measurement relative to 1.0 pW power level into 600 Ω. Generally used for noise measurements, 0 dBrn = –90 dBm.

dBrnC — Indicates a dBrn measurement using a C-message weighting filter.

DTMF — Dual Tone Multifrequency. It is the "tone dialing" system based on outputting two non-harmonic related frequencies simultaneously to identify the number dialed. Eight frequencies have been assigned to the four rows and four columns of a keypad.

FAULT — An incorrect condition where Tip is accidentally connected to the battery voltage, or Ring is connected to ground, or both. The most common fault is Ring to ground.

FOUR WIRE CIRCUIT — The portion of a telephone, or central office, which operates on two pairs of wires. One pair is for the transmit path, and one pair is for the receive path.

FULL DUPLEX — A transmission system which permits communication in both directions simultaneously. The standard handset telephone system is full duplex.

GAIN — The change in signal amplitude (increase or decrease) after passing through an amplifier, or other circuit stage. Usually expressed in dB, an increase is a positive number, and a decrease is a negative number.

HALF DUPLEX — A transmission system which permits communication in one direction at a time. CB radios, with "push-to-talk" switches, and voice activated speakerphones, are half duplex.

HOOKSWITCH — A switch, within the telephone, which connects the telephone circuit to the subscriber loop. The name derives from old telephones where the switch was activated by lifting the receiver off and onto a hook on the side of the phone.

HYBRID — Another name for a two-to-four wire converter.

IDLE CHANNEL NOISE — Residual background noise when transmit and receive signals are absent.

LINE CARD — The PC board and circuitry in the CO or PBX which connects to the subscriber's phone line. A line card may hold circuitry for one subscriber, or a number of subscribers.

2

LONGITUDINAL BALANCE — The ability of the SLIC to reject longitudinal signals on Tip and Ring.

LONGITUDINAL SIGNALS — Common mode signals.

LOOP — The loop formed by the two subscriber wires (Tip and Ring) connected to the telephone at one end, and the central office (or PBX) at the other end. Generally, it is a floating system not referred to ground, or AC power.

LOOP CURRENT — The DC current which flows through the subscriber loop. It is typically provided by the central office or PBX, and ranges from 20 to 120 mA.

OFF HOOK — The condition when the telephone is connected to the phone system, permitting the loop current to flow. The central office detects the DC current as an indication that the phone is busy.

ON HOOK — The condition when the telephone is disconnected from the phone system, and no DC loop current flows. The central office regards an on-hook phone as available for ringing.

PABX — Private Automatic Branch Exchange. In effect, a miniature central office, it is a customer owned switching system servicing the phones within a facility, such as an office building. A portion of the PABX connects to the Bell (or other local) telephone system.

PROTECTION, PRIMARY — Usually consisting of carbon blocks or gas discharge tubes, it absorbs the bulk of a lightning induced transient by clamping the voltages to less than ±1500 V.

PROTECTION, SECONDARY — Usually located on the line card, it protects the SLIC and associated circuits from transient surges. Typically, it must be capable of clamping a ±1.5 kV surge of 1.0 ms duration.

PULSE DIALING — A dialing system whereby the loop current is interrupted a number of times in quick succession. The number of interruptions corresponds to the number dialed, and the interruption rate is typically 10 per second. The old rotary phones, and many new pushbutton phones, use pulse dialing.

RECEIVE PATH — Within the CO or PBX it is the speech path from the internal switching system towards the phone line (Tip & Ring).

REN — Ringer Equivalence Number. An indication of the impedance or loading factor of a telephone bell or ringer circuit. An REN of 1.0 equals ≈8.0 kΩ. The Bell system typically permits a maximum of 5.0 REN (1.6 kΩ) on an individual subscriber line. A minimum REN of 0.2 (40 kΩ) is required by the Bell system.

RETURN LOSS — Expressed in dB, it is a measure of how well the SLIC's AC impedance matches the line's AC characteristic impedance. With a perfect match, there is no reflected signal, and therefore infinite return loss. It is calculated from:

$$RL = 20 \bullet \log \frac{(Z_{LINE} + Z_{CKT})}{(Z_{LINE} - Z_{CKT})}$$

RING — One of the two wires connecting the central office to a telephone. The name derives from the ring portion of the plugs used by operators (in older equipment) to make the connection. Ring is traditionally negative with respect to Tip.

SLIC — Subscriber Line Interface Circuit. It is the circuitry within the CO or PBX which connects to the user's phone line.

SUBSCRIBER — The customer at the telephone end of the line.

SUBSCRIBER LINE — The system consisting of the user's telephone, the interconnecting wires, and the central office equipment dedicated to that subscriber (also referred to as a loop).

TIP — One of the two wires connecitng the central office to a telephone. The name derives from the tip of the plugs used by operators (in older equipment) to make the connection. Tip is traditionally positive with respect to Ring.

TRANSHYBRID REJECTION — The rejection (in dB) of the reflected signal in the transmit path resulting from a receive signal applied to the SLIC.

TRANSMIT PATH — Within the CO or PBX it is the speech path from the phone line (Tip & Ring) towards the internal switching system.

TWO WIRE CIRCUIT — Refers to the two wires connecting the central office to the subscriber's telephone. Commonly referred to as Tip and Ring, the two wires carry both transmit and receive signals in a differential manner.

TWO-TO-FOUR WIRE CONVERTER — A circuit which has four wires (on one side) — two (signal & ground) for the outgoing signal, and two for the incoming signal. The outgoing signal is sent out differentially on the two wire side (the other side), and incoming differential signals received on the two wire side are directed to the four wire side. Additional circuit within cancels the reflected outgoing signal to keep it separate from the incoming signal.

VOICEBAND — That portion of the audio frequency range used for transmission across the telephone system. Typically it is 300 to 3400 Hz.

MC33121

Low Voltage Subscriber Loop Interface Circuit

LOW VOLTAGE SUBSCRIBER LOOP INTERFACE CIRCUIT (SLIC)

THIN FILM SILICON MONOLITHIC INTEGRATED CIRCUIT

2

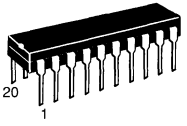
The MC33121 is designed to provide the interface between the 4-wire side of a central office, or PBX, and the 2-wire subscriber line. Interface functions include battery feed, proper loop termination AC impedance, hookswitch detection, adjustable transmit, receive, and transhybrid gains, and single/double fault indication. Additionally, the MC33121 provides a minimum of 58 dB of longitudinal balance (4-wire and 2-wire).

The transmit and receive signals are referenced to analog ground, while digital signals are referenced to digital ground, easing the interface to codecs, filters, etc. The 2 status outputs (hookswitch and faults) and the Power Down Input are TTL/CMOS compatible. The Power Down Input permits local shutdown of the circuit.

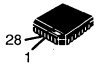
Internal drivers allow the external loop current pass transistors to be standard bipolar transistors (non-Darlington).

The MC33121 is available in a 20 pin DIP and a 28 pin PLCC surface mount package.

- 58 dB Longitudinal Balance Guaranteed; 4-wire and 2-wire
- Transmit, Receive, and Transhybrid Gains Externally Adjustable
- Return Loss Externally Adjustable
- Proper Hookswitch Detection With 30 kΩ Leakage
- Single/Double Fault Indication With Shutdown for Thermal Protection
- Critical Sense Resistors Included Internally
- Standard Power Supplies: – 21.6 V to – 42 V, and + 5.0 V, ± 10%
- On-Hook Transmission
- Power Down Input (TTL and CMOS Compatible)
- Operating Ambient Temperature: – 40°C to + 85°C
- Available in a 20 Pin DIP and 28 Pin PLCC Package



P SUFFIX
PLASTIC PACKAGE
CASE 738

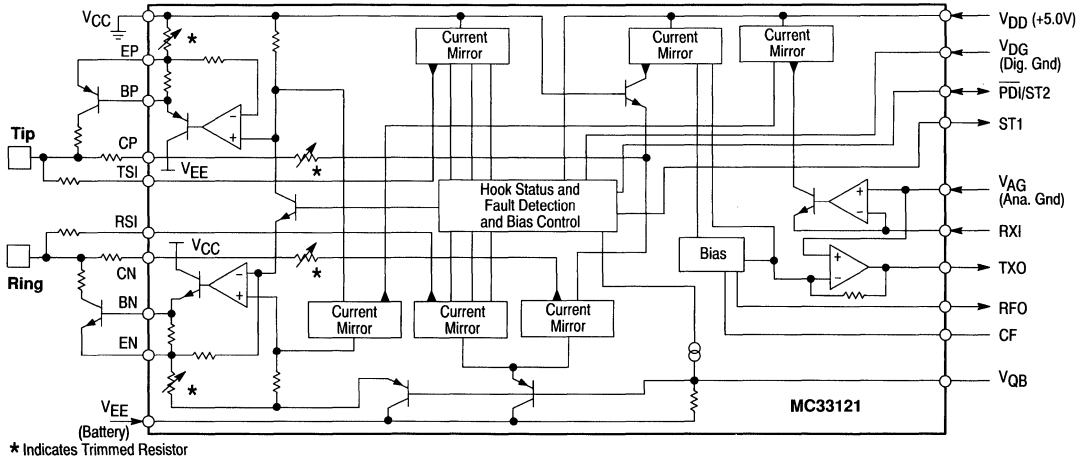


FN SUFFIX
PLCC
CASE 776

ORDERING INFORMATION

Device	Temperature Range	Package
MC33121P	– 40° to + 85°C	Plastic DIP
MC33121FN		PLCC

SIMPLIFIED BLOCK DIAGRAM



MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Supply Voltage (with respect to V_{CC}) (with respect to V_{DG})	 V_{EE} V_{DD}	 – 60, +0.5 – 0.5, +7.0	Vdc
Voltage @ PDI, (with respect to V_{DG}) @ CP, CN EP, TSI BP RSI, EN BN	V_{in}	 – 0.5, +7.0 V_{EE} – 0.5, V_{CC} +0.5 V_{CC} – 7.0, V_{CC} +0.5 V_{CC} – 14, V_{CC} +0.5 V_{EE} – 0.5, V_{EE} +14 V_{EE} – 1.0, V_{EE} +21	Vdc
Junction Temperature	T_J	150	°C
Storage Temperature	T_{stg}	– 65 to +150	°C

Devices should not be operated at these limits. The "Recommended Operating Conditions" table provides for actual device operation.

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Voltage (with respect to V_{CC}) (with respect to V_{DG})	 V_{EE} V_{DD}	 – 42 +4.5	 – 24 +5.0	 – 21.6 +5.5	Vdc
(with respect to V_{CC}) (with respect to V_{CC}) (with respect to V_{AG})	V_{AG} V_{DG}	– 3.0 – 3.0 – 3.0	0 0 0	+10 +7.0 +10	
(with respect to V_{EE}) (with respect to V_{CC} and V_{AG})	V_{DD}	— 3.5	— —	47.5 —	
Loop Current	I_L	15	—	50	mA
PDI Input Voltage	V_{PDI}	0	—	V_{DD}	Vdc
Sink Current ST1 ST2	 I_{ST1L} I_{ST2L}	 0 0	 — —	 1.0 1.0	mA
Transmit Signal Level at Tip & Ring Receive Signal Level at V_{RX}	S_{TX} S_{RX}	– 48 – 48	— —	+3.0 +3.0	dBm
Loop Resistance V_{EE} = – 42 V V_{EE} = – 24 V	R_L	0 0	— —	2.0 k 800	Ω
External Transistor Beta	H_{fe}	40	—	500	A/A
Operating Ambient Temperature (See text for derating)	T_A	– 40	—	+85	°C

All limits are not necessarily functional concurrently.

ELECTRICAL CHARACTERISTICS (V_{EE}= – 24 V, V_{DD}= +5.0 V, unless otherwise noted. V_{CC}=V_{AG}=V_{DG}= 0 V, T_A= 25°C, see Figure 1.)

Characteristic	Symbol	Min	Typ	Max	Unit
POWER SUPPLIES					
V_{EE} Current On Hook (R_L > 10 MΩ, V_{EE} = – 42 V) Off Hook (R_L = 0 Ω, V_{EE} = – 42 V)*	 I_{EEN} I_{EEF}	 – 2.7 – 72	 – 1.0 – 55	 — – 41	mA
V_{DD} Current On Hook (R_L > 10 MΩ, V_{DD} = +5.5 V) Off Hook (R_L = 0 Ω, V_{DD} = +5.5 V)	 I_{DDN} I_{DDF}	 — 4.0	 1.4 7.0	 2.7 14	
V_{EE} Ripple Rejection f = 1.0 kHz, @ V_{TX} (4-wire) f = 1.0 kHz, @ Tip/Ring (2-wire) V_{DD} Ripple Rejection f = 1.0 kHz, @ V_{TX} (4-wire) f = 1.0 kHz, @ Tip/Ring (2-wire)	PSRR 	 40 40 37 37	 62 52 52 48	 — — — —	dB

*Includes loop current.

ELECTRICAL CHARACTERISTICS (V_{EE}= – 24 V, V_{DD}= +5.0 V, unless otherwise noted. V_{CC}=V_{AG}=V_{DG}= 0 V, T_A= 25°C, see Figure 1.)

Characteristic	Symbol	Min	Typ	Max	Unit
LOOP FUNCTIONS					
Loop Current					mA
Maximum (RRF = 4.7 k, R_L = 10 Ω)	$I_{L(max)}$	37	41	51	
Nominal (RRF = 4.7 k, R_L = 367 Ω)	I_L	21	27	34	
Minimum (RRF = 4.7 k, R_L = 796 Ω)	$I_{L(min)}$	16	17.5	—	
Battery Feed Resistance (RRF = 4.7 k, R_L = 796 Ω)*	R_{BF}	475	575	675	Ω
Hookswitch Threshold					kΩ
On-to-Off Hook	R_{NF}	2.0	4.1	—	
Off-to-On Hook	R_{FN}	—	7.7	10	
Fault Detection Threshold					Ω
Ring-to-Ground (R_L = 367 Ω)	R_{RG}	600	1100	—	
Tip-to-Battery (R_L = 367 Ω)	R_{TB}	600	1100	—	

*Calculated from [(24/$I_{L(min)}$) – 796]

GAIN LEVELS

Transmit Voltage Gain (CP, CN to TXO)	G_{TX1}	—	0.328	—	V/V
Transmit Voltage Gain (V_{TX}/V_L)					dB
V_L = 0 dBm, f = 1.0 kHz	G_{TX2}	– 0.3	0	0.3	
V_L = 0 dBm, f = 3.4 kHz, with respect to G_{TX2}		– 0.1	0	0.1	
V_L = +3.0 dBm, f = 1.0 kHz, with respect to G_{TX2}		– 0.15	0	0.15	
V_L = – 48 dBm, f = 1.0 kHz, with respect to G_{TX2}		—	±0.1	—	
Transmit Distortion (at Pin 11)	THD_T				%
(f = 300 Hz to 4.0 kHz, – 40 dBm ≤ V_{T-R} ≤ +5.0 dBm)		—	0.05	—	
Receive Current Gain (I_{EP}/I_{RXI})	G_{RX1}	94	102	110	mA/mA
Receive Voltage Gain (V_L/V_{RXI}) (R_L = 600 Ω)					dB
V_{RXI} = 0 dBm, f = 1.0 kHz	G_{RX2}	– 0.3	0	0.3	
V_{RXI} = 0 dBm, f = 3.4 kHz, with respect to G_{RX2}		– 0.1	0	0.1	
V_{RXI} = +3.0 dBm, f = 1.0 kHz, with respect to G_{RX2}		– 0.15	0	0.15	
V_{RXI} = – 48 dBm, f = 1.0 kHz, with respect to G_{RX2}		—	±0.1	—	
Receive Distortion	THD_R	—	0.05	—	%
(f = 300 Hz to 4.0 kHz, – 40 dBm ≤ V_{RXI} ≤ +5.0 dBm)					
Return Loss (Reference = 600 Ω resistive, f = 1.0 kHz)	RL	30	>40	—	dB
Transhybrid Rejection (R_L = 600 Ω resistive, f = 1.0 kHz, Figure 4)	THR	—	44	—	dB

LONGITUDINAL SIGNALS (V_{CM} = 1.0 Vrms, see Figures 1 and 2)

2-Wire Balance, f = 1.0 kHz, Z_{ac} = 600 Ω (@ Tip/Ring)	LB	58	64	—	dB
4-Wire Balance, f = 1.0 kHz, Z_{ac} = 600 Ω (@ V_{TX})		58	64	—	
2-Wire Balance, f = 330 Hz, Z_{ac} = 600 Ω (@ Tip/Ring)		58	64	—	
4-Wire Balance, f = 330 Hz, Z_{ac} = 600 Ω (@ V_{TX})		58	64	—	
2-Wire Balance, f = 3.3 kHz, Z_{ac} = 600 Ω (@ Tip/Ring)		53	60	—	
4-Wire Balance, f = 3.3 kHz, Z_{ac} = 600 Ω (@ V_{TX})		53	60	—	
2-Wire Balance, f = 1.0 kHz, Z_{ac} = 900 Ω (@ Tip/Ring)		—	62	—	
4-Wire Balance, f = 1.0 kHz, Z_{ac} = 900 Ω (@ V_{TX})		—	62	—	
Signal Balance, f = 1.0 kHz (Figure 3)		40	55	—	
Longitudinal Impedance, RS = 9100 Ω	Z_{Long}	150	180	210	Ω
Maximum Longitudinal Current, per side	$I_{Long(max)}$				mA
f = 1.0 kHz, I_{Loop} = $I_{L(min)}$, C_T = 0.1 μF		8.5	16	—	
V_{EE} = – 42, VCM = 5.12 Vrms					

ELECTRICAL CHARACTERISTICS (V_{EE} = – 24 V, V_{DD} = +5.0 V, unless otherwise noted. V_{CC}=V_{AG}=V_{DG}= 0 V, T_A = 25°C, see Figure 1.)

Characteristic	Symbol	Min	Typ	Max	Unit
LOGIC INTERFACE					
ST1 Output Voltage					Vdc
Low (I_{ST1} = 1.0 mA, V_{DD} = 5.5 V)	V_{OL}	V_{DG}	0.17	0.4	
High (I_{ST1} = – 100 µA, V_{DD} = 4.5 V)	V_{OH}	2.4	3.2	—	
ST2 Output Voltage					
Low (I_{ST2} = 1.0 mA, V_{DD} = 5.5 V)	V_{OL}	V_{DG}	0.17	0.4	
High (I_{ST2} = – 100 µA, V_{DD} = 4.5 V)	V_{OH}	2.4	4.3	—	
Time Delay					µs
Hookswitch Closure to ST1 Change	t_{ST11}	—	10	—	
Hookswitch Opening to ST1 Change	t_{ST12}	—	200	—	
Hookswitch Closure to 90% of Loop Current (C_T = 0.1 µF)	t_{HS}	—	19	—	ms
PDI Taken High-to-Low to 10% of Loop Current	t_{ST21}	—	18	—	ms
PDI Taken Low-to-High to 90% of Loop Current	t_{ST22}	—	10	—	µs
PDI Input Current	I_{IH}				µA
V_{PDI} = 3.0 V, R_L = 367 Ω, V_{DD} = 5.0 V		– 1250	– 800	– 300	
V_{PDI} = 0 V, R_L = 367 Ω, V_{DD} = 5.5 V		—	– 800	—	
PDI Input Voltage					Vdc
Low	V_{IL}	V_{DG}	—	0.8	
High	V_{IH}	2.0	—	V_{DD}	
MISCELLANEOUS					
V_{QB} Voltage (V_{QB} – V_{EE})	V_{QB}				Vdc
@ I_L = 20 mA		—	0.82	—	
@ I_L = 40 mA		—	0.95	—	
TXO Offset Voltage (V_{TXO} – V_{AG}) @ R_L = 600 Ω	V_{TXO}	– 400	+30	+400	mVdc
TXO Output Current	I_{TXO}	±275	±800	—	µA pk
RXI Offset Voltage (V_{RXI} – V_{AG}) @ R_L = 600 Ω	V_{RXOS}	—	0.8	—	mVdc
V_{AG} Input Current @ R_L = 600 Ω	I_{VAG}	—	0.2	—	µA
Idle Channel Noise (with C-message filter, R_L = 600 Ω)					dBrnc
@ TXO (Pin 11)	N_{IC4}	—	– 10	—	
@ Tip/Ring	N_{IC2}	—	– 5.0	—	
Thermal Resistance — Junction to Ambient	θ_{JA}				°C/W
(Either package, in still air, soldered to a PC board) (@ T_A = +25°C)		—	62	—	
(@ T_A = +85°C)		—	36	—	

Figure 1. Test Circuit

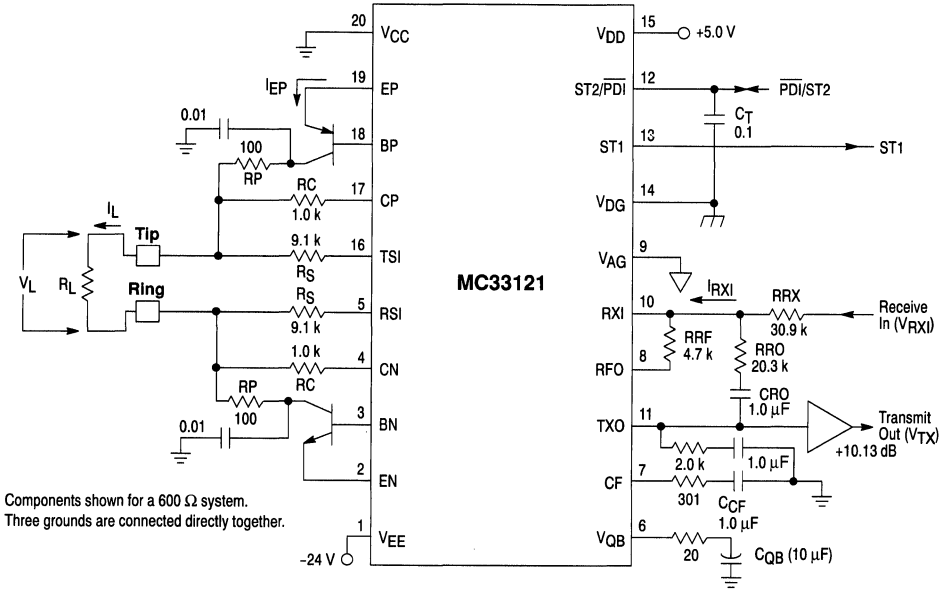


Figure 2. Longitudinal Balance Test

(Per IEEE-455)

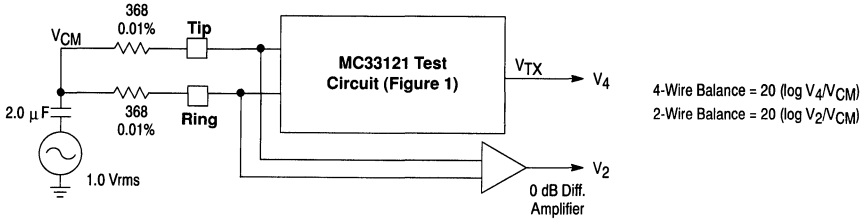


Figure 3. Signal Balance Test

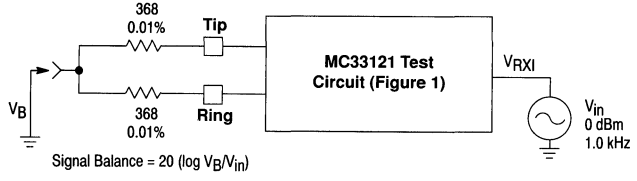
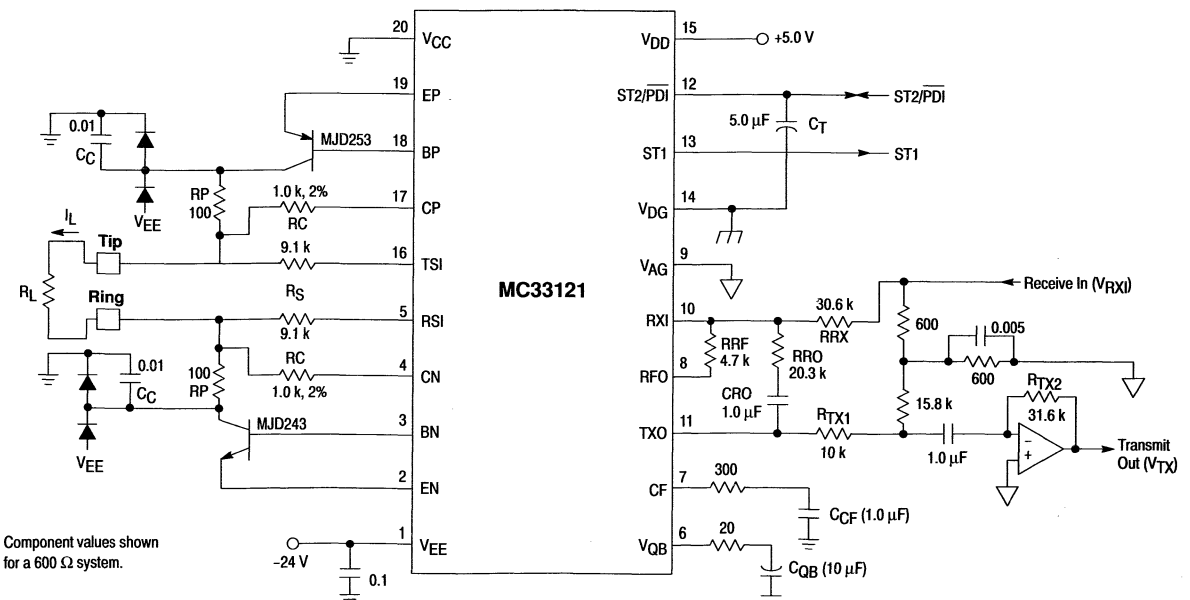


Figure 4. Application Circuit



PIN FUNCTION DESCRIPTION

Symbol	Pin		Description
	DIP	PLCC	
V_{CC}	20	28	Connect to noise-free battery ground. Carries loop current and some bias currents.
EP	19	27	Connect to the emitter of the PNP pass transistor.
BP	18	26	Connect to the base of the PNP pass transistor.
CP	17	24	Connect to TIP through a current limiting protection resistor (R_C). CP is the noninverting input to the internal transmit amplifier (Figure 28). Input impedance is 31 kΩ.
TSI	16	23	Sense input. Connect to TIP through a current limiting protection resistor (R_S) which also sets the longitudinal impedance. Input impedance is ≈100 Ω to V_{CC}.
V_{DD}	15	22	Connect to a +5.0 V, ±10% supply, referenced to digital ground. Powers logic section and provides some bias currents for the loop current drivers.
V_{DG}	14	20	Digital Ground. Reference for ST1, ST2 and V_{DD}. Connect to system digital ground.
ST1	13	18	Status Output (TTL/CMOS). Indicates hook switch status — high when on-hook, low when off-hook, and pulse dialing information. Used with ST2 to indicate fault conditions.
ST2/PDI	12	17	Status output and an input (TTL/CMOS). As an output, ST2 can indicate hook status — Low when on-hook, high when off-hook. Used with ST1 to indicate fault conditions. As an input, it can be taken low (when off-hook) to deny subscriber loop current.
TXO	11	16	Transmit voltage output. Amplitude is ≈1/3 that across CP and CN. Nominally capable of 800 μA output current. DC referenced to V_{AG}.
RXI	10	14	Receive current input. Current at this pin is multiplied by 102 at EP and EN to generate loop current. RXI is a virtual ground at V_{AG} level. Current flow is out of this pin.
V_{AG}	9	13	Analog ground, reference for TXO and RXI. Connect to system analog ground. Current flow is into this pin.
RFO	8	12	A resistor from this pin and RXI sets the maximum loop current and DC feed resistance. Minimum resistor value is 3.3 k (see Figures 5 to 7).
CF	7	10	A low leakage capacitor between this pin and V_{AG} provides DC and AC signal separation. A series resistor is required for battery supply turn-on/off transient protection (Figure 4).
V_{QB}	6	8	Quiet Battery. A capacitor between V_{QB} and V_{CC} filters noise and ripple from V_{EE}, providing a quiet battery source for the speech amplifiers. A series resistor is required for battery supply turn-on/off transient protection (Figure 4).
RSI	5	7	Sense input. Connect to RING through a current limiting protection resistor which also sets the longitudinal impedance. Input impedance is ≈100 Ω to V_{QB}.
CN	4	6	Connect to RING through a current limiting protection resistor. CN is the inverting input to the internal transmit amplifier (Figure 28). Input impedance is 31 kΩ.
BN	3	4	Connect to the base of the NPN pass transistor.
EN	2	3	Connect to the emitter of the NPN pass transistor.
V_{EE}	1	2	Connect to battery voltage (– 21.6 V to – 42 V).

(Pins 1, 5, 9, 11, 15, 19, 21, and 25 are not internally connected on the PLCC package.)

Figure 5. Loop Current versus Loop Resistance and RRF

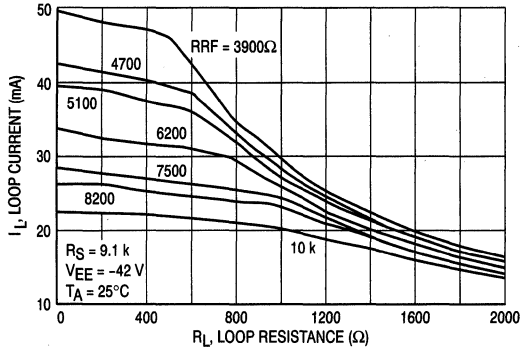


Figure 6. Loop Current versus Loop Resistance and RRF

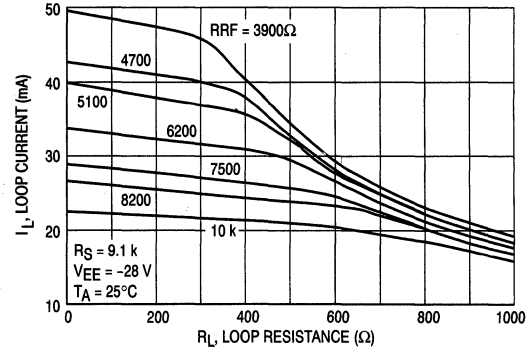


Figure 7. Loop Current versus Loop Resistance and RRF

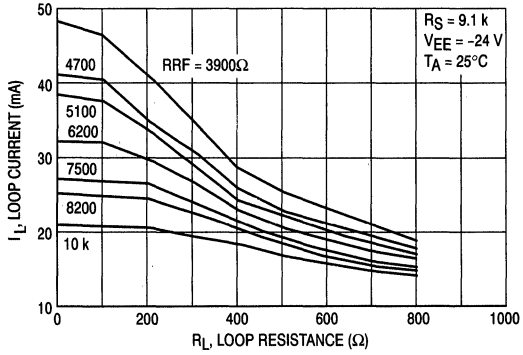


Figure 8. Off-Hook to On-Hook Threshold versus RRF

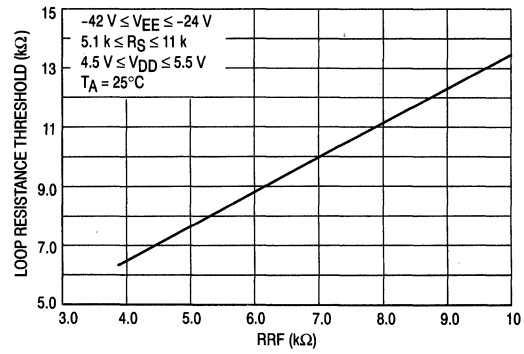


Figure 9. On-Hook to Off-Hook Threshold versus R_S

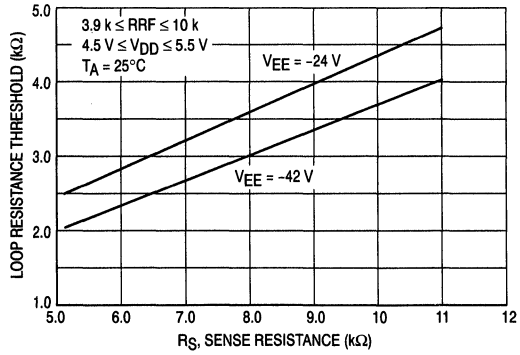


Figure 10. I_{DD} versus Loop Current

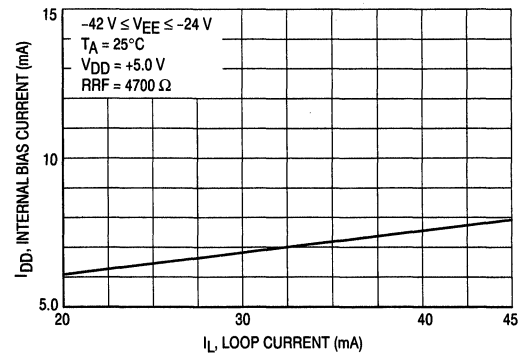


Figure 11. Fault Threshold (On-Hook) versus R_S

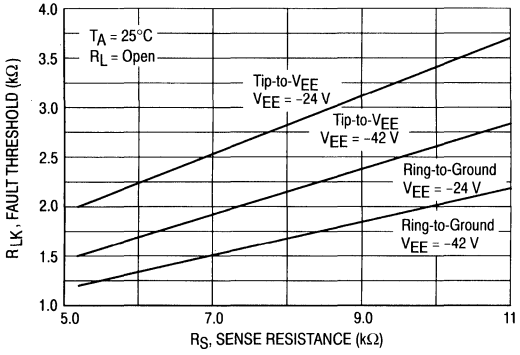


Figure 12. Fault Threshold (Off-Hook) versus Loop Resistance

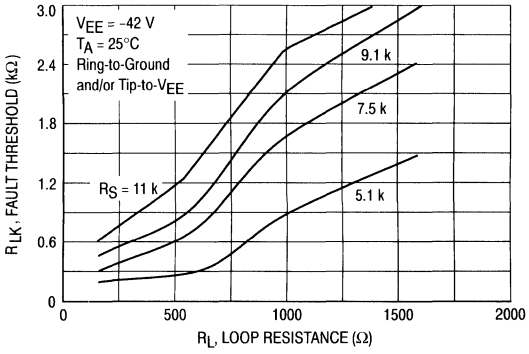


Figure 13. Fault Threshold (Off-Hook) versus Loop Resistance

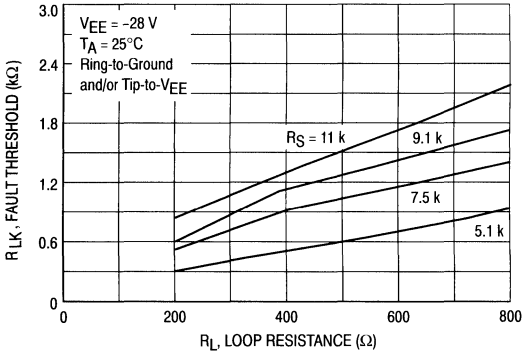


Figure 14. Fault Threshold (Off-Hook) versus Loop Resistance

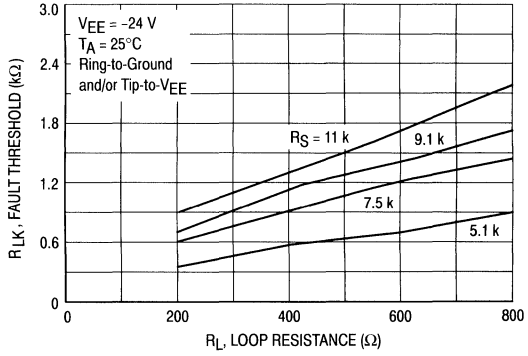


Figure 15. Fault Threshold (Off-Hook) versus R_S

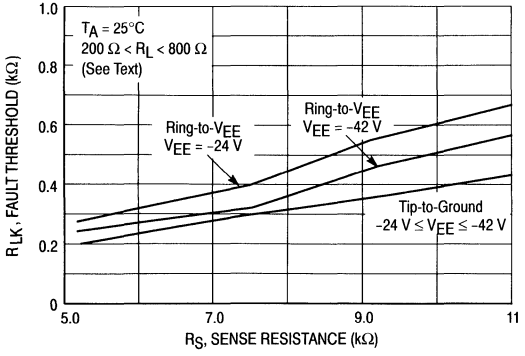


Figure 16. V_{DD} Ripple Rejection versus Frequency

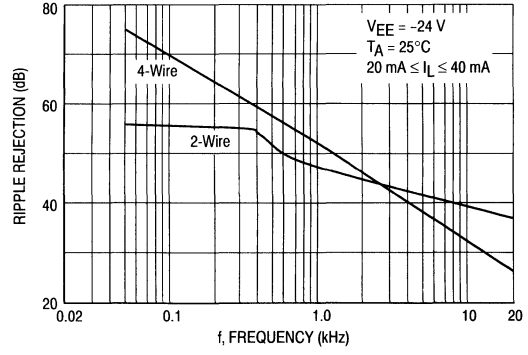


Figure 17. V_{EE} Ripple Rejection versus Frequency

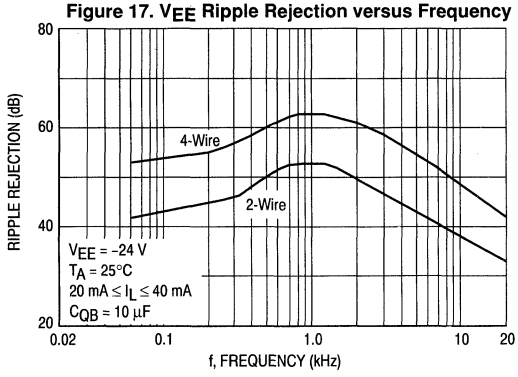


Figure 18. V_{EE} Ripple Rejection versus Frequency and C_{QB}

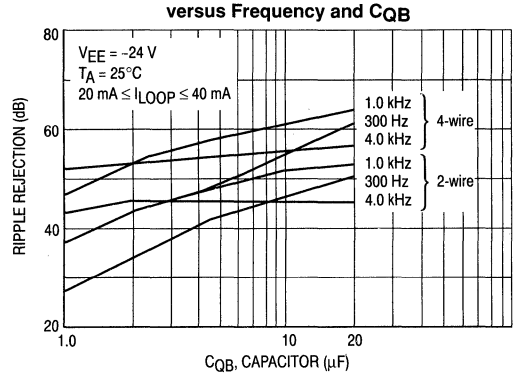


Figure 19. ST1, V_{OL} versus I_{OL}

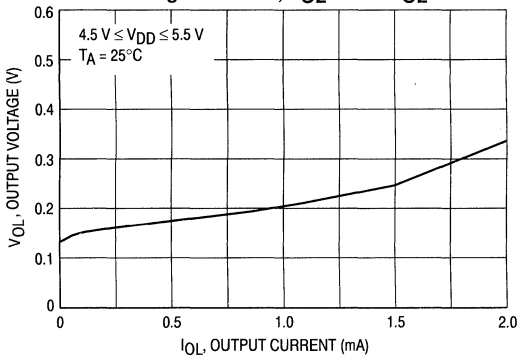


Figure 20. ST1, V_{OH} versus I_{OH}

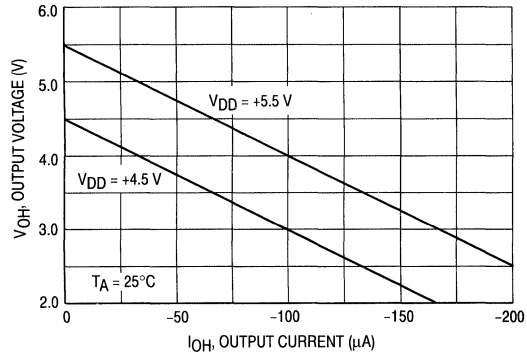


Figure 21. ST2, V_{OL} versus I_{OL}

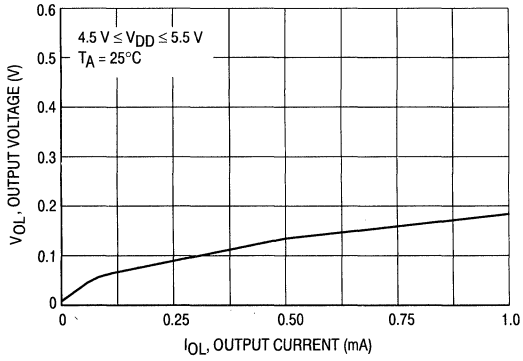


Figure 22. ST2, V_{OH} versus I_{OH}

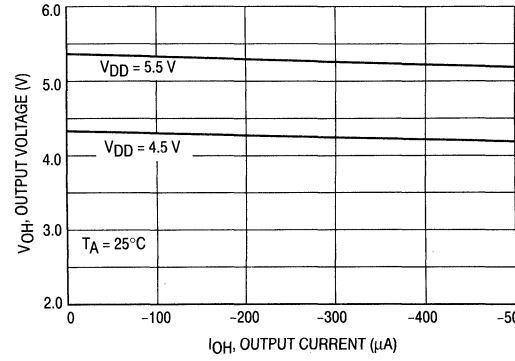


Figure 23. IC Power Dissipation versus Loop Resistance and RRF

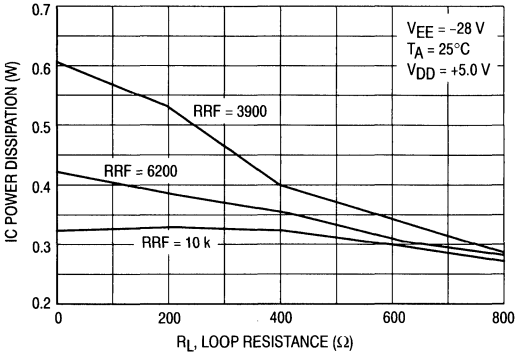


Figure 24. Transistor Power Dissipation versus Loop Resistance and RRF

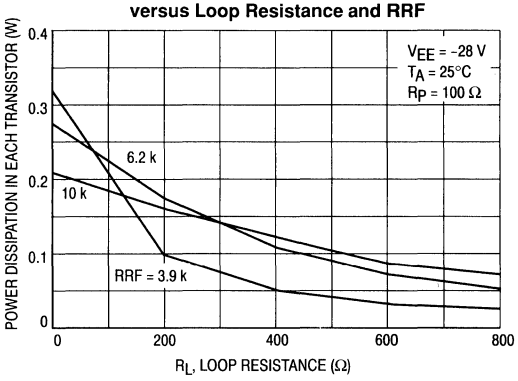


Figure 25. Maximum Longitudinal Current versus Loop Current

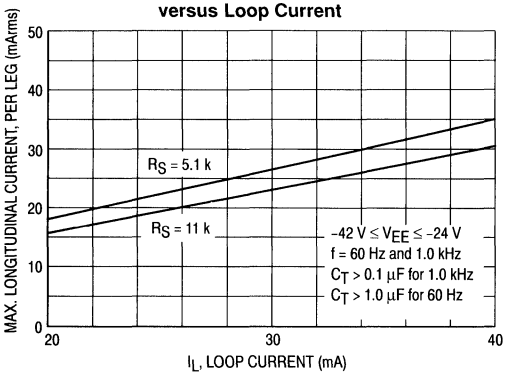
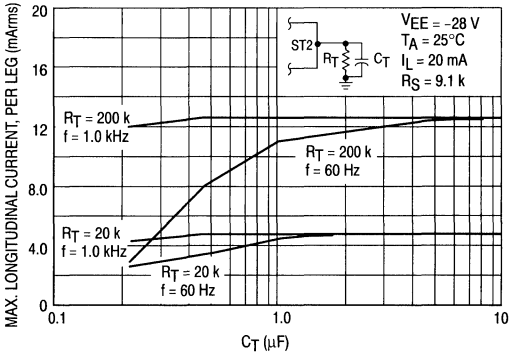


Figure 26. Maximum Longitudinal Current versus C_T, R_T and Frequency



Introduction

The MC33121 is a solid state SLIC (Subscriber Line Interface Circuit) which provides the interface between the two wire telephone line and the four wire side of a Central Office or PBX. Most of the BORSCHT functions are provided, specifically:

— **B**attery feed of the loop current to the line, with programmable maximum current for short lines and battery feed resistance for long lines.
— **O**vervoltage protection through internal clamp diodes and external resistors and diodes.
— **S**upervision, in that hook status is indicated in the presence of ≥30 kΩ leakage, and regardless of whether or not the circuit is powered down intentionally by the Central Office or PBX. Fault conditions are detected and indicated to the system. Dialing (pulse and DTMF) information is passed through the MC33121 to the 4-wire side.
— **H**ybrid function, in that the MC33121 is a 2-to-4 wire converter. Transmit, receive, return loss, and transhybrid gains are independently adjustable.

The MC33121 does not provide ring insertion, ring trip, digital coding/decoding of the speech signals, nor test functions. These must be provided external to this device.

The MC33121 controls two external transistors (one NPN and one PNP) through which the loop current flows. By appropriate circuit design, the power dissipation (which can exceed 3.0 W under certain worst case conditions) is approximately equally distributed among the two transistors and the IC, thereby lowering junction temperatures and increasing long term reliability. In most situations, heatsinks will not be required.

The MC33121 incorporates critical sense resistors internally, which are trimmed for optimum performance. With this technique, the external resistors on the two wire side, which generally must be high wattage for transient protection reasons, can be non-precision.

Longitudinal balance is tested to a minimum of 58 dB @ 1.0 kHz (refer to Electrical Characteristics and Figure 2) for both the two-wire and four-wire side, and typically measures in the mid-60s. The longitudinal current capability is tested to a minimum of 8.5 mArms per side (refer to Electrical Characteristics and Figure 2) at a loop current of 20 mA.

Following is a description of the individual sections. Figure 4 is the reference schematic.

DC Loop Current

The DC loop current is determined by the battery voltage (V_{EE}), the load resistance across Tip and Ring, and the resistor at RFO. Varying the 4 resistors R_S and RC will influence the loop current a small amount (<5%). The curves of Figures 5 to 7 indicate the loop current versus loop resistance, different values of RRF, and for various values of V_{EE}. The graphs represent performance at T_A = 25°C and after the IC had reached a steady state temperature (>5 minutes).

Figure 27. DC Loop Current Path

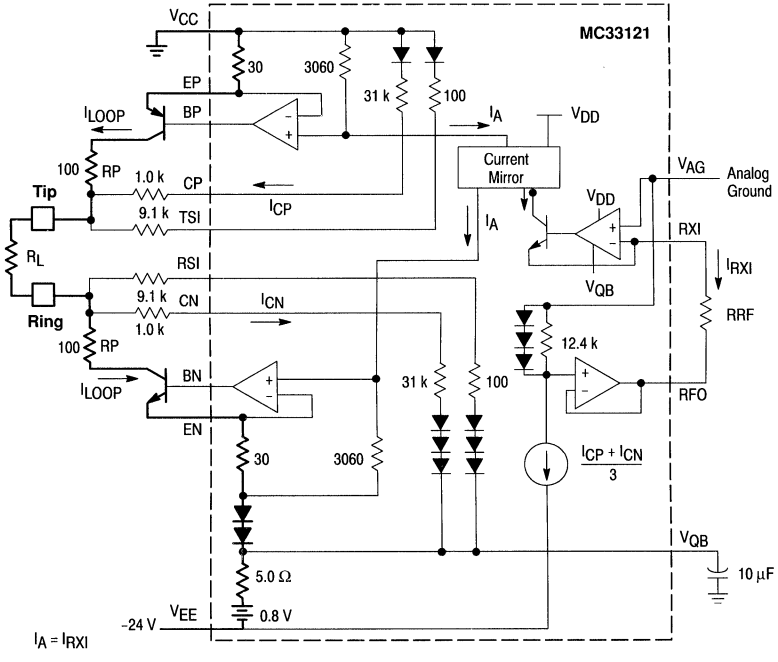


Figure 27 is representative of the DC loop current path (bold lines). On a long line (R_L > 400 Ω), the loop current can be determined from the following equation:

$$I_L = \frac{(|V_{EE}| - 3.6\ V) \bullet 13}{RRF + \{(R_L + 5) \bullet 13\}} \quad (1)$$

On short lines (R_L < 400 Ω), the three diodes across the 12.4 k resistor clamp the voltage at RFO, thereby preventing the RXI current from increasing as the load resistance is decreased. The maximum loop current is:

$$I_{L(max)} = \frac{1.85\ V \bullet 102}{RRF} \ (T_A = 25°C) \quad (2)$$

Due to the temperature dependence of a diode's forward voltage, the maximum loop current will change with temperature by ≈ –0.3%/°C.

The battery feed resistance ($\Delta V_{TIP}/\Delta I_L$) is ≈400 Ω, but depends on the loop current, V_{EE}, RRF, and is a valid parameter only on long lines where the current limit is not in effect. On short lines, the feed resistance is high since the loop current is clamped at a near constant level. The AC impedance (Return Loss) however, is not determined nor affected by the DC parameters. See the Applications Section for Return Loss information.

Transmit Path

The transmit path, shown in Figure 28, consists of an internal amplifier which has inputs at CP and CN, and its output at TXO. The gain is internally fixed at 0.328 V/V (–9.7 dB). The output is in phase with the signal at CP (normally the same as TIP), and is out of phase with the signal at CN. The signal at TXO is also out of phase with that at V_{RX}, the receive signal input, described in another section.

The TXO output can swing ≈3.0 Vp-p, with a nominal current capability of ±800 µA peak (±275 µA minimum). The load on TXO is the parallel combination of RTX1 and the RRO network (described later). TXO is nominally internally biased at the V_{AG} DC level, but has an offset which varies with loop current.

In normal applications, the signal at CP/CN is reduced slightly from that at Tip/Ring by the voltage divider composed of the external RC resistors, and the internal 31 k resistors. The value of the RC resistors depends on the transient protection needed, described in another section, with 1.0 kΩ resistors being suitable for most applications. The resulting signal at TXO needs to be gained up to obtain 0 dB from Tip/Ring to V_{TX} (the 4-wire output). The common method involves an external op amp, as shown in Figure 28, with a gain of RTX2/RTX1. The gain from V_L to V_{TX} is:

$$\frac{V_{TX}}{V_L} = \frac{RTX2 \bullet 31\ k \bullet 0.328}{RTX1 \bullet (RC + 31\ k)} \quad (3)$$

If a codec/filter is used, many of which include an internal op amp, a separate op amp is not needed. CTX is primarily for DC blocking (of the TXO offset), and is usually large (1.0 µF) so as to not affect the gain.

Receive Path

The receive path, shown in Figure 29, consists of the input at RXI, the transistor driver amplifiers, the external transistors, and the load at Tip/Ring.

RXI is a virtual ground (DC level = V_{AG}) and is a current input. Current flow is out of the pin. The RXI current is mirrored to the two transistor drivers which provide a gain of 102. The two external transistors are then two current sources, in series, operating at the same value. An additional internal circuit (not shown) balances the two current sources to maintain operation in their linear region.

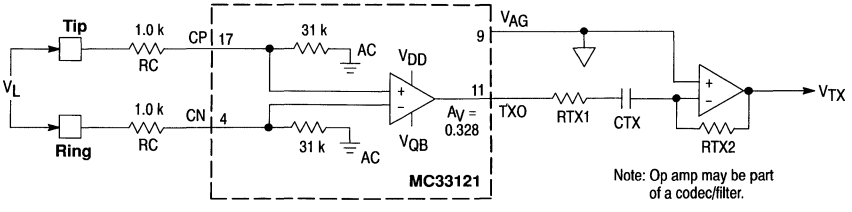
The load current (through R_L) is slightly different from the transistor current due to the sense resistors RC and RS. The sense resistors add to the DC loop current, but subtract from the AC load current.

In normal operation, the current at RXI is composed of a DC current (from RFO), an AC current (from V_{RX}) which is the receive signal, and an AC current from TXO, which is the feedback signal to set the return loss (setting the return loss is discussed in the section on AC Terminating Impedance). The resulting AC signal at Tip is inverted from that at V_{RX}, while the signal at Ring is in phase with V_{RX}.

The resistors RP are for transient protection, and their value (defined in another section) depends on the amount of protection required. A nominal value of 100 Ω is suitable for most applications.

The system receive gain, from V_{RX} to Tip/Ring, is not described in this section since in normal applications, it involves the feedback which sets the AC terminating impedance. The Applications Section discusses these in detail.

Figure 28. Transmit Path



Logic Interface (Hook status, pulse dialing, faults)

The logic interface section provides hookswitch status, fault information, and pulse dialing information to the 4-wire side of the system at the ST1 and ST2 outputs. Figure 30 is a representative diagram.

The logic outputs operate according to the truth table in Table 1:

Table 1. Status Output Truth Table

Hook Status	Fault Detection	Outputs ST 1	Outputs ST2	Circuit Condition
On-Hook	No Fault	Hi	Lo	Internally powered down
Off-Hook	No Fault	Lo	Hi	Powered up
On-Hook	Fault	Lo	Lo	Internally powered down
Off-Hook	Fault	Lo	Lo	Internally powered down

Referring to Figure 30, ST1 is configured as an active NPN pulldown with a 15 kΩ pullup resistor. ST2 has a 800 µA current source pullup, and a 1.0 mA current source for a pulldown. Current limiting this output controls the discharge from the external capacitor when ST2 switches low.

The condition where both ST1 and ST2 are high is not valid, but may occur momentarily during an off-hook to on-hook transition. The condition where both ST1 and ST2 are low may occur momentarily during an on-hook to off-hook transition — this should not be interpreted as a fault condition. ST1 and ST2 are TTL/CMOS compatible and are powered by the +5.0 V supply (V_{DD}). Refer to the Applications Section for more details.

Power Supplies, Grounds

The MC33121 requires 2 power supplies: battery voltage between – 21.6 V and – 42 V (V_{EE}), and an auxiliary voltage between +4.5 V and +5.5 V (V_{DD}).

V_{EE} is nominally – 24 V, with a typical range of – 21.6 V to – 42 V, and must be referenced to V_{CC} (battery ground). A 0.1 µF bypass capacitor should be provided between V_{CC}

Figure 29. Receive Path

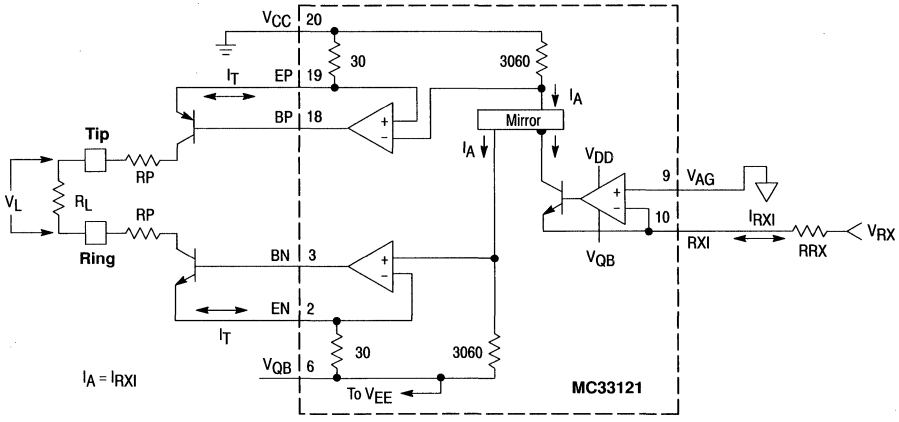
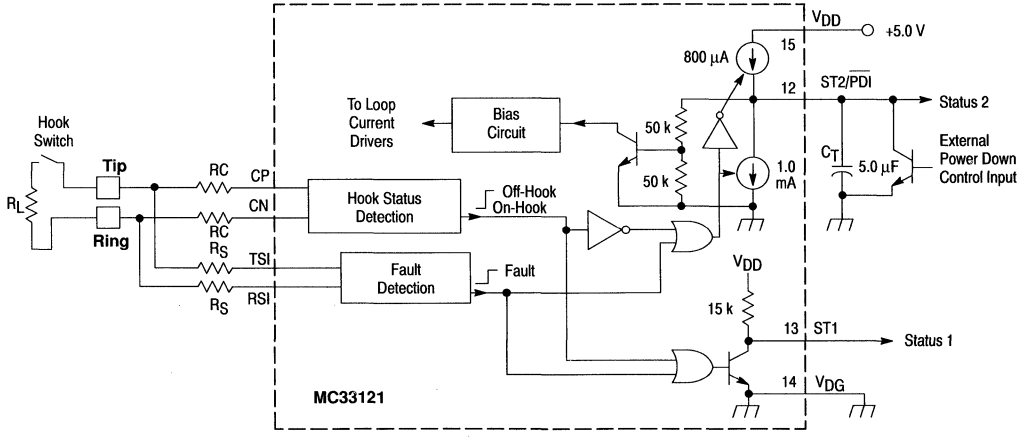


Figure 30. Logic Interface



and V_{EE}. The V_{EE} current (I_{EE}) is nominally 1.0 mA when on-hook, 8.0 to 12 mA more than the loop current when off-hook, and ≈5.0 mA when off-hook but powered down by using the PDI pin. Ripple and noise rejection from V_{EE} is a minimum of 40 dB (with a 10 μF capacitor at V_{QB}), and is dependent on the size and quality of the V_{QB} capacitor (C_{QB}) since V_{QB} is the actual internal supply voltage for the speech amplifiers. The absolute maximum for V_{EE} is – 60 V, and should not be exceeded by the combination of the battery voltage, its tolerance, and its ripple.

V_{DD} is normally supplied from the line card's digital +5.0 V supply, and is referenced to V_{DG} (digital ground). A 0.1 μF capacitor should be provided between V_{DD} and V_{DG}. The V_{DD} current (I_{DD}) is nominally 1.7 mA when on-hook and between 6.0 and 8.0 mA when off-hook (see Figure 10). When the MC33121 is intentionally powered down using the PDI pin, I_{DD} changes by <1.0 mA from the normal off-hook value.

V_{AG} is the analog ground for the MC33121, and is the reference for the speech signals (RXI and TXO). Current flow is **into** the pin, and is typically <0.5 μA.

Normally, V_{CC}, V_{DG} and V_{AG} are to be at the same DC level. However, if strong transients are expected at Tip and Ring, as in a Central Office application, or any application where the phone line is outdoors, V_{CC} should not be connected directly to V_{DG} and V_{AG} in order to prevent possible damage to the +5.0 V system. The MC33121 is designed to tolerate as much as ±30 V between V_{CC} and the other two grounds on a transient basis only. This feature permits V_{CC} and the other grounds to be kept separate (on an AC basis) on the line card by transient suppressors, or to be connected together farther into the system (at the power supplies). See the Applications Section on ground arrangements and transient protection for further information on connecting the MC33121 to the system supplies.

2

APPLICATIONS INFORMATION

This section contains information on the following topics:

Design Procedure

This section describes the step-by-step sequence for designing in the MC33121 SLIC into a typical line card application for either a PBX or Central Office. The sequence is important so that each new component value which is calculated does not affect components previously determined. Figure 4 (Typical Application Circuit) is the reference circuit for most of this discussion. The recommended sequence (detailed below), consists of establishing the DC aspects first, and then the AC aspects:

1) Determine the maximum loop current for the shortest line, select RRF. Power dissipation must be considered here.
2) Select the main protection resistors (RP), and diodes, based on the expected transient voltages. Transient protection configuration must also be considered here.
3) Select RC based on the expected transient voltages.
4) Select RS based on the desired longitudinal impedance at Tip and Ring. Transient voltages are also a factor here.
5) Calculate RRO based on the desired AC terminating impedance (return loss).
6) Calculate RRX based on the desired receive gain.
7) Calculate RTX2 and RTX1 based on the desired transmit gain.
8) Calculate the balance resistor (RB), or network, as appropriate for desired transhybrid rejection.
9) Logic Interface

Preliminary

There is a primary AC feedback loop which has its main sense points at CP and CN (see Figure 34). The loop extends from there to TXO, through RRO to RXI, through the internal amplifiers to the transistor drivers, through RP to Tip and Ring, and through the RCs to CP and CN. Components within this loop, such as RP, RC, the transistors, and the compensation capacitors need not be tightly matched to each other in order to maintain good longitudinal balance. The tolerance requirements on these components, and others, are described in subsequent sections. Any components, however, which are placed outside the loop for additional line card functions, such as test relay contacts, fuses, resistors in series with Tip and Ring, etc. will affect longitudinal balance, signal balance, and gains if their values and mismatch is not carefully considered. The MC33121 cannot compensate for mismatch among components outside the loop.

The compensation capacitors (0.01 μF) shown at the transistor collectors (Figure 4) compensate the transistor driver amplifiers, providing the required loop stability. The required tolerance on these capacitors can be determined from the following guidelines:

- A 10% mismatch (±5% tolerance) will degrade the longitudinal balance by ≈1.0 dB on a 60 dB device, and by ≈3.0 dB on a 70 dB device.
- A 20% mismatch (±10% tolerance) will degrade the longitudinal balance by ≈3.0 dB on a 60 dB device, and by ≈6.0 dB on a 70 dB device.

High quality ceramic capacitors are recommended since they serve the secondary function of providing a bleedoff path for RF signals picked up on the phone line. These capacitors should be connected to a good quality RF ground.

The capacitors used at C_{QB} and C_F must be low leakage to obtain proper performance. Leakage at the C_{QB} capacitor will affect the DC loop current characteristics, while leakage at the C_F capacitor will affect the AC gain parameters, and possibly render the IC inoperative.

1) Maximum Loop Current and Battery Feed Resistance

The maximum loop current (at R_L = 0) is determined by the RRF resistor between RFO and RXI. The current limit is accomplished by three internal series diodes (see Figure 27) which clamp the voltage across RRF as the loop resistance decreases, thereby limiting the current at RXI. Since the loop current is 102 x I_{RXI}, the loop current is therefore clamped. The graphs of Figures 5 to 7 indicate the maximum

loop current at an ambient temperature of +25°C, and after the IC has reached thermal equilibrium (approx. 10 minutes).

Although the maximum loop current is primarily a function of the RRF resistor, it is also affected by ambient temperature, and slightly by V_{EE}. The ambient temperature effects are due to the temperature dependence of the diodes' forward voltage drop, causing the maximum loop current to change by $\approx -0.3\%/°C$. Changing V_{EE} affects the maximum current in that the power dissipation is changed, thereby changing the die temperature, which affects the diodes' voltage.

The maximum loop current is affected slightly (<5%) by the choice of the RS and RC resistors, since the sense currents through those resistors add to the current supplied by the transistors.

The battery feed resistance is determined by RRF, and is not adjustable independently of the current limit. Defined as $\Delta V_{TIP}/\Delta I_L$, it is ≈400 Ω, and is a valid parameter only on long lines where the current limit is not in effect. On short lines, the feed resistance is high since the loop current is clamped at a near constant level. The AC impedance (Return Loss) however, is not determined nor affected by these DC parameters. Return loss is discussed in another section.

If the application requires that the current limit value have a low temperature dependence, refer to the section following this design sequence which describes an alternate configuration.

2) Main Protection Resistors (RP) and Transient Currents

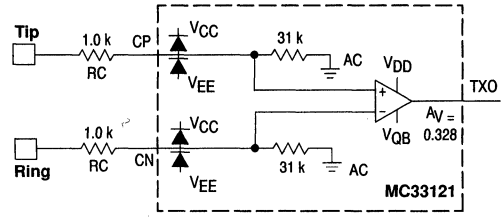
The purpose of the protection resistors (RP), along with the 4 clamp diodes shown in Figure 4, is to absorb the bulk of the transient energy when transient voltages come in from the phone line. The resistor value must be selected to limit the transient current to a value which can be tolerated by the diodes, while dissipating the energy. The recommended value shown (100 Ω) will limit the current from a 1500 V transient to 15 A, which can be carried by 1N4002 diodes under surge conditions. The resistors must be of a type which can tolerate the high instantaneous energy associated with transients. Resistor manufacturers should be consulted for this information.

Referring to Figure 4, a positive transient on either Tip or Ring, or both, will cause the transient current to be delivered to Ground. A negative transient will cause the transient current to come from the V_{EE} supply line. Therefore, the PC board track supplying V_{CC} and V_{EE} to the MC33121 must be designed to carry the transient currents as well as the normal operating currents. Additionally, since a negative transient will cause a current flow **out** of the power supply's negative output, which is opposite to the normal flow of current, provisions must be made for this reverse current flow. One suggested method is to place a zener transient suppressor (1N6287 for –42 V, 1N6282 for –28 V and –24 V) across the battery supply pins (V_{CC} to V_{EE}) physically adjacent to the MC33121. The inductance associated with PC board tracks and wiring will result in insufficient protection for the MC33121 if the suppressor is located at the opposite end of the line card, or at the power supplies.

Transient currents can be reduced by increasing the value of RP, with an upper limit determined by the DC conditions on the longest line (highest loop resistance) and minimum V_{EE} supply voltage. These conditions determine the minimum DC voltage across the transistors, which must be sufficient to handle the largest AC (transmit and receive) signals. If too large a value is selected for RP, the AC signals will be clipped. It is recommended that each transistor have no less than one volt (DC) across their collector to emitter. System AC specifications may require more than this.

Since the RP resistors are within the loop, their tolerance can be ±5% with no substantial degradation of longitudinal balance. A ±10% tolerance (20% mismatch) will degrade balance by ≈4.0 dB on a 65 dB device.

Figure 32. RC Protection Resistors



3) Selecting the RC Resistors

The primary purpose of the RC resistors is to protect the CP and CN pins from transient voltages and destructive currents. Internally, these pins have clamp diodes to V_{CC} and V_{EE} rated for a maximum of 1.0 A under surge conditions only (Figure 32). The 1.0 kΩ resistors shown in the figures, for example, will provide protection against surges up to 1.0 kV. Resistor manufacturers must be consulted for the proper type of resistor for this environment.

The RC resistors are in series with internal 31 kΩ resistors, and therefore form a voltage divider to the inputs of the transmit amplifier, as shown in Figure 32. This will affect the transmit gain, receive gain, return loss, and transhybrid rejection (described in subsequent sections). The tolerance of the RC resistors depends on the value selected for them, since any mismatch between them will create a differential voltage at CP and CN when longitudinal voltages are present on Tip and Ring. To ensure a minimum of 58 dB of longitudinal balance, the resistors' absolute value must not differ by more than 39 Ω. With a nominal value of 1.0 kΩ, their tolerance must be ±2%, or less. If their nominal value is 390 Ω or less, their tolerance can be ±5%.

4) Longitudinal Impedance (Z_{Long}) — Selecting the R_S Resistors

The longitudinal impedance is determined by the R_S resistors at the TSI and RSI pins according to the following equation:

$$Z_{Long} = \frac{R_S + 100}{51} \qquad (4)$$

Z_{Long} is defined as V_{Long}/I_{Long} as shown in Figure 33; for R_S = 9.1 kΩ, Z_{Long} = 180 Ω. The calculated value of Z_{Long} includes the fact that the R_S resistors are in parallel with the synthesized impedance. The tolerance of the R_S resistors therefore depends on how much mismatch can be tolerated between the longitudinal impedances at Tip and at Ring. Calculations indicate the two R_S resistors can have a ±5% tolerance, and still comfortably provide a minimum of 58 dB longitudinal balance.

The resistors must be able to withstand transient voltages expected at Tip and Ring. The TSI and RSI pins have internal clamp diodes rated for a maximum of 1.0 A under surge conditions only (Figure 33). Resistor manufacturers must be consulted for the proper type of resistor for this environment.

5) AC Terminating Impedance and Source Impedance (Z_{ac}) — Return Loss

The return loss measurement is a measure of how closely the AC impedance of the SLIC circuit matches the characteristic impedance of the phone line, or a reference impedance. The reference impedance can be, in some cases, a pure resistance (commonly 600 Ω or 900 Ω), a series resistor and capacitor (900 Ω + 2.16 μF), or a more complex network. To achieve proper return loss with the MC33121, the RRO impedance shown in Figure 34 is to have the same configuration as the reference impedance, but with values scaled according to the equations mentioned below.

CRO, used primarily for DC blocking, is generally a large value (1.0 μF) so as to not affect the impedance of RRO. However, it can be included in the RRO network if a complex network is required.

Figure 33. Longitudinal Impedance

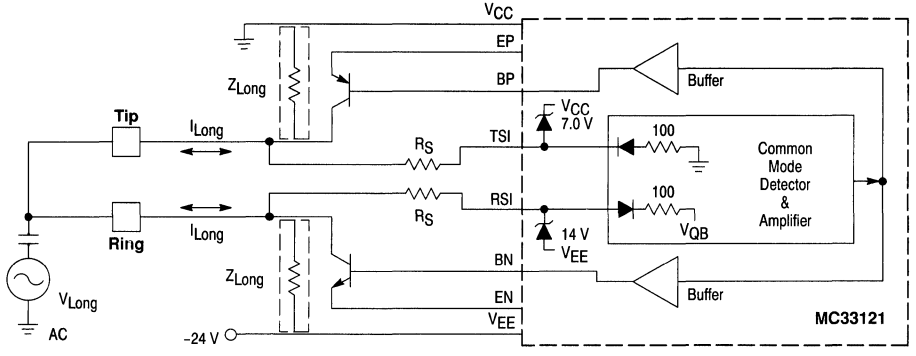
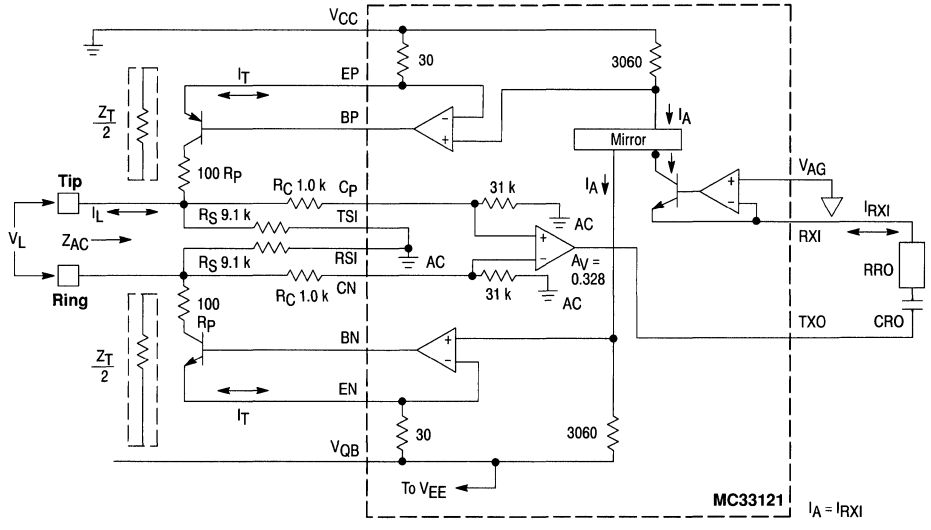


Figure 34. AC Terminating Impedance



Z_{ac} is the impedance looking into the circuit from Tip and Ring (set by RRO), and is defined as V_L/I_L. Half of Z_{ac} is from Tip to V_{CC}, and the other half is from Ring to V_{QB} (an AC ground). Each half is made up of a synthesized impedance ($Z_T/2$) in parallel with R_S and (RC + 31 k). Therefore, Z_{ac} is equal to:

$$Z_{ac} = [Z_T/2 \,//R_S//(RC + 31\ k)] \bullet 2 \qquad (5)$$

$$\text{and } \frac{Z_T}{2} = \frac{\{R_S//(RC + 31\ k)\} \bullet (Z_{ac}/2)}{\{R_S//(RC + 31\ k)\} - (Z_{ac}/2)} \qquad (6)$$

The synthesized impedance Z_T is created as follows:

An incoming signal V_L produces a differential voltage at CP and CN, and therefore at TXO equal to:

$$V_{TXO} = \frac{V_L \bullet 31\ k \bullet 0.328}{(RC + 31\ k)} \qquad (7)$$

The signal at TXO creates an AC current I_{RXI} through RRO. RXI is a virtual ground, and CRO is insignificant for first order calculations.

I_{RXI} is gained up by a factor of 102 to produce the current I_T through the transistors.

Z_T is therefore V_L/I_T. The relationship between Z_T and RRO is:

$$RRO = \frac{Z_T \bullet 1.037 \bullet 10^6}{(31\ k + RC)} \qquad (8)$$

While equation 8 gives the exact value for RRO, a first order approximation is $Z_{ac} \bullet 33.5$.

a) Resistive Loads (with RC = 1.0 k, R_S = 9.1 k):

For a 600 Ω resistive system, Z_T calculates to 626 Ω, and RRO calculates to 20.3 kΩ.

For a 900 Ω resistive system, Z_T calculates to 961 Ω, and RRO calculates to 31.14 kΩ.

b) Complex Loads

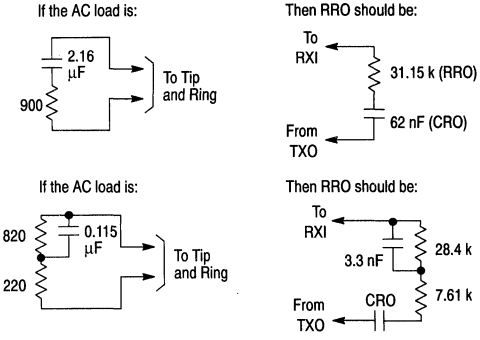
For complex (nonresistive) loads, the MC33121 must be made to look like a termination impedance equal to that complex load. This is accomplished by configuring RRO the same as the complex load, but with all impedance values increased according to the scaling factor of Equation 9.

$$SF = \frac{[(RC + 31\ k)//RS] \bullet 1.037 \bullet 10^6}{(RC + 31\ k) \bullet [(RC + 31\ k)//R_S - (Z_{ac}/2)]} \qquad (9)$$

Z_{ac} is computed at a nominal frequency of interest. A first order approximation of Equation 9 is:

$$SF = 1.037 \bullet 10^6/(RC + 31\ k) \qquad (9a)$$

For example:

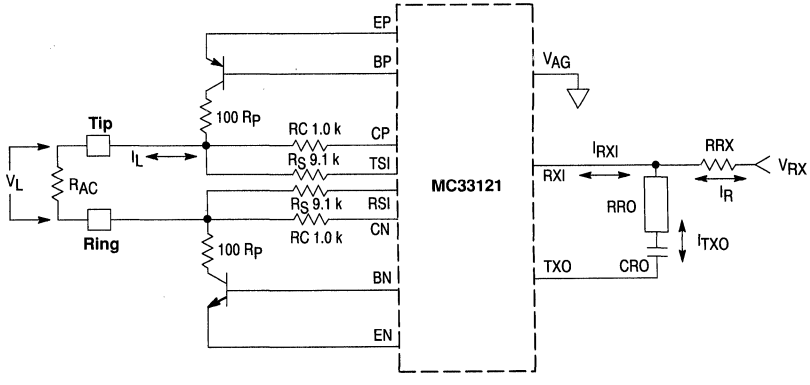


CRO must remain in series with the network to provide DC blocking. If the load network does not include a series capacitor (as in the second example above), CRO should be large (1.0 µF) so its impedance does not affect the RRO network. The above procedure will yield a return loss measurement which is constant with respect to frequency. The RRO resistor, or network, must have a tolerance equal to or better than the required system tolerance for return loss and receive gain.

6) Receive Gain (G_{RX})

The receive gain involves the same circuit as Figure 34, but with the addition of the RRX resistor (or network) which sets the receive gain. See Figure 35.

Figure 35. Receive Gain



The receive gain (G_{RX}), defined as the voltage gain from V_{RX} to V_L, is calculated as follows:

RXI is a virtual ground, and R_{ac} is the AC impedance of the load (phone line).

The AC current generated in the transistors is 102 • I_{RXI}, which is equal to 102 • (I_R – I_{TXO}).

$I_R = V_{RX}/RRX$, and

$$I_{TXO} = \frac{V_{TXO}}{RRO} = \frac{V_L \bullet 31\ k \bullet 0.328}{RRO \bullet (31\ k + RC)} \quad (10)$$

Using equations 5 and 8, involving Z_{ac}, RS and RC, and the above equations yields:

$$\frac{V_L}{V_{RX}} = G_{RX} = \frac{102 \bullet (R_{ac}//Z_{ac})}{RRX} \quad (11)$$

$$\text{Therefore, } RRX = \frac{102 \bullet (R_{ac}//Z_{ac})}{G_{RX}} \quad (12)$$

Equation 12 applies **only** for the case where R_{ac} and Z_{ac} have the same configuration. If they also have the same magnitude, then set RRX = 51 • R_{ac} to set a receive gain of 0 dB. The AC source impedance of the above circuit to Tip and Ring is Z_{ac}. For the case where $R_{ac} \neq Z_{ac}$, use the following equation:

$$\frac{V_L}{V_{RX}} = \frac{102}{RRX \bullet \left[\frac{1}{Z_L} + \frac{1.037 \bullet 10^6}{(31k + RC) \bullet RRO}\right]} \quad (13)$$

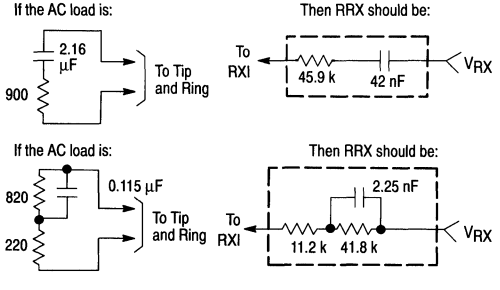
$$\text{where } Z_L = \left[\frac{R_{ac}}{2} // R_S // (RC + 31\ k)\right] \bullet 2 \quad (14)$$

a) Resistive Loads

For a 600 Ω resistive system, set RRX = 30.6 kΩ, and for a 900 Ω resistive system, set RRX = 45.9 kΩ.

b) Complex Loads

For complex (nonresistive) loads, the RRX resistor needs to be replaced with a network having the same configuration as the complex load, but with all impedance values scaled up by a factor of 51 (for 0 dB gain). If a gain other than 0 dB is desired, the scaling factor is determined from Equation 12. This method applies **only** if the RRO network has been made complex comparable to the load according to the procedure in the previous section (Equations 5-9a), such that $R_{ac} = Z_{ac}$. Using a scaling factor of 51, and the previous examples, yields:



The preceeding procedure will yield a receive gain which is constant with respect to frequency. The RRX resistor, or network, must have a tolerance equal to or better than the required system tolerance for receive gain.

7) Transmit Gain (G_{TX})

Setting the transmit gain involves selecting RTX1 and RTX2 in Figure 28. The voltage gain from V_L to V_{TX} is calculated from the following:

$$G_{TX} = \frac{V_{TX}}{V_L} = \frac{RTX2 \bullet 31\ k \bullet 0.328}{RTX1 \bullet (RC + 31\ k)} \quad (15)$$

For 0 dB gain, set RTX2 = 3.15 x RTX1 (for RC = 1.0 k). The actual values of RTX2 and RTX1 are not critical — only their ratio so as to provide the proper gain at the op amp. Once the ratio is established, the two resistors can be selected from a set of standard resistor values. The minimum value for RTX1 is limited by the drive capability of TXO, which is a nominal ±800 µA peak (±275 µA minimum). As a general rule, RTX1 should be between 5.0 kΩ and 20 kΩ. The load on TXO is the parallel combination of RTX1 and RRO.

CTX is for DC blocking, and is typically a large value (1.0 µF) so as to not be a significant impedance. In general, it should **not** be used for low frequency rolloff as that will affect the transhybrid rejection (discussed in the next section). Low frequency rolloff should be done after the op amp. High frequency roll-off can be set by placing a capacitor across RTX2.

For complex loads (at Tip and Ring), if RRO and RRX have been made complex comparable to the load as described in the previous sections, neither RTX1 nor RTX2 needs to be complex since both the transmit and receive signals which appear at TXO will be flat with respect to frequency.

RTX1 and RTX2 must have a tolerance equal to or better than the required system tolerance for the transmit gain.

8) Balance Network (RB) — Transhybrid Rejection

When a receive signal is applied to V_{RX} to produce a signal at Tip and Ring, the two-to-four wire arrangement of a hybrid (the MC33121) results in a reflected signal at TXO. Transhybrid rejection involves canceling that reflected signal before it appears at V_{TX}. The method used is to insert the RB resistor (or network) as shown in Figure 36. The current I_B, supplied from V_{RX}, cancels the current I_{TX1} supplied from TXO (Node A is a virtual ground). Good transhybrid cancellation requires that the currents be equal in magnitude **and** 180° out of phase at Node A.

Using the equations for transmit and receive gains, the current I_{TX1} is equal to:

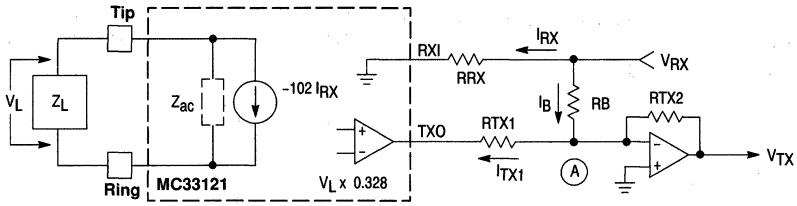
$$I_{TX1} = \frac{33.5 \bullet V_{RX} \bullet Z_{ac} \bullet Z_L \bullet 31\ k}{RRX \bullet [Z_{ac} + Z_L] \bullet RTX1 \bullet (RC + 31\ k)} \quad (16)$$

a) For the case where RRO and RRX are comparable in configuration to Z_L:

Since $I_B = V_{RX}/RB$, then RB can be determined from:

$$RB = \frac{RRX \bullet RTX1 \bullet (RC + 31\ k)}{33.5 \bullet [Z_{ac}//Z_L] \bullet 31\ k} \quad (17)$$

Figure 36. Balance Resistor



2

Equation 17 provides a value for an RB resistor which will provide the correct magnitude for I_B. The correct phase relationship is provided by the fact that the signal at TXO is out of phase with that at V_{RX}. The phase relationship will be 180° **only** if RRO and RRX are of a configuration identical to that of the load. This applies regardless of whether the load, Z_L, (and RRO and RRX) are purely resistive or of a complex nature. Equation 17 reduces to a non-complex resistance if RRX, Z_{ac}, and Z_L are all comparably complex.

For the case where $Z_{ac} = Z_L$, RRX = 51 • Z_{ac}, and RC = 1.0 k, Equation 17 reduces to:

$$RB = 3.15 \bullet RTX1 \qquad (18)$$

b) For the case where Z_{ac} and Z_L do not have the same frequency characteristics:

For the case where, for reasons of cost and/or simplicity, the load (R_L) is considered resistive (whereas in reality it is not a pure resistance) and therefore resistors, rather than networks, were selected for RRO and RRX, using a simple resistor for RB may not provide sufficient transhybrid rejection due to a phase angle difference between V_{RX} and TXO. The terminating impedance may therefore not necessarily be matched exactly to the line impedance, but the resulting circuit still provides sufficiently correct performance for receive gain, transmit gain, and return loss. The rejection can be improved in this case by replacing RB with the configuration shown in Figure 37. Even on a very short phone line there is a reactive component to the load due to the two compensation capacitors (C_C, Figure 4) at the transistor collectors. The two capacitors can be considered in series with each other, and across the load as shown in Figure 37.

To simplify the explanation, the current source and Z_{ac} of Figure 36 are replaced with the Thevenin voltage source and series Z_{ac}. Since Z_L and Z_{ac} are not matched, there will be a phase shift from V_{RX} to the signal across Tip and Ring. This phase shift is also present at TXO. The same phase shift is generated at node B in the RB network by making RB1 equal to Z_{ac}, and Z_L equal to the load. RB2 is then calculated from:

$$RB2 = \frac{RRX \bullet RTX1 \bullet (RC + 31\ k)}{33.5 \bullet Z_{ac} \bullet 31\ k} \qquad (19)$$

For example, for a system where the load is considered a 600 Ω resistor (RRO = 20.3 kΩ, RRX = 30.6 kΩ, RTX1 = 10 kΩ, and RC = 1.0 kΩ), RB1 would be a 600 Ω resistor, Z_L (in the RB network) would be a 600 Ω resistor in parallel with a 0.005 µF capacitor, and RB2 calculates to 15.715 kΩ.

The RB resistor, or network, must have a tolerance equal to or better than the required system tolerance for transhybrid rejection.

9) Logic Interface

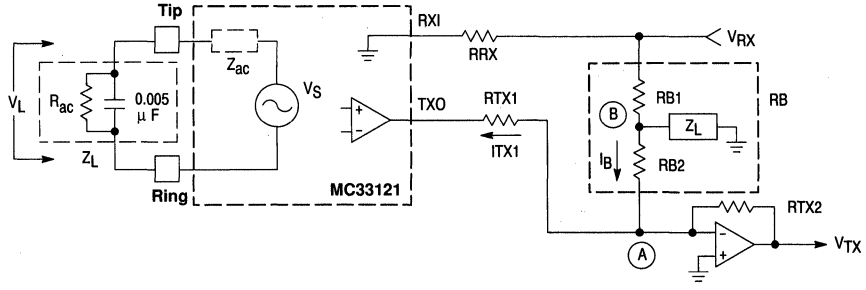
The logic circuit (output ST1, and the I/O labeled ST2/PDI) is depicted in Figure 30, and functions according to the Status Output Truth Table (Table 1).

a) Output Characteristics

ST1 is a traditional NPN pull-down with a 15 kΩ pull-up resistor. Figures 19 and 20 indicate its output characteristics.

ST2 is configured with the following items: a) a 1.0 mA current source for a pull-down which is active only when ST2 is internally set low; b) an 800 µA current source pull-up which is active only when ST2 is internally set high; c) a positive feedback aspect within this output circuit which

Figure 37. Balance Network



provides considerable hysteresis for stability reasons. Its output characteristics are shown in Figures 21 and 22. Due to this configuration, any external pull-up resistance which is applied to this pin must be greater than 15 kΩ, or the output may not reliably switch from high to low. Any external pull-down resistance does not affect this output's ability to switch from low-to-high, but does affect the maximum longitudinal currents which can be accepted by the circuit (see the section on Longitudinal Current Capability). The capacitor (C_T) is required to provide a time delay, for stability reasons, during transitions between off-hook and on-hook. This capacitor additionally affects maximum longitudinal currents, as well as stability during pulse dialing (explained below).

b) Hook Status

The MC33121 uses the sense currents at CP and CN to activate the hook status circuit. The sensing is configured such that the circuit monitors the impedance across Tip/Ring, which results in the hookswitch thresholds are minimally affected by the battery voltage. The off-hook to on-hook threshold is affected by the choice of RRF according to the graph of Figure 8, but is not affected by the value of RS. The on-hook to off-hook threshold is affected by the value of RS according to the graph of Figure 9, but is not affected by RRF. Varying the RC resistors does not affect the thresholds significantly.

When the telephone is on-hook (ST1 = High, ST2 = Low), the MC33121 is internally powered down, the external transistors are shut off, and power consumption is at a minimum. Upon closure of the phone's hookswitch, ST1 will switch low within 10 µs. ST2 will then change state slowly due to the external capacitor (C_T = 5.0 µF). There is a ≈8.0 ms delay for ST2 to reach the threshold necessary to activate the internal bias circuit, which in turn activates the external drive transistors to supply loop current. This delay is necessary to prevent instabilities during the transition to off-hook.

Upon opening the telephone's hookswitch, ST1 will switch high within ≈200 µs. ST2 then requires ≈60 ms to reach the threshold to switch off the internal bias circuit, which in turn shuts down the external drive transistors.

c) Pulse Dialing

During pulse dialing, ST1 will change state concurrent with the hookswitch. ST2 is kept from switching during pulse dialing by the external capacitor (C_T), which keeps the MC33121 in a powered up condition and stable. If the C_T capacitor is too small, the voltage at ST2 could drop to the PDI threshold (see section e below) during each pulse. This could cause the MC33121 to create additional noise on the line as it would cycle between a power-up and power-down condition with each dialing pulse.

d) Fault Detection

Faults are defined as excessive leakage from Tip to V_{EE} and/or ground, and from Ring to V_{EE} and/or ground. A single fault is any one of the above conditions, while a double fault is defined as excessive leakage from Tip to V_{EE} **and** from Ring to V_{CC}, as depicted in Figure 38. Refer to Figures 11-15 for the resistance, R_{LK}, which will cause the MC33121 to switch to a power-down condition. If the leakage resistance is less than that indicated in the graphs, the MC33121 will power-down itself and the two external transistors, thereby protecting them from overheating. Both status outputs (ST1 and ST2) will be at a logic low, indicating a fault condition. A fault condition is detected by monitoring an imbalance in the magnitudes of the currents at TSI and RSI, and/or a polarity reversal at Tip and Ring.

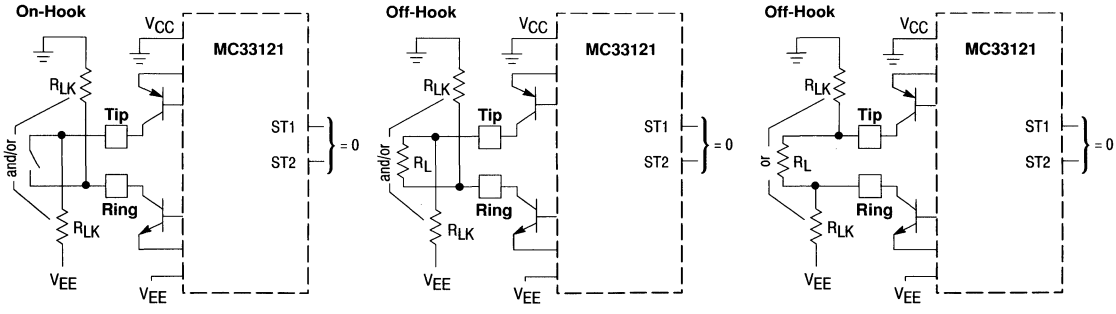
The MC33121 will detect the following conditions:

1) When on-hook (see Figure 11):
   a) <2.6 kΩ between Ring and V_{CC} (depending on R_S and V_{EE}), with no hysteresis at this threshold, or
   b) <3.7 kΩ between Tip and V_{EE} (depending on R_S and V_{EE}), with no hysteresis at this threshold, or
   c) Both a and b simultaneously.

Leakage from Tip to V_{CC} and/or Ring to V_{EE} are not detected as faults while the MC33121 is on-hook.

2) When off-hook (367 Ω between Tip and Ring):
   a) <400 Ω between Tip and V_{CC} (R_S = 6.2 kΩ), or
   b) <1800 Ω between Tip and V_{EE}, or
   c) <400 Ω between Ring and V_{EE} (R_S = 6.2 kΩ), or
   d) <1800 Ω between Ring and V_{CC}, or
   e) Both b and d simultaneously

Figure 38. Fault Detection



A simultaneous occurrence of conditions a) and c) is not detected as a fault. See Figures 12 to 15 for the threshold variation with R_L and V_{EE}. Resetting of the fault detection circuit requires that the leakage resistance be increased to a value between 10 kΩ and 20 kΩ, depending on V_{EE}, R_L, and R_S. Both ST1 and ST2 should be monitored for hookswitch status to preclude not detecting a fault condition.

Figure 15 indicates the variation in fault thresholds for Tip-to-V_{CC} and Ring-to-Battery faults, and is valid only for loop resistances of 200 Ω to 800 Ω. On loops larger than 800 Ω, the MC33121 does not reliably indicate the fault condition at ST1 and ST2, but may indicate on-hook status instead. This does not apply to Tip-to-Battery and Ring-to-V_{CC} faults which are correctly detected for lines beyond 800 Ω.

2

e) PDI Input

The ST2 output can also be used as an input (PDI Input) to power down the circuit, denying loop current to the subscriber (by shutting off the external pass transistors), regardless of the hookswitch position. Powering down is accomplished by pulling PDI to a logic low with an open collector output, or an NPN transistor as shown in Figure 30. The switching threshold is ≈1.5 V. The current out of PDI, when pulled low, is ≈800 μA. Releasing PDI allows the MC33121 to resume normal operation.

If the external telephone is off-hook while the MC33121 is powered down, sense currents at CP and TSI will result in some loop current flowing through the loop and back into CN and RSI. This current is generally on the order of 1.0 to 3.0 mA, determined primarily by the R_S resistors, loop resistance, and V_{EE}. ST1 will continue to indicate the telephone's actual hook status while PDI is held low. The on-to-off hook threshold is the same as that during normal operation, but the off-to-on hook threshold is >250 kΩ.

When powered down with the PDI pin, the receive gain (V_{RXI} to Tip/Ring) is muted by >90 dB, and the transmit gain (Tip/Ring to TXO) is muted by >30 dB.

Power Dissipation, Calculation and Considerations

a) Reliability

The maximum power dissipated by the MC33121 must be considered, and managed, so as to not exceed the junction temperature listed in the Maximum Ratings Table. Exceeding this temperature on a recurring basis will reduce long term reliability, and possibly degrade performance. The junction temperature also affects the statistical lifetime of the device, due to long term thermal effects within the package. Today's plastic integrated circuit packages are as reliable as ceramic packages under most environmental conditions. However, when the ultimate in system reliability is required, thermal managements must be considered as a prime system design goal.

Modern plastic package assembly technology utilizes gold wire bonded to aluminum bonding pads throughout the electronics industry. When exposed to high temperatures for protracted periods of time an intermetallic compound can form in the bond area resulting in high impedance contacts and degradation of device performance. Since the formation of intermetallic compounds is directly related to device junction temperature, it is incumbent on the designer to determine that the device junction temperature is consistent with system reliability goals.

Based on the results of almost ten years of +125°C operating life testing, Table 2 has been derived indicating the relationship between junction temperature and time to 0.1% wire bond failure.

Table 2. Statistical Lifetime

Junction Temperature (°C)	Time (Hours)	TIme (Years)
80	1,032,200	117.8
90	419,300	47.9
100	178,700	20.4
110	79,600	9.4
120	37,000	4.2
130	17,800	2.0
140	8,900	1.0

Motorola MECL Device Data, DL122

The "Time" in Table 2 refers to the time the device is operating at that junction temperature. Since the MC33121 is at a low power condition (nominally 40 mW) when on-hook, the duty cycle must be considered. For example, if a statistical duty cycle of 20% off-hook time is used, operation at 130°C junction temperature (when off-hook) would result in a statistical lifetime of ≈10 years.

b) Power and Junction Temperature Calculation

The power within the IC is calculated by subtracting the power dissipated in the two-wire side (the transistors and the load) from the power delivered to the IC by the power supplies. Refer to Figure 4 and 27.

$$P_D = |V_{DD} \bullet I_{DD}| + |V_{EE} \bullet I_{EE}| - (I_L \bullet |V_{EP} - V_{EN}|) \quad (20)$$

The terms V_{EP} and V_{EN} are the DC voltages, with respect to ground, at the EP and EN pins. These voltages can be measured, or can be approximated by:

$$V_{EP} \approx -(30\ \Omega \bullet I_L)$$
$$V_{EN} \approx |V_{EE}| + 2.1\ V + (I_L \bullet 35\ \Omega)$$

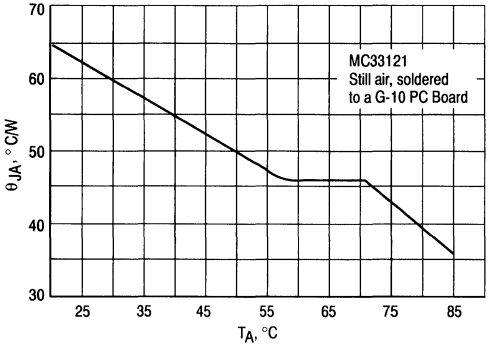
Refer to Figure 23. The junction temperature is then calculated from:

$$T_J = T_A + (P_D \bullet \theta_{JA}) \quad (21)$$

where T_A is the ambient air temperature at the IC package, and θ_{JA} is the junction-to-ambient thermal resistance shown in Figure 39. The highest junction temperature will occur at maximum V_{EE} and V_{DD}, maximum loop current, and maximum ambient temperature.

If the above calculations indicate the junction temperature will exceed the maximum specified, then it is necessary to reduce the maximum loop current, ambient temperature, and/or V_{EE} supply voltage. Air flow should not be restricted near the IC by tall components or other objects since even a small amount of air flow can substantially reduce junction temperature. For example, typically an air flow of 300 LFPM (3.5 mph) can reduce the effective θ_{JA} by 14 to 20% from that which occurs in still air. Additionally, providing as much copper area as possible at the IC pins will assist in drawing away heat from within the IC package. For additional information on this subject, refer to the "Thermal Considerations" section of *Motorola MECL System Design Handbook*, and the "System Design Considerations" section of *Motorola MECL Device Data*.

Figure 39. Thermal Resistance (Junction-to-Ambient)



Selecting the Transistors

The specifications for the two loop current pass transistors involve their current gain, voltage rating, and power dissipation capabilities at the highest ambient temperatures. Power dissipation during both normal operation and faults must be considered when determining worst case situations. Generally, more power is dissipated during a fault condition than during normal operation.

The transistors' minimum beta is recommended to be 40 at the loop currents involved in the application. A lower beta could degrade gain and balance performance. Maximum beta should be less than 500 to prevent possible oscillations. Darlington type transistors should not be used. The voltage rating should be consistent with the maximum V_{EE}, expected transients, and the protection scheme used.

Referring to Figure 27, during normal operation the loop current and the voltage across the transistors are both at a maximum when the load impedance (R_L) is at a minimum. The loop current is determined by RRF and the graphs of Figures 5-7. The voltage across each transistor is determined from the following:

$$V_T = \frac{|V_{EE}| - 2.1 - [(65 + 2RP + R_L) \bullet I_L]}{2} \qquad (22)$$

The power in each transistor is then ($V_T \bullet I_L$). The voltage across the two transistors will always be nearly equal during normal operation, resulting in equal power dissipation. The graph of Figure 24 indicates the power dissipated in each transistor where RP = 100 Ω.

During a fault condition, depicted in Figure 38, if the leakage resistance from Tip to V_{EE} or from Ring to V_{CC} is less than that shown in Figures 12-14 (when off-hook), the MC33121 will power down the transistors to protect them from overheating. Should the leakage resistance be slightly higher than that shown in the graphs, however, and the fault detection has not been activated, the power in one transistor (in a single fault, both transistors in a double fault) will be higher than normal. The power will depend on V_{EE}, R_L, RP and the leakage resistance. Table 3 is a guide of the power in the transistor dissipating the higher power level.
The power (in watts) in the two right columns indicates the power dissipated by that transistor if it is carrying the maximum fault current. The system designer should attempt to predict possible fault conditions for the system, and then measure the conditions on the transistors during the worse case fault(s).

Table 3. Transistor Power During a Fault

V_{EE}	RL	P_{PNP}	P_{NPN}
–42	150	0.835	0.615
–24	150	0.257	0.176
–42	600	0.601	0.185
–24	600	0.109	0.057

For most applications involving a maximum loop current of 30-40 mA, and a maximum T_A of +85°C, and where faults may occur, the MJD243 and MJD253 DPAK transistors are recommended. When mounted as described in their data sheet, they will handle both the normal loop current as well as most fault conditions. If faults are not expected to occur in a particular application, then smaller package transistors, such as MPS6717 and MPS6729, may be used. Each application must be evaluated individually when selecting the transistors.

Other possible transistors which can be considered:

PNP	NPN
MJD253-1	MJD243-1
MJE253	MJE243
MJD32	MJD31
MJD42	MJD41
MJD350	MJD340
TIP30A,B,C	TIP29A,B,C

Longitudinal Current Capability

The maximum longitudinal current which can be handled without distortion is a function of loop current, battery feed resistance, the longitudinal impedance, and the components on ST2.

Since the pass transistors cannot pass current in the reverse direction, the DC loop current provides one upper boundary for the peak longitudinal current plus peak speech signal current. The battery feed resistance determines, in effect, the DC voltage across the transistors, which is a measure of the headroom available for the circuit to handle the peak longitudinal voltage plus peak speech signal voltage. The longitudinal impedance, determined by the R_S resistors (equation 4), determines the longitudinal current for a given longitudinal voltage.

While analysis of the above items may yield one value of maximum longitudinal current, a different limit (which may be higher or lower) is imposed by the capacitor C_T, and any pulldown resistance R_T, on Pin 12 (ST2). This is due to the fact that the sense currents at TSI and RSI will be alternately mismatched as Tip and Ring move up and down together in the presence of longitudinal signals. When the longitudinals are strong, the internal fault detect circuit is activated with each 1/2 cycle, which attempts to switch ST2 low (see the section on Fault Detection). The speed at which ST2 can switch low is a function of both the external capacitor, C_T and any pulldown resistance, R_T.

The graphs of Figures 25 and 26 indicate the maximum longitudinal current which can be handled (in Tip and in Ring) without distortion or causing ST2 to switch low.

PC Board Layout Considerations

PC board considerations include thermal, RFI/EMI, transient conditions, interconnection of the four wire side to the codec/filter, and others. Wirewrapped boards should be

avoided — breadboarding should be done on a (at least) reasonably neat PC board.

a) Thermal

Power dissipated by the MC33121 and the two transistors must be removed to prevent excessively high junction temperatures. The equations for calculating junction temperatures are mentioned elsewhere in this data sheet. Heat is removed by both air flow and copper foil on the PC board. Since even a small amount of air flow substantially reduces junction temperatures compared to still air, tall components or other objects should not be placed such that they block air flow across the heat generating devices. Increasing, wherever possible, the area of the copper foil at the IC pins will provide additional heat removal capability. A ground plane can generally help here, while at the same time helping to reduces RFI problems.

b) RFI/EMI

While the MC33121 is intended for use at audio frequencies, the internal amplifiers have bandwidths in excess of 1.0 MHz, and can therefore respond to externally induced RFI and EMI. Interference signals can come in on the phone line, or be radiated on to the PC board from nearby radio stations or from high frequency circuitry (digital & microprocessor circuitry) in the vicinity of the line card.

Usually RFI entering from the phone line at Tip and Ring can be removed by the compensation capacitors (C_C) provided they are connected to a good quality RF ground (generally the same ground which connects to V_{CC} on the MC33121). The ground track should be as wide and as direct as possible to minimize lead inductance. Generally better results can be obtained if an RF bleedoff to earth (or chassis) ground can be provided where the twisted pair phone line comes into the system.

To minimize problems due to noise radiating directly onto the PC board from nearby high frequency circuitry, all components associated with the MC33121 should be physically as close as possible to the IC. The most sensitive pins in this respect are the CP, CN, RSI, TSI, VAG and RXI pins. Keeping the tracks short minimizes their "antenna" effect.

c) Transient Conditions

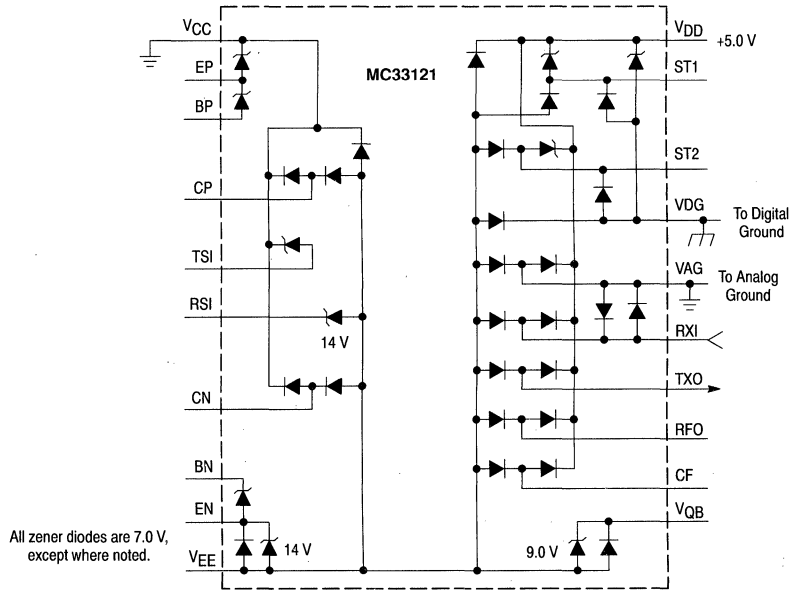
When transient voltages come in to Tip and Ring, the transient currents, which can be several amperes, must be carried by the ground line (V_{CC}) and/or the V_{EE} line. These tracks, along with the protection and clamping devices, must be designed for these currents at the frequencies involved. If the tracks are narrow, not only may they be destroyed by the high currents, but their inductance can allow the voltage at the IC, and other nearby components, to rise to damaging levels.

The protection circuits shown in Figure 4, and in other figures in this data sheet, are such that the bulk of the transient energy is dissipated by external components (the protection resistors and the clamp diodes). The MC33121 has internal diodes to limit voltage excursions on the pins, and to pass a small amount of the transient current — typically less than 1.0 A peak. The arrangement of the diodes is shown in Figure 40.

d) Interconnection of the four-wire side

The connections on the four-wire side to the codec and other digital circuitry involves keeping digital noise out of the speech paths, and also ensuring that potentially destructive transients on Tip and Ring do not get through to the +5.0 V system.

Figure 40. Protection Diodes



Basically, digital connections to ST1 and ST2 should be referenced to the V_{DD} and V_{DG} pins, while the transmit and receive analog signals should be referenced to the analog ground (V_{AG}). V_{CC} should be connected to a clean battery ground, and generally should not be connected directly to V_{DG} and/or V_{AG} (on the line card) when strong transients are anticipated. Even with a good layout, V_{CC} can move several volts when a transient hits, possibly damaging components on the +5.0 V line if their grounds have a direct connection at the line card. The MC33121 is designed to allow V_{CC} to move as much as ±30 V with respect to V_{DG} and V_{AG} on a transient basis only. V_{CC} and the other grounds should preferably be connected together at the power supply rather than at the IC. Internally, the MC33121 has clamp diodes on the 4-wire side pins as indicated in Figure 40.

If the codec has a single ground pin, as in Figure 41, it will be the reference for both the digital and analog signals, and must be connected to both V_{AG} and V_{DG} on the MC33121. If the codec has separate digital and analog grounds, as in Figure 42 (the MC145503 internally generates the analog ground), then each ground should be connected to the appropriate ground on the MC33121.

e) Other

A 0.1 µF capacitor should be provided across V_{CC} to V_{EE} on the MC33121 to help keep idle channel noise to a minimum.

The C_{QB} capacitor (on the V_{QB} pin) forms a pole with an internal 7.5 kΩ resistor to filter noise from the V_{EE} pin, providing an internal quiet battery supply for the speech amplifiers. Power supply rejection will depend on the value and quality of this capacitor at the frequencies of concern. Tantalum capacitors generally have better high frequency characteristics then electrolytics. See Figure 17 and 18 for ripple rejection characteristics (the four-wire data was measured at pin 11 (TXO)). Figure 16 indicates ripple rejection from the +5.0 V supply (V_{DD}).

In general, pc board tracks carrying analog signals (on the four-wire side and Tip/Ring) should not be routed through the digital section where they could pick up digital noise. Any tracks longer than a few inches should be considered an

Figure 41. Connection to a CODEC With a Single Ground

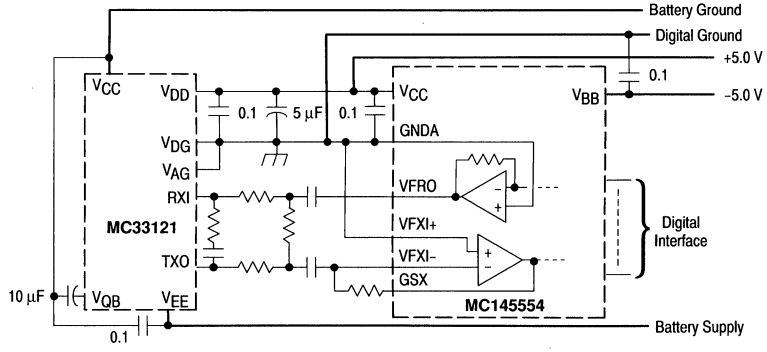
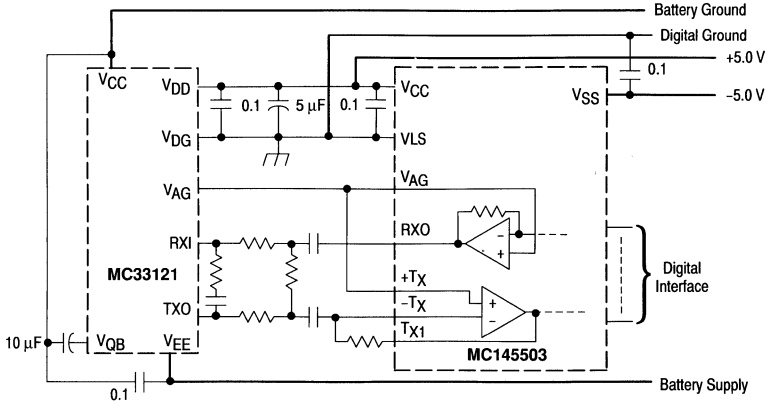


Figure 42. Connection to a CODEC With Separate Grounds



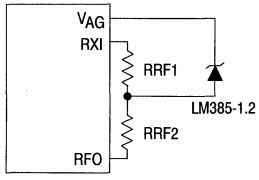
antenna and should be checked for potential noise or RFI pickup which could affect the circuit operation.

Alternate Circuit Configurations

a) Loop Current Limit

Replacing the RRF resistor with the circuit in Figure 43 will change the DC loop current characteristics in two ways from the graphs of Figures 5-7; a) the maximum loop current on a short line can be reduced while increasing the current on a long line, and b) the temperature dependence of the maximum current is reduced to the TC of the external reference diode.

Figure 43. Alternate Current Limit Circuit



The LM385-1.2 is a precision temperature stable zener diode. As the load impedance at Tip and Ring is reduced, the voltage at RFO goes increasingly negative. When the zener diode is turned on, the current into RXI is then clamped at a value determined by RRF1 and the zener diode. To calculate the two resistors, use the following procedure:

RRF1 must be >0.7 • (RRF1 + RRF2);

Determine RRF1 to set the current limit on a short line by using the following equation:

$$RRF1 = \frac{102 \bullet 1.23\ V}{I_{L(max)} - 3.0\ mA} \qquad (23)$$

Then using Equation 1 calculate RRF for the long line current. RRF2 is then determined by;

$$RRF2 = RRF - RRF1 \qquad (24)$$

Figure 44 illustrates one example using the above circuit. Comparing this graph to the 5100 Ω curve of Figure 7 shows a substantial decrease in the current limit (at R_L = 0), resulting in reduced power consumption and dissipation. Use of this circuit does not affect the hookswitch or fault thresholds.

b) Protection Scheme

The protection circuit shown in Figure 45 has the advantage of drawing ≈90% of the transient current from ground (V_{CC}) on a negative transient, rather than from the V_{EE} line as the circuit of Figure 4 does. The majority of the transient current flows through the RP resistors and the Mosorbs while a small amount (≈10%) flows through the sense resistors and the CP, CN, RSI pins. On a positive transient, all the current is directed to ground. The diode in the NPN's collector prevents reverse current through the base-collector junction of the transistor during a negative transient.

Figure 44. Loop Current versus Loop Resistance Alternate Loop Current Limit Configuration

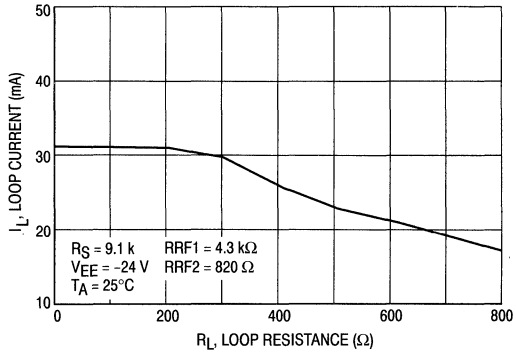
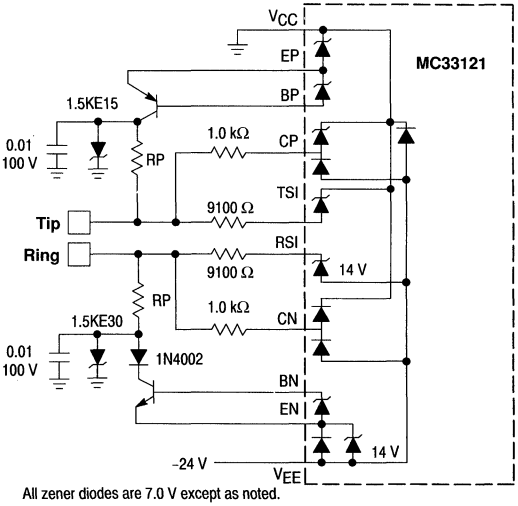


Figure 45. Alternate Protection Scheme



All zener diodes are 7.0 V except as noted.

CIRCUIT PERFORMANCE

The following three circuits are presented as typical application examples, and the accompanying graphs indicate their measured performance. The first circuit (Figure 46) has a 600 Ω pure resistance as the AC load. The second circuit (Figures 47) has as an AC load a 900 Ω resistor in series with a 2.16 μF capacitor. The third circuit (Figure 48) has as an AC load, a complex network composed of an 820 Ω resistor in parallel with 0.115 μF, and those in series with a 220 Ω resistor. In the graphs of Figures 49-51, R_L = Return Loss, THR = Transhybrid Rejection, GTX = Transmit Gain, GRX = Receive Gain.

Figure 46. 600 Ω System

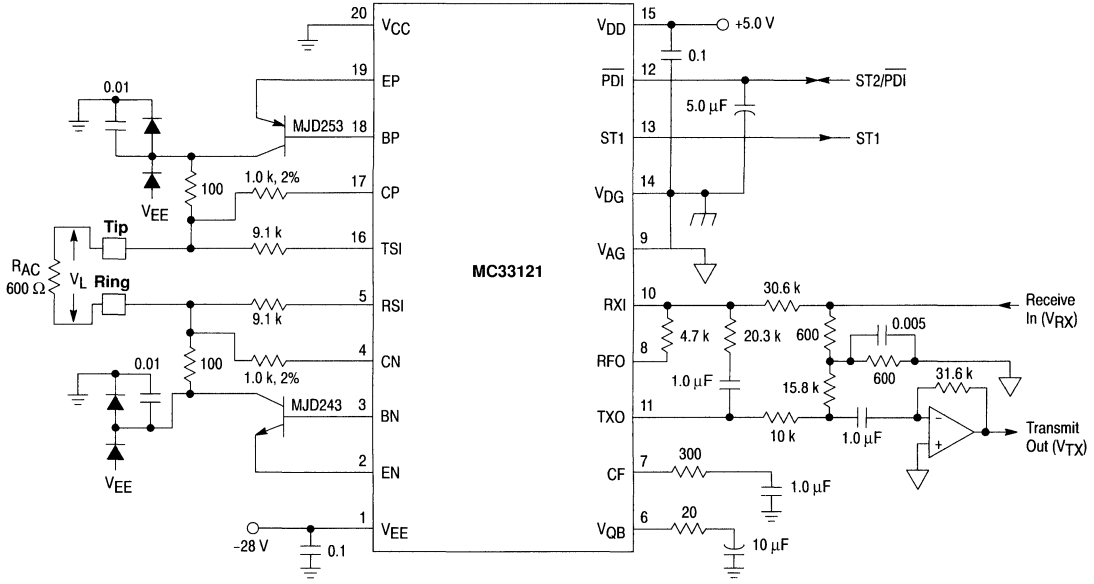


Figure 47. 900 Ω and 2.16 μF System

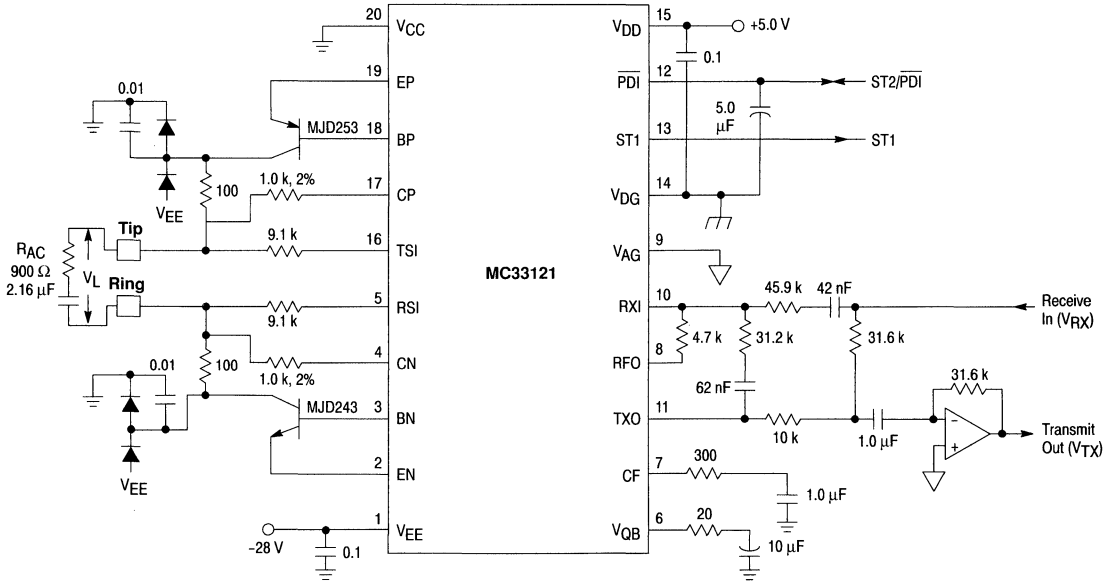


Figure 48. 220 Ω and 820 Ω//0.115 μF System

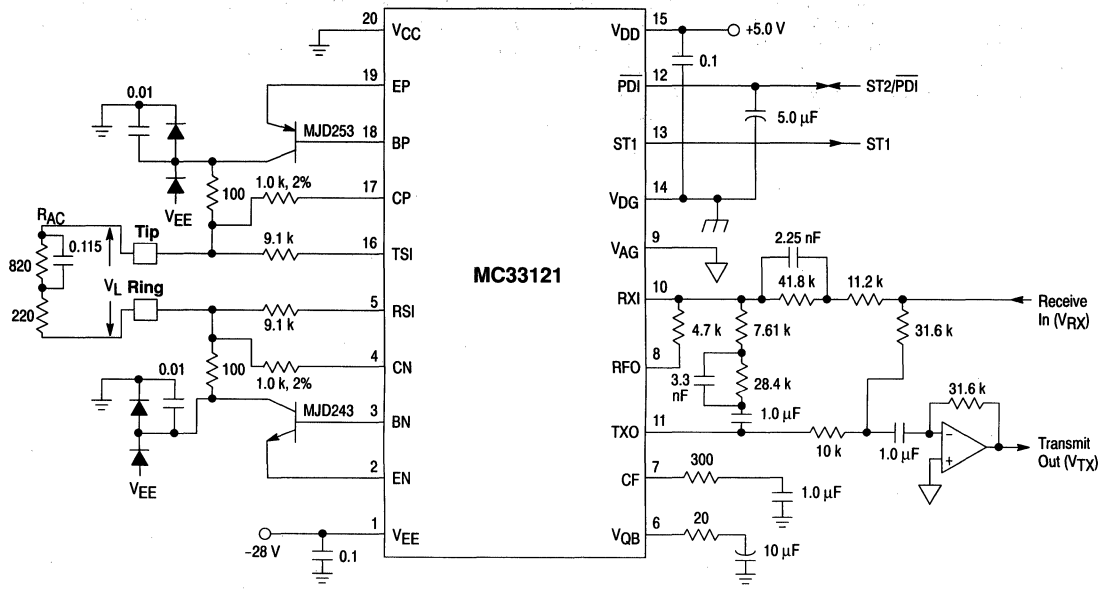


Figure 49. Circuit Performance, 600 Ω System

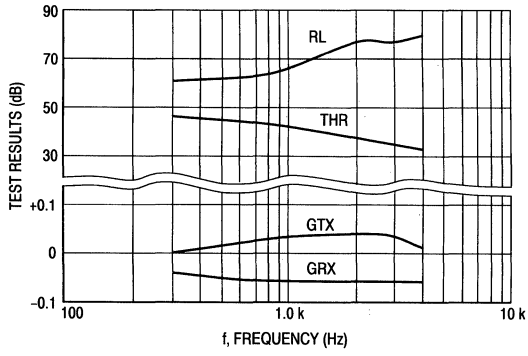


Figure 50. Circuit Performance 900 Ω and 2.16 μF System

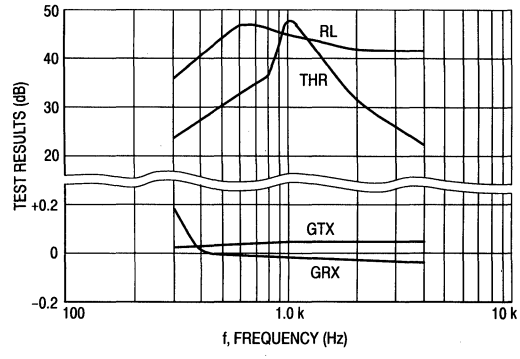


Figure 51. Circuit Performance 820 Ω//0.115 μF and 220 Ω System

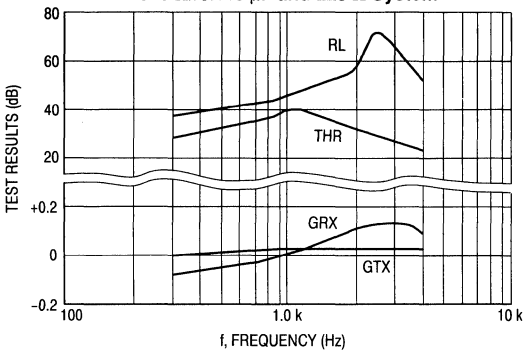
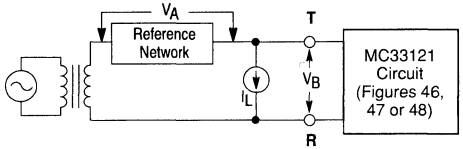


Figure 52. Return Loss Test Circuit for Figures 46 to 51



Reference Network = R_{AC} of Figures 46 to 48.

Return Loss = $20 \log \left| \frac{V_A + V_B}{V_A - V_B} \right|$

2

GLOSSARY

ATTENUATION — A decrease in magnitude of a communication signal, usually expressed in dB.

BALANCE NETWORK — That part of the SLIC circuit which provides transhybrid rejection.

BANDWIDTH — The range of information carrying frequencies of a communication system.

BATTERY — The voltage which provides the loop current, and in some cases powers the SLIC circuit. The name derives from the fact that COs have always used batteries, in conjunction with AC power, to provide this voltage.

BATTERY FEED RESISTANCE — The equivalent Thevenin DC resistance of the SLIC circuit for supplying loop current. Traditionally it is 400 Ω.

C-MESSAGE FILTER — A frequency weighting which evaluates the effects of noise on a typical subscriber's system.

CENTRAL OFFICE — Abbreviated CO, it is a main telephone office, usually within a few miles of its subscribers, that houses switching gear for interconnection within its exchange area, and to the rest of the telephone system. A typical CO can handle up to 10,000 subscriber numbers.

CODEC — Coder/Decoder — Interfacing between the SLIC and the digital switch, it converts the SLIC's transmit signal to digital, and converts the digital receive signal to analog.

dB — A power or voltage measurement unit, referred to another power or voltage. It is generally computed as:
10 • log (P_1 / P_2) for power measurements, and
20 • log (V_1 / V_2) for voltage measurements.

dBm — An indication of signal power. 1.0 mW across 600 Ω, or 0.775 Vrms, is defined as 0 dBm. Any other voltage level is converted to dBm by:
dBm = 20 • log (Vrms/0.775), or
dBm = [20 • log (Vrms)] + 2.22.

dBmp — Indicates dBm measurement using a psophometric weighting filter.

dBrn — Indicates a dBm measurement relative to 1.0 pW power level into 600 Ω. Generally used for noise measurements, 0 dBrn = –90 dBm.

dBrnC — Indicates a dBrn measurement using a C-message weighting filter.

DTMF — Dual Tone Multifrequency. It is the "tone dialing" system based on outputting two non-harmonic related frequencies simultaneously to identify the number dialed. Eight frequencies have been assigned to the four rows and four columns of a keypad.

FAULT — An incorrect condition where Tip is accidentally connected to the battery voltage, or Ring is connected to ground, or both. The most common fault is Ring to ground.

FOUR WIRE CIRCUIT — The portion of a telephone, or central office, which operates on two pairs of wires. One pair is for the transmit path, and one pair is for the receive path.

FULL DUPLEX — A transmission system which permits communication in both directions simultaneously. The standard handset telephone system is full duplex.

GAIN — The change in signal amplitude (increase or decrease) after passing through an amplifier, or other circuit stage. Usually expressed in dB, an increase is a positive number, and a decrease is a negative number.

HALF DUPLEX — A transmission system which permits communication in one direction at a time. CB radios, with "push-to-talk" switches, and voice activated speakerphones, are half duplex.

HOOKSWITCH — A switch, within the telephone, which connects the telephone circuit to the subscriber loop. The name derives from old telephones where the switch was activated by lifting the receiver off and onto a hook on the side of the phone.

HYBRID — Another name for a two-to-four wire converter.

IDLE CHANNEL NOISE — Residual background noise when transmit and receive signals are absent.

LINE CARD — The PC board and circuitry in the CO or PBX which connects to the subscriber's phone line. A line card may hold circuitry for one subscriber, or a number of subscribers.

LONGITUDINAL BALANCE — The ability of the SLIC to reject longitudinal signals on Tip and Ring.

LONGITUDINAL SIGNALS — Common mode signals.

LOOP — The loop formed by the two subscriber wires (Tip and Ring) connected to the telephone at one end, and the central office (or PBX) at the other end. Generally, it is a floating system not referred to ground, or AC power.

LOOP CURRENT — The DC current which flows through the subscriber loop. It is typically provided by the central office or PBX, and ranges from 20 to 120 mA.

OFF-HOOK — The condition when the telephone is connected to the phone system, permitting the loop current to flow. The central office detects the DC current as an indication that the phone is busy.

ON-HOOK — The condition when the telephone is disconnected from the phone system, and no DC loop current flows. The central office regards an on-hook phone as available for ringing.

PABX — Private Automatic Branch Exchange. In effect, a miniature central office, it is a customer owned switching system servicing the phones within a facility, such as an office building. A portion of the PABX connects to the Bell (or other local) telephone system.

PROTECTION, PRIMARY — Usually consisting of carbon blocks or gas discharge tubes, it absorbs the bulk of a lightning induced transient by clamping the voltages to less than ±1500 V.

PROTECTION, SECONDARY — Usually located on the line card, it protects the SLIC and associated circuits from transient surges. Typically, it must be capable of clamping a ±1.5 kV surge of 1.0 ms duration.

PULSE DIALING — A dialing system whereby the loop current is interrupted a number of times in quick succession. The number of interruptions corresponds to the number dialed, and the interruption rate is typically 10 per second. The old rotary phones, and many new pushbutton phones, use pulse dialing.

RECEIVE PATH — Within the CO or PBX it is the speech path from the internal switching system towards the phone line (Tip & Ring).

REN — Ringer Equivalence Number. An indication of the impedance or loading factor of a telephone bell or ringer circuit. An REN of 1.0 equals ≈8.0 kΩ. The Bell system typically permits a maximum of 5.0 REN (1.6 kΩ) on an individual subscriber line. A minimum REN of 0.2 (40 kΩ) is required by the Bell system.

RETURN LOSS — Expressed in dB, it is a measure of how well the SLIC's AC impedance matches the line's AC characteristic impedance. With a perfect match, there is no reflected signal, and therefore infinite return loss. It is calculated from:

$$RL = 20 \bullet \log \frac{(Z_{Line} + Z_{CKT})}{(Z_{Line} - Z_{CKT})}$$

RING — One of the two wires connecting the central office to a telephone. The name derives from the ring portion of the plugs used by operators (in older equipment) to make the connection. Ring is traditionally negative with respect to Tip.

SLIC — Subscriber Line Interface Circuit. It is the circuitry within the CO or PBX which connects to the user's phone line.

SUBSCRIBER — The customer at the telephone end of the line.

SUBSCRIBER LINE — The system consisting of the user's telephone, the interconnecting wires, and the central office equipment dedicated to that subscriber (also referred to as a loop).

TIP — One of the two wires connecting the central office to a telephone. The name derives from the tip of the plugs used by operators (in older equipment) to make the connection. Tip is traditionally positive with respect to Ring.

TRANSHYBRID REJECTION — The rejection (in dB) of the reflected signal in the transmit path resulting from a receive signal applied to the SLIC.

TRANSMIT PATH — Within the CO or PBX it is the speech path from the phone line (Tip & Ring) towards the internal switching system.

TWO WIRE CIRCUIT — Refers to the two wires connecting the central office to the subscriber's telephone. Commonly referred to as Tip and Ring, the two wires carry both transmit and receive signals in a differential manner.

TWO-TO-FOUR WIRE CONVERTER — A circuit which has four wires (on one side) — two (signal & ground) for the outgoing signal, and two for the incoming signal. The outgoing signal is sent out differentially on the two wire side (the other side), and incoming differential signals received on the two wire side are directed to the four wire side. Additional circuit within cancels the reflected outgoing signal to keep it separate from the incoming signal.

VOICEBAND — That portion of the audio frequency range used for transmission across the telephone system. Typically, it is 300 to 3400 Hz.

MOTOROLA

Advance Information

Voice Switched Speakerphone with Microprocessor Interface

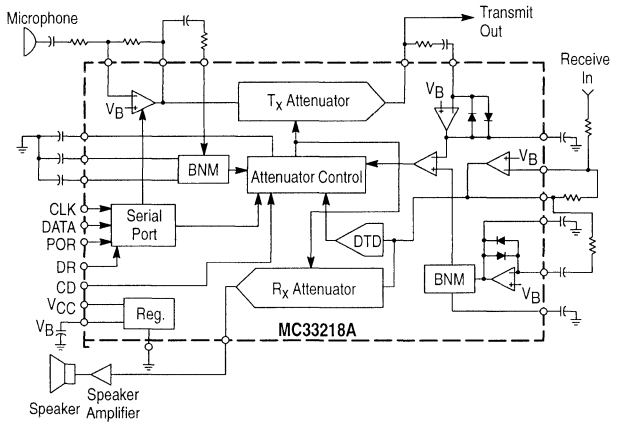
The Motorola MC33218A Voice Switched Speakerphone Circuit incorporates the necessary amplifiers, attenuators, level detectors, and control algorithm to form the heart of a high quality hands–free speakerphone system. Included are a microphone amplifier with mute, transmit and receive attenuators, a background monitoring system for both the transmit and receive paths, and level detectors for each path. An AGC system reduces the receive gain on long lines where loop current and power are in short supply. A dial tone detector prevents fading of dial tone. A Chip Disable pin permits conserving power when the circuit is not in use.

Additionally, the MC33218A has a serial data port which permits microprocessor control of the receive volume level, microphone mute, attenuator range, and selection of transmit, receive, idle or normal modes. The data port can be operated at up to 1.0 MHz.

The MC33218A can be operated from a power supply, or from the telephone line, requiring typically 4.6 mA. It can be used in conjunction with a variety of speech networks. Applications include not only speakerphones, but intercoms and other voice switched devices.

- Supply Voltage Range: 2.7 to 6.5 V
- Attenuator Range: 53 or 27 dB (Selectable)
- 2 Point Sensing with Background Noise Monitor in Each Path
- Microprocessor Port for Control of:
  - Volume Control (40 dB Range over 16 Levels)
  - Mute Microphone Amplifier
  - Force to Receive, Transmit, or Idle Modes
  - Attenuator Range Selection (27 or 53 dB)
- Chip Disable Pin Powers Down the Entire IC
- 24 Pin Narrow Body (300 mil) DIP and 24 Pin SOIC

Simplified Block Diagram



This device contains 610 active transistors.

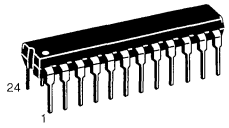
This document contains information on a new product. Specifications and information herein are subject to change without notice.

MC33218A

VOICE SWITCHED SPEAKERPHONE WITH µPROCESSOR INTERFACE

SEMICONDUCTOR TECHNICAL DATA

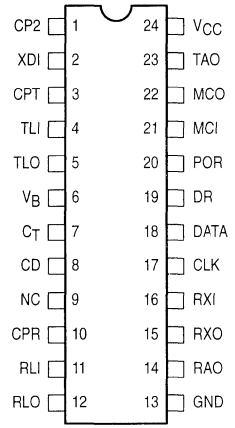
2



P SUFFIX
PLASTIC PACKAGE
CASE 724

DW SUFFIX
PLASTIC PACKAGE
CASE 751E

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC33218ADW	$T_A = -40°$ to $+85°C$	SO–24L
MC33218AP		Plastic DIP

MAXIMUM RATINGS

Rating	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	–0.5	7.0	Vdc
Any Input	V_{in}	–0.4	V_{CC} + 0.4	Vdc
Maximum Junction Temperature	T_J	–	+150	°C
Storage Temperature Range	T_{stg}	–65	+150	°C

NOTE: Devices should not be operated at or outside these values. The "Recommended Operating Limits" provide for actual device operation.

2

RECOMMENDED OPERATING LIMITS

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Voltage (Non–AGC Range) (AGC Range)	V_{CC}	3.5 2.7	– –	6.5 3.5	Vdc
Maximum Attenuator Input Signal	$V_{in(max)}$	–	–	300	mVrms
Logic Input Voltage (Pins 8, 17–19) Low High	V_{INL}	 0 2.0	 – –	 0.8 V_{CC}	Vdc
Clock and Data Rate (Serial Port)	F_{DATA}	0	–	1.0	MHz
V_B Output Current	I_{VB}	–	See Figure 14	–	mA
Operating Ambient Temperature Range	T_A	–40	–	+85	°C

ELECTRICAL CHARACTERISTICS (T_A = +25°C, V_{CC} = 5.0 V, CD ≤ 0.8 V, unless noted, see Figure 3.)

Characteristic	Symbol	Min	Typ	Max	Unit
POWER SUPPLY					
Supply Current (Enabled, CD ≤ 0.8, V_B Open, See Figure 13) Idle Mode T_X Mode R_X Mode	I_{CCE}	 3.0 – –	 4.6 4.6 5.3	 6.0 – –	mA
Supply Current (Disabled, CD = 2.0 V, V_B Open) V_{CC} = 3.0 V V_{CC} = 5.0 V V_{CC} = 6.5 V	I_{CCD}	 – 50 –	 67 110 150	 – 170 –	µA
V_B Output Voltage (I_{VB} = 0, CD = 0) V_{CC} = 2.7 V V_{CC} = 5.0 V V_{CC} = 6.5 V	V_B	 – 2.1 –	 0.9 2.2 3.0	 – 2.3 –	Vdc
V_B Output Resistance (I_{VB} ≤ –1.0 mA)	R_{OVB}	–	600	–	Ω
PSRR @ V_B versus V_{CC}, f = 1.0 KHz, C_{VB} = 100 µF	PSRR	–	57	–	dB
ATTENUATOR CONTROL					
C_T Voltage (with Respect to V_B) (Full Range, B5 = 0) R_X Mode (Maximum Volume) Idle Mode T_X Mode (Half Range, B5 = 1) R_X Mode (Maximum Volume Idle Mode T_X Mode	$V_{CT} - V_B$	 – – – – – –	 +150 0 –100 +85 0 –35	 – – – – – –	mV
C_T Source Current (Switching to R_X Mode)	I_{CTR}	–55	–42	–33	µA
C_T Sink Current (Switching to T_X Mode)	I_{CTT}	33	42	55	µA
C_T Idle Current	I_{CTI}	–3.0	0	3.0	µA
Dial Tone Detector Threshold (with Respect to V_B at RXO)	V_{DT}	–40	–20	–8.0	mV

ELECTRICAL CHARACTERISTICS (continued) (T_A = +25°C, V_{CC} = 5.0 V, CD ≤ 0.8 V, unless noted, see Figure 3.)

Characteristic	Symbol	Min	Typ	Max	Unit
ATTENUATORS					
Receive Attenuator Gain (f = 1.0 kHz, Maximum Volume)					dB
Full Attenuation Range (B5 = 0)					
R_X Mode	G_{RXF}	3.0	6.7	9.0	
T_X Mode	G_{RXTF}	−49	−47	−43	
Idle Mode	G_{RXIF}	−28	−25	−22	
Range (R_X to T_X Mode)	ΔG_{RXF}	50	53	56	
Half Attenuation Range (B5 = 1)					
R_X Mode	G_{RXH}	−10	−7.0	−4.0	
T_X Mode	G_{RXTH}	−37	−34	−31	
Idle Mode	G_{RXIH}	−28	−25	−22	
Range (R_X to T_X Mode)	ΔG_{RXH}	23	27	29	
Volume Control Range (R_X Mode Only, B3–B0 Changed from 0000 to 1111, See Figures 6, 7)	V_{CR}				dB
Full Range		34	40	46	
Half Range		–	25	–	
AGC Attenuation Range (V_{CC} = 3.5 to 2.7 V, Receive Mode Only, B3–B0 = 0000, See Figure 8)	G_{AGC}				dB
Full Range		12	21	28	
Half Range		–	19	–	
Transmit Attenuator Gain (f = 1.0 kHz, Maximum Volume)					dB
Full Attenuation Range (B5 = 0)					
T_X Mode	G_{TXF}	3.0	6.7	9.0	
R_X Mode	G_{TXRF}	−49	−47	−43	
Idle Mode	G_{TXIF}	−19	−16	−13	
Range (T_X to R_X Mode)	ΔG_{TXF}	50	53	56	
Half Attenuation Range (B5 = 1)					
T_X Mode	G_{TXH}	−9.0	−6.5	−3.0	
R_X Mode	G_{TXRH}	−36	−34	−30	
Idle Mode	G_{TXIH}	−19	−16	−13	
Range (T_X to R_X Mode)	ΔG_{TXH}	23	27	29	
RAO, TAO Output Current Capability	I_{OATT}	–	2.0	–	mA
RAO Offset Voltage with Respect to V_B	V_{RAO}				mVdc
R_X Mode		–	−50	–	
Idle Mode		–	0	–	
T_X Mode		–	−2.0	–	
TAO Offset Voltage with Respect to V_B	V_{TAO}				mVdc
R_X Mode		–	−2.0	–	
Idle Mode		–	−5.0	–	
T_X Mode		–	−50	–	
MICROPHONE AMPLIFIER (Pins 21, 22)					
Output Offset with Respect to V_B (RF = 300 kΩ)	MCO_{VOS}	–	−10	–	mVdc
Input Bias Current (Pin 21)	I_{MBIAS}	–	−30	–	nA
Open Loop Gain (f < 100 Hz)	A_{VOLM}	–	80	–	dB
Gain Bandwidth	GBW_M	–	1.5	–	MHz
Maximum Output Voltage Swing (Note 1)	V_{OMAX}	–	350	–	mVrms
Maximum Output Current Capability	I_{OMCO}	–	2.0	–	mA
MUTING (Δ Gain)					
Microphone Amplifier Only (Measured at Pin 22)	AMT				dB
RF = 300 kΩ		–	73	–	
RF = 100 kΩ		–	64	–	
Microphone Amplifier + Transmit Attenuator in Receive Mode (Measured at Pin 23) RF = 300 kΩ	TMT	95	113	–	dB

NOTE: 1. Output swing is limited by the capability of the transmit attenuator input. See Figure 16.

ELECTRICAL CHARACTERISTICS (continued) (T_A = +25°C, V_{CC} = 5.0 V, CD ≤ 0.8 V, unless noted, see Figure 3.)

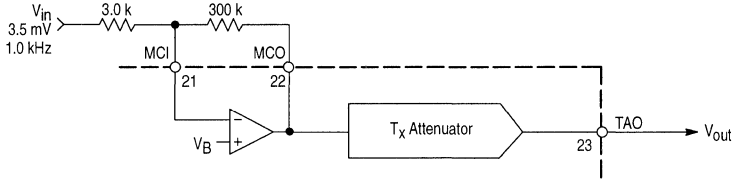
Characteristic	Symbol	Min	Typ	Max	Unit
MUTING (Δ Gain)					
Timing from Data Ready Lo–to–Hi (See Figure 27)					µs
To Mute	t_{MM}	–	2.0	–	
To Enable	t_{ENM}	–	1.0	–	
RECEIVE AMPLIFIER (Pins 15, 16)					
Output Offset with Respect to V_B (RF = 10 kΩ)	RXO_{VOS}	–	–1.3	–	mVdc
Input Bias Current (Pin 16)	I_{RBIAS}	–	–30	–	nA
Open Loop Gain (f < 100 Hz)	A_{VOLR}	–	80	–	dB
Gain Bandwidth	G_{BWR}	–	1.5	–	MHz
Maximum Output Voltage Swing (Note 2)	V_{OMAX}	–	350	–	mVrms
Maximum Output Current Capability	I_{ORXO}	–	2.0	–	mA
LEVEL DETECTORS AND BACKGROUND NOISE MONITORS					
T_X–R_X Switching Threshold (Pins 4, 11)	I_{TH}	0.8	1.0	1.2	µA/µA
CPR, CPT Output Resistance (for Pulldown)	R_{CP}	–	5.0	–	Ω
CPR, CPT Leakage Current	I_{CPLK}	–	–0.2	–	µA
CPR, CPT Nominal DC Voltage (No Signal)	V_{CP}	–	1.9	–	Vdc
TLO, RLO, CP2 Source Current (@ V_B – 1.0 V)	I_{LDOH}	–	–2.0	–	mA
TLO, RLO, CP2 Output Resistance	R_{LD}	–	500	–	Ω
TLO, RLO, CP2 Sink Current (@ V_B + 1.0 V)	I_{LDOL}	–	2.0	–	µA
CD INPUT (Pin 8)					
Switching Threshold	V_{THCD}	–	1.5	–	Vdc
Input Resistance (V_{in} = 0.8 V)	R_{CD}	170	235	300	kΩ
Input Current (V_{in} = 5.0 V)	I_{CD}	–	40	–	µA
Timing					µs
To Disable	t_{CD}	–	3.0	–	
To Enable	t_{ENC}	–	See Figure 26	–	
POR INPUT (Pin 20)					
Switching Threshold (2.7 V ≤ V_{CC} ≤ 6.5 V)	V_{THPOR}	–	1.2	–	Vdc
Nominal DC Voltage (2.7 V ≤ V_{CC} ≤ 6.5 V)	V_{POR}	–	1.5	–	Vdc
Effective Resistance (0 V < V_{in} < 0.5 V)	R_{POR}	70	115	160	kΩ
Input Current	I_{POR}				µA
V_{in} = 0 V		–	–40	–	
V_{in} = 5.0 V		–	630	–	
Timing to Reset (Pin 20 Taken to < 1.2 V)	t_{POR}	–	30	–	µs
Minimum Power On Reset Time (See Figure 20)	T_{MPOR}				ms
C = 0.1 µF V_{CC} = 6.5 V		–	2.7	–	
V_{CC} = 5.0 V		–	3.7	–	
V_{CC} = 2.7 V		–	10.6	–	

NOTE: 2. Output swing is limited by the capability of the receive attenuator input. See Figure 16.

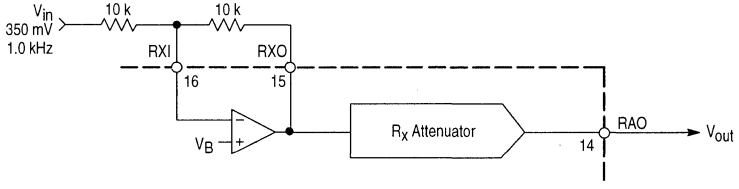
ELECTRICAL CHARACTERISTICS (continued) (T_A = +25°C, V_{CC} = 5.0 V, CD ≤ 0.8 V, unless noted, see Figure 3.)

Characteristic	Symbol	Min	Typ	Max	Unit
SERIAL PORT (Pins 17–19)					
Switching Threshold	V_{THSP}	–	1.3	–	Vdc
Clock Input Current (Pin 17)	I_{INCK}				µA
DR ≤ 0.8 V V_{in} = 0.9 V		5.6	7.5	12.8	
V_{in} = 5.0 V		–	75	–	
DR ≥ 2.0 V V_{in} = 0.6 V		5.2	7.9	13.3	
V_{in} = 5.0 V		–	84	–	
Data Input Current (Pin 18)	I_{INDA}				µA
V_{in} = 0.9 V		5.6	7.5	12.8	
V_{in} = 5.0 V		–	75	–	
Data Ready Input Current (Pin 19)	I_{INDR}				µA
V_{in} = 0.9 V		13.8	20	36	
V_{in} = 5.0 V		–	200	–	
Timing (Minimum Requirements) (See Figure 2)					ns
Data Ready Falling Edge to Clock	t_1	–	200	–	
8th Clock Rising Edge to DR Rising Edge	t_2	–	100	–	
Data Setup Time	t_3	–	100	–	
Data Hold Time	t_4	–	100	–	
Clock High Time	t_5	–	200	–	
SYSTEM DISTORTION (See Figure 1)					
Microphone Amplifier + T_X Attenuator Distortion	THD_T	–	0.2	3.0	%
Receive Amplifier + R_X Attenuator Distortion	THD_R	–	0.2	3.0	%

Figure 1. System Distortion Test



NOTE: T_X Attenuator forced to transmit mode.



NOTE: R_X Attenuator forced to receive mode.

TYPICAL TEMPERATURE PERFORMANCE

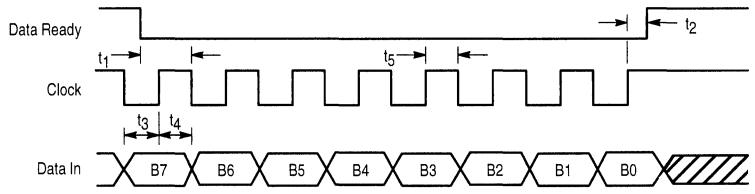
Characteristics	−40°C	0°C	+25°C	+85°C	Unit
Power Supply Current Enabled, V_B Open Disabled, V_B Open	 5.4 129	 4.9 118	 4.6 110	 4.2 125	 mA µA
V_B Output Voltage (I_{VB} = 0)	2.0	2.15	2.2	2.3	Vdc
C_T Source Current (Switching to R_X Mode)	−37	−41	−42	−42	µA
C_T Sink Current (Switching to T_X Mode)	36	41	42	43	µA
Attenuator "On" Gain (Full Range)	6.7	6.7	6.7	6.4	dB
Attenuator Range (Full Range)	53	53	53	53	dB
Volume Control Range (R_X Mode Only, B3–B0 Changed from 0000 to 1111)	36	39	40	42	dB
AGC Attenuation Range	38	20	21	22	dB

NOTE: Temperature data is typical performance only, based on sample characterization, and does not provide guaranteed limits over temperature.

PIN FUNCTION DESCRIPTION

Pin	Symbol	Description
1	CP2	A capacitor at this pin stores voltage representing the transmit background noise and speech levels for the background noise monitor.
2	XDI	Input to the transmit background noise monitor.
3	CPT	An RC sets the time constant for the transmit background noise monitor.
4	TLI	Input to the transmit level detector.
5	TLO	Output of the transmit level detector.
6	V_B	A mid–supply reference voltage, and analog ground for the amplifiers. This must be well bypassed for proper power supply rejection.
7	C_T	An RC sets the switching time between transmit, receive and idle modes.
8	CD	Chip Disable (Logic Input). When low, the IC is active. When high, the entire IC is powered down and non–functional, except for V_B. Input impedance is nominally 235 kΩ.
9	NC	No internal connection.
10	CPR	An RC sets the time constant for the receive background noise monitor.
11	RLI	Input to the receive level detector.
12	RLO	Output of the receive level detector.
13	GND	Ground pin for the entire IC.
14	RAO	Output of the receive attenuator.
15	RXO	Output of the receive path input amplifier, and input of the receive attenuator and the dial tone detector.
16	RXI	Inverting input of the receive amplifier. Bias current flows out of the pin.
17	CLK	Serial Port Clock. 1.0 MHz maximum. Data is entered on clock's rising edge.
18	DATA	Serial Port Data Input. Data consists of an 8 bit word, B7 first, B0 last.
19	DR	Serial Port Data Ready. Taking this line high latches new data into the registers.
20	POR	Power On Reset for the serial port. Upon power up, or when CD is active, all internal registers are set to logic 0. This logic input may be taken low to reset the registers.
21	MCI	Inverting input of the microphone amplifier. Bias current flows out of the pin.
22	MCO	Output of the microphone amplifier, and input of the transmit attenuator.
23	TAO	Output of the transmit attenuator.
24	V_{CC}	Power Supply Pin. Operating Range is 2.7 V to 6.5 Vdc. Bypassing is requried.

Figure 2. Serial Port Timing Diagram



NOTES: 1. Maximum clock and data rate is 1.0 MHz. There is no required minimum rate.
2. B7 is to be entered first, B0 last.
3. Data is entered on the clock rising edge.
4. Clock can continue to toggle after B0 is entered if Data Ready goes high before the clock's next rising edge. This is not recommended due to possible noise problems.
5. Upon power up, all bits are internally set to logic 0, by the POR pin.
6. Data Ready must go low before the first falling clock edge after the clock rising edge associated with B7. See text for additional information.

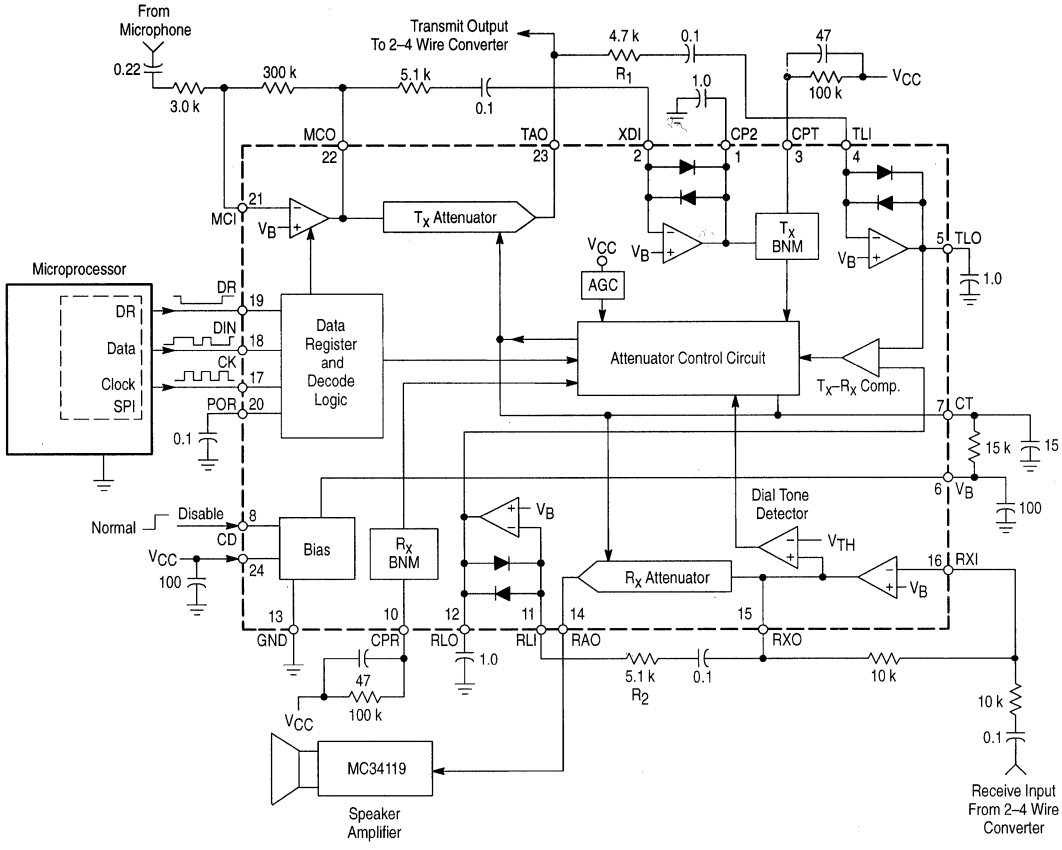
2

SERIAL PORT CONTROL BITS

Bits	Code	Function
B7, B6	00	Normal voice switched operation
	01	Force to receive mode
	10	Force to idle mode
	11	Force to transmit mode
B5	0	Attenuator range is 53 dB
	1	Attenuator range is 27 dB
B4	0	Microphone amplifier is active
	1	Microphone amplifier is muted
B3–B0 (Note 1)	0000	Maximum receive volume
	1111	Minimum receive volume

NOTE: 1. Bit B0 is the LSB for the volume control.

Figure 3. MC33218A Block Diagram and Test Circuit



NOTES: 1. All capacitors are in μF unless otherwise noted.
2. Values shown are suggested initial values only. See Applications Information for circuit adjustments.

Figure 4. Attenuator Gain versus V_{CT} (Pin 7)
(Full Attenuator Range)

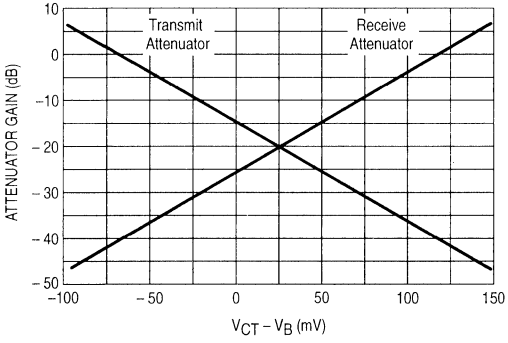


Figure 5. Attenuator Gain versus V_{CT}
(Half Attenuation Range)

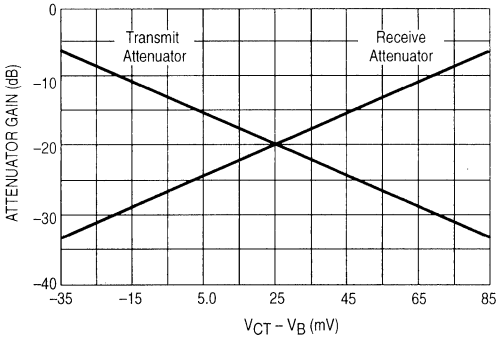


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Figure 6. Receive Gain versus Volume Control Levels (Full Attenuation Range)

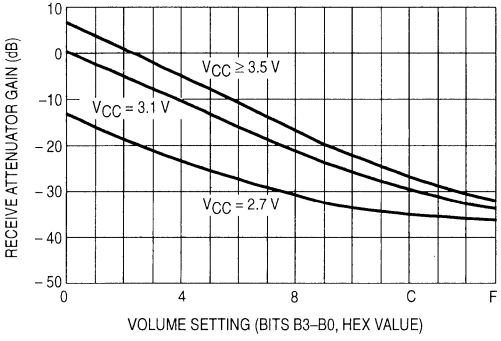

Figure 7. Receive Gain versus Volume Control Levels (Half Attenuation Range)

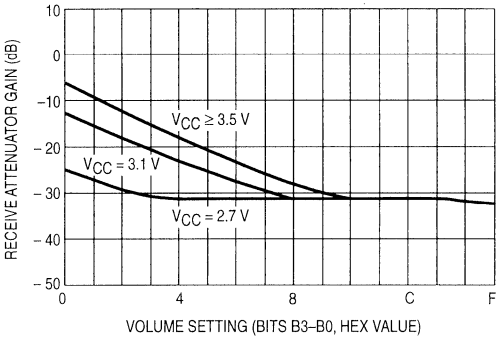

Figure 8. Receive Gain versus V_{CC}

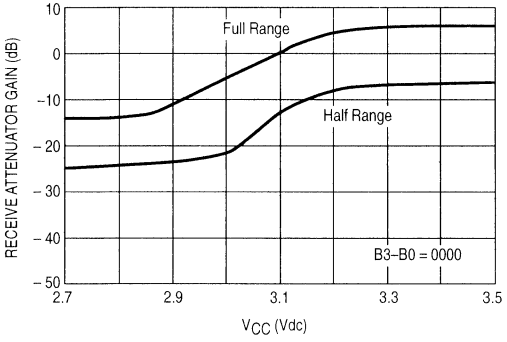

Figure 9. Level Detector AC Transfer Characteristics

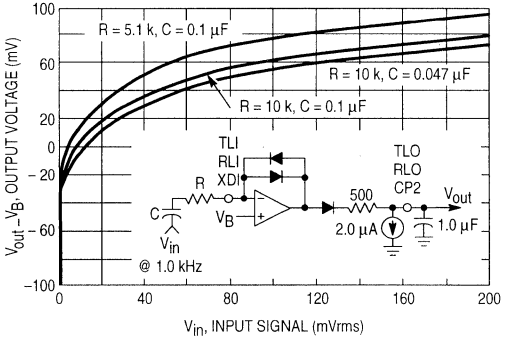

Figure 10. Level Detector AC Transfer Characteristics versus Frequency

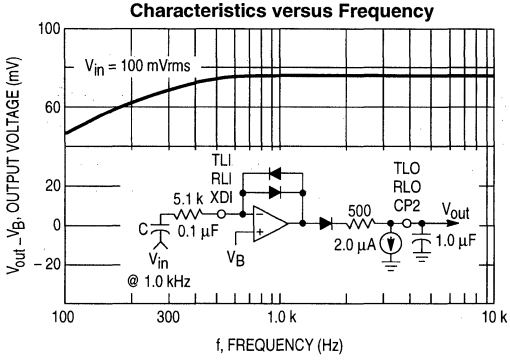

Figure 11. Level Detector DC Transfer Characteristics

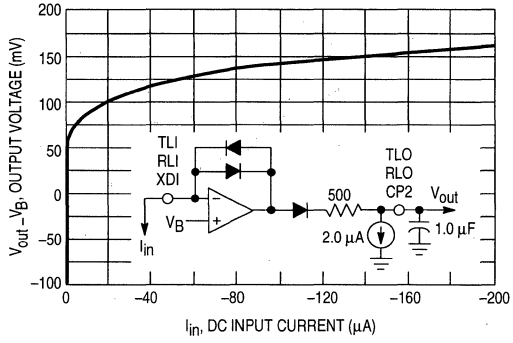

Figure 12. CD Input Characteristics (Pin 8)

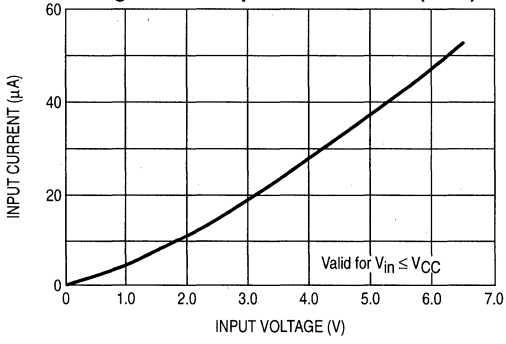

Figure 13. Power Supply Current

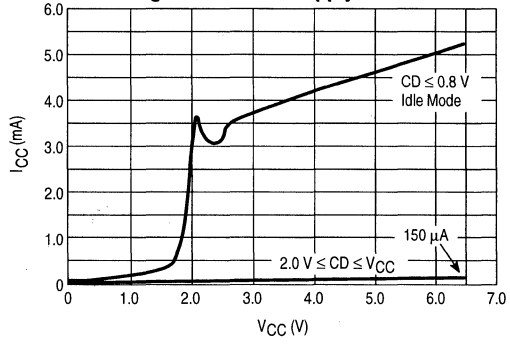

Figure 14. V_B Output Characteristics

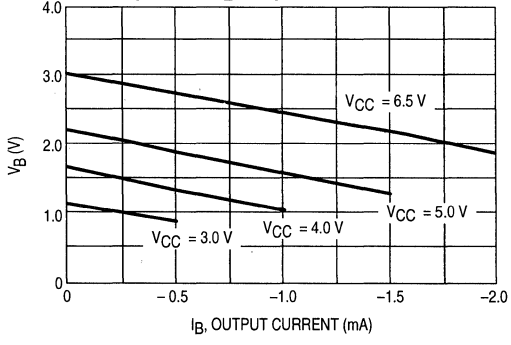

Figure 15. V_B Power Supply Rejection versus Frequency and V_B Capacitor

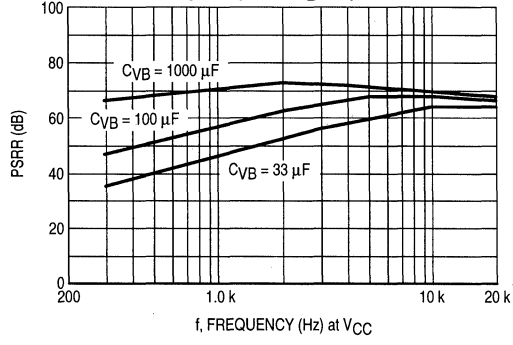

Figure 16. Receive Amp and Microphone Amp Output Swing

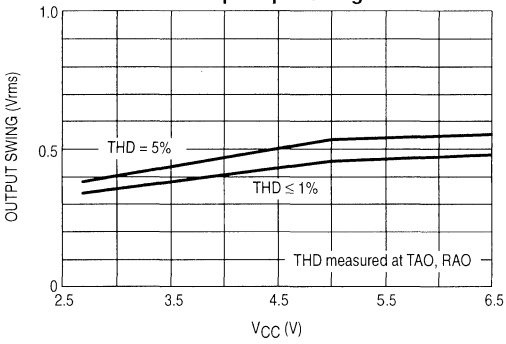

Figure 17. Microphone Amplifier Muting versus Feedback Resistor

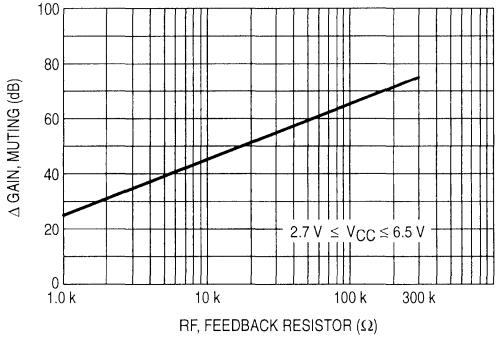

Figure 18. Serial Port Input Characteristics (Pins 17, 18, 19)

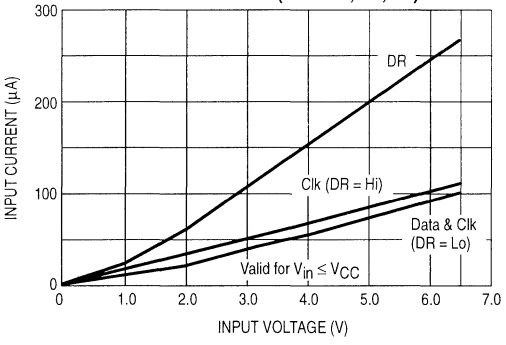

Figure 19. POR Input Characteristics (Pin 20)

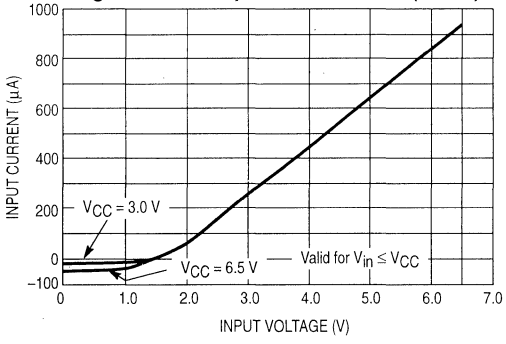

Figure 20. Minimum Reset Time versus V_{CC} and Pin 20 Capacitor

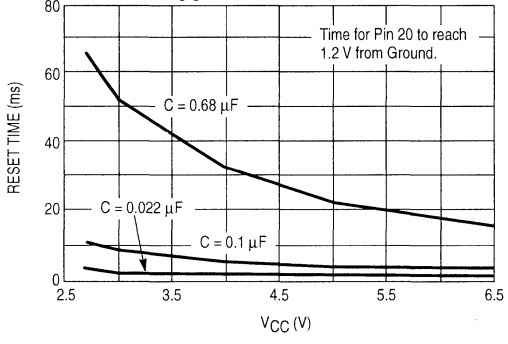

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Figure 21. Idle ◄——► Transmit Timing

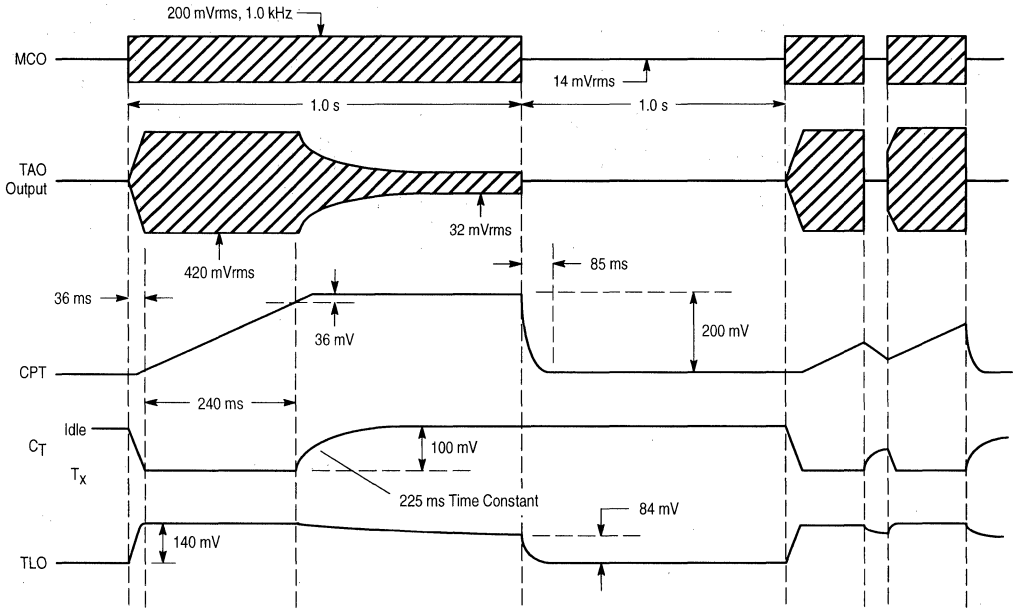
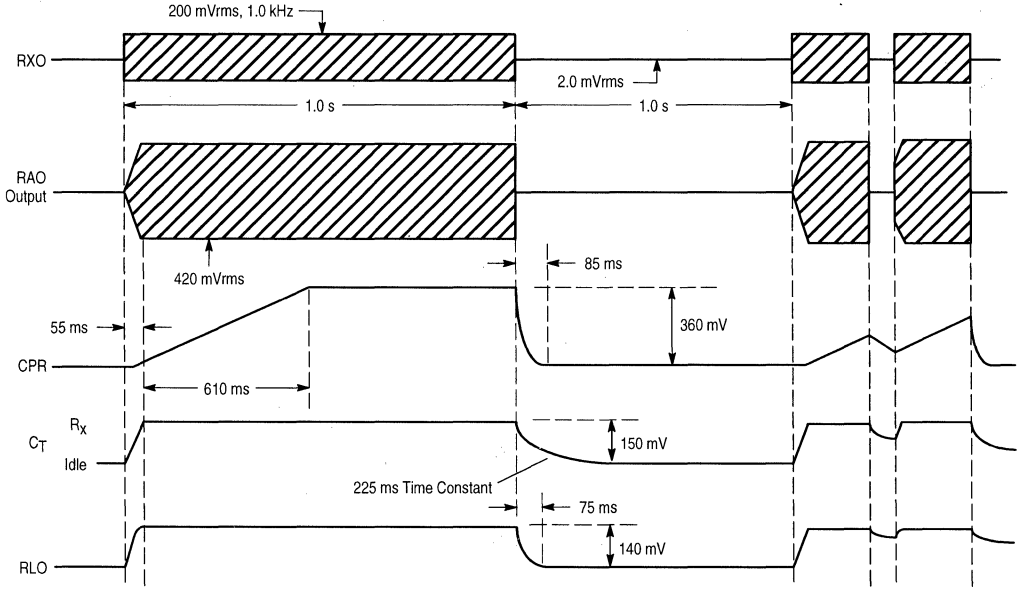
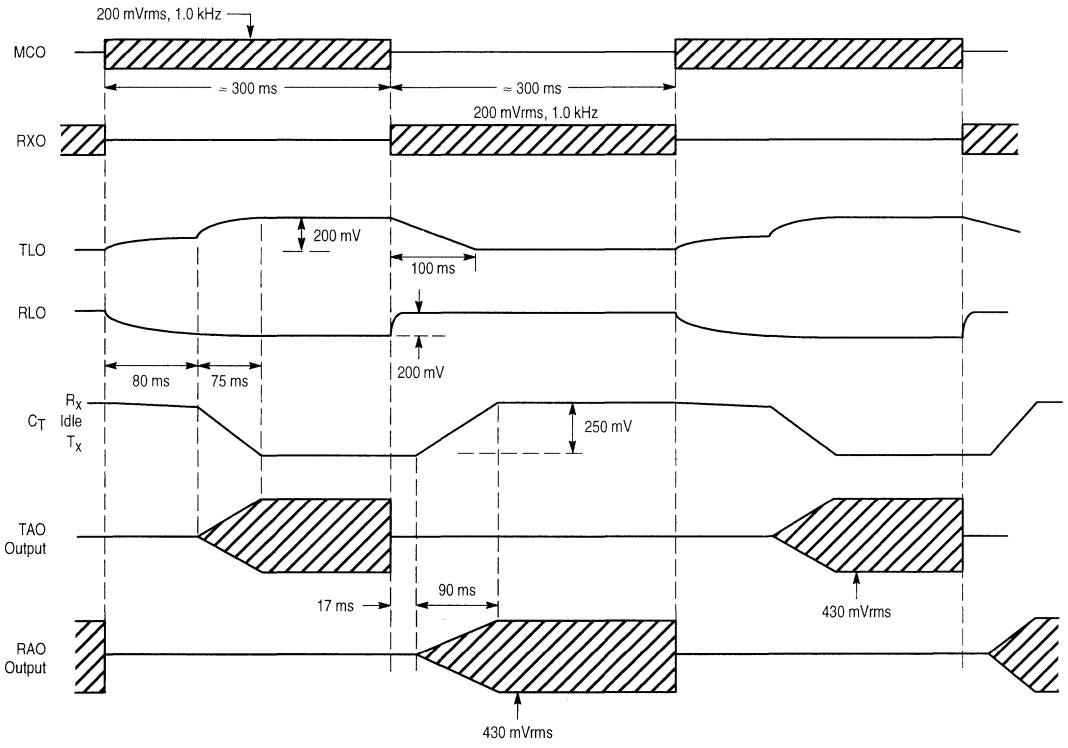


Figure 22. Idle ◄——► Receive Timing



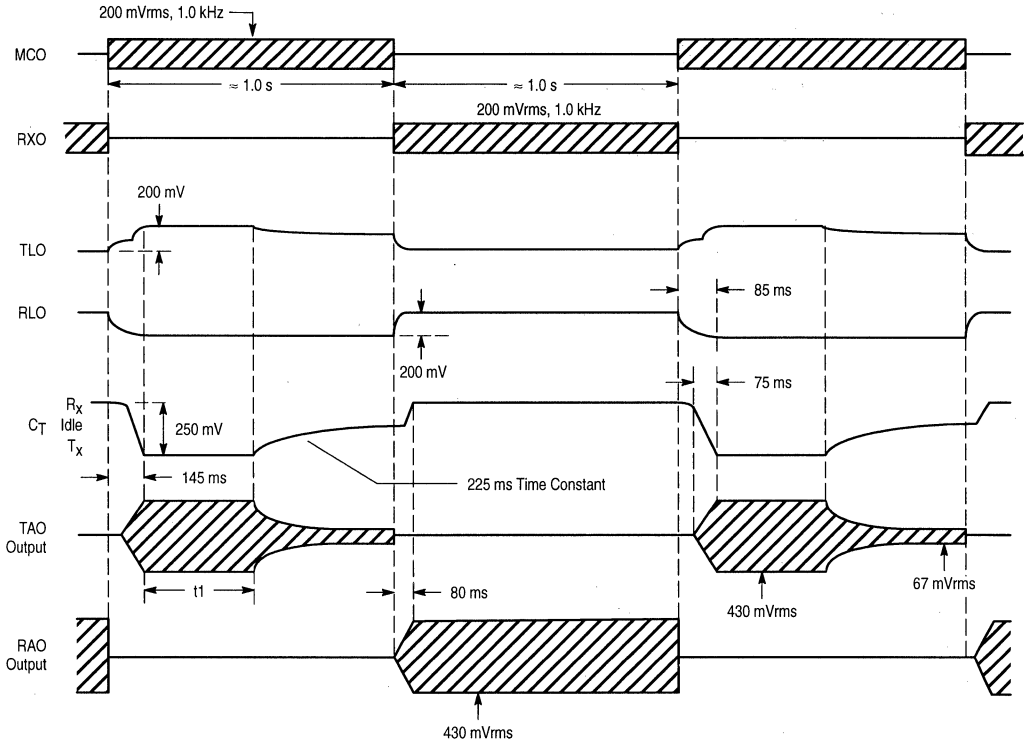
NOTE: Refer to Figure 3 for component values. Timing and output amplitudes shown are nominal, and are for the indicated input signal and component values. Actual timing and outputs will vary with the application. Bits B7, B6 = 00.

Figure 23. Transmit ◄——► Receive Timing (Short Cycle Timing)



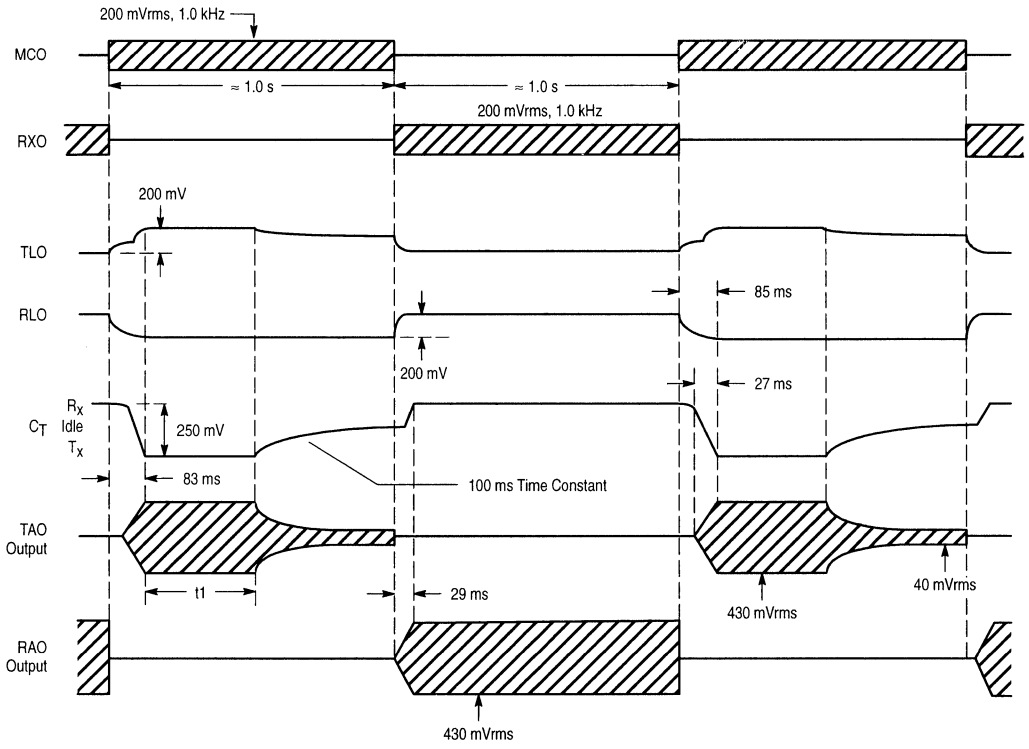
NOTE: External component values are those shown in Figure 3. Timing and output amplitudes shown are nominal, and are for the indicated input signal and component values. Actual timing and outputs will vary with the application. Bits B7, B6 = 00.

Figure 24. Transmit ⟷ Receive Timing (Long Cycle Timing)



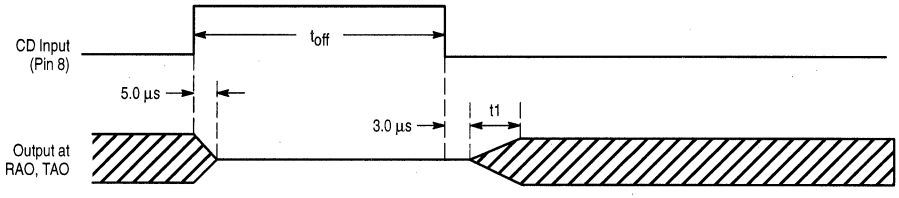
NOTE: External component values are those shown in Figure 3. Timing and output amplitudes shown are nominal, and are for the indicated input signal and component values. Actual timing and outputs will vary with the application. Time t1 depends on the ratio of the "on"/"off" amplitude of the signal at MCO. Bits B7, B6 = 00.

Figure 25. Transmit ⟷ Receive Timing (Long Cycle Timing)



NOTE: External component values are those shown in Figure 3, except the capacitor at C_T is 6.8 µF. Timing and output amplitudes shown are nominal, and are for the indicated input signal and component values. Actual timing and outputs will vary with the application. Time t1 depends on the ratio of the "on"/"off" amplitude of the signal at MCO. Bits B7, B6 = 00.

Figure 26. Chip Disable Timing



2

NOTE: Enable time t1 depends on the length of t_{off} according to the following chart:

t_{off}	t1
10 ms	25 ms
20 ms	45 ms
≥ 50 ms	60 ms

Figure 27. Mute Timing

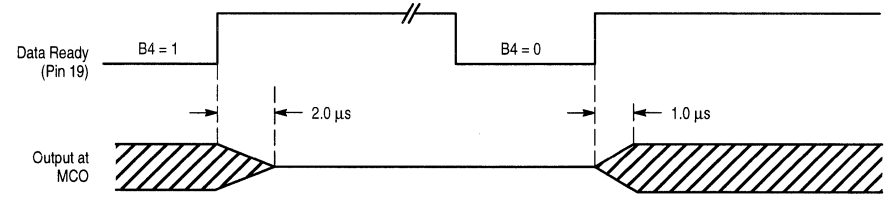
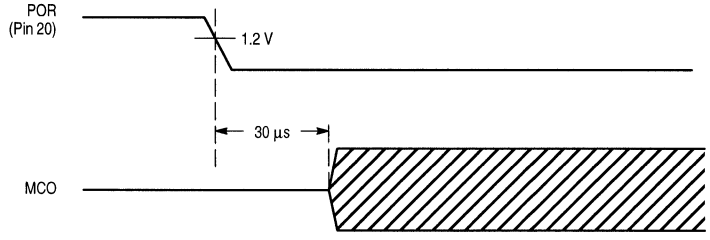


Figure 28. POR Timing



NOTE: Above time established by first muting the microphone amplifier (B4 = 1). Then the POR pin is taken low. The 30 µs is representative if the internal delay for the internal registers to be reset to 0, and the associated function change. The registers will remain set to 0 when POR goes high, until new data is written.

FUNCTIONAL DESCRIPTION

Introduction

The fundamental difference between the operation of a speakerphone and a telephone handset is that of half–duplex versus full–duplex. The handset is full duplex, meaning conversation can occur in both directions (transmit and receive) simultaneously. This is possible due to both the low sound level at the receiver, and the fact that the acoustic coupling from the earpiece to the mouthpiece is almost non–existent (the receiver is normally held against a person's ear). The loop gain from the receiver to the microphone and through the circuit is well below that needed to sustain oscillations.

A speakerphone, on the other hand, has higher gain levels in both the transmit and receive paths, and attempting to converse full duplex results in oscillatory problems due to the loop that exists within the speakerphone circuit. The loop is formed by the hybrid, the acoustic coupling (speaker to microphone), and the transmit and receive paths (between the hybrid and the speaker/microphone). The only practical and economical method used to date is to design the speakerphone to function in a half duplex mode – i.e., only one person speaks at a time, while the other listens. To achieve this requires a circuit which can detect who is talking (in reality, who is talking louder), switch "on" the appropriate path (transmit or receive), and switch "off" (attenuate) the other path. In this way, the loop gain is maintained less than unity. When the talkers exchange function, the circuit must quickly detect this, and switch the circuit appropriately. By providing speech level detectors, the circuit operates in a "hands–free" mode, eliminating the need for a "push–to–talk" switch.

The MC33218A provides the necessary circuitry to perform a voice switched, half duplex, speakerphone function. The IC includes transmit and receive attenuators, pre–amplifiers, and level detectors and background noise monitors for each path. An attenuator control circuit automatically adjusts the gain of the transmit and receive attenuators based on the relative strengths of the voice signals present, the volume control, and the supply voltage (when low). The detection sensitivity and timing are externally controllable.

The MC33218A is unique compared to most speakerphone integrated circuits in that it has a microprocessor serial port for control of various functions. Those functions are:

- Volume level (15 steps of ≈ 3.0 dB each)
- Microphone amplifier mute
- Attenuator range selection (53 dB or 27 dB)
- Force to receive, idle, or transmit to override the automatic switching.

Please refer to the Block Diagram (Figure 3) when reading the following sections.

Transmit and Receive Attenuators (Full Range B5 = 0)

The transmit and receive attenuators are complementary, performing a log–antilog function. When one is at maximum gain (≈ 6.7 dB), the other is at maximum attenuation (–47 dB) – they are never both fully "on" or fully "off". Both attenuators are controlled by a single output from the Attenuator Control Circuit which ensures the sum of their gains will remain constant at a typical value of –40 dB. Their purpose is to provide the half–duplex operation required in a speakerphone.

The attenuators are non–inverting, and have a usable bandwidth of 50 kHz. Their input signal (at MCO and RXO) should be limited to 300 mVrms (850 mVp–p) to prevent distortion. That maximum recommended input signal is independent of the volume control setting. Both the inputs and outputs are biased at ≈ V_B. The output impedance is <10 Ω until the output current limit (typically 2.0 mA peak) is reached.

The attenuators are controlled by the single output of the Attenuator Control Circuit, which is measurable at C_T (Pin 7). When the circuit detects speech signals directing it to the receive mode (by means of the level detectors described below), an internal current source of 42 μA will charge the C_T capacitor to a voltage positive with respect to V_B (see Figure 29). At the maximum volume control setting, this voltage will be approximately +150 mV, and the receive attenuator will have a gain of +6.7 dB. When the circuit detects speech signals directing it to the transmit mode, an internal current source of 42 μA will take the capacitor to approximately –100 mV with respect to V_B (the transmit attenuator will have a gain of +6.7 dB). When there is no speech present in either path, the current sources are shut off, and the voltage at C_T will decay to be equal to V_B. This is the idle mode, and the attenuators' gains are nearly half–way between their fully "on" and fully "off" positions (–25 dB for the R_X attenuator, –16 dB for the T_X attenuator). Monitoring the C_T voltage (with respect to V_B) is the most direct method of monitoring the circuit's mode, and its response.

Transmit and Receive Attenuators (Half Range B5 = 1)

With the attenuators set to the half range, the attenuator which is "on" will have a gain of ≈ –7.0 dB, while the "off" attenuator will have a gain of ≈ –34 dB. The idle mode is the same as for the full range (–25 dB for the R_X attenuator, –16 dB for the T_X attenuator). The voltage at the C_T pin, with respect to V_B, will be –35 mV for the transmit mode, and +85 mV for the receive mode.

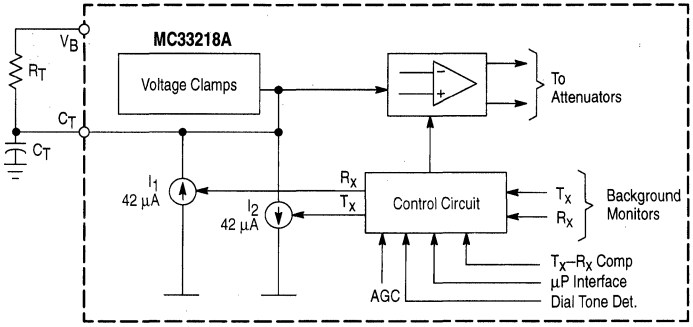
Attenuator Control Circuit

The inputs to the Attenuator Control Section (Figure 29) are six: The T_X–R_X comparator operated by the level detectors, two background noise monitors, the AGC circuit, the dial–tone detector, and the microprocessor interface. These six functions are described as follows.

Level Detectors, T_X–R_X Comparator

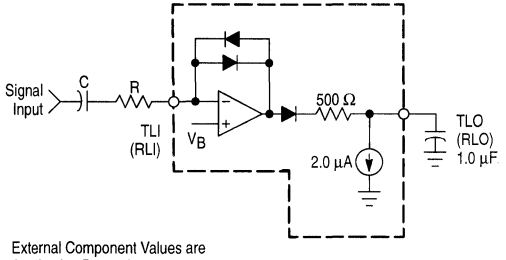
There are two identical level detectors – one on the receive side and one on the transmit side (refer to Figure 30). Each level detector is a high gain amplifier with back–to–back diodes in the feedback path, resulting in non–linear gain, which permits operation over a wide dynamic range of speech levels. Refer to the graphs of Figures 9, 10, and 11 for their DC and AC transfer characteristics. The sensitivity of each level detector is determined by the external resistor and capacitor at their input (TLI and RLI). The output charges an external capacitor through a diode and limiting resistor, thus providing a DC representation of the input AC signal level. The outputs have a quick rise time (determined by the capacitor and an internal 500 Ω resistor), and a slow decay time set by an internal current source and the capacitor. The capacitors at RLO and TLO should have the same value (±10%) to prevent timing problems.

Figure 29. C_T Attenuator Control Circuit



Referring to Figure 3, the outputs of the two level detectors drive the T_X–R_X comparator. The comparator's output state depends on whether the transmit or receive speech signal is stronger, as sensed by the level detectors. The Attenuator Control Circuit uses this signal, along with the background noise monitors, to determine which mode to set.

Figure 30. Level Detector



External Component Values are Application Dependent.

Background Noise Monitors

The purpose of a background noise monitor is to distinguish speech (which consists of bursts) from background noise (a relatively constant signal). There are two background noise monitors – one for the receive path and one for the transmit path. Referring to Figure 32, each is operated on by a level detector, which provides a dc voltage representative of the combined speech and noise level. The peaks, valleys, and bursts, which are characteristic of speech, will cause that DC voltage (at CP2 or RLO) to increase relatively quickly, causing the output of the next amplifier to also rise quickly. If that increase exceeds the 36 mV offset, at a speed faster than the time constant at CPT (CPR), the output of the last comparator will change, indicating the presence of speech to the attenuator control circuit. This will keep the circuit in either the transmit or the receive mode, depending on which side has the stronger signals. Whenever a new continuous signal is applied, the time constant at CPT (CPR) determines how long it takes the circuit to decide that the new sound is continuous, and therefore background noise. The system requires that the average speech signal be stronger than the background noise level (by 6.0–7.0 dB) for proper speech detection to occur.

When only background noise is present in both paths, the output of the monitors will indicate the absence of speech, allowing the circuit to go to the idle mode.

AGC Circuit

In the receive mode only, the AGC circuit decreases the gain of the receive attenuator when the supply voltage at V_{CC} falls below 3.5 V, according to the graph of Figure 8. The gain of the transmit path changes in a complementary manner.

The purpose of this feature is to reduce the power (and current) used by the speaker when the speakerphone is powered by the phone line, and is connected to a long telephone line, where the available power is limited. Reducing the speaker power controls the voltage sag at V_{CC}, reduces clipping and distortion at the speaker output, and prevents possible erratic operation.

Dial Tone Detector

When a speakerphone is initially taken off–hook, the dial tone signal will switch the circuit to the receive mode. However, since the dial tone is a continuous signal, the MC33218A will consider it as background noise, rather than speech, and would switch from receive to idle, causing the dial tone sound to fade. The dial tone detector prevents the fading by disabling the receive background noise monitor.

The dial tone detector is a comparator with one side connected to the receive attenuator input (RXO), and the other input connected to V_B with a –20 mV offset (see Figure 31). If the circuit is in the receive mode, and the incoming signal has peaks greater than 20 mV (14 mV rms), the comparator's output will change, keeping the circuit from switching to the idle mode. The receive attenuator will then be at a gain determined solely by the volume control. **NOTE:** The dial tone detector is **not** a frequency discriminating circuit.

Figure 31. Dial Tone Detector

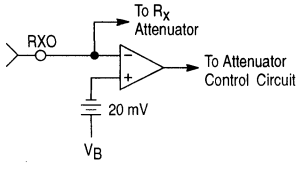
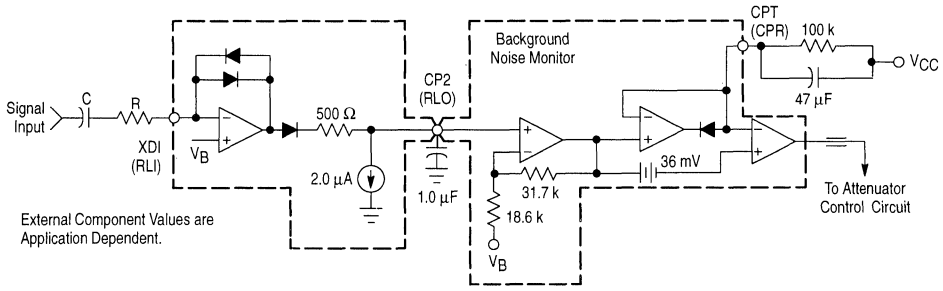


Figure 32. Background Noise Monitor



2

Microprocessor Interface

The three line SPI port (Pins 17–19) is used for setting various functions with a single 8 bit word. The functions are as follows:

– Volume Control: Bits B0–B3 control the gain of the attenuators only when in the receive mode. Setting B3–B0 = 0000 sets the receive attenuator to its maximum gain (+6.7 dB in full range, –7.0 dB in half range), and therefore maximum volume at the speaker. Setting B3–B0 = 1111 sets the receive attenuator to a minimum gain level (≈ –32 dB), and is the minimum volume setting. B0 is the LSB for this function, and each step changes the gain by ≈ 3.0 dB at the high volume end (see Figure 6 and 7). The transmit attenuator gain is varied in a complementary manner. These bits have no effect in the idle or transmit modes.

– Muting of the Microphone Amplifier: Bit B4 is used to set the microphone amplifier to the normal or the muted mode. When this bit is a 1, the amplifier is muted. See the paragraph entitled "Microphone Amplifier, Mute" elsewhere in this document.

– Attenuator Range: Bit B5 is used to select the attenuator range. When it is a 0, the range is 53 dB (from full "on" to full "off"). When it is a 1, the range is 27 dB. The 53 dB range is used for the majority of applications, such as desktop speakerphones (home or office use), intercom units, and any application where the speaker and microphone are in close proximity. The 27 dB range is commonly used in European speakerphone applications, where the typical design involves using the handset for the microphone function, and is therefore somewhat separated from the speaker.

– Operating Mode: Bits B7 and B6 set the circuit operating mode. When 00, the normal voice activated switching is enabled, and the circuit responds to the speech levels as described elsewhere in this document. When 01, the circuit is forced to the receive mode in that the receive attenuator is "on" and the transmit attenuator is "off". The volume control (Bits B3–B0) is effective in this mode. When 10, the circuit is forced to the idle mode. When 11, the circuit is forced to the transmit mode. The volume control bits have no effect in the idle or transmit modes.

The eight bits are entered serially, B7 first and B0 last. Each bit is entered on a clock rising edge. The maximum clock and data rate is 1.0 MHz, and there is no minimum required speed. Data Ready, which is normally high, is to be held low while the eight bits are clocked in. The eight bits take effect when Data Ready is taken high. There is no chip address, or other protocol or handshaking required. See Figure 2 for a timing diagram. Note that Data Ready need not be taken low before the first clock rising edge. It must be taken low before the first clock falling edge which follows the first clock rising edge. This allows Data Ready to be taken low coincident with the first clock rising edge, if desired, as well as before that.

It is recommended that DR be kept high when not entering data, to prevent disruption of the circuit by transients or glitches on the clock or data lines. This is not required, and DR may be taken low after latching in data, if desired.

The clock input can be stopped after B0 is entered, or it may continue to run as long as Data Ready is taken high before the next clock rising edge. It is recommended that the clock not be continued to prevent possible noise problems.

The three inputs must be kept within the range of V_{CC} and GND. If an input is taken more than 0.5 V above V_{CC} or below GND excessive currents will flow, and the device's operation will be distorted. See Figure 18 for input current requirements at these pins.

Power On Reset

The Power On Reset, when at a logic low (below its threshold of 1.2 V) resets the internal registers to a logic 0, independent of the Clock, Data, or Data Ready position. A capacitor on this pin provides a power up time delay to allow V_{CC} to stabilize before the registers can accept data. Alternately, Pin 20 can be driven directly from a logic source if desired. The POR input must be kept within the range of V_{CC} and GND. If the input is taken more than 0.5 V above V_{CC} or below GND excessive currents will flow, and the device's operation will be distorted. The configuration of this pin is shown in Figure 33.

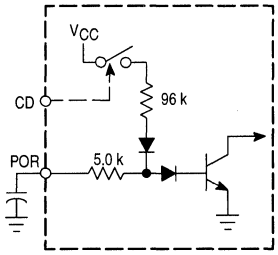
When V_{CC} is applied to the MC33218A, the registers will be enabled when the voltage at POR exceeds 1.2 V. The time to reach this level depends on the capacitor at POR, and V_{CC}, and will not be less than the time shown in Figure 20. The actual reset time is affected by the rise time of V_{CC}. Any data written to the registers while POR is below 1.2 V will not be stored or effective.

The nominal DC voltage at POR is ≈ 1.5 V.

The registers may be intentionally reset by external control by pulling POR to ground with (for example) an open collector NPN transistor. The time to reset is shown in Figure 28. When POR once again goes high, the registers' data will remain at 0 until new data is entered. Old data is not retained. The time required to release the registers after releasing POR (by turning "off" the NPN transistor) is shown in Figure 20.

If POR is driven by an external logic output, its input current requirement is shown in Figure 19.

Figure 33. Power On Reset Pin

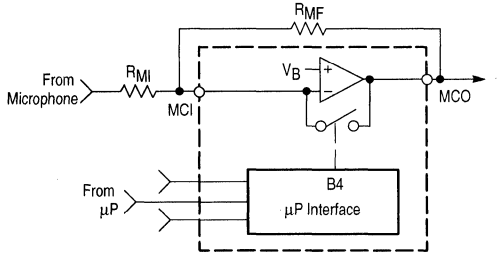


Microphone Amplifier, Mute

The microphone amplifier (Pins 21, 22) has the non–inverting input internally connected to V_B, while the inverting input and the output are pinned out. Unlike most op–amps, the amplifier has an all–NPN output stage, which maximizes phase margin and gain–bandwidth. This feature ensures stability at gains less than unity, as well as with a wide range of reactive loads. The open loop gain is typically 80 dB (f <100 Hz), and the gain–bandwidth is typically 1.5 MHz. The maximum output swing, for 1.0% or less distortion, is determined by the input capability of the transmit attenuator (300–350 mVrms), and by V_{CC} at low supply voltages (see Figure 16). The output impedance is <10 Ω until current limiting is reached (typically 2.0 mA peak). The input bias current at MCI is typically 30 nA out of the pin.

The mute function, when activated, will reduce the gain of the amplifier by shorting the external feedback resistor (RMF Figure 34). The amplifier is not disabled in this mode – MCO remains a low impedance output, and MCI remains a virtual ground at V_B. The amount of muting (the **change** in gain) depends on the value of the external feedback resistor, according to the graph of Figure 17. Muting is enabled by setting bit B4 to a logic 1.

Figure 34. Microphone Amplifier and Mute



Receive Amplifier

The receive amplifier (Pins 15, 16) has the non–inverting input internally connected to V_B, while the inverting input and the output are pinned out. Unlike most op–amps, the amplifier has an all–NPN output stage, which maximizes phase margin and gain–bandwidth. This feature ensures stability at gains less than unity, as well as with a wide range of reactive loads. The open loop gain is typically 80 dB (f <100 Hz), and the gain–bandwidth is typically 1.5 MHz. The maximum p–p output swing, for 1.0% or less distortion, is determined by the input capability of the receive attenuator (300–350 mVrms), and by V_{CC} at low supply voltages (see Figure 16). The output impedance is <10 Ω until current limiting is reached (typically 2.0 mA peak). The input bias current at RXI is typically 30 nA out of the pin.

Power Supply, V_B and Chip Disable

The power supply voltage at Pin 24 is to be between 3.5 and 6.5 V for normal operation, and down to 2.7 V with the AGC in effect (see AGC section). The supply current required is typically 4.6 mA in the idle and transmit modes (at 5.0 V), and slightly more in the receive mode. Figure 13 shows the supply current for both the normal and disabled modes.

The output voltage at V_B (Pin 6) is approximately equal to $(V_{CC} - 0.7)/2$, and provides an ac ground for the internal amplifiers, and the system. The output impedance at V_B is approximately 600 Ω, and in conjunction with the external capacitor at V_B, forms a low pass filter for power supply noise rejection. The choice of the V_B capacitor size is application dependent based on whether the circuit is powered by the telephone line or a regulated supply. See Figure 15 for PSRR data from V_{CC} to V_B. Since V_B biases the microphone and receive amplifiers, the amount of supply rejection at their outputs is a function of the rejection at V_B, as well as the gains of the amplifiers.

The amount of current which can be sourced out of the V_B pin depends on the V_{CC} voltage (see Figure 14). Drawing current in excess of that shown in Figure 14 will cause V_B to drop low enough to disrupt the circuit's operation. This pin can sink ≈ 100 μA when enabled, and 0 μA when disabled.

The Chip Disable (Pin 8) permits powering down the IC for power conservation. With CD between 0 and 0.8 V, normal operation is in effect. With CD between 2.0 V and V_{CC}, the IC is powered down, and the supply current drops to ≈ 110 μA (at V_{CC} = 5.0 V, see Figure 13). When CD is high, the microphone and receive amplifiers, the level detectors, and the two attenuators are disabled (their outputs go to a high impedance). The background noise monitors are disabled, and Pins 3 and 10 will go to V_{CC}. The V_B output, however, remains active, except that it cannot sink any current. The serial port is disabled so that new data may not be entered. Upon re–enabling the circuit, the 8 internal registers will be set to 0, regardless of their previous contents. Figure 26 indicates the disable and enable timing.

The CD input must be kept within the range of V_{CC} and GND. See Figure 12 for input current requirements. If the input is taken more than 0.5 V above V_{CC} or below GND, excessive currents will flow, and the device's operation will be distorted. If the disable function is not used, the pin should be connected to ground.

APPLICATIONS INFORMATION

Switching and Response Time Theory

The switching time of the MC33218A circuit is dominated by the components at C_T (Pin 7, refer to Figure 3), and second by the capacitors at the level detector outputs (RLO, TLO).

The transition time to receive or to transmit mode from idle, or from the other mode, is determined by the capacitor at C_T, together with the internal current sources (refer to Figure 29). The switching time is:

$$\Delta T = \frac{\Delta V \times C_T}{I}$$

When switching from idle to receive, ΔV = 150 mV, I = 42 μA, the C_T capacitor is 15 μF, and ΔT calculates to ≈ 53 ms. When switching from idle to transmit, ΔV = 100 mV, I = 42 μA, the C_T capacitor is 15 μF, and ΔT calculates to ≈ 36 ms.

When the circuit switches to idle, the internal current sources are shut "off", and the time constant is determined by the C_T capacitor and RT, the external resistor (see Figure 29). With C_T = 15 μF, and RT = 15 kΩ, the time constant is ≈ 225 ms, giving a total switching time of ≈ 0.68 s (for 95% change). The switching period to idle begins when both speakers have stopped talking. The switching time back to the original mode will depend on how soon that speaker begins speaking again. The sooner the speaking starts during the "decay to idle" period, the quicker the switching time since a smaller voltage excursion is required. That switching time is determined by the internal current sources as described above.

When the circuit switches directly from receive to transmit (or vice–versa), the total switching time depends not only on the components and currents at the C_T pin, but also on the response of the level detectors, the relative amplitude of the two speech signals, and the mode of the circuit, since the two level detectors are connected differently to the two attenuators.

The rise time of the level detector's outputs (RLO, TLO) is not significant since it is so short. The decay time, however, provides a significant part of the "hold time" necessary to hold the circuit (in transmit or receive) during the normal pauses in speech. The capacitors at the two outputs must be equal value (±10%) to prevent problems in timing and signal response.

The components at the inputs of the level detectors (RLI, TLI) do not affect the switching time, but rather affect the relative signal levels required to switch the circuit, as well as the frequency response of the detectors. They must be adjusted for proper switching response as described later in this document.

Switching and Response Time Measurements

Using burst of 1.0 kHz sine waves to force the circuit to switch among its modes, the timing results were measured and are indicated in Figures 21–25.

a) In Figure 21, when a signal is applied to the transmit attenuator only (normally via the microphone and the microphone amplifier), the transmit background noise monitor immediately indicates the "presence of speech" as evidenced by the fact that CPT begins rising. The slope of the rising CPT signal is determined by the external resistor and capacitor on that pin. Even though the transmit attenuator is initially in the idle mode (–16 dB), there is sufficient signal at its output to cause TLO to increase. The attenuator control circuit then forces the circuit to the transmit mode, evidenced by the change at the C_T pin. The attenuator output signal is then 6.7 dB above the input.

With the steady sine wave applied to the transmit input, the circuit will stay in the transmit mode until the CPT pin gets to within 36 mV of its final value. At that point the internal comparator (see Figure 32) switches, indicating to the attenuator control circuit that the signal is not speech, but rather it is background noise. The circuit now begins to decay to idle, as evidenced by the change at C_T and TLO, and the change in amplitude at TAO.

When the transmit signal at MCO is removed (or reduced), the CPT pin drops quickly, allowing the CPT to quickly respond to any new speech which may appear afterwards. The voltage at C_T decays according to the time constant of its external components, if not already at idle.

The voltage change at CP2, CPT, and TAO depend on the input signal's amplitude, and the components at XDI and TLI. The change at C_T is internally fixed at the level shown. The timing numbers shown depend both on the signal amplitudes and the components at the C_T and CPT pins.

b) Figure 22 indicates what happens when the same signal is applied to the receive side only. RLO and CPR react similarly to TLO and CPT. However, the circuit does not switch to idle when CPR finishes transitioning since the dial tone detector disables the background noise monitor, allowing the circuit to stay in the receive mode as long as there is a signal present. If the input signal amplitude had been less than the dial tone detector's threshold, the circuit response would have been similar to that shown in Figure 21. The voltage change at C_T depends on the setting of the volume control (bits B3–B0). The +150 mV represent maximum volume.

c) Figure 23 indicates the circuit response when transmit and receive signals are alternately applied, with relatively short cycle times (300 ms each) so that neither attenuator will begin to go to idle during its "on" time. Figure 24 indicates the circuit response with longer cycle times (1 s each), where the transmit side is allowed to go to idle. Figure 25 is the same as Figure 24, except the capacitor at CT has been reduced from 15 μF to 6.8 μF, providing a quicker switching time. The reactions at the various pins are shown. The response times at TAO and RAO are different, and typically slightly longer than what is shown in Figures 21 and 22 due to:

– The larger transition required at CT pin,

– The greater difference in the levels at RLO and TLO due to the positions of the attenuators, as well as their decay time, and

– Response time of background noise monitors.

The timing responses shown in these three figures are representative for those input signal amplitudes, and burst durations. Actual response time will vary for different signal conditions.

NOTE: While it may seem desirable to decrease the switching time between modes by reducing the capacitor at CT, this should be done with caution for two reasons:

1) If the switching time is too short, the circuit response may appear to be "too quick" to the user, who may consider its operation erratic. The recommended values in this data sheet, along with the accompanying timings, provide what

experience has shown to be a "comfortable response" by the circuit.

2) The distortion in the receive attenuator will increase as the CT capacitor value is decreased. The extra THD will be most noticeable at the lower frequencies, and at the lower amplitudes. Table 1 provides a guideline for this issue.

Table 1. THD versus CT Capacitor

CT Capacitor	Idle–R_X Transition	Input @ RAI	Freq.	THD @ RAO
15 µF	53 ms	20 mVrms	300 Hz	1.5%
			1.0 kHz	0.3%
		100 mVrms	300 Hz	0.6%
			1.0 kHz	0.12%
6.8 µF	24 ms	20 mVrms	300 Hz	3.6%
			1.0 kHz	1.0%
		100 mVrms	300 Hz	1.4%
			1.0 kHz	0.4%
3.3 µF	12 ms	20 mVrms	300 Hz	7.0%
			1.0 kHz	1.9%
		100 mVrms	300 Hz	2.8%
			1.0 kHz	0.7%

Considerations in the Design of a Speakerphone

The design and adjustment of a speakerphone involves human interfaces issues, as well as proper signal levels. Because of this fact, it is not practical to do all of the design mathematically. Certain parts of the design must be done by trial and error, most notably the switching response and the "How does it sound?" part of the testing. Among the recommendations for a successful design are:

1) Design the enclosure **concurrently** with the electronics. Do not leave the case design to the end as its properties are just as important (just as *equally* important) as the electronics. One of the major issues involved in a speakerphone design is the acoustic coupling of the speaker to the microphone, which must be minimized. This parameter is dependent entirely on the design of the enclosure, the mounting of the speaker and the microphone, and their characteristics.

2) Ensure the speaker is optimally mounted. This fact alone can make a difference of several dB in the sound level from the speaker, as well as the sound quality. The speaker manufacturer should be consulted for this information.

3) Do not breadboard the circuit with the microphone and speaker hanging out in midair. It will not work. The speaker and microphone must be in a suitable enclosure, preferably one resembling the end product. If this is not feasible, temporarily use some other properly designed enclosure, such as one of the many speakerphones on the market.

4) Do not breadboard the circuit on a wirewrapped board or a plug–in prototyping board. Use a PC board, preferably with a ground plane. Proper filtering of the supply voltage, at the V_{CC} pin, is essential.

5) The speakerphone must be tested with the intended hybrid, and connected to a phone line, or phone line simulator. The performance of the hybrid is just as important as the enclosure and the speakerphone IC.

6) When testing the speakerphone, be conscious of the environment. If the speakerphone is in a room with large windows and tile floors, it will sound different than if it is in a carpeted room with drapes. Additionally, be conscious of the background noise in a room.

7) When testing the speakerphone on a phone line, make sure the person at the other end of the phone line is **not** in the same room as the speakerphone.

Design and Adjustment Procedure

Assuming the end product enclosure is available, with the intended production microphone and speaker installed, and the PC boards installed (or temporary substitutes for the PC boards) a recommended sequence is as follows (refer to Figure 35):

1) Design the hybrid, ensuring it interfaces properly with the phone line for both DC and AC characteristics. The return loss must be adjusted so as to comply with the appropriate regulatory agency. The sidetone should then be adjusted according to the intent of the product. If the product is a speakerphone only, without a handset, the sidetone gain (GST) should be adjusted for maximum loss. If a handset is part of the end product, the sidetone must be adjusted for the minimum acceptable sidetone levels in the handset. Generally, for the speakerphone, 10–20 dB sidetone loss is preferred for GST.

2) Check the acoustic coupling of the enclosure (GAC in Figure 35). With a steady sound coming out of the speaker, measure the rms voltage on the speaker terminals, and the rms voltage out of the microphone. Experience has shown that the loss should be at least 40 dB, preferably 50 dB. This should be checked over the frequency range of 20 Hz to 10 kHz.

3) Adjust the transmit path for proper signal levels, based on the lowest speech levels as well as the loudest. Based on the typical levels from commonly available microphones, a gain of about 35–45 dB is required from the microphone terminals to Tip and Ring. Most of that gain should be in the microphone amplifier so as to make best use of the transmit attenuator, but make sure the maximum attenuator input level at MCO is not exceeded. If a signal generator is used instead of a microphone for testing, the circuit can be locked into the transmit mode by grounding CPT (Pin 3), or using bits B7 and B6 (set to 11). Frequency response can generally be tailored with capacitors at the microphone amplifier.

4) Adjust the receive path for proper signal levels, based on the lowest speech levels as well as the loudest. A gain of about 30 dB is required from Tip and Ring to the speaker terminals for most applications (at max. volume). Most of that gain should be in the receive amplifier (at RXI, RXO) so as to make best use of the receive attenuator, but make sure the max. attenuator input level at RXO is not exceeded. If a signal generator is used for signal injection during testing, the circuit can be locked into the receive mode by grounding CPR (Pin 10), although this is usually not necessary since the dial tone detector will keep the circuit in the receive mode. As an alternate, bits B7 and B6 can be set to 01. Frequency response can generally be tailored with capacitors at the receive amplifier.

5) Check that the loop gain (i.e., the receive path gain + acoustic coupling gain + transmit path gain + sidetone gain) is less than 0 dB over all frequencies. If not, "singing" will occur – a steady oscillation at some audible frequency.

6) a) The final step is to adjust the resistors at the level detector inputs (RLI and TLI) for proper switching response (the switchpoint occurs when $I_1 = I_2$). This has to be the last step

as the resistor values depend on all of the above adjustments, which are based on the mechanical, as well as the electrical, characteristics of the system. **NOTE:** An extreme case of level detector misadjustment can result in "motorboating". In this condition, with a receive signal applied, sound from the speaker enters the microphone, and causes the circuit to switch to the transmit mode. This causes the speaker sound to stop (as well as the sound into the microphone), allowing the circuit to switch back to the receive mode. This sequence is then repeated, usually, at a rate of a few Hz. The first thing to check is the acoustic coupling, and then the level detector input resistors.

b) Starting with the recommended values for R_1 and R_2 (in Figure 3), hold a normal conversation with someone on another phone. If the resistor values are not optimum, one of the talkers will dominate, and the other will have difficulty getting through. If, for example, the person at the speakerphone is dominant, the transmit path is overly sensitive, and the receive path is not sensitive enough. In this case, R_1 should be increased, or R_2 decreased, or both. Their exact value is not critical at this point, only their relative value. Keeping R_1 and R_2 in the range of 2.0–20 K, adjust them until a suitable switching response is obtained.

c) Then have the person at the other end of the phone line speak continuously loudly, or connect to a recording which is somewhat strong. Monitor the state of the circuit (by measuring the C_T versus V_B pins, and by listening carefully to the speaker) to check that the sound out of the speaker is not attempting to switch the circuit to the transmit side (through acoustic coupling). If it is, increase R_1 (at TLI) in small steps just enough to stop the switching (this de–sensitizes the transmit side). If R_1 has been changed a large amount, it may be necessary to readjust R_2. If this cannot be achieved in a reasonable manner, the acoustic coupling is too strong.

d) Then have the person at the speakerphone speak somewhat loudly, and again monitor the state of the circuit, primarily by having the person at the other end listen carefully for fading. If there is obvious fading of the sound, increase R_2 so as to de–sensitize the receive side. Increase R_2 just enough to stop the fading. If this cannot be achieved in a reasonable manner, the sidetone coupling is too strong.

e) If necessary, readjust R_1 and R_2, relative to each other, a small amount to further optimize the switching response.

Microprocessor Interface

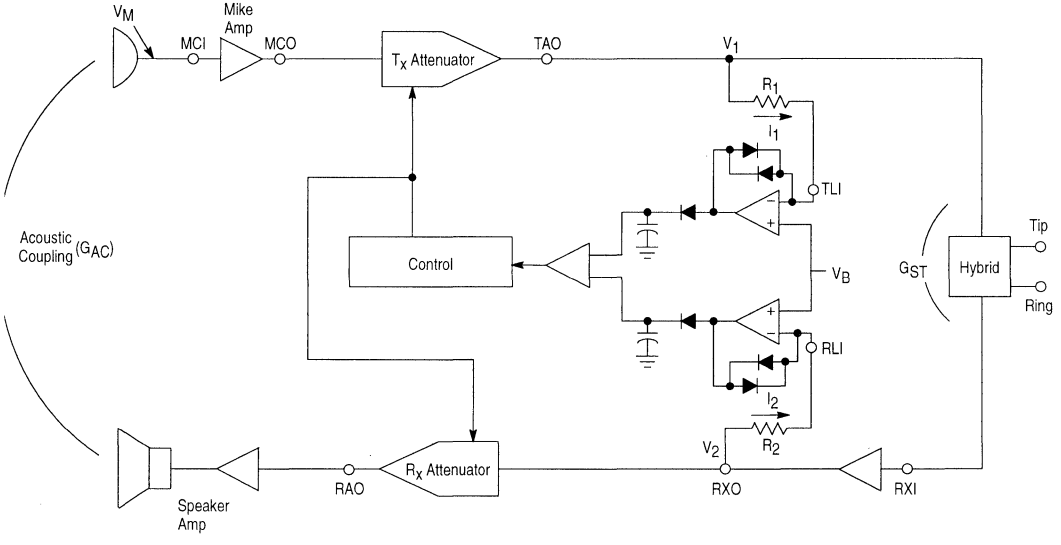
The microprocessor interface (Pins 17–19) can be controlled by any microprocessor with an SPI port, or from a general purpose port which can be configured to provide the correct signals. The MC33218A requires one 8–bit word to set the various parameters – there is no chip address, or other protocol or handshaking required. See Figure 2 for a timing diagram. The function of each of the bits is described in the Functional Description, as well as in a table near the beginning of this document. The pin's functions are as follows:

– DATA: Bit B7 is entered first, and B0 last, and each bit is entered on a clock rising edge. The minimum setup and hold times indicated in the Electrical Characteristics must be adhered to. If more than 8 bits are entered, the last 8 bits to be entered will be stored in the registers.

– CLOCK: The clock enters the data on each rising edge. There is no minimum required frequency, and the maximum frequency is 1.0 MHz. It is recommended that the clock be stopped when data is not being entered to minimize the possibility of creating audible noise in the speech paths. This input is disabled when Data Ready is high.

– DATA READY: This input must be held low while data is being entered, and then taken high to latch in the new data. The new data will not affect the MC33218A until Data Ready is taken high. It is recommended that Data Ready be kept high at all times except when entering data, although this is not required for the IC to function correctly.

Figure 35. Basic Block Diagram for Design Purposes



Upon powering up the MC33218A, or when the IC is disabled by means of the CD pin (Pin 8), the eight registers are internally set to a logic 0, regardless of their previous contents. This default condition corresponds to normal voice switched operation, 53 dB attenuator range, active microphone amplifier, and maximum receive volume level.

The amplitude of the three inputs must be less than 0.8 V for a logic 0, and between 2.0 V and V_{CC} for a logic 1. The three inputs must be kept within the range of V_{CC} and GND. If any input is taken more than 0.5 V above V_{CC} or below GND excessive currents will flow, and the device's operation will be distorted.

2

Power On Reset

The Power On Reset function sets the 8 internal registers to logic 0's whenever the MC33218A is powered up, or whenever the Chip Disable pin (Pin 8) is taken high. A capacitor on Pin 20 (POR) creates a time delay, allowing V_{CC} to stabilize before the registers can accept data. The effective resistance at this pin, for timing purposes, is ≈ 115 kΩ. A 0.1 µF capacitor, for example, provides a time delay of ≈ 3.7 ms (at V_{CC} = 5.0 V).

Alternately, Pin 20 can be driven directly from a logic source if desired, – the switching threshold is ≈ 1.2 V. When taken low, the registers are reset to 0, independent of the Clock or Data Ready position. The POR input must be kept within the range of V_{CC} and GND. If the input is taken more than 0.5 V above V_{CC} or below GND excessive currents will flow, and the device's operation will be distorted. See Figure 33 for the circuit configuration.

Transmit/Receive Detection Priority

Although the MC33218A was designed to have an idle mode such that the transmit side has a small priority (the idle mode position is closer to the full transmit side than the receive side), the idle mode position can be moved with respect to the transmit or the receive side. With this done, the ability to gain control of the circuit by each talker will be changed.

By connecting a resistor from C_T (Pin 7) to ground, the circuit will be biased more towards the transmit side. The resistor value is calculated from:

$$R = R_T \left[\frac{V_B}{\Delta V} - 1 \right]$$

where R is the added resistor, R_T is the resistor normally between Pins 6 and 7 (typically 15 kΩ), and ΔV is the desired change in the C_T voltage at idle. V_B is the voltage at Pin 6.

By connecting a resistor from C_T (Pin 7) to V_{CC}, the circuit will be biased towards the receive side. The resistor value is calculated from:

$$R = R_T \left[\frac{V_{CC} - V_B}{\Delta V} - 1 \right]$$

R, R_T, ΔV, and V_B are the same as above. Switching response and the switching time will be somewhat affected in each case due to the different voltage excursions required to get to transmit and receive from idle. For practical considerations, the ΔV shift should not exceed 50 mV.

Disabling the Idle Mode

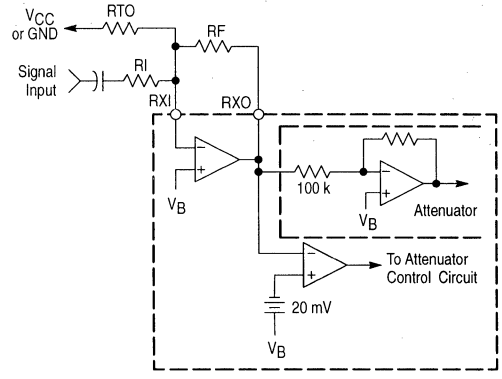
In order to test the gain, and performance, of the transmit path and the receive path, they can each be set to their full "on" positions using bits B7 and B6 of the serial port. However, if it is desired to tests these paths with the IC in the normal voice switched mode (B7, 6 = 00), the transmit or receive attenuator can be set to the "on" position, even with steady signals applied, by disabling the background noise monitors. Grounding the CPT pin will disable the transmit background noise monitor, causing the circuit to stay in the full transmit mode, even with a low level continuous signal applied to the transmit path. Grounding CPR does the same for the receive path. Additionally, the receive background noise monitor is automatically disabled by the dial tone detector whenever the receive signal exceeds that detector's threshold.

Dial Tone Detector Threshold

The threshold for the dial tone detector is internally set at ≈ 20 mV (14 mVrms) below V_B (see Figure 31). That threshold can be changed if desired by changing the DC bias level at RXO.

Since the attenuator input is DC coupled to the receive amplifier, the threshold is changed by forcing an offset through the receive amplifier. As shown in Figure 36, connect a resistor (RTO) from the summing node to either ground or V_{CC}, depending on whether the dial tone detector threshold is to be increased or decreased. RF and RI are the resistors normally used to set the receive audio gain.

Figure 36. Adjusting Dial Tone Detector Threshold



Adding RTO, and connecting it to ground will shift RXO up, thereby increasing the dial tone detector threshold. In this case, RTO is calculated from:

$$RTO = \frac{V_B \times RF}{\Delta V}$$

V_B is the voltage at Pin 6, and ΔV is the amount that the detector's threshold is to be increased. For example, if V_B = 2.2 V, RF = 10 K, and ΔV = 20 mV, RTO calculates to 1.1 MΩ.

Connecting RTO to V_{CC} will shift RXO down, thereby decreasing the dial tone detector threshold. In this case, RTO is calculated from:

$$RTO = \frac{(V_{CC} - V_B) \times RF}{\Delta V}$$

For example, if V_{CC} = 5.0 V, V_B = 2.2 V, RF = 10 K, and ΔV = 10 mV, RTO calculates to 2.8 MΩ.

Board Layout, RFI Interference

Although the MC33218A is meant to be used at audio frequencies, the various amplifiers within have bandwidths exceeding 1.0 MHz, and can therefore oscillate due to stray capacitance and other parasitics if care is not taken in the board layout. A PC board, with a ground plane, is recommended for breadboarding as well as production. Factors to keep in mind are:

– The heavy current draw in a speakerphone type product is in the speaker, and consequently, in the speaker amplifier. The power supply and ground connection to the speaker amplifier must be done with care so as to not create significant ripple, or ground noise, for the remaining circuitry.

– The power supply bypass for the MC33218A should be 100 μF if powered by a regulated power supply, and 1000 μF if powered by the phone line. The bypass capacitor must be physically close to the IC – preferably within one inch. This is particularly important in a circuit powered by the phone line. Oscillations, or instabilities, can result if this guideline is not followed.

– As with any circuit which involves mixing analog and digital circuitry, care must be taken in the layout to prevent digital noise from getting into the analog speech paths. As a general rule, all the analog circuitry (phone line interface, speech network, speakerphone, and speaker amplifier) should be "in its own area". Mixing of the analog and digital circuits can result in the high speed logic transitions creating frequencies in the audible range.

– Generally it is not necessary to have a separate analog and digital ground. With many mixed mode devices (such as the MC33218A), this is impractical since there is only one ground pin on the IC. The significant factors here are that the ground plane be continuous, the various circuit sections be arranged logically, and that the V_{CC} distribution be done so as to not distribute noise to the analog circuits.

– Potential radio frequency interference (RFI) problems should be addressed early in the electrical and mechanical design of the speakerphone. RFI may enter the circuit through Tip and Ring, through the microphone wiring to the microphone amplifier (this wiring should be short), or through any of the PC board traces. The most sensitive pins on the MC33218A are the inputs to the level detectors (RLI, TLI, XDI) since, when there is no speech present, the inputs are high impedance and these op amps are in a near open loop condition. The board traces to these pins should be kept short, and the resistor and capacitor for each of these pins should be physically close to the pins. All other input pins should also be considered sensitive to RFI signals.

In The Final Analysis ...

Proper operation of a speakerphone is a combination of proper mechanical (acoustic) design as well as proper electronic design. The acoustics of the enclosure must be considered early in the design of a speakerphone. In general, electronics cannot compensate for poor acoustics, low speaker quality, low microphone quality, or any combination of these items. Proper acoustic separation of the speaker and microphone is essential. The physical location of the microphone, along with the characteristics of the selected microphone, will play a large role in the quality of the transmitted sound. The microphone and speaker vendors can usually provide additional information on the use of their products.

In the final analysis, the circuit will have to be fine tuned to match the acoustics of the enclosure, the specific hybrid, and the specific speaker and microphone selected. The components shown in this data sheet should be considered as starting points only. The gains of the transmit and receive paths are easily adjusted at the microphone and receive amplifiers, respectively. The switching response can then be fine tuned by varying (in small steps) the components at the level detector inputs (TLI, RLI) until satisfactory operation is obtained for both long and short lines.

For additional information on speakerphone design please refer to The Bell System Technical Journal, Volume XXXIX (March 1960, No. 2).

DEFINITIONS

Attenuation – A decrease in magnitude of a communication signal, usually expressed in dB.

Bandwidth – The range of information carrying frequencies of a communication system.

Battery – The voltage which provides the loop current to the telephone from the CO. The name derives from the fact that COs have always used batteries, in conjunction with AC power, to provide this voltage.

C–Message Filter – A frequency weighting which evaluates the effects of noise on a typical subscriber's system.

Central Office – Abbreviated CO, it is a main telephone office, usually within of a few miles of its subscribers, that houses switching gear for interconnection within its exchange area, and to the rest of the telephone system. A CO can handle up to 10,000 subscriber numbers.

CO – See Central Office.

CODEC – Coder/Decoder – In the Central Office, it converts the transmit signal to digital, and converts the digital receive signal to analog.

dB – A power or voltage measurement unit, referred to another power or voltage. It is generally computed as:

$$10 \times \log (P_1/P_2)$$

for power measurements, and

$$20 \times \log (V_1/V_2)$$

for voltage measurements.

dBm – An indication of signal power. 1.0 mW across 600 Ω, or 0.775 Vrms, is defined as 0 dBm. Any other voltage level is converted to dBm by:

$$dBm = 20 \times \log (Vrms/0.775), \text{ or}$$
$$dBm = [20 \times \log (Vrms)] + 2.22.$$

dBmp – Indicates dBm measurement using a psophometric weighting filter.

dBrn – Indicates a dBm measurement relative to 1.0 pW power level into 600 Ω. Generally used for noise measurements, 0 dBrn = –90 dBm.

dBrnC – Indicates a dBrn measurement using a C–message weighting filter.

DTMF – Dual Tone MultiFrequency. It is the "tone dialing" system based on outputting two non–harmonic related frequencies simultaneously to identify the number dialed. Eight frequencies have been assigned to the four rows and four columns of a keypad.

Four Wire Circuit – The portion of a telephone, or central office, which operates on two pairs of wires. One pair is for the Transmit path, and one pair is for the Receive path.

Full Duplex – A transmission system which permits communication in both directions simultaneously. The standard handset telephone system is full duplex.

Gain – The change in signal amplitude (increase or decrease) after passing through an amplifier, or other circuit stage. Usually expressed in dB, an increase is a positive number, and a decrease is a negative number.

Half Duplex – A transmission system which permits communication in one direction at a time. CB radios, with "push–to–talk" switches, and voice activated speakerphones, are half duplex.

Hookswitch – A switch, within the telephone, which connects the telephone circuit to the subscriber loop. The name derives from old telephones where the switch was activated by lifting the receiver off and onto a hook on the side of the phone.

Hybrid – A two–to–four wire converter.

Idle Channel Noise – Residual background noise when transmit and receive signals are absent.

Line Card – The pc board, and circuitry, in the CO or PBX which connects to the subscriber's phone line. A line card may hold circuitry for one subscriber, or a number of subscribers.

Longitudinal Balance – The ability of the telephone circuit to reject longitudinal signals on Tip and Ring.

Longitudinal Signals – Common mode signals.

Loop – The loop formed by the two subscriber wires (Tip and Ring) connected to the telephone at one end, and the central office (or PBX) at the other end. Generally it is a floating system, not referred to ground, or AC power.

Loop Current – The DC current which flows through the subscriber loop. It is typically provided by the central office or PBX, and ranges from 20–120 mA.

Mute – Reducing the level of an audio signal, generally so that it is inaudible. Partial muting is used in some applications.

Off Hook – The condition when the telephone is connected to the phone system, permitting the loop current to flow. The central office detects the DC current as an indication that the phone is busy.

On Hook – The condition when the telephone is disconnected from the phone system, and no DC loop current flows. The central office regards an on hook phone as available for ringing.

PABX – Private Automatic Branch Exchange. In effect, a miniature central office, it is a customer owned switching system servicing the phones within a facility, such as an office building. A portion of the PABX connects to the Bell (or other local) telephone system.

Power Supply Rejection Ratio – The ability of a circuit to reject outputting noise, or ripple, which is present on the power supply lines. PSRR is usually expressed in dB.

Protection, Primary – Usually consisting of carbon blocks or gas discharge tubes, it absorbs the bulk of a lightning induced transient on the phone line by clamping the voltages to less than ±1500 V.

Protection, Secondary – Usually located within the telephone, it protects the phone circuit from transient surges. Typically, it must be capable of clamping a ±1.5 kV surge of 1.0 ms duration.

Pulse Dialing – A dialing system whereby the loop current is interrupted a number of times in quick succession. The number of interruptions corresponds to the number dialed, and the interruption rate is typically 10 per second. The old rotary phones, and many new pushbutton phones, use pulse dialing.

Receive Path – Within the telephone it is the speech path from the phone line (Tip and Ring) towards the receiver or speaker.

REN – Ringer Equivalence Number. An indication of the impedance, or loading factor, of a telephone bell or ringer circuit. An REN of 1.0 equals ≈ 8.0 kΩ. The Bell system typically permits a maximum of 5.0 REN (1.6 kΩ) on an individual subscriber line. A minimum REN of 0.2 (40 kΩ) is required by the Bell system.

Return Loss – Expressed in dB, it is a measure of how well the telephone's AC impedance matches the line's AC characteristic impedance. With a perfect match, there is no reflected signal, and therefore infinite return loss. It is calculated from:

$$RL = 20 \times \log \frac{(Z_{LINE} + Z_{CKT})}{(Z_{LINE} - Z_{CKT})}$$

Ring – One of the two wires connecting the central office to a telephone. The name derives from the ring portion of the plugs used by operators (in older equipment) to make the connection. Ring is traditionally negative with respect to Tip.

SPI – Serial Port Interface. A three line microprocessor interface port which is used to clock in data serially. The three lines are clock, data, and a control line which enables entry of the data. Some serial ports are bidirectional.

Sidetone Rejection – The rejection (in dB) of the reflected signal in the receive path resulting from a transmit signal applied to the phone, and phone line.

SLIC – Subscriber Line Interface Circuit. It is the circuitry within the CO or PBX which connects to the user's phone line.

Subscriber – The customer at the telephone end of the line.

Subscriber Line – The system consisting of the user's telephone, the interconnecting wires, and the central office equipment dedicated to that subscriber (also referred to as a loop).

Tip – One of the two wires connecting the central office to a telephone. The name derives from the tip of the plugs used by operators (in older equipment) to make the connection. Tip is traditionally positive with respect to Ring.

Transmit Path – Within the telephone it is the speech path from the microphone towards the phone line (Tip and Ring).

Two Wire Circuit – Refers to the two wires connecting the central office to the subscriber's telephone. Commonly referred to as Tip and Ring, the two wires carry both transmit and receive signals in a differential manner.

Two–to–Four Wire Converter – A circuit which has four wires (on one side) – two (signal and ground) for the outgoing signal, and two for the incoming signal. The outgoing signal is sent out differentially on the two wire side, and incoming differential signals received on the two wire side are directed to the receive path of the four wire side. Additional circuit within cancels the reflected outgoing signal to keep it separate from the incoming signal.

Voiceband – That portion of the audio frequency range used for transmission across the telephone system. Typically it is 300–3400 Hz.

2

Suggested Vendors

Microphones

Primo Microphones Inc.
Bensenville, IL 60106
1–800–76–PRIMO

Telecom Transformers

Microtran Co., Inc.
Valley Stream, NY 11528
516–561–6050
(Ask for Application Bulletin F232)

Stancor Products
Logansport, IN 46947
219–722–2244

PREM Magnetics, Inc.
McHenry, IL 60050
815–385–2700

Motorola does not endorse or warrant the suppliers referenced.

MC33219A

Voice Switched Speakerphone

VOICE SWITCHED SPEAKERPHONE CIRCUIT

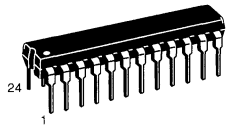
SEMICONDUCTOR TECHNICAL DATA

The Motorola MC33219A Voice Switched Speakerphone Circuit incorporates the necessary amplifiers, attenuators, level detectors, and control algorithm to form the heart of a high quality hands–free speakerphone system. Included are a microphone amplifier with mute, transmit and receive attenuators, a background monitoring system for both the transmit and receive paths, and level detectors for each path. An AGC system reduces the receive gain on long lines where loop current and power are in short supply. A dial tone detector prevents fading of dial tone. A Chip Disable pin permits conserving power when the circuit is not in use. The volume control can be implemented with a potentiometer.

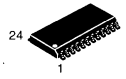
The MC33219A can be operated from a power supply, or from the telephone line, requiring typically 3.2 mA. It can be used in conjunction with a variety of speech networks. Applications include not only speakerphones, but intercoms and other voice switched devices.

The MC33219A is available in a 24 pin narrow body DIP, and a wide body SOIC package.

- Supply Voltage Range: 2.7 to 6.5 V
- Attenuator Range: 53 dB
- Background Noise Monitor for Each Path
- 2 Point Signal Sensing
- Volume Control Range: Typically 40 dB
- Microphone and Receive Amplifiers Pinned Out for Flexibility
- Microphone Amplifier can be Muted
- Mute and Chip Disable are Logic Level Inputs
- Chip Deselect Pin Powers Down the Entire IC
- Ambient Operating Temperature: −40 to +85°C
- 24 Pin Narrow Body (300 mil) DIP and 24 Pin SOIC

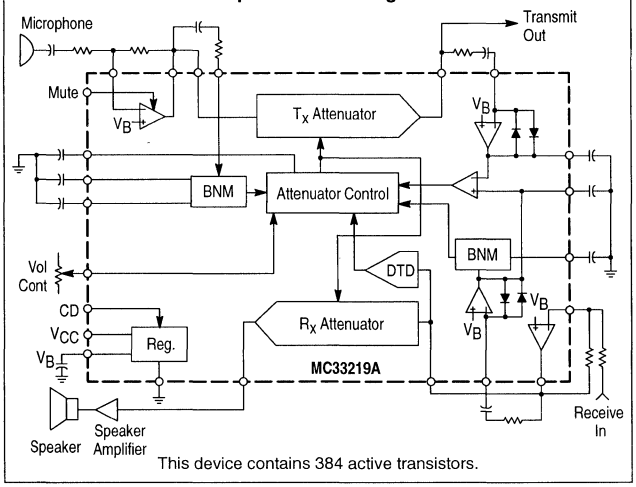


P SUFFIX
PLASTIC PACKAGE
CASE 724



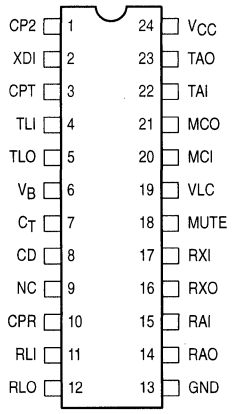
DW SUFFIX
PLASTIC PACKAGE
CASE 751E

Simplified Block Diagram



This device contains 384 active transistors.

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC33219ADW	$T_A = -40°$ to +85°C	SOIC
MC33219AP		Plastic DIP

MAXIMUM RATINGS

Rating	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	−0.5	7.0	Vdc
Any Input	V_{in}	−0.4	V_{CC} + 0.4	Vdc
Maximum Junction Temperature	T_J	–	+150	°C
Storage Temperature Range	T_{stg}	−65	+150	°C

NOTE: Devices should not be operated at or outside these values. The "Recommended Operating Conditions" provide for actual device operation.

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Voltage (Non–AGC Range) (AGC Range)	V_{CC}	3.5 2.7	– –	6.5 3.5	Vdc
Maximum Attenuator Input Signal	$V_{in(max)}$	–	–	300	mVrms
Volume Control Input (Pin 19)	V_{INVLC}	V_B – 1.1	–	V_B	Vdc
Logic Input Voltage (Pins 8, 18) Low High	V_{INL}	 0 2.0	 – –	 0.8 V_{CC}	Vdc
Operating Temperature Range	T_A	−40	–	85	°C
V_B Output Current (V_{CC} = 5.0 V)	I_{VB}	–	See Figure 12	–	mA

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 V, CD ≤ 0.8 V, unless noted. See Figure 2.)

Characteristic	Symbol	Min	Typ	Max	Unit
POWER SUPPLY					
Supply Current (Enabled, CD ≤ 0.8, V_B Open) Idle Mode T_x Mode R_x Mode	I_{CCE}	 2.0 – –	 3.2 4.2 4.0	 5.0 – –	mA
Supply Current (Disabled, CD = 2.0 V, V_B Open) V_{CC} = 3.0 V V_{CC} = 5.0 V V_{CC} = 6.5 V	I_{CCD}	 – 50 –	 65 110 145	 – 170 –	µA
V_B Output Voltage (I_{VB} = 0, CD = 0) V_{CC} = 2.7 V V_{CC} = 5.0 V V_{CC} = 6.5 V	V_B	 – 2.1 –	 0.9 2.2 3.0	 – 2.3 –	Vdc
V_B Output Resistance (I_{VB} ≤ −1.0 mA)	R_{OVB}	–	600	–	Ω
PSRR @ V_B versus V_{CC}, f = 1.0 kHz, C_{VB} = 100 µF	PSRR	–	57	–	dB
ATTENUATOR CONTROL					
C_T Voltage (with Respect to V_B) R_x Mode (VLC = V_B) Idle Mode T_x Mode	$V_{CT} - V_B$	 – – –	 150 0 −100	 – – –	mV
C_T Source Current (Switching to R_x Mode)	I_{CTR}	−110	−90	−70	µA
C_T Sink Current (Switching to T_x Mode)	I_{CTT}	35	50	65	µA
C_T Idle Current	I_{CTI}	−3.0	0	3.0	µA
Dial Tone Detector Threshold (with Respect to V_B at RAI)	V_{DT}	−40	−20	−8.0	mV
VLC Input Current @ VLC = V_B VLC = V_B – 1.0 V	I_{VLC}	 – −8.0	 0 −6.0	 – −3.0	µA
VLC Input Resistance	R_{VLC}	–	167	–	kΩ

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 V, CD ≤ 0.8 V, unless noted. See Figure 2.)

Characteristic	Symbol	Min	Typ	Max	Unit
ATTENUATORS					
Receive Attenuator Gain (f = 1.0 kHz)					dB
Full Volume					
R_X Mode	G_{RX}	3.0	6.7	9.0	
T_X Mode	G_{RXT}	−49	−46	−43	
Idle Mode	G_{RXI}	−28	−25	−22	
Range (R_X to T_X Mode)	ΔG_{RX}	50	53	56	
Volume Control Range (R_X Mode Only, VLC Varied from V_B to (V_B − 1.0 V))	V_{CR}	34	40	46	dB
AGC Attenuation Range (V_{CC} = 3.5 to 2.7 V, Receive Mode Only, VLC = V_B)	G_{AGC}	20	26	36	dB
Transmit Attenuator Gain (f = 1.0 kHz)					dB
T_X Mode	G_{TX}	3.0	6.7	9.0	
R_X Mode	G_{TXR}	−49	−46	−43	
Idle Mode	G_{TXI}	−19	−16	−13	
Range (T_X to R_X Mode)	ΔG_{TX}	50	53	56	
RAO, TAO Output Current Capability	I_{OATT}				mA peak
V_{CC} ≥ 3.0 V		–	2.5	–	
V_{CC} < 3.0 V		–	0.7	–	
RAO Offset Voltage with Respect to V_B	V_{RAO}				mVdc
R_X Mode		–	120	–	
Idle Mode		–	0	–	
T_X Mode		–	−10	–	
TAO Offset Voltage with Respect to V_B	V_{TAO}				mVdc
R_X Mode		–	0	–	
Idle Mode		–	−8.0	–	
T_X Mode		–	70	–	
RAI, TAI Input Impedance (V_{in} < 300 mVrms)	R_{INATT}	–	100	–	kΩ
RAI, TAI Input Offset Voltage with Respect to V_B	V_{INATT}	–	0	–	mVdc
MICROPHONE AMPLIFIER (Pins 20, 21)					
Output Offset with Respect to V_B (RF = 300 kΩ)	MCO_{VOS}	–	−9.0	–	mVdc
Input Bias Current (Pin 20)	I_{MBIAS}	–	−30	–	nA
Open Loop Gain (f < 100 Hz)	V_{VOLM}	–	70	–	dB
Gain Bandwidth	GBW_M	–	1.5	–	MHz
Maximum Output Voltage Swing (1% THD)	V_{OMAX}	–	4.1	–	Vp–p
Maximum Output Current Capability	I_{OMCO}	–	2.0	–	mA peak
Muting (Δ Gain) –	GMT				dB
RF = 300 kΩ		70	78	–	
RF = 100 kΩ		–	68	–	
RECEIVE AMPLIFIER (Pins 16, 17)					
Output Offset with Respect to V_B (RF = 10 kΩ)	RXO_{VOS}	–	−1.0	–	mVdc
Input Bias Current (Pin 17)	I_{RBIAS}	–	−30	–	nA
Open Loop Gain (f < 100 Hz)	A_{VOLR}	–	70	–	dB
Gain Bandwidth	G_{BWR}	–	1.5	–	MHz
Maximum Output Voltage Swing (1% THD)	V_{OMAX}	–	4.1	–	Vp–p
Maximum Output Current Capability	I_{ORXO}	–	2.0	–	mA peak

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 V, CD ≤ 0.8 V, unless noted. See Figure 2)

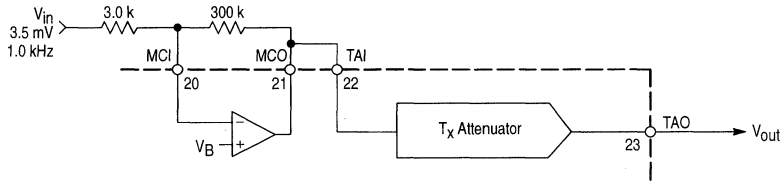
Characteristic	Symbol	Min	Typ	Max	Unit
LEVEL DETECTORS AND BACKGROUND NOISE MONITORS					
T_X–R_X Switching Threshold (Pins 4, 11)	I_{TH}	0.8	1.0	1.2	µA
CPR, CPT Output Resistance (for Pulldown)	R_{CP}	–	5.0	–	Ω
CPR, CPT Leakage Current	I_{CPLK}	–	–0.2	–	µA
CPR, CPT Nominal DC Voltage (No Signal)	V_{CP}	–	1.9	–	Vdc
TLO, RLO, CP2 Source Current (@ V_B – 1.0 V)	I_{LDOH}	–	–2.0	–	mA
TLO, RLO, CP2 Output Resistance	R_{LD}	–	500	–	Ω
TLO, RLO, CP2 Sink Current (@ V_B + 1.0 V)	I_{LDOL}	–	2.0	–	µA
MUTE INPUT (Pin 18)					
Switching Threshold (See Text)	V_{THMT}	–	1.0–1.4	–	Vdc
Input Resistance (V_{in} = 0.85 V)	R_{MT}	70	115	160	kΩ
Input Current (V_{in} = 5.0 V)	I_{MT}	–	75	–	µA
Timing To Mute To Enable	 t_{MT} t_{ENM}	 – –	 1.5 5.0	 – –	µs
CD INPUT (Pin 8)					
Switching Threshold	V_{THCD}	–	1.5	–	Vdc
Input Resistance (V_{in} = 0.8 V)	R_{CD}	150	235	350	kΩ
Input Current (V_{in} = 5.0 V)	I_{CD}	–	40	–	µA
Timing To Disable To Enable	 t_{CD} t_{ENC}	 – –	 5.0 See Figure 22	 – –	µs
SYSTEM DISTORTION (See Figure 1)					
Microphone Amplifier + T_X Attenuator Distortion	THD_T	–	0.05	3.0	%
Receive Amplifier + R_X Attenuator Distortion	THD_R	–	0.05	3.0	%

TYPICAL TEMPERATURE PERFORMANCE

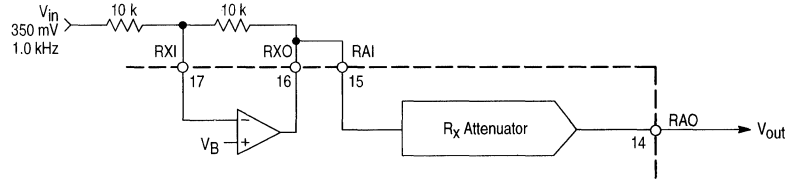
Characteristic	–40°C	0°C	25°C	85°C	Unit
Power Supply Current Enabled, V_B Open Disabled, V_B Open	 3.18 131	 3.23 119	 3.23 110	 3.12 121	 mA µA
V_B Output Voltage (I_{VB} = 0)	2.09	2.17	2.22	2.31	Vdc
CT Source Current Switching to R_X Mode	–80	–87	–90	–90	µA
CT Sink Current Switching to T_X Mode	43	47	50	51	µA
Attenuator "On" Gain	6.9	6.8	6.7	6.6	dB
Attenuator Range	53	53	53	53	dB
Volume Control Range (R_X Mode Only, V_{LC} Varied from V_B to (V_B – 1.0 V))	36	39	40	41	dB
AGC Attenuation Range	32	24	26	30	dB

Temperature data is typical performance only, based on sample characterization, and does not provide guaranteed limits over temperature.

Figure 1. System Distortion Test



NOTE: T_X Attenuator forced to transmit mode.

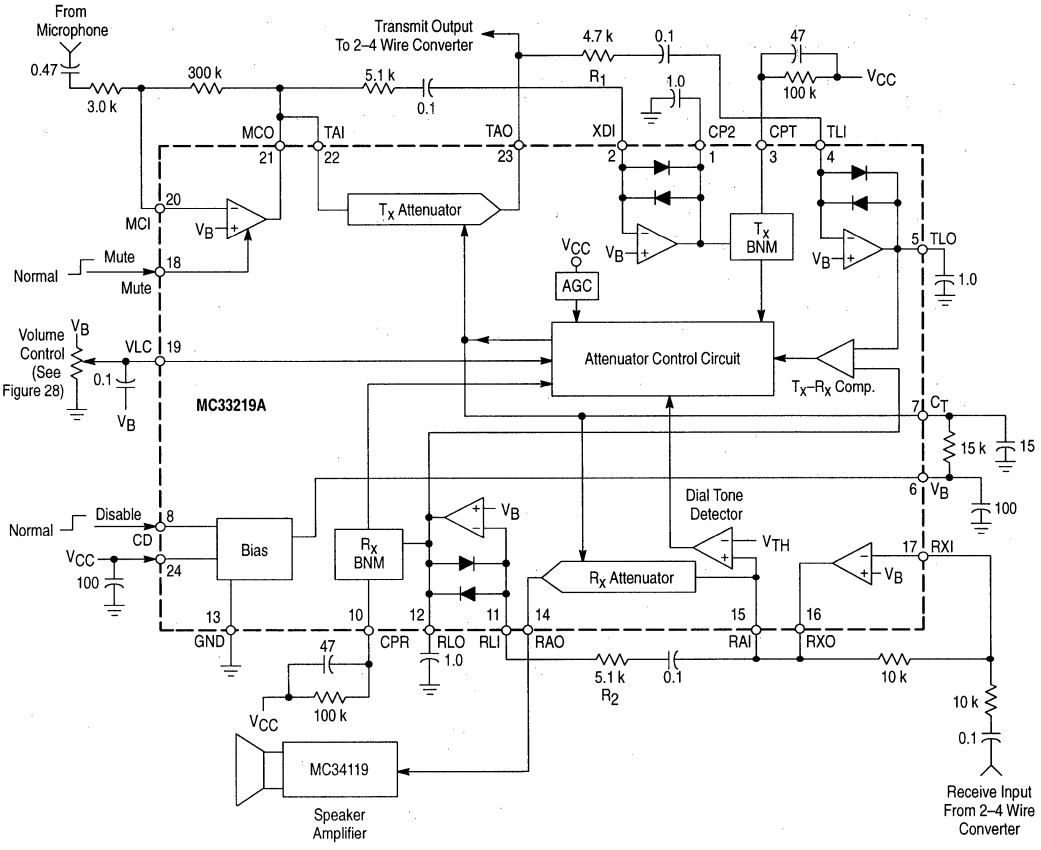


NOTE: R_X Attenuator forced to receive mode.

PIN FUNCTION DESCRIPTION

Pin	Symbol	Description
1	CP2	A capacitor at this pin stores voltage representing the transmit background noise and speech levels for the background noise monitor.
2	XDI	Input to the transmit background noise monitor.
3	CPT	An RC sets the time constant for the transmit background noise monitor.
4	TLI	Input to the transmit level detector.
5	TLO	Output of the transmit level detector.
6	V_B	A mid–supply reference voltage, and analog ground for the amplifiers. This must be well bypassed for proper power supply rejection.
7	C_T	An RC sets the switching time between transmit, receive and idle modes.
8	CD	Chip Disable (Logic Input). When low, the IC is active. When high, the entire IC is powered down and non–functional, except for V_B. Input impedance is nominally 125 kΩ.
9	NC	No internal connection.
10	CPR	An RC sets the time constant for the receive background noise monitor.
11	RLI	Input to the receive level detector.
12	RLO	Output of the receive level detector.
13	GND	Ground pin for the entire IC.
14	RAO	Output of the receive attenuator.
15	RAI	Input to the receive attenuator and the dial tone detector. Input impedance is nominally 100 kΩ.
16	RXO	Output of the receive amplifier.
17	RXI	Inverting input of the receive amplifier. Bias current flows out of the pin.
18	MUTE	Mute Input (Logic Input). A logic low sets normal operation. A logic high mutes the microphone amplifier only. Input impedance is nominally 67 kΩ.
19	VLC	Volume control. When VLC = V_B, maximum receive gain is set when in the receive mode. When VLC = V_B – 1.0 V, receive gain is down ≈ 40 dB. No effect in the transmit or idle mode. Current flow is out of the pin. Input impedance is nominally 167 kΩ.
20	MCI	Inverting input of the microphone amplifier. Bias current flows out of the pin.
21	MCO	Output of the microphone amplifier.
22	TAI	Input of the transmit attenuator. Input impedance is nominally 100 kΩ.
23	TAO	Output of the transmit attenuator.
24	V_{CC}	Power Supply Pin. Operating Range is 2.7 V to 6.5 Vdc. Bypassing is required.

Figure 2. MC33219A Block Diagram and Test Circuit



NOTES: 1. All capacitors are in μF unless otherwise noted.
2. Values shown are suggested initial values only. See Applications Information for circuit adjustments.

Figure 3. Attenuator Gain versus V_{CT} (Pin 7)

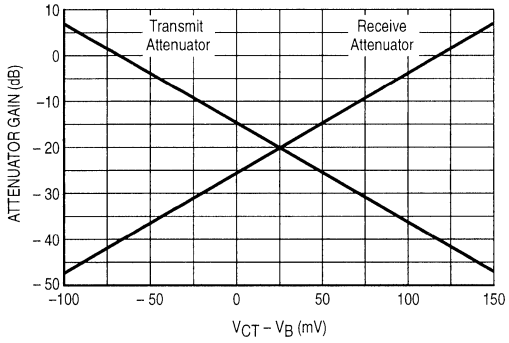


Figure 4. Receive Attenuator versus Volume Control

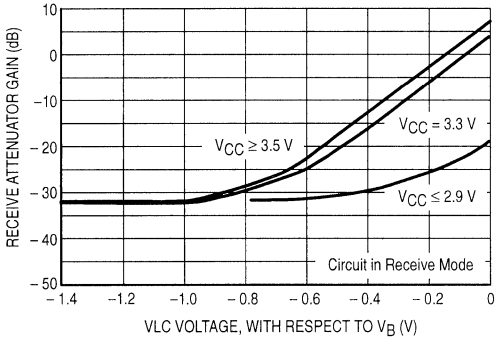


Figure 5. Receive Gain versus V_{CC}

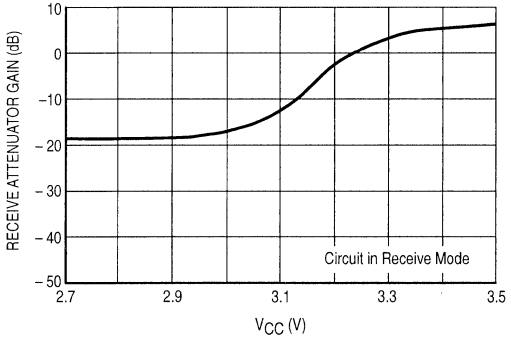


Figure 6. Level Detector DC Transfer Characteristics

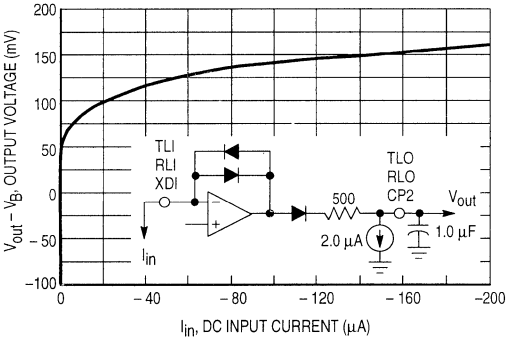


Figure 7. Level Detector AC Transfer Characteristics

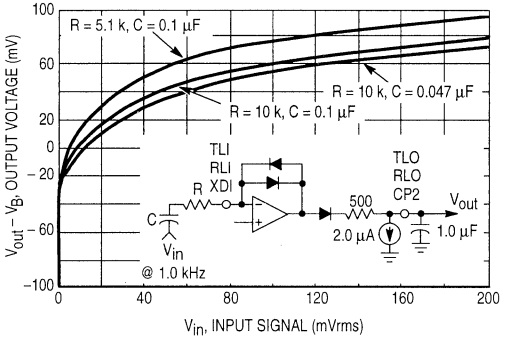


Figure 8. Level Detector AC Transfer Characteristics versus Frequency

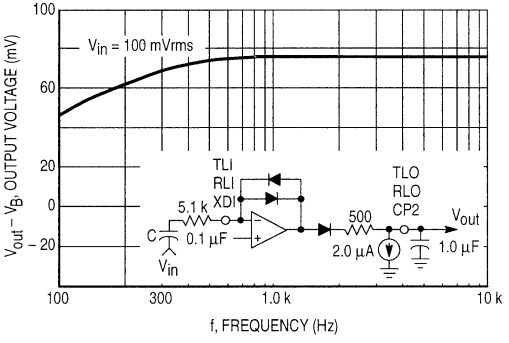


Figure 9. CD Input Characteristics (Pin 8)

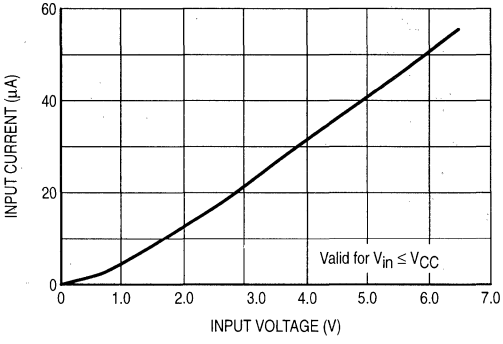


Figure 10. Mute Input Characteristics (Pin 18)

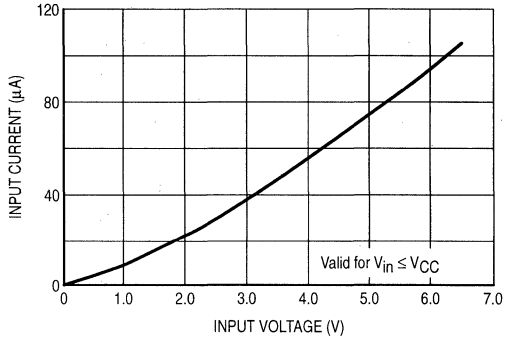


Figure 11. Power Supply Current

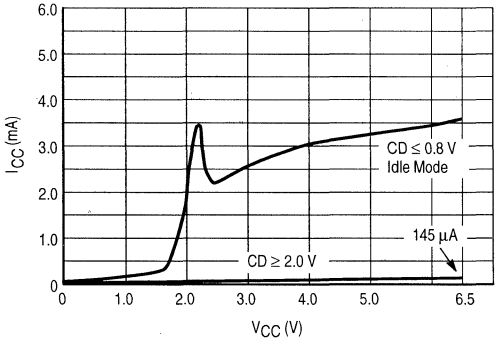


Figure 12. V_B Output Characteristics

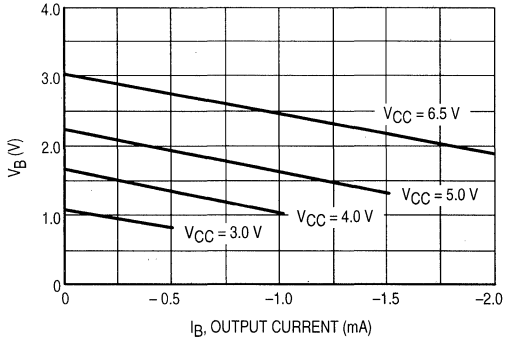


Figure 13. V_B Power Supply Rejection versus Frequency and V_B Capacitor

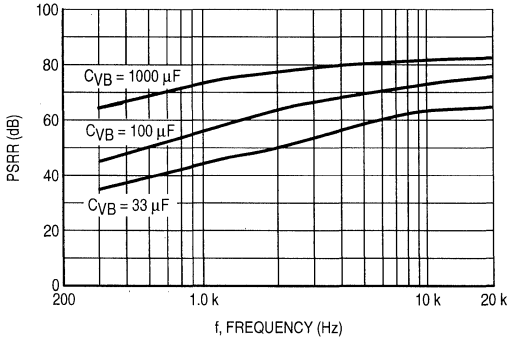


Figure 14. Receive Amp and Microphone Amp Output Swing

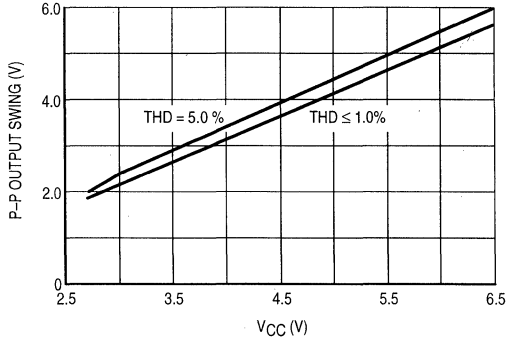


Figure 15. Microphone Amplifier Muting versus Feedback Resistor

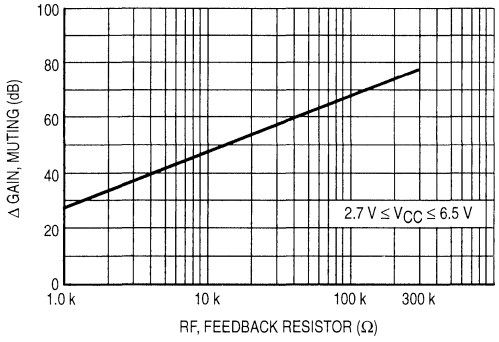
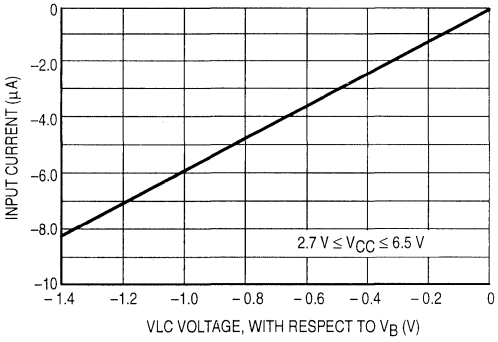
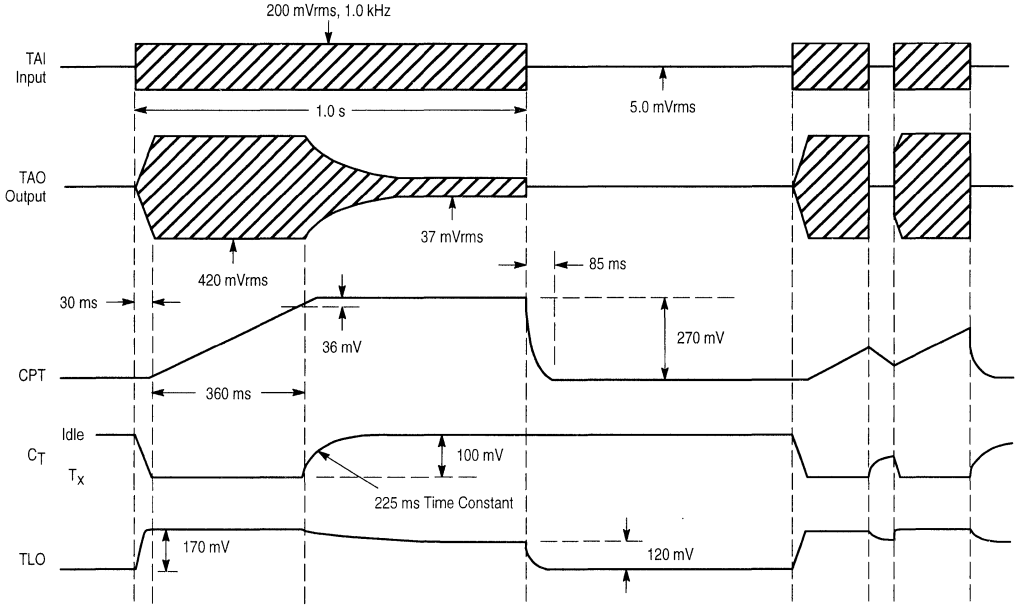


Figure 16. VLC Input Current (Pin 19)



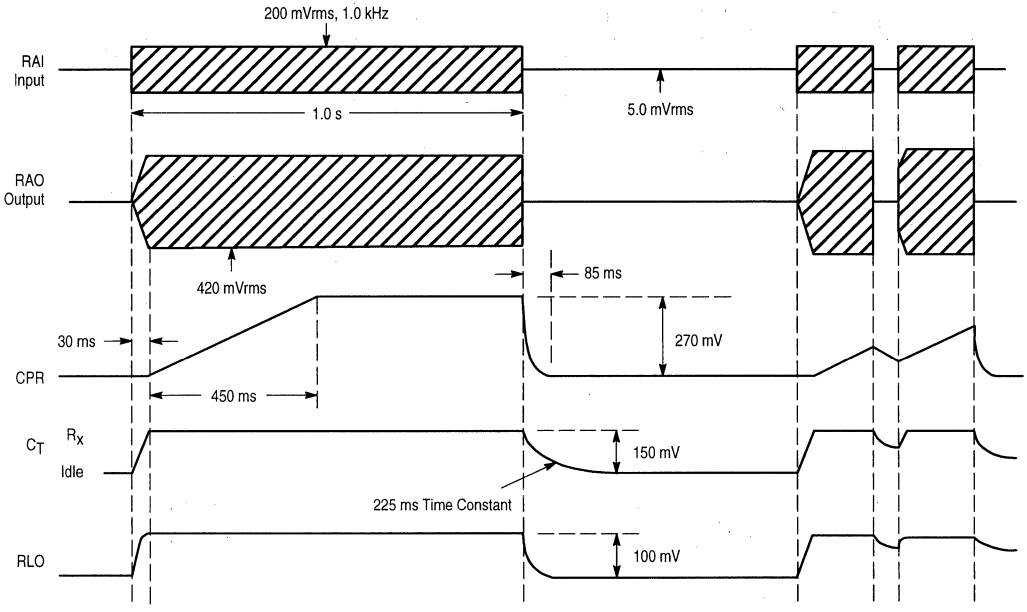
2

Figure 17. Idle ◄——► Transmit Timing



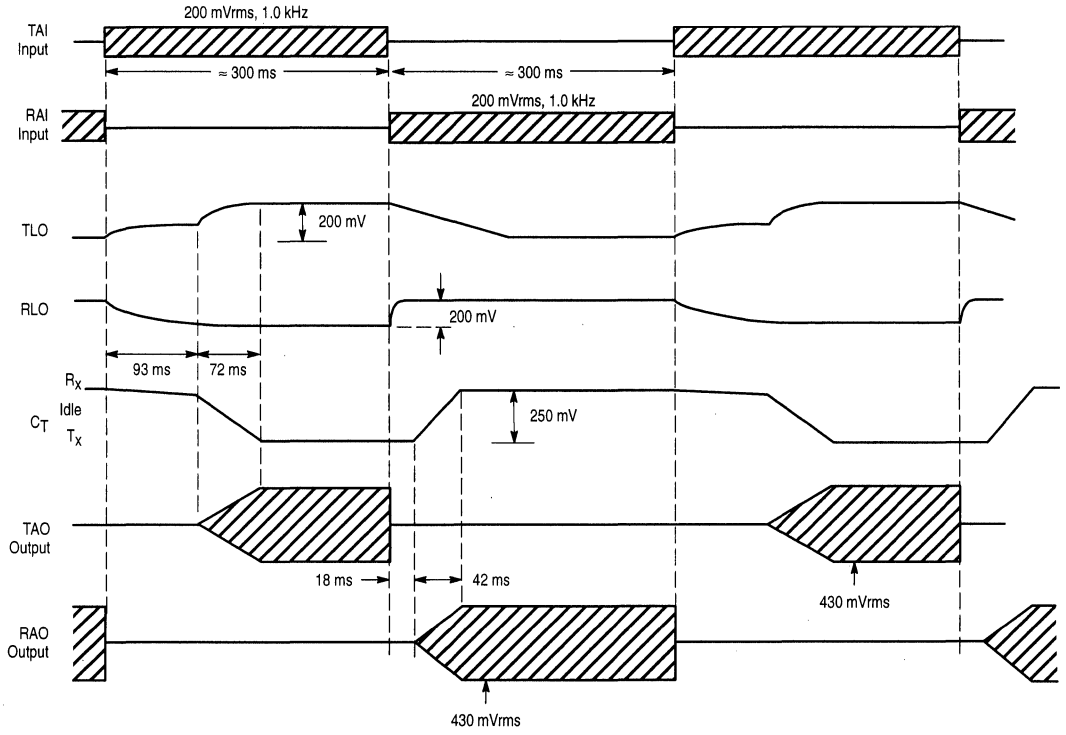
NOTE: Refer to Figure 2 for component values. Timing and output amplitudes shown are nominal, and are for the indicated input signal and component values. Actual timing and outputs will vary with the application.

Figure 18. Idle ⟷ Receive Timing



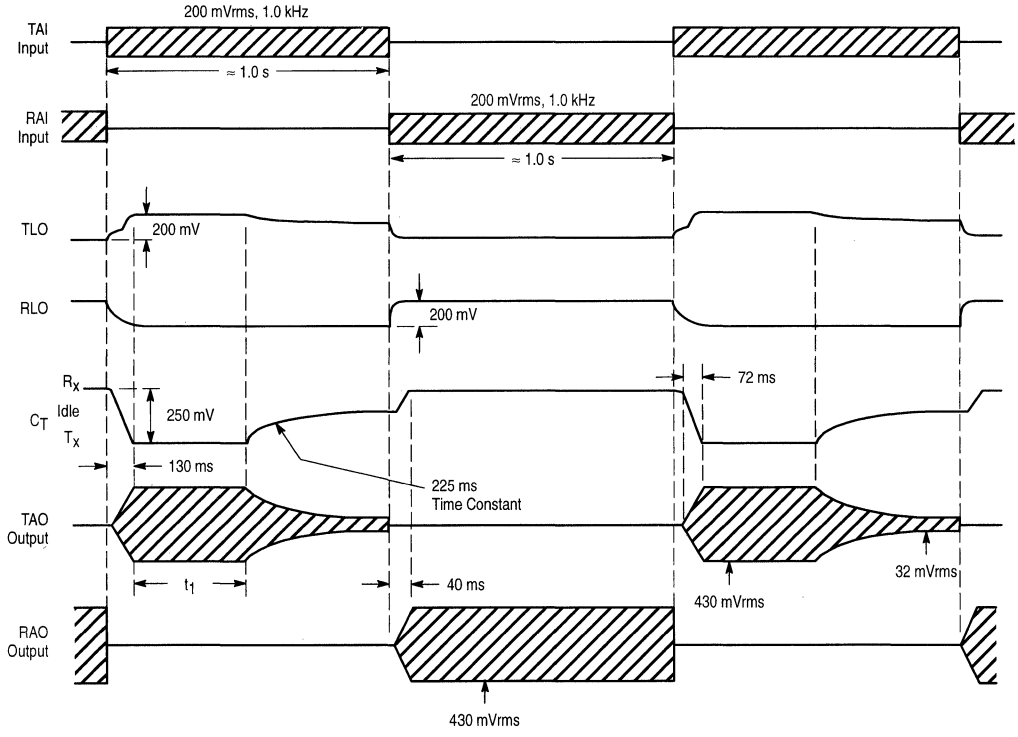
NOTE: Refer to Figure 2 for component values. Timing and output amplitudes shown are nominal, and are for the indicated input signal and component values. Actual timing and outputs will vary with the application.

Figure 19. Transmit ◄——► Receive Timing (Short Cycle Timing)



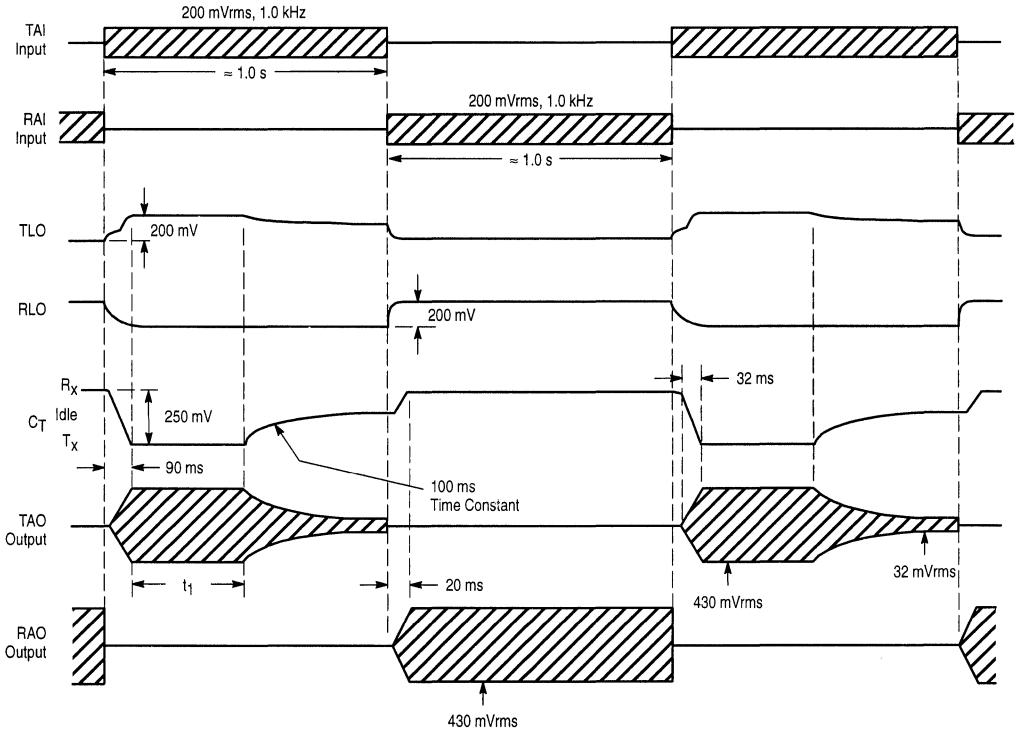
NOTE: 1. External component values are those shown in Figure 2.
2. Timing and output amplitudes shown are nominal, and are for the indicated input signal and component values. Actual timing and outputs will vary with the application.

Figure 20. Transmit ◄——► Receive Timing (Long Cycle Timing)



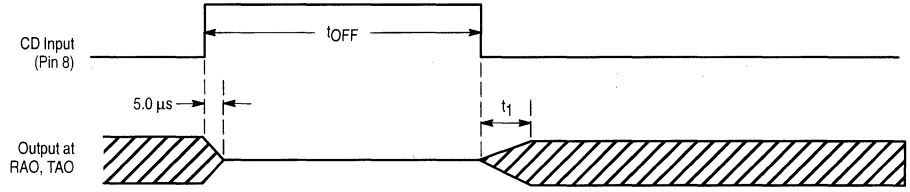
NOTE: 1. External component values are those shown in Figure 2.
2. Timing and output amplitudes shown are nominal, and are for the indicated input signal and component values. Actual timing and outputs will vary with the application.
3. Time t_1 depends on the ratio of the on–off amplitude of the signal at TAI.

Figure 21. Transmit ⟷ Receive Timing (Long Cycle Timing)



NOTE: 1. External component values are those shown in Figure 2, except the capacitor at C_T is 6.8 μF.
2. Timing and output amplitudes shown are nominal, and are for the indicated input signal and component values. Actual timing and outputs will vary with the application.
3. Time t_1 depends on the ratio of the on–off amplitude of the signal at TAI.

Figure 22. Chip Disable Timing

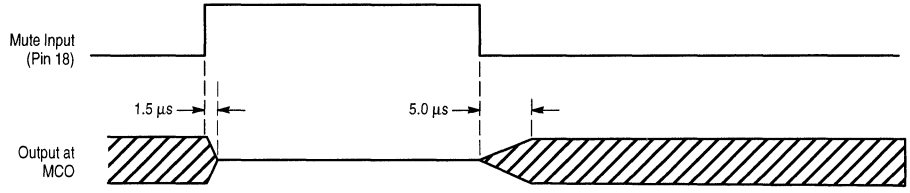


2

NOTE: Enable time t_1 depends on the length of t_{OFF} according to the following chart:

	t_1	
t_{OFF}	to 60%	to 100%
≤ 50 ms	–	5.0 µs
100 ms	5.0 µs	14 ms
500 ms	64 ms	72 ms
5.0 s	80 ms	100 ms

Figure 23. Mute Timing



FUNCTIONAL DESCRIPTION

Introduction

The fundamental difference between the operation of a speakerphone and a telephone handset is that of half–duplex versus full–duplex. The handset is full duplex, meaning conversation can occur in both directions (transmit and receive) simultaneously. This is possible due to both the low sound level at the receiver, and the fact that the acoustic coupling from the earpiece to the mouthpiece is almost non–existent (the receiver is normally held against a person's ear). The loop gain from the receiver to the microphone and through the circuit is well below that needed to sustain oscillations.

A speakerphone, on the other hand, has higher gain levels in both the transmit and receive paths, and attempting to converse full duplex results in oscillatory problems due to the loop that exists within the speakerphone circuit. The loop is formed by the hybrid, the acoustic coupling (speaker to microphone), and the transmit and receive paths (between the hybrid and the speaker/microphone). The only practical and economical method used to date is to design the speakerphone to function in a half duplex mode; i.e., only one person speaks at a time, while the other listens. To achieve this requires a circuit which can detect who is talking (in reality, who is talking louder), switch on the appropriate path (transmit or receive), and switch off (attenuate) the other path. In this way, the loop gain is maintained less than unity. When the talkers exchange function, the circuit must quickly detect this, and switch the circuit appropriately. By providing speech level detectors, the circuit operates in a "hands–free" mode, eliminating the need for a "push–to–talk" switch.

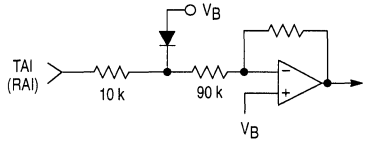
The MC33219A provides the necessary circuitry to perform a voice switched, half duplex, speakerphone function. The IC includes transmit and receive attenuators, pre–amplifiers, level detectors and background noise monitors for each path. An attenuator control circuit automatically adjusts the gain of the transmit and receive attenuators based on the relative strengths of the voice signals present, the volume control, and the supply voltage (when low). The detection sensitivity and timing are externally controllable. Please refer to the Block Diagram (Figure 2) when reading the following sections.

Transmit and Receive Attenuators

The transmit and receive attenuators are complementary, performing a log–antilog function. When one is at maximum gain (≈ 6.7 dB), the other is at maximum attenuation (≈ –46 dB); they are never both fully on or fully off. Both attenuators are controlled by a single output from the Attenuator Control Circuit which ensures the sum of their gains will remain constant at a typical value of –40 dB. Their purpose is to provide the half–duplex operation required in a speakerphone.

The attenuators are non–inverting, and have a usable bandwidth of 50 kHz. The input impedance of each attenuator (TXI and RXI) is nominally 100 kΩ (see Figure 24), and the input signal should be limited to 300 mVrms (850 mV p–p) to prevent distortion. That maximum recommended input signal is independent of the volume control setting. Both the input and output are biased at ≈ V_B. The output impedance is <10 Ω until the output current limit (see specs) is reached.

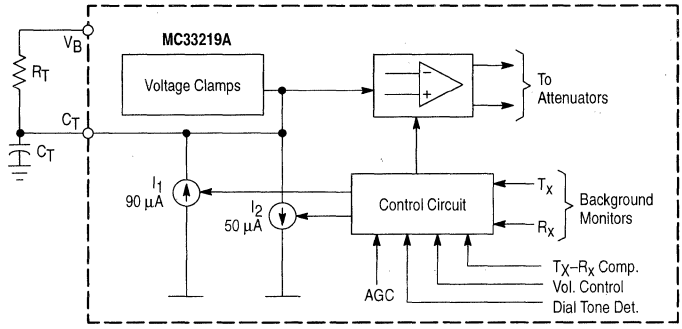
Figure 24. Attenuator Input Stage



The attenuators are controlled by the single output of the Attenuator Control Circuit, which is measurable at C_T (Pin 7). When the circuit detects speech signals directing it to the receive mode (by means of the level detectors described below), an internal current source of 90 μA will charge the C_T capacitor to a voltage positive with respect to V_B (see Figure 25). At the maximum volume control setting, this voltage will be approximately 150 mV, and the receive attenuator will have a gain of 6.7 dB. When the circuit detects speech signals directing it to the transmit mode, an internal current source of 50 μA will take the capacitor to approximately –100 mV with respect to V_B (the transmit attenuator will have a gain of 6.7 dB). When there is no speech present in either path, the current sources are shut off, and the voltage at C_T will decay to be equal to V_B. This is the idle mode, and the attenuators' gains are nearly halfway between their fully ON and fully OFF positions (–25 dB for the R_X attenuator, –16 dB for the T_X attenuator). Monitoring the C_T voltage (with respect to V_B) is the most direct method of monitoring the circuit's mode, and its response.

The inputs to the Attenuator Control Section are six: The T_X–R_X comparator operated by the level detectors, two background noise monitors, the volume control, the dialtone detector, and the AGC circuit. These six functions are described as follows.

Figure 25. C_T Attenuator Control Circuit

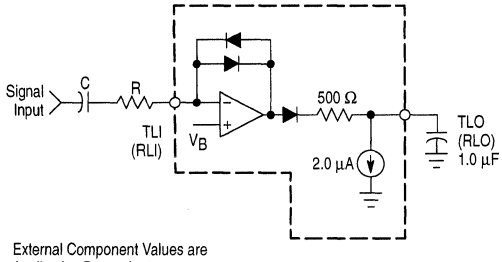


Level Detectors

There are two identical level detectors: one on the receive side and one on the transmit side (refer to Figure 26). Each level detector is a high gain amplifier with back–to–back diodes in the feedback path, resulting in non–linear gain, which permits operation over a wide dynamic range of speech levels. Refer to the graphs of Figures 6, 7 and 8 for their DC and AC transfer characteristics. The sensitivity of each level detector is determined by the external resistor and capacitor at their input (TLI and RLI). The output charges an external capacitor through a diode and limiting resistor, thus providing a DC representation of the input AC signal level. The outputs have a quick rise time (determined by the capacitor and an internal 500 Ω resistor), and a slow decay time set by an internal current source and the capacitor. The capacitors on the two outputs should have the same value (±10%) to prevent timing problems.

Referring to Figure 2, the outputs of the two level detectors drive the T_X–R_X comparator. The comparator's output state depends on whether the transmit or receive speech signal is stronger, as sensed by the level detectors. The Attenuator Control Circuit uses this signal, along with the background noise monitors, to determine which mode to set.

Figure 26. Level Detector



External Component Values are Application Dependent.

Background Noise Monitors

The purpose of the background noise monitors is to distinguish speech (which consists of bursts) from background noise (a relatively constant signal). There are two background noise monitors: one for the receive path and one for the transmit path. Refering to Figure 27, each is operated on by a level detector, which provides a DC voltage representative of the combined speech and noise level. However, the peaks, valleys, and bursts, which are characteristic of speech, will cause the DC voltage (at CP2 or RLO) to increase relatively quickly, causing the output of the next amplifier to also rise quickly. If that increase exceeds the 36 mV offset, and at a speed faster than the time constant at CPT (CPR), the output of the last comparator will change, indicating the presence of speech to the attenuator control circuit. This will keep the circuit in either the transmit or the receive mode, depending on which side has the stronger signals. When a new continuous signal is applied, the time constant at CPT (CPR) determines how long it takes the circuit to decide that the new sound is continuous, and is therefore background noise. The system requires that the average speech signal be stronger than the background noise level (by 6.0–7.0 dB) for proper speech detection.

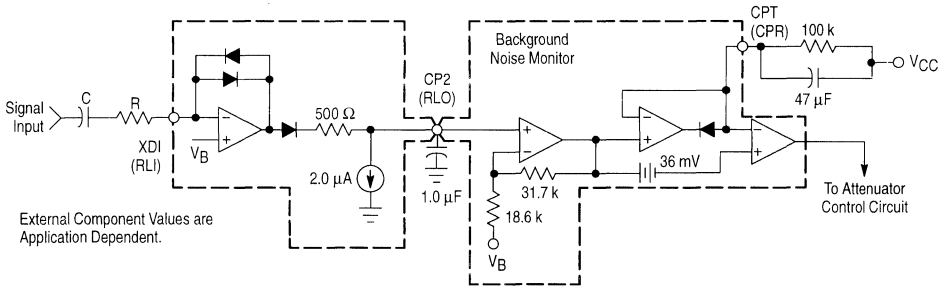
When only background noise is present in both paths, the output of the monitors will indicate the absence of speech, allowing the circuit to go to the idle mode.

AGC Circuit

In the receive mode only, the AGC circuit decreases the gain of the receive attenuator when the supply voltage at V_{CC} falls below 3.5 V, according to the graph of Figure 5. The gain of the transmit path changes in a complementary manner.

The purpose of this feature is to reduce the power (and current) used by the speaker when the speakerphone is powered by the phone line, and is connected to a long telephone line, where the available power is limited. Reducing the speaker power controls the voltage sag at V_{CC}, reduces clipping and distortion at the speaker output, and prevents possible erratic operation.

Figure 27. Background Noise Monitor



Volume Control

The volume control input at VLC (Pin 19) is sensed as a voltage with respect to V_B. The volume control affects the attenuators in the receive mode ***only***. It has no effect in the idle or transmit modes.

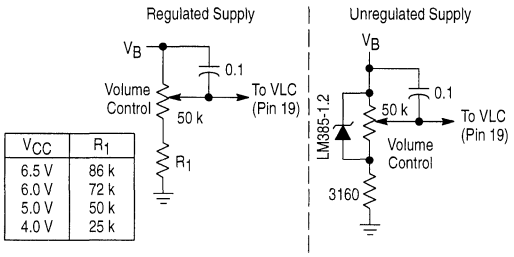
By varying the voltage at the VLC pin (Pin 19), the volume control varies the gain of the attenuators. Maximum receive attenuator gain (6.7 dB) occurs when VLC = V_B. As VLC is reduced below V_B, the gain of the receive attenuator is reduced, and the transmit attenuator gain increases in a complementary manner. The usable range of the VLC pin is ≈ 1.1 V for V_{CC} ≥ 3.5 V, providing a range of ≈ 40 dB (see Figure 4). At V_{CC} < 3.5 V, the range is reduced due to the lower V_B voltage, and the AGC function.

The configuration of the external volume control potentiometer circuit depends on whether the V_{CC} supply voltage is regulated or if it varies, such as in a phone line powered circuit (see Figure 28). If the supply voltage is regulated, the circuit on the left can be used. The value of the lower resistor (R_1) depends on the value of V_{CC}, so that Pin 19 can be varied from V_B to ≈ 1.1 V below V_B.

In a phone line powered circuit, the value of V_{CC}, and consequently V_B, will vary with line length and with the amount of sound at the speaker. In this case, the circuit on the right side of Figure 28 must be used to provide a fixed reference voltage for the potentiometer. With this circuit, the volume setting will not vary when V_{CC} is ≥ 3.5 V. As V_{CC} falls below 3.5 V, the zener diode will drop out of regulation, but the AGC circuit will ensure that instabilities do not occur.

The bias current at VLC flows out of the pin and depends on the voltage at the pin (see Figure 16). The capacitor from VLC to V_B helps reduce any effects of ripple or noise on V_B.

Figure 28. Volume Control



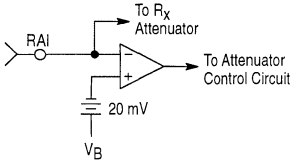
V_{CC}	R_1
6.5 V	86 k
6.0 V	72 k
5.0 V	50 k
4.0 V	25 k

Dial Tone Detector

When the speakerphone is initially taken off–hook, the dial tone signal will switch the circuit to the receive mode. However, since the dial tone is a continuous signal, the MC33219A would consider it as background noise rather than speech, and would therefore switch from receive to idle, causing the dial tone sound level to fade. The dial tone detector prevents the fading by disabling the background noise monitor.

The dial tone detector is a comparator with one side connected to the receive attenuator input (RAI), and the other input connected to V_B with a –20 mV offset (see Figure 29). If the circuit is in the receive mode and the incoming signal has peaks greater than 20 mV (14 mV rms), the comparator's output will change, disabling the receive idle mode. The receive attenuator will then be at a setting determined solely by the volume control. **NOTE:** The dial tone detector is **not** a frequency discriminating circuit.

Figure 29. Dial Tone Detector



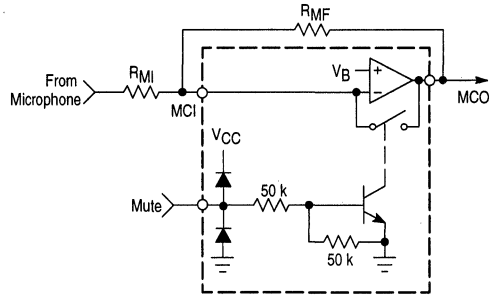
Microphone Amplifier, Mute

The microphone amplifier (Pins 20, 21) has the non–inverting input internally connected to V_B, while the inverting input and the output are pinned out. Unlike most op amps, the amplifier has an all NPN output stage, which maximizes phase margin and gain–bandwidth. This feature ensures stability at gains less than unity, as well as with a wide range of reactive loads. The open loop gain is typically 70 dB (f < 100 Hz), and the gain–bandwidth is typically 1.5 MHz. The maximum p–p output swing, for 1.0% or less distortion, is shown in Figure 14. The output impedance is <10 Ω until current limiting is reached (typically 2.0 mA peak). The input bias current at MCI is typically 30 nA out of the pin.

The mute function (Pin 18), when activated, will reduce the gain of the amplifier by shorting the external feedback resistor (RMF in Figure 30). The amplifier is not disabled in this mode; MCO remains a low impedance output, and MCI remains a virtual ground at V_B. The amount of muting (the

change in gain) depends on the value of the external feedback resistor, according to the graph of Figure 15. Muting occurs as the mute input pin is taken from ≈ 1.0 V to ≈ 1.4 V. The voltage on this pin must be ≤ 0.8 V for normal operation, and ≥ 2.0 V for muting. See Figure 10 for input current requirements. The input must be kept within the range of V_{CC} and GND. If the input is taken more than 0.4 V above V_{CC} or below GND excessive currents will flow, and the device's operation will be distorted. If the mute function is not used, the pin should be grounded.

Figure 30. Microphone Amplifier and Mute



Receive Amplifier

The receive amplifier (Pins 16, 17) has the non–inverting input internally connected to V_B, while the inverting input and the output are pinned out. Unlike most op amps, the amplifier has an all NPN output stage, which maximizes phase margin and gain–bandwidth. This feature ensures stability at gains less than unity, as well as with a wide range of reactive loads. The open loop gain is typically 70 dB (f < 100 Hz), and the gain–bandwidth is typically 1.5 MHz. The maximum p–p output swing for 1.0% or less distortion is shown in Figure 14. The output impedance is <10 Ω until current limiting is reached (typically 2.0 mA peak). The input bias current at RXI is typically 30 nA out of the pin.

Power Supply, V_B and Chip Disable

The power supply voltage at Pin 24 is to be between 3.5 and 6.5 V for normal operation, and down to 2.7 V with the AGC in effect (see AGC section). The supply current required is typically 3.2 mA in the idle mode, and ≈ 4.0 mA in the transmit and receive modes. Figure 11 shows the supply current for both the normal and disabled modes.

The output voltage at V_B (Pin 6) is approximately equal to $(V_{CC} - 0.7)/2$, and provides an AC ground for the internal amplifiers and the system. The output impedance at V_B is approximately 600 Ω, and in conjunction with the external capacitor at V_B forms a low pass filter for power supply noise rejection. The choice of the V_B capacitor size is application dependent based on whether the circuit is powered by the telephone line or a regulated supply. See Figure 13 for PSRR information. Since V_B biases the microphone and receive amplifiers, the amount of supply rejection at their outputs is a function of the rejection at V_B, as well as the gains of the amplifiers.

The amount of current which can be sourced out of the V_B pin depends on the V_{CC} voltage (see Figure 12). Drawing current in excess of that shown in Figure 12 will cause V_B to drop low enough to disrupt the circuit's operation. This pin can sink ≈ 100 μA when enabled, and 0 μA when disabled.

The Chip Disable (Pin 8) permits powering down the IC for power conservation. With CD between 0 and 0.8 V, normal operation is in effect. With CD between 2.0 V and V_{CC}, the IC is powered down, and the supply current drops to about 110 μA (at V_{CC} = 5.0 V, see Figure 11). When CD is high, the microphone and receive amplifiers, the level detectors, and the two attenuators are disabled (their outputs go to a high impedance). The background noise monitors are disabled, and Pins 3 and 10 will go to V_{CC}. The V_B output, however, remains active, except that it cannot sink any current.

The CD input must be kept within the range of V_{CC} and GND. See Figure 9 for input current requirements. If the input is taken more than 0.4 V above V_{CC} or below GND excessive currents will flow, and the device's operation will be distorted. If the disable function is not used, the pin should be connected to ground.

APPLICATIONS INFORMATION

Switching and Response Time Theory

The switching time of the MC33219A circuit is dominated first by the components at C_T (Pin 7, see Figure 2), and second by the capacitors at the level detector outputs (RLO, TLO).

The transition time to receive or to transmit mode from either idle or the other mode is determined by the capacitor at CT, along with the internal current sources (refer to Figure 25). The switching time is:

$$\Delta T = \frac{\Delta V \times C_T}{I}$$

When switching from idle to receive, ΔV = 150 mV, I = 90 μA, the C_T capacitor is 15 μF, and ΔT calculates to ≈ 25 ms. When switching from idle to transmit, ΔV = 100 mV, I = 50 μA, the C_T capacitor is 15 μF, and ΔT calculates to ≈ 30 ms.

When the circuit switches to idle, the internal current sources are shut off, and the time constant is determined by the C_T capacitor and RT, the external resistor (see Figure 25). With C_T = 15 μF, and RT = 15 kΩ, the time constant is ≈ 225 ms, giving a total switching time of ≈ 0.68 s (for 95% change). The switching period to idle begins when both speakers have stopped talking. The switching time back to the original mode will depend on how soon that speaker begins speaking again. The sooner the speaking starts during the "decay to idle" period, the quicker the switching time, since a smaller voltage excursion is required. That switching time is determined by the internal current sources as described above.

When the circuit switches directly from receive to transmit (or vice versa), the total switching time depends not only on the components and currents at the C_T pin, but also on the response of the level detectors, the relative amplitude of the two speech signals, and the mode of the circuit, since the two level detectors are connected differently to the two attenuators.

The rise time of the level detector's outputs (RLO, TLO) is not significant since it is so short. The decay time, however, provides a significant part of the "hold time" necessary to hold the circuit (in transmit or receive) during the normal pauses in speech. The capacitors at the two outputs must be equal value (±10%) to prevent problems in timing and level response.

The components at the inputs of the level detectors (RLI, TLI) do not affect the switching time, but rather affect the relative signal levels required to switch the circuit, as well as the frequency response of the detectors. They must be adjusted for proper switching response as described later in this section.

Switching and Response Time Measurements

Using burst of 1.0 kHz sine waves to force the circuit to switch among its modes, the timing results were measured and are indicated in Figures 17–21.

a) In Figure 17, when a signal is applied to the transmit attenuator only (normally via the microphone and the microphone amplifier), the transmit background noise monitor immediately indicates the "presence of speech" as evidenced by the fact that CPT begins rising. The slope of the rising CPT signal is determined by the external resistor and capacitor on that pin. Even though the transmit attenuator is initially in the idle mode (–16 dB), there is sufficient signal at its output to cause TLO to increase. The attenuator control circuit then forces the circuit to the transmit mode, evidenced by the change at the C_T pin. The attenuator output signal is then 6.7 dB above the input.

With the steady sine wave applied to the transmit input, the circuit will stay in the transmit mode until the CPT pin gets to within 36 mV of its final value. At that point, the internal comparator (see Figure 27) switches, indicating to the attenuator control circuit that the signal is not speech, but rather it is a steady background noise. The circuit now begins to decay to idle, as evidenced by the change at C_T and TLO, and the change in amplitude at TAO.

When the input signal at TAI is removed (or reduced), the CPT pin drops quickly, allowing the circuit to quickly respond to any new speech which may appear afterwards. The voltage at C_T decays according to the time constant of its external components, if not already at idle.

The voltage change at CP2, CPT, and TAO depends on the input signal's amplitude and the components at XDI and TLI. The change at C_T is internally fixed at the level shown. The timing numbers shown depend both on the signal amplitudes and the components at the C_T and CPT pins.

b) Figure 18 indicates what happens when the same signal is applied to the receive side only. RLO and CPR react similarly to TLO and CPT. However, the circuit does not switch to idle when CPR finishes transitioning since the dial tone detector disables the background noise monitor, allowing the circuit to stay in the receive mode as long as there is a signal present. If the input signal amplitude had been less than the dial tone detector's threshold, the circuit response would have been similar to that shown in Figure 17. The voltage change at C_T depends on the setting of the volume control (Pin 19). The 150 mV represent maximum volume setting.

c) Figure 19 indicates the circuit response when transmit and receive signals are alternately applied, with relatively short cycle times (300 ms each) so that neither attenuator will begin to go to idle during its "on" time. Figure 20 indicates the circuit response with longer cycle times (1.0 s each), where the transmit side is allowed to go to idle. Figure 21 is the same as Figure 20, except the capacitor at C_T has been reduced from 15 μF to 6.8 μF, providing a quicker switching time. The reactions at the various pins are shown. The response times at TAO and RAO are different, and typically slightly longer than what is shown in Figures 17 and 18 due to:

– the larger transition required at the C_T pin,

– the greater difference in the levels at RLO and TLO due to the positions of the attenuators as well as their decay time, and

– response time of the background noise monitors.

The timing responses shown in these three figures are representative for those input signal amplitudes and burst durations. Actual response time will vary for different signal conditions.

NOTE: While it may seem desirable to decrease the switching time between modes by reducing the capacitor at C_T, this should be done with caution for two reasons:

1) If the switching time is too short, the circuit response may appear to be "too quick" to the user, who may consider its operation erratic. The recommended values in this data sheet, along with the accompanying timings, provide what

experience has shown to be a "comfortable response" by the circuit.

2) The distortion in the receive attenuator will increase as the C_T capacitor value is decreased. The extra THD will be most noticeable at the lower frequencies and at the lower ampitudes. Table 1 provides a guideline for this issue.

Table 1. THD versus C_T Capacitor

C_T Capacitor	Idle – R_X Transition	Input @ RAI	Freq.	THD @ RAO
15 µF	25 ms	20 mVrms	300 Hz	1.2%
			1.0 KHz	0.25%
		100 mVrms	300 Hz	0.5%
			1.0 KHz	0.2%
6.8 µF	12 ms	20 mVrms	300 Hz	5.0%
			1.0 KHz	0.7%
		100 mVrms	300 Hz	1.3%
			1.0 KHz	0.35%
3.0 µF	5.0 ms	20 mVrms	300 Hz	11%
			1.0 KHz	1.8%
		100 mVrms	300 Hz	2.6%
			1.0 KHz	0.7 %

Considerations in the Design of a Speakerphone

The design and adjustment of a speakerphone involves human interface issues as well as proper signal levels. Because of this fact, it is not practical to do all of the design mathematically. Certain parts of the design must be done by trial and error, most notably the switching response and the "How does it sound?" part of the testing. Among the recommendations for a successful design are:

1) Design the enclosure **concurrently** with the electronics. Do not leave the case design to the end as its properties are just as important (just as *equally* important) as the electronics. One of the major issues involved in a speakerphone design is the acoustic coupling of the speaker to the microphone, which must be minimized. This parameter is dependent entirely on the design of the enclosure, the mounting of the speaker and the microphone, and their characteristics.

2) Ensure the speaker is optimally mounted. This fact alone can make a difference of several dB in the sound level from the speaker, as well as the sound quality. The speaker manufacturer should be consulted for this information.

3) Do not breadboard the circuit with the microphone and speaker hanging out in midair. It will not work. The speaker and microphone must be in a suitable enclosure, preferably one resembling the end product. If this is not feasible, temporarily use some other properly designed enclosure, such as one of the many speakerphones on the market.

4) Do not breadboard the circuit on a wirewrapped board or a plug–in prototyping board. Use a PC board, preferably with a ground plane. Proper filtering of the supply voltage at the V_{CC} pin is essential.

5) The speakerphone must be tested with the intended hybrid and connected to a phone line or phone line simulator. The performance of the hybrid is just as important as the enclosure and the speakerphone IC.

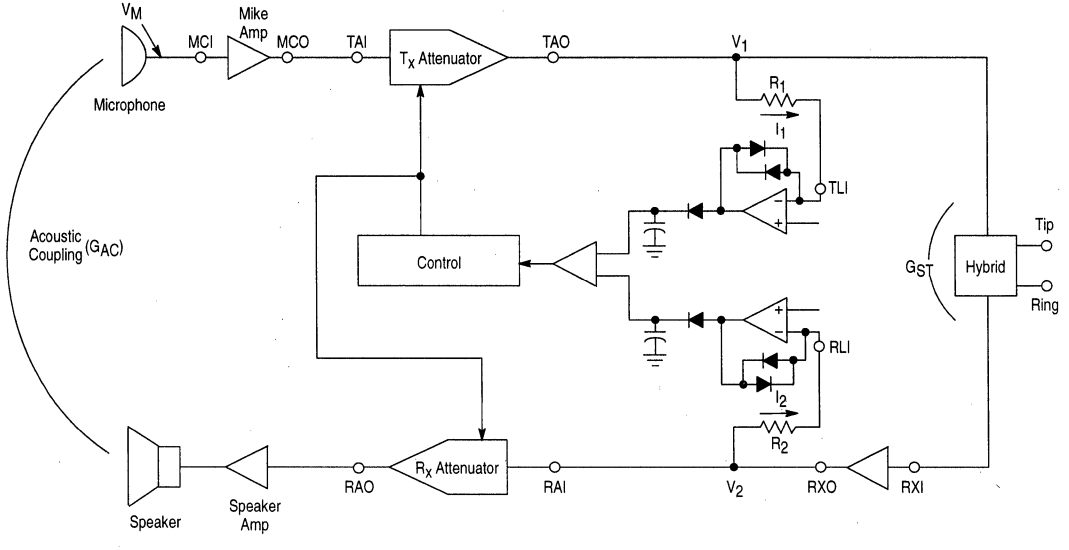
6) When testing the speakerphone, be conscious of the environment. If the speakerphone is in a room with large windows and tile floors, it will sound different than if it is in a carpeted room with drapes. Additionally, be conscious of the background noise in a room.

7) When testing the speakerphone on a phone line, make sure the person at the other end of the phone line is **not** in the same room as the speakerphone.

Design Procedure

A recommended sequence follows in Figure 31, assuming the end product enclosure is available, with the intended production microphone and speaker installed, and the PC boards or temporary substitutes installed.

Figure 31. Basic Block Diagram for Design Purposes



1) Design the hybrid, ensuring proper interface with the phone line for both DC and AC characteristics. The return loss must be adjusted to comply with the appropriate regulatory agency. The sidetone should then be adjusted according to the intent of the product. If the product is a speakerphone only (without a handset), the sidetone gain (GST) should be adjusted for maximum loss. If a handset is part of the end product, the sidetone must be adjusted for the minimum acceptable sidetone levels in the handset. Generally, for the speakerphone interface, 10–20 dB sidetone loss is preferred for GST.

2) Check the acoustic coupling of the enclosure (GAC in Figure 31). With a steady sound coming out of the speaker, measure the rms voltage on the speaker terminals and the rms voltage out of the microphone. Experience has shown that the loss should be at least 40 dB, preferably 50 dB. This should be checked over the frequency range of 20 Hz to 10 kHz.

3) Adjust the transmit path for proper signal levels, based on the lowest speech levels as well as the loudest. Based on the typical levels from commonly available microphones, a gain of about 35–45 dB is required from the microphone terminals to Tip and Ring. Most of that gain should be in the microphone amplifier to make best use of the transmit attenuator, but the maximum input level at TAI must not be exceeded. If a signal generator is used instead of a microphone for testing, the circuit can be locked into the transmit mode by grounding CPT (Pin 3). Frequency response can generally be tailored with capacitors at the microphone amplifier.

4) Adjust the receive path for proper signal levels based on the lowest speech levels as well as the loudest. A gain of about 30 dB is required from Tip and Ring to the speaker terminals for most applications (at maximum volume). Most of that gain should be in the receive amplifier (at RXI, RXO) to make best use of the receive attenuator, but the maximum input level at RAI must not be exceeded. If a signal generator is used for signal injection during testing, the circuit can be locked into the receive mode by grounding CPR (Pin 10), although this is usually not necessary since the dial tone detector will keep the circuit in the receive mode. Frequency response can generally be tailored with capacitors at the receive amplifier.

5) Check that the loop gain (i.e., the receive path gain + acoustic coupling gain + transmit path gain + sidetone gain) is less than 0 dB over all frequencies. If not, "singing" will occur: a steady oscillation at some audible frequency.

6) a) The final step is to adjust the resistors at the level detector inputs (RLI and TLI) for proper switching response (the switchpoint occurs when $I_1 = I_2$). This has to be the last step, as the resistor values depend on all of the above adjustments, which are based on the mechanical, as well as the electrical, characteristics of the system. **NOTE:** An extreme case of level detector misadjustment can result in "motorboating". In this condition, with a receive signal applied, sound from the speaker enters the microphone, and causes the circuit to switch to the transmit mode. This causes the speaker sound to stop (as well as the sound into the microphone), allowing the circuit to switch back to the receive mode. This sequence is then repeated, usually, at a rate of a few Hz. The first thing to check is the acoustic coupling, and then the level detectors.

b) Starting with the recommended values for R_1 and R_2 (in Figure 2), hold a normal conversation with someone on another phone. If the resistor values are not optimum, one of the talkers will dominate, and the other will have difficulty getting through. If, for example, the person at the speakerphone is dominant, the transmit path is overly sensitive, and the receive path is not sensitive enough. In this case, R_1 (at TLI) should be increased, or R_2 (at RLI) decreased, or both. Their exact value is not critical at this point, only their relative value. Keeping R_1 and R_2 in the range of 2.0–20 k, adjust them until a suitable switching response is found.

c) Then have the person at the other end of the phone line speak loud continuously, or connect to a recording which is somewhat strong. Monitor the state of the circuit (by measuring the C_T versus V_B pins, and by listening carefully to the speaker) to check that the sound out of the speaker is not attempting to switch the circuit to the transmit side (through acoustic coupling). If it is, increase R_1 (at TLI) in small steps just enough to stop the switching (this desensitizes the transmit side). If R_1 has been changed a large amount, it may be necessary to readjust R_2 for switching response. If this cannot be achieved in a reasonable manner, the acoustic coupling is too strong.

d) Next, have the person at the speakerphone speak somewhat loudly, and again monitor the state of the circuit, primarily by having the person at the other end listen carefully for fading. If there is obvious fading of the sound, increase R_2 so as to desensitize the receive side. Increase R_2 just enough to stop the fading. If this cannot be achieved in a reasonable manner, the sidetone coupling is too strong.

e) If necessary, readjust R_1 and R_2 a small amount relative to each other, to further optimize the switching response.

Transmit/Receive Detection Priority

Although the MC33219A was designed to have an idle mode such that the transmit side has a small priority (the idle mode position is closer to the full transmit side), the idle mode position can be moved with respect to the transmit or the receive side. With this done, the ability to gain control of the circuit by each talker will be changed.

By connecting a resistor from C_T (Pin 7) to ground, the circuit will be biased more towards the transmit side. The resistor value is calculated from:

$$R = R_T \left[\frac{V_B}{\Delta V} - 1 \right]$$

where R is the added resistor, R_T is the resistor normally between Pins 6 and 7 (typically 15 kΩ), and ΔV is the desired change in the C_T voltage at idle.

By connecting a resistor from C_T (Pin 7) to V_{CC}, the circuit will be biased towards the receive side. The resistor value is calculated from:

$$R = R_T \left[\frac{V_{CC} - V_B}{\Delta V} - 1 \right]$$

R, R_T, and ΔV are the same as above. Switching response and the switching time will be somewhat affected in each case due to the different voltage excursions required to get to transmit and receive from idle. For practical considerations, the ΔV shift should not exceed 50 mV.

Disabling the Idle Mode

For testing or circuit analysis purposes, the transmit or receive attenuators can be set to the ON position, even with steady signals applied, by disabling the background noise monitors. Grounding the CPR pin will disable the receive background noise monitor, thereby indicating the "presence

of speech" to the attenuator control block. Grounding CPT does the same for the transmit path.

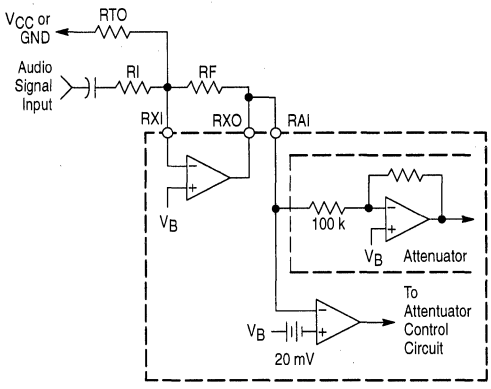
Additionally, the receive background noise monitor is automatically disabled by the dial tone detector whenever the receive signal exceeds the detector's threshold.

Dial Tone Detector Threshold

The threshold for the dial tone detector is internally set at ≈ 20 mV (14 mVrms) below V_B (see Figure 29). That threshold can be adjusted if desired by changing the bias at RAI. The method used depends on how the input of the receive attenuator is connected to other circuitry.

a) If the attenuator input (RAI) is DC coupled to the receive amplifier (Pins 15 to 16 as in Figure 2), or to some other amplifier in the system, then the threshold is changed by forcing a small offset on that amplifier. As shown in Figure 32, connect a resistor (RTO) from the summing node to either ground or V_{CC}, depending on whether the dial tone detector threshold is to be increased or decreased. RF and RI are the resistors normally used to set the gain of that amplifier.

Figure 32. Adjusting Dial Tone Detector Threshold (DC Coupled)



Adding RTO and connecting it to ground will shift RXO and RAI upward, thereby increasing the dial tone detector threshold. In this case, RTO is calculated from:

$$RTO = \frac{V_B \times RF}{\Delta V}$$

V_B is the voltage at Pin 6, and ΔV is the amount that the detector's threshold is increased. For example, if V_B = 2.2 V, and RF = 10 k, and the threshold is to be increased by 20 mV, RTO calculates to 1.1 MΩ.

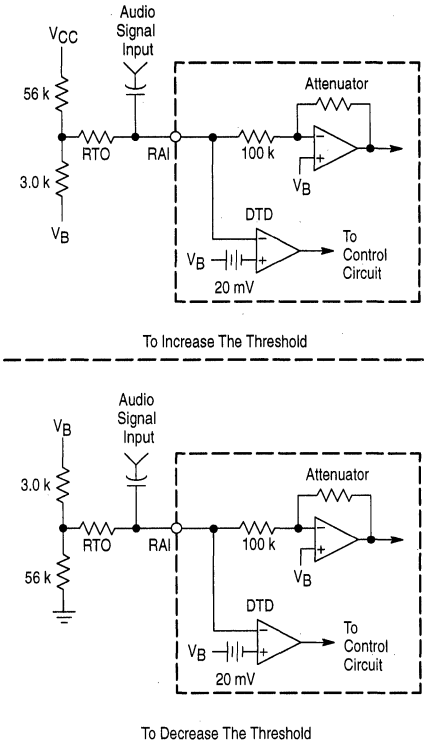
Connecting RTO to V_{CC} will shift RXO downward, thereby decreasing the dial tone detector threshold. In this case, RTO is calculated from:

$$RTO = \frac{(V_{CC} - V_B) \times RF}{\Delta V}$$

For example, if V_{CC} = 5.0 V, V_B = 2.2 V, and RF = 10 k and the threshold is to be decreased by 10 mV, RTO calculates to 2.8 MΩ.

b) If the receive attenuator input is AC coupled to the receive amplifier or to other circuitry, then the offset is set at RAI. The circuits in Figure 33 are suggested for changing the threshold.

Figure 33. Adjusting Dial Tone Detector Threshold (AC Coupled)



To increase the threshold, use the first circuit in Figure 33. The voltage at the top of the 3.0 k resistor is between 90 and 180 mV above V_B (depending on V_{CC}). RTO and the 100 k input impedance form a voltage divider to create the desired offset at RAI. RTO is calculated from:

$$RTO = \left[\frac{((V_{CC} - V_B) \times 0.05)}{\Delta V} - 1\right] (100\ k)$$

For example, if V_{CC} = 5.0 V, and the threshold is to be increased by 20 mV (ΔV), RTO calculates to ≈ 600 kΩ.

If the threshold is to be decreased, use the second circuit in Figure 33. RTO is calculated from:

$$RTO = \left[\frac{(V_B \times 0.05)}{\Delta V} - 1\right] (100\ k)$$

RFI Interference

Potential radio frequency interference (RFI) problems should be addressed early in the electrical and mechanical design of the speakerphone. RFI may enter the circuit through Tip and Ring, through the microphone wiring to the microphone amplifier (which should be short), or through any of the PC board traces. The most sensitive pins on the MC33219A are the inputs to the level detectors (RLI, TLI, XDI) since, when there is no speech present, the inputs are high impedance and these op amps are in a near open–loop

condition. The board traces to these pins should be kept short, and the resistor and capacitor for each of these pins should be physically close to the pins. All other input pins should also be considered sensitive to RFI signals.

In The Final Analysis ...

Proper operation of a speakerphone is a combination of proper mechanical (acoustic) design in addition to proper electronic design.The acoustics of the enclosure must be considered early in the design of a speakerphone. In general, electronics cannot compensate for poor acoustics, low speaker quality, low microphone quality, or any combination of these items. Proper acoustic separation of the speaker and microphone is essential. The physical location of the microphone, along with the characteristics of the selected microphone, will play a large role in the quality of the transmitted sound. The microphone and speaker vendors can usually provide additional information on the use of their products.

In the final analysis, the circuit will have to be fine–tuned to match the acoustics of the enclosure, the specific hybrid, and the specific speaker and microphone selected. The components shown in this data sheet should be considered as starting points only. The gains of the transmit and receive paths are easily adjusted at the microphone and receive amplifiers, respectively. The switching response can then be fine tuned by varying (in small steps) the components at the level detector inputs (TLI, RLI) until satisfactory operation is obtained for both long and short lines.

For additional information on speakerphone design please refer to The Bell System Technical Journal, Volume XXXIX (March 1960, No. 2).

Attenuation – A decrease in magnitude of a communication signal, usually expressed in dB.

Bandwidth – The range of information carrying frequencies of a communication system.

Battery – The voltage which provides the loop current to the telephone from the CO. The name is derived from the fact that COs have always used batteries, in conjunction with AC power, to provide this voltage.

C–Message Filter – A frequency weighting which evaluates the effects of noise on a typical subscriber's system.

Central Office – Abbreviated CO, it is a main telephone office, usually within of a few miles of its subscribers, that houses switching gear for interconnection within its exchange area, and to the rest of the telephone system. A CO can handle up to 10,000 subscriber numbers.

CO – See Central Office.

CODEC – Coder/Decoder – In the Central Office, it converts the transmit signal to digital, and converts the digital receive signal to analog.

dB – A power or voltage measurement unit, referred to another power or voltage. It is generally computed as:

$$10 \times \log (P_1/P_2)$$

for power measurements, and

$$20 \times \log(V_1/V_2)$$

for voltage measurements.

dBm – An indication of signal power. 1.0 mW across 600 Ω, or 0.775 Vrms, is defined as 0 dBm. Any other voltage level is converted to dBm by:

dBm = 20 x log (Vrms/0.775), or

dBm = [20 x log (Vrms)] + 2.22.

dBmp – Indicates dBm measurement using a psophometric weighting filter.

dBrn – Indicates a dBm measurement relative to 1.0 pW power level into 600 Ω. Generally used for noise measurements, 0 dBrn = –90 dBm.

dBrnC – Indicates a dBrn measurement using a C–message weighting filter.

DTMF – Dual Tone MultiFrequency. It is the "tone dialing" system based on outputting two non–harmonic related frequencies simultaneously to identify the number dialed. Eight frequencies have been assigned to the four rows and four columns of a keypad.

Four Wire Circuit – The portion of a telephone, or central office, which operates on two pairs of wires. One pair is for the Transmit path, and one pair is for the Receive path.

Full Duplex – A transmission system which permits communication in both directions simultaneously. The standard handset telephone system is full duplex.

Gain – The change in signal amplitude (increase or decrease) after passing through an amplifier or other circuit stage. Usually expressed in dB, an increase is a positive number and a decrease is a negative number.

Half Duplex – A transmission system which permits communication in one direction at a time. CB radios, with "push–to–talk" switches, and voice activated speakerphones are half duplex.

Hookswitch – A switch within the telephone which connects the telephone circuit to the subscriber loop. The name is derived from old telephones where the switch was activated by lifting the receiver off and onto a hook on the side of the phone.

Hybrid – A two–to–four wire converter.

Idle Channel Noise – Residual background noise when transmit and receive signals are absent.

Line Card – The printed circuit board and circuitry in the CO or PBX which connects to the subscriber's phone line. A line card may hold circuitry for one subscriber or a number of subscribers.

Longitudinal Balance – The ability of the telephone circuit to reject longitudinal signals on Tip and Ring.

Longitudinal Signals – Common mode signals.

Loop – The loop formed by the two subscriber wires (Tip and Ring) connected to the telephone at one end, and the central office (or PBX) at the other end. Generally it is a floating system, not referred to ground, or AC power.

Loop Current – The DC current which flows through the subscriber loop. It is typically provided by the central office or PBX, and ranges from 20–120 mA.

Mute – Reducing the level of an audio signal, generally so that it is inaudible. Partial muting is used in some applications.

OFF Hook – The condition when the telephone is connected to the phone system, permitting the loop current to flow. The central office detects the DC current as an indication that the phone is busy.

ON Hook – The condition when the telephone is disconnected from the phone system, and no DC loop current flows. The central office regards an ON hook phone as available for ringing.

PABX – Private Automatic Branch Exchange. In effect, a miniature central office; it is a customer owned switching system servicing the phones within a facility, such as an office building. A portion of the PABX connects to the Bell (or other local) telephone system.

Power Supply Rejection Ratio – The ability of a circuit to reject outputting noise or ripple, which is present on the power supply lines. PSRR is usually expressed in dB.

Protection, Primary – Usually consisting of carbon blocks or gas discharge tubes, it absorbs the bulk of a lightning induced transient on the phone line by clamping the voltages to less than ±1500 V.

Protection, Secondary – Usually located within the telephone, it protects the phone circuit from transient surges. Typically, it must be capable of clamping a ±1.5 kV surge of 1.0 ms duration.

Pulse Dialing – A dialing system whereby the loop current is interrupted a number of times in quick succession. The number of interruptions corresponds to the number dialed, and the interruption rate is typically 10 per second. The old rotary phones and many new pushbutton phones use pulse dialing.

Receive Path – Within the telephone, it is the speech path from the phone line (Tip and Ring) towards the receiver or speaker.

REN – Ringer Equivalence Number. An indication of the impedance (or loading factor) of a telephone bell or ringer circuit. An REN of 1.0 equals ≈ 8.0 kΩ. The Bell system typically permits a maximum of 5.0 REN (1.6 kΩ) on an individual subscriber line. A minimum REN of 0.2 (40 kΩ) is required by the Bell system.

Return Loss – Expressed in dB, it is a measure of how well the telephone's AC impedance matches the line's AC characteristic impedance. With a perfect match, there is no reflected signal, and therefore infinite return loss. It is calculated from:

$$RL = 20 \times \log \frac{(Z_{LINE} + Z_{CKT})}{(Z_{LINE} - Z_{CKT})}$$

Ring – One of the two wires connecting the central office to a telephone. The name is derived from the ring portion of the plugs used by operators (in older equipment) to make the connection. Ring is traditionally negative with respect to Tip.

Sidetone Rejection – The rejection (in dB) of the reflected signal in the receive path resulting from a transmit signal applied to the phone and phone line.

SLIC – Subscriber Line Interface Circuit. It is the circuitry within the CO or PBX which connects to the user's phone line.

Subscriber – The customer at the telephone end of the line.

Subscriber Line – The system consisting of the user's telephone, the interconnecting wires, and the central office equipment dedicated to that subscriber (also referred to as a loop).

Tip – One of the two wires connecting the central office to a telephone. The name is derived from the tip of the plugs used by operators (in older equipment) to make the connection. Tip is traditionally positive with respect to Ring.

Transmit Path – Within the telephone it is the speech path from the microphone towards the phone line (Tip and Ring).

Two Wire Circuit – Refers to the two wires connecting the central office to the subscriber's telephone. Commonly referred to as Tip and Ring, the two wires carry both transmit and receive signals in a differential manner.

Two–to–Four Wire Converter – A circuit which has four wires (on one side): two (signal and ground) for the outgoing signal and two for the incoming signal. The outgoing signal is sent out differentially on the two wire side, and incoming differential signals received on the two wire side are directed to the receive path of the four wire side. Additional circuit within cancels the reflected outgoing signal to keep it separate from the incoming signal.

Voiceband – That portion of the audio frequency range used for transmission across the telephone system. Typically it is 300–3400 Hz.

Suggested Vendors

Microphones

Primo Microphones Inc.
Bensenville, IL 60106
1–800–76–PRIMO

Telecom Transformers

Microtran Co., Inc.
Valley Stream, NY 11528
516–561–6050
Various models – ask for catalog
and Application Bulletin F232

PREM Magnetics, Inc.
McHenry, IL 60050
815–385–2700
Various models – ask for catalog

Stancor Products
Logansport, IN 46947
219–722–2244
Various models – ask for catalog

Motorola does not endorse or warrant the suppliers referenced.

MC34010

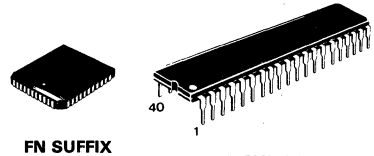
Advance Information

ELECTRONIC TELEPHONE CIRCUIT

- Provides All Basic Telephone Station Apparatus Functions in a Single IC, Including DTMF Dialer, Tone Ringer, Speech Network and Line Voltage Regulator
- DTMF Generator Uses Low-Cost Ceramic Resonator with Accurate Frequency Synthesis Technique
- Tone Ringer Drives Piezoelectric Transducer and Satisfies EIA RS-470 Impedance Signature Requirements
- Speech Network Provides Two–Four Wire Conversion with Adjustable Sidetone Utilizing an Electret Transmitter
- On-Chip Regulator Insures Stable Operation Over Wide Range of Loop Lengths
- I^2L Technology Provides Low 1.4 Volt Operation and High Static Discharge Immunity
- Microprocessor Interface Port for Automatic Dialing Features

ELECTRONIC TELEPHONE CIRCUIT

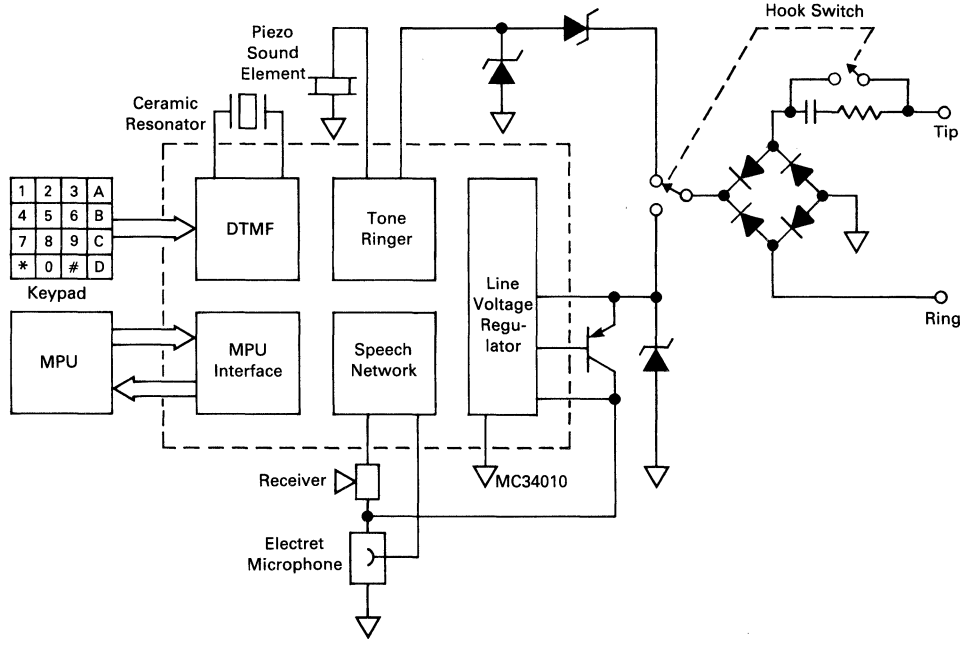
BIPOLAR LINEAR/I^2L



FN SUFFIX
44-PIN
PLCC
CASE 777

P SUFFIX
PLASTIC PACKAGE
CASE 711

FIGURE 1 — ELEMENTS OF THE ELECTRONIC TELEPHONE

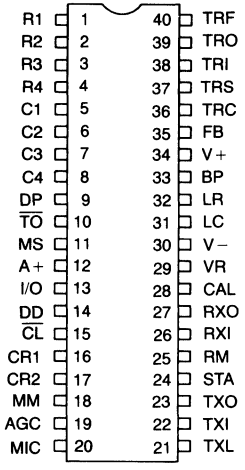


This document contains information on a new product. Specifications and information herein are subject to change without notice.

MAXIMUM RATINGS (Voltage References to V−)

Parameter	Value	Unit
V+ Terminal Voltage (Pin 34)	+20, −1.0	V
VR Terminal Voltage (Pin 29)	+2.0, −1.0	V
RXO Terminal Voltage (Pin 27)	+2.0, −1.0	V
TRS Terminal Voltage (Pin 37)	+35, −1.0	V
TRO (With Tone Ringer Inactive) Terminal Voltage	+2.0, −1.0	V
R1–R4 Terminal Current (Pins 1–4) C1–C4 (Pins 5–8)	±100	mA
$\overline{CL}$, $\overline{TO}$, DD, I/O, A+	+122, −1.0	V
Operating Ambient Temperature Range	−20 to +60	°C
Storage Temperature Range	−65 to +150	°C

PIN CONNECTIONS



2

GENERAL CIRCUIT DESCRIPTION

Introduction

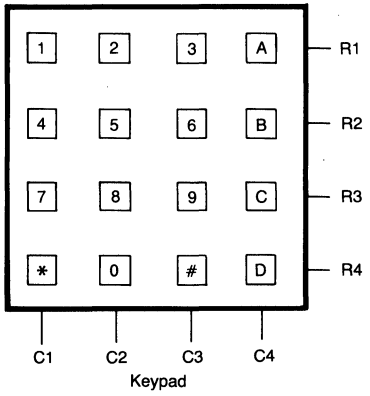
The MC34010 Electronic Telephone Circuit (ETC) provide all the necessary elements of a tone dialing telephone in a single IC. The functional blocks of the ETC include the DTMF dialer, speech network, tone ringer, and dc line interface circuit (Figure 1). The MC34010 also provides a microprocessor interface port that facilitates automatic dialing features.

Low voltage operation is a necessity for telephones in networks where parallel telephone connections are common. An electronic speech network operating in parallel with a conventional telephone may receive line voltages below 2.5 volts. DTMF dialers operate at similarly low-line voltages when signaling through battery powered station carrier equipment. These low voltage requirements have been addressed by realizing the MC34010 in a bipolar/I^2L technology with appropriate circuit techniques. The resulting speech and dialer circuits maintain specified performance with instantaneous input voltage as low as 1.4 volts.

Line Voltage Regulator

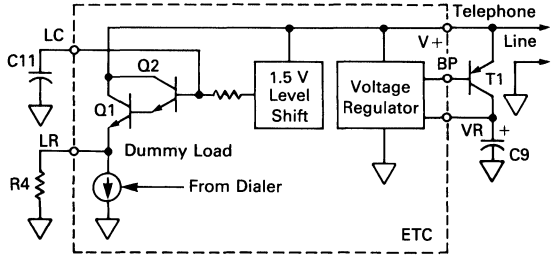
The dc line interface circuit (Figure 3) determines the dc input characteristic of the telephone. At low input voltages (less than 3 volts) the ETC draws only the

FIGURE 2 — MPU INTERFACE CODES



Key	Row	Column	Code (B3–B0)
1	1	1	1111
2	1	2	0111
3	1	3	1011
4	2	1	1101
5	2	2	0101
6	2	3	1001
7	3	1	1110
8	3	2	0110
9	3	3	1010
0	4	2	0100
A	1	4	0011
B	2	4	0001
C	3	4	0010
D	4	4	0000
*	4	1	1100
#	4	3	1000

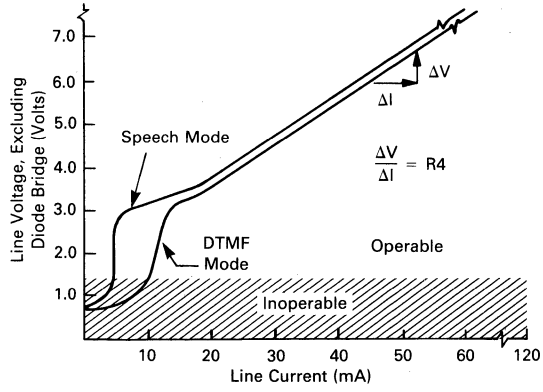
FIGURE 3 — DC LINE INTERFACE BLOCK DIAGRAM



GENERAL CIRCUIT DESCRIPTION (continued)

speech and dialer bias currents through the VR regulator. As input voltage increases, Q1 conducts the excess dc line current through resistor R4. The 1.5 volt level shift prevents saturation of Q2 with telephone line signals up to 2.0 volts peak (+5.2 dBm). A constant current (dummy load) is switched off when the DTMF dialer is activated to reduce line current transients. Figure 4 illustrates the dc voltage/current characteristic of an MC34010 telephone.

FIGURE 4 — DC V-I CHARACTERISTIC OF THE ETC



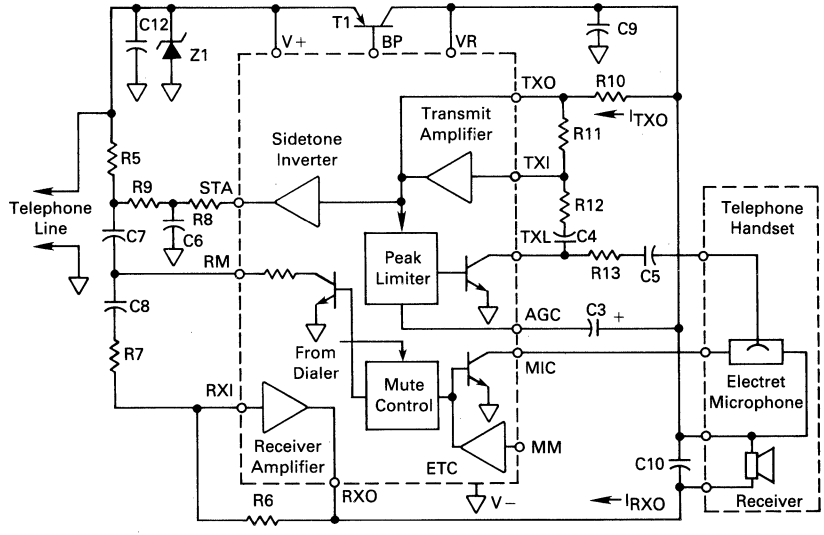
Speech Network

The speech network (Figure 5) provides the two-to-four wire interface between the telephone line and the instrument's transmitter and receiver. An electret microphone biased from VR drives the transmit amplifier. For very loud talkers, the peak limiter circuit reduces the transmit input level to maintain low distortion. The transmit amplifier output signal is inverted at the STA terminal and driven through an external R-C network to control the receiver sidetone level. The switched ac resistance at the RM terminal reduces receiver signal when dialing and suppresses clicks due to hook or keypad switch transitions. When transmitting, audio signal currents (i_{TXO} and i_{RXO}) flow through the voltage regulator pass transistor (T1) to drive the telephone line. This feature has two consequences: 1) In the transmitting mode the receiver sidetone current i_{RXO} contributes to the total signal on the line along with i_{TXO}; 2) The ac impedance of the telephone is determined by the receiver impedance and the voltage gain from the line to the receiver amplifier output.

DTMF Dialer

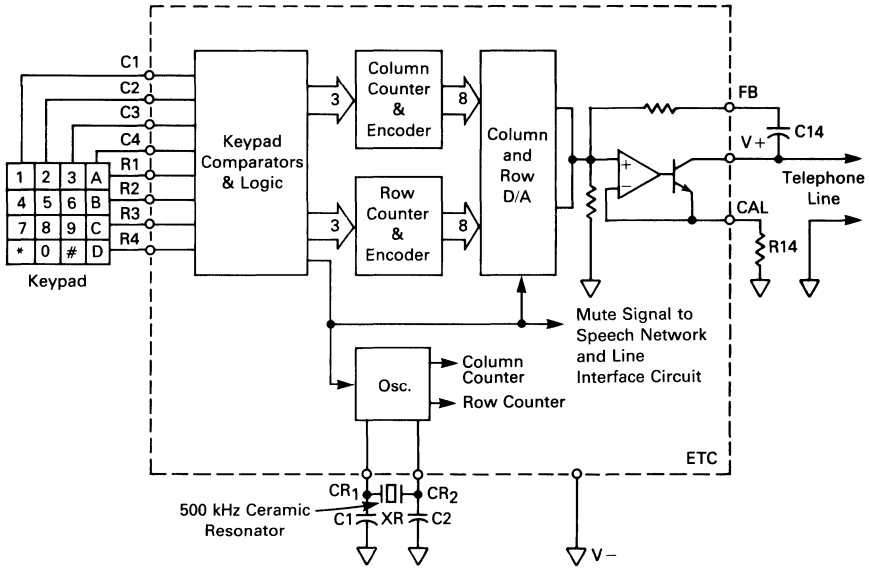
Keypad interface comparators activate the DTMF row and column tone generators (Figure 6) when a row and column input are connected through a SPST keypad. The keypad interface is designed to function with contact resistances up to 1.0 kΩ and leakage resistances as low as 150 kΩ. Single tones may be initiated by depressing two keys in the same row or column.

FIGURE 5 — SPEECH NETWORK BLOCK DIAGRAM



The programmable counters employ a novel design to produce non-integer frequency ratios. The various DTMF tones are synthesized with frequency division errors less than ±0.16% (Table 1). Consequently an inexpensive ceramic resonator can be used instead of a quartz crystal as the DTMF frequency reference. Total frequency error less than ±0.8% can be achieved with ±0.3% ceramic resonator. The row and column D/A converters produce 16-step approximations of sinusoidal waveforms. Feedback through terminal FB reduces the DTMF output impedance to approximately 2.0 kΩ to satisfy return loss specifications.

FIGURE 6 — DTMF DIALER BLOCK DIAGRAM



Tone Ringer

The tone ringer (Figure 7) generates a warbling square wave output drive to a piezo sound element when the ac line voltage exceeds a predetermined threshold level. The threshold detector uses a current mode comparator to prevent on/off chatter when the output current reduces the voltage available at the ringer input. When the average current into the tone ringer exceeds the threshold level, the ringer output TRO commences driving the piezo transducer. This output current sourced from TRI increases the average current measured by the threshold detector. As a result, hysteresis is produced beween the tone ringer on and off thresholds. The output frequency at TRO alternates between $f_O/8$ and $f_O/10$ at a warble rate of $f_O/640$, where f_O is the ringer oscillator frequency.

Microprocessor Interface

The MPU interface connects the keypad and DTMF sections of the ETC to a microprocessor for storing and retrieving numbers to be dialed. Figure 8 shows the major blocks of the MPU interface section and the interconnections between the keypad interface, DTMF generator and microprocessor. Each button of a 12 or 16 number keypad is represented by a four-bit code (Figure 2). This four-bit code is used to load the programmable counters to generate the appropriate row and column tones. The code is transferred serially to or from the microprocessor when the shift register is clocked by the microprocessor. Data is transferred through the I/O terminal, and the direction of data flow is determined by the Data Direction (DD) input terminal. In the manual dialing mode, DD is a Logic "0" and the four-bit code from the keypad is fed to the DTMF generator by the digital multiplexer and also output on the I/O terminal through the four-bit shift register. The data sequence on the I/O terminal is B3, B2, B1, B0 and is transferred on the negative edge of the clock input ($\overline{CL}$). In this mode the shift register load enable circuit cycles the register between the load and read modes such that multiple read cycles may be run for a single-key closure. Six complete clock cycles are required to output data from the ETC and reload the register for a second look.

In the automatic dialing mode, DD is a Logic "1" and the four-bit code is serially entered in the sequence B3, B2, B1, B0 into the four-bit shift register. Thus, only four clock cycles are required to transfer a number into the ETC. The keypad is disabled in this mode. A Logic "1" on the Tone Output ($\overline{TO}$) will disable tone outputs until valid data from the microprocessor is in place. Subsequently $\overline{TO}$ is switched to a Logic "0" to enable the DTMF generator. Figures 9 and 10 show the timing waveforms for the manual and automatic dialing modes and Table 2 specifies timing limitations.

The keypad decoder's exclusive OR circuit generates the DP and MS output signals. The DP output indicates (when at a Logic "1") that one, and only one, key is

depressed, thereby indicating valid data is available to the MPU. The DP output can additionally be used to initiate a data transfer sequence to the microprocessor. The MS output (when at a Logic "1") indicates the DTMF generator is enabled and the speech network is muted.

Pin A+ is to be connected to a source of 2.5 to 10 volts (generally from the microprocessor circuit) to enable the pullup circuits on the microprocessor interface outputs (DP, MS, I/O). Additionally, this voltage will power the entire circuitry (except Tone Ringer) in the absence of voltage at V+. This permits use of the transmit and receive amplifiers, keypad interface, and DTMF generator for non-typical telephone functions.

See Figure 45 for a typical interconnection to an MC6821 PIA (Peripheral Interface Adapter). Connection to a port on any other class of microprocessor will be similar.

FIGURE 7 — TONE RINGER BLOCK DIAGRAM

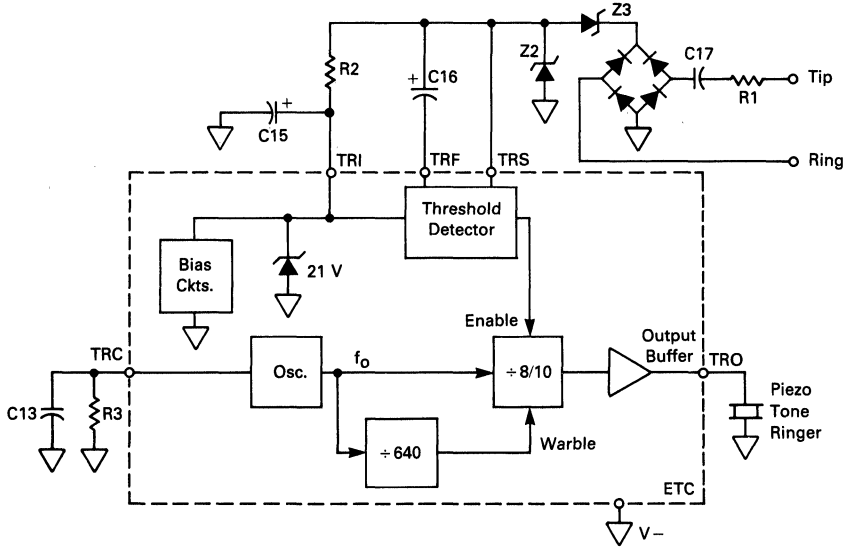


FIGURE 8 — MICROPROCESSOR INTERFACE BLOCK DIAGRAM

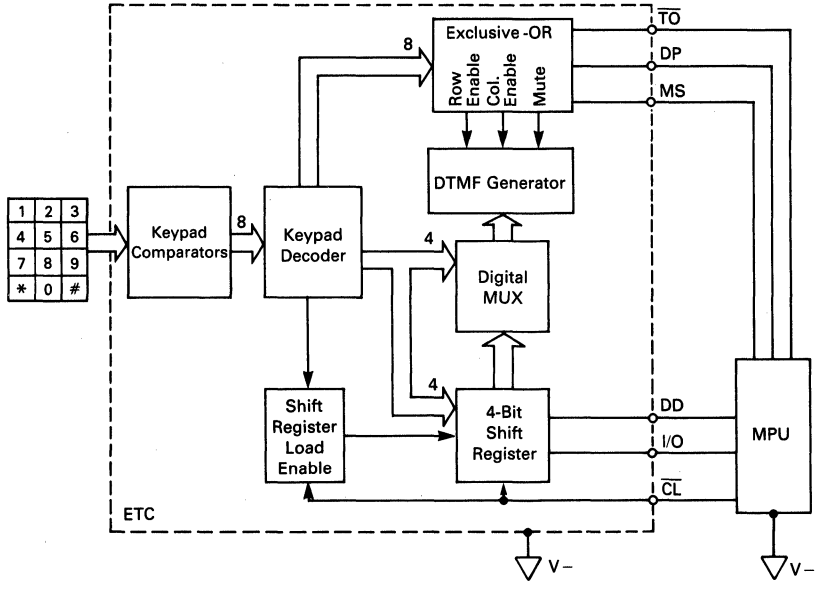


FIGURE 9 — OUTPUT DATA CYCLE

NOTE: $\overline{TO}$ may be low (Tone generator enabled) if desired.

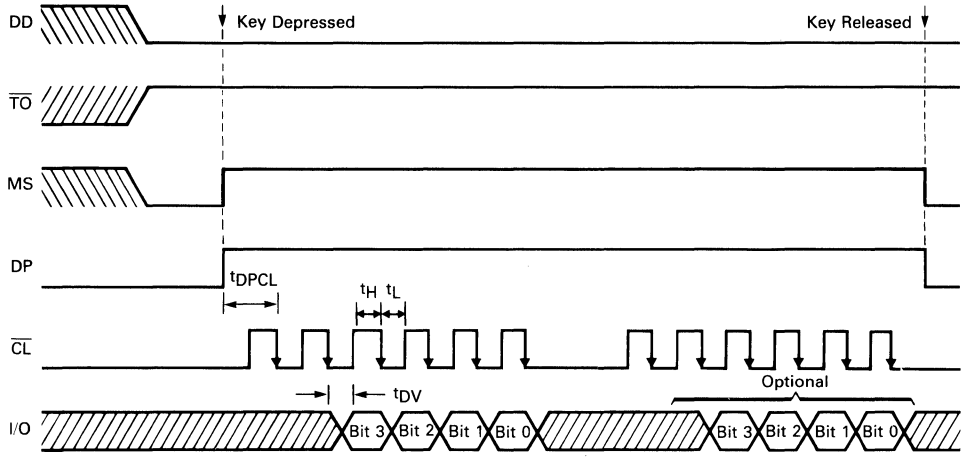


FIGURE 10 — INPUT DATA CYCLE

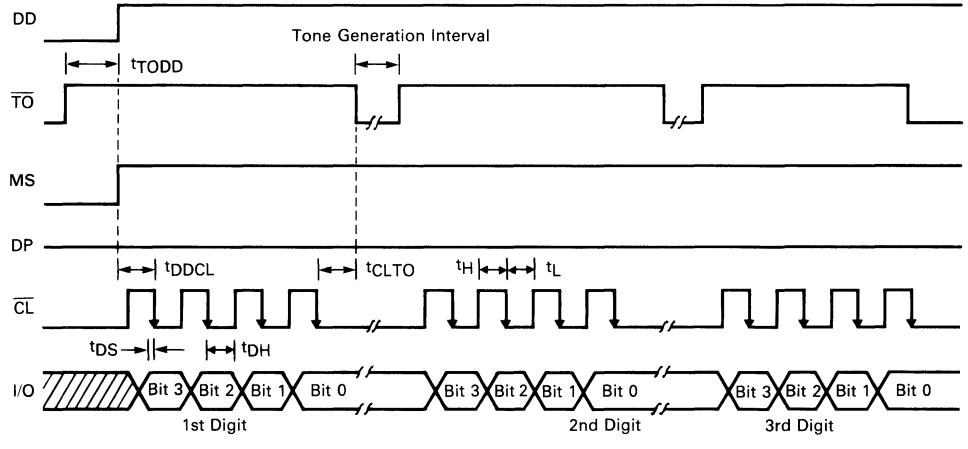


TABLE 1 — FREQUENCY SYNTHESIZER ERRORS

	DTMF Standard (Hz)	Tone Output Frequency with 500 kHz Oscillator	% Deviation from Standard
Row 1	697	696.4	−0.086
Row 2	770	769.2	−0.104
Row 3	852	853.2	+0.141
Row 4	941	939.8	−0.128
Column 1	1209	1207.7	−0.108
Column 2	1336	1336.9	+0.067
Column 3	1477	1479.3	+0.156
Column 4	1633	1634.0	+0.061

TABLE 2 — TIMING LIMITATIONS

Symbol	Parameter	Min	Typ	Max	Unit	Ref
f_{CL}	Clock Frequency	0	20	30	kHz	
t_H	Clock High Time	15	—	—	μs	Figs. 9,10
t_L	Clock Low Time	15	—	—	μs	Figs. 9,10
t_r, t_f	Clock Rise, Fall Time	—	—	2.0	μs	
t_{DV}	Clock Transition to Data Valid	—	—	10	μs	Fig. 9
t_{DPCL}	Time from DP High to $\overline{CL}$ Low	20	—	—	μs	Fig. 9
t_{DDCL}	Time from DD High to $\overline{CL}$ Low	20	—	—	μs	Fig. 10
t_{DS}	Data Setup Time	10	—	—	μs	Fig. 10
t_{DH}	Data Hold Time	10	—	—	μs	Fig. 10
t_{CLTO}	Time from $\overline{CL}$ Low to $\overline{TO}$ Low	10	—	—	μs	Fig. 10
t_{TODD}	Time from $\overline{TO}$ High to DD High	20	—	—	μs	Fig. 10

PIN DESCRIPTION

(See Figure 45 for external component identifications.)

PIN (PLCC)	PIN (DIP)	Designation	Function
1–4	1–4	R1–R4	Keypad inputs for Rows 1 through 4. When open, internal 8.0 kΩ resistors pull up the row inputs to a regulated (≈0.5 volt) supply. In normal operation, a row and a column input are connected through a SPST switch by the telephone keypad. Row inputs can also be activated by a Logic "0" (<250 mV) from a microprocessor port.
7–10	5–8	C1–C4	Keypad inputs for Columns 1 through 4. When open, internal 8.0 kΩ resistors pull down the column inputs to V−. In normal operation, connecting any column input to any row input produces the respective row and column DTMF tones. In addition to being connected to a row input, column inputs can be activated by a Logic "1" (>250 mV and <1.0 volt).
11	9	DP	Depressed Pushbutton (Output) — Normally low; A Logic "1" indicates one and only one, button of the DTMF keypad is depressed.
12	10	$\overline{TO}$	$\overline{\text{Tone Output}}$ (Input) — When a Logic "1," disables the DTMF generator. Keypad is not disabled.
13	11	MS	Mute/Single Tone (Output) — A Logic "1" indicates the tone generator is enabled. A Logic "0" indicates tone generator is disabled.
14	12	A+	MPU Power Supply (Input) — Enables pullups on the microprocessor section outputs. Additionally, this voltage will power the entire circuit (except Tone Ringer) in the absence of voltage at V+.
15	13	I/O	Input/Output — Serial Input or Output data (determined by DD input) to or from the microprocessor for storing or retrieving telephone numbers. Guaranteed to be a Logic "1" on powerup if DD = Logic "0."
16	14	DD	Data Direction (Input) — Determines direction of data flow through I/O pin. As a Logic "1," I/O is an input to the DTMF generator. As a Logic "0," I/O outputs keypad entries to the microprocessor.
17	15	$\overline{CL}$	$\overline{\text{Clock}}$ (Input) — Serially shifts data in or out of I/O pin. Data is transferred on negative edge typically at 20 kHz.
18,19	16,17	CR1, CR2	Ceramic Resonator oscillator input and feedback terminals, respectively. The DTMF dialer is intended to operate with a 500 kHz ceramic resonator from which row and column tones are synthesized.
31	28	CAL	Amplitude CALibration terminal for DTMF dialer. Resistor R14 from the CAL pin to V− controls the DTMF output signal level at Tip and Ring.
38	35	FB	FeedBack terminal for DTMF output. Capacitor C14 connected from FB to V+ provides ac feedback to reduce the output impedance to Tip and Ring when tone dialing.
32	29	VR	Voltage Regulator output terminal. VR is the output of a 1.1 volt voltage regulator which supplies power to the speech network amplifiers and DTMF generator during signaling. To improve regulator efficiency at low line current conditions, an external PNP pass-transistor T1 is used in the regulator circuit. Capacitor C9 frequency compensates the VR regulator to prevent oscillation.
36	33	BP	Base of a PNP Pass-transistor. Under long-loop conditions where low line voltages would cause VR to fall below 1.1 volts, BP drives the PNP transistor T1 into saturation, thereby minimizing the voltage drop across the pass transistor. At line voltages which maintain VR above 1.1 volts, BP biases T1 in the linear region thereby regulating the VR voltage. Transistor T1 also couples the ac speech signals from the transmit amplifier to Tip and Ring at V+.
37	34	V+	The more positive input to the regulator, speech, and DTMF sections connected to Tip and Ring through the polarity guard diode bridge.
33	30	V−	The dc common (more negative input) connected to Tip and Ring through the polarity guard bridge.
35	32	LR	DC Load Resistor. Resistor R4 from LR to V− determines the dc input resistance at Tip and Ring. This resistor is external not only to enable programming the dc resistance but also to avoid high on-chip power dissipation with short telephone lines. It acts as a shunt load conducting the excess dc line current. At low line voltages (<3.0 volts), no current flows through LR.
34	31	LC	DC Load Capacitor. Capacitor C11 from LC to V− forms a low-pass filter which prevents the resistor at LR from loading ac speech and DTMF signals.
22	20	MIC	MICrophone negative supply terminal. The dc current from the electret microphone is returned to V− through the MIC terminal which is connected to the collector of an on-chip NPN transistor. The base of this transistor is controlled either internally by the mute signal from the DTMF generator, or externally by the logic input pin MM.

(continued)

PIN DESCRIPTION (continued)

PIN (PLCC)	PIN (DIP)	Designation	Function
20	18	MM	Microphone Mute. The MM pin provides a means to mute the microphone in response to a digital control signal. When this pin is connected to a Logic "1" (>2.0 V) the microphone dc return path through the MIC terminal is disabled.
25	22	TXI	Transmit amplifier Input. TXI is the input to the transmit amplifier from an electret microphone. AC coupling capacitors allow the dc offset at TXI to be maintained approximately 0.6 V above V− by feedback through resistor R11 from TXO.
24	21	TXL	Transmit Input Limiter. An internal variable resistance element at the TXL terminal controls the transmitter input level to prevent clipping with high signal levels. Coupling capacitors C4 and C5 prevent dc current flow through TXL. The dynamic range of the transmit peak limiter is controlled by resistors R12 and R13.
26	23	TXO	Transmit Amplifier Output. The transmit amplifier output drives ac current through the voltage regulator pass-transistor T1 via resistor R10. The dc bias voltage at TXO is typically 0.6 volts above V−. The transmit amplifier gain is controlled by the R11/(R12 + R13) ratio.
21	19	AGC	Automatic Gain Control low-pass filter terminal. Capacitor C3 connected between AGC and VR sets the attack and decay time of the transmit limiter circuit. This capacitor also aids in reducing clicks in the receiver due to hook-switch transients and DTMF on/off transients. In conjunction with internal resistors, C3 (1.0 μF) forms a timer which mutes the receiver amplifier for approximately 20 milliseconds after the user goes off-hook or releases a DTMF Key.
30	27	RXO	Receiver Amplifier Output. This terminal is connected to the open-collector NPN output transistor of the receiver amplifier. DC bias current for the output device is sourced through the receiver from VR. The bias voltage at RXO is typically 0.6 volts above the V−. Capacitor C10 from RXO to VR provides frequency compensation for the receiver amplifier.
29	26	RXI	Receiver Amplifier Input. RXI is the input terminal of the receiver amplifier which is driven by ac signals from V+ and STA. Input coupling capacitor C8 allows RXI to be biased approximately 0.6 volts above the V− via feedback resistor R6.
28	25	RM	Receiver Amplifier Mute. A switched resistance at the RM terminal attenuates the receiver amplifier input signal produced by DTMF dialing tones at V+. RM also mutes clicks at the receiver which result from keypad or hook switch transitions. The ac resistance at RM is typically 540 Ω in the mute mode and 200 kΩ otherwise. Coupling capacitors C7 and C8 prevent dc current flow through RM.
27	24	STA	SideTone Amplifier output. STA is the output of the sidetone inverter amplifier whose input is driven by the transmit signal at TXO. The inverted transmit signal from STA subtracts from the receiver amplifier input current from V+, thus reducing the receiver sidetone level. Since the transmitted signal at V+ is phase shifted with respect to TXO by the reactive impedance of the phone line, the signal from STA must be similarly phase-shifted in order to provide adequate sidetone reduction. This phase relationship between the transmit signal at TXO and the sidetone cancellation signal from STA is controlled by R8, R9, and C6.
41	37	TRS	Tone Ringer Input Sense. TRS is the most positive input terminal of the tone ringer and the reference for the threshold detector.
42	38	TRI	Tone Ringer Input terminal. TRI is the positive supply voltage terminal for tone ringer circuitry. Current is supplied to TRI through resistor R2. When the average voltage across R2 exceeds an internal reference voltage (typically 1.6 volts) the tone ringer output is enabled.
44	40	TRF	Tone Ringer Input Filter capacitor terminal. Capacitor C16 connected from TRF to TRS forms a low-pass filter. This filter averages the signal across resistor R2 and presents this dc voltage to the input of the threshold detector. Line voltage transients are rejected if the duration is insufficient to charge C16 to 1.6 volts.
40	36	TRC	Tone Ringer oscillator Capacitor and resistor terminal. The relaxation oscillator frequency f_O is set by resistor R3 and capacitor C13 connected from TRC to V−. Typically, $f_O = (R3C13 + 8.0\ \mu s)^{-1}$.
43	39	TRO	Tone Ringer Output terminal. The frequency of the square wave output signal at TRO alternates from $f_O/8$ to $f_O/10$ at a warble rate of $f_O/640$. Typical output frequencies are 1000 Hz and 800 Hz with a 12.5 Hz warble rate. TRO sources or sinks up to 20 mA to produce an output voltage swing of 18 volts peak-to-peak across the piezo transducer. Tone ringer volume control can be implemented by a variable resistor in series with the piezo transducer.

ELECTRICAL CHARACTERISTICS (T_A = 25°C)

KEYPAD INTERFACE CIRCUIT

Characteristic	Test Method	Symbol	Min	Typ	Max	Unit
Row Input Pullup Resistance m^{th} Row Terminal: m = 1,2,3,4	7	R_{Rm}	4.0	8.0	11	kΩ
Column Input Pulldown Resistance n^{th} Column Terminal: n = 1,2,3,4	8	R_{Cn}	4.0	8.0	11	kΩ
Ratio of Row-to-Column Input Resistances $K_{m,n} = \frac{R_{Rm}, \; m = 1,2,3,4}{R_{Cn} \quad n = 1,2,3,4}$	7 & 8	$K_{m,n}$	0.88	1.0	1.12	—
Row Terminal Open Circuit Voltage	7a	V_{ROC}	280	380	500	mVdc
Row Threshold Voltage for m^{th} Row Terminal: m = 1,2,3,4	9	V_{Rm}	0.70 V_{ROC}	—	—	Vdc
Column Threshold Voltage for n^{th} Column Terminal: n = 1,2,3,4	10	V_{Cn}	—	—	0.39 V_{ROC}	Vdc

MICROPROCESSOR INTERFACE

Voltage Regulator Output A+ Regulator	29	$V_{R/A+}$	0.95	1.1	1.3	V
A+ Input Current Off-Hook	28a	I_A(off)	300	500	700	μA
A+ Input Current On-Hook	28b	I_A(on)	4.0	6.0	9.0	mA
Input Resistance (DD, $\overline{TO}$, $\overline{CL}$)	30	R_{in}	50	100	150	kΩ
Input Current (I/O)	31	I_{in}	—	80	200	μA
Input High Voltage (DD, $\overline{TO}$, $\overline{CL}$, I/O)	—	V_{IH}	2.0	—	A+	V
Input Low Voltage (DD, $\overline{TO}$, $\overline{CL}$, I/O)	—	V_{IL}	—	—	0.8	V
Output High Voltage (MS, DP, I/O)	32	V_{OH}	2.4	4.0	—	V
Output Low Voltage (MS, DP, I/O)	33	V_{OL}	—	0.1	0.4	V

LINE VOLTAGE REGULATOR

Voltage Regulator Output	1a	V_R	1.0	1.1	1.2	Volts
V+ Current in DTMF Mode	2a	I_{DT}	8.0	12	14	mA
Change in I_{DT} with Change in V+ Voltage	2b	ΔI_{DT}	—	0.8	2.0	mA
V+ Current in Speech Mode		I_{SP}				mA
V+ = 1.7 V	1b		3.5	5.0	7.0	
V+ = 5.0 V	1c		8.0	11	15	
Speech to DTMF Mode Current Difference	3	ΔI_{TR}	−2.0	2.0	3.5	mA
LR Level Shift		ΔV_{LR}				Vdc
V+ = 5.0 V, I_{LR} = 10 mA	4a		2.5	2.9	3.5	
V+ = 18 V, I_{LR} = 110 mA	4b		2.8	3.3	4.0	
LC Terminal Resistance	5	R_{LC}	30	50	75	kΩ
Load Regulation	6	ΔV_R	−20	−6.0	20	mVdc

ELECTRICAL CHARACTERISTICS (continued)

SPEECH NETWORK

Characteristic	Test Method	Symbol	Min	Typ	Max	Unit
MIC Terminal Saturation Voltage	20	V_{MIC}	—	60	125	mVdc
MIC Terminal Leakage Current	21a	I_{MIC}	—	0.0	12.0	μA
MM Terminal Input Resistance	21b	R_{MM}	50	100	170	kΩ
TXO Terminal Bias	22a	B_{TXO}	0.46	0.53	0.62	—
TXI Terminal Input Bias Current	22b	I_{TXI}	—	50	250	nA
TXO Terminal Positive Swing	22c	$V_{TXO(+)}$	—	25	60	mVdc
TXO Terminal Negative Swing	22d	$V_{TXO(-)}$	—	130	200	mVdc
Transmit Amplifier Closed-Loop Gain	23a	G_{TX}	16.5	19	20	V/V
Sidetone Amplifier Gain	23b	G_{STA}	0.41	0.45	0.55	V/V
STA Terminal Output Current	24	I_{STA}	50	100	250	μA
RXO Terminal Bias	25a	B_{RXO}	0.46	0.62	0.62	—
RXI Terminal Input Bias Current	25b	I_{RXI}	—	100	400	nA
RXO Terminal Positive Swing	25c	$V_{RXO(+)}$	—	1.0	20	mVdc
RXO Terminal Negative Swing	25d	$V_{RXO(-)}$	—	40	100	mVdc
TXL Terminal OFF Resistance	26a	$R_{TXL(OFF)}$	125	200	300	kΩ
TXL Terminal ON Resistance	26b	$R_{TXL(ON)}$	—	20	100	Ω
RM Terminal OFF Resistance	27a	$R_{RM(OFF)}$	125	180	300	kΩ
RM Terminal ON Resistance	27b	$R_{RM(ON)}$	410	570	770	Ω

DTMF GENERATOR

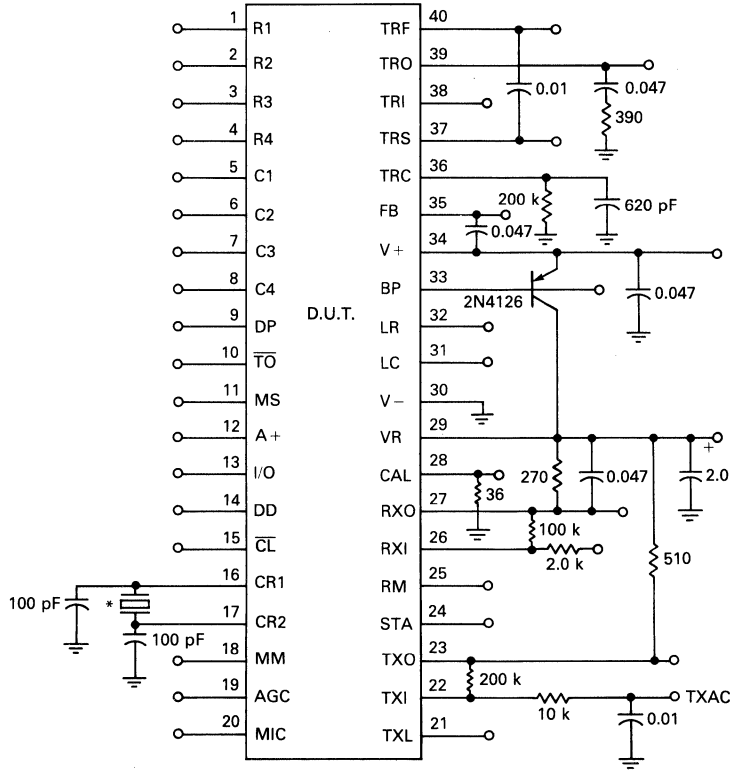
Row Tone Frequency	Row 1	11a, 11b	f_{Rm}	692.9	696.4	699.9	Hz
	Row 2			765.3	769.2	773.0	
	Row 3			848.9	853.2	857.5	
	Row 4			935.1	939.8	944.5	
Column Tone Frequency	Column 1	11c, 11d	f_{Cn}	1201.6	1207.7	1213.7	Hz
	Column 2			1330.2	1336.9	1343.6	
	Column 3			1471.9	1479.3	1486.7	
	Column 4			1625.2	1633.4	1641.5	
Row Tone Amplitude		11e	V_{Row}	0.34	0.39	0.50	V_{rms}
Column Tone Amplitude		11f	V_{Col}	0.43	0.48	0.62	V_{rms}
Column Tone Pre-emphasis		11g	dB_{CR}	0.5	1.8	3.0	dB
DTMF Distortion		12	% Dis	—	4.0	6.0	%
DTMF Output Resistance		13	R_o	1.0	2.5	3.0	kΩ

ELECTRICAL CHARACTERISTICS (continued)

TONE RINGER

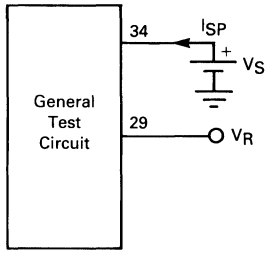
Characteristic	Test Method	Symbol	Min	Typ	Max	Unit
TRI Terminal Voltage	14	V_{TRI}	20	21.5	23	Vdc
TRS Terminal Input Current		I_{TRS}				
V_{TRS} = 24 volts	15a		70	120	170	μA
V_{TRS} = 30 volts	15b		0.4	0.8	1.5	mA
TRF Threshold Voltage	16a	V_{TRF}	1.2	1.6	1.9	Vdc
TRF Threshold Hysteresis	16b	ΔV_{TRF}	100	200	400	mVdc
TRF Filter Resistance	17	R_{TRF}	30	50	75	kΩ
High Tone Frequency	18	f_H	920	1000	1080	Hz
Low Tone Frequency	18	f_L	736	800	864	Hz
Warble Frequency	18	f_W	11.5	12.5	13.5	Hz
Tone Ringer Output Voltage	19	$V_{o(p-p)}$	18	20	22	Vp-p

FIGURE 11 — GENERAL TEST CIRCUIT



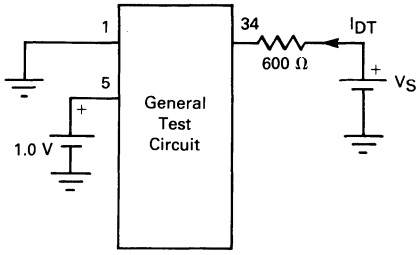
Notes:
1. *Selected ceramic resonator: 500 kHz ±2.0 kHz.
2. Capacitances in μF unless noted.
3. All resistances in ohms.
4. Pin outs shown are for the 40 pin DIP.

FIGURE 12 — TEST ONE



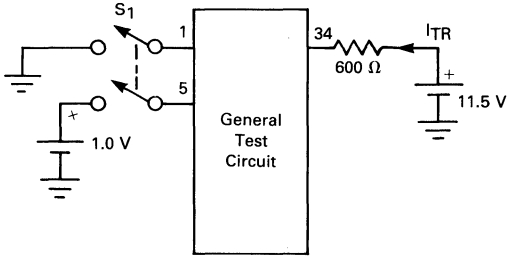
a. Measure V_R with V_S = 1.7 V
b. Measure I_{SP} with V_S = 1.7 V
c. Measure I_{SP} with V_S = 5.0 V

FIGURE 13 — TEST TWO



a. Measure I_{DT} with V_S = 11.5 V
b. Measure I_{DT} with V_S = 26 V. Calculate
$\Delta I_{DT} = I_{DT}\Big|_{26\ V} - I_{DT}\Big|_{11.5\ V}$

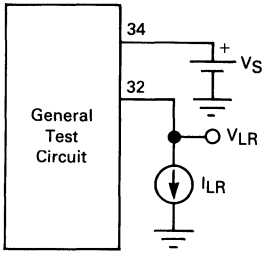
FIGURE 14 — TEST THREE



With S_1 open measure I_{TR}. Close S_1 and again measure I_{TR}. Calculate:

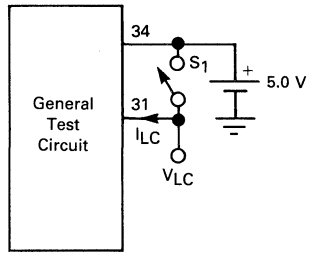
$\Delta I_{TR} = I_{TR}\Big|_{S_1\ Closed} - I_{TR}\Big|_{S_1\ Open}$

FIGURE 15 — TEST FOUR



a. Set V_S = 5.0 V and I_{LR} = 10 mA. Measure V_{LR}. Calculate $\Delta V_{LR} = V_S - V_{LR}$
b. Repeat Test 4a with V_S = 18 V and I_{LR} = 110 mA

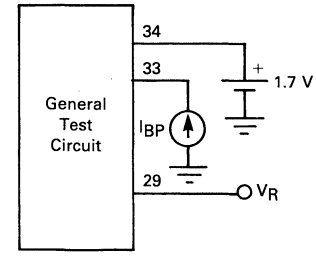
FIGURE 16 — TEST FIVE



With S_1 open measure V_{LC}.
Close S_1 and measure I_{LC}.
Calculate:

$$R_{LC} = \frac{5.0 - V_{LC}}{I_{LC}}$$

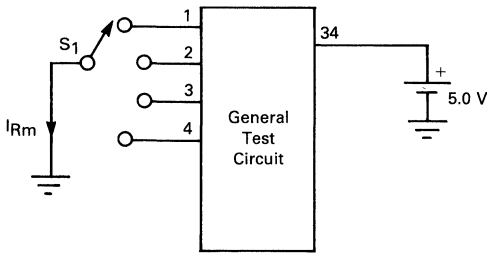
FIGURE 17 — TEST SIX



Set I_{BP} = 0.0 μA and measure V_R.
Set I_{BP} = 150 μA and measure V_R. Calculate:

$$\Delta V_R = V_R\Big|_{0.0\ \mu A} - V_R\Big|_{150\ \mu A}$$

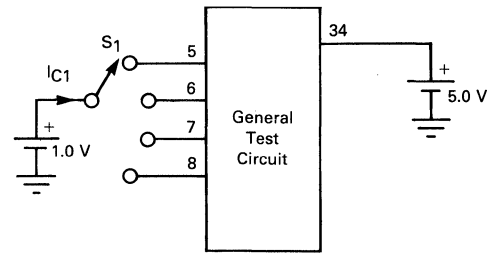
FIGURE 18 — TEST SEVEN



Subscript m corresponds to row number.

a. Set S_1 to Terminal 2 and measure voltage at Terminal 1 (V_{ROC}).
b. Set S_1 to Terminal 1 (m = 1) and measure I_{R1}. Calculate:
$R_{R1} = V_{ROC} \div I_{R1}$
c,d,e. Repeat Test 7b for m = 2,3,4.

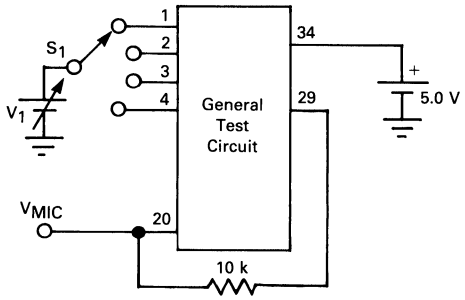
FIGURE 19 — TEST EIGHT



Subscript n corresponds to column number.

a. Set S_1 to Terminal 5 (n = 1) and measure I_{C1}. Calculate:
$R_{C1} = 1.0\ V \div I_{C1}$
b,c,d. Repeat Test 8a for n = 2,3,4.

FIGURE 20 — TEST NINE

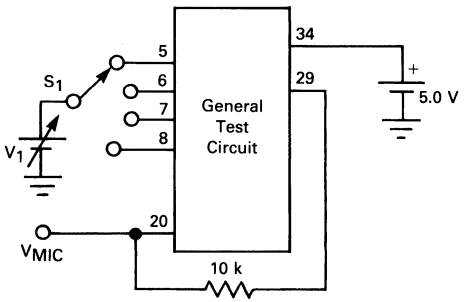


m corresponds to row number.

a. Set S_1 to Terminal 1 (m = 1) with V_1 = 1.0 Vdc. Verify V_{MIC} is Low (V_{MIC} < 0.3 Vdc). Decrease V_1 to 0.70 V_{ROC} and verify V_{MIC} switches high. (V_{MIC} > 0.5 Vdc). V_{ROC} is obtained from Test 7a.

b,c,d. Repeat Test 9a for rows 2,3, and 4. (m = 2,3,4)

FIGURE 21 — TEST TEN

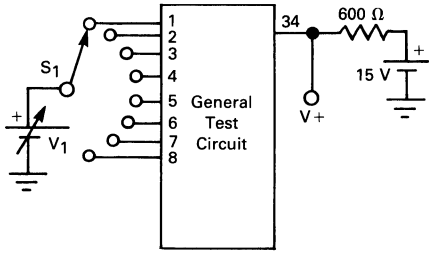


n corresponds to column number.

a. Set S_1 to Terminal 5 (n = 1) with V_1 = 0 Vdc. Verify V_{MIC} is low (V_{MIC} < 0.3 Vdc). Increase V_1 to 0.39 V_{ROC} and verify V_{MIC} switches high, (V_{MIC} > 0.5 Vdc). V_{ROC} is obtained from Test 7a.

b,c,d. Repeat Test 10a for columns 2,3, and 4. (n = 2,3,4)

FIGURE 22 — TEST ELEVEN



m corresponds to row number.
n corresponds to column number.

a. With V_1 = 0.0 V set S_1 to Terminal 1 (m = 1) and measure frequency of tone at V+.

b. Repeat Test 11a for rows 2,3 and 4. (m = 2,3,4).

c. With V_1 = 1.0 V set S_1 to Terminal 5. (n = 1) and measure frequency of tone at V+.

d. Repeat Test for columns 2,3, and 4. (n = 2,3,4).

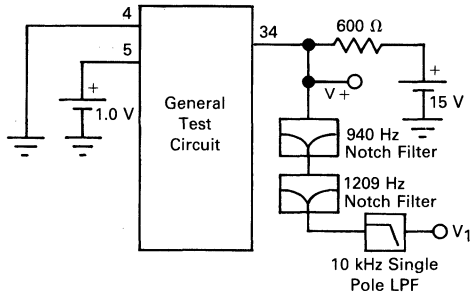
e. Set S_1 to Terminal 4 and V_1 = 0.0 V. Measure row tone amplitude at V+ (V_{ROW}).

f. Set S_1 to Terminal 8 and V_1 = 1.0 V. Measure column tone amplitude at V+. (V_{COL}).

g. Using results of Tests 11e and 11f, calculate:

$$dB_{CR} = 20 \log_{10} \frac{V_{COL}}{V_{ROW}}$$

FIGURE 23 — TEST TWELVE

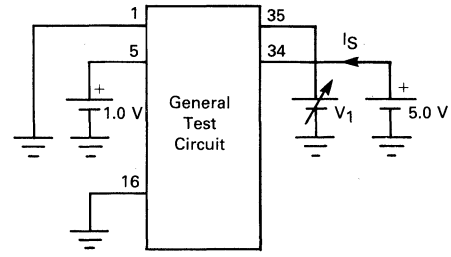


Note: The notch filters must have 50 dB attenuation at their respective center frequencies.

Measure V+ and V_1 with a true rms voltmeter. Calculate:

$$\% \text{ DIS} = \frac{V_1(\text{rms})}{V+(\text{rms})} \times 100$$

FIGURE 24 — TEST THIRTEEN

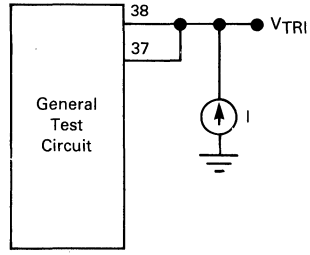


Measure I_S at V_1 = 1.8 V and V_1 = 2.8 V.

Calculate:

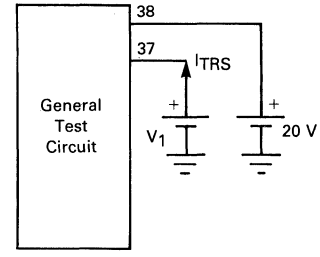
$$R_o = 1.0 \text{ V} \div \left[I_S\Big|_{2.8 \text{ V}} - I_S\Big|_{1.8 \text{ V}} \right]$$

FIGURE 25 — TEST FOURTEEN



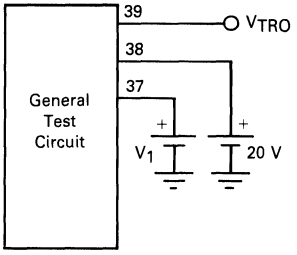
Set I = 1.0 mA and measure V_{TRI}.

FIGURE 26 — TEST FIFTEEN



a. Measure I_{TRS} with V_1 = 24 V.
b. Measure I_{TRS} with V_1 = 30 V.

FIGURE 27 — TEST SIXTEEN



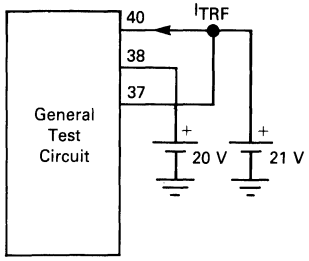
a. Increase V_1 from 21 V until V_{TRO} switches on. Note that V_{TRO} will be an 16 V_{pp} square wave. Record this value of V_1. Calculate:

$V_{TRF} = V_1 - 20\ V$

b. Decrease V_1 from its setting in Test 16a until V_{TRO} ceases switching. Record this value of V_1. Calculate:

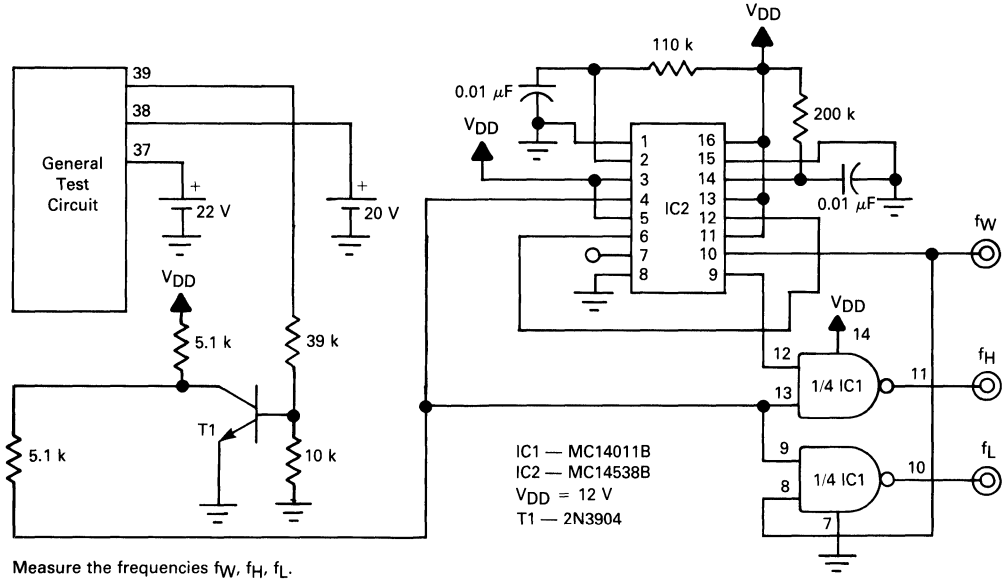
$\Delta V_{TRF} = V_1\big|_{\text{Test 16a}} - V_1\big|_{\text{Test 16b}}$

FIGURE 28 — TEST SEVENTEEN



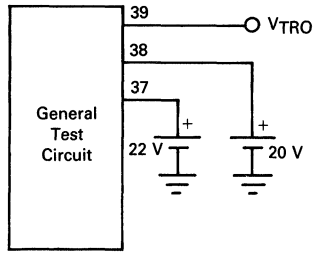
Measure I_{TRF}. Calculate: $R_{TRF} = 1.0 \div I_{TRF}$.

FIGURE 29 — TEST EIGHTEEN



Measure the frequencies f_W, f_H, f_L.

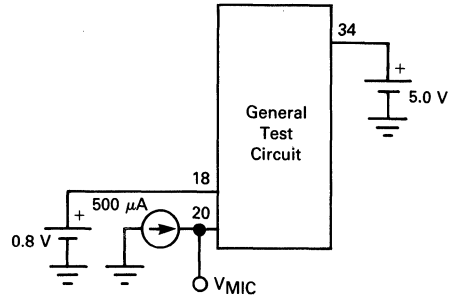
FIGURE 30 — TEST NINETEEN



Measure V_{TRO} peak-to-peak voltage swing. Using V_{TRI} from Test 14 Calculate:

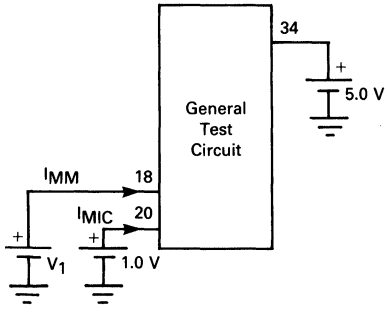
$V_{o(p-p)} = V_{TRI} - 20\ V + V_{TRO}$

FIGURE 31 — TEST TWENTY



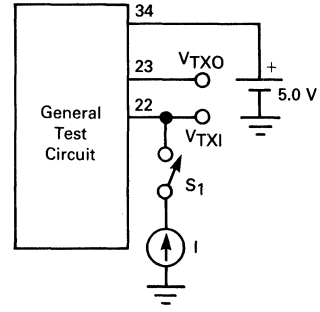
Measure V_{MIC}

FIGURE 32 — TEST TWENTY-ONE



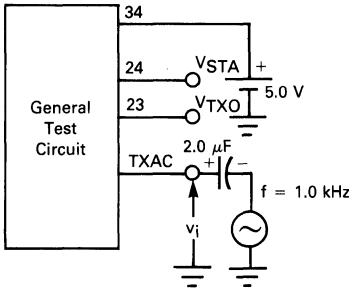
a. Set V_1 = 2.0 V and measure I_{MIC}.
b. Set V_1 = 5.0 V and measure I_{MM}. Calculate: $R_{MM} = 5.0\ V \div I_{MM}$

FIGURE 33 — TEST TWENTY-TWO



a. With S_1 open, measure V_{TXO}. Using V_R obtained in Test 1 Calculate: $B_{TXO} = V_{TXO} \div V_R$
b. With S_1 open, measure V_{TXO} and V_{TXI}. Calculate: $I_{TXI} = (V_{TXO} - V_{TXI}) \div 200\ k\Omega$
c. Close S_1 and set I = −10 μA. Measure V_{TXO}. Calculate: $V_{TXO}(+) = V_R - V_{TXO}$ where V_R is obtained from Test 1.
d. Close S_1 and set I = +10 μA. Measure V_{TXO}. $V_{TXO}(-) = V_{TXO}$.

FIGURE 34 — TEST TWENTY-THREE



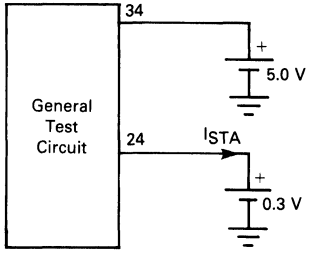
a. Set the generator for v_i = 3.0 mV_{rms}. Measure ac voltage V_{TXO}. Calculate:

$$G_{TX} = \frac{V_{TXO}}{v_i}$$

b. Measure ac voltage V_{STA}. Using V_{TXO} from Test 23a calculate:

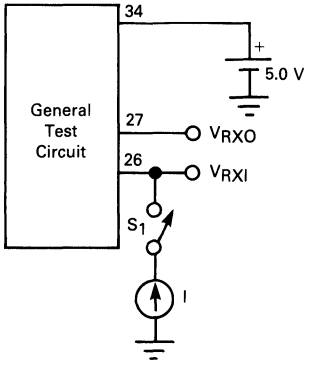
$$G_{STA} = \frac{V_{STA}}{V_{TXO}}$$

FIGURE 35 — TEST TWENTY-FOUR



Measure I_{STA}.

FIGURE 36 — TEST TWENTY-FIVE



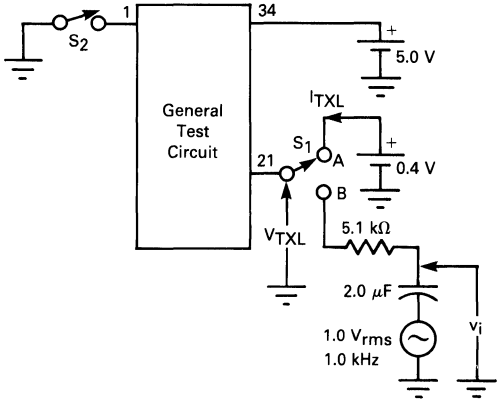
a. With S_1 open, measure V_{RXO}. Using V_R obtained in Test 1, calculate: $B_{RXO} = V_{RXO} \div V_R$.

b. With S_1 open, measure V_{RXO} and V_{RXI}. Calculate: $I_{RXI} = (V_{RXO} - V_{RX1}) \div 100\ k\Omega$

c. Close S_1 and set I = −10 μA. Measure V_{RXO}. Using V_R obtained in Test 1, calculate: $V_{RXO}(+) = V_R - V_{RXO}$.

d. Close S_1 and set I = +10 μA and measure V_{RXO}. $V_{RXO}(-) = V_{RXO}$.

FIGURE 37 — TEST TWENTY-SIX

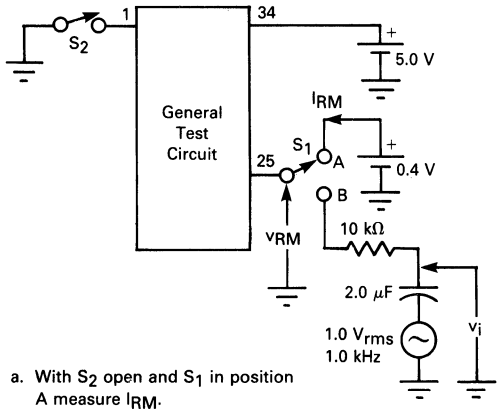


a. Set S_1 to position A with S_2 open. Measure I_{TXL}. Calculate: R_{TXL} (OFF) = 0.4 V ÷ I_{TXL}.

b. Set S_1 to position B and close S_2. Measure ac voltages v_i and V_{TXL}. Calculate:

$$R_{TXL}\ (ON) = \frac{V_{TXL}}{v_i - V_{TXL}} \times 5.1\ k\Omega$$

FIGURE 38 — TEST TWENTY-SEVEN



a. With S_2 open and S_1 in position A measure I_{RM}.

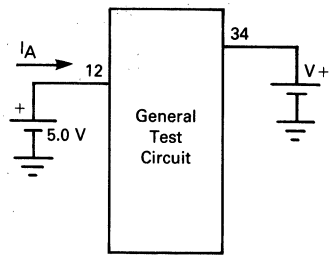
Calculate: $R_{RM}(OFF) = 0.4\ V \div I_{RM}$

b. Close S_2 and switch S_1 to position B. Measure ac voltages v_i and V_{RM}.

Calculate:

$$R_{RM}(ON) = \frac{V_{RM}}{v_i - V_{RM}} \times 10\ k\Omega$$

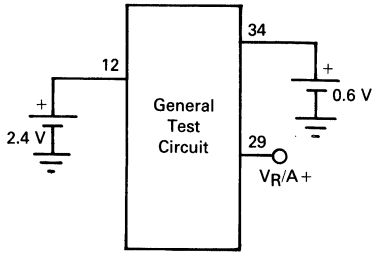
FIGURE 39 — TEST TWENTY-EIGHT



a. Set V+ = 1.4 V. Measure $I_A(OFF)$

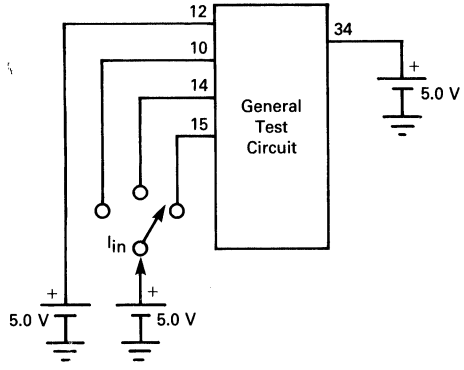
b. Set V+ = 0.6 V. Measure $I_A(ON)$

FIGURE 40 — TEST TWENTY-NINE



Measure $V_R/A+$

FIGURE 41 — TEST THIRTY



Measure I_{in} at each of three inputs. For each, calculate: $R_{in} = 5.0\ V/I_{in}$

FIGURE 42 — TEST THIRTY-ONE

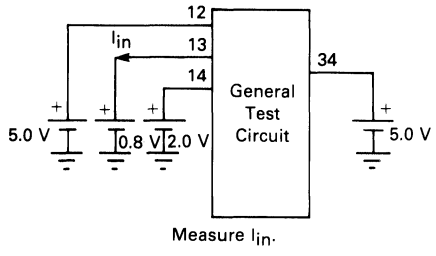
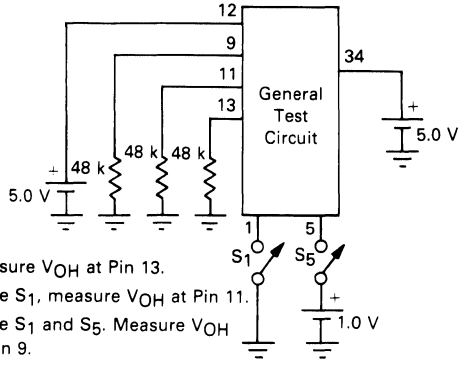
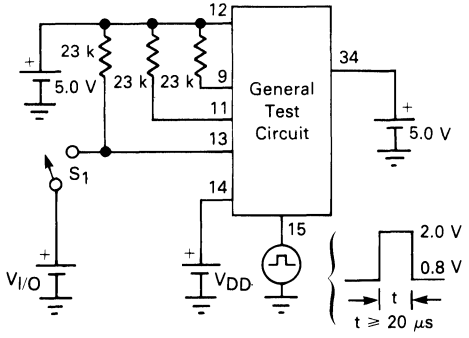


FIGURE 43 — TEST THIRTY-TWO



a. Measure V_{OH} at Pin 13.
b. Close S_1, measure V_{OH} at Pin 11.
c. Close S_1 and S_5. Measure V_{OH} at Pin 9.

FIGURE 44 — TEST THIRTY-THREE



a. Set V_{DD} to 0.8 V Measure V_{OL} voltages at Pins 9 and 11.
b. Close S_1. Force $V_{I/O}$ to 0.8 V and V_{DD} to 2.0 V. Apply 4 clock pulses to Pin 15. Open S_1 and decrease V_{DD} to 0.8 V. Measure V_{OL} at Pin 13.

APPLICATIONS INFORMATION

Figure 45 specifies a typical application circuit for the MC34010. Complete listings of external components are provided at the end of this section along with nominal component values.

The hook switch and polarity guard bridge configuration in Figure 45 is one of several options. If two bridges are used, one for the tone ringer and the other for speech and dialer circuits, then the hook switch can be simplified. Component values should be varied to optimize telephone performance parameters for each application. The relationships between the application circuit components and certain telephone parameters are briefly described in the following:

On-Hook Input Impedance

R1, C17, and Z3 are the significant components for on-hook impedance. C17 dominates at low frequencies, R1 at high frequencies and Z3 provides the non-linearity required for 2.5 V and 10 V impedance signature tests. C17 must generally be ≤ 1.0 μF to satisfy 5.0 Hz impedance specifications.

Tone Ringer Output Frequencies

R3 and C13 control the frequency (f_o) of a relaxation oscillator. Typically $f_o = (R3C13 + 8.0\ \mu s)^{-1}$. The output tone frequencies are $f_o/10$ and $f_o/8$. The warble rate is $f_o/640$. The tone ringer will operate with f_o from 1.0 kHz to 10 kHz. R3 should be limited to values between 150 k and 300 k.

Tone Ringer Input Threshold

After R1, C17, and Z3 are chosen to satisfy on-hook impedance specifications, R2 is chosen for the desired ring start threshold. Increasing R2 reduces the ac input voltage required to activate the tone ringer output. R2 should be limited to values between 0.8 k and 2.0 kΩ.

Off-Hook DC Resistance

R4 conducts the dc line current in excess of the speech and dialer bias current. Increasing R4 increases the input resistance of the telephone for line currents above 10 mA. R4 should be selected between 30 Ω and 120 Ω.

Off-Hook AC Impedance

The ac input impedance is equal to the receive amplifier load impedance (at RXO) divided by the receive amplifier gain (voltage gain from V+ to RXO). Increasing the impedance of the receiver increases the impedance of the telephone. Increasing the gain of the receiver amplifier decreases the impedance of the telephone.

DTMF Output Amplitude

R14 controls the amplitude of the row and column DTMF tones. Decreasing R14 increases the level of tones generated at V+. The ratio of the row and column tone amplitudes is internally fixed. R14 should be greater than 20 Ω to avoid excessive current in the DTMF output amplifier.

Transmit Output Level

R10 controls the maximum signal amplitude produced at V+ by the transmit amplifier. Decreasing R10 increases the transmit output signal at V+. R10 should be greater than 220 Ω to limit current in the transmit amplifier output.

Transmit Gain

The gain from the microphone to the telephone line varies directly with R11. Increasing R11 increases the signal applied to R10 and the ac current driven through R10 to the telephone line. The closed loop-gain from the microphone to the TXO terminal should be greater than 10 to prevent transmit amplifier oscillations.

Note: Adjustments to transmit level and gain are complicated by the addition of receiver sidetone current to the transmit amplifier output current at V+. Normally the sidetone current from the receiver will increase the transmit signal (if the current in the receiver is in phase with that in R10). Thus the transmit gain and sidetone levels cannot be adjusted independently.

Receiver Gain

Feedback resistor R6 adjusts the gain at the receiver amplifier. Increasing R6 increases the receiver amplifier gain.

Sidetone Level

Sidetone reduction is achieved by the cancellation of receiver amplifier input signals from R9 and R5. R8, R15, and C6 determine the phase of the sidetone balance signal in R9. The ac voltage at the junction of R8 and R9 should be 180° out of phase with the voltage at V+. R9 is selected such that the signal current in R9 is slightly greater than that in R5. This insures that the sidetone current in the receiver adds to the transmit amplifier output current.

Hook-Switch Click Suppression

When the telephone is switched to the off-hook condition C3 charges from 0 volts to a 300 mV bias voltage. During this time interval, receiver clicks are suppressed by a low impedance at the RM terminal. If this click suppression mechanism is desired during a rapid succession of hook switch transitions, then C3 must be quickly discharged when the telephone is on-hook, R16 and S3 provide a rapid discharge path for C3 to reset the click suppression timer. R16 is selected to limit the discharge current in S3 to prevent damage to switch contacts.

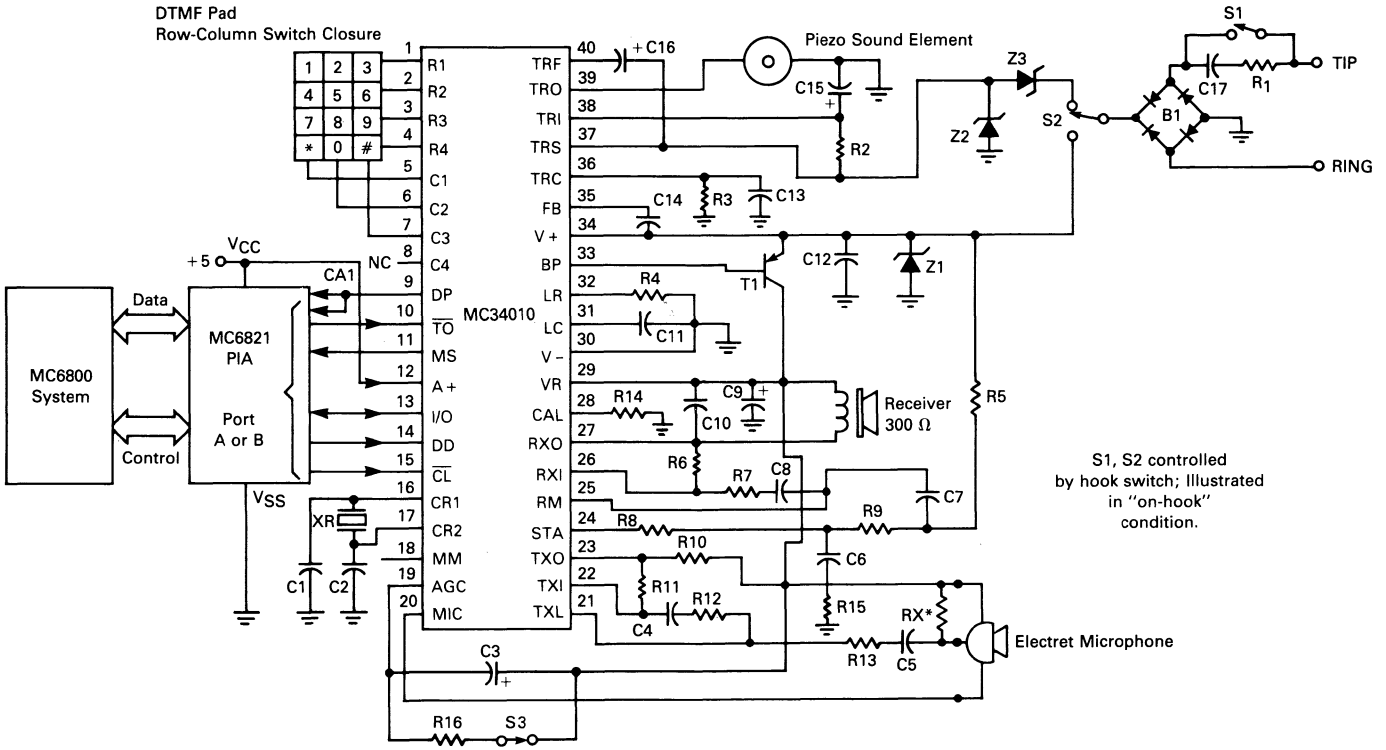
Microprocessor Interface

The six microprocessor interface lines (DP, $\overline{TO}$, MS, DD, I/O, and $\overline{CL}$) can be connected directly to a port, as shown in Figure 47. The DP line (Depressed Pushbutton) is also connected to an interrupt line to signal the microprocessor to begin a read data sequence when storing a number into memory. The MC34010A clock speed requirement is slow enough (typically 20 kHz) so that it is not necessary to divide down the processor's system clock, but rather a port output can be toggled. This facilitates synchronizing the clock and data transfer, eliminating the need for hardware to generate the clock.

The DD pin must be maintained at a Logic "0" when the microprocessor section is not in use, so as to permit normal operation of the keypad.

When the microprocessor interface section is not in use, the supply voltage at Pin 12 (A+) may be disconnected to conserve power. Normally the speech circuitry is powered by the voltage supplied at the V+ terminal (Pin 34) from the telephone lines. During this time, A+ powers only the active pullups on the three microprocessor outputs (DP, MS, and I/O). When the telephone is "on-hook," and V+ falls below 0.6 volts, power is then supplied to the telephone speech and dialer circuitry from A+. Powering the circuit from the A+ pin permits communication with a microprocessor, and/or use of the transmit and receiver amplifiers, while the telephone is "on-hook."

FIGURE 45 — ELECTRONIC TELEPHONE APPLICATION CIRCUIT



*RX used with 2-Terminal mike only.

EXTERNAL COMPONENTS

(Component Labels Referenced to Figure 45)

Capacitors	Nominal Value	Description
C1, C2	100 pF	Ceramic Resonator oscillator capacitors.
C3	1.0 μF, 3.0 V	Transmit limiter low-pass filter capacitor: controls attack and decay time of transmit peak limiter.
C4, C5	0.1 μF	Transmit amplifier input capacitors: prevent dc current flow into TXL pin and attenuate low-frequency noise on microphone lead.
C6	0.05 μF	Sidetone network capacitor: provides phase-shift in sidetone path to match that caused by telephone line reactance.
C7, C8	0.05 μF	Receiver amplifier input capacitors: prevent dc current flow into RM terminal and attenuates low frequency noise on the telephone line.
C9	2.2 μF, 3.0 V	VR regulator capacitor: frequency compensates the VR regulator to prevent oscillation.
C10	0.01 μF	Receiver amplifier output capacitor: frequency compensates the receiver amplifier to prevent oscillation.
C11	0.1 μF	DC load filter capacitor: prevents the dc load circuit from attenuating ac signals on V+.
C12	0.01 μF	Telephone line bypass capacitor: terminates telephone line for high frequency signals and prevents oscillation in the VR regulator.
C13	620 pF	Tone ringer oscillator capacitor: determines clock frequency for tone and warble frequency synthesizers.
C14	0.1 μF	DTMF output feedback capacitor: ac couples feedback around the DTMF output amplifier which reduces output impedance.
C15	4.7 μF, 25 V	Tone ringer input capacitor: filters the rectified tone ringer input signal to smooth the supply potential for oscillator and output buffer.
C16	1.0 μF, 10 V	Tone ringer filter capacitor: integrates the voltage from current sense resistor R2 at the input of the threshold detector.
C17	1.0 μF, 250 Vac Non-polarized	Tone ringer line capacitor: ac couples the tone ringer to the telephone line; partially controls the on-hook input impedance of telephone.

Resistors	Nominal Value	Description
R1	6.8 k	Tone ringer input resistor: limits current into the tone ringer from transients on the telephone line and partially controls the on-hook impedance of the telephone.
R2	1.8 k	Tone ringer current sense resistor: produces a voltage at the input of the threshold detector in proportion to the tone ringer input current.
R3	200 k	Tone ringer oscillator resistor: determines the clock frequency for tone and warble frequency synthesizers.
R4	82, 1.0 W	DC load resistor: conducts all dc line current in excess of the current required for speech or dialing circuits; controls the off-hook dc resistance of the telephone.
R5, R7	150 k, 56 k	Receiver amplifier input resistors: couple ac input signals from the telephone line to the receiver amplifier; signal in R5 subtracts from that in R9 to reduce sidetone in receiver.
R6	200 k	Receiver amplifier feedback resistor: controls the gain of the receiver amplifier.
R8, R9	1.5 k, 30 k	Sidetone network resistors: drive receiver amplifier input with the inverted output signal from the transmitter; phase of signal in R9 should be opposite that in R5.
R10	270	Transmit amplifier load resistor: converts output voltage of transmit amplifier into a current that drives the telephone line; controls the maximum transmit level.
R11	200 k	Transmit amplifier feedback resistor: controls the gain of the transmit amplifier.
R12, R13	4.7 k, 4.7 k	Transmit amplifier input resistors: couple signal from microphone to transmit amplifier; control the dynamic range of the transmit peak limiter.
R14	36	DTMF calibration resistor: controls the output amplitude of the DTMF dialer.
R15	2.0 k	Sidetone network resistor (optional): reduces phase shift in sidetone network at high frequencies.
R16	100	Hook switch click suppression current limit resistor (optional): limits current when S3 discharges C3 after switching to the on-hook condition.
R_X	3.0 k	Microphone bias resistor: sources current from VR to power a 2-terminal electret microphone; R_X is not used with 3-terminal microphones.

EXTERNAL COMPONENTS (continued)

Semiconductors	Electret Mic	Receiver
B1 = MDA101A, or equivalent, or 4-1N4005 T1 = 2N4126 or equivalent Z1 = 18 V, 1.5 W, 1N5931A Z2 = 30 V, 1.5 W, 1N5936A Z3 = 4.7 V, 1/2 W, 1N750 XR — muRata Erie CSB 500 kHz Resonator, or equivalent Piezo — PBL 5030BC Toko Buzzer or equivalent	2 Terminal, Primo EM-95 (Use R_X) or equivalent 3 Terminal, Primo 07A181P (Remove R_X) or equivalent	Primo Model DH-34 (300 Ω) or equivalent

Motorola Inc. does not endorse or warrant the suppliers referenced.

MC34012-1
MC34012-2
MC34012-3

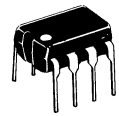
2

TELEPHONE TONE RINGER

- Complete Telephone Bell Replacement Circuit with Minimum External Components
- On-Chip Diode Bridge and Transient Protection
- Direct Drive for Piezoelectric Transducers
- Base Frequency Options—MC34012-1: 1.0 kHz
  MC34012-2: 2.0 kHz
  MC34012-3: 500 Hz
- Input Impedance Signature Meets Bell and EIA Standards
- Rejects Rotary Dial Transients

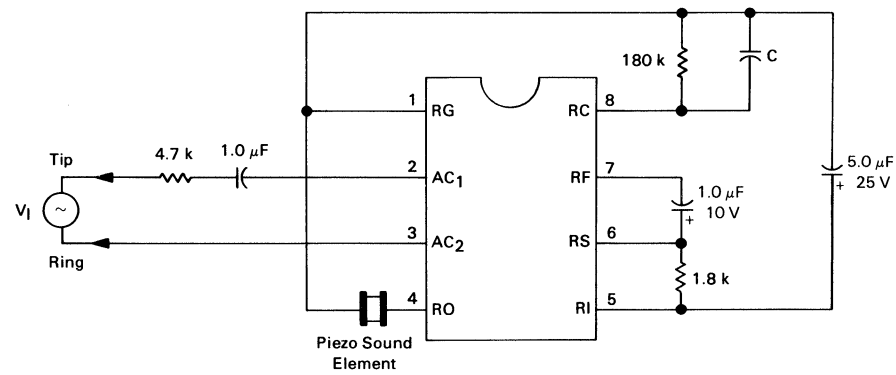
TELEPHONE TONE RINGER

BIPOLAR LINEAR/I^2L



PLASTIC PACKAGE
CASE 626

APPLICATION CIRCUIT



MC34012-1: C = 1000 pF
MC34012-2: C = 500 pF
MC34012-3: C = 2000 pF

APPLICATION CIRCUIT PERFORMANCE

Characteristic	Typical Value	Units
Output Tone Frequencies MC34012-1 MC34012-2 MC34012-3 Warble Frequency	 832/1040 1664/2080 416/520 13	 Hz
Output Voltage ($V_I \geq 60\ V_{rms}$, 20 Hz)	20	V_{p-p}
Output Duty Cycle	50	%
Ringing Start Input Voltage (20 Hz)	36	V_{rms}
Ringing Stop Input Voltage (20 Hz)	28	V_{rms}
Maximum ac Input Voltage ($\leq$ 68 Hz)	150	V_{rms}
Impedance When Ringing $V_I = 40\ V_{rms}$, 15 Hz $V_I = 130\ V_{rms}$, 23 Hz	 20 10	kΩ
Impedance When Not Ringing $V_I = 10\ V_{rms}$, 24 Hz $V_I = 2.5\ V_{rms}$, 24 Hz $V_I = 10\ V_{rms}$, 5.0 Hz $V_I = 3.0\ V_{rms}$, 200–3200 Hz	 28 >1.0 55 >1.0	 kΩ MΩ kΩ MΩ
Maximum Transient Input Voltage ($T \leq 2.0$ ms)	1500	V

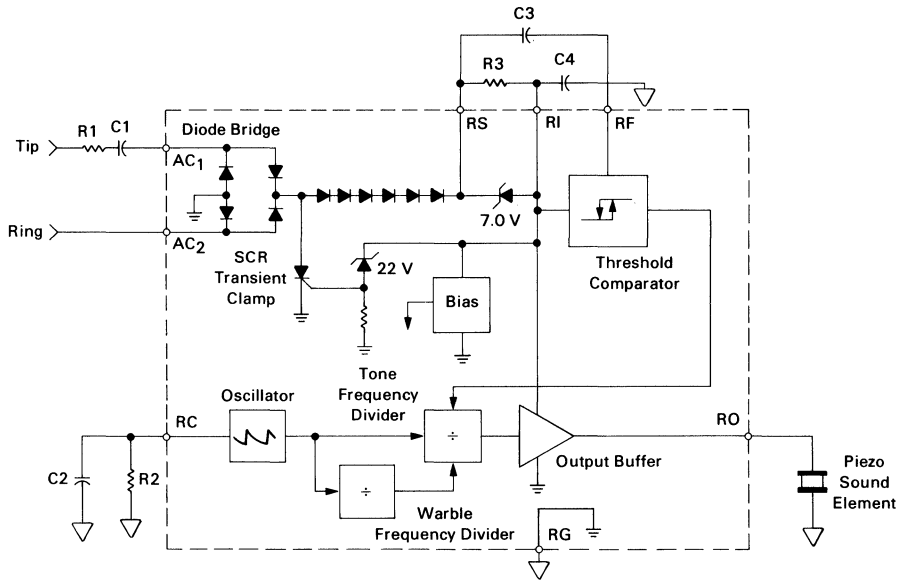
PIN DESCRIPTIONS

Name	Description
AC_1, AC_2	The input terminals to the full-wave diode bridge. The ac ringing signal from the telephone line energizes the ringer through this bridge.
RS	The positive output of diode bridge to which an external current sense resistor is connected.
RI	The positive supply terminal for the oscillator, frequency divider and output buffer circuits.
RF	The terminal for the filter capacitor used in detection of ringing input signals.
RO	The tone ringer output terminal through which the sound element is driven.
RG	The negative output of the diode bridge and the negative supply terminal of the tone generating circuitry.
RC	The oscillator terminal for the external resistor and capacitor which control the tone ringer frequencies.

ELECTRICAL CHARACTERISTICS (T_A = 25°C)

Characteristic	Test	Symbol	Min	Typ	Max	Units
Ringing Start Voltage ($V_{Start} = V_I$ @ Ring Start)						Vdc
$V_I > 0$	1a	$V_{Start(+)}$	31	34.5	38	
$V_I < 0$	1b	$V_{Start(-)}$	-31	-34.5	-38	
Ringing Stop Voltage ($V_{Stop} = V_I$ @ Ring Stop)	1c	V_{Stop}				Vdc
MC34012-1			16	20	25	
MC34012-2			13	18	22	
MC34012-3			16	20	25	
Output Frequencies (V_I = 50 V)	1d					Hz
MC34012-1 High Tone		f_H	967	1040	1113	
Low Tone		f_L	774	832	890	
Warble Tone		f_W	12	13	14	
MC34012-2 High Tone		f_H	1934	2080	2226	
Low Tone		f_L	1548	1664	1780	
Warble Tone		f_W	12	13	14	
MC34012-3 High Tone		f_H	967	1040	1113	
Low Tone		f_L	774	832	890	
Warble Tone		f_W	24	26	28	
Output Voltage (V_I = 50 V)	6	V_O	19	20	23	V_{p-p}
Output Short-Circuit Current	2	I_O	35	50	80	mA_{p-p}
Input Diode Voltage (I_I = 1.0 mA)	3	V_D	4.6	5.1	5.6	Vdc
Input Voltage—SCR Off (I_I = 30 mA)	4a	V_{off}	37	42	47	Vdc
Input Voltage—SCR On (I_I = 100 mA)	4b	V_{on}	3.2	4.2	6.0	Vdc
Threshold Filter Resistance $R_{RF} = 2.0\ V/I_{RF}$	5	R_{RF}	30	50	80	kΩ

BLOCK DIAGRAM



CIRCUIT DESCRIPTION

The MC34012 Tone Ringer derives its power supply by rectifying the ac ringing signal. It uses this power to activate a tone generator and drive a piezo-ceramic transducer. The tone generation circuitry includes a relaxation oscillator and frequency dividers which produce high and low frequency tones as well as the tone warble frequency. The relaxation oscillator frequency f_O is set by resistor R2 and capacitor C2 connected to pin RC. The oscillator will operate with f_O from 1.0 kHz to 10 kHz with the proper choice of external components (See Figure 1).

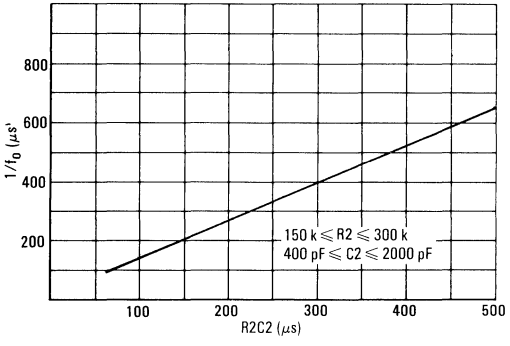
The frequency of the tone ringer output signal at pin RO alternates between $f_O/4$ to $f_O/5$. The warble rate at which the frequency changes is $f_O/320$ for the MC34012-1, $f_O/640$ for the MC34012-2, or $f_O/160$ for the MC34012-3. With a 4.0 kHz oscillator frequency, the MC34012-1 produces 800 Hz and 1000 Hz tones with a 12.5 Hz warble rate. The MC34012-2 generates 1600 Hz and 2000 Hz tones with a similar 12.5 Hz warble frequency from an 8.0 Hz oscillator frequency. The MC34012-3 will produce 400 Hz and 500 Hz tones with a 12.5 Hz warble rate from a 2.0 kHz oscillator frequency. The tone ringer output circuit can source or sink 20 mA with an output voltage swing of 20 volts peak-to-peak. Volume control is readily implemented by adding a variable resistance in series with the piezo transducer.

Input signal detection circuitry activates the tone ringer output when the ac line voltage exceeds programmed threshold level. Resistor R3 determines the ringing signal amplitude at which an output signal will be generated at RO. The ac ringing signal is rectified by the internal diode bridge. The rectified input signal produces a current through R3 which is input at terminal RI. The voltage across resistor R3 is filtered by capacitor C3 at the input to the threshold circuit. When the voltage on capacitor C3 exceeds 1.7 volts, the threshold comparator enables the tone ringer output. Line transients produced by pulse dialing telephones do not charge capacitor C3 sufficiently to activate the tone ringer output.

Capacitors C1 and C4 and resistor R1 determine the 10 volt, 24 Hz signature test impedance. C4 also provides filtering for the output stage power supply to prevent droop in the square wave output signal. Six diodes in series with the rectifying bridge provide the necessary non-linearity for the 2.5 volt, 24 Hz signature tests.

An internal shunt voltage regulator between the RI and RG terminals provides dc voltage to power output stage, oscillator, and frequency dividers. The dc voltage at RI is limited to approximately 22 volts in regulation. To protect the IC from telephone line transients, an SCR is triggered when the regulator current exceeds 50 mA. The SCR diverts current from the shunt regulator and reduces the power dissipation within the IC.

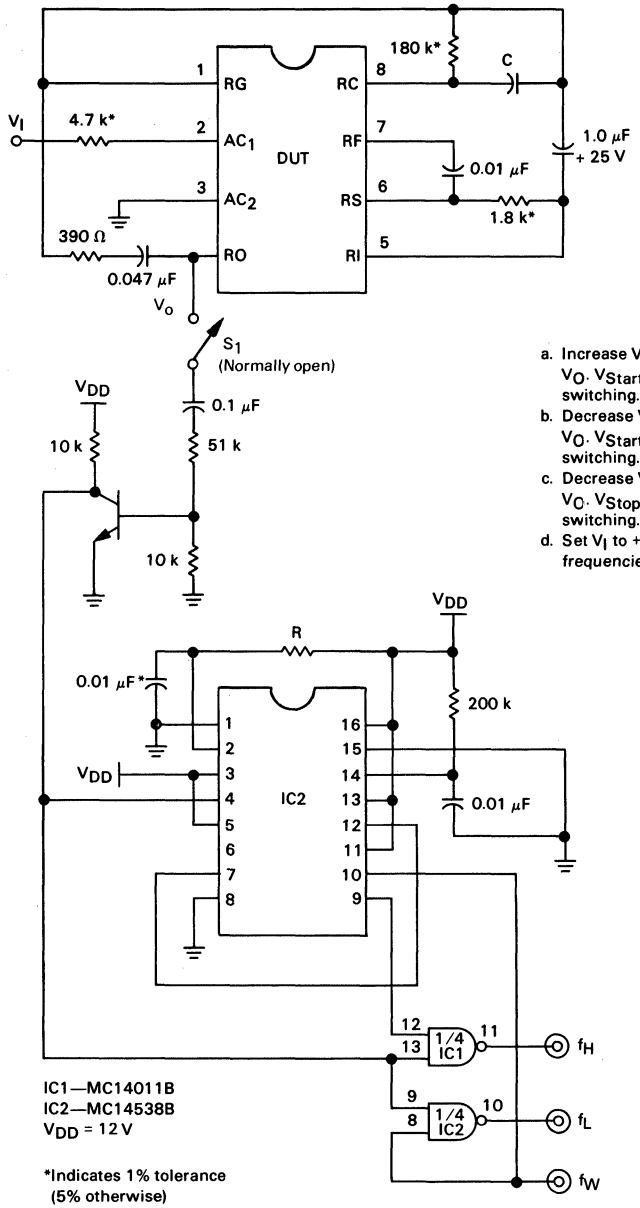
FIGURE 1 — OSCILLATOR PERIOD ($1/f_O$) versus OSCILLATOR R2 C2 PRODUCT



EXTERNAL COMPONENTS

R1	Line input resistor. R1 controls the tone ringer input impedance. It also influences ringing threshold voltage and limits current from line transients. (Range: 2.0 kΩ to 10 kΩ).
C1	Line input capacitor. C1 ac couples the tone ringer to the telephone line and controls ringer input impedance at low frequencies. (Range: 0.4 μF to 2.0 μF).
R2	Oscillator resistor. (Range: 150 kΩ to 300 kΩ).
C2	Oscillator capacitor. (Range: 400 pF to 2000 pF).
R3	Input current sense resistor. R3 controls the ringing threshold voltage. Increasing R3 decreases the ring-start voltage. (Range: 0.8 kΩ to 2.0 kΩ).
C3	Ringing threshold filter capacitor. C3 filters the ac voltage across R3 at the input of the ringing threshold comparator. It also provides dialer transient rejection. (Range: 0.5 μF to 5.0 μF).
C4	Ringer supply capacitor. C4 filters supply voltage for the tone generating circuits. It also provides an ac current path for the 10 V_{rms} ringer signature impedance. (Range: 1.0 μF to 10 μF).

FIGURE 2 — TEST ONE



MC34012-1: C = 1000 pF*
MC34012-2: C = 500 pF*
MC34012-3: C = 1000 pF*

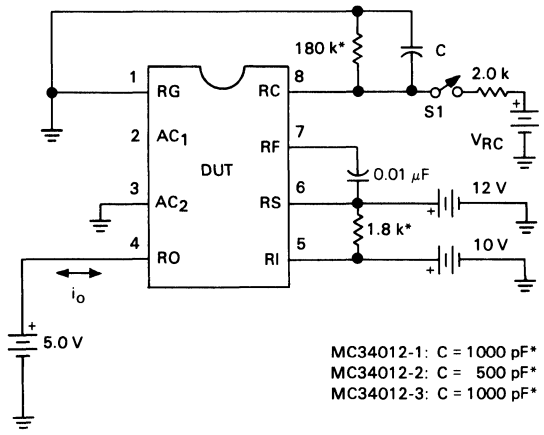
a. Increase V_I from +30 volts while monitoring V_O. $V_{Start(+)}$ equals V_I when V_O commences switching.
b. Decrease V_I from −30 volts while monitoring V_O. $V_{Start(-)}$ equals V_I when V_O commences switching.
c. Decrease V_I from +40 volts while monitoring V_O. V_{Stop} equals V_I when V_O ceases switching.
d. Set V_I to +50 volts. Close S1. Measure frequencies f_H, f_L, and f_W.

IC1—MC14011B
IC2—MC14538B
V_{DD} = 12 V

*Indicates 1% tolerance
(5% otherwise)

MC34012-1: R = 110 kΩ*
MC34012-2: R = 55 kΩ*
MC34012-3: R = 110 kΩ*

FIGURE 3 — TEST TWO



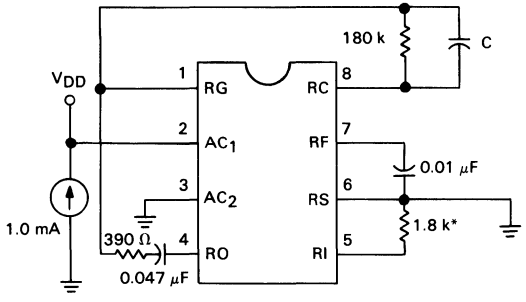
MC34012-1: C = 1000 pF*
MC34012-2: C = 500 pF*
MC34012-3: C = 1000 pF*

With V_{RC} = 3.5 volts, close S1. Measure the current at Pin 4 (I_{O1}). Repeatedly switch V_{RC} between 3.5 volts and 0 volts until Pin 4 current changes polarity. Measure this opposite polarity current (I_{O2}).
Calculate:

$I_O = |I_{O1}| + |I_{O2}|$

*Indicates 1% tolerance (5% otherwise)

FIGURE 4 — TEST THREE

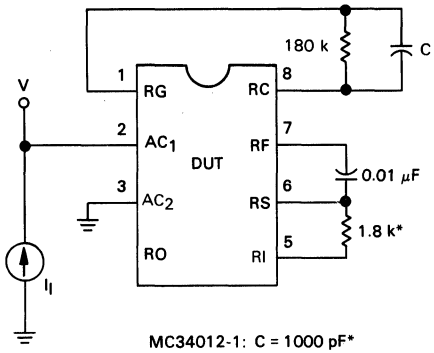


MC34012-1: C = 1000 pF*
MC34012-2: C = 500 pF*
MC34012-3: C = 1000 pF*

Measure voltage at Pin 2.

*Indicates 1% tolerance (5% otherwise)

FIGURE 5 — TEST FOUR

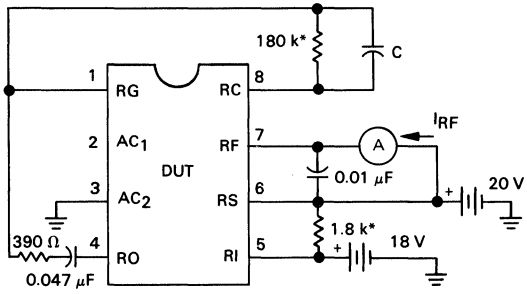


a. Set I_I to 30 mA. Measure voltage at Pin 2 (V_{off}).
b. Set I_I to 100 mA. Measure voltage at Pin 2 (V_{on}).

MC34012-1: C = 1000 pF*
MC34012-2: C = 500 pF*
MC34012-3: C = 1000 pF*

*Indicates 1% tolerance (5% otherwise)

FIGURE 6 — TEST FIVE



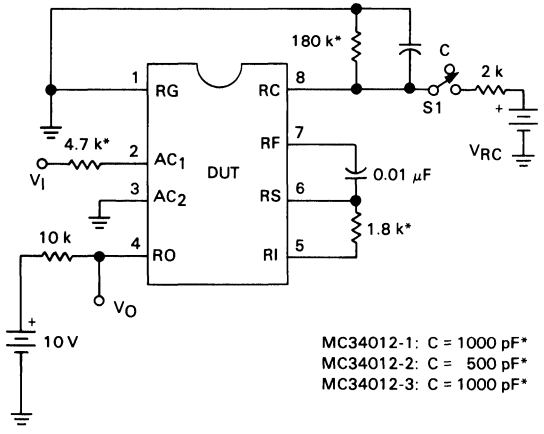
Measure current into Pin 7 (I_{RF}).
Calculate:

R_{RF} = 2 volts ÷ I_{RF}

MC34012-1: C = 1000 pF*
MC34012-2: C = 500 pF*
MC34012-3: C = 1000 pF*

*Indicates 1% tolerance (5% otherwise)

FIGURE 7 — TEST SIX



MC34012-1: C = 1000 pF*
MC34012-2: C = 500 pF*
MC34012-3: C = 1000 pF*

With V_{RC} = 3.5 volts, close S1. Set V_I to 50 volts. Measure dc voltage at Pin 4 (V_{O1}). Repeatedly change V_{RC} between 3.5 volts and 0 volts until Pin 4 changes state. Measure the new voltage at Pin 4 (V_{O2}).
Calculate the peak-to-peak output voltage:

$$V_{Op\text{-}p} = | V_{O2} - V_{O1} |$$

*Indicates 1% tolerance (5% otherwise)

MC34014

Specifications and Applications Information

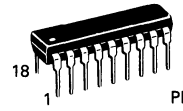
TELEPHONE SPEECH NETWORK WITH DIALER INTERFACE

The MC34014 is a Telephone Speech Network integrated circuit which incorporates adjustable transmit, receive, and sidetone functions, a dc loop interface circuit, tone dialer interface, and a regulated output voltage for a pulse/tone dialer. Also included is an equalization circuit which compensates gains for line length variations. The conversion from 2-to-4 wire is accomplished with a supply voltage as low as 1.5 volts. The MC34014 is packaged in a standard 18-pin (0.3″ wide) plastic DIP and a 20-pin SOIC package.

- Transmit, Receive, and Sidetone Gains Set by External Resistors
- Loop Length Equalization for Transmit, Receive, and Sidetone Functions
- Operates Down to 1.5 volts (V+) in Speech Mode
- Provides Regulated Voltage for CMOS Dialer
- Speech Amplifiers Muted During Pulse and Tone Dialing
- DTMF Output Level Adjustable with a Single Resistor
- Compatible with 2-Terminal Electret Microphones
- Compatible with Receiver Impedances of 150 Ω and Higher

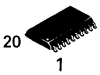
TELEPHONE SPEECH NETWORK WITH DIALER INTERFACE

SILICON MONOLITHIC INTEGRATED CIRCUIT

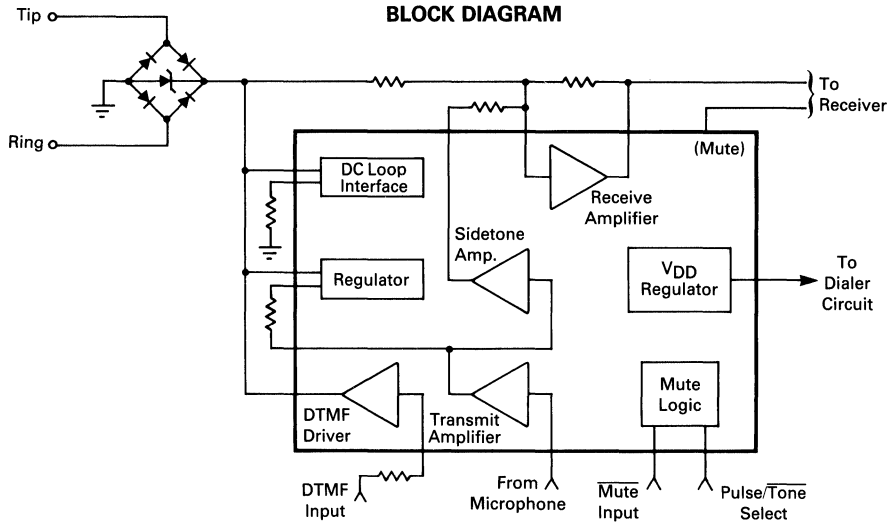


P SUFFIX
PLASTIC PACKAGE
CASE 707

DW SUFFIX
PLASTIC PACKAGE
CASE 751D
SO-20L



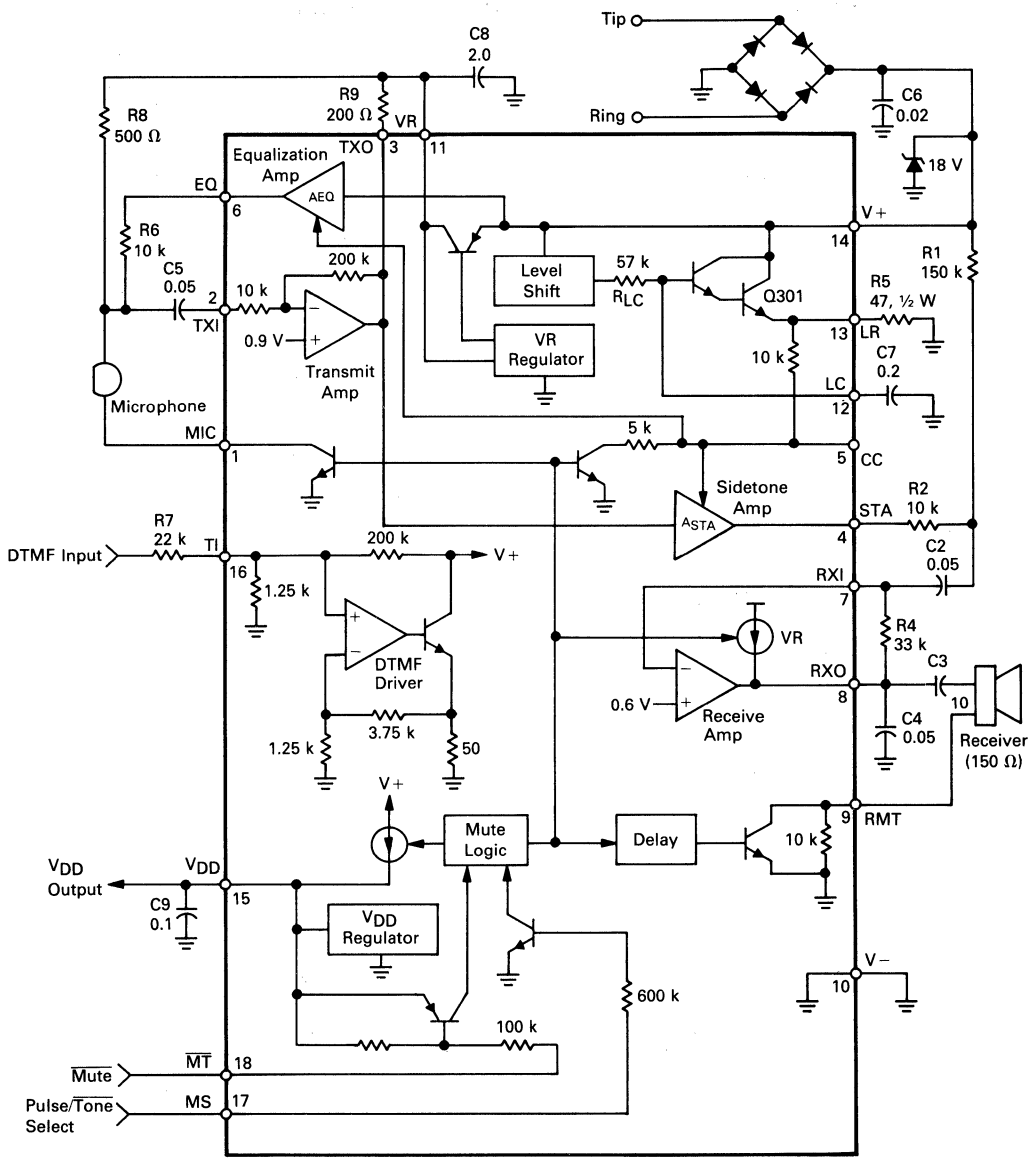
BLOCK DIAGRAM



PIN DESCRIPTION (See Figure 1)

Pin # SOIC	Pin # DIP	Name	Description
1	1	MIC	Microphone negative supply. Bias current from the electret microphone is returned to V− through this pin, through an open collector NPN transistor whose base is controlled by an internal mute signal. During dialing, the transistor is off, disabling the microphone.
2	2	TXI	Transmit amplifier input. Input impedance is 10 kΩ. Signals from the microphone are input through capacitor C5 to TXI.
3	3	TXO	Transmit amplifier output. The ac signal current from this output flows through the V_R series pass transistor via R9 to drive the line at V+. Increasing R9 will decrease the signal at V+. The output is biased at ≈0.65 V to allow for maximum swing of ac signals. The closed loop gain from TXI to TXO is internally set at 26 dB.
4	4	STA	Sidetone amplifier output. Input to this amplifier is TXO. The signal at STA cancels the sidetone signals in the receive amplifier. The signal level at STA increases with loop length.
5	5	CC	Compensation Capacitor. A capacitor from CC to ground will compensate the loop length equalization circuit when additional stability is required. In most applications, CC remains open.
7	6	EQ	Equalization amplifier output. A portion of the V+ signal is present on this pin to provide negative feedback around the transmit amplifier. The feedback decreases with increasing loop length, causing the ac impedance of the circuit to increase.
8	7	RXI	Receive amplifier input. Input impedance is >100 kΩ. Signals from the line and sidetone amplifier are summed at RXI.
9	8	RXO	Receive Amplifier output. RXO is biased by a 2.5 mA current source. Feedback maintains the dc bias voltage at ≈0.65 V. Increasing R4 (between RXO and RXI) will increase the receive gain. C4 stabilizes the amplifier. C3 couples the signals to the receiver. The 2.5 mA current source is reduced to 0.4 mA when dialing.
10	9	RMT	Receiver Mute. The ac receiver current is returned to V− through an open collector NPN transistor and a parallel 10 kΩ resistor. The base of the NPN is controlled by an internal mute signal. During dialing the transistor is off, leaving the 10 kΩ resistor in series with the receiver.
11	10	V−	Negative supply. The most negative input connected to Tip and Ring through the polarity guard diode bridge.
12	11	VR	Regulated voltage output. The VR voltage is regulated at 1.2 V and biases the microphone and the speech circuits. An internal series pass PNP transistor allows for regulation with a line voltage as low as 1.5 V. Capacitor C8 stabilizes the regulator.
13	12	LC	DC load capacitor. An external capacitor C7 and an internal resistor form a low pass filter between V+ and LR to prevent ac signals from being loaded by the dc load resistor R5. Forcing LC to V− will turn off the dc load current and increase the V+ voltage.
14	13	LR	DC load resistor. Resistor R5 from LR to V− determines the dc resistance of the telephone, and removes power dissipation from the chip. The LR pin is biased 2.8 volts below the V+ voltage (4.5 volts in the tone dialing mode).
15	14	V+	Positive supply. V+ is the positive line voltage (from Tip & Ring) through the polarity guard bridge. All sections of the MC34014 are powered by V+.
17	15	V_{DD}	V_{DD} regulator. V_{DD} is the output of a shunt type regulator with a nominal voltage of 3.3 V. The nominal output current is increased from 550 μA to 2 mA when dialing. Capacitor C9 stabilizes the regulator and sustains the V_{DD} voltage during pulse dialing.
18	16	TI	Tone input. The DTMF signal from a dialer circuit is input at TI through an external resistor R7. The current at TI is amplified to drive the line at V+. Increasing R7 will reduce the DTMF output levels. The input impedance at TI is nominally 1.25 kΩ.
19	17	MS	Mode select. This pin is connected through an internal 600 kΩ resistor to the base of an NPN transistor. A Logic "1" (>2.0 V) selects the pulse dialing mode. A Logic "0" (<0.3 V) selects the tone dialing mode.
20	8	$\overline{MT}$	Mute input. $\overline{MT}$ is connected through an internal 100 kΩ resistor to the base of a PNP transistor, with the emitter at V_{DD}. A Logic "0" (<1.0 V) will mute the network for either pulse or tone dialing. A Logic "1" (>V_{DD} − 0.3 V) puts the MC34014 into the speech mode.

FIGURE 1 — TEST CIRCUIT



NOTE: Pin numbers are for 18 pin DIP.

ABSOLUTE MAXIMUM RATINGS (Voltages referred to V−, T_A = 25°C) (See Note 1.)

Parameter	Value	Units
V+ Voltage	−1.0, +18	Vdc
V_{DD} (externally applied, V+ = 0)	−1.0, +6	Vdc
V_{LR}	−1.0, V+ − 3.0	Vdc
$\overline{MT}$, MS Inputs	−1.0, V_{DD} +1.0	Vdc
Storage Temperature	−65, +150	°C

NOTE 1: Devices should not be operated at these values. The "Recommended Operating Conditions" provide conditions for actual device operation.

RECOMMENDED OPERATING CONDITIONS

Parameter	Value	Units
V+ Voltage (Speech Mode) (Tone Dialing Mode)	+1.5 to +15 +3.3 to +15	Vdc Vdc
I_{TXO} (Instantaneous)	0 to 10	mA
Ambient Temperature	−20 to +60	°C

ELECTRICAL CHARACTERISTICS (Refer to Figure 1) (T_A = 25°C)

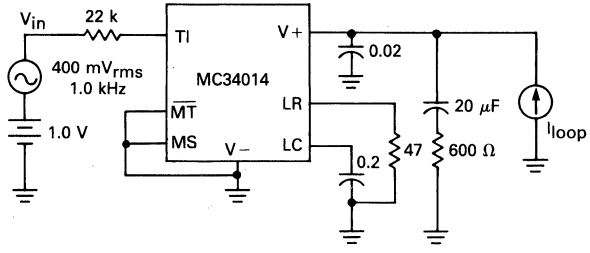
Parameter	Symbol	Min	Typ	Max	Units
LINE INTERFACE					
V+ Voltage	V+				Vdc
I_{loop} = 20 mA (Speech/Pulse Mode)		2.6	3.2	3.8	
I_{loop} = 30 mA (Speech/Pulse Mode)		3.0	3.7	4.4	
I_{loop} = 120 mA (Speech/Pulse Mode)		7.0	8.2	9.5	
I_{loop} = 20 mA (Tone Mode)		4.1	4.9	5.7	
I_{loop} = 30 mA (Tone Mode)		4.6	5.4	6.2	
V+ Current (Pin 12 Grounded)	I+				mA
V+ = 1.7 V (Speech Mode)		4.0	6.6	8.5	
V+ = 12 V (Speech/Pulse Modes)		5.5	8.4	12.5	
V+ = 12 V (Tone Mode)		6.0	8.8	14.0	
LR Level Shift (V+ − V_{LR})	ΔV_{LR}				Vdc
(Speech/Pulse Mode)		—	2.7	—	
(Tone Mode)		—	4.3	—	
LC Terminal Resistance	R_{LC}	36	57	94	kΩ
VOLTAGE REGULATORS					
VR Voltage (V+ = 1.7 V)	V_R	1.1	1.2	1.3	Vdc
Load Regulation (0 mA < I_R < 6.0 mA)	ΔV_{RLD}	—	20	—	mV
Line Regulation (2.0 V < V+ < 6.5 V)	ΔV_{RLN}	—	25	—	mV
V_{DD} Voltage (V+ = 4.5 V)	V_{DD}	3.0	3.3	3.8	Vdc
Load Regulation (0 < I_{DD} < 1.6 mA) (Dialing Mode)	ΔV_{DDLD}	—	0.25	—	Vdc
Line Regulation (All Modes) (4.0 V < V+ < 9.0 V)	ΔV_{DDLN}	—	50	—	mV
Max. Output Current (Speech Mode)	I_{DDSP}	375	550	1000	μA
Max. Output Current (Dialing Mode)	I_{DDDL}	1.6	2.0	3.6	mA
V_{DD} Leakage Current (V+ = 0, V_{DD} = 3.0 V)	I_{DDLK}	—	—	1.5	μA
SPEECH AMPLIFIERS					
Transmit Amplifier					
Gain (TXI to TXO)	A_{TXO}	—	20	—	V/V
TXO Bias Voltage (Speech/Pulse Mode)	V_{TXOSP}	0.45	0.52	0.60	x V_R
TXO Bias Voltage (Tone Mode Mode)	V_{TXODL}	VR−25	VR−5.0	—	mV
TXO High Voltage (Speech/Pulse Mode)	V_{TXOH}	VR−25	VR−5.0	—	mV
TXO Low Voltage (Speech/Pulse Mode)	V_{TXOL}	—	125	250	mV
TXI Input Resistance	R_{TXI}	—	10	—	kΩ
Receive Amplifier					
RXO Bias Voltage (All Modes)	V_{RXO}	0.45	0.52	0.60	x VR
RXO Source Current (Speech Mode)	I_{RXOSP}	1.5	2.0	—	mA
RXO Source Current (Pulse/Tone Mode)	I_{RXODL}	200	400	—	μA
RXO High Voltage (All Modes)	V_{RXOH}	VR−100	VR−50	—	mV
RXO Low Voltage (All Modes)	V_{RXOL}	—	50	150	mV

ELECTRICAL CHARACTERISTICS — (continued) (T_A = 25°C)

Parameter	Symbol	Min	Typ	Max	Units
MICROPHONE, RECEIVER CONTROLS					
MIC Saturation Voltage (Speech Mode, I = 500 μA)	$V_{OL_{MIC}}$	—	50	125	mV
MIC Leakage Current (Dialing Mode, Pin 1 = 3.0 V)	$I_{MIC_{LK}}$	—	0	5.0	μA
RMT Resistance (Speech Mode) (Dialing Mode)	$R_{RMT_{SP}}$ $R_{RMT_{DL}}$	— 5.0	8.0 10	15 18	Ω kΩ
RMT Delay (Dialing to Speech)	t_{RMT}	2.0	4.0	20	ms
DIALING INTERFACE					
$\overline{MT}$ Input Resistance	R_{MT}	58	100	—	kΩ
$\overline{MT}$ Input High Voltage	V_{IHMT}	$V_{DD}-0.3$	—	—	Vdc
$\overline{MT}$ Input Low Voltage	V_{ILMT}	—	—	1.0	Vdc
MS Input Resistance	R_{MS}	280	600	—	kΩ
MS Input High Voltage	V_{IHMS}	2.0	—	—	Vdc
MS Input Low Voltage	V_{ILMS}	—	—	0.3	Vdc
TI Input Resistance	R_{TI}	—	1.25	—	kΩ
DTMF Gain (See Figure 2) (V+/V_{in})	A_{DTMF}	3.2	4.8	6.2	dB
SIDETONE AMPLIFIER					
Gain (TXO to STA) (Speech Mode) @ V_{LR} = 0.5 V (Speech Mode) @ V_{LR} = 2.5 V (Pulse Mode) @ V_{LR} = 0.2 V (Pulse Mode) @ V_{LR} = 1.0 V	A_{STA}	 — — — —	 −15 −21 −15 −21	 — — — —	dB
STA Bias Voltage (All Modes)	V_{STA}	0.65	0.8	0.9	x V_R
EQUALIZATION AMPLIFIER					
Gain (V+ to EQ) (Speech Mode) @ V_{LR} = 0.5 V (Speech Mode) @ V_{LR} = 2.5 V (Pulse Mode) @ V_{LR} = 0.2 V (Pulse Mode) @ V_{LR} = 1.0 V	A_{EQ}	 — — — —	 −12 −2.5 −12 −2.5	 — — — —	dB
EQ Bias Voltage (Speech Mode) @ V_{LR} = 0.5 V (Pulse Mode) @ V_{LR} = 0.5 V (Speech, Pulse) @ V_{LR} = 2.5 V	V_{EQ}	 — — —	 0.66 1.3 3.3	 — — —	Vdc

NOTE: Typical values are not tested or guaranteed.

FIGURE 2 — DTMF DRIVER TEST



SYSTEM SPECIFICATIONS (T_A = 25°C) (See Figures 1–4)

Parameter	Min	Typ	Max	Unit
Tip-Ring Voltage (including polarity guard bridge drop of 1.4 V)				Vdc
(Speech Mode) I_{loop} = 5.0 mA	—	2.4	—	
I_{loop} = 10 mA	—	3.9	—	
I_{loop} = 20 mA	—	4.6	—	
I_{loop} = 40 mA	—	5.6	—	
I_{loop} = 60 mA	—	6.6	—	
Transmit				
Gain from V_S to V+ (Figure 3) (I_{loop} = 20 mA)	28	30	31	dB
Gain change as I_{loop} is increased to 60 mA	−6.0	−4.5	−3.6	dB
Distortion	—	2.0	—	%
Output noise	—	11	—	dBrnc
Receive				
V_{RXO}/V_S (f = 1.0 kHz, I_{loop} = 20 mA) (See Figure 4)	−16	−15	−13	dB
Receive gain change as I_{loop} is increased to 60 mA	−5.0	−3.0	−2.0	dB
Distortion	—	2.0	—	%
Sidetone Level				dB
$V_{RXO}/V+$ (Figure 3)				
I_{loop} = 20 mA	—	−36	—	
I_{loop} = 60 mA	—	−21	—	
Sidetone Cancellation	20	26	—	dB
$\left[\frac{V_{RXO}}{V+}\text{ (Figure 4)}\right]$ dB − $\left[\frac{V_{RXO}}{V+}\text{ (Figure 3)}\right]$ dB I_{loop} = 20 mA				
DTMF Driver	3.2	4.8	6.2	dB
$V+/V_{in}$ (Figure 2) I_{loop} = 20 mA				
AC Impedance				Ω
Speech mode (incl. C_6, See Figure 4) I_{loop} = 20 mA	—	750	—	
$Z_{ac} = (600)V+/(V_S - V+)$ I_{loop} = 60 mA	—	300	—	
Tone mode (including C_6) 20 mA < I_{loop} < 60 mA	—	1650	—	

NOTE: Typicals are not tested or guaranteed.

FIGURE 3 — TRANSMIT AND SIDETONE LEVEL TEST

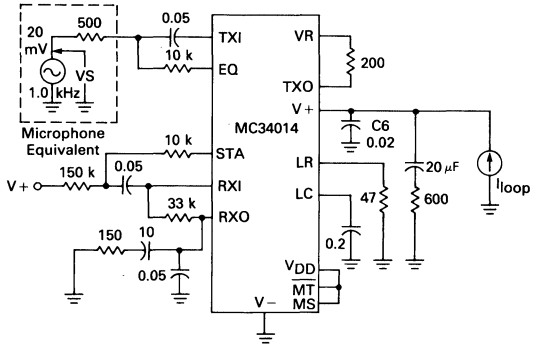
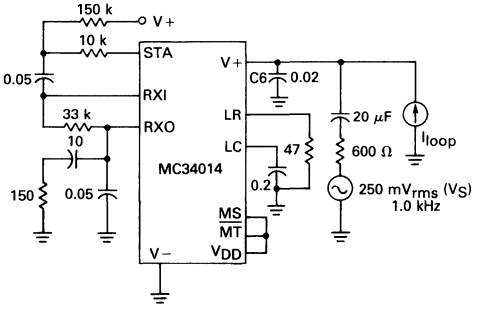


FIGURE 4 — AC IMPEDANCE, RECEIVE AND SIDETONE CANCELLATION TEST



DESIGN GUIDELINES (Refer to Figure 1)

INTRODUCTION

The MC34014 is a speech network meant for connection to the Tip & Ring lines through a polarity guard bridge. The circuit incorporates four amplifiers: transmit, receive, sidetone, and equalization. Some parameters of each amplifier are set by external components, and in addition, the gains of the sidetone and equalization amplifiers vary with loop current.

The line interface portion determines the dc voltage versus loop current characteristics, and provides the required regulated voltages for internal and external use.

The dialer interface provides three modes of operation: speech (non-dialing), pulse dialing, and tone (DTMF) dialing. When switching to either dialing mode some parameters of the various sections are changed in order to optimize the circuit operation for that mode. The following table summarizes those changes:

2

TABLE 1 — OPERATING PARAMETERS AS A FUNCTION OF OPERATING MODE

Function	Speech	Pulse	Tone
LR Level Shift ($V+ - V_{LR}$)	2.7 V	2.7 V	4.3 V
V_{DD} Source Current	550 μA	2.0 mA	2.0 mA
Transmit Amplifier	Functional	Functional	Inoperative
MIC Switch (Pin 1)	On	Off	Off
Equalization Amplifier	See Transfer Curves — Figure 8		
Sidetone Amplifier	See Transfer Curves — Figure 6		
Receive Amplifier Output Current	2.5 mA	400 μA	400 μA
RMT (Pin 9) Impedance	8.0 Ω	10 kΩ	10 kΩ
DTMF Amplifier	Inoperative	Inoperative	Functional
CC Voltage	$V_{LR}/3$	V_{LR}	V_{LR}

DC LINE INTERFACE (Figure 5)

The dc line interface circuit (Pins 10, 12–14) sets the dc voltage characteristics with respect to the loop current. The loop current enters at Pin 14 where the internal circuitry of the MC34014 draws 5–6 mA. Pin 3 sinks (typically) 3 mA through R_9. The remainder of the loop current is passed through Q_{301} and R_5. The resulting voltage across the entire circuit is therefore equal to the voltage across R_5, plus the level shift voltage from Pin 13 (LR) to Pin 14 (V+), nominally 2.7 volts in the speech and pulse modes. In the tone mode, the level shift increases to 4.3 volts, the internal current changes slightly (Figure 6), and the current required at Pin 3 decreases to near zero. These changes increase the equivalent dc resistance of the circuit, raising the voltage at V+ to ensure adequate voltage at V_{DD} for the external tone dialer. See Figure 7 for typical voltage versus loop current characteristics.

Capacitor C_7 at Pin 12 provides high frequency rolloff (above 10 Hz) so that R_5 does not load down the speech and DTMF signals.

The voltage at V_R is an internally regulated 1.2 volt supply which provides the bias currents for the microphone and the transmit amplifier output (Pin 3), as well as internal bias for the various amplifiers. Capacitor C_8 stabilizes the regulator. The use of an (internal) PNP transistor allows V_R to be regulated with a V+ voltage as low as 1.5 volts.

FIGURE 5 — DC LINE INTERFACE

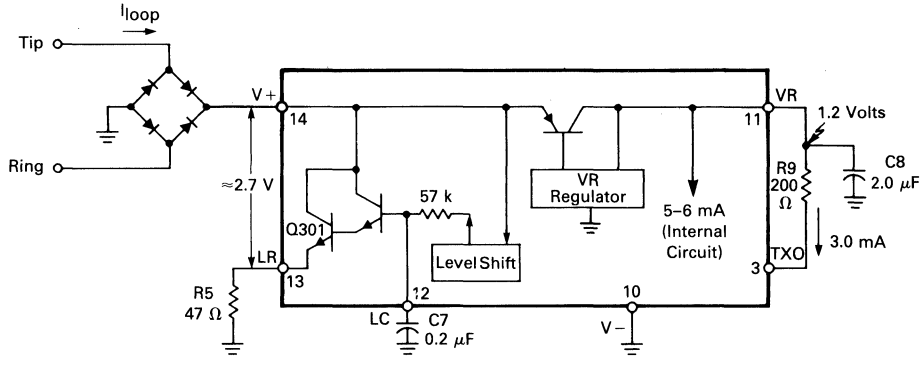


FIGURE 6 — INTERNAL CURRENT versus VOLTAGE

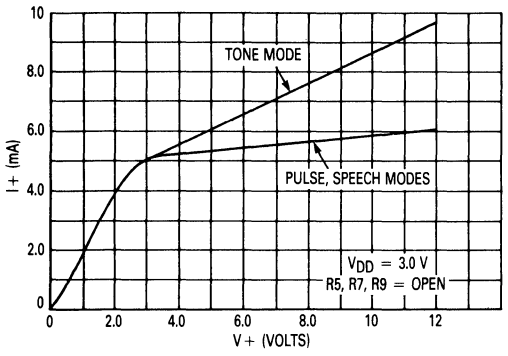
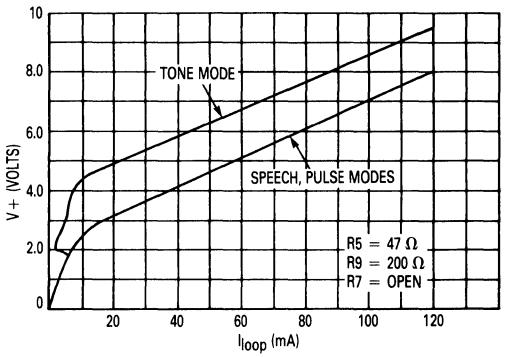


FIGURE 7 — CIRCUIT VOLTAGE versus LOOP CURRENT



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TRANSMIT AMPLIFIER

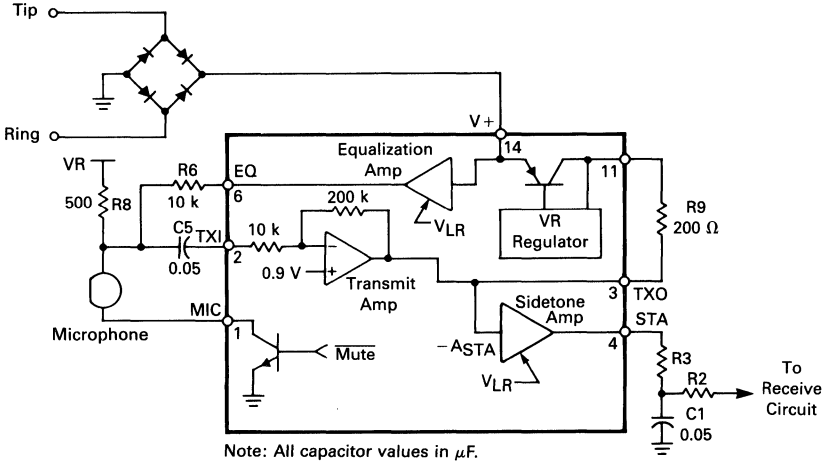
The transmit amplifier (from TXI to TXO) is inverting, with a fixed internal gain of 20 V/V (26 dB), and a typical input impedance of 10 kΩ (Figure 8). The input bias currents are internally supplied, allowing capacitive coupling of the microphone signals to the amplifier.

In the speech and pulse modes, the dc bias level at TXO is typically 0.52 x VR (≈0.63 V), which permits the output to swing 0.55 volts in both positive and negative directions without clipping. The ac voltage signal at TXO (the amplified speech signal) is converted to an ac current by R_9. The ac current passes through the VR series pass transistor to V+, modulating the loop current. The voltage signal at V+ is out of phase with the signal at TXI.

In the tone dialing mode, the TXO dc bias level is clamped at approximately VR-10 mV, rendering the amplifier inoperative. This action also reduces the TXO bias current from 3.0 mA to less than 125 μA.

MIC (Pin 1) is connected to an open-collector NPN transistor, and provides the ground path for the microphone bias current. In either dialing mode, the transistor is off, disabling the microphone.

FIGURE 8 — TRANSMIT SECTION



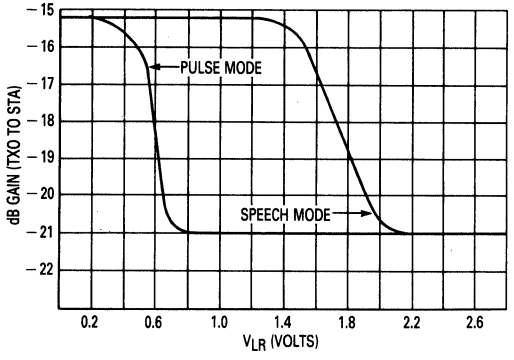
Note: All capacitor values in μF.

SIDETONE AMPLIFIER

The sidetone amplifier provides inversion of the TXO signal for the reduction of the sidetone signal at the receive amplifier (Figure 8). Resistors R_2 and R_3 determine the amount of sidetone cancellation. Capacitor C_1 provides phase shift to compensate for the phase shift created by the complex impedance of the Tip & Ring lines.

The gain of the sidetone amplifier varies with the voltage at LR (Pin 13), in effect making it a function of the loop current. The maximum gain is −15 dB (0.17 V/V) at low loop currents, and the minimum gain is −21 dB (0.09 V/V) at high loop current (see Figure 9 for transfer curves). For example, using 47 Ω for R_5, the gain would begin to decrease at ≈30 mA, and would stop decreasing at ≈57 mA (speech mode). The dc bias voltage at STA (Pin 4) changes slightly (≈50 mV) with variations in loop current. The output is inverted from TXO, which is the input to this amplifier. Since the transmit amplifier is inoperative in the tone dialing mode, the sidetone amplifier is also inoperative in that mode.

FIGURE 9 — SIDETONE AMPLIFIER GAIN



RECEIVE AMPLIFIER

The gain of the receive amplifier (from V+ to RXO) is determined according to the following equation (refer to Figure 10):

$$\frac{V_{RXO}}{V+} = \frac{R_4}{R_1} + \frac{(X_C//R_2)\,(A_{EQ})\,(A_{TXO})\,(A_{STA}) \times R_A \times R_4}{((X_C//R_2)+R_3)\,(R_A+R_6) \times R_2}$$

Where R_A = R_8//10 kΩ (10 kΩ = R_{in} of T_X Amp)
A_{EQ} = Gain of Equalization Amp
A_{TXO} = Gain of Transmit Amp (20 V/V)
A_{STA} = Gain of sidetone Amp
X_C = Impedance of C_1 at frequency of interest

The waveform at STA (Pin 4) is in phase with that at V+ (for receive signals), hence the plus sign between the terms. Due to the variations of A_{EQ} and A_{STA} with loop current, the receive gain will vary by ≈1.5 dB. If capacitor C_1 is not used, the above equation is simplified by deleting the terms containing X_C.

The output at RXO is inverted from V+ in the receive mode. In the transmit mode, the V+-to-RXO phase relationship depends on the amount of sidetone cancellation (determined by R_2 and R_3 and C_1), and can vary from 0° to 180°.

In the speech mode, the output current capability (at RXO) is typically 2.0 mA. In either dialing mode, the current capability is reduced to 400 μA in order to reduce internal current consumption. This feature is beneficial when this device is used in conjunction with a line-powered speakerphone circuit, such as the MC34018, where the majority of the loop current is needed for the speakerphone.

RMT (Pin 9) is the return path for the receiver's ac current. This pin is internally connected to an open collector NPN transistor, paralleled by a 10 kΩ resistor. In the speech mode, the transistor is on, providing a low impedance from RMT to ground. In either dialing mode, the transistor is off, muting the receive signal. This prevents loud "clicks" or loud DTMF tones from being heard in the receiver during dialing. When switching from either dialing mode to the speech mode ($\overline{MT}$ switches from low to high), the RMT pin switches back to a low impedance after a delay of 2–20 ms. The delay reduces clicks in the receiver associated with switching from the dialing to speech mode.

EQUILIZATION AMPLIFIER

The equalization amplifier gain varies with loop current, and is configured in the circuit so as to cause a variation of the network ac impedance (when looking in from the Tip & Ring lines). The gain varies with the voltage at LR (Pin 13), in effect making it a function of the loop current. The maximum gain is −2.5 dB (0.75 V/V) at high loop current, and the minimum gain is −12 dB (0.25 V/V) and low loop current (see Figure 11 for transfer curve). For example, using 47 Ω for R_5, the gain would begin to increase at ≈30 mA, and would stop increasing at ≈57 mA (speech mode). The output signal is in phase with the signal at V+, which is the input to this amplifier.

The dc bias level at EQ (Pin 6) varies with the voltage at LR (Pin 13) according to the curve of Figure 12. In most applications, this level shift is of little consequence, and may be ignored. If a particular circuit configuration should be sensitive to the shift, however, the output signal at EQ may be ac coupled to the rest of the circuit.

The equalization amplifier remains functional in all three modes, although in the tone mode, its function has no consequence when the circuit is configured as shown in Figure 1.

V_{DD} REGULATOR

The V_{DD} regulator is a shunt type regulator which supplies a nominal 3.3 volts for external dialers, and/or

other circuitry. In the speech mode, the output current capability at Pin 15 is typically 550 μA. In either dialing mode, the current capacity is increased to 2.0 mA.

V_{DD} will be regulated whenever V+ is >300 mV above the regulated value. As V+ is lowered, and the internal pass transistor becomes saturated, the circuit steers current away from the external load through an internal current source, in order that the V_{DD} capacitor (C9) does not load down speech and DTMF signals at V+. As V+ is lowered below 1 volt, Pin 15 switches to a high impedance state to prevent discharging of any storage capacitors, or batteries used for memory retention.

The V_{DD} voltage is unaffected by the choice of operating mode.

DIALER INTERFACE

The dialer interface consists of the mode control pins, $\overline{MT}$ and MS (Pins 18 and 17), and the DTMF current amplifier.

The $\overline{MT}$ pin, when at a Logic "1" (> V_{DD} − 0.3 V), sets the circuit into the speech mode, independent of the state of the MS pin. When the $\overline{MT}$ pin is at a Logic "0" (< 1.0 V), the dialing mode is determined by the MS pin. When MS is at a Logic "1" (> 2.0 V), the circuit is in the pulse dialing mode, and when at a Logic "0" (< 0.3 V) the tone (DTMF) mode is in effect.

The input impedance of the $\overline{MT}$ pin is typically 100 kΩ, with the input current flowing out of the pin (from V_{DD}). The input impedance of the MS pin is typically 600 kΩ, and the input current flows into the pin (Figure 1).

The DTMF amplifier (Figure 13) is a current amplifier which transmits DTMF signals to the V+ pin, and consequently onto the Tip & Ring lines. Waveforms from a DTMF dialer are input at TI (Pin 16) through a current limiting resistor (R_7). Negative feedback around the amplifier reduces the overall gain so that return loss specifications may be met. The voltage gain is calculated using the following equation:

$$\frac{V+}{V_i} = \frac{80\ R_E}{(1\ +\ 0.795R_7\ +\ 0.4R_ER_7)}$$

(R_E, R_7 in kΩ)
where $R_E = R_L//2$ kΩ (2 kΩ = internal dynamic impedance)

Using 22 kΩ for R_7, and 600 Ω for R_L, the voltage gain is a nominal 4.3 dB. The minimum loop current at which the circuit of Figure 1 will operate without distortion is 12 mA.

The DTMF amplifier is functional only in the tone dialing mode, and the waveform at V+ is inverted from that at TI. The TI pin requires a dc bias current (into the pin) of 20–50 μA, which may be supplied by the Tone dialer circuit, or by using the biasing scheme of Figure 14.

CC (PIN 5)

The CC pin (Compensation Capacitor) has two functions: 1) to provide equalization loop stability where the normal stabilizing components are ineffective; and 2) to allow optional control of the equalization functions.

In most applications, the capacitor at LC (Pin 12) provides the required stability, and no further compensation is required. In applications where changes are forced at Pin 12 and/or 13 (e.g., see Figure 23), the LC capacitor's effectiveness may be lost. The addition of a 10 μF capacitor to Pin 5 will provide the required additional compensation.

The CC pin may be used to force the loop length compensation circuits to specific modes. Grounding CC will set the sidetone and equalization amplifiers at the low loop current values. Connecting CC to V_R will set the amplifiers at the high loop current values.

Variations in the curves of Figures 9 and 11 may be obtained by using external resistors from LR to CC, and from CC to V−.

FIGURE 10 — RECEIVE CIRCUIT

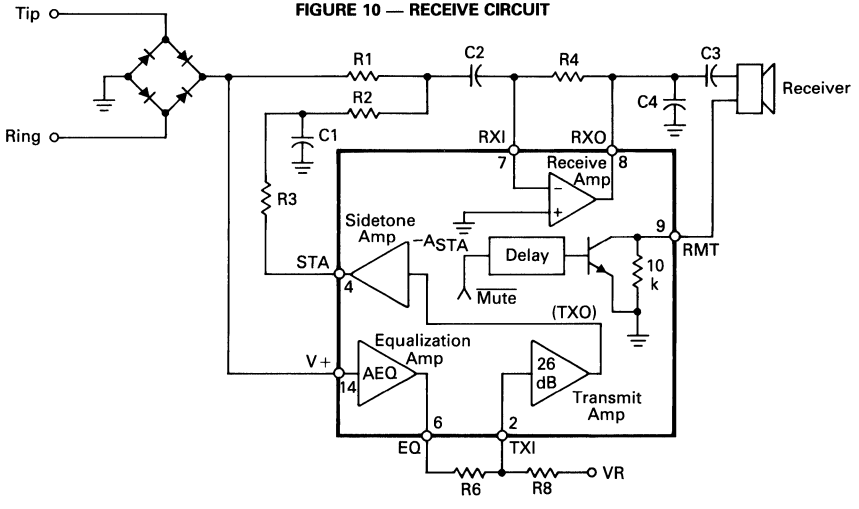


FIGURE 11 — EQUALIZATION AMPLIFIER GAIN

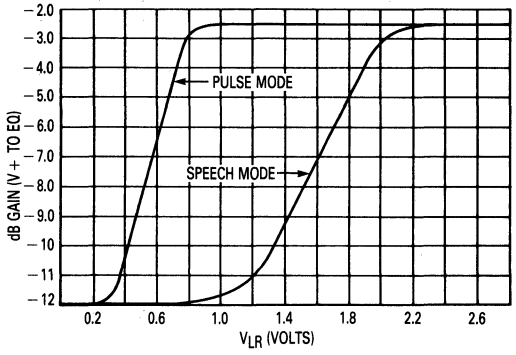


FIGURE 12 — EQ (PIN 6) DC VOLTAGE

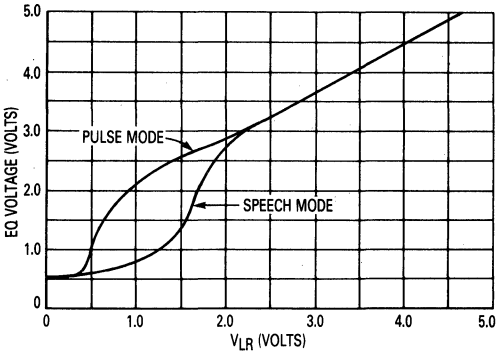


FIGURE 13 — DTMF TONE DIALER

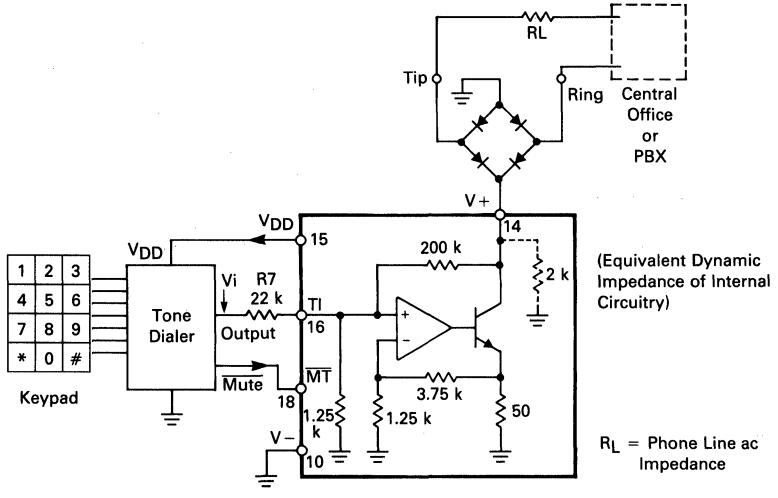
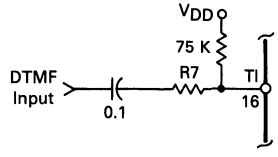


FIGURE 14 — INPUT BIASING



APPLICATIONS INFORMATION

AC IMPEDANCE

One of the basic problems with early telephones is that the performance varied with different line lengths (distance from the Central Office to the telephone). If a particular phone were optimized for short loops and then connected to a long loop, both the transmitted and receive signals would be difficult to hear. On the other hand, phones optimized for long loops would then be annoyingly loud on short loops. The process of equalization is one whereby the performance is forced to vary with loop length inversly to the expected variations. Monitoring of loop length is accomplished by monitoring the loop current at the telephone. In the MC34014, loop length equalization is provided by varying the ac impedance of the telephone circuit. In this manner the MC34014 mimics a passive network, with varistors providing the equalization.

Figure 15 depicts the situation in the receive mode. The receive signal coming from the Central Office is V_S and is independent of the loop length. Z_R is the ac impedance of the Central Office, nominally 900 Ω. Z_L is the characteristic impedance of the phone line, and is a nominal 600 Ω. The signal applied to the line (V_1) is therefore a portion of V_S. That signal is attenuated by the distributive impedance of the phone line, with a resulting signal V_2 at the telephone. The amplitude of V_2 depends on the amount of attenuation, the impedance of the phone line at the telephone and the ac impedance of the telephone (Z_{ac}), according to:

$$V_2 = \frac{V_1' \times Z_{ac}}{Z_{ac} + Z_L}$$

where V_1' is the equivalent signal source at the receive end of the phone line, providing the signal V_2 through the impedance equal to the characteristic impedance of the line (Z_L). The value of V_1' depends on how much V_1 has been attenuated by the length of phone line. By increasing Z_{ac} on long loops, V_2 is a greater portion of V_1', resulting in a stronger receive signal at the telephone.

FIGURE 15 — RECEIVE MODE

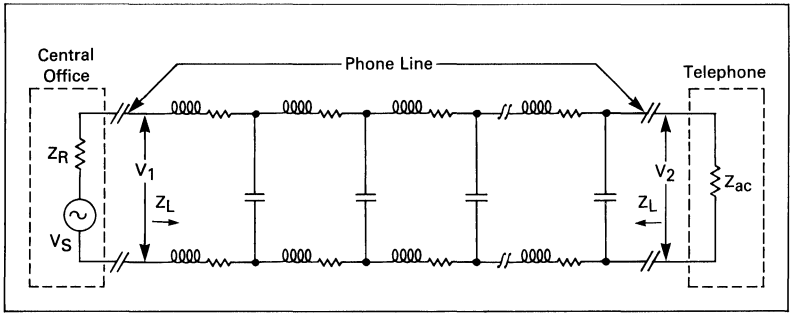
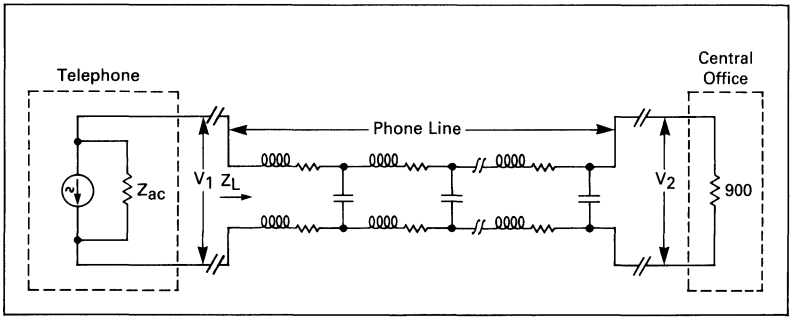


Figure 16 depicts the situation in the transmit mode. In this mode, the MC34014 is an ac current source, with a finite output impedance, modulating the loop current. The voltage signal V_1 is therefore equal to the ac signal current acting on Z_{ac} in parallel with the characteristic impedance of the phone line (Z_L). The signal is attenuated by the distributive impedance of the phone line, and so only a portion of that signal (V_2) appears at the Central Office. By increasing Z_{ac} on long loops, V_1 is increased, resulting in a higher signal level at V_2.

FIGURE 16 — TRANSMIT MODE



The ac impedance of the telephone circuit is determined by the transmit amplifier, equalization amplifier, and external resistors R_6, R_8, and R_9. In Figure 17, a portion of the receive signal at V+ appears at EQ. That signal is reduced at TXI by the R_8-R_6 divider (the electret microphone is a high impedance). The signal at TXI is then amplified by 20, and that signal (at TXO) is converted to an ac current by R9. The ac impedance of the circuit is therefore $V+/I_{TXO}$, and is defined by the following equation:

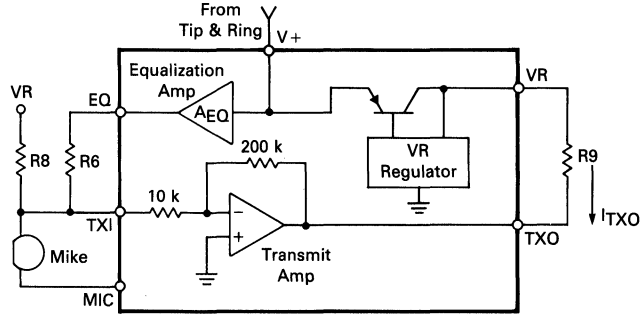
$$Z_{ac} = \frac{(1 + R_8/R_6)(R_9)}{20 \times A \times (R_8/R_6)}$$

where A = the gain of the equalization amplifier (0.25 to 0.75)

Since the gain of the equalization amplifier varies by a factor of 3, the ac impedance will vary the same amount. Using the resistor values indicated in Figure 1, the ac impedance will vary from 280 Ω (short loop) to 840 Ω (long loop).

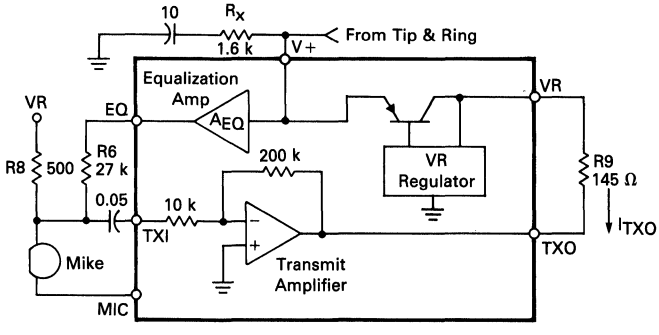
When calculating or measuring the ac impedance, capacitor C_6 (≈8.0 kΩ at 1.0 kHz) and the dynamic impedance of the MC34014 (≈10 kΩ) must be taken into account. If the microphone has an impedance lower than that of a typical electret, then its dynamic impedance must be accounted for in the above equation.

FIGURE 17 — DETERMINING AC IMPEDANCE



If a variation in Z_{ac} of less than 3:1 is desired, the circuit configuration of Figure 18 may be used. The ac impedance is the parallel combination of R_X and the impedance presented by the remainder of the circuit. With the values shown in Figure 18, the ac impedance varies from 400 Ω to 800 Ω.

FIGURE 18 — REDUCED AC IMPEDANCE VARIATION



TRANSMIT DESIGN PROCEDURE

Referring to Figure 17, first select R_9 for the desired maximum output level at Tip & Ring, assuming a signal level at TXO of 1.0 V p-p. The maximum signal level at Tip & Ring will be approximately:

$$\frac{(V_{TXO})\ (Z_L)}{R_9}$$

where Z_L is the characteristic ac impedance of the phone line. Capacitor C_6 and the ≈10 kΩ dynamic impedance of the MC34014 must also be considered in the above computation, since they are in parallel with Z_L.

The next step is to select the R_6/R_8 ratio, according to the required Z_{ac}, using the equation on the previous page. Then R_8 is selected to set the microphone sensitivity. R_8 is typically in the range of 0.5 k to 1.5 kΩ, and is dependent on the characteristics of the microphone. R_6 is then calculated from the above mentioned ratio.

HANDSET/HANDS-FREE TELEPHONE

Figure 23 indicates a circuit using the MC34014 speech network, MC34018 speakerphone circuit, and the MC34017 tone ringer to provide a complete telephone/speakerphone. Switch HS (containing one normally open and one normally closed contact) is the hook switch actuated by the handset, shown in the on-hook position. When the handset is off-hook (HS1 open, HS2 closed), power is applied to the MC34014, and consequently the handset, and the $\overline{CS}$ pin of the MC34018 is held high so as to disable it. Upon closing the two poles of switch SS, and placing switch HS in the on-hook position, power is then applied to both the MC34014 and the MC34018, and $\overline{CS}$ is held low, enabling the speakerphone function. Anytime the handset is removed from switch HS, the circuit reverts to the handset mode. The diode circuitry sets the MC34014 to the pulse dialing mode to mute the handset microphone and receiver when using the speakerphone. To compensate for the different equalization response of the MC34014 when in the pulse dialing mode (Figures 9 and 11), the 47 Ω resistor normally found at Pin 13 of the MC34014 is instead divided into two resistors (33 Ω and 15 Ω). This arrangement provides similar equalization response in both the handset and in the speakerphone modes. Since the LC capacitor (Pin 12) is ineffective in the speakerphone mode, a capacitor is added at Pin 5 (CC) to provide compensation for the equalization loop when the speakerphone mode is in effect.

FIGURE 19 — ALTERNATE MICROPHONE BIAS

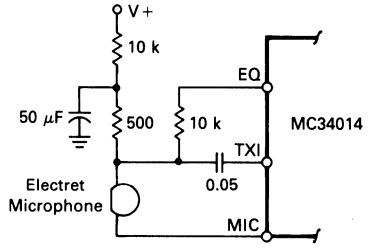
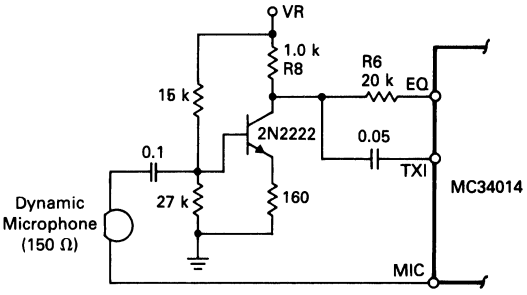


FIGURE 20 — INTERFACING A DYNAMIC MICROPHONE



The overall gain from the microphone to V+ will vary with loop current due to the influence of the equalization amplifier on TXI. The signal at EQ is out of phase with that at TXI, therefore the signal at V+ decreases as loop current (and the EQ signal) increases. Variations are typically 2.0 to 5.0 dB and depend largely on the impedance characteristics of the microphone.

ALTERNATE MICROPHONE BIASING

In the event that the microphone cannot be properly biased from the 1.2 volt VR supply, a higher voltage can be obtained by biasing from the V+ supply. The configuration shown in Figure 19, provides a higher voltage to the microphone, and also filters the speech signals at V+ from reaching it, preventing an oscillatory loop from forming. The maximum voltage limit of the microphone must be considered when biasing this way.

If a dynamic microphone is to be used in place of an electret unit, the circuit in Figure 20 will buffer its low impedance from the MC34014 circuit, maintaining the high impedance required at the junction of R_8 and R_6. The circuit shown provides a gain of ≈2.6 for the microphone signals, and can be adjusted by varying the 160 Ω resistor.

SWITCHABLE TONE/PULSE TELEPHONE

Figure 21 indicates a switchable tone/pulse telephone circuit using the MC145412 tone/pulse dialer, MC34014 speech network, and the MC34017 tone ringer. The dialer is programmable, and can store up to 10 phone numbers. As can be seen, the interface to the MC34014 is straightforward.

PULSE ONLY TELEPHONE

Figure 22 indicates a pulse only telephone circuit using the MC145409 pulse dialer, MC34014 speech network, and the MC34017 tone ringer. The dialer has last number redial, and provides a pacifier tone to the receiver during dialing.

FIGURE 21 — COMPLETE TELEPHONE WITH PULSE/TONE DIALING

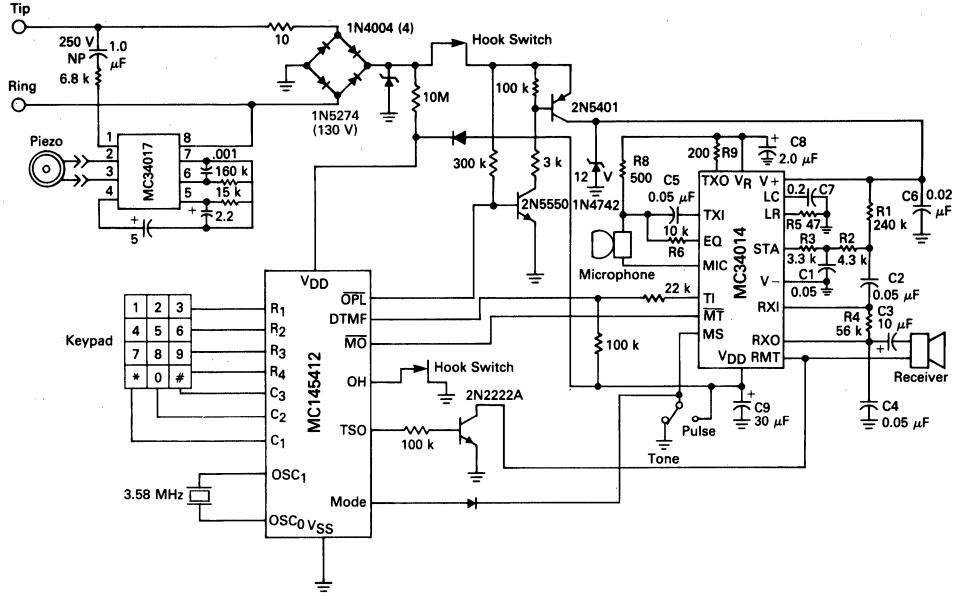


FIGURE 22 — COMPLETE TELEPHONE WITH PULSE DIALING

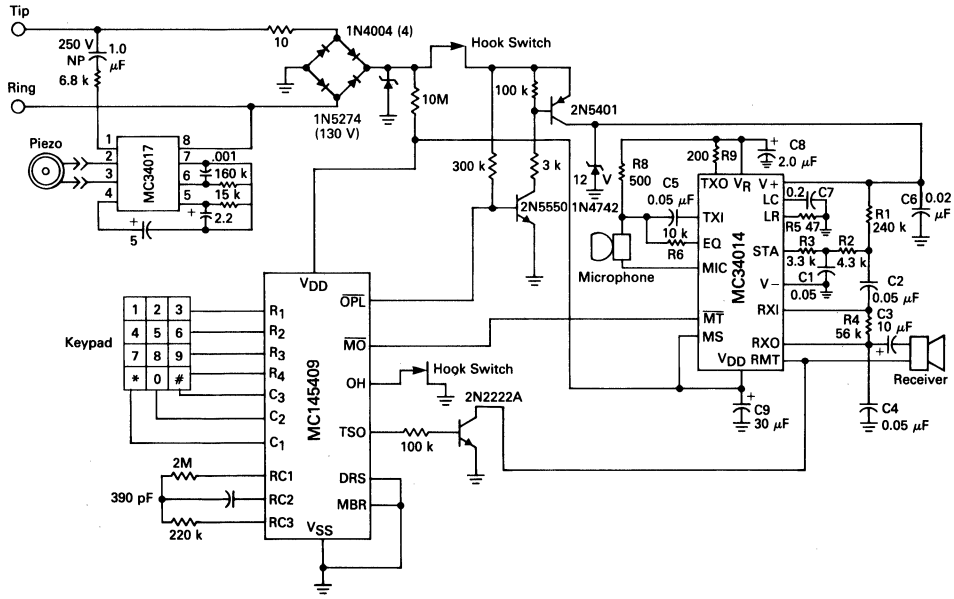
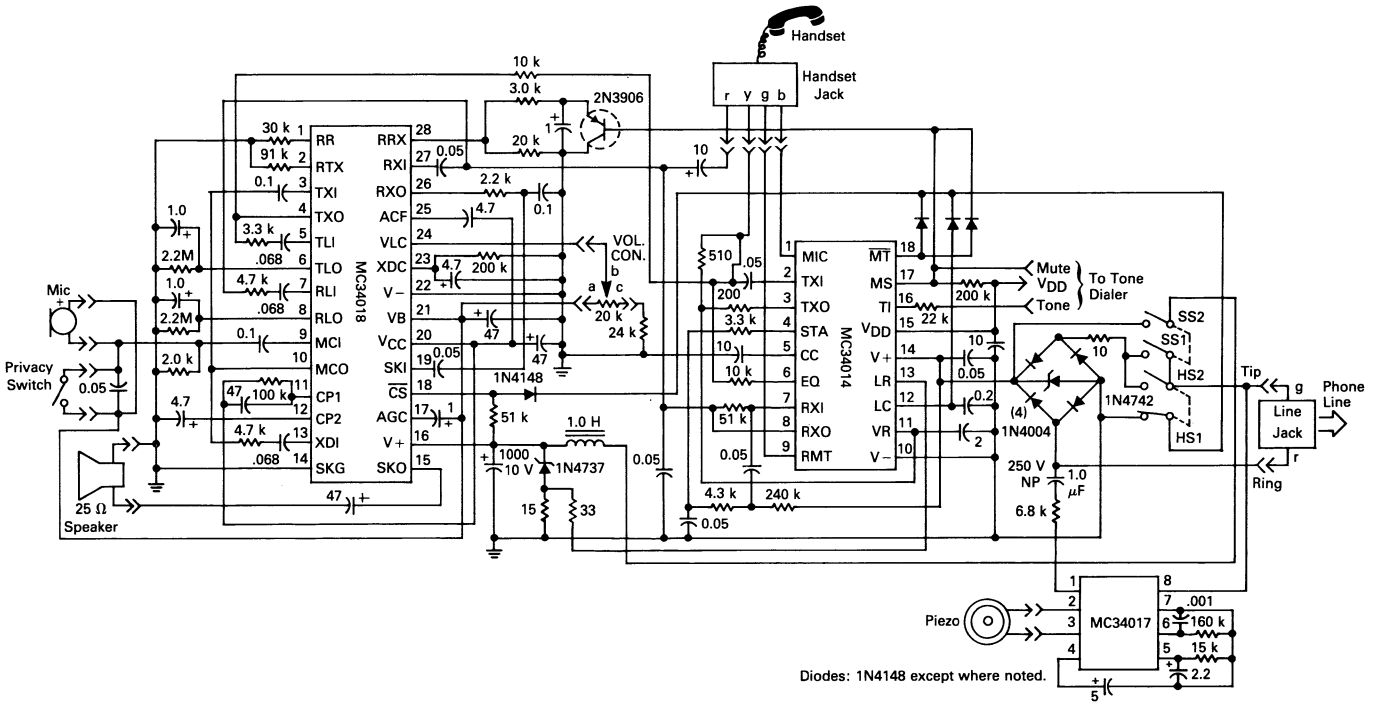


FIGURE 23 — SWITCHABLE HANDSET/HANDSFREE SYSTEM



Recommended External Components

Piezo Sounder
Models KSN 1113-1116
Motorola, Inc.
Albuquerque, N.M.
505-822-8801

Microphone/Receiver
Microphone model EM-95
Receiver model DH-34
Primo Microphone, Inc.
Elk Grove Village, Ill.
312-595-1022

Microphone Model KUC2123
Hosiden Electronics
Chicago, Ill.
312-956-7707

2

TRANSIENT PROTECTION & RFI SUPPRESSION

Protection from voltage transients is necessary in most telephone circuits, and may take the form of zener diodes, RC or LC filters, transient suppressors, or a combination of the above.

Potential radio frequency interference problems should be addressed early in the electrical and mechanical design of the telephone. RFI may enter the circuitry through the Tip & Ring lines, through the microphone and/or receiver leads in the handset cord, or through any of the wiring or PC board traces. Ceramic decoupling capacitors, ferrite beads, and other RFI suppression techniques may be needed. Good PC board design techniques, such as the avoidance of loops, should be used. Long tracks on high impedance nodes should be avoided.

MOTOROLA

MC34016

Advance Information

Cordless Universal Telephone Interface

The MC34016 is a telephone line interface meant for use in cordless telephone base stations for CT0, CT1, CT2 and DECT. The circuit forms the interface towards the telephone line and performs all speech and line interface functions like dc and ac line termination, 2–4 wire conversion, automatic gain control and hookswitch control. Adjustment of transmission parameters is accomplished by two 8 bit registers accessible via the integrated serial bus interface and by external components.

- DC Masks for Voltage and Current Regulation
- Supports Passive or Active AC Set Impedance Applications
- Double Wheatstone Bridge Sidetone Architecture
- Symmetrical Inputs and Outputs with Large Signal Swing Capability
- Gain Setting and Mute Function for T_X and R_X Amplifiers
- Very Low Noise Performance
- Serial Bus Interface SPI Compatible
- Operation from 3.0 V to 5.5 V

FEATURES

Line Driver Architecture

- Two DC Masks for Voltage Regulation
- Two DC Masks for Current Regulation
- Passive or Active Set Impedance Adjustment
- Double Wheatstone Bridge Architecture
- Automatic Gain Control Function

Transmit Channel

- Symmetrical Inputs Capable of Handling Large Voltage Swing
- Gain Select Option via Serial Bus Interface
- Transmit Mute Function, Programmable via Bus
- Large Voltage Swing Capability at the Telephone Line

Receive Channel

- Double Sidetone Architecture for Optimum Line Matching
- Symmetrical Outputs Capable of Producing High Voltage Swing
- Gain Select Option via Serial Bus Interface
- Receive Mute Function, Programmable via Serial Bus

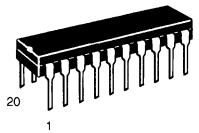
Serial Bus Interface

- 3–Wire Connection to Microcontroller
- One Programmable Output Meant for Driving a Hookswitch
- Two Programmable Outputs Capable of Driving Low Ohmic Loads
- Two Eight Bit Registers for Parameter Adjustment

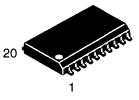
CORDLESS UNIVERSAL TELEPHONE INTERFACE

SEMICONDUCTOR TECHNICAL DATA

2

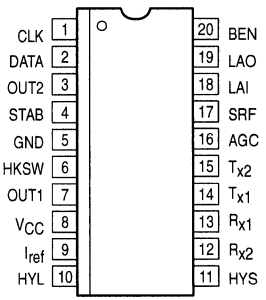


P SUFFIX
PLASTIC PACKAGE
CASE 738



DW SUFFIX
PLASTIC PACKAGE
CASE 751D

PIN CONNECTIONS



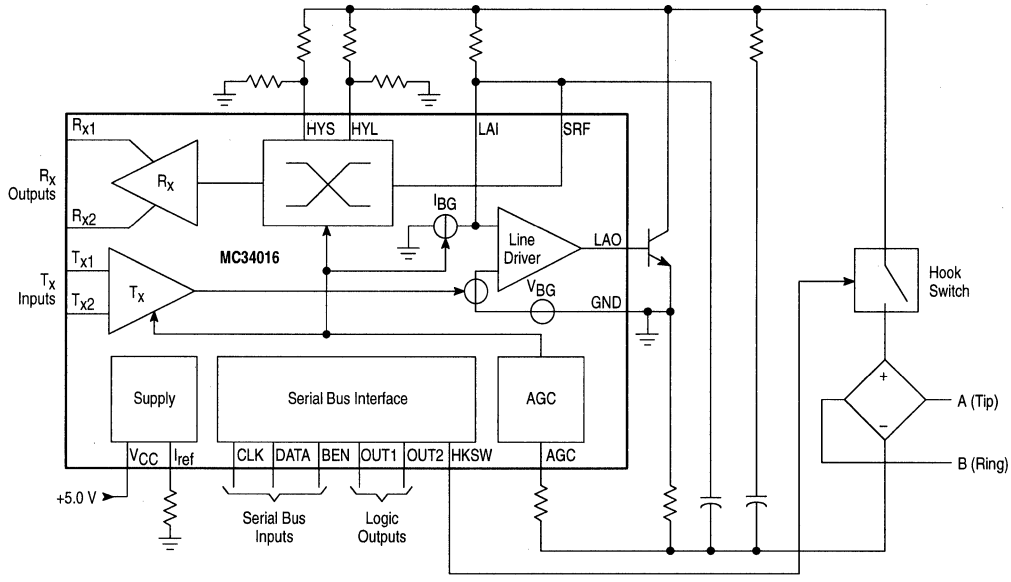
(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC34016P	T_A = –20° to +70°C	DIP
MC34016DW		SO–20

This document contains information on a new product. Specifications and information herein are subject to change without notice.

Representative Block Diagram



This device contains 610 active transistors + 242 gates.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Operation Supply Voltage	V_{CC}	–0.5, 6.5	V
All Other Inputs	V_{in}	–0.5, V_{CC} +0.5	V
Operating Ambient Temperature	T_A	–20 to +70	°C
Junction Temperature	T_J	+150	°C

DC ELECTRICAL CHARACTERISTICS (All parameters are specified with Bit 0 of Register 1 set to 1, the rest of the bits in both registers set to 0, T_A = 25°C, V_{CC} = 5.0 V, I_{line} = 15 mA, f = 1.0 kHz, Test Circuit in Figure 9, unless otherwise noted.)

Parameter	Condition	Min	Typ	Max	Unit
VOLTAGE REGULATION					
Line Voltage V_{line}	I_{line} = 5.0 mA I_{line} = 15 mA I_{line} = 60 mA	3.7 4.2 6.4	3.9 4.4 6.65	4.1 4.6 6.9	V
CURRENT REGULATION (Bit 4, Reg.1 = 1; Bit 1, Reg. 2 = 1; R_{AGC} = 47 kΩ)					
Line Voltage V_{line}	I_{line} = 15 mA	4.2	4.4	4.6	V
Line Current I_{line}	V_{line} = 10 V V_{line} = 35 V	– –	33 54	– –	mA
Line Current I_{line} in Protection Mode	V_{line} = 70 V	–	28	–	mA
DC BIASING					
Operating Supply Voltage V_{CC}	–	3.0	–	5.5	V
Current Consumption from V_{CC}	V_{CC} = 3.0 V, all Bits to 0 V_{CC} = 5.0 V, all Bits to 0	– –	3.0 3.5	4.0 4.5	mA
Source Capabiltiy Pin LAO in Speech Mode	V_{LAO} = 0.7 V	–	–	–2.0	mA
Source Capability Pin LAO in Dialing Mode (Bit 5, Reg. 1 Set)	V_{LAO} = 0.7 V	–	–	–5.0	mA
Internal Pull Down Resistor at Pin LAO	–	–	12	–	kΩ
Bias Voltage at Pins HYL, HYS and LAI	–	–	1.25	–	V
Bias Voltage at Pins T_{x1} and T_{x2}	–	–	1.5	–	V
Bias Voltage at Pins R_{x1} and R_{x2}	–	–	1.25	–	V
LOGIC INPUTS					
Logic Low Level Pins CLK, DATA, BEN	–	–	–	0.6	V
Logic High Level Pins CLK, DATA, BEN	–	2.2	–	–	V
LOGIC OUTPUTS					
Source Capability from Pins HKSW, OUT1, OUT2	Output Voltage at V_{CC} – 1.3 V	–	–	–1.0	mA
Sink Capability into Pins HKSW, OUT1, OUT2	Output Voltage at 0.5 V	5.0	–	–	mA

AC ELECTRICAL CHARACTERISTICS (All parameters are specified with Bit 0 of Register 1 set to 1, the rest of the bits in both registers set to 0, T_A = 25°C, V_{CC} = 5.0 V, I_{line} = 15 mA, f = 1.0 kHz, Test Circuit in Figure 9, unless otherwise noted.)

Parameter	Condition	Min	Typ	Max	Unit
TRANSMIT CHANNEL					
Transmit Gain from VT_X to V_{line}	VT_X = 0.1 Vrms	–1.0	0	1.0	dB
Gain Variation with Line Current Referred to I_{line} = 15 mA with the AGC Function Switched "Off"	I_{line} = 10 mA to 70 mA Bit 0, Reg. 2 = 1	–0.5	0	0.5	dB
Gain Increase in 6.0 dB Mode	Bit 4, Reg. 2 = 1	5.0	6.0	7.0	dB
Gain Reduction in Mute Condition	Bit 2, Reg. 2 = 1	70	–	–	dB
Input Impedance at T_{x1} or T_{x2}	–	24	30	36	kΩ
Maximum Input Swing for VT_X	THD ≤ 2%	–	4.0	–	V_{pp}
THD at the Line (V_{line})	VT_X = 3.0 dBm	–	1.0	2.0	%
Psophometrically Weighted Noise Level at the Line (V_{line})	200 Ω Between T_{x1} and T_{x2}	–	–79	–	dBmp
RECEIVE CHANNEL					
Receive Gain from V_{line} to VR_X	V_{line} = 0.1 Vrms	–1.0	0	1.0	dB
Gain Variation with Line Current Referred to I_{line} = 15 mA with the AGC Function Switched "Off"	I_{line} = 10 mA to 70 mA Bit 0, Reg. 2 = 1	–0.5	0	0.5	dB

AC ELECTRICAL CHARACTERISTICS (continued) (All parameters are specified with Bit 0 of Register 1 set to 1, the rest of the bits in both registers set to 0, T_A = 25°C, V_{CC} = 5.0 V, I_{line} = 15 mA, f = 1.0 kHz, Test Circuit in Figure 9, unless otherwise noted.)

Parameter	Condition	Min	Typ	Max	Unit
RECEIVE CHANNEL					
Gain Increase in 6.0 dB Mode	Bit 5, Reg. 2 = 1	5.0	6.0	7.0	dB
Gain Reduction in Mute Condition	Bit 3, Reg. 2 = 1	70	–	–	dB
Input Impedance at HYL or HYS	–	24	30	36	kΩ
Output Impedance at R_{X1} or R_{X2}	–	–	150	–	Ω
Maximum Input Swing at HYL or HYS	for THD ≤ 2%	–	800	–	mV_{pp}
Maximum Output Swing VR_X	for THD ≤ 10%	–	3.5	–	V_{pp}
Total Harmonic Distortion at VR_X	V_{line} = 3.0 dBm	–	1.0	2.0	%
Psophometrically Weighted Noise Level at VR_X	200 Ω Between T_{X1} and T_{X2}	–	80	–	µVrms
AUTOMATIC GAIN CONTROL					
Gain Reduction in Transmit and Receive Channel with Respect to I_{line} = 15 mA	I_{line} = 70 mA	5.0	6.0	7.0	dB
Highest Line Current for Maximum Gain	–	–	20	–	mA
Lowest Line Current for Minimum Gain	–	–	60	–	mA
Gain Reduction in Transmit and Receive Channel with Respect to I_{line} = 35 mA	I_{line} = 85 mA Bit 1, Reg. 2 = 1	5.0	6.0	7.0	dB
Highest Line Current for Maximum Gain	Bit 1, Reg. 2 = 1	–	40	–	mA
Lowest Line Current for Minimum Gain	Bit 1, Reg. 2 = 1	–	80	–	mA
BALANCE RETURN LOSS					
Balance Return Loss with Respect to 600Ω	f = 200–4000 Hz	18	–	–	dB
	f = 1.0 kHz	20	–	–	dB
SIDETONE					
Voltage Gain from VT_X to VR_X	I_{line} = 15 mA and 70 mA, Bit 0, Reg. 2 = 1	–	–	–20	dB
SERIAL BUS					
Clock Frequency	–	–	–	550	kHz
BEN Rising Edge Setup Time Before First CLK Rising Edge	See t_1 in Timing Diagram	500	–	–	ns
DATA Setup Time Before CLK Rising Edge	See t_2 in Timing Diagram	500	–	–	ns
DATA Hold Time After CLK Rising Edge	See t_3 in Timing Diagram	500	–	–	ns
BEN Falling Edge Delay Time After Last CLK Rising Edge	See t_4 in Timing Diagram	1.5	–	–	µs
BEN Rising Edge Delay Time After Last BEN Falling Edge	See t_5 in Timing Diagram	6.0	–	–	µs
Power Supply Reset Voltage V_{CC}	–	–	2.5	–	V

PIN FUNCTION DESCRIPTION

Pin	Symbol	Description
1	CLK	Serial bus clock input
2	DATA	Serial bus data input
3	OUT2	Logic output 2
4	STAB	Line driver compensation
5	GND	Ground
6	HKSW	Logic output for the hook switch
7	OUT1	Logic output 1
8	V_{CC}	Supply input (+5.0 V)
9	I_{ref}	Reference current adjustment
10	HYL	Hybrid input for long lines
11	HYS	Hybrid input for short lines
12	R_{X2}	Receive output 2
13	R_{X1}	Receive output 1
14	T_{X1}	Transmit input 1
15	T_{X2}	Transmit input 2
16	AGC	Automatic gain control input
17	SRF	Sidetone reference input
18	LAI	Line amplifier input
19	LAO	Line amplifier output
20	BEN	Serial bus enable input

Throughout this part, please refer to the typical application of Figure 10. The data given in this chapter refers to typical data of the characteristics.

DC OPERATION

For dc, the MC34016 incorporates four different masks which can be selected via the serial bus interface:

Bit 4, Reg. 1 'DC Mask'	Bit 5, Reg. 1 'DC Mode'	Bit 1, Reg. 2 'AGC Ratio'	DC Mask Selected
0	0	X	Voltage Regulation Mask
X	1	X	Pulse Dial Mask
1	0	0	Current Regulation Mask with AGC Ratio 1:2
1	0	1	Current Regulation Mask with AGC Ratio 3:5

X = don't care

Voltage Regulation Mask

The voltage regulation mask is the default setting of the MC34016 after power–up. In this mode, the circuit behaves as a zener with a series resistor. The line voltage can be expressed as:

$$V_{line} = V_{BG} + (I_{DC} \times R_{DC1}) + (I_{line} \times R_S)$$

with: V_{BG} = 1.25 V
I_{DC} = 5.1 µA
R_{DC1} = DC setting resistor of 470 kΩ in the typical application
I_{line} = Line current
R_S = Slope resistor of 50 Ω in the typical application

thus: $V_{line} = 3.65 + (50 \times I_{line})$

By choosing different values of R_{DC1}, the zener voltage can be adjusted to fit country specific requirements. In Figure 1, a curve shows V_{line} versus I_{line} for different R_{DC1} values.

Pulse Dial Mask

In this mask, the circuit is forced into a very low voltage drop mode meant for pulse dialing (e.g. make period during pulse dialing). Pin LAO of the MC34016 sources a current of 5.0 mA in this mode, saturating output transistor Q1. The line voltage V_{line} is now determined by the saturation voltage of Q1 and the dc slope resistor R_S:

$$V_{line} = V_{CE(sat)Q1} + (R_S \times I_{line}) \cong 0.1 + (50 \times I_{line})$$

Figure 2 shows V_{line} versus I_{line}.

Current Regulation Masks

These masks are equal to the voltage regulation mask up to a knee current. Above this current, the dc slope changes to a higher value fulfilling requirements such as those in France.

$$V_{line} = 3.65 + (R_S \times I_{line}) \quad \text{for } I_{AGC} < I_{knee}$$
$$V_{line} = [I_{DC} + (2.5 \times (I_{AGC} - I_{knee}))] \times R_{DC1} + [V_{BG} + (R_S \times I_{line})] \quad \text{for } I_{AGC} > I_{knee}$$

with: $I_{AGC} = I_{line} \times \frac{R_S}{R_{AGC}}$

I_{knee} = 20 µA for AGC ratio 1:2
I_{knee} = 30 µA for AGC ratio 3:5

With R_S = 50 Ω and R_{AGC} = 47 kΩ, and the AGC ratio set to 3:5, I_{AGC} will equal I_{knee} at a line current of 28.2 mA. With the AGC ratio set to 1:2, the knee occurs at 18.8 mA. Above these line currents, it can be derived that the dc slope of the circuit changes to:

$$R_{Slope} = 2.5 \times \frac{R_S \times R_{DC1}}{R_{AGC}} + R_S$$

With the component values mentioned, a slope of 1300 Ω will occur. Figure 3 and 4 shows V_{line} versus I_{line} in the two current regulation masks for different values of R_{DC1}.

When I_{AGC} reaches 60 µA for AGC ratio 3:5 or 50 µA in case of AGC ratio 1:2, the MC34016 will enter protection mode after about 800 ms. In practice this mode occurs only under overload conditions. In protection mode, the MC34016 decreases the power dissipation in Q1 by drastically increasing the dc slope starting from I_{knee}. This results in a reduced line current which remains practically constant over line voltage. With the equation for Iagc it can be derived that:

AGC ratio	Line Current to Enter Protection Mode	Line Current in Protection Mode
3:5	56.4 mA	28.2 mA
1:2	47.0 mA	18.8 mA

Once the MC34016 enters protection mode, it remains there until the output HKSW is toggled via Bit 0 of Register 1 (on–hook, off–hook).

Supply Voltage V_{CC}

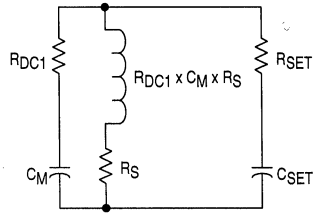
The MC34016 operates from an external supply within a voltage range of 3.0 V to 5.5 V. The current consumption with all bits set to 0, equals 3.0 mA at 3.0 V and 3.5 mA at 5.5 V.

AC SET IMPEDANCE

The MC34016 offers two possibilities for the adjustment of the ac set impedance. Either a passive or an active set impedance can be obtained.

Passive Set Impedance

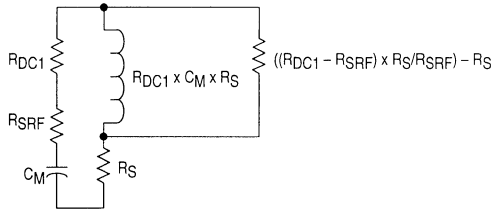
In this application, the set impedance is formed by the ac impedance of the circuit itself in parallel with resistor R_{SET} and capacitor C_{SET}. An equivalent network equals:



With the component values of the typical application, the inductor has a value of about 2.4 H and R_{DC1} equals 470 kΩ. In the audio range of 300–3400Hz, these components form a fairly large parallel impedance to R_{SET} and C_{SET}. Therefore, the set impedance is mainly determined by the passive network R_{SET} and C_{SET}. In the typical application, R_{SET} is 600 Ω, but it can easily be replaced by a complex network to obtain a complex set impedance.

Active Set Impedance

An active set impedance can be obtained by placing a resistor between pin LAI and SRF (R_{SRF}) as shown in Figure 11. By doing so, the MC34016 itself generates the ac set impedance and R_{SET} and C_{SET} can be omitted. An equivalent network now equals:



Ignoring the effect of the inductor and the parallel path R_{DC1} + R_{SRF} again for audio frequencies, the set impedance is now determined by:

$$Z_{SET} = \frac{R_S}{R_{SRF}} \times (R_{DC1} + R_{SRF})$$

With R_S = 50 Ω and R_{DC1} = 470 kΩ, R_{SRF} should be 43 kΩ to obtain a 600 Ω set impedance. To obtain a complex set impedance, R_{DC1} can be made complex. In such case, the dc mask can be adjusted with the dc value of R_{DC1} and the set impedance can be adjusted with the ac value of R_{DC1}. An application with an active set impedance is interesting, particularly in countries like France, where with the dc current regulation mask, rather high line voltages can be reached. With a passive set impedance, this would result in a high cost for capacitor C_{SET}.

TRANSMIT CHANNEL

Inputs

The inputs T_{X1} and T_{X2} are designed to handle large signal levels of up to +3.0 dBm. The input impedance for both T_{X1} and T_{X2} equals 30 kΩ. The inputs are designed for symmetrical as well as asymmetrical use. In asymmetrical drive, one input can be tied to GND via an external capacitor.

Gain

The gain from inputs T_{X1} and T_{X2} to the line is dependent on the set impedance, the line load impedance and dc slope resistor R_S in the following way:

$$A_{TX} = \frac{1}{6 \times R_S} \times \frac{Z_{SET} \times Z_{line}}{Z_{SET} + Z_{line}}$$

With Z_{SET} = 600 Ω, Z_{line}=600 Ω and R_S = 50 Ω the gain equals 0 dB. By setting Bit 4 of Register 2 to 1, the gain is raised by 6.0 dB.

Outputs

In order to transmit signals to the line, the output stage of the MC34016 (line driver) modulates the zener previously described. To guarantee stability of the output stage capacitor C_{STB} of 100 pF is required

SIDETONE

The MC34016 is equipped with a double Wheatstone bridge architecture to optimize sidetone. One sidetone network is used for short lines and one for long lines. Switchover between both networks is dependent on line current and is described in the automatic gain control section. Different sidetone equations apply depending on whether a passive or an active set impedance is set.

Sidetone Cancellation with Passive Set Impedance

In a passive set impedance application, the set impedance is a part of the equations for optimum sidetone. For short lines optimum cancellation occurs if:

$$Z_{HS1} = \frac{R_{HS2}}{R_S} \times \frac{Z_{SET} \times Z_{lineshort}}{Z_{SET} + Z_{lineshort}}$$

with: $Z_{lineshort}$ = impedance of a short telephone line

and for long lines:

$$Z_{HL1} = \frac{R_{HL2}}{R_S} \times \frac{Z_{SET} \times Z_{linelong}}{Z_{SET} + Z_{linelong}}$$

with: $Z_{linelong}$ = impedance of a long telephone line

Sidetone Cancellation with Active Set Impedance

In the active set impedance application, the set impedance does not appear in the equations for optimum sidetone cancellation as it does in the passive application. For short lines, optimum cancellation occurs if:

$$Z_{HS1} = \frac{R_{HS2}}{R_S} \times Z_{lineshort}$$

and for long lines:

$$Z_{HL1} = \frac{R_{HL2}}{R_S} \times Z_{linelong}$$

RECEIVE CHANNEL

Inputs

The inputs HYS and HYL have an input resistance of 30 kΩ and can handle signals up to 800 mV_{pp}. This corresponds to a signal at the telephone line of about 8.0 dBm in the typical application. The switchover from HYS to HYL is dependent on line current and described in the automatic gain control section.

Gain

The overall gain from telephone line to R_{X1} and R_{X2} is 0 dB for the typical application. This gain can be raised by 6.0 dB by setting Bit 5 of Register 2.

Outputs

The outputs R_{X1} and R_{X2} of the receive channel have an output impedance of 150 Ω and are designed to drive a 10 kΩ resistive load or a 47 nF capacitive load with a 3.5 V_{pp} swing.

AUTOMATIC GAIN CONTROL

The automatic gain control function (AGC) controls the transmit and receive gains and the switchover for the sidetone networks for short and long lines according to the line current (which represents line length). The effect of AGC on the transmit and receive amplifiers is 6.0 dB at default and it can be disabled via the serial bus. The switchover for the sidetone networks tracks the AGC curves for the transmit and receive amplifier gain. This feature can also be disabled via the serial bus:

Bit 6, Reg. 2 'PABX Mode'	Bit 0, Reg. 2 'AGC Range'	Description
0	0	AGC Gain Range of 6.0 dB, Sidetone Switchover Enabled
0	1	No AGC Gain Range, Sidetone Switchover Enabled
1	0	AGC Range of 6.0 dB, only HYS Input Active, HYL Muted
1	1	No AGC Gain Range, only HYS Input Active, HYL Muted

The ratio between start and stop current for the AGC curves is programmable for both voltage and current regulation mode:

Bit 4, Reg. 1 'DC Mask'	Bit 1, Reg. 2 'AGC Ratio'	AGC Ratio Selected	$I_{AGCstart}$ (µA)	$I_{AGCstop}$ (µA)
0	0	Voltage Regulation, AGC Ratio 1:3	10	30
0	1	Voltage Regulation, AGC Ratio 1:2	20	40
1	0	Current Regulation, AGC Ratio 1:2	20	40
1	1	Current Regulation, AGC Ratio 3:5	30	50

The relation between line current and I_{start} and I_{stop} is given by:

$$I_{linestart} = \frac{R_{AGC}}{R_S} \times I_{AGCstart}$$

$$I_{linestop} = \frac{R_{AGC}}{R_S} \times I_{AGCstop}$$

Figures 5, 6, 7 and 8 show the AGC curves for both voltage regulation and current regulation. In current regulation, the start point for the AGC curves is coupled to the knee point of the dc characteristic, or: $I_{knee} = I_{AGCstart}$.

LOGIC OUTPUT DRIVERS

The MC34016 is equipped with three logic outputs meant to interface to the front end of a telephone. The outputs can be controlled via the serial bus interface. As shown in the characteristics, the logic outputs are capable of sourcing at least 1.0 mA and sinking at least 5.0 mA.

Output HKSW

Output HKSW is dedicated to drive the hookswitch. With HKSW low, the line is opened via Q2 and Q3 and automatically switches off the line driver transistor Q1. This feature guarantees fast dc settling after line breaks occurring during pulse dialing.

Outputs OUT1 and OUT2

Outputs OUT1 and OUT2 may be used for any logic function, such as control of an earth switch and/or a shunt wire.

SERIAL BUS INTERFACE

The serial interface of the MC34016 enables a simple three wire connection to a micro controller.

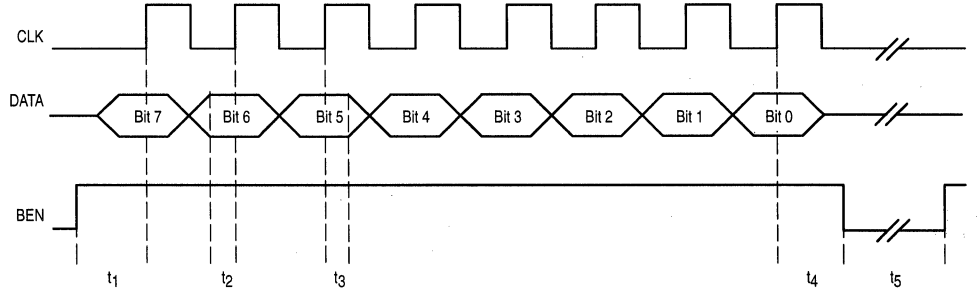
Timing

Times t_1, t_2, t_3, t_4 and t_5 are specified in the electrical characteristics.

With BEN high, data can be clocked into the serial port by using DATA and CLK lines. On the rising edge of the CLK, the data enters the MC34016. The last 8 bits of data entered are shifted into the registers when BEN is forced low. With BEN low, the serial port of the MC34016 is disabled. BEN must be kept low until the next register update is needed. Data should be written by entering the most significant bit first (Bit 7) and the least significant bit (Bit 0) last.

With BEN low, the DATA and CLK lines may be used to control other devices in the application.

Timing Diagram



Registers

The MC34016 is equipped with 2 eight bit registers which are selected by the value of the most significant bit (Bit 7). If the supply voltage of the MC34016 drops below 2.5 V, all registers are set to 0. This RESET function enables a smooth power–up of the device. The registers are as follows:

Register 1 (Bit 7 = 0)

Bit	Function	Operation	Default
0	Output HKSW	0: HKSW is Low 1: HKSW is High	0
1	Output OUT1	0: OUT1 is Low 1: OUT1 is High	0
2	Output OUT2	0: OUT2 is Low 1: OUT2 is High	0
3	Not Used	–	–
4	DC Mask	0: Voltage Regulation Mask 1: Current Regulation Mask for France	0
5	DC Mode	0: Speech Mode/Normal Operation 1: Dialing Mode for Low Voltage Drop	0
6	Test Mode	Only Used During Manufacturing	0

Register 2 (Bit 7 = 1)

Bit	Function	Operation		Default
0	AGC Range	0: AGC Range 6.0 dB 1: AGC Range 0 dB (Switched "Off")		0
1	AGC Ratio	Voltage Regulation: (Bit 4, Reg. 1 = 0) 0: Ratio 1:3 1: Ratio 1:2	Current Regulation: (Bit 4, Reg. 1 = 1) 0: Ratio 1:2 1: Ratio 3:5	0
2	Transmit Mute	0: Transmit Channel Active 1: Transmit Channel Muted		0
3	Receive Mute	0: Receive Channel Active 1: Receive Channel Muted		0
4	Transmit Gain	0: Transmit Channel Gain = 0 dB 1: Transmit Channel Gain = 6.0 dB		0
5	Receive Gain	0: Receive Channel Gain = 0 dB 1: Receive Channel Gain = 6.0 dB		0
6	PABX Mode	0: Normal Mode 1: PABX Mode (only Input HYS Selected)		0

Figure 1. Line Voltage versus Line Current
(Voltage Regulation Mask)

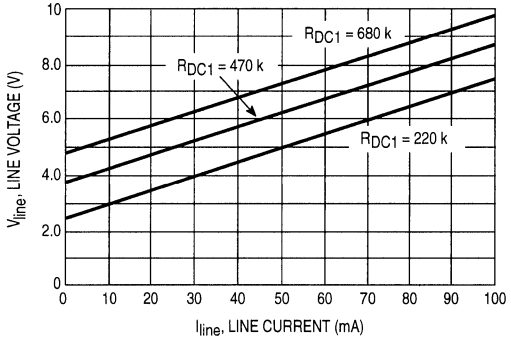


Figure 2. Line Voltage versus Line Current
(Pulse Dial Mask)

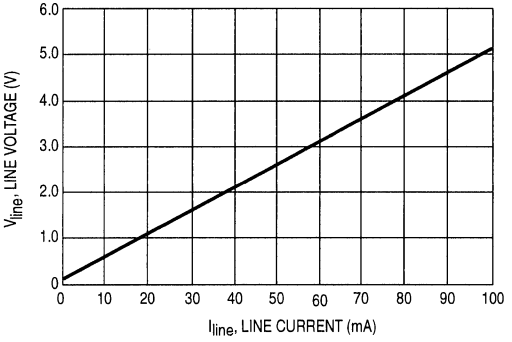


Figure 3. Line Voltage versus Line Current
(Current Regulation Mask)

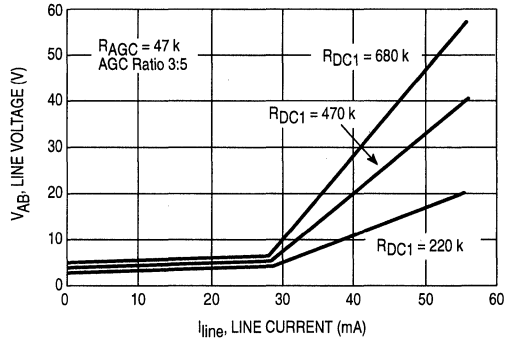


Figure 4. Line Voltage versus Line Current
(Current Regulation Mask)

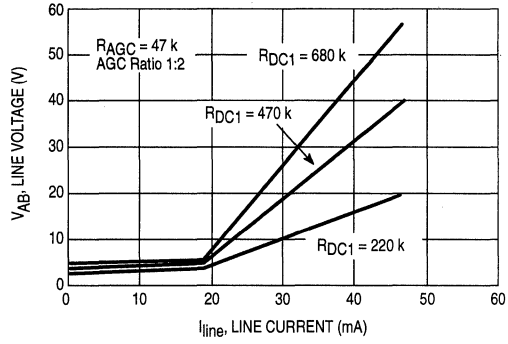


Figure 5. AGC Weighting Factor versus I_{line}
(Voltage Regulation Mask)

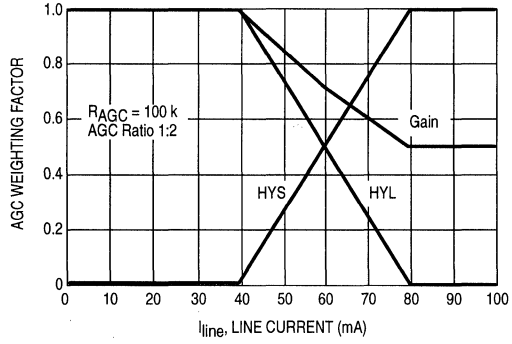


Figure 6. AGC Weighting Factor versus I_{line}
(Voltage Retulation Mask)

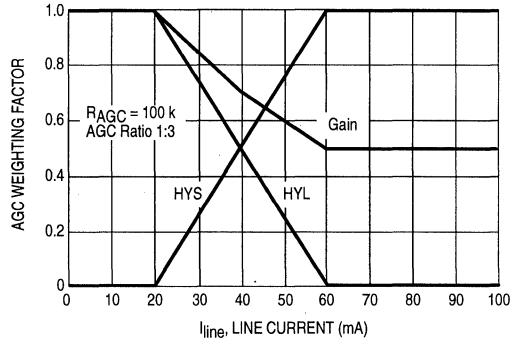


Figure 7. AGC Weighting Factor versus I_{line}
(Current Regulation Mask)

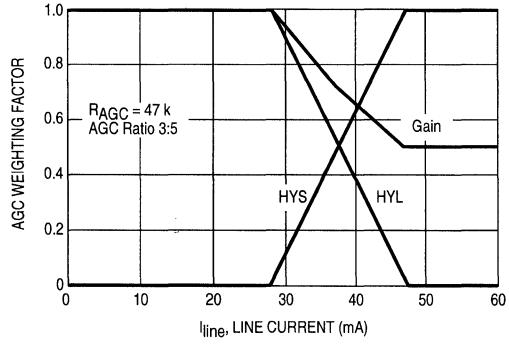


Figure 8. AGC Weighting Factor versus I_{line}
(Currrent Regulation Mask)

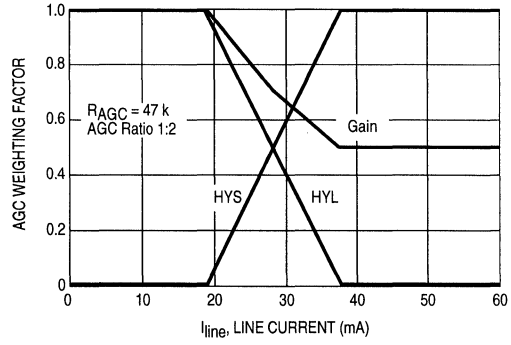


Figure 9. Test Diagram

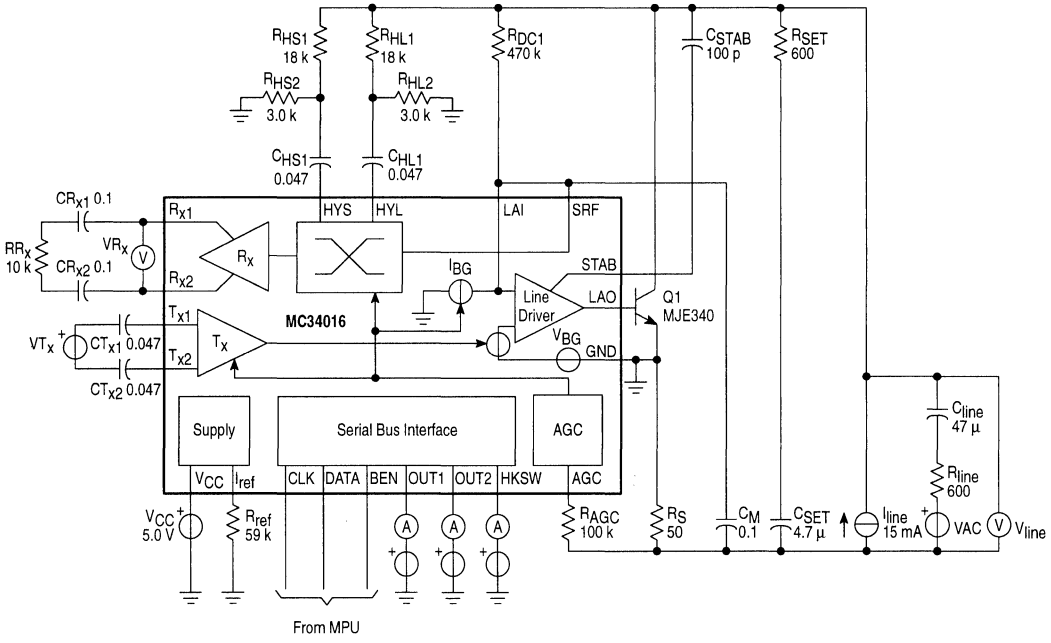


Figure 10. Typical Application with Passive Impedance

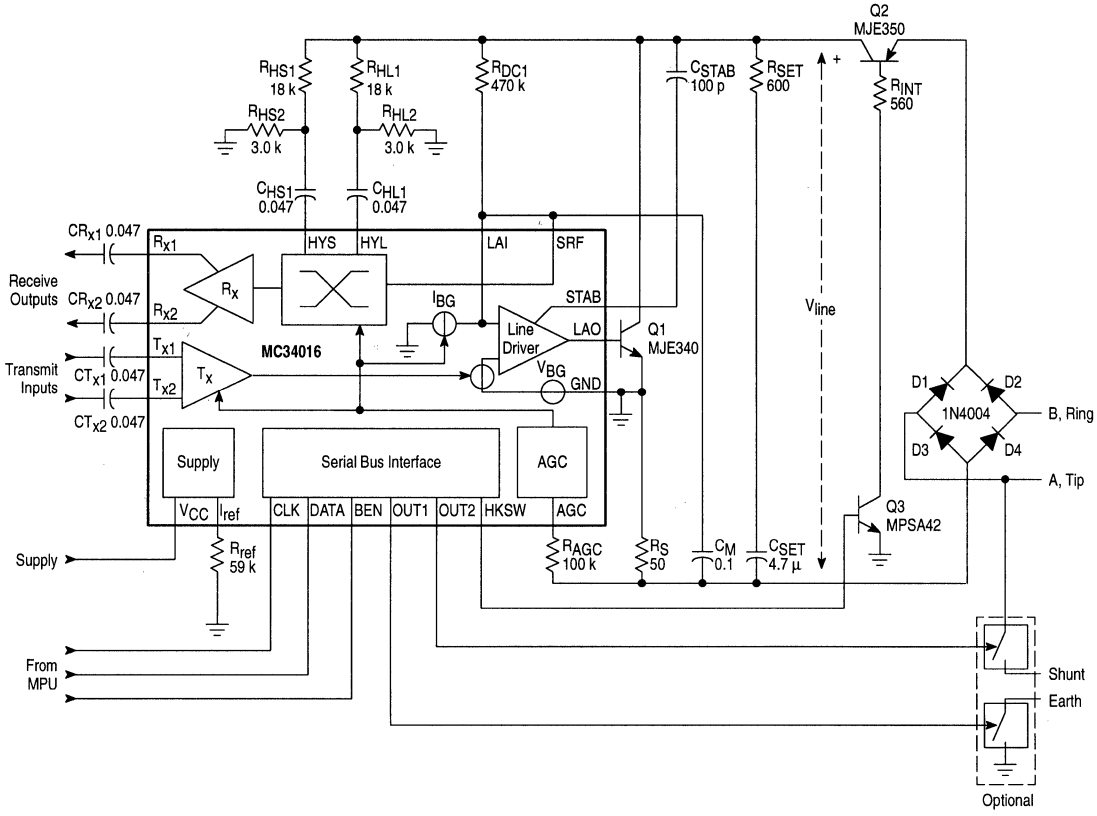
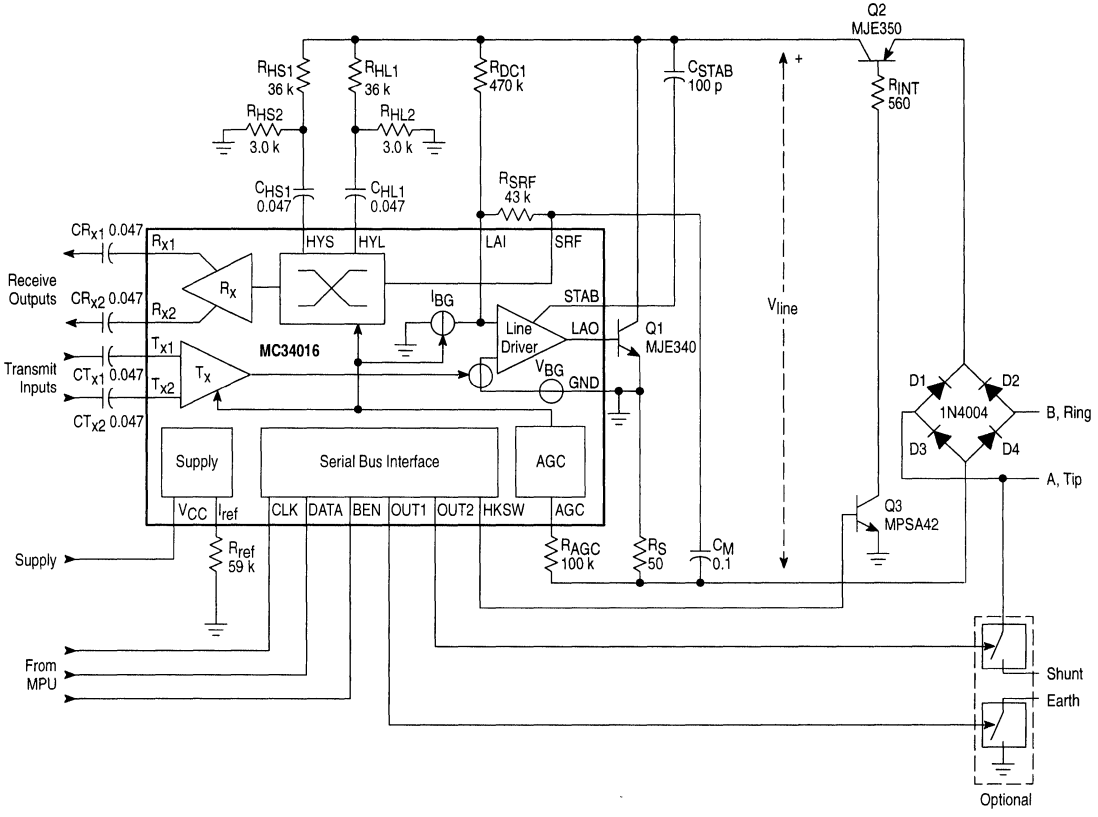


Figure 11. Typical Application with Active Impedance

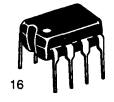


MC34017

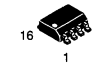
Telephone Tone Ringer

Bipolar Linear/I²L

- Complete Telephone Bell Replacement Circuit with Minimum External Components
- On–Chip Diode Bridge and Transient Protection
- Direct Drive for Piezoelectric Transducers
- Push Pull Output Stage for Greater Output Power Capability
- Base Frequency Options — MC34017–1: 1.0 kHz
  MC34017–2: 2.0 kHz
  MC34017–3: 500 Hz
- Input Impedance Signature Meets Bell and EIA Standards
- Rejects Rotary Dial Transients



P SUFFIX
PLASTIC DIP
CASE 626

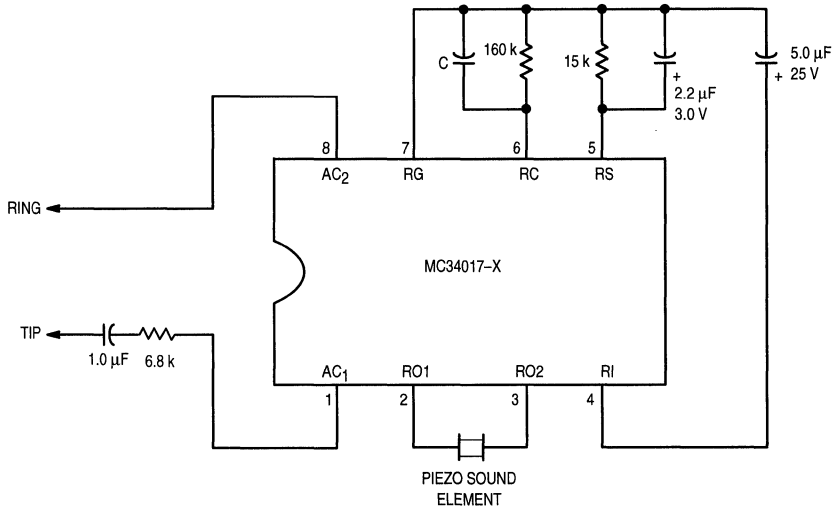


D SUFFIX
SOIC PACKAGE
CASE 751

ORDERING INFORMATION

MC34017P	Plastic DIP
MC34017D	Plastic SOIC

APPLICATION CIRCUIT



MC34017–1: C = 1000 pF
MC34017–2: C = 500 pF
MC34017–3: C = 2000 pF

REV
9/95

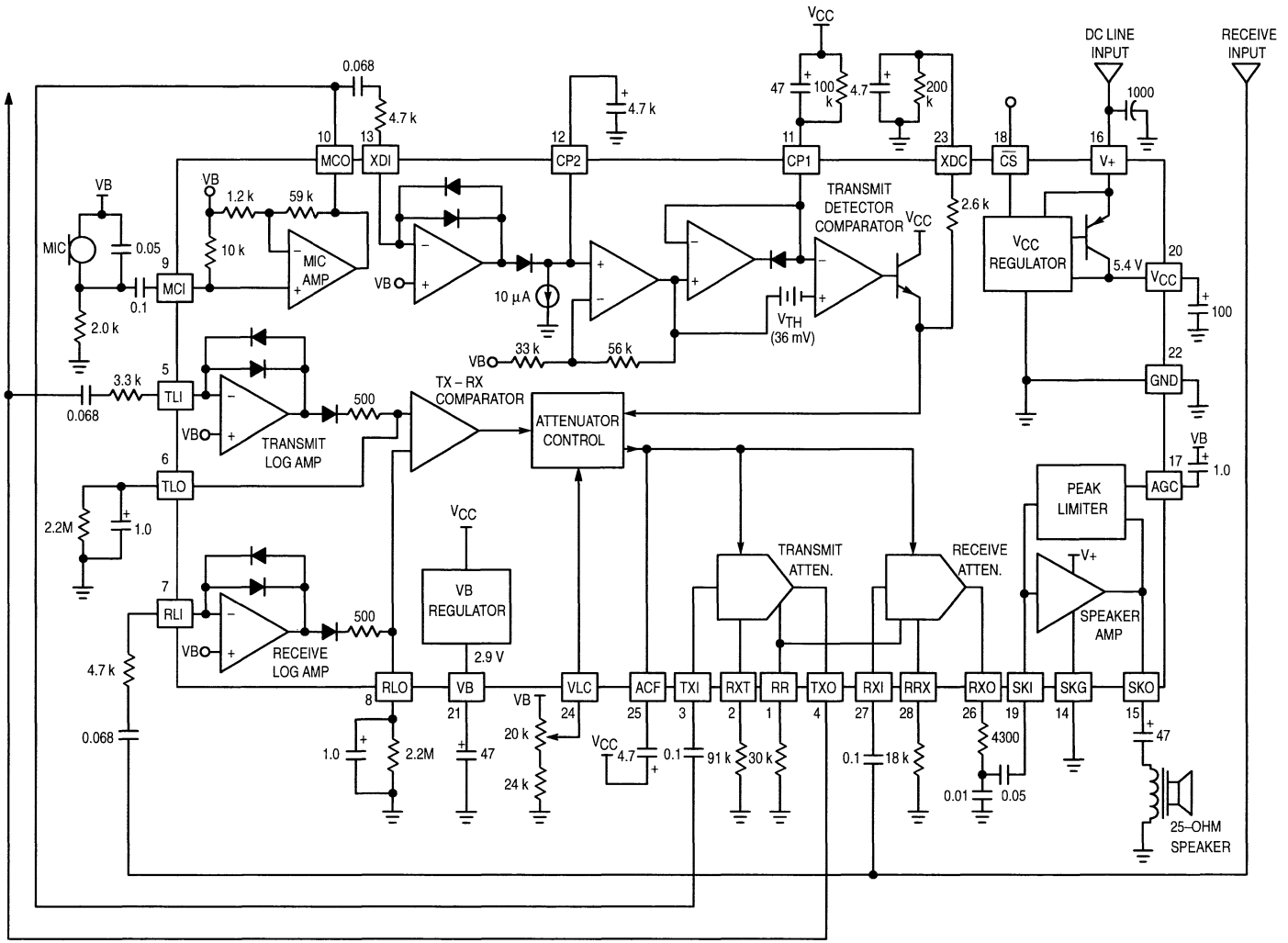


Figure 1. Test Circuit

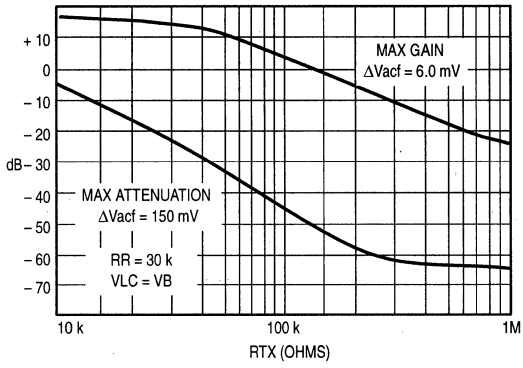


Figure 2. Transmit Attenuator versus RTX

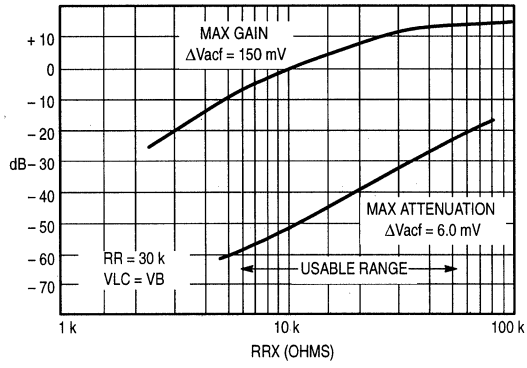
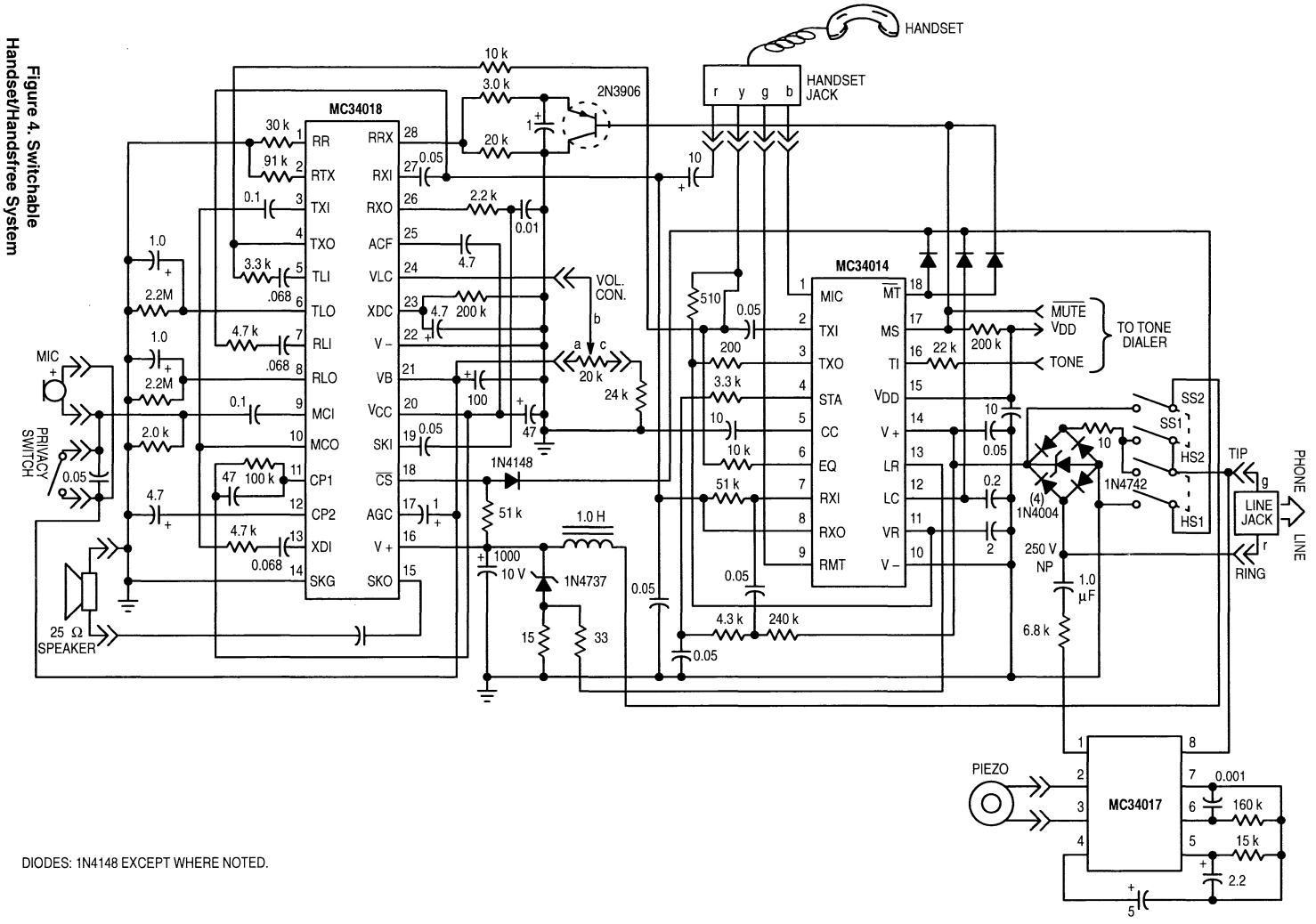


Figure 3. Receive Attenuator versus RRX

Figure 4. Switchable Handset/Handsfree System



DIODES: 1N4148 EXCEPT WHERE NOTED.

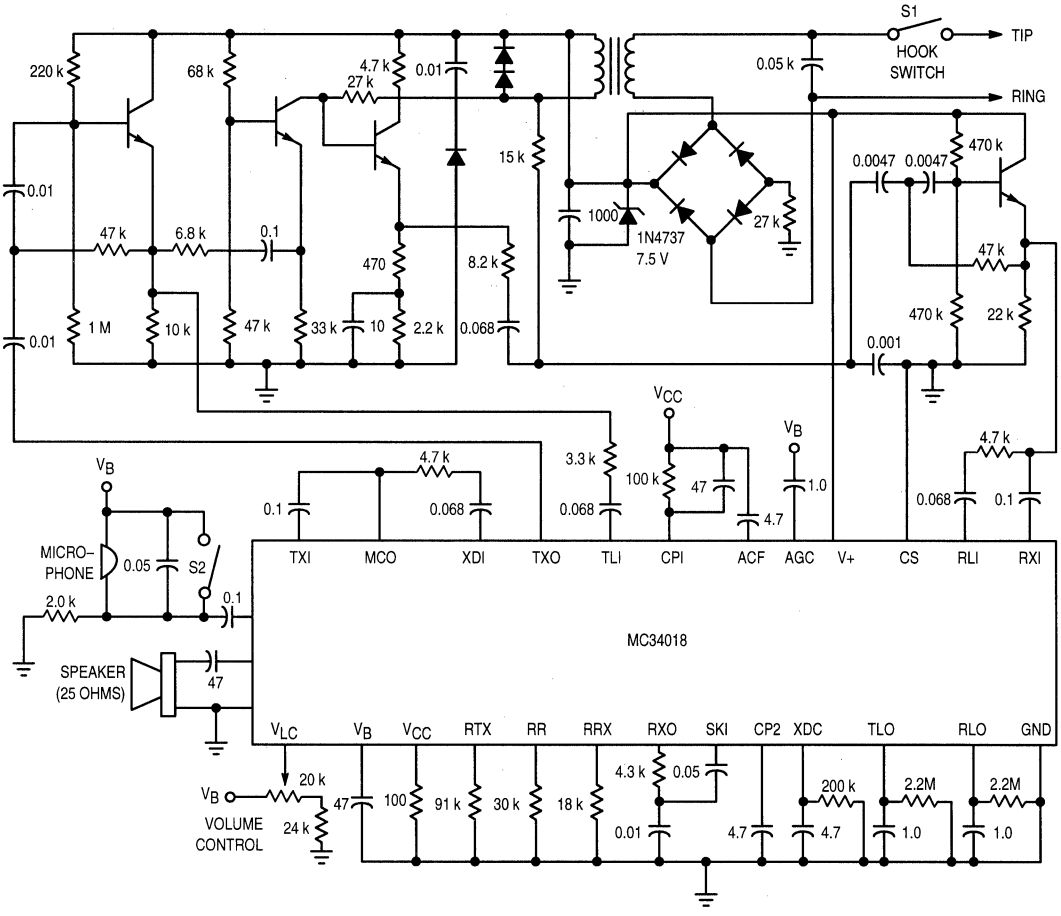


Figure 5. Basic Line Powered Speakerphone

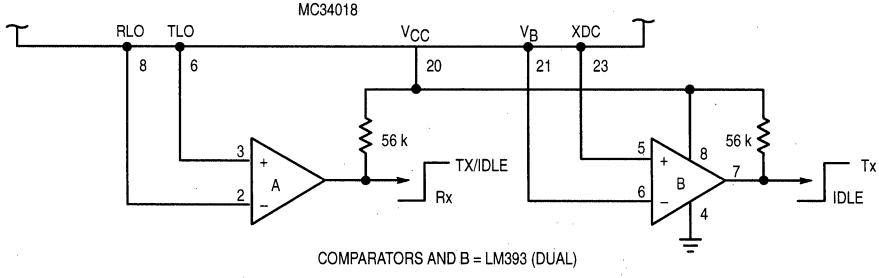


Figure 6. Digital Transmit/Idle/Receive Indication

MC34018

Specifications and Applications Information

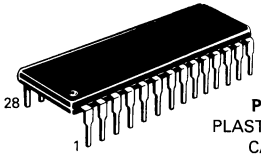
VOICE SWITCHED SPEAKERPHONE CIRCUIT

The MC34018 Speakerphone integrated circuit incorporates the necessary amplifiers, attenuators, and control functions to produce a high quality hands-free speakerphone system. Included are a microphone amplifier, a power audio amplifier for the speaker, transmit and receive attenuators, a monitoring system for background sound level, and an attenuation control system which responds to the relative transmit and receive levels as well as the background level. Also included are all necessary regulated voltages for both internal and external circuitry, allowing line-powered operation (no additional power supplies required). A Chip Select pin allows the chip to be powered down when not in use. A volume control function may be implemented with an external potentiometer. MC34018 applications include speakerphones for household and business use, intercom systems, automotive telephones, and others.

- All necessary level detection and attenuation controls for a hands-free telephone in a single integrated circuit
- Background noise level monitoring with long time constant
- Wide operating dynamic range through signal compression
- On-chip supply and reference voltage regulation
- Typical 100 mW output power (into 25 Ohms) with peak limiting to minimize distortion
- Chip Select pin for active/standby operation
- Linear Volume Control Function
- Standard 28-pin plastic DIP package (0.600 inch wide) and SOIC package

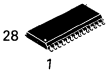
VOICE SWITCHED SPEAKERPHONE CIRCUIT

SILICON MONOLITHIC INTEGRATED CIRCUIT

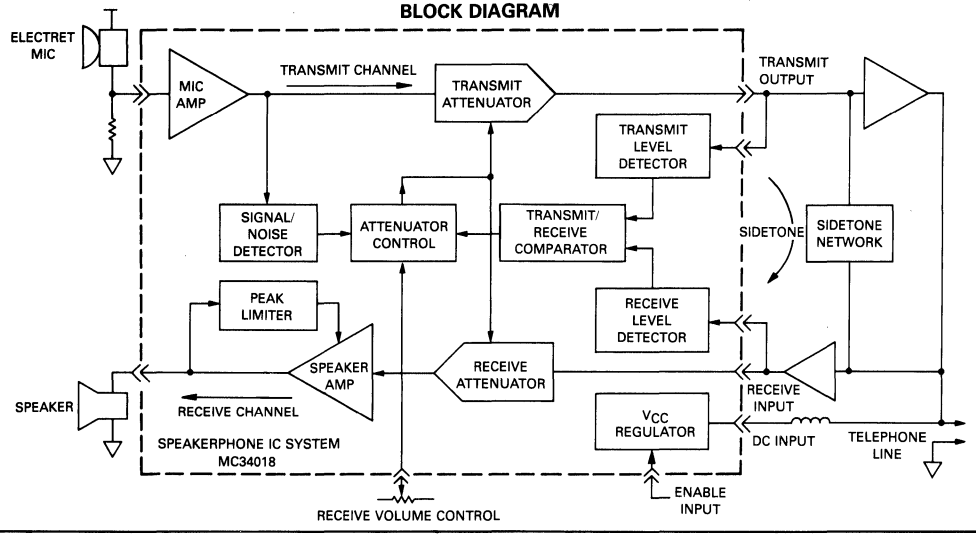


P SUFFIX
PLASTIC PACKAGE
CASE 710

DW SUFFIX
PLASTIC PACKAGE
CASE 751F
SO-28



BLOCK DIAGRAM



PIN DESCRIPTION

Pin	Name	Description
1	RR	A resistor to ground provides a reference current for the transmit and receive attenuators.
2	RTX	A resistor to ground determines the nominal gain of the transmit attenuator. The transmit channel gain is inversely proportional to the RTX resistance.
3	TXI	Input to the transmit attenuator. Input resistance is nominally 5.0 k ohms.
4	TXO	Output of the transmit attenuator. The TXO output signal drives the input of the transmit level detector, as well as the external circuit which drives the telephone line.
5	TLI	Input of the transmit level detector. An external resistor ac coupled to the TLI pin sets the detection level. Decreasing this resistor increases the sensitivity to transmit channel signals.
6	TLO	Output of the transmit level detector. The external resistor and capacitor set the time the comparator will hold the system in the transmit mode after speech ceases.
7	RLI	Input of the receive level detector. An external resistor ac coupled to the RLI pin sets the detection level. Decreasing this resistor increases the sensitivity to receive channel signals.
8	RLO	Output of the receive level detector. The external resistor and capacitor set the time the comparator will hold the system in the receive mode after the receive signal ceases.
9	MCI	Microphone amplifier input. Input impedance is nominally 10 k ohms and the dc bias voltage is approximately equal to VB.
10	MCO	Microphone amplifier output. The mic amp gain is internally set at 34 dB (50 V/V).
11	CP1	A parallel resistor and capacitor connected between this pin and V_{CC} holds a voltage corresponding to the background noise level. The transmit detector compares the CP1 voltage with the speech signal from CP2.
12	CP2	A capacitor at this pin peak detects the speech signals for comparison with the background noise level held at CP1.
13	XDI	Input to the transmit detector system. The microphone amplifier output is ac coupled to the XDI pin through an external resistor.
14	SKG	High current ground pin for the speaker amp output stage. The SKG voltage should be within 10 mV of the ground voltage at Pin 22.
15	SKO	Speaker amplifier output. The SKO pin will source and sink up to 100 mA when ac coupled to the speaker. The speaker amp gain is internally set at 34 dB (50 V/V).
16	V+	Input dc supply voltage. V+ can be powered from Tip and Ring if an ac decoupling inductor is used to prevent loading ac line signals. The required V+ voltage is 6.0 to 11 V (7.5 V nominal) at 7.0 mA.
17	AGC	A capacitor from this pin to VB stabilizes the speaker amp gain control loop, and additionally controls the attack and decay time of this circuit. The gain control loop limits the speaker amp input to prevent clipping at SKO. The internal resistance at the AGC pin is nominally 110 k ohms.
18	$\overline{CS}$	Digital chip select input. When at a Logic "0" (<0.7 V) the V_{CC} regulator is enabled. When at a Logic "1" (>1.6 V), the chip is in the standby mode drawing 0.5 mA. An open $\overline{CS}$ pin is a Logic "0". Input impedance is nominally 140 k ohms. The input voltage should not exceed 11 V.
19	SKI	Input to the speaker amplifier. Input impedance is nominally 20 k ohms.
20	V_{CC}	A 5.4 V regulated output which powers all circuits except the speaker amplifier output stage. V_{CC} can be used to power external circuitry such as a microprocessor (3.0 mA max). A filter capacitor is required. The MC34018 can be powered by a separate regulated supply by connecting V+ and V_{CC} to a voltage between 4.5 V and 6.5 V while maintaining $\overline{CS}$ at a Logic "1".
21	VB	An output voltage equal to approximately $V_{CC}/2$ which serves as an analog ground for the speakerphone system. Up to 1.5 mA of external load current may be sourced from VB. Output impedance is 250 ohms. A filter capacitor is required.
22	Gnd	Ground pin for the IC (except the speaker amplifier).
23	XDC	Transmit detector output. A resistor and capacitor at this pin hold the system in the transmit mode during pauses between words or phrases. When the XDC pin voltage decays to ground, the attenuators switch from the transmit mode to the idle mode. The internal resistor at XDC is nominally 2.6 k ohms (see Figure 1).
24	VLC	Volume control input. Connecting this pin to the slider of a variable resistor provides receive mode volume control. The VLC pin voltage should be less than or equal to VB.
25	ACF	Attenuator control filter. A capacitor connected to this pin reduces noise transients as the attenuator control switches levels of attenuation.
26	RXO	Output of the receive attenuator. Normally this pin is ac coupled to the input of the speaker amplifier.
27	RXI	Input of the receive attenuator. Input resistance is nominally 5.0 k ohms.
28	RRX	A resistor to ground determines the nominal gain of the receive attenuator. The receive channel gain is directly proportional to the RRX resistance.

Note: Pin numbers are identical for the DIP and SOIC packages.

ABSOLUTE MAXIMUM RATINGS

(Voltages referred to Pin 22) (T_A = 25°C)

Parameter	Value	Units
V+ Terminal Voltage (Pin 16)	+12, −1.0	V
$\overline{CS}$ (Pin 18)	+12, −1.0	V
Speaker Amp Ground (Pin 14)	+3.0, −1.0	V
VLC (Pin 24)	V_{CC}, −1.0	V
Storage Temperature	−65 to +150	°C

"Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed.
They are not meant to imply that the devices should be operated at these limits.
The "Electrical Characteristics" tables provide conditions for actual device operation.

2

RECOMMENDED OPERATING CONDITIONS

Parameter	Value	Units
V+ Terminal Voltage (Pin 16)	+6.0 to +11	V
$\overline{CS}$ (Pin 18)	0 to +11	V
I_{CC} (Pin 20)	0 to 3.0	mA
VLC (Pin 24)	0.55VB to VB	V
Receive Signal (Pin 27)	0 to 250	mV_{rms}
Microphone Signal (Pin 9)	0 to 5.0	mV_{rms}
Speaker Amp Ground (Pin 14)	−10 to +10	mVdc
Ambient Temperature	−20 to +60	°C

ELECTRICAL CHARACTERISTICS (Refer to Figure 1)

Parameter	Symbol	Pin	Min	Typ	Max	Units
SUPPLY VOLTAGES						
V+ Supply Current	I_{V+}	16				
V+ = 11 V, Pin 18 = 0.7 V			—	—	9.0	mA
V+ = 11 V, Pin 18 = 1.6 V			—	—	800	μA
V_{CC} Voltage (V+ = 7.5 V)	V_{CC}	20	4.9	5.4	5.9	Vdc
Line Regulation (6.5 V < V+ < 11 V)	$\Delta V_{CC\ LN}$		—	65	150	mV
Output Resistance (I_{CC} = 3.0 mA)	R_{OVCC}		—	6.0	20	ohms
Dropout Voltage (V+ = 5.0 V)	$V_{CC\ SAT}$		—	80	300	mV
VB Voltage (V+ = 7.5 V)	V_B	21	2.5	2.9	3.3	Vdc
Output Resistance (IB = 1.7 mA)	R_{OVB}		—	250	—	ohms
ATTENUATORS						
Receive Attenuator Gain (@ 1.0 kHz)		26,				
Rx Mode, Pin 24 = VB; Pin 27 = 250 mV_{rms}	G_{RX}	27	2.0	6.0	10	dB
Range (Rx to Tx Modes)	ΔG_{RX}		40	44	48	dB
Idle Mode, Pin 27 = 250 mV_{rms}	G_{RXI}		−20	−16	−12	dB
RXO Voltage (Rx Mode)	V_{RXO}		1.8	2.3	3.2	Vdc
Delta RXO Voltage (Switch from RX to TX Mode)	ΔV_{RXO}		—	—	100	mV
RXO Sink Current (Rx Mode)	I_{RXOL}		75	—	—	μA
RXO Source Current (Rx Mode)	I_{RXOH}		1.0	—	3.0	mA
RXI Input Resistance	R_{RXI}		3.5	5.0	8.0	kΩ
Volume Control Range (Rx Attenuator Gain, Rx Mode, 0.6 VB < Pin 24 < VB)	V_{CR}		24.5	—	32.5	dB

ELECTRICAL CHARACTERISTICS (continued)

Parameter	Symbol	Pin	Min	Typ	Max	Units
ATTENUATORS						
Transmit Attenuator Gain (@ 1.0 kHz)		3,				
Tx Mode, Pin 3 = 250 mV_{rms}	G_{TX}	4	4.0	6.0	8.0	dB
Range, (Tx to Rx Mode)	ΔG_{TX}		40	44	48	dB
Idle Mode, Pin 3 = 250 mV_{rms}	G_{TXI}		−16.5	−13	−8.5	dB
TXO Voltage (Tx Mode)	V_{TXO}		1.8	2.3	3.2	Vdc
Delta TXO Voltage (Switch from Tx to Rx Mode)	ΔV_{TXO}		—	—	100	mV
TXO Sink Current (Tx Mode)	I_{TXOL}		75	—	—	μA
TXO Source Current (Tx Mode)	I_{TXOH}		1.0	—	3.0	mA
TXI Input Resistance	R_{TXI}		3.5	5.0	8.0	kΩ
ACF Voltage (V_{CC} − Pin 25 Voltage)	ΔV_{ACF}	20,				
Rx Mode		25	—	150	—	mV
Rx Mode			—	6.0	—	mV
Idle Mode			—	75	—	mV
SPEAKER AMPLIFIER						
Speaker Amp Gain (Pin 19 = 20 mV_{rms})	G_{SPK}	15, 19	33	34	35	dB
SKI Input Resistance	R_{SKI}		15	22	37	kΩ
SKO Voltage (Pin 19 = Cap Couple to GND)	V_{SKO}		2.4	3.0	3.6	Vdc
SKO High Voltage (Pin 19 = 0.1 V, −100 mA load at Pin 15)	V_{SKOH}		5.5	—	—	Vdc
SKO Low Voltage (Pin 19 = −0.1 V, +100 mA load at Pin 15)	V_{SKOL}		—	—	600	mV
MICROPHONE AMPLIFIER						
Mike Amp Gain (Pin 9 = 10 mV_{rms}, 1.0 kHz)	G_{MCI}	9, 10	32.5	34	35	dB
Mike Amp Input Resistance	R_{MCI}		6.5	10	16	kΩ
LOGAMPS						
RLO Leakage Current (Pin 8 = VB + 1.0 V)	I_{LKRLO}	8	—	—	2.0	μA
TLO Leakage Current (Pin 6 = VB + 1.0 V)	I_{LKTLO}	6	—	—	2.0	μA
Transmit-Receive Switching Threshold (Ratio of ITLI to IRLI — at 20 μA — to switch Tx-Rx Comparator)	I_{TH}	5,7 25	0.8	—	1.2	
TRANSMIT DETECTOR						
XDC Voltage — Idle Mode	V_{XDC}	23	—	0	—	Vdc
Tx Mode			—	4.0	—	Vdc
CP2 Current Source	I_{CP2}	12	5.0	10	13	μA
DISTORTION						
Rx Mode — RXI to SKO (Pin 27 = 10 mV_{rms}, 1.0 kHz)	R_{XD}	27, 15	—	1.5	—	%
Tx Mode — MCI to TXO (Pin 9 = 5.0 mV_{rms}, 1.0 kHz)	T_{XD}	4,9	—	2.0	—	%

NOTES: 1. V+ = 7.5 V, $\overline{CS}$ = 0.7 V except where noted.
2. Rx Mode: Pin 7 = −100 μA, Pin 5 = +100 μA, except where noted.
Tx Mode: Pin 5, 13 = −100 μA, Pin 7 = +100 μA, Pin 11 = 0 volts.
Idle Mode: Pin 5 = −100 μA, Pin 7, 13 = +100 μA.
3. Current into a pin designated as +; current out of a pin designated as −
4. Voltages referred to Pin 22. T_A = +25°C.

TEMPERATURE CHARACTERISTICS (−20 to +60°C)

Parameter	Pin	Typical Change	Units
V+ Supply Current (V+ = 11 V, Pin 18 = 0.7 V)	16	−0.2	%/°C
V+ Supply Current (V+ = 11 V, Pin 18 = 1.6 V)	16	−0.4	%/°C
V_{CC} Voltage (V+ = 7.5 V)	20	+0.1	%/°C
Attenuator Gain (Max and Min Settings)		±0.003	dB/°C
Delta RXO, TXO Voltages	4,26	±0.24	%/°C
Speaker Amp Gain	15,19	±0.003	dB/°C
Microphone Amp Gain	9,10	±0.001	dB/°C
Microphone Amp Input Resistance	9	+0.4	%/°C
Tx-Rx Switching Threshold (@ 20 μA)	5,7	±0.2	nA/°C

DESIGN GUIDELINES (Refer to Figure 1)

ATTENUATORS

The transmit and receive attenuators are complementary in function, i.e., when one is at maximum gain the other is at maximum attenuation, and vice versa. They are never both on or both off. Their main purpose is to control the transmit and receive paths to provide the half-duplex operation required of a speakerphone. The attenuators are controlled solely by the voltage at the ACF pin (Pin 25). The ACF voltage is provided by the Attenuator Control block, which receives 3 inputs: a) the Rx-Tx Comparator, b) the Transmit Detector Comparator, and c) the Volume Control. The response of the attenuators is based on the difference of the ACF voltage from V_{CC}, and therefore a simple method for monitoring the circuit operation is to monitor this voltage difference (referred to as ΔVacf). If ΔVacf is approximately 6 millivolts the transmit attenuator is fully on and the receive attenuator is fully off (transmit mode). If ΔVacf is approximately 150 millivolts the circuit is in the receive mode. If ΔVacf is approximately 75 millivolts, the circuit is in the idle mode, and the two attenuators are at gain settings approximately half way (in dB) between their fully on and fully off positions.

The maximum gain and attenuation values are determined by the three resistors RR, RTX, and RRX (Refer to Figures 2, 3 and 4). RR affects both attenuators according to its value RELATIVE to RTX and RRX, which is why Figure 4 indicates the variations versus the ratio of the other resistors to RR. (GRX and GTX are the maximum gains, and ARX and ATX are the maximum attenuations). RTX affects the gain and attenuation of only the transmit attenuator according to the curves of Figure 2, while RRX affects only the receive attenuator according to Figure 3. As can be seen from the figures, the gain difference (from on to off) is a reasonably constant 45 dB until the upper gain limit is approached. A value of 30 k is recommended for RR as a starting point, and then RTX and RRX selected to suit the particular design goals.

The input impedance of the attenuators (at TXI and RXI) is typically 5.0 kΩ, and the maximum input signal which will not cause output distortion is 250 mV_{rms} (707 mVp-p). The 4300 ohm resistor and 0.01 μF capacitor at RXO (in Figure 1) filters out high frequency components in the receive path. This helps minimize high frequency acoustic feedback problems which may occur if the filter were not present. The filter's insertion loss is 1.5 dB at 1.0 kHz. The outputs of the attenuators are inverted from their inputs.

Referring to the attenuator control block, the ΔVacf voltage at its output is determined by three inputs. The relationship of the inputs and output is summarized in the following truth table:

Tx-Rx Comp	Transmit Det Comp	Volume Control	ΔVacf	Mode
Transmit	Transmit	No Effect	6.0 mV	Transmit
Transmit	Idle	No Effect	75 mV	Idle
Receive	Transmit	Affects ΔVacf	50–150 mV	Receive
Receive	Idle	Affects ΔVacf	50–150 mV	Receive

As can be seen from the truth table, the Tx-Rx comparator dominates. The Transmit Detector Comparator is effective only in the transmit mode, and the Volume Control is effective only in the receive mode.

The Tx-Rx comparator is in the transmit position when there is sufficient transmit signal present over and above any receive signal. The Transmit Detector Comparator then determines whether the transmit signal is a result of background noise (a relatively stable signal), or speech which consists of bursts. If the signal is due to background noise, the attenuators will be put into the idle mode (ΔVacf = 75 mV). If the signal consists of speech, the attenuators will be switched to the transmit mode (ΔVacf = 6.0 mV.) A further explanation of this function will be found in the section on the Transmit Detector Circuit.

The Tx-Rx comparator is in the receive position when there is sufficient receive signal to overcome the background noise **AND** any speech signals. The ΔVacf voltage will now be 150 mV **IF** the volume control is at the maximum position, i.e. VLC (Pin 24) = VB. IF VLC is less than VB, the gain of the receive attenuator, and the attenuation of the transmit attenuator, will vary in a complementary manner as shown in Figure 5. It can be seen that at the minimum recommended operating level (VLC = 0.55 VB) the gain of the transmit attenuator is actually greater than that of the receive attenuator. The effect of varying VLC is to vary ΔVacf, with a resulting variation in the gains of the attenuators. Figure 6 shows the gain variations with ΔVacf.

The capacitor at ACF (Pin 25) smooths the transition between operating modes. This keeps down any "clicks" in the speaker or transmit signal when the ACF voltage switches.

The gain separation of the two attenuators can be reduced from the typical 45 dB by adding a resistor between Pins 20 (V_{CC}) and 25 (ACF). The effect is a reduction of the maximum ΔVacf voltage in the receive mode, while not affecting ΔVacf in the transmit mode. As an example, adding a 12 kΩ resistor will reduce ΔVacf by approximately 15 mV (to 135 mV), decrease the gain of the receive attenuator by approximately 5.0 dB, and increase the gain of the transmit attenuator by a similar amount. If the circuit requires the receive attenuator gain to be +6.0 dB in the receive mode, RRX must be adjusted (to ≈ 27 k) to re-establish this value. This change will also increase the receive attenuator gain in the transmit mode by a similar amount. The resistor at TLI may also require changing to reset the sensitivity of the transmit level detector.

2

LOG AMPLIFIERS
(Transmit and Receive Level Detectors)

The log amps monitor the levels of the transmit and receive signals, so as to tell the Tx-Rx comparator which mode should be in effect. The input signals are applied to the amplifiers (at TLI and RLI) through AC coupling capacitors and current limiting resistors. The value of these components determines the sensitivity of the respective amplifiers, and has an effect on the switching times between transmit and receive modes. The feedback elements for the amplifiers are back-to-back diodes which provide a logarithmic gain curve, thus allowing operation over a wide range of signal levels. The outputs of the amplifiers are rectified, having a quick rise time and a slow decay time. The rise time is determined primarily by the external capacitor (at TLO or RLO) and an internal 500 ohm resistor, and is on the order of a fraction of a millisecond. The decay time is determined by the external resistor and capacitor, and is on the order of a fraction of a second. The switching time is not fixed, but depends on the relative values of the transmit and receive signals, as well as these external components. Figure 7 indicates the dc transfer characteristics of the log amps, and Figure 8 indicates the transfer characteristics with respect to an ac input signal. The dc level at TLI, RLI, TLO, and RLO is approximately VB.

The Tx-Rx comparator responds to the voltages at TLO and RLO, which in turn are functions of the currents sourced out of TLI and RLI, respectively. If an offset at the comparator input is desired, e.g., to prevent noise from switching the system, or to give preference to either the transmit or receive channel, this may be achieved by biasing the appropriate input (TLI or RLI). A resistor to ground will cause a DC current to flow out of that input, thus forcing the output of that amplifier to be biased slightly higher than normal. This amplifier then becomes the preferred one in the system operation. Resistor values from 500 k to 10 M ohms are recommended for this purpose.

SPEAKER AMPLIFIER

The speaker amplifier has a fixed gain of 34 dB (50 V/V), and is noninverting. The input impedance is nominally 22 kΩ as long as the output signal is below that required to activate the Peak Limiter. Figure 9 indicates the typical output swing available at SKO (Pin 15). Since the output current capability is 100 mA, the lower curve is limited to a 5.0 volt swing. The output impedance depends on the output signal level and is relatively low as long as the signal level is not near the maximum limits. At 3 volts p-p the output impedance is <0.5 ohms, and at 4.5 volts p-p it is <3 ohms. The output is short circuit protected at approximately 300 mA.

When the amplifier is overdriven, the peak limiter causes a portion of the input signal to be shunted to ground, in order to maintain a constant output level. The effect is that of a gain reduction caused by a reduction of the input impedance (at SKI) to a value not less than 2.0 kΩ.

The capacitor at Pin 17 (AGC) determines the response time of the peak limiter circuit. When a large input signal is applied to SKI, the voltage at AGC (Pin 17) will drop quickly as a current source is applied to the external capacitor. When the large input signal is reduced, the current source is turned off, and an internal 110 kΩ resistor discharges the capacitor so the voltage at AGC can return to its normal value (1.9 Vdc). The capacitor additionally stabilizes the peak limiting feedback loop.

If there is a need to mute the speaker amplifier without disabling the rest of the circuit, this may be accomplished by connecting a resistor from the AGC pin to ground. A 100 kΩ resistor will reduce the gain by 34 dB (0 dB from SKI to SKO), and a 10 k resistor will reduce the gain by almost 50 dB.

TRANSMIT DETECTOR CIRCUIT

The transmit detector circuit, also known as the background noise monitor, distinguishes speech (which consists of bursts) from the background noise (a relatively constant signal). It does this by storing a voltage level, representative of the average background noise, in the capacitor at CP1 (Pin 11). The resistor and capacitor at this pin have a time constant of approximately 5 seconds (in Figure 1). The voltage at Pin 11 is applied to the inverting input of the Transmit Detector Comparator. In the absence of speech signals, the noninverting input receives the same voltage level minus an offset of 36 mV. In this condition, the output of the comparator will be low, the output transistor turned off, and the voltage at XDC (Pin 23) will be at ground. If the Tx-Rx comparator is in the transmit position, the attenuators will be in the idle mode (ΔVacf = 75 mV). When speech is presented to the microphone, the signal burst appearing at XDI reaches the noninverting input of the transmit detector comparator before the voltage at the inverting input can change, causing the output to switch high, driving the voltage at XDC up to approximately 4 volts. This high level causes the attenuator control block to switch the attenuators from the idle mode to the transmit mode (assuming the Tx-Rx comparator is in

the transmit mode). As long as the speech continues to arrive, and is maintained at a level above the background, the voltage at XDC will be maintained at a high level, and the circuit will remain in the transmit mode. The time constant of the components at XDC will determine how much time the circuit requires to return to the idle mode after the cessation of microphone speech signals, such as occurs during the normal pauses in speech.

The series resistor and capacitor at XDI (Pin 13) determine the sensitivity of the transmit detector circuit. Figure 10 indicates the change in DC voltage levels at CP2 and CP1 in response to a steady state sine wave applied at the input of the 0.068 μF capacitor and 4700 ohm resistor (the voltage change at CP1 is 2.7 times greater than the change at CP2). Increasing the resistor, or lowering the capacitor, will reduce the response at these pins. The first amplifier (between XDI and CP2) is logarithmic in order that this circuit be able to handle a wide range of signal levels (or in other words, it responds equally well to people who talk quietly and to people who shout). Figure 7 indicates the dc transfer characteristics of the log amp.

Figure 11 indicates the response at Pins 11, 12, and 23 to a varying signal at the microphone. The series of events in Figure 11 is as follows:

1) CP2 (Pin 12) follows the peaks of the speech signals, and decays at a rate determined by the 10 μA current source and the capacitor at this pin.

2) CP1 (Pin 11) increases at a rate determined by the RC at this pin after CP2 has made a positive transition. It will follow the decay pattern of CP2.

3) The noninverting input of the Transmit Detector Comparator follows CP2, gained up by 2.7, and reduced by an offset of 36 mV. This voltage, compared to CP1, determines the output of the comparator.

4) XDC (Pin 23) will rise quickly to 4 Vdc in response to a positive transition at CP2, but will decay at a rate determined by the RC at this pin. When XDC is above 3.25 Vdc, the circuit will be in the transmit mode. As it decays towards ground, the attenuators are taken to the idle mode.

MICROPHONE AMPLIFIER

The microphone amplifier is noninverting, has an internal gain of 34 dB (50 V/V), and a nominal input impedance of 10 kΩ. The output impedance is typically <15 ohms. The maximum p-p voltage swing available at the output is approximately 2.0 volts less than V_{CC}, which is substantially more than what is required in most applications. The input at MCI (Pin 9) should be ac coupled to the microphone so as to not upset the bias voltage. Generally, microphone sensitivity may be adjusted by varying the 2 k microphone bias resistor, rather than by attempting to vary the gain of the amplifier.

POWER SUPPLY

The voltage supply for the MC34018 at V+ (Pin 16) should be in the range of 6.0 to 11 volts, although the circuit will operate down to 4.0 volts. The voltage can be supplied either from Tip and Ring, or from a separate supply. The required supply current, with no signal to the speaker, is shown in Figure 12. The upper curve indicates the normal operating current when $\overline{\text{Chip Select}}$ (Pin 18) is at a Logic "0". Figure 13 indicates the average dc current required when supplying various power levels to a 25 ohm speaker. Figure 13 also indicates the minimum supply voltage required to provide the indicated power levels. The peak in the power supply current at 5.0–5.4 volts occurs as the V_{CC} circuit comes into regulation.

It is imperative that the V+ supply (Pin 16) be a good ac ground for stability reasons. If this pin is not well filtered (by a 1000 μF capacitor AT THE IC), any variation at V+ caused by the required speaker current flowing through this pin can cause a low frequency oscillation. The result is usually that the circuit will cut the speaker signal on and off at the rate of a few hertz. Experiments have shown that only a few inches of wire between the supply and the IC can cause the problem if the filter capacitor is not physically adjacent to the IC. It is equally imperative that both ground pins (Pins 14 and 22) have a low loss connection to the power supply ground.

V_{CC}

V_{CC} (Pin 20) is a regulated output voltage of 5.4 volts, +/−0.5 V. Regulation will be maintained as long as V+ is (typically) 80 mV greater than the regulated value of V_{CC}. Up to 3 milliamps can be sourced from this supply for external use. The output impedance is <20 ohms.

The 47 μF capacitor indicated for connection to Pin 20 is essential for stability reasons. It must be located adjacent to the IC.

If the circuit is deselected (see section on Chip Select), the V_{CC} voltage will go to 0 volts.

If the MC34018 is to be powered from a regulated supply (not the Tip and Ring lines) of less than 6.5 volts, the configuration of Figure 14 may be used so as to ensure that V_{CC} is regulated. The regulated voltage is applied to both V+ and V_{CC}, with $\overline{\text{CS}}$ held at a Logic "1" so as to turn off the internal regulator (the Chip Select function is not available when the circuit is used in this manner). Figure 15 indicates the supply current used by this configuration, with no signal at the speaker. When a signal is sent to the speaker, the curves of Figure 13 apply.

VB

VB is a regulated output voltage with a nominal value of 2.9 volts, +/−0.4 volts. It is derived from V_{CC} and tracks it, holding a value of approximately 54% of V_{CC}. 1.5 milliamps can be sourced from this supply at a typical output impedance of 250 ohms.

The 47 μF capacitor indicated for connection to the VB pin is required for stability reasons, and must be adjacent to the IC.

If the circuit is deselected (see section on Chip Select), the VB voltage will go to 0 volts.

CHIP SELECT

The Chip Select pin (Pin 18) allows the chip to be powered down anytime its functions are not required. A Logic "1" level in the range of 1.6 V to 11 V deselects the chip, and the resulting supply current (at V+) is shown in Figure 12. The input resistance at Pin 18 is >75 kΩ. The V_{CC} and VB regulated voltages go to 0.0 when the chip is deselected. Leaving Pin 18 open is equivalent to a Logic "0" (chip enabled).

FIGURE 1 — TEST CIRCUIT

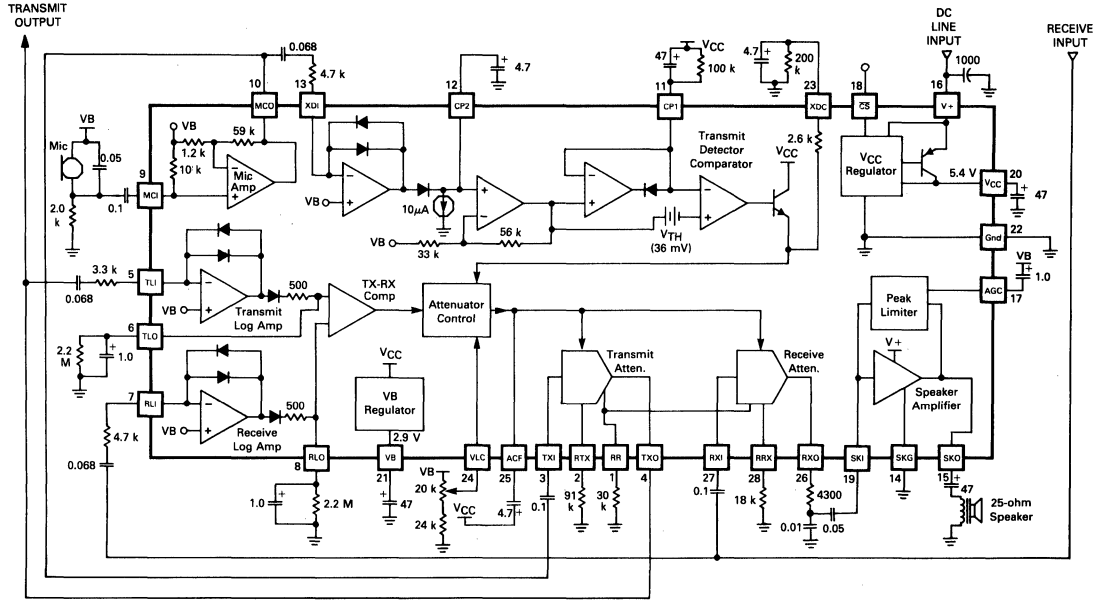


FIGURE 2 — TRANSMIT ATTENUATOR versus RTX

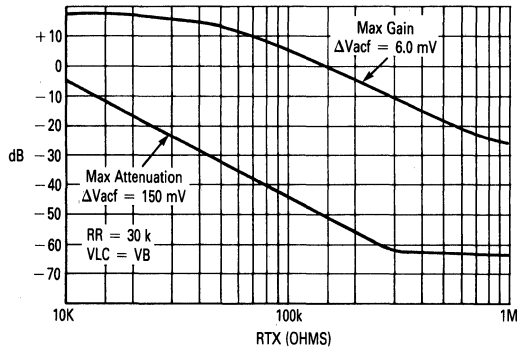


FIGURE 3 — RECEIVE ATTENUATOR versus RRX

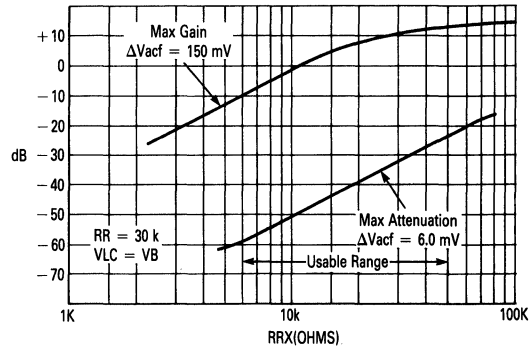


FIGURE 4 — GAIN AND ATTENUATION versus RESISTOR RATIOS

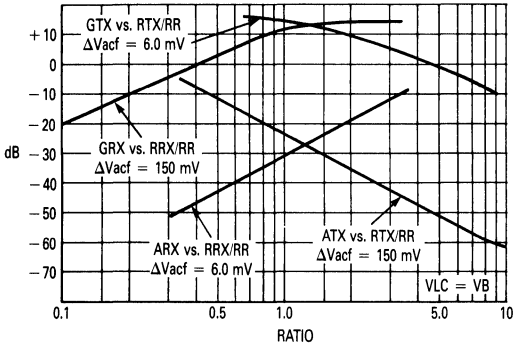


FIGURE 5 — ATTENUATOR GAIN versus VLC

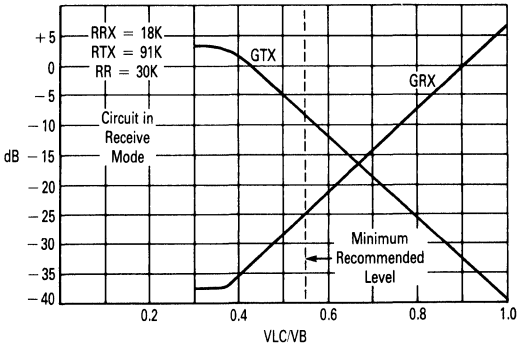


FIGURE 6 — ATTENUATOR GAIN versus ΔVacf

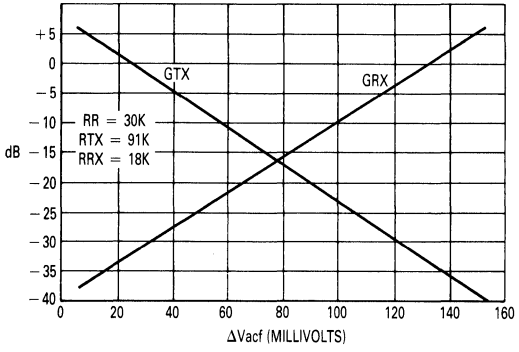


FIGURE 7 — LOG AMP TRANSFER CHARACTERISTICS

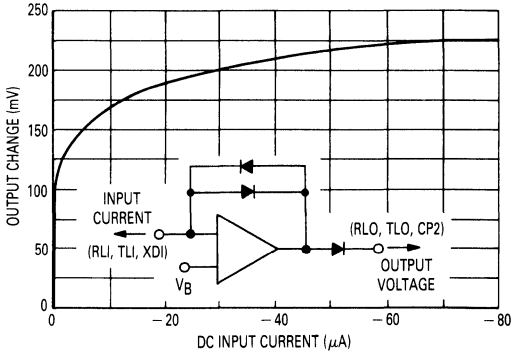


FIGURE 8 — LOG AMP TRANSFER CHARACTERISTICS

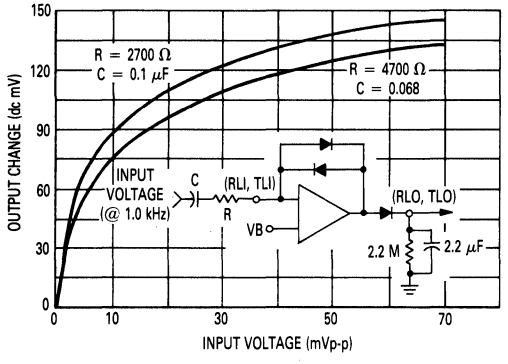
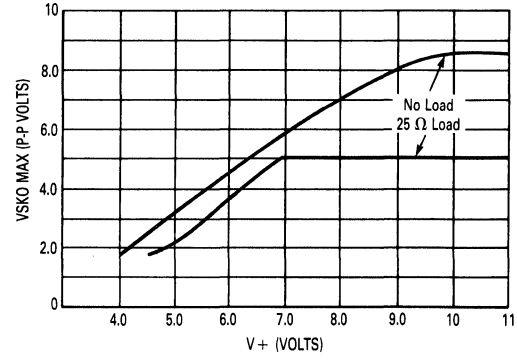


FIGURE 9 — SPEAKER AMP OUTPUT versus SUPPLY VOLTAGE



2

FIGURE 10 — RESPONSE AT CP2 AND CP1

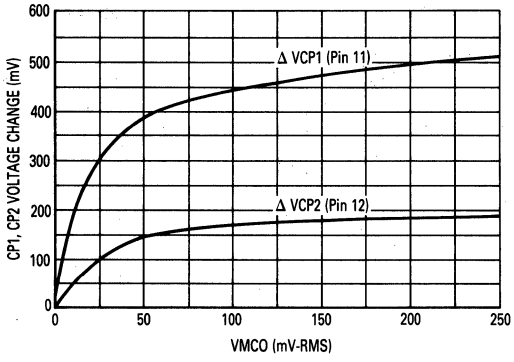


FIGURE 11 — TRANSMIT DETECTOR OPERATION

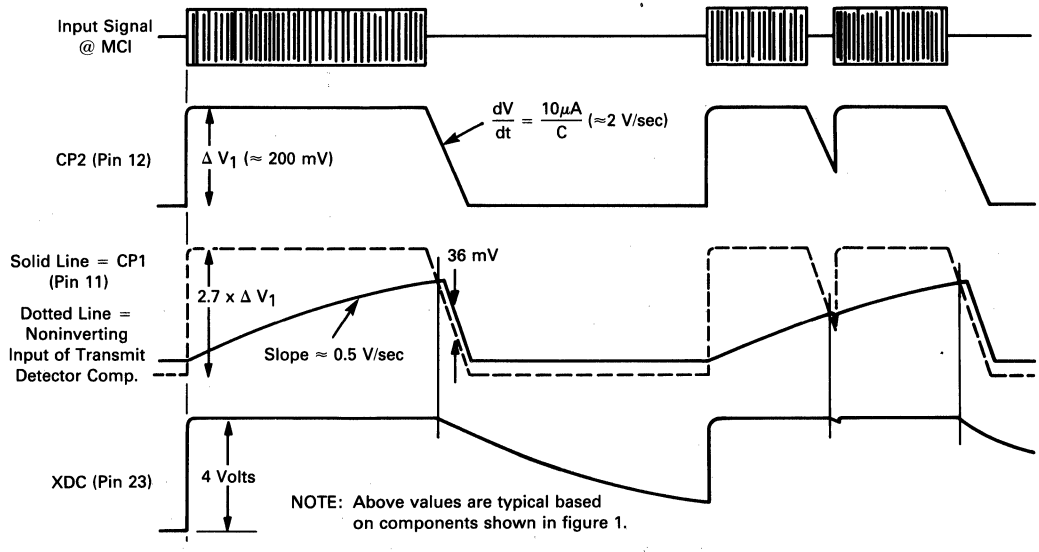


FIGURE 12 — SUPPLY CURRENT versus SUPPLY VOLTAGE

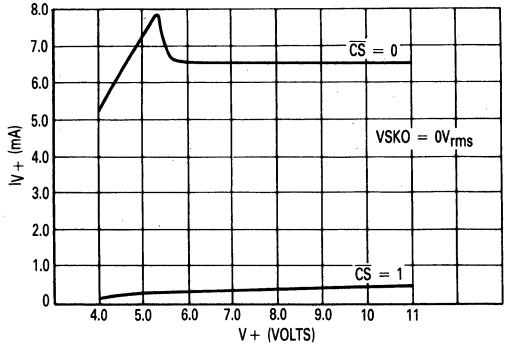


FIGURE 13 — SUPPLY CURRENT versus SUPPLY VOLTAGE versus SPEAKER POWER

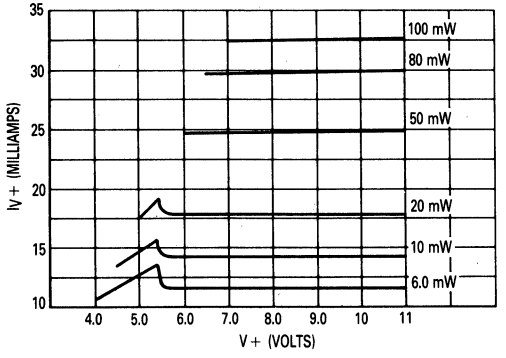


FIGURE 14 — ALTERNATE POWER SUPPLY CONFIGURATION

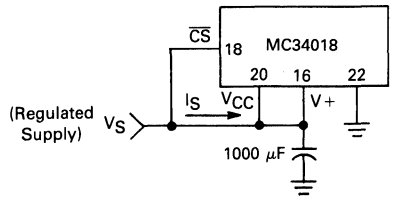
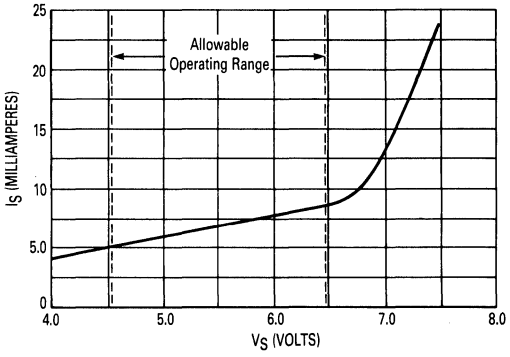


FIGURE 15 — SUPPLY CURRENT versus SUPPLY VOLTAGE (SEE FIGURE 14)



SWITCHING TIME

The switching times of the speakerphone circuit depend not only on the various external components, but also on the operating condition of the circuit at the time a change is to take effect. For example, the switching time from idle to transmit is generally quicker than the switching time from receive to transmit (or transmit to receive).

The components which most significantly affect the timing between the transmit and receive modes are those at Pins 5 (transmit turn-on), 6 (transmit turn-off), 7 (receive turn-on), and 8 (receive turn-off). These four timing functions are not independent, but interact since the Tx-Rx comparator operates on a RELATIVE Tx-Rx comparison, rather than on absolute values. The components at Pins 11, 12, 13, and 23 affect the timing from the transmit to the idle mode. Timing from the idle mode to transmit mode is relatively quick (due to the quick charging of the various capacitors), and is not greatly affected by the component values. Pins 5–8 do not affect the idle-to-transmit timing since the Tx-Rx comparator must already be in the transmit mode for this to occur.

The following table provides a summary of the effect on the switching time of the various components, including the volume control:

Additionally, the following should be noted:

1) The RCs at Pins 5 and 7 have a dual function in that they affect the sensitivity of the respective log amplifiers, or in other words, how loud the speech must be in order to gain control of the speakerphone circuit.

2) The RC at Pin 13 also has a dual function in that it determines the sensitivity of the transmit detector circuit.

3) The volume control affects the switching speed, and the relative response to transmit signals, in the following manner: When the circuit is in the receive mode, reducing the volume control setting increases the signal at TXO, and consequently the signal to the TLI pin. Therefore a given signal at TXI will switch the circuit into the transmit mode quicker at low volume settings.

The photographs of Figures 16 and 17 indicate experimentally obtained switching response times for the circuit of Figure 1. In Figure 16, the circuit is provided a continuous receive signal of 1.1 mVp-p at RXI (trace #3). A repetitive burst signal of 7.2 mVp-p, lasting 120

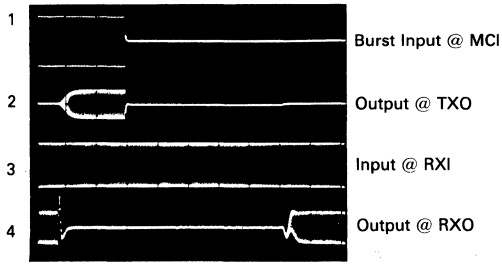
Components	Tx to Rx	Rx to Tx	Tx to Idle
RC @ Pin 5	Moderate	Significant	No effect
RC @ Pin 6	Significant	Moderate	No effect
RC @ Pin 7	Significant	Moderate	No effect
RC @ Pin 8	Moderate	Significant	No effect
RC @ Pin 11	No effect	Slight	Moderate
C @ Pin 12	No effect	Slight	Significant
RC @ Pin 13	No effect	Slight	Slight
RC @ Pin 23	No effect	Slight	Significant
V @ Pin 24	No effect	Moderate	No effect
C @ Pin 25	Moderate	Moderate	Slight

milliseconds, and repeated every 1 second, is applied to MCI (Trace #1). Trace #2 is the output at TXO, and is approximately 650 mVp-p at its maximum. Trace #4 is the output at RXO, and is approximately 2.2 mVp-p at its maximum. The time to switch from the receive mode to the transmit mode is approximately 40 ms, as indicated by the time required for TXO to turn on, and for RXO to turn off. After the signal at MCI is shut off, the switching time back to the receive mode is approximately 210 ms.

In Figure 17, a continuous signal of 7.6 mVp-p is applied to MCI (Trace #1), and a repetitive burst signal of 100 mVp-p is applied to RXI (Trace #3), lasting approximately 120 ms, and repeated every 1 second. Trace #2 is the output at TXO and is approximately 90 mVp-p at its maximum, and Trace #4 indicates the output at RXO, and is approximately 150 mVp-p at its maximum. In this sequence, the circuit switches between the idle and receive modes. The time required to switch from idle to receive is approximately 70 ms, as indicated by the first part of Traces 2 and 4. After the receive signal is shut off, the time to switch back to the idle mode is approximately 100 ms.

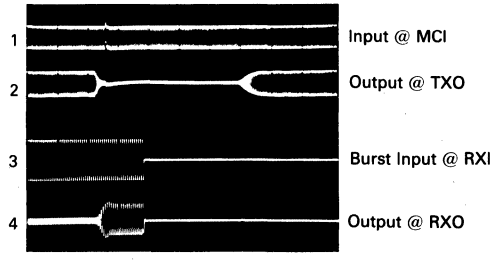
All of the above mentioned times will change significantly by varying the amplitude of the input signals, as well as by varying the external components.

FIGURE 16 — TRANSMIT-RECEIVE SWITCHING



Time Base = 40 ms/Div

FIGURE 17 — IDLE-RECEIVE SWITCHING



Time Base = 30 ms/Div

APPLICATIONS INFORMATION

The MC34018 Speakerphone IC is designed to provide the functions additionally required when a speakerphone is added to a standard telephone. The IC provides the necessary relative level detection and comparison of the speech signals provided by the talkers at the speakerphone (near end speaker) and at the distant telephone (far end speaker).

The MC34018 is designed for use with an electret type microphone, a 25 ohm speaker, and has an output power capability of (typically) 100 mW. All external components surrounding this device are passive, however, this IC does require additional circuitry to interface to the Tip and Ring telephone lines. Two suggested circuits are shown in this data sheet.

Figure 18 depicts a circuit using the MC34014 Speech Network (to provide the line interface), as well as the circuitry necessary to switch between the handset mode and the speakerphone mode. Switch HS (containing one normally open and one normally closed contact) is the hook switch actuated by the handset, shown in the on-hook position. When the handset is off-hook (HS1 open, HS2 closed), power is applied to the MC34014 speech network, and consequently the handset, and the $\overline{CS}$ pin of the MC34018 is held high so as to disable it. Upon closing the two poles of switch SS, **AND** placing switch HS in the on-hook position, power is then applied to both the MC34014 and the MC34018, and $\overline{CS}$ is held low, enabling the speakerphone function. Anytime the handset is removed from switch HS, the circuit reverts to the handset mode. The diode circuitry sets the operational mode of the MC34014 so as to optimize the speakerphone operation (see the MC34014 data sheet for further details). The tone dialer interface is meant for connection to a DTMF dialer with an active low MUTE signal. The V_{DD} supply from the MC34014 is a nominal 3.3 volts. The MC34017 and piezo sounder provide the ringing function.

Figure 19 depicts a configuration which does not include a handset, dialer, or ringer. The only controls are S1 (to make the connection to the line), S2 (a "privacy" switch), and the volume control. It is meant to be used in parallel with a normal telephone which has the dialing and ringing functions.

Figure 20 depicts a means of providing logic level signals that indicate which mode of operation the MC34018 is in. Comparator A indicates whether the circuit is in the receive or transmit/idle mode, and comparator B indicates (when in the transmit/idle mode) whether the circuit is in the transmit or idle mode. The LM393 dual comparator was chosen because of its low current requirement (<1.0 mA), low voltage requirement (as low as 2.0 volts), and low cost.

FIGURE 18 — SWITCHABLE HANDSET/HANDSFREE SYSTEM

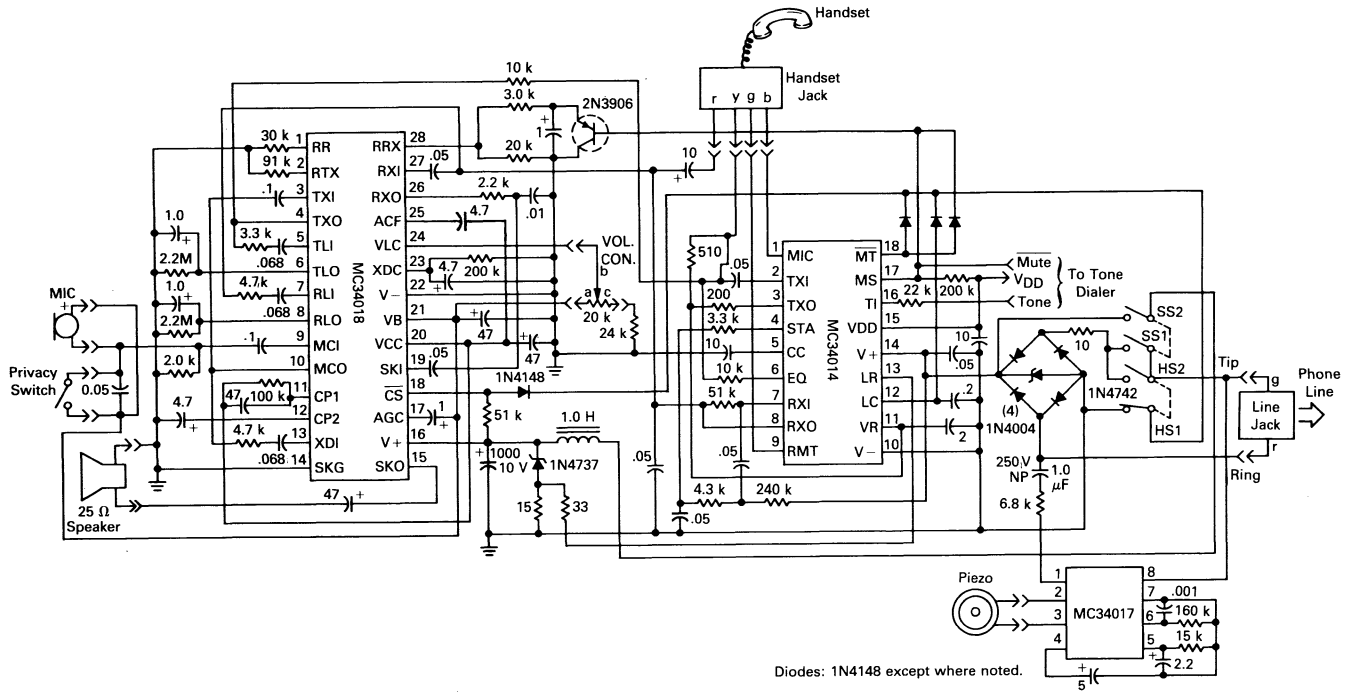
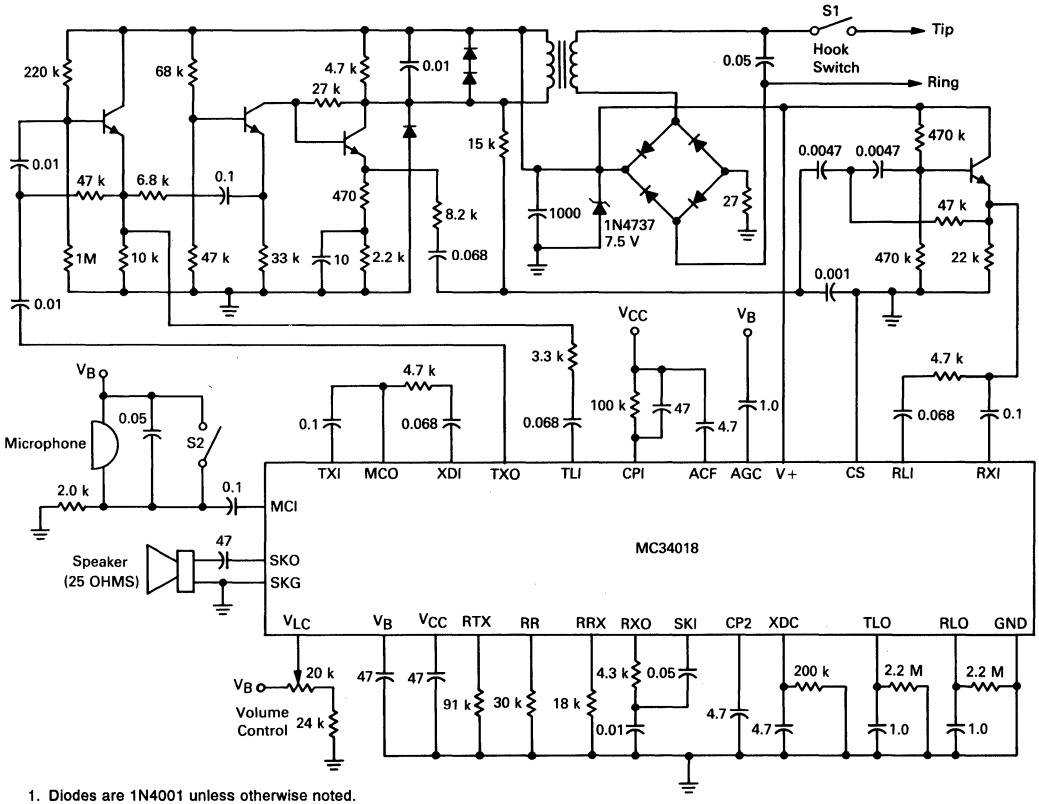
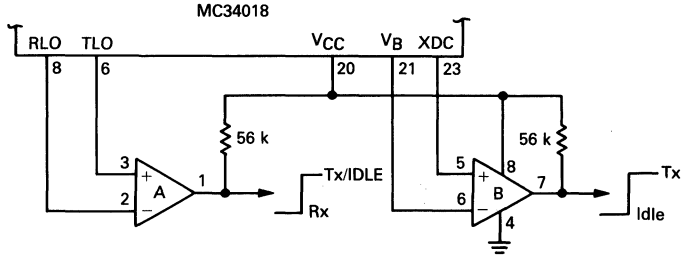


FIGURE 19 — BASIC LINE POWERED SPEAKERPHONE



1. Diodes are 1N4001 unless otherwise noted.
2. 4 Transistors are 2N3904.
3. Recommended Transformer: Microtran T5115.

FIGURE 20 — DIGITAL TRANSMIT/IDLE/RECEIVE INDICATION



Comparators A & B = LM393 (Dual)

MC34114

Specifications and Applications Information

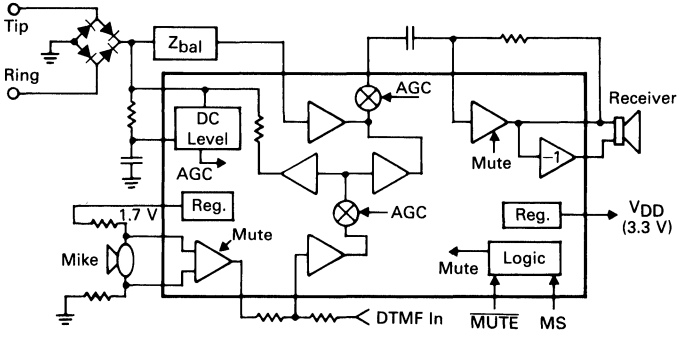
TELEPHONE SPEECH NETWORK WITH DIALER INTERFACE

The MC34114 is a monolithic integrated telephone speech network designed to replace the bulky magnetic hybrid circuit of a telephone set. The MC34114 incorporates the necessary functions of transmit amplification, receive amplification, and sidetone control, each with externally adjustable gain. Loop length equalization varies the gains based on loop current. The microphone amplifier has a balanced, differential input stage designed to reduce RFI problems. A $\overline{\text{MUTE}}$ input mutes the microphone and receive amplifiers during dialing. A regulated output voltage is provided for biasing of the microphone, and a separate output voltage powers an external dialer, microprocessor, or other circuitry. The MC34114 is designed to operate at a minimum of 1.2 volts, making party line operation possible.

A circuit using the MC34114 can be made to comply with Bell Telephone, British Telecom (BT), and NTT (Nippon Telegraph & Telephone) standards. It is available in a standard 18-pin DIP, and a 20-pin SOIC (surface mount) package.

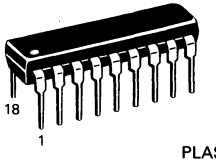
- Operation Down to 1.2 Volts
- Externally Adjustable Transmit, Receive, and Sidetone Gains
- Differential Microphone Amplifier Input Minimizes RFI Susceptibility
- Transmit, Receive, and Sidetone Equalization on Both Voice and DTMF Signals
- Regulated 1.7 Volts Output for Biasing Microphone
- Regulated 3.3 Volts Output for Powering External Dialer or MPU
- Microphone and Receive Amplifiers Muted During Dialing
- Differential Receive Amplifier Output Eliminates Coupling Capacitor
- Operates with Receiver Impedances of 50 Ohms and Higher
- Complies with NTT, Bell Telephone and BT Standards

SIMPLIFIED BLOCK DIAGRAM

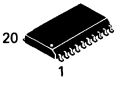


TELEPHONE SPEECH NETWORK WITH DIALER INTERFACE

SILICON MONOLITHIC INTEGRATED CIRCUIT

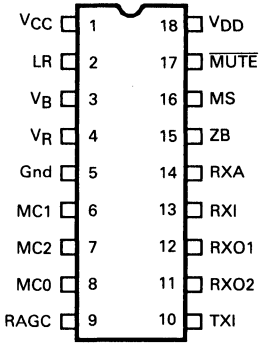


P SUFFIX
PLASTIC PACKAGE
CASE 707



DW SUFFIX
PLASTIC PACKAGE
CASE 751D

PIN CONNECTIONS
(Top View)
(DIP Package)



ORDERING INFORMATION

Package	Part No.
18-Pin Plastic DIP	MC34114P
20-Pin Surface Mount	MC34114DW

ABSOLUTE MAXIMUM RATINGS

Parameter	Value	Units
V_{CC} Supply Voltage	−1.0, +12	Vdc
Voltage at V_{DD} (Externally Applied, V_{CC} = 0)	−1.0, +6.0	Vdc
Voltage at $\overline{MUTE}$, MS (V_{CC} > 1.5 Volts)	−1.0, V_{DD} + 0.5	Vdc
Voltage at $\overline{MUTE}$, MS (V_{CC} = 0)	−1.0, +6.0	Vdc
Voltage at RAGC (0 < V_{CC} < 12 Volts)	−1.0, +6.0	Vdc
Current through V_{CC}, LR	130	mA
Current into Z_B (Pin 15)	3.0	mA
Storage Temperature	−65, +150	°C

"Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices can be operated at these limits. The "Recommended Operating Conditions" provides conditions for actual device operation.

RECOMMENDED OPERATING LIMITS

Parameter	Min	Typ	Max	Units
V_{CC} Voltage (Speech, Pulse Mode) (Tone Dialing Mode)	+1.2 +3.3	— —	+10.5 +10.5	Vdc
Loop Current (into V_{CC}) (Speech, Pulse Mode) (Tone Dialing Mode)	4.0 15	— —	120 120	mA
Receiver Impedance	50	—	—	Ω
Voltage at $\overline{MUTE}$, MS (V_{CC} > 1.5 Volts)	0	—	V_{DD}	Vdc
R1 (Resistor from V_{CC} to V_B)	100	—	1800	Ω
Ambient Temperature	−20	—	+70	°C

All limits are not necessarily functional concurrently.

ELECTRICAL CHARACTERISTICS (T_A = 25°C, See Figure 1)

Parameter	Symbol	Min	Typ	Max	Units
SUPPLY CURRENT					
Supply Current into V_{CC} (Pin 2 open, R12 = 25 k, V_{DD} unloaded)					mA
Speech Mode (Figure 2) V_{CC} = 1.2 Volts	I_{ccsp}	4.0	5.0	5.5	
V_{CC} = 3.5 Volts		9.0	11	12	
V_{CC} = 8.0 Volts		10	12	14	
V_{CC} = 10.5 Volts		—	13	—	
Tone Mode (Figure 4) V_{CC} = 3.3 Volts	I_{cct}	—	14	—	
V_{CC} = 8.0 Volts		—	16	—	
V_{CC} = 10 Volts		—	18	—	
VOLTAGE REGULATORS					
V_R Voltage (I_R = 65 μA, V_{CC} = 2.5 V, Figure 5)	V_R	1.6	1.7	1.85	Vdc
Load Regulation (0 < I_R < 300 μA, V_{CC} = 2.5 V)		—	0.2	0.5	Vdc
Line Regulation (I_R = 65 μA, 2.5 < V_{CC} < 10.5 V)		−70	±20	+70	mVdc
V_{DD} Voltage (V_{CC} ≥ 3.8 V, I_{DD} = 0, Figure 6)	V_{DD}	3.1	3.3	3.7	Vdc
Line Regulation (I_{DD} = 0, 5.0 V < V_{CC} < 10.5 V)		−70	±30	+70	mVdc
Maximum Output Current (V_{CC} = 3.8 V, V_{DD} ≥ 3.0 V)	I_{DDMAX}				mA
Speech Mode		0.8	1.0	—	
Pulse, Tone Mode		2.2	2.5	—	
Input Leakage Current (V_{CC} = 0, 3.3 Volts applied to V_{DD})	I_{lkg}				μA
$\overline{Mute}$ open or at V_{DD}		—	0.02	0.5	
$\overline{Mute}$ = 0 Volts		—	180	—	

ELECTRICAL CHARACTERISTICS — continued (T_A = 25°C, See Figure 1)

Parameter	Symbol	Min	Typ	Max	Units
MICROPHONE AMPLIFIER					
Gain ($\overline{Mute}$ = V_{DD})	G_{MIC}	28	30	32	dB
Input Common Mode Rejection Ratio (1.0 kHz)	CMRR	20	26	—	dB
Input Impedance (Each Input)	R_{INMIC}	14	20	27	kΩ
MCO DC Bias Voltage (V_{CC} > 3.4 V, $\overline{Mute}$ = Hi) (V_{CC} = 1.2 V, $\overline{Mute}$ = Hi) ($\overline{Mute}$ = 0 V)	V_{MCODC}	0.85 0.6 —	1.1 0.71 0.08	1.25 0.93 —	Vdc
MCO Max Voltage Swing (THD = 5%, V_{CC} > 2.7 V) (THD = 5%, V_{CC} = 1.2 V)	V_{MCOAC}	— —	2.0 500	— —	Vp-p mVp-p
MCO Output Impedance	Z_{MCO}	—	270	—	Ω
MCO Output Current Capability (THD = 5%)	I_{MCO}	—	160	—	μA
Gain Reduction when Muted ($\overline{Mute}$ = 0 Volts, f = 1.0 kHz)	G_{MUT}	55	70	—	dB
RECEIVE AMPLIFIER					
RXI Bias Current (Mute = Hi)	I_{IBR}	—	50	—	nA
RXO1, RXO2 Bias Voltage (V_{CC} = 1.2 V) (V_{CC} > 3.0. V)	R_{XDC}	580 585	630 650	695 720	mVdc
RXO1–RXO2 Offset Voltage (V_{CC} > 3.0 V)	R_{XVOS}	−35	0	+35	mVdc
RXO1–RXO2 Max Voltage Swing (Figure 9) (THD = 5%, Receiver = ∞) (THD = 5%, Receiver = 150 Ω)	V_{RXAC}	 — —	 2.2 800	 — —	 Vp-p mVp-p
Internal Feedback Resistor (for muting)	R_{FINT}	—	1.0	—	kΩ
RXO1 & RXO2 Source Current	I_{RX}	2.6	3.2	3.5	mA
INTERNAL CURRENT AMPLIFIERS					
TXI Input Impedance	R_{TXI}	0.85	1.0	1.15	kΩ
ZB Input Impedance	R_{ZB}	—	500	—	Ω
RXA Output Impedance	R_{RXA}	—	10	—	kΩ
AC Current Gain TXI to V_{CC} (V_{RAGC} = 0 V) TXI to V_{CC} (V_{RAGC} = 1.3 V) ZB to RXA (V_{RAGC} = 0 V, RXA = AC Gnd) ZB to RXA (V_{RAGC} = 1.3 V, RXA = AC Gnd) TXI to RXA (V_{RAGC} = 0 V, RXA = AC Gnd) TXI to RXA (V_{RAGC} = 1.3 V, RXA = AC Gnd)	 G_{TX} G_{ZB} G_{STA} 	 — — — — — —	 100 50 0.5 0.25 1.22 0.61	 — — — — — —	A/A
DC INTERFACE					
LR Level Shift (V_{CC}–V_{LR}) (I_{LOOP} = 20 mA, $\overline{Mute}$ = V_{DD}) (I_{LOOP} = 80 mA, $\overline{Mute}$ = V_{DD}) (I_{LOOP} = 20 mA, $\overline{Mute}$ & MS = 0 V) (I_{LOOP} = 80 mA, $\overline{Mute}$ & MS = 0 V)	 ΔV_{LRS} ΔV_{LRT} 	 — — — —	 2.8 3.5 3.8 5.0	 — — — —	Vdc
V_{CC} Boost (I_{LOOP} = 20 mA, $\overline{Mute}$ & MS switched from Hi to Lo, R1 = 620 Ω)	ΔV_{LRB}	0.7	1.0	1.2	Vdc
RAGC Current (V_{RAGC} = 0 V) (V_{RAGC} = 1.0 V)	I_{RAGC}	— —	−40 −12	— —	μA

ELECTRICAL CHARACTERISTICS — continued (T_A = 25°C, See Figure 1)

Parameter	Symbol	Min	Typ	Max	Units
LOGIC INPUTS					
$\overline{\text{MUTE}}$ Input Impedance (V_{CC} > 1.2 V)	R_{MUT}	—	60	—	kΩ
(V_{CC} = 0 V, 0 < $\overline{\text{Mute}}$ < 6.0 V)		—	>60	—	MΩ
Input Low Voltage	V_{ILMT}	0	—	1.0	Vdc
Input High Voltage	V_{IHMT}	V_{DD} − 0.5	—	V_{DD}	Vdc
Holdover (Delay for Receive amplifier to return to full gain after Pin 17 switches from 0 to V_{DD})	T_{MUT}	8.0	11	25	mSec
MS Input Impedance (V_{CC} > 1.2 V)	R_{MS}	—	60	—	kΩ
(V_{CC} = 0 V, $\overline{\text{Mute}}$ = open or V_{DD})		—	>50	—	MΩ
(V_{CC} = 0, $\overline{\text{Mute}}$ = 0)		—	4.0	—	kΩ
Input Low Voltage	V_{ILMS}	0	—	0.3	Vdc
Input High Voltage	V_{IHMS}	2.0	—	V_{DD}	Vdc

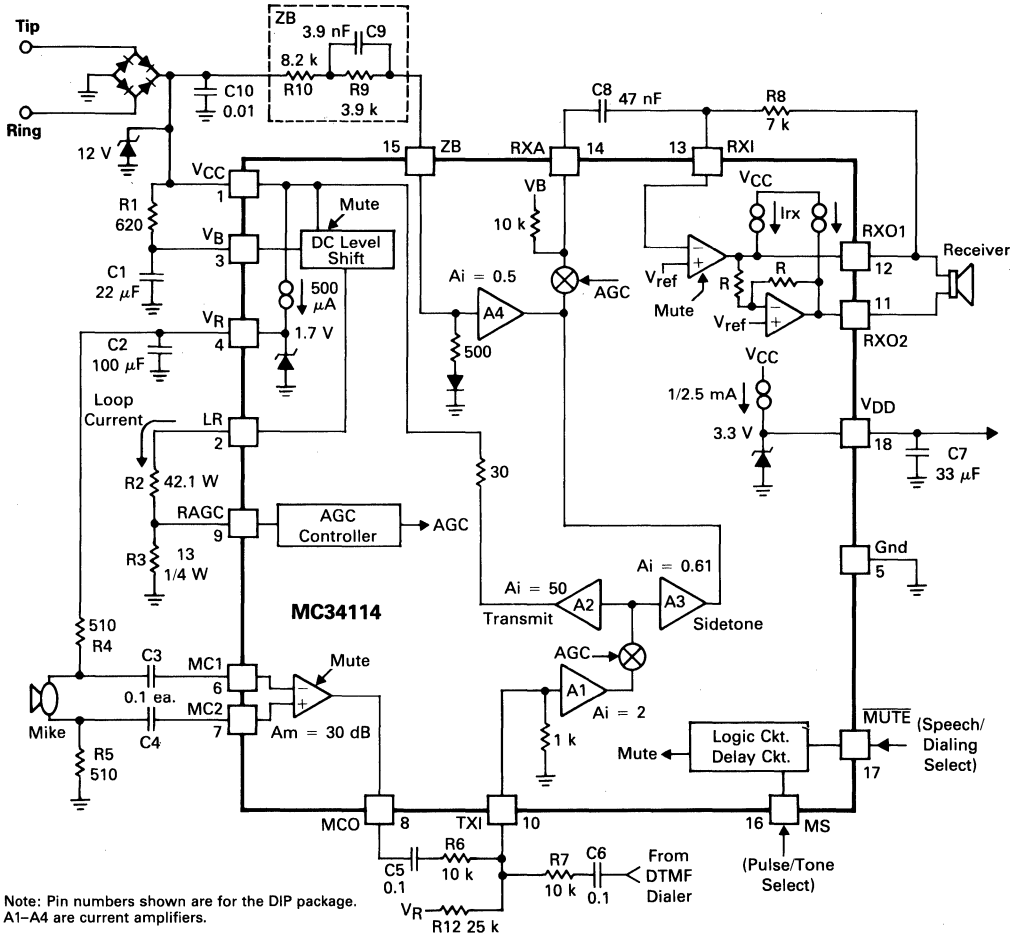
SYSTEM SPECIFICATIONS (f = 1.0 kHz unless noted, T_A = 25°C, Refer to Figure 1)

Parameter	Symbol	Min	Typ	Max	Units
LINE INTERFACE					
V_{CC} DC Voltage (Pin 1)	V_{CC}				Vdc
Bell Telephone Standard and NTT Specs. (R2 = 43 Ω, R3 = 13 Ω)					
Speech Mode I_{LOOP} = 10 mA			1.7	2.0	2.3	
I_{LOOP} = 20 mA			3.0	3.4	3.7	
I_{LOOP} = 30 mA			3.5	4.1	4.5	
I_{LOOP} = 120 mA			8.5	9.9	10.5	
Tone Mode I_{LOOP} = 20 mA			3.9	4.1	4.3	
I_{LOOP} = 30 mA			4.5	5.1	5.5	
British Telecom Standard (R2 = 43 Ω + 2.5 V Zener, R3 = 13 Ω)					
Speech Mode I_{LOOP} = 10 mA			—	4.3	—	
I_{LOOP} = 20 mA			—	5.9	—	
I_{LOOP} = 30 mA			—	6.9	—	
I_{LOOP} = 70 mA			—	10	—	
AC Terminating Impedance (I_{LOOP} = 20 mA, Figure 11)	Z_{AC}	500	600	700	Ω
RECEIVE PATH					
Gain (V_{CC} to RXO1–RXO2, Figures 14, 15)	G_{RX}				dB
I_{LOOP} = 20 mA			−7.2	−6.1	−5.0	
I_{LOOP} = 100 mA			−13.5	−11	−9.5	
ΔGain (G_{RX} @ 100 mA versus 20 mA)	ΔG_{RX}	−7.5	−6.0	−4.5	dB
Muted Gain ($\overline{\text{Mute}}$ = Logic 0, I_{LOOP} = 20 mA)	G_{RXM}	—	−22	−20	dB
Distortion (at RXO1–RXO2, V_{CC} = 250 mVrms)	THD_R				%
f = 300 Hz		—	0.3	—	
f = 1.0 kHz		—	0.2	2.0	
f = 3.4 kHz		—	0.02	—	
Output Noise Across RXO1–RXO2 (@ 1.0 kHz)	N_{RXO}	—	4.0	—	μVrms
TRANSMIT PATH					
Gain (MC1–MC2 to V_{CC}, Figures 12, 13)	G_{TX}				dB
I_{LOOP} = 20 mA		36	38.5	40.5	
I_{LOOP} = 100 mA		29	32.5	35.5	
ΔGain (G_{TX} @ 100 mA versus 20 mA)	ΔG_{TX}	−7.5	−6.0	−4.5	dB
Max V_{CC} Voltage Swing (THD = 5%, Figure 8)	VTX_{MAX}				Vp-p
I_{LOOP} = 20 mA		—	3.0	—	
I_{LOOP} = 100 mA		—	2.3	—	
Gain Reduction when muted (MC1–MC2 to V_{CC}, $\overline{\text{Mute}}$ = 0 V)	G_{TXM}	—	68	—	dB
Distortion (0 dBm @ V_{CC})	THD_T				%
f = 300 Hz		—	0.5	—	
f = 1.0 kHz		—	1.5	3.0	
f = 3.4 kHz		—	1.3	—	
Output Noise at V_{CC} (@ 1.0 kHz)	N_{TXO}	—	17	—	μVrms
SIDETONE					
Sidetone Gain (Gain from V_{CC} to RXO1–RXO2 with signal applied to MC1/MC2, I_{LOOP} = 20 mA)	G_{ST}	—	−27	−22	dB

PIN DESCRIPTIONS

Symbol	Pin Number (SOIC)	Pin Number (DIP)	Description
V_{CC}	1	1	Power supply pin for the IC. Supply voltage is derived from loop current. Transmit amp output operates on this pin.
LR	2	2	Resistors R2 + R3 at this pin set the DC characteristics of the circuit. The majority of the loop current flows through these resistors. Other components may be used to produce required DC characteristics for individual regulatory agencies.
V_B	3	3	A resistor or appropriate network (R1) connected from this pin to V_{CC} sets the AC terminating impedance (return loss spec).
V_R	4	4	A 1.7 volt regulated output which can be used to bias the microphone. Additionally, this voltage powers a portion of the internal circuitry. Can nominally supply 300–500 μA.
GND	5	5	Ground pin for the entire IC. Normally this is not connected to, nor to be confused with earth ground.
MC1	6	6	Inverting differential input to the microphone amplifier. Input impedance is typically 20 kΩ.
MC2	7	7	Non-inverting differential input to the microphone amplifier. Input impedance is typically 20 kΩ.
MC0	8	8	Microphone amplifier output. Amplifier's gain is fixed at 30 dB.
RAGC	10	9	Loop current sensing input. The voltage at this pin, determined by the loop current and R3, operates the loop length equalization circuit.
TXI	11	10	Input to the transmit amplifier from the microphone amplifier, DTMF source, and other sources. Input impedance $\approx$ 1.0 kΩ.
RXO2	12	11	Receive amplifier non-inverting differential output. Current capability to the receiver is typically set at $\pm$3.0 mA peak.
RXO1	14	12	Receive amplifier inverting differential output. Current capability to the receiver is typically $\pm$3.0 mA peak. Gain is set by R8.
RXI	15	13	Summing input to the receive amplifier. This pin is an AC virtual ground.
RXA	16	14	Summed outputs of the receive current amplifier, sidetone amplifier, and an AGC point. Normally connected to the receive amplifier input (RXI) through a coupling capacitor.
ZB	17	15	Input to the receive current amplifier. A balance network (ZB) is connected between this pin and V_{CC}. The network affects the receive level and sidetone performance. Input impedance is $\approx$500 Ω in series with a diode.
MS	18	16	Mode Select Input. A logic "1" sets the IC for pulse dialing. A logic "0" sets the IC for tone (DTMF) dialing. Effective only if $\overline{\text{MUTE}}$ is at a logic "0". Input impedance is $\approx$ 60 kΩ.
$\overline{\text{MUTE}}$	19	17	$\overline{\text{Mute}}$ input. A logic "1" sets normal speech mode. A logic "0" mutes the microphone and receive amplifiers and allows MS to be functional. Input impedance is $\approx$60 kΩ referenced to V_{DD}. An internal fixed delay of 11 mSec minimizes clicks in the receiver when returning to the speech mode.
V_{DD}	20	18	A regulated 3.3 volt output for an external dialer. Output source current capability is 1.0 mA in speech mode, 2.5 mA in tone dialing mode.

FIGURE 1 — BLOCK DIAGRAM AND TEST CIRCUIT



Note: Pin numbers shown are for the DIP package.
A1–A4 are current amplifiers.

FIGURE 2 — I_{CC} versus V_{CC} (SPEECH MODE)

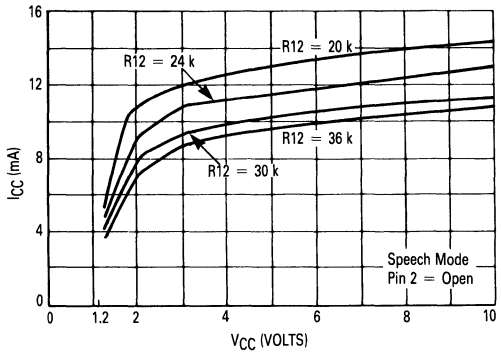


FIGURE 3 — I_{CC} versus V_{CC} (PULSE DIALING MODE)

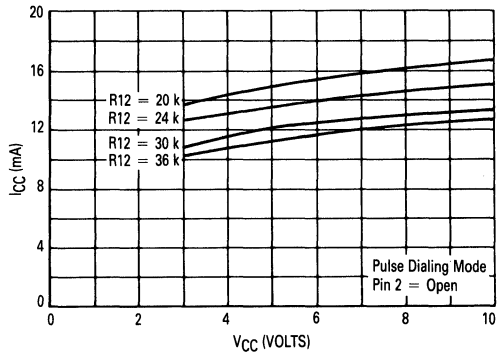


FIGURE 4 — I_{CC} versus V_{CC} (TONE DIALING MODE)

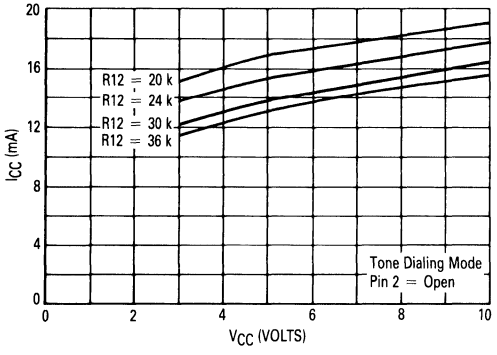


FIGURE 5 — V_R versus I_R versus V_{CC}

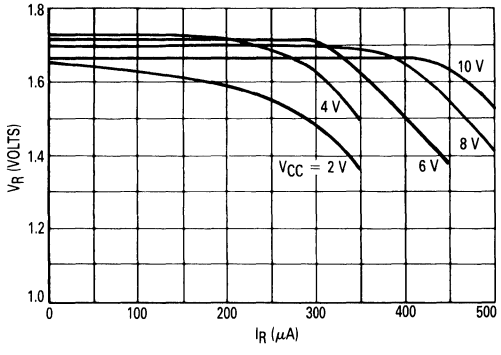


FIGURE 6 — V_{DD} versus I_{DD}

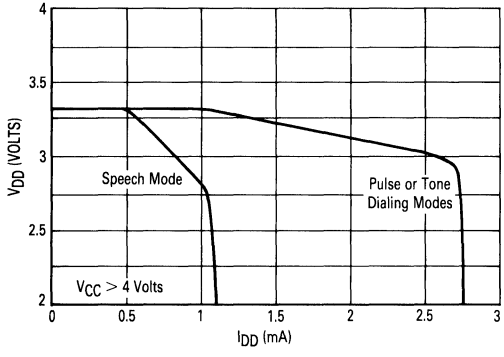


FIGURE 7 — AGC GAIN versus VOLTAGE AT PIN 9

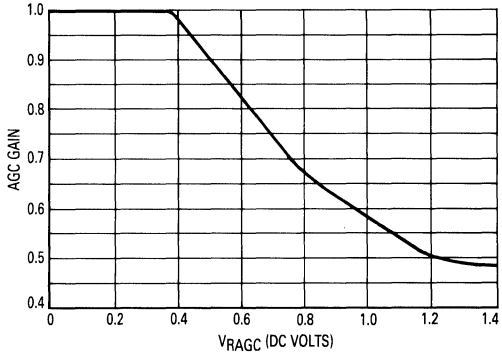


FIGURE 8 — MAXIMUM TRANSMIT SIGNAL AT V_{CC}

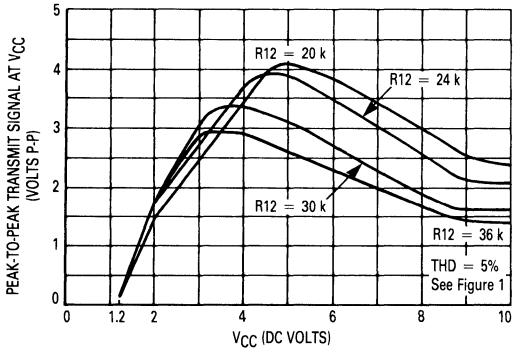
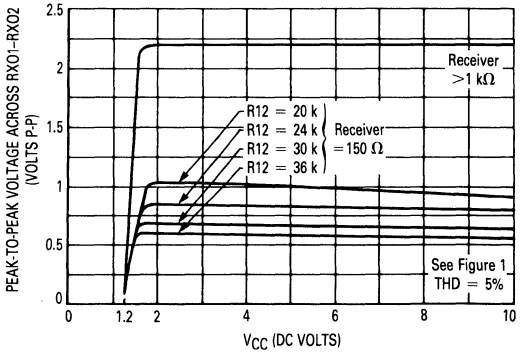


FIGURE 9 — MAXIMUM RECEIVER SIGNAL



SYSTEM PERFORMANCE

FIGURE 10 — TIP/RING VOLTAGE versus LOOP CURRENT

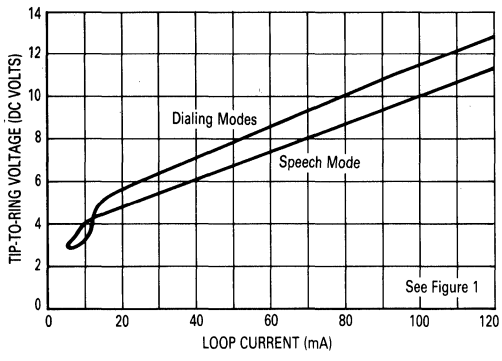


FIGURE 11 — AC TERMINATING IMPEDANCE versus LOOP CURRENT

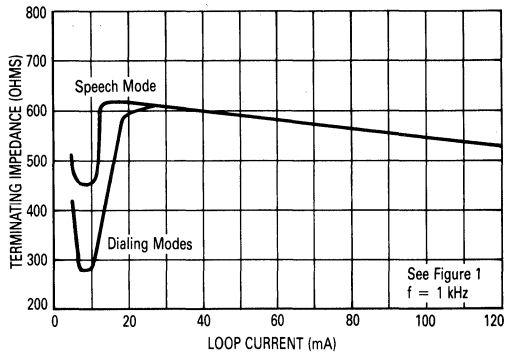


FIGURE 12 — TRANSMIT GAIN versus LOOP CURRENT

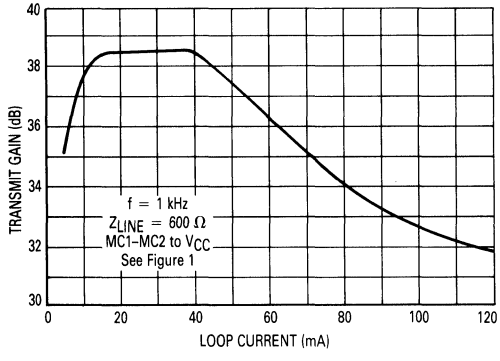


FIGURE 13 — TRANSMIT GAIN versus FREQUENCY

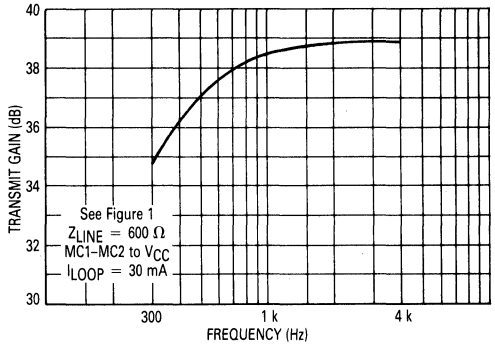


FIGURE 14 — RECEIVE GAIN versus LOOP CURRENT

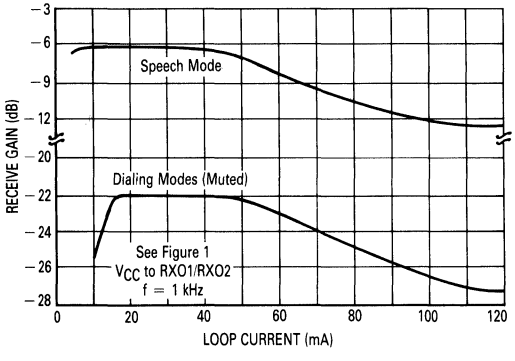
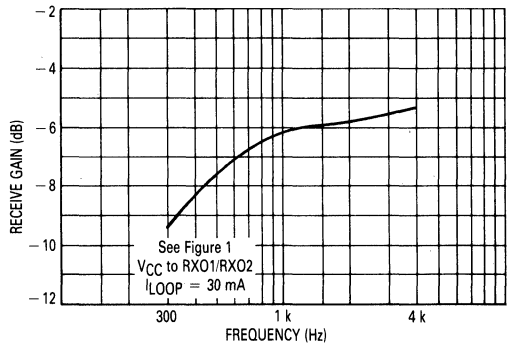


FIGURE 15 — RECEIVE GAIN versus FREQUENCY



SYSTEM PERFORMANCE

FIGURE 16 — TRANSMIT NOISE SPECTRUM

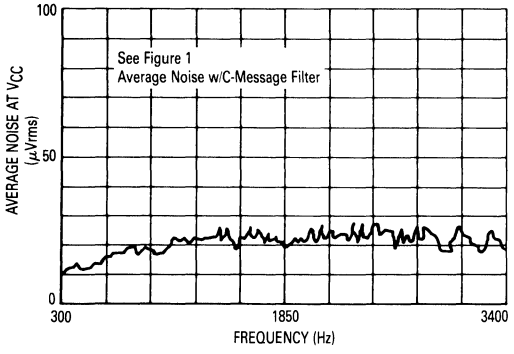


FIGURE 17 — RECEIVE NOISE SPECTRUM

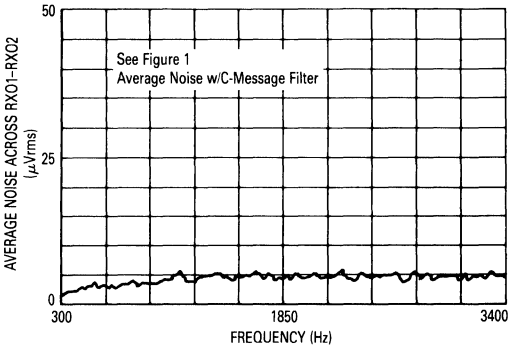


FIGURE 18 — V_{CC} versus TEMPERATURE

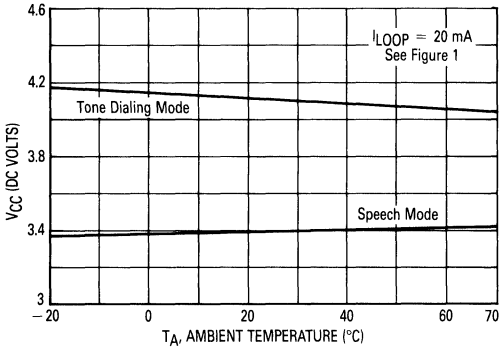


FIGURE 19 — TRANSMIT GAIN versus TEMPERATURE

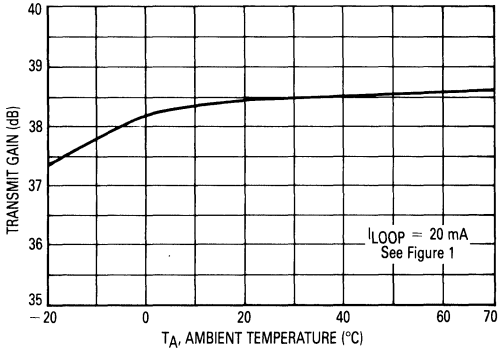


FIGURE 20 — RECEIVE GAIN versus TEMPERATURE

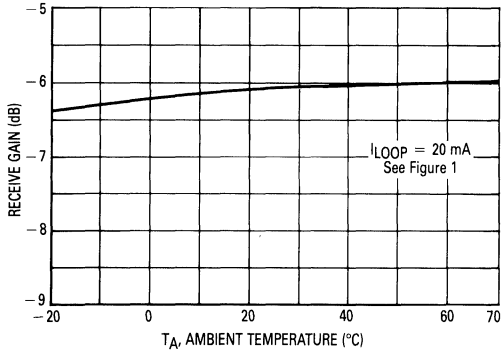
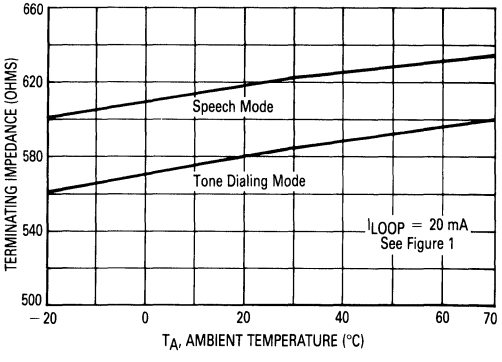


FIGURE 21 — AC TERMINATING IMPEDANCE versus TEMPERATURE



FUNCTIONAL DESCRIPTION

INTRODUCTION

The MC34114 is a speech network which provides the hybrid function and the DC loop current interface of a telephone, and is meant to connect to Tip and Ring through a polarity guard bridge. The transmit, receive, and sidetone gains are externally adjustable, and additionally, line length compensation varies the gains with variations in loop current. The microphone amplifier employs a differential input to minimize RFI susceptibility.

The loop current interface portion determines the dc voltage versus current characteristics, and provides the required regulated voltages for internal and external use.

The dialer interface provides three modes of operation: speech (non-dialing), pulse dialing and tone (DTMF) dialing. When switching among the modes, some parameters are changed in order to optimize the circuit operation for that mode. The following table summarizes those changes:

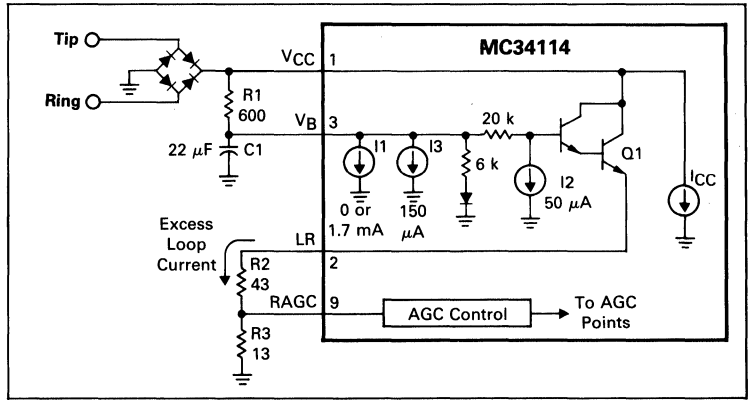
TABLE 1 — OPERATING PARAMETERS versus OPERATING MODE

Function	Speech	Pulse	Tone
LR Level Shift (V_{CC} – VLR)	2.8 V	2.8 V	3.8 V
V_{DD} Current Capability	1.0 mA	2.5 mA	2.5 mA
Microphone Amplifier	Functional	Muted	Muted
Receive Amp. Internal Feedback Resistor	Switched Out	Switched In	Switched In

DC LINE INTERFACE AND LINE LENGTH COMPENSATION

The DC line interface circuit (Pins 1, 2, 3) sets the DC voltage characteristics with respect to loop current. See Figure 22.

FIGURE 22 — DC LINE INTERFACE EQUIVALENT



The DC voltage at V_{CC} is determined by the level shift from V_{CC} to LR, plus the voltage across R2 and R3. I_{CC} is the internal bias current required by the MC34114, nominally in the range of 10 mA. I_{CC} can be reduced, if necessary, by increasing R12, consistent with the transmit and receive signal requirements (see the Transmit Path section). See Figures 2–4, 8 and 9.

In the speech and pulse dialing modes current source I1 is off, and the level shift is due to Q1's base-emitter drop (≈1.4 V), 1.0 volt across the 20 k resistor, and the voltage across R1, which varies with V_{CC} from 0.15 volts to ≈1.0 volt. When the loop current coming in from Tip and Ring exceeds the I_{CC} requirement, the excess current flows through Q1, R2 and R3, to set the slope of the V-I characteristic for the circuit (Q1 has an equivalent resistance of ≈10 Ω). See Figure 10.

In the tone dialing mode, current source I1 is on, drawing an additional 1.7 mA through R1, increasing the level shift by ≈1.0 volts (for R1 = 600 Ω). This feature ensures that, at low loop currents, sufficient voltage is present at V_{CC} for the DTMF signals, and that the V_{DD} regulator supplies sufficient voltage to an external dialer. The I_{CC} current increases by ≈1.3 mA in this mode.

R1 must be kept in the range of 100 to 1800 Ω. If it is too large, insufficient current will flow into V_B to bias up the circuit. If it is too small, insufficient filtering at V_B will result unless C1 is increased accordingly. Speech signals must be well filtered from V_B.

The voltage across R3 determines the operation of the AGC circuit (line length compensation). As the voltage at RAGC increases from ≈0.4 volts to ≈1.2 volts, the AGC Control varies the current gain of the two AGC

points (Figure 1) from 1.0 to 0.5, thereby reducing the gain of the transmit and receive paths by 6.0 dB. See Figure 7. Pin 9 is a high impedance input.

The values of R2 and R3 can be varied as required to comply with various regulatory agencies, to compensate for additional circuitry powered by the loop current (microprocessor, etc.), or to change the starting point of the AGC function. If the AGC is not used, Pin 9 should be connected to ground for high gains, or to V_R for low gains.

VOLTAGE REGULATORS

The MC34114 has two internal voltage regulators which are used to power external as well as internal circuitry.

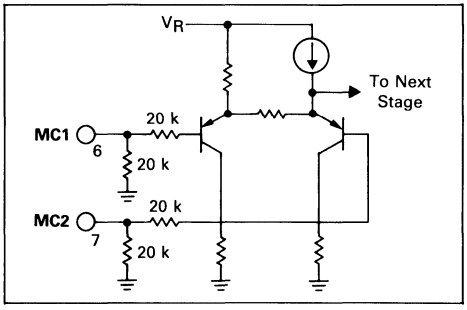
The V_R regulator provides 1.7 volts at a maximum current of 500 μA (see Figure 5). This output is normally used to set the DC bias into TXI (Pin 10), and to bias the electret microphone. V_R will typically be ≈300 mV less than V_{CC} when V_{CC} is below 2.0 volts.

The V_{DD} regulator provides 3.3 volts at a maximum of 1.0 mA in the speech mode, and 2.5 mA in the pulse or tone dialing modes (see Figure 6). It is normally used to power an external dialer, and other associated circuitry. V_{DD} is normally ≈0.5 volts less than V_{CC} until V_{DD} regulates. It is a shunt type regulator which automatically switches to a high impedance mode when V_{CC} falls below 1.4 volts. This feature prevents excessive battery drain in the event a memory sustaining battery is used with the external dialer. Leakage current (with V_{CC} = 0) is typically 0.02 μA with an applied voltage of up to 6.0 volts at V_{DD}, with pin 17 open or at V_{DD}. If Pin 17 is at ground, a current of several hundred microamps will flow into V_{DD} and out of pin 17 (see paragraph on Logic Interface).

MICROPHONE AMPLIFIER

The microphone amplifier (Pins 6, 7, 8) has a differential input, single ended output, and a fixed internal gain of +30 dB (31.1 V/V). The output is in phase with MC2, and out of phase with MC1. The inputs (see Figure 23) have a nominal impedance of 20 kΩ, and are matched to provide a high common mode rejection (typically 26 dB).

FIGURE 23 — INPUT STAGE



To preserve a high CMRR against unwanted signals induced in the microphone leads, the microphone should be biased with two equal value resistors as shown in Figure 1.

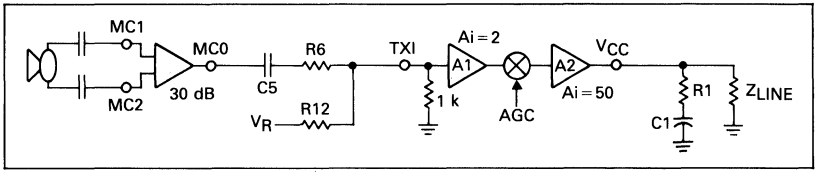
The output (MCO) has a DC bias voltage of ≈1.1 volts (V_{CC} > 3.0 volts), and can nominally swing ≈2.0 volts p-p (500 mV p-p at V_{CC} = 1.2 volts). The output impedance is ≈270 Ω, and has a peak current capability of ≈160 μA for 5% THD.

When the MC34114 is switched to either dialing mode, the microphone amplifier is muted by ≈70 dB (300 Hz–4 kHz), effectively disabling the microphone. The DC voltage at MCO is ≈80 mV when muted.

TRANSMIT PATH

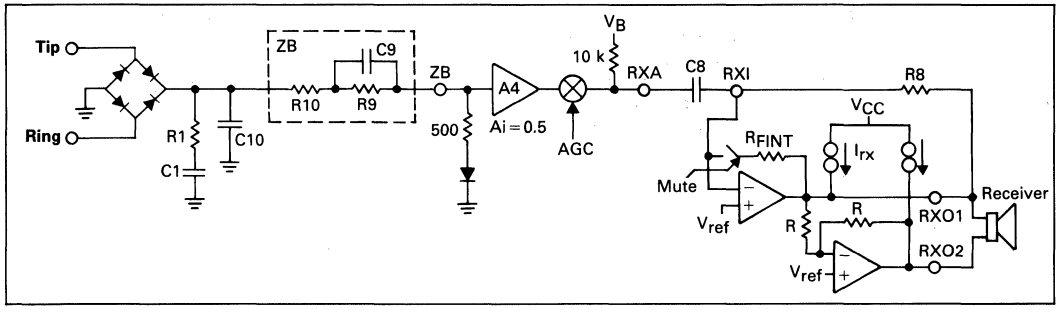
The AC transmit path consists of the components shown in Figure 24 (taken from Figure 1).

FIGURE 24 — TRANSMIT PATH



The voltage output at MCO is converted to a current into TXI by C5, R6, and TXI's 1.0 k input impedance (with a slight error due to R12). A1 and A2 are current amplifiers with a combined gain of 100. The AGC point has a current gain of 1.0 at low loop currents, and decreases to 0.5 as loop current increases. Therefore the current gain from TXI to V_{CC} varies from 100 to 50 as loop current is increased. The resulting current output at V_{CC} acts on R1 and the line impedance (nominally 600 Ω each, C1 is an AC short) to generate a voltage

FIGURE 25 — RECEIVE PATH



signal at V_{CC}, and consequently, at Tip and Ring. The voltage gain from MC1–MC2 to Tip and Ring is therefore (first order):

$$G_{TX} = \frac{Am \times 100 \times AGC \times R1//Z_{LINE}}{(R6 + 1.0\ k)} \qquad \text{(Equation 1)}$$

where Am is the gain of the microphone amplifier (31.1 V/V). At low loop currents G_{TX} ≈84 V/V (38.5 dB), and decreases to ≈42 V/V (32.5 dB) at higher loop currents, for the component values shown in Figure 1 (@ 1.0 kHz).

For more precise calculations, consideration should be given to the effects of C5 (in series with R6), R12 and R7 (each in parallel with TXI's 1.0 k impedance), and C10 and the ZB network (each in parallel with R1 and Z_{LINE}). The cumulative effects of these additional components is ≈1.5 dB.

The voltage signal at V_{CC} is out of phase with that at TXI, and in phase with that at MC1.

The maximum available voltage swing at V_{CC} is a function of the impedance at V_{CC} ($R1//Z_{LINE}$), the DC bias current at A2's output, and the V_{CC} DC voltage. A2's bias current is determined by the bias current through R12 ($V_R/\{R12 + 1.0\ k\}$) which is gained up by A1, A2 and the AGC point. Figure 8 indicates the maximum voltage swing at V_{CC} (with 5% THD).

RECEIVE PATH

The AC receive path consists of the components shown in Figure 25 (taken from Figure 1).

R1, typically 600 Ω, provides the AC termination (return loss) for the receive signals coming in on Tip and Ring (C1 is an AC short). The receive signal creates an AC current through the ZB network and the 500 Ω resistor at the ZB pin. A4 reduces that current by 1/2, and then feeds it through the AGC point which has a gain of 1.0 at low loop currents. The AGC gain is reduced to 0.5 as loop current increases. The AC current out of the AGC point feeds through C8 to RXI, the receive amp's summing node (If C8 is large, RXA can be considered a virtual ground, and no AC current flows through the internal 10 k resistor). The voltage swing at RXO1 is then determined by the current through C8 and the R8 feedback resistor. The second op amp (at RXO2) is internally configured for inverting unity gain. The voltage gain from Tip and Ring to RXO1–RXO2 (differential) is (first order):

$$G_{RX} = \frac{R8 \times AGC}{(ZB + 500)} \qquad \text{(Equation 2)}$$

where ZB = R10 + R9//C9 (≈R10 + R9).

For more precise calculations, the effects of C9 and C8 must be considered. C9 provides a phase shift to aid sidetone cancellation (see paragraph on Sidetone), and C8 can be selected to provide low frequency roll-off. High frequency roll-off can be obtained by adding a feedback capacitor across R8. For the component values shown in Figure 1, the receive gain measured ≈0.495 V/V (−6.1 dB) at low loop currents, and reduces to ≈0.25 V/V (−12 dB) at higher loop currents (@ 1.0 kHz).

When the MC34114 is switched to either dialing mode ($\overline{Mute}$ = low), the receive gain is muted by the switching in of the internal feedback resistor (R_{FINT} from RXO1 to RXI) — typically 1.0 kΩ. The effective feedback resistor for the amplifier is now the parallel combination of R8 and R_{FINT}. The amount of muting (in dB) can be calculated from:

$$G_{RXM} = 20 \times \log\left(\frac{R8 + R_{FINT}}{R_{FINT}}\right) \qquad \text{(Equation 3)}$$

The internal resistor is switched in coincident with $\overline{Mute}$ (Pin 17) switching low. However, when $\overline{Mute}$ is switched high, a delay (nominally 11 mSec) occurs before the internal resistor is switched out. This feature prevents dialing transients (particularly during pulse dialing) from being heard as loud clicks in the receiver.

The DC bias voltages at RXI, RXO1 and RXO2 is ≈0.65 volts. The bias current at RXI is ≈50 nA into the pin. The maximum voltage swing at RXO1 and RXO2 is a function of the receiver impedance (typically 100–150 Ω), and the value of the two I_{rx} current sources in Figure 25. I_{rx}, set by R12 (between V_R and TXI), is equal to:

$$I_{rx} = \frac{V_R \times 50 \times AGC}{(R12 + 1.0\ k)} \qquad \text{(Equation 4)}$$

Figure 9 indicates the maximum voltage swing available to the receiver.

SIDETONE CANCELLATION

Sidetone cancellation is provided by current amplifier A3 (see Figure 1) which generates a current representative of the transmit signal to cancel the reflected sidetone signal coming in through ZB and A4. To achieve perfect cancellation (no AC current out of RXA), it is necessary that:

$$ZB = (40 \times R1 // Z_{LINE}) - 500\ \Omega \quad \text{(Equation 5)}$$

where ZB is the network composed of R9, R10, and C9, and Z_{LINE} is the AC impedance of the line. The reactive components of the line's impedance can be compensated for by making the ZB network comparably reactive. In Figure 1, C9 provides a phase shift to compensate for the phase shift created by the phone line.

LOGIC INTERFACE ($\overline{\text{Mute}}$ and MS)

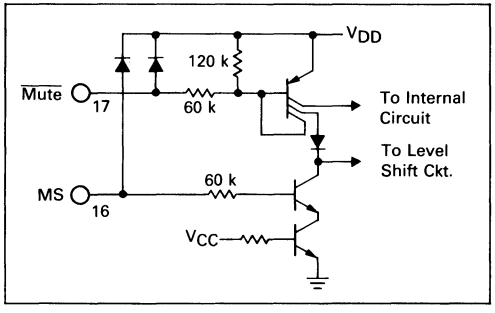
The two logic inputs ($\overline{\text{Mute}}$ and MS) are used to switch the MC34114 between the speech and dialing modes according to the following table:

TABLE 2 — LOGIC INPUTS

$\overline{\text{Mute}}$	MS	Mode
High	X	Speech
Low	High	Pulse Dialing
Low	Low	Tone Dialing

Table 2, together with Table 1, describes the condition of the MC34114 in the various modes. Figure 26 shows the input configuration for the $\overline{\text{Mute}}$ and MS pins.

FIGURE 26 — LOGIC INPUTS



The $\overline{\text{Mute}}$ input has a nominal input impedance of 60 kΩ, referenced to V_{DD}. This pin may be left open for a logic "1," or connected to V_{DD}. A logic "1" is defined as between V_{DD}–0.5 volts and V_{DD}. A logic "0" is defined as between ground and 1.0 volt. The switching threshold is ≈2.3 volts. When $\overline{\text{Mute}}$ is switched low (speech to dialing), the changes listed in Table 1 will occur within 10 μs. Upon switching high (back to speech mode), however, the receive amplifier feedback resistor will be switched out after a delay of (typically) 11 ms. This feature prevents dialing transients (particularly during pulse dialing) from being heard as loud clicks in the receiver. The other functions listed in Table 1 transfer within 10 μs.

The MS pin is functional only when $\overline{\text{Mute}}$ is low and its only function is to provide an additional voltage level shift between V_{CC} and LR in the tone dialing mode (see the section on DC Interface). The input impedance is ≈60 kΩ when $V_{CC} > 1.5$ volts. A logic "0" is between ground and 0.3 volts, and a logic "1" is between 2.0 volts and V_{DD}. The switching threshold is typically 0.75 volts. If unused, this pin must be connected to ground or V_{DD}, and not left open.

When $V_{CC} = 0$ (on-hook condition), and a voltage in the range of 0 to 6.0 volts is applied to $\overline{\text{Mute}}$, a leakage current of (typically) 0.02 μA will flow if $\overline{\text{Mute}}$ and V_{DD} are at the same voltage. If $\overline{\text{Mute}}$ is at a voltage different from V_{DD}, current will flow through the internal resistors and/or diode. If a memory sustaining battery is used in conjunction with an external dialer, and is configured so that its voltage appears at V_{DD}, $\overline{\text{Mute}}$ must be allowed to float or be connected to V_{DD} — otherwise current (in the range of 100–200 μA) will flow from the battery through V_{DD} and out of the $\overline{\text{Mute}}$ pin.

When $V_{CC} = 0$, and a voltage in the range of 0 to 6.0 volts is applied to MS, a leakage current of (typically) 0.01 μA will result as long as $\overline{\text{Mute}}$ is open or at V_{DD}. If $\overline{\text{Mute}}$ is at ground, an equivalent 3.5 kΩ parasitic resistance exists between MS and $\overline{\text{Mute}}$.

When $V_{CC} < 1.5$ volts, the Mute function is nonexistent and the MC34114 will be in the speech mode.

APPLICATIONS INFORMATION

DESIGN SEQUENCE

The design sequence for incorporating the MC34114 into most applications will be as follows (refer to Figure 1):

1) Decide on the AC terminating impedance (return loss), and select R1 to be that value (typically 600 Ω). If there are other devices powered by the loop current which will be in parallel with R1 (such as a pulse dialing circuit) which lower the effective terminating impedance, R1 can be increased accordingly.

2) Select the maximum value of R12 which will provide the minimum required transmit and receive signals according to Figures 8 and 9.

3) Select the sum {R2 + R3} to provide the desired Tip and Ring DC voltage versus loop current characteristics. Then select R3 for the desired starting point of the loop length compensation. The compensation begins when the voltage across R3 is ≈0.4 volt.

4) Select R4 and R5 (they should be equal) to properly bias the microphone. The microphone's manufacturer should be consulted for this information.

5) Select R6 for proper transmit gain. See equation 1. Then select C5 to provide low frequency roll-off. Adjust R6 as required.

6) Select the ZB network (R9, R10, C9) to provide sidetone cancellation. See equation 5.

7) Select R8 for proper receive gain (depends on the specific receiver used). See equation 2. Then select C8 to provide low frequency roll-off. Adjust R8 as required.

Additional comments on Figure 1 components:

1) Capacitors C1, C2, and C7 are required to stabilize the respective regulators. In most applications it should not be necessary to change from the values shown in Figure 1.

2) C3 and C4 can be selected to provide low frequency roll-off for the microphone signals.

3) C10 filters noise generated by the MC34114, and should be close to the V_{CC} pin. Its recommended value (0.01 μF) is such that it does not noticeably affect the system parameters. It can be increased, if desired, to provide high frequency roll-off for both transmit and receive signals. This, however, will affect the return loss specification at higher frequencies.

4) Since TXI is a (relatively) low impedance current input, it is a convenient point for injecting any signals which are to be transmitted out onto Tip and Ring. C6 and R7 are shown for transmitting the DTMF signals from a dialer. Additional RC networks can be connected to TXI for transmitting signals from speakerphones, modems, or other signal sources. The voltage gain from each signal source to Tip and Ring is:

$$G_S = \frac{Z_{LINE}//R1 \times 100 \times AGC}{(R_X + Z_{CX})} \quad \text{(Equation 6)}$$

where R_X and Z_{CX} represent the impedances of the R and C for the particular signal source. If several signal sources are connected to TXI, the parallel combination of R6, R12, the internal 1.0 k resistor, and any other RCs at this pin must be considered when setting the gain for each signal.

5) The 12 volt zener diode shown in Figure 1 is for transient protection, and normally does not conduct. Transient and overvoltage protection **MUST** be provided externally so that the Absolute Maximum Ratings are not exceeded.

BASIC TELEPHONE CIRCUIT

Figure 27 depicts a complete basic telephone using the MC34114 speech network, the MC145412 pulse/tone dialer, and the MC34017 tone ringer.

The MC34114 provides the speech network/hybrid functions, and its component values are calculated as described previously in this data sheet. The resistor from V_{CC} to V_B is 820 Ω (rather than 600 Ω) in this example since it is in parallel with the 2.0 kΩ resistor in the pulse dialing transistor network (providing and effective 600 Ω termination).

The MC145412 dialer is a pulse/tone dialer with 10 number memory, including last number redial. Power to the dialer is from the MC34114's V_{DD} output, diode connected with a memory sustaining battery.

The MC34017 tone ringer (see its data sheet for details) is connected directly to Tip and Ring as it is not necessary to disconnect it when off-hook. This circuit has an REN ≈0.5, and meets all EIA-470 and Bell system requirements for impedance, anti-bell tapping, and turn-on/off thresholds.

OPERATION WITH A POWER SUPPLY

Figure 28 indicates how to incorporate the MC34114 into a circuit where a power supply is used.

FIGURE 27 — BASIC PULSE/TONE TELEPHONE

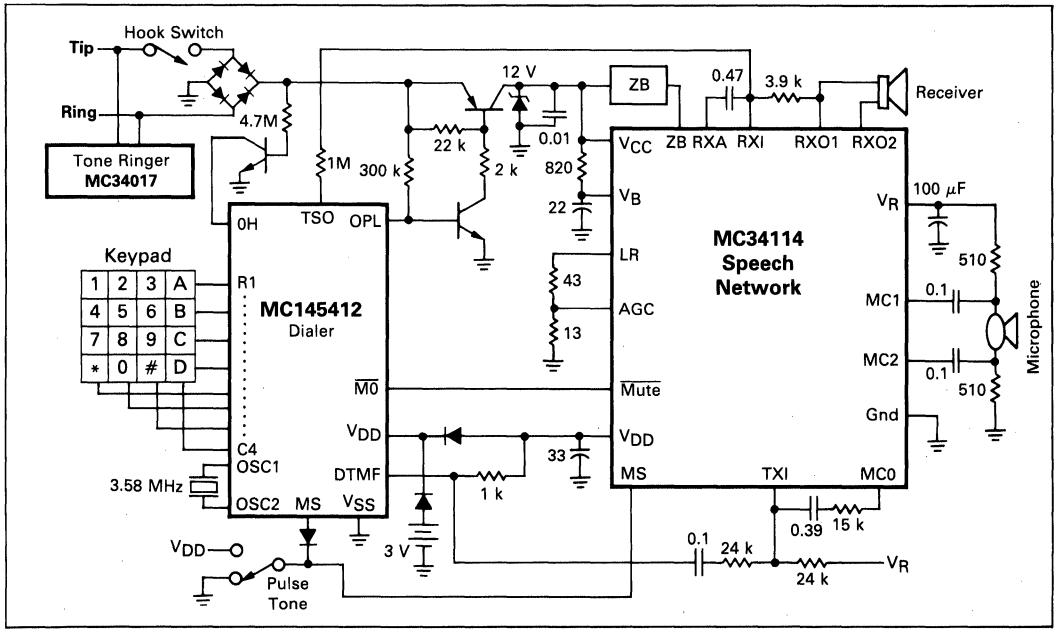
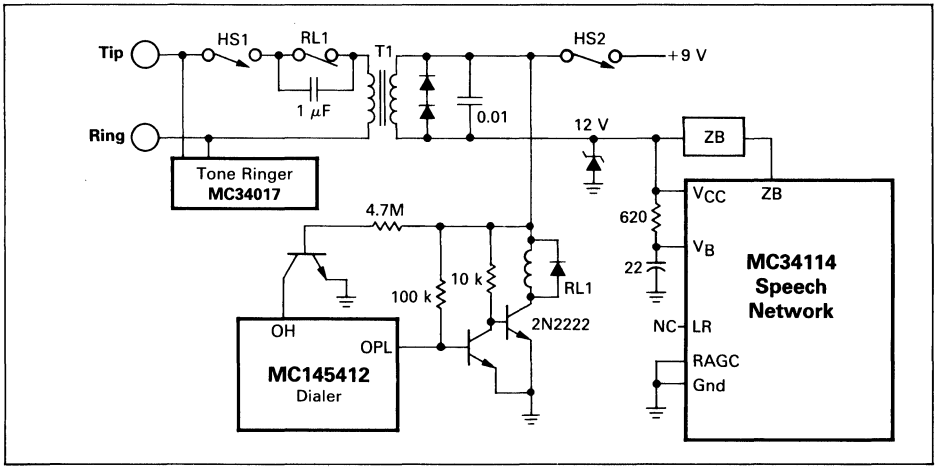


FIGURE 28 — USE WITH A POWER SUPPLY



A transformer (T1) is required at Tip and Ring to provide the isolation required between the phone line and any AC power and earth ground. (The transformer must be rated to handle the loop current.) Since the loop current does not pass through the MC34114, loop length compensation is not possible in this circuit, and pin 2 (LR) is left open. The RAGC pin is grounded, setting the transmit and receive gains to their maximum.

The transformer provides a path for the power supply to reach the MC34114, while simultaneously coupling speech signals between Tip/Ring and the MC34114. The two series diodes provide transient clamping, as does the 12 volt zener diode. Although a +9.0 volt supply is shown, other voltages can be used as long as the MC34114 receives between 4.0 and 10.5 volts at V_{CC}.

Because of the isolation requirement, the MC145412 dialer requires a relay (RL1) to break the loop current during pulse dialing. The relay is normally off, and energized only during pulse dialing. The 1.0 μF capacitor (rated 250 volts min., NPO) across the relay contacts helps absorb transients generated during pulse dialing.

ALTERNATE MICROPHONE CONFIGURATIONS

The MC34114 is designed for use with electret microphones, although dynamic microphones can be used. Carbon microphones are not recommended as they generally require considerable bias current which is not available from the MC34114's regulators.

When using an electret microphone which requires more than 1.7 volts, but less than 1.0 mA for bias, it can be biased from V_{DD} instead.

If a three terminal electret microphone (containing an internal biasing resistor or equivalent) is used, it should be connected to the MC34114 as shown in Figure 29. The common mode rejection of the balanced circuit shown in Figure 1 is not present however, and care should be taken to prevent unwanted signals (radio stations, noise, etc.) from being picked up by the microphone leads.

FIGURE 29 — 3-TERMINAL MICROPHONE

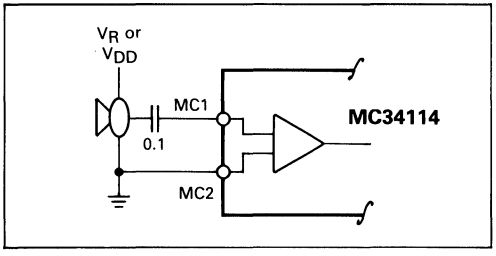
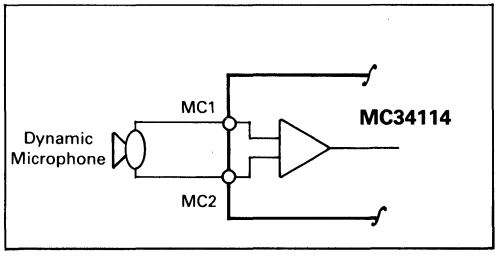


Figure 30 indicates use of the MC34114 with a dynamic microphone. The output level of dynamic microphones is generally lower than electret units, and so the gain of the transmit path will have to be adjusted accordingly.

FIGURE 30 — DYNAMIC MICROPHONE

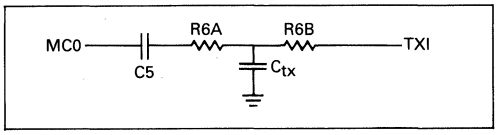


FREQUENCY CHARACTERISTICS

Frequency characteristics for both transmit and receive signals are dependent entirely on the external components. The amplifiers within the IC have bandwidths from DC extending to in excess of 50 kHz, and therefore do not provide roll-off within the voiceband.

Low frequency roll-off for the transmit signals can be set by adjusting C3 and C4, or C5, or a combination of the three. High frequency roll-off can be provided by replacing R6 with the network shown in Figure 31.

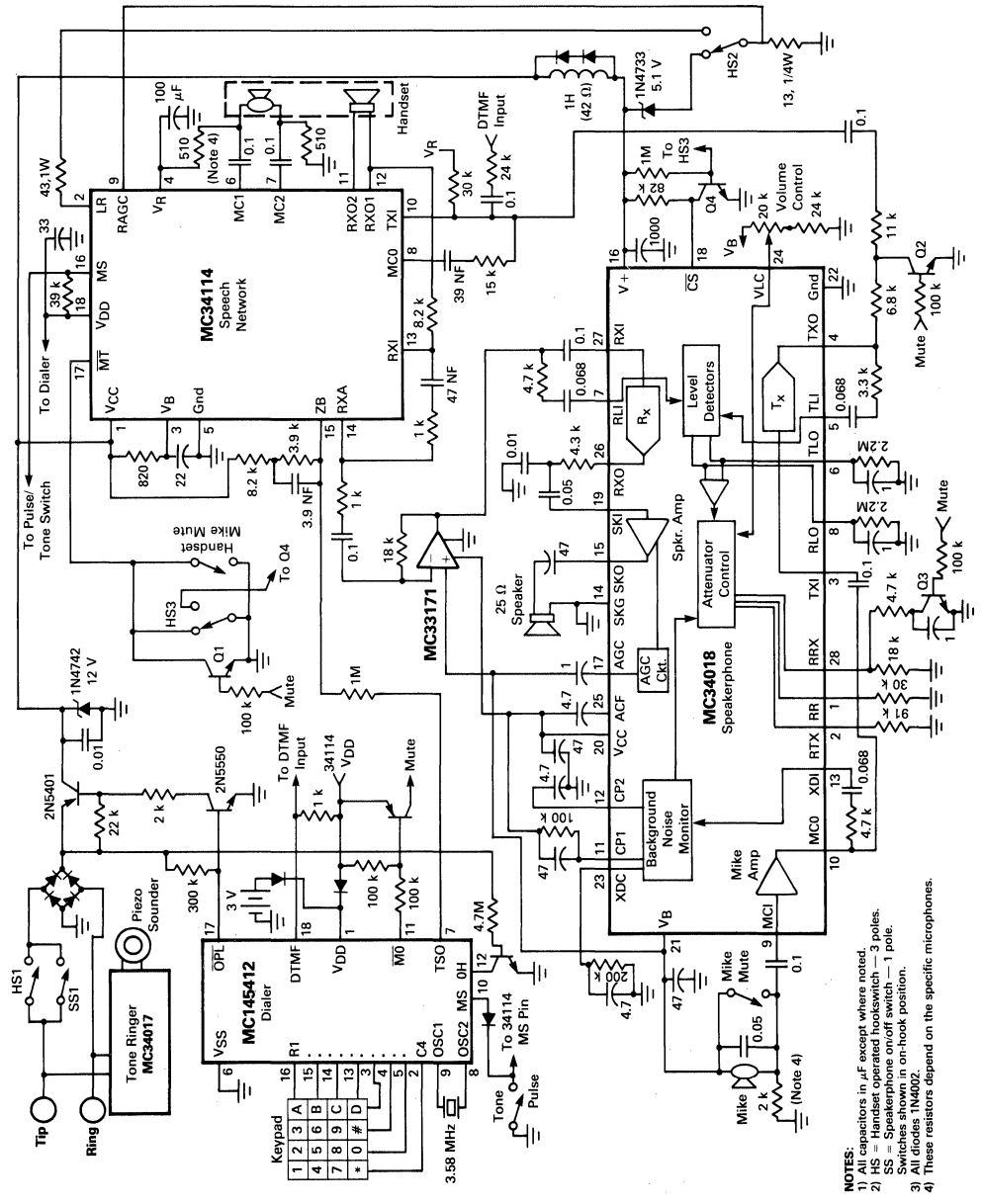
FIGURE 31 — TRANSMIT HF ROLL-OFF



The 3.0 dB upper frequency is determined by:

$$f = \frac{(R6A + R6B + 1.0\ k)}{2\pi\ (R6A \times (R6B + 1.0\ k) \times C_{tx})} \quad \text{(Equation 7)}$$

FIGURE 32 — PULSE/TONE FEATUREPHONE WITH MEMORY — LINE POWERED



Low frequency roll-off for the receive signals can be set by adjusting C8, and high frequency roll-off can be set by placing a capacitor across R8.

FEATUREPHONE DESIGN

Figure 32 and Figure 33 depict two featurephone circuits which include the following functions: selectable handset and speakerphone operation, ten number memory pulse/tone dialer, tone ringer, a "Privacy" (Mike mute) function, and line length compensation for both handset and speakerphone operation. Figure 32 uses the MC34018 speakerphone IC, while Figure 33 uses the MC34118 speakerphone IC. Application notes AN1002 and AN1004 (for Figure 32 and Figure 33 respectively) should be consulted for design and performance details, as well as variations of these two circuits.

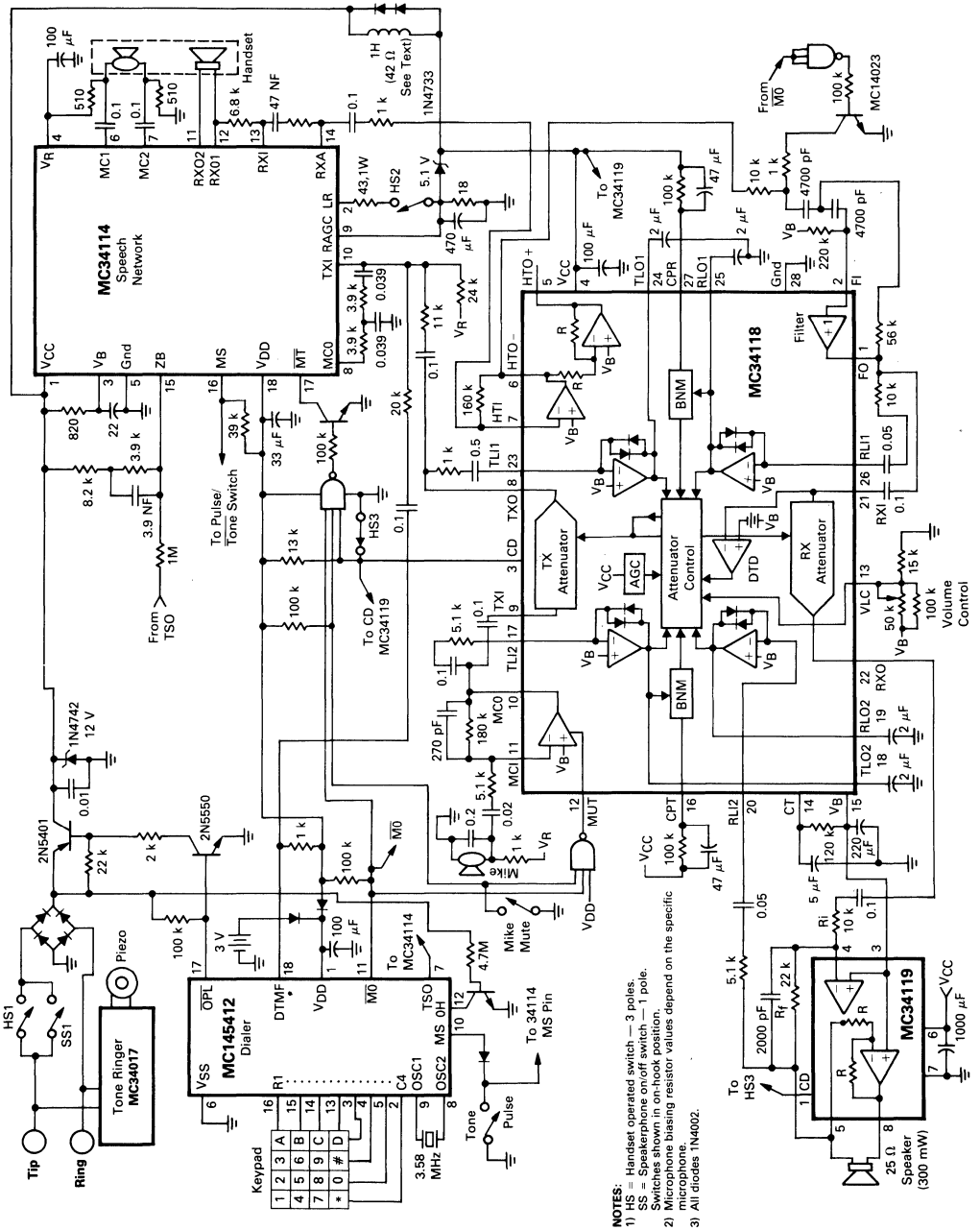


FIGURE 33 — PULSE/TONE FEATUREPHONE WITH MEMORY — LINE POWERED

NOTES:
1) HS = Handset operated switch — 3 poles.
SS = Speakerphone on/off switch — 1 pole.
Switches shown in on-hook position.
2) Microphone biasing resistor values depend on the specific microphone.
3) All diodes 1N4002.

EMI SUSCEPTIBILITY

Potential EMI susceptibility problems should be addressed early in the electrical and mechanical design of the telephone. EMI may enter the circuit through Tip and Ring, through the microphone wiring, or through any of the PC board traces. The most sensitive pins on the MC34114 are the microphone amplifier inputs (MC1, MC2). Board traces to these pins should be kept short, and the associated components should preferably be physically close to the pins. TXI, RXI, and ZB should also be considered sensitive to EMI signals.

The microphone wires within the handset cord can act as an antenna, and pick up nearby radio stations. If this is a problem in the final design, adding RF filters (consisting of ferrite beads and small (0.001 μF) ceramic capacitors) to the PC board where the wires attach to the board can generally reduce the problem.

2

SUGGESTED VENDORS

Microphones

Primo Microphones Inc.
Bensenville, Ill. 60106
312-595-1022
Model EM-60

MURA Corp.
Westbury, N.Y. 11590
516-935-3640
Model EC-983-7

Hosiden America Corp.
Elk Grove Village, Ill. 60007
312-981-1144
Model KUC2123

Telecom Transformers

Microtran Co., Inc.
Valley Stream, N.Y. 11528
516-561-6050
Ask for Applications
Bulletin F232

Stancor Products
Logansport, IN 46947
219-722-2244

PREM Magnetics, Inc.
McHenry, Ill. 60050
815-385-2700

Onan Power/Electronics
Minneapolis, MN 55437
612-921-5600

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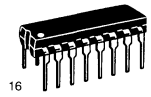
Compliance with FCC or other regulatory agencies of the circuits described herein is not implied or guaranteed by Motorola Inc.

MC34115

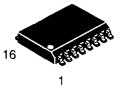
Continuously Variable Slope Delta Modulator/Demodulator

Providing a simplified approach to digital speech encoding/decoding, the MC34115 CVSD is designed for speech synthesis and commercial telephone applications. A single IC provides both encoding and decoding functions.

- Encode and Decode Functions Selectable with a Digital Input
- Utilization of Compatible I^2L — Linear Bipolar Technology
- CMOS Compatible Digital Output
- Digital Input Threshold Selectable ($V_{CC}/2$ Reference Provided On Chip)
- 3–Bit Algorithm



P SUFFIX
PLASTIC PACKAGE
CASE 648

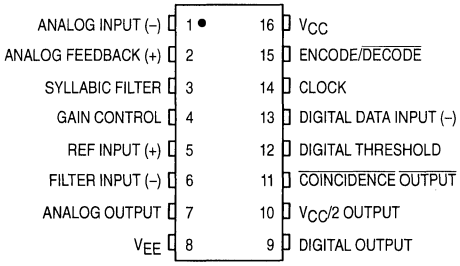


DW SUFFIX
SOG PACKAGE
CASE 751G

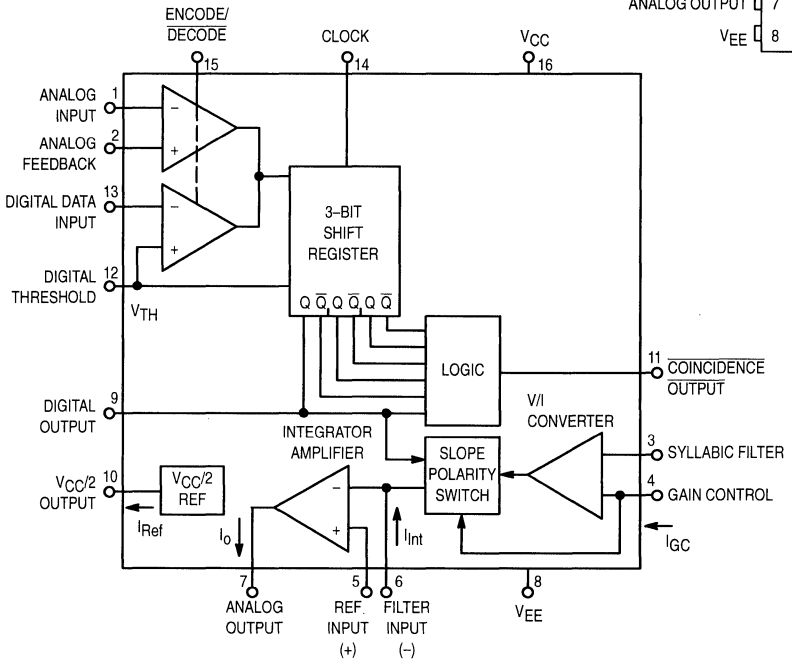
ORDERING INFORMATION

MC34115P	Plastic Package
MC34115DW	SOG Package

PIN ASSIGNMENT



CVSD BLOCK DIAGRAM



REV
9/95

MC34118

Specifications and Applications Information

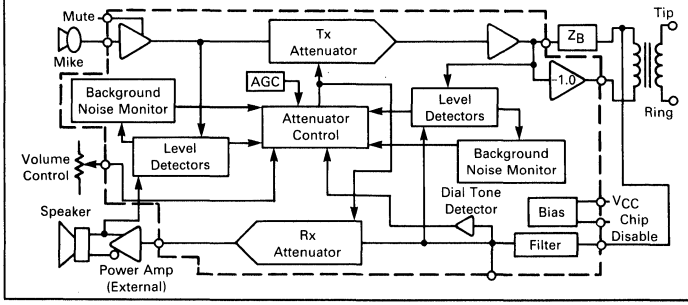
VOICE SWITCHED SPEAKERPHONE CIRCUIT

The MC34118 Voice Switched Speakerphone Circuit incorporates the necessary amplifiers, attenuators, level detectors, and control algorithm to form the heart of a high quality hands-free speakerphone system. Included are a microphone amplifier with adjustable gain and MUTE control, Transmit and Receive attenuators which operate in a complementary manner, level detectors at both input and output of both attenuators, and background noise monitors for both the transmit and receive channels. A Dial Tone Detector prevents the dial tone from being attenuated by the Receive background noise monitor circuit. Also included are two line driver amplifiers which can be used to form a hybrid network in conjunction with an external coupling transformer. A high-pass filter can be used to filter out 60 Hz noise in the receive channel, or for other filtering functions. A Chip Disable pin permits powering down the entire circuit to conserve power on long loops where loop current is at a minimum.

The MC34118 may be operated from a power supply, or it can be powered from the telephone line, requiring typically 5.0 mA. The MC34118 can be interfaced directly to Tip and Ring (through a coupling transformer) for stand-alone operation, or it can be used in conjunction with a handset speech network and/or other features of a featurephone.

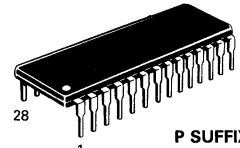
- Improved Attenuator Gain Range: 52 dB Between Transmit and Receive
- Low Voltage Operation for Line-Powered Applications (3.0–6.5 V)
- 4-Point Signal Sensing for Improved Sensitivity
- Background Noise Monitors for Both Transmit and Receive Paths
- Microphone Amplifier Gain Set by External Resistors — Mute Function Included
- Chip Disable for Active/Standby Operation
- On Board Filter Pinned-Out for User Defined Function
- Dial Tone Detector to Inhibit Receive Idle Mode During Dial Tone Presence
- Standard 28-Pin Plastic DIP Package and SOIC Package Available
- Compatible with MC34119 Speaker Amplifier

SIMPLIFIED BLOCK DIAGRAM

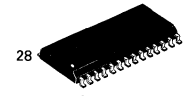


VOICE SWITCHED SPEAKERPHONE CIRCUIT

SILICON MONOLITHIC INTEGRATED CIRCUIT



P SUFFIX
PLASTIC PACKAGE
CASE 710



DW SUFFIX
PLASTIC PACKAGE
CASE 751F

PIN CONNECTIONS

(Top View)

FO	1	28	GND
FI	2	27	CPR
CD	3	26	RLI1
V_{CC}	4	25	RLO1
HTO+	5	24	TLO1
HTO−	6	23	TLI1
HTI	7	22	RXO
TXO	8	21	RXI
TXI	9	20	RLI2
MCO	10	19	RLO2
MCI	11	18	TLO2
MUT	12	17	TLI2
VLC	13	16	CPT
CT	14	15	V_B

(Pin assignments same for both packages)

ABSOLUTE MAXIMUM RATINGS

Parameter	Value	Units
Supply Voltage (Pin 4)	−1.0, +7.0	Vdc
Voltage at CD (Pin 3), MUT (Pin 12)	−1.0, V_{CC} + 1.0	Vdc
Voltage at VLC (Pin 13)	−1.0, V_{CC} + 0.5	Vdc
Voltage at TXI (Pin 9), RXI (Pin 21), FI (Pin 2)	−0.5, V_{CC} + 0.5	Vdc
Storage Temperature Range	−65 to +150	°C

Devices should not be operated at or outside these values. The "Recommended Operating Limits" provide for actual device operation.

RECOMMENDED OPERATING LIMITS

Parameter	Min	Typ	Max	Units
Supply Voltage (Pin 4) (See Text)	3.5	—	6.5	Vdc
CD Input (Pin 3), MUT Input (Pin 12)	0	—	V_{CC}	Vdc
I_{VB} Current (Pin 15)	—	—	500	μA
VLC (Pin 13)	0.3 x V_B	—	V_B	Vdc
Attenuator Input Signal Voltage (Pins 9, 21)	0	—	350	mVrms
Microphone Amplifier, Hybrid Amplifier Gain	0	—	40	dB
Load Current @ RXO, TXO (Pins 8, 22) @ MCO (Pin 10) @ HTO−, HTO+ (Pins 6, 5)	0 0 0	— — —	±2.0 ±1.0 ±5.0	mA
Ambient Operating Temperature Range	−20	—	+60	°C

ELECTRICAL CHARACTERISTICS (T_A = +25°C, V_{CC} = 5.0 V, CD ≤ 0.8 V, unless noted)

Parameter	Symbol	Min	Typ	Max	Units
POWER SUPPLY					
V_{CC} Supply Current (V_{CC} = 6.5 V, CD = 0.8 V) (V_{CC} = 6.5 V, CD = 2.0 V)	I_{CC}	— —	5.5 600	8.0 800	mA μA
CD Input Resistance (V_{CC} = V_{CD} = 6.5 V) CD Input Voltage — High — Low	R_{CD} V_{CDH} V_{CDL}	50 2.0 0	90 — —	— V_{CC} 0.8	kΩ Vdc Vdc
V_B Output Voltage (V_{CC} = 3.5 V) (V_{CC} = 5.0 V)	V_B	— 1.8	1.3 2.1	— 2.4	Vdc
V_B Output Resistance (I_{VB} = 1.0 mA)	R_{OVB}	—	400	—	Ω
V_B Power Supply Rejection Ratio (C_{VB} = 220 μF, f = 1.0 kHz)	PSRR	—	54	—	dB
ATTENUATORS (T_A = +25°C)					
Receive Attenuator Gain (f = 1.0 kHz, V_{LC} = V_B) Rx Mode, RXI = 150 mVrms (V_{CC} = 5.0 V) Rx Mode, RXI = 150 mVrms (V_{CC} = 3.5 V) Gain Change − V_{CC} = 3.5 V versus V_{CC} = 5.0 V AGC Gain Change − V_{CC} = 2.8 V versus V_{CC} = 5.0 V* Idle Mode, RXI = 150 mVrms Range (Rx to Tx Mode)	 G_{RX} G_{RX} ΔG_{RX1} ΔG_{RX2} G_{RXI} ΔG_{RX3}	 +4.0 +4.0 −0.5 — −22 49	 +6.0 +6.0 0 −25 −20 52	 +8.0 +8.0 +0.5 −15 −17 54	dB
Volume Control Range (Rx Mode, 0.3 V_B < V_{LC} < V_B)	V_{CR}	27	35	—	dB
RXO DC Voltage (Rx Mode)	V_{RXO}	—	V_B	—	Vdc
ΔRXO DC Voltage (Rx to Tx Mode)	ΔV_{RXO}	—	±10	±150	mV
RXO High Voltage (I_{out} = −1.0 mA RXI = V_B + 1.5 V)	V_{RXOH}	3.7	—	—	Vdc
RXO Low Voltage (I_{out} = +1.0 mA, RXI = V_B − 1.0, Output measured with respect to V_B)*	V_{RXOL}	—	−1.5	−1.0	Vdc
RXI Input Resistance (RXI < 350 mVrms)	R_{RXI}	7.0	10	14	kΩ

(continued)

ELECTRICAL CHARACTERISTICS (T_A = +25°C, V_{CC} = 5.0 V, CD ≤ 0.8 V, unless noted)

Parameter	Symbol	Min	Typ	Max	Units
ATTENUATORS — continued (T_A = +25°C)					
Transmit Attenuator Gain (f = 1.0 kHz) Tx Mode, TXI = 150 mVrms Idle Mode, TXI = 150 mVrms Range (Tx to Rx Mode)	 G_{TX} G_{TXI} ΔG_{TXI}	 +4.0 −22 49	 +6.0 −20 52	 +8.0 −17 54	dB
TXO DC Voltage (Tx Mode)	V_{TXO}	—	V_B	—	Vdc
ΔTXO DC Voltage (Tx to Rx Mode)	ΔV_{TXO}	—	±30	±150	mV
TXO High Voltage (I_{out} = −1.0 mA TXI = V_B + 1.5 V)	V_{TXOH}	3.7	—	—	Vdc
TXO Low Voltage (I_{out} = +1.0 mA, TXI = V_B − 1.0 V, Output measured with respect to V_B)*	V_{TXOL}	—	−1.5	−1.0	Vdc
TXI Input Resistance (TXI < 350 mVrms)	R_{TXI}	7.0	10	14	kΩ
Gain Tracking (G_{RX} + G_{TX}, @ Tx, Idle, Rx)*	G_{TR}	—	±0.1	—	dB

*See text for explanation.

ATTENUATOR CONTROL (T_A = +25°C)

C_T Voltage (Pin 14 − V_B) Rx Mode (V_{LC} = V_B) Idle Mode Tx Mode	V_{CT}	 — — —	 +240 0 −240	 — — —	mV
C_T Source Current (switching to Rx mode)	I_{CTR}	−85	−60	−40	μA
C_T Sink Current (switching to Tx mode)	I_{CTT}	+40	+60	+85	μA
C_T Slow Idle Current	I_{CTS}	—	0	—	μA
C_T Fast Idle Internal Resistance	R_{FI}	1.5	2.0	3.6	kΩ
V_{LC} Input Current	I_{VLC}	—	−60	—	nA
Dial Tone Detector Threshold	V_{DT}	10	15	20	mV

MICROPHONE AMPLIFIER (T_A = +25°C, V_{MUT} ≤ 0.8 V, A_{VCL} = 31 dB unless otherwise noted)

Ouptut Offset (V_{MCO} − V_B, Feedback R = 180 kΩ)	MCO_{VOS}	−50	0	+50	mVdc
Open Loop Gain (f < 100 Hz)	A_{VOLM}	70	80	—	dB
Gain Bandwidth	GBW_M	—	1.0	—	MHz
Output High Voltage (I_{out} = −1.0 mA, V_{CC} = 5.0 V)	V_{MCOH}	3.7	—	—	Vdc
Output Low Voltage (I_{out} = +1.0 mA)	V_{MCOL}	—	—	200	mVdc
Input Bias Current (@ MCI)	I_{BM}	—	−40	—	nA
Muting (ΔGain) (f = 1.0 kHz, V_{MUT} = 2.0 V) (300 Hz < f < 10 kHz)	GMT	−55 —	— −68	— —	dB
MUT Input Resistance (V_{CC} = V_{MUT} = 6.5 V)	R_{MUT}	50	90	—	kΩ
MUT Input — High	V_{MUTH}	2.0	—	V_{CC}	Vdc
MUT Input — Low	V_{MUTL}	0	—	0.8	Vdc
Distortion (300 Hz < f < 10 kHz)	THD_M	—	0.15	—	%

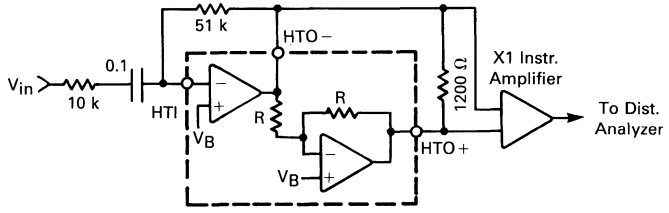
HYBRID AMPLIFIERS (T_A = +25°C)

HTO− Offset (V_{HTO-} − V_B, Feedback R = 51 kΩ)	H_{VOS}	−20	0	+20	mVdc
HTO− to HTO+ Offset (Feedback R = 51 kΩ)	HB_{VOS}	−30	0	+30	mVdc
Open Loop Gain (HTI to HTO−, f < 100 Hz)	A_{VOLH}	60	80	—	dB
Gain Bandwidth	GBW_H	—	1.0	—	MHz
Closed Loop Gain (HTO− to HTO+)	A_{VCLH}	−0.35	0	+0.35	dB
Input Bias Current (@HTI)	I_{BH}	—	−30	—	nA
HTO− High Voltage (I_{out} = −5.0 mA)	V_{HT-H}	3.7	—	—	Vdc
HTO− Low Voltage (I_{out} = +5.0 mA)	V_{HT-L}	—	—	250	mVdc
HTO+ High Voltage (I_{out} = −5.0 mA)	V_{HT+H}	3.7	—	—	Vdc
HTO+ Low Voltage (I_{out} = +5.0 mA)	V_{HT+L}	—	—	450	mVdc
Distortion (300 Hz < f < 10 kHz, See Figure 1)	THD_H	—	0.3	—	%

Parameter	Symbol	Min	Typ	Max	Units
LEVEL DETECTORS AND BACKGROUND NOISE MONITORS (T_A = +25°C)					
Transmit-Receive Switching Threshold (Ratio of Current at RLI1 + RLI2 to 20 μA at TLI1 + TLI2 to switch from Tx to Rx)	I_{TH}	0.8	1.0	1.2	
Source Current at RLO1, RLO2, TLO1, TLO2	I_{LSO}	—	−2.0	—	mA
Sink Current at RLO1, RLO2, TLO1, TLO2	I_{LSK}	—	4.0	—	μA
CPR, CPT Output Resistance (I_{out} = 1.5 mA)	R_{CP}	—	35	—	Ω
CPR, CPT Leakage Current	I_{CPLK}	—	−0.2	—	μA
FILTER (T_A = +25°C)					
Voltage Offset at FO (V_{FO} − V_B, 220 kΩ from V_B to FI)	FO_{VOS}	−200	−90	0	mV
FO Sink Current	I_{FO}	150	260	400	μA
FI Bias Current	I_{FI}	—	−50	—	nA
SYSTEM DISTORTION (T_A = +25°C, f = 1.0 kHz)					
Rx Mode (From FI to RXO, FO connected to RXI)	THD_R	—	0.5	3.0	%
Tx Mode (From MCI to HTO−/HTO+, includes Tx attenuator)	THD_T	—	0.8	3.0	%

1. All currents into a device pin are positive, those out of a pin are negative. Algebraic convention rather than magnitude is used to define limits.

FIGURE 1 — HYBRID AMPLIFIER DISTORTION TEST



TEMPERATURE CHARACTERISTICS

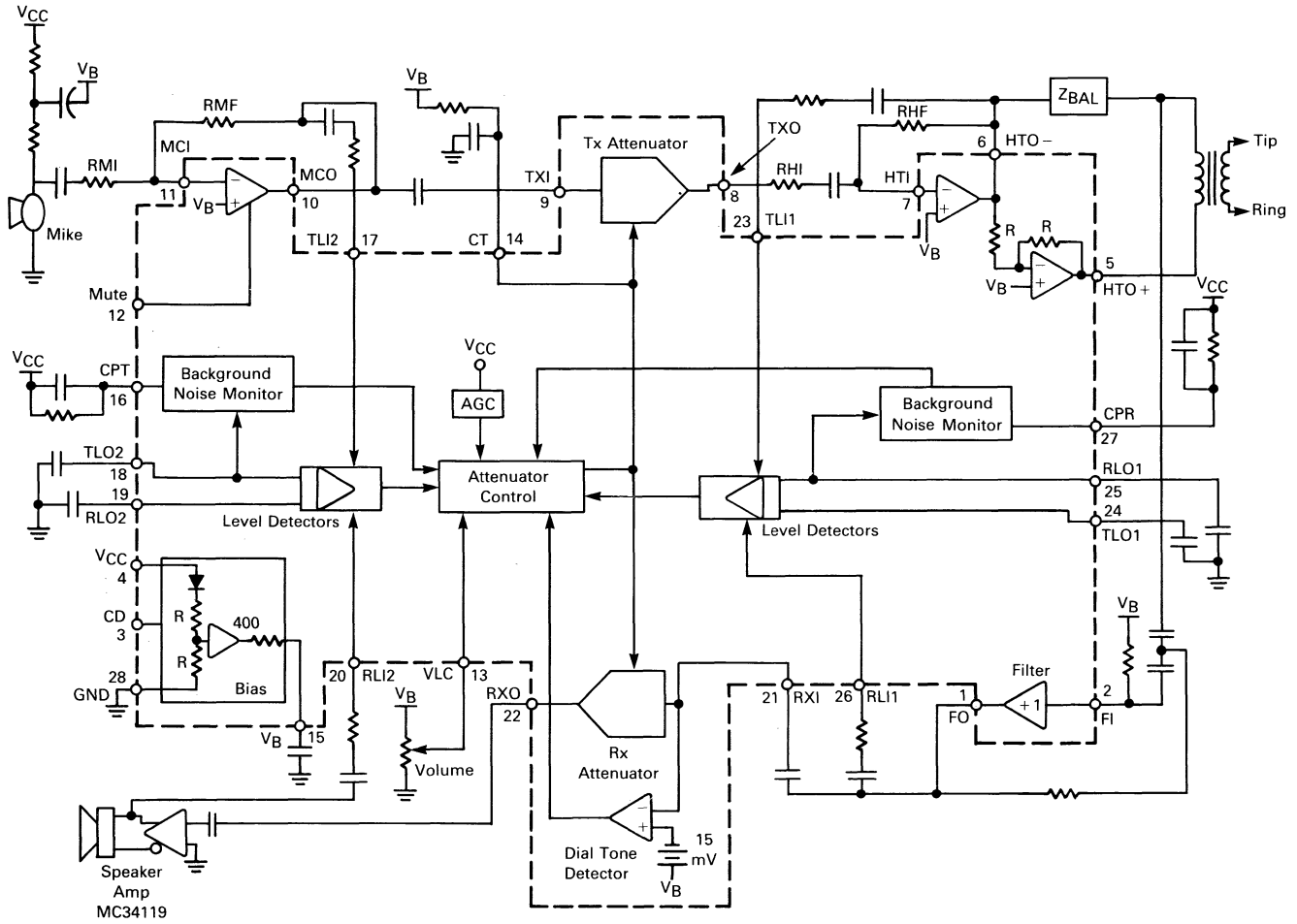
Parameter	Typical Value @ 25°C	Typical Change −20 to +60°C
V_{CC} Supply Current (CD = 0.8 V)	5.0 mA	−0.3 %/°C
V_{CC} Supply Current (CD = 2.0 V)	400 μA	−0.4 %/°C
V_B Output Voltage (V_{CC} = 5.0 V)	2.1 V	+0.8 %/°C
Attenuator Gain (Max Gain)	+6.0 dB	0.0008 dB/°C
Attenuator Gain (Max Attenuation)	−46 dB	0.004 dB/°C
Attenuator Input Resistance (@ TXI, RXI)	10 kΩ	+0.6 %/°C
Dial Tone Detector Threshold	15 mV	+20 μV/°C
CT Source, Sink Current	±60 μA	−0.15 %/°C
Microphone, Hybrid Amplifier Offset	0 mV	±4.0 μV/°C
Transmit-Receive Switching Threshold	1.0	±0.02 %/°C
Sink Current at RLO1, RLO2, TLO1, TLO2	4.0 μA	−10 nA/°C
Closed Loop Gain (HTO− to HTO+)	0 dB	0.001 %/°C

PIN DESCRIPTION

Pin	Name	Description
1	FO	Filter output. Output impedance is less than 50 ohms.
2	FI	Filter input. Input impedance is greater than 1.0 Mohm.
3	CD	Chip Disable. A logic low (<0.8 V) sets normal operation. A logic high (>2.0 V) disables the IC to conserve power. Input impedance is nominally 90 kΩ.
4	V_{CC}	A supply voltage of +2.8 to +6.5 volts is required, at ≈ 5.0 mA. As V_{CC} falls from 3.5 to 2.8 volts, an AGC circuit reduces the receive attenuator gain by ≈ 25 dB (when in the receive mode).
5	HTO+	Output of the second hybrid amplifier. The gain is internally set at −1.0 to provide a differential output, in conjunction with HTO−, to the hybrid transformer.
6	HTO−	Output of the first hybrid amplifier. The gain of the amp is set by external resistors.
7	HTI	Input and summing node for the first hybrid amplifier. DC level is ≈V_B.
8	TXO	Output of the transmit attenuator. DC level is approximately V_B.
9	TXI	Input to the transmit attenuator. Max. signal level is 350 mVrms. Input impedance is ≈10 kΩ.
10	MCO	Output of the microphone amplifier. The gain of the amplifier is set by external resistors.
11	MCI	Input and summing node of the microphone amplifier. DC level is ≈ V_B.
12	MUT	Mute input. A logic low (<0.8 V) sets normal operation. A logic high (>2.0 V) mutes the microphone amplifier without affecting the rest of the circuit. Input impedance is nominally 90 kΩ.
13	VLC	Volume control input. When VLC = V_B, the receive attenuator is at maximum gain when in the receive mode. When VLC = 0.3 V_B, the receive gain is down 35 dB. Does not affect the transmit mode.
14	C_T	An RC at this pin sets the response time for the circuit to switch modes.
15	V_B	An output voltage ≈V_{CC}/2. This voltage is a system ac ground, and biases the volume control. A filter cap is required.
16	CPT	An RC at this pin sets the time constant for the transmit background monitor.
17	TLI2	Input to the transmit level detector on the mike/speaker side.
18	TLO2	Output of the transmit level detector on the mike/speaker side, and input to the transmit background monitor.
19	RLO2	Output of the receive level detector on the mike/speaker side.
20	RLI2	Input to the receive level detector on the mike/speaker side.
21	RXI	Input to the receive attenuator and dial tone detector. Max input level is 350 mV RMS. Input impedance is ≈10 kΩ.
22	RXO	Output of the receive attenuator. DC level is approximately V_B.
23	TLI1	Input to the transmit level detector on the line side.
24	TLO1	Output of the transmit level detector on the line side.
25	RLO1	Output of the receive level detector on the line side, and input to the receive background monitor.
26	RLI1	Input to the receive level detector on the line side.
27	CPR	An RC at this pin sets the time constant for the receive background monitor.
28	GND	Ground pin for the entire IC.

Note: Pin numbers are identical for the DIP package and the SOIC package.

FIGURE 2 — MC34118 BLOCK DIAGRAM



INTRODUCTION

The fundamental difference between the operation of a speakerphone and a handset is that of half-duplex versus full-duplex. The handset is full duplex since conversation can occur in both directions (transmit and receive) simultaneously. A speakerphone has higher gain levels in both paths, and attempting to converse full duplex results in oscillatory problems due to the loop that exists within the system. The loop is formed by the receive and transmit paths, the hybrid, and the acoustic coupling (speaker to microphone). The only practical and economical solution used to date is to design the speakerphone to function in a half duplex mode — i.e., only one person speaks at a time, while the other listens. To achieve this requires a circuit which can detect who is talking, switch on the appropriate path (transmit or receive), and switch off (attenuate) the other path. In this way, the loop gain is maintained less than unity. When the talkers exchange function, the circuit must quickly detect this, and switch the circuit appropriately. By providing speech level detectors, the circuit operates in a "hands-free" mode, eliminating the need for a "push-to-talk" switch.

The handset, by the way, has the same loop as the speakerphone. But since the gains are considerably lower, and since the acoustic coupling from the earpiece to the mouthpiece is almost non-existent (the receiver is normally held against a person's ear), oscillations don't occur.

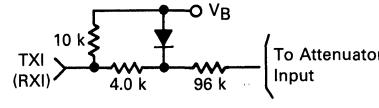
The MC34118 provides the necessary level detectors, attenuators, and switching control for a properly operating speakerphone. The detection sensitivity and timing are externally controllable. Additionally, the MC34118 provides background noise monitors which make the circuit insensitive to room and line noise, hybrid amplifiers for interfacing to Tip and Ring, the microphone amplifier, and other associated functions. Please refer to the Block Diagram (Figure 2) when reading the following sections.

ATTENUATORS

The transmit and receive attenuators are complementary in function, i.e., when one is at maximum gain (+6.0 dB), the other is at maximum attenuation (−46 dB), and vice versa. They are never both fully on or both fully off. The sum of their gains remains constant (within a nominal error band of ±0.1 dB) at a typical value of −40 dB (see Figure 10). Their purpose is to control the transmit and receive paths to provide the half-duplex operation required in a speakerphone.

The attenuators are non-inverting, and have a −3.0 dB (from max gain) frequency of ≈100 kHz. The input impedance of each attenuator (TXI and RXI) is nominally 10 kΩ (see Figure 3), and the input signal should be limited to 350 mVrms (990 mVp-p) to prevent distortion. That maximum recommended input signal is independent of the volume control setting. The diode clamp on the inputs limits the input swing, and therefore the maximum negative output swing. This is the reason for V_{RXOL} and V_{TXOL} specification being defined as they are in the Electrical Characteristics. The output impedance is <10 Ω until the output current limit (typically 2.5 mA) is reached.

FIGURE 3 — ATTENUATOR INPUT STAGE



The attenuators are controlled by the single output of the Control Block, which is measurable at the C_T pin (Pin 14). When the C_T pin is at +240 millivolts with respect to V_B, the circuit is in the receive mode (receive attenuator is at +6.0 dB). When the C_T pin is at −240 millivolts with respect to V_B, the circuit is in the transmit mode (transmit attenuator is at +6.0 dB). The circuit is in an idle mode when the C_T voltage is equal to V_B, causing the attenuators' gains to be halfway between their fully on and fully off positions (−20 dB each). Monitoring the C_T voltage (with respect to V_B) is the most direct method of monitoring the circuit's mode.

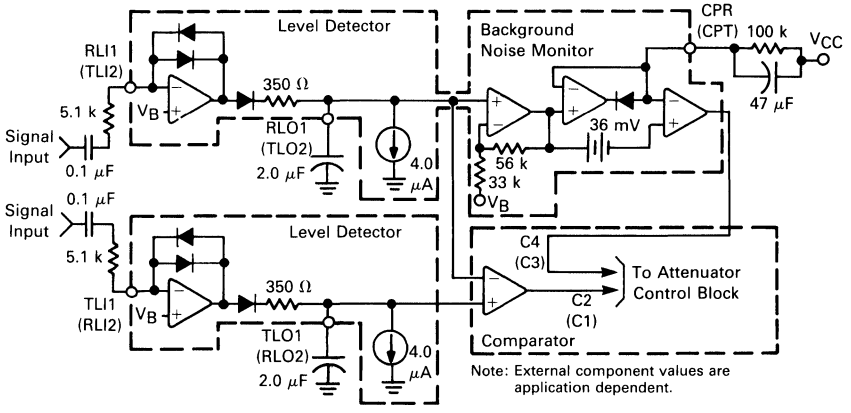
The inputs to the Control Block are seven: 2 from the comparators operated by the level detectors, 2 from the background noise monitors, the volume control, the dial-tone detector, and the AGC circuit. These seven inputs are described below.

LEVEL DETECTORS

There are four level detectors — two on the receive side and two on the transmit side. Refer to Figure 4 — the terms in parentheses form one system, and the other terms form the second system. Each level detector is a high gain amplifier with back-to-back diodes in the feedback path, resulting in non-linear gain, which permits operation over a wide dynamic range of speech levels. Refer to the graphs of Figures 11, 12 and 13 for their dc and ac transfer characteristics. The sensitivity of each level detector is determined by the external resistor and capacitor at each input (TLI1, TLI2, RLI1, and RLI2). Each output charges an external capacitor through a diode and limiting resistor, thus providing a dc representation of the input ac signal level. The outputs have a quick rise time (determined by the capacitor and an internal 350 Ω resistor), and a slow decay time set by an internal current source and the capacitor. The capacitors on the four outputs should have the same value (±10%) to prevent timing problems.

Referring to Figure 2, on the receive side, one level detector (RLI1) is at the receive input receiving the same

FIGURE 4 — LEVEL DETECTORS



signal as at Tip and Ring, and the other (RLI2) is at the output of the speaker amplifier. On the transmit side, one level detector (TLI2) is at the output of the microphone amplifier, while the other (TLI1) is at the hybrid output. Outputs RLO1 and TLO1 feed a comparator, the output of which goes to the Attenuator Control Block. Likewise, outputs RLO2 and TLO2 feed a second comparator which also goes to the Attenuator Control Block. The truth table for the effects of the level detectors on the Control Block is given in the section describing the Control Block.

BACKGROUND NOISE MONITORS

The purpose of the background noise monitors is to distinguish speech (which consists of bursts) from background noise (a relatively constant signal level). There are two background noise monitors — one for the receive path and one for the transmit path. Referring to Figure 4, the receive background noise monitor is operated on by the RLI1-RLO1 level detector, while the transmit background noise monitor is operated on by the TLI2-TLO2 level detector. They monitor the background noise by storing a dc voltage representative of the respective noise levels in capacitors at CPR and CPT. The voltages at these pins have slow rise times (determined by the external RC), but fast decay times. If the signal at RLI1 (or TLI2) changes slowly, the voltage at CPR (or CPT) will remain more positive than the voltage at the non-inverting input of the monitor's output comparator. When speech is present, the voltage on the non-inverting input of the comparator will rise quicker than the voltage at the inverting input (due to the burst characteristic of speech), causing its output to change. This output is sensed by the Attenuator Control Block.

The 36 mV offset at the comparator's input keeps the comparator from changing state unless the speech level exceeds the background noise by ≈4.0 dB. The time constant of the external RC (≈4.7 seconds) determines the response time to background noise variations.

VOLUME CONTROL

The volume control input at VLC (Pin 13) is sensed as a voltage with respect to V_B. The volume control affects the attenuators *only* in the receive mode. It has no effect in the idle or transmit modes.

When in the receive mode, the gain of the receive attenuator will be +6.0 dB, and the gain of the transmit attenuator will be −46 dB only when VLC is equal to V_B. As VLC is reduced below V_B, the gain of the receive attenuator is reduced (see Figure 14), and the gain of the transmit attenuator is increased such that their sum remains constant. Changing the voltage at VLC changes the voltage at C_T (see the Attenuator Control Block section), which in turn controls the attenuators.

The volume control setting does not affect the maximum attenuator input signal at which noticeable distortion occurs.

The bias current at VLC is typically 60 nA out of the pin, and does not vary significantly with the VLC voltage or with V_{CC}.

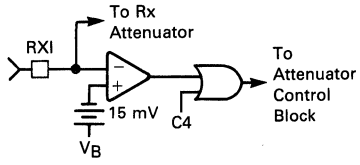
DIAL TONE DETECTOR

The dial tone detector is a comparator with one side connected to the receive input (RXI) and the other input connected to V_B with a 15 mV offset (see Figure 5). If the circuit is in the receive mode, and the incoming signal is greater than 15 mV (10 mVrms), the comparator's output will change, disabling the receive idle mode. The receive attenuator will then be at a setting determined solely by the volume control.

The purpose of this circuit is to prevent the dial tone

(which would be considered as continuous noise) from fading away as the circuit would have the tendency to switch to the idle mode. By disabling the receive idle mode, the dial tone remains at the normally expected full level.

FIGURE 5 — DIAL TONE DETECTOR



2

AGC

The AGC circuit affects the circuit only in the receive mode, and only when the supply voltage (V_{CC}) is less than 3.5 volts. As V_{CC} falls below 3.5 volts, the gain of the receive attenuator is reduced according to the graph of Figure 15. The transmit path attenuation changes such that the sum of the transmit and receive gains remains constant.

The purpose of this feature is to reduce the power (and current) used by the speaker when a line-powered speakerphone is connected to a long line, where the available power is limited. By reducing the speaker power, the voltage sag at V_{CC} is controlled, preventing possible erratic operation.

ATTENUATOR CONTROL BLOCK

The Attenuator Control Block has the seven inputs described above:

— The output of the comparator operated by RLO2 and TLO2 (microphone/speaker side) — designated C1.
— The output of the comparator operated by RLO1 and TLO1 (Tip/Ring side) — designated C2.
— The output of the transmit background noise monitor — designated C3.
— The output of the receive background noise monitor — designated C4.
— The volume control.
— The dial tone detector.
— The AGC circuit.

The single output of the Control Block controls the two attenuators. The effect of C1–C4 is as follows:

Inputs				Output
C1	C2	C3	C4	Mode
Tx	Tx	1	X	Transmit
Tx	Rx	y	y	Fast Idle
Rx	Tx	y	y	Fast Idle
Rx	Rx	X	1	Receive
Tx	Tx	0	X	Slow Idle
Tx	Rx	0	0	Slow Idle
Rx	Tx	0	0	Slow Idle
Rx	Rx	X	0	Slow Idle

X = Don't Care; y = C3 and C4 are not both 0.

A definition of the above terms:

1) "Transmit" means the transmit attenuator is fully on (+6.0 dB), and the receive attenuator is at max. attenuation (−46 dB).
2) "Receive" means both attenuators are controlled by the volume control. At max. volume, the receive attenuator is fully on (+6.0 dB), and the transmit attenuator is at max. attenuation (−46 dB).
3) "Fast Idle" means both transmit and receive speech are present in approximately equal levels. The attenuators are quickly switched (30 ms) to idle until one speech level dominates the other.
4) "Slow Idle" means speech has ceased in both transmit and receive paths. The attenuators are then slowly switched (1 second) to the idle mode.
5) Switching to the full transmit or receive modes from any other mode is at the fast rate (≈30 ms).

A summary of the truth table is as follows:

1) The circuit will switch to transmit if: a) *both* transmit level detectors sense higher signal levels relative to the respective receive level detectors (TLI1 versus RLI1, TLI2 versus RLI2), *and* b) the transmit background noise monitor indicates the presence of speech.

2) The circuit will switch to receive if: a) *both* receive level detectors sense higher signal levels relative to the respective transmit level detectors, *and* b) the receive background noise monitor indicates the presence of speech.

3) The circuit will switch to the fast idle mode if the level detectors *disagree* on the relative strengths of the signal levels, *and* at least one of the background noise monitors indicates speech. For example, referring to the Block Diagram (Figure 2), if there is sufficient signal at the microphone amp output (TLI2) to override the speaker signal (RLI2), *and* there is sufficient signal at the receive input (RLI1) to override the signal at the hybrid output (TLI1), *and* either or both background monitors indicate speech, then the circuit will be in the fast idle mode. Two conditions which can cause the fast idle mode to occur are a) when both talkers are attempting to gain control of the system by talking at the same time, and b) when one talker is in a very noisy environment, forcing the other talker to continually override that noise level. In general, the fast idle mode will occur infrequently.

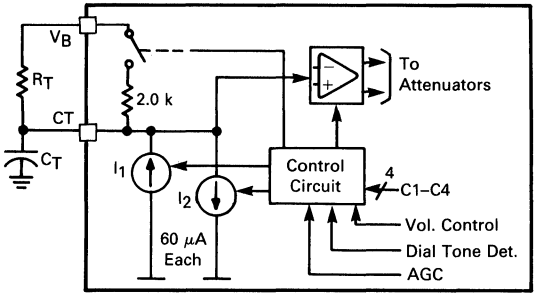
4) The circuit will switch to the slow idle mode when a) both talkers are quiet (no speech present), or b) when one talker's speech level is continuously overriden by noise at the other speaker's location.

The time required to switch the circuit between transmit, receive, fast idle and slow idle is determined in part by the components at the C_T pin (Pin 14). (See the section on Switching Times for a more complete explanation of the switching time components.) A schematic of the C_T circuitry is shown in Figure 6, and operates as follows:

— R_T is typically 120 kΩ, and C_T is typically 5.0 μF.
— To switch to the receive mode, I_1 is turned on (I_2 is off), charging the external capacitor to +240 mV above V_B. (An internal clamp prevents further charging of the capacitor.)
— To switch to the transmit mode, I_2 is turned on (I_1 is off) bringing down the voltage on the capacitor to −240 mV with respect to V_B.

— To switch to idle quickly (fast idle), the current sources are turned off, and the internal 2.0 kΩ resistor is switched in, discharging the capacitor to V_B with a time constant = 2.0 k x C_T.
— To switch to idle slowly (slow idle), the current sources are turned off, the switch at the 2.0 kΩ resistor is open, and the capacitor discharges to V_B through the external resistor R_T with a time constant = R_T x C_T.

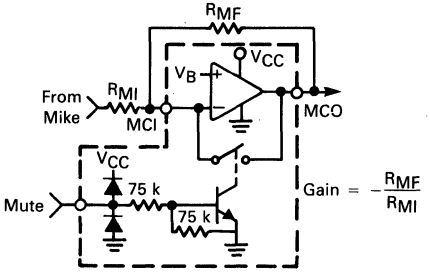
FIGURE 6 — CT ATTENUATOR CONTROL BLOCK CIRCUIT



MICROPHONE AMPLIFIER

The microphone amplifier (Pins 10, 11) has the noninverting input internally connected to V_B, while the inverting input and the output are pinned out. Unlike most op-amps, the amplifier has an all-NPN output stage, which maximizes phase margin and gain-bandwidth. This feature ensures stability at gains less than unity, as well as with a wide range of reactive loads. The open loop gain is typically 80 dB (f <100 Hz), and the gain-bandwidth is typically 1.0 MHz (See Figure 16). The maximum p-p output swing is typically 1.0 volt less than V_{CC} with an output impedance of <10 Ω until current limiting is reached (typically 1.5 mA). Input bias current at MCI is typically 40 nA out of the pin.

FIGURE 7 — MICROPHONE AMPLIFIER AND MUTE



The muting function (Pin 12), when activated, will reduce the gain of the amplifier to ≈ −39 dB (with RMI = 5.1 kΩ) by shorting the output to the inverting input (see Figure 7). The mute input has a threshold of ≈1.5 volts, and the voltage at this pin must be kept within the range of ground and V_{CC} (see Figure 17). If the mute function is not used, the pin should be grounded.

HYBRID AMPLIFIERS

The two hybrid amplifiers (at HTO +, HTO −, and HTI), in conjunction with an external transformer, provide the two-to-four wire converter for interfacing to the telephone line. The gain of the first amplifier (HTI to HTO −) is set by external resistors (gain = $-R_{HF}/R_{HI}$ in Figure 2), and its output drives the second amplifier, the gain of which is internally set at −1.0. Unlike most op-amps, the amplifiers have an all-NPN output stage, which maximizes phase margin and gain-bandwidth. This feature ensures stability at gains less than unity, as well as with a wide range of reactive loads. The open loop gain of the first amplifier is typically 80 dB, and the gain bandwidth of each amplifier is ≈1.0 MHz (see Figure 16). The maximum p-p output swing of each amplifier is typically 1.2 volts less than V_{CC} with an output impedance of <10 Ω until current limiting is reached (typically 8.0 mA). The output current capability is guaranteed to be a minimum of 5.0 mA. The bias current at HTI is typically 30 nA out of the pin.

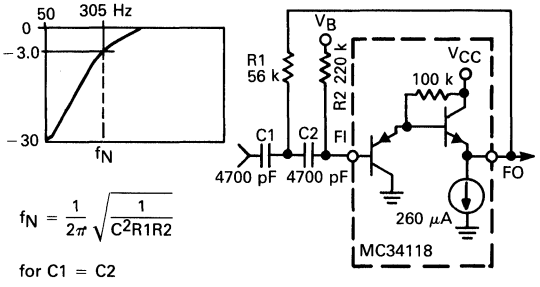
The connections to the coupling transformer are shown in the Block Diagram (Figure 2). The block labeled ZBal is the balancing network necessary to match the line impedance.

FILTER

The operation of the filter circuit is determined by the external components. The circuit within the MC34118, from pins FI to FO is a buffer with a high input impedance (>1.0 MΩ), and a low output impedance (<50 Ω). The configuration of the external components determines whether the circuit is a high-pass filter (as shown in Figure 2), a low-pass filter, or a band-pass filter.

As a high pass filter, with the components shown in Figure 8, the filter will keep out 60 Hz (and 120 Hz) hum which can be picked up by the external telephone lines.

FIGURE 8 — HIGH PASS FILTER



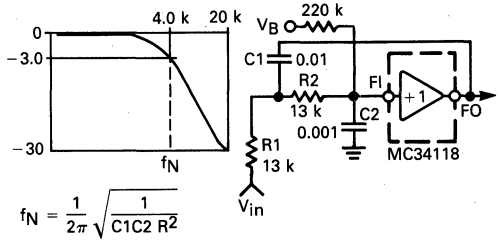
$$f_N = \frac{1}{2\pi}\sqrt{\frac{1}{C^2R1R2}}$$

for C1 = C2

As a low pass filter (Figure 9), it can be used to roll off the high end frequencies in the receive circuit, which aids in protecting against acoustic feedback problems.

With an appropriate choice of an input coupling capacitor to the low pass filter, a band pass filter is formed.

FIGURE 9 — LOW PASS FILTER



$$f_N = \frac{1}{2\pi}\sqrt{\frac{1}{C1C2\,R^2}}$$

for R1 = R2

POWER SUPPLY, V_B, AND CHIP DISABLE

The power supply voltage at V_{CC} (Pin 4) is to be between 3.5 and 6.5 volts for normal operation, with reduced operation possible down to 2.8 volts (see Figure 15 and the AGC section). The power supply current is shown in Figure 18 for both the power-up and power-down mode.

The output voltage at V_B (Pin 15) is $\approx(V_{CC} - 0.7)/2$, and provides the ac ground for the system. The output impedance at V_B is $\approx$400 Ω (see Figure 19), and in conjunction with the external capacitor at V_B, forms a low pass filter for power supply rejection. Figure 20 indicates the amount of rejection with different capacitors. The choice of capacitor is application dependent based on whether the circuit is powered by the telephone line or a power supply.

Since V_B biases the microphone and hybrid amplifiers, the amount of supply rejection at their outputs is directly related to the rejection at V_B, as well as their respective gains. Figure 21 depicts this graphically.

The Chip Disable (Pin 3) permits powering down the IC to conserve power and/or for muting purposes. With CD ≤0.8 volts, normal operation is in effect. With CD ≥2.0 volts and ≤V_{CC}, the IC is powered down. In the powered down mode, the microphone and the hybrid amplifiers are disabled, and their outputs go to a high impedance state. Additionally, the bias is removed from the level detectors. The bias is not removed from the filter (Pins 1, 2), the attenuators (Pins 8, 9, 21, 22), or from Pins 13, 14, and 15 (the attenuators are disabled, however, and will not pass a signal). The input impedance at CD is typically 90 kΩ, has a threshold of ≈1.5 volts, and the voltage at this pin must be kept within the range of ground and V_{CC} (see Figure 17). If CD is not used, the pin should be grounded.

FIGURE 10 — ATTENUATOR GAIN versus V_{CT} (PIN 14)

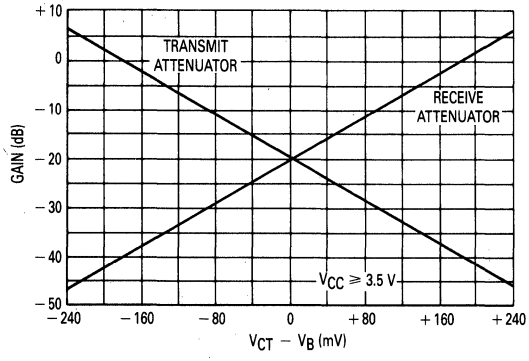


FIGURE 11 — LEVEL DETECTOR DC TRANSFER CHARACTERISTICS

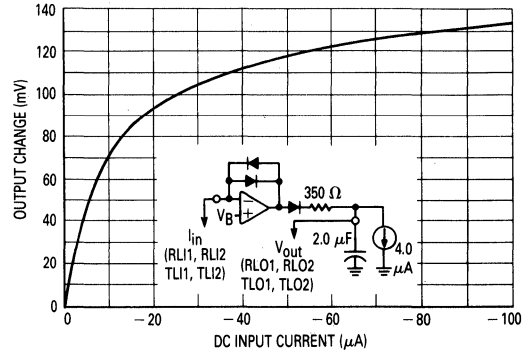


FIGURE 12 — LEVEL DETECTOR AC TRANSFER CHARACTERISTICS

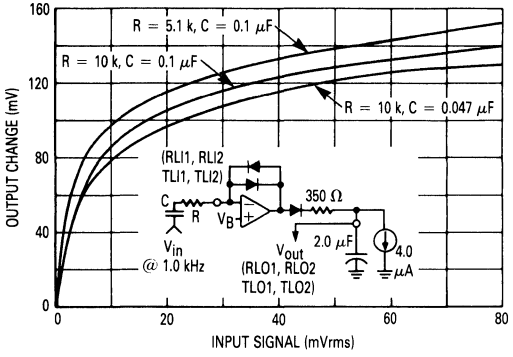


FIGURE 13 — LEVEL DETECTOR AC TRANSFER CHARACTERISTICS versus FREQUENCY

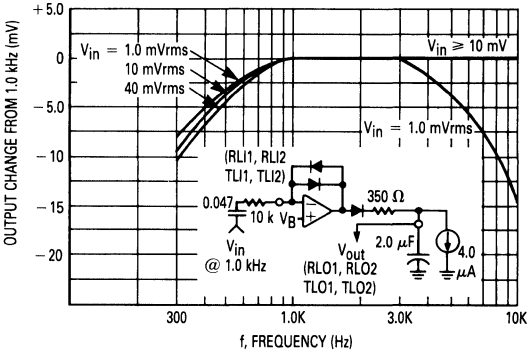


FIGURE 14 — RECEIVE ATTENUATOR versus VOLUME CONTROL

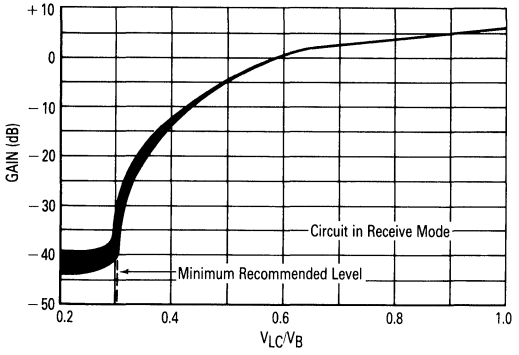


FIGURE 15 — RECEIVE ATTENUATION GAIN versus V_{CC}

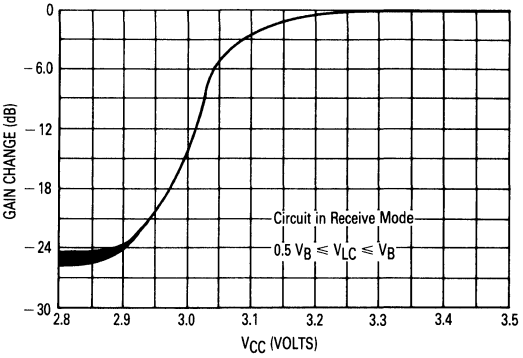


FIGURE 16 — MICROPHONE AMPLIFIER AND 1ST HYBRID AMPLIFIER OPEN LOOP GAIN AND PHASE

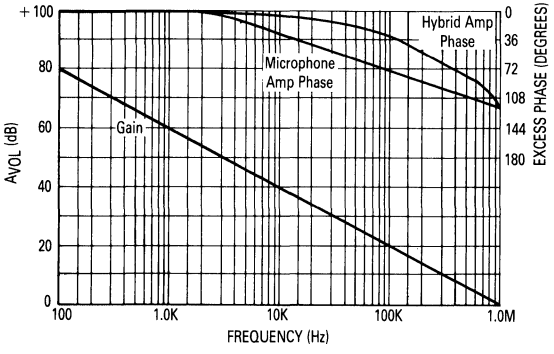
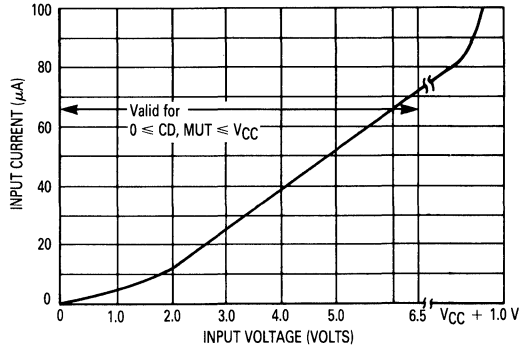


FIGURE 17 — INPUT CHARACTERISTICS @ CD, MUT



2

FIGURE 18 — SUPPLY CURRENT versus SUPPLY VOLTAGE

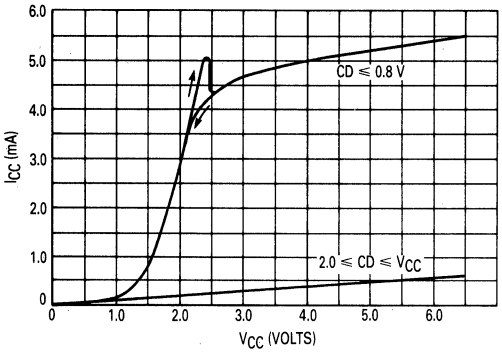


FIGURE 19 — V_B OUTPUT CHARACTERISTICS

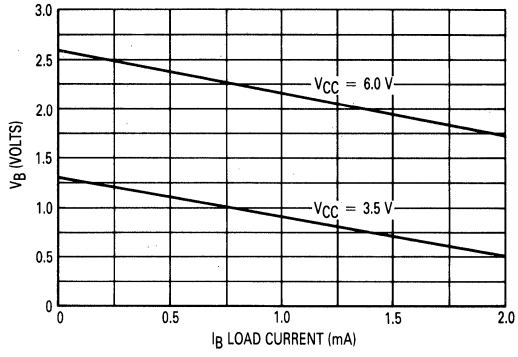


FIGURE 20 — V_B POWER SUPPLY REJECTION versus FREQUENCY AND V_B CAPACITOR

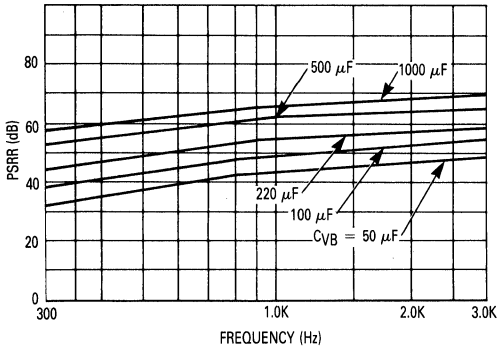


FIGURE 21 — POWER SUPPLY REJECTION OF THE MICROPHONE AND HYBRID AMPLIFIERS

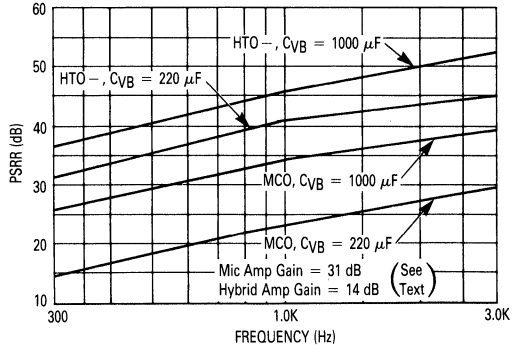
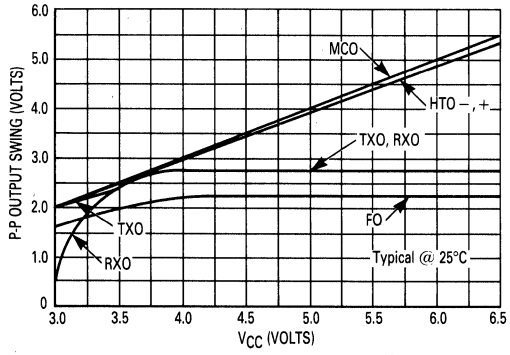


FIGURE 22 — TYPICAL OUTPUT SWING versus V_{CC}



DESIGN GUIDELINES

SWITCHING TIME

The switching time of the MC34118 circuit is dominated by the components at C_T (Pin 14, refer to Figure 6), and secondarily by the capacitors at the level detector outputs (RLO1, RLO2, TLO1, TLO2).

The time to switch to receive or to transmit from idle is determined by the capacitor at C_T, together with the internal current sources (refer to Figure 6). The switching time is:

$$\Delta T = \frac{\Delta V \times C_T}{I}$$

For the typical case where ΔV = 240 mV, I = 60 μA, and C_T is 5.0 μF, ΔT = 20 ms. If the circuit switches directly from receive to transmit (or vice-versa), the total switching time would be 40 ms.

The switching time from either receive or transmit to idle depends on which type of idle mode is in effect. If the circuit is going to "fast idle," the time constant is determined by the C_T capacitor, and the internal 2.0 kΩ resistor (Figure 6). With C_T = 5.0 μF, the time constant is $\approx$10 ms, giving a switching time to idle of $\approx$30 ms (for 95% change). Fast idle is an infrequent occurrence, however, occurring when both speakers are talking and competing for control of the circuit. The switching time from idle back to either transmit or receive is described above.

If the circuit is switching to "slow idle," the time constant is determined by the C_T capacitor and R_T, the external resistor (see Figure 6). With C_T = 5.0 μF, and R_T = 120 kΩ, the time constant is $\approx$600 ms, giving a switching time of $\approx$1.8 seconds (for 95% change). The switching period to slow idle begins when both speakers have stopped talking. The switching time back to the original mode will depend on how soon that speaker begins speaking again. The sooner the speaking starts during the 1.8 second period, the quicker the switching time since a smaller voltage excursion is required. That switching time is determined by the internal current sources as described above.

The above switching times occur, however, after the level detectors have detected the appropriate signal levels, since their outputs operate the Attenuator Control Block. Referring to Figure 4, the rise time of the level detectors' outputs to new speech is quick by comparison ($\approx$1.0 ms), determined by the internal 350 Ω resistor and the external capacitor (typically 2.0 μF). The output's decay time is determined by the external capacitor, and an internal 4.0 μA current source giving a decay rate of $\approx$60 ms for a 120 mV excursion at RLO or TLO. However, the overall response time of the circuit is not a constant since it depends on the relative strength of the signals at the different level detectors, as well as the timing of the signals with respect to each other. The capacitors at the four outputs (RLO1, RLO2, TLO1, TLO2) must be equal value ($\pm$10%) to prevent problems in timing and level response.

The rise time of the level detector's outputs is not significant since it is so short. The decay time, however, provides a significant part of the "hold time" necessary to hold the circuit during the normal pauses in speech.

The components at the inputs of the level detectors (RLI1, RLI2, TLI1, TLI2) do not affect the switching time, but rather affect the relative signal levels required to switch the circuit, as well as the frequency response of the detectors.

DESIGN EQUATIONS

Referring to Figure 24 (the coupling capacitors have been omitted for simplicity), and the circuit of Figure 23, the following definitions will be used (all measurements are at 1.0 kHz):

- G_{MA} is the gain of the microphone amplifier measured from the microphone output to TXI (typically 35 V/V, or 31 dB);
- G_{TX} is the gain of the transmit attenuator, measured from TXI to TXO;
- G_{HA} is the gain of hybrid amplifiers, measured from TXO to the HTO−/HTO+ differential output (typically 10.2 V/V, or 20.1 dB);
- G_{HT} is the gain from HTO−/HTO+ to Tip/Ring for transmit signals, and includes the balance network (measured at 0.4 V/V, or −8.0 dB);
- G_{ST} is the sidetone gain, measured from HTO−/HTO+ to the filter input (measured at 0.18 V/V, or −15 dB);
- G_{HR} is the gain from Tip/Ring to the filter input for receive signals (measured at 0.833 V/V or −1.6 dB);
- G_{FO} is the gain of the filter stage, measured from the input of the filter to RXI, typically 0 dB at 1.0 kHz;
- G_{RX} is the gain of the receive attenuator measured from RXI to RXO;
- G_{SA} is the gain of the speaker amplifier, measured from RXO to the differential output of the MC34119 (typically 22 V/V or 26.8 dB);
- G_{AC} is the acoustic coupling, measured from the speaker differential voltage to the microphone output voltage.

I) Transmit Gain

The transmit gain, from the microphone output (V_M) to Tip and Ring, is determined by the output characteristics of the microphone, and the desired transmit level. For example, a typical electret microphone will produce $\approx$0.35 mVrms under normal speech conditions. To achieve 100 mVrms at Tip/Ring, an overall gain of 285 V/V is necessary. The gain of the transmit attenuator is fixed at 2.0 (+6.0 dB), and the gain through the hybrid of Figure 23 (G_{HT}) is nominally 0.4 (−8.0 dB). Therefore a gain of 357 V/V is required of the microphone and hybrid amplifiers. It is desirable to have the majority of that gain in the microphone amplifier for three reasons: 1) the low level signals from the microphone should be amplified as soon as possible to minimize signal/noise

FIGURE 23 — MC34118 APPLICATION CIRCUIT (BASIC LINE POWERED SPEAKERPHONE)

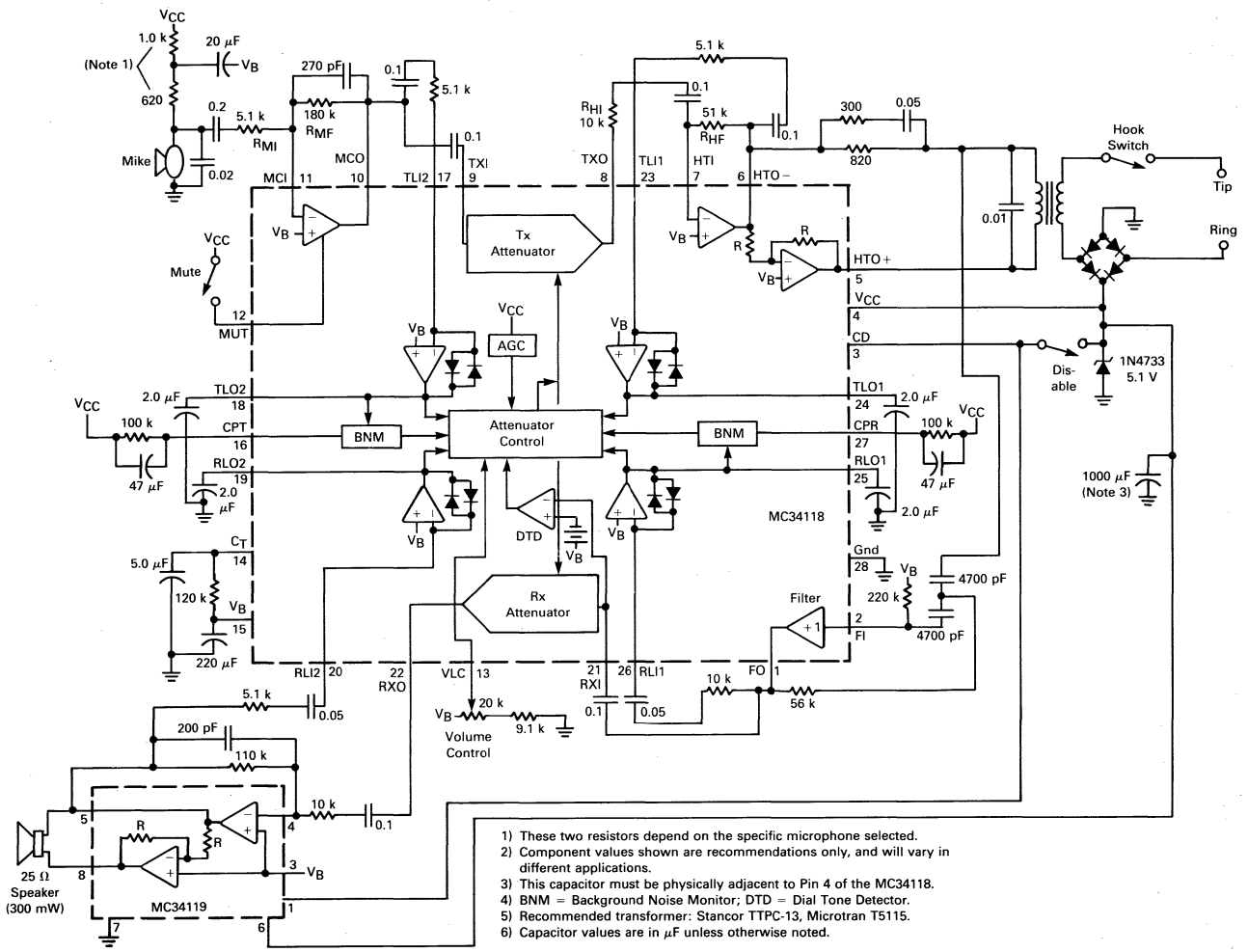
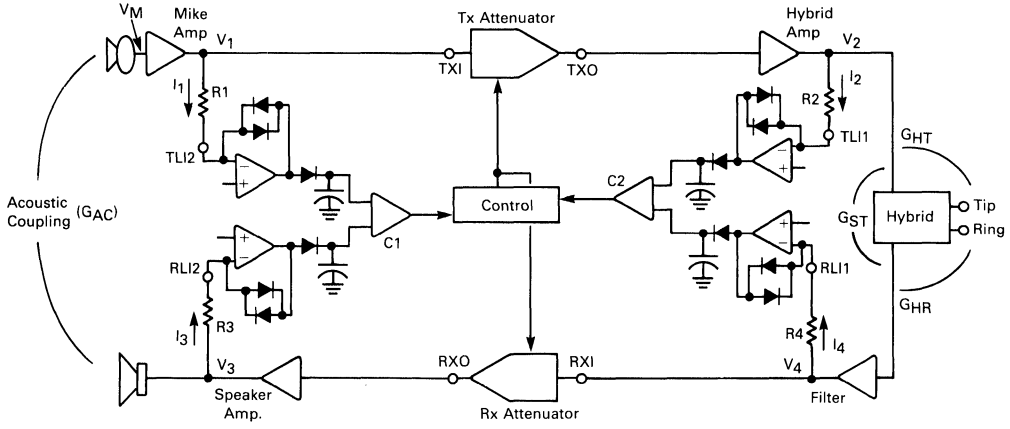


FIGURE 24 — BASIC BLOCK DIAGRAM FOR DESIGN PURPOSES



problems; 2) to provide a reasonable signal level to the TLI2 level detector; and 3) to minimize any gain applied to broadband noise generated within the attenuator. However, to cover the normal voiceband, the microphone amplifier's gain should not exceed 48 dB (see Figure 16). For the circuit of Figure 23, the gain of the microphone amplifier was set at 35 V/V (31 dB), and the differential gain of the hybrid amplifiers was set at 10.2 V/V (20.1 dB).

II) Receive Gain

The overall receive gain depends on the incoming signal level, and the desired output power at the speaker. Nominal receive levels (independent of the peaks) at Tip/Ring can be 35 mVrms (−27 dBm), although on long lines that level can be down to 8.0 mVrms (−40 dBm). The speaker power is:

$$P_{SPK} = \frac{10^{dBm/10} \times 0.6}{R_S} \qquad \text{(Equation 1)}$$

where R_S is the speaker impedance, and the dBm term is the incoming signal level increased by the gain of the receive path. Experience has shown that ≈30 dB gain is a satisfactory amount for the majority of applications. Using the above numbers and Equation 1, it would appear that the resulting power to the speaker is extremely low. However, Equation 1 does not consider the peaks in normal speech, which can be 10 to 15 times the rms value. Considering the peaks, the overall average power approaches 20–30 mW on long lines, and much more on short lines.

Referring to Figure 23, the gain from Tip/Ring to the filter input was measured at 0.833 V/V (−1.6 dB), the filter's gain is unity, and the receive attenuator's gain is 2.0 V/V (+6.0 dB) at maximum volume. The speaker amplifier's gain is set at 22 V/V (26.8 dB), which puts the overall gain at ≈31.2 dB.

III) Loop Gain

The total loop gain (of Figure 24) must add up to less than zero dB to obtain a stable circuit. This can be expressed as:

$$G_{MA} + G_{TX} + G_{HA} + G_{ST} + G_{FO} + G_{RX} + G_{SA} + G_{AC} < 0 \qquad \text{(Equation 2)}$$

Using the typical numbers mentioned above, and knowing that $G_{TX} + G_{RX} = -40$ dB, the required acoustic coupling can be determined:

$$G_{AC} < -[31 + 20.1 + (-15) + 0 + (-40) + 26.8] = -22.9 \text{ dB}. \qquad \text{(Equation 3)}$$

An acoustic loss of at least 23 dB is necessary to prevent instability and oscillations, commonly referred to as "singing." However, the following equations show that greater acoustic loss is necessary to obtain proper level detection and switching.

IV) Switching Thresholds

To switch comparator C1, currents I_1 and I_3 need to be determined. Referring to Figure 24, with a receive signal V_L applied to Tip/Ring, a current I_3 will flow through R3 into RLI2 according to the following equation:

$$I_3 = \frac{V_L}{R3}\left[G_{HR} \times G_{FO} \times G_{RX} \times \frac{G_{SA}}{2}\right] \qquad \text{(Equation 4)}$$

where the terms in the brackets are the V/V gain terms. The speaker amplifier gain is divided by two since G_{SA} is the differential gain of the amplifier, and V_3 is obtained from one side of that output. The current I_1, coming from the microphone circuit, is defined by:

$$I_1 = \frac{V_M \times G_{MA}}{R1} \qquad \text{(Equation 5)}$$

where V_M is the microphone voltage. Since the switching threshold occurs when $I_1 = I_3$, combining the above two equations yields:

$$V_M = V_L \times \frac{R1}{R3} \frac{[G_{HR} \times G_{FO} \times G_{RX} \times G_{SA}]}{G_{MA} \times 2} \qquad \text{(Equation 6)}$$

This is the general equation defining the microphone voltage necessary to switch comparator C1 when a receive signal V_L is present. The highest V_M occurs when the receive attenuator is at maximum gain (+6.0 dB). Using the typical numbers for Equation 6 yields:

$$V_M = 0.52\ V_L \qquad \text{(Equation 7)}$$

To switch comparator C2, currents I_2 and I_4 need to be determined. With sound applied to the microphone, a voltage V_M is created by the microphone, resulting in a current I_2 into TLI1:

$$I_2 = \frac{V_M}{R2}\left[G_{MA} \times G_{TX} \times \frac{G_{HA}}{2}\right] \qquad \text{(Equation 8)}$$

Since G_{HA} is the differential gain of the hybrid amplifiers, it is divided by two to obtain the voltage V_2 applied to R2. Comparator C2 switches when $I_4 = I_2$. I_4 is defined by:

$$I_4 = \frac{V_L}{R4}[G_{HR} \times G_{FO}] \qquad \text{(Equation 9)}$$

Setting $I_4 = I_2$, and combining the above equations results in:

$$V_L = V_M \times \frac{R4}{R2} \times \frac{[G_{MA} \times G_{TX} \times G_{HA}]}{[G_{HR} \times G_{FO} \times 2]} \qquad \text{(Equation 10)}$$

This equation defines the line voltage at Tip/Ring necessary to switch comparator C2 in the presence of a microphone voltage. The highest V_L occurs when the circuit is in the transmit mode (G_{TX} = +6.0 dB). Using the typical numbers for Equation 10 yields:

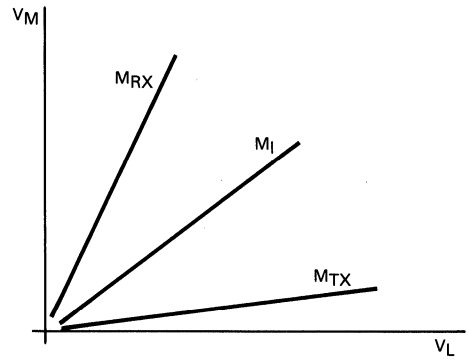
$$V_L = 840\ V_M \quad (\text{or } V_M = 0.0019\ V_L) \qquad \text{(Equation 11)}$$

At idle, where the gain of the two attenuators is −20 dB (0.1 V/V), Equations 6 and 10 yield the same result:

$$V_M = 0.024\ V_L \qquad \text{(Equation 12)}$$

Equations 7, 11, and 12 define the thresholds for switching, and are represented in the following graph:

FIGURE 25 — SWITCHING THRESHOLDS



The "M" terms are the slopes of the lines (0.52, 0.024, and 0.0019) which are the coefficients of the three equations. The M_{RX} line represents the receive to transmit threshold in that it defines the microphone signal level necessary to switch to transmit in the presence of a given receive signal level. The M_{TX} line represents the transmit to receive threshold. The M_I line represents the idle condition, and defines the threshold level on one side (transmit or receive) necessary to overcome noise on the other.

Some comments on the above graph:

— Acoustic coupling and sidetone coupling were not included in Equations 7 and 12. Those couplings will affect the actual performance of the final speakerphone due to their interaction with speech at the microphone, and the receive signal coming in at Tip/Ring. The effects of those couplings are difficult to predict due to their associated phase shifts and frequency response. In some cases the coupling signal will add, and other times subtract from the incoming signal. The physical design of the speakerphone enclosure, as well as the specific phone line to which it is connected, will affect the acoustic and sidetone couplings, respectively.

— The M_{RX} line helps define the maximum acoustic coupling allowed in a system, which can be found from the following equation:

$$G_{AC\text{-}MAX} = \frac{R1}{2 \times R3 \times G_{MA}} \qquad \text{(Equation 13)}$$

Equation 13 is independent of the volume control setting. Conversely, the acoustic coupling of a designed system helps determine the minimum slope of that line. Using the component values of Figure 23 in Equation

13 yields a $G_{AC\text{-}MAX}$ of −37 dB. Experience has shown, however, that an acoustic coupling loss of >40 dB is desirable.

— The M_{TX} line helps define the maximum sidetone coupling (G_{ST}) allowed in the system, which can be found from the following equation:

$$G_{ST} = \frac{R4}{2 \times R2 \times G_{FO}} \qquad \text{(Equation 14)}$$

Using the component values of Figure 23 in Equation 14 yields a maximum sidetone of 0 dB. Experience has shown, however, that a minimum of 6.0 dB loss is preferable.

The above equations can be used to determine the resistor values for the level detector inputs. Equation 6 can be used to determine the R1/R3 ratio, and Equation 10 can be used to determine the R4/R2 ratio. In Figure 24, R1–R4 each represent the combined impedance of the resistor and coupling capacitor at each level detector input. The magnitude of each RC's impedance should be kept within the range of 2.0 k–15 kΩ in the voiceband (due to the typical signal levels present) to obtain the best performance from the level detectors. The specific R and C at each location will determine the frequency response of that level detector.

APPLICATION INFORMATION

DIAL TONE DETECTOR

The threshold for the dial tone detector is internally set at 15 mV (10 mVrms) below V_B (see Figure 5). That threshold can be reduced by connecting a resistor from RXI to ground. The resistor value is calculated from:

$$R = 10\text{ k}\left[\frac{V_B}{\Delta V} - 1\right]$$

where V_B is the voltage at Pin 15, and ΔV is the amount of threshold reduction. By connecting a resistor from V_{CC} to RXI, the threshold can be increased. The resistor value is calculated from:

$$R = 10\text{ k}\left[\frac{V_{CC} - V_B}{\Delta V} - 1\right]$$

where ΔV is the amount of the threshold increase.

BACKGROUND NOISE MONITORS

For testing or circuit analysis purposes, the transmit or receive attenuators can be set to the "on" position, by disabling the background noise monitors, and applying a signal so as to activate the level detectors. Grounding the CPR pin will disable the receive background noise monitor, thereby indicating the "presence of speech" to the attenuator control block. Grounding CPT does the same for the transmit path.

Additionally, the receive background noise monitor is automatically disabled by the dial tone detector whenever the receive signal exceeds the detector's threshold.

TRANSMIT/RECEIVE DETECTION PRIORITY

Although the MC34118 was designed to have an idle mode such that the attenuators are halfway between their full on and full off positions, the idle mode can be biased towards the transmit or the receive side. With this done, gaining control of the circuit from idle will be easier for that side towards which it is biased since that path will have less attenuation at idle.

By connecting a resistor from C_T (Pin 14) to ground, the circuit will be biased towards the transmit side. The resistor value is calculated from:

$$R = R_T\left[\frac{V_B}{\Delta V} - 1\right]$$

where R is the added resistor, R_T is the resistor normally between Pins 14 and 15 (typically 120 kΩ), and ΔV is the difference between V_B and the voltage at C_T at idle (refer to Figure 10).

By connecting a resistor from C_T (Pin 14) to V_{CC}, the circuit will be biased towards the receive side. The resistor value is calculated from:

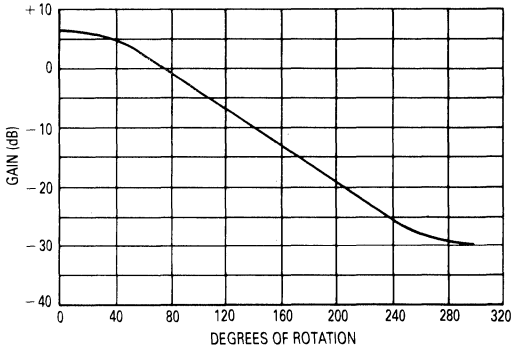
$$R = R_T\left[\frac{V_{CC} - V_B}{\Delta V} - 1\right]$$

R, R_T, and ΔV are the same as above. Switching time will be somewhat affected in each case due to the different voltage excursions required to get to transmit and receive from idle. For practical considerations, the ΔV shift should not exceed 100 mV.

VOLUME CONTROL

If a potentiometer with a standard linear taper is used for the volume control, the graph of Figure 14 indicates that the receive gain will not vary in a linear manner with respect to the pot's position. In situations where this may be objectionable, a potentiometer with an audio taper (commonly used in radio volume controls) will provide a more linear relationship as indicated in Figure 26. The slight non-linearity at each end of the graph is due to the physical construction of the potentiometer, and will vary among different manufacturers.

FIGURE 26 — RECEIVE ATTENUATOR GAIN versus POTENTIOMETER POSITION USING AUDIO TAPER



APPLICATION CIRCUIT

The circuit of Figure 23 is a basic speakerphone, to be used in parallel with any other telephone which con-

tains the ringer, dialer, and handset functions. The circuit is powered entirely by the telephone line's loop current, and its characteristics are shown in Figures 27–30.

FIGURE 27 — DC V-I CHARACTERISTICS

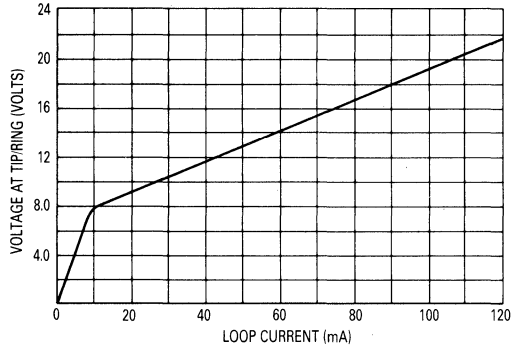


FIGURE 28 — AC TERMINATION IMPEDANCE

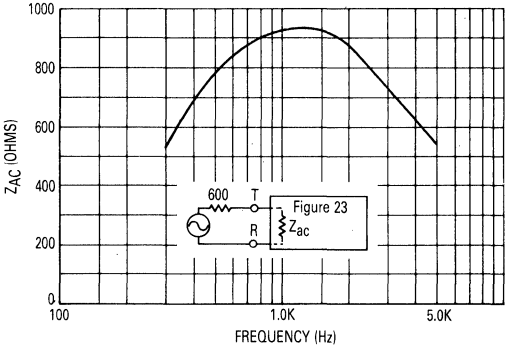


FIGURE 29 — TRANSMIT GAIN — MICROPHONE TO TIP/RING

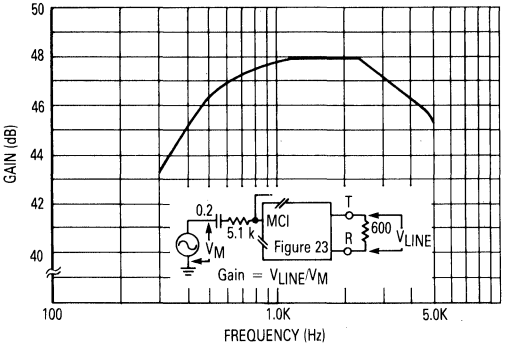


FIGURE 30 — RECEIVE GAIN

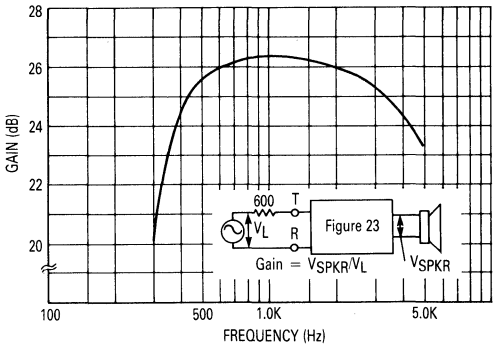
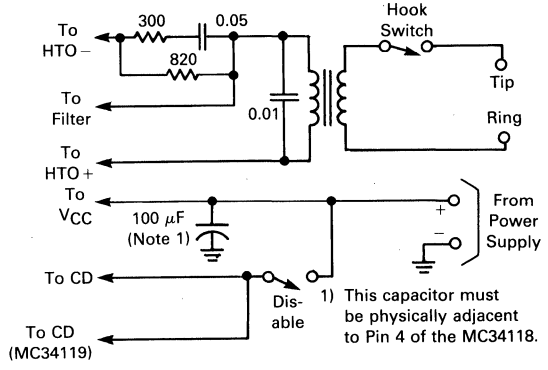


Figure 31 shows how the same circuit can be configured to be powered from a 3.5–6.0 volt power supply rather than the phone line.

FIGURE 31 — OPERATING FROM A POWER SUPPLY



ADDING A DIALER

Figure 32 shows the addition of a dialer to the circuit of Figure 23, with the additional components shown in bold. The MC145412 pulse/tone dialer is shown configured for DTMF operation. The DTMF output (Pin 18) is fed to the hybrid amplifiers at HTI, and the DTMF levels at Tip/Ring are adjusted by varying the 39 kΩ resistor. The Mute Output (active low at Pin 11) mutes the microphone amplifier, and attenuates the DTMF signals in the receive path (by means of the 10 k/3.0 k divider). The MC34118 is forced into the fast idle mode during dialing. The 3.0 volt battery provides for memory retention of the dialer's 10 number storage when the circuit is unpowered.

RFI INTERFERENCE

Potential radio frequency interference problems should be addressed early in the electrical and mechanical design of the speakerphone. RFI may enter the cir-

cuit through Tip and Ring, through the microphone wiring to the microphone amplifier, or through any of the PC board traces. The most sensitive pins on the MC34118 are the inputs to the level detectors (RLI1, RLI2, TLI1, TLI2) since, when there is no speech present, the inputs are high impedance and these op amps are in a near open loop condition. The board traces to these pins should be kept short, and the resistor and capacitor for each of these pins should be physically close to the pins. Any other high impedance input pin (MCI, HTI, FI, VLC) should be considered sensitive to RFI signals.

IN THE FINAL ANALYSIS . . .

Proper operation of a speakerphone is a combination of proper mechanical (acoustic) design as well as proper electronic design. The acoustics of the enclosure must be considered early in the design of a speakerphone. In general, electronics cannot compensate for poor acoustics, low speaker quality, or any combination of the two. Proper acoustic separation of the speaker and microphone, as described in the Design Equations, is essential. The physical location of the microphone, along with the characteristics of the selected microphone, will play a large role in the quality of the transmitted sound. The microphone and speaker vendors can usually provide additional information on the use of their products.

In the final analysis, the circuits shown in this data sheet will have to be "fine tuned" to match the acoustics of the enclosure, the specific hybrid, and the specific microphone and speaker selected. The component values shown in this data sheet should be considered as starting points only. The gains of the transmit and receive paths are easily adjusted at the microphone and speaker amplifiers, respectively. The switching response can then be fine tuned by varying (in small steps) the components at the level detector inputs until satisfactory operation is obtained for both long and short lines.

SUGGESTED VENDORS

Microphones

Primo Microphones Inc.
Bensenville, IL 60106
312-595-1022
Model EM-60

MURA Corp.
Westbury, N.Y. 11590
516-935-3640
Model EC-983-7

Hosiden America Corp.
Elk Grove Village, IL 60007
312-981-1144
Model KUC2123

25 Ω Speakers

Panasonic Industrial Co.
Seacaucus, N.J. 07094
201-348-5233
Model EAS-45P19S

Telecom Transformers

Microtran Co., Inc.
Valley Stream, N.Y. 11528
516-561-6050
Various models — ask for catalog and Application Bulletin F232

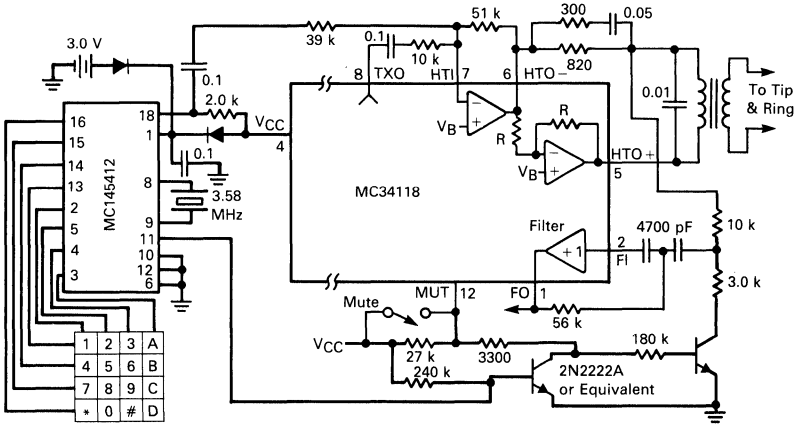
Stancor Products
Logansport, IN 46947
219-722-2244
Various models — ask for catalog

PREM Magnetics, Inc.
McHenry, IL 60050
815-385-2700
Various models — ask for catalog

Onan Power/Electronics
Minneapolis, MN 55437
612-921-5600
Model TC 38-6

Motorola Inc. does not endorse or warrant the suppliers referenced.

FIGURE 32 — ADDING A DIALER TO THE SPEAKERPHONE



MC34119

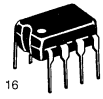
Low Power Audio Amplifier

Silicon Monolithic Integrated Circuit

2

The MC34119 is a low power audio amplifier integrated circuit intended (primarily) for telephone applications, such as in speakerphones. It provides differential speaker outputs to maximize output swing at low supply voltages (2.0 volts minimum). Coupling capacitors to the speaker are not required. Open loop gain is 80 dB, and the closed loop gain is set with two external resistors. A Chip Disable pin permits powering down and/or muting the input signal. The MC34119 is available in a standard 8–pin DIP or a surface mount package.

- Wide Operating Supply Voltage Range (2 – 16 Volts) — Allows Telephone Line Powered Applications
- Low Quiescent Supply Current (2.7 mA Typical) for Battery Powered Applications
- Chip Disable Input to Power Down the IC
- Low Power–Down Quiescent Current (65 μA Typical)
- Drives a Wide Range of Speaker Loads (8 Ohms and Up)
- Output Power Exceeds 250 mW with 32 Ohm Speaker
- Low Total Harmonic Distortion (0.5% Typical)
- Gain Adjustable from < 0 dB to > 46 dB for Voice Band
- Requires Few External Components



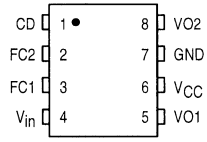
P SUFFIX
PLASTIC DIP
CASE 626

D SUFFIX
SOIC PACKAGE
CASE 751

ORDERING INFORMATION

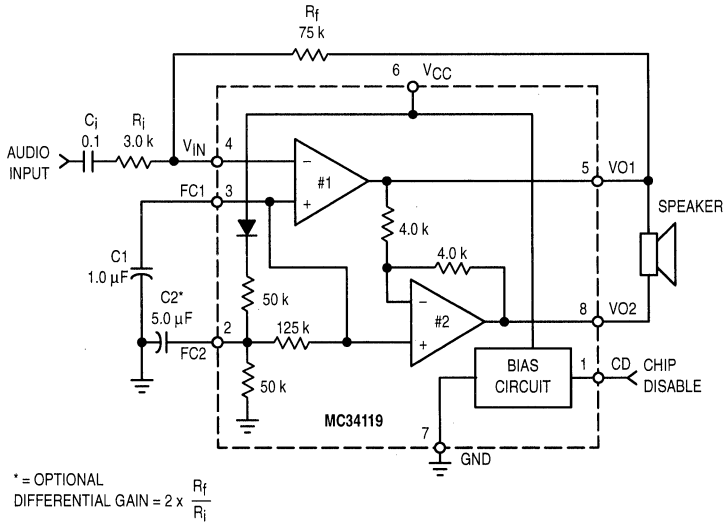
MC34119P	Plastic DIP
MC34119D	Plastic SOIC

PIN ASSIGNMENT



(TOP VIEW)

BLOCK DIAGRAM AND TYPICAL APPLICATION CIRCUIT



* = OPTIONAL
DIFFERENTIAL GAIN = $2 \times \frac{R_f}{R_i}$

REV
9/95

MC34129
MC33129

High Performance Current Mode Controllers

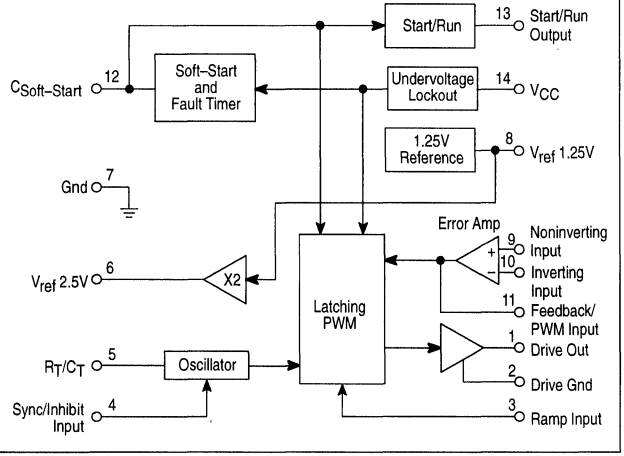
The MC34129/MC33129 are high performance current mode switching regulators specifically designed for use in low power digital telephone applications. These integrated circuits feature a unique internal fault timer that provides automatic restart for overload recovery. For enhanced system efficiency, a start/run comparator is included to implement bootstrapped operation of V_{CC}. Other functions contained are a temperature compensated reference, reference amplifier, fully accessible error amplifier, sawtooth oscillator with sync input, pulse width modulator comparator, and a high current totem pole driver ideally suited for driving a power MOSFET.

Also included are protective features consisting of soft–start, undervoltage lockout, cycle–by–cycle current limiting, adjustable dead time, and a latch for single pulse metering.

Although these devices are primarily intended for use in digital telephone systems, they can be used cost effectively in many other applications.

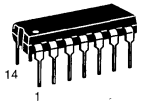
- Current Mode Operation to 300 kHz
- Automatic Feed Forward Compensation
- Latching PWM for Cycle–by–Cycle Current Limiting
- Continuous Retry after Fault Timeout
- Soft–Start with Maximum Peak Switch Current Clamp
- Internally Trimmed 2% Bandgap Reference
- High Current Totem Pole Driver
- Input Undervoltage Lockout
- Low Start–Up and Operating Current
- Direct Interface with Motorola SENSEFET Products

Simplified Block Diagram



HIGH PERFORMANCE CURRENT MODE CONTROLLERS

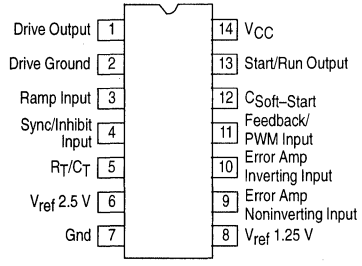
SEMICONDUCTOR TECHNICAL DATA



P SUFFIX
PLASTIC PACKAGE
CASE 646

D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO–14)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Tested Operating Temperature Range	Package
MC34129D	T_A = 0° to +70°C	SO–14
MC34129P		Plastic DIP
MC33129D	T_A = −40° to +85°C	SO–14
MC33129P		Plastic DIP

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
V_{CC} Zener Current	$I_{Z(VCC)}$	50	mA
Start/Run Output Zener Current	$I_{Z(Start/Run)}$	50	mA
Analog Inputs (Pins 3, 5, 9, 10, 11, 12)	–	–0.3 to 5.5	V
Sync Input Voltage	V_{sync}	–0.3 to V_{CC}	V
Drive Output Current, Source or Sink	I_{DRV}	1.0	A
Current, Reference Outputs (Pins 6, 8)	I_{ref}	20	mA
Power Dissipation and Thermal Characteristics D Suffix, Plastic Package Case 751A Maximum Power Dissipation @ T_A = 70°C Thermal Resistance, Junction–to–Air P Suffix, Plastic Package Case 646 Maximum Power Dissipation @ T_A = 70°C Thermal Resistance, Junction–to–Air	 P_D $R_{\theta JA}$ P_D $R_{\theta JA}$	 552 145 800 100	 mW °C/W mW °C/W
Operating Junction Temperature	T_J	+150	°C
Operating Ambient Temperature MC34129 MC33129	T_A	 0 to +70 –40 to +85	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 10 V, T_A = 25°C [Note 1], unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
REFERENCE SECTIONS					
Reference Output Voltage, T_A = 25°C 1.25 V Ref., I_L = 0 mA 2.50 V Ref., I_L = 1.0 mA	V_{ref}	 1.225 2.375	 1.250 2.500	 1.275 2.625	V
Reference Output Voltage, T_A = T_{low} to T_{high} 1.25 V Ref., I_L = 0 mA 2.50 V Ref., I_L = 1.0 mA	V_{ref}	 1.200 2.250	 – –	 1.300 2.750	V
Line Regulation (V_{CC} = 4.0 V to 12 V) 1.25 V Ref., I_L = 0 mA 2.50 V Ref., I_L = 1.0 mA	Reg_{line}	 – –	 2.0 10	 12 50	mV
Load Regulation 1.25 V Ref., I_L = –10 µA to +500 µA 2.50 V Ref., I_L = –0.1 mA to +1.0 mA	Reg_{load}	 – –	 1.0 3.0	 12 25	mV
ERROR AMPLIFIER					
Input Offset Voltage (V_{in} = 1.25 V) T_A = 25°C T_A = T_{low} to T_{high}	V_{IO}	 – –	 1.5 –	 – 10	mV
Input Offset Current (V_{in} = 1.25 V)	I_{IO}	–	10	–	nA
Input Bias Current (V_{in} = 1.25 V) T_A = 25°C T_A = T_{low} to T_{high}	I_{IB}	 – –	 25 –	 – 200	nA
Input Common Mode Voltage Range	V_{ICR}	–	0.5 to 5.5	–	V
Open–Loop Voltage Gain (V_O = 1.25 V)	A_{VOL}	65	87	–	dB
Gain Bandwidth Product (V_O = 1.25 V, f = 100 kHz)	GBW	500	750	–	kHz
Power Supply Rejection Ratio (V_{CC} = 5.0 V to 10 V)	PSRR	65	85	–	dB
Output Source Current (V_O = 1.5 V)	I_{Source}	40	80	–	µA
Output Voltage Swing High State (I_{Source} = 0 µA) Low State (I_{Sink} = 500 µA)	 V_{OH} V_{OL}	 1.75 –	 1.96 0.1	 2.25 0.15	V

NOTE: 1. T_{low} = 0°C for MC34129, –40°C for MC33129 T_{high} = +70°C for MC34129, +85°C for MC33129

ELECTRICAL CHARACTERISTICS (V_{CC} = 10 V, T_A = 25°C [Note 1], unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
PWM COMPARATOR					
Input Offset Voltage (V_{in} = 1.25 V)	V_{IO}	150	275	400	mV
Input Bias Current	I_{IB}	–	–120	–250	µA
Propagation Delay, Ramp Input to Drive Output	$t_{PLH(IN/DRV)}$	–	250	–	ns
SOFT–START					
Capacitor Charge Current (Pin 12 = 0 V)	I_{chg}	0.75	1.2	1.50	µA
Buffer Input Offset Voltage (V_{in} = 1.25 V)	V_{IO}	–	15	40	mV
Buffer Output Voltage (I_{Sink} = 100 µA)	V_{OL}	–	0.15	0.225	V
FAULT TIMER					
Restart Delay Time	t_{DLY}	200	400	600	µs
START/RUN COMPARATOR					
Threshold Voltage (Pin 12)	V_{th}	–	2.0	–	V
Threshold Hysteresis Voltage (Pin 12)	V_H	–	350	–	mV
Output Voltage (I_{Sink} = 500 µA)	V_{OL}	9.0	10	10.3	V
Output Off–State Leakage Current (V_{OH} = 15 V)	$I_{S/R(leak)}$	–	0.4	2.0	µA
Output Zener Voltage (I_Z = 10 mA)	V_Z	–	(V_{CC} + 7.6)	–	V
OSCILLATOR					
Frequency (R_T = 25.5 kΩ, C_T = 390 pF)	f_{OSC}	80	100	120	kHz
Capacitor C_T Discharge Current (Pin 5 = 1.2 V)	I_{dischg}	240	350	460	µA
Sync Input Current High State (V_{in} = 2.0 V) Low State (V_{in} = 0.8 V)	 I_{IH} I_{IL}	 – –	 40 15	 125 35	µA
Sync Input Resistance	R_{in}	12.5	32	50	kΩ
DRIVE OUTPUT					
Output Voltage High State (I_{Source} = 200 mA) Low State (I_{Source} = 200 mA)	 V_{OH} V_{OL}	 8.3 –	 8.9 1.4	 – 1.8	V
Low State Holding Current	I_H	–	225	–	µA
Output Voltage Rise Time (C_L = 500 pF)	t_r	–	390	–	ns
Output Voltage Fall Time (C_L = 500 pF)	t_f	–	30	–	ns
Output Pull–Down Resistance	R_{PD}	100	225	350	kΩ
UNDERVOLTAGE LOCKOUT					
Start–Up Threshold	V_{th}	3.0	3.6	4.2	V
Hysteresis	V_H	5.0	10	15	%
TOTAL DEVICE					
Power Supply Current R_T = 25.5 kΩ, C_T = 390 pF, C_L = 500 pF	I_{CC}	1.0	2.5	4.0	mA
Power Supply Zener Voltage (I_Z = 10 mA)	V_Z	12	14.3	–	V

NOTE: 1. T_{low} = 0°C for MC34129, –40°C for MC33129 T_{high} = +70°C for MC34129, +85°C for MC33129

Figure 1. Timing Resistor versus Oscillator Frequency

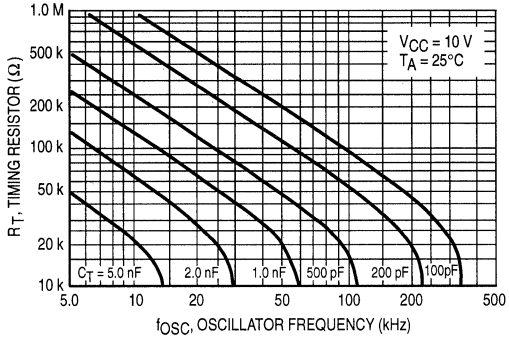


Figure 2. Output Dead–Time versus Oscillator Frequency

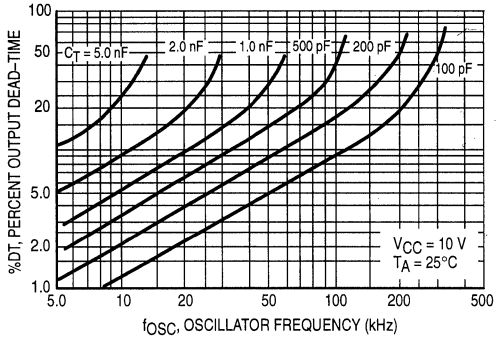


Figure 3. Oscillator Frequency Change versus Temperature

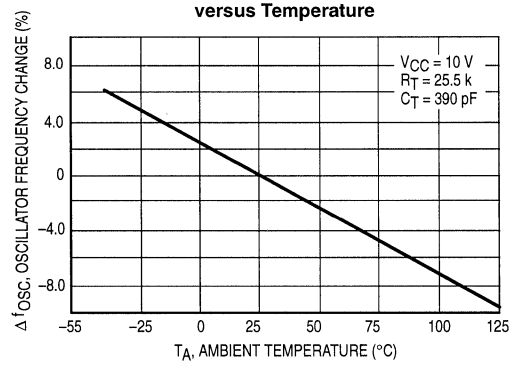


Figure 4. Error Amp Open Loop Gain and Phase versus Frequency

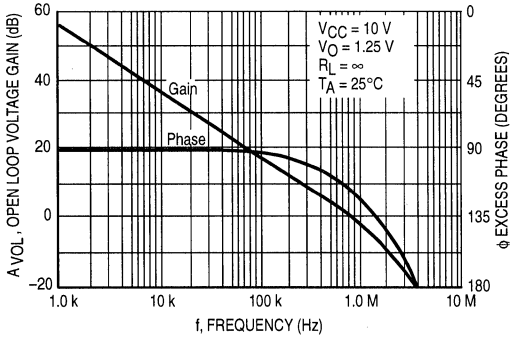


Figure 5. Error Amp Small–Signal Transient Response

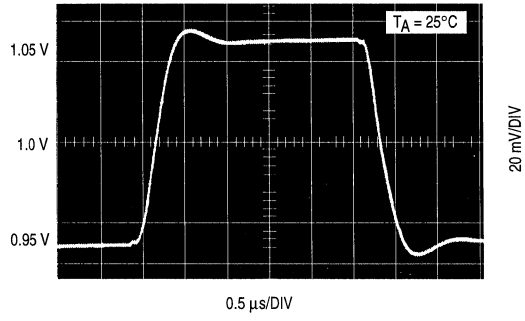


Figure 6. Error Amp Large–Signal Transient Response

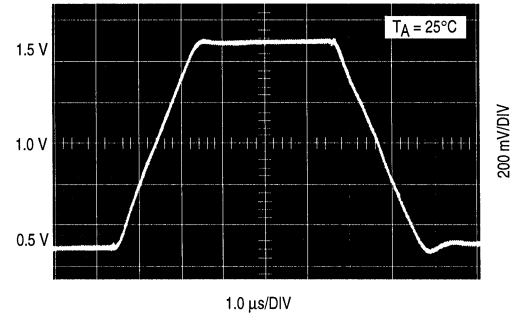


Figure 7. Error Amp Open–Loop DC Gain versus Load Resistance

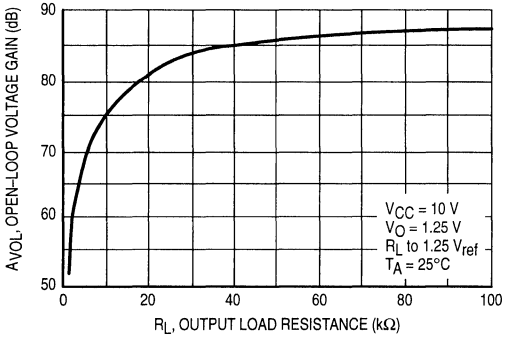


Figure 8. Error Amp Output Saturation versus Sink Current

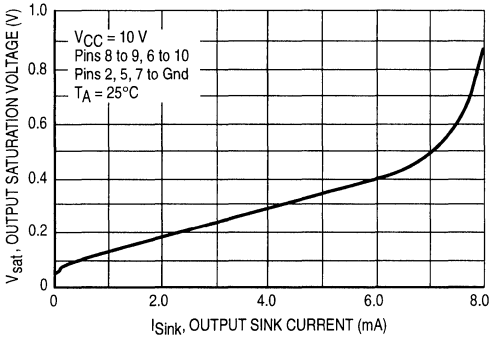


Figure 9. Soft–Start Buffer Output Saturation versus Sink Current

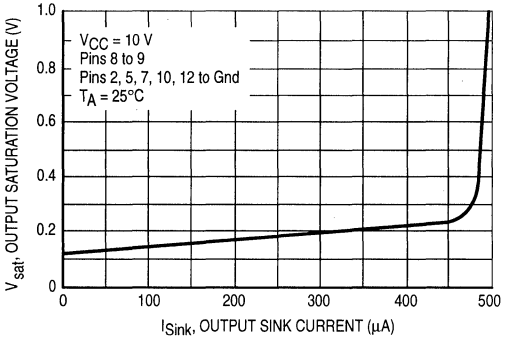


Figure 10. Reference Output Voltage versus Supply Voltage

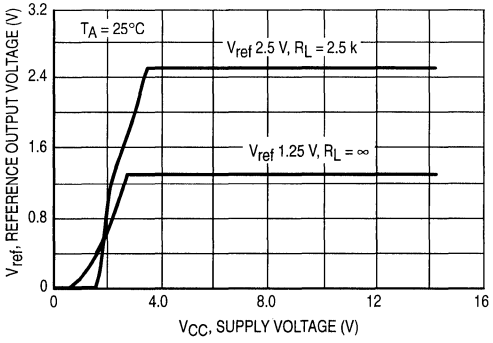


Figure 11. 1.25 V Reference Output Voltage Change versus Source Current

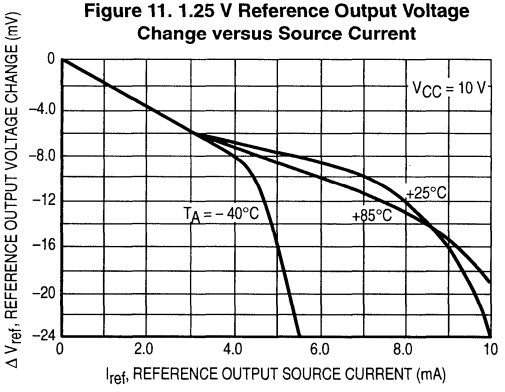


Figure 12. 2.5 V Reference Output Voltage Change versus Source Current

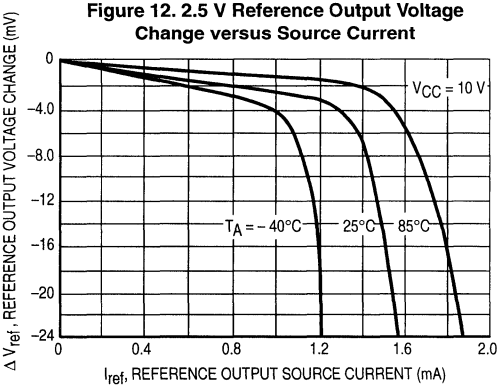


Figure 13. 1.25 V Reference Output Voltage versus Temperature

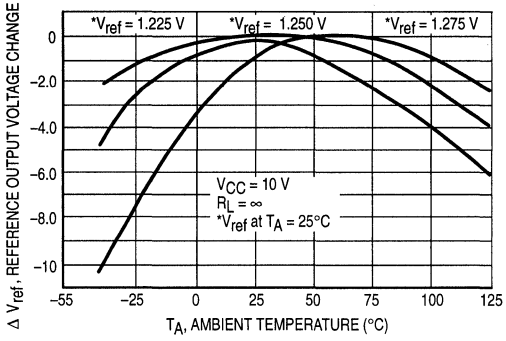


Figure 14. 2.5 V Reference Output Voltage versus Temperature

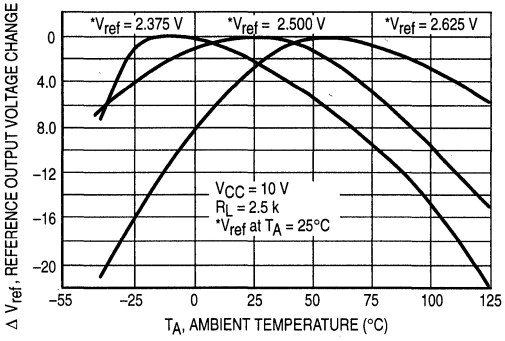


Figure 15. Drive Output Saturation versus Load Current

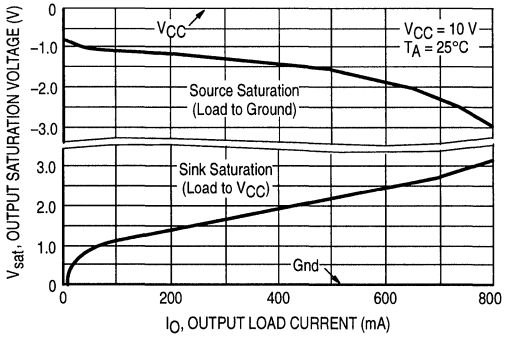


Figure 16. Drive Output Waveform

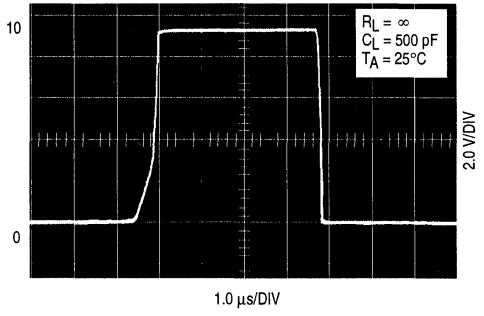
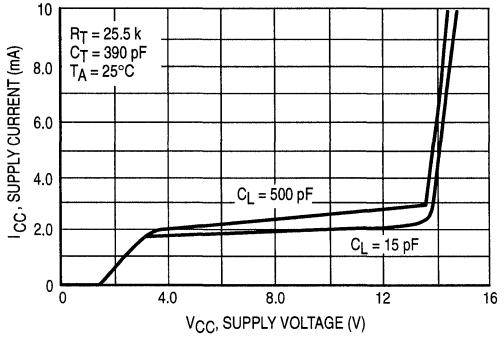


Figure 17. Supply Current versus Supply Voltage



PIN FUNCTION DESCRIPTION

Pin	Function	Description
1	Drive Output	This output directly drives the gate of a power MOSFET. Peak currents up to 1.0 A are sourced and sinked by this pin.
2	Drive Ground	This pin is a separate power ground return that is connected back to the power source. It is used to reduce the effects of switching transient noise on the control circuitry.
3	Ramp Input	A voltage proportional to the inductor current is connected to this input. The PWM uses this information to terminate output switch conduction.
4	Sync/Inhibit Input	A rectangular waveform applied to this input will synchronize the Oscillator and limit the maximum Drive Output duty cycle. A dc voltage within the range of 2.0 V to V_{CC} will inhibit the controller.
5	R_T/C_T	The free–running Oscillator frequency and maximum Drive Output duty cycle are programmed by connecting resistor R_T to V_{ref} 2.5 V and capacitor C_T to Ground. Operation to 300 kHz is possible.
6	V_{ref} 2.50 V	This output is derived from V_{ref} 1.25 V. It provides charging current for capacitor C_T through resistor R_T.
7	Ground	This pin is the control circuitry ground return and is connected back to the source ground.
8	V_{ref} 1.25 V	This output furnishes a voltage reference for the Error Amplifier noninverting input.
9	Error Amp Noninverting Input	This is the noninverting input of the Error Amplifier. It is normally connected to the 1.25 V reference.
10	Error Amp Inverting Input	This is the inverting input of the Error Amplifier. It is normally connected to the switching power supply output through a resistor divider.
11	Feedback/PWM Input	This pin is available for loop compensation. It is connected to the Error Amplifier and Soft–Start Buffer outputs, and the Pulse Width Modulator input.
12	$C_{Soft–Start}$	A capacitor $C_{Soft–Start}$ is connected from this pin to Ground for a controlled ramp–up of peak inductor current during start–up.
13	Start/Run Output	This output controls the state of an external bootstrap transistor. During the start mode, operating bias is supplied by the transistor from V_{in}. In the run mode, the transistor is switched off and bias is supplied by an auxiliary power transformer winding.
14	V_{CC}	This pin is the positive supply of the control IC. The controller is functional over a minimum V_{CC} range of 4.2 V to 12 V.

OPERATING DESCRIPTION

The MC34129 series are high performance current mode switching regulator controllers specifically designed for use in low power telecommunication applications. Implementation will allow remote digital telephones and terminals to shed their power cords and derive operating power directly from the twisted pair used for data transmission. Although these devices are primarily intended for use in digital telephone systems, they can be used cost effectively in a wide range of converter applications. A representative block diagram is shown in Figure 18.

2

Oscillator

The oscillator frequency is programmed by the values selected for the timing components R_T and C_T. Capacitor C_T is charged from the 2.5 V reference through resistor R_T to approximately 1.25 V and discharged by an internal current sink to ground. During the discharge of C_T, the oscillator generates an internal blanking pulse that holds the lower input of the NOR gate high. This causes the Drive Output to be in a low state, thus producing a controlled amount of output deadtime. Figure 1 shows Oscillator Frequency versus R_T and Figure 2 Output Deadtime versus Frequency, both for given values of C_T. Note that many values of R_T and C_T will give the same oscillator frequency but only one combination will yield a specific output deadtime at a give frequency. In many noise sensitive applications it may be desirable to frequency–lock one or more switching regulators to an external system clock. This can be accomplished by applying the clock signal to the Synch/Inhibit Input. For reliable locking, the free–running oscillator frequency should be about 10% less than the clock frequency. Referring to the timing diagram shown Figure 19, the rising edge of the clock signal applied to the Sync/Inhibit Input, terminates charging of C_T and Drive Output conduction. By tailoring the clock waveform, accurate duty cycle clamping of the Drive Output can be achieved. A circuit method is shown in Figure 20. The Sync/Inhibit Input may also be used as a means for system shutdown by applying a dc voltage that is within the range of 2.0 V to V_{CC}.

PWM Comparator and Latch

The MC34129 operates as a current mode controller whereby output switch conduction is initiated by the oscillator and terminated when the peak inductor current reaches a threshold level established by the output of the Error Amp or Soft–Start Buffer (Pin 11). Thus the error signal controls the peak inductor current on a cycle–by–cycle basis. The PWM Comparator–Latch configuration used, ensures that only a single pulse appears at the Drive Output during any given oscillator cycle. The inductor current is converted to a voltage by inserting the ground–referenced resistor R_S in series with the source of output switch Q_1. The Ramp Input adds an offset of 275 mV to this voltage to guarantee that no pulses appear at the Drive Output when Pin 11 is at its lowest state. This occurs at the beginning of the soft–start interval or when the power supply is operating and the load is removed. The peak inductor current under normal operating conditions is controlled by the voltage at Pin 11 where:

$$I_{pk} = \frac{V_{(Pin\ 11)} - 0.275\ V}{R_S}$$

Abnormal operating conditions occur when the power supply output is overloaded or if output voltage sensing is lost. Under these conditions, the voltage at Pin 11 will be internally clamped to 1.95 V by the output of the Soft–Start Buffer. Therefore the maximum peak switch current is:

$$I_{pk(max)} = \frac{1.95\ V - 0.275}{R_S} = \frac{1.675\ V}{R_S}$$

When designing a high power switching regulator it becomes desirable to reduce the internal clamp voltage in order to keep the power dissipation of R_S to a reasonable level. A simple method which adjusts this voltage in discrete increments is shown in Figure 22. This method is possible because the Ramp Input bias current is always negative (typically –120 μA). A positive temperature coefficient equal to that of the diode string will be exhibited by $I_{pk(max)}$. An adjustable method that is more precise and temperature stable is shown in Figure 23. Erratic operation due to noise pickup can result if there is an excessive reduction of the clamp voltage. In this situation, high frequency circuit layout techniques are imperative.

A narrow spike on the leading edge of the current waveform can usually be observed and may cause the power supply to exhibit an instability when the output is lightly loaded. This spike is due to the power transformer interwinding capacitance and output rectifier recovery time. The addition of an RC filter on the Ramp Input with a time constant that approximates the spike duration will usually eliminate the instability; refer to Figure 25.

Error Amp and Soft–Start Buffer

A fully–compensated Error Amplifier with access to both inputs and output is provided for maximum design flexibility. The Error Amplifier output is common with that of the Soft–Start Buffer. These outputs are open–collector (sink only) and are ORed together at the inverting input of the PWM Comparator. With this configuration, the amplifier that demands lower peak inductor current dominates control of the loop. Soft–Start is mandatory for stable start–up when power is provided through a high source impedance such as the long twisted pair used in telecommunications. It effectively removes the load from the output of the switching power supply upon initial start–up. The Soft–Start Buffer is configured as a unity gain follower with the noninverting input connected to Pin 12. An internal 1.0 μA current source charges the soft–start capacitor ($C_{Soft–Start}$) to an internally clamped level of 1.95 V. The rate of change of peak inductor current, during start–up, is programmed by the capacitor value selected. Either the Fault Timer or the Undervoltage Lockout can discharge the soft–start capacitor.

Figure 18. Representative Block Diagram

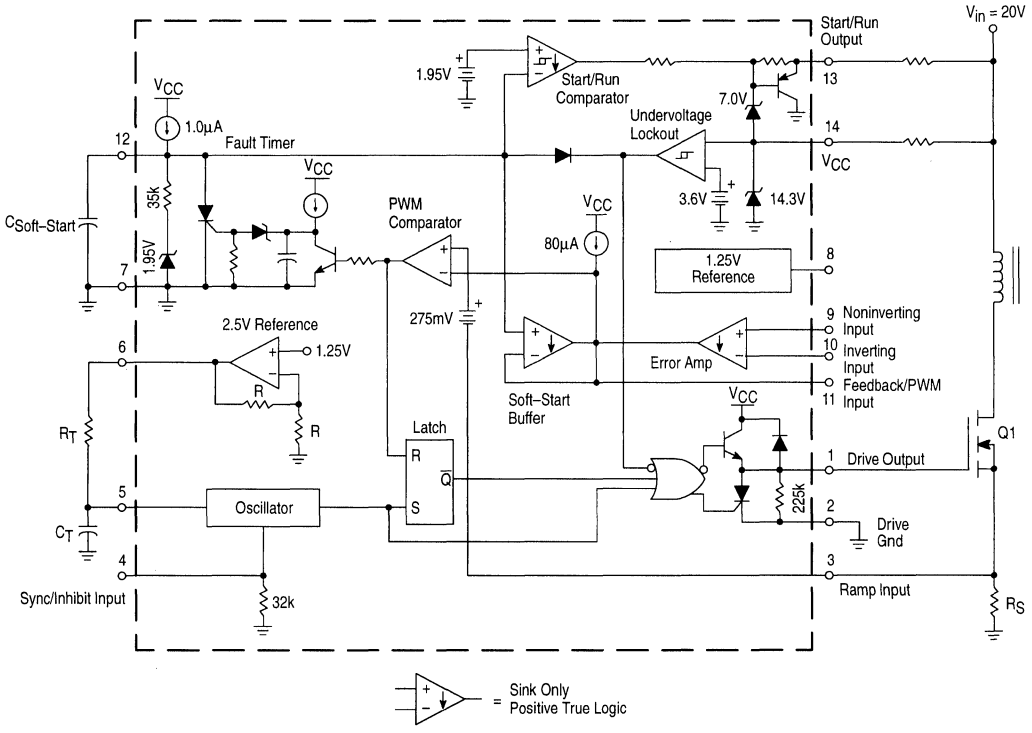
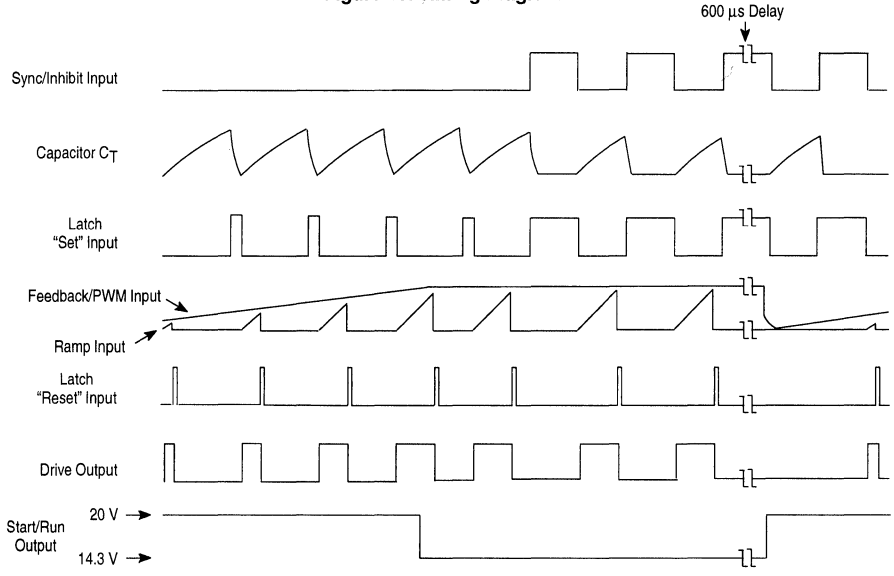


Figure 19. Timing Diagram



Fault Timer

This unique circuit prevents sustained operating in a lockout condition. This can occur with conventional switching control ICs when operating from a power source with a high series impedance. If the power required by the load is greater than that available from the source, the input voltage will collapse, causing the lockout condition. The Fault Timer provides automatic recovery when this condition is detected. Under normal operating conditions, the output of the PWM Comparator will reset the Latch and discharge the internal Fault Timer capacitor on a cycle–by–cycle basis. Under operating conditions where the required power into the load is greater than that available from the source (V_{in}), the Ramp Input voltage (plus offset) will not reach the comparator threshold level (Pin 11), and the output of the PWM Comparator will remain low. If this condition persists for more that 600 μs, the Fault Timer will active, discharging $C_{Soft–Start}$ and initiating a soft–start cycle. The power supply will operate in a skip cycle or hiccup mode until either the load power or source impedance is reduced. The minimum fault timeout is 200 μs, which limits the useful switching frequency to a minimum of 5.0 kHz.

Start/Run Comparator

A bootstrap start–up circuit is included to improve system efficiency when operating from a high input voltage. The output of the Start/Run Comparator controls the state of an external transistor. A typical application is shown in Figure 21. While $C_{Soft–Start}$ is charging, start–up bias is supplied to V_{CC} (Pin 14) from V_{in} through transistor Q2. When $C_{Soft–Start}$ reaches the 1.95 V clamp level, the Start–Run output switches low (V_{CC} = 50 mV), turning off Q2. Operating bias is now derived from the auxiliary bootstrap winding of the transformer, and all drive power is efficiently converted down from V_{in}. The start time must be long enough for the power supply output to reach regulation. This will ensure that there is sufficient bias voltage at the auxiliary bootstrap winding for sustained operation.

$$t_{Start} = \frac{1.95 V C_{Soft–Start}}{1.0\ \mu A} = 1.95\ C_{Soft–Start}\ \text{in}\ \mu F$$

The Start/Run Comparator has 350 mV of hysteresis. The output off–state is clamped to V_{CC} + 7.6 V by the internal zener and PNP transistor base–emitter junction.

Drive Output and Drive Ground

The MC34129 contains a single totem–pole output stage that was specifically designed for direct drive of power MOSFETs. It is capable of up to ±1.0 A peak drive current and has a typical fall time of 30 ns with a 500 pF load. The totem–pole stage consists of an NPN transistor for turn–on drive and a high speed SCR for turn–off. The SCR design requires less average supply current (I_{CC}) when compared to conventional switching control ICs that use an all NPN totem–pole. The SCR accomplishes this during turn–off of the MOSFET, by utilizing the gate charge as regenerative on–bias, whereas the conventional all transistor design requires continuous base current. Conversion efficiency in low power applications is greatly enhanced with this reduction of I_{CC}. The SCR's low–state holding current (I_H) is typically 225 μA. An internal 225 kΩ pull–down resistor is included to shunt the Drive Output off–state leakage to ground when the Undervoltage Lockout is active. A separate Drive Ground is provided to reduce the effects of switching transient noise imposed on the Ramp Input. This feature becomes particularly useful when the $I_{pk(max)}$ clamp level is reduced. Figure 24 shows the proper implementation of the MC34129 with a current sensing power MOSFET.

Undervoltage Lockout

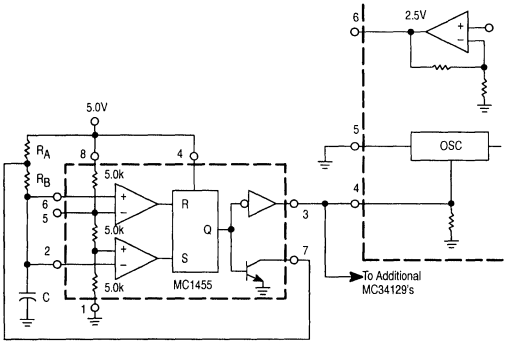
The Undervoltage Lockout comparator holds the Drive Output and $C_{Soft–Start}$ pins in the low state when V_{CC} is less than 3.6 V. This ensures that the MC34129 is fully functional before the output stage is enabled and a soft–start cycle begins. A built–in hysteresis of 350 mV prevents erratic output behavior as V_{CC} crosses the comparator threshold voltage. A 14.3 V zener is connected as a shunt regulator from V_{CC} to ground. Its purpose is to protect the MOSFET gate from excessive drove voltage during system start–up. An external 9.1 V zener is required when driving low threshold MOSFETs. Refer to Figure 21. The minimum operating voltage range of the IC is 4.2 V to 12 V.

References

The 1.25 V bandgap reference is trimmed to ±2.0% tolerance at T_A = 25°C. It is intended to be used in conjunction with the Error Amp. The 2.50 V reference is derived from the 1.25 V reference by an internal op amp with a fixed gain of 2.0. It has an output tolerance of ±5.0% at T_A = 25°C and its primary purpose is to supply charging current to the oscillator timing capacitor.

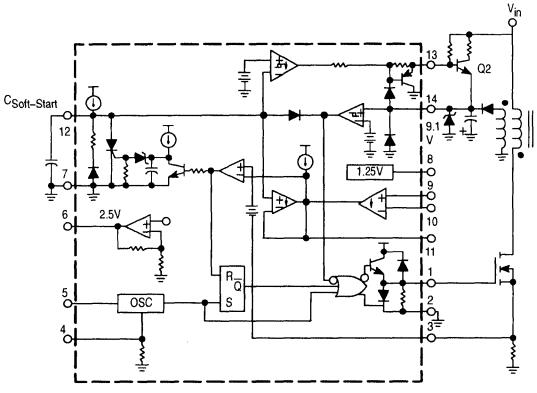
For further information, please refer to AN976.

Figure 20. External Duty Cycle Clamp and Multi–Unit Synchronization



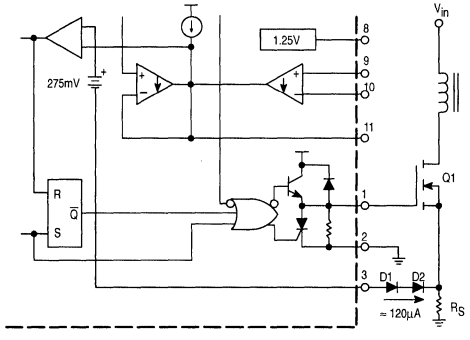
$$f = \frac{1.44}{(R_A + 2R_B)C} \qquad D_{max} = \frac{R_B}{R_A + 2R_B}$$

Figure 21. Bootstrap Start–Up



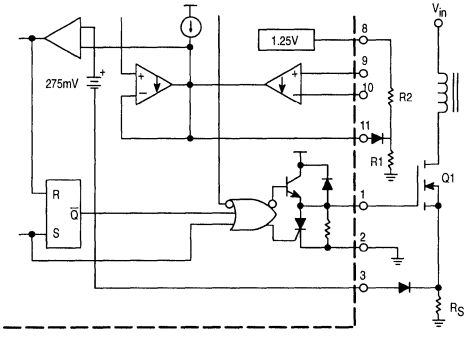
The external 9.1 V zener is required when driving low threshold MOSFETs.

Figure 22. Discrete Step Reduction of Clamp Level



$$I_{pk(max)} = \frac{1.675 - (V_{F(D1)} + V_{F(D2)})}{R_S}$$

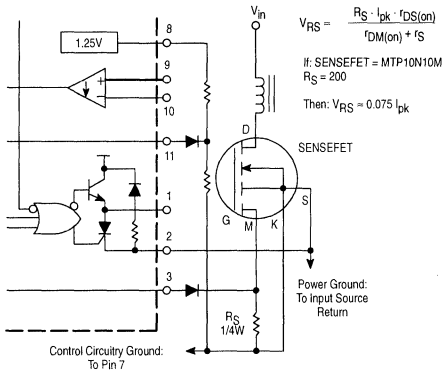
Figure 23. Adjustable Reduction of Clamp Level



If: $\frac{1.25\ V}{R1 + R2} \geq 1.0\ mA$ Then: $I_{pk(max)} \approx \frac{\frac{1.25}{\left(\frac{R2}{R1} + 1\right)} - 0.275}{R_S}$

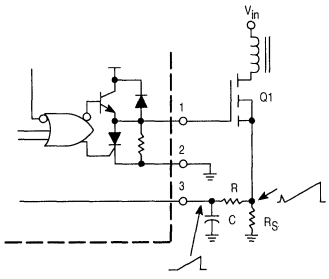
2

Figure 24. Current Sensing Power MOSFET



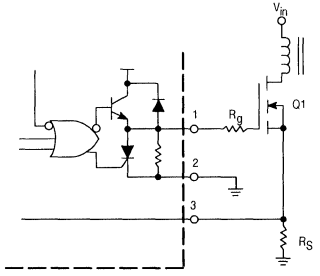
Virtually lossless current sensing can be achieved with the implementation of a SENSEFET power switch.

Figure 25. Current Waveform Spike Suppression



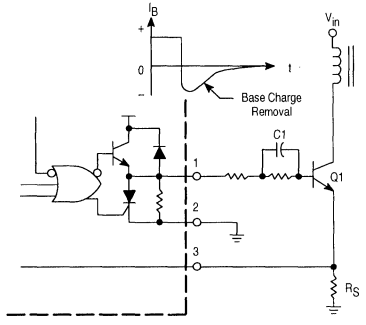
The addition of the RC filter will eliminate instability caused by the leading edge spike on the current waveform.

Figure 26. MOSFET Parasitic Oscillations



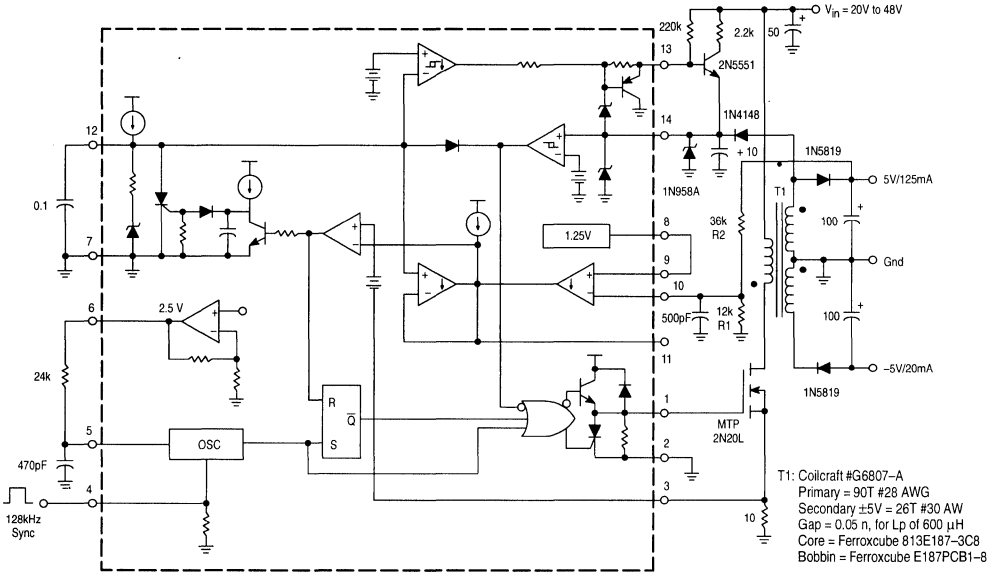
Series gate resistor R_g will damp any high frequency parasitic oscillations caused by the MOSFET input capacitance and any series wiring inductance in the gate–source circuit.

Figure 27. Bipolar Transistor Drive



The totem–pole output can furnish negative base current for enhanced transistor turn–off, with the addition of capacitor C1.

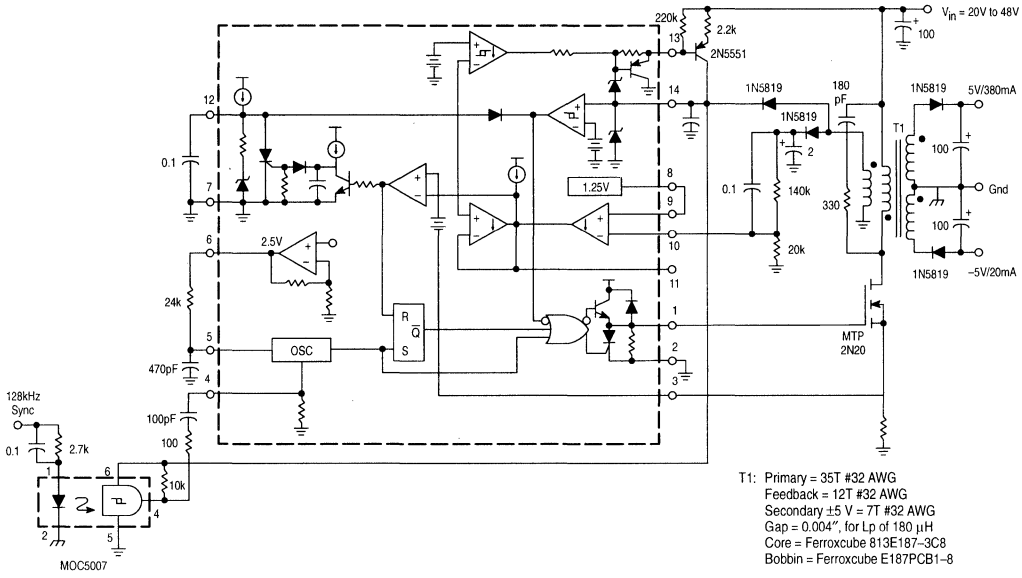
Figure 28. Non–Isolated 725 mW Flyback Regulator



Test	Conditions	Results
Line Regulation 5.0 V	V_{in} = 20 V to 40 V, I_{out} 5.0 V = 125 mA, I_{out} –5.0 V = 20 mA	Δ = 1.0 mV
Load Regulation 5.0 V	V_{in} = 30 V, I_{out} 5.0 V = 0 mA to 150 mA, I_{out} –5.0 V = 20 mA	Δ = 2.0 mV
Output Ripple 5.0 V	V_{in} = 30 V, I_{out} 5.0 V = 125 mA, I_{out} –5.0 V = 20 mA	150 mVp–p
Efficiency	V_{in} = 30 V, I_{out} 5.0 V = 125 mA, I_{out} –5.0 V = 20 mA	77%

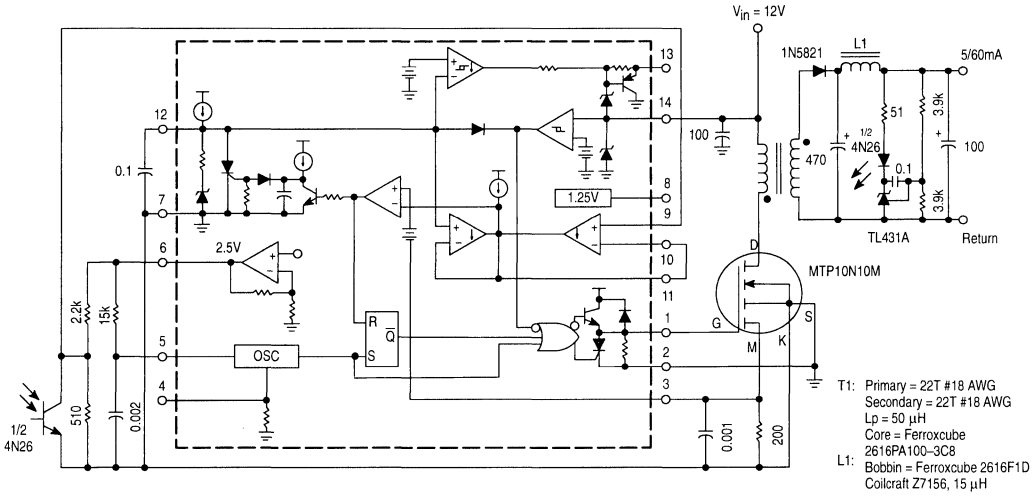
$$V_{out} = 1.25 \left(\frac{R2}{R1} + 1 \right)$$

Figure 29. Isolated 2.0 W Flyback Regulator



Test	Conditions	Results
Line Regulation 5.0 V	V_{in} = 20 V to 40 V, I_{out} 5.0 V = 380 mA, I_{out} −5.0 V = 20 mA	Δ = 1.0 mV
Load Regulation 5.0 V	V_{in} = 30 V, I_{out} 5.0 V = 100 mA to 380 mA, I_{out} −5.0 V = 20 mA	Δ = 15 mV
Output Ripple 5.0 V	V_{in} = 30 V, I_{out} 5.0 V = 380 mA, I_{out} −5.0 V = 20 mA	150 mVp−p
Efficiency	V_{in} = 30 V, I_{out} 5.0 V = 380 mA, I_{out} −5.0 V = 20 mA	73%

Figure 30. Isolated 3.0 W Flyback Regulator with Secondary Side Sensing



Test	Conditions	Results
Line Regulation	V_{in} = 8.0 V to 12 V, I_{out} 600 mA	Δ = 1.0 mV
Load Regulation	V_{in} = 12 V, I_{out} = 100 mA to 600 mA	Δ = 8.0 mV
Output Ripple	V_{in} = 12 V, I_{out} = 600 mA	20 mVp–p
Efficiency	V_{in} = 12 V, I_{out} = 600 mA	81%

An economical method of achieving secondary sensing is to combine the TL431A with a 4N26 optocoupler.

MOTOROLA

MC34216

Product Preview

Programmable Telephone Line Interface Circuit with Loudspeaker Amplifier

PROGRAMMABLE TELEPHONE LINE INTERFACE CIRCUIT WITH LOUDSPEAKER AMPLIFIER

SEMICONDUCTOR TECHNICAL DATA

2

The MC34216 is developed for use in telephone applications where besides the standard telephone functions also the group listening–in feature is required. In cooperation with a microcontroller, the circuit performs all basic telephone functions including DTMF generation and pulse dialing. The listening–in part includes a loudspeaker amplifier, an anti–howling circuit and a strong supply. In combination with the TCA3385, the ringing is performed via the loudspeaker.

FEATURES

Line Driver and Supply

- DC and AC Termination of the Line
- Selectable Masks: France, U.K., Low Voltage
- Current Protection
- Adjustable Set Impedance for Resistive and Complex Termination
- Efficient Supply Point for Loudspeaker Amplifier and Peripherals

Handset Operation

- Transmit and Receive Amplifiers
- Adjustable Sidetone Network
- Line Length AGC
- Microphone and Earpiece Mute
- Earpiece Gain Increase Switch
- Microphone Squelch Function
- Transmit Amplifier Soft Clipping

Dialing and Ringing

- Generates DTMF, Pilot Tones and Ring Signal
- Interrupter Driver for Pulse–Dialing
- Low Current While Pulse–Dialing
- Optimized for Ringing via Loudspeaker
- Programmable Ring Melodies
- Uses Inexpensive 500 kHz Resonator

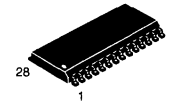
Loudspeaking Facility

- Integrated Loudspeaker Amplifier
- Peak–to–Peak Limiter Prevents Distortion
- Programmable Volume
- Anti–Howling Circuitry for Group Listening–In
- Interfacing for Handsfree Conversation

Application Areas

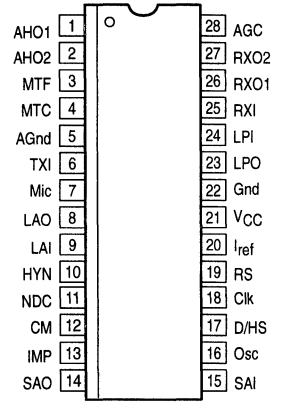
- Corded Telephony with Group Listening–In
- Cordless Telephony Base Station with Group Listening–In
- Telephones with Answering Machines
- Fax, Intercom, Modem

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.



DW SUFFIX
PLASTIC PACKAGE
CASE 751F

PIN CONNECTIONS



(Top View)

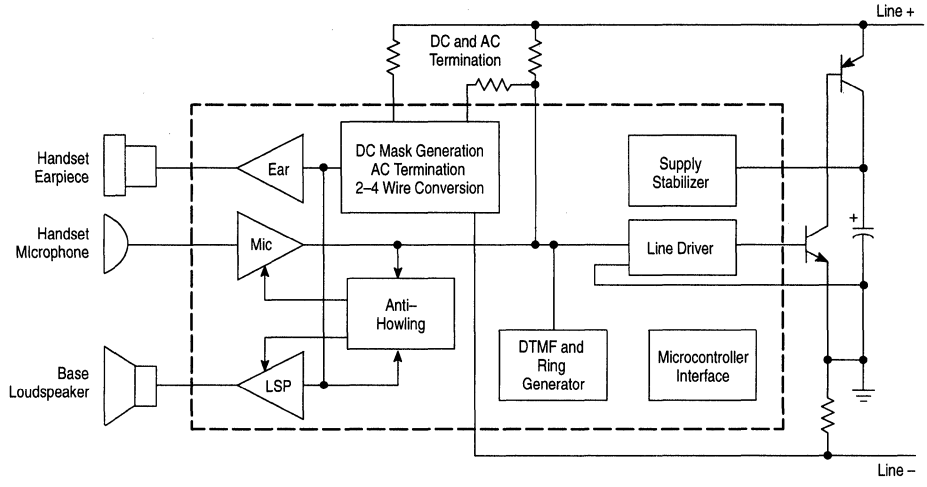
ORDERING INFORMATION

Device	Tested Operating Temperature Range	Package
MC34216DW	T_A = 0° to +70°C	SO–28L

PIN FUNCTION DESCRIPTION

Pin	Symbol	Description
1	AHO1	Anti–Howling Timing, Speakerphone Input
2	AHO2	Anti–Howling Timing, Low Voltage Line Driver Disable
3	MTF	Microphone Threshold Filtering
4	MTC	Microphone Threshold Timing
5	AGnd	Small Signal Ground
6	TXI	Microphone Amplifier Input
7	Mic	Microphone Bias Current Sink
8	LAO	Line Driver Amplifier Output
9	LAI	Line Driver Amplifier Input
10	HYN	Hybrid Network Input
11	NDC	Noise Decoupling
12	CM	DC Mask Signal Filtering
13	IMP	Reference Voltage
14	SAO	Line Current Sense Amplifier Output
15	SAI	Line Current Sense Amplifier Input
16	Osc	Oscillator Input. Connect to 500 kHz Resonator
17	D/HS	Data Input, Hookstatus Output
18	Clk	Clock Input
19	RS	Reset Output
20	I_{ref}	Reference Current
21	V_{CC}	Supply Voltage
22	Gnd	Large Signal Ground
23	LPO	Loudspeaker Amplifier Output
24	LPI	Loudspeaker Amplifier Input
25	RXI	Receive Amplifier Input
26	RXO1	Receive Amplifier Output
27	RXO2	Receive Amplifier Output
28	AGC	Loudspeaker AGC Timing

Simplified Block Diagram



This device contains 6,507 active transistors.

CIRCUIT DESCRIPTION

With the MC34216, a microcontroller and a switched mode power supply, a telephone set with listening–in function and ringing via loudspeaker can be built as shown in Figure 1.

The block diagram of the MC34216 (see Figure 2), shows the basic blocks of the device plus the essential external components.

Figure 1. Telephone Concept with MC34216

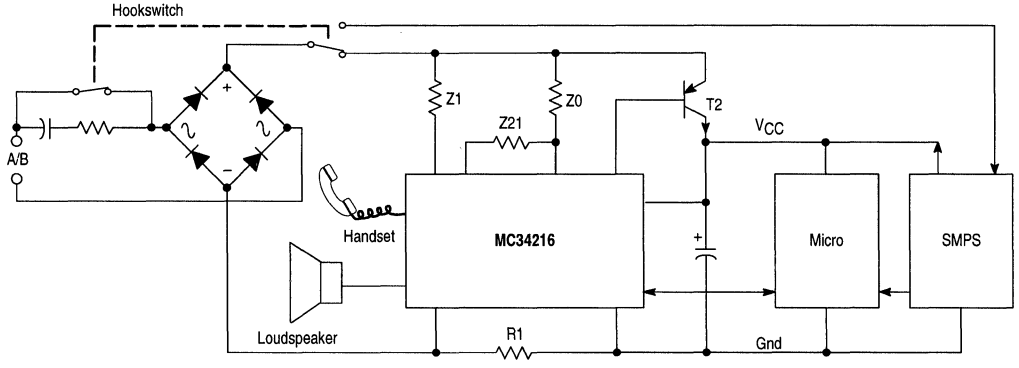


Figure 2. Block Diagram of the MC34216 with Essential Components

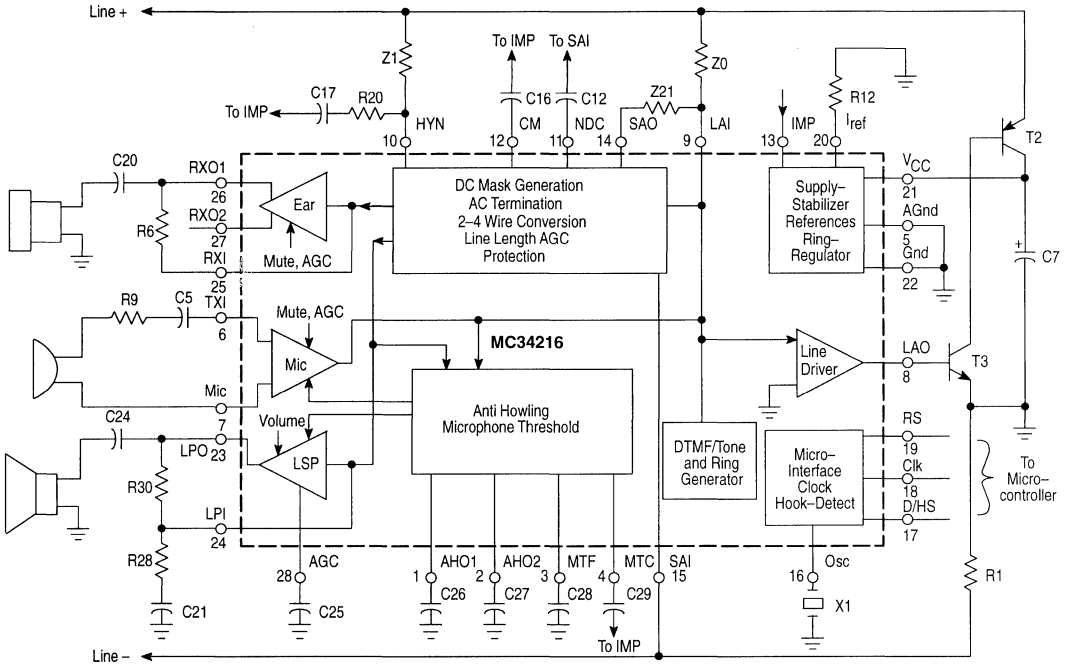


Table 1

A1, A0	Data	Symbol	Function	Comments
00	D0	MicM	Microphone Mute	On/Off
	D1	EM	Earphone Mute	On/Off
	D2	LD	Loop Disconnect	For Pulse–Dialing
	D3	PT	Pilot Tone	On/Off
	D4	IT	Idle Tone	On/Off
	D5	MicP	Microphone Power	On/Off
01	D0	MFC0	Tone Control	Switch On/Off DTMF & Tone Generator
	D1	MFC1	Tone Control	
	D2	MF0	Tone Select	Select DTMF & Tone Frequency
	D3	MF1	Tone Select	
	D4	MF2	Tone Select	
	D5	MF3	Tone Select	
10	D0	R/S	Ring/Speech Mode	Select
	D1	EA	Earphone Gain +6.0 dB	On/Off
	D2	G0	Loudspeaker Gain	Reduce Gain up to 27 dB in 4.5 dB Steps & Mute
	D3	G1	Loudspeaker Gain	
	D4	G2	Loudspeaker Gain	
	D5	RT	Ring Tone	On/Off
11	D0	DCM0	DC Mask Control	Select French, U.K., or Low Voltage Mask
	D1	DCM1	DC Mask Control	
	D2	Sp	Speakerphone Mode	On/Off
	D3	GR	Line Length AGC	On/Off
	D4	HPI	Anti–Howling	On/Off
	D5	Mth	Microphone Threshold	On/Off

When off–hook, the loop current flows through transistor T2 and supplies the externals (microcontroller, etc.) at V_{CC} which is stabilized by the MC34216. The V–I line characteristic is programmed by the microcontroller and adjusted by the external components Z0, Z1, Z21 and R1 which are in a regulator loop, acting on transistor T2. The ac impedance is generated in a similar way. The handset and loudspeaker can be connected directly to the MC34216 to perform handset and listening–in operation. Via the bus, the microcontroller programs the MC34216 to perform the DTMF/pulse–dialing and provide supervisory tones, as well as control other functions. The user keypad has to be connected to the microcontroller. When on–hook, the SMPS (TCA3385) supplies the circuit in the presence of a ringing signal. The microcontroller programs the MC34216 and a ringing melody can be generated via the loudspeaker.

A summary of the control bits which can be programmed from the microcontroller are in Table 1.

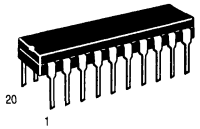
MC44107

Product Preview

IR Remote Control Transmitter
CMOS

The MC44107 remote control transmitter converts a keyboard input into a pulse code modulated signal suitable for infrared transmission to an appropriate receiver. Its large command capacity, 512 commands, makes it highly suited to remote control applications in TV, video, hi–fi, etc. The transmitter is an LSI circuit realized in complementary MOS technology.

- Binary Coded, 9–Bit PCM Data Word
- Simple Modulator Requirements
- One–Pin Reference Oscillator for External Ceramic Resonator
- Very Low (Maximum 1 μA) Standby Current Consumption
- Wide Operating Voltage Range: 4 to 10 V
- Operating Temperature Range: – 40 to 85° C

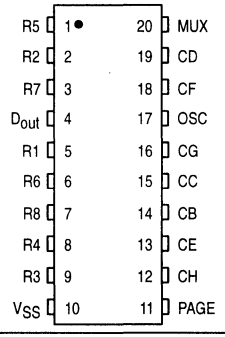


P SUFFIX
PLASTIC DIP
CASE 738

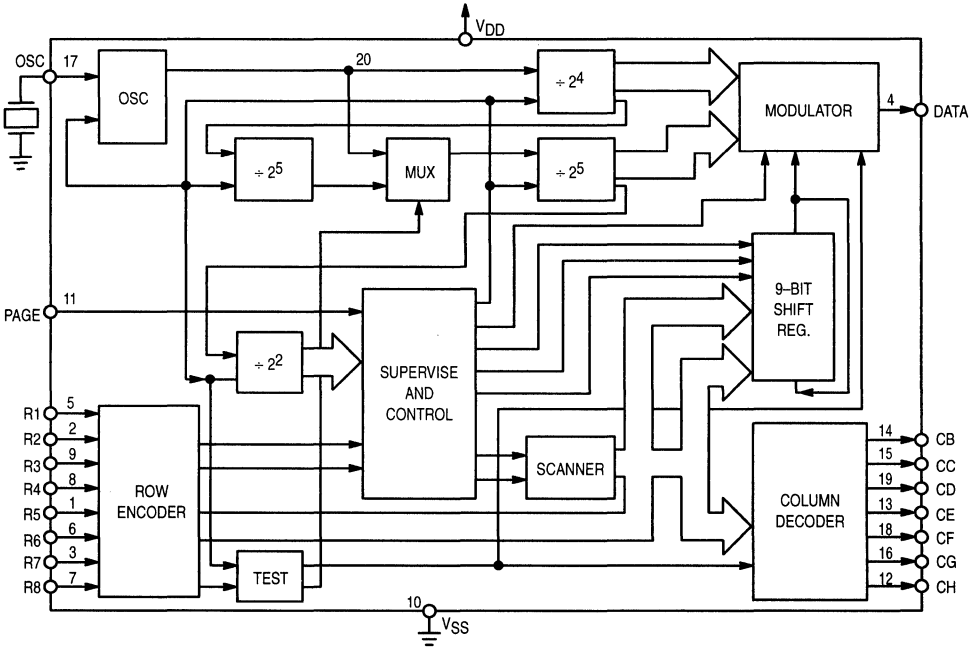
ORDERING INFORMATION

MC44107P	Plastic DIP

PIN ASSIGNMENT



BLOCK DIAGRAM



REV 2
8/95

MAXIMUM RATINGS* (Voltages referenced to V_{SS})

Parameter	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	– 0.5 to + 12	V
Input Voltage, All Inputs	V_{in}	– 0.5 to V_{DD} + 0.5	V
DC Current Drain per Pin (Except Signal Out and V_{DD})	I	2	mA
DC Current Drain (Signal Out and V_{DD})	I	10	mA
Storage Temperature Range	T_{stg}	– 65 to + 150	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Descriptions section.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields; however, it is advised that precautions be taken to avoid application of voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

2

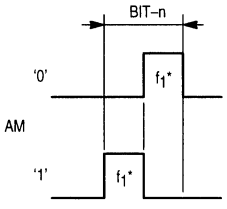
ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} V_{dc}	– 40°C Min	– 40°C Max	25°C Min	25°C Typ	25°C Max	85°C Min	85°C Max	Unit
Inputs R1...R8 and PAGE (with Pull–Up)	I_{in}									µA
I_{in} at V_{in} = 1.2 V		4	—	70	—	—	50	—	40	
I_{in} at V_{in} = 3 V		10	—	350	—	—	250	—	200	
I_{in} at V_{in} = 2.8 V		4	5	—	4	—	—	3	—	
I_{in} at V_{in} = 7 V		10	25	—	20	—	—	15	—	
V_{IH}	V_{IH}	4	2.8	—	2.8	—	—	2.8	—	V
V_{IH}		10	7	—	7	—	—	7	—	
V_{IL}	V_{IL}	4	—	1.2	—	—	1.2	—	1.2	V
V_{IL}		10	—	3	—	—	3	—	3	
Outputs CB...CH (Open Drain)	I_{on}									µA
I_{on} at V_{on} = 1.2 V		4	270	—	200	—	—	160	—	
I_{on} at V_{on} = 3 V		10	1350	—	1000	—	—	800	—	
I_{off}	I_{off}	4	—	1	—	1	—	—	1	µA
I_{off}		10	—	1	—	1	—	—	1	
Output DATA V_{OH} at I_{source} = 1.0 mA	V_{OH}	4	3.2	—	3.0	—	1	2.8	—	V
		10	9.6	—	9.5	—	0.5	9.4	—	
V_{OL} at I_{sink} = 1.0 mA	V_{OL}	4	—	0.8	—	—	1	—	1.2	V
		10	—	0.4	—	—	0.5	—	0.6	
Supply Voltage	V_{DD}	—	4	10	4	—	10	4	10	V
Standby Current	I_{DDSTB}	4	—	—	—	0.02	1	—	—	µA
		10	—	—	—	0.02	1	—	—	
Active Mode Current	I_{DDACT}	4	—	—	—	0.07	1	—	—	mA
		10	—	—	—	0.45	2	—	—	
Oscillator Frequency	f_{osc}	—	—	—	430	—	530	—	—	kHz

CIRCUIT OPERATION

The transmitter emits a 9–bit, labelled A (LSB) to I (MSB), binary code able to encode 512 commands organized as 8 pages of 64 commands. All of these commands are user selectable except the last command (511) which is used as an SST, Start/Stop Transmission code.

Each bit of the transmitted signal is in the form of a biphase pulse code modulated (PCM) signal, whose coding is shown in Figure 1.



* f_1 is a train of pulses at the carrier frequency ÷ 16.

Figure 1. Signal Coding

The keyboard can be a simple switch matrix, connected between the eight row inputs (1 to 8) and the seven column outputs (B to H). V_{SS} acts as the eight column line to give the full complement of 64 commands per page. The maximum "ON" resistance of the keyboard must be limited to 500 Ω.

Page access is accomplished by connecting, by means of a key, the page input to one of the seven column outputs or by leaving the input circuit open.

One of the circuit's major features is its low standby current consumption — typically less than 1 μA. For this reason the battery may be left continuously in circuit.

As soon as a key is selected, the circuit switches to its active mode and enables the oscillator. To allow for accidental activation and/or key bounce, the circuit requires that the key is held for a minimum delay of t_{key}, which in the case of a 500 kHz oscillator is 65.6 ms. After this delay the column/row/page command, consisting of a string of messages (see Figure 2), appropriate to the key selected will be transmitted and repeated until the key is released.

Any page key required must be selected before, and held during, the selection of the column/row matrix key. If this sequence is not followed, the circuit will default to the appropriate command between 0 and 63. If two or more page keys are accidentally held down, only the first one pressed will be detected.

A command consists of several messages. Each command starts with the message 511 (SST) followed by the message appropriate to the key selected. These messages are repeated until the key is released. The final message is always followed by the SST message, 511.

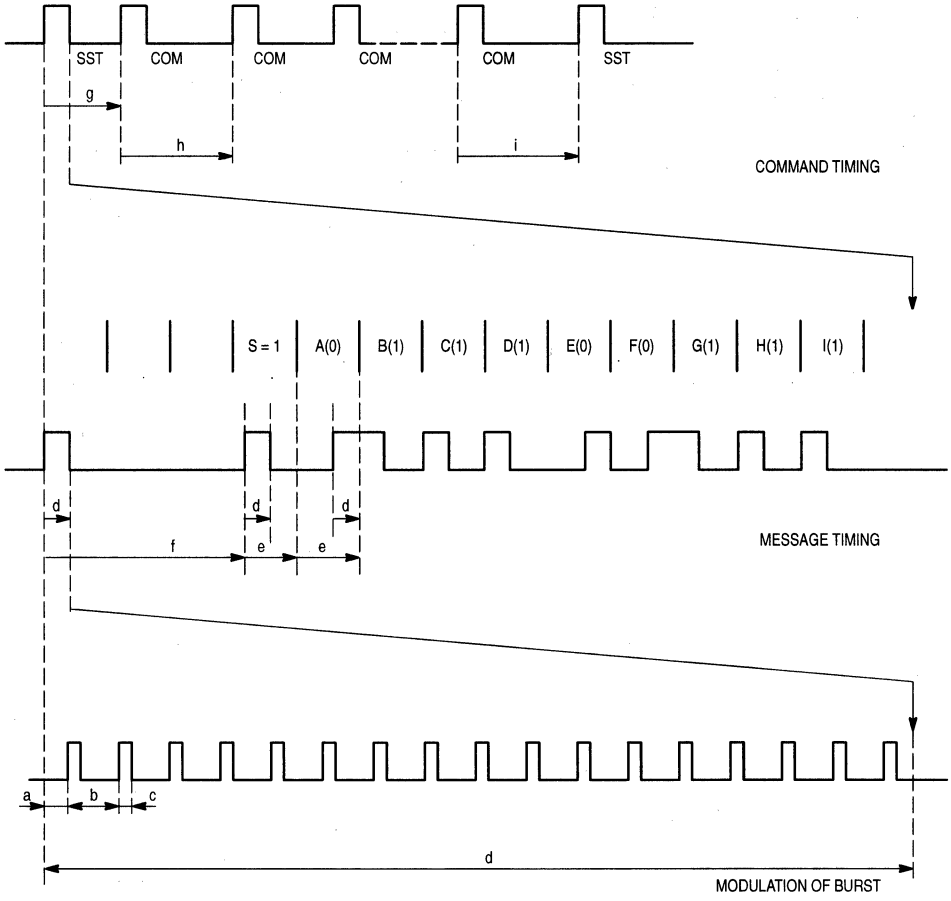
Every message consists of a pre–bit, a pre–bit pause, a start–bit, and nine data bits, where the pre–bit and the start–bit are always logical "1". The pre–bit allows for the set up of the AGC loop in the receiving preamplifier. The truth tables for data bits are given in Tables 1 and 2, while Figure 2 shows the timing relationships between the commands, messages, and modulation.

In the event of accidental multi–key operation, the circuit will react in one of three ways, depending on the combination of the keys selected.

When two or more keys are connected to the same row input and any column output except A, the command appropriate to the first key selected will be transmitted until that key is released. After the SST code has been transmitted, assuming another key is still selected, the command appropriate to that key will be transmitted. If the other key has been released in the meantime, the circuit will revert to standby.

If two keys are selected in the same row with one being connected to column A, any transmission will terminate with the SST code and then the circuit will transmit the command appropriate to the key connected to column A.

In the case where two or more keys connected to the same column are selected, the circuit reacts in a normal manner to the first key activated. Upon selection of the second key, the SST code is transmitted and the circuit will revert to the standby mode. Only when the multi–key condition is released and a single key is selected will the circuit resume operation, as previously described.



CIRCUIT TIMING*

Modulation	$a = 4/f_{osc}$	8 µs	
	$b = 16/f_{osc}$	32 µs	1/f Carrier
	$c = 4/f_{osc}$	8 µs	
	$d = 256/f_{osc}$	512 µs	Half–Bit Time
Message Timing	$d = 256/f_{osc}$	512 µs	Half–Bit Time
	$e = 512/f_{osc}$	1.02 ms	Bit Time
	$f = 1536/f_{osc}$	3.072 ms	Pre–Pulse Time
Command Timing	g = 32 x Bit Time	32.8 ms	
	h = 128 x Bit Time	131 ms	
	i = 128 x Bit Time	131 ms	
	t_{key} = 64 x Bit Time	65.6 ms	

* Times indicated are typical and refer to an oscillator frequency of 500 kHz.

Figure 2. MC44107 Remote Control Transmitter Timing Diagram

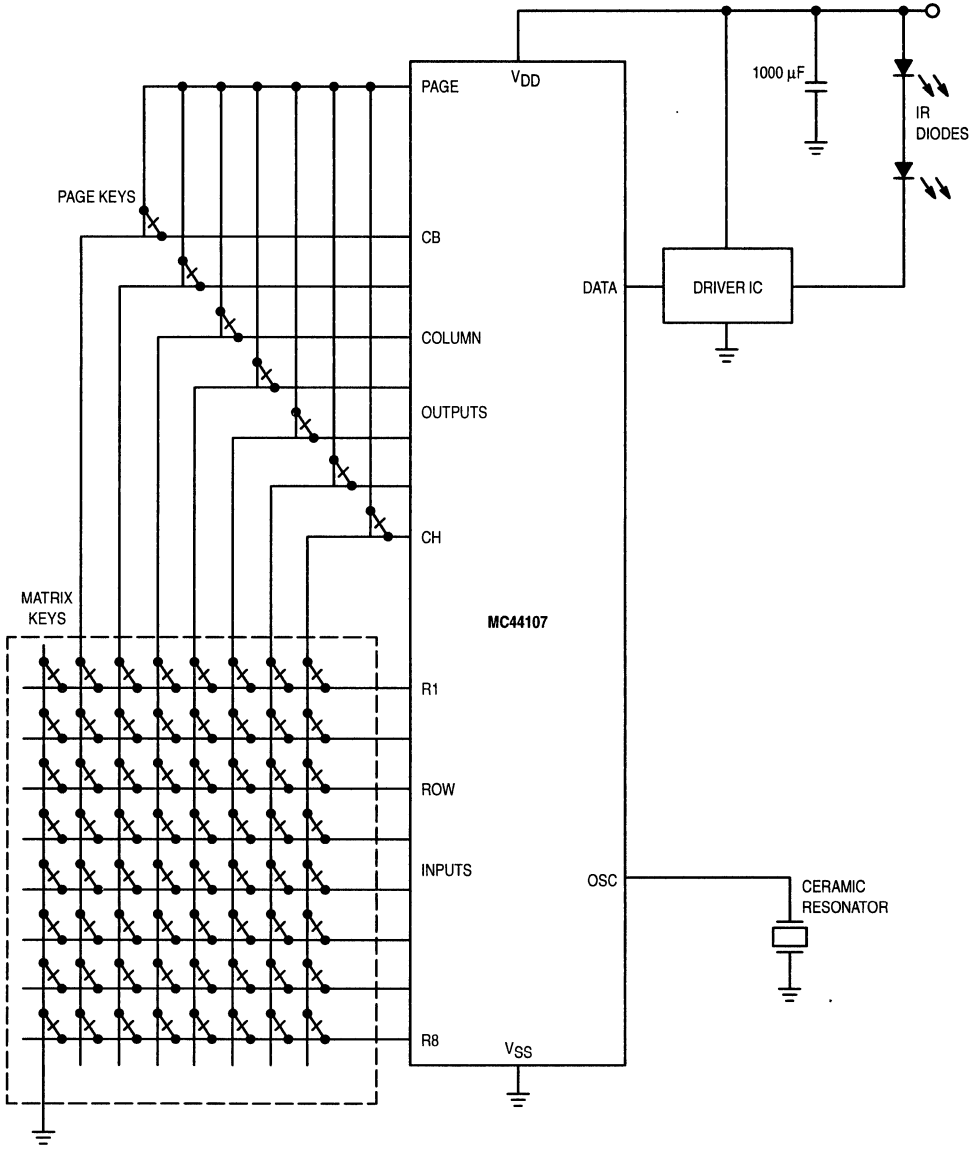


Figure 3. Transmitter Circuit

PIN DESCRIPTIONS

ROW INPUTS

1 to 8 (Pins 1, 2, 3, and 5 – 9) In the standby mode these inputs are held high by internal pull–up resistors. As soon as a key is pressed, a logical "0" is presented by the column output on that particular line. This switches the circuit to the active mode and starts the oscillator.

COLUMN OUTPUTS

B to H (Pins 12 – 16, 18, and 19) In the standby mode these pins are held low, logical "0". When a key is selected and the oscillator starts, the outputs are released and the scanning routine starts.

PAGE INPUT

(Pin 11) This input is connected directly to the transmitter's supervisory and control circuitry and may be connected to one of the column outputs, via a key, or left open. If the pin is left open, the first page of 64 commands will be available (see Table 1). If connected to one of the column outputs, the remaining pages become available (see Table 2). The specified standby current consumption is maintained regardless of the load applied to the input: 0 V < V page < V_{DD}.

OSCILLATOR

(Pin 17) A one–pin oscillator is incorporated into the circuit, which has been specifically designed for use with an inexpensive ceramic resonator between 430 kHz and 530 kHz. It is possible to use a tuned LC circuit with a series capacitor, in place of the ceramic resonator.

DATA OUTPUT

(Pin 4) This output provides the modulated signal for subsequent external amplification.

SPECIAL NOTE: KEYBOARD

It is important, when considering a keyboard, that the maximum "ON" resistance, even after aging, of 500 Ω is strictly observed.

Table 1. Transmitted Codes

Message Number	Matrix Connect Row/Col	Binary Code									Message Number	Matrix Connect Row/Col	Binary Code								
		A	B	C	D	E	F	G	H	I			A	B	C	D	E	F	G	H	I
0	1A	0	0	0	0	0	0	0	0	0	32	5A	0	0	0	0	0	1	0	0	0
1	1B	1	0	0	0	0	0	0	0	0	33	5B	1	0	0	0	0	1	0	0	0
2	1C	0	1	0	0	0	0	0	0	0	34	5C	0	1	0	0	0	1	0	0	0
3	1D	1	1	0	0	0	0	0	0	0	35	5D	1	1	0	0	0	1	0	0	0
4	1E	0	0	1	0	0	0	0	0	0	36	5E	0	0	1	0	0	1	0	0	0
5	1F	1	0	1	0	0	0	0	0	0	37	5F	1	0	1	0	0	1	0	0	0
6	1G	0	1	1	0	0	0	0	0	0	38	5G	0	1	1	0	0	1	0	0	0
7	1H	1	1	1	0	0	0	0	0	0	39	5H	1	1	1	0	0	1	0	0	0
8	2A	0	0	0	1	0	0	0	0	0	40	6A	0	0	0	1	0	1	0	0	0
9	2B	1	0	0	1	0	0	0	0	0	41	6B	1	0	0	1	0	1	0	0	0
10	2C	0	1	0	1	0	0	0	0	0	42	6C	0	1	0	1	0	1	0	0	0
11	2D	1	1	0	1	0	0	0	0	0	43	6D	1	1	0	1	0	1	0	0	0
12	2E	0	0	1	1	0	0	0	0	0	44	6E	0	0	1	1	0	1	0	0	0
13	2F	1	0	1	1	0	0	0	0	0	45	6F	1	0	1	1	0	1	0	0	0
14	2G	0	1	1	1	0	0	0	0	0	46	6G	0	1	1	1	0	1	0	0	0
15	2H	1	1	1	1	0	0	0	0	0	47	6H	1	1	1	1	0	1	0	0	0
16	3A	0	0	0	0	1	0	0	0	0	48	7A	0	0	0	0	1	1	0	0	0
17	3B	1	0	0	0	1	0	0	0	0	49	7B	1	0	0	0	1	1	0	0	0
18	3C	0	1	0	0	1	0	0	0	0	50	7C	0	1	0	0	1	1	0	0	0
19	3D	1	1	0	0	1	0	0	0	0	51	7D	1	1	0	0	1	1	0	0	0
20	3E	0	0	1	0	1	0	0	0	0	52	7E	0	0	1	0	1	1	0	0	0
21	3F	1	0	1	0	1	0	0	0	0	53	7F	1	0	1	0	1	1	0	0	0
22	3G	0	1	1	0	1	0	0	0	0	54	7G	0	1	1	0	1	1	0	0	0
23	3H	1	1	1	0	1	0	0	0	0	55	7H	1	1	1	0	1	1	0	0	0
24	4A	0	0	0	1	1	0	0	0	0	56	8A	0	0	0	1	1	1	0	0	0
25	4B	1	0	0	1	1	0	0	0	0	57	8B	1	0	0	1	1	1	0	0	0
26	4C	0	1	0	1	1	0	0	0	0	58	8C	0	1	0	1	1	1	0	0	0
27	4D	1	1	0	1	1	0	0	0	0	59	8D	1	1	0	1	1	1	0	0	0
28	4E	0	0	1	1	1	0	0	0	0	60	8E	0	0	1	1	1	1	0	0	0
29	4F	1	0	1	1	1	0	0	0	0	61	8F	1	0	1	1	1	1	0	0	0
30	4G	0	1	1	1	1	0	0	0	0	62	8G	0	1	1	1	1	1	0	0	0
31	4H	1	1	1	1	1	0	0	0	0	63	8H	1	1	1	1	1	1	0	0	0

Table 2. Page Table

Message	Page Input Connected To	G	H	I
0 to 63	Not Connected	0	0	0
64 to 127	CB	1	0	0
128 to 191	CC	0	1	0
192 to 255	CD	1	1	0
256 to 319	CE	0	0	1
320 to 383	CF	1	0	1
384 to 447	CG	0	1	1
448 to 511	CH	1	1	1

MC144110
MC144111

Digital-to-Analog Converters with Serial Interface

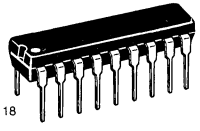
CMOS LSI

The MC144110 and MC144111 are low–cost 6–bit D/A converters with serial interface ports to provide communication with CMOS microprocessors and microcomputers. The MC144110 contains six static D/A converters; the MC144111 contains four converters.

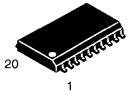
Due to a unique feature of these DACs, the user is permitted easy scaling of the analog outputs of a system. Over a 5 to 15 V supply range, these DACs may be directly interfaced to CMOS MPUs operating at 5 V.

- Direct R–2R Network Outputs
- Buffered Emitter–Follower Outputs
- Serial Data Input
- Digital Data Output Facilitates Cascading
- Direct Interface to CMOS µP
- Wide Operating Voltage Range: 4.5 to 15 V
- Wide Operating Temperature Range: 0 to 85°C
- Software Information is Contained in Document M68HC11RM/AD

MC144110

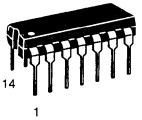


P SUFFIX
PLASTIC DIP
CASE 707

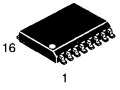


DW SUFFIX
SOG PACKAGE
CASE 751D

MC144111



P SUFFIX
PLASTIC DIP
CASE 646

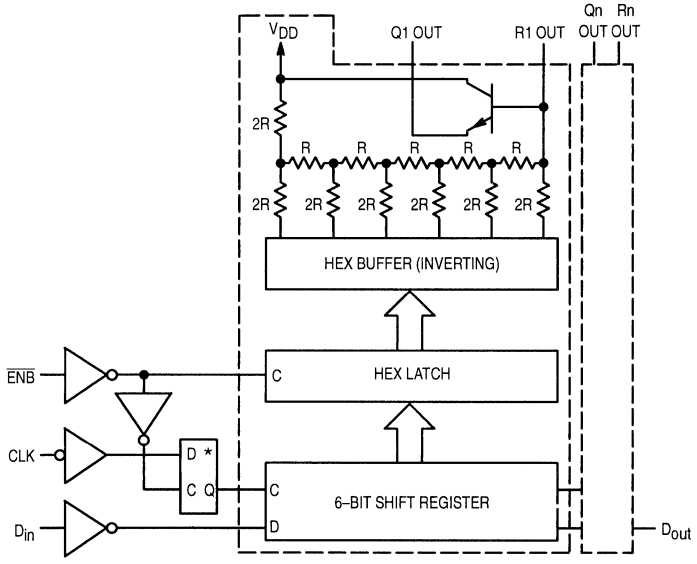


DW SUFFIX
SOG PACKAGE
CASE 751G

ORDERING INFORMATION

MC144110P	Plastic DIP
MC144110DW	SOG Package
MC144111P	Plastic DIP
MC144111DW	SOG Package

BLOCK DIAGRAM

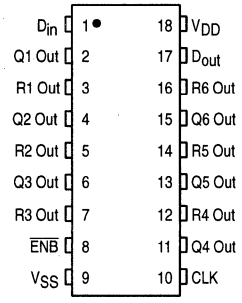


* Transparent Latch

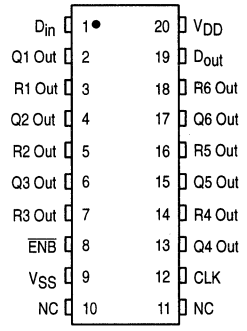
REV 1
8/95

PIN ASSIGNMENTS

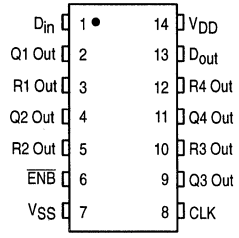
MC144110P



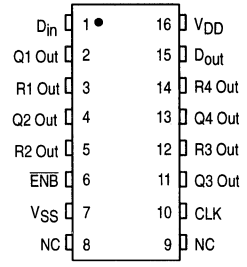
MC144110DW



MC144111P



MC144111DW



NC = NO CONNECTION

MAXIMUM RATINGS* (Voltages referenced to V_{SS})

Parameter	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	– 0.5 to + 18	V
Input Voltage, All Inputs	V_{in}	– 0.5 to V_{DD} + 0.5	V
DC Input Current, per Pin	I	± 10	mA
Power Dissipation (Per Output) T_A = 70°C, MC144110 MC144111 T_A = 85°C, MC144110 MC144111	P_{OH}	 30 50 10 20	mW
Power Dissipation (Per Package) T_A = 70°C, MC144110 MC144111 T_A = 85°C, MC144110 MC144111	P_D	 100 150 25 50	mW
Storage Temperature Range	T_{stg}	– 65 to + 150	°C

* Maximum Ratings are those values beyond which damage to the device may occur.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields; however, it is advised that precautions be taken to avoid application of voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

2

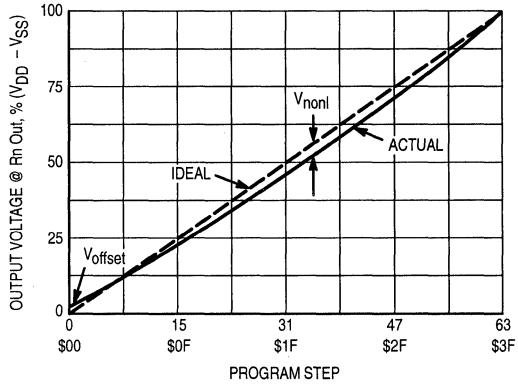
ELECTRICAL CHARACTERISTICS (Voltages referenced to V_{SS}, T_A = 0 to 85°C unless otherwise indicated)

Symbol	Parameter	Test Conditions	V_{DD}	Min	Max	Unit
V_{IH}	High–Level Input Voltage (D_{in}, $\overline{ENB}$, CLK)		5 10 15	3.0 3.5 4	— — —	V
V_{IL}	Low–Level Input Voltage (D_{in}, $\overline{ENB}$, CLK)		5 10 15	— — —	0.8 0.8 0.8	V
I_{OH}	High–Level Output Current (D_{out})	$V_{out} = V_{DD} - 0.5$ V	5	– 200	—	µA
I_{OL}	Low–Level Output Current (D_{out})	V_{out} = 0.5 V	5	200	—	µA
I_{DD}	Quiescent Supply Current MC144110 MC144111	I_{out} = 0 µA	15 15	— —	12 8	mA
I_{in}	Input Leakage Current (D_{in}, $\overline{ENB}$, CLK)	$V_{in} = V_{DD}$ or 0 V	15	—	± 1	µA
V_{nonl}	Nonlinearity Voltage (Rn Out)	See Figure 1	5 10 15	— — —	100 200 300	mV
V_{step}	Step Size (Rn Out)	See Figure 2	5 10 15	19 39 58	137 274 411	mV
V_{offset}	Offset Voltage from V_{SS}	D_{in} = $00, See Figure 1	—	—	1	LSB
I_E	Emitter Leakage Current	$V_{Rn\ Out}$ = 0 V	15	—	10	µA
h_{FE}	DC Current Gain	I_E = 0.1 to 10.0 mA T_A = 25°C	—	40	—	—
V_{BE}	Base–to–Emitter Voltage Drop	I_E = 1.0 mA	—	0.4	0.7	V

SWITCHING CHARACTERISTICS

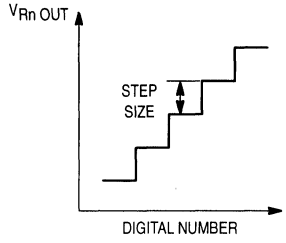
(Voltages referenced to V_{SS}, T_A = 0 to 85°C, C_L = 50 pF, Input $t_r = t_f$ = 20 ns unless otherwise indicated)

Symbol	Parameter	V_{DD}	Min	Max	Unit
t_{wH}	Positive Pule Width, CLK (Figures 3 and 4)	5 10 15	2 1.5 1	— — —	µs
t_{wL}	Negative Pulse Width, CLK (Figure 3 and 4)	5 10 15	5 3.5 2	— — —	µs
t_{su}	Setup Time, $\overline{ENB}$ to CLK (Figures 3 and 4)	5 10 15	5 3.5 2	— — —	µs
t_{su}	Setup Time, D_{in} to CLK (Figures 3 and 4)	5 10 15	1000 750 500	— — —	ns
t_h	Hold Time, CLK to $\overline{ENB}$ (Figures 3 and 4)	5 10 15	5 3.5 2	— — —	µs
t_h	Hold Time, CLK to D_{in} (Figures 3 and 4)	5 10 15	5 3.5 2	— — —	µs
t_r, t_f	Input Rise and Fall Times	5 – 15	—	2	µs
C_{in}	Input Capacitance	5 – 15	—	7.5	pF



LINEARITY ERROR (integral linearity). A measure of how straight a device's transfer function is, it indicates the worst–case deviation of linearity of the actual transfer function from the best–fit straight line. It is normally specified in parts of an LSB.

Figure 1. D/A Transfer Function



$$\text{Step Size} = \frac{V_{DD}}{64} \pm 0.75\,\frac{V_{DD}}{64}$$

(For any adjacent pair of digital numbers)

Figure 2. Definition of Step Size

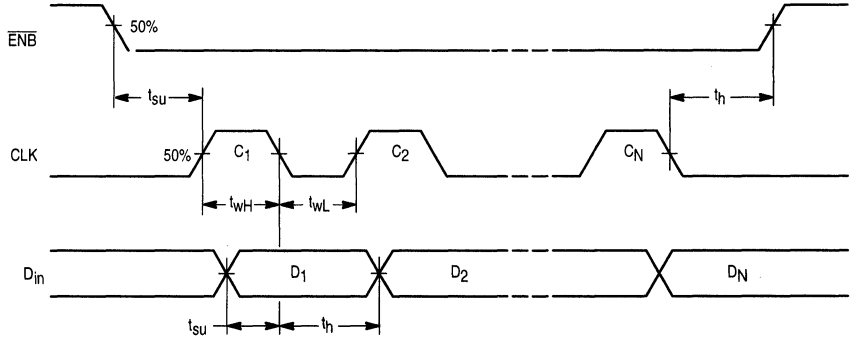


Figure 3. Serial Input, Positive Clock

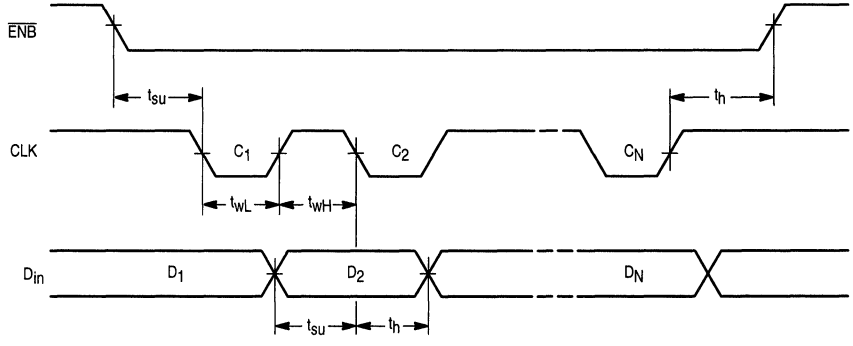


Figure 4. Serial Input, Negative Clock

PIN DESCRIPTIONS

INPUTS

D_{in}
Data Input

Six–bit words are entered serially, MSB first, into digital data input, D_{in}. Six words are loaded into the MC144110 during each D/A cycle; four words are loaded into the MC144111.

The last 6–bit word shifted in determines the output level of pins Q1 Out and R1 Out. The next–to–last 6–bit word affects pins Q2 Out and R2 Out, etc.

$\overline{ENB}$
Negative Logic Enable

The $\overline{ENB}$ pin must be low (active) during the serial load. On the low–to–high transition of $\overline{ENB}$, data contained in the shift register is loaded into the latch.

CLK
Shift Register Clock

Data is shifted into the register on the high–to–low transition of CLK. CLK is fed into the D–input of a transparent latch, which is used for inhibiting the clocking of the shift register when $\overline{ENB}$ is high.

The number of clock cycles required for the MC144110 is usually 36. The MC144111 usually uses 24 cycles. See Table 1 for additional information.

OUTPUTS

D_{out}
Data Output

The digital data output is primarily used for cascading the DACs and may be fed into D_{in} of the next stage.

R1 Out through Rn Out
Resistor Network Outputs

These are the R–2R resistor network outputs. These outputs may be fed to high–impedance input FET op amps to bypass the on–chip bipolar transistors. The R value of the resistor network ranges from 7 to 15 kΩ.

Q1 Out through Qn Out
NPN Transistor Outputs

Buffered DAC outputs utilize an emitter–follower configuration for current–gain, thereby allowing interface to low–impedance circuits.

SUPPLY PINS

V_{SS}
Negative Supply Voltage

This pin is usually ground.

V_{DD}
Positive Supply Voltage

The voltage applied to this pin is used to scale the analog output swing from 4.5 to 15 V p–p.

Table 3. Number of Channels vs Clocks Required

Number of Channels Required	Number of Clock Cycles	Outputs Used on MC144110	Outputs Used on MC144111
1	6	Q1/R1	Q1/R1
2	12	Q1/R1, Q2/R2	Q1/R1, Q2/R2
3	18	Q1/R1, Q2/R2, Q3/R3	Q1/R1, Q2/R2, Q3/R3
4	24	Q1/R1, Q2/R2, Q3/R3, Q4/R4	Q1/R1, Q2/R2, Q3/R3, Q4/R4
5	30	Q1/R1, Q2/R2, Q3/R3, Q4/R4, Q5/R5	Not Applicable
6	36	Q1/R1, Q2/R2, Q3/R3, Q4/R4, Q5/R5, Q6/R6	Not Applicable

MC145026
MC145027
MC145028
SC41343
SC41344

2

Encoder and Decoder Pairs
CMOS

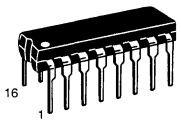
These devices are designed to be used as encoder/decoder pairs in remote control applications.

The MC145026 encodes nine lines of information and serially sends this information upon receipt of a transmit enable ($\overline{TE}$) signal. The nine lines may be encoded with trinary data (low, high, or open) or binary data (low or high). The words are transmitted twice per encoding sequence to increase security.

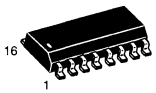
The MC145027 decoder receives the serial stream and interprets five of the trinary digits as an address code. Thus, 243 addresses are possible. If binary data is used at the encoder, 32 addresses are possible. The remaining serial information is interpreted as four bits of binary data. The valid transmission (VT) output goes high on the MC145027 when two conditions are met. First, two addresses must be consecutively received (in one encoding sequence) which both match the local address. Second, the 4 bits of data must match the last valid data received. The active VT indicates that the information at the Data output pins has been updated.

The MC145028 decoder treats all nine trinary digits as an address which allows 19,683 codes. If binary data is encoded, 512 codes are possible. The VT output goes high on the MC145028 when two addresses are consecutively received (in one encoding sequence) which both match the local address.

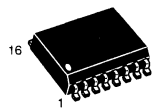
- Operating Temperature Range: – 40 to + 85°C
- Very–Low Standby Current for the Encoder: 300 nA Maximum @ 25°C
- Interfaces with RF, Ultrasonic, or Infrared Modulators and Demodulators
- RC Oscillator, No Crystal Required
- High External Component Tolerance; Can Use ± 5% Components
- Internal Power–On Reset Forces All Decoder Outputs Low
- For Infrared Applications, See Applications Notes AN1016 and AN1126
- Operating Voltage Range: MC145026 = 2.5 to 18 V*
  MC145027, MC145028 = 4.5 to 18 V
- Low–Voltage Versions Available:
  SC41343 = 2.8 to 10 V Version of the MC145027
  SC41344 = 2.8 to 10 V Version of the MC145028



P SUFFIX
PLASTIC DIP
CASE 648



D SUFFIX
SOG PACKAGE
CASE 751B

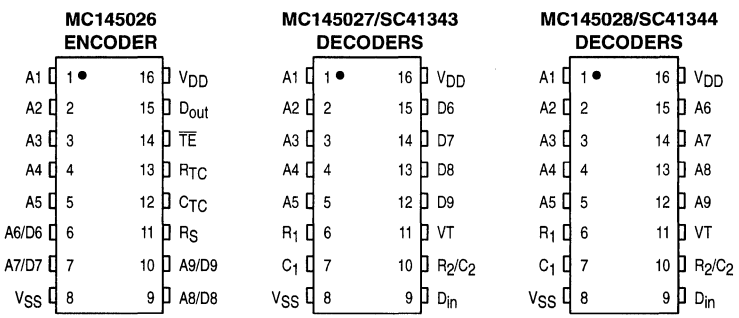


DW SUFFIX
SOG PACKAGE
CASE 751G

ORDERING INFORMATION

MC145026P	Plastic DIP
MC145026D	SOG Package
MC145027P, SC41343P	Plastic DIP
MC145027DW, SC41343DW	SOG Package
MC145028P, SC41344P	Plastic DIP
MC145028DW, SC41344DW	SOG Package

PIN ASSIGNMENTS



* All MC145026 devices manufactured after date code 9314 or 314 are guaranteed over this wider voltage range. All previous designs using the low–voltage SC41342 should convert to the MC145026, which is a drop–in replacement. The SC41342 part number will be discontinued.

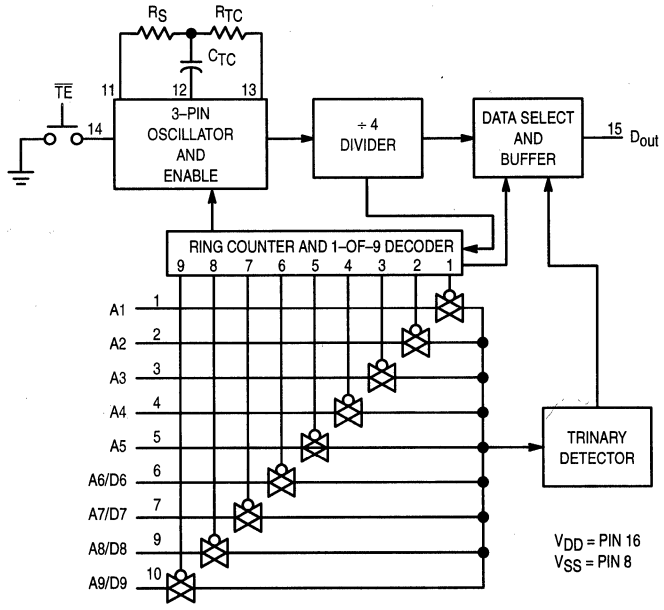


Figure 1. MC145026 Encoder Block Diagram

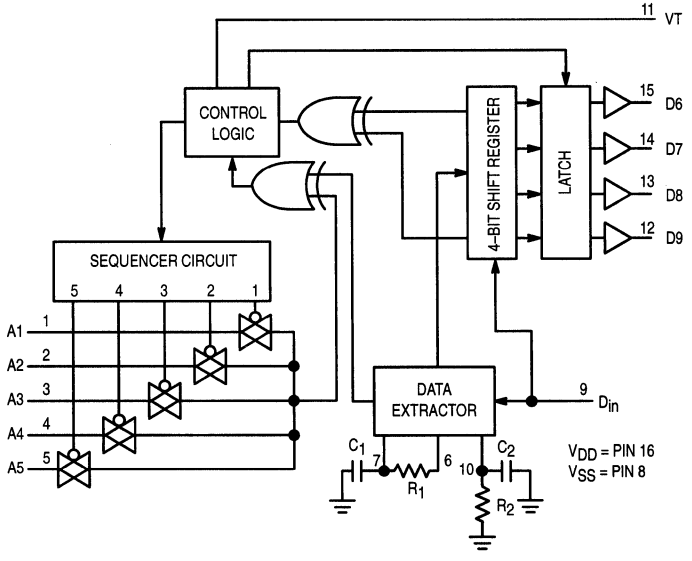


Figure 2. MC145027 Decoder Block Diagram

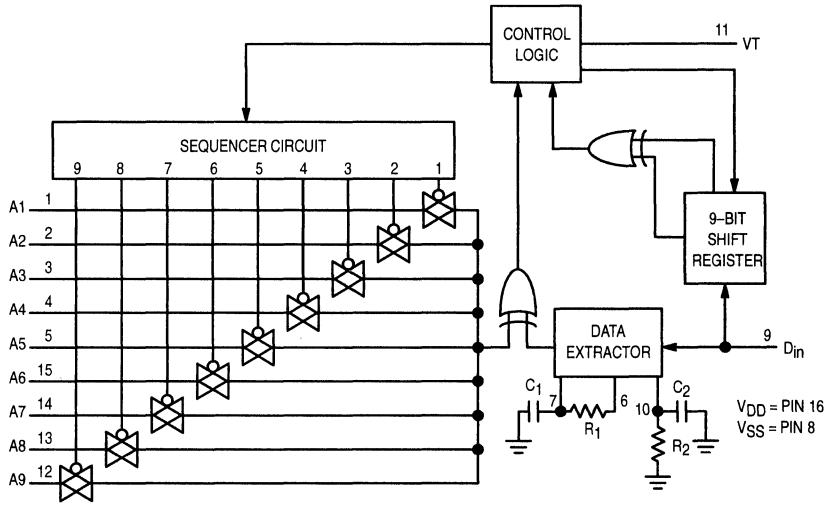


Figure 3. MC145028 Decoder Block Diagram

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Rating	Symbol	Value	Unit
V_{DD}	DC Supply Voltage (except SC41343, SC41344)	– 0.5 to + 18	V
V_{DD}	DC Supply Voltage (SC41343, SC41344 only)	– 0.5 to + 10	V
V_{in}	DC Input Voltage	– 0.5 to V_{DD} + 0.5	V
V_{out}	DC Output Voltage	– 0.5 to V_{DD} + 0.5	V
I_{in}	DC Input Current, per Pin	± 10	mA
I_{out}	DC Output Current, per Pin	± 10	mA
P_D	Power Dissipation, per Package	500	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds	260	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Descriptions section.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

ELECTRICAL CHARACTERISTICS — MC145026*, MC145027, and MC145028 (Voltage Referenced to V_{SS})

Symbol	Characteristic	V_{DD} V	Guaranteed Limit – 40°C Min	– 40°C Max	25°C Min	25°C Max	85°C Min	85°C Max	Unit
V_{OL}	Low–Level Output Voltage (V_{in} = V_{DD} or 0)	5.0	—	0.05	—	0.05	—	0.05	V
		10	—	0.05	—	0.05	—	0.05	
		15	—	0.05	—	0.05	—	0.05	
V_{OH}	High–Level Output Voltage (V_{in} = 0 or V_{DD})	5.0	4.95	—	4.95	—	4.95	—	V
		10	9.95	—	9.95	—	9.95	—	
		15	14.95	—	14.95	—	14.95	—	
V_{IL}	Low–Level Input Voltage								V
	(V_{out} = 4.5 or 0.5 V)	5.0	—	1.5	—	1.5	—	1.5	
	(V_{out} = 9.0 or 1.0 V)	10	—	3.0	—	3.0	—	3.0	
	(V_{out} = 13.5 or 1.5 V)	15	—	4.0	—	4.0	—	4.0	
V_{IH}	High–Level Input Voltage								V
	(V_{out} = 0.5 or 4.5 V)	5.0	3.5	—	3.5	—	3.5	—	
	(V_{out} = 1.0 or 9.0 V)	10	7.0	—	7.0	—	7.0	—	
	(V_{out} = 1.5 or 13.5 V)	15	11	—	11	—	11	—	
I_{OH}	High–Level Output Current								mA
	(V_{out} = 2.5 V)	5.0	– 2.5	—	– 2.1	—	– 1.7	—	
	(V_{out} = 4.6 V)	5.0	– 0.52	—	– 0.44	—	– 0.36	—	
	(V_{out} = 9.5 V)	10	– 1.3	—	– 1.1	—	– 0.9	—	
	(V_{out} = 13.5 V)	15	– 3.6	—	– 3.0	—	– 2.4	—	
I_{OL}	Low–Level Output Current								mA
	(V_{out} = 0.4 V)	5.0	0.52	—	0.44	—	0.36	—	
	(V_{out} = 0.5 V)	10	1.3	—	1.1	—	0.9	—	
	(V_{out} = 1.5 V)	15	3.6	—	3.0	—	2.4	—	
I_{in}	Input Current — $\overline{TE}$	5.0	—	—	3.0	11	—	—	μA
	(MC145026, Pull–Up Device)	10	—	—	16	60	—	—	
		15	—	—	35	120	—	—	
I_{in}	Input Current	15	—	± 0.3	—	± 0.3	—	± 1.0	μA
	R_S (MC145026), D_{in} (MC145027, MC145028)								
I_{in}	Input Current								μA
	A1 – A5, A6/D6 – A9/D9 (MC145026),	5.0	—	—	—	± 110	—	—	
	A1 – A5 (MC145027),	10	—	—	—	± 500	—	—	
	A1 – A9 (MC145028)	15	—	—	—	± 1000	—	—	
C_{in}	Input Capacitance (V_{in} = 0)	—	—	—	—	7.5	—	—	pF
I_{DD}	Quiescent Current — MC145026	5.0	—	—	—	0.1	—	—	μA
		10	—	—	—	0.2	—	—	
		15	—	—	—	0.3	—	—	
I_{DD}	Quiescent Current — MC145027, MC145028	5.0	—	—	—	50	—	—	μA
		10	—	—	—	100	—	—	
		15	—	—	—	150	—	—	
I_{dd}	Dynamic Supply Current — MC145026	5.0	—	—	—	200	—	—	μA
	(f_c = 20 kHz)	10	—	—	—	400	—	—	
		15	—	—	—	600	—	—	
I_{dd}	Dynamic Supply Current — MC145027, MC145028	5.0	—	—	—	400	—	—	μA
	(f_c = 20 kHz)	10	—	—	—	800	—	—	
		15	—	—	—	1200	—	—	

* Also see next Electrical Characteristics table for 2.5 V specifications.

ELECTRICAL CHARACTERISTICS — MC145026 (Voltage Referenced to V_{SS})

Symbol	Characteristic	V_{DD} V	Guaranteed Limit						Unit
			– 40°C		25°C		85°C		
			Min	Max	Min	Max	Min	Max	
V_{OL}	Low–Level Output Voltage (V_{in} = 0 V or V_{DD})	2.5	—	0.05	—	0.05	—	0.05	V
V_{OH}	High–Level Output Voltage (V_{in} = 0 V or V_{DD})	2.5	2.45	—	2.45	—	2.45	—	V
V_{IL}	Low–Level Input Voltage (V_{out} = 0.5 V or 2.0 V)	2.5	—	0.3	—	0.3	—	0.3	V
V_{IH}	High–Level Input Voltage (V_{out} = 0.5 V or 2.0 V)	2.5	2.2	—	2.2	—	2.2	—	V
I_{OH}	High–Level Output Current (V_{out} = 1.25 V)	2.5	0.28	—	0.25	—	0.2	—	mA
I_{OL}	Low–Level Output Current (V_{out} = 0.4 V)	2.5	0.22	—	0.2	—	0.16	—	mA
I_{in}	Input Current ($\overline{TE}$ — Pull–Up Device)	2.5	—	—	0.09	1.8	—	—	µA
I_{in}	Input Current (A1–A5, A6/D6–A9/D9)	2.5	—	—	—	± 25	—	—	µA
I_{DD}	Quiescent Current	2.5	—	—	—	0.05	—	—	µA
I_{dd}	Dynamic Supply Current (f_c = 20 kHz)	2.5	—	—	—	40	—	—	µA

ELECTRICAL CHARACTERISTICS — SC41343 and SC41344 (Voltage Referenced to V_{SS})

Symbol	Characteristic	V_{DD} V	Guaranteed Limit						Unit
			– 40°C		25°C		85°C		
			Min	Max	Min	Max	Min	Max	
V_{OL}	Low–Level Output Voltage (V_{in} = 0 V or V_{DD})	2.8	—	0.05	—	0.05	—	0.05	V
		5.0	—	0.05	—	0.05	—	0.05	
		10	—	0.05	—	0.05	—	0.05	
V_{OH}	High–Level Output Voltage (V_{in} = 0 V or V_{DD})	2.8	2.75	—	2.75	—	2.75	—	V
		5.0	4.95	—	4.95	—	4.95	—	
		10	9.95	—	9.95	—	9.95	—	
V_{IL}	Low–Level Input Voltage								V
	(V_{out} = 2.3 V or 0.5 V)	2.8	—	0.84	—	0.84	—	0.84	
	(V_{out} = 4.5 V or 0.5 V)	5.0	—	1.5	—	1.5	—	1.5	
	(V_{out} = 9.0 V or 1.0 V)	10	—	3.0	—	3.0	—	3.0	
V_{IH}	High–Level Input Voltage								V
	(V_{out} = 0.5 V or 2.3 V)	2.8	1.96	—	1.96	—	1.96	—	
	(V_{out} = 0.5 V or 4.5 V)	5.0	3.5	—	3.5	—	3.5	—	
	(V_{out} = 1.0 V or 9.0 V)	10	7.0	—	7.0	—	7.0	—	
I_{OH}	High–Level Output Current								mA
	(V_{out} = 1.4 V)	2.8	– 0.73	—	– 0.7	—	– 0.55	—	
	(V_{out} = 4.5 V)	5.0	– 0.59	—	– 0.5	—	– 0.41	—	
	(V_{out} = 9.0 V)	10	– 1.3	—	– 1.1	—	– 0.9	—	
I_{OL}	Low–Level Output Current								mA
	(V_{out} = 0.4 V)	2.8	0.35	—	0.3	—	0.24	—	
	(V_{out} = 0.5 V)	5.0	0.8	—	0.6	—	0.4	—	
	(V_{out} = 1.0 V)	10	3.5	—	2.9	—	2.3	—	
I_{in}	Input Current — D_{in}	10	—	± 0.3	—	± 0.3	—	± 1.0	µA
I_{in}	Input Current	2.8	—	—	—	± 30	—	—	µA
	A1 – A5 (SC41343)	5.0	—	—	—	± 140	—	—	
	A1 – A9 (SC41344)	10	—	—	—	± 600	—	—	
C_{in}	Input Capacitance (V_{in} = 0)	—	—	—	—	7.5	—	—	pF
I_{DD}	Quiescent Current	2.8	—	—	—	60	—	—	µA
		5.0	—	—	—	75	—	—	
		10	—	—	—	150	—	—	
I_{dd}	Dynamic Supply Current (f_c = 20 kHz)	2.8	—	—	—	300	—	—	µA
		5.0	—	—	—	500	—	—	
		10	—	—	—	1000	—	—	

SWITCHING CHARACTERISTICS — MC145026*, MC145027, and MC145028 (C_L = 50 pF, T_A = 25°C)

Symbol	Characteristic	Figure No.	V_{DD}	Guaranteed Limit		Unit
				Min	Max	
t_{TLH}, t_{THL}	Output Transition Time	4,8	5.0 10 15	— — —	200 100 80	ns
t_r	D_{in} Rise Time — Decoders	5	5.0 10 15	— — —	15 15 15	µs
t_f	D_{in} Fall Time — Decoders	5	5.0 10 15	— — —	15 5.0 4.0	µs
f_{osc}	Encoder Clock Frequency	6	5.0 10 15	0.001 0.001 0.001	2.0 5.0 10	MHz
f	Decoder Frequency — Referenced to Encoder Clock	12	5.0 10 15	1.0 1.0 1.0	240 410 450	kHz
t_W	$\overline{TE}$ Pulse Width — Encoders	7	5.0 10 15	65 30 20	— — —	ns

* Also see next Switching Characteristics table for 2.5 V specifications.

SWITCHING CHARACTERISTICS — MC145026 (C_L = 50 pF, T_A = 25°C)

Symbol	Characteristic	Figure No.	V_{DD}	Guaranteed Limit		Unit
				Min	Max	
t_{TLH}, t_{THL}	Output Transition Time	4, 8	2.5	—	450	ns
f_{osc}	Encoder Clock Frequency	6	2.5	1.0	250	kHz
t_W	$\overline{TE}$ Pulse Width	7	2.5	1.5	—	µs

SWITCHING CHARACTERISTICS — SC41343 and SC41344 (C_L = 50 pF, T_A = 25°C)

Symbol	Characteristic	Figure No.	V_{DD}	Guaranteed Limit		Unit
				Min	Max	
t_{TLH}, t_{THL}	Output Transition Time	4, 8	2.8 5.0 10	— — —	320 200 100	ns
t_r	D_{in} Rise Time	5	2.8 5.0 10	— — —	15 15 15	µs
t_f	D_{in} Fall Time	5	2.8 5.0 10	— — —	15 15 5.0	µs
f	Decoder Frequency — Referenced to Encoder Clock	12	2.8 5.0 10	1.0 1.0 1.0	100 240 410	kHz

Figure 4.

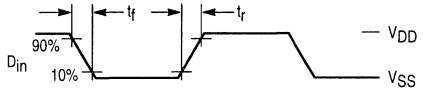


Figure 5.

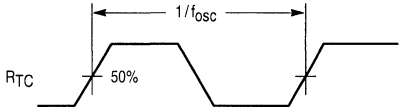


Figure 6.

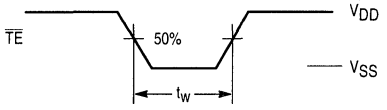
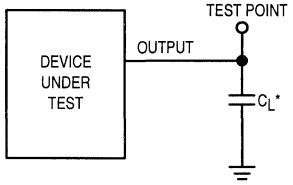


Figure 7.



* Includes all probe and fixture capacitance.

Figure 8. Test Circuit

OPERATING CHARACTERISTICS

MC145026

The encoder serially transmits trinary data as defined by the state of the A1 – A5 and A6/D6 – A9/D9 input pins. These pins may be in either of three states (low, high, or open) allowing 19,683 possible codes. The transmit sequence is initiated by a low level on the $\overline{TE}$ input pin. Upon power–up, the MC145026 can continuously transmit as long as $\overline{TE}$ remains low (also, the device can transmit two–word sequences by pulsing $\overline{TE}$ low). However, no MC145026 application should be designed to rely upon the first data word transmitted immediately after power–up because this word may be invalid. Between the two data words, no signal is sent for three data periods (see Figure 10).

Each transmitted trinary digit is encoded into pulses (see Figure 11). A logic 0 (low) is encoded as two consecutive short pulses, a logic 1 (high) as two consecutive long pulses, and an open (high impedance) as a long pulse followed by a short pulse. The input state is determined by using a weak "output" device to try to force each input high then low. If only a high state results from the two tests, the input is assumed to be hardwired to V_{DD}. If only a low state is obtained, the input is assumed to be hardwired to V_{SS}. If both a high and a low can be forced at an input, an open is assumed and is encoded as such. The "high" and "low" levels are 70% and 30% of the supply voltage as shown in the Electrical Characteristics table. The weak "output" device sinks/sources up to 110 μA at a 5 V supply level, 500 μA at 10 V, and 1 mA at 15 V.

The $\overline{TE}$ input has an internal pull–up device so that a simple switch may be used to force the input low. While $\overline{TE}$ is high, the encoder is completely disabled, the oscillator is inhibited, and the current drain is reduced to quiescent current. When $\overline{TE}$ is brought low, the oscillator is started and the transmit sequence begins. The inputs are then sequentially selected, and determinations are made as to the input logic states. This information is serially transmitted via the D_{out} pin.

MC145027

This decoder receives the serial data from the encoder and outputs the data, if it is valid. The transmitted data, consisting of two identical words, is examined bit by bit during reception. The first five trinary digits are assumed to be the address. If the received address matches the local address, the next four (data) bits are internally stored, but are not transferred to the output data latch. As the second encoded word is received, the address must again match. If a match occurs, the new data bits are checked against the previously stored data bits. If the two nibbles of data (four bits each) match, the data is transferred to the output data latch by VT and remains until new data replaces it. At the same time, the VT output pin is brought high and remains high until an error is received or until no input signal is received for four data periods (see Figure 10).

Although the address information may be encoded in trinary, the data information must be either a 1 or 0. A trinary (open) data line is decoded as a logic 1.

MC145028

This decoder operates in the same manner as the MC145027 except that nine address lines are used and no data output is available. The VT output is used to indicate that a valid address has been received. For transmission security, two identical transmitted words must be consecutively received before a VT output signal is issued.

The MC145028 allows 19,683 addresses when trinary levels are used. 512 addresses are possible when binary levels are used.

PIN DESCRIPTIONS

MC145026 ENCODER

A1 – A5, A6/D6 – A9/D9
Address, Address/Data Inputs (Pins 1 – 7, 9, and 10)

These address/data inputs are encoded and the data is sent serially from the encoder via the D_{out} pin.

R_S, C_{TC}, R_{TC}
(Pins 11, 12, and 13)

These pins are part of the oscillator section of the encoder (see Figure 9).

If an external signal source is used instead of the internal oscillator, it should be connected to the R_S input and the R_{TC} and C_{TC} pins should be left open.

$\overline{TE}$
Transmit Enable (Pin 14)

This active–low transmit enable input initiates transmission when forced low. An internal pull–up device keeps this input normally high. The pull–up current is specified in the Electrical Characteristics table.

D_{out}
Data Out (Pin 15)

This is the output of the encoder that serially presents the encoded data word.

V_{SS}
Negative Power Supply (Pin 8)

The most–negative supply potential. This pin is usually ground.

V_{DD}
Positive Power Supply (Pin 16)

The most–positive power supply pin.

MC145027 AND MC145028 DECODERS

A1 – A5, A1 – A9
Address Inputs (Pins 1 – 5) — MC145027,
Address Inputs (Pins 1 – 5, 15, 14, 13, 12) — MC145028

These are the local address inputs. The states of these pins must match the appropriate encoder inputs for the VT pin to go high. The local address may be encoded with trinary or binary data.

D6 – D9
Data Outputs (Pins 15, 14, 13, 12) — MC145027 Only

These outputs present the binary information that is on encoder inputs A6/D6 through A9/D9. Only binary data is

acknowledged; a trinary open at the MC145026 encoder is decoded as a high level (logic 1).

D_{in}
Data In (Pin 9)

This pin is the serial data input to the decoder. The input voltage must be at CMOS logic levels. The signal source driving this pin must be dc coupled.

R_1, C_1
Resistor 1, Capacitor 1 (Pins 6, 7)

As shown in Figures 2 and 3, these pins accept a resistor and capacitor that are used to determine whether a narrow pulse or wide pulse has been received. The time constant $R_1 \times C_1$ should be set to 1.72 encoder clock periods:

$$R_1 C_1 = 3.95 R_{TC} C_{TC}$$

R_2/C_2
Resistor 2/Capacitor 2 (Pin 10)

As shown in Figures 2 and 3, this pin accepts a resistor and capacitor that are used to detect both the end of a received word and the end of a transmission. The time constant $R_2 \times C_2$ should be 33.5 encoder clock periods (four data periods per Figure 11): $R_2 C_2 = 77 R_{TC} C_{TC}$. This time constant is used to determine whether the D_{in} pin has remained low for four data periods (end of transmission). A separate on–chip comparator looks at the voltage–equivalent two data periods ($0.4 R_2 C_2$) to detect the dead time between received words within a transmission.

VT
Valid Transmission Output (Pin 11)

This valid transmission output goes high after the second word of an encoding sequence when the following conditions are satisfied:

1. the received addresses of both words match the local decoder address, and
2. the received data bits of both words match.

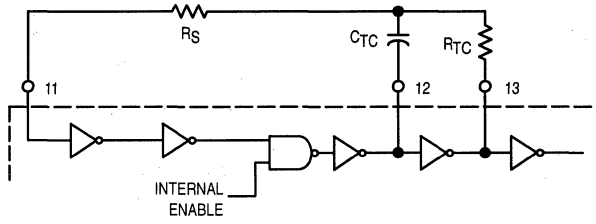
VT remains high until either a mismatch is received or no input signal is received for four data periods.

V_{SS}
Negative Power Supply (Pin 8)

The most–negative supply potential. This pin is usually ground.

V_{DD}
Positive Power Supply (Pin 16)

The most–positive power supply pin.



2

This oscillator operates at a frequency determined by the external RC network; i.e.,

$$f \approx \frac{1}{2.3\ R_{TC}\ C_{TC'}} \text{ (Hz)}$$

for 1 kHz ≤ f ≤ 400 kHz

where: $C_{TC'} = C_{TC} + C_{layout} + 12$ pF
$R_S \approx 2\ R_{TC}$
$R_S \geq 20$ k
$R_{TC} \geq 10$ k
400 pF < C_{TC} < 15 µF

The value for R_S should be chosen to be ≥ 2 times R_{TC}. This range ensures that current through R_S is insignificant compared to current through R_{TC}. The upper limit for R_S must ensure that R_S x 5 pF (input capacitance) is small compared to R_{TC} x C_{TC}.

For frequencies outside the indicated range, the formula is less accurate. The minimum recommended oscillation frequency of this circuit is 1 kHz. Susceptibility to externally induced noise signals may occur for frequencies below 1 kHz and/or when resistors utilized are greater than 1 MΩ.

Figure 9. Encoder Oscillator Information

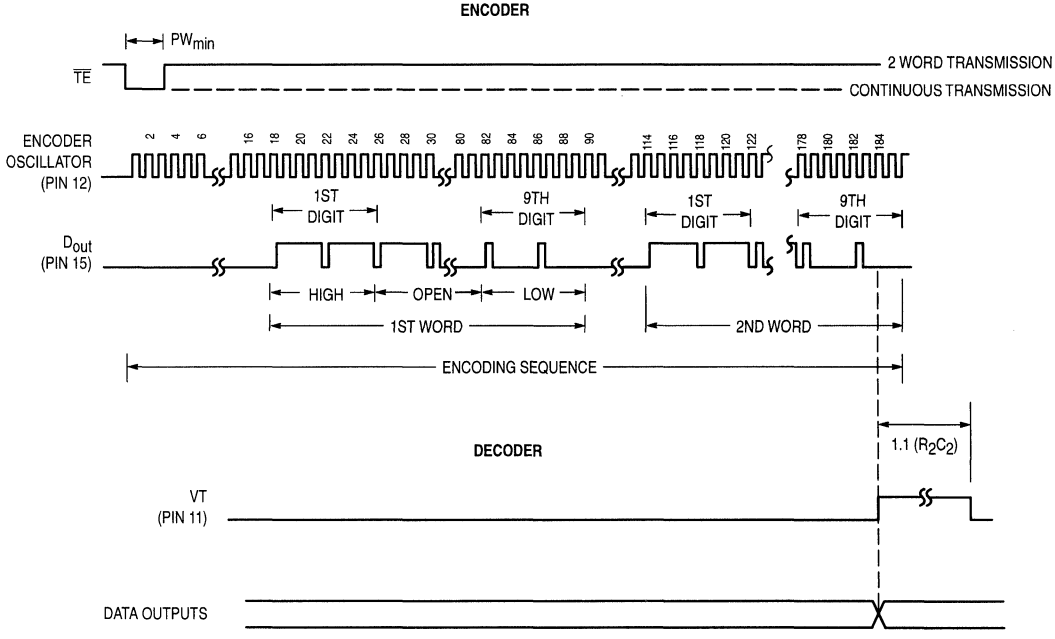


Figure 10. Timing Diagram

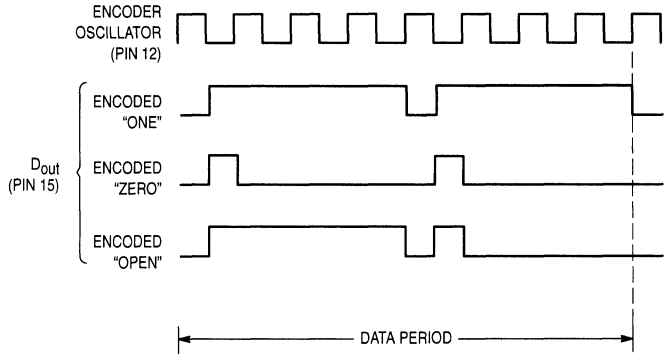


Figure 11. Encoder Data Waveforms

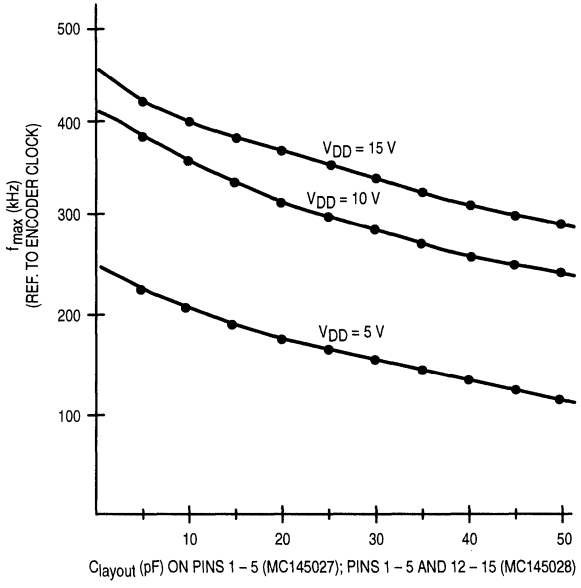


Figure 12. f_{max} vs C_{layout} — Decoders Only

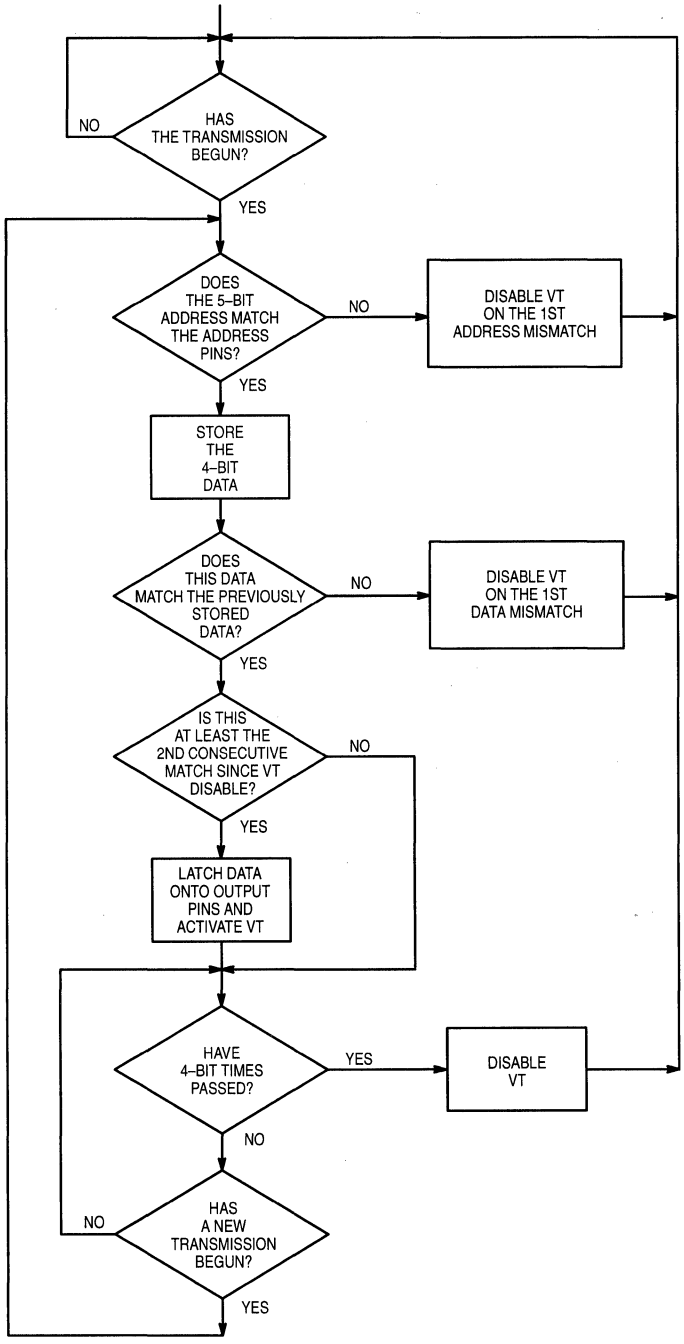


Figure 13. MC145027 Flowchart

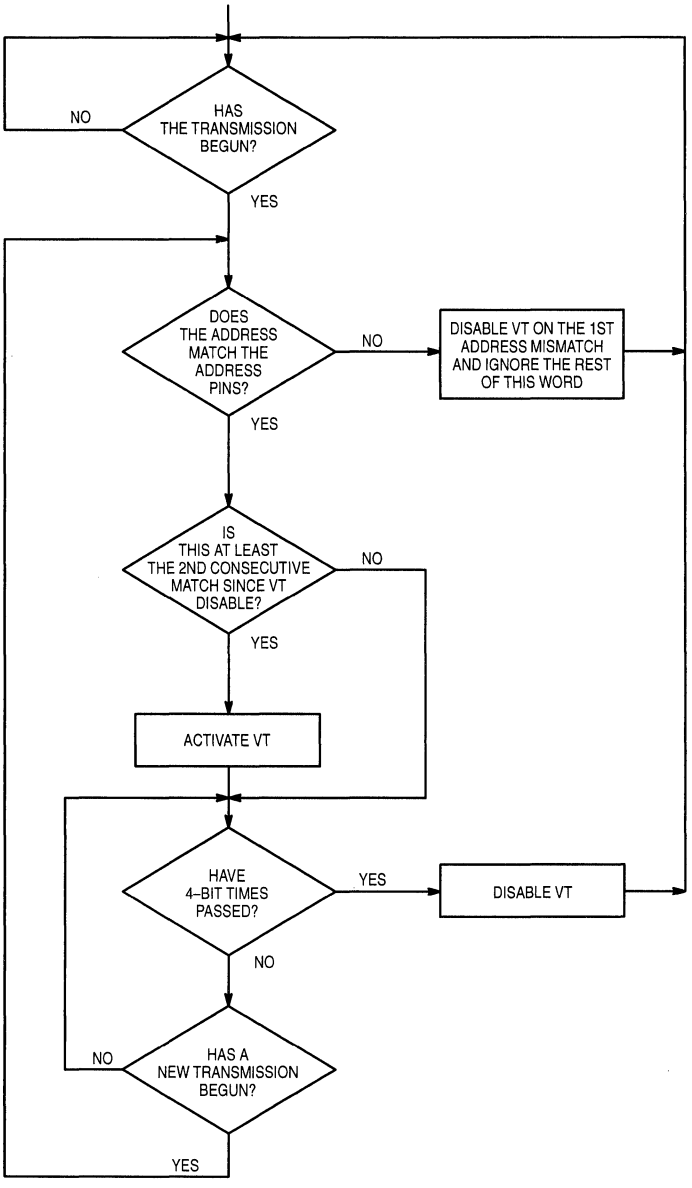


Figure 14. MC145028 Flowchart

MC145027 AND MC145028 TIMING

To verify the MC145027 or MC145028 timing, check the waveforms on C1 (Pin 7) and R2/C2 (Pin 10) as compared to the incoming data waveform on D_{in} (Pin 9).

The R–C decay seen on C1 discharges down to 1/3 V_{DD} before being reset to V_{DD}. This point of reset (labelled "DOS" in Figure 15) is the point in time where the decision is made whether the data seen on D_{in} is a 1 or 0. DOS should not be too close to the D_{in} data edges or intermittent operation may occur.

The other timing to be checked on the MC145027 and MC145028 is on R2/C2 (see Figure 16). The R–C decay is continually reset to V_{DD} as data is being transmitted. Only between words and after the end–of–transmission (EOT) does R2/C2 decay significantly from V_{DD}. R2/C2 can be used to identify the internal end–of–word (EOW) timing edge which is generated when R2/C2 decays to 2/3 V_{DD}. The internal EOT timing edge occurs when R2/C2 decays to 1/3 V_{DD}. When the waveform is being observed, the R–C decay should go down between the 2/3 and 1/3 V_{DD} levels, but not too close to either level before data transmission on D_{in} resumes.

Verification of the timing described above should ensure a good match between the MC145026 transmitter and the MC145027 and MC145028 receivers.

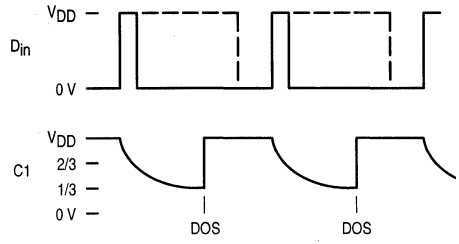


Figure 15. R–C Decay on Pin 7 (C1)

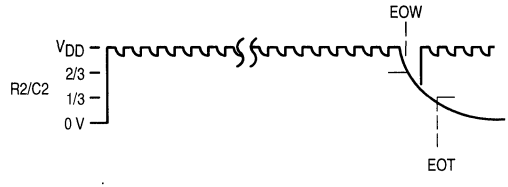
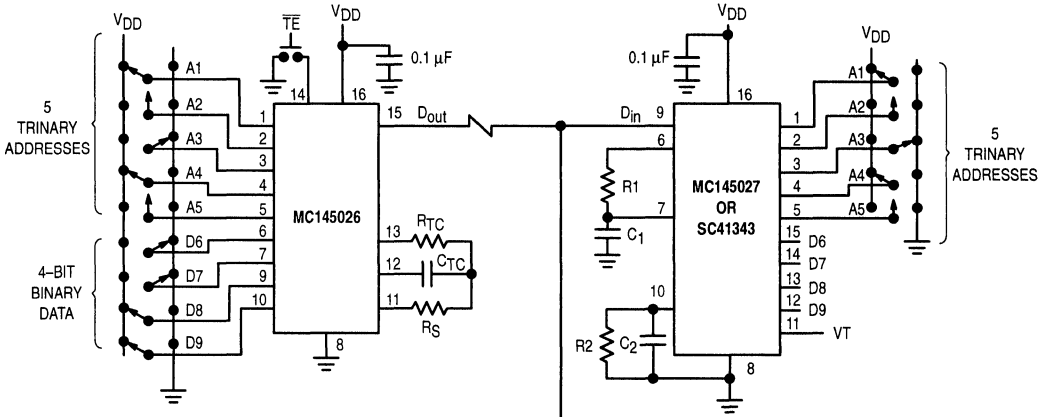


Figure 16. R–C Decay on Pin 10 (R2/C2)



$$f_{osc} = \frac{1}{2.3\ R_{TC}C_{TC'}}$$

$R_1C_1 = 3.95\ R_{TC}C_{TC}$

$R_2C_2 = 77\ R_{TC}C_{TC}$

$C_{TC'} = C_{TC} + C_{layout} + 12\ pF$

$100\ pF \le C_{TC} \le 15\ \mu F$

$R_{TC} \ge 10\ k\Omega$; $R_S \approx 2\ R_{TC}$

$R_1 \ge 10\ k\Omega$

$C_1 \ge 400\ pF$

$R_2 \ge 100\ k\Omega$

$C_2 \ge 700\ pF$

Example R/C Values (All Resistors and Capacitors are ± 5%)

($C_{TC'} = C_{TC} + 20\ pF$)

f_{osc} (kHz)	R_{TC}	$C_{TC'}$	R_S	R_1	C_1	R_2	C_2
362	10 k	120 pF	20 k	10 k	470 pF	100 k	910 pF
181	10 k	240 pF	20 k	10 k	910 pF	100 k	1800 pF
88.7	10 k	490 pF	20 k	10 k	2000 pF	100 k	3900 pF
42.6	10 k	1020 pF	20 k	10 k	3900 pF	100 k	7500 pF
21.5	10 k	2020 pF	20 k	10 k	8200 pF	100 k	0.015 µF
8.53	10 k	5100 pF	20 k	10 k	0.02 µF	200 k	0.02 µF
1.71	50 k	5100 pF	100 k	50 k	0.02 µF	200 k	0.1 µF

Figure 17. Typical Application

APPLICATIONS INFORMATION

INFRARED TRANSMITTER

In Figure 18, the MC145026 encoder is set to run at an oscillator frequency of about 4 to 9 kHz. Thus, the time required for a complete two–word encoding sequence is about 20 to 40 ms. The data output from the encoder gates an RC oscillator running at 50 kHz; the oscillator shown starts rapidly enough to be used in this application. When the "send" button is not depressed, both the MC145026 and oscillator are in a low–power standby state. The RC oscillator has to be trimmed for 50 kHz and has some drawbacks for frequency stability. A superior system uses a ceramic resonator oscillator running at 400 kHz. This oscillator feeds a divider as shown in Figure 19. The unused inputs of the MC14011UB must be grounded.

The MLED81 IRED is driven with the 50 kHz square wave at about 200 to 300 mA to generate the carrier. If desired, two IREDs wired in series can be used (see Application Note AN1016 for more information). The bipolar IRED switch, shown in Figure 18, offers two advantages over a FET. First, a logic FET has too much gate capacitance for the MC14011UB to drive without waveform distortion. Second, the bipolar drive permits lower supply voltages, which are an advantage in portable battery–powered applications.

The configuration shown in Figure 18 operates over a supply range of 4.5 to 18 V. A low–voltage system which operates down to 2.5 V could be realized if the oscillator section of a MC74HC4060 is used in place of the MC14011UB. The data output of the MC145026 is inverted and fed to the RESET pin of the MC74HC4060. Alternately, the MC74HCU04 could be used for the oscillator.

Information on the MC14011UB is in book number DL131/D. The MC74HCU04 and MC74HC4060 are found in book number DL129/D.

INFRARED RECEIVER

The receiver in Figure 20 couples an IR–sensitive diode to input preamp A1, followed by band–pass amplifier A2 with a gain of about 10. Limiting stage A3 follows, with an output of about 800 mV p–p. The limited 50 kHz burst is detected by comparator A4 that passes only positive pulses, and peak–detected and filtered by a diode/RC network to extract the data envelope from the burst. Comparator A5 boosts the signal to logic levels compatible with the MC145027/28 data input. The D_{in} pin of these decoders is a standard CMOS high–impedance input which must ***not*** be allowed to float. Therefore, direct coupling from A5 to the decoder input is utilized.

Shielding should be used on at least A1 and A2, with good ground and high–sensitivity circuit layout techniques applied.

For operation with supplies higher than + 5 V, limiter A4's positive output swing needs to be limited to 3 to 5 V. This is accomplished via adding a zener diode in the negative feedback path, thus avoiding excessive system noise. The biasing resistor stack should be adjusted such that V3 is 1.25 to 1.5 V.

This system works up to a range of about 10 meters. The gains of the system may be adjusted to suit the individual design needs. The 100 Ω resistor in the emitter of the first 2N5088 and the 1 kΩ resistor feeding A2 may be altered if different gain is required. In general, more gain does not necessarily result in increased range. This is due to noise floor limitations. The designer should increase transmitter power and/or increase receiver aperature with Fresnal lensing to greatly improve range. See Application Note AN1016 for additional information.

Information on the MC34074 is in data book DL128/D.

TRINARY SWITCH MANUFACTURERS

Midland Ross–Electronic Connector Div.
617/491–5400
Greyhill
312/354–1040
Augat/Alcoswitch
617/685–4371
Aries Electronics
201/996–6841

The above companies may not have the switches in a DIP. For more information, call them or consult *eem Electronic Engineers Master Catalog* or the *Gold Book*. ***Ask for SPDT with center OFF.***

Alternative: An SPST can be placed in series between a SPDT and the Encoder or Decoder to achieve trinary action.

Motorola cannot recommend one supplier over another and in no way suggests that this is a complete listing of trinary switch manufacturers.

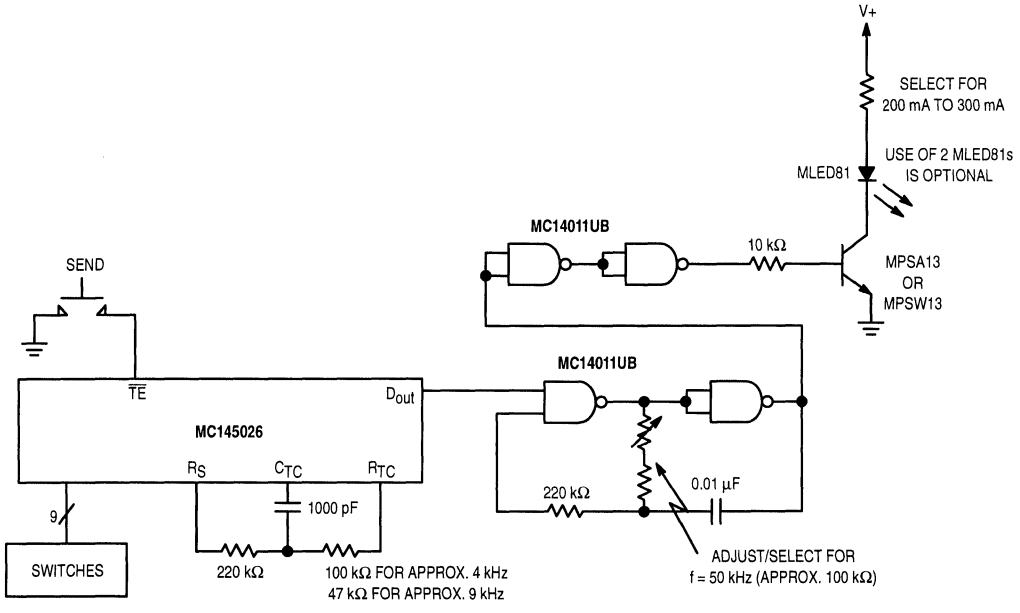


Figure 18. IRED Transmitter Using RC Oscillator to Generate Carrier Frequency

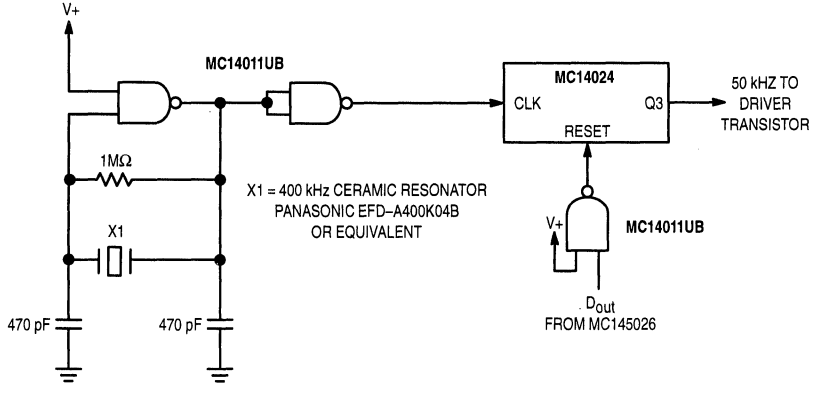


Figure 19. Using a Ceramic Resonator to Generate Carrier Frequency

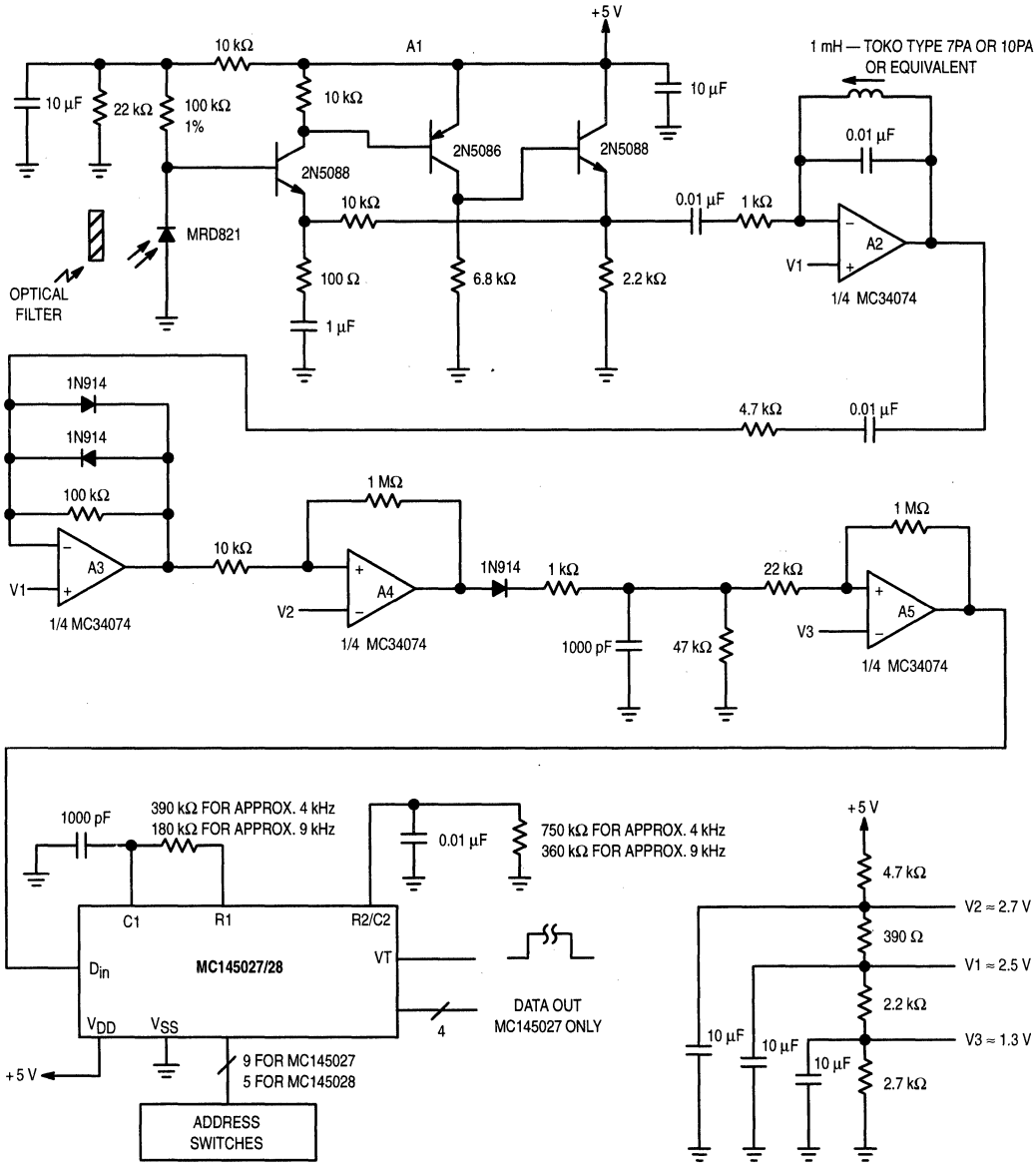
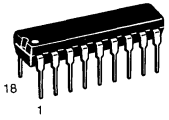


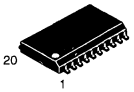
Figure 20. Infrared Receiver

MC145106

PLL Frequency Synthesizer
CMOS



P SUFFIX
PLASTIC DIP
CASE 707



DW SUFFIX
SOG PACKAGE
CASE 751D

ORDERING INFORMATION

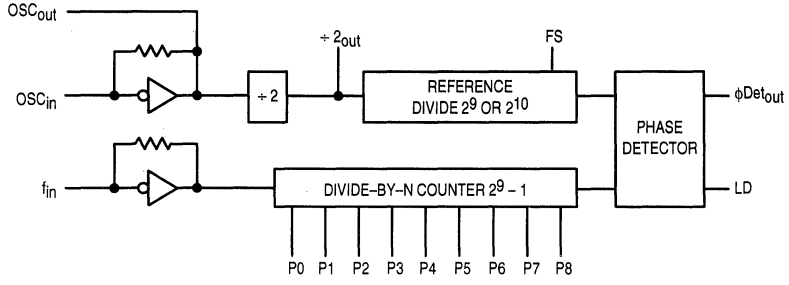
MC145106P	Plastic DIP
MC145106DW	SOG Package

The MC145106 is a phase–locked loop (PLL) frequency synthesizer constructed in CMOS on a single monolithic structure. This synthesizer finds applications in such areas as CB and FM transceivers. The device contains an oscillator/amplifier, a 2^{10} or 2^{11} divider chain for the oscillator signal, a programmable divider chain for the input signal, and a phase detector. The MC145106 has circuitry for a 10.24 MHz oscillator or may operate with an external signal. The circuit provides a 5.12 MHz output signal, which can be used for frequency tripling. A 2^9 programmable divider divides the input signal frequency for channel selection. The inputs to the programmable divider are standard ground–to–supply binary signals. Pull–down resistors on these inputs normally set these inputs to ground enabling these programmable inputs to be controlled from a mechanical switch or electronic circuitry.

The phase detector may control a VCO and yields a high level signal when input frequency is low, and a low level signal when input frequency is high. An out–of–lock signal is provided from the on–chip lock detector with a "0" level for the out–of–lock condition.

- Single Power Supply
- Wide Supply Range: 4.5 to 12 V
- Provision for 10.24 MHz Crystal Oscillator
- 5.12 MHz Output
- Programmable Division Binary Input Selects up to 2^9
- On–Chip Pull–Down Resistors on Programmable Divider Inputs
- Selectable Reference Divider, 2^{10} or 2^{11} (Including ÷ 2)
- Three–State Phase Detector
- See Application Note AN535 and Article Reprint AR254
- Chip Complexity: 880 FETs or 220 Equivalent Gates

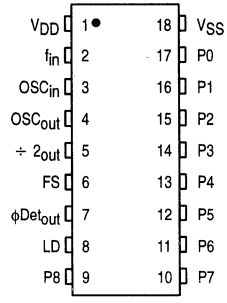
BLOCK DIAGRAM



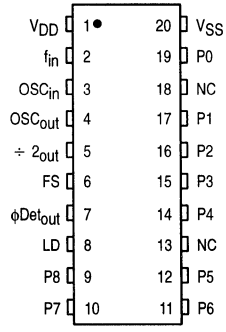
REV 2
8/95

PIN ASSIGNMENTS

PLASTIC DIP



SOG PACKAGE



NC = NO CONNECTION

MAXIMUM RATINGS (Voltages Referenced to V_{SS})

Parameter	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	− 0.5 to + 12	V
Input Voltage, All Inputs	V_{in}	− 0.5 to V_{DD} + 0.5	V
DC Input Current, per Pin	I	± 10	mA
Operating Temperature Range	T_A	− 40 to + 85	°C
Storage Temperature Range	T_{stg}	− 65 to + 150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

ELECTRICAL CHARACTERISTICS (T_A = 25°C Unless Otherwise Stated, Voltages Referenced to V_{SS})

Characteristic		Symbol	V_{DD} Vdc	All Types			Unit
				Min	Typ*	Max	
Power Supply Voltage Range		V_{DD}	—	4.5	—	12	V
Supply Current		I_{DD}	5.0	—	6	10	mA
			10	—	20	35	
			12	—	28	50	
Input Voltage	"0" Level	V_{IL}	5.0	—	—	1.5	V
			10	—	—	3.0	
			12	—	—	3.6	
	"1" Level	V_{IH}	5.0	3.5	—	—	
			10	7.0	—	—	
			12	8.4	—	—	
Input Current	"0" Level	I_{in}	5.0	– 5.0	– 20	– 50	µA
FS, Pull–Up Resistor Source Current)			10	– 15	– 60	– 150	
			12	– 20	– 80	– 200	
(P0 – P8)			5.0	—	—	– 0.3	
			10	—	—	– 0.3	
			12	—	—	– 0.3	
(FS)	"1" Level		5.0	—	—	0.3	
			10	—	—	0.3	
			12	—	—	0.3	
(P0 – P8, Pull–Down Resistor Sink Current)			5.0	7.5	30	75	
			10	22.5	90	225	
			12	30	120	300	
(OSC_{in}, f_{in})	"0" Level		5.0	– 2.0	– 6.0	– 15	
			10	– 6.0	– 25	– 62	
			12	– 9.0	– 37	– 92	
(OSC_{in}, f_{in})	"1" Level		5.0	2.0	6.0	15	
			10	6.0	25	62	
			12	9.0	37	92	
Output Drive Current		I_{OH}					mA
(V_O = 4.5 V)	Source		5.0	– 0.7	– 1.4	—	
(V_O = 9.5 V)			10	– 1.1	– 2.2	—	
(V_O = 11.5 V)			12	– 1.5	– 3.0	—	
(V_O = 0.5 V)	Sink	I_{OL}	5.0	0.9	1.8	—	
(V_O = 0.5 V)			10	1.4	2.8	—	
(V_O = 0.5 V)			12	2.0	4.0	—	
Input Amplitude		—					V p–p
(f_{in} @ 4.0 MHz)			—	1.0	0.2	—	Sine
(OSC_{in} @ 10.24 MHz)			—	1.5	0.3	—	
Input Resistance		R_{in}					MΩ
(OSC_{in}, f_{in})			5.0	—	1.0	—	
			10	—	0.5	—	
			12	—	—	—	
Input Capacitance		C_{in}	—	—	6.0	—	pF
(OSC_{in}, f_{in})							
Three–State Leakage Current		I_{OZ}	5.0	—	—	1.0	µA
(ϕDet_{out})			10	—	—	1.0	
			12	—	—	1.0	
Input Frequency		f_{in}	4.5	0	—	4.0	MHz
(– 40 to + 85°C)			12	0	—	4.0	
Oscillator Frequency		OSC_{in}	4.5	0.1	—	10.24	MHz
(– 40 to + 85°C)			12	0.1	—	10.24	

*Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

TYPICAL CHARACTERISTICS*

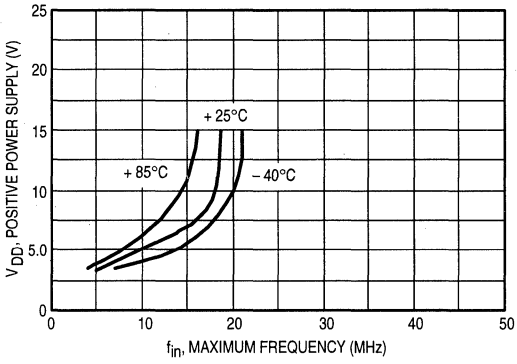


Figure 1. Maximum Divider Input Frequency versus Supply Voltage

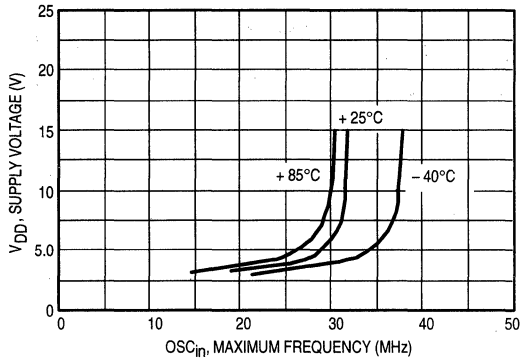


Figure 2. Maximum Oscillator Input Frequency versus Supply Voltage

* Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

TRUTH TABLE

Selection									
P8	P7	P6	P5	P4	P3	P2	P1	P0	Divide by N
0	0	0	0	0	0	0	0	0	2*
0	0	0	0	0	0	0	0	1	3*
0	0	0	0	0	0	0	1	0	2
0	0	0	0	0	0	0	1	1	3
0	0	0	0	0	0	1	0	0	4
•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•
0	1	1	1	1	1	1	1	1	255
•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•
1	1	1	1	1	1	1	1	1	511

1: Voltage level = V_{DD}.
0: Voltage level = 0 or open circuit input.
* The binary setting of 00000000 and 00000001 on P8 to P0 results in a 2 and 3 division which is not in the $2^N - 1$ sequence. When pin is not connected the logic signal on that pin can be treated as a "0".

PIN DESCRIPTIONS

P0 – P8
Programmable Inputs (PDIP — Pins 17 – 9; SOG — Pins 19, 17 – 14, 12 – 9)

Programmable divider inputs (binary).

f_{in}
Frequency Input (PDIP, SOG — Pin 2)

Frequency input to programmable divider (derived from VCO).

OSC_{in}, OSC_{out}
Oscillator Input and Oscillator Output (PDIP, SOG — Pins 3, 4)

Oscillator/amplifier input and output terminals.

LD
Lock Detector (PDIP, SOG — Pin 8)

LD is high when loop is locked, pulses low when out–of–lock.

ϕDet_{out} (PDIP, SOG — Pin 7)

Signal for control of external VCO, output high when f_{in}/N is less than the reference frequency; output low when f_{in}/N is greater than the reference frequency. Reference frequency is the divided down oscillator — input frequency typically 5.0 or 10 kHz.

NOTE

Phase Detector Gain = $V_{DD}/4\pi$.

FS
Reference Oscillator Frequency Division Select (PDIP, SOG — Pin 6)

When using 10.24 MHz OSC frequency, this control selects 10 kHz, a "0" selects 5.0 kHz.

$\div 2_{out}$ (PDIP, SOG — Pin 5)

Reference OSC frequency divided by 2 output; when using 10.24 MHz OSC frequency, this output is 5.12 MHz for frequency tripling applications.

V_{DD}
Positive Power Supply (PDIP, SOG — Pin 1)

V_{SS}
Ground (PDIP — Pin 18, SOG — Pin 20)

PLL SYNTHESIZER APPLICATIONS

The MC145106 is well suited for applications in CB radios because of the channelized frequency requirements. A typical 40 channel CB transceiver synthesizer, using a single crystal reference, is shown in Figure 3 for receiver IF values of 10.695 MHz and 455 kHz.

In addition to applications in CB radios, the MC145106 can be used as a synthesizer for several other systems. Various frequency spectrums can be achieved through the use of proper offset, prescaling, and loop programming techniques. In general, 300 – 400 channels can be synthesized using a single loop, with many additional channels available when multiple loop approaches are employed. Figures 4 and 5 are examples of some possibilities.

In the aircraft synthesizer of Figure 5, the VHF loop (top) will provide a 50 kHz, 360 channel system with 10.7 MHz R/T offset when only the 11.0500 MHz (transmit) and 12.1200 MHz (receive) frequencies are provided to mixer #1. When these signals are provided with crystal oscillators, the result is a three crystal 360 channel, 50 kHz step synthesizer. When using the offset loop (bottom) in Figure 5 to provide the indicated injection frequencies for mixer #1 (two for transmit and two for receive) 360 additional channels are possible. This results in a 720–channel, 25 kHz step synthesizer which requires only two crystals and provides R/T offset capability. The receive offset value is determined by the 11.31 MHz crystal frequency and is 10.7 MHz for the example.

The VHF marine synthesizer in Figure 4 depicts a single loop approach for FM transceivers. The VCO operates on frequency during transmit and is offset downward during receive. The offset corresponds to the receive IF (10.7 MHz) for channels having identical receive/transmit frequencies (simplex), and is (10.7 – 4.6 = 6.1) MHz for duplex channels. Carrier modulation is introduced in the loop during transmit.

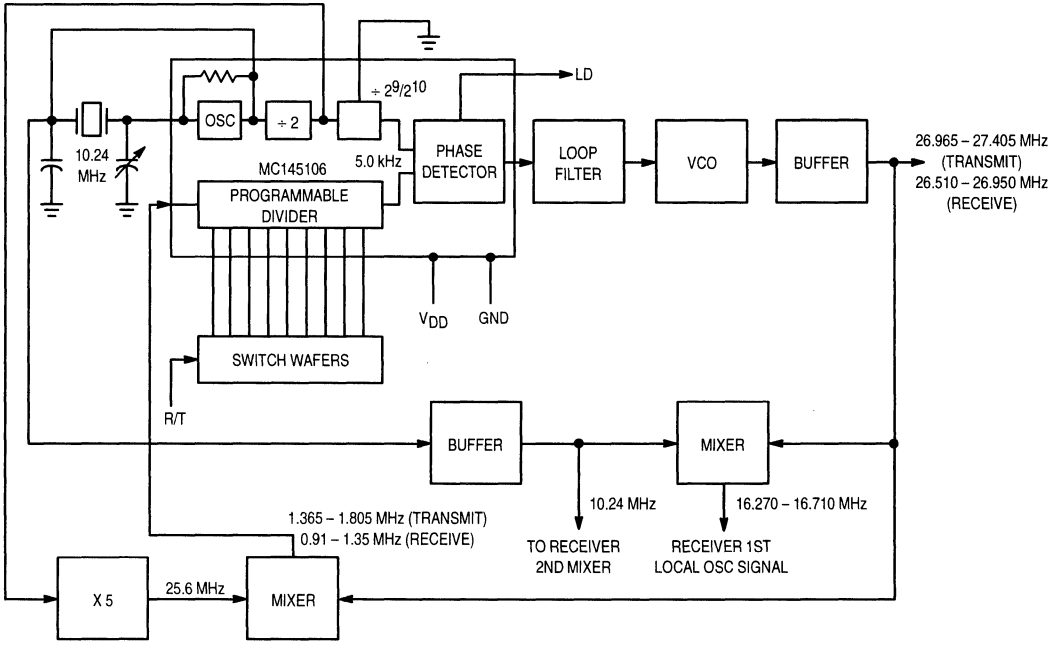
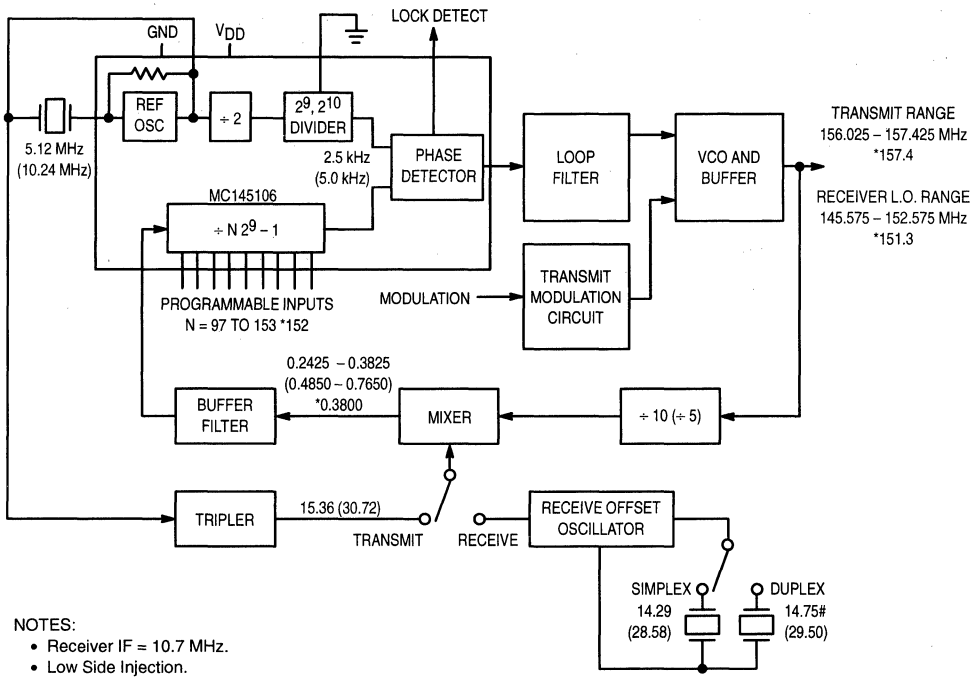


Figure 3. Single Crystal CB Synthesizer Featuring On–Frequency VCO During Transmit



NOTES:
- Receiver IF = 10.7 MHz.
- Low Side Injection.
- Duplex Offset = 4.6 MHz.
- Step Size = 25 kHz.
- Frequencies in MHz unless noted.
- Values in parentheses are for a 5.0 kHz reference frequency.
- Example frequencies for Channel 28 shown by *.

#Can be eliminated by adding 184 to ÷ N for Duplex Channels.

Figure 4. VHF Marine Transceiver Synthesizer

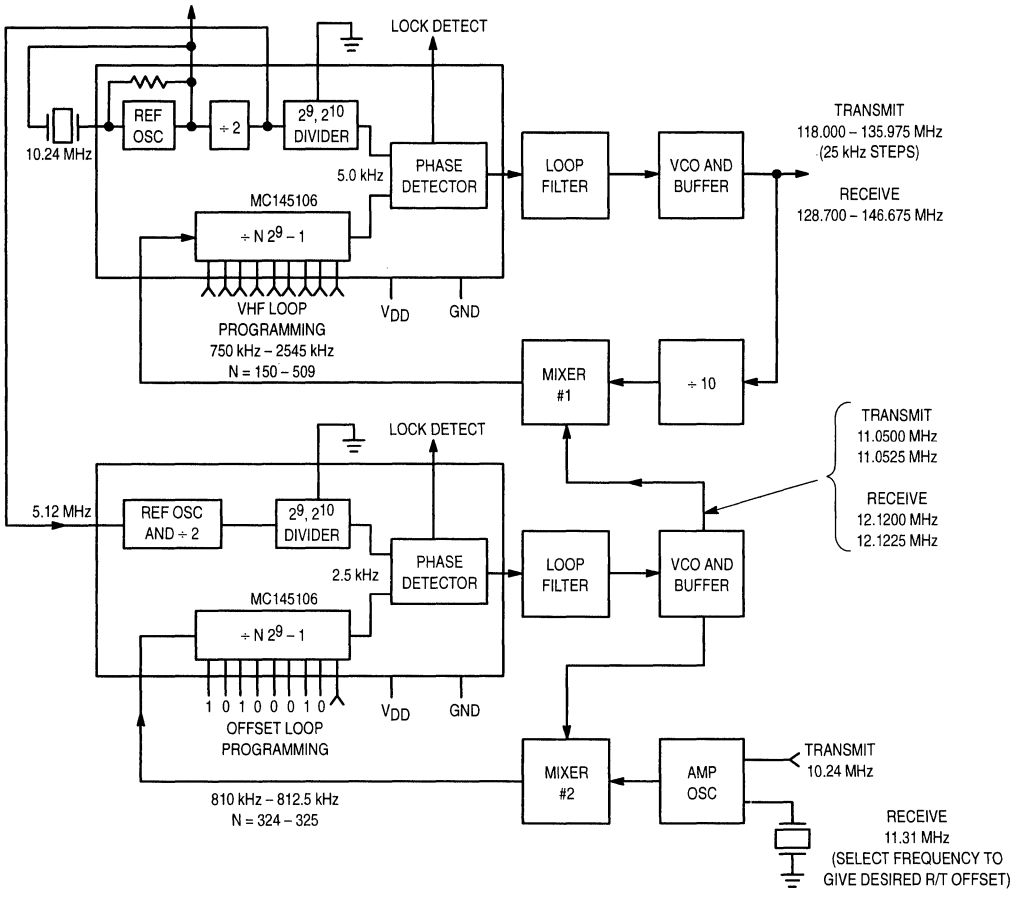


Figure 5. VHF Aircraft 720 Channel Two Crystal Frequency Synthesizer

MC145145-2

4-Bit Data Bus Input PLL Frequency Synthesizer

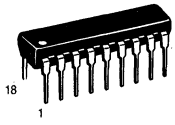
Interfaces with Single–Modulus Prescalers

2

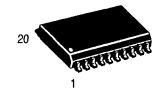
The MC145145–2 is programmed by a 4–bit input, with strobe and address lines. The device features consist of a reference oscillator, 12–bit programmable reference divider, digital phase detector, 14–bit programmable divide–by–N counter, and the necessary latch circuitry for accepting the 4–bit input data. When combined with a loop filter and VCO, the MC145145–2 can provide all of the remaining functions for a PLL frequency synthesizer operating up to the device frequency limit. For higher VCO frequency operation, a down mixer or a fixed divide prescaler can be used between the VCO and the MC145145–2.

The MC145145–2 is an improved performance drop–in replacement for the MC145145–1. Power consumption has decreased and ESD and latch–up performance have improved.

- Operating Temperature Range: – 40 to 85°C
- Low Power Consumption Through the Use of CMOS Technology
- 3.0 to 9.0 V Supply Range
- Single Modulus 4–Bit Data Bus Programming
- On– or Off–Chip Reference Oscillator Operation
- ÷N Range = 3 to 16,383, ÷R Range = 3 to 4,095
- "Linearized" Digital Phase Detector Enhances Transfer Function Linearity
- Two Error Signal Options:
  - Single–Ended (Three–State)
  - Double–Ended
- Chip Complexity: 5,692 FETs or 1,423 Equivalent Gates



P SUFFIX
PLASTIC DIP
CASE 707



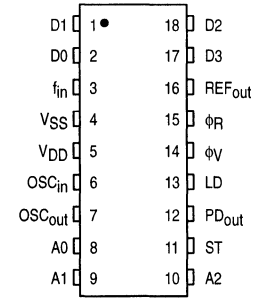
DW SUFFIX
SOG PACKAGE
CASE 751D

ORDERING INFORMATION

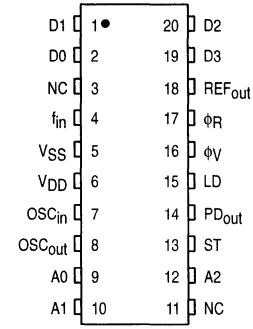
MC145145P2	Plastic DIP
MC145145DW2	SOG Package

PIN ASSIGNMENTS

PLASTIC DIP

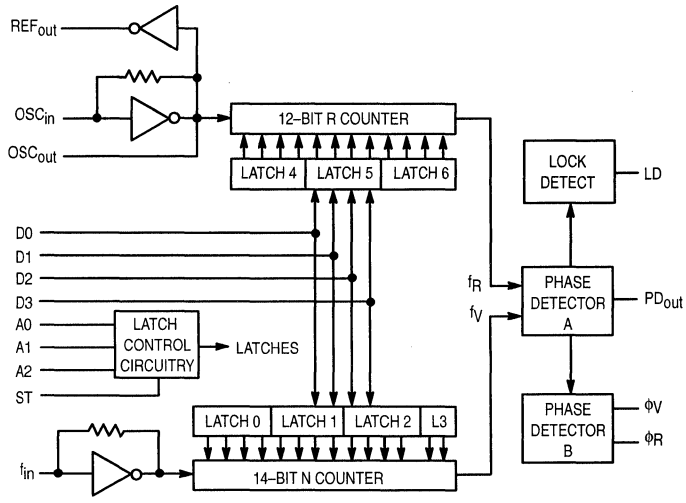


SOG PACKAGE



NC = NO CONNECTION

BLOCK DIAGRAM



REV 1
8/95

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +10	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	−0.5 to V_{DD} +0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
I_{DD}, I_{SS}	Supply Current, V_{DD} or V_{SS} Pins	±30	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds	260	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Descriptions section.

†Power Dissipation Temperature Derating:
Plastic DIP: −12 mW/°C from 65 to 85°C
SOG Package: −7.0 mW/°C from 65 to 85°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to these high–impedance circuits. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}), except for inputs with pull–up devices. Unused outputs must be left open.

2

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Symbol	Parameter	Test Conditions	V_{DD} V	−40°C Min	−40°C Max	25°C Min	25°C Max	85°C Min	85°C Max	Unit
V_{DD}	Power Supply Voltage Range		—	3.0	9.0	3.0	9.0	3.0	9.0	V
I_{SS}	Dynamic Supply Current	$f_{in} = OSC_{in}$ = 10 MHz, 1 V p–p ac coupled sine wave R = 128, A = 32, N = 128	3.0 5.0 9.0	— — —	3.5 10 30	— — —	3.0 7.5 24	— — —	3.0 7.5 24	mA
I_{SS}	Quiescent Supply Current	$V_{in} = V_{DD}$ or V_{SS} I_{out} = 0 µA	3.0 5.0 9.0	— — —	800 1200 1600	— — —	800 1200 1600	— — —	1600 2400 3200	µA
V_{in}	Input Voltage — f_{in}, OSC_{in}	Input ac coupled sine wave	—	500	—	500	—	500	—	mV p–p
V_{IL}	Low–Level Input Voltage — f_{in}, OSC_{in}	$V_{out} \ge 2.1$ V Input $V_{out} \ge 3.5$ V dc coupled $V_{out} \ge 6.3$ V square wave	3.0 5.0 9.0	— — —	0 0 0	— — —	0 0 0	— — —	0 0 0	V
V_{IH}	High–Level Input Voltage — f_{in}, OSC_{in}	$V_{out} \le 0.9$ V Input $V_{out} \le 1.5$ V dc coupled $V_{out} \le 2.7$ V square wave	3.0 5.0 9.0	3.0 5.0 9.0	— — —	3.0 5.0 9.0	— — —	3.0 5.0 9.0	— — —	V
V_{IL}	Low–Level Input Voltage — except f_{in}, OSC_{in}		3.0 5.0 9.0	— — —	0.9 1.5 2.7	— — —	0.9 1.5 2.7	— — —	0.9 1.5 2.7	V
V_{IH}	High–Level Input Voltage — except f_{in}, OSC_{in}		3.0 5.0 9.0	2.1 3.5 6.3	— — —	2.1 3.5 6.3	— — —	2.1 3.5 6.3	— — —	V
I_{in}	Input Current (f_{in}, OSC_{in})	$V_{in} = V_{DD}$ or V_{SS}	9.0	±2.0	±50	±2.0	±25	±2.0	±22	µA
I_{IL}	Input Leakage Current (all inputs except f_{in}, OSC_{in})	$V_{in} = V_{SS}$	9.0	—	−0.3	—	−0.1	—	−1.0	µA
I_{IH}	Input Leakage Current (all inputs except f_{in}, OSC_{in})	$V_{in} = V_{DD}$	9.0	—	0.3	—	0.1	—	1.0	µA
C_{in}	Input Capacitance		—	—	10	—	10	—	10	pF
V_{OL}	Low–Level Output Voltage — OSC_{out}	$I_{out} \approx 0$ µA $V_{in} = V_{DD}$	3.0 5.0 9.0	— — —	0.9 1.5 2.7	— — —	0.9 1.5 2.7	— — —	0.9 1.5 2.7	V
V_{OH}	High–Level Output Voltage — OSC_{out}	$I_{out} \approx 0$ µA $V_{in} = V_{SS}$	3.0 5.0 9.0	2.1 3.5 6.3	— — —	2.1 3.5 6.3	— — —	2.1 3.5 6.3	— — —	V

(continued)

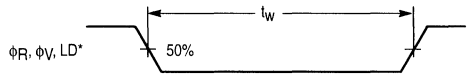
ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	V_{DD} V	−40°C Min	−40°C Max	25°C Min	25°C Max	85°C Min	85°C Max	Unit
V_{OL}	Low–Level Output Voltage— Other Outputs	$I_{out} \approx 0$ µA	3.0 5.0 9.0	— — —	0.05 0.05 0.05	— — —	0.05 0.05 0.05	— — —	0.05 0.05 0.05	V
V_{OH}	High–Level Output Voltage— Other Outputs	$I_{out} \approx 0$ µA	3.0 5.0 9.0	2.95 4.95 8.95	— — —	2.95 4.95 8.95	— — —	2.95 4.95 8.95	— — —	V
I_{OL}	Low–Level Sinking Current— Lock Detect	$V_{out} = 0.3$ V $V_{out} = 0.4$ V $V_{out} = 0.5$ V	3.0 5.0 9.0	0.25 0.64 1.3	— — —	0.2 0.51 1.0	— — —	0.15 0.36 0.7	— — —	mA
I_{OH}	High–Level Sourcing Current—Lock Detect	$V_{out} = 2.7$ V $V_{out} = 4.6$ V $V_{out} = 8.5$ V	3.0 5.0 9.0	−0.25 −0.64 −1.3	— — —	−0.2 −0.51 −1.0	— — —	−0.15 −0.36 −0.7	— — —	mA
I_{OL}	Low–Level Sinking Current— Other Outputs	$V_{out} = 0.3$ V $V_{out} = 0.4$ V $V_{out} = 0.5$ V	3.0 5.0 9.0	0.44 0.64 1.3	— — —	0.35 0.51 1.0	— — —	0.22 0.36 0.7	— — —	mA
I_{OH}	High–Level Sourcing Current—Other Outputs	$V_{out} = 2.7$ V $V_{out} = 4.6$ V $V_{out} = 8.5$ V	3.0 5.0 9.0	−0.44 −0.64 −1.3	— — —	−0.35 −0.51 −1.0	— — —	−0.22 −0.36 −0.7	— — —	mA
I_{OZ}	Output Leakage Current— PD_{out}	$V_{out} = V_{DD}$ or V_{SS} Output in Off State	9.0	—	± 0.3	—	± 0.1	—	± 1.0	µA
C_{out}	Output Capacitance—PD_{out}	PD_{out} — Three–State	—	—	10	—	10	—	10	pF

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 10 ns)

Symbol	Parameter	Figure No.	V_{DD} V	Guaranteed Limit 25°C	Guaranteed Limit −40 to 85°C	Unit
t_w	Output Pulse Width, ϕ_R, ϕ_V, and LD with f_R in Phase with f_V	1, 5	3.0 5.0 9.0	25 to 200 20 to 100 10 to 70	25 to 260 20 to 125 10 to 80	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, LD	2, 5	3.0 5.0 9.0	180 90 70	200 120 90	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Other Outputs	2, 5	3.0 5.0 9.0	160 80 60	175 100 65	ns
t_{su}	Minimum Setup Time, Data to ST	3	3.0 5.0 9.0	10 10 10	— — —	ns
t_{su}	Minimum Setup Time, Address to ST	3	3.0 5.0 9.0	25 20 15	— — —	ns
t_h	Minimum Hold Time, Address to ST	3	3.0 5.0 9.0	10 10 10	— — —	ns
t_h	Minimum Hold Time, Data to ST	3	3.0 5.0 9.0	25 20 15	— — —	ns
t_w	Minimum Input Pulse Width, ST	4	3.0 5.0 9.0	40 30 20	— — —	ns

SWITCHING WAVEFORMS



* f_R in phase with f_V

Figure 1.

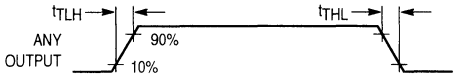


Figure 2.

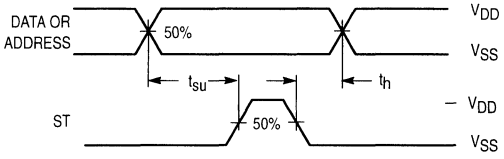


Figure 3.

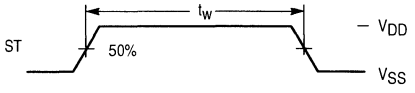
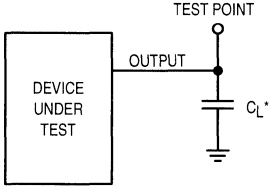


Figure 4.

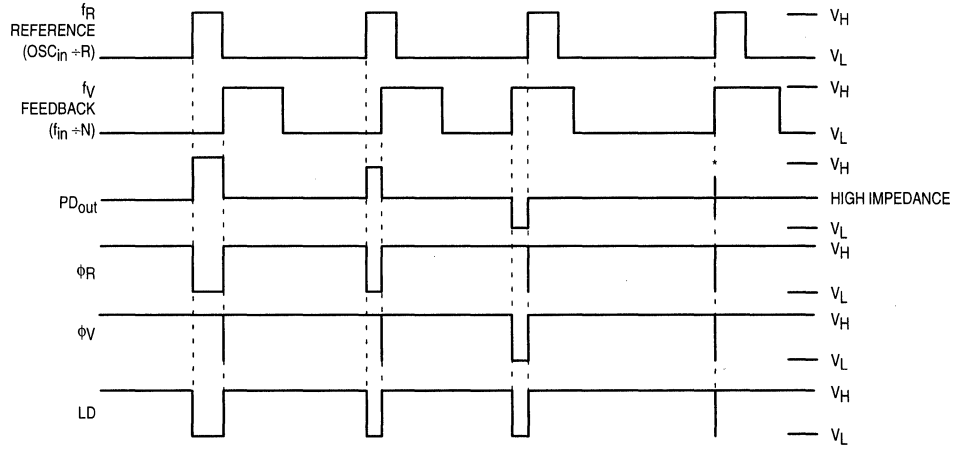


* Includes all probe and fixture capacitance.

Figure 5. Test Circuit

FREQUENCY CHARACTERISTICS (Voltages Referenced to V_{SS}, C_L = 50 pF, Input $t_r = t_f$ = 10 ns unless otherwise indicated)

Symbol	Parameter	Test Conditions	V_{DD} V	−40°C		25°C		85°C		Unit
				Min	Max	Min	Max	Min	Max	
f_i	Input Frequency (f_{in}, OSC_{in})	R ≥ 8, A ≥ 0, N ≥ 8 V_{in} = 500 mV p–p ac coupled sine wave	3.0 5.0 9.0	— — —	6.0 15 15	— — —	6.0 15 15	— — —	6.0 15 15	MHz
		R ≥ 8, A ≥ 0, N ≥ 8 V_{in} = 1.0 V p–p ac coupled sine wave	3.0 5.0 9.0	— — —	12 22 25	— — —	12 20 22	— — —	7.0 20 22	MHz
		R ≥ 8, A ≥ 0, N ≥ 8 V_{in} = V_{DD} to V_{SS} dc coupled square wave	3.0 5.0 9.0	— — —	13 25 25	— — —	12 22 25	— — —	8.0 22 25	MHz



V_H = High voltage level.
V_L = Low voltage level.
* At this point, when both f_R and f_V are in phase, the output is forced to near mid supply.
NOTE: The PD_{out} generates error pulses during out–of–lock conditions. When locked in phase and frequency, the output is high impedance and the voltage at that pin is determined by the low–pass filter capacitor.

Figure 6. Phase/Frequency Detectors and Lock Detector Output Waveforms

PIN DESCRIPTIONS

INPUT PINS

D0 – D3
Data Inputs (PDIP – Pins 2, 1, 18, 17; SOG – Pins 2, 1, 20, 19)

Information at these inputs is transferred to the internal latches when the ST input is in the high state. D3 is most significant bit.

f_{in}
Frequency Input (PDIP – Pin 3, SOG – Pin 4)

Input to ÷N portion of synthesizer. f_{in} is typically derived from the loop VCO and is ac coupled. For larger amplitude signals (standard CMOS–logic levels) dc coupling may be used.

OSC_{in}/OSC_{out}
Reference Oscillator Input/Output (PDIP – Pins 6, 7; SOG – Pins 7, 8)

These pins form an on–chip reference oscillator when connected to terminals of an external parallel resonant crystal. Frequency setting capacitors of appropriate value must be connected from OSC_{in} to ground and OSC_{out} to ground. OSC_{in} may also serve as input for an externally–generated reference signal. This signal is typically ac coupled to OSC_{in}, but for larger amplitude signals (standard CMOS–logic levels) dc coupling may also be used. In the external reference mode, no connection is required to OSC_{out}.

A0 – A2
Address Inputs (PDIP – Pins 8, 9, 10; SOG – Pins 9, 10, 12)

A0, A1, and A2 are used to define which latch receives the information on the data input lines. The addresses refer to the following latches:

A2	A1	A0	Selected	Function	D0	D1	D2	D3
0	0	0	Latch 0	÷ N Bits	0	1	2	3
0	0	1	Latch 1	÷ N Bits	4	5	6	7
0	1	0	Latch 2	÷ N Bits	8	9	10	11
0	1	1	Latch 3	÷ N Bits	12	13	—	—
1	0	0	Latch 4	Reference Bits	0	1	2	3
1	0	1	Latch 5	Reference Bits	4	5	6	7
1	1	0	Latch 6	Reference Bits	8	9	10	11
1	1	1	—	—	—	—	—	—

ST
Strobe Transfer (PDIP – Pin 11, SOG – Pin 13)

The rising edge of strobe transfers data into the addressed latch, the falling edge of strobe latches data into the latch. This pin should normally be held low to avoid loading latches with invalid data.

OUTPUT PINS

PD_{out}
Single–Ended Phase Detector Output (PDIP – Pin 12, SOG – Pin 14)

Three–state output of phase detector for use as loop–error signal.

Frequency $f_V > f_R$ or f_V Leading: Negative Pulses
Frequency $f_V < f_R$ or f_V Lagging: Positive Pulses
Frequency $f_V = f_R$ and Phase Coincidence: High–Impedance State

LD
Lock Detector Signal (PDIP – Pin 13, SOG – Pin 15)

High level when loop is locked (f_R, f_V of same phase and frequency). Pulses low when loop is out of lock.

ϕV, ϕR
Phase Detector Outputs (PDIP – Pins 14, 15; SOG – Pins 16, 17)

These phase detector outputs can be combined externally for a loop–error signal. A single–ended output is also available for this purpose (see PD_{out}).

If frequency f_V is greater than f_R or if the phase of f_V is leading, then error information is provided by ϕV pulsing low. ϕR remains essentially high.

If the frequency f_V is less than f_R or if the phase of f_V is lagging, then error information is provided by ϕR pulsing low. ϕV remains essentially high.

If the frequency of $f_V = f_R$ and both are in phase, then both ϕV and ϕR remain high except for a small minimum time period when both pulse low in phase.

REF_{out}
Buffered Reference Output (PDIP – Pin 16, SOG – Pin 18)

Buffered output of on–chip reference oscillator or externally provided reference–input signal.

POWER SUPPLY PINS

V_{SS}
Ground (PDIP – Pin 4, SOG – Pin 5)

Circuit Ground.

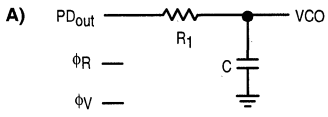
V_{DD}
Positive Power Supply (PDIP – Pin 5, SOG – Pin 6)

The positive supply voltage may range from 3.0 to 9.0 V with respect to V_{SS}.

DESIGN CONSIDERATIONS

PHASE–LOCKED LOOP — LOW–PASS FILTER DESIGN

A)

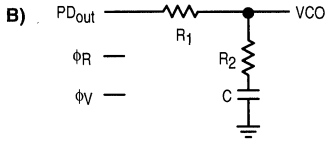


$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NR_1C}}$$

$$\zeta = \frac{N\omega_n}{2K_\phi K_{VCO}}$$

$$F(s) = \frac{1}{R_1sC + 1}$$

B)

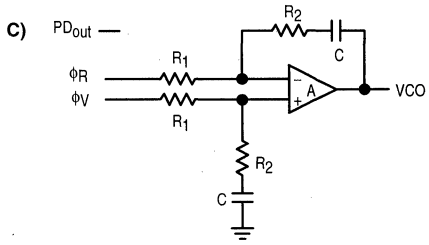


$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NC(R_1 + R_2)}}$$

$$\zeta = 0.5\,\omega_n \left(R_2C + \frac{N}{K_\phi K_{VCO}}\right)$$

$$F(s) = \frac{R_2sC + 1}{(R_1 + R_2)sC + 1}$$

C)



$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NCR_1}}$$

$$\zeta = \frac{\omega_n R_2 C}{2}$$

ASSUMING GAIN A IS VERY LARGE, THEN:

$$F(s) = \frac{R_2sC + 1}{R_1sC}$$

NOTE: Sometimes R_1 is split into two series resistors, each $R_1 \div 2$. A capacitor C_C is then placed from the midpoint to ground to further filter ϕ_V and ϕ_R. The value of C_C should be such that the corner frequency of this network does not significantly affect ω_n.

DEFINITIONS:

N = Total Division Ratio in feedback loop

K_ϕ (Phase Detector Gain) = $V_{DD}/4\pi$ for PD_{out}

K_ϕ (Phase Detector Gain) = $V_{DD}/2\pi$ for ϕ_V and ϕ_R

K_{VCO} (VCO Gain) = $\frac{2\pi\Delta f_{VCO}}{\Delta V_{VCO}}$

for a typical design w_n (Natural Frequency) $\approx \frac{2\pi fr}{10}$ (at phase detector input).

Damping Factor: $\zeta \cong 1$

RECOMMENDED READING:

Gardner, Floyd M., *Phaselock Techniques (second edition).* New York, Wiley–Interscience, 1979.

Manassewitsch, Vadim, *Frequency Synthesizers: Theory and Design (second edition).* New York, Wiley–Interscience, 1980.

Blanchard, Alain, *Phase–Locked Loops: Application to Coherent Receiver Design.* New York, Wiley–Interscience, 1976.

Egan, William F., *Frequency Synthesis by Phase Lock.* New York, Wiley–Interscience, 1981.

Rohde, Ulrich L., *Digital PLL Frequency Synthesizers Theory and Design.* Englewood Cliffs, NJ, Prentice–Hall, 1983.

Berlin, Howard M., *Design of Phase–Locked Loop Circuits, with Experiments.* Indianapolis, Howard W. Sams and Co., 1978.

Kinley, Harold, *The PLL Synthesizer Cookbook.* Blue Ridge Summit, PA, Tab Books, 1980.

AN535, Phase–Locked Loop Design Fundamentals, Motorola Semiconductor Products, Inc., 1970.

AR254, Phase–Locked Loop Design Articles, Motorola Semiconductor Products, Inc., Reprinted with permission from *Electronic Design,* 1987.

CRYSTAL OSCILLATOR CONSIDERATIONS

The following options may be considered to provide a reference frequency to Motorola's CMOS frequency synthesizers.

Use of a Hybrid Crystal Oscillator

Commercially available temperature–compensated crystal oscillators (TCXOs) or crystal–controlled data clock oscillators provide very stable reference frequencies. An oscillator capable of sinking and sourcing 50 μA at CMOS logic levels may be direct or dc coupled to OSC_{in}. In general, the highest frequency capability is obtained utilizing a direct–coupled square wave having a rail–to–rail (V_{DD} to V_{SS}) voltage swing. If the oscillator does not have CMOS logic levels on the outputs, capacitive or ac coupling to OSC_{in} may be used. OSC_{out}, an unbuffered output, should be left floating.

For additional information about TCXOs and data clock oscillators, please consult the latest version of the *eem Electronic Engineers Master Catalog,* the *Gold Book,* or similar publications.

Design an Off–Chip Reference

The user may design an off–chip crystal oscillator using ICs specifically developed for crystal oscillator applications, such as the MC12061 MECL device. The reference signal from the MECL device is ac coupled to OSC_{in}. For large amplitude signals (standard CMOS logic levels), dc coupling is used. OSC_{out}, an unbuffered output, should be left floating. In general, the highest frequency capability is obtained with a direct–coupled square wave having rail–to–rail voltage swing.

Use of the On–Chip Oscillator Circuitry

The on–chip amplifier (a digital inverter) along with an appropriate crystal may be used to provide a reference source frequency. A fundamental mode crystal, parallel resonant at the desired operating frequency, should be connected as shown in Figure 7.

For V_{DD} = 5.0 V, the crystal should be specified for a loading capacitance, C_L, which does not exceed 32 pF for frequencies to approximately 8.0 MHz, 20 pF for frequencies in the area of 8.0 to 15 MHz, and 10 pF for higher frequencies. These are guidelines that provide a reasonable compromise between IC capacitance, drive capability, swamping variations in stray and IC input/output capacitance, and realistic C_L values. The shunt load capacitance, C_L, presented across the crystal can be estimated to be:

$$C_L = \frac{C_{in}C_{out}}{C_{in} + C_{out}} + C_a + C_o + \frac{C1 \cdot C2}{C1 + C2}$$

where

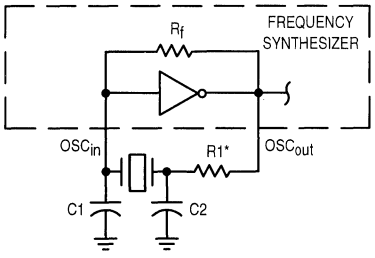
C_{in} = 5.0 pF (see Figure 8)
C_{out} = 6.0 pF (see Figure 8)
C_a = 1.0 pF (see Figure 8)
C_O = the crystal's holder capacitance (see Figure 9)
C1 and C2 = external capacitors (see Figure 7)

The oscillator can be "trimmed" on–frequency by making a portion or all of C1 variable. The crystal and associated components must be located as close as possible to the OSC_{in} and OSC_{out} pins to minimize distortion, stray capacitance, stray inductance, and startup stabilization time. In some cases, stray capacitance should be added to the value for C_{in} and C_{out}.

Power is dissipated in the effective series resistance of the crystal, R_e, in Figure 9. The drive level specified by the crystal manufacturer is the maximum stress that a crystal can withstand without damage or excessive shift in frequency. R1 in Figure 7 limits the drive level. The use of R1 may not be necessary in some cases (i.e., R1 = 0 Ω).

To verify that the maximum dc supply voltage does not overdrive the crystal, monitor the output frequency as a function of voltage at OSC_{out}. (Care should be taken to minimize loading.) The frequency should increase very slightly as the dc supply voltage is increased. An overdriven crystal will decrease in frequency or become unstable with an increase in supply voltage. The operating supply voltage must be reduced or R1 must be increased in value if the overdriven condition exists. The user should note that the oscillator start–up time is proportional to the value of R1.

Through the process of supplying crystals for use with CMOS inverters, many crystal manufacturers have developed expertise in CMOS oscillator design with crystals. Discussions with such manufacturers can prove very helpful. (see Table 1).



* May be deleted in certain cases. See text.

Figure 7. Pierce Crystal Oscillator Circuit

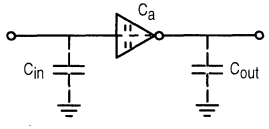
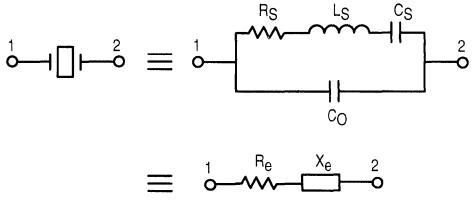


Figure 8. Parasitic Capacitances of the Amplifier



NOTE: Values are supplied by crystal manufacturer (parallel resonant crystal).

Figure 9. Equivalent Crystal Networks

Table 1. Partial List of Crystal Manufacturers

Name	Address	Phone
United States Crystal Corp.	3605 McCart Ave., Ft. Worth, TX 76110	(817) 921–3013
Crystek Crystal	2351 Crystal Dr., Ft. Myers, FL 33907	(813) 936–2109
Statek Corp.	512 N. Main St., Orange, CA 92668	(714) 639–7810

NOTE: Motorola cannot recommend one supplier over another and in no way suggests that this is a complete listing of crystal manufacturers.

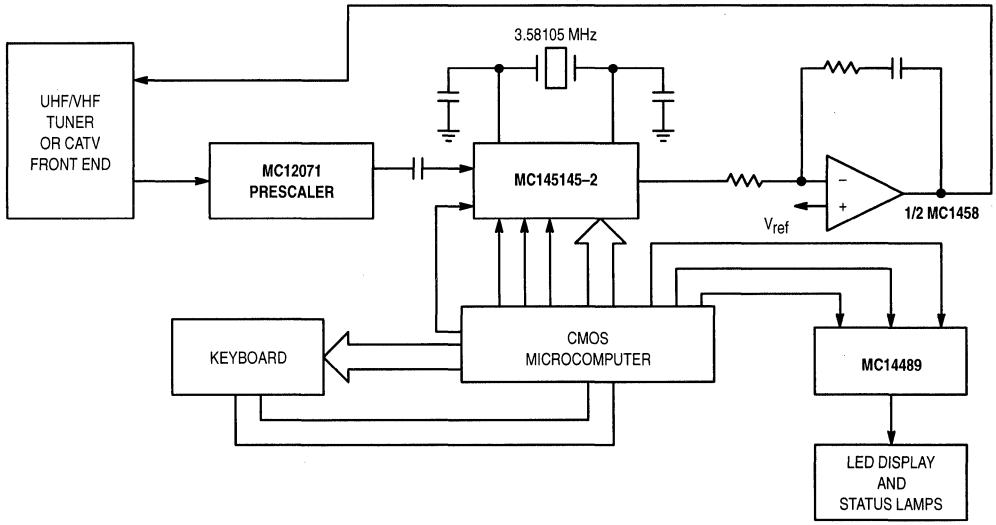


Figure 10. TV/CATV Tuning System

RECOMMENDED READING

Technical Note TN–24, Statek Corp.

Technical Note TN–7, Statek Corp.

E. Hafner, "The Piezoelectric Crystal Unit – Definitions and Method of Measurement", *Proc. IEEE,* Vol. 57, No. 2 Feb., 1969.

D. Kemper, L. Rosine, "Quartz Crystals for Frequency Control", *Electro–Technology,* June, 1969.

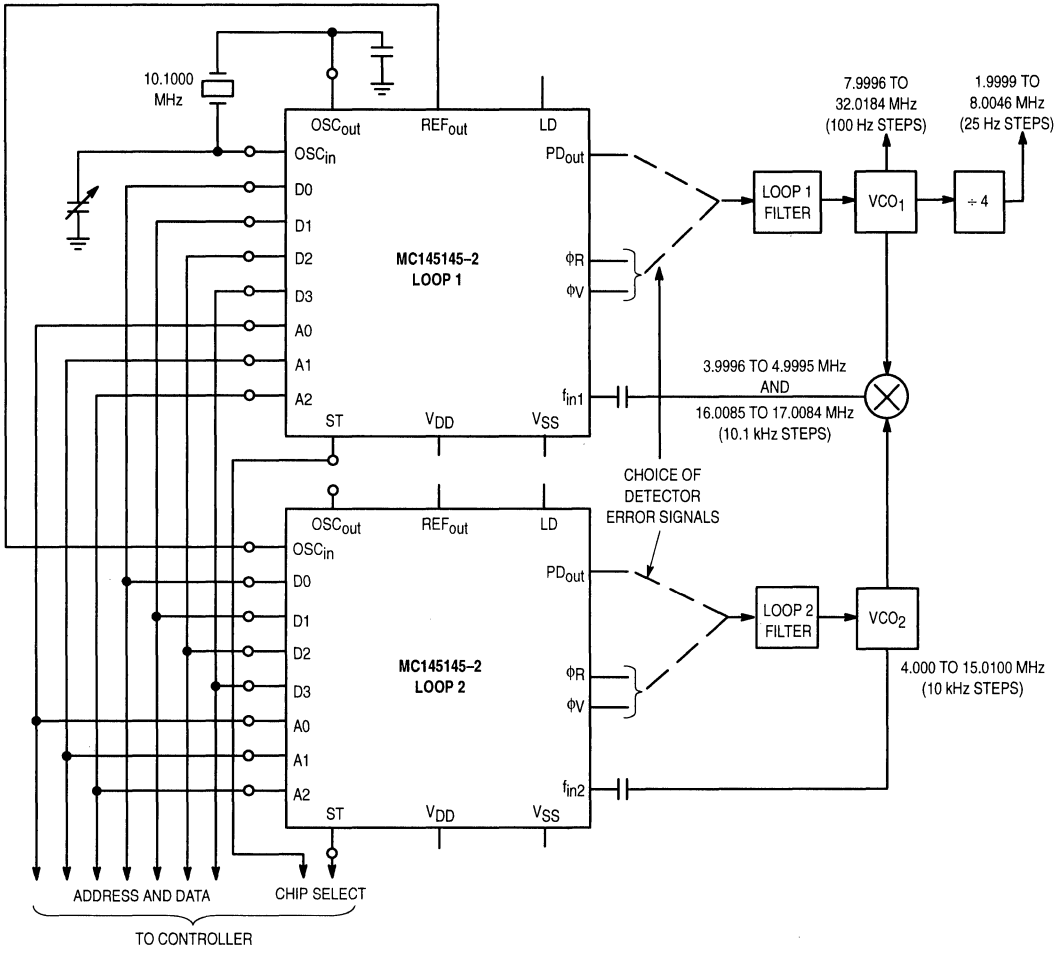
P. J. Ottowitz, "A Guide to Crystal Selection", *Electronic Design*, May, 1966.

APPLICATIONS

The features of the MC145145–2 permit bus operation with a dedicated wire needed only for the strobe input. In a microprocessor–controlled system this strobe input is accessed when the PLL is addressed. The remaining data and address inputs will directly interface to the microprocessor's data and address buses.

The ÷ R programmability is used to advantage in Figure 10. Here, the nominal ÷ R value is 3667, but by programming small changes in this value, fine tuning is accomplished. Better tuning resolution is achievable with this method than by changing the ÷ N, due to the use of the large fixed prescaling value of ÷ 256 provided by the MC12071.

The two–loop synthesizer, in Figure 11, takes advantage of these features to control the phase–locked loop with a minimum of dedicated lines while preserving optimal loop performance. Both 25 Hz and 100 Hz steps are provided while the relatively large reference frequencies of 10 kHz or 10.1 kHz are maintained.



NOTES:
1. Table 2 provides program sequence for the ÷ N1 (Loop 1) and ÷ N2 (Loop 2) Counters.
2. ÷ R1 = 1000, f_{R1} = 10.1 kHz, ÷ R2 = 1010, f_{R2} = 10 kHz.
3. $f_{VCO1} = N1(f_{R1}) + N2(f_{R2}) = N1(f_{R2} + \Delta f) + N2(f_{R2})$ where Δf = 100 Hz.
4. Other f_{R1} and f_{R2} values may be used with appropriate ÷N1 and ÷ N2 changes.

Figure 11. Two–Loop Synthesizer Provides 25 and 100 Hz Frequency Steps While Maintaining High Detector Comparison Frequencies of 10 and 10.1 kHz

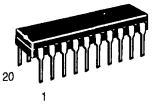
Table 2. Programming Sequence for Two–Loop Synthesizer of Figure 11

÷ N1	f_{in1} (MHz)	÷ N2	f_{VCO2} (MHz)	f_{VCO1} (MHz)
396 "A" 397 495	3.9996 "B" 4.0097 4.9995	400 399 301	4.0000 3.9900 3.0100	7.9996 7.9997 8.0095
"A"	"B"	401 400 303	4.0100 4.0000 3.0200	8.0096 8.0097 8.0195
"A"	"B"	402 "C" 401 303	4.0200 "D" 4.0100 3.0300	8.0196 8.0197 8.0295
"A"	"B"	1500	15.0000	Increasing In 100 Hz Steps 19.9995
"A"	"B"	1600 1599 1501	16.0000 15.9900 15.0100	19.9996 19.9997 20.0095
1585 "E" 1586 1684	16.0085 "F" 16.0186 17.0084			20.0085 20.0086 20.0184
"E"	"F"	"C"	"D"	20.0185 20.0186 20.0284
				Increasing In 100 Hz Steps 32.0084
"E"	"F"			32.0085 32.0086 32.0184

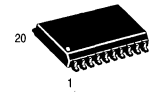
MC145146-2

4-Bit Data Bus Input PLL Frequency Synthesizer

Interfaces with Dual–Modulus Prescalers



P SUFFIX
PLASTIC DIP
CASE 738



DW SUFFIX
SOG PACKAGE
CASE 751D

ORDERING INFORMATION

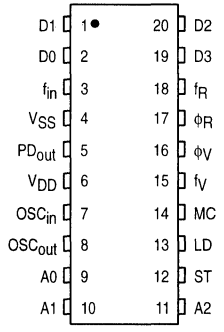
MC145146P2	Plastic DIP
MC145146DW2	SOG Package

The MC145146–2 is programmed by a 4–bit input, with strobe and address lines. The device features consist of a reference oscillator, 12–bit programmable reference divider, digital phase detector, 10–bit programmable divide–by–N counter, 7–bit divide–by–A counter, and the necessary latch circuitry for accepting the 4–bit input data. When combined with a loop filter and VCO, the MC145146–2 can provide all of the remaining functions for a PLL frequency synthesizer operating up to the device frequency limit. For higher VCO frequency operation, a down mixer or a dual–modulus prescaler can be used between the VCO and the MC145146–2.

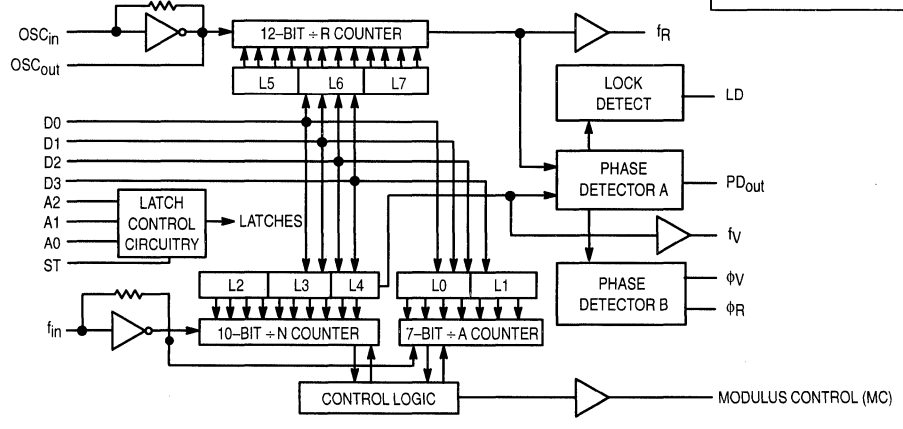
The MC145146–2 is an improved performance drop–in replacement for the MC145146–1. Power consumption has decreased and ESD and latch–up performance have improved.

- Operating Temperature Range: – 40 to 85°C
- Low Power Consumption Through the Use of CMOS Technology
- 3.0 to 9.0 V Supply Range
- Programmable Reference Divider for Values Between 3 and 4095
- On– or Off–Chip Reference Oscillator Operation
- Dual–Modulus 4–Bit Data Bus Programming
- ÷ N Range = 3 to 1023, ÷ A Range = 0 to 127
- "Linearized" Digital Phase Detector Enhances Transfer Function Linearity
- Two Error Signal Options:
  Single–Ended (Three–State)
  Double–Ended
- Chip Complexity: 5,692 FETs or 1,423 Equivalent Gates

PIN ASSIGNMENT



BLOCK DIAGRAM



REV 1
8/95

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	– 0.5 to + 10	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	– 0.5 to V_{DD} + 0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	± 10	mA
I_{DD}, I_{SS}	Supply Current, V_{DD} or V_{SS} Pins	± 30	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds	260	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Descriptions section.

†Power Dissipation Temperature Derating:
Plastic DIP: –12 mW/°C from 65 to 85°C
SOG Package: –7.0 mW/°C from 65 to 85°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to these high–impedance circuits. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}), except for inputs with pull–up devices. Unused outputs must be left open.

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Symbol	Parameter	Test Conditions	V_{DD} V	–40°C Min	–40°C Max	25°C Min	25°C Max	85°C Min	85°C Max	Unit
V_{DD}	Power Supply Voltage Range		—	3.0	9.0	3.0	9.0	3.0	9.0	V
I_{SS}	Dynamic Supply Current	$f_{in} = OSC_{in}$ = 10 MHz, 1 V p–p ac coupled sine wave R = 128, A = 32, N = 128	3.0 5.0 9.0	— — —	3.5 10 30	— — —	3.0 7.5 24	— — —	3.0 7.5 24	mA
I_{SS}	Quiescent Supply Current	$V_{in} = V_{DD}$ or V_{SS} I_{out} = 0 µA	3.0 5.0 9.0	— — —	800 1200 1600	— — —	800 1200 1600	— — —	1600 2400 3200	µA
V_{in}	Input Voltage — f_{in}, OSC_{in}	Input ac coupled sine wave	—	500	—	500	—	500	—	mV p–p
V_{IL}	Low–Level Input Voltage — f_{in}, OSC_{in}	$V_{out} \ge 2.1$ V Input dc $V_{out} \ge 3.5$ V coupled $V_{out} \ge 6.3$ V square wave	3.0 5.0 9.0	— — —	0 0 0	— — —	0 0 0	— — —	0 0 0	V
V_{IH}	High–Level Input Voltage — f_{in}, OSC_{in}	$V_{out} \le 0.9$ V Input dc $V_{out} \le 1.5$ V coupled $V_{out} \le 2.7$ V square wave	3.0 5.0 9.0	3.0 5.0 9.0	— — —	3.0 5.0 9.0	— — —	3.0 5.0 9.0	— — —	V
V_{IL}	Low–Level Input Voltage — except f_{in}, OSC_{in}		3.0 5.0 9.0	— — —	0.9 1.5 2.7	— — —	0.9 1.5 2.7	— — —	0.9 1.5 2.7	V
V_{IH}	High–Level Input Voltage — except f_{in}, OSC_{in}		3.0 5.0 9.0	2.1 3.5 6.3	— — —	2.1 3.5 6.3	— — —	2.1 3.5 6.3	— — —	V
I_{in}	Input Current (f_{in}, OSC_{in})	$V_{in} = V_{DD}$ or V_{SS}	9.0	± 2.0	± 50	± 2.0	± 25	± 2.0	± 22	µA
I_{IL}	Input Leakage Current (all inputs except f_{in}, OSC_{in})	$V_{in} = V_{SS}$	9.0	—	–0.3	—	–0.1	—	–1.0	µA
I_{IH}	Input Leakage Current (all inputs except f_{in}, OSC_{in})	$V_{in} = V_{DD}$	9.0	—	0.3	—	0.1	—	1.0	µA
C_{in}	Input Capacitance		—	—	10	—	10	—	10	pF
V_{OL}	Low–Level Output Voltage— OSC_{out}	$I_{out} \approx 0$ µA $V_{in} = V_{DD}$	3.0 5.0 9.0	— — —	0.9 1.5 2.7	— — —	0.9 1.5 2.7	— — —	0.9 1.5 2.7	V
V_{OH}	High–Level Output Voltage— OSC_{out}	$I_{out} \approx 0$ µA $V_{in} = V_{SS}$	3.0 5.0 9.0	2.1 3.5 6.3	— — —	2.1 3.5 6.3	— — —	2.1 3.5 6.3	— — —	V

(continued)

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	V_{DD} V	−40°C Min	−40°C Max	25°C Min	25°C Max	85°C Min	85°C Max	Unit
V_{OL}	Low–Level Output Voltage— Other Outputs	$I_{out} \approx 0$ µA	3.0 5.0 9.0	— — —	0.05 0.05 0.05	— — —	0.05 0.05 0.05	— — —	0.05 0.05 0.05	V
V_{OH}	High–Level Output Voltage— Other Outputs	$I_{out} \approx 0$ µA	3.0 5.0 9.0	2.95 4.95 8.95	— — —	2.95 4.95 8.95	— — —	2.95 4.95 8.95	— — —	V
I_{OL}	Low–Level Sinking Current — Modulus Control (MC)	V_{out} = 0.3 V V_{out} = 0.4 V V_{out} = 0.5 V	3.0 5.0 9.0	1.3 1.9 3.8	— — —	1.1 1.7 3.3	— — —	0.66 1.08 2.1	— — —	mA
I_{OH}	High–Level Sourcing Current — Modulus Control (MC)	V_{out} = 2.7 V V_{out} = 4.6 V V_{out} = 8.5 V	3.0 5.0 9.0	−0.6 −0.9 −1.5	— — —	−0.5 −0.75 −1.25	— — —	−0.3 −0.5 −0.8	— — —	mA
I_{OL}	Low–Level Sinking Current — Lock Detect (LD)	V_{out} = 0.3 V V_{out} = 0.4 V V_{out} = 0.5 V	3.0 5.0 9.0	0.25 0.64 1.3	— — —	0.2 0.51 1.0	— — —	0.15 0.36 0.7	— — —	mA
I_{OH}	High–Level Sourcing Current — Lock Detect (LD)	V_{out} = 2.7 V V_{out} = 4.6 V V_{out} = 8.5 V	3.0 5.0 9.0	−0.25 −0.64 −1.3	— — —	−0.2 −0.51 −1.0	— — —	−0.15 −0.36 −0.7	— — —	mA
I_{OL}	Low–Level Sinking Current — Other Outputs	V_{out} = 0.3 V V_{out} = 0.4 V V_{out} = 0.5 V	3.0 5.0 9.0	0.44 0.64 1.3	— — —	0.35 0.51 1.0	— — —	0.22 0.36 0.7	— — —	mA
I_{OH}	High–Level Sourcing Current — Other Outputs	V_{out} = 2.7 V V_{out} = 4.6 V V_{out} = 8.5 V	3.0 5.0 9.0	−0.44 −0.64 −1.3	— — —	−0.35 −0.51 −1.0	— — —	−0.22 −0.36 −0.7	— — —	mA
I_{OZ}	Output Leakage Current — PD_{out}	$V_{out} = V_{DD}$ or V_{SS} Output in Off State	9.0	—	±0.3	—	±0.1	—	±1.0	µA
C_{out}	Output Capacitance — PD_{out}	PD_{out} — Three–State	—	—	10	—	10	—	10	pF

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 10 ns)

Symbol	Parameter	Figure No.	V_{DD} V	Guaranteed Limit 25°C	Guaranteed Limit −40°C to 85°C	Unit
t_{PLH}, t_{PHL}	Maximum Propagation Delay, f_{in} to MC	1, 6	3.0 5.0 9.0	110 60 35	120 70 40	ns
t_W	Output Pulse Width, ϕ_R, ϕ_V, and LD with f_R in Phase with f_V	2, 6	3.0 5.0 9.0	25 to 200 20 to 100 10 to 70	25 to 260 20 to 125 10 to 80	ns
t_{TLH}	Maximum Output Transition Time, MC	3, 6	3.0 5.0 9.0	115 60 40	115 75 60	ns
t_{THL}	Maximum Output Transition Time, MC	3, 6	3.0 5.0 9.0	60 34 30	70 45 38	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, LD	3, 6	3.0 5.0 9.0	180 90 70	200 120 90	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Other Outputs	3, 6	3.0 5.0 9.0	160 80 60	175 100 65	ns
t_{su}	Minimum Set–Up Time, Data to ST	4	3.0 5.0 9.0	10 10 10	— — —	ns
t_{su}	Minimum Set–Up Time, Address to ST	4	3.0 5.0 9.0	25 20 15	— — —	ns

(continued)

AC ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Figure No.	V_{DD} V	Guaranteed Limit 25°C	Guaranteed Limit −40°C to 85°C	Unit
t_h	Minimum Hold Time, Address to ST	4	3.0 5.0 9.0	10 10 10	— — —	ns
t_h	Minimum Hold Time, Data to ST	4	3.0 5.0 9.0	25 20 15	— — —	ns
t_w	Minimum Input Pulse Width, ST	5	3.0 5.0 9.0	40 30 20	— — —	ns

2

SWITCHING WAVEFORMS

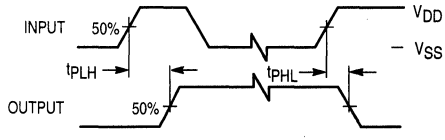
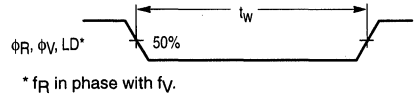


Figure 1.



* f_R in phase with f_V.

Figure 2.

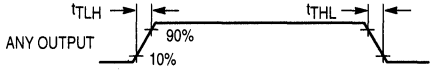


Figure 3.

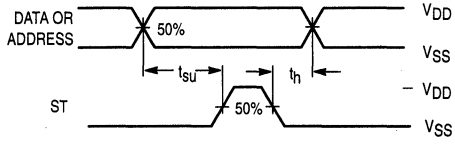


Figure 4.

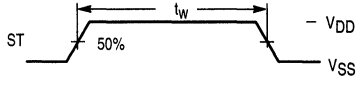
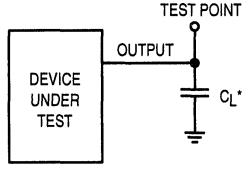


Figure 5.



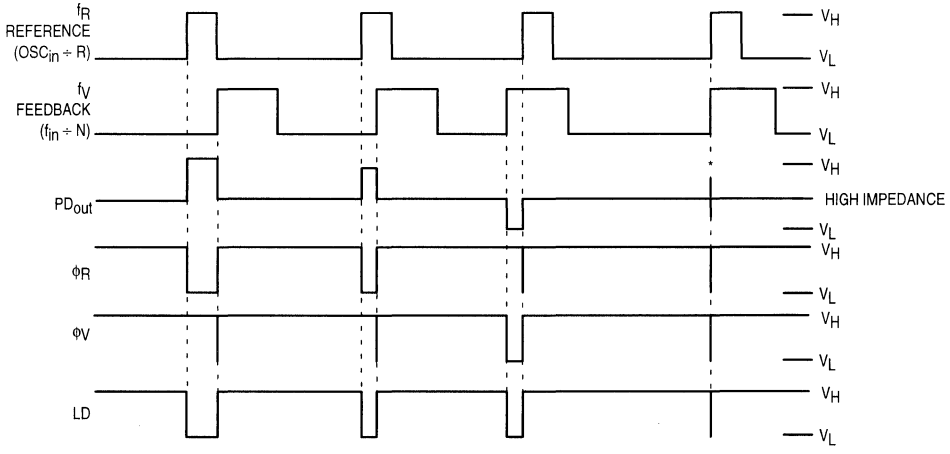
* Includes all probe and fixture capacitance.

Figure 6. Test Circuit

FREQUENCY CHARACTERISTICS (Voltages Referenced to V_{SS}, C_L = 50 pF, Input $t_r = t_f$ = 10 ns unless otherwise specified)

Symbol	Parameter	Test Conditions	V_{DD} V	−40°C Min	−40°C Max	25°C Min	25°C Max	85°C Min	85°C Max	Unit
f_i	Input Frequency (f_{in}, OSC_{in})	R ≥ 8, A ≥ 0, N ≥ 8 V_{in} = 500 mV p–p ac coupled sine wave	3.0 5.0 9.0	— — —	6.0 15 15	— — —	6.0 15 15	— — —	6.0 15 15	MHz
		R ≥ 8, A ≥ 0, N ≥ 8 V_{in} = 1.0 V p–p ac coupled sine wave	3.0 5.0 9.0	— — —	12 22 25	— — —	12 20 22	— — —	7.0 20 22	MHz
		R ≥ 8, A ≥ 0, N ≥ 8 V_{in} = V_{DD} to V_{SS} dc coupled square wave	3.0 5.0 9.0	— — —	13 25 25	— — —	12 22 25	— — —	8.0 22 25	MHz

NOTE: Usually, the PLL's propagation delay from f_{in} to MC plus the set–up time of the prescaler determines the upper frequency limit of the system. The upper frequency limit is found with the following formula: $f = P/(t_p + t_{set})$ where f is the upper frequency in Hz, P is the lower of the dual–modulus prescaler ratios, t_p is the f_{in} to MC propagation delay in seconds, and t_{set} is the prescaler set–up time in seconds. For example, with a 5 V supply, the f_{in} to MC delay is 70 ns. If the MC12028A prescaler is used, the set–up time is 16 ns. Thus, if the 64/65 ratio is utilized, the upper frequency limit is $f = P/(t_p + t_{set}) = 64/(70 + 16) = 744$ MHz.



V_H = High voltage level.
V_L = Low voltage level.
* At this point, when both f_R and f_V are in phase, the output is forced to near mid supply.
NOTE: The PD_{out} generates error pulses during out–of–lock conditions. When locked in phase and frequency, the output is high impedance and the voltage at that pin is determined by the low–pass filter capacitor.

Figure 7. Phase/Frequency Detectors and Lock Detector Output Waveforms

PIN DESCRIPTIONS

INPUT PINS

D0 – D3
Data Inputs (Pins 2, 1, 20, 19)

Information at these inputs is transferred to the internal latches when the ST input is in the high state. D3 (Pin 19) is the most significant bit.

f_{in}
Frequency Input (Pin 3)

Input to ÷N portion of synthesizer. f_{in} is typically derived from loop VCO and is ac coupled into Pin 3. For larger amplitude signals (standard CMOS–logic levels) dc coupling may be used.

OSC_{in}/OSC_{out}
Reference Oscillator Input/Output (Pins 7 and 8)

These pins form an on–chip reference oscillator when connected to terminals of an external parallel resonant crystal. Frequency setting capacitors of appropriate value must be connected from OSC_{in} to ground and OSC_{out} to ground. OSC_{in} may also serve as input for an externally–generated reference signal. This signal is typically ac coupled to OSC_{in}, but for larger amplitude signals (standard CMOS–logic levels) dc coupling may also be used. In the external reference mode, no connection is required to OSC_{out}.

A0 – A2
Address Inputs (Pins 9, 10, 11)

A0, A1, and A2 are used to define which latch receives the information on the data input lines. The addresses refer to the following latches:

A2	A1	A0	Selected	Function	D0	D1	D2	D3
0	0	0	Latch 0	÷ A Bits	0	1	2	3
0	0	1	Latch 1	÷ A Bits	4	5	6	—
0	1	0	Latch 2	÷ N Bits	0	1	2	3
0	1	1	Latch 3	÷ N Bits	4	5	6	7
1	0	0	Latch 4	÷ N Bits	8	9	—	—
1	0	1	Latch 5	Reference Bits	0	1	2	3
1	1	0	Latch 6	Reference Bits	4	5	6	7
1	1	1	Latch 7	Reference Bits	8	9	10	11

ST
Strobe Transfer (Pin 12)

The rising edge of strobe transfers data into the addressed latch. The falling edge of strobe latches data into the latch. This pin should normally be held low to avoid loading latches with invalid data.

OUTPUT PINS

PD_{out}
Single–Ended Phase Detector Output (Pin 5)

Three–state output of phase detector for use as loop error signal.

Frequency $f_V > f_R$ or f_V Leading: Negative Pulses
Frequency $f_V < f_R$ or f_V Lagging: Positive Pulses
Frequency $f_V = f_R$ and Phase Coincidence: High–Impedance State

LD
Lock Detector (Pin 13)

High level when loop is locked (f_R, f_V of same phase and frequency). Pulses low when loop is out of lock.

MC
Modulus Control (Pin 14)

Signal generated by the on–chip control logic circuitry for controlling an external dual–modulus prescaler. The modulus control level is low at the beginning of a count cycle and remains low until the ÷A counter has counted down from its programmed value. At this time, modulus control goes high and remains high until the ÷ N counter has counted the rest of the way down from its programmed value (N – A additional counts since both ÷ N and ÷ A are counting down during the first portion of the cycle). Modulus control is then set back low, the counters preset to their respective programmed values, and the above sequence repeated. This provides for a total programmable divide value (N_T) = N • P + A where P and P + 1 represent the dual–modulus prescaler divide values respectively for high and low modulus control levels; N the number programmed into the ÷ N counter and A the number programmed into the ÷ A counter.

f_V
÷N Counter Output (Pin 15)

This pin is the output of the ÷ N counter that is internally connected to the phase detector input. With this output available, the ÷ N counter can be used independently.

ϕ_V, ϕ_R
Phase Detector Outputs (Pins 16 and 17)

These phase detector outputs can be combined externally for a loop error signal. A single–ended output is also available for this purpose (see PD_{out}).

If frequency f_V is greater than f_R or if the phase of f_V is leading, then error information is provided by ϕ_V pulsing low. ϕ_R remains essentially high.

If the frequency f_V is less than f_R or if the phase of f_V is lagging, then error information is provided by ϕ_R pulsing low. ϕ_V remains essentially high.

If the frequency of $f_V = f_R$ and both are in phase, then both ϕ_V and ϕ_R remain high except for a small minimum time period when both pulse low in phase.

f_R
÷R Counter Output (Pin 18)

This is the output of the ÷ R counter that is internally connected to the phase detector input. With this output available, the ÷ R counter can be used independently.

POWER SUPPLY PINS

V_{SS}
Ground (Pin 4)

Circuit Ground.

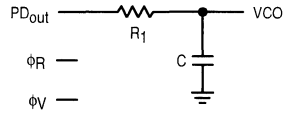
V_{DD}
Positive Power Supply (Pin 6)

The positive supply voltage may range from 3.0 to 9.0 V with respect to V_{SS}.

DESIGN CONSIDERATIONS

PHASE–LOCKED LOOP — LOW–PASS FILTER DESIGN

A)

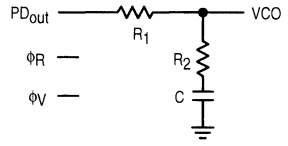


$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NR_1C}}$$

$$\zeta = \frac{N\omega_n}{2K_\phi K_{VCO}}$$

$$F(s) = \frac{1}{R_1sC + 1}$$

B)

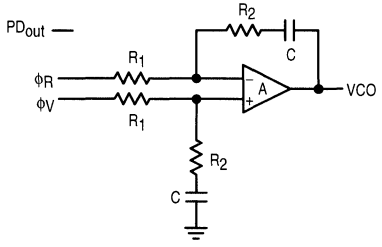


$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NC(R_1 + R_2)}}$$

$$\zeta = 0.5\,\omega_n \left(R_2C + \frac{N}{K_\phi K_{VCO}}\right)$$

$$F(s) = \frac{R_2sC + 1}{(R_1 + R_2)\,sC + 1}$$

C)



$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NCR_1}}$$

$$\zeta = \frac{\omega_n R_2 C}{2}$$

ASSUMING GAIN A IS VERY LARGE, THEN:

$$F(s) = \frac{R_2sC + 1}{R_1sC}$$

NOTE: Sometimes R_1 is split into two series resistors, each $R_1 \div 2$. A capacitor C_C is then placed from the midpoint to ground to further filter ϕ_V and ϕ_R. The value of C_C should be such that the corner frequency of this network does not significantly affect ω_n.

DEFINITIONS:

N = Total Division Ratio in feedback loop

K_ϕ (Phase Detector Gain) = $V_{DD}/4\pi$ for PD_{out}

K_ϕ (Phase Detector Gain) = $V_{DD}/2\pi$ for ϕ_V and ϕ_R

K_{VCO} (VCO Gain) = $\dfrac{2\pi\Delta f_{VCO}}{\Delta V_{VCO}}$

for a typical design w_n (Natural Frequency) $\approx \dfrac{2\pi fr}{10}$ (at phase detector input)

Damping Factor: $\zeta \approx 1$

RECOMMENDED READING:

Gardner, Floyd M., *Phaselock Techniques (second edition).* New York, Wiley–Interscience, 1979.

Manassewitsch, Vadim, *Frequency Synthesizers: Theory and Design (second edition).* New York, Wiley–Interscience, 1980.

Blanchard, Alain, *Phase–Locked Loops: Application to Coherent Receiver Design.* New York, Wiley–Interscience, 1976.

Egan, William F., *Frequency Synthesis by Phase Lock.* New York, Wiley–Interscience, 1981.

Rohde, Ulrich L., *Digital PLL Frequency Synthesizers Theory and Design.* Englewood Cliffs, NJ, Prentice–Hall, 1983.

Berlin, Howard M., *Design of Phase–Locked Loop Circuits, with Experiments.* Indianapolis, Howard W. Sams and Co., 1978.

Kinley, Harold, *The PLL Synthesizer Cookbook.* Blue Ridge Summit, PA, Tab Books, 1980.

AN535, Phase–Locked Loop Design Fundamentals, Motorola Semiconductor Products, Inc., 1970.

AR254, Phase–Locked Loop Design Articles, Motorola Semiconductor Products, Inc., Reprinted with permission from *Electronic Design,* 1987.

DESIGN CONSIDERATIONS

CRYSTAL OSCILLATOR CONSIDERATIONS

The following options may be considered to provide a reference frequency to Motorola's CMOS frequency synthesizers. The most desirable is discussed first.

Use of a Hybrid Crystal Oscillator

Commercially available temperature–compensated crystal oscillators (TCXOs) or crystal–controlled data clock oscillators provide very stable reference frequencies. An oscillator capable of sinking and sourcing 50 μA at CMOS logic levels may be direct or dc coupled to OSC_{in}. In general, the highest frequency capability is obtained utilizing a direct–coupled square wave having a rail–to–rail (V_{DD} to V_{SS}) voltage swing. If the oscillator does not have CMOS logic levels on the outputs, capacitive or ac coupling to OSC_{in} may be used. OSC_{out}, an unbuffered output, should be left floating.

For additional information about TCXOs and data clock oscillators, please consult the latest version of the *eem Electronic Engineers Master Catalog,* the *Gold Book,* or similar publications.

Design an Off–Chip Reference

The user may design an off–chip crystal oscillator using ICs specifically developed for crystal oscillator applications, such as the MC12061 MECL device. The reference signal from the MECL device is ac coupled to OSC_{in}. For large amplitude signals (standard CMOS logic levels), dc coupling is used. OSC_{out}, an unbuffered output, should be left floating. In general, the highest frequency capability is obtained with a direct–coupled square wave having rail–to–rail voltage swing.

Use of the On–Chip Oscillator Circuitry

The on–chip amplifier (a digital inverter) along with an appropriate crystal may be used to provide a reference source frequency. A fundamental mode crystal, parallel resonant at the desired operating frequency, should be connected as shown in Figure 8.

For V_{DD} = 5.0 V, the crystal should be specified for a loading capacitance, C_L, which does not exceed 32 pF for frequencies to approximately 8.0 MHz, 20 pF for frequencies in the area of 8.0 to 15 MHz, and 10 pF for higher frequencies. These are guidelines that provide a reasonable compromise between IC capacitance, drive capability, swamping variations in stray and IC input/output capacitance, and realistic C_L values. The shunt load capacitance, C_L, presented across the crystal can be estimated to be:

$$C_L = \frac{C_{in}C_{out}}{C_{in} + C_{out}} + C_a + C_o + \frac{C1 \cdot C2}{C1 + C2}$$

where

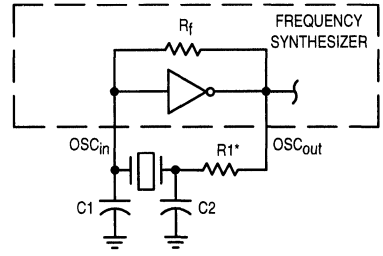
C_{in} = 5.0 pF (see Figure 9)
C_{out} = 6.0 pF (see Figure 9)
C_a = 1.0 pF (see Figure 9)
C_O = the crystal's holder capacitance (see Figure 10)
C1 and C2 = external capacitors (see Figure 8)

The oscillator can be "trimmed" on–frequency by making a portion or all of C1 variable. The crystal and associated components must be located as close as possible to the OSC_{in} and OSC_{out} pins to minimize distortion, stray capacitance, stray inductance, and startup stabilization time. In some cases, stray capacitance should be added to the value for C_{in} and C_{out}.

Power is dissipated in the effective series resistance of the crystal, R_e, in Figure 10. The drive level specified by the crystal manufacturer is the maximum stress that a crystal can withstand without damaging or excessive shift in frequency. R1 in Figure 8 limits the drive level. The use of R1 may not be necessary in some cases (i.e., R1 = 0 ohms).

To verify that the maximum dc supply voltage does not overdrive the crystal, monitor the output frequency as a function of voltage at OSC_{out}. (Care should be taken to minimize loading.) The frequency should increase very slightly as the dc supply voltage is increased. An overdriven crystal will decrease in frequency or become unstable with an increase in supply voltage. The operating supply voltage must be reduced or R1 must be increased in value if the overdriven condition exists. The user should note that the oscillator start–up time is proportional to the value of R1.

Through the process of supplying crystals for use with CMOS inverters, many crystal manufacturers have developed expertise in CMOS oscillator design with crystals. Discussions with such manufacturers can prove very helpful. See Table 1.



* May be deleted in certain cases. See text.

Figure 8. Pierce Crystal Oscillator Circuit

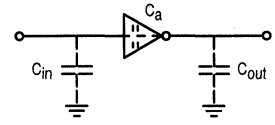
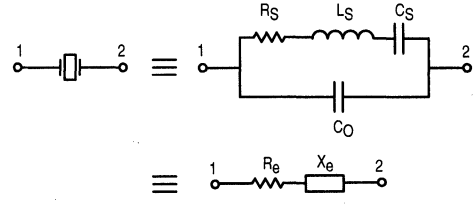


Figure 9. Parasitic Capacitances of the Amplifier



NOTE: Values are supplied by crystal manufacturer (parallel resonant crystal).

Figure 10. Equivalent Crystal Networks

Table 1. Partial List of Crystal Manufacturers

Name	Address	Phone
United States Crystal Corp.	3605 McCart Ave., Ft. Worth, TX 76110	(817) 921–3013
Crystek Crystal	2351 Crystal Dr., Ft. Myers, FL 33907	(813) 936–2109
Statek Corp.	512 N. Main St., Orange, CA 92668	(714) 639–7810

NOTE: Motorola cannot recommend one supplier over another and in no way suggests that this is a complete listing of crystal manufacturers.

RECOMMENDED READING

Technical Note TN–24, Statek Corp.

Technical Note TN–7, Statek Corp.

E. Hafner, "The Piezoelectric Crystal Unit – Definitions and Method of Measurement", *Proc. IEEE,* Vol. 57, No. 2 Feb., 1969.

D. Kemper, L. Rosine, "Quartz Crystals for Frequency Control", *Electro–Technology,* June, 1969.

P. J. Ottowitz, "A Guide to Crystal Selection", *Electronic Design*, May, 1966.

DUAL–MODULUS PRESCALING

OVERVIEW

The technique of dual–modulus prescaling is well established as a method of achieving high performance frequency synthesizer operation at high frequencies. Basically, the approach allows relatively low–frequency programmable counters to be used as high–frequency programmable counters with speed capability of several hundred MHz. This is possible without the sacrifice in system resolution and performance that results if a fixed (single–modulus) divider is used for the prescaler.

In dual–modulus prescaling, the lower speed counters must be uniquely configured. Special control logic is necessary to select the divide value P or P + 1 in the prescaler for the required amount of time (see modulus control definition). Motorola's dual–modulus frequency synthesizers contain this feature and can be used with a variety of dual–modulus prescalers to allow speed, complexity and cost to be tailored to the system requirements. Prescalers having P, P + 1 divide values in the range of ÷ 3/÷ 4 to ÷ 128/÷ 129 can be controlled by most Motorola frequency synthesizers.

Several dual–modulus prescaler approaches suitable for use with the MC145146–2 are:

MC12009	÷ 5/÷ 6	440 MHz
MC12011	÷ 8/÷ 9	500 MHz
MC12013	÷ 10/÷ 11	500 MHz
MC12015	÷ 32/÷ 33	225 MHz
MC12016	÷ 40/÷ 41	225 MHz
MC12017	÷ 64/÷ 65	225 MHz
MC12018	÷ 128/÷ 129	520 MHz
MC12022A	÷ 64/65 or ÷ 128/129	1.1 GHz
MC12032A	÷ 64/65 or ÷ 128/129	2.0 GHz

DESIGN GUIDELINES

The system total divide value, N_{total} (N_T) will be dictated by the application, i.e.,

$$N_T = \frac{\text{frequency into the prescaler}}{\text{frequency into the phase detector}} = N \bullet P + A$$

N is the number programmed into the ÷ N counter, A is the number programmed into the ÷ A counter, P and P + 1 are the two selectable divide ratios available in the dual–modulus prescalers. To have a range of N_T values in sequence, the ÷ A counter is programmed from zero through P – 1 for a particular value N in the ÷ N counter. N is then incremented to N + 1 and the ÷ A is sequenced from 0 through P – 1 again.

There are minimum and maximum values that can be achieved for N_T. These values are a function of P and the size of the ÷ N and ÷ A counters. The constraint $N \geq A$ always applies. If $A_{max} = P - 1$, then $N_{min} \geq P - 1$. Then $N_{Tmin} = (P - 1)\ P + A$ or $(P - 1)\ P$ since A is free to assume the value of 0.

$$N_{Tmax} = N_{max} \bullet P + A_{max}$$

To maximize system frequency capability, the dual–modulus prescaler output must go from low to high after each group of P or P + 1 input cycles. The prescaler should divide by P when its modulus control line is high and by P + 1 when its modulus control is low.

For the maximum frequency into the prescaler (f_{VCO} max), the value used for P must be large enough such that:

1. f_{VCO} max divided by P may not exceed the frequency capability of f_{in} (input to the ÷ N and ÷ A counters).
2. The period of f_{VCO} divided by P must be greater than the sum of the times:
   a. Propagation delay through the dual–modulus prescaler.
   b. Prescaler setup or release time relative to its modulus control signal.
   c. Propagation time from f_{in} to the modulus control output for the frequency synthesizer device.

A sometimes useful simplification in the programming code can be achieved by choosing the values for P of 8, 16, 32, or 64. For these cases, the desired value of N_T results when N_T in binary is used as the program code to the ÷ N and ÷ A counters treated in the following manner:

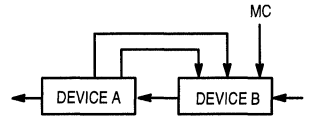
1. Assume the ÷ A counter contains "a" bits where $2^a \geq P$.
2. Always program all higher order ÷ A counter bits above "a" to 0.
3. Assume the ÷ N counter and the ÷ A counter (with all the higher order bits above "a" ignored) combined into a single binary counter of n + a bits in length (n = number of divider stages in the ÷ N counter). The MSB of this "hypothetical" counter is to correspond to the MSB of ÷ N and the LSB is to correspond to the LSB of ÷ A. The system divide value, NT, now results when the value of NT in binary is used to program the "new" n + a bit counter.

By using the two devices, several dual–modulus values are achievable (shown in Figure 11).

APPLICATIONS

The features of the MC145146–2 permit bus operation with a dedicated wire needed only for the strobe input. In a microprocessor–controlled system this strobe input is accessed when the phase lock loop is addressed. The remaining data and address inputs will directly interface to the microprocessor's data and address buses.

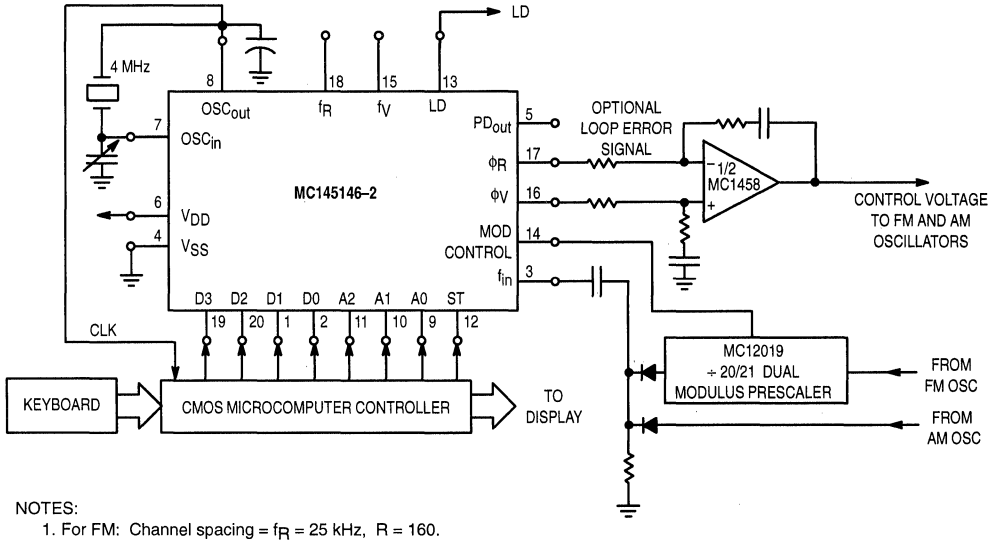
The device architecture allows the user to establish any integer reference divide value between 3 and 4095. The wide selection of ÷R values permits a high degree of flexibility in choosing the reference oscillator frequency. As a result the reference oscillator can frequently be chosen to serve multiple system functions such as a second local oscillator in a receiver design or a microprocessor system clock. Typical applications that take advantage of these MC145146–2 features including the dual modulus capability are shown in Figures 12, 13, and 14.



DEVICE A \ DEVICE B	MC12009	MC12011	MC12013
MC10131	÷ 20/÷ 21	÷ 32/÷ 33	÷ 40/÷ 41
MC10138	÷ 50/÷ 51	÷ 80/÷ 81	÷ 100/÷ 101
MC10154	÷ 40/÷ 41 OR ÷ 80/÷ 81	÷ 64/÷ 65 OR ÷ 128/÷ 129	÷ 80/÷ 81

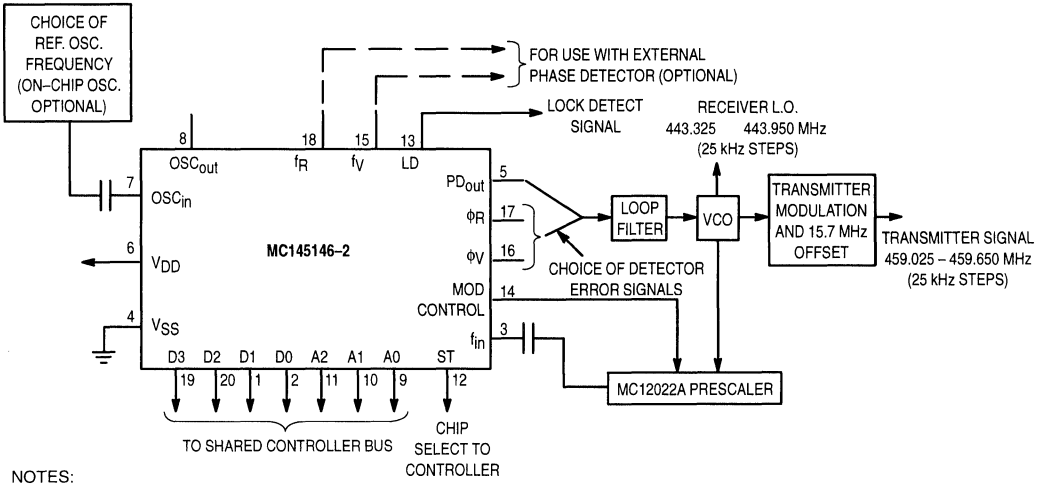
NOTE: MC12009, MC12011, and MC12013 are pin equivalent.
MC12015, MC12016, and MC12017 are pin equivalent.

Figure 11. Dual Modulus Values



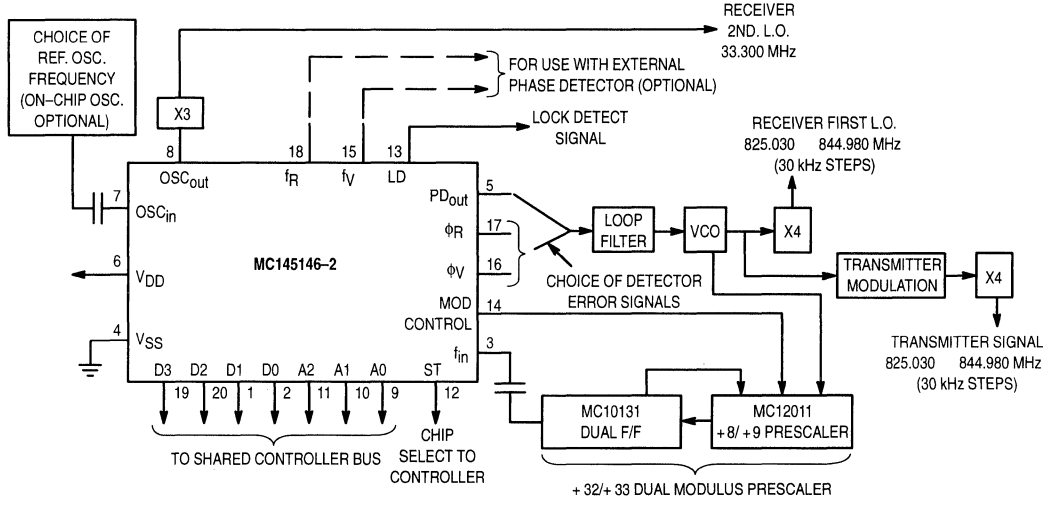
NOTES:
1. For FM: Channel spacing = f_R = 25 kHz, R = 160.
   For AM: Channel spacing = f_R = 1 kHz, R = 4000.
2. Various channel spacings and reference oscillator frequencies can be chosen since any R value from 3 to 4095 can be established.
3. Data and address lines are inactive and high impedance when pin 12 is low. Their interface with the controller may therefore be shared with other system functions if desired.

Figure 12. FM/AM Broadcast Radio Synthesizer



NOTES:
1. Receiver I.F. = 10.7 MHz, low side injection.
2. Duplex operation with 5 MHz receive/transmit separation.
3. f_R = 25 kHz, ÷ R chosen to correspond with desired reference oscillator frequency.
4. N_{total} = 17,733 to 17,758 = N • P + A; N = 277, A = 5 to 30 for P = 64.

Figure 13. Synthesizer for UHF Mobile Radio Telephone Channels Demonstrates Use of the MC145146–2 in Microprocessor/Microcomputer Controlled Systems Operating to Several Hundred MHz



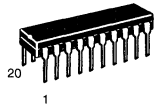
NOTES:
1. Receiver 1st I.F. = 45 MHz, low side injection; Receiver 2nd I.F. = 11.7 MHz, low side injection.
2. Duplex operation with 45 MHz receive/transmit separation.
3. f_R = 7.5 kHz, ÷ R = 1480.
4. N_{total} = N • 32 + A = 27,501 to 28,166; N = 859 to 880; A = 0 to 31.
5. Only one implementation is shown. Various other configurations and dual–modulus prescaling values to ÷ 128/÷ 129 are possible.

Figure 14. 666 Channel, Computer Controlled, Mobile Radio Telephone Synthesizer for 800 MHz Cellular Radio Systems

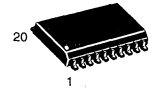
MC145149

Dual PLL Frequency Synthesizer

Interfaces with Dual–Modulus Prescalers



P SUFFIX
PLASTIC DIP
CASE 738



DW SUFFIX
SOG PACKAGE
CASE 751D

ORDERING INFORMATION

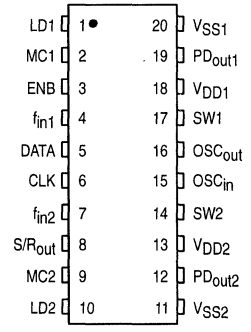
MC145149P	Plastic DIP
MC145149DW	SOG Package

The MC145149 contains two PLL Frequency Synthesizers which share a common serial data port and common reference oscillator. The device contains two 14–stage R counters, two 10–stage N counters, and two 7–stage A counters. All six counters are fully programmable through a serial port. The divide ratios are latched into the appropriate counter latch according to the last data bits (control bits) entered.

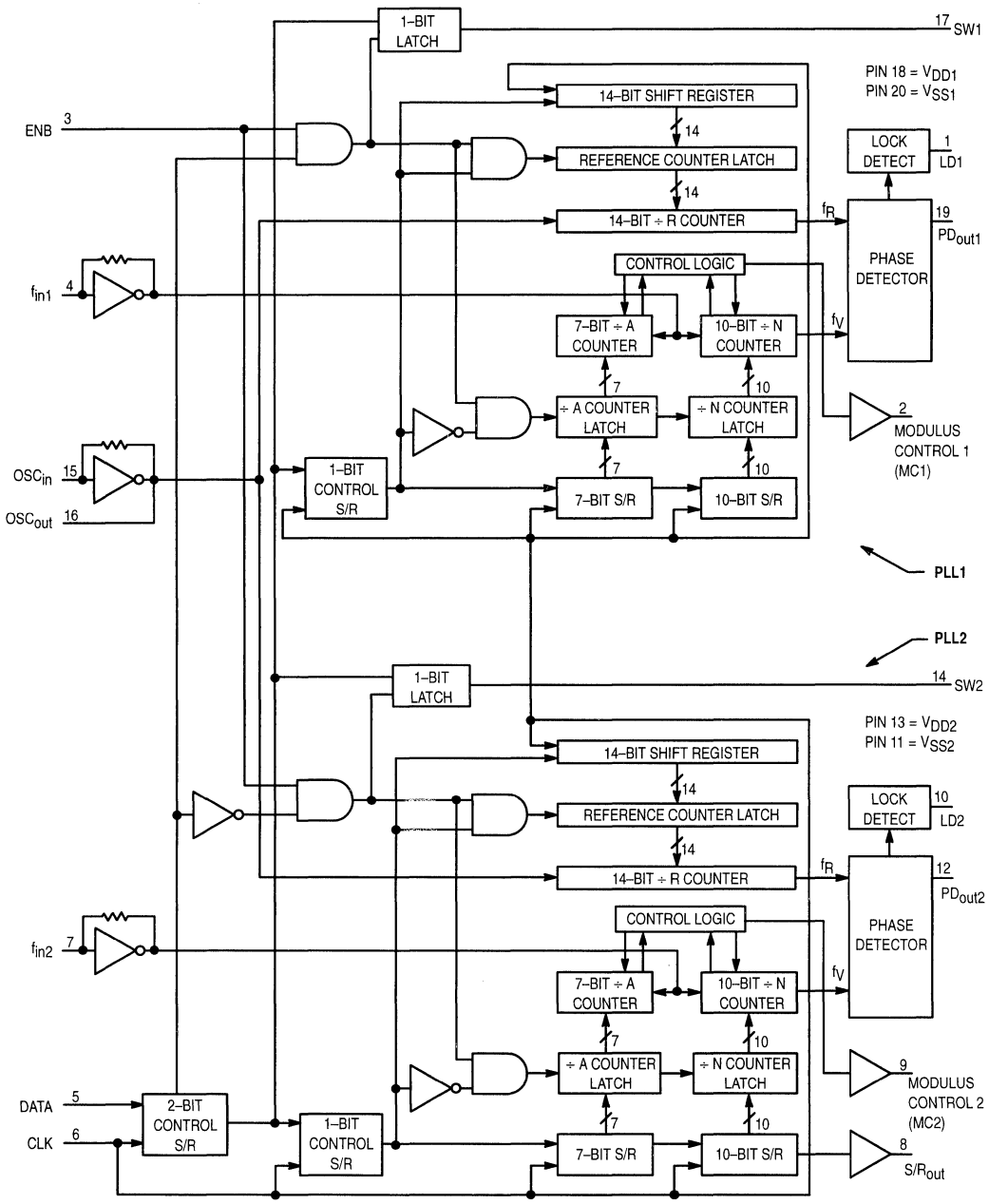
When combined with external low–pass filters and voltage controlled oscillators (VCOs), the MC145149 can provide all the remaining functions for two PLL frequency synthesizers operating up to the device's frequency limit. For higher VCO frequency operation, a down mixer or dual–modulus prescaler can be used between the VCO and the synthesizer IC.

- Low Power Consumption Through Use of CMOS Technology
- Wide Operating Voltage Range: 3 to 9 V
- Operating Temperature Range: – 40 to + 85°C
- ÷ R Range = 3 to 16,383
- ÷ N Range = 3 to 1023
- ÷ A Range = 0 to 127
- Two "Linearized" Three–State Digital Phase Detectors with No Dead Zone
- Two Lock Detect Signals (LD1 and LD2)
- Two Open–Drain Port Expander Outputs (SW1 and SW2)
- Compatible with the Serial Peripheral Interface (SPI) on CMOS MCUs

PIN ASSIGNMENT



BLOCK DIAGRAM



MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Rating	Value	Unit
V_{DD}	DC Supply Voltage	– 0.5 to + 10	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient) except SW1, SW2	– 0.5 to V_{DD} + 0.5	V
V_{out}	Output Voltage (DC or Transient) — SW1, SW2	– 0.5 to 15	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	± 10	mA
I_{DD}, I_{SS}	Supply Current, V_{DD} or V_{SS} Pins	± 30	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature (8–Second Soldering)	260	°C

* Maximum Ratings are those values beyond which damage to the device may occur.
†Power Dissipation Temperature Derating:
Plastic DIP: – 12 mW/°C from 65 to 85°C
SOG Package: – 7 mW/°C from 65 to 85°C

This device contains circuitry to protect against damage due to high static voltages or electric fields, however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$ except SW1 and SW2 which may range up to 15 V.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs should be left floating.

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Symbol	Characteristic		V_{DD} V	– 40°C Min	– 40°C Max	25°C Min	25°C Max	85°C Min	85°C Max	Unit
V_{DD}	Power Supply Voltage Range		—	3	9	3	9	3	9	V
V_{OL}	Output Voltage V_{in} = 0 V or V_{DD} I_{out} = 0 µA	0 Level	3 5 9	— — —	0.05 0.05 0.05	— — —	0.05 0.05 0.05	— — —	0.05 0.05 0.05	V
V_{OH}		1 Level	3 5 9	2.95 4.95 8.95	— — —	2.95 4.95 8.95	— — —	2.95 4.95 8.95	— — —	
V_{IL}	Input Voltage V_{out} = 0.5 V or V_{DD} – 0.5 V (All Outputs Except OSC_{out})	0 Level	3 5 9	— — —	0.9 1.5 2.7	— — —	0.9 1.5 2.7	— — —	0.9 1.5 2.7	V
V_{IH}		1 Level	3 5 9	2.1 3.5 6.3	— — —	2.1 3.5 6.3	— — —	2.1 3.5 6.3	— — —	
I_{OH}	Output Current — MC1, MC2 V_{out} = 2.7 V V_{out} = 4.6 V V_{out} = 8.5 V	Source	3 5 9	– 0.60 – 0.90 – 1.50	— — —	– 0.50 – 0.75 – 1.25	— — —	– 0.30 – 0.50 – 0.80	— — —	mA
I_{OL}	V_{out} = 0.3 V V_{out} = 0.4 V V_{out} = 0.5 V	Sink	3 5 9	1.30 1.90 3.80	— — —	1.10 1.70 3.30	— — —	0.66 1.08 2.10	— — —	
I_{OL}	Output Current — SW1, SW2 V_{out} = 0.3 V V_{out} = 0.4 V V_{out} = 0.5 V	Sink	3 5 9	0.80 1.50 3.50	— — —	0.48 0.90 2.10	— — —	0.24 0.45 1.50	— — —	mA
I_{OH}	Output Current — Other Outputs V_{out} = 2.7 V V_{out} = 4.6 V V_{out} = 8.5 V	Source	3 5 9	– 0.44 – 0.64 – 1.30	— — —	– 0.35 – 0.51 – 1.00	— — —	– 0.22 – 0.36 – 0.70	— — —	mA
I_{OL}	V_{out} = 0.3 V V_{out} = 0.4 V V_{out} = 0.5 V	Sink	3 5 9	0.44 0.64 1.30	— — —	0.35 0.51 1.00	— — —	0.22 0.36 0.70	— — —	
I_{in}	Input Current — DATA, CLK, ENB		9	—	± 0.3	—	± 0.1	—	± 1.0	µA
I_{in}	Input Current — f_{in}, OSC_{in}		9	—	± 50	—	± 25	—	± 22	µA

(continued)

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Characteristic	V_{DD} V	−40°C		25°C		85°C		Unit
			Min	Max	Min	Max	Min	Max	
C_{in}	Input Capacitance	—	—	10	—	10	—	10	pF
C_{out}	Three–State Output Capacitance — PD_{out}	—	—	10	—	10	—	10	pF
I_{DD}	Quiescent Current V_{in} = 0 V or V_{DD} I_{out} = 0 µA	3 5 9	— — —	800 1200 1600	— — —	800 1200 1600	— 	1600 2400 3200	µA
I_{OZ}	Three–State Leakage Current — PD_{out} V_{out} = 0 V or 9 V	9	—	±0.3	—	±0.1	—	±3.0	µA
I_{OZ}	Off–State Leakage Current — SW1, SW2 V_{out} = 9 V	9	—	0.3	—	0.1	—	3.0	µA

SWITCHING CHARACTERISTICS (T_A = 25°C, C_L = 50 pF)

Symbol	Characteristic	Figure No.	V_{DD} V	Min	Max	Unit
t_{TLH}	Output Rise Time, MC1 and MC2	1, 6	3 5 9	— — —	115 60 40	ns
t_{THL}	Output Fall Time, MC1 and MC2	1, 6	3 5 9	— — —	60 34 30	ns
t_{TLH}, t_{THL}	Output Rise and Fall Time, LD and S/R_{out}	1, 6	3 5 9	— — —	140 80 60	ns
t_{PLH}, t_{PHL}	Propagation Delay Time, f_{in} to MC1 or MC2	2, 6	3 5 9	— — —	125 80 50	ns
t_{su}	Setup Time, DATA to CLK	3	3 5 9	30 20 18	— — —	ns
t_{su}	Setup Time, CLK to ENB	3	3 5 9	70 32 25	— — —	ns
t_h	Hold Time, CLK to DATA	3	3 5 9	12 12 15	— — —	ns
t_{rec}	Recovery Time, ENB to CLK	3	3 5 9	5 10 20	— — —	ns
t_r, t_f	Input Rise and Fall Times, Any Input	4	3 5 9	— — —	5 2 0.5	µs
t_w	Input Pulse Width, ENB and CLK	5	3 5 9	40 35 25	— — —	ns

FREQUENCY CHARACTERISTICS (Voltages Referenced to V_{SS}, C_L = 50 pF, Input $t_r = t_f$ = 10 ns unless otherwise indicated)

Symbol	Parameter	Test Conditions	V_{DD} V	– 40°C		25°C		85°C		Unit
				Min	Max	Min	Max	Min	Max	
f_i	Input Frequency (f_{in}, OSC_{in})	R ≥ 8, A ≥ 0, N ≥ 8 V_{in} = 500 mV p–p ac coupled sine wave	3 5 9	— — —	6 15 15	— — —	6 15 15	— — —	6 15 15	MHz
		R ≥ 8, A ≥ 0, N ≥ 8 V_{in} = V_{DD} to V_{SS} dc coupled square wave	3 5 9	— — —	6 15 15	— — —	6 15 15	— — —	6 15 15	MHz

2

SWITCHING WAVEFORMS

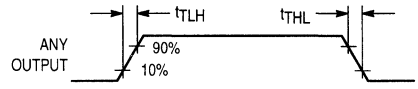


Figure 1.

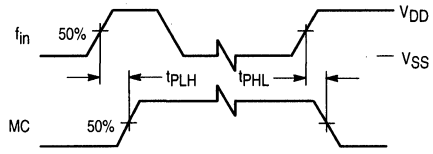


Figure 2.

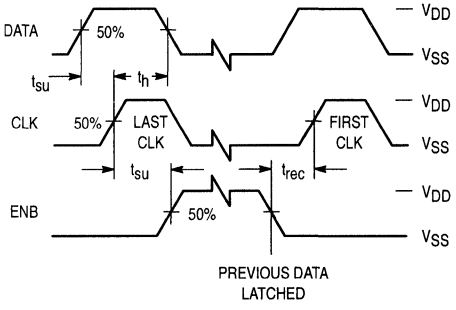


Figure 3.

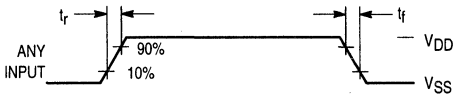


Figure 4.

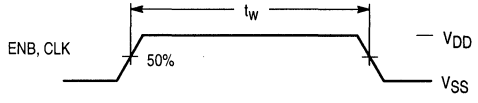
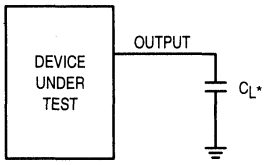


Figure 5.



* Includes all probe and fixture capacitance.

Figure 6.

PIN DESCRIPTIONS

INPUT PINS

OSC_{in}, OSC_{out}
Reference Oscillator Input/Output (Pins 15, 16)

These pins form a reference oscillator when connected to terminals of an external parallel–resonant crystal. Frequency–setting capacitors of appropriate value must be connected from OSC_{in} and OSC_{out} to ground.

OSC_{in} may also serve as input for an externally–generated reference signal. The signal is typically ac coupled to OSC_{in}, but for signals with CMOS logic levels, dc coupling may be used. When used with an external reference, OSC_{out} should be left open.

f_{in1}, f_{in2}
Frequency Inputs (Pins 4, 7)

Input frequency from an external VCO output. Each rising–edge signal on f_{in1} decrements the N counter, and when appropriate, the A counter of PLL 1. Similarly, f_{in2} decrements the counters of PLL 2.

These inputs have inverters biased on the linear region which allows ac coupling for signals as low as 500 mV p–p. With square wave signals which swing from V_{SS} to V_{DD}, dc coupling may be used.

DATA, CLK
Data, Clock Inputs (Pins 5, 6)

Shift register data and clock inputs. Each low–to–high transition on the clock pin shifts one bit of data into the on–chip shift registers. Refer to Figure 7 for the following discussion.

The last bit entered is a steering bit that determines which set of latches are activated. A logic high selects the latches for PLL 1. A logic low selects PLL 2.

The second–to–last bit controls the appropriate port expander output, SW1 or SW2. A logic low forces the output low. A logic high forces the output to the high–impedance state.

The third–to–last bit determines which storage latch is activated. A logic low selects the ÷ A and ÷ N counter latches. A logic high selects the reference counter latch.

When writing to either set of ÷ A and ÷ N counter latches, 20 clock cycles are typically used. However, if a byte–oriented MCU is utilized, 24 clock cycles may be used with the first 4 bits being "Don't Care."

When writing to either reference counter latch, 17 clock cycles are typically used. However, if a byte–oriented MCU is utilized, 24 clock cycles may be used with the first 7 bits being "Don't Care".

ENB
Latch Enable Input (Pin 3)

A positive pulse on this input transfers data from the shift registers to the selected latches, as determined by the control and steering data bits. A logic low level on this pin allows the user to shift data into the shift registers without affecting the data in the latches or counters. Enable is normally held low and is pulsed high to transfer data into the latches.

OUTPUT PINS

PD_{out1}, PD_{out2}
Single–Ended Phase Detector Outputs (Pins 19, 12)

Each single–ended (three–state) phase detector output produces a loop error signal that is used with a loop filter to control a VCO (see Figure 8).

Frequency $f_V > f_R$ or f_V Leading: Negative Pulses
Frequency $f_V < f_R$ or f_V Lagging: Positive Pulses
Frequency $f_V = f_R$ and Phase Coincidence: High–Impedance State

S/R_{out}
Shift Register Output (Pin 8)

This output can be connected to an external shift register to provide band switching or control information. S/R_{out} may also be used to check the counter programming bit stream.

MC1, MC2
Modulus Control Outputs (Pins 2, 9)

Each output generates a signal by the on–chip control logic circuitry for controlling an external dual–modulus prescaler. The modulus control level is low at the beginning of a count cycle and remains low until the ÷ A counter has counted down from its programmed value. At this time, modulus control goes high and remains high until the ÷ N counter has counted the rest of the way down from its programmed value (N–A additional counts since both ÷ N and ÷ A are counting down during the first portion of the cycle). Modulus control is then set back low, the counters are preset to their respective programmed values, and the above sequence is repeated. This provides for a total programmable divide value (N_T) = N • P + A where P and P + 1 represent the dual–modulus prescaler divide values respectively for high and low modulus control levels, N the number programmed into the ÷ N counter, and A the number programmed into the ÷ A counter.

Note that when a prescaler is needed, the dual–modulus version offers a distinct advantage. The dual–modulus prescaler allows a higher reference frequency at the phase detector input, increasing system performance capability, and simplifying the loop filter design.

LD1, LD2
Lock Detect Signals (Pins 1, 10)

Each output is essentially at a high logic level when the corresponding loop is locked (f_R and f_V of the same phase and frequency). Each output pulses low when the corresponding loop is out of lock (see Figure 8).

SW1, SW2
Latched Open–Drain Switch Outputs (Pins 17, 14)

The state of each output is controlled by the "SW STATE" bit shown in Figure 7. If the bit is a logic high, the corresponding SW output assumes the high–impedance state. If the bit is low, the SW output goes low.

To control output SW1, steering bit PLL 1/PLL 2 shown in Figure 7 must be high. To control SW2, bit PLL 1/PLL 2 must be low.

These outputs have an output voltage range of V_{SS} to 15 V.

POWER SUPPLY PINS

V_{DD1}, V_{DD2}
Positive Power Supply (Pins 18, 13)

The most positive power supply potentials. Both of these pins are connected to the substrate of the chip. Therefore, both must be tied to the same voltage potential. This potential may range from 3 to 9 V with respect to the V_{SS} pins.

For optimum performance, V_{DD1} should be bypassed to V_{SS1} and V_{DD2} bypassed to V_{SS2}. That is, two separate bypass capacitors should be utilized.

V_{SS1}, V_{SS2}
Negative Power Supply (Pins 20, 11)

The most negative power supply potentials. Both of these pins should be tied to ground.

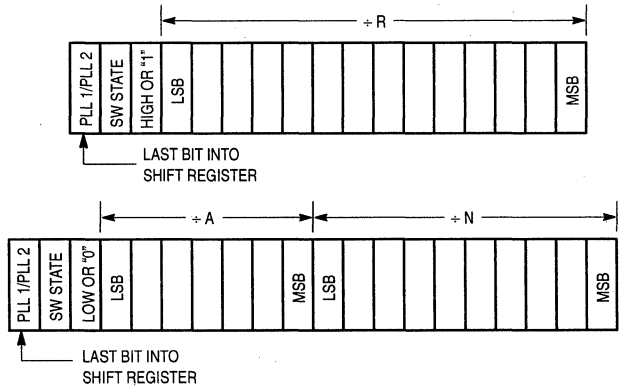
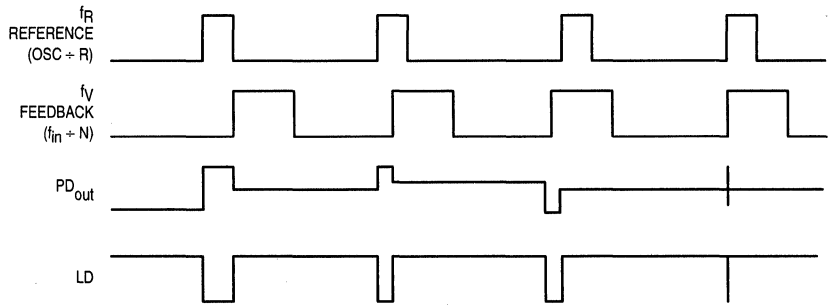


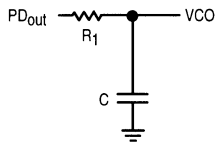
Figure 7. Bit Stream Formats



NOTE: The PD output state is equal to either V_{DD} or V_{SS} when active. When not active, the output is high impedance and the voltage at that pin is determined by the low–pass filter capacitor.

Figure 8. Phase Detector/Lock Detector Output Waveforms

A)

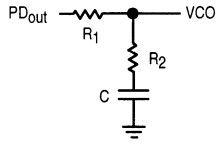


$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NR_1C}}$$

$$\zeta = \frac{N\omega_n}{2K_\phi K_{VCO}}$$

$$F(s) = \frac{1}{R_1sC + 1}$$

B)



$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NC(R_1 + R_2)}}$$

$$\zeta = 0.5\,\omega_n \left(R_2C + \frac{N}{K_\phi K_{VCO}}\right)$$

$$F(s) = \frac{R_2sC + 1}{(R_1 + R_2)sC + 1}$$

DEFINITIONS:

N = Total Division Ratio in Feedback Loop

K_ϕ (Phase Detector Gain) = $V_{DD}/4\pi$ for PD_{out}

K_{VCO} (VCO Gain) = $\frac{2\pi\Delta f_{VCO}}{\Delta V_{VCO}}$

for a typical design ω_n (Natural Frequency) $\approx \frac{2\pi fr}{10}$ (at phase detector input).

Damping Factor: $\zeta \approx 1$

RECOMMENDED READING:

Gardner, Floyd M., *Phaselock Techniques (second edition).* New York, Wiley–Interscience, 1979.
Manassewitsch, Vadim, *Frequency Synthesizers: Theory and Design (second edition).* New York, Wiley–Interscience, 1980.
Blanchard, Alain, *Phase–Locked Loops: Application to Coherent Receiver Design.* New York, Wiley–Interscience, 1976.
Egan, William F., *Frequency Synthesis by Phase Lock.* New York, Wiley–Interscience, 1981.
Rohde, Ulrich L., *Digital PLL Frequency Synthesizers Theory and Design.* Englewood Cliffs, NJ, Prentice–Hall, 1983.
Berlin, Howard M., *Design of Phase–Locked Loop Circuits, with Experiments.* Indianapolis, Howard W. Sams and Co., 1978.
Kinley, Harold, *The PLL Synthesizer Cookbook.* Blue Ridge Summit, PA, Tab Books, 1980.
AN535, Phase–Locked Loop Design Fundamentals, Motorola Semiconductor Products, Inc., 1970.
AR254, Phase–Locked Loop Design Articles, Motorola Semiconductor Products, Inc., Reprinted with permission from *Electronic Design,* 1987.

Figure 9. Phase–Locked Loop Low–Pass Filter Design

DESIGN CONSIDERATIONS

CRYSTAL OSCILLATOR CONSIDERATIONS

The following options may be considered to provide a reference frequency to Motorola's CMOS frequency synthesizers.

Use of a Hybrid Crystal Oscillator

Commercially available temperature–compensate crystal oscillators (TCXOs) or crystal–controlled data clock oscillators provide very stable reference frequencies. An oscillator capable of sinking and sourcing 50 μA at CMOS logic levels may be direct or dc coupled to OSC_{in}. In general, the highest frequency capability is obtained utilizing a direct–coupled square wave having a rail–to–rail (V_{DD} to V_{SS}) voltage swing. If the oscillator does not have CMOS logic levels on the outputs, capacitive or ac coupling to OSC_{in} may be used. OSC_{out}, an unbuffered output, should be left floating.

For additional information about TCXOs and data clock oscillators, please consult the latest version of the *eem Electronic Engineers Master Catalog,* the *Gold Book,* or similar publications.

Design an Off–Chip Reference

The user may design an off–chip crystal oscillator using ICs specifically developed for crystal oscillator applications, such as the MC12061 MECL device. The reference signal from the MECL device is ac coupled to OSC_{in}. For large amplitude signals (standard CMOS logic levels), dc coupling is used. OSC_{out}, an unbuffered output, should be left floating. In general, the highest frequency capability is obtained with a direct–coupled square wave having rail–to–rail voltage swing.

Use of the On–Chip Oscillator Circuitry

The on–chip amplifier (a digital inverter) along with an appropriate crystal may be used to provide a reference source frequency. A fundamental mode crystal, parallel resonant at

the desired operating frequency, should be connected as shown in Figure 10.

For V_{DD} = 5.0 V, the crystal should be specified for a loading capacitance, C_L, which does not exceed 32 pF for frequencies to approximately 8 MHz, 20 pF for frequencies in the area of 8 to 15 MHz, and 10 pF for higher frequencies. These are guidelines that provide a reasonable compromise between IC capacitance, drive capability, swamping variations in stray and IC input/output capacitance, and realistic C_L values. The shunt load capacitance, C_L, presented across the crystal can be estimated to be:

$$C_L = \frac{C_{in}C_{out}}{C_{in} + C_{out}} + C_a + C_O + \frac{C1 \cdot C2}{C1 + C2}$$

where

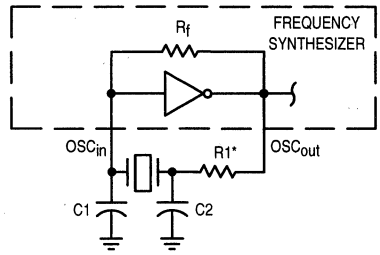
C_{in} = 5 pF (see Figure 11)
C_{out} = 6 pF (see Figure 11)
C_a = 1 pF (see Figure 11)
C_O = the crystal's holder capacitance (see Figure 12)
C1 and C2 = external capacitors (see Figure 10)

The oscillator can be "trimmed" on–frequency by making a portion or all of C1 variable. The crystal and associated components must be located as close as possible to the OSC_{in} and OSC_{out} pins to minimize distortion, stray capacitance, stray inductance, and startup stabilization time. In some cases, stray capacitance should be added to the value for C_{in} and C_{out}.

Power is dissipated in the effective series resistance of the crystal, R_e, in Figure 12. The drive level specified by the crystal manufacturer is the maximum stress that a crystal can withstand without damaging or excessive shift in frequency. R1 in Figure 10 limits the drive level. The use of R1 may not be necessary in some cases (i.e., R1 = 0 Ω).

To verify that the maximum dc supply voltage does not overdrive the crystal, monitor the output frequency as a function of voltage at OSC_{out}. (Care should be taken to minimize loading.) The frequency should increase very slightly as the dc supply voltage is increased. An overdriven crystal will decrease in frequency or become unstable with an increase in supply voltage. The operating supply voltage must be reduced or R1 must be increased in value if the overdriven condition exists. The user should note that the oscillator start–up time is proportional to the value of R1.

Through the process of supplying crystals for use with CMOS inverters, many crystal manufacturers have developed expertise in CMOS oscillator design with crystals. Discussions with such manufacturers can prove very helpful (see Table 1).



* May be deleted in certain cases. See text.

Figure 10. Pierce Crystal Oscillator Circuit

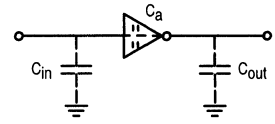
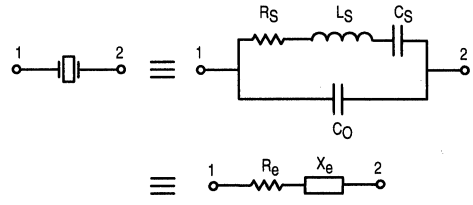


Figure 11. Parasitic Capacitances of the Amplifier



NOTE: Values are supplied by crystal manufacturer (parallel resonant crystal).

Figure 12. Equivalent Crystal Networks

RECOMMENDED READING

Technical Note TN–24, Statek Corp.

Technical Note TN–7, Statek Corp.

E. Hafner, "The Piezoelectric Crystal Unit – Definitions and Method of Measurement", *Proc. IEEE,* Vol. 57, No. 2 Feb., 1969.

D. Kemper, L. Rosine, "Quartz Crystals for Frequency Control", *Electro–Technology,* June, 1969.

P. J. Ottowitz, "A Guide to Crystal Selection", *Electronic Design*, May, 1966.

Table 1. Partial List of Crystal Manufacturers

Name	Address	Phone
United States Crystal Corp.	3605 McCart Ave., Ft. Worth, TX 76110	(817) 921–3013
Crystek Crystal	2351 Crystal Dr., Ft. Myers, FL 33907	(813) 936–2109
Statek Corp.	512 N. Main St., Orange, CA 92668	(714) 639–7810

NOTE: Motorola cannot recommend one supplier over another and in no way suggests that this is a complete listing of crystal manufacturers.

DUAL–MODULUS PRESCALING

OVERVIEW

The technique of dual–modulus prescaling is well established as a method of achieving high performance frequency synthesizer operation at high frequencies. Basically, the approach allows relatively low–frequency programmable counters to be used as high–frequency programmable counters with speed capability of several hundred MHz. This is possible without the sacrifice in system resolution and performance that results if a fixed (single–modulus) divider is used for the prescaler.

In dual–modulus prescaling, the lower speed counters must be uniquely configured. Special control logic is necessary to select the divide value P or P + 1 in the prescaler for the required amount of time (see modulus control definition). Motorola's dual–modulus frequency synthesizers contain this feature and can be used with a variety of dual–modulus prescalers to allow speed, complexity, and cost to be tailored to the system requirements. Prescalers having P, P + 1 divide values in the range of ÷ 3/÷ 4 to ÷ 128/÷ 129 can be controlled by most Motorola frequency synthesizers.

Several dual–modulus prescaler approaches suitable for use with the MC145149 are:

MC12009	÷ 5/÷ 6	440 MHz
MC12011	÷ 8/÷ 9	500 MHz
MC12013	÷ 10/÷ 11	500 MHz
MC12015	÷ 32/÷ 33	225 MHz
MC12016	÷ 40/÷ 41	225 MHz
MC12017	÷ 64/÷ 65	225 MHz
MC12018	÷ 128/÷ 129	520 MHz
MC12022A	÷ 64/65 or ÷ 128/129	1.1 GHz
MC12032A	÷ 64/65 or ÷ 128/129	2.0 GHz

DESIGN GUIDELINES

The system total divide value, N_{total} (N_T) will be dictated by the application, i.e.,

$$N_T = \frac{\text{frequency into the prescaler}}{\text{frequency into the phase detector}} = N \bullet P + A$$

N is the number programmed into the ÷ N counter, A is the number programmed into the ÷ A counter, P and P + 1 are the two selectable divide ratios available in the dual–modulus prescalers. To have a range of N_T values in sequence, the ÷ A counter is programmed from 0 through P – 1 for a particular value N in the ÷ N counter. N is then incremented to N + 1 and the ÷ A is sequenced from 0 through P – 1 again.

There are minimum and maximum values that can be achieved for N_T. These values are a function of P and the size of the ÷ N and ÷ A counters.

The constraint $N \geq A$ always applies. If $A_{max} = P - 1$, then $N_{min} \geq P - 1$. Then $N_{Tmin} = (P - 1)\,P + A$ or $(P - 1)\,P$ since A is free to assume the value of 0.

$$N_{Tmax} = N_{max} \bullet P + A_{max}$$

To maximize system frequency capability, the dual–modulus prescaler output must go from low to high after each group of P or P + 1 input cycles. The prescaler should divide by P when its modulus control line is high and by P + 1 when its modulus control is low.

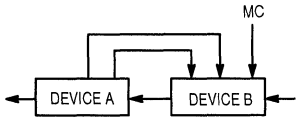
For the maximum frequency into the prescaler (f_{VCO} max), the value used for P must be large enough such that:

1. f_{VCO} max divided by P may not exceed the frequency capability of f_{in} (input to the ÷ N and ÷ A counters).
2. The period of f_{VCO} divided by P must be greater than the sum of the times:
   a. Propagation delay through the dual–modulus prescaler.
   b. Prescaler setup or release time relative to its modulus control signal.
   c. Propagation time from f_{in} to the modulus control output for the frequency synthesizer device.

A sometimes useful simplification in the programming code can be achieved by choosing the values for P of 8, 16, 32, or 64. For these cases, the desired value of N_T results when N_T in binary is used as the program code to the ÷ N and ÷ A counters treated in the following manner:

1. Assume the ÷ A counter contains "a" bits where $2^a \geq P$.
2. Always program all higher order ÷ A counter bits above "a" to 0.
3. Assume the ÷ N counter and the ÷ A counter (with all the higher order bits above "a" ignored) combined into a single binary counter of n + a bits in length (n = number of divider stages in the ÷ N counter). The MSB of this "hypothetical" counter is to correspond to the MSB of ÷ N and the LSB is to correspond to the LSB of ÷ A. The system divide value, N_T, now results when the value of N_T in binary is used to program the "new" n + a bit counter.

By using the two devices, several dual–modulus values are achievable.



DEVICE A \ DEVICE B	MC12009	MC12011	MC12013
MC10131	÷ 20/÷ 21	÷ 32/÷ 33	÷ 40/÷ 41
MC10138	÷ 50/÷ 51	÷ 80/÷ 81	÷ 100/÷ 101
MC10154	÷ 40/÷ 41 OR ÷ 80/÷ 81	÷ 64/÷ 65 OR ÷ 128/÷ 129	÷ 80/÷ 81

NOTE: MC12009, MC12011, and MC12013 are pin equivalent.
MC12015, MC12016, and MC12017 are pin equivalent.

MC145151-2
MC145152-2
MC145155-2
MC145156-2
MC145157-2
MC145158-2

PLL Frequency Synthesizer Family

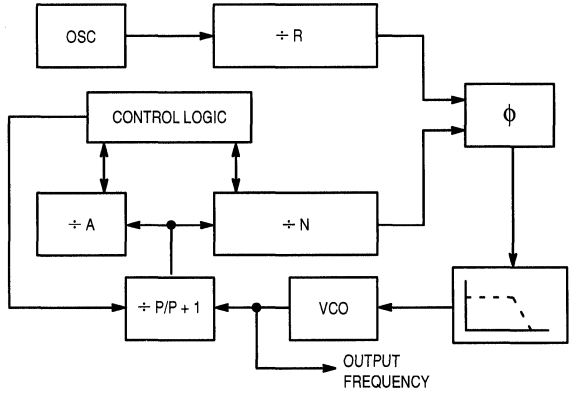
CMOS

2

The devices described in this document are typically used as low–power, phase–locked loop frequency synthesizers. When combined with an external low–pass filter and voltage–controlled oscillator, these devices can provide all the remaining functions for a PLL frequency synthesizer operating up to the device's frequency limit. For higher VCO frequency operation, a down mixer or a prescaler can be used between the VCO and the synthesizer IC.

These frequency synthesizer chips can be found in the following and other applications:

CATV	TV Tuning
AM/FM Radios	Scanning Receivers
Two–Way Radios	Amateur Radio



CONTENTS

REV 1
8/95

MC145151-2

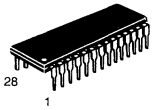
Parallel-Input PLL Frequency Synthesizer

Interfaces with Single–Modulus Prescalers

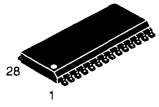
The MC145151–2 is programmed by 14 parallel–input data lines for the N counter and three input lines for the R counter. The device features consist of a reference oscillator, selectable–reference divider, digital–phase detector, and 14–bit programmable divide–by–N counter.

The MC145151–2 is an improved–performance drop–in replacement for the MC145151–1. The power consumption has decreased and ESD and latch–up performance have improved.

- Operating Temperature Range: – 40 to 85°C
- Low Power Consumption Through Use of CMOS Technology
- 3.0 to 9.0 V Supply Range
- On– or Off–Chip Reference Oscillator Operation
- Lock Detect Signal
- ÷ N Counter Output Available
- Single Modulus/Parallel Programming
- 8 User–Selectable ÷ R Values: 8, 128, 256, 512, 1024, 2048, 2410, 8192
- ÷ N Range = 3 to 16383
- "Linearized" Digital Phase Detector Enhances Transfer Function Linearity
- Two Error Signal Options: Single–Ended (Three–State) or Double–Ended
- Chip Complexity: 8000 FETs or 2000 Equivalent Gates



P SUFFIX
PLASTIC DIP
CASE 710

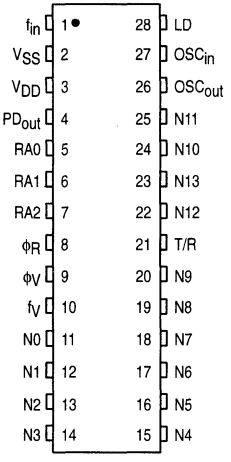


DW SUFFIX
SOG PACKAGE
CASE 751F

ORDERING INFORMATION

MC145151P2	Plastic DIP
MC145151DW2	SOG Package

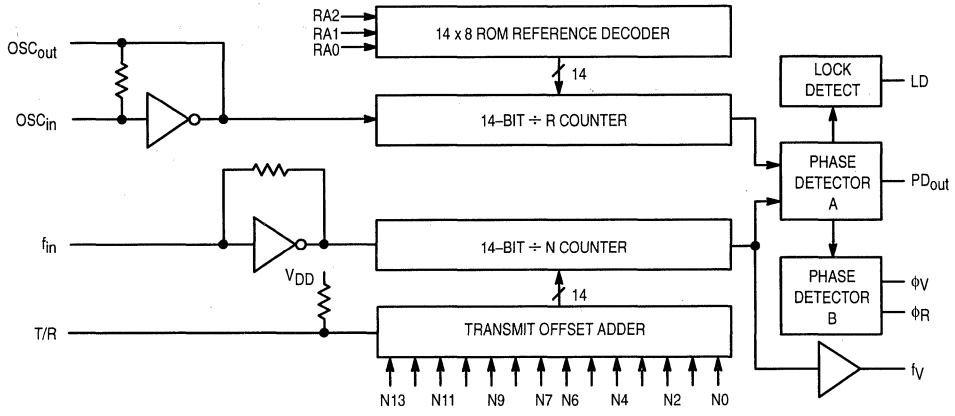
PIN ASSIGNMENT



2

REV 1
8/95

MC145151–2 BLOCK DIAGRAM



NOTE: N0 – N13 inputs and inputs RA0, RA1, and RA2 have pull–up resistors that are not shown.

PIN DESCRIPTIONS

INPUT PINS

f_{in}
Frequency Input (Pin 1)

Input to the ÷ N portion of the synthesizer. f_{in} is typically derived from loop VCO and is ac coupled into the device. For larger amplitude signals (standard CMOS logic levels) dc coupling may be used.

RA0 – RA2
Reference Address Inputs (Pins 5, 6, 7)

These three inputs establish a code defining one of eight possible divide values for the total reference divider, as defined by the table below.

Pull–up resistors ensure that inputs left open remain at a logic 1 and require only a SPST switch to alter data to the zero state.

Reference Address Code			Total Divide Value
RA2	RA1	RA0	
0	0	0	8
0	0	1	128
0	1	0	256
0	1	1	512
1	0	0	1024
1	0	1	2048
1	1	0	2410
1	1	1	8192

N0 – N11
N Counter Programming Inputs (Pins 11 – 20, 22 – 25)

These inputs provide the data that is preset into the ÷ N counter when it reaches the count of zero. N0 is the least significant and N13 is the most significant. Pull–up resistors ensure that inputs left open remain at a logic 1 and require only an SPST switch to alter data to the zero state.

T/R
Transmit/Receive Offset Adder Input (Pin 21)

This input controls the offset added to the data provided at the N inputs. This is normally used for offsetting the VCO frequency by an amount equal to the IF frequency of the transceiver. This offset is fixed at 856 when T/R is low and gives no offset when T/R is high. A pull–up resistor ensures that no connection will appear as a logic 1 causing no offset addition.

OSC_{in}, OSC_{out}
Reference Oscillator Input/Output (Pins 27, 26)

These pins form an on–chip reference oscillator when connected to terminals of an external parallel resonant crystal. Frequency setting capacitors of appropriate value must be connected from OSC_{in} to ground and OSC_{out} to ground. OSC_{in} may also serve as the input for an externally–generated reference signal. This signal is typically ac coupled to OSC_{in}, but for larger amplitude signals (standard CMOS logic levels) dc coupling may also be used. In the external reference mode, no connection is required to OSC_{out}.

OUTPUT PINS

PD_{out}
Phase Detector A Output (Pin 4)

Three–state output of phase detector for use as loop–error signal. Double–ended outputs are also available for this purpose (see ϕV and ϕR).

Frequency $f_V > f_R$ or f_V Leading: Negative Pulses
Frequency $f_V < f_R$ or f_V Lagging: Positive Pulses
Frequency $f_V = f_R$ and Phase Coincidence: High–Impedance State

ϕ_R, ϕ_V
Phase Detector B Outputs (Pins 8, 9)

These phase detector outputs can be combined externally for a loop–error signal. A single–ended output is also available for this purpose (see **PD_{out}**).

If frequency f_V is greater than f_R or if the phase of f_V is leading, then error information is provided by ϕ_V pulsing low. ϕ_R remains essentially high.

If the frequency f_V is less than f_R or if the phase of f_V is lagging, then error information is provided by ϕ_R pulsing low. ϕ_V remains essentially high.

If the frequency of $f_V = f_R$ and both are in phase, then both ϕ_V and ϕ_R remain high except for a small minimum time period when both pulse low in phase.

f_V
N Counter Output (Pin 10)

This is the buffered output of the ÷ N counter that is internally connected to the phase detector input. With this output available, the ÷ N counter can be used independently.

LD
Lock Detector Output (Pin 28)

Essentially a high level when loop is locked (f_R, f_V of same phase and frequency). Pulses low when loop is out of lock.

POWER SUPPLY

V_{DD}
Positive Power Supply (Pin 3)

The positive power supply potential. This pin may range from + 3 to + 9 V with respect to V_{SS}.

V_{SS}
Negative Power Supply (Pin 2)

The most negative supply potential. This pin is usually ground.

2

TYPICAL APPLICATIONS

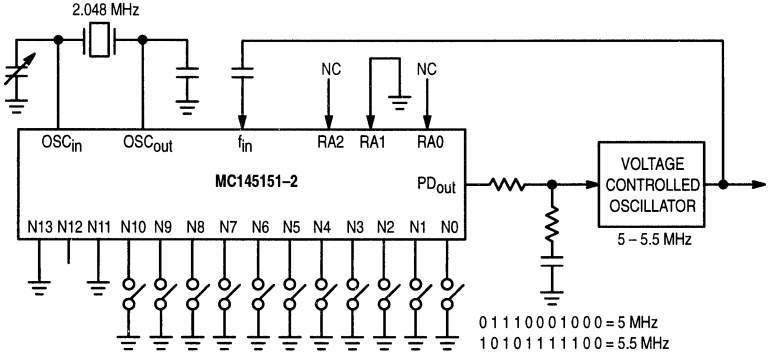
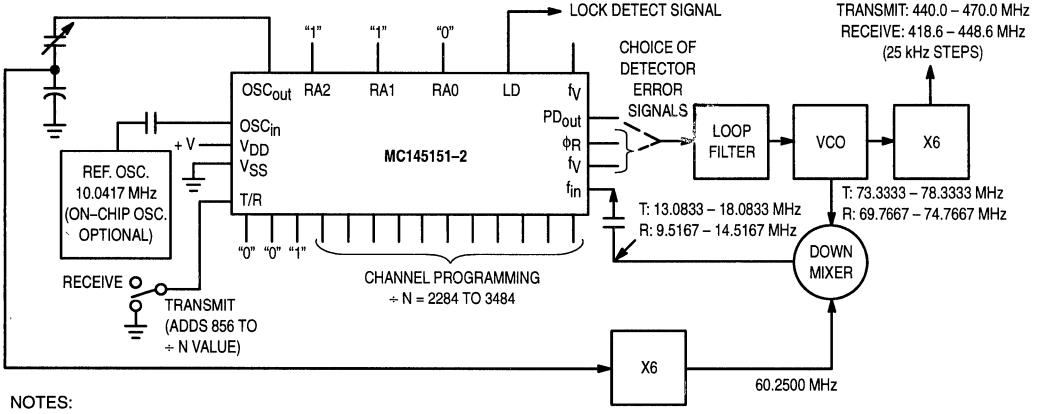


Figure 1. 5 MHz to 5.5 MHz Local Oscillator Channel Spacing = 1 kHz



NOTES:
1. f_R = 4.1667 kHz; ÷ R = 2410; 21.4 MHz low side injection during receive.
2. Frequency values shown are for the 440 – 470 MHz band. Similar implementation applies to the 406 – 440 MHz band. For 470 – 512 MHz, consider reference oscillator frequency X9 for mixer injection signal (90.3750 MHz).

Figure 2. Synthesizer for Land Mobile Radio UHF Bands

MC145151–2 Data Sheet Continued on Page 2–650

MC145152-2

Parallel-Input PLL Frequency Synthesizer

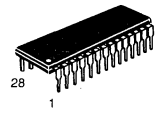
Interfaces with Dual–Modulus Prescalers

2

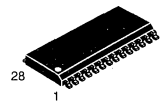
The MC145152–2 is programmed by sixteen parallel inputs for the N and A counters and three input lines for the R counter. The device features consist of a reference oscillator, selectable–reference divider, two–output phase detector, 10–bit programmable divide–by–N counter, and 6–bit programmable ÷ A counter.

The MC145152–2 is an improved–performance drop–in replacement for the MC145152–1. Power consumption has decreased and ESD and latch–up performance have improved.

- Operating Temperature Range: – 40 to 85°C
- Low Power Consumption Through Use of CMOS Technology
- 3.0 to 9.0 V Supply Range
- On– or Off–Chip Reference Oscillator Operation
- Lock Detect Signal
- Dual Modulus/Parallel Programming
- 8 User–Selectable ÷ R Values: 8, 64, 128, 256, 512, 1024, 1160, 2048
- ÷ N Range = 3 to 1023, ÷ A Range = 0 to 63
- Chip Complexity: 8000 FETs or 2000 Equivalent Gates
- See Application Note AN980



P SUFFIX
PLASTIC DIP
CASE 710

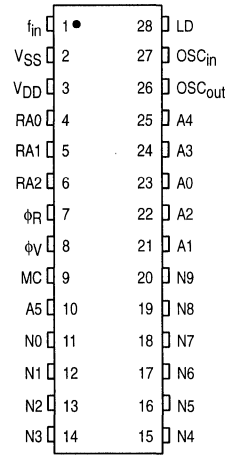


DW SUFFIX
SOG PACKAGE
CASE 751F

ORDERING INFORMATION

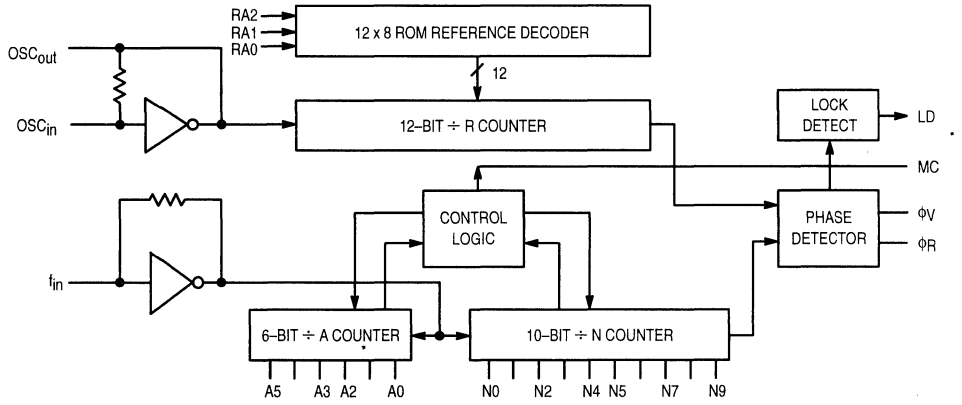
MC145152P2	Plastic DIP
MC145152DW2	SOG Package

PIN ASSIGNMENT



REV 1
8/95

MC145152–2 BLOCK DIAGRAM



NOTE: N0 – N9, A0 – A5, and RA0 – RA2 have pull–up resistors that are not shown.

PIN DESCRIPTIONS

INPUT PINS

f_{in}
Frequency Input (Pin 1)

Input to the positive edge triggered ÷ N and ÷ A counters. f_{in} is typically derived from a dual–modulus prescaler and is ac coupled into the device. For larger amplitude signals (standard CMOS logic levels) dc coupling may be used.

RA0, RA1, RA2
Reference Address Inputs (Pins 4, 5, 6)

These three inputs establish a code defining one of eight possible divide values for the total reference divider. The total reference divide values are as follows:

Reference Address Code			Total Divide Value
RA2	RA1	RA0	
0	0	0	8
0	0	1	64
0	1	0	128
0	1	1	256
1	0	0	512
1	0	1	1024
1	1	0	1160
1	1	1	2048

N0 – N9
N Counter Programming Inputs (Pins 11 – 20)

The N inputs provide the data that is preset into the ÷ N counter when it reaches the count of 0. N0 is the least significant digit and N9 is the most significant. Pull–up resistors ensure that inputs left open remain at a logic 1 and require only a SPST switch to alter data to the zero state.

A0 – A5
A Counter Programming Inputs
(Pins 23, 21, 22, 24, 25, 10)

The A inputs define the number of clock cycles of f_{in} that require a logic 0 on the MC output (see **Dual–Modulus Prescaling** section). The A inputs all have internal pull–up resistors that ensure that inputs left open will remain at a logic 1.

OSC_{in}, OSC_{out}
Reference Oscillator Input/Output (Pins 27, 26)

These pins form an on–chip reference oscillator when connected to terminals of an external parallel resonant crystal. Frequency setting capacitors of appropriate value must be connected from OSC_{in} to ground and OSC_{out} to ground. OSC_{in} may also serve as the input for an externally–generated reference signal. This signal is typically ac coupled to OSC_{in}, but for larger amplitude signals (standard CMOS logic levels) dc coupling may also be used. In the external reference mode, no connection is required to OSC_{out}.

OUTPUT PINS

ϕR, ϕV
Phase Detector B Outputs (Pins 7, 8)

These phase detector outputs can be combined externally for a loop–error signal.

If the frequency f_V is greater than f_R or if the phase of f_V is leading, then error information is provided by ϕV pulsing low. ϕR remains essentially high.

If the frequency f_V is less than f_R or if the phase of f_V is lagging, then error information is provided by ϕR pulsing low. ϕV remains essentially high.

If the frequency of $f_V = f_R$ and both are in phase, then both ϕV and ϕR remain high except for a small minimum time period when both pulse low in phase.

MC
Dual–Modulus Prescale Control Output (Pin 9)

Signal generated by the on–chip control logic circuitry for controlling an external dual–modulus prescaler. The MC level will be low at the beginning of a count cycle and will remain low until the ÷ A counter has counted down from its programmed value. At this time, MC goes high and remains high until the ÷ N counter has counted the rest of the way down from its programmed value (N – A additional counts since both ÷ N and ÷ A are counting down during the first

portion of the cycle). MC is then set back low, the counters preset to their respective programmed values, and the above sequence repeated. This provides for a total programmable divide value (N_T) = N • P + A where P and P + 1 represent the dual–modulus prescaler divide values respectively for high and low MC levels, N the number programmed into the ÷ N counter, and A the number programmed into the ÷ A counter.

LD
Lock Detector Output (Pin 28)

Essentially a high level when loop is locked (f_R, f_V of same phase and frequency). Pulses low when loop is out of lock.

POWER SUPPLY

V_{DD}
Positive Power Supply (Pin 3)

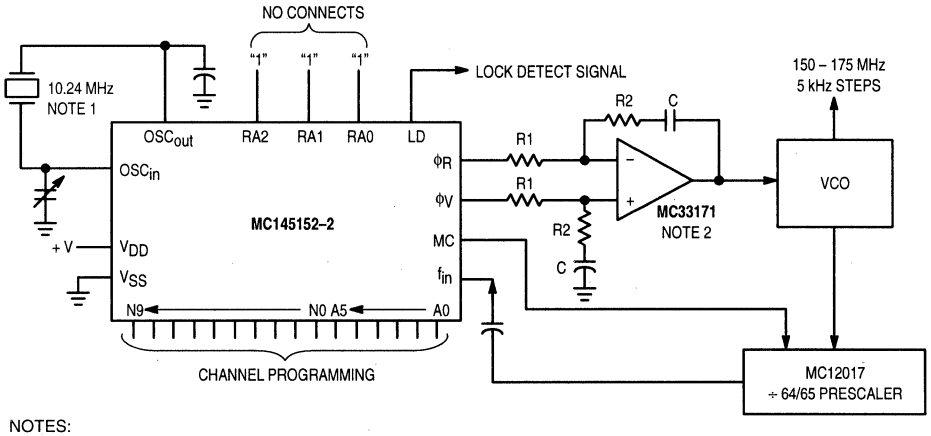
The positive power supply potential. This pin may range from + 3 to + 9 V with respect to V_{SS}.

V_{SS}
Negative Power Supply (Pin 2)

The most negative supply potential. This pin is usually ground.

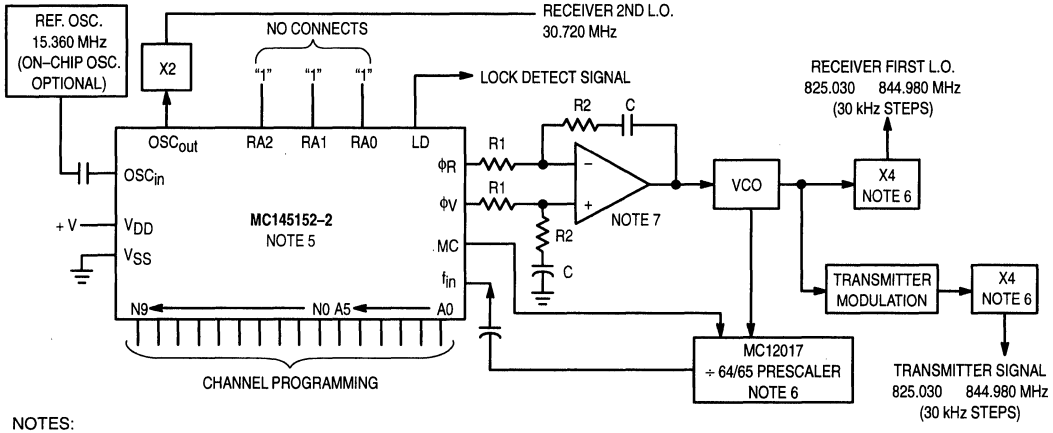
2

TYPICAL APPLICATIONS



NOTES:
1. Off–chip oscillator optional.
2. The ϕ_R and ϕ_V outputs are fed to an external combiner/loop filter. See the Phase–Locked Loop — Low–Pass Filter Design page for additional information. The ϕ_R and ϕ_V outputs swing rail–to–rail. Therefore, the user should be careful not to exceed the common mode input range of the op amp used in the combiner/loop filter.

Figure 1. Synthesizer for Land Mobile Radio VHF Bands



NOTES:

1. Receiver 1st I.F. = 45 MHz, low side injection; Receiver 2nd I.F. = 11.7 MHz, low side injection.
2. Duplex operation with 45 MHz receiver/transmit separation.
3. f_R = 7.5 kHz; ÷ R = 2048.
4. N_{total} = N • 64 + A = 27501 to 28166; N = 429 to 440; A = 0 to 63.
5. MC145158–2 may be used where serial data entry is desired.
6. High frequency prescalers (e.g., MC12018 [520 MHz] and MC12022 [1 GHz]) may be used for higher frequency VCO and f_{ref} implementations.
7. The ϕ_R and ϕ_V outputs are fed to an external combiner/loop filter. See the Phase–Locked Loop — Low–Pass Filter Design page for additional information. The ϕ_R and ϕ_V outputs swing rail–to–rail. Therefore, the user should be careful not to exceed the common mode input range of the op amp used in the combiner/loop filter.

Figure 2. 666–Channel, Computer–Controlled, Mobile Radiotelephone Synthesizer for 800 MHz Cellular Radio Systems

MC145152–2 Data Sheet Continued on Page 2–650

MC145155-2

Serial-Input PLL Frequency Synthesizer

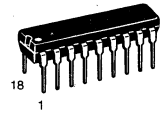
Interfaces with Single–Modulus Prescalers

2

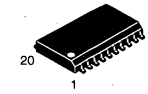
The MC145155–2 is programmed by a clocked, serial input, 16–bit data stream. The device features consist of a reference oscillator, selectable–reference divider, digital–phase detector, 14–bit programmable divide–by–N counter, and the necessary shift register and latch circuitry for accepting serial input data.

The MC145155–2 is an improved–performance drop–in replacement for the MC145155–1. Power consumption has decreased and ESD and latch–up performance have improved.

- Operating Temperature Range: – 40 to 85°C
- Low Power Consumption Through Use of CMOS Technology
- 3.0 to 9.0 V Supply Range
- On– or Off–Chip Reference Oscillator Operation with Buffered Output
- Compatible with the Serial Peripheral Interface (SPI) on CMOS MCUs
- Lock Detect Signal
- Two Open–Drain Switch Outputs
- 8 User–Selectable ÷ R Values: 16, 512, 1024, 2048, 3668, 4096, 6144, 8192
- Single Modulus/Serial Programming
- ÷ N Range = 3 to 16383
- "Linearized" Digital Phase Detector Enhances Transfer Function Linearity
- Two Error Signal Options: Single–Ended (Three–State) or Double–Ended
- Chip Complexity: 6504 FETs or 1626 Equivalent Gates



P SUFFIX
PLASTIC DIP
CASE 707



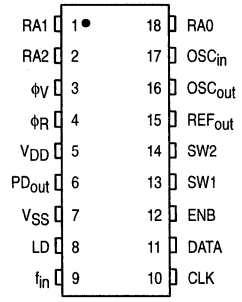
DW SUFFIX
SOG PACKAGE
CASE 751D

ORDERING INFORMATION

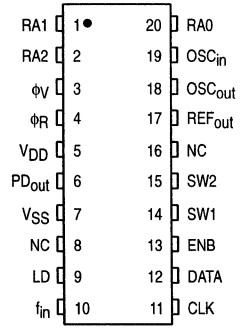
MC145155P2	Plastic DIP
MC145155DW2	SOG Package

PIN ASSIGNMENTS

PLASTIC DIP



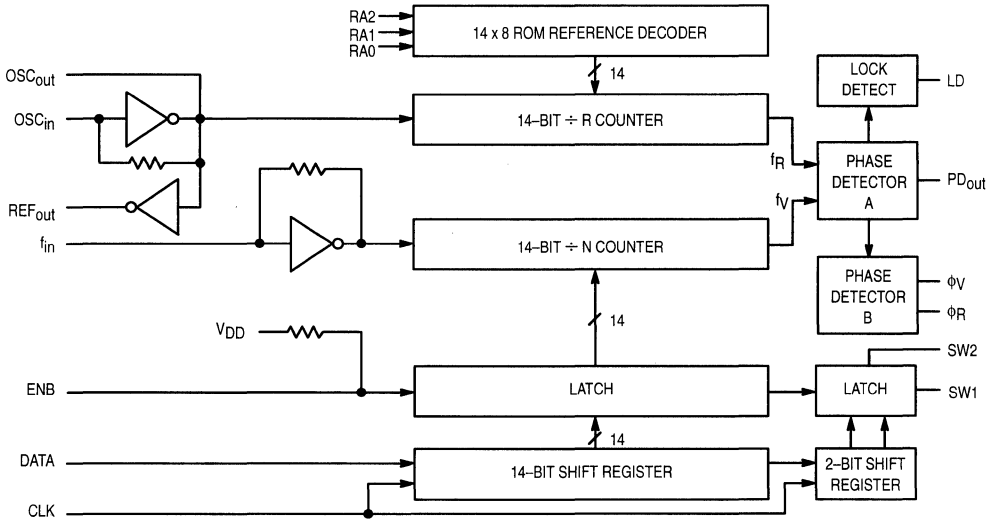
SOG PACKAGE



NC = NO CONNECTION

REV 1
8/95

MC145155–2 BLOCK DIAGRAM



PIN DESCRIPTIONS

INPUT PINS

f_{in}
Frequency Input (PDIP – Pin 9, SOG – Pin 10)

Input to the ÷ N portion of the synthesizer. f_{in} is typically derived from loop VCO and is ac coupled into the device. For larger amplitude signals (standard CMOS logic levels) dc coupling may be used.

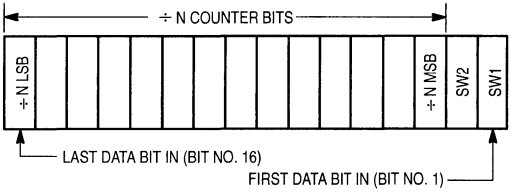
RA0, RA1, RA2
Reference Address Inputs (PDIP – Pins 18, 1, 2; SOG – Pins 20, 1, 2)

These three inputs establish a code defining one of eight possible divide values for the total reference divider, as defined by the table below:

Reference Address Code			Total Divide Value
RA2	RA1	RA0	
0	0	0	16
0	0	1	512
0	1	0	1024
0	1	1	2048
1	0	0	3668
1	0	1	4096
1	1	0	6144
1	1	1	8192

CLK, DATA
Shift Register Clock, Serial Data Inputs (PDIP – Pins 10, 11; SOG – Pins 11, 12)

Each low–to–high transition clocks one bit into the on–chip 16–bit shift register. The Data input provides programming information for the 14–bit ÷ N counter and the two switch signals SW1 and SW2. The entry format is as follows:



ENB
Latch Enable Input (PDIP – Pin 12, SOG – Pin 13)

When high (1), ENB transfers the contents of the shift register into the latches, and to the programmable counter inputs, and the switch outputs SW1 and SW2. When low (0), ENB inhibits the above action and thus allows changes to be made in the shift register data without affecting the counter programming and switch outputs. An on–chip pull–up establishes a continuously high level for ENB when no external signal is applied. ENB is normally low and is pulsed high to transfer data to the latches.

OSC_{in}, OSC_{out}
Reference Oscillator Input/Output (PDIP – Pins 17, 16; SOG – Pins 19, 18)

These pins form an on–chip reference oscillator when connected to terminals of an external parallel resonant crystal. Frequency setting capacitors of appropriate value must be connected from OSC_{in} to ground and OSC_{out} to ground. OSC_{in} may also serve as the input for an externally–generated reference signal. This signal is typically ac coupled to OSC_{in}, but for larger amplitude signals (standard CMOS logic levels) dc coupling may also be used. In the external reference mode, no connection is required to OSC_{out}.

OUTPUT PINS

PD_{out}
Phase Detector A Output (PDIP, SOG – Pin 6)

Three–state output of phase detector for use as loop error signal. Double–ended outputs are also available for this purpose (see ϕ_V and ϕ_R).

Frequency $f_V > f_R$ or f_V Leading: Negative Pulses
Frequency $f_V < f_R$ or f_V Lagging: Positive Pulses
Frequency $f_V = f_R$ and Phase Coincidence: High–Impedance State

ϕ_R, ϕ_V
Phase Detector B Outputs (PDIP, SOG – Pins 4, 3)

These phase detector outputs can be combined externally for a loop–error signal. A single–ended output is also available for this purpose (see **PD_{out}**).

If frequency f_V is greater than f_R or if the phase of f_V is leading, then error information is provided by ϕ_V pulsing low. ϕ_R remains essentially high.

If the frequency f_V is less than f_R or if the phase of f_V is lagging, then error information is provided by ϕ_R pulsing low. ϕ_V remains essentially high.

If the frequency of $f_V = f_R$ and both are in phase, then both ϕ_V and ϕ_R remain high except for a small minimum time period when both pulse low in phase.

LD
Lock Detector Output (PDIP – Pin 8, SOG – Pin 9)

Essentially a high level when loop is locked (f_R, f_V of same phase and frequency). LD pulses low when loop is out of lock.

SW1, SW2
Band Switch Outputs (PDIP – Pins 13, 14; SOG – Pins 14, 15)

SW1 and SW2 provide latched open–drain outputs corresponding to data bits numbers one and two. These outputs can be tied through external resistors to voltages as high as 15 V, independent of the V_{DD} supply voltage. These are typically used for band switch functions. A logic 1 causes the output to assume a high–impedance state, while a logic 0 causes the output to be low.

REF_{out}
Buffered Reference Oscillator Output (PDIP, SOG – Pin 15)

Buffered output of on–chip reference oscillator or externally provided reference–input signal.

POWER SUPPLY

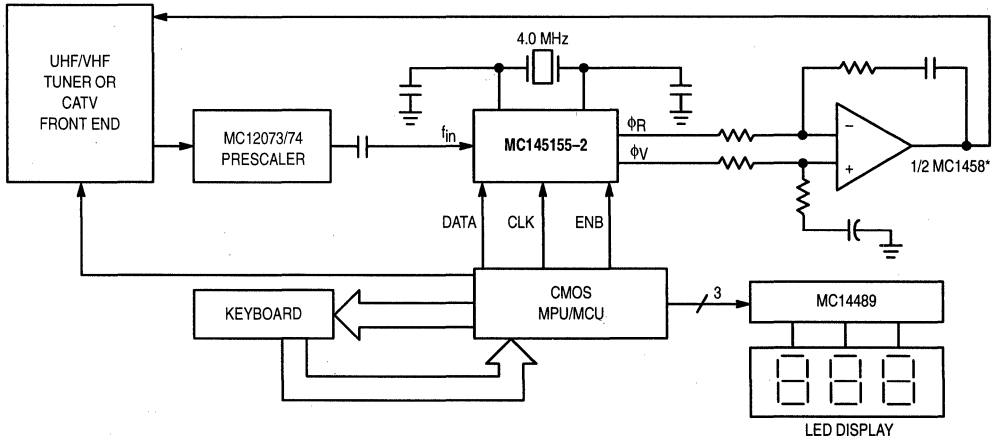
V_{DD}
Positive Power Supply (PDIP, SOG – Pin 5)

The positive power supply potential. This pin may range from + 3 to + 9 V with respect to V_{SS}.

V_{SS}
Negative Power Supply (PDIP, SOG – Pin 7)

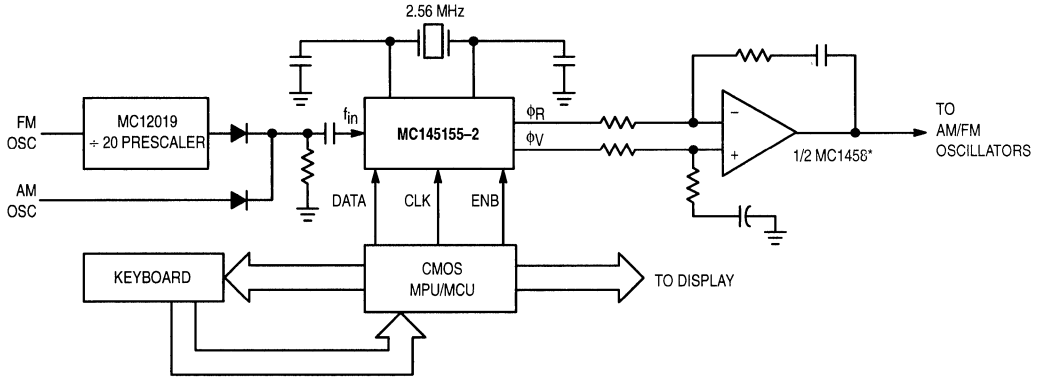
The most negative supply potential. This pin is usually ground.

TYPICAL APPLICATIONS



* The ϕ_R and ϕ_V outputs are fed to an external combiner/loop filter. See the Phase–Locked Loop — Low–Pass Filter Design page for additional information. The ϕ_R and ϕ_V outputs swing rail–to–rail. Therefore, the user should be careful not to exceed the common mode input range of the op amp used in the combiner/loop filter.

Figure 1. Microprocessor–Controlled TV/CATV Tuning System with Serial Interface



* The ϕ_R and ϕ_V outputs are fed to an external combiner/loop filter. See the Phase–Locked Loop — Low–Pass Filter Design page for additional information. The ϕ_R and ϕ_V outputs swing rail–to–rail. Therefore, the user should be careful not to exceed the common mode input range of the op amp used in the combiner/loop filter.

Figure 2. AM/FM Radio Synthesizer

MC145155–2 Data Sheet Continued on Page 2–650

MC145156-2

Serial-Input PLL Frequency Synthesizer

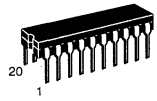
Interfaces with Dual–Modulus Prescalers

2

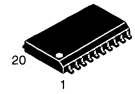
The MC145156–2 is programmed by a clocked, serial input, 19–bit data stream. The device features consist of a reference oscillator, selectable–reference divider, digital–phase detector, 10–bit programmable divide–by–N counter, 7–bit programmable divide–by–A counter, and the necessary shift register and latch circuitry for accepting serial input data.

The MC145156–2 is an improved–performance drop–in replacement for the MC145156–1. Power consumption has decreased and ESD and latch–up performance have improved.

- Operating Temperature Range: – 40 to 85°C
- Low Power Consumption Through Use of CMOS Technology
- 3.0 to 9.0 V Supply Range
- On– or Off–Chip Reference Oscillator Operation with Buffered Output
- Compatible with the Serial Peripheral Interface (SPI) on CMOS MCUs
- Lock Detect Signal
- Two Open–Drain Switch Outputs
- Dual Modulus/Serial Programming
- 8 User–Selectable ÷ R Values: 8, 64, 128, 256, 640, 1000, 1024, 2048
- ÷ N Range = 3 to 1023, ÷ A Range = 0 to 127
- "Linearized" Digital Phase Detector Enhances Transfer Function Linearity
- Two Error Signal Options: Single–Ended (Three–State) or Double–Ended
- Chip Complexity: 6504 FETs or 1626 Equivalent Gates



P SUFFIX
PLASTIC DIP
CASE 738

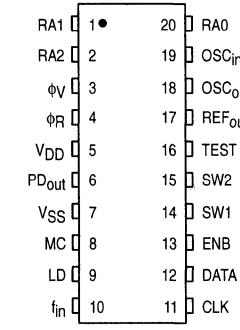


DW SUFFIX
SOG PACKAGE
CASE 751D

ORDERING INFORMATION

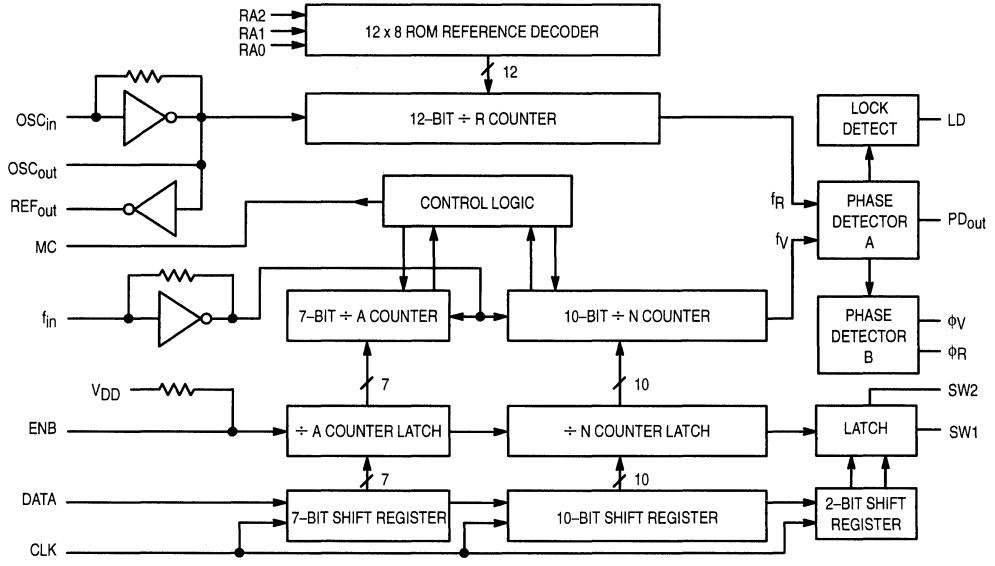
MC145156P2	Plastic DIP
MC145156DW2	SOG Package

PIN ASSIGNMENT



REV 1
8/95

MC145156–2 BLOCK DIAGRAM



PIN DESCRIPTIONS

INPUT PINS

f_{in}
Frequency Input (Pin 10)

Input to the positive edge triggered ÷ N and ÷ A counters. f_{in} is typically derived from a dual–modulus prescaler and is ac coupled into the device. For larger amplitude signals (standard CMOS logic levels), dc coupling may be used.

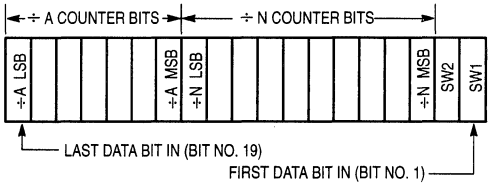
RA0, RA1, RA2
Reference Address Inputs (Pins 20, 1, 2)

These three inputs establish a code defining one of eight possible divide values for the total reference divider, as defined by the table below:

Reference Address Code			Total Divide Value
RA2	RA1	RA0	
0	0	0	8
0	0	1	64
0	1	0	128
0	1	1	256
1	0	0	640
1	0	1	1000
1	1	0	1024
1	1	1	2048

CLK, DATA
Shift Register Clock, Serial Data Inputs (Pins 11, 12)

Each low–to–high transition clocks one bit into the on–chip 19–bit shift register. The data input provides programming information for the 10–bit ÷ N counter, the 7–bit ÷ A counter, and the two switch signals SW1 and SW2. The entry format is as follows:



ENB
Latch Enable Input (Pin 13)

When high (1), ENB transfers the contents of the shift register into the latches, and to the programmable counter inputs, and the switch outputs SW1 and SW2. When low (0), ENB inhibits the above action and thus allows changes to be made in the shift register data without affecting the counter programming and switch outputs. An on–chip pull–up establishes a continuously high level for ENB when no external signal is applied. ENB is normally low and is pulsed high to transfer data to the latches.

OSC_{in}, OSC_{out}
Reference Oscillator Input/Output (Pins 19, 18)

These pins form an on–chip reference oscillator when connected to terminals of an external parallel resonant crystal. Frequency setting capacitors of appropriate value must be connected from OSC_{in} to ground and OSC_{out} to ground. OSC_{in} may also serve as the input for an externally–generated reference signal. This signal is typically ac coupled to OSC_{in}, but for larger amplitude signals (standard CMOS logic levels) dc coupling may also be used. In the external reference mode, no connection is required to OSC_{out}.

TEST
Factory Test Input (Pin 16)

Used in manufacturing. Must be left open or tied to V_{SS}.

OUTPUT PINS

PD_{out}
Phase Detector A Output (Pin 6)

Three–state output of phase detector for use as loop–error signal. Double–ended outputs are also available for this purpose (see ϕV and ϕR).

Frequency $f_V > f_R$ or f_V Leading: Negative Pulses
Frequency $f_V < f_R$ or f_V Lagging: Positive Pulses
Frequency $f_V = f_R$ and Phase Coincidence: High–Impedance State

2

ϕR, ϕV
Phase Detector B Outputs (Pins 4, 3)

These phase detector outputs can be combined externally for a loop–error signal. A single–ended output is also available for this purpose (see **PD_{out}**).

If frequency f_V is greater than f_R or if the phase of f_V is leading, then error information is provided by ϕV pulsing low. ϕR remains essentially high.

If the frequency f_V is less than f_R or if the phase of f_V is lagging, then error information is provided by ϕR pulsing low. ϕV remains essentially high.

If the frequency of $f_V = f_R$ and both are in phase, then both ϕV and ϕR remain high except for a small minimum time period when both pulse low in phase.

MC
Dual–Modulus Prescale Control Output (Pin 8)

Signal generated by the on–chip control logic circuitry for controlling an external dual–modulus prescaler. The MC level will be low at the beginning of a count cycle and will remain low until the ÷ A counter has counted down from its programmed value. At this time, MC goes high and remains high until the ÷ N counter has counted the rest of the way down from its programmed value (N – A additional counts since both ÷ N and ÷ A are counting down during the first portion of the cycle). MC is then set back low, the counters preset to their respective programmed values, and the above sequence repeated. This provides for a total programmable divide value (N_T) = N • P + A where P and P + 1 represent the dual–modulus prescaler divide values respectively for high and low MC levels, N the number programmed into the ÷ N counter, and A the number programmed into the ÷ A counter.

LD
Lock Detector Output (Pin 9)

Essentially a high level when loop is locked (f_R, f_V of same phase and frequency). LD pulses low when loop is out of lock.

SW1, SW2
Band Switch Outputs (Pins 14, 15)

SW1 and SW2 provide latched open–drain outputs corresponding to data bits numbers one and two. These outputs can be tied through external resistors to voltages as high as 15 V, independent of the V_{DD} supply voltage. These are typically used for band switch functions. A logic 1 causes the output to assume a high–impedance state, while a logic 0 causes the output to be low.

REF_{out}
Buffered Reference Oscillator Output (Pin 17)

Buffered output of on–chip reference oscillator or externally provided reference–input signal.

POWER SUPPLY

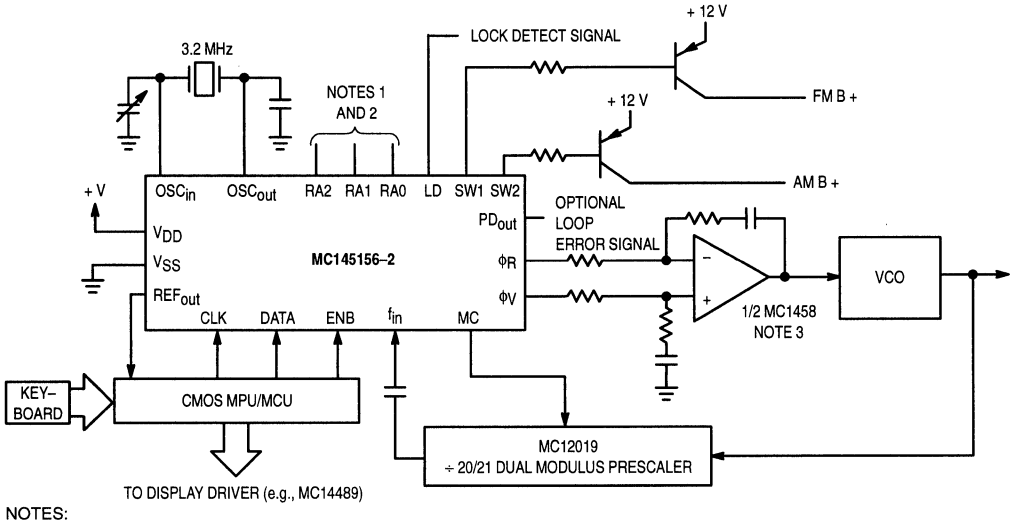
V_{DD}
Positive Power Supply (Pin 5)

The positive power supply potential. This pin may range from + 3 to + 9 V with respect to V_{SS}.

V_{SS}
Negative Power Supply (Pin 7)

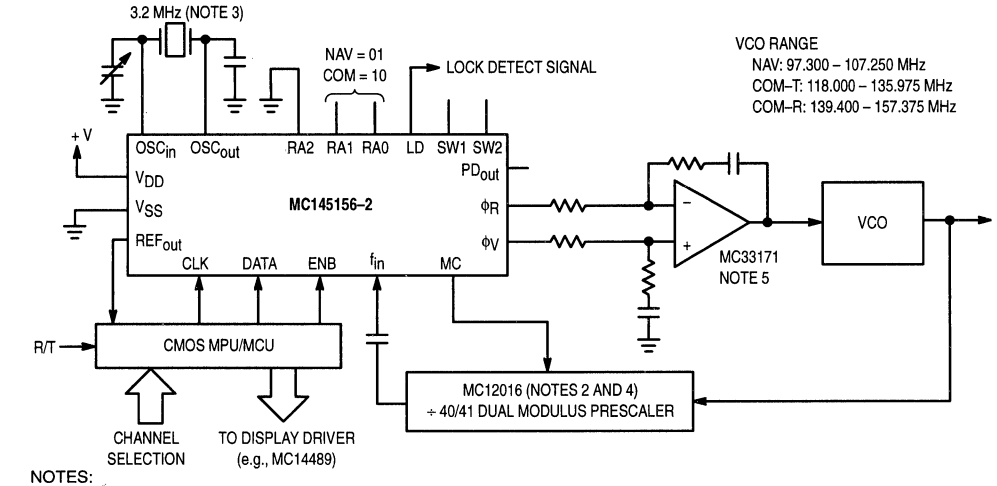
The most negative supply potential. This pin is usually ground.

TYPICAL APPLICATIONS



NOTES:
1. For AM: channel spacing = 5 kHz, ÷ R = ÷ 640 (code 100).
2. For FM: channel spacing = 25 kHz, ÷ R = ÷ 128 (code 010).
3. The ϕ_R and ϕ_V outputs are fed to an external combiner/loop filter. See the Phase–Locked Loop — Low–Pass Filter Design page for additional information. The ϕ_R and ϕ_V outputs swing rail–to–rail. Therefore, the user should be careful not to exceed the common mode input range of the op amp used in the combiner/loop filter.

Figure 1. AM/FM Radio Broadcast Synthesizer



NOTES:
1. For NAV: f_R = 50 kHz, ÷ R = 64 using 10.7 MHz lowside injection, N_{total} = 1946 – 2145.
   For COM–T: f_R = 25 kHz, ÷ R = 128, N_{total} = 4720 – 5439.
   For COM–R: f_R = 25 kHz, ÷ R = 128, using 21.4 MHz highside injection, N_{total} = 5576 – 6295.
2. A ÷ 32/33 dual modulus approach is provided by substituting an MC12015 for the MC12016. The devices are pin equivalent.
3. A 6.4 MHz oscillator crystal can be used by selecting ÷ R = 128 (code 010) for NAV and ÷ R = 256 (code 011) for COM.
4. MC12013 + MC10131 combination may also be used to form the ÷ 40/41 prescaler.
5. The ϕ_R and ϕ_V outputs are fed to an external combiner/loop filter. See the Phase–Locked Loop — Low–Pass Filter Design page for additional information. The ϕ_R and ϕ_V outputs swing rail–to–rail. Therefore, the user should be careful not to exceed the common mode input range of the op amp used in the combiner/loop filter.

Figure 2. Avionics Navigation or Communication Synthesizer

MC145156–2 Data Sheet Continued on Page 2–650

MC145157-2

Serial-Input PLL Frequency Synthesizer

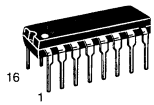
Interfaces with Single–Modulus Prescalers

2

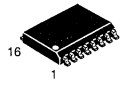
The MC145157–2 has a fully programmable 14–bit reference counter, as well as a fully programmable ÷ N counter. The counters are programmed serially through a common data input and latched into the appropriate counter latch, according to the last data bit (control bit) entered.

The MC145157–2 is an improved–performance drop–in replacement for the MC145157–1. Power consumption has decreased and ESD and latch–up performance have improved.

- Operating Temperature Range: – 40 to 85°C
- Low Power Consumption Through Use of CMOS Technology
- 3.0 to 9.0 V Supply Range
- Fully Programmable Reference and ÷ N Counters
- ÷ R Range = 3 to 16383
- ÷ N Range = 3 to 16383
- f_V and f_R Outputs
- Lock Detect Signal
- Compatible with the Serial Peripheral Interface (SPI) on CMOS MCUs
- "Linearized" Digital Phase Detector
- Single–Ended (Three–State) or Double–Ended Phase Detector Outputs
- Chip Complexity: 6504 FETs or 1626 Equivalent Gates



P SUFFIX
PLASTIC DIP
CASE 648

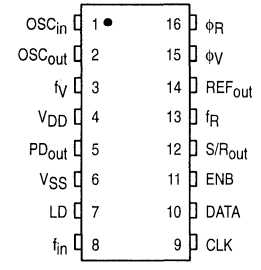


DW SUFFIX
SOG PACKAGE
CASE 751G

ORDERING INFORMATION

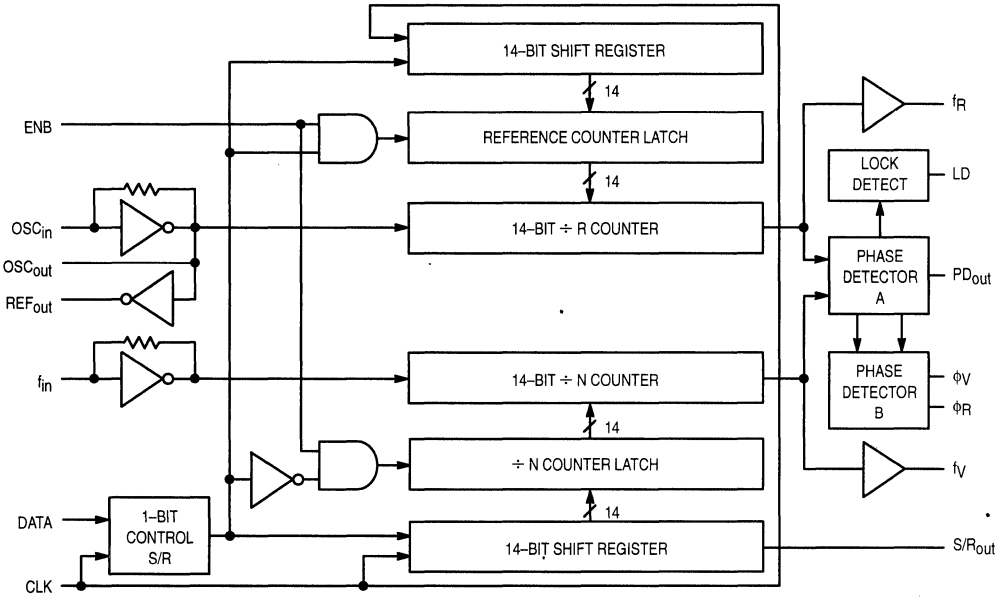
MC145157P2	Plastic DIP
MC145157DW2	SOG Package

PIN ASSIGNMENT



REV 1
8/95

MC145157–2 BLOCK DIAGRAM



PIN DESCRIPTIONS

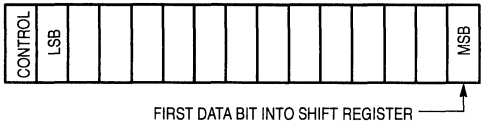
INPUT PINS

f_{in}
Frequency Input (Pin 8)

Input frequency from VCO output. A rising edge signal on this input decrements the ÷ N counter. This input has an inverter biased in the linear region to allow use with ac coupled signals as low as 500 mV p–p. For larger amplitude signals (standard CMOS logic levels), dc coupling may be used.

CLK, DATA
Shift Clock, Serial Data Inputs (Pins 9, 10)

Each low–to–high transition of the clock shifts one bit of data into the on–chip shift registers. The last data bit entered determines which counter storage latch is activated; a logic 1 selects the reference counter latch and a logic 0 selects the ÷ N counter latch. The entry format is as follows:



ENB
Latch Enable Input (Pin 11)

A logic high on this pin latches the data from the shift register into the reference divider or ÷ N latches depending on the control bit. The reference divider latches are activated if the control bit is at a logic high and the ÷ N latches are activated if the control bit is at a logic low. A logic low on this pin allows the user to change the data in the shift registers without affecting the counters. ENB is normally low and is pulsed high to transfer data to the latches.

OSC_{in}, OSC_{out}
Reference Oscillator Input/Output (Pins 1, 2)

These pins form an on–chip reference oscillator when connected to terminals of an external parallel resonant crystal. Frequency setting capacitors of appropriate value must be connected from OSC_{in} to ground and OSC_{out} to ground. OSC_{in} may also serve as the input for an externally–generated reference signal. This signal is typically ac coupled to OSC_{in}, but for larger amplitude signals (standard CMOS logic levels) dc coupling may also be used. In the external reference mode, no connection is required to OSC_{out}.

OUTPUT PINS

PD_{out}
Single–Ended Phase Detector A Output (Pin 5)

This single–ended (three–state) phase detector output produces a loop–error signal that is used with a loop filter to control a VCO.

Frequency $f_V > f_R$ or f_V Leading: Negative Pulses
Frequency $f_V < f_R$ or f_V Lagging: Positive Pulses
Frequency $f_V = f_R$ and Phase Coincidence: High–Impedance State

ϕR, ϕV
Double–Ended Phase Detector B Outputs (Pins 16, 15)

These outputs can be combined externally for a loop–error signal. A single–ended output is also available for this purpose (see **PD_{out}**).

If frequency f_V is greater than f_R or if the phase of f_V is leading, then error information is provided by ϕ_V pulsing low. ϕ_R remains essentially high.

If the frequency f_V is less than f_R or if the phase of f_V is lagging, then error information is provided by ϕ_R pulsing low. ϕ_V remains essentially high.

If the frequency of $f_V = f_R$ and both are in phase, then both ϕ_V and ϕ_R remain high except for a small minimum time period when both pulse low in phase.

f_R, f_V
R Counter Output, N Counter Output (Pins 13, 3)

Buffered, divided reference and f_{in} frequency outputs. The f_R and f_V outputs are connected internally to the ÷ R and ÷ N counter outputs respectively, allowing the counters to be used independently, as well as monitoring the phase detector inputs.

LD
Lock Detector Output (Pin 7)

This output is essentially at a high level when the loop is locked (f_R, f_V of same phase and frequency), and pulses low when loop is out of lock.

REF_{out}
Buffered Reference Oscillator Output (Pin 14)

This output can be used as a second local oscillator, reference oscillator to another frequency synthesizer, or as the system clock to a microprocessor controller.

S/R_{out}
Shift Register Output (Pin 12)

This output can be connected to an external shift register to provide band switching, control information, and counter programming code checking.

POWER SUPPLY

V_{DD}
Positive Power Supply (Pin 4)

The positive power supply potential. This pin may range from +3 to +9 V with respect to V_{SS}.

V_{SS}
Negative Power Supply (Pin 6)

The most negative supply potential. This pin is usually ground.

MC145157–2 Data Sheet Continued on Page 2–650

MC145158-2

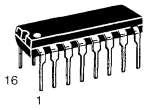
Serial-Input PLL Frequency Synthesizer

Interfaces with Dual–Modulus Prescalers

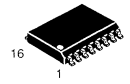
The MC145158–2 has a fully programmable 14–bit reference counter, as well as fully programmable ÷ N and ÷ A counters. The counters are programmed serially through a common data input and latched into the appropriate counter latch, according to the last data bit (control bit) entered.

The MC145158–2 is an improved–performance drop–in replacement for the MC145158–1. Power consumption has decreased and ESD and latch–up performance have improved.

- Operating Temperature Range: – 40 to 85°C
- Low Power Consumption Through Use of CMOS Technology
- 3.0 to 9.0 V Supply Range
- Fully Programmable Reference and ÷ N Counters
- ÷ R Range = 3 to 16383
- ÷ N Range = 3 to 1023
- Dual Modulus Capability; ÷ A Range = 0 to 127
- f_V and f_R Outputs
- Lock Detect Signal
- Compatible with the Serial Peripheral Interface (SPI) on CMOS MCUs
- "Linearized" Digital Phase Detector
- Single–Ended (Three–State) or Double–Ended Phase Detector Outputs
- Chip Complexity: 6504 FETs or 1626 Equivalent Gates



P SUFFIX
PLASTIC DIP
CASE 648

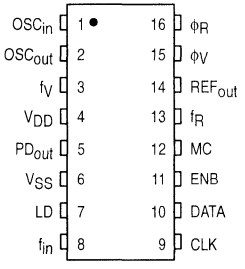


DW SUFFIX
SOG PACKAGE
CASE 751G

ORDERING INFORMATION

MC145158P2	Plastic DIP
MC145158DW2	SOG Package

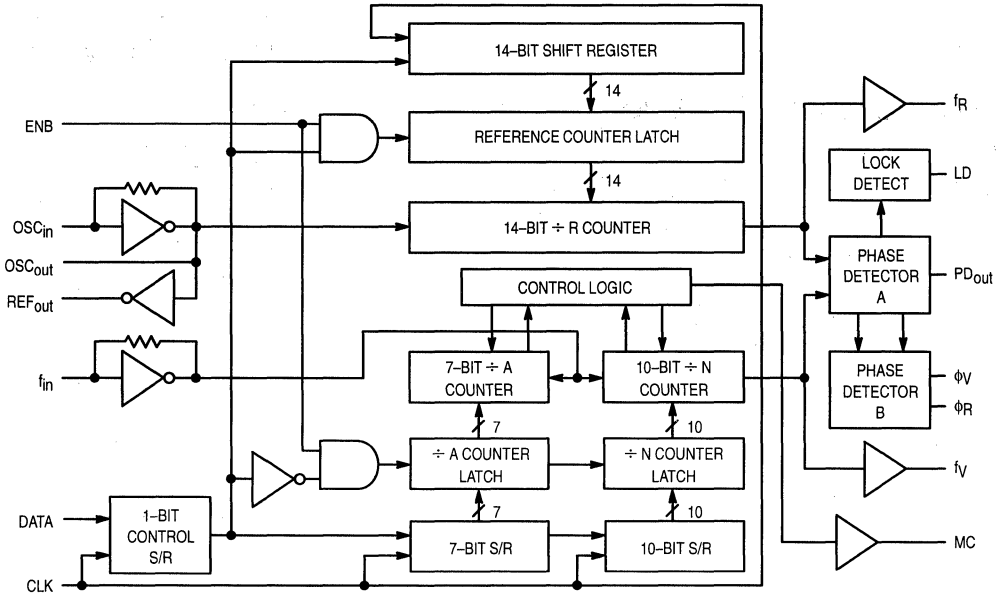
PIN ASSIGNMENT



2

REV 1
8/95

MC145158–2 BLOCK DIAGRAM



PIN DESCRIPTIONS

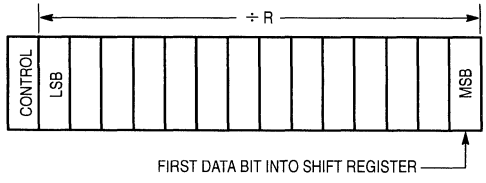
INPUT PINS

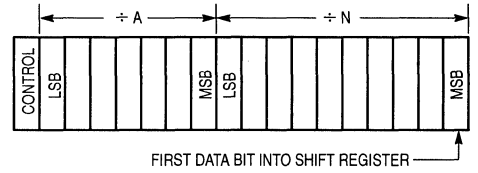
f_{in}
Frequency Input (Pin 8)

Input frequency from VCO output. A rising edge signal on this input decrements the ÷ A and ÷ N counters. This input has an inverter biased in the linear region to allow use with ac coupled signals as low as 500 mV p–p. For larger amplitude signals (standard CMOS logic levels), dc coupling may be used.

CLK, DATA
Shift Clock, Serial Data Inputs (Pins 9, 10)

Each low–to–high transition of the CLK shifts one bit of data into the on–chip shift registers. The last data bit entered determines which counter storage latch is activated; a logic 1 selects the reference counter latch and a logic 0 selects the ÷ A, ÷ N counter latch. The data entry format is as follows:





ENB
Latch Enable Input (Pin 11)

A logic high on this pin latches the data from the shift register into the reference divider or ÷ N, ÷ A latches depending on the control bit. The reference divider latches are activated if the control bit is at a logic high and the ÷ N, ÷ A latches are activated if the control bit is at a logic low. A logic low on this pin allows the user to change the data in the shift registers without affecting the counters. ENB is normally low and is pulsed high to transfer data to the latches.

OSC_{in}, OSC_{out}
Reference Oscillator Input/Output (Pins 1, 2)

These pins form an on–chip reference oscillator when connected to terminals of an external parallel resonant crystal. Frequency setting capacitors of appropriate value must be connected from OSC_{in} to ground and OSC_{out} to ground. OSC_{in} may also serve as the input for an externally–generated reference signal. This signal is typically ac coupled to OSC_{in}, but for larger amplitude signals (standard CMOS logic levels) dc coupling may also be used. In the external reference mode, no connection is required to OSC_{out}.

OUTPUT PINS

PD_{out}
Phase Detector A Output (Pin 5)

This single–ended (three–state) phase detector output produces a loop–error signal that is used with a loop filter to control a VCO.

Frequency $f_V > f_R$ or f_V Leading: Negative Pulses
Frequency $f_V < f_R$ or f_V Lagging: Positive Pulses
Frequency $f_V = f_R$ and Phase Coincidence: High–Impedance State

ϕR, ϕV
Phase Detector B Outputs (Pins 16, 15)

Double–ended phase detector outputs. These outputs can be combined externally for a loop–error signal. A single–ended output is also available for this purpose (see **PD_{out}**).

If frequency f_V is greater than f_R or if the phase of f_V is leading, then error information is provided by ϕV pulsing low. ϕR remains essentially high.

If the frequency f_V is less than f_R or if the phase of f_V is lagging, then error information is provided by ϕR pulsing low. ϕV remains essentially high.

If the frequency of $f_V = f_R$ and both are in phase, then both ϕV and ϕR remain high except for a small minimum time period when both pulse low in phase.

MC
Dual–Modulus Prescale Control Output (Pin 12)

This output generates a signal by the on–chip control logic circuitry for controlling an external dual–modulus prescaler. The MC level is low at the beginning of a count cycle and remains low until the ÷ A counter has counted down from its programmed value. At this time, MC goes high and remains high until the ÷ N counter has counted the rest of the way down from its programmed value (N – A additional counts since both ÷ N and ÷ A are counting down during the first portion of the cycle). MC is then set back low, the counters preset to their respective programmed values, and the above sequence repeated. This provides for a total programmable divide value (N_T) = N • P + A where P and P + 1 represent the dual–modulus prescaler divide values respectively for high and low modulus control levels, N the number programmed into the ÷ N counter, and A the number programmed into the ÷ A counter. Note that when a prescaler is needed, the dual–modulus version offers a distinct advantage. The dual–modulus prescaler allows a higher reference frequency at the phase detector input, increasing system performance capability, and simplifying the loop filter design.

f_R, f_V
R Counter Output, N Counter Output (Pins 13, 3)

Buffered, divided reference and f_{in} frequency outputs. The f_R and f_V outputs are connected internally to the ÷ R and ÷ N counter outputs respectively, allowing the counters to be used independently, as well as monitoring the phase detector inputs.

LD
Lock Detector Output (Pin 7)

This output is essentially at a high level when the loop is locked (f_R, f_V of same phase and frequency), and pulses low when loop is out of lock.

REF_{out}
Buffered Reference Oscillator Output (Pin 14)

This output can be used as a second local oscillator, reference oscillator to another frequency synthesizer, or as the system clock to a microprocessor controller.

POWER SUPPLY

V_{DD}
Positive Power Supply (Pin 4)

The positive power supply potential. This pin may range from + 3 to + 9 V with respect to V_{SS}.

V_{SS}
Negative Power Supply (Pin 6)

The most negative supply potential. This pin is usually ground.

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	– 0.5 to + 10.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient) except SW1, SW2	– 0.5 to V_{DD} + 0.5	V
V_{out}	Output Voltage (DC or Transient), SW1, SW2 ($R_{pull-up}$ = 4.7 kΩ)	– 0.5 to + 15	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	± 10	mA
I_{DD}, I_{SS}	Supply Current, V_{DD} or V_{SS} Pins	± 30	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 seconds	260	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Descriptions section.

†Power Dissipation Temperature Derating:
Plastic DIP: – 12 mW/°C from 65 to 85°C
SOG Package: – 7 mW/°C from 65 to 85°C

These devices contain protection circuitry to protect against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to these high–impedance circuits. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$ except for SW1 and SW2.

SW1 and SW2 can be tied through external resistors to voltages as high as 15 V, independent of the supply voltage.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}), except for inputs with pull–up devices. Unused outputs must be left open.

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Symbol	Parameter	Test Condition	V_{DD} V	– 40°C Min	– 40°C Max	25°C Min	25°C Max	85°C Min	85°C Max	Unit
V_{DD}	Power Supply Voltage Range		—	3	9	3	9	3	9	V
I_{ss}	Dynamic Supply Current	$f_{in} = OSC_{in}$ = 10 MHz, 1 V p–p ac coupled sine wave R = 128, A = 32, N = 128	3 5 9	— — —	3.5 10 30	— — —	3 7.5 24	— — —	3 7.5 24	mA
I_{SS}	Quiescent Supply Current (not including pull–up current component)	$V_{in} = V_{DD}$ or V_{SS} I_{out} = 0 µA	3 5 9	— — —	800 1200 1600	— — —	800 1200 1600	— — —	1600 2400 3200	µA
V_{in}	Input Voltage — f_{in}, OSC_{in}	Input ac coupled sine wave	—	500	—	500	—	500	—	mV p–p
V_{IL}	Low–Level Input Voltage — f_{in}, OSC_{in}	$V_{out} \ge 2.1$ V Input dc $V_{out} \ge 3.5$ V coupled $V_{out} \ge 6.3$ V square wave	3 5 9	— — —	0 0 0	— — —	0 0 0	— — —	0 0 0	V
V_{IH}	High–Level Input Voltage — f_{in}, OSC_{in}	$V_{out} \le 0.9$ V Input dc $V_{out} \le 1.5$ V coupled $V_{out} \le 2.7$ V square wave	3 5 9	3.0 5.0 9.0	— — —	3.0 5.0 9.0	— — —	3.0 5.0 9.0	— — —	V
V_{IL}	Low–Level Input Voltage — except f_{in}, OSC_{in}		3 5 9	— — —	0.9 1.5 2.7	— — —	0.9 1.5 2.7	— — —	0.9 1.5 2.7	V
V_{IH}	High–Level Input Voltage — except f_{in}, OSC_{in}		3 5 9	2.1 3.5 6.3	— — —	2.1 3.5 6.3	— — —	2.1 3.5 6.3	— — —	V
I_{in}	Input Current (f_{in}, OSC_{in})	$V_{in} = V_{DD}$ or V_{SS}	9	± 2	± 50	± 2	± 25	± 2	± 22	µA
I_{IL}	Input Leakage Current (Data, CLK, ENB — without pull–ups)	$V_{in} = V_{SS}$	9	—	– 0.3	—	– 0.1	—	– 1.0	µA
I_{IH}	Input Leakage Current (all inputs except f_{in}, OSC_{in})	$V_{in} = V_{DD}$	9	—	0.3	—	0.1	—	1.0	µA

(continued)

DC ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Condition	V_{DD} V	– 40°C		25°C		85°C		Unit
				Min	Max	Min	Max	Min	Max	
I_{IL}	Pull–up Current (all inputs with pull–ups)	$V_{in} = V_{SS}$	9	– 20	– 400	– 20	– 200	– 20	– 170	µA
C_{in}	Input Capacitance		—	—	10	—	10	—	10	pF
V_{OL}	Low–Level Output Voltage — OSC_{out}	$I_{out} \approx 0$ µA $V_{in} = V_{DD}$	3 5 9	— — —	0.9 1.5 2.7	— — —	0.9 1.5 2.7	— — —	0.9 1.5 2.7	V
V_{OH}	High–Level Output Voltage — OSC_{out}	$I_{out} \approx 0$ µA $V_{in} = V_{SS}$	3 5 9	2.1 3.5 6.3	— — —	2.1 3.5 6.3	— — —	2.1 3.5 6.3	— — —	V
V_{OL}	Low–Level Output Voltage — Other Outputs	$I_{out} \approx 0$ µA	3 5 9	— — —	0.05 0.05 0.05	— — —	0.05 0.05 0.05	— — —	0.05 0.05 0.05	V
V_{OH}	High–Level Output Voltage — Other Outputs	$I_{out} \approx 0$ µA	3 5 9	2.95 4.95 8.95	— — —	2.95 4.95 8.95	— — —	2.95 4.95 8.95	— — —	V
$V_{(BR)DSS}$	Drain–to–Source Breakdown Voltage — SW1, SW2	$R_{pull–up} = 4.7$ kΩ	—	15	—	15	—	15	—	V
I_{OL}	Low–Level Sinking Current — MC	$V_{out} = 0.3$ V $V_{out} = 0.4$ V $V_{out} = 0.5$ V	3 5 9	1.30 1.90 3.80	— — —	1.10 1.70 3.30	— — —	0.66 1.08 2.10	— — —	mA
I_{OH}	High–Level Sourcing Current — MC	$V_{out} = 2.7$ V $V_{out} = 4.6$ V $V_{out} = 8.5$ V	3 5 9	– 0.60 – 0.90 – 1.50	— — —	– 0.50 – 0.75 – 1.25	— — —	– 0.30 – 0.50 – 0.80	— — —	mA
I_{OL}	Low–Level Sinking Current — LD	$V_{out} = 0.3$ V $V_{out} = 0.4$ V $V_{out} = 0.5$ V	3 5 9	0.25 0.64 1.30	— — —	0.20 0.51 1.00	— — —	0.15 0.36 0.70	— — —	mA
I_{OH}	High–Level Sourcing Current — LD	$V_{out} = 2.7$ V $V_{out} = 4.6$ V $V_{out} = 8.5$ V	3 5 9	– 0.25 – 0.64 – 1.30	— — —	– 0.20 – 0.51 – 1.00	— — —	– 0.15 – 0.36 – 0.70	— — —	mA
I_{OL}	Low–Level Sinking Current — SW1, SW2	$V_{out} = 0.3$ V $V_{out} = 0.4$ V $V_{out} = 0.5$ V	3 5 9	0.80 1.50 3.50	— — —	0.48 0.90 2.10	— — —	0.24 0.45 1.05	— — —	mA
I_{OL}	Low–Level Sinking Current — Other Outputs	$V_{out} = 0.3$ V $V_{out} = 0.4$ V $V_{out} = 0.5$ V	3 5 9	0.44 0.64 1.30	— — —	0.35 0.51 1.00	— — —	0.22 0.36 0.70	— — —	mA
I_{OH}	High–Level Sourcing Current — Other Outputs	$V_{out} = 2.7$ V $V_{out} = 4.6$ V $V_{out} = 8.5$ V	3 5 9	– 0.44 – 0.64 – 1.30	— — —	– 0.35 – 0.51 – 1.00	— — —	– 0.22 – 0.36 – 0.70	— — —	mA
I_{OZ}	Output Leakage Current — PD_{out}	$V_{out} = V_{DD}$ or V_{SS} Output in Off State	9	—	± 0.3	—	± 0.1	—	± 1.0	µA
I_{OZ}	Output Leakage Current — SW1, SW2	$V_{out} = V_{DD}$ or V_{SS} Output in Off State	9	—	± 0.3	—	± 0.1	—	± 3.0	µA
C_{out}	Output Capacitance — PD_{out}	PD_{out} — Three–State	—	—	10	—	10	—	10	pF

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 10 ns)

Symbol	Parameter	V_{DD} V	Guaranteed Limit 25°C	Guaranteed Limit – 40 to 85°C	Unit
t_{PLH}, t_{PHL}	Maximum Propagation Delay, f_{in} to MC (Figures 1 and 4)	3 5 9	110 60 35	120 70 40	ns
t_{PHL}	Maximum Propagation Delay, ENB to SW1, SW2 (Figures 1 and 5)	3 5 9	160 80 50	180 95 60	ns
t_W	Output Pulse Width, ϕ_R, ϕ_V, and LD with f_R in Phase with f_V (Figures 2 and 4)	3 5 9	25 to 200 20 to 100 10 to 70	25 to 260 20 to 125 10 to 80	ns
t_{TLH}	Maximum Output Transition Time, MC (Figures 3 and 4)	3 5 9	115 60 40	115 75 60	ns
t_{THL}	Maximum Output Transition Time, MC (Figures 3 and 4)	3 5 9	60 34 30	70 45 38	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, LD (Figures 3 and 4)	3 5 9	180 90 70	200 120 90	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Other Outputs (Figures 3 and 4)	3 5 9	160 80 60	175 100 65	ns

SWITCHING WAVEFORMS

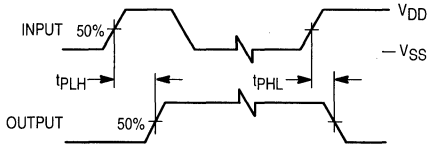
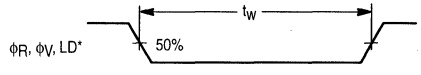


Figure 1.



* f_R in phase with f_V.

Figure 2.

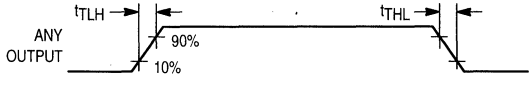
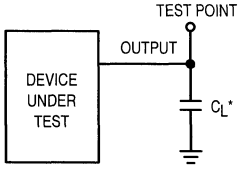
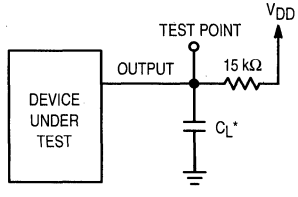


Figure 3.



* Includes all probe and fixture capacitance.

Figure 4. Test Circuit



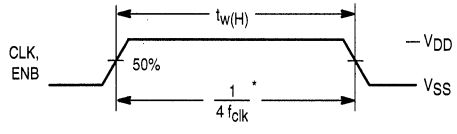
* Includes all probe and fixture capacitance.

Figure 5. Test Circuit

TIMING REQUIREMENTS (Input $t_r = t_f = 10$ ns unless otherwise indicated)

Symbol	Parameter	V_{DD} V	Guaranteed Limit 25°C	Guaranteed Limit – 40 to 85°C	Unit
f_{clk}	Serial Data Clock Frequency, Assuming 25% Duty Cycle NOTE: Refer to CLK $t_{w(H)}$ below (Figure 6)	3 5 9	dc to 5.0 dc to 7.1 dc to 10	dc to 3.5 dc to 7.1 dc to 10	MHz
t_{su}	Minimum Setup Time, Data to CLK (Figure 7)	3 5 9	30 20 18	30 20 18	ns
t_h	Minimum Hold Time, CLK to Data (Figure 7)	3 5 9	40 20 15	40 20 15	ns
t_{su}	Minimum Setup Time, CLK to ENB (Figure 7)	3 5 9	70 32 25	70 32 25	ns
t_{rec}	Minimum Recovery Time, ENB to CLK (Figure 7)	3 5 9	5 10 20	5 10 20	ns
$t_{w(H)}$	Minimum Pulse Width, CLK and ENB (Figure 6)	3 5 9	50 35 25	70 35 25	ns
t_r, t_f	Maximum Input Rise and Fall Times — Any Input (Figure 8)	3 5 9	5 4 2	5 4 2	µs

SWITCHING WAVEFORMS



*Assumes 25% Duty Cycle.

Figure 6.

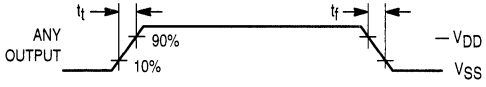


Figure 8.

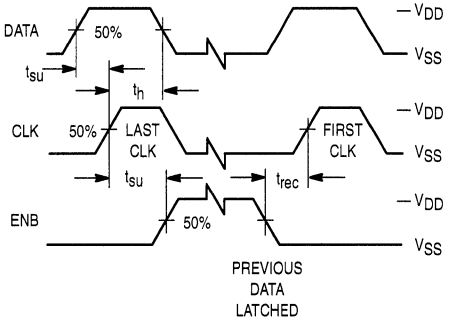
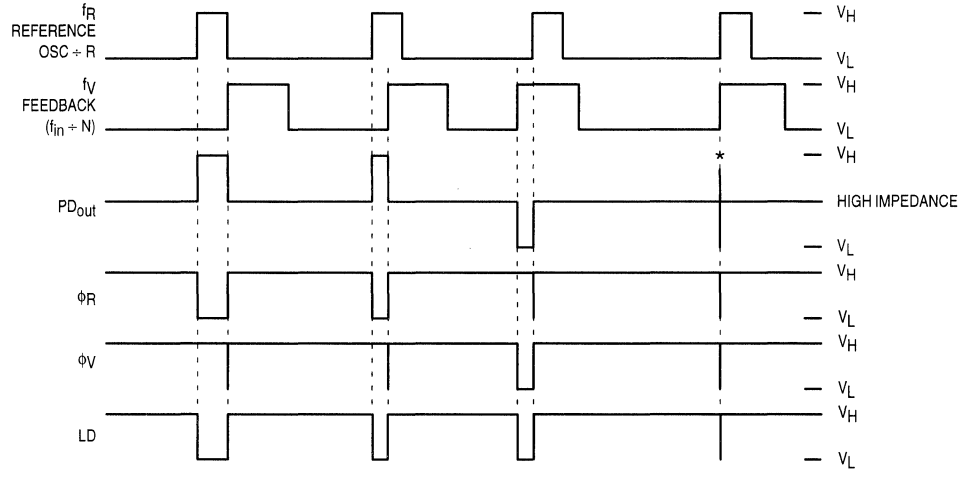


Figure 7.

FREQUENCY CHARACTERISTICS (Voltages References to V_{SS}, C_L = 50 pF, Input $t_r = t_f$ =10 ns unless otherwise indicated)

Symbol	Parameter	Test Condition	V_{DD} V	– 40°C		25°C		85°C		Unit
				Min	Max	Min	Max	Min	Max	
f_i	Input Frequency (f_{in}, OSC_{in})	R ≥ 8, A ≥ 0, N ≥ 8 V_{in} = 500 mV p–p ac coupled sine wave	3 5 9	— — —	6 15 15	— — —	6 15 15	— — —	6 15 15	MHz
		R ≥ 8, A ≥ 0, N ≥ 8 V_{in} = 1 V p–p ac coupled sine wave	3 5 9	— — —	12 22 25	— — —	12 20 22	— — —	7 20 22	MHz
		R ≥ 8, A ≥ 0, N ≥ 8 V_{in} = V_{DD} to V_{SS} dc coupled square wave	3 5 9	— — —	13 25 25	— — —	12 22 25	— — —	8 22 25	MHz

NOTE: Usually, the PLL's propagation delay from f_{in} to MC plus the setup time of the prescaler determines the upper frequency limit of the system. The upper frequency limit is found with the following formula: $f = P/(t_P + t_{set})$ where f is the upper frequency in Hz, P is the lower of the dual modulus prescaler ratios, t_P is the f_{in} to MC propagation delay in seconds, and t_{set} is the prescaler setup time in seconds.
For example, with a 5 V supply, the f_{in} to MC delay is 70 ns. If the MC12028A prescaler is used, the setup time is 16 ns. Thus, if the 64/65 ratio is utilized, the upper frequency limit is $f = P/(t_P + t_{set}) = 64/(70 + 16) = 744$ MHz.



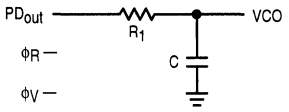
V_H = High Voltage Level.
V_L = Low Voltage Level.
* At this point, when both f_R and f_V are in phase, the output is forced to near mid–supply.
NOTE: The PD_{out} generates error pulses during out–of–lock conditions. When locked in phase and frequency the output is high and the voltage at this pin is determined by the low–pass filter capacitor.

Figure 9. Phase Detector/Lock Detector Output Waveforms

DESIGN CONSIDERATIONS

PHASE–LOCKED LOOP — LOW–PASS FILTER DESIGN

A)

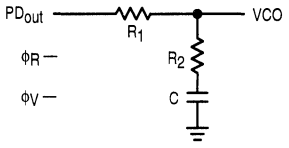


$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NR_1C}}$$

$$\zeta = \frac{N\omega_n}{2K_\phi K_{VCO}}$$

$$F(s) = \frac{1}{R_1sC + 1}$$

B)

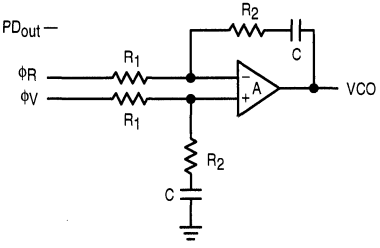


$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NC(R_1 + R_2)}}$$

$$\zeta = 0.5\,\omega_n \left(R_2C + \frac{N}{K_\phi K_{VCO}}\right)$$

$$F(s) = \frac{R_2sC + 1}{(R_1 + R_2)sC + 1}$$

C)



$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NCR_1}}$$

$$\zeta = \frac{\omega_n R_2 C}{2}$$

ASSUMING GAIN A IS VERY LARGE, THEN:

$$F(s) = \frac{R_2sC + 1}{R_1sC}$$

NOTE: Sometimes R_1 is split into two series resistors, each $R_1 \div 2$. A capacitor C_C is then placed from the midpoint to ground to further filter ϕ_V and ϕ_R. The value of C_C should be such that the corner frequency of this network does not significantly affect ω_n. The ϕ_R and ϕ_V outputs swing rail–to–rail. Therefore, the user should be careful not to exceed the common mode input range of the op amp used in the combiner/loop filter.

DEFINITIONS:

N = Total Division Ratio in feedback loop

K_ϕ (Phase Detector Gain) = $V_{DD}/4\pi$ for PD_{out}

K_ϕ (Phase Detector Gain) = $V_{DD}/2\pi$ for ϕ_V and ϕ_R

K_{VCO} (VCO Gain) = $\dfrac{2\pi\Delta f_{VCO}}{\Delta V_{VCO}}$

for a typical design w_n (Natural Frequency) $\approx \dfrac{2\pi fr}{10}$ (at phase detector input).

Damping Factor: $\zeta \cong 1$

RECOMMENDED READING:

Gardner, Floyd M., *Phaselock Techniques (second edition)*. New York, Wiley–Interscience, 1979.

Manassewitsch, Vadim, *Frequency Synthesizers: Theory and Design (second edition)*. New York, Wiley–Interscience, 1980.

Blanchard, Alain, *Phase–Locked Loops: Application to Coherent Receiver Design*. New York, Wiley–Interscience, 1976.

Egan, William F., *Frequency Synthesis by Phase Lock*. New York, Wiley–Interscience, 1981.

Rohde, Ulrich L., *Digital PLL Frequency Synthesizers Theory and Design*. Englewood Cliffs, NJ, Prentice–Hall, 1983.

Berlin, Howard M., *Design of Phase–Locked Loop Circuits, with Experiments*. Indianapolis, Howard W. Sams and Co., 1978.

Kinley, Harold, *The PLL Synthesizer Cookbook*. Blue Ridge Summit, PA, Tab Books, 1980.

AN535, Phase–Locked Loop Design Fundamentals, Motorola Semiconductor Products, Inc., 1970.

AR254, Phase–Locked Loop Design Articles, Motorola Semiconductor Products, Inc., Reprinted with permission from *Electronic Design*, 1987.

CRYSTAL OSCILLATOR CONSIDERATIONS

The following options may be considered to provide a reference frequency to Motorola's CMOS frequency synthesizers.

Use of a Hybrid Crystal Oscillator

Commercially available temperature–compensated crystal oscillators (TCXOs) or crystal–controlled data clock oscillators provide very stable reference frequencies. An oscillator capable of sinking and sourcing 50 μA at CMOS logic levels may be direct or dc coupled to OSC_{in}. In general, the highest frequency capability is obtained utilizing a direct–coupled square wave having a rail–to–rail (V_{DD} to V_{SS}) voltage swing. If the oscillator does not have CMOS logic levels on the outputs, capacitive or ac coupling to OSC_{in} may be used. OSC_{out}, an unbuffered output, should be left floating.

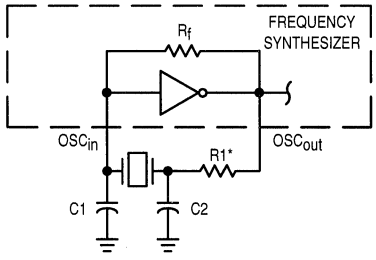
For additional information about TCXOs and data clock oscillators, please consult the latest version of the *eem Electronic Engineers Master Catalog,* the *Gold Book,* or similar publications.

Design an Off–Chip Reference

The user may design an off–chip crystal oscillator using ICs specifically developed for crystal oscillator applications, such as the MC12061 MECL device. The reference signal from the MECL device is ac coupled to OSC_{in}. For large amplitude signals (standard CMOS logic levels), dc coupling is used. OSC_{out}, an unbuffered output, should be left floating. In general, the highest frequency capability is obtained with a direct–coupled square wave having rail–to–rail voltage swing.

Use of the On–Chip Oscillator Circuitry

The on–chip amplifier (a digital inverter) along with an appropriate crystal may be used to provide a reference source frequency. A fundamental mode crystal, parallel resonant at the desired operating frequency, should be connected as shown in Figure 10.



* May be deleted in certain cases. See text.

Figure 10. Pierce Crystal Oscillator Circuit

For V_{DD} = 5.0 V, the crystal should be specified for a loading capacitance, C_L, which does not exceed 32 pF for frequencies to approximately 8.0 MHz, 20 pF for frequencies in the area of 8.0 to 15 MHz, and 10 pF for higher frequencies. These are guidelines that provide a reasonable compromise between IC capacitance, drive capability, swamping variations in stray and IC input/output capacitance, and realistic C_L values. The shunt load capacitance, C_L, presented across the crystal can be estimated to be:

$$C_L = \frac{C_{in}C_{out}}{C_{in} + C_{out}} + C_a + C_o + \frac{C1 \cdot C2}{C1 + C2}$$

where

C_{in} = 5 pF (see Figure 11)
C_{out} = 6 pF (see Figure 11)
C_a = 1 pF (see Figure 11)
C_O = the crystal's holder capacitance (see Figure 12)
C1 and C2 = external capacitors (see Figure 10)

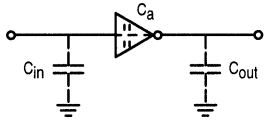
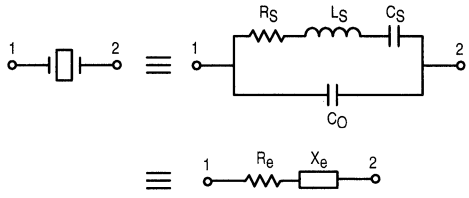


Figure 11. Parasitic Capacitances of the Amplifier



NOTE: Values are supplied by crystal manufacturer (parallel resonant crystal).

Figure 12. Equivalent Crystal Networks

The oscillator can be "trimmed" on–frequency by making a portion or all of C1 variable. The crystal and associated components must be located as close as possible to the OSC_{in} and OSC_{out} pins to minimize distortion, stray capacitance, stray inductance, and startup stabilization time. In some cases, stray capacitance should be added to the value for C_{in} and C_{out}.

Power is dissipated in the effective series resistance of the crystal, R_e, in Figure 12. The drive level specified by the crystal manufacturer is the maximum stress that a crystal can withstand without damage or excessive shift in frequency. R1 in Figure 10 limits the drive level. The use of R1 may not be necessary in some cases (i.e., R1 = 0 Ω).

To verify that the maximum dc supply voltage does not overdrive the crystal, monitor the output frequency as a function of voltage at OSC_{out}. (Care should be taken to minimize loading.) The frequency should increase very slightly as the dc supply voltage is increased. An overdriven crystal will decrease in frequency or become unstable with an increase in supply voltage. The operating supply voltage must be reduced or R1 must be increased in value if the overdriven condition exists. The user should note that the oscillator start–up time is proportional to the value of R1.

Through the process of supplying crystals for use with CMOS inverters, many crystal manufacturers have developed expertise in CMOS oscillator design with crystals. Discussions with such manufacturers can prove very helpful (see Table 1).

Table 1. Partial List of Crystal Manufacturers

Name	Address	Phone
United States Crystal Corp.	3605 McCart Ave., Ft. Worth, TX 76110	(817) 921–3013
Crystek Crystal	2351 Crystal Dr., Ft. Myers, FL 33907	(813) 936–2109
Statek Corp.	512 N. Main St., Orange, CA 92668	(714) 639–7810

NOTE: Motorola cannot recommend one supplier over another and in no way suggests that this is a complete listing of crystal manufacturers.

RECOMMENDED READING

Technical Note TN–24, Statek Corp.

Technical Note TN–7, Statek Corp.

E. Hafner, "The Piezoelectric Crystal Unit – Definitions and Method of Measurement", *Proc. IEEE,* Vol. 57, No. 2 Feb., 1969.

D. Kemper, L. Rosine, "Quartz Crystals for Frequency Control", *Electro–Technology,* June, 1969.

P. J. Ottowitz, "A Guide to Crystal Selection", *Electronic Design*, May, 1966.

DUAL–MODULUS PRESCALING

OVERVIEW

The technique of dual–modulus prescaling is well established as a method of achieving high performance frequency synthesizer operation at high frequencies. Basically, the approach allows relatively low–frequency programmable counters to be used as high–frequency programmable counters with speed capability of several hundred MHz. This is possible without the sacrifice in system resolution and performance that results if a fixed (single–modulus) divider is used for the prescaler.

In dual–modulus prescaling, the lower speed counters must be uniquely configured. Special control logic is necessary to select the divide value P or P + 1 in the prescaler for the required amount of time (see modulus control definition). Motorola's dual–modulus frequency synthesizers contain this feature and can be used with a variety of dual–modulus prescalers to allow speed, complexity and cost to be tailored to the system requirements. Prescalers having P, P + 1 divide values in the range of ÷ 3/÷ 4 to ÷ 128/÷ 129 can be controlled by most Motorola frequency synthesizers.

Several dual–modulus prescaler approaches suitable for use with the MC145152–2, MC145156–2, or MC145158–2 are:

MC12009	÷ 5/÷ 6	440 MHz
MC12011	÷ 8/÷ 9	500 MHz
MC12013	÷ 10/÷ 11	500 MHz
MC12015	÷ 32/÷ 33	225 MHz
MC12016	÷ 40/÷ 41	225 MHz
MC12017	÷ 64/÷ 65	225 MHz
MC12018	÷ 128/÷ 129	520 MHz
MC12022A	÷ 64/65 or ÷ 128/129	1.1 GHz
MC12032A	÷ 64/65 or ÷ 128/129	2.0 GHz

DESIGN GUIDELINES

The system total divide value, N_{total} (N_T) will be dictated by the application:

$$N_T = \frac{\text{frequency into the prescaler}}{\text{frequency into the phase detector}} = N \bullet P + A$$

N is the number programmed into the ÷ N counter, A is the number programmed into the ÷ A counter, P and P + 1 are the two selectable divide ratios available in the dual–modulus prescalers. To have a range of N_T values in sequence, the ÷ A counter is programmed from zero through P – 1 for a particular value N in the ÷ N counter. N is then incremented to N + 1 and the ÷ A is sequenced from 0 through P – 1 again.

There are minimum and maximum values that can be achieved for N_T. These values are a function of P and the size of the ÷ N and ÷ A counters.

The constraint N ≥ A always applies. If $A_{max} = P - 1$, then $N_{min} \geq P - 1$. Then $N_{Tmin} = (P - 1)\,P + A$ or $(P - 1)\,P$ since A is free to assume the value of 0.

$$N_{Tmax} = N_{max} \bullet P + A_{max}$$

To maximize system frequency capability, the dual–modulus prescaler output must go from low to high after each group of P or P + 1 input cycles. The prescaler should divide by P when its modulus control line is high and by P + 1 when its MC is low.

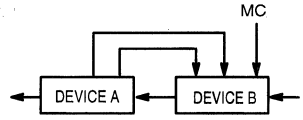
For the maximum frequency into the prescaler (f_{VCOmax}), the value used for P must be large enough such that:

1. f_{VCOmax} divided by P may not exceed the frequency capability of f_{in} (input to the ÷ N and ÷ A counters).
2. The period of f_{VCO} divided by P must be greater than the sum of the times:
   a. Propagation delay through the dual–modulus prescaler.
   b. Prescaler setup or release time relative to its MC signal.
   c. Propagation time from f_{in} to the MC output for the frequency synthesizer device.

A sometimes useful simplification in the programming code can be achieved by choosing the values for P of 8, 16, 32, or 64. For these cases, the desired value of N_T results when N_T in binary is used as the program code to the ÷ N and ÷ A counters treated in the following manner:

1. Assume the ÷ A counter contains "a" bits where $2^a \geq P$.
2. Always program all higher order ÷ A counter bits above "a" to 0.
3. Assume the ÷ N counter and the ÷ A counter (with all the higher order bits above "a" ignored) combined into a single binary counter of n + a bits in length (n = number of divider stages in the ÷ N counter). The MSB of this "hypothetical" counter is to correspond to the MSB of ÷ N and the LSB is to correspond to the LSB of ÷ A. The system divide value, N_T, now results when the value of N_T in binary is used to program the "new" n + a bit counter.

By using the two devices, several dual–modulus values are achievable (shown in Figure 13).



DEVICE A \ DEVICE B	MC12009	MC12011	MC12013
MC10131	÷ 20/÷ 21	÷ 32/÷ 33	÷ 40/÷ 41
MC10138	÷ 50/÷ 51	÷ 80/÷ 81	÷ 100/÷ 101
MC10154	÷ 40/÷ 41 OR ÷ 80/÷ 81	÷ 64/÷ 65 OR ÷ 128/÷ 129	÷ 80/÷ 81

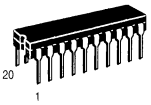
NOTE: MC12009, MC12011, and MC12013 are pin equivalent.
MC12015, MC12016, and MC12017 are pin equivalent.

Figure 13. Dual–Modulus Values

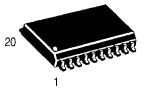
MC145159-1

Serial-Input PLL Frequency Synthesizer with Analog Phase Detector

Interfaces with Dual–Modulus Prescalers



P SUFFIX
PLASTIC DIP
CASE 738



DW SUFFIX
SOG PACKAGE
CASE 751D

VF SUFFIX
SSOP
CASE TBD

ORDERING INFORMATION

MC145159P1	Plastic DIP
MC145159DW1	SOG Package
MC145159VF1	SSOP

2

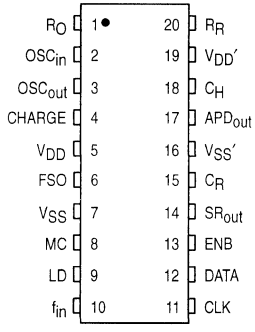
The MC145159–1 has a programmable 14–bit reference counter, as well as fully programmable divide–by–N/divide–by–A counters. The counters are programmed serially through a common data input and latched into the appropriate counter latch, according to the last data bit (control bit) entered.

When combined with a loop filter and VCO, this device can provide all the remaining functions for a PLL frequency synthesizer operating up to the device's frequency limit. For higher VCO frequency operations, a down mixer or a dual–modulus prescaler can be used between the VCO and the PLL.

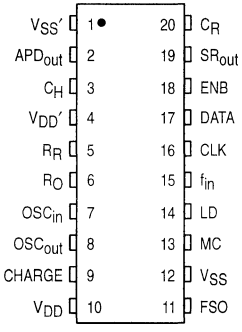
- Operating Temperature Range: – 40 to 85°C
- Low Power Consumption Through Use of CMOS Technology
- 3.0 to 9.0 V Supply Range
- On– or Off–Chip Reference Oscillator Operation
- Compatible with the Serial Peripheral Interface (SPI) on CMOS MCUs
- ÷ R Range = 3 to 16383
- ÷ N Range = 16 to 1023, ÷ A Range = 0 to 127
- High–Gain Analog Phase Detector
- See Application Note AN969

PIN ASSIGNMENTS

PLASTIC DIP AND SOG PACKAGE

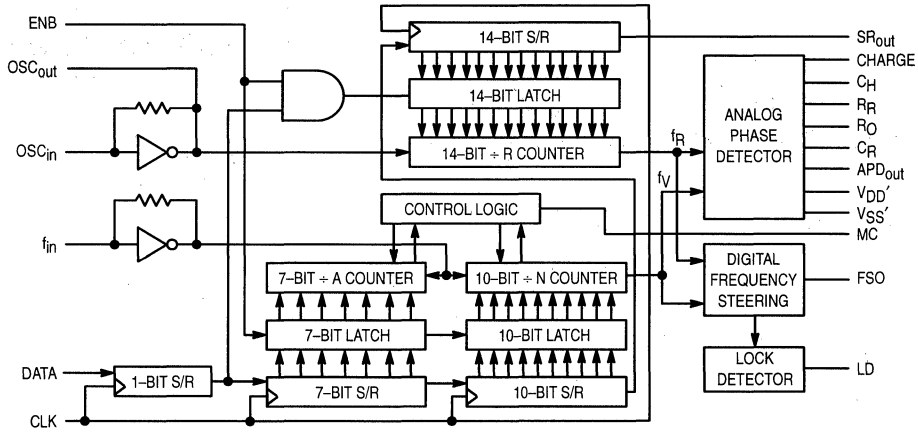


SSOP



REV 1
8/95

BLOCK DIAGRAM



* FSO is not and cannot be used as a digital phase detector output.

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	– 0.5 to + 10	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	– 0.5 to V_{DD} + 0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	± 10	mA
I_{DD}, I_{SS}	Supply Current, V_{DD} or V_{SS} Pins	± 30	mA
P_D	Power Dissipation, per Package	500	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature (8–Second Soldering)	260	°C

* Maximum Ratings are those values beyond which damage to the device may occur.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS} except I_{CR} and I_{APD} which are referenced to V_{SS}′)

Characteristic	Symbol	V_{DD}	−40°C Min	−40°C Max	25°C Min	25°C Max	85°C Min	85°C Max	Unit
Power Supply Voltage Range	V_{DD}	—	3	9	3	9	3	9	V
Output Voltage 0 Level V_{in} = 0 V or V_{DD} I_{out} = 0 μA (Except OSC_{out} and APD_{out})	V_{OL}	3 5 9	— — —	0.05 0.05 0.05	— — —	0.05 0.05 0.05	— — —	0.05 0.05 0.05	V
1 Level	V_{OH}	3 5 9	2.95 4.95 8.95	— — —	2.95 4.95 8.95	— — —	2.95 4.95 8.95	— — —	
Output Voltage 0 Level OSC_{out} V_{in} = 0 V or V_{DD}	V_{OL}	3 5 9	— — —	0.9 1.5 2.7	— — —	0.9 1.5 2.7	— — —	0.9 1.5 2.7	V
1 Level	V_{OH}	3 5 9	2.1 3.5 6.3	— — —	2.1 3.5 6.3	— — —	2.1 3.5 6.3	— — —	
ΔVoltage, $V_{CH} - V_{APDout}$, $I_{APDout} \approx 0$ μA	ΔV	—	—	—	—	1.05	—	—	V
Input Voltage 0 Level V_{out} = 0.5 V or V_{DD} − 0.5 V (All Outputs Except OSC_{out})	V_{IL}	3 5 9	— — —	0.9 1.5 2.7	— — —	0.9 1.5 2.7	— — —	0.9 1.5 2.7	V
1 Level	V_{IH}	3 5 9	2.1 3.5 6.3	— — —	2.1 3.5 6.3	— — —	2.1 3.5 6.3	— — —	
Input Voltage* — OSC_{in} V_O = 2.1 V or 0.9 V V_O = 3.5 V or 1.5 V V_O = 6.3 V or 2.7 V	V_{IL} 0 Level	3 5 9	— — —	0 0 0	— — —	0 0 0	— — —	0 0 0	V
1 Level V_O = 0.9 V or 2.1 V V_O = 1.5 V or 3.5 V V_O = 2.7 V or 6.3 V	V_{IH}	3 5 9	3.0 5.0 9.0	— — —	3.0 5.0 9.0	— — —	3.0 5.0 9.0	— — —	V
Output Current — MC V_{out} = 2.7 V Source V_{out} = 4.6 V V_{out} = 8.5 V	I_{OH}	3 5 9	− 0.60 − 0.90 − 1.50	— — —	− 0.50 − 0.75 − 1.25	— — —	− 0.30 − 0.50 − 0.80	— — —	mA
V_{out} = 0.3 V Sink V_{out} = 0.4 V V_{out} = 0.5 V	I_{OL}	3 5 9	1.30 1.90 3.80	— — —	1.10 1.70 3.30	— — —	0.66 1.08 2.10	— — —	
Output Current, C_R, V_{CR} = 4.5 V, R_R = 240 k	I_{CR}	9	—	—	− 90	− 110	—	—	μA
Output Current, APD_{out} R_O = 240 k, V_{CH} = 0 V, V_{APDout} = 4.5 V	I_{APD}	9	—	—	170	350	—	—	μA
Output Current — Other Outputs V_{out} = 2.7 V Source V_{out} = 4.6 V V_{out} = 8.5 V	I_{OH}	3 5 9	− 0.44 − 0.64 − 1.30	— — —	− 0.35 − 0.51 − 1.00	— — —	− 0.22 − 0.36 − 0.70	— — —	mA
V_{out} = 0.3 V Sink V_{out} = 0.4 V V_{out} = 0.5 V	I_{OL}	3 5 9	0.44 0.64 1.30	— — —	0.35 0.51 1.00	— — —	0.22 0.36 0.70	— — —	
Input Current — Data, CLK, ENB	I_{in}	9	—	± 0.3	—	± 0.1	—	± 1.0	μA
Input Current — f_{in}, OSC_{in}	I_{in}	9	± 2	± 50	± 2	± 25	± 2	± 22	μA
Input Capacitance	C_{in}	—	—	10	—	10	—	10	pF
Three−State Output Capacitance — FSO	C_{out}	—	—	10	—	10	—	10	pF
Quiescent Current V_{in} = 0 V or V_{DD} I_{out} = 0 μA	I_{DD}	3 5 9	— — —	800 1200 1600	— — —	800 1200 1600	— — —	1600 2400 3200	μA
Three−State Leakage Current, V_{out} = 0 V or 9 V	I_{OZ}	9	—	± 0.3	—	± 0.1	—	± 3.0	μA

* dc coupled square wave.

SWITCHING CHARACTERISTICS (T_A = 25°C, C_L = 50 pF)

Characteristic	Figure No.	Symbol	V_{DD}	Min	Max	Unit
Output Rise Time — MC	4, 9	t_{TLH}	3 5 9	— — —	115 60 40	ns
Output Fall Time — MC	4, 9	t_{THL}	3 5 9	— — —	60 34 30	ns
Output Rise and Fall Time — LD and SR_{out}	4, 9	t_{TLH}, t_{THL}	3 5 9	— — —	140 80 60	ns
Propagation Delay Time — f_{in} to MC	5, 9	t_{PLH}, t_{PHL}	3 5 9	— — —	125 80 50	ns
Setup Times — Data to CLK	6	t_{su}	3 5 9	30 20 18	— — —	ns
CLK to ENB			3 5 9	70 32 25	— — —	
Hold Time — CLK to Data	6	t_h	3 5 9	12 12 15	— — —	ns
Recovery Time — ENB to CLK	6	t_{rec}	3 5 9	5 10 20	— — —	ns
Input Rise and Fall Times — CLK, OSC_{in}, f_{in}	7	t_r, t_f	3 5 9	— — —	5 2 0.5	µs
Input Pulse Width — ENB and CLK	8	t_w	3 5 9	40 35 25	— — —	ns

NOTE: Refer to the graphs and text in application note AN969 for maximum frequency information.

PIN DESCRIPTIONS

INPUT PINS

OSC_{in}, OSC_{out}
Oscillator Input and Oscillator Output (PDIP, SOG – Pins 2, 3; SSOP – Pins 7, 8)

These pins form an on–chip reference oscillator when connected to terminals of an external parallel–resonant crystal. Frequency–setting capacitors of appropriate value must be connected from OSC_{in} to V_{SS} and OSC_{out} to V_{SS}. OSC_{in} may also serve as input for an externally–generated reference signal. This signal will typically be ac coupled to OSC_{in}, but for larger amplitude signals (standard CMOS logic levels), dc coupling may also be used. In the external reference mode, no connection is required to OSC_{out}.

f_{in}
Frequency Input (PDIP, SOG – Pin 10, SSOP – Pin 15)

Input to the positive edge triggered divide–by–N and divide–by–A counters. f_{in} is typically derived from a dual–modulus prescaler and is ac coupled. This input has an inverter biased in the linear region to allow use with ac coupled signals as low as 500 mV peak–to–peak or direct coupled signals swinging from V_{DD} to V_{SS}.

DATA
Serial Data Input (PDIP, SOG – Pin 12, SSOP – Pin 17)

Counter and control information is shifted into this input. The last data bit entered goes into the one–bit control shift register. A logic 1 allows the reference counter information to be loaded into its 14–bit latch when ENB goes high. A logic 0 entered as the control bit disables the reference counter latch. The divide–by–A/divide–by–N counter latch is loaded, regardless of the contents of the control register, when ENB goes high. The data entry format is shown in Figure 1.

ENB
Transparent Latch Enable (PDIP, SOG – Pin 13, SSOP – Pin 18)

A logic high on this input allows data to be entered into the divide–by–A/divide–by–N latch and, if the control bit is high, into the reference counter latch. Counter programming is unaffected when ENB is low. ENB should be kept normally low and pulsed high to transfer data to the latches.

CLK
Shift Register Clock (PDIP, SOG – Pin 11, SSOP – Pin 16)

A low–to–high transition on this input shifts data from the serial data input into the shift registers.

COMPONENT PINS

C_R
Ramp Capacitor (PDIP, SOG – Pin 15, SSOP – Pin 20)

The capacitor connected from this pin to V_{SS}' is charged linearly, at a rate determined by R_R. The voltage on this capacitor is proportional to the phase difference of the frequencies present at the internal phase detector inputs. A polystyrene or mylar capacitor is recommended.

R_R
Ramp Current Bias Resistor (PDIP, SOG – Pin 20, SSOP – Pin 5)

A resistor connected from this pin to V_{SS}' determines the rate at which the ramp capacitor is charged, thereby affecting the phase detector gain (see Figure 2).

C_H
Hold Capacitor (PDIP, SOG – Pin 18, SSOP – Pin 3)

The charge stored on the ramp capacitor is transferred to the capacitor connected from this pin to either V_{DD}' or V_{SS}'. The ratio of C_R to C_H should be large enough to have no effect on the phase detector gain ($C_R > 10\ C_H$). A low–leakage capacitor should be used.

R_O
Output Bias Current Resistor (PDIP, SOG – Pin 1, SSOP – Pin 6)

A resistor connected from this pin to V_{SS}' biases the output N–Channel transistor, thereby setting a current sink on the analog phase detector output. This resistor adjusts the APD_{out} bias current (see Figure 3).

OUTPUT PINS

APD_{out}
Analog Phase Detector Output (PDIP, SOG – Pin 17, SSOP – Pin 2)

This output produces a voltage that controls an external VCO. The voltage range of this output (V_{DD} = + 9 V) is from below + 0.5 V to + 8 V or more. The source impedance of this output is the equivalent of a source follower with an externally variable source resistor. The source resistor depends upon the output bias current controlled by the output bias current resistor, R_O. The bias current is adjustable from 0.01 mA to 0.5 mA. The output voltage is not more than 1.05 V below the sampled point on the ramp. With a constant sample of the ramp voltage at 9 V and the hold capacitor of 50 pF, the instantaneous output ripple is about 5 mV peak–to–peak.

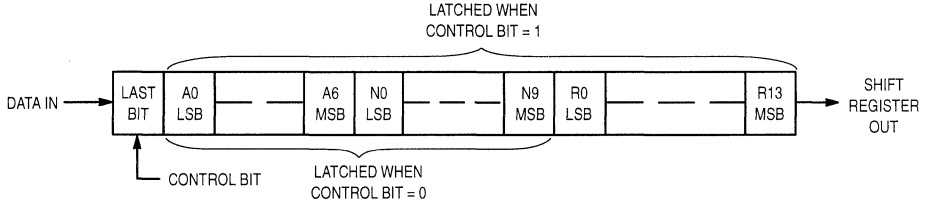


Figure 1. Data Entry Format

CHARGE
Ramp Charge Indicator (PDIP, SOG – Pin 4, SSOP – Pin 9)

This output is high from the time f_R goes high to the time f_V goes high (f_R and f_V are the frequencies at the phase detector inputs). This high voltage indicates that the ramp capacitor, C_R, is being charged.

FSO
Three–State Frequency Steering Output (PDIP, SOG – Pin 6, SSOP – Pin 11)

If the counted down input frequency on f_{in} is higher than the counted down reference frequency of OSC_{in}, this output goes low. If the counted down VCO frequency is lower than that of the counted down OSC_{in}, this output goes high.

The repetition rate of the frequency steering output pulses is approximately equal to the difference of the frequencies of the two counted down inputs from the VCO and OSC_{in}. See Application Note AN969 for further information.

LD
Lock Detector Indicator (PDIP, SOG – Pin 9, SSOP – Pin 14)

This output is high during lock and goes low to indicate a non–lock condition. The frequency and duration of the non–lock pulses will be the same as either polarity of the frequency steering output.

MC
Dual Modulus Prescaler Control (PDIP, SOG – Pin 8, SSOP – Pin 13)

The modulus control level is low at the beginning of a count cycle and remains low until the divide–by–A counter has counted down from its programmed value. At that time, the modulus control goes high and remains high until the divide–by–N counter has counted the rest of the way down from its programmed value (N – A additional counts since both divide–by–N and divide–by–A are counting down during the first portion of the cycle). Modulus control is then set back low, the counters preset to their respective programmed values, and the above sequence repeated. This provides for a total programmable divide value of $N_T = N \bullet P + A$, where P and P + 1 represent the dual modulus prescaler divide values respectively for high and low modulus control levels, N is the number programmed into the divide–by–N counter, and A is the number programmed into the divide–by–A counter.

SR_{out}
Shift Register Output (PDIP, SOG – Pin 14, SSOP – Pin 19)

This pin is the non–inverted output of the last stage of the 32–bit serial data shift register. It is not latched by the ENB line. If unused, SR_{out} should be floated.

POWER SUPPLY

V_{DD}
Positive Power Supply (PDIP, SOG – Pin 5, SSOP – Pin 10)

Positive power supply input for all sections of the device except the analog phase detector. V_{DD} and V_{DD}' should be powered up at the same time to avoid damage to the MC145159–1. V_{DD} must be tied to the same potential as V_{DD}'.

V_{SS}
Negative Power Supply (PDIP, SOG – Pin 7, SSOP – Pin 12)

Circuit ground for all sections of the MC145159–1 except the analog phase detector. V_{SS} must be tied to the same potential as V_{SS}'.

V_{SS}'
Analog Phase Detector Circuit Ground (PDIP, SOG – Pin 16, SSOP – Pin 1)

Separate power supply and ground inputs are provided to help reduce the effects in the analog section of noise coming from the digital sections of this device and the surrounding circuitry.

V_{DD}'
Analog Power Supply (PDIP, SOG – Pin 19, SSOP – Pin 4)

Separate power supply and ground inputs are provided to help reduce the effects in the analog section of noise coming from the digital sections of this device and the surrounding circuitry.

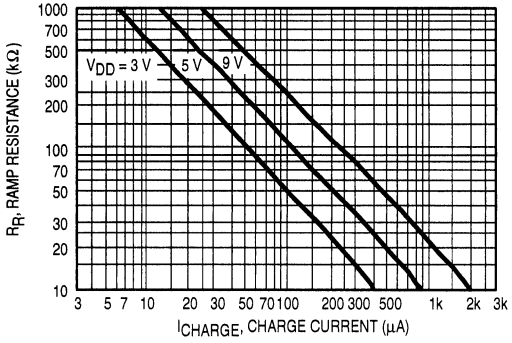


Figure 2. Charge Current vs Ramp Resistance

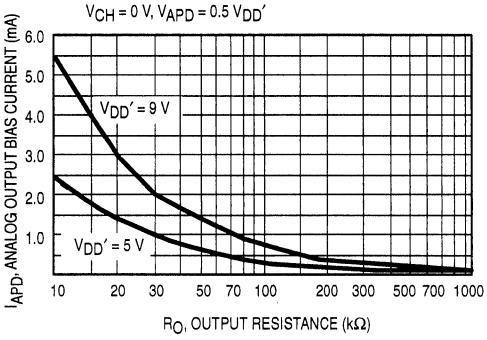


Figure 3. APD_{out} Bias Current vs Output Resistance

2

DESIGN EQUATION

$$K_\phi = \frac{I_{CHARGE}}{2\pi f_R C_R}$$

where

K_ϕ = phase detector gain, I_{CHARGE} is from Figure 2
f_R = reference frequency
C_R = ramp capacitor (in farads)

SWITCHING WAVEFORMS

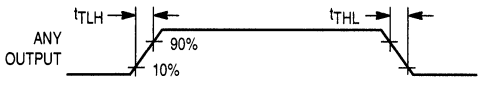


Figure 4.

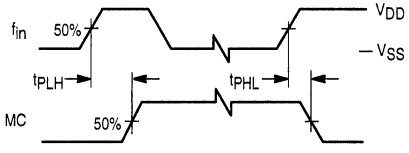


Figure 5.

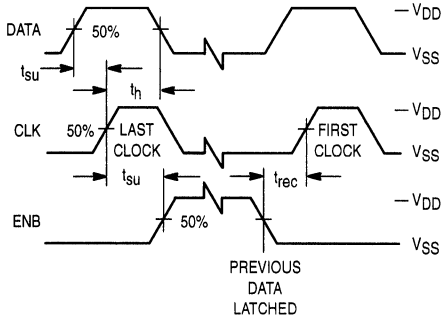


Figure 6.

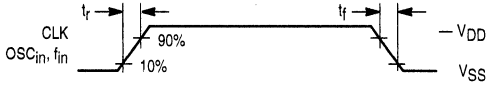


Figure 7.

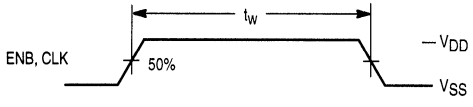
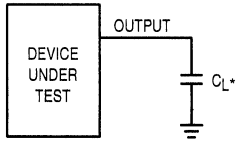


Figure 8.



* Includes all probe and fixture capacitance.

Figure 9. Test Circuit

DESIGN CONSIDERATIONS

CRYSTAL OSCILLATOR CONSIDERATIONS

The following options may be considered to provide a reference frequency to Motorola's CMOS frequency synthesizers.

Use of a Hybrid Crystal Oscillator

Commercially available temperature–compensated crystal oscillators (TCXOs) or crystal–controlled data clock oscillators provide very stable reference frequencies. An oscillator capable of sinking and sourcing 50 μA at CMOS logic levels may be direct or dc coupled to OSC_{in}. In general, the highest frequency capability is obtained utilizing a direct coupled square wave having a rail–to–rail (V_{DD} to V_{SS}) voltage swing. If the oscillator does not have CMOS logic levels on the outputs, capacitive or ac coupling to OSC_{in} may be used. OSC_{out}, an unbuffered output, should be left floating.

For additional information about TCXOs and data clock oscillators, please consult the latest version of the *eem Electronic Engineers Master Catalog,* the *Gold Book,* or similar publications.

Design an Off–Chip Reference

The user may design an off–chip crystal oscillator using ICs specifically developed for crystal oscillator applications, such as the MC12061 MECL device. The reference signal from the MECL device is ac coupled to OSC_{in}. For large amplitude signals (standard CMOS logic levels), dc coupling is used. OSC_{out}, an unbuffered output, should be left floating. In general, the highest frequency capability is obtained with a direct–coupled square wave having rail–to–rail voltage swing.

Use of the On–Chip Oscillator Circuitry

The on–chip amplifier (a digital inverter) along with an appropriate crystal may be used to provide a reference source frequency. A fundamental mode crystal, parallel resonant at the desired operating frequency, should be connected as shown in Figure 10.

For V_{DD} = 5 V, the crystal should be specified for a loading capacitance, C_L, which does not exceed 32 pF for frequencies to approximately 8 MHz, 20 pF for frequencies in the area of 8 to 15 MHz, and 10 pF for higher frequencies. These are guidelines that provide a reasonable compromise between IC capacitance, drive capability, swamping variations in stray and IC input/output capacitance, and realistic C_L values. Assuming R1 = 0 Ω. the shunt load capacitance, C_L, presented across the crystal can be estimated to be:

$$C_L = \frac{C_{in}C_{out}}{C_{in} + C_{out}} + C_a + C_{stray} + \frac{C1 \cdot C2}{C1 + C2}$$

where

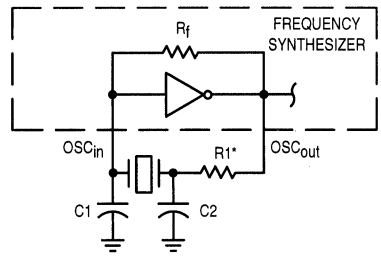
C_{in} = 5 pF (see Figure 11)
C_{out} = 6 pF (see Figure 11)
C_a = 1 pF (see Figure 11)
C1 and C2 = external capacitors (see Figure 10)
C_{stray} = the total equivalent external circuit stray capacitance appearing across the crystal terminals

The oscillator can be "trimmed" on–frequency by making a portion or all of C1 variable. The crystal and associated components must be located as close as possible to the OSC_{in} and OSC_{out} pins to minimize distortion, stray capacitance, stray inductance, and start–up stabilization time. Circuit stray capacitance can also be handled by adding the appropriate stray value to the values for C_{in} and C_{out}. For this approach, the term C_{stray} becomes zero in the above expression for C_L.

Power is dissipated in the effective series resistance of the crystal, R_e, in Figure 12. The maximum drive level specified by the crystal manufacturer represents the maximum stress that a crystal can withstand without damaging or excessive shift in operating frequency. R1 in Figure 10 limits the drive level. The use of R1 is not necessary in most cases.

To verify that the maximum dc supply voltage does not overdrive the crystal, monitor the output frequency as a function of voltage at OSC_{out}. (Care should be taken to minimize loading.) The frequency should increase very slightly as the dc supply voltage is increased. An overdriven crystal will decrease in frequency or become unstable with an increase in supply voltage. The operating supply voltage must be reduced or R1 must be increased in value if the overdriven condition exists. The user should note that the oscillator start–up time is proportional to the value of R1.

Through the process of supplying crystals for use with CMOS inverters, many crystal manufacturers have developed expertise in CMOS oscillator design with crystals. Discussions with such manufacturers can prove very helpful. See Table 1.



* May be deleted in certain cases. See text.

Figure 10. Pierce Crystal Oscillator Circuit

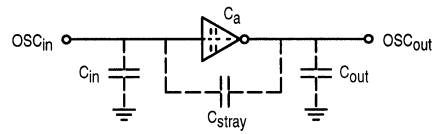
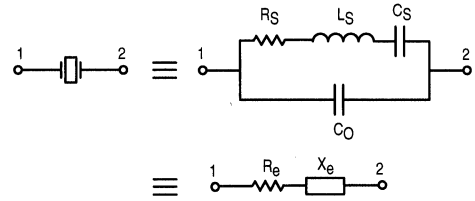


Figure 11. Parasitic Capacitances of the Amplifier and C_{stray}



NOTE: Values are supplied by crystal manufacturer (parallel resonant crystal).

Figure 12. Equivalent Crystal Networks

Table 1. Partial List of Crystal Manufacturers

Name	Address	Phone
United States Crystal Corp.	3605 McCart Ave., Ft. Worth, TX 76110	(817) 921–3013
Crystek Crystal	2351 Crystal Dr., Ft. Myers, FL 33907	(813) 936–2109
Statek Corp.	512 N. Main St., Orange, CA 92668	(714) 639–7810

NOTE: Motorola cannot recommend one supplier over another and in no way suggests that this is a complete listing of crystal manufacturers.

RECOMMENDED READING

Technical Note TN–24, Statek Corp.

Technical Note TN–7, Statek Corp.

E. Hafner, "The Piezoelectric Crystal Unit – Definitions and Method of Measurement", *Proc. IEEE*, Vol. 57, No. 2 Feb., 1969.

D. Kemper, L. Rosine, "Quartz Crystals for Frequency Control", *Electro–Technology*, June, 1969.

P. J. Ottowitz, "A Guide to Crystal Selection", *Electronic Design*, May, 1966.

D. Babin, "Designing Crystal Oscillators", *Machine Design*, March 7, 1985.

D. Babin, "Guidelines for Crystal Oscillator Design", *Machine Design*, April 25, 1985.

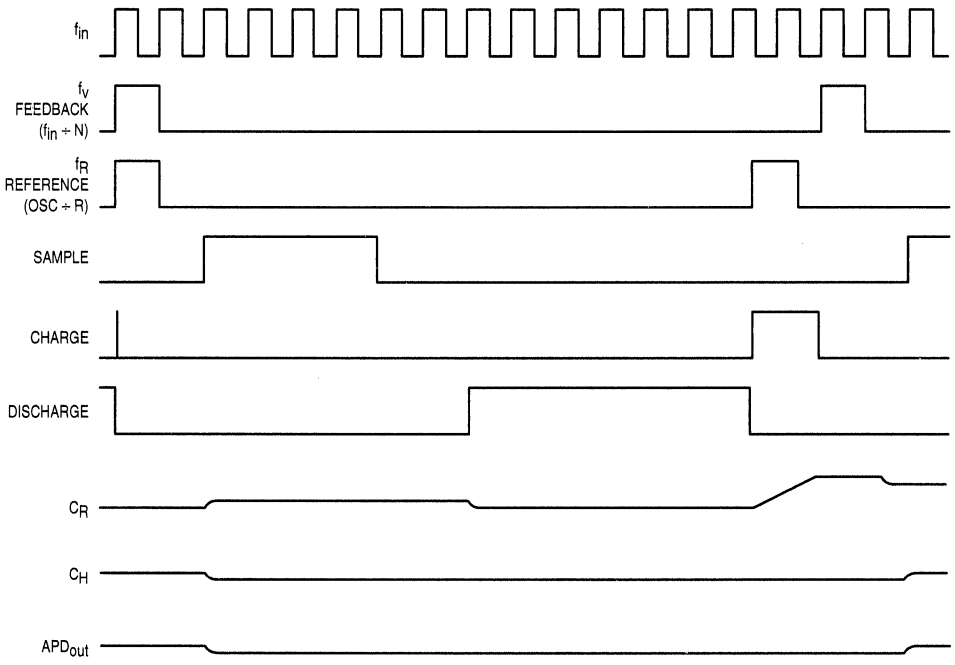


Figure 13. Timing Diagram for Minimum Divide Value (N = 16)

MC145162
MC145162-1

2

Advance Information

60 MHz and 85 MHz Universal Programmable Dual PLL Frequency Synthesizers

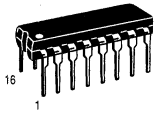
CMOS

The MC145162 is a dual phase–locked loop (PLL) frequency synthesizer especially designed for CT–1 cordless phone applications worldwide. This frequency synthesizer is also for any product with a frequency operation at 60 MHz or below.

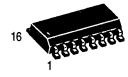
The MC145162–1 is a high frequency derivative of the MC145162, for products with operating frequencies of 85 MHz or below.

The device features fully programmable receive, transmit, reference, and auxiliary reference counters accessed through an MCU serial interface. This feature allows this device to operate in any CT–1 cordless phone application. The device consists of two independent phase detectors for transmit and receive loops. A common reference oscillator, driving two independent reference frequency counters, provides independent reference frequencies for transmit and receive loops. The auxiliary reference counter allows the user to select an additional reference frequency for receive and transmit loops if required.

- Operating Voltage Range: 2.5 to 5.5 V
- Operating Temperature Range: – 40 to + 75°C
- Operating Power Consumption: 3.0 mA @ 2.5 V
- Maximum Operating Frequency:
  MC145162 — 60 MHz @ 200 mV p–p, V_{DD} = 2.5 V
  MC145162–1 — 85 MHz @ 250 mV p–p, V_{DD} = 2.5 V
- Three or Four Pins Used for Serial MCU Interface
- Built–In MCU Clock Output with Frequency of Reference Oscillator ÷3/÷4
- Power Saving Mode Controlled by MCU
- Lock Detect Signal
- On–Chip Reference Oscillator Supports External Crystals to 16.0 MHz
- Reference Frequency Counter Division Range: 16 to 4095
- Auxiliary Reference Frequency Counter Division Range: 16 to 16,383
- Transmit Counter Division Range: 16 to 65,535
- Receive Counter Division Range: 16 to 65,535



P SUFFIX
PLASTIC DIP
CASE 648

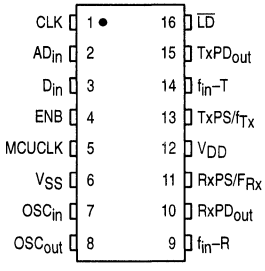


D SUFFIX
SOG PACKAGE
CASE 751B

ORDERING INFORMATION

MC145162P	Plastic DIP
MC145162D	SOG Package
MC145162P1	Plastic DIP
MC145162D1	SOG Package

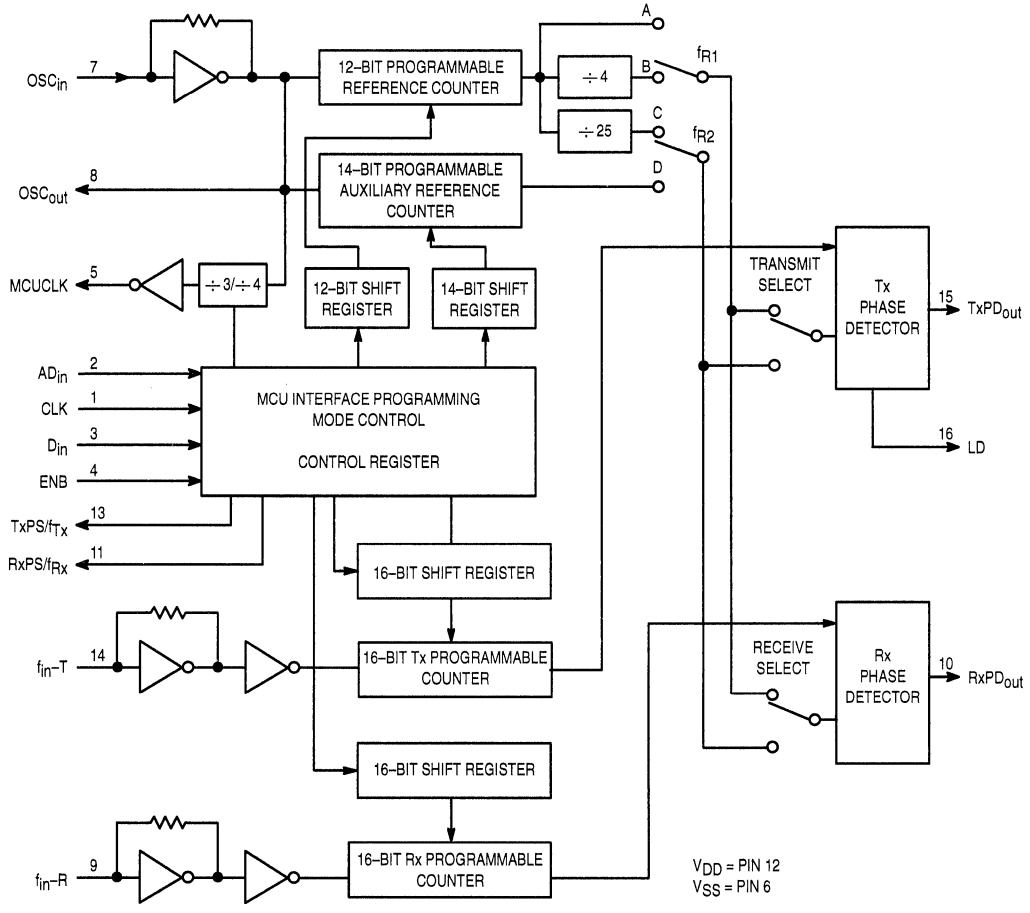
PIN ASSIGNMENT



This document contains information on a new product. Specifications and information herein are subject to change without notice.

REV 2
8/95

BLOCK DIAGRAM



MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Rating	Value	Unit
V_{DD}	DC Supply Voltage	– 0.5 to + 6.0	V
V_{in}	Input Voltage, All Inputs	– 0.5 to V_{DD} + 0.5	V
I_{in}, I_{out}	DC Current Drain Per Pin	10	mA
I_{DD}, I_{SS}	DC Current Drain V_{DD} or V_{SS} Pins	30	mA
T_{stg}	Storage Temperature Range	– 65 to + 150	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Descriptions section.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused pins must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

2

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS}, T_A = 25°C)

Symbol	Characteristic	V_{DD}	Guaranteed Limit		Unit
			Min	Max	
V_{DD}	Power Supply Voltage Range	—	2.5	5.5	V
V_{OL}	Output Voltage (I_{out} = 0) 0 Level	2.5 5.5	— —	0.1 0.1	V
V_{OH}	(V_{in} = V_{DD} or 0) 1 Level	2.5 5.5	2.45 5.45	— —	
V_{IL}	Input Voltage (V_{out} = 0.5 V or V_{DD} – 0.5 V) 0 Level	2.5 5.5	— —	0.75 1.65	V
V_{IH}	1 Level	2.5 5.5	1.75 3.85	— —	
I_{OH}	Output Current (V_{out} = 2.2 V) (V_{out} = 5.0 V) Source	2.5 5.5	– 0.18 – 0.55	— —	mA
I_{OL}	(V_{out} = 0.3 V) (V_{out} = 0.5 V) Sink	2.5 5.5	0.18 0.55	— —	
I_{IL}	Input Current (V_{in} = 0) OSC_{in}, f_{in}–T, f_{in}–R	2.5 5.5	— —	– 30 – 66	μA
	AD_{in}, CLK, D_{in}, ENB	2.5 5.5	— —	– 1.0 – 1.0	
I_{IH}	(V_{in} = V_{DD} – 0.5) OSC_{in}, f_{in}–T, f_{in}–R	2.5 5.5	— —	30 66	
	AD_{in}, CLK, D_{in}, ENB	2.5 5.5	— —	5.0 5.0	
I_{OZ}	Three–State Leakage Current (V_{out} = 0 V or 5.5 V)	5.5	—	± 100	nA
C_{in}	Input Capacitance	—	—	8.0	pF
C_{out}	Output Capacitance	—	—	8.0	pF
$I_{DD(stdby)}$	Standby Current (All Counters are in Power–Down Mode with Oscillator On)	2.5 5.5	— —	0.3 1.5	mA
I_{DD}	Operating Current MC145162: 200 mV p–p input at f_{in}–T and f_{in}–R = 60 MHz MC145162–1: 250 mV p–p input at f_{in}–T and f_{in}–R = 85 MHz with OSC = 10.24 MHz	2.5 5.5	— —	3.0 10	mA

SWITCHING CHARACTERISTICS (T_A = 25°C, C_L = 50 pF)

Symbol	Characteristic		Figure No.	V_{DD}	Guaranteed Limit		Unit
					Min	Max	
t_{TLH}	Output Rise Time		1	2.5 5.5	— —	200 100	ns
t_{THL}	Output Fall Time		1	2.5 5.5	— —	200 100	ns
t_r, t_f	Input Rise and Fall Time	OSC_{in}	2	2.5 5.5	— —	5.0 4.0	µs
t_w	Input Pulse Width	CLK and ENB	3	2.5 5.5	80 60	— —	ns
f_{max}	Input Frequency Input = Sine Wave @ ≥ 200 mV p–p for MC145162 Input = Sine Wave @ ≥ 250 mV p–p for MC145162–1	OSC_{in} f_{in}–R, f_{in}–T f_{in}–R, f_{in}–T		2.5 – 5.5 2.5 – 5.5 2.5 – 5.5	— — —	16 60 85	MHz
t_{su}	Setup Time	DATA to CLK ENB to CLK	5	2.5 5.5	100 200	— —	ns
t_h	Hold Time	CLK to DATA	5	3.0 5.0	80 40	— —	ns
t_{rec}	Recovery Time	ENB to CLK	5	3.0 5.0	80 40	— —	ns
t_{su1}	Setup Time	ENB to CLK	4	2.5 – 5.5	80	—	ns
t_{h1}	Hold Time	CLK to ENB	4	2.5 – 5.5	600	—	ns

SWITCHING WAVEFORMS

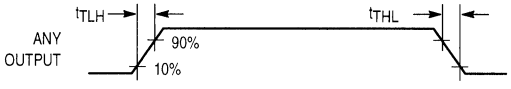


Figure 1.

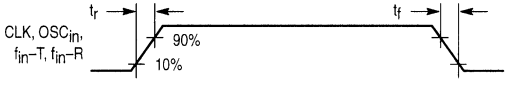


Figure 2.

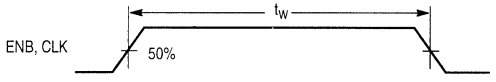


Figure 3.

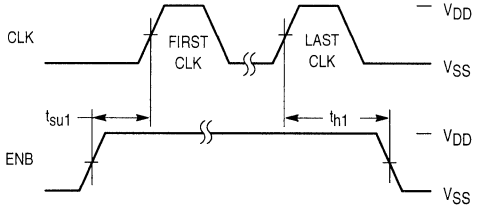


Figure 4. ENB High During Serial Transfer

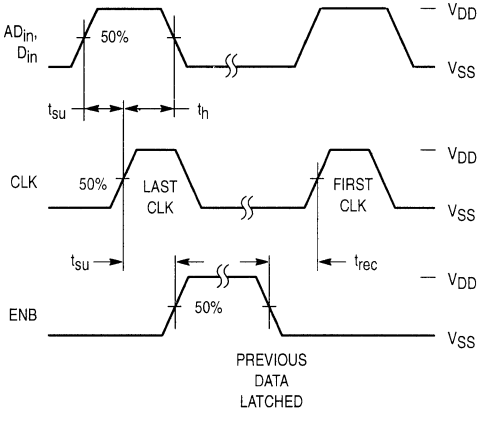


Figure 5. ENB Low During Serial Transfer

PIN DESCRIPTIONS

INPUT PINS

OSC_{in} /OSC_{out}
Reference Oscillator Input/Output (Pins 7, 8)

These pins form a reference oscillator when connected to an external parallel–resonant crystal. Figure 6 shows the relationship of different crystal frequencies and reference frequencies for cordless phone applications in various countries. OSC_{in} may also serve as input for an externally generated reference signal which is typically ac coupled.

MCUCLK
System Clock (Pin 5)

This output pin provides a signal of the crystal frequency (OSC_{out}) divided by 3 or 4 that is controlled by a bit in the control register.

This signal can be a clock source for the MCU or other system clocks.

AD_{in}, D_{in}, CLK, ENB
Auxiliary Data In, Data In, Clock, Enable (Pins 2, 3, 1, 4)

These four pins provide an MCU serial interface for programming the reference counter, the transmit–channel counter, and the receive–channel counter. They also provide various controls of the PLL including the power saving mode and the programming format.

$TxPS/f_{Tx}$, $RxPS/f_{Rx}$
Transmit Power Save, Receive Power Save (Pins 13, 11)

For a normal application, these output pins provide the status of the internal power saving mode operation. If the transmit–channels counter circuitry is in power down mode, $TxPS/f_{Tx}$ outputs a high state. If the receive–channels counter circuitry is in power down mode, $RxPS/f_{Rx}$ is set high. These outputs can be applied for controlling the external power switch for the transmitter and the receiver to save MCU control pins.

In the Tx/Rx channel counter test mode, the $TxPS/f_{Tx}$ and $RxPS/f_{Rx}$ pins output the divided value of the transmit channel counter (f_{Tx}) and the receive channel counter (f_{Rx}), respectively. This test mode operation is controlled by the control register. Details of the counter test mode are in the **Tx/Rx Channel Counter Test** section of this data sheet.

f_{in}–T/f_{in}–R
Transmit/Receive Counter Inputs (Pins 14, 9)

f_{in}–T and f_{in}–R are inputs to the transmit and the receive counters, respectively. These signals are typically driven from the loop VCO and ac coupled. The minimum input signal level is 200 mV p–p @ 60.0 MHz.

OUTPUT PINS

$TxPD_{out}$/$RxPD_{out}$
Transmit/Receive Phase Detector Outputs (Pins 15, 10)

These are three–state outputs of the transmit and receive phase detectors for use as loop error signals (see Figure 7 for phase detector output waveforms). Phase detector gain is $V_{DD}/4\ \pi$ volts per radian.

Frequency $f_V > f_R$ or f_V leading: output = negative pulse.
Frequency $f_V < f_R$ or f_V lagging: output = positive pulse.
Frequency $f_V = f_R$ and phase coincidence: output = high–impedance state.
NOTE: f_R is the divided–down reference frequency at the phase detector input and f_V is the divided–down VCO frequency at the phase detector input.

$\overline{LD}$
Lock Detect (Pin 16)

The lock detect signal is associated with the transmit loop. The output at a high level indicates an out–of–lock condition (see Figure 7 for the $\overline{LD}$ output waveform).

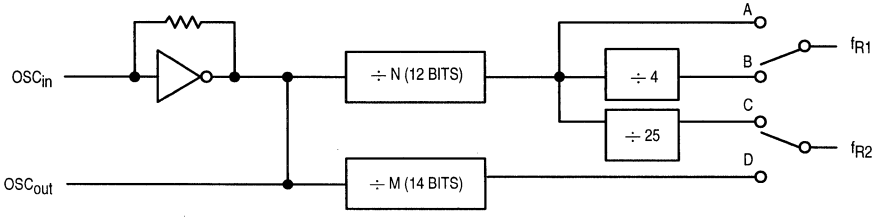
POWER SUPPLY

V_{DD}
Positive Power Supply (Pin 12)

V_{DD} is the most positive power supply potential ranging from 2.5 to 5.5 V with respect to V_{SS}.

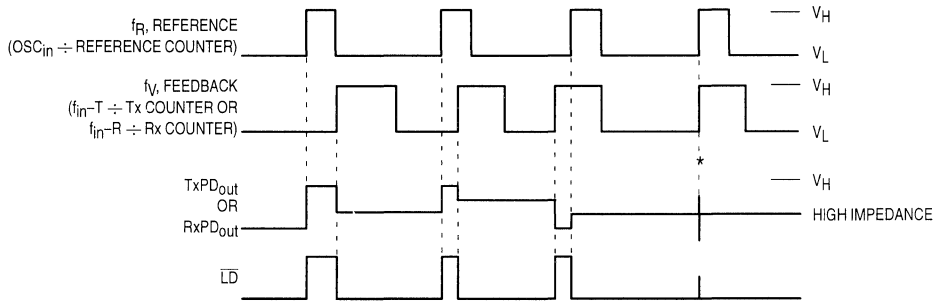
V_{SS}
Negative Power Supply (Pin 6)

V_{SS} is the most negative supply potential and is usually connected to ground.



Crystal	÷ N Value	f_{R1} B	f_{R2} C
11.150 MHz	446	6.25 kHz	1.0 kHz
11.150 MHz	223	12.5 kHz	
10.240 MHz	512	5.0 kHz	
12.000 MHz	600	5.0 kHz	

Figure 6. Reference Frequencies for Cordless Phone Applications of Various Countries



V_H = High voltage level.
V_L = Low voltage level.
*At this point, when both f_R and f_V are in phase, the output is forced to near mid supply.

NOTE: The $TxPD_{out}$ and $RxPD_{out}$ generate error pulses during out–of–lock conditions. When locked in phase and frequency, the output is high impedance and the voltage at that pin is determined by the low–pass filter capacitor.

Figure 7. Phase Detector/Lock Detector Output Waveforms

MCU PROGRAMMING SCHEME

The MCU programming scheme is defined in two formats controlled by the ENB input. If the enable signal is high during the serial data transfer, control register/reference frequency programming is selected. If the ENB is low, programming of the transmit and receive counters is selected. During programming of the transmit and receive counters, both AD_{in} and D_{in} pins can input the data to the transmit and receive counters. Both counters' data is clocked into the PLL internal shift register at the leading edge of the CLK signal. It is not necessary to reprogram the reference frequency counter/control register when using the enable signal to program the transmit/receive channels.

In programming the control register/reference frequency scheme, the most significant bit (MSB) of the programming word identifies whether the input data is the control word or the reference frequency data word. If the MSB is 1, the input data is the control word (Figure 8). Also see Figure 8 and Table 1 for control register and bit function. If the MSB is 0, the input data is the reference frequency (Figure 9).

The reference frequency data word is a 32–bit word containing the 12–bit reference frequency data, the 14–bit auxiliary reference frequency counter information, the reference frequency selection plus, the auxiliary reference frequency counter enable bit (Figure 9).

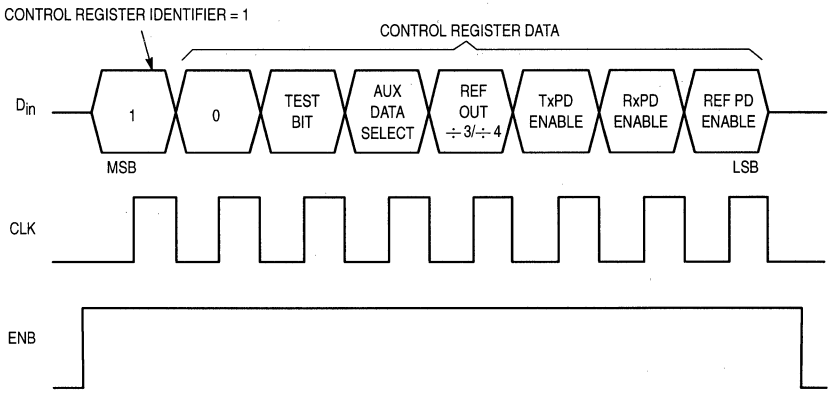
If the AUX REF ENB bit is high, the 14–bit auxiliary reference frequency counter provides an additional phase reference frequency output for the loops. If AUX REF ENB bit is low, the auxiliary reference frequency counter is forced into power–down mode for current saving. (Other power down modes are also provided through the control register per Table 2 and Figure 8.) At the falling edge of the ENB signal, the data is stored in the registers.

There are two interfacing schemes for the universal channel mode: the three–pin and the four–pin interfacing schemes. The three–pin interfacing scheme is suited for use with the MCU SPI (serial peripheral interface) (Figure 10), while the four–pin interfacing scheme is commonly used for general I/O port connection (Figure 11).

For the three–pin interfacing scheme, the auxiliary data select bit is set to 0. All 32 bits of data, which define both the 16–bit transmit counter and the 16–bit receive counter, latch into the PLL internal register through the data in pins at the leading edge of CLK. See Figures 12 and 13.

For the four–pin interfacing scheme, the auxiliary data select bit is set to 1. In this scheme, the 16–bit transmit counter's data enters into the AD_{in} pin at the same time as the 16–bit receive counter's data enters into the D_{in} pin. This simultaneous entry of the transmit and receive counters causes the programming period of the four–pin scheme to be half that of the three–pin scheme (see Figures 14 and 15).

While programming Tx/Rx Channel Counter, the ENB pin must be pulsed to provide falling edge to latch the shifted data after the rising edge of the last clock. Maximum data transfer rate is 500 kbps.



NOTE: ENB must be high during the serial transfer.

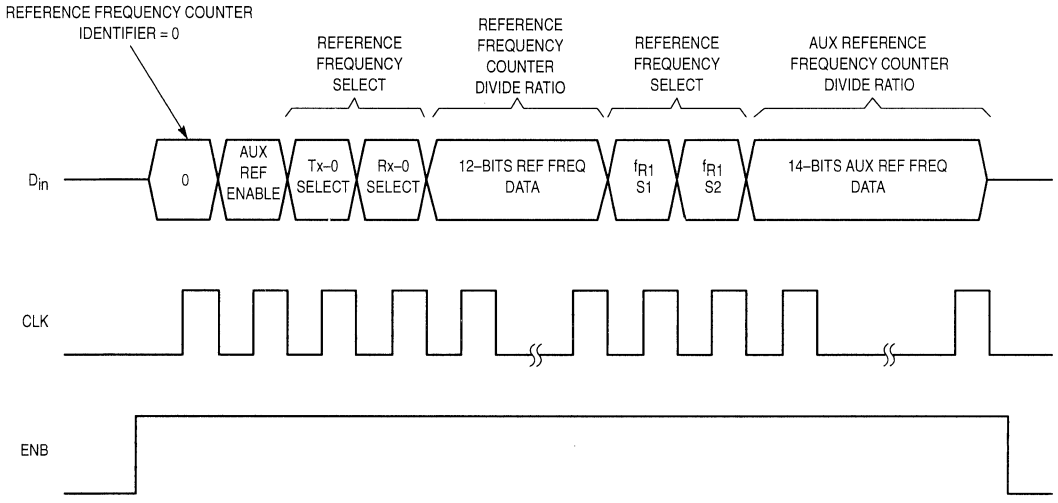
Figure 8. Programming Format of the Control Register

Table 1. Control Register Function Bits Description

Test Bit	Set to 1 for Tx/Rx channel counter test mode Set to 0 for normal application
Aux Data Select	Set to 1 for both AD_{in} and D_{in} pins inputting the transmit 16–bits data and receive 16–bits data respectively. Set to 0 for normal application interfacing with MCU serial peripheral interface. Does not use AD_{in} pin; tie AD_{in} to V_{SS}.
$REF_{out} \div 3/\div 4$	If set to 1, REF_{out} output frequency is equal to $OSC_{out} \div 3$. If set to 0, REF_{out} output is $OSC_{out} \div 4$.
TxPD Enable	If set to 1, the transmit counter, transmit phase detector, and the associated circuitry is in power–down mode. Tx PS/f_{Tx} is set "High".
RxPD Enable	If set to 1, the receive counter, receive phase detector, and the associated circuitry is in power–down mode. Rx PS/f_{Rx} is set "High".
Ref PD Enable	If set to 1, both 12–bit and 14–bit reference frequency counters are in power–down mode.

Table 2. Control Register Power Down Bits Function

TxPD Enable	RxPD Enable	REF PD Enable	Tx–Channel Counter	Rx–Channel Counter	Reference Frequency Counter
0	0	0	—	—	—
0	0	1	—	—	Power Down
0	1	0	—	Power Down	—
0	1	1	—	Power Down	Power Down
1	0	0	Power Down	—	—
1	0	1	Power Down	—	Power Down
1	1	0	Power Down	Power Down	—
1	1	1	Power Down	Power Down	Power Down



NOTE: ENB must be high during the serial transfer.

Figure 9. Programming Format of the Auxiliary/Reference Frequency Counters

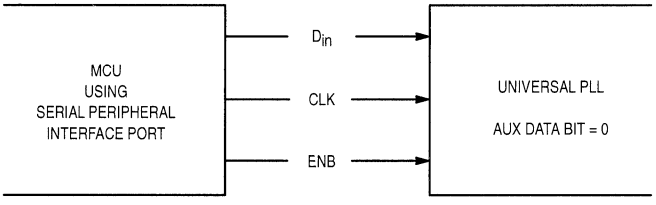


Figure 10. MCU Interface Using SPI

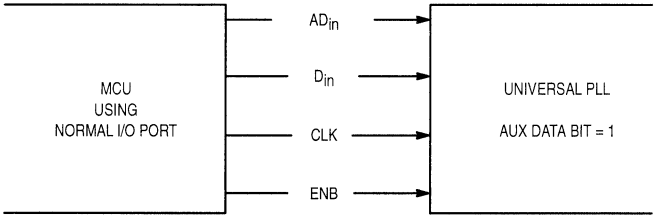
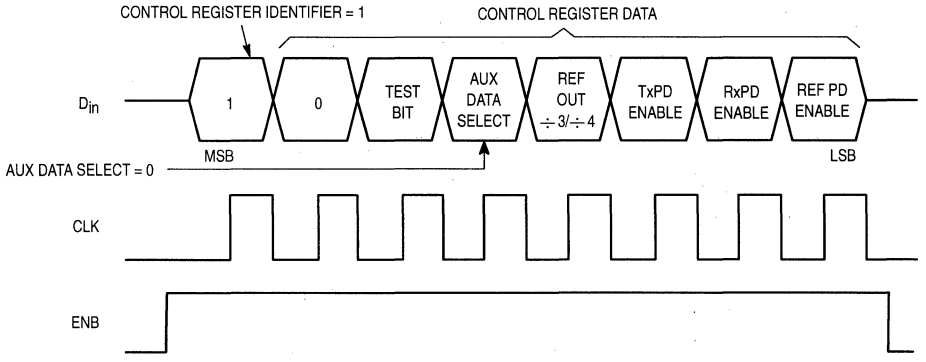
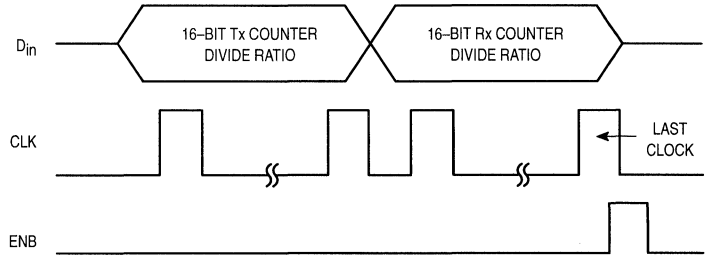


Figure 11. MCU Interface Using Normal I/O Ports with Both D_{in} and AD_{in} for Faster Programming Time



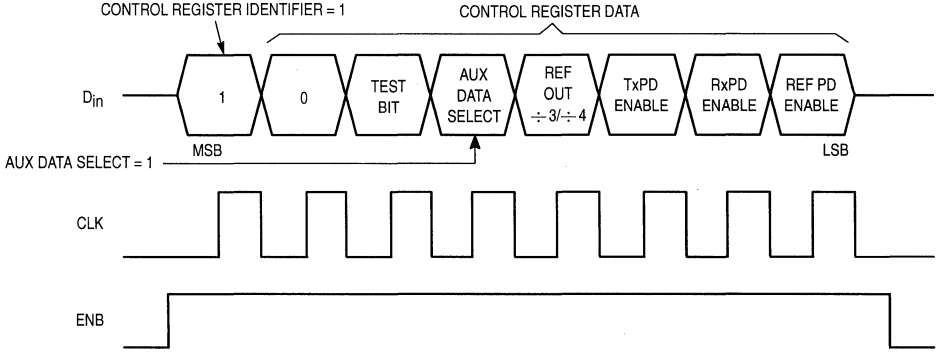
NOTE: ENB must be high during the serial transfer.

Figure 12. Programming Format for Control Register (3–Pin Interfacing Scheme)



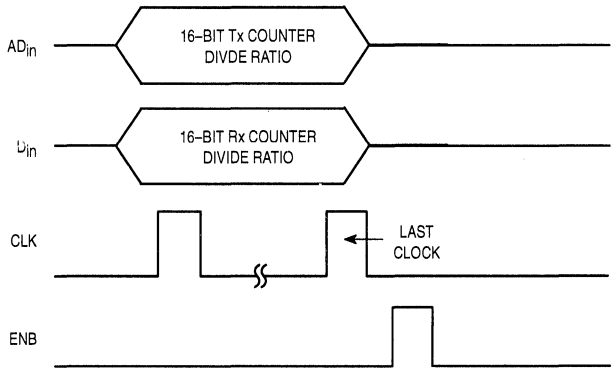
NOTE: ENB must be low during the serial transfer.

Figure 13. Programming Format for Transmit and Receive Counters (3–Pin Interfacing Scheme)



NOTE: ENB must be high during the serial transfer.

Figure 14. Programming Format for Control Register (4–Pin Interfacing Scheme)



NOTE: ENB must be low during the serial transfer.

Figure 15. Programming Format for Transmit and Receive Counters (4–Pin Interfacing Scheme)

Table 3. Global CT–1 Reference Frequency Setting vs Channel Frequencies

Country	Channels Frequency	f_{R1}	f_{R2}
U.S.A.	46/49 MHz (10, 15, 25 Channels)	5.0 kHz	—
France	26/41 MHz	6.25 kHz/12.5 kHz	—
Spain	31/41 MHz	5.0 kHz	—
Australia	30/39 MHz	5.0 kHz	—
U.K.	1.7/47 MHz	6.25 kHz	1.0 kHz
New Zealand	1.7/34/40 MHz	6.25 kHz	1.0 kHz

REFERENCE FREQUENCY SELECTION AND PROGRAMMING

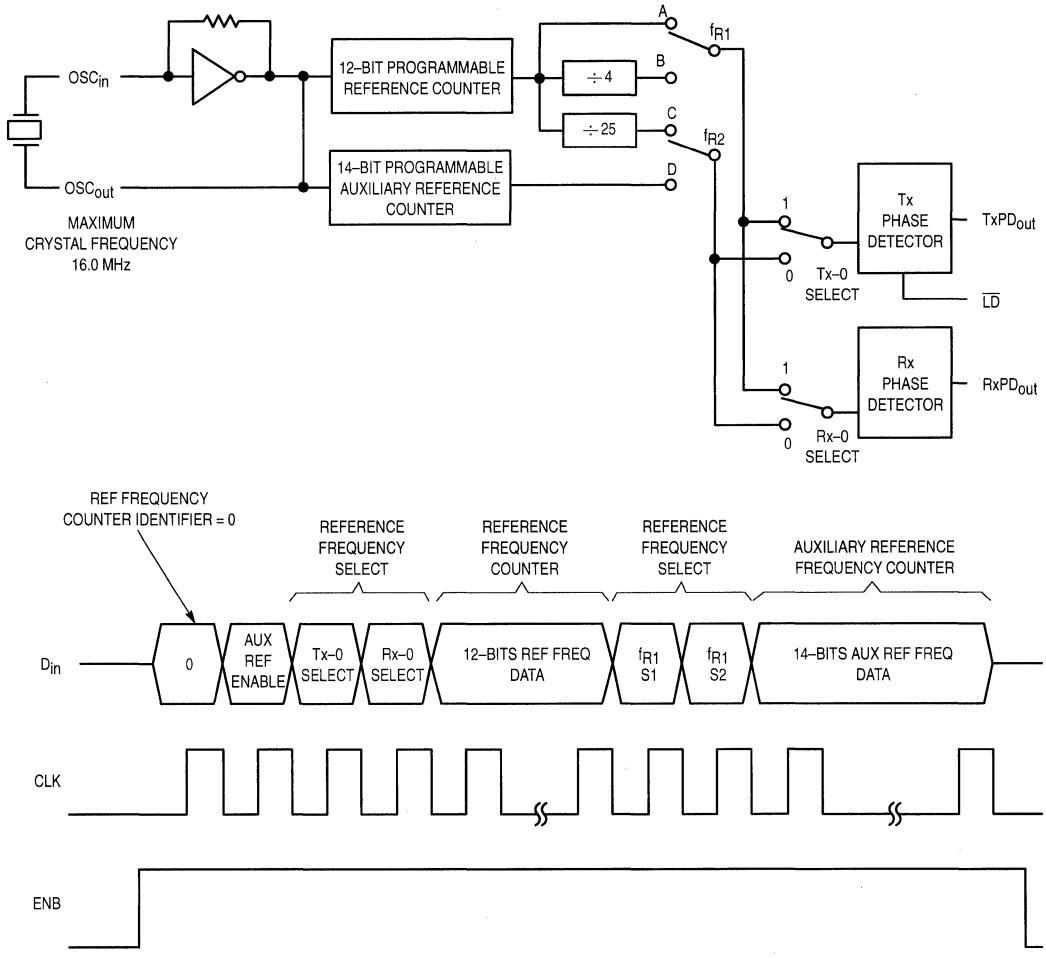
Figure 16 shows the bit function of the reference frequency programming word. The user can either select the "fixed" reference frequency for all channels accordingly or provide a specific reference frequency for a particular channel by using two reference frequency counters (e.g., for an application in France, the base set transmit channel common fixed reference frequency is 6.25 kHz or 12.5 kHz). (See Table 3 and Figure 6 for reference frequencies for various countries.) However, transmit channels 6, 8, and 14 can be set to 25 kHz, and channel 8 reference frequency can be set to 50 kHz. But this reference frequency may not be applied to the receiving side; therefore, the receiving side reference frequency must be generated by another reference frequency counter. The higher the reference frequency, the better the phase noise performance and faster the lock time, but the PLL consumes more current if both reference frequency counters are in operation.

In general, the 12–bit reference frequency counter plus the ÷ 4 and ÷ 25 module can offer all the reference frequencies for global CT–1 transmit and receive channel requirements. Users can select their own reference frequency by introducing the additional 14–bit auxiliary reference frequency counter.

Again, the 14–bit auxiliary reference frequency counter can be shut down by the auxiliary reference enable bit in the reference counter programming word by setting the bit to 0. At this state, the f_{R2} is automatically connected to point C (the ÷ 25 block output), and f_{R1} can be connected to point A or B by setting the f_{R1}–S1 and f_{R1}–S2 bits in the reference counter program word. The 14–bit auxiliary reference frequency counter data will be in "Don't Care" state.

If the 14–bit auxiliary reference frequency counter is enabled (auxiliary reference enable = 1), then f_{R2} is automatically connected to point D (14–bit counter output), and f_{R1} can be selected to connect to point A, B, or C, depending on the bit setting of f_{R1}–S1 and f_{R1}–S2.

Table 4 and Figure 16 describe the functions of the auxiliary reference enable bit and the f_{R1}–S1 and f_{R1}–S2 bits selection.



NOTE: ENB must be high during the serial transfer.

Figure 16. Reference Frequency Counter/Selection Programming Mode

Table 4. Bit Function and the Reference Frequency Selection Bit Setting of the Reference Frequency Counter Programming Word

AUX REF Enable	Auxiliary Reference Frequency Counter Mode	Module Select	f_{R1} S1	f_{R1} S2	f_{R1} Routing
0	14–Bit Auxiliary Reference Frequency Counter Disable	f_{R2} C	0	0	N/A
			0	1	f_{R1} A
			1	0	f_{R1} B
			1	1	N/A
1	14–Bit Auxiliary Reference Frequency Counter Enable	f_{R2} D	0	0	N/A
			0	1	f_{R1} A
			1	0	f_{R1} B
			1	1	f_{R1} C

N/A = Not Applicable

POWER SAVING OPERATION

This PLL has a programmable power–saving scheme. The transmit and receive counters and the reference frequency counter can be powered down individually by setting the TxPD enable, RxPD enable, and Ref PD enable bits of the control register. The functions of the power down control bits are explained in Table 2 and the programming format is in Figure 8.

The output pins TxPS/f_{Tx} and RxPS/f_{Rx} output the status of the internal power saving setting. If the bit TxPD enable is set "high" (transmit counter is set to power–down mode), then the TxPS/f_{Tx} pin will also output a "high" state. This TxPS/f_{Tx} output can control an external power switch to switch off the transmitter, as shown in Figure 17. This scheme can be applied to the RxPS/f_{Rx} output to control the receiver power saving operation as required.

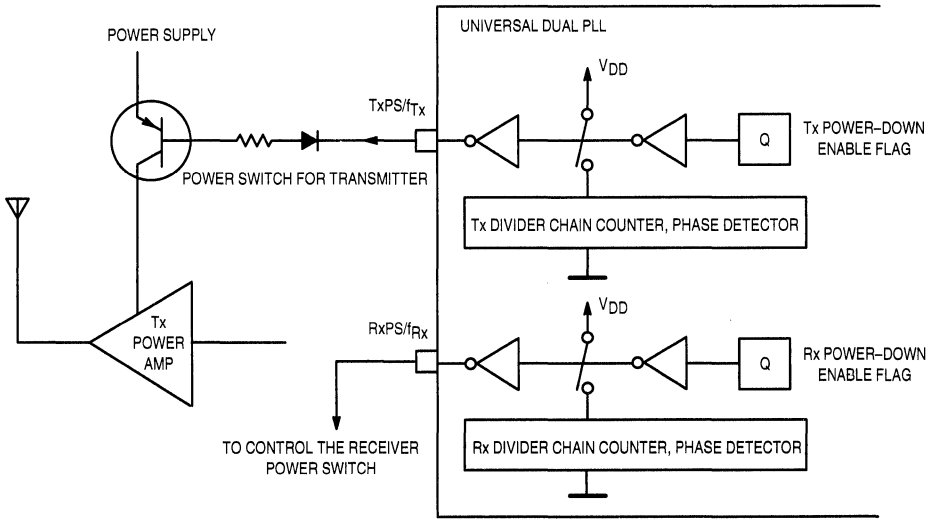


Figure 17. TxPS/f_{Tx} and RxPS/f_{Rx} Outputs to Control Power Switches of the Transmitter and the Receiver

Tx/Rx CHANNEL COUNTER TEST

In normal applications, the TxPS/f_{Tx} and the RxPS/f_{Rx} output pins indicate the power saving mode status. However, the user can examine the Tx and Rx channel counter outputs by setting the Test bit in the control register to 1. The final value of the transmit–channel counter and the receive–channel counter multiplex out to TxPS/f_{Tx} and RxPS/f_{Rx} respectively. The user can verify the divided–down output waveform associated with the RF input level in the PLL circuitry implementation (Figure 18).

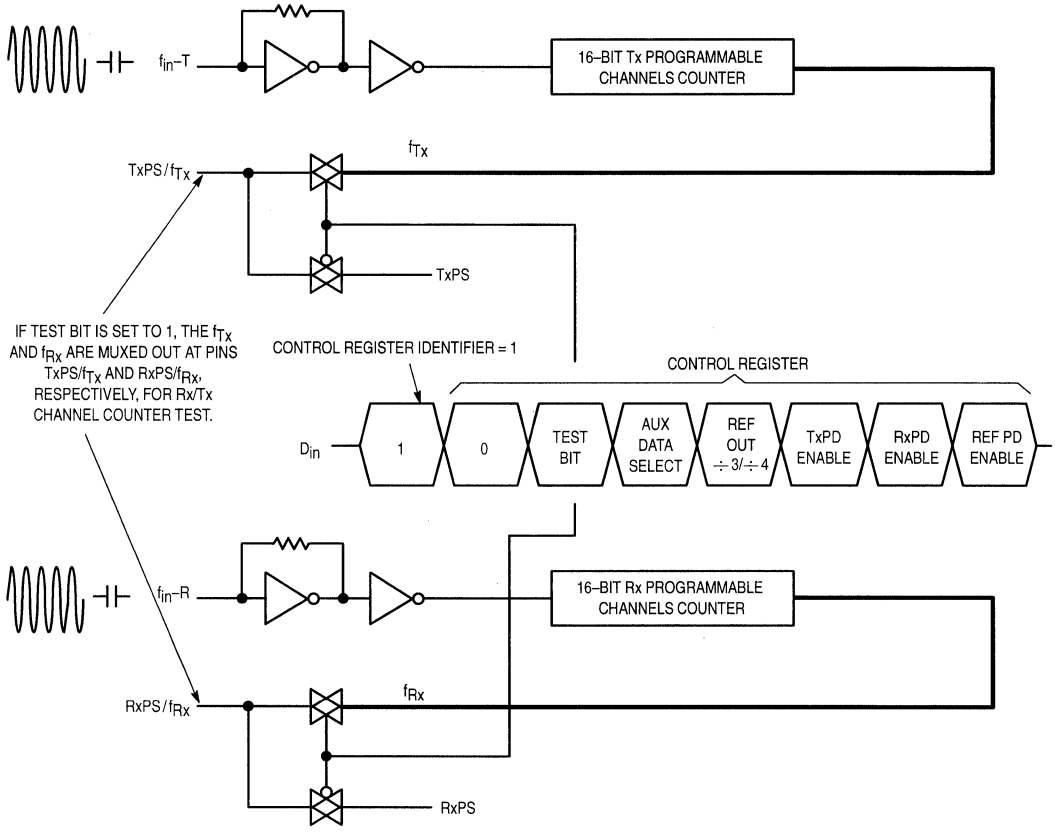


Figure 18. RF Buffer Sensitivity

Table 5. France CT–1 Base Set Frequency

Channel Number	Tx Channel Frequency (MHz)	Tx Counter Value (Ref. Freq. = 6.25 kHz)	f_{in}–R Input Frequency (MHz) [1st IF = 10.7 MHz]	Rx Counter Value (Ref. Freq. = 6.25 kHz)
1	26.4875	4238	30.7875	4926
2	26.4750	4236	30.7750	4924
3	26.4625	4234	30.7625	4922
4	26.4500	4232	30.7500	4920
5	26.4375	4230	30.7375	4918
6	26.4250	4228	30.7250	4916
7	26.4125	4226	30.7125	4914
8	26.4000	4224	30.7000	4912
9	26.3875	4222	30.6875	4910
10	26.3750	4220	30.6750	4908
11	26.3625	4218	30.6625	4906
12	26.3500	4216	30.6500	4904
13	26.3375	4214	30.6375	4902
14	26.3250	4212	30.6250	4900
15	26.3125	4210	30.6125	4898

Table 6. France CT–1 Handset Frequency

Channel Number	Tx Channel Frequency (MHz)	Tx Counter Value (Ref. Freq. = 6.25 kHz)	f_{in}–R Input Frequency (MHz) [1st IF = 10.7 MHz]	Rx Counter Value (Ref. Freq. = 6.25 kHz)
1	41.4875	6638	37.1875	5950
2	41.4750	6636	37.1750	5948
3	41.4625	6634	37.1625	5946
4	41.4500	6632	37.1500	5944
5	41.4375	6630	37.1375	5942
6	41.4250	6628	37.1250	5940
7	41.4125	6626	37.1125	5938
8	41.4000	6624	37.1000	5936
9	41.3875	6622	37.0875	5934
10	41.3750	6620	37.0750	5932
11	41.3625	6618	37.0625	5930
12	41.3500	6616	37.0500	5928
13	41.3375	6614	37.0375	5926
14	41.3250	6612	37.0250	5924
15	41.3125	6610	37.0125	5922

Table 7. Spain CT–1 Base Set Frequency

Channel Number	Tx Channel Frequency (MHz)	Tx Counter Value (Ref. Freq. = 5.00 kHz)	f_{in}–R Input Frequency (MHz) [1st IF = 10.695 MHz]	Rx Counter Value (Ref. Freq. = 5.00 kHz)
1	31.0250	6205	29.2300	5846
2	31.0500	6210	29.2550	5851
3	31.0750	6215	29.2800	5856
4	31.1000	6220	29.3050	5861
5	31.1250	6225	29.3300	5866
6	31.1500	6230	29.3550	5871
7	31.1750	6235	29.3800	5876
8	31.2000	6240	29.4050	5881
9	31.2500	6250	29.4550	5891
10	31.2750	6255	29.4800	5896
11	31.3000	6260	29.5050	5901
12	31.3250	6265	29.5300	5906

Table 8. Spain CT–1 Handset Frequency

Channel Number	Tx Channel Frequency (MHz)	Tx Counter Value (Ref. Freq. = 5.00 kHz)	f_{in}–R Input Frequency (MHz) [1st IF = 10.7 MHz]	Rx Counter Value (Ref. Freq. = 5.00 kHz)
1	39.9250	7985	20.3300	4066
2	39.9500	7990	20.3550	4071
3	39.9750	7995	20.3800	4076
4	40.0000	8000	20.4050	4081
5	40.0250	8005	20.4300	4086
6	40.0500	8010	20.4550	4091
7	40.0750	8015	20.4800	4096
8	40.1000	8020	20.5050	4101
9	40.1500	8030	20.5550	4111
10	40.1750	8035	20.5800	4116
11	40.2000	8040	20.6050	4121
12	40.2250	8045	20.6300	4126

Table 9. New Zealand CT–1 Base Set Frequency

Channel Number	Tx Channel Frequency (MHz)	Tx Counter Value	f_{in}–R Input Frequency (MHz) [1st IF = 10.7 MHz]	Rx Counter Value (Ref. Freq. = 6.25 kHz)
1	1.7820	1782	29.7625	4762
2	1.7620	1762	29.7500	4760
3	1.7420	1742	29.7375	4758
4	1.7220	1722	29.7250	4756
5	1.7020	1702	29.7125	4754
6	34.3500	5496	29.7000	4752
7	34.3625	5498	29.6875	4750
8	34.3750	5500	29.6750	4748
9	34.3875	5502	29.6625	4746
10	34.4000	5504	29.6500	4744

Ref Freq = 1.0 kHz (Tx Counter Value)

Ref Freq = 6.25 kHz (Tx Counter Value)

Table 10. New Zealand CT–1 Handset Frequency

Channel Number	Tx Channel Frequency (MHz)	Tx Counter Value (Ref. Freq. = 6.25 kHz)	f_{in}–R Input Frequency (MHz)	Rx Counter Value
1	40.4625	6474	2.2370	2237
2	40.4500	6472	2.2170	2217
3	40.4375	6470	2.1970	2197
4	40.4250	6468	2.1770	2177
5	40.4125	6466	2.1570	2157
6	40.4000	6464	23.6500	3784
7	40.3875	6462	23.6625	3786
8	40.3750	6460	23.6750	3788
9	40.3625	6458	23.6875	3790
10	40.3500	6456	23.7000	3792

Ref Freq = 455 kHz (f_{in}–R Input Frequency)

Ref Freq = 1.0 kHz (Rx Counter Value)

Ref Freq = 10.7 kHz (f_{in}–R Input Frequency)

Ref Freq = 6.25 kHz (Rx Counter Value)

Table 11. Australia CT–1 Base Set Frequency

Channel Number	Tx Channel Frequency (MHz)	Tx Counter Value (Ref. Freq. = 5.00 kHz)	f_{in}–R Input Frequency (MHz) [1st IF = 10.695 MHz]	Rx Counter Value (Ref. Freq. = 5.00 kHz)
1	30.0750	6015	29.0800	5816
2	30.1250	6025	29.1300	5826
3	30.1750	6035	29.1800	5836
4	30.2250	6045	29.2300	5846
5	30.2750	6055	29.2800	5856
6	30.1000	6020	29.1050	5821
7	30.1500	6030	29.1550	5831
8	30.2000	6040	29.2050	5841
9	30.2500	6050	29.2550	5851
10	30.3000	6060	29.3050	5861

Table 12. Australia CT–1 Handset Frequency

Channel Number	Tx Channel Frequency (MHz)	Tx Counter Value (Ref. Freq. = 5.00 kHz)	f_{in}–R Input Frequency (MHz) [1st IF = 10.7 MHz]	Rx Counter Value (Ref. Freq. = 5.00 kHz)
1	39.7750	7955	19.3800	3876
2	39.8250	7965	19.4300	3886
3	39.8750	7975	19.4800	3896
4	39.9250	7985	19.5300	3906
5	39.9750	7995	19.5800	3916
6	39.8000	7960	19.4050	3881
7	39.8500	7970	19.4550	3891
8	39.9000	7980	19.5050	3901
9	39.9500	7990	19.5550	3911
10	40.0000	8000	19.6050	3921

Table 13. U.K. CT–1 Base Set Frequency

Channel Number	Tx Channel Frequency (MHz)	Tx Counter Value (Ref. Freq. = 1.00 kHz)	f_{in}–R Input Frequency (MHz) [1st IF = 10.7 MHz]	Rx Counter Value (Ref. Freq. = 6.25 kHz)
1	1.6420	1642	36.75625	5881
2	1.6620	1662	36.76875	5883
3	1.6820	1682	36.78125	5885
4	1.7020	1702	36.79375	5887
5	1.7220	1722	36.80625	5889
6	1.7420	1742	36.81875	5891
7	1.7620	1762	36.83125	5893
8	1.7820	1782	36.84375	5895

Table 14. U.K. CT–1 Handset Frequency

Channel Number	Tx Channel Frequency (MHz)	Tx Counter Value (Ref. Freq. = 6.25 kHz)	f_{in}–R Input Frequency (MHz) [1st IF = 455 kHz]	Rx Counter Value (Ref. Freq. = 1.00 kHz)
1	47.45625	7593	2.097	2097
2	47.46875	7595	2.117	2117
3	47.48125	7597	2.137	2137
4	47.49375	7599	2.157	2157
5	47.50625	7601	2.177	2177
6	47.51875	7603	2.197	2197
7	47.53125	7605	2.217	2217
8	47.54375	7607	2.237	2237

Table 15. U.S.A. (10 Channels) CT–1 Base Set Frequency

Channel Number	Tx Channel Frequency (MHz)	Tx Counter Value (Ref. Freq. = 5.00 kHz)	f_{in}–R Input Frequency (MHz) [1st IF = 10.695 MHz]	Rx Counter Value (Ref. Freq. = 5.00 kHz)
1	46.610	9322	38.975	7795
2	46.630	9326	38.150	7830
3	46.670	9334	38.165	7833
4	46.710	9342	39.075	7815
5	46.730	9346	39.180	7836
6	46.770	9354	39.135	7827
7	46.830	9366	39.195	7839
8	46.870	9374	39.235	7847
9	46.930	9386	39.295	7859
10	46.970	9394	39.275	7855

Table 16. U.S.A. (10 Channels) CT–1 Handset Frequency

Channel Number	Tx Channel Frequency (MHz)	Tx Counter Value (Ref. Freq. = 5.00 kHz)	f_{in}–R Input Frequency (MHz) [1st IF = 10.7 MHz]	Rx Counter Value (Ref. Freq. = 5.00 kHz)
1	49.670	9934	35.915	7183
2	49.845	9969	35.935	7187
3	49.860	9972	35.975	7195
4	49.770	9954	36.015	7203
5	49.875	9975	36.035	7207
6	49.830	9966	36.075	7215
7	49.890	9978	36.135	7227
8	49.930	9986	36.175	7235
9	49.990	9998	36.235	7247
10	49.970	9994	36.275	7255

Table 17. U.S.A. (25 Channels) CT–1 Base Set Frequency

Channel Number	Tx Channel Frequency (MHz)	Tx Counter Value (Ref. Freq. = 5.00 kHz)	f_{in}–R Input Frequency (MHz) [1st IF = 10.7 MHz]	Rx Counter Value (Ref. Freq. = 5.00 kHz)
1	43.72	8744	38.06	7612
2	43.74	8748	38.14	7628
3	43.82	8764	38.16	7632
4	43.84	8768	38.22	7644
5	43.92	8784	38.32	7664
6	43.96	8788	38.38	7676
7	44.12	8824	38.40	7680
8	44.16	8832	38.46	7692
9	44.18	8836	38.50	7700
10	44.20	8840	38.54	7708
11	44.32	8864	38.58	7716
12	44.36	8872	38.66	7732
13	44.40	8880	38.70	7740
14	44.46	8892	38.76	7752
15	44.48	8896	38.80	7760
16	46.61	9322	38.97	7794
17	46.63	9326	39.145	7829
18	46.67	9334	39.16	7832
19	46.71	9342	39.07	7814
20	46.73	9346	39.175	7835
21	46.77	9354	39.13	7826
22	46.83	9366	39.19	7838
23	46.87	9374	39.23	7846
24	46.93	9386	39.29	7858
25	46.97	9394	39.27	7854

Table 18. U.S.A. (25 Channels) CT–1 Handset Frequency

Channel Number	Tx Channel Frequency (MHz)	Tx Counter Value (Ref. Freq. = 5.00 kHz)	f_{in}–R Input Frequency (MHz) [1st IF = 10.7 MHz]	Rx Counter Value (Ref. Freq. = 5.00 kHz)
1	48.76	9752	33.02	6604
2	48.84	9768	33.04	6608
3	48.86	9772	33.12	6624
4	48.92	9748	33.14	6628
5	49.02	9804	33.22	6644
6	49.08	9816	33.26	6652
7	49.10	9820	33.42	6684
8	49.16	9832	33.46	6692
9	49.20	9840	33.48	6696
10	49.24	9848	33.50	6700
11	49.28	9856	33.62	6724
12	49.36	9872	33.66	6732
13	49.40	9880	33.70	6740
14	49.46	9892	33.76	6752
15	49.50	9900	33.78	6756
16	49.67	9934	33.91	7182
17	49.845	9969	33.93	7186
18	49.86	9972	33.97	7194
19	49.77	9954	36.01	7202
20	49.875	9975	36.03	7206
21	49.83	9966	36.07	7214
22	49.89	9978	36.13	7226
23	49.93	9986	36.17	7234
24	49.99	9998	36.23	7246
25	49.97	9994	36.27	7254

Table 19. Korea CT–1 Base Set Frequency

Channel Number	Tx Channel Frequency (MHz)	Tx Counter Value (Ref. Freq. = 5.00 kHz)	f_{in}–R Input Frequency (MHz) [1st IF = 10.695 MHz]	Rx Counter Value (Ref. Freq. = 5.00 kHz)
1	46.610	9322	38.975	7795
2	46.630	9326	38.150	7830
3	46.670	9334	38.165	7833
4	46.710	9342	39.075	7815
5	46.730	9346	39.180	7836
6	46.770	9354	39.135	7827
7	46.830	9366	39.195	7839
8	46.870	9374	39.235	7847
9	46.930	9386	39.295	7859
10	46.970	9394	39.275	7855
11	46.510	9302	39.000	7800
12	46.530	9306	39.015	7803
13	46.550	9310	39.030	7806
14	46.570	9314	39.045	7809
15	46.590	9318	39.060	7812

Table 20. Korea CT–1 Handset Frequency

Channel Number	Tx Channel Frequency (MHz)	Tx Counter Value (Ref. Freq. = 5.00 kHz)	f_{in}–R Input Frequency (MHz) [1st IF = 10.7 MHz]	Rx Counter Value (Ref. Freq. = 5.00 kHz)
1	49.670	9934	35.915	7183
2	49.845	9969	35.935	7187
3	49.860	9972	35.975	7195
4	49.770	9954	36.015	7203
5	49.875	9975	36.035	7207
6	49.830	9966	36.075	7215
7	49.890	9978	36.135	7227
8	49.930	9986	36.175	7235
9	49.990	9998	36.235	7247
10	49.970	9994	36.275	7255
11	49.695	9939	35.815	7163
12	49.710	9942	35.835	7167
13	49.725	9945	35.855	7171
14	49.740	9948	35.875	7175
15	49.755	9951	35.895	7179

Table 21. China CT–1 Base Set Frequency

Channel Number	Tx Channel Frequency (MHz)	Tx Counter Value (Ref. Freq. = 5.00 kHz)	f_{in}–R Input Frequency (MHz) [1st IF = 10.7 MHz]	Rx Counter Value (Ref. Freq. = 5.00 kHz)
1	45.250	9050	37.550	7510
2	45.275	9055	37.575	7515
3	45.300	9060	37.600	7520
4	45.325	9065	37.625	7525
5	45.350	9070	37.650	7530
6	45.375	9075	37.675	7535
7	45.400	9080	37.700	7540
8	45.425	9085	37.725	7545
9	45.450	9090	37.750	7550
10	45.475	9095	37.775	7555

Table 22. China CT–1 Handset Frequency

Channel Number	Tx Channel Frequency (MHz)	Tx Counter Value (Ref. Freq. = 5.00 kHz)	f_{in}–R Input Frequency (MHz) [1st IF = 10.7 MHz]	Rx Counter Value (Ref. Freq. = 5.00 kHz)
1	48.250	9650	34.550	6910
2	48.275	9655	34.575	6915
3	48.300	9660	34.600	6920
4	48.325	9665	34.625	6925
5	48.350	9670	34.650	6930
6	48.375	9675	34.675	6935
7	48.400	9680	34.700	6940
8	48.425	9685	34.725	6945
9	48.450	9690	34.750	6950
10	48.475	9695	34.775	6955

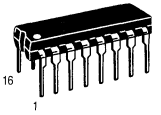
2

MC145165

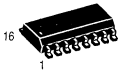
Advance Information

Low-Voltage 60 MHz Universal Programmable Dual PLL Frequency Synthesizer

CMOS



P SUFFIX
PLASTIC DIP
CASE 648



D SUFFIX
SOG PACKAGE
CASE 751B

ORDERING INFORMATION

MC145165P	Plastic DIP
MC145165D	SOG Package

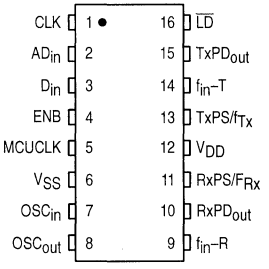
The MC145165 is a low–voltage dual phase–locked loop (PLL) frequency synthesizer especially designed for CT–1 cordless phone applications worldwide. This frequency synthesizer is also for any product with a frequency operation at 60 MHz or below.

This chip is suitable for any portable RF products which use two 1.2 V chargeable Ni–Cd batteries. The feature of low operating voltage can reduce the current consumption and the cost of the portable RF products by reducing the number of batteries used.

The device features fully programmable receive, transmit, reference, and auxiliary reference counters accessed through an MCU serial interface. This feature allows this device to operate in any CT–1 cordless phone application. The device consists of two independent phase detectors for transmit and receive loops. A common reference oscillator, driving two independent reference frequency counters, provides independent reference frequencies for transmit and receive loops. The auxiliary reference counter allows the user to select an additional reference frequency for receive and transmit loops if required. All of the functions and features of the MC145165 are fully compatible with the MC145162.

- Operating Voltage Range: 1.8 to 3.6 V
- Operating Temperature Range: – 40 to + 75°C
- Operating Power Consumption: 1.5 mA @ 1.8 V
- Maximum Operating Frequency: 60 MHz
- Minimum Input Sensitivity: 60 MHz @ 200 mV p–p, V_{DD} = 1.8 V
- Three or Four Pins Used for Serial MCU Interface
- Built–In MCU Clock Output with Frequency of Reference Oscillator ÷ 3/÷ 4
- Power Saving Mode Controlled by MCU
- Lock Detect Signal
- On–Chip Reference Oscillator Supports External Crystals to 16.0 MHz
- Reference Frequency Counter Division Range: 16 to 4095
- Auxiliary Reference Frequency Counter Division Range: 16 to 16,383
- Transmit Counter Division Range: 16 to 65,535
- Receive Counter Division Range: 16 to 65,535

PIN ASSIGNMENT



This document contains information on a new product. Specifications and information herein are subject to change without notice.

REV 0
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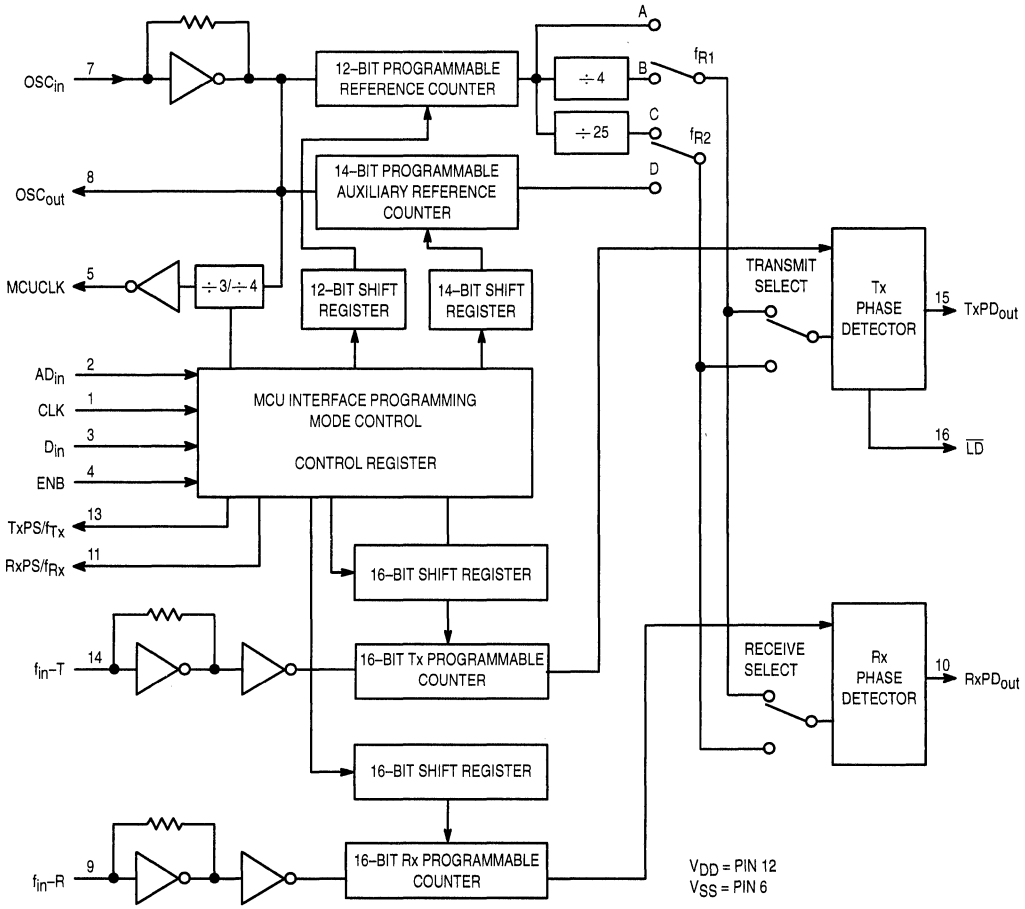
BLOCK DIAGRAM



MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Rating	Value	Unit
V_{DD}	DC Supply Voltage	– 0.5 to + 3.6	V
V_{in}	Input Voltage, All Inputs	– 0.5 to V_{DD} + 0.5	V
I_{in}, I_{out}	DC Current Drain Per Pin	10	mA
I_{DD}, I_{SS}	DC Current Drain V_{DD} or V_{SS} Pins	30	mA
T_{stg}	Storage Temperature Range	– 65 to + 150	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Descriptions section.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused pins must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

2

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS}, T_A = 25°C)

Symbol	Characteristic	V_{DD}	Guaranteed Limit		Unit
			Min	Max	
V_{DD}	Power Supply Voltage Range	—	1.8	3.6	V
V_{OL}	Output Voltage 0 Level (I_{out} = 0)	1.8	—	0.1	V
		3.6	—	0.1	
V_{OH}	(V_{in} = V_{DD} or 0) 1 Level	1.8	1.7	—	
		3.6	3.5	—	
V_{IL}	Input Voltage 0 Level (V_{out} = 0.5 V or V_{DD} – 0.5 V)	1.8	—	0.4	V
		3.6	—	0.6	
V_{IH}	1 Level	1.8	1.4	—	
		3.6	3.0	—	
I_{OH}	Output Current (V_{out} = 1.4 V) Source	1.8	– 0.18	—	mA
	(V_{out} = 3.0 V)	3.6	– 0.55	—	
I_{OL}	(V_{out} = 0.4 V) Sink	1.8	0.18	—	
	(V_{out} = 0.6 V)	3.6	0.55	—	
I_{IL}	Input Current (V_{in} = 0) OSC_{in}, f_{in}–T, f_{in}–R	1.8	—	– 30	µA
		3.6	—	– 66	
	AD_{in}, CLK, D_{in}, ENB	1.8	—	– 1.0	
		3.6	—	– 1.0	
I_{IH}	(V_{in} = V_{DD} – 0.5) OSC_{in}, f_{in}–T, f_{in}–R	1.8	—	30	
		3.6	—	66	
	AD_{in}, CLK, D_{in}, ENB	1.8	—	5.0	
		3.6	—	5.0	
I_{OZ}	Three–State Leakage Current (V_{out} = 0 V or 5.5 V)	3.6	—	± 100	nA
C_{in}	Input Capacitance	—	—	8.0	pF
C_{out}	Output Capacitance	—	—	8.0	pF
$I_{DD(stdby)}$	Standby Current (All Counters are in Power–Down Mode with Oscillator On)	1.8	—	0.2	mA
		3.6	—	0.6	
I_{DD}	Operating Current (200 mV_{p-p} input at f_{in}–T = 60 MHz and f_{in}–R = 60 MHz, OSC = 10.24 MHz)	1.8	—	1.5	mA
		3.6	—	5.5	

SWITCHING CHARACTERISTICS (T_A = 25°C, C_L = 50 pF)

Symbol	Characteristic		Figure No.	V_{DD}	Guaranteed Limit		Unit
					Min	Max	
t_{TLH}	Output Rise Time		1	1.8 – 3.6	—	200	ns
t_{THL}	Output Fall Time		1	1.8 – 3.6	—	200	ns
t_r, t_f	Input Rise and Fall Time	OSC_{in}	2	1.8 3.6	— —	6.0 5.0	µs
t_w	Input Pulse Width	CLK and ENB	3	1.8 – 3.6	1	—	µs
f_{max}	Input Sine Wave Frequency @ 200 mV p–p	OSC_{in} f_{in}–R, f_{in}–T		1.8 – 3.6 1.8 – 3.6	— —	16 60	MHz
t_{su1}	Setup Time	DATA to CLK	5	1.8 – 3.6	100	—	ns
t_{su2}	Setup Time	CLK to ENB	5	1.8 – 3.6	200	—	ns
t_{su3}	Setup Time	ENB to CLK	4	1.8 – 3.6	100	—	ns
t_{h1}	Hold Time	CLK to DATA	5	1.8 – 3.6	100	—	ns
t_{h2}	Hold Time	ENB to CLK	4	1.8 – 3.6	900	—	ns
t_{rec}	Recovery Time	ENB to CLK	5	1.8 – 3.6	100	—	ns

SWITCHING WAVEFORMS

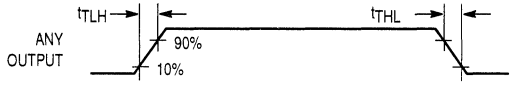


Figure 1.

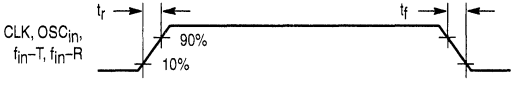


Figure 2.

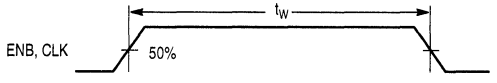


Figure 3.

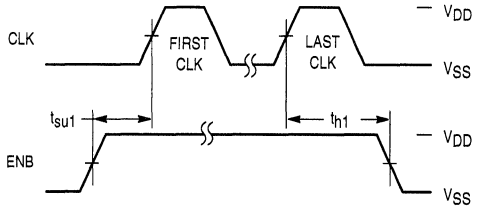


Figure 4. ENB High During Serial Transfer

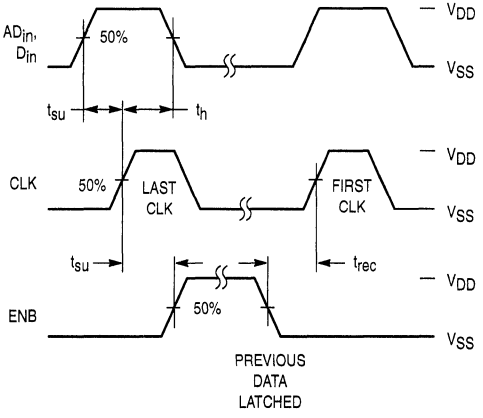


Figure 5. ENB Low During Serial Transfer

PIN DESCRIPTIONS

INPUT PINS

OSC_{in} /OSC_{out}
Reference Oscillator Input/Output (Pins 7, 8)

These pins form a reference oscillator when connected to an external parallel–resonant crystal. Figure 6 shows the relationship of different crystal frequencies and reference frequencies for cordless phone applications in various countries. OSC_{in} may also serve as input for an externally generated reference signal which is typically ac coupled.

MCUCLK
System Clock (Pin 5)

This output pin provides a signal of the crystal frequency (OSC_{out}) divided by 3 or 4 that is controlled by a bit in the control register.

This signal can be a clock source for the MCU or other system clocks.

AD_{in}, D_{in}, CLK, ENB
Auxiliary Data In, Data In, Clock, Enable (Pins 2, 3, 1, 4)

These four pins provide an MCU serial interface for programming the reference counter, the transmit–channel counter, and the receive–channel counter. They also provide various controls of the PLL including the power saving mode and the programming format.

$TxPS/f_{Tx}$, $RxPS/f_{Rx}$
Transmit Power Save, Receive Power Save (Pins 13, 11)

For a normal application, these output pins provide the status of the internal power saving mode operation. If the transmit–channels counter circuitry is in power down mode, $TxPS/f_{Tx}$ outputs a high state. If the receive–channels counter circuitry is in power down mode, $RxPS/f_{Rx}$ is set high. These outputs can be applied for controlling the external power switch for the transmitter and the receiver to save MCU control pins.

In the Tx/Rx channel counter test mode, the $TxPS/f_{Tx}$ and $RxPS/f_{Rx}$ pins output the divided value of the transmit channel counter (f_{Tx}) and the receive channel counter (f_{Rx}), respectively. This test mode operation is controlled by the control register. Details of the counter test mode are in the **Tx/Rx Channel Counter Test** section of this data sheet.

f_{in}–T/f_{in}–R
Transmit/Receive Counter Inputs (Pins 14, 9)

f_{in}–T and f_{in}–R are inputs to the transmit and the receive counters, respectively. These signals are typically driven from the loop VCO and ac coupled. The minimum input signal level is 200 mV p–p @ 60.0 MHz.

OUTPUT PINS

$TxPD_{out}$/$RxPD_{out}$
Transmit/Receive Phase Detector Outputs (Pins 15, 10)

These are three–state outputs of the transmit and receive phase detectors for use as loop–error signals (see Figure 7 for phase detector output waveforms). Phase detector gain is $V_{DD}/4\ \pi$ volts per radian.

Frequency $f_V > f_R$ or f_V leading: output = negative pulse.
Frequency $f_V < f_R$ or f_V lagging: output = positive pulse.
Frequency $f_V = f_R$ and phase coincidence: output = high–impedance state.
NOTE: f_R is the divided–down reference frequency at the phase detector input and f_V is the divided–down VCO frequency at the phase detector input.

$\overline{LD}$
Lock Detect (Pin 16)

The lock detect signal is associated with the transmit loop. The output at a high level indicates an out–of–lock condition (see Figure 7 for the $\overline{LD}$ output waveform).

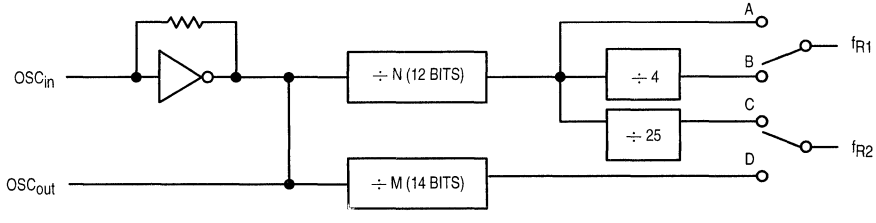
POWER SUPPLY

V_{DD}
Positive Power Supply (Pin 12)

V_{DD} is the most positive power supply potential ranging from 1.8 to 3.6 V with respect to V_{SS}.

V_{SS}
Negative Power Supply (Pin 6)

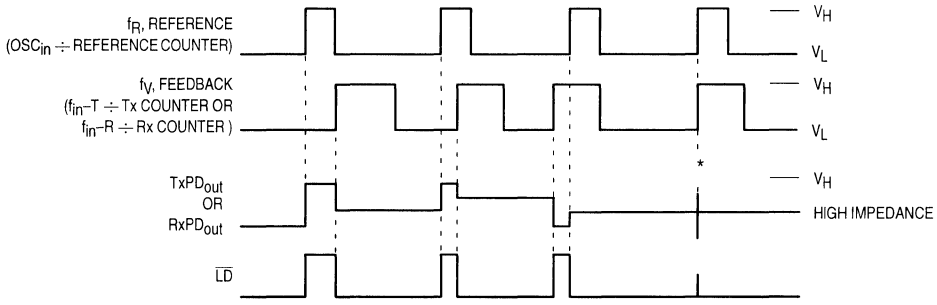
V_{SS} is the most negative supply potential and is usually connected to ground.



Reference Frequency vs Crystal Frequency

Crystal	÷ N Value	f_{R1} B	f_{R2} C
11.150 MHz	446	6.25 kHz	1.0 kHz
11.150 MHz	223	12.5 kHz	
10.240 MHz	512	5.0 kHz	
12.000 MHz	600	5.0 kHz	

Figure 6. Reference Frequencies for Cordless Phone Applications of Various Countries



V_H = High voltage level.
V_L = Low voltage level.
*At this point, when both f_R and f_V are in phase, the output is forced to near mid supply.

NOTE: The $TxPD_{out}$ and $RxPD_{out}$ generate error pulses during out–of–lock conditions. When locked in phase and frequency, the output is high impedance and the voltage at that pin is determined by the low–pass filter capacitor.

Figure 7. Phase Detector/Lock Detector Output Waveforms

MCU PROGRAMMING SCHEME

The MCU programming scheme is defined in two formats controlled by the ENB input. If the enable signal is high during the serial data transfer, control register/reference frequency programming is selected. If the ENB is low, programming of the transmit and receive counters is selected. During programming of the transmit and receive counters, both AD_{in} and D_{in} pins can input the data to the transmit and receive counters. Both counters' data is clocked into the PLL internal shift register at the leading edge of the CLK signal. It is not necessary to reprogram the reference frequency counter/control register when using the enable signal to program the transmit/receive channels.

In programming the control register/reference frequency scheme, the most significant bit (MSB) of the programming word identifies whether the input data is the control word or the reference frequency data word. If the MSB is 1, the input data is the control word (Figure 8). Also see Figure 8 and Table 1 for control register and bit function. If the MSB is 0, the input data is the reference frequency (Figure 9).

The reference frequency data word is a 32–bit word containing the 12–bit reference frequency data, the 14–bit auxiliary reference frequency counter information, the reference frequency selection plus, the auxiliary reference frequency counter enable bit (Figure 9).

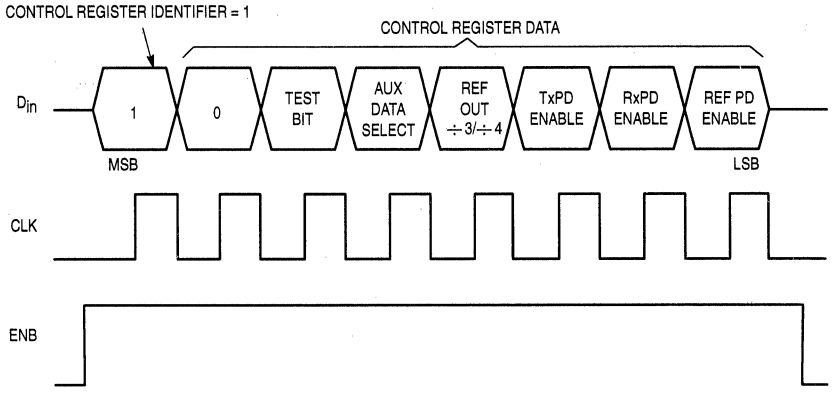
If the AUX REF ENB bit is high, the 14–bit auxiliary reference frequency counter provides an additional phase reference frequency output for the loops. If AUX REF ENB bit is low, the auxiliary reference frequency counter is forced into power–down mode for current saving. (Other power down modes are also provided through the control register per Table 2 and Figure 8.) At the falling edge of the ENB signal, the data is stored in the registers.

There are two interfacing schemes for the universal channel mode: the three–pin and the four–pin interfacing schemes. The three–pin interfacing scheme is suited for use with the MCU SPI (serial peripheral interface) (Figure 10), while the four–pin interfacing scheme is commonly used for general I/O port connection (Figure 11).

For the three–pin interfacing scheme, the auxiliary data select bit is set to 0. All 32 bits of data, which define both the 16–bit transmit counter and the 16–bit receive counter, latch into the PLL internal register through the data in pins at the leading edge of CLK. See Figures 12 and 13.

For the four–pin interfacing scheme, the auxiliary data select bit is set to 1. In this scheme, the 16–bit transmit counter's data enters into the AD_{in} pin at the same time as the 16–bit receive counter's data enters into the D_{in} pin. This simultaneous entry of the transmit and receive counters causes the programming period of the four–pin scheme to be half that of the three–pin scheme (see Figures 14 and 15).

While programming Tx/Rx Channel Counter, the ENB pin must be pulsed to provide falling edge to latch the shifted data after the rising edge of the last clock. Maximum data transfer rate is 500 kbps.



NOTE: ENB must be high during the serial transfer.

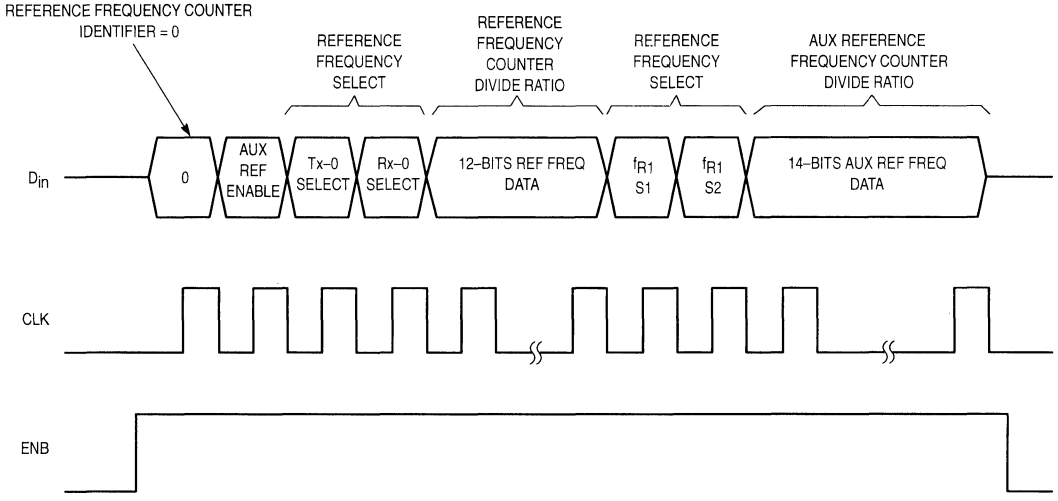
Figure 8. Programming Format of the Control Register

Table 1. Control Register Function Bits Description

Test Bit	Set to 1 for Tx/Rx channel counter test mode Set to 0 for normal application
Aux Data Select	Set to 1 for both AD_{in} and D_{in} pins inputting the transmit 16–bits data and receive 16–bits data respectively. Set to 0 for normal application interfacing with MCU serial peripheral interface. Does not use AD_{in} pin; tie AD_{in} to V_{SS}.
$REF_{out} \div 3/\div 4$	If set to 1, REF_{out} output frequency is equal to $OSC_{out} \div 3$. If set to 0, REF_{out} output is $OSC_{out} \div 4$.
TxPD Enable	If set to 1, the transmit counter, transmit phase detector, and the associated circuitry is in power–down mode. Tx PS/f_{Tx} is set "High".
RxPD Enable	If set to 1, the receive counter, receive phase detector, and the associated circuitry is in power–down mode. Rx PS/f_{Rx} is set "High".
Ref PD Enable	If set to 1, both 12–bit and 14–bit reference frequency counters are in power–down mode.

Table 2. Control Register Power Down Bits Function

TxPD Enable	RxPD Enable	REF PD Enable	Tx–Channel Counter	Rx–Channel Counter	Reference Frequency Counter
0	0	0	—	—	—
0	0	1	—	—	Power Down
0	1	0	—	Power Down	—
0	1	1	—	Power Down	Power Down
1	0	0	Power Down	—	—
1	0	1	Power Down	—	Power Down
1	1	0	Power Down	Power Down	—
1	1	1	Power Down	Power Down	Power Down



NOTE: ENB must be high during the serial transfer.

Figure 9. Programming Format of the Auxiliary/Reference Frequency Counters

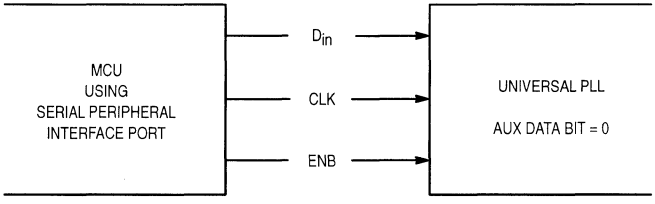


Figure 10. MCU Interface Using SPI

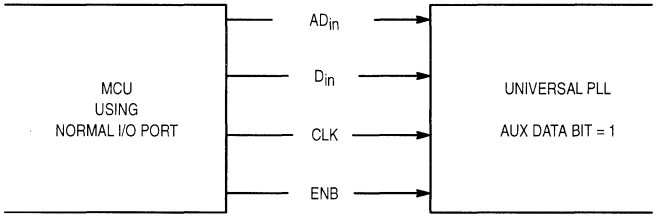
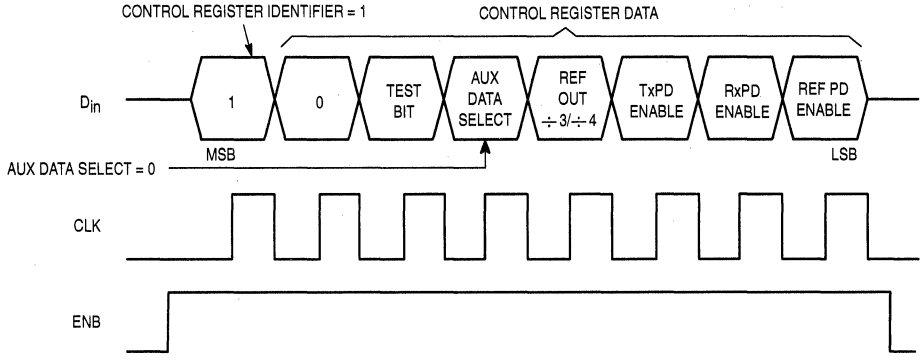
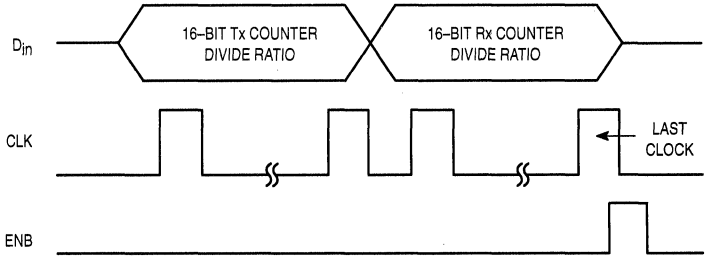


Figure 11. MCU Interface Using Normal I/O Ports with Both D_{in} and AD_{in} for Faster Programming Time



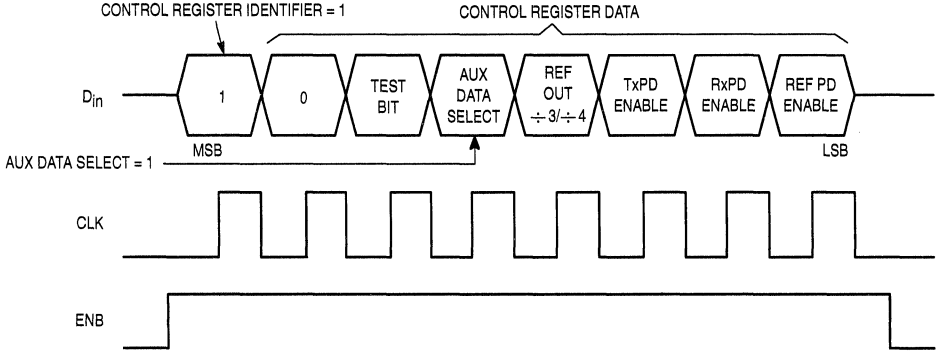
NOTE: ENB must be high during the serial transfer.

Figure 12. Programming Format for Control Register (3–Pin Interfacing Scheme)



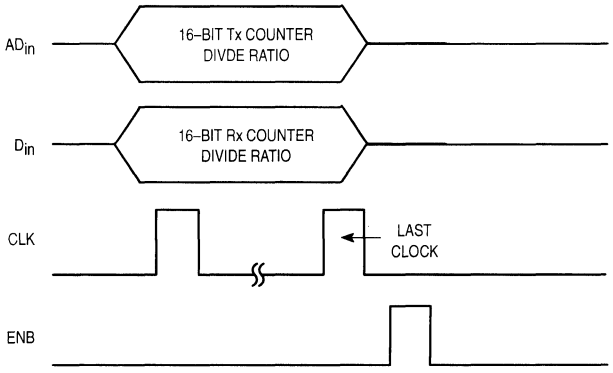
NOTE: ENB must be low during the serial transfer.

Figure 13. Programming Format for Transmit and Receive Counters (3–Pin Interfacing Scheme)



NOTE: ENB must be high during the serial transfer.

Figure 14. Programming Format for Control Register (4–Pin Interfacing Scheme)



NOTE: ENB must be low during the serial transfer.

Figure 15. Programming Format for Transmit and Receive Counters (4–Pin Interfacing Scheme)

Table 3. Global CT–1 Reference Frequency Setting vs Channel Frequencies

Country	Channels Frequency	f_{R1}	f_{R2}
U.S.A.	46/49 MHz (10, 15, 25 Channels)	5.0 kHz	—
France	26/41 MHz	6.25 kHz/12.5 kHz	—
Spain	31/41 MHz	5.0 kHz	—
Australia	30/39 MHz	5.0 kHz	—
U.K.	1.7/47 MHz	6.25 kHz	1.0 kHz
New Zealand	1.7/34/40 MHz	6.25 kHz	1.0 kHz

REFERENCE FREQUENCY SELECTION AND PROGRAMMING

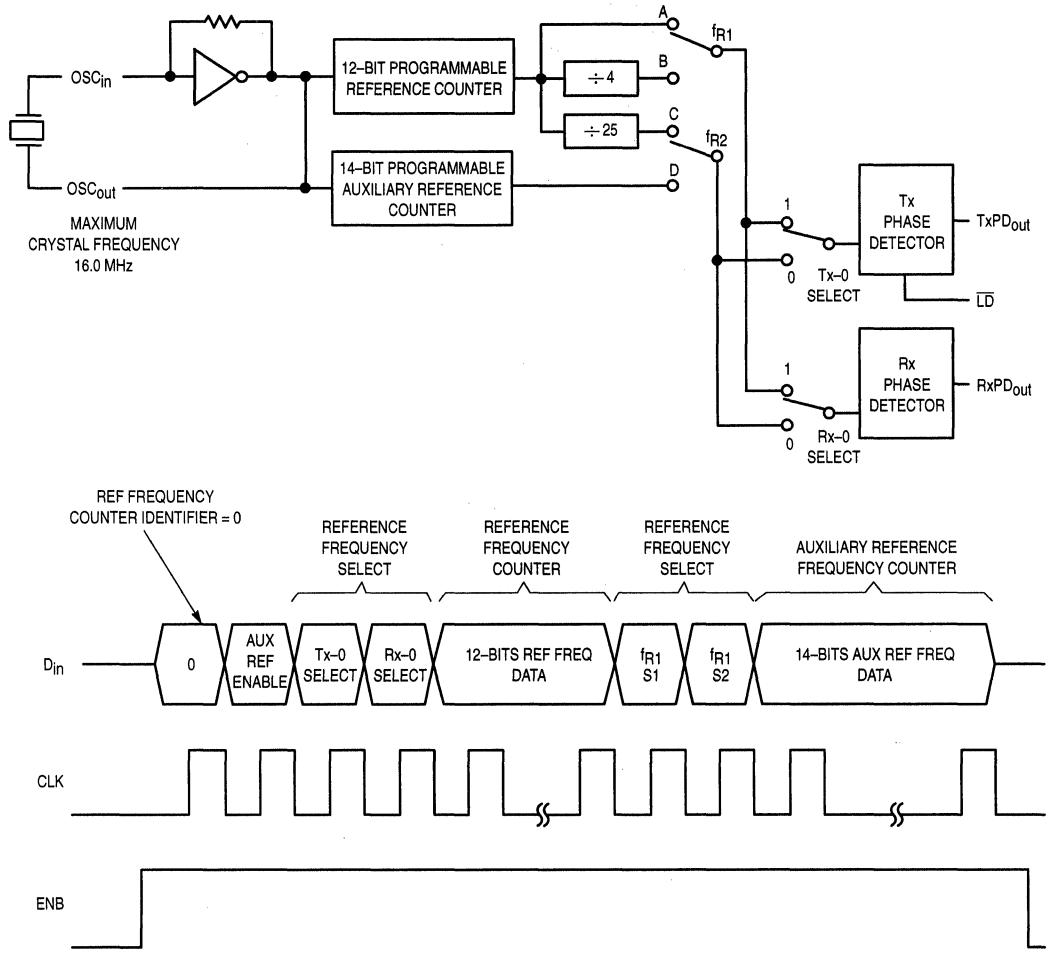
Figure 16 shows the bit function of the reference frequency programming word. The user can either select the "fixed" reference frequency for all channels accordingly or provide a specific reference frequency for a particular channel by using two reference frequency counters (e.g., for an application in France, the base set transmit channel common fixed reference frequency is 6.25 kHz or 12.5 kHz). (See Table 3 and Figure 6 for reference frequencies for various countries.) However, transmit channels 6, 8, and 14 can be set to 25 kHz, and channel 8 reference frequency can be set to 50 kHz. But this reference frequency may not be applied to the receiving side; therefore, the receiving side reference frequency must be generated by another reference frequency counter. The higher the reference frequency, the better the phase noise performance and faster the lock time, but the PLL consumes more current if both reference frequency counters are in operation.

In general, the 12–bit reference frequency counter plus the ÷ 4 and ÷ 25 module can offer all the reference frequencies for global CT–1 transmit and receive channel requirements. Users can select their own reference frequency by introducing the additional 14–bit auxiliary reference frequency counter.

Again, the 14–bit auxiliary reference frequency counter can be shut down by the auxiliary reference enable bit in the reference counter programming word by setting the bit to 0. At this state, the f_{R2} is automatically connected to point C (the ÷ 25 block output), and f_{R1} can be connected to point A or B by setting the f_{R1}–S1 and f_{R1}–S2 bits in the reference counter program word. The 14–bit auxiliary reference frequency counter data will be in "Don't Care" state.

If the 14–bit auxiliary reference frequency counter is enabled (auxiliary reference enable = 1), then f_{R2} is automatically connected to point D (14–bit counter output), and f_{R1} can be selected to connect to point A, B, or C, depending on the bit setting of f_{R1}–S1 and f_{R1}–S2.

Table 4 and Figure 16 describe the functions of the auxiliary reference enable bit and the f_{R1}–S1 and f_{R1}–S2 bits selection.



NOTE: ENB must be high during the serial transfer.

Figure 16. Reference Frequency Counter/Selection Programming Mode

Table 4. Bit Function and the Reference Frequency Selection Bit Setting of the Reference Frequency Counter Programming Word

AUX REF Enable	Auxiliary Reference Frequency Counter Mode	Module Select	f_{R1} S1	f_{R1} S2	f_{R1} Routing
0	14–Bit Auxiliary Reference Frequency Counter Disable	f_{R2} C	0	0	N/A
			0	1	f_{R1} A
			1	0	f_{R1} B
			1	1	N/A
1	14–Bit Auxiliary Reference Frequency Counter Enable	f_{R2} D	0	0	N/A
			0	1	f_{R1} A
			1	0	f_{R1} B
			1	1	f_{R1} C

N/A = Not Applicable

POWER SAVING OPERATION

This PLL has a programmable power–saving scheme. The transmit and receive counters and the reference frequency counter can be powered down individually by setting the TxPD enable, RxPD enable, and Ref PD enable bits of the control register. The functions of the power down control bits are explained in Table 2 and the programming format is in Figure 8.

The output pins TxPS/f_{Tx} and RxPS/f_{Rx} output the status of the internal power saving setting. If the bit TxPD enable is set "high" (transmit counter is set to power–down mode), then the TxPS/f_{Tx} pin will also output a "high" state. This TxPS/f_{Tx} output can control an external power switch to switch off the transmitter, as shown in Figure 17. This scheme can be applied to the RxPS/f_{Rx} output to control the receiver power saving operation as required.

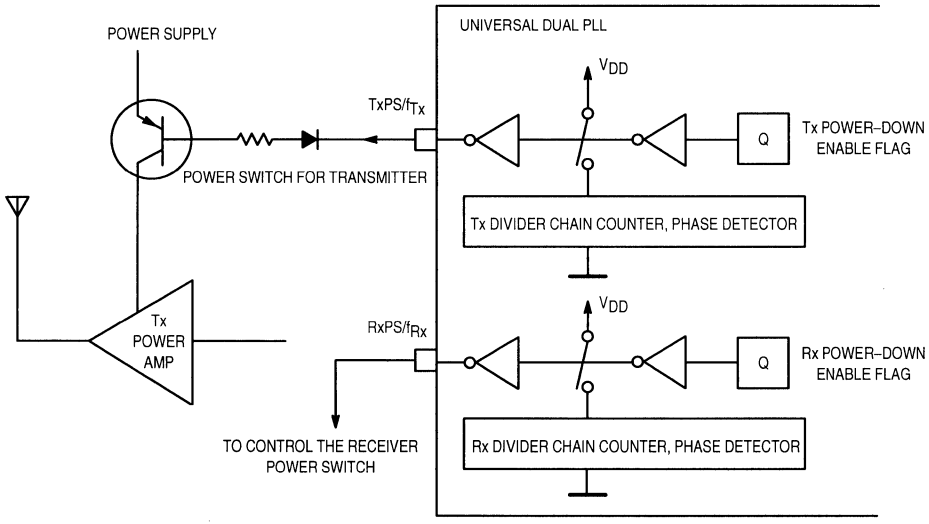


Figure 17. TxPS/f_{Tx} and RxPS/f_{Rx} Outputs to Control Power Switches of the Transmitter and the Receiver

Tx/Rx CHANNEL COUNTER TEST

In normal applications, the TxPS/f_{Tx} and the RxPS/f_{Rx} output pins indicate the power saving mode status. However, the user can examine the Tx and Rx channel counter outputs by setting the Test bit in the control register to 1. The final value of the transmit–channel counter and the receive–channel counter multiplex out to TxPS/f_{Tx} and RxPS/f_{Rx} respectively. The user can verify the divided–down output waveform associated with the RF input level in the PLL circuitry implementation (Figure 18).

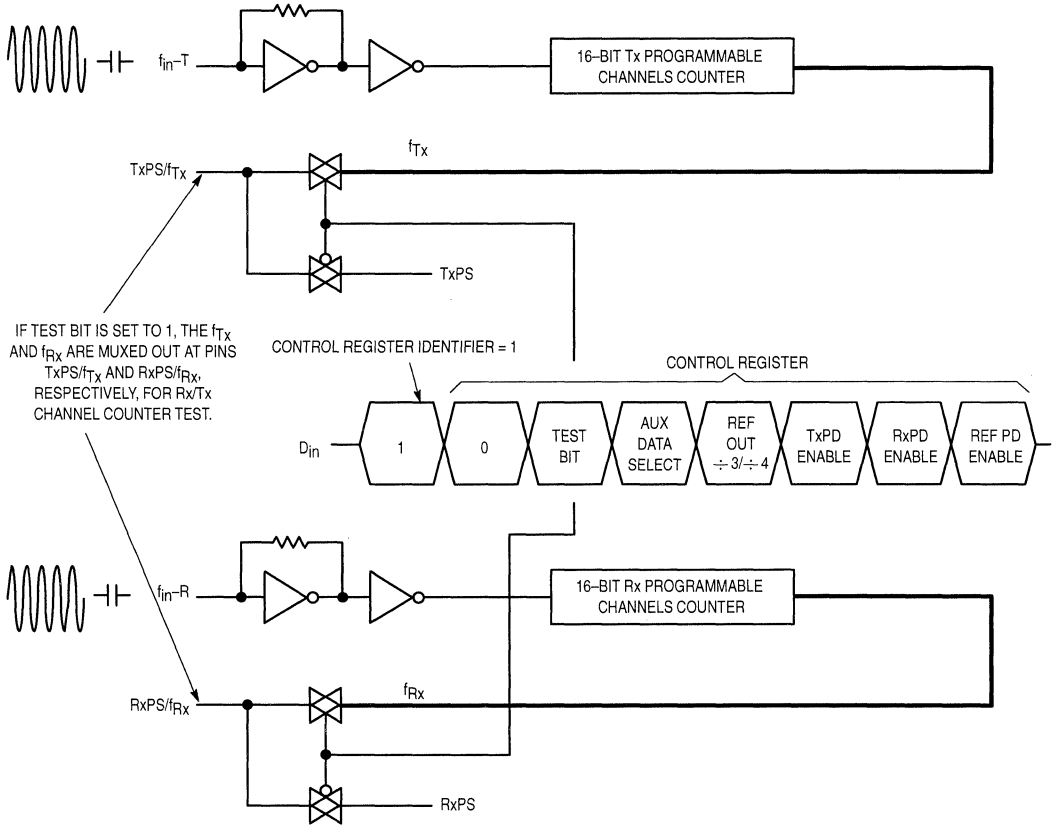


Figure 18. RF Buffer Sensitivity

Table 5. France CT–1 Base Set Frequency

Channel Number	Tx Channel Frequency (MHz)	Tx Counter Value (Ref. Freq. = 6.25 kHz)	f_{in}–R Input Frequency (MHz) [1st IF = 10.7 MHz]	Rx Counter Value (Ref. Freq. = 6.25 kHz)
1	26.4875	4238	30.7875	4926
2	26.4750	4236	30.7750	4924
3	26.4625	4234	30.7625	4922
4	26.4500	4232	30.7500	4920
5	26.4375	4230	30.7375	4918
6	26.4250	4228	30.7250	4916
7	26.4125	4226	30.7125	4914
8	26.4000	4224	30.7000	4912
9	26.3875	4222	30.6875	4910
10	26.3750	4220	30.6750	4908
11	26.3625	4218	30.6625	4906
12	26.3500	4216	30.6500	4904
13	26.3375	4214	30.6375	4902
14	26.3250	4212	30.6250	4900
15	26.3125	4210	30.6125	4898

Table 6. France CT–1 Handset Frequency

Channel Number	Tx Channel Frequency (MHz)	Tx Counter Value (Ref. Freq. = 6.25 kHz)	f_{in}–R Input Frequency (MHz) [1st IF = 10.7 MHz]	Rx Counter Value (Ref. Freq. = 6.25 kHz)
1	41.4875	6638	37.1875	5950
2	41.4750	6636	37.1750	5948
3	41.4625	6634	37.1625	5946
4	41.4500	6632	37.1500	5944
5	41.4375	6630	37.1375	5942
6	41.4250	6628	37.1250	5940
7	41.4125	6626	37.1125	5938
8	41.4000	6624	37.1000	5936
9	41.3875	6622	37.0875	5934
10	41.3750	6620	37.0750	5932
11	41.3625	6618	37.0625	5930
12	41.3500	6616	37.0500	5928
13	41.3375	6614	37.0375	5926
14	41.3250	6612	37.0250	5924
15	41.3125	6610	37.0125	5922

Table 7. Spain CT–1 Base Set Frequency

Channel Number	Tx Channel Frequency (MHz)	Tx Counter Value (Ref. Freq. = 5.00 kHz)	f_{in}–R Input Frequency (MHz) [1st IF = 10.695 MHz]	Rx Counter Value (Ref. Freq. = 5.00 kHz)
1	31.0250	6205	29.2300	5846
2	31.0500	6210	29.2550	5851
3	31.0750	6215	29.2800	5856
4	31.1000	6220	29.3050	5861
5	31.1250	6225	29.3300	5866
6	31.1500	6230	29.3550	5871
7	31.1750	6235	29.3800	5876
8	31.2000	6240	29.4050	5881
9	31.2500	6250	29.4550	5891
10	31.2750	6255	29.4800	5896
11	31.3000	6260	29.5050	5901
12	31.3250	6265	29.5300	5906

Table 8. Spain CT–1 Handset Frequency

Channel Number	Tx Channel Frequency (MHz)	Tx Counter Value (Ref. Freq. = 5.00 kHz)	f_{in}–R Input Frequency (MHz) [1st IF = 10.7 MHz]	Rx Counter Value (Ref. Freq. = 5.00 kHz)
1	39.9250	7985	20.3300	4066
2	39.9500	7990	20.3550	4071
3	39.9750	7995	20.3800	4076
4	40.0000	8000	20.4050	4081
5	40.0250	8005	20.4300	4086
6	40.0500	8010	20.4550	4091
7	40.0750	8015	20.4800	4096
8	40.1000	8020	20.5050	4101
9	40.1500	8030	20.5550	4111
10	40.1750	8035	20.5800	4116
11	40.2000	8040	20.6050	4121
12	40.2250	8045	20.6300	4126

Table 9. New Zealand CT–1 Base Set Frequency

Channel Number	Tx Channel Frequency (MHz)	Tx Counter Value	f_{in}–R Input Frequency (MHz) [1st IF = 10.7 MHz]	Rx Counter Value (Ref. Freq. = 6.25 kHz)
1	1.7820	1782	29.7625	4762
2	1.7620	1762	29.7500	4760
3	1.7420	1742	29.7375	4758
4	1.7220	1722	29.7250	4756
5	1.7020	1702	29.7125	4754
6	34.3500	5496	29.7000	4752
7	34.3625	5498	29.6875	4750
8	34.3750	5500	29.6750	4748
9	34.3875	5502	29.6625	4746
10	34.4000	5504	29.6500	4744

Ref Freq = 1.0 kHz (Tx Counter Value)

Ref Freq = 6.25 kHz (Tx Counter Value)

Table 10. New Zealand CT–1 Handset Frequency

Channel Number	Tx Channel Frequency (MHz)	Tx Counter Value (Ref. Freq. = 6.25 kHz)	f_{in}–R Input Frequency (MHz)	Rx Counter Value
1	40.4625	6474	2.2370	2237
2	40.4500	6472	2.2170	2217
3	40.4375	6470	2.1970	2197
4	40.4250	6468	2.1770	2177
5	40.4125	6466	2.1570	2157
6	40.4000	6464	23.6500	3784
7	40.3875	6462	23.6625	3786
8	40.3750	6460	23.6750	3788
9	40.3625	6458	23.6875	3790
10	40.3500	6456	23.7000	3792

Ref Freq = 455 kHz (f_{in}–R Input Frequency)

Ref Freq = 1.0 kHz (Rx Counter Value)

Ref Freq = 10.7 kHz (f_{in}–R Input Frequency)

Ref Freq = 6.25 kHz (Rx Counter Value)

Table 11. Australia CT–1 Base Set Frequency

Channel Number	Tx Channel Frequency (MHz)	Tx Counter Value (Ref. Freq. = 5.00 kHz)	f_{in}–R Input Frequency (MHz) [1st IF = 10.695 MHz]	Rx Counter Value (Ref. Freq. = 5.00 kHz)
1	30.0750	6015	29.0800	5816
2	30.1250	6025	29.1300	5826
3	30.1750	6035	29.1800	5836
4	30.2250	6045	29.2300	5846
5	30.2750	6055	29.2800	5856
6	30.1000	6020	29.1050	5821
7	30.1500	6030	29.1550	5831
8	30.2000	6040	29.2050	5841
9	30.2500	6050	29.2550	5851
10	30.3000	6060	29.3050	5861

Table 12. Australia CT–1 Handset Frequency

Channel Number	Tx Channel Frequency (MHz)	Tx Counter Value (Ref. Freq. = 5.00 kHz)	f_{in}–R Input Frequency (MHz) [1st IF = 10.7 MHz]	Rx Counter Value (Ref. Freq. = 5.00 kHz)
1	39.7750	7955	19.3800	3876
2	39.8250	7965	19.4300	3886
3	39.8750	7975	19.4800	3896
4	39.9250	7985	19.5300	3906
5	39.9750	7995	19.5800	3916
6	39.8000	7960	19.4050	3881
7	39.8500	7970	19.4550	3891
8	39.9000	7980	19.5050	3901
9	39.9500	7990	19.5550	3911
10	40.0000	8000	19.6050	3921

Table 13. U.K. CT–1 Base Set Frequency

Channel Number	Tx Channel Frequency (MHz)	Tx Counter Value (Ref. Freq. = 1.00 kHz)	f_{in}–R Input Frequency (MHz) [1st IF = 10.7 MHz]	Rx Counter Value (Ref. Freq. = 6.25 kHz)
1	1.6420	1642	36.75625	5881
2	1.6620	1662	36.76875	5883
3	1.6820	1682	36.78125	5885
4	1.7020	1702	36.79375	5887
5	1.7220	1722	36.80625	5889
6	1.7420	1742	36.81875	5891
7	1.7620	1762	36.83125	5893
8	1.7820	1782	36.84375	5895

Table 14. U.K. CT–1 Handset Frequency

Channel Number	Tx Channel Frequency (MHz)	Tx Counter Value (Ref. Freq. = 6.25 kHz)	f_{in}–R Input Frequency (MHz) [1st IF = 455 kHz]	Rx Counter Value (Ref. Freq. = 1.00 kHz)
1	47.45625	7593	2.097	2097
2	47.46875	7595	2.117	2117
3	47.48125	7597	2.137	2137
4	47.49375	7599	2.157	2157
5	47.50625	7601	2.177	2177
6	47.51875	7603	2.197	2197
7	47.53125	7605	2.217	2217
8	47.54375	7607	2.237	2237

Table 15. U.S.A. (10 Channels) CT–1 Base Set Frequency

Channel Number	Tx Channel Frequency (MHz)	Tx Counter Value (Ref. Freq. = 5.00 kHz)	f_{in}–R Input Frequency (MHz) [1st IF = 10.695 MHz]	Rx Counter Value (Ref. Freq. = 5.00 kHz)
1	46.610	9322	38.975	7795
2	46.630	9326	38.150	7830
3	46.670	9334	38.165	7833
4	46.710	9342	39.075	7815
5	46.730	9346	39.180	7836
6	46.770	9354	39.135	7827
7	46.830	9366	39.195	7839
8	46.870	9374	39.235	7847
9	46.930	9386	39.295	7859
10	46.970	9394	39.275	7855

Table 16. U.S.A. (10 Channels) CT–1 Handset Frequency

Channel Number	Tx Channel Frequency (MHz)	Tx Counter Value (Ref. Freq. = 5.00 kHz)	f_{in}–R Input Frequency (MHz) [1st IF = 10.7 MHz]	Rx Counter Value (Ref. Freq. = 5.00 kHz)
1	49.670	9934	35.915	7183
2	49.845	9969	35.935	7187
3	49.860	9972	35.975	7195
4	49.770	9954	36.015	7203
5	49.875	9975	36.035	7207
6	49.830	9966	36.075	7215
7	49.890	9978	36.135	7227
8	49.930	9986	36.175	7235
9	49.990	9998	36.235	7247
10	49.970	9994	36.275	7255

Table 17. U.S.A. (25 Channels) CT–1 Base Set Frequency

Channel Number	Tx Channel Frequency (MHz)	Tx Counter Value (Ref. Freq. = 5.00 kHz)	f_{in}–R Input Frequency (MHz) [1st IF = 10.7 MHz]	Rx Counter Value (Ref. Freq. = 5.00 kHz)
1	43.72	8744	38.06	7612
2	43.74	8748	38.14	7628
3	43.82	8764	38.16	7632
4	43.84	8768	38.22	7644
5	43.92	8784	38.32	7664
6	43.96	8788	38.38	7676
7	44.12	8824	38.40	7680
8	44.16	8832	38.46	7692
9	44.18	8836	38.50	7700
10	44.20	8840	38.54	7708
11	44.32	8864	38.58	7716
12	44.36	8872	38.66	7732
13	44.40	8880	38.70	7740
14	44.46	8892	38.76	7752
15	44.48	8896	38.80	7760
16	46.61	9322	38.97	7794
17	46.63	9326	39.145	7829
18	46.67	9334	39.16	7832
19	46.71	9342	39.07	7814
20	46.73	9346	39.175	7835
21	46.77	9354	39.13	7826
22	46.83	9366	39.19	7838
23	46.87	9374	39.23	7846
24	46.93	9386	39.29	7858
25	46.97	9394	39.27	7854

Table 18. U.S.A. (25 Channels) CT–1 Handset Frequency

Channel Number	Tx Channel Frequency (MHz)	Tx Counter Value (Ref. Freq. = 5.00 kHz)	f_{in}–R Input Frequency (MHz) [1st IF = 10.7 MHz]	Rx Counter Value (Ref. Freq. = 5.00 kHz)
1	48.76	9752	33.02	6604
2	48.84	9768	33.04	6608
3	48.86	9772	33.12	6624
4	48.92	9748	33.14	6628
5	49.02	9804	33.22	6644
6	49.08	9816	33.26	6652
7	49.10	9820	33.42	6684
8	49.16	9832	33.46	6692
9	49.20	9840	33.48	6696
10	49.24	9848	33.50	6700
11	49.28	9856	33.62	6724
12	49.36	9872	33.66	6732
13	49.40	9880	33.70	6740
14	49.46	9892	33.76	6752
15	49.50	9900	33.78	6756
16	49.67	9934	33.91	7182
17	49.845	9969	33.93	7186
18	49.86	9972	33.97	7194
19	49.77	9954	36.01	7202
20	49.875	9975	36.03	7206
21	49.83	9966	36.07	7214
22	49.89	9978	36.13	7226
23	49.93	9986	36.17	7234
24	49.99	9998	36.23	7246
25	49.97	9994	36.27	7254

Table 19. Korea CT–1 Base Set Frequency

Channel Number	Tx Channel Frequency (MHz)	Tx Counter Value (Ref. Freq. = 5.00 kHz)	f_{in}–R Input Frequency (MHz) [1st IF = 10.695 MHz]	Rx Counter Value (Ref. Freq. = 5.00 kHz)
1	46.610	9322	38.975	7795
2	46.630	9326	38.150	7830
3	46.670	9334	38.165	7833
4	46.710	9342	39.075	7815
5	46.730	9346	39.180	7836
6	46.770	9354	39.135	7827
7	46.830	9366	39.195	7839
8	46.870	9374	39.235	7847
9	46.930	9386	39.295	7859
10	46.970	9394	39.275	7855
11	46.510	9302	39.000	7800
12	46.530	9306	39.015	7803
13	46.550	9310	39.030	7806
14	46.570	9314	39.045	7809
15	46.590	9318	39.060	7812

Table 20. Korea CT–1 Handset Frequency

Channel Number	Tx Channel Frequency (MHz)	Tx Counter Value (Ref. Freq. = 5.00 kHz)	f_{in}–R Input Frequency (MHz) [1st IF = 10.7 MHz]	Rx Counter Value (Ref. Freq. = 5.00 kHz)
1	49.670	9934	35.915	7183
2	49.845	9969	35.935	7187
3	49.860	9972	35.975	7195
4	49.770	9954	36.015	7203
5	49.875	9975	36.035	7207
6	49.830	9966	36.075	7215
7	49.890	9978	36.135	7227
8	49.930	9986	36.175	7235
9	49.990	9998	36.235	7247
10	49.970	9994	36.275	7255
11	49.695	9939	35.815	7163
12	49.710	9942	35.835	7167
13	49.725	9945	35.855	7171
14	49.740	9948	35.875	7175
15	49.755	9951	35.895	7179

Table 21. China CT–1 Base Set Frequency

Channel Number	Tx Channel Frequency (MHz)	Tx Counter Value (Ref. Freq. = 5.00 kHz)	f_{in}–R Input Frequency (MHz) [1st IF = 10.7 MHz]	Rx Counter Value (Ref. Freq. = 5.00 kHz)
1	45.250	9050	37.550	7510
2	45.275	9055	37.575	7515
3	45.300	9060	37.600	7520
4	45.325	9065	37.625	7525
5	45.350	9070	37.650	7530
6	45.375	9075	37.675	7535
7	45.400	9080	37.700	7540
8	45.425	9085	37.725	7545
9	45.450	9090	37.750	7550
10	45.475	9095	37.775	7555

Table 22. China CT–1 Handset Frequency

Channel Number	Tx Channel Frequency (MHz)	Tx Counter Value (Ref. Freq. = 5.00 kHz)	f_{in}–R Input Frequency (MHz) [1st IF = 10.7 MHz]	Rx Counter Value (Ref. Freq. = 5.00 kHz)
1	48.250	9650	34.550	6910
2	48.275	9655	34.575	6915
3	48.300	9660	34.600	6920
4	48.325	9665	34.625	6925
5	48.350	9670	34.650	6930
6	48.375	9675	34.675	6935
7	48.400	9680	34.700	6940
8	48.425	9685	34.725	6945
9	48.450	9690	34.750	6950
10	48.475	9695	34.775	6955

MC145166
MC145167

Advance Information

Dual PLLs for 46/49 MHz Cordless Telephones

CMOS

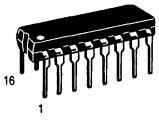
2

These devices are dual phase–locked loop (PLL) frequency synthesizers intended for use primarily in 46/49 MHz cordless phones with up to 10 channels. These parts contain two mask–programmable counter ROMs for receive and transmit loops with two independent phase detect circuits. A common reference oscillator and reference divider are shared by the receive and transmit circuits.

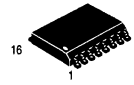
Frequency selection is accomplished via a 4–bit parallel input for the MC145166. The MC145167 utilizes a serial interface.

Other features include a lock detect circuit for the transmit loop, illegal code default, and a 5 kHz tone output.

- Synthesizes Up to Ten Channel Pairs
- Maximum Operating Frequency: 60 MHz @ V_{in} = 200 mV p–p
- Operating Temperature Range: – 40 to + 75°C
- Operating Voltage Range: 2.5 to 5.5 V
- On–Chip Oscillator Circuit Supports External Crystal
- Lock Detect Signal
- Operating Power Consumption: 3.0 mA @ 3.0 V
- Standby Mode for Power Savings: 1.5 mA @ 3.0 V



P SUFFIX
PLASTIC DIP
CASE 648



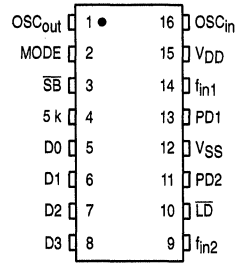
DW SUFFIX
SOG PACKAGE
CASE 751G

ORDERING INFORMATION

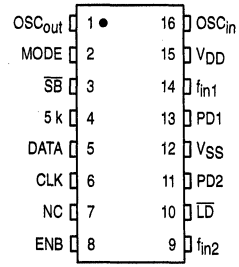
MC145166P	Plastic DIP
MC145166DW	SOG Package
MC145167P	Plastic DIP
MC145167DW	SOG Package

PIN ASSIGNMENTS

MC145166P
MC145166DW



MC145167P
MC145167DW

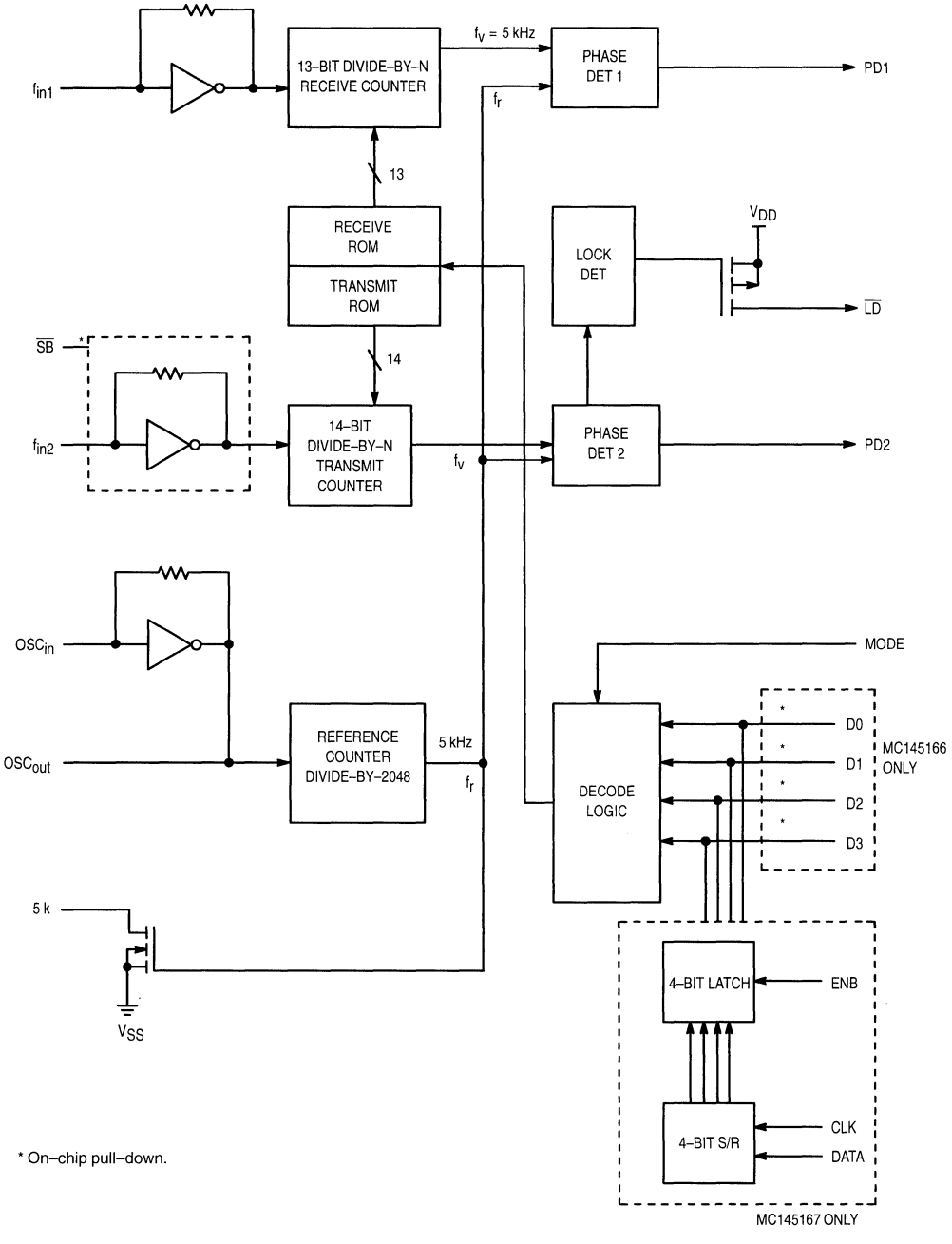


NC = NO CONNECTION

This document contains information on a new product. Specifications and information herein are subject to change without notice.

REV 1
8/95
Replaces MC145160/D

BLOCK DIAGRAM



* On–chip pull–down.

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Rating	Value	Unit
V_{DD}	DC Supply Voltage	– 0.5 to + 6.0	V
V_{in}	Input Voltage, All Inputs	– 0.5 to V_{DD} + 0.5	V
I_{in}, I_{out}	DC Current Drain Per Pin	10	mA
I_{DD}, I_{SS}	DC Current Drain V_{DD} or V_{SS} Pins	30	mA
T_{stg}	Storage Temperature Range	– 65 to + 150	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Descriptions section.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

2

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS}, T_A = 25°C)

Symbol	Characteristic		V_{DD}	Guaranteed Limit		Unit
				Min	Max	
V_{DD}	Power Supply Voltage Range		—	2.5	5.5	V
V_{OL}	Output Voltage (I_{out} = 0)	0 Level	2.5 5.5	— —	0.05 0.05	V
V_{OH}	(V_{in} = V_{DD} or 0)	1 Level	2.5 5.5	2.45 5.45	— —	
V_{IL}	Input Voltage (V_{out} = 0.5 V or V_{DD} – 0.5 V)	0 Level	2.5 5.5	— —	0.75 1.65	V
V_{IH}		1 Level	2.5 5.5	1.75 3.85	— —	
I_{OH}	Output Current (V_{out} = 2.2 V) (V_{out} = 5.0 V)	Source	2.5 5.5	– 0.18 – 0.55	— —	mA
I_{OL}	(V_{out} = 0.3 V) (V_{out} = 0.5 V)	Sink	2.5 5.5	0.18 0.55	— —	
I_{IL}	Input Current (V_{in} = 0)	OSC_{in}, f_{in1}, f_{in2}	2.5 5.5	— —	– 30 – 66	µA
		DATA, $\overline{SB}$, Mode	2.5 5.5	— —	– 0.05 – 0.11	
I_{IH}	(V_{in} = V_{DD} – 0.5)	OSC_{in}, f_{in1}, f_{in2}	2.5 5.5	— —	30 66	µA
		DATA, $\overline{SB}$, Mode	2.5 5.5	— —	50 121	
C_{in}	Input Capacitance		—	—	14.0	pF
C_{out}	Output Capacitance		—	—	8.0	pF
I_{DD}	Standby Current, $\overline{SB}$ = V_{SS} or Open		2.5 5.5	— —	1.4 3.6	mA
I_{dd}	Operating Current (200 mV p–p input at f_{in1} and f_{in2}, $\overline{SB}$ = V_{DD})		2.5 5.5	— —	2.8 6.2	mA
I_{OZ}	Three–State Leakage Current (V_{out} = 0 or 5.5 V)		5.5	—	± 1.0	µA

SWITCHING CHARACTERISTICS (T_A = 25°C, C_L = 50 pF)

Symbol	Characteristic	Figure No.	V_{DD}	Guaranteed Limit		Unit
				Min	Max	
t_{TLH}	Output Rise Time	1, 5	3.0 5.0	— —	200 100	ns
t_{THL}	Output Fall Time	1, 5	3.0 5.0	— —	200 100	ns
t_r, t_f	Input Rise and Fall Time, OSC_{in}	2	3.0 5.0	— —	5.0 4.0	µs
f_{max}	Input Frequency OSC_{in} Input = Sine Wave 200 mV p–p f_{in1} f_{in2}		3.0 – 5.0 3.0 – 5.0 3.0 – 5.0	— — —	12 60 60	MHz
t_{su}	Setup Time (MC145167) DATA to CLK	3	3.0 5.0	100 50	— —	ns
	ENB to CLK		3.0 5.0	200 100	— —	
t_h	Hold Time (MC145167), CLK to DATA	3	3.0 5.0	80 40	— —	ns
t_{rec}	Recovery Time (MC145167), ENB to CLK	3	3.0 5.0	80 40	— —	ns
t_w	Input Pulse Width (MC145167), CLK and ENB	4	3.0 5.0	80 60	— —	ns

SWITCHING WAVEFORMS

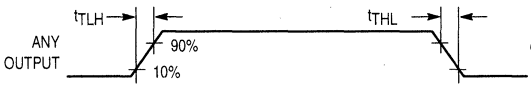


Figure 1.

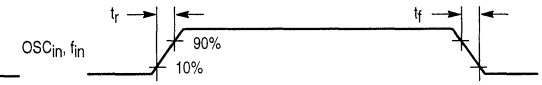


Figure 2.

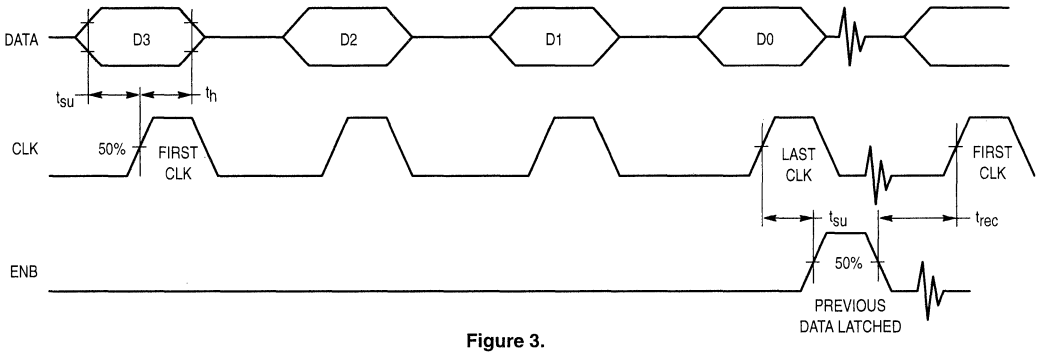


Figure 3.

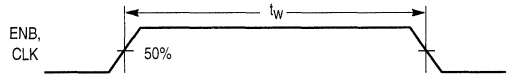


Figure 4.

PIN DESCRIPTIONS

INPUT PINS

OSC_{in}/OSC_{out}
Reference Oscillator Input/Output (Pins 1,16)

These pins form a reference oscillator when connected to an external parallel–resonant crystal. For a 46/49 MHz cordless phone application, a 10.24 MHz crystal is needed. OSC_{in} may also serve as input for an externally generated reference signal. This signal is typically ac coupled to OSC_{in}, but for larger amplitude signals (standard CMOS logic levels) dc coupling may also be used. In the external reference mode, no connection is required for OSC_{out}.

MODE
Mode Select (Pin 2)

Mode is for determining whether the part is to be used in the base or handset of a cordless phone. Internally, this pin is used in the decoding logic for selecting the ROM address. When high, the device is set in the base mode, and when low, it is set in the handset mode. This input has an internal pull–down device.

$\overline{SB}$
Standby Input (Pin 3)

The standby pin is used to save power when not transmitting. When high, both the transmit and receive loops are in operation. When low, the transmit loop is disabled, thereby reducing power consumption. This input has an internal pull–down device.

D0 – D3
Data Inputs (MC145166 — Pins 5 – 8)

These inputs provide the BCD code for selecting the one of ten channels to be locked in both the transmit and receive loop. When address data other than 1 – 10 are input, the decoding logic defaults to channel 10. The frequency assignments with reference to Mode and D0 – D3 are shown in Table 1. These inputs have internal pull–down devices.

f_{in1}, f_{in2}
Frequency Inputs (Pins 14, 9)

f_{in1} and f_{in2} are inputs to the divide–by–N receive and transmit counters, respectively. These signals are typically derived from the loop VCO and are ac coupled. For larger amplitude signals (standard CMOS logic levels), dc coupling may be used. The minimum input level is 200 mV p–p.

CLK, DATA
Clock, Data (MC145167 — Pins 5, 6)

These pins provide the BCD input by using serial channel programming instead of parallel. Logical high represents a 1. Each low–to–high transition of the clock shifts one bit of data into the on–chip shift register.

ENB
Enable (MC145167 — Pin 8)

The enable pin controls the data transfer from the shift register to the 4–bit latch. A positive pulse latches the data.

OUTPUT PINS

5 k
5 kHz Tone Signals (Pin 4)

The 5 kHz tone signals are N–channel, open–drain outputs derived from the reference oscillator.

$\overline{LD}$
Lock Detect Signal (Pin 10)

The lock detect signal is associated with the transmit loop. The lock output goes high to indicate an out–of–lock condition. This is a P–channel open–drain output.

PD1, PD2
Phase Detector Outputs (Pins 13, 11)

These are three–state outputs of the transmit and receive phase detectors for use as loop error signals. Phase detector gain is $V_{DD}/4\ \pi$ volts per radian.

Frequency $f_V > f_r$ or f_V leading: Output = Negative pulses
Frequency $f_V < f_r$ or f_V lagging: Output = Positive pulses
Frequency $f_V = f_r$ and phase coincidence: Output = High–impedance state

POWER SUPPLY

V_{SS}
Negative Power Supply (Pin 12)

This pin is the negative supply potential and is usually ground.

V_{DD}
Positive Power Supply (Pin 15)

This pin is the positive supply potential and may range from + 2.5 to + 5.5 V with respect to V_{SS}.

Table 1. MC145166/67 Divide Ratios and VCO Frequencies

Channels					Handset (Mode = 0)				Base (Mode = 1)			
					Transmit		Receive		Transmit		Receive	
D3	D2	D1	D0	CH#	f_{in2} (MHz)	÷ N	f_{in1} (MHz)	÷ N	f_{in2} (MHz)	÷ N	f_{in1} (MHz)	÷ N
0	0	0	1	1	49.670	9934	35.915	7183	46.610	9322	38.975	7795
0	0	1	0	2	49.845	9969	35.935	7187	46.630	9326	39.150	7830
0	0	1	1	3	49.860	9972	35.975	7195	46.670	9334	39.165	7833
0	1	0	0	4	49.770	9954	36.015	7203	46.710	9342	39.075	7815
0	1	0	1	5	49.875	9975	36.035	7207	46.730	9346	39.180	7836
0	1	1	0	6	49.830	9966	36.075	7215	46.770	9354	39.135	7827
0	1	1	1	7	49.890	9978	36.135	7227	46.830	9366	39.195	7839
1	0	0	0	8	49.930	9986	36.175	7235	46.870	9374	39.235	7847
1	0	0	1	9	49.990	9998	36.235	7247	46.930	9386	39.295	7859
1	0	1	0	10	49.970	9994	36.275	7255	46.970	9394	39.275	7855

NOTES:
1. Other input combinations will be defaulted to channel 10.
2. 0 = logic low, 1 = logic high.

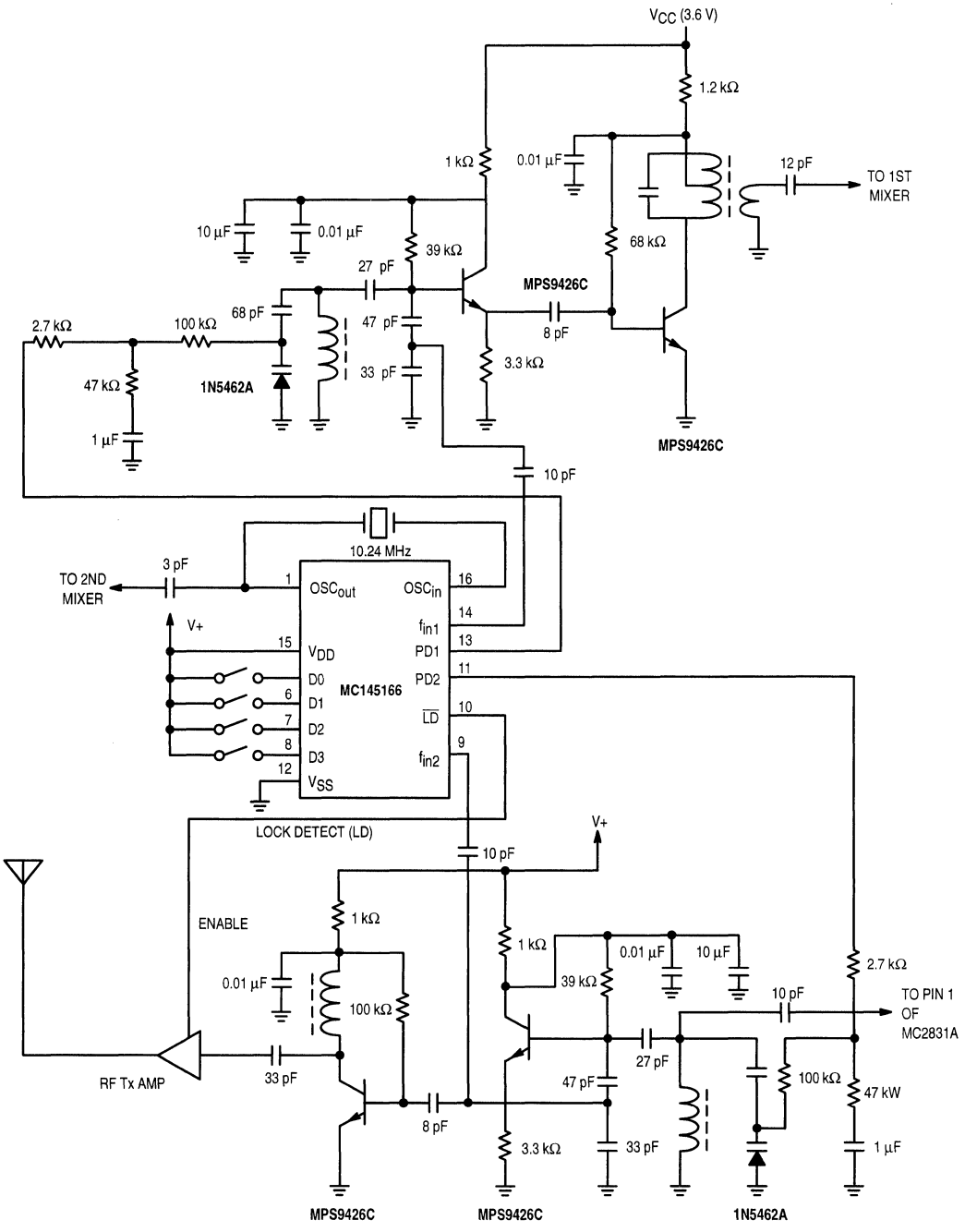


Figure 5. MC145166 Circuit Example

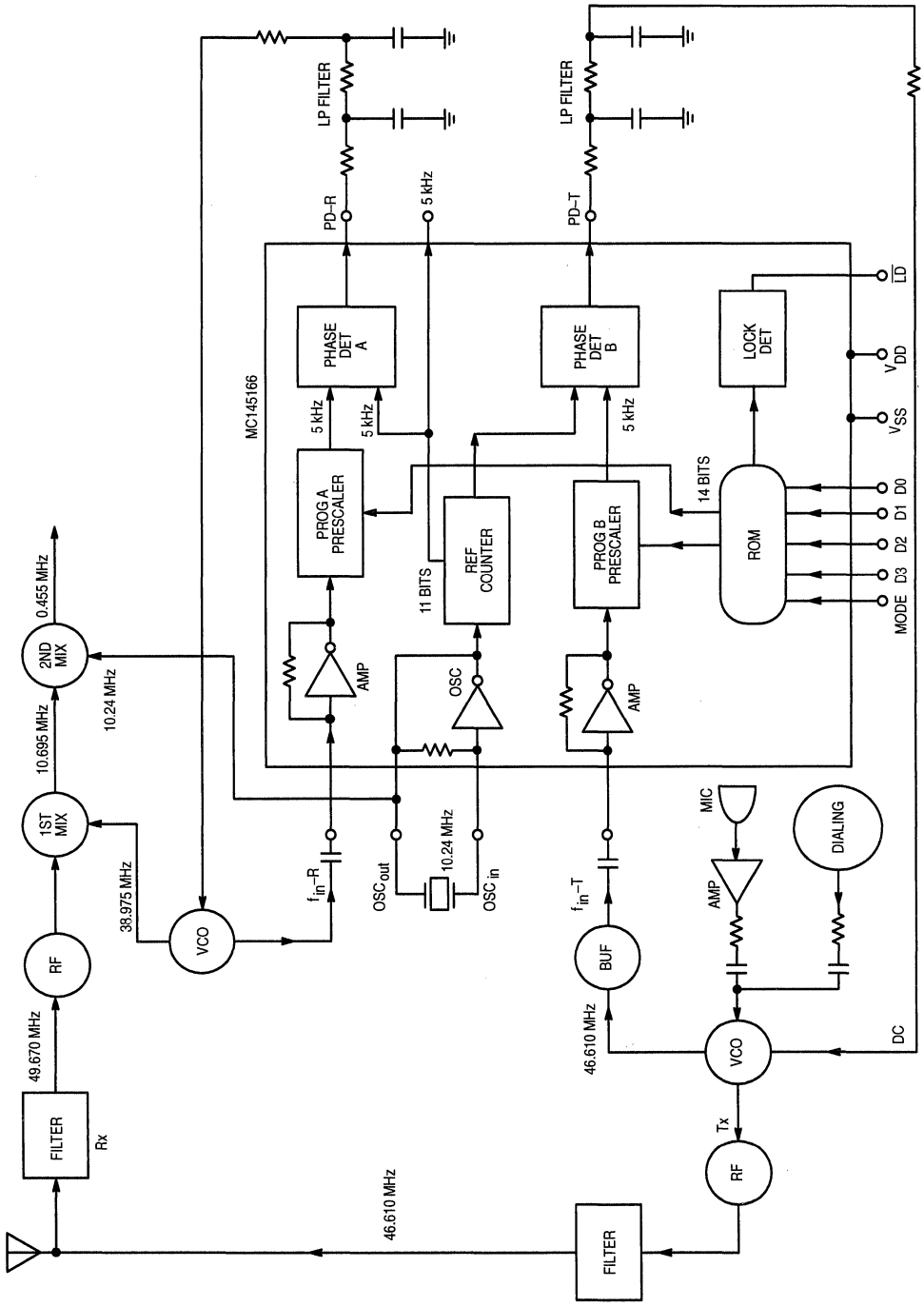


Figure 6. DPLL Application in 46/49 MHz Cordless Phone

MC145168
MC145169

Advance Information

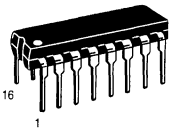
Dual PLLs for 46/49 MHz Cordless Telephones

CMOS

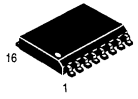
These devices are dual phase–locked loop frequency synthesizers intended for use primarily in 46/49 MHz cordless phones with up to 15 channels. These parts contain two mask–programmable counter ROMs for receive and transmit loops with two independent phase detect circuits. A common reference oscillator and reference divider are shared by the receive and transmit circuits.

Other features include a lock detect circuit for the transmit loop, illegal code default, a buffered oscillator output for mixing purposes in the system, and a 5.0 kHz tone output.

- Maximum Operating Frequency: 60 MHz @ V_{in} = 200 mV p–p
- Operating Temperature Range: – 40 to + 75°C
- Operating Voltage Range: 2.5 to 5.5 V
- On–Chip Oscillator Circuit Supports External Crystal
- Operating Power Consumption: 3.0 mA @ 3.0 V
- Lock Detect Signal
- Standby Mode for Power Savings: 1.5 mA @ 3.0 V
- Two Versions:
  - MC145168 — Up to 15–Channel ROM with 4–Bit Binary Code Input for Channel Pair Selection
  - MC145169 — Up to 15–Channel ROM with Serial Interface for Channel Pair Selection
- Custom 20–Channel ROM Versions of the MC145169 are Possible; Consult Factory



P SUFFIX
PLASTIC DIP
CASE 648

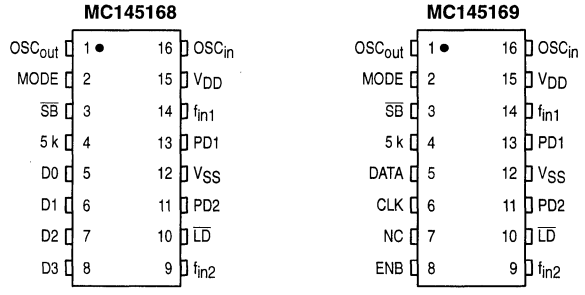


DW SUFFIX
SOG PACKAGE
CASE 751G

ORDERING INFORMATION

MC145168P	Plastic DIP
MC145168DW	SOG Package
MC145169P	Plastic DIP
MC145169DW	SOG Package

PIN ASSIGNMENTS

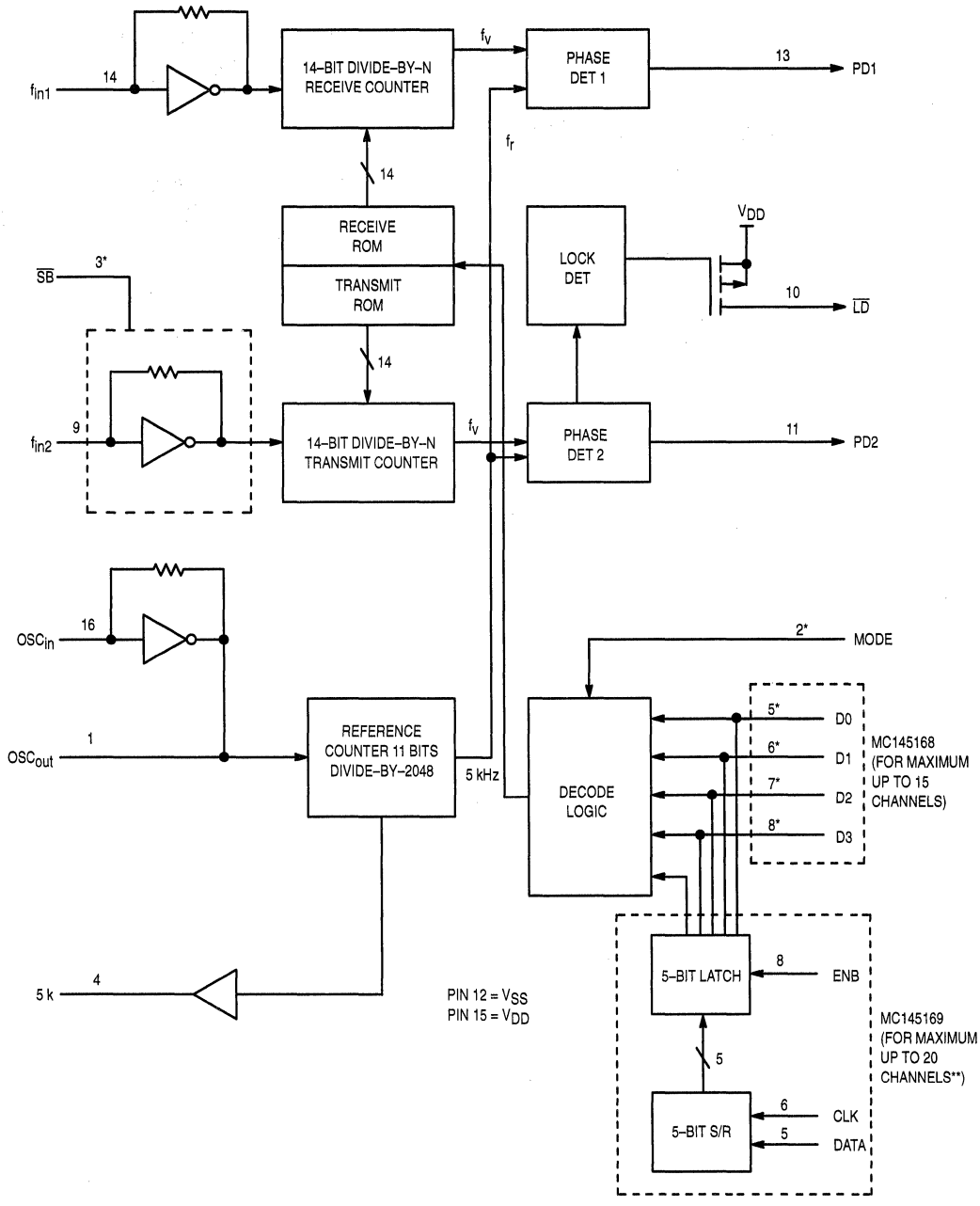


NC = NO CONNECTION

This document contains information on a new product. Specifications and information herein are subject to change without notice.

REV 1
8/95

BLOCK DIAGRAM



*On-chip pull-down.
**The standard MC145169 is 15 channels; see Tables 1 and 2. Custom versions up to 20 channels are possible.

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Rating	Value	Unit
V_{DD}	DC Supply Voltage	– 0.5 to + 6.0	V
V_{in}	Input Voltage, All Inputs	– 0.5 to V_{DD} + 0.5	V
I_{in}, I_{out}	DC Current Drain Per Pin	10	mA
I_{DD}, I_{SS}	DC Current Drain V_{DD} or V_{SS} Pins	30	mA
T_{stg}	Storage Temperature Range	– 65 to + 150	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Descriptions section.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

2

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS}, T_A = 25°C)

Symbol	Characteristic		V_{DD}	Guaranteed Limit Min	Guaranteed Limit Max	Unit
V_{DD}	Power Supply Voltage Range		—	2.5	5.5	V
V_{OL}	Output Voltage (I_{out} = 0)	0 Level	2.5 5.5	— —	0.05 0.05	V
V_{OH}	(V_{in} = V_{DD} or 0)	1 Level	2.5 5.5	2.45 5.45	— —	
V_{IL}	Input Voltage (V_{out} = 0.5 V or V_{DD} – 0.5 V)	0 Level	2.5 5.5	— —	0.75 1.65	V
V_{IH}		1 Level	2.5 5.5	1.75 3.85	— —	
I_{OH}	Output Current (V_{out} = 2.2 V) (V_{out} = 5.0 V)	Source	2.5 5.5	– 0.18 – 0.55	— —	mA
I_{OL}	(V_{out} = 0.3 V) (V_{out} = 0.5 V)	Sink	2.5 5.5	0.18 0.55	— —	
I_{IL}	Input Current (V_{in} = 0)	OSC_{in}, f_{in1}, f_{in2}	2.5 5.5	— —	– 30 – 66	µA
		DATA, $\overline{SB}$, Mode	2.5 5.5	— —	– 0.05 – 0.11	
I_{IH}	(V_{in} = V_{DD} – 0.5)	OSC_{in}, f_{in1}, f_{in2}	2.5 5.5	— —	30 66	µA
		DATA, $\overline{SB}$, Mode	2.5 5.5	— —	50 121	
C_{in}	Input Capacitance		—	—	14.0	pF
C_{out}	Output Capacitance		—	—	8.0	pF
I_{DD}	Standby Current, $\overline{SB}$ = V_{SS} or Open		2.5 5.5	— —	1.4 3.6	mA
I_{dd}	Operating Current (200 mV p–p input at f_{in1}, f_{in2}, $\overline{SB}$ = V_{DD})		2.5 5.5	— —	2.8 6.2	mA
I_{OZ}	Three–State Leakage Current (V_{out} = 0 V or 5.5 V)		5.5	—	± 1.0	µA

SWITCHING CHARACTERISTICS (T_A=25°C, C_L=50 pF)

Symbol	Characteristic	Figure No.	V_{DD}	Guaranteed Limit		Unit
				Min	Max	
t_{TLH}	Output Rise Time	1, 5	3.0 5.0	— —	200 100	ns
t_{THL}	Output Fall Time	1, 5	3.0 5.0	— —	200 100	ns
t_r, t_f	Input Rise and Fall Time, OSC_{in}	2	3.0 5.0	— —	5.0 4.0	µs
f_{max}	Input Frequency OSC_{in} Input = Sine Wave 200 mV p–p f_{in1} f_{in2}		3.0 – 5.0 3.0 – 5.0 3.0 – 5.0	— — —	12 60 60	MHz
t_{su}	Setup Time (MC145169) DATA to CLK	3	3.0 5.0	100 50	— —	ns
	ENB to CLK	3	3.0 5.0	200 100	— —	
t_h	Hold Time (MC145169), CLK to DATA	3	3.0 5.0	80 40	— —	ns
t_{rec}	Recovery Time (MC145169), ENB to CLK	3	3.0 5.0	80 40	— —	ns
t_w	Input Pulse Width (MC145169), CLK and ENB	4	3.0 5.0	80 60	— —	ns

SWITCHING WAVEFORMS

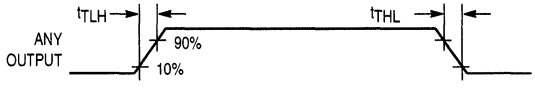


Figure 1.

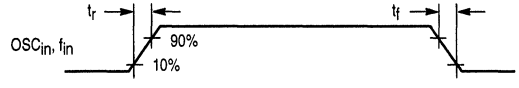


Figure 2.

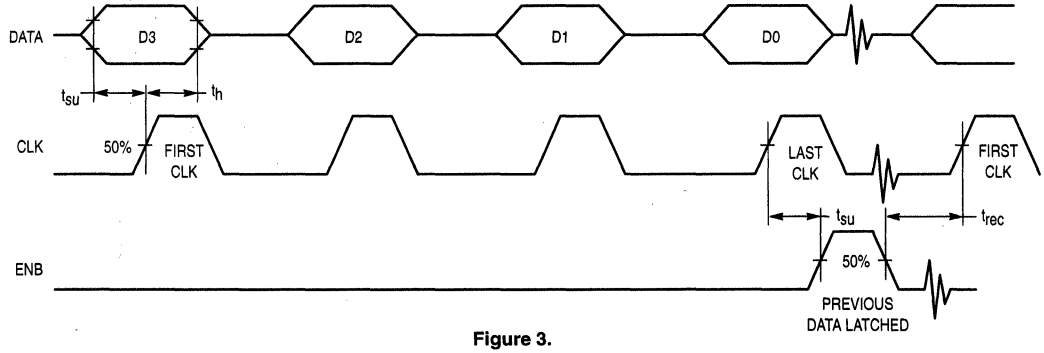


Figure 3.

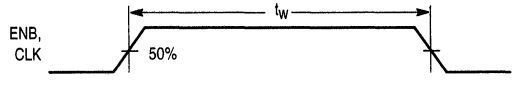


Figure 4.

PIN DESCRIPTIONS

INPUT PINS

OSC_{in}/OSC_{out}
Reference Oscillator Input/Output (Pins 16, 1)

These pins form a reference oscillator when connected to an external parallel–resonant crystal. For a 46/49 MHz cordless phone application, a 10.24 MHz crystal is needed. OSC_{in} may also serve as input for an externally generated reference signal. This signal is typically ac coupled to OSC_{in}, but for larger amplitude signals (standard CMOS logic levels) dc coupling may also be used. In the external reference mode, no connection is required for OSC_{out}.

MODE
Mode Select (Pin 2)

Mode is for determining whether the part is to be used in the base or handset of a cordless phone. Internally, this pin is used in the decoding logic for selecting the ROM address. When high, the device is set in the base mode, and when low, it is set in the handset mode. This input has an internal pull–down device.

$\overline{SB}$
Standby (Pin 3)

The standby pin is used to save power when not transmitting. When high, both the transmit and receive loops are in operation. When low, the transmit loop is disabled, thereby reducing power consumption. This input has an internal pull–down device.

D0 – D3 (MC145168 Only)
Data Inputs (Pins 5, 6, 7, 8)

These inputs provide the 4–bit binary code for selecting the 1 of 15 channels for the transmit and receive loops. When address data other than 1 – 15 are input, the decoding logic defaults to channel 1. The frequency assignments, with reference to Mode and D0 – D3, are shown in Tables 1 and 2. These inputs have internal pull–down devices.

f_{in1}, f_{in2}
Frequency Inputs (Pins 14, 9)

f_{in1} and f_{in2} are inputs to the divide–by–N receive and transmit counters, respectively. These signals are typically derived from the loop VCO and are ac coupled. The minimum input level is 200 mV p–p. For larger amplitude signals (standard CMOS logic levels), dc coupling may be used.

DATA, CLK (MC145169 Only)
Data, Clock (Pins 5, 6)

These pins provide the binary input by using serial channel programming. A logic high represents a 1. Each low–to–high transition of the clock shifts one bit of data into the on–chip shift register. Data is entered MSB first (see Figure 3).

ENB (MC145169 Only)
Enable (Pin 8)

The enable pin controls the data transfer from the shift register to the latch. A positive pulse transfers the data. This pin should normally be held low to avoid loading erroneous data into the latch.

OUTPUT PINS

5 k
5–kHz Tone Signal (Pin 4)

This is a 5 kHz tone signal derived from the reference oscillator. This pin is a push–pull output.

$\overline{LD}$
Lock Detect Signal (Pin 10)

The lock detect signal is associated with the transmit loop. The lock output goes high to indicate an out–of–lock condition. This is a P–channel open–drain output.

PD1/PD2
Transmit/Receive Phase Detector Outputs (Pins 13, 11)

These are three–state outputs of the transmit and receive phase detectors for use as loop error signals. Phase detector gain is $V_{DD}/4\ \pi$ volts per radian.

Frequency $f_V > f_r$ or f_V leading: negative pulses
Frequency $f_V < f_r$ or f_V lagging: positive pulses
Frequency $f_V = f_r$ and phase coincidence: high–impedance state
NOTE: f_V is the output of the N counter. f_r is the output of the reference counter.

POWER SUPPLY

V_{DD} (Pin 15)

This pin is the positive supply potential and may range from +2.5 to +5.5 V with respect to V_{SS}.

V_{SS} (Pin 12)

This pin is the negative supply potential and is usually ground.

Table 1. Handset Frequencies of Each Corresponding Channel in a 46/49 MHz Cordless Phone for the Korean Market

Channels					RX Freq	Receive (Note 3)		TX Freq	Transmit		
D3	D2	D1	D0	CH#	(MHz)	f_{in1} (MHz)	÷ N	(MHz)	f_{in2} (MHz)	÷ N	Mode
0	0	0	1	1	46.610	35.915	7183	49.670	49.670	9934	0
0	0	1	0	2	46.630	35.935	7187	49.845	49.845	9969	0
0	0	1	1	3	46.670	35.975	7195	49.860	49.860	9972	0
0	1	0	0	4	46.710	36.015	7203	49.770	49.770	9954	0
0	1	0	1	5	46.730	36.035	7207	49.875	49.875	9975	0
0	1	1	0	6	46.770	36.075	7215	49.830	49.830	9966	0
0	1	1	1	7	46.830	36.135	7227	49.890	49.890	9978	0
1	0	0	0	8	46.870	36.175	7235	49.930	49.930	9986	0
1	0	0	1	9	46.930	36.235	7247	49.990	49.990	9998	0
1	0	1	0	10	46.970	36.275	7255	49.970	49.970	9994	0
1	0	1	1	11	46.510	35.815	7163	49.695	49.695	9939	0
1	1	0	0	12	46.530	35.835	7167	49.710	49.710	9942	0
1	1	0	1	13	46.550	35.855	7171	49.725	49.725	9945	0
1	1	1	0	14	46.570	35.875	7175	49.740	49.740	9948	0
1	1	1	1	15	46.590	35.895	7179	49.755	49.755	9951	0

NOTES:
1. 0 = logic low, 1 = logic high.
2. Power–up and illegal inputs are defaulted to channel 1 in the MC145169. Illegal inputs are defaulted to channel 1 in MC145168.
3. First IF frequency of receive is 10.695 MHz; second IF is 455 kHz.
4. ÷ N = (f_{in}/f_{ref}) where f_{in} is the VCO frequency and f_{ref} is the reference frequency (5.0 kHz).

Table 2. Base Frequencies of Each Corresponding Channel in a 46/49 MHz Cordless Phone for the Korean Market

Channels					RX Freq	Receive (Note 3)		TX Freq	Transmit		
D3	D2	D1	D0	CH#	(MHz)	f_{in1} (MHz)	÷ N	(MHz)	f_{in2} (MHz)	÷ N	Mode
0	0	0	1	1	49.670	38.975	7795	46.610	46.610	9322	1
0	0	1	0	2	49.845	39.150	7830	46.630	46.630	9326	1
0	0	1	1	3	49.860	39.165	7833	46.670	46.670	9334	1
0	1	0	0	4	49.770	39.075	7815	46.710	46.710	9342	1
0	1	0	1	5	49.875	39.180	7836	46.730	46.730	9346	1
0	1	1	0	6	49.830	39.135	7827	46.770	46.770	9354	1
0	1	1	1	7	49.890	39.195	7839	46.830	46.830	9366	1
1	0	0	0	8	49.930	39.235	7847	46.870	46.870	9374	1
1	0	0	1	9	49.990	39.295	7859	46.930	46.930	9386	1
1	0	1	0	10	49.970	39.275	7855	46.970	46.970	9394	1
1	0	1	1	11	49.695	39.000	7800	46.510	46.510	9302	1
1	1	0	0	12	49.710	39.015	7803	46.530	46.530	9306	1
1	1	0	1	13	49.725	39.030	7806	46.550	46.550	9310	1
1	1	1	0	14	49.740	39.045	7809	46.570	46.570	9314	1
1	1	1	1	15	49.755	39.060	7812	46.590	46.590	9318	1

NOTES:
1. 0 = logic low, 1 = logic high.
2. Power–up and illegal inputs are defaulted to channel 1 in the MC145169. Illegal inputs are defaulted to channel 1 in MC145168.
3. First IF frequency of receive is 10.695 MHz; second IF is 455 kHz.
4. ÷ N = (f_{in}/f_{ref}) where f_{in} is the VCO frequency and f_{ref} is the reference frequency (5.0 kHz).

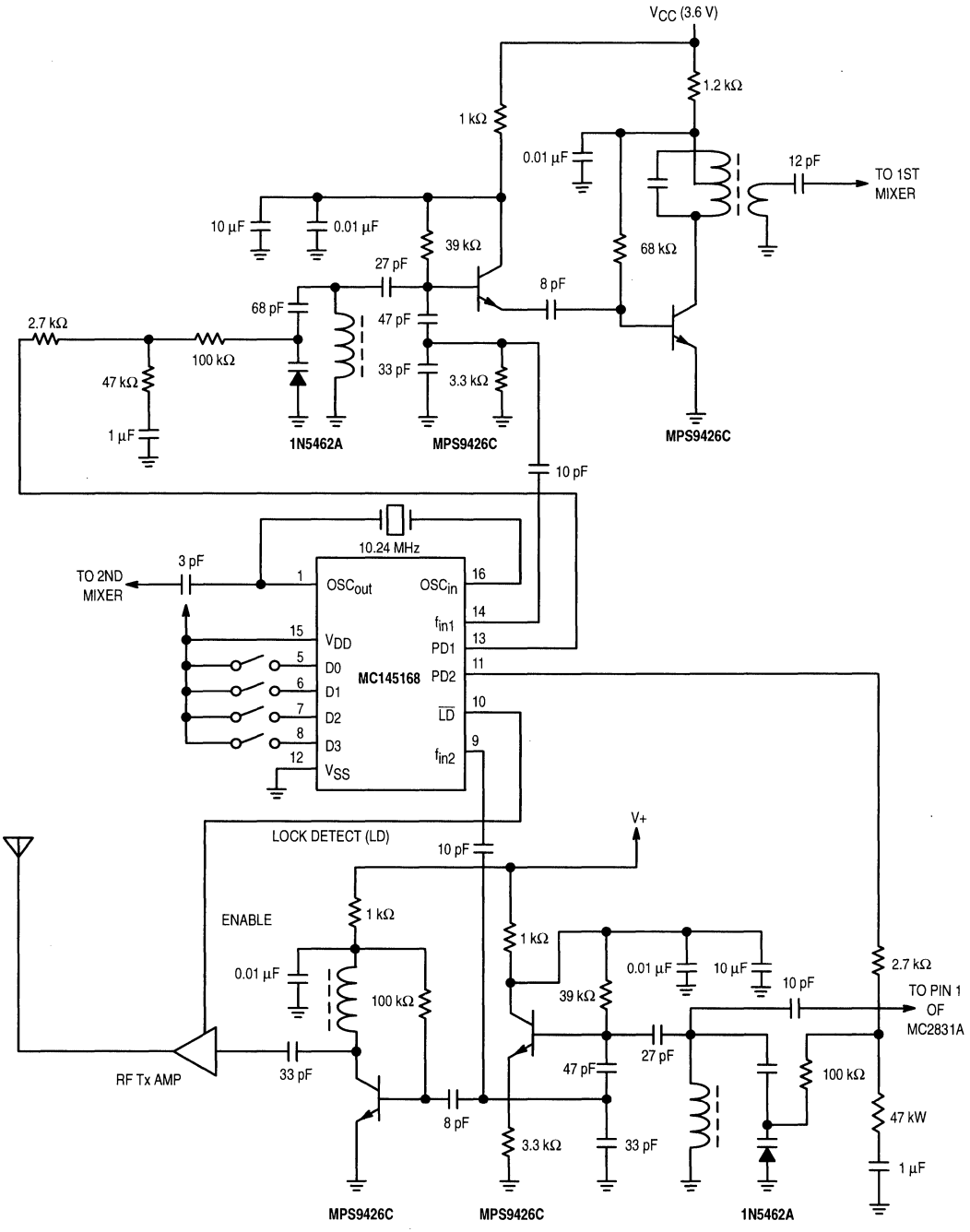


Figure 5. MC145168 Circuit Example

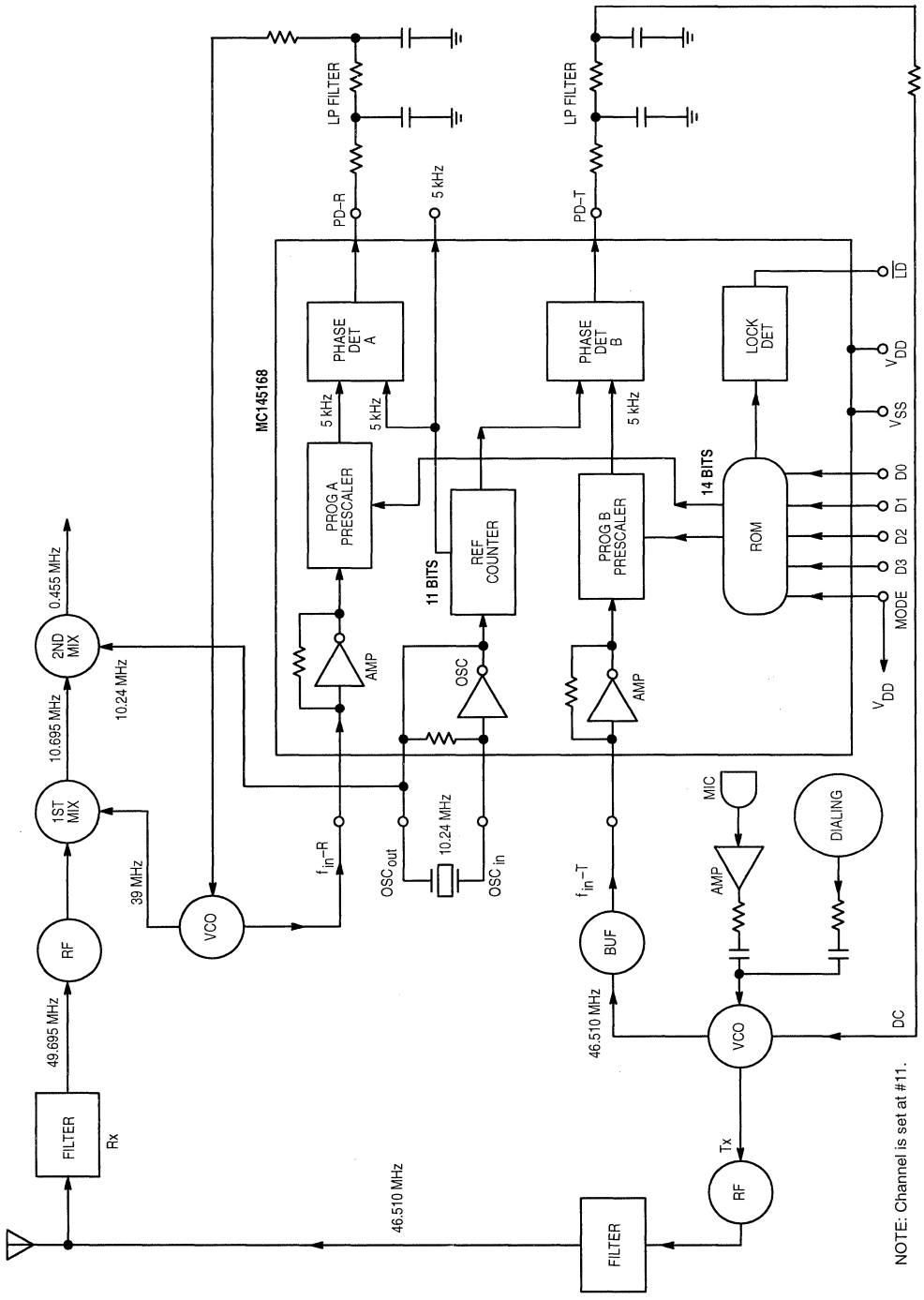


Figure 6. DPLL Application in 46/49 MHz Cordless Phone 15–Channel Base

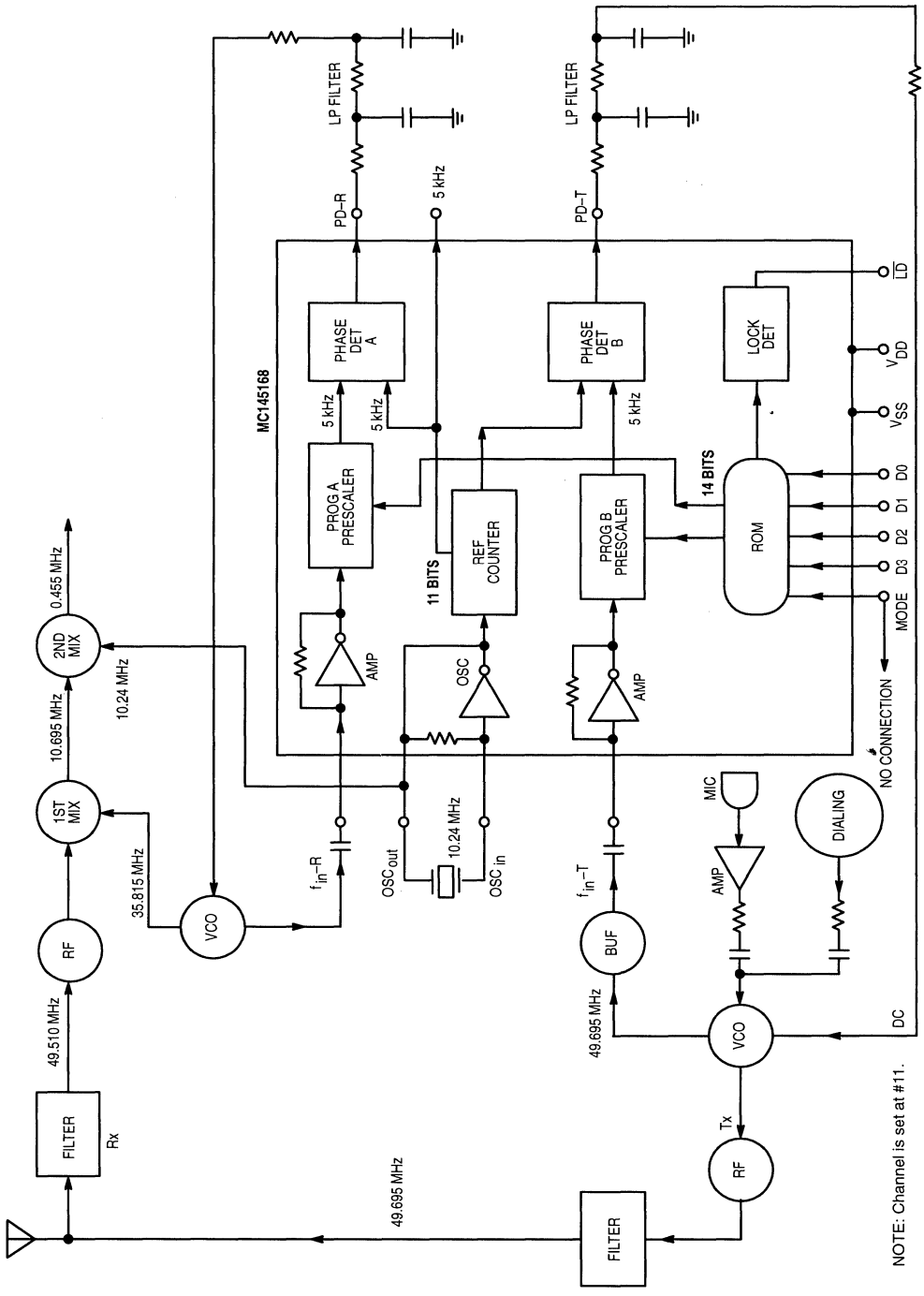


Figure 7. DPLL Application in 46/49 MHz Cordless Phone 15–Channel Handset

MC145170

PLL Frequency Synthesizer with Serial Interface

CMOS

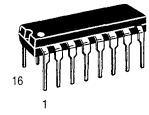
2

The MC145170 is a single–chip synthesizer capable of direct usage in the MF, HF, and VHF bands. A special architecture makes this PLL the easiest to program in the industry. Either a bit– or byte–oriented format may be used. Due to the patented BitGrabber™ registers, no address/steering bits are required for *random access* of the three registers. Thus, tuning can be accomplished via a 2–byte serial transfer to the 16–bit N register.

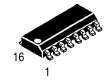
The device features fully programmable R and N counters, an amplifier at the f_{in} pin, on–chip support of an external crystal, a programmable reference output, and both single– and double–ended phase detectors with linear transfer functions. A new feature on the MC145170 is the C register (configuration register). The C register allows the part to be configured to meet various applications. A patented feature allows the C register to shut off unused outputs, thereby minimizing noise and interference.

In order to reduce lock times and prevent erroneous data from being loaded into the counters, a patented jam–load feature is included. Whenever a new divide ratio is loaded into the N register, both the N and R counters are jam loaded with their respective values and begin counting down together. The phase detectors are also initialized during the jam load.

- Operating Voltage Range: 2.5 to 6.0 V
- Maximum Operating Frequency:
  160 MHz @ V_{in} = 500 mV p–p, 4.5 V Minimum Supply
  100 MHz @ V_{in} = 500 mV p–p, 3.0 V Minimum Supply
- Operating Temperature Range: – 40 to 85°C
- R Counter Division Range: 5 to 32,767 Plus Direct Access to Phase Detector Input
- N Counter Division Range: 40 to 65,535
- Direct Interface to Motorola SPI and National MICROWIRE™ Serial Data Ports
- Higher Frequency Versions Available (Part Numbers MC145170P1 and MC145170D1)
- Chip Complexity: 4800 FETs or 1200 Equivalent Gates
- See Application Note AN1207



P SUFFIX
PLASTIC DIP
CASE 648

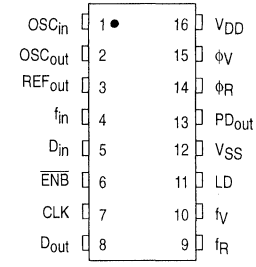


D SUFFIX
SOG PACKAGE
CASE 751B

ORDERING INFORMATION

MC145170P	Plastic DIP
MC145170D	SOG Package

PIN ASSIGNMENT

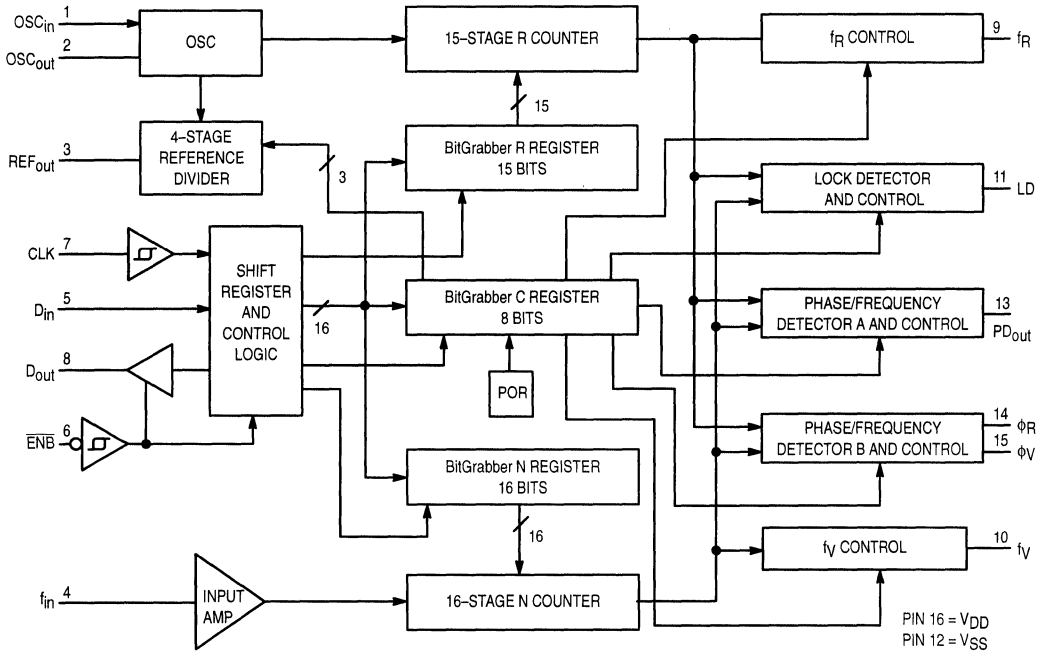


For new designs, the MC145170P1 and MC145170D1 are preferred devices over the MC145170P and MC145170D, respectively. Please see the MC145170–1 data sheet.

BitGrabber is a trademark of Motorola, Inc.
MICROWIRE is a trademark of National Semiconductor Corp.

REV 2
8/95

BLOCK DIAGRAM



MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	– 0.5 to + 6.0	V
V_{in}	DC Input Voltage	– 0.5 to V_{DD} + 0.5	V
V_{out}	DC Output Voltage	– 0.5 to V_{DD} + 0.5	V
I_{in}	DC Input Current, per Pin	± 10	mA
I_{out}	DC Output Current, per Pin	± 20	mA
I_{DD}	DC Supply Current, V_{DD} and V_{SS} Pins	± 30	mA
P_D	Power Dissipation, per Package	300	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 seconds	260	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Descriptions section.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS}, T_A = – 40 to +85°C)

Symbol	Parameter	Test Condition	V_{DD} V	Guaranteed Limit	Unit
V_{DD}	Power Supply Voltage Range		—	2.5 to 6.0	V
V_{IL}	Maximum Low–Level Input Voltage (D_{in}, CLK, $\overline{ENB}$)		2.5 4.5 6.0	0.50 1.35 1.80	V
V_{IH}	Minimum High–Level Input Voltage (D_{in}, CLK, $\overline{ENB}$)		2.5 4.5 6.0	2.00 3.15 4.20	V
V_{Hys}	Minimum Hysteresis Voltage (CLK, $\overline{ENB}$)		2.5 6.0	0.15 0.20	V
V_{OL}	Maximum Low–Level Output Voltage (Any Output)	I_{out} = 20 µA	2.5 6.0	0.1 0.1	V
V_{OH}	Minimum High–Level Output Voltage (Any Output)	I_{out} = – 20 µA	2.5 6.0	2.4 5.9	V
I_{OL}	Minimum Low–Level Output Current (PD_{out}, REF_{out}, f_R, f_V, LD, ϕ_R, ϕ_V)	V_{out} = 0.3 V V_{out} = 0.4 V V_{out} = 0.5 V	2.5 4.5 6.0	0.12 0.36 0.50	mA
I_{OH}	Minimum High–Level Output Current (PD_{out}, REF_{out}, f_R, f_V, LD, ϕ_R, ϕ_V)	V_{out} = 2.2 V V_{out} = 4.1 V V_{out} = 5.5 V	2.5 4.5 6.0	– 0.12 – 0.36 – 0.50	mA
I_{OL}	Minimum Low–Level Output Current (D_{out})	V_{out} = 0.4 V	4.5	1.6	mA
I_{OH}	Minimum High–Level Output Current (D_{out})	V_{out} = 4.1 V	4.5	– 1.6	mA
I_{in}	Maximum Input Leakage Current (D_{in}, CLK, $\overline{ENB}$, OSC_{in})	V_{in} = V_{DD} or V_{SS}	6.0	± 1.0	µA
I_{in}	Maximum Input Current (f_{in})	V_{in} = V_{DD} or V_{SS}	6.0	± 120	µA
I_{OZ}	Maximum Output Leakage Current (PD_{out})	V_{in} = V_{DD} or V_{SS}, Output in High–Impedance State	6.0	± 100	nA
	(D_{out})		6.0	± 5	µA
I_{DD}	Maximum Quiescent Supply Current	V_{in} = V_{DD} or V_{SS}; Outputs Open; Excluding f_{in} Amp Input Current Component	6.0	100	µA
I_{dd}	Maximum Operating Supply Current	f_{in} = 160 MHz @ 500 mV p–p; OSC_{in} = 10 MHz @ 1 V p–p; f_R, f_V, REF_{out} = Inactive and No Connect; OSC_{out}, ϕ_V, ϕ_R, PD_{out}, LD = No Connect; D_{in}, ENB, CLK = V_{DD} or V_{SS}	5.0	*	mA

* The nominal value is 7 mA. This is not a guaranteed limit.
Current consumption is reduced at lower frequencies and/or lower supply voltages (i.e., at 100 MHz with a 3 V supply, the device draws about 2.5 mA).

AC INTERFACE CHARACTERISTICS (T_A = – 40 to + 85°C, C_L = 50 pF, Input $t_r = t_f$ = 10 ns unless otherwise indicated)

Symbol	Parameter	Figure No.	V_{DD} V	Guaranteed Limit	Unit
f_{clk}	Serial Data Clock Frequency (Note: Refer to Clock t_w Below)	1	2.5 4.5 6.0	— dc to 4.0 dc to 4.0	MHz
t_{PLH}, t_{PHL}	Maximum Propagation Delay, CLK to D_{out}	1, 5	2.5 4.5 6.0	— 85 85	ns
t_{PLZ}, t_{PHZ}	Maximum Disable Time, D_{out} Active to High Impedance	2, 6	2.5 4.5 6.0	— 200 200	ns
t_{PZL}, t_{PZH}	Access Time, D_{out} High Impedance to Active	2, 6	2.5 4.5 6.0	— 0 to 100 0 to 100	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, D_{out} CL = 50 pF	1, 5	2.5 4.5 6.0	— 50 50	ns
	CL = 200 pF	1, 5	2.5 4.5 6.0	— 150 150	ns
C_{in}	Maximum Input Capacitance — D_{in}, $\overline{ENB}$, CLK		—	10	pF
C_{out}	Maximum Output Capacitance — D_{out}		—	15	pF

NOTE: For low–voltage applications, the MC145170–1 is recommended. The new MC145170–1 data sheet contains guaranteed 2.5 V parameters.

TIMING REQUIREMENTS (T_A = – 40 to + 85°C, Input $t_r = t_f$ = 10 ns unless otherwise indicated)

Symbol	Parameter	Figure No.	V_{DD} V	Guaranteed Limit	Unit
t_{su}, t_h	Minimum Setup and Hold Times, D_{in} vs CLK	3	2.5 4.5 6.0	— 40 40	ns
t_{su}, t_h, t_{rec}	Minimum Setup, Hold, and Recovery Times, $\overline{ENB}$ vs CLK	4	2.5 4.5 6.0	— 100 100	ns
$t_{w(H)}$	Minimum Inactive–High Pulse Width, $\overline{ENB}$	4	2.5 4.5 6.0	— 300 300	ns
t_w	Minimum Pulse Width, CLK	1	2.5 4.5 6.0	— 125 125	ns
t_r, t_f	Maximum Input Rise and Fall Times, CLK	1	2.5 4.5 6.0	100 100 100	µs

NOTE: For low–voltage applications, the MC145170–1 is recommended. The new MC145170–1 data sheet contains guaranteed 2.5 V parameters.

SWITCHING WAVEFORMS

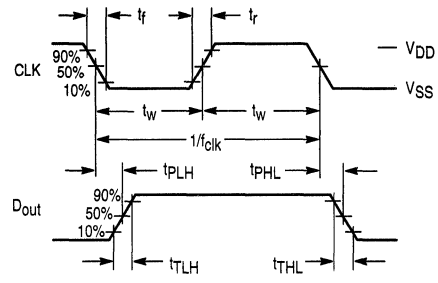


Figure 1.

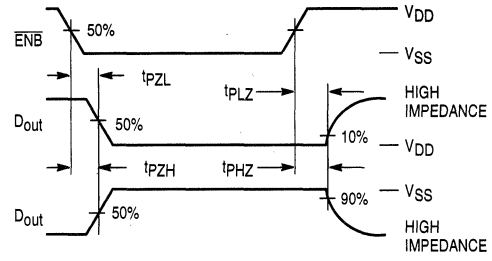


Figure 2.

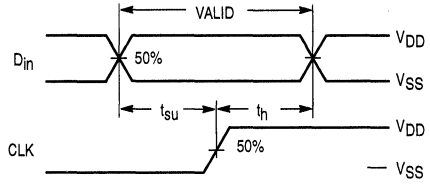


Figure 3.

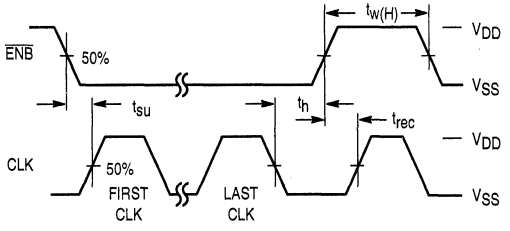
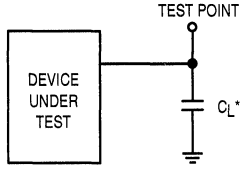
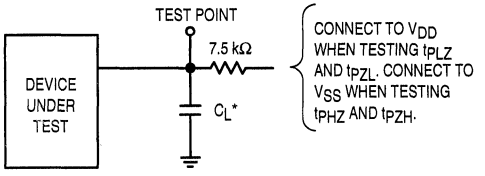


Figure 4.



* Includes all probe and fixture capacitance.

Figure 5. Test Circuit



* Includes all probe and fixture capacitance.

Figure 6. Test Circuit

LOOP SPECIFICATIONS (T_A = – 40 to + 85°C)

Symbol	Parameter	Test Condition	Figure No.	V_{DD} V	Guaranteed Range		Unit
					Min	Max	
f	Input Frequency, f_{in}	V_{in} ≥ 500 mV p–p Sine Wave, N Counter set to divide ratio such that f_V ≤ 2 MHz	7	2.5 3.0 4.5 6.0	— — — —	— 100 160 160	MHz
f	Input Frequency, OSC_{in} Externally Driven with ac Coupled Signal	V_{in} ≥ 1 V p–p Sine Wave, OSC_{out} = No Connect, R Counter set to divide ratio such that f_R ≤ 2 MHz	8	2.5 3.0 4.5 6.0	1 1 1 1	12 14 20 20	MHz
f_{XTAL}	Crystal Frequency, OSC_{in} and OSC_{out}	C1 ≤ 30 pF C2 ≤ 30 pF Includes Stray Capacitance	9	2.5 3.0 4.5 6.0	2 2 2 2	12 12 15 15	MHz
f_{out}	Output Frequency, REF_{out}	C_L = 30 pF	10, 12	2.5 3.0 4.5 6.0	dc dc dc dc	— — 10 10	MHz
f	Operating Frequency of the Phase Detectors			2.5 3.0 4.5 6.0	dc dc dc dc	— — 2 2	MHz
t_W	Output Pulse Width, ϕ_R, ϕ_V, and LD	f_R in Phase with f_V C_L = 50 pF	11, 12	2.5 3.0 4.5 6.0	— — 20 16	— — 100 90	ns
t_{TLH}, t_{THL}	Output Transition Times, ϕ_R, ϕ_V, LD, f_R, and f_V	C_L = 50 pF	11, 12	2.5 3.0 4.5 6.0	— — — —	— — 65 60	ns
C_{in}	Input Capacitance f_{in} OSC_{in}		— —	— —	— —	5 5	pF

NOTE: For low–voltage applications, the MC145170–1 is recommended. The new MC145170–1 data sheet contains guaranteed 2.5 V parameters.

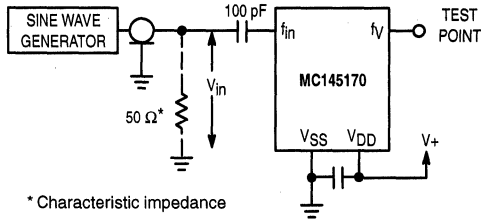


Figure 7. Test Circuit

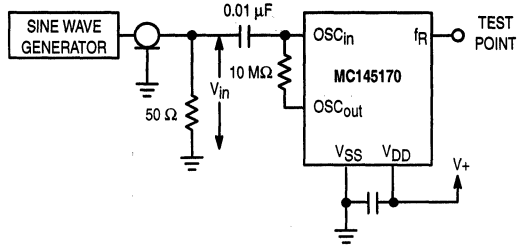


Figure 8. Test Circuit

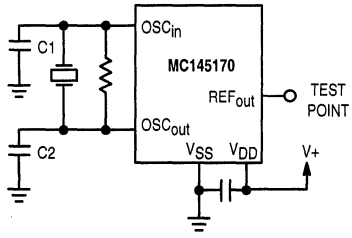


Figure 9. Test Circuit

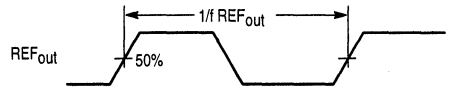


Figure 10. Switching Waveform

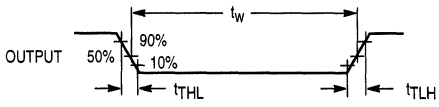


Figure 11. Switching Waveform

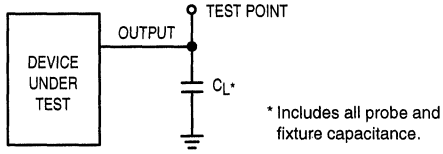


Figure 12. Test Circuit

PIN DESCRIPTIONS

DIGITAL INTERFACE PINS

D_{in}
Serial Data Input (Pin 5)

The bit stream begins with the most significant bit (MSB) and is shifted in on the low–to–high transition of CLK. The bit pattern is 1 byte (8 bits) long to access the C or configuration register, 2 bytes (16 bits) to access the N register, or 3 bytes (24 bits) to access the R register. Optionally, the R register can be accessed with a 15–bit transfer (see Table 1). The values in the C, N, and R registers do not change during shifting because the transfer of data to the registers is controlled by $\overline{ENB}$.

The bit stream needs neither address nor steering bits due to the innovative BitGrabber registers. Therefore, all bits in the stream are available to be data for the three registers. Random access of any register is provided (i.e., the registers may be accessed in any sequence). Data is retained in the registers over a supply range of 2.5 to 6.0 V. The formats are shown in Figures 13, 14, and 15.

D_{in} typically switches near 50% of V_{DD} to maximize noise immunity. This input can be directly interfaced to CMOS devices with outputs guaranteed to switch near rail–to–rail. When interfacing to NMOS or TTL devices, either a level shifter (MC74HC14A, MC14504B) or pull–up resistor of 1 to 10 kΩ must be used. Parameters to consider when sizing the resistor are worst–case I_{OL} of the driving device, maximum tolerable power consumption, and maximum data rate.

Table 1. Register Access
(MSBs are shifted in first, C0, N0, and R0 are the LSBs)

Number of Clocks	Accessed Register	Bit Nomenclature
8	C Register	C7, C6, C5, . . ., C0
16	N Register	N15, N14, N13, . . ., N0
15 or 24	R Register	R14, R13, R12, . . ., R0
Other Values ≤ 32	None	
Values > 32	TBD	

CLK
Serial Data Clock Input (Pin 7)

Low–to–high transitions on Clock shift bits available at D_{in}, while high–to–low transitions shift bits from D_{out}. The chip's 16–1/2–stage shift register is static, allowing clock rates down to dc in a continuous or intermittent mode.

Eight clock cycles are required to access the C register. Sixteen clock cycles are needed for the N register. Either 15 or 24 cycles can be used to access the R register (see Table 1 and Figures 13, 14, and 15).

CLK typically switches near 50% of V_{DD} and has a Schmitt–triggered input buffer. Slow CLK rise and fall times are allowed. See the last paragraph of **D_{in}** for more information.

CAUTION

To guarantee proper operation of the power–on reset (POR) circuit, the CLK pin must be held at the potential of either the V_{SS} or V_{DD} pin during power up. Do ***not*** float or toggle the CLK input during power up.

$\overline{ENB}$
Active Low Enable Input (Pin 6)

This pin is used to activate the serial interface to allow the transfer of data to/from the device. When $\overline{ENB}$ is in an inactive high state, shifting is inhibited, D_{out} is forced to the high–impedance state, and the port is held in the initialized state. To transfer data to the device, $\overline{ENB}$ (which must start inactive high) is taken low, a serial transfer is made via D_{in} and CLK, and $\overline{ENB}$ is taken back high. The low–to–high transition on $\overline{ENB}$ transfers data to the C, N, or R register depending on the data stream length per Table 1.

CAUTION

Transitions on $\overline{ENB}$ must not be attempted while CLK is high. This puts the device out of synchronization with the microcontroller. Resynchronization occurs when $\overline{ENB}$ is high and CLK is low.

This input is also Schmitt–triggered and switches near 50% of V_{DD}, thereby minimizing the chance of loading erroneous data into the registers. See the last paragraph of **D_{in}** for more information.

D_{out}
Three–State Serial Data Output (Pin 8)

Data is transferred out of the 16–1/2 stage shift register through D_{out} on the high–to–low transition of CLK. This output is a No Connect, unless used in one of the manners discussed below.

D_{out} could be fed back to an MCU/MPU to perform a wrap–around test of serial data. This could be part of a system check conducted at power up to test the integrity of the system's processor, PC board traces, solder joints, etc.

The pin could be monitored at an in–line QA test during board manufacturing.

Finally, D_{out} facilitates troubleshooting a system.

REFERENCE PINS

OSC_{in}/OSC_{out}
Reference Oscillator Input/Output (Pins 1, 2)

These pins form a reference oscillator when connected to terminals of an external parallel–resonant crystal. Frequency–setting capacitors of appropriate values as recommended by the crystal supplier are connected from each pin to ground (up to a maximum of 30 pF each, including stray capacitance). An external feedback resistor of 1 to 15 MΩ is connected directly across the pins to ensure linear operation of the amplifier. The MC145170 is designed to operate with crystals up to 15 MHz with a 4.5 to 6.0 V supply. With supplies less than 4.5 V, up to 12 MHz crystals may be used. (See Figure 9.)

If desired, an external clock source can be ac coupled to OSC_{in}. A 0.01 µF coupling capacitor is used for measurement purposes and is the minimum size recommended for applications. An external feedback resistor of approximately 10 MΩ is required across the OSC_{in} and OSC_{out} pins in the ac–coupled case (see Figure 8). *OSC_{out} is an internal node on the device and should not be used to drive any loads* (i.e., OSC_{out} is unbuffered). However, the buffered REF_{out} is available to drive external loads.

The external signal level must be at least 1 V p–p; the maximum frequencies are given in the **Loop Specifications** table. These maximum frequencies apply for R Counter divide ratios as indicated in the table. For very small ratios, the

maximum frequency is limited to the divide ratio times 2 MHz when the internal phase/frequency detectors are used. (Reason: the phase/frequency detectors are limited to a maximum input frequency of 2 MHz.)

If an external source is available which swings from at least the V_{IL} to V_{IH} levels listed in the **Electrical Characteristics** table, then dc coupling can be used. In the dc coupled case, no external feedback resistor is needed. OSC_{out} must be a No Connect to avoid loading an internal node on the MC145170, as noted above. For frequencies below 1 MHz, dc coupling must be used. The R counter is a static counter and may be operated down to dc. However, wave shaping by a CMOS buffer may be required to ensure fast rise and fall times into the OSC_{in} pin.

Each rising edge on the OSC_{in} pin causes the R counter to decrement by one.

REF_{out}
Reference Frequency Output (Pin 3)

This output is the buffered output of the crystal–generated reference frequency or externally provided reference source. This output may be enabled, disabled, or scaled via bits in the C register (see Figure 13).

REF_{out} can be used to drive a microprocessor clock input, thereby saving a crystal. Upon power up, the on–chip power–on–initialize circuit forces REF_{out} to the OSC_{in} divided–by–8 mode.

REF_{out} is capable of operation to 10 MHz; see the **Loop Specifications** table. Therefore, divide values for the reference divider are restricted to two or higher for OSC_{in} frequencies above 10 MHz.

If unused, the pin should be floated and should be disabled via the C register to minimize dynamic power consumption and electromagnetic interference (EMI).

COUNTER OUTPUT PINS

f_R
R Counter Output (Pin 9)

This signal is the buffered output of the 15–stage R counter. f_R can be enabled or disabled via the C register (patented). The output is disabled (static low logic level) upon power up. If unused, the output should be left disabled and unconnected to minimize interference with external circuitry.

The f_R signal can be used to verify the R counter's divide ratio. This ratio extends from 5 to 32,767 and is determined by the binary value loaded into the R register. Also, direct access to the phase detector via the OSC_{in} pin is allowed by choosing a divide value of 1 (see Figure 14). The maximum frequency which the phase detectors operate is 2 MHz. Therefore, the frequency of f_R must not exceed 2 MHz unless an external phase detector is used. The maximum frequency for driving external phase detectors is TBD.

When activated, the f_R signal appears as normally low and pulses high.

f_V
N Counter Output (Pin 10)

This signal is the buffered output of the 16–stage N counter. f_V can be enabled or disabled via the C register (patented). The output is disabled (static low logic level) upon power up. If unused, the output should be left disabled and unconnected to minimize interference with external circuitry.

The f_V signal can be used to verify the N counter's divide ratio. This ratio extends from 40 to 65,535 and is determined by the binary value loaded into the N register. The maximum frequency which the phase detectors operate is 2 MHz. Therefore, the frequency of f_V must not exceed 2 MHz unless an external phase detector is used. The maximum frequency for driving external phase detectors is TBD.

When activated, the f_V signal appears as normally low and pulses high.

LOOP PINS

f_{in}
Frequency Input (Pin 4)

This pin is a frequency input from the VCO. This pin feeds the on–chip amplifier which drives the N counter. This signal is normally sourced from an external voltage–controlled oscillator (VCO), and is ac coupled into f_{in}. A 100 pF coupling capacitor is used for measurement purposes and is the minimum size recommended for applications (see Figure 7). The frequency capability of this input is dependent on the supply voltage as listed in the **Loop Specifications** table. For small divide ratios, the maximum frequency is limited to the divide ratio times 2 MHz when the internal phase/frequency detectors are used. (Reason: the phase/frequency detectors are limited to a maximum frequency of 2 MHz.)

For signals which swing from at least the V_{IL} to V_{IH} levels listed in the **Electrical Characteristics** table, dc coupling may be used. Also, for low frequency signals, dc coupling is a requirement. The N counter is a static counter and may be operated down to dc. However, wave shaping by a CMOS buffer may be required to ensure fast rise and fall times into the f_{in} pin.

Each rising edge on the f_{in} pin causes the N counter to decrement by 1.

PD_{out}
Single–Ended Phase/Frequency Detector Output (Pin 13)

This is a three–state output for use as a loop–error signal when combined with an external low–pass filter. Through use of a Motorola patented technique, the detector's dead zone has been eliminated. Therefore, the phase/frequency detector is characterized by a linear transfer function. The operation of the phase/frequency detector is described below and is shown in Figure 16.

POL bit (C7) in the C register = low (see Figure 13)
- Frequency of $f_V > f_R$ or Phase of f_V Leading f_R: negative pulses from high impedance
- Frequency of $f_V < f_R$ or Phase of f_V Lagging f_R: positive pulses from high impedance
- Frequency and Phase of $f_V = f_R$: essentially high–impedance state; voltage at pin determined by loop filter

POL bit (C7) = high
- Frequency of $f_V > f_R$ or Phase of f_V Leading f_R: positive pulses from high impedance
- Frequency of $f_V < f_R$ or Phase of f_V Lagging f_R: negative pulses from high impedance
- Frequency and Phase of $f_V = f_R$: essentially high–impedance state; voltage at pin determined by loop filter

This output can be enabled, disabled, and inverted via the C register. If desired, PD_{out} can be forced to the high–impedance state by utilization of the disable feature in the C register (patented).

ϕ_R and ϕ_V
Double–Ended Phase/Frequency Detector Outputs (Pins 14, 15)

These outputs can be combined externally to generate a loop–error signal. Through use of a Motorola patented technique, the detector's dead zone has been eliminated. Therefore, the phase/frequency detector is characterized by a linear transfer function. The operation of the phase/frequency detector is described below and is shown in Figure 16.

POL bit (C7) in the C register = low (see Figure 13)
- Frequency of $f_V > f_R$ or Phase of f_V Leading f_R: ϕ_V = negative pulses, ϕ_R = essentially high
- Frequency of $f_V < f_R$ or Phase of f_V Lagging f_R: ϕ_V = essentially high, ϕ_R = negative pulses
- Frequency and Phase of $f_V = f_R$: ϕ_V and ϕ_R remain essentially high, except for a small minimum time period when both pulse low in phase

POL bit (C7) = high
- Frequency of $f_V > f_R$ or Phase of f_V Leading f_R: ϕ_R = negative pulses, ϕ_V = essentially high
- Frequency of $f_V < f_R$ or Phase of f_V Lagging f_R: ϕ_R = essentially high, ϕ_V = negative pulses
- Frequency and Phase of $f_V = f_R$: ϕ_V and ϕ_R remain essentially high, except for a small minimum time period when both pulse low in phase

These outputs can be enabled, disabled, and interchanged via the C register (patented).

LD
Lock Detector Output (Pin 11)

This output is essentially at a high level with narrow low–going pulses when the loop is locked (f_R and f_V of the same phase and frequency). The output pulses low when f_V and f_R are out of phase or different frequencies (see Figure 16).

This output can be enabled and disabled via the C register (patented). Upon power–up, on–chip initialization circuitry disables LD to a static low logic level to prevent a false "lock" signal. If unused, LD should be disabled and left open.

POWER SUPPLY

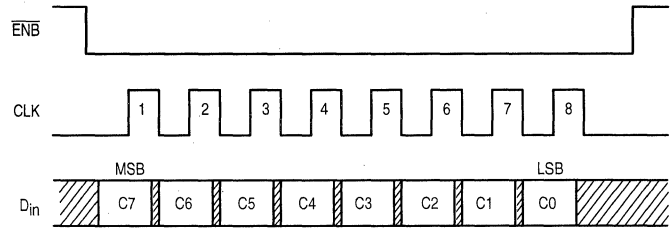
V_{DD}
Most Positive Supply Potential (Pin 16)

This pin may range from + 2.5 to 6.0 V with respect to V_{SS}.

For optimum performance, V_{DD} should be bypassed to V_{SS} using low–inductance capacitor(s) mounted very close to the MC145170. Lead lengths on the capacitor(s) should be minimized. (The very fast switching speed of the device causes current spikes on the power leads.)

V_{SS}
Most Negative Supply Potential (Pin 12)

This pin is usually ground. For measurement purposes, the V_{SS} pin is tied to a ground plane.



C7 – POL: Selects the output polarity of the phase/frequency detectors. When set high, this bit inverts PD_{out} and interchanges the ϕ_R function with ϕ_V as depicted in Figure 16. Also see the phase detector output pin descriptions for more information. This bit is cleared low at power–up.

C6 – PDA/B: Selects which phase/frequency detector is to be used. When set high, enables the output of phase/frequency detector A (PD_{out}) and disables phase/frequency detector B by forcing ϕ_R and ϕ_V to the static high state. When cleared low, phase/frequency detector B is enabled (ϕ_R and ϕ_V) and phase/frequency detector A is disabled with PD_{out} forced to the high–impedance state. This bit is cleared low at power–up.

C5 – LDE: Enables the lock detector output when set high. When the bit is cleared low, the LD output is forced to a static low level. This bit is cleared low at power–up.

C4 – C2, OSC2 – OSC0: Reference output controls which determine the REF_{out} characteristics as shown below. Upon power–up, the bits are initialized such that $OSC_{in}/8$ is selected.

C4	C3	C2	REF_{out} Frequency
0	0	0	dc (Static Low)
0	0	1	OSC_{in}
0	1	0	$OSC_{in}/2$
0	1	1	$OSC_{in}/4$
1	0	0	$OSC_{in}/8$
1	0	1	$OSC_{in}/16$
1	1	0	$OSC_{in}/8$
1	1	1	$OSC_{in}/16$

C1 – f_VE: Enables the f_V output when set high. When cleared low, the f_V output is forced to a static low level. The bit is cleared low upon power–up.

C0 – f_RE: Enables the f_R output when set high. When cleared low, the f_R output is forced to a static low level. The bit is cleared low upon power–up.

Figure 13. C Register Access and Format (8 Clock Cycles are Used)

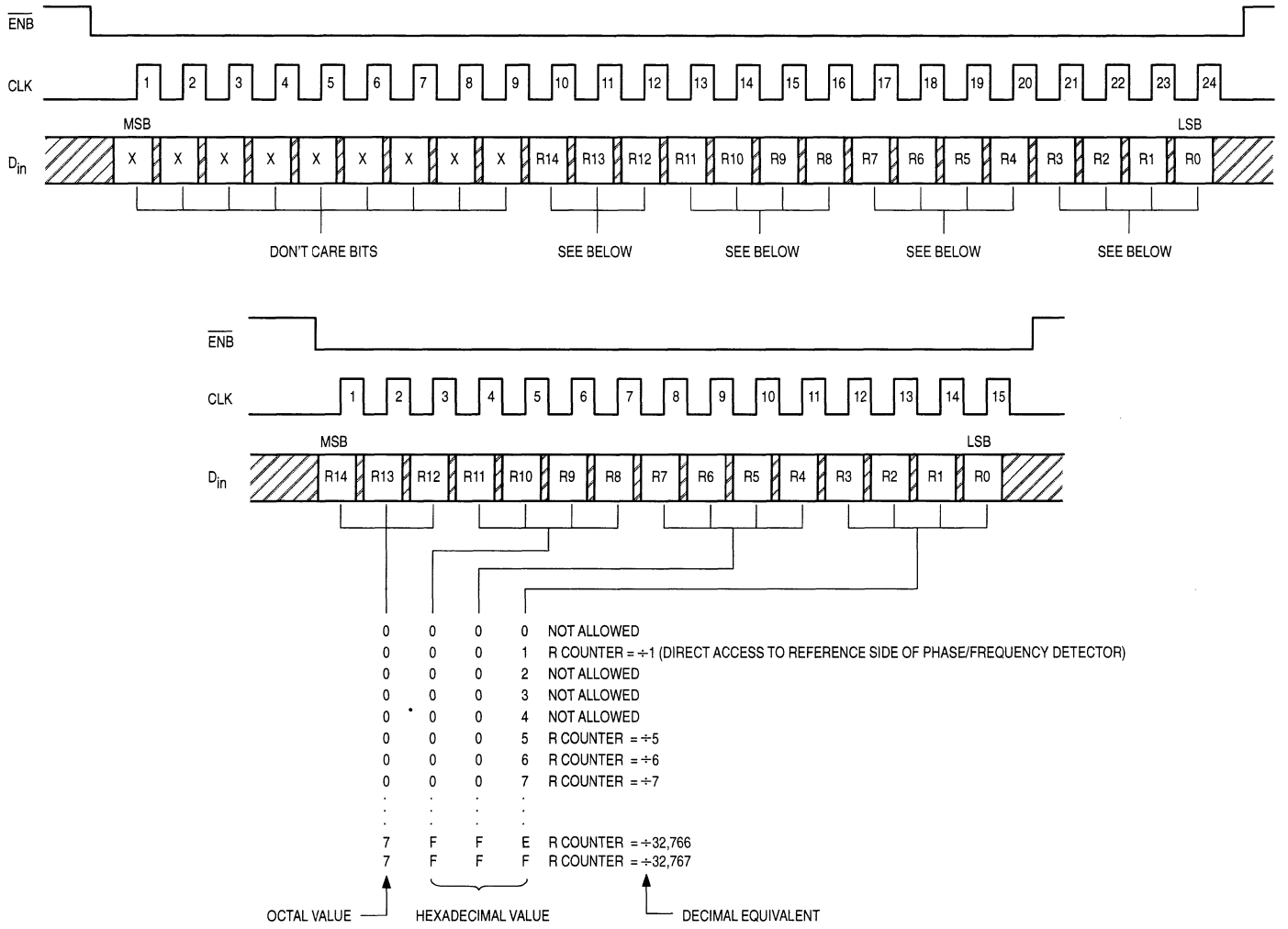


Figure 14. R Register Access and Formats (Either 24 or 15 Clock Cycles can be Used)

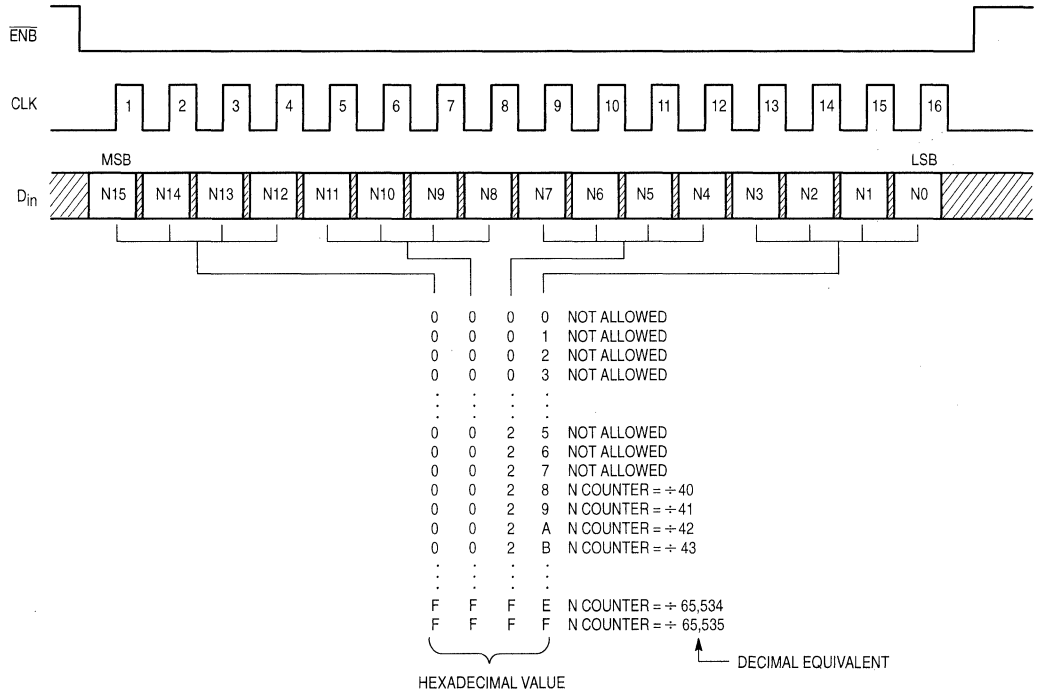
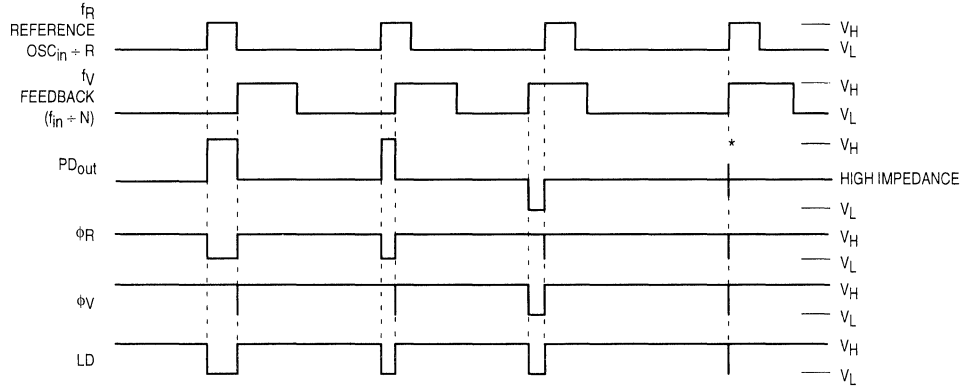


Figure 15. N Register Access and Format (16 Clock Cycles are Used)



V_H = High voltage level.
V_L = Low voltage level.
* At this point, when both f_R and f_V are in phase, both the source and sink turn on for a very short time.
NOTE: The PD_{out} generates error pulses during out–of–lock conditions. When locked in phase and frequency, the output is high impedance and the voltage at that pin is determined by the low–pass filter capacitor. PD_{out}, ϕR, and ϕV are shown with the polarity bit (POL) = low; see Figure 13 for POL.

Figure 16. Phase/Frequency Detectors and Lock Detector Output Waveforms

DESIGN CONSIDERATIONS

CRYSTAL OSCILLATOR CONSIDERATIONS

The following options may be considered to provide a reference frequency to Motorola's CMOS frequency synthesizers.

Use of a Hybrid Crystal Oscillator

Commercially available temperature–compensated crystal oscillators (TCXOs) or crystal–controlled data clock oscillators provide very stable reference frequencies. An oscillator capable of CMOS logic levels at the output may be direct or dc coupled to OSC_{in}. If the oscillator does not have CMOS logic levels on the outputs, capacitive or ac coupling to OSC_{in} may be used (see Figure 8).

For additional information about TCXOs and data clock oscillators, please consult the latest version of the *eem Electronic Engineers Master Catalog,* the *Gold Book,* or similar publications.

Design an Off–Chip Reference

The user may design an off–chip crystal oscillator using discrete transistors or ICs specifically developed for crystal oscillator applications, such as the MC12061 MECL device. The reference signal from the MECL device is ac coupled to OSC_{in} (see Figure 8). For large amplitude signals (standard CMOS logic levels), dc coupling is used.

Use of the On–Chip Oscillator Circuitry

The on–chip amplifier (a digital inverter) along with an appropriate crystal may be used to provide a reference source frequency. A fundamental mode crystal, parallel resonant at the desired operating frequency, should be connected as shown in Figure 17.

The crystal should be specified for a loading capacitance (C_L) which does not exceed 20 pF when used at the highest operating frequency. Larger C_L values are possible for lower frequencies. Assuming R1 = 0 Ω, the shunt load capacitance (C_L) presented across the crystal can be estimated to be:

$$C_L = \frac{C_{in}C_{out}}{C_{in} + C_{out}} + C_a + C_{stray} + \frac{C1 \bullet C2}{C1 + C2}$$

where

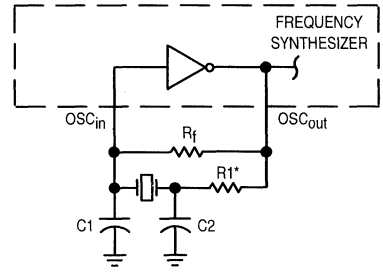
C_{in} = 5 pF (see Figure 18)
C_{out} = 6 pF (see Figure 18)
C_a = 1 pF (see Figure 18)
C1 and C2 = external capacitors (see Figure 17)
C_{stray} = the total equivalent external circuit stray capacitance appearing across the crystal terminals

The oscillator can be "trimmed" on–frequency by making a portion or all of C1 variable. The crystal and associated components must be located as close as possible to the OSC_{in} and OSC_{out} pins to minimize distortion, stray capacitance, stray inductance, and startup stabilization time. Circuit stray capacitance can also be handled by adding the appropriate stray value to the values for C_{in} and C_{out}. For this approach, the term C_{stray} becomes 0 in the above expression for C_L.

Power is dissipated in the effective series resistance of the crystal, R_e, in Figure 19. The maximum drive level specified by the crystal manufacturer represents the maximum stress that the crystal can withstand without damage or excessive shift in operating frequency. R1 in Figure 17 limits the drive level. The use of R1 is not necessary in most cases.

To verify that the maximum dc supply voltage does not cause the crystal to be overdriven, monitor the output frequency at the REF_{out} pin (OSC_{out} is not used because loading impacts the oscillator). The frequency should increase very slightly as the dc supply voltage is increased. An overdriven crystal decreases in frequency or becomes unstable with an increase in supply voltage. The operating supply voltage must be reduced or R1 must be increased in value if the overdriven condition exists. The user should note that the oscillator start–up time is proportional to the value of R1.

Through the process of supplying crystals for use with CMOS inverters, many crystal manufacturers have developed expertise in CMOS oscillator design with crystals. Discussions with such manufacturers can prove very helpful (see Table 2).



* May be needed in certain cases. See text.

Figure 17. Pierce Crystal Oscillator Circuit

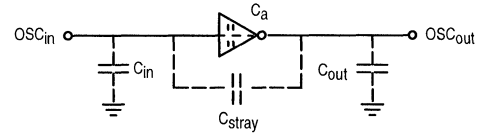
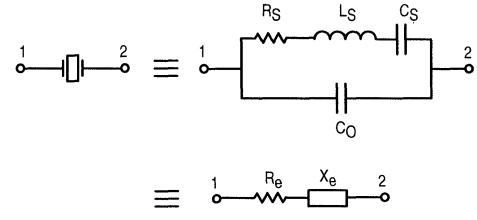


Figure 18. Parasitic Capacitances of the Amplifier and C_{stray}



NOTE: Values are supplied by crystal manufacturer (parallel resonant crystal).

Figure 19. Equivalent Crystal Networks

RECOMMENDED READING

Technical Note TN–24, Statek Corp.

Technical Note TN–7, Statek Corp.

E. Hafner, "The Piezoelectric Crystal Unit–Definitions and Method of Measurement", *Proc. IEEE,* Vol. 57, No. 2, Feb. 1969.

D. Kemper, L. Rosine, "Quartz Crystals for Frequency Control", *Electro–Technology,* June 1969.

P. J. Ottowitz, "A Guide to Crystal Selection", *Electronic Design*, May 1966.

D. Babin, "Designing Crystal Oscillators", *Machine Design*, March 7, 1985.

D. Babin, "Guidelines for Crystal Oscillator Design", *Machine Design*, April 25, 1985.

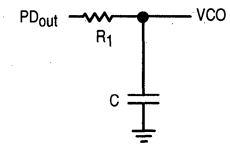
Table 2. Partial List of Crystal Manufacturers

Name	Address	Phone
United States Crystal Corp.	3605 McCart Ave., Ft. Worth, TX 76110	(817) 921–3013
Crystek Crystal	2351 Crystal Dr., Ft. Myers, FL 33907	(813) 936–2109
Statek Corp.	512 N. Main St., Orange, CA 92668	(714) 639–7810
Fox Electronics	5570 Enterprise Parkway, Ft. Myers, FL 33905	(813) 693–0099

NOTE: Motorola cannot recommend one supplier over another and in no way suggests that this is a complete listing of crystal manufacturers.

2

(A)

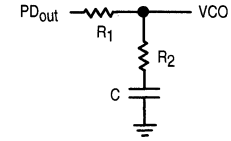


$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NR_1C}}$$

$$\zeta = \frac{N\omega_n}{2K_\phi K_{VCO}}$$

$$F(s) = \frac{1}{R_1sC + 1}$$

(B)

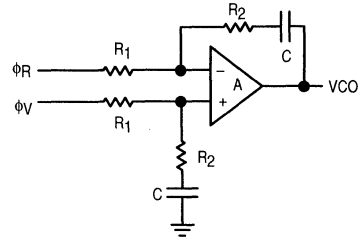


$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NC(R_1 + R_2)}}$$

$$\zeta = 0.5\,\omega_n \left(R_2C + \frac{N}{K_\phi K_{VCO}}\right)$$

$$F(s) = \frac{R_2sC + 1}{(R_1 + R_2)sC + 1}$$

(C)



$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NCR_1}}$$

$$\zeta = \frac{\omega_n R_2 C}{2}$$

ASSUMING GAIN A IS VERY LARGE, THEN:

$$F(s) = \frac{R_2sC + 1}{R_1sC}$$

NOTE:

For (C), R_1 is frequently split into two series resistors; each resistor is equal to R_1 divided by 2. A capacitor C_C is then placed from the midpoint to ground to further filter the error pulses. The value of C_C should be such that the corner frequency of this network does not significantly affect ω_n.

DEFINITIONS:

N = Total Division Ratio in Feedback Loop

K_ϕ (Phase Detector Gain) = $V_{DD}/ 4\pi$ V/radian for PD_{out}

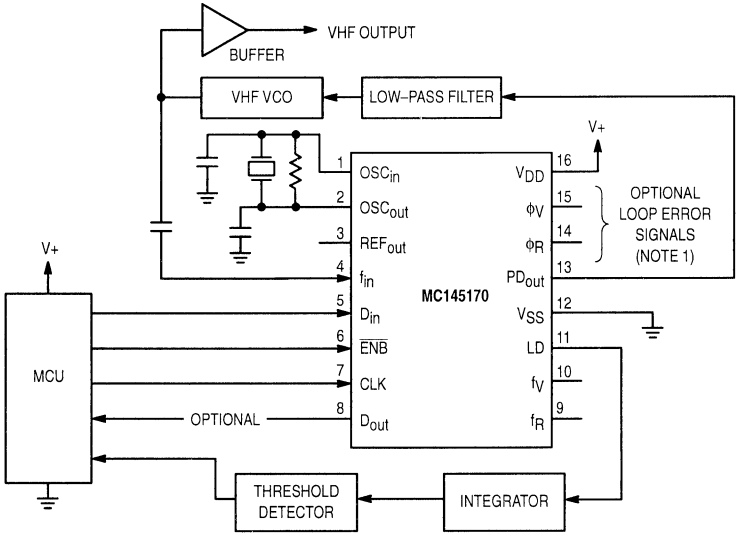
K_ϕ (Phase Detector Gain) = $V_{DD}/2\pi$ V/radian for ϕ_V and ϕ_R

$$K_{VCO}\text{ (VCO Gain)} = \frac{2\pi\Delta f_{VCO}}{\Delta V_{VCO}}$$

For a nominal design starting point, the user might consider a damping factor $\zeta \approx 0.7$ and a natural loop frequency $\omega_n \approx (2\pi f_R/50)$ where f_R is the frequency at the phase detector input. Larger ω_n values result in faster loop lock times and, for similar sideband filtering, higher f_R–related VCO sidebands.

RECOMMENDED READING:

Gardner, Floyd M., *Phaselock Techniques (second edition).* New York, Wiley–Interscience, 1979.
Manassewitsch, Vadim, *Frequency Synthesizers: Theory and Design (second edition).* New York, Wiley–Interscience, 1980.
Blanchard, Alain, *Phase–Locked Loops: Application to Coherent Receiver Design.* New York, Wiley–Interscience, 1976.
Egan, William F., *Frequency Synthesis by Phase Lock.* New York, Wiley–Interscience, 1981.
Rohde, Ulrich L., *Digital PLL Frequency Synthesizers Theory and Design.* Englewood Cliffs, NJ, Prentice–Hall, 1983.
Berlin, Howard M., *Design of Phase–Locked Loop Circuits, with Experiments.* Indianapolis, Howard W. Sams and Co., 1978.
Kinley, Harold, *The PLL Synthesizer Cookbook.* Blue Ridge Summit, PA, Tab Books, 1980.
Seidman, Arthur H., *Integrated Circuits Applications Handbook,* Chapter 17, pp. 538–586. New York, John Wiley & Sons.
Fadrhons, Jan, "Design and Analyze PLLs on a Programmable Calculator," *EDN.* March 5, 1980.
AN535, Phase–Locked Loop Design Fundamentals, Motorola Semiconductor Products, Inc., 1970.
AR254, Phase–Locked Loop Design Articles, Motorola Semiconductor Products, Inc., Reprinted with permission from *Electronic Design,* 1987.
AN1207, The MC145170 in Basic HF and VHF Oscillators, Motorola Semiconductor Products, Inc., 1992.



NOTES:

1. The ϕ_R and ϕ_V outputs are fed to an external combiner/loop filter. See the Phase–Locked Loop — Low–Pass Filter Design page for additional information.
2. For optimum performance, bypass the V_{DD} pin to V_{SS} (GND) with one or more low–inductance capacitors.
3. The R counter is programmed for a divide value = OSC_{in}/f_R. Typically, f_R is the tuning resolution required for the VCO. Also, the VCO frequency divided by f_R = N, where N is the divide value of the N counter.

Figure 20. Example Application

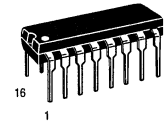
MC145170-1

Advance Information

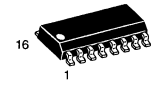
PLL Frequency Synthesizer with Serial Interface

CMOS

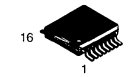
2



P SUFFIX
PLASTIC DIP
CASE 648



D SUFFIX
SOG PACKAGE
CASE 751B



DT SUFFIX
TSSOP
CASE 948C

ORDERING INFORMATION

MC145170P1	Plastic DIP
MC145170D1	SOG Package
MC145170DT1	TSSOP

The new MC145170–1 is pin–for–pin compatible with the MC145170. A comparison of the two parts is shown in the table below. The MC145170–1 is recommended for new designs.

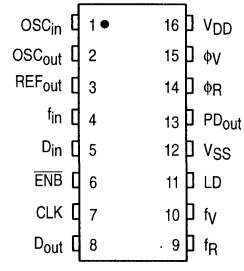
The MC145170–1 is a single–chip synthesizer capable of direct usage in the MF, HF, and VHF bands. A special architecture makes this PLL the easiest to program in the industry. Either a bit– or byte–oriented format may be used. Due to the patented BitGrabber™ registers, no address/steering bits are required for *random access* of the three registers. Thus, tuning can be accomplished via a 2–byte serial transfer to the 16–bit N register.

The device features fully programmable R and N counters, an amplifier at the f_{in} pin, on–chip support of an external crystal, a programmable reference output, and both single– and double–ended phase detectors with linear transfer functions (no dead zones). A configuration (C) register allows the part to be configured to meet various applications. A patented feature allows the C register to shut off unused outputs, thereby minimizing noise and interference.

In order to reduce lock times and prevent erroneous data from being loaded into the counters, a patented jam–load feature is included. Whenever a new divide ratio is loaded into the N register, both the N and R counters are jam–loaded with their respective values and begin counting down together. The phase detectors are also initialized during the jam load.

- Operating Voltage Range: 2.5 to 5.5 V
- Maximum Operating Frequency:
  185 MHz @ V_{in} = 500 mV p–p, 4.5 V Minimum Supply
  100 MHz @ V_{in} = 500 mV p–p, 3.0 V Minimum Supply
- Operating Supply Current: TBD
- Operating Temperature Range: – 40 to 85°C
- R Counter Division Range: 1 and 5 to 32,767
- N Counter Division Range: 40 to 65,535
- Direct Interface to Motorola SPI and National MICROWIRE™ Serial Data Ports
- Chip Complexity: 4800 FETs or 1200 Equivalent Gates
- See Application Note AN1207/D

PIN ASSIGNMENT



COMPARISION OF THE PLL FREQUENCY SYNTHESIZERS

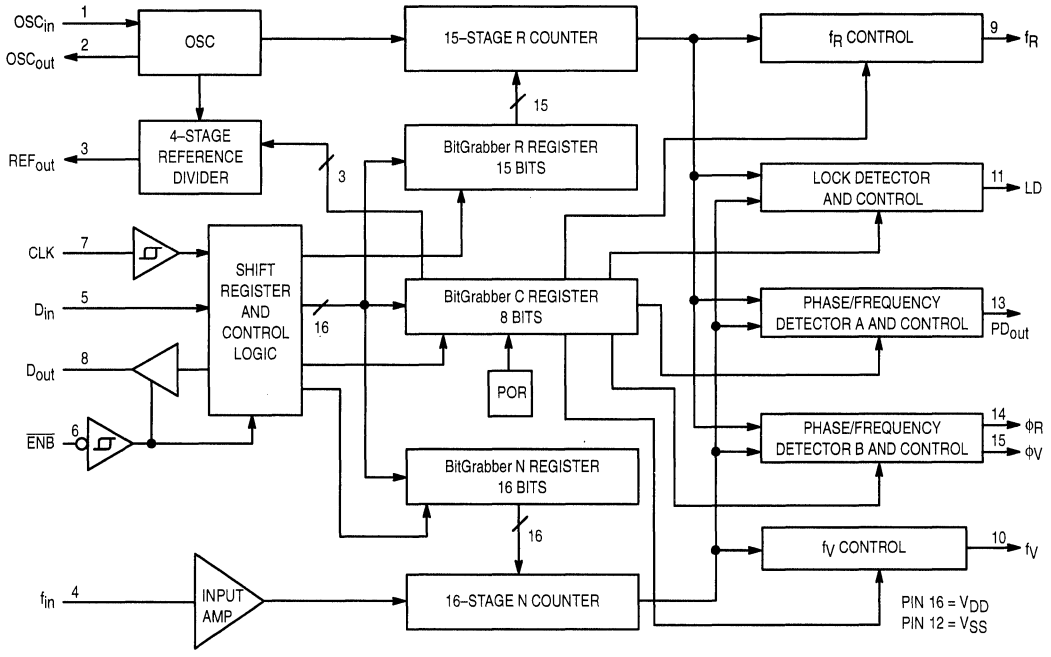
Parameter	MC145170–1	MC145170
Technology	1.2 µm CMOS	1.5 µm CMOS
Maximum Frequency with 5 V ± 10% Supply, f_{in}	185 MHz	160 MHz
Maximum Frequency with 5 V ± 10% Supply, OSC_{in}	25 MHz	20 MHz
Maximum Supply Voltage	5.5 V	6.0 V
Maximum Input Capacitance, f_{in}	7 pF	5 pF

This document contains information on a new product. Specifications and information herein are subject to change without notice.

BitGrabber is a trademark of Motorola Inc. MICROWIRE is a trademark of National Semiconductor Corp.

REV 0
10/95

BLOCK DIAGRAM



MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	– 0.5 to + 5.5	V
V_{in}	DC Input Voltage	– 0.5 to V_{DD} + 0.5	V
V_{out}	DC Output Voltage	– 0.5 to V_{DD} + 0.5	V
I_{in}	DC Input Current, per Pin	± 10	mA
I_{out}	DC Output Current, per Pin	± 20	mA
I_{DD}	DC Supply Current, V_{DD} and V_{SS} Pins	± 30	mA
P_D	Power Dissipation, per Package	300	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 seconds	260	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Descriptions section.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS}, T_A = – 40 to + 85°C)

Symbol	Parameter	Test Condition	V_{DD} V	Guaranteed Limit	Unit
V_{DD}	Power Supply Voltage Range		—	2.5 to 5.5	V
V_{IL}	Maximum Low–Level Input Voltage* (D_{in}, CLK, $\overline{ENB}$, f_{in})	dc Coupling to f_{in}	2.5 4.5 5.5	0.50 1.35 1.65	V
V_{IH}	Minimum High–Level Input Voltage* (D_{in}, CLK, $\overline{ENB}$, f_{in})	dc Coupling to f_{in}	2.5 4.5 5.5	2.00 3.15 3.85	V
V_{Hys}	Minimum Hysteresis Voltage (CLK, $\overline{ENB}$)		2.5 5.5	0.15 0.20	V
V_{OL}	Maximum Low–Level Output Voltage (Any Output)	I_{out} = 20 µA	2.5 5.5	0.1 0.1	V
V_{OH}	Minimum High–Level Output Voltage (Any Output)	I_{out} = – 20 µA	2.5 5.5	2.4 5.4	V
I_{OL}	Minimum Low–Level Output Current (PD_{out}, REF_{out}, f_R, f_V, LD, ϕ_R, ϕ_V)	V_{out} = 0.3 V V_{out} = 0.4 V V_{out} = 0.5 V	2.5 4.5 5.5	0.12 0.36 0.36	mA
I_{OH}	Minimum High–Level Output Current (PD_{out}, REF_{out}, f_R, f_V, LD, ϕ_R, ϕ_V)	V_{out} = 2.2 V V_{out} = 4.1 V V_{out} = 5.0 V	2.5 4.5 5.5	– 0.12 – 0.36 – 0.36	mA
I_{OL}	Minimum Low–Level Output Current (D_{out})	V_{out} = 0.4 V	4.5	1.6	mA
I_{OH}	Minimum High–Level Output Current (D_{out})	V_{out} = 4.1 V	4.5	– 1.6	mA
I_{in}	Maximum Input Leakage Current (D_{in}, CLK, $\overline{ENB}$, OSC_{in})	V_{in} = V_{DD} or V_{SS}	5.5	± 1.0	µA
I_{in}	Maximum Input Current (f_{in})	V_{in} = V_{DD} or V_{SS}	5.5	± 120	µA
I_{OZ}	Maximum Output Leakage Current (PD_{out})	V_{in} = V_{DD} or V_{SS}, Output in High–Impedance State	5.5	± 100	nA
	(D_{out})		5.5	± 5	µA
I_{DD}	Maximum Quiescent Supply Current	V_{in} = V_{DD} or V_{SS}; Outputs Open; Excluding f_{in} Amp Input Current Component	5.5	100	µA
I_{dd}	Maximum Operating Supply Current	f_{in} = 160 MHz @ 500 mV p–p; OSC_{in} = 10 MHz @ 1 V p–p; f_R, f_V, REF_{out} = Inactive and No Connect; OSC_{out}, ϕ_V, ϕ_R, PD_{out}, LD = No Connect; D_{in}, ENB, CLK = V_{DD} or V_{SS}	5.0	**	mA

*When dc coupling to the OSC_{in} pin is used, the pin must be driven rail–to–rail. In this case, OSC_{out} should be floated.

**The nominal value is TBD. This is not a guaranteed limit. Current consumption is reduced at lower frequencies and/or lower supply voltages (i.e., at 100 MHz with a 3 V supply, the device draws about TBD).

AC INTERFACE CHARACTERISTICS (T_A = – 40 to + 85°C, C_L = 50 pF, Input $t_r = t_f$ = 10 ns unless otherwise indicated)

Symbol	Parameter	Figure No.	V_{DD} V	Guaranteed Limit	Unit
f_{clk}	Serial Data Clock Frequency (Note: Refer to Clock t_w Below)	1	2.5 4.5 5.5	dc to 3.0 dc to 4.0 dc to 4.0	MHz
t_{PLH}, t_{PHL}	Maximum Propagation Delay, CLK to D_{out}	1, 5	2.5 4.5 5.5	150 85 85	ns
t_{PLZ}, t_{PHZ}	Maximum Disable Time, D_{out} Active to High Impedance	2, 6	2.5 4.5 5.5	300 200 200	ns
t_{PZL}, t_{PZH}	Access Time, D_{out} High Impedance to Active	2, 6	2.5 4.5 5.5	0 to 200 0 to 100 0 to 100	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, D_{out} CL = 50 pF	1, 5	2.5 4.5 5.5	150 50 50	ns
	CL = 200 pF	1, 5	2.5 4.5 5.5	900 150 150	ns
C_{in}	Maximum Input Capacitance – D_{in}, $\overline{ENB}$, CLK		—	10	pF
C_{out}	Maximum Output Capacitance – D_{out}		—	10	pF

TIMING REQUIREMENTS (T_A = – 40 to + 85°C, Input $t_r = t_f$ = 10 ns unless otherwise indicated)

Symbol	Parameter	Figure No.	V_{DD} V	Guaranteed Limit	Unit
t_{su}, t_h	Minimum Setup and Hold Times, D_{in} vs CLK	3	2.5 4.5 5.5	55 40 40	ns
t_{su}, t_h, t_{rec}	Minimum Setup, Hold, and Recovery Times, $\overline{ENB}$ vs CLK	4	2.5 4.5 5.5	135 100 100	ns
$t_{w(H)}$	Minimum Inactive–High Pulse Width, $\overline{ENB}$	4	2.5 4.5 5.5	400 300 300	ns
t_w	Minimum Pulse Width, CLK	1	2.5 4.5 5.5	166 125 125	ns
t_r, t_f	Maximum Input Rise and Fall Times, CLK	1	2.5 4.5 5.5	100 100 100	µs

SWITCHING WAVEFORMS

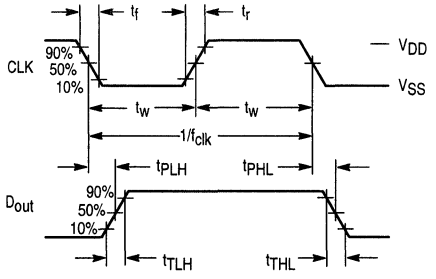


Figure 1.

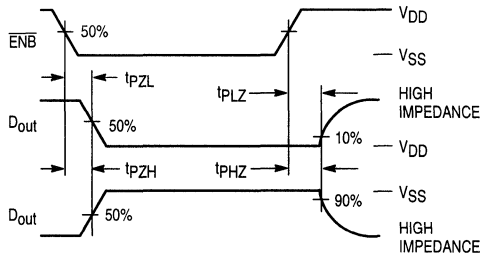


Figure 2.

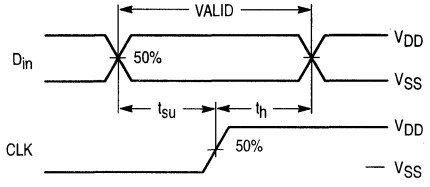


Figure 3.

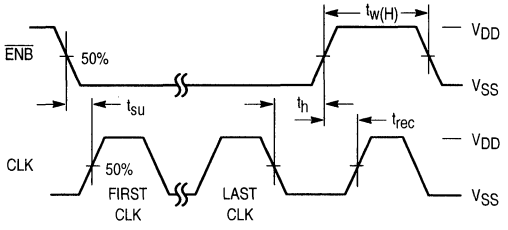
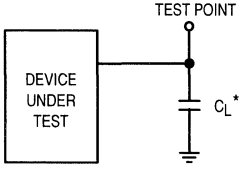
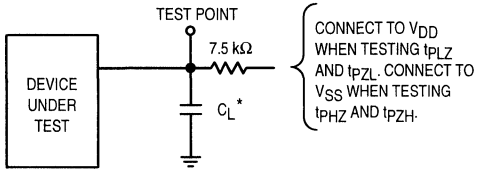


Figure 4.



* Includes all probe and fixture capacitance.

Figure 5. Test Circuit



* Includes all probe and fixture capacitance.

Figure 6. Test Circuit

LOOP SPECIFICATIONS (T_A = −40 to +85°C)

Symbol	Parameter	Test Condition	Figure No.	V_{DD} V	Guaranteed Range		Unit
					Min	Max	
f	Input Frequency, f_{in}	V_{in} ≥ 500 mV p–p Sine Wave, N Counter Set to Divide Ratio Such that f_V ≤ 2 MHz	7	2.5 3.0 4.5 5.5	5* 5* 25* 45*	TBD 100 185 185	MHz
f	Input Frequency, OSC_{in} Externally Driven with ac–Coupled Signal	V_{in} ≥ 1 V p–p Sine Wave, OSC_{out} = No Connect, R Counter Set to Divide Ratio Such that f_R ≤ 2 MHz	8	2.5 3.0 4.5 5.5	1* 1* 1* 1*	12 14 25 25	MHz
f_{XTAL}	Crystal Frequency, OSC_{in} and OSC_{out}	C1 ≤ 30 pF C2 ≤ 30 pF Includes Stray Capacitance	9	2.5 3.0 4.5 5.5	2 2 2 2	12 12 15 15	MHz
f_{out}	Output Frequency, REF_{out}	C_L = 30 pF	10, 12	2.5 4.5 5.5	dc dc dc	TBD 10 10	MHz
f	Operating Frequency of the Phase Detectors			2.5 4.5 5.5	dc dc dc	TBD 2 2	MHz
t_W	Output Pulse Width, ϕ_R, ϕ_V, and LD	f_R in Phase with f_V C_L = 50 pF	11, 12	2.5 4.5 5.5	TBD 20 16	TBD 100 90	ns
t_{TLH}, t_{THL}	Output Transition Times, ϕ_R, ϕ_V, LD, f_R, and f_V	C_L = 50 pF	11, 12	2.5 4.5 5.5	— — —	TBD 65 60	ns
C_{in}	Input Capacitance f_{in} OSC_{in}		— —	— —	— —	7 7	pF

* If lower frequency is desired, use wave shaping or higher amplitude sinusoidal signal in ac–coupled case. Also, see Figure 22 for dc decoupling.

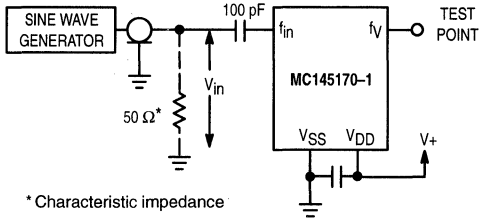


Figure 7. Test Circuit

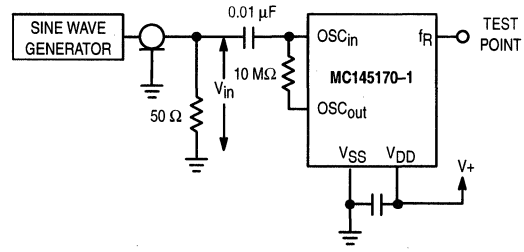


Figure 8. Test Circuit

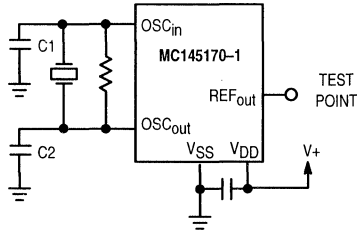


Figure 9. Test Circuit

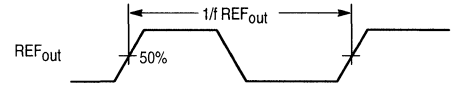


Figure 10. Switching Waveform

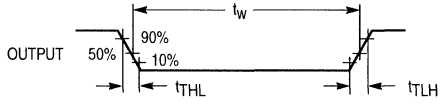


Figure 11. Switching Waveform

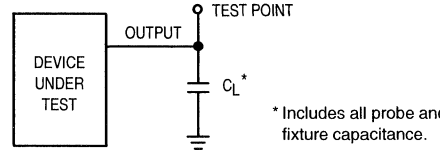


Figure 12. Test Circuit

PIN DESCRIPTIONS

DIGITAL INTERFACE PINS

D_{in}
Serial Data Input (Pin 5)

The bit stream begins with the most significant bit (MSB) and is shifted in on the low–to–high transition of CLK. The bit pattern is 1 byte (8 bits) long to access the C or configuration register, 2 bytes (16 bits) to access the N register, or 3 bytes (24 bits) to access the R register. Additionally, the R register can be accessed with a 15–bit transfer (see Table 1). An optional pattern which resets the device is shown in Figure 13. The values in the C, N, and R registers do not change during shifting because the transfer of data to the registers is controlled by $\overline{ENB}$.

The bit stream needs neither address nor steering bits due to the innovative BitGrabber registers. Therefore, all bits in the stream are available to be data for the three registers. Random access of any register is provided (i.e., the registers may be accessed in any sequence). Data is retained in the registers over a supply range of 2.5 to 5.5 V. The formats are shown in Figures 13, 14, 15, and 16.

D_{in} typically switches near 50% of V_{DD} to maximize noise immunity. This input can be directly interfaced to CMOS devices with outputs guaranteed to switch near rail–to–rail. When interfacing to NMOS or TTL devices, either a level shifter (MC74HC14A, MC14504B) or pull–up resistor of 1 to 10 kΩ must be used. Parameters to consider when sizing the resistor are worst–case I_{OL} of the driving device, maximum tolerable power consumption, and maximum data rate.

Table 1. Register Access
(MSBs are shifted in first, C0, N0, and R0 are the LSBs)

Number of Clocks	Accessed Register	Bit Nomenclature
4 + 5	(Reset)	
8	C Register	C7, C6, C5, . . ., C0
16	N Register	N15, N14, N13, . . ., N0
15 or 24	R Register	R14, R13, R12, . . ., R0
Other Values ≤ 32	None	
Values > 32	See Figures 24 — 31	

CLK
Serial Data Clock Input (Pin 7)

Low–to–high transitions on Clock shift bits available at D_{in}, while high–to–low transitions shift bits from D_{out}. The chip's 16–1/2–stage shift register is static, allowing clock rates down to dc in a continuous or intermittent mode.

Four clock cycles followed by five clock cycles are needed to reset the device; this is optional. Eight clock cycles are required to access the C register. Sixteen clock cycles are needed for the N register. Either 15 or 24 cycles can be used to access the R register (see Table 1 and Figures 13, 14, 15, and 16). For cascaded devices, see Figures 24 — 31.

CLK typically switches near 50% of V_{DD} and has a Schmitt–triggered input buffer. Slow CLK rise and fall times are allowed. See the last paragraph of **D_{in}** for more information.

NOTE

To guarantee proper operation of the power–on reset (POR) circuit, the CLK pin must be held at the potential of either the V_{SS} or V_{DD} pin during power up. That is, the CLK input should not be floated or toggled while the V_{DD} pin is ramping from 0 to at least 2.5 V. If control of the CLK pin is not practical during power up, the initialization sequence shown in Figure 13 must be used.

$\overline{ENB}$
Active–Low Enable Input (Pin 6)

This pin is used to activate the serial interface to allow the transfer of data to/from the device. When $\overline{ENB}$ is in an inactive high state, shifting is inhibited, D_{out} is forced to the high–impedance state, and the port is held in the initialized state. To transfer data to the device, $\overline{ENB}$ (which must start inactive high) is taken low, a serial transfer is made via D_{in} and CLK, and $\overline{ENB}$ is taken back high. The low–to–high transition on $\overline{ENB}$ transfers data to the C, N, or R register depending on the data stream length per Table 1.

NOTE

Transitions on $\overline{ENB}$ must not be attempted while CLK is high. This puts the device out of synchronization with the microcontroller. Resynchronization occurs when $\overline{ENB}$ is high and CLK is low.

This input is also Schmitt–triggered and switches near 50% of V_{DD}, thereby minimizing the chance of loading erroneous data into the registers. See the last paragraph of **D_{in}** for more information.

D_{out}
Three–State Serial Data Output (Pin 8)

Data is transferred out of the 16–1/2–stage shift register through D_{out} on the high–to–low transition of CLK. This output is a No Connect, unless used in one of the manners discussed below.

D_{out} could be fed back to an MCU/MPU to perform a wrap–around test of serial data. This could be part of a system check conducted at power up to test the integrity of the system's processor, PC board traces, solder joints, etc.

The pin could be monitored at an in–line QA test during board manufacturing.

Finally, D_{out} facilitates troubleshooting a system and permits cascading devices.

REFERENCE PINS

OSC_{in}/OSC_{out}
Reference Oscillator Input/Output (Pins 1, 2)

These pins form a reference oscillator when connected to terminals of an external parallel–resonant crystal. Frequency–setting capacitors of appropriate values as recommended by the crystal supplier are connected from each pin to ground (up to a maximum of 30 pF each, including stray capacitance). An external feedback resistor of 1 to 15 MΩ is connected directly across the pins to ensure linear operation of the amplifier. The required connections for the components are shown in Figure 9.

If desired, an external clock source can be ac coupled to OSC_{in}. A 0.01 µF coupling capacitor is used for measurement purposes and is the minimum size recommended for applications. An external feedback resistor of approximately 10 MΩ is required across the OSC_{in} and OSC_{out} pins in the ac–coupled case (see Figure 8). *OSC_{out} is an internal node on the device and should not be used to drive any loads* (i.e., OSC_{out} is unbuffered). However, the buffered REF_{out} is available to drive external loads.

The external signal level must be at least 1 V p–p; the maximum frequencies are given in the **Loop Specifications** table. These maximum frequencies apply for R Counter divide ratios as indicated in the table. For very small ratios, the maximum frequency is limited to the divide ratio times 2 MHz. (Reason: the phase/frequency detectors are limited to a maximum input frequency of 2 MHz.)

If an external source is available which swings rail–to–rail (V_{DD} to V_{SS}), then dc coupling can be used. In the dc–coupled case, no external feedback resistor is needed. OSC_{out} must be a No Connect to avoid loading an internal node on the device, as noted above. *For frequencies below 1 MHz, dc coupling must be used.* The R counter is a static counter and may be operated down to dc. However, wave shaping by a CMOS buffer may be required to ensure fast rise and fall times into the OSC_{in} pin. See Figure 22.

Each rising edge on the OSC_{in} pin causes the R counter to decrement by one.

REF_{out}
Reference Frequency Output (Pin 3)

This output is the buffered output of the crystal–generated reference frequency or externally provided reference source. This output may be enabled, disabled, or scaled via bits in the C register (see Figure 14).

REF_{out} can be used to drive a microprocessor clock input, thereby saving a crystal. Upon power up, the on–chip power–on–initialize circuit forces REF_{out} to the OSC_{in} divided–by–8 mode.

REF_{out} is capable of operation to 10 MHz; see the **Loop Specifications** table. Therefore, divide values for the reference divider are restricted to two or higher for OSC_{in} frequencies above 10 MHz.

If unused, the pin should be floated and should be disabled via the C register to minimize dynamic power consumption and electromagnetic interference (EMI).

COUNTER OUTPUT PINS

f_R
R Counter Output (Pin 9)

This signal is the buffered output of the 15–stage R counter. f_R can be enabled or disabled via the C register (patented). The output is disabled (static low logic level) upon power up. If unused, the output should be left disabled and unconnected to minimize interference with external circuitry.

The f_R signal can be used to verify the R counter's divide ratio. This ratio extends from 5 to 32,767 and is determined by the binary value loaded into the R register. Also, direct access to the phase detector via the OSC_{in} pin is allowed by choosing a divide value of 1 (see Figure 15). The maximum frequency which the phase detectors operate is 2 MHz. Therefore, the frequency of f_R must not exceed 2 MHz.

When activated, the f_R signal appears as normally low and pulses high.

f_V
N Counter Output (Pin 10)

This signal is the buffered output of the 16–stage N counter. f_V can be enabled or disabled via the C register (patented). The output is disabled (static low logic level) upon power up. If unused, the output should be left disabled and unconnected to minimize interference with external circuitry.

The f_V signal can be used to verify the N counter's divide ratio. This ratio extends from 40 to 65,535 and is determined by the binary value loaded into the N register. The maximum frequency which the phase detectors operate is 2 MHz. Therefore, the frequency of f_V must not exceed 2 MHz.

When activated, the f_V signal appears as normally low and pulses high.

LOOP PINS

f_{in}
Frequency Input (Pin 4)

This pin is a frequency input from the VCO. This pin feeds the on–chip amplifier which drives the N counter. This signal is normally sourced from an external voltage–controlled oscillator (VCO), and is ac–coupled into f_{in}. A 100 pF coupling capacitor is used for measurement purposes and is the minimum size recommended for applications (see Figure 7). The frequency capability of this input is dependent on the supply voltage as listed in the **Loop Specifications** table. For small divide ratios, the maximum frequency is limited to the divide ratio times 2 MHz. (Reason: the phase/frequency detectors are limited to a maximum frequency of 2 MHz.)

For signals which swing from at least the V_{IL} to V_{IH} levels listed in the **Electrical Characteristics** table, dc coupling may be used. Also, for low frequency signals (less than the minimum frequencies shown in the **Loop Specifications** table), dc coupling is a requirement. The N counter is a static counter and may be operated down to dc. However, wave shaping by a CMOS buffer may be required to ensure fast rise and fall times into the f_{in} pin. See Figure 22.

Each rising edge on the f_{in} pin causes the N counter to decrement by 1.

PD_{out}
Single–Ended Phase/Frequency Detector Output (Pin 13)

This is a three–state output for use as a loop error signal when combined with an external low–pass filter. Through use of a Motorola patented technique, the detector's dead zone has been eliminated. Therefore, the phase/frequency detector is characterized by a linear transfer function. The operation of the phase/frequency detector is described below and is shown in Figure 17.

POL bit (C7) in the C register = low (see Figure 14)

Frequency of $f_V > f_R$ or Phase of f_V Leading f_R: negative pulses from high impedance

Frequency of $f_V < f_R$ or Phase of f_V Lagging f_R: positive pulses from high impedance

Frequency and Phase of $f_V = f_R$: essentially high–impedance state; voltage at pin determined by loop filter

POL bit (C7) = high

Frequency of $f_V > f_R$ or Phase of f_V Leading f_R: positive pulses from high impedance

Frequency of $f_V < f_R$ or Phase of f_V Lagging f_R: negative pulses from high impedance

Frequency and Phase of $f_V = f_R$: essentially high–impedance state; voltage at pin determined by loop filter

This output can be enabled, disabled, and inverted via the C register. If desired, PD_{out} can be forced to the high–impedance state by utilization of the disable feature in the C register (patented).

ϕ_R and ϕ_V
Double–Ended Phase/Frequency Detector Outputs (Pins 14, 15)

These outputs can be combined externally to generate a loop error signal. Through use of a Motorola patented technique, the detector's dead zone has been eliminated. Therefore, the phase/frequency detector is characterized by a linear transfer function. The operation of the phase/frequency detector is described below and is shown in Figure 17.

POL bit (C7) in the C register = low (see Figure 14)

Frequency of $f_V > f_R$ or Phase of f_V Leading f_R: ϕ_V = negative pulses, ϕ_R = essentially high

Frequency of $f_V < f_R$ or Phase of f_V Lagging f_R: ϕ_V = essentially high, ϕ_R = negative pulses

Frequency and Phase of $f_V = f_R$: ϕ_V and ϕ_R remain essentially high, except for a small minimum time period when both pulse low in phase

POL bit (C7) = high

Frequency of $f_V > f_R$ or Phase of f_V Leading f_R: ϕ_R = negative pulses, ϕ_V = essentially high

Frequency of $f_V < f_R$ or Phase of f_V Lagging f_R: ϕ_R = essentially high, ϕ_V = negative pulses

Frequency and Phase of $f_V = f_R$: ϕ_V and ϕ_R remain essentially high, except for a small minimum time period when both pulse low in phase

These outputs can be enabled, disabled, and interchanged via the C register (patented).

LD
Lock Detector Output (Pin 11)

This output is essentially at a high level with narrow low–going pulses when the loop is locked (f_R and f_V of the same phase and frequency). The output pulses low when f_V and f_R are out of phase or different frequencies (see Figure 17).

This output can be enabled and disabled via the C register (patented). Upon power up, on–chip initialization circuitry disables LD to a static low logic level to prevent a false "lock" signal. If unused, LD should be disabled and left open.

POWER SUPPLY

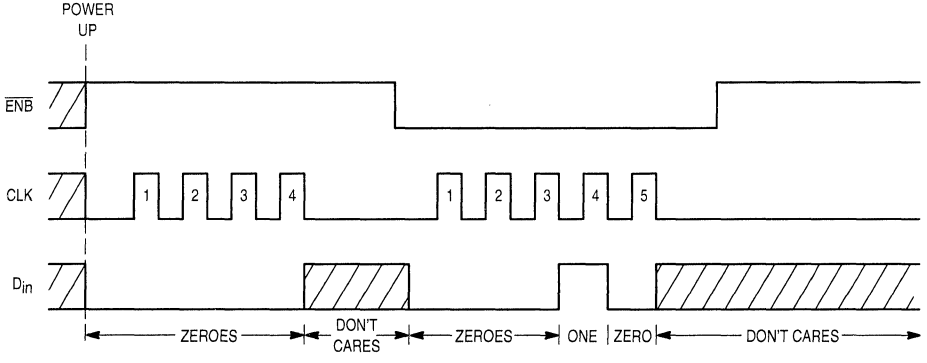
V_{DD}
Most Positive Supply Potential (Pin 16)

This pin may range from + 2.5 to 5.5 V with respect to V_{SS}.

For optimum performance, V_{DD} should be bypassed to V_{SS} using low–inductance capacitor(s) mounted very close to the device. Lead lengths on the capacitor(s) should be minimized. (The very fast switching speed of the device causes current spikes on the power leads.)

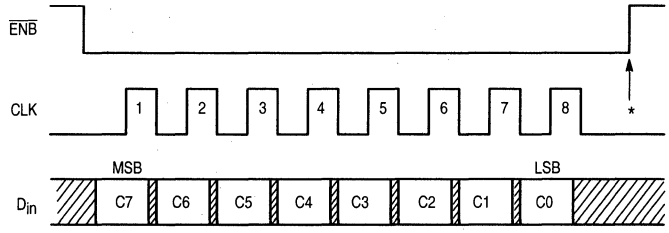
V_{SS}
Most Negative Supply Potential (Pin 12)

This pin is usually ground. For measurement purposes, the V_{SS} pin is tied to a ground plane.



NOTE: This initialization sequence must be used immediately after power up if control of the CLK pin is not possible. That is, if CLK (pin 7) toggles or floats upon power up, use the above sequence to reset the device.
Also, use this sequence if power is momentarily interrupted such that the supply voltage to the device is reduced to below 2.5 V, but not down to 0 V (for example, the supply drops down to 1 V). This is necessary because the on–chip power–on reset is only activated when the supply ramps up from 0 V.

Figure 13. Reset Sequence



* At this point, the new byte is transferred to the C register and stored. No other registers are affected.

2

C7 — POL: Selects the output polarity of the phase/frequency detectors. When set high, this bit inverts PD_{out} and interchanges the ϕ_R function with ϕ_V as depicted in Figure 17. Also see the phase detector output pin descriptions for more information. This bit is cleared low at power up.

C6 — PDA/B: Selects which phase/frequency detector is to be used. When set high, enables the output of phase/frequency detector A (PD_{out}) and disables phase/frequency detector B by forcing ϕ_R and ϕ_V to the static high state. When cleared low, phase/frequency detector B is enabled (ϕ_R and ϕ_V) and phase/frequency detector A is disabled with PD_{out} forced to the high–impedance state. This bit is cleared low at power up.

C5 — LDE: Enables the lock detector output when set high. When the bit is cleared low, the LD output is forced to a static low level. This bit is cleared low at power up.

C4 – C2, OSC2 – OSC0: Reference output controls which determine the REF_{out} characteristics as shown below. Upon power up, the bits are initialized such that $OSC_{in}/8$ is selected.

C4	C3	C2	REF_{out} Frequency
0	0	0	dc (Static Low)
0	0	1	OSC_{in}
0	1	0	$OSC_{in}/2$
0	1	1	$OSC_{in}/4$
1	0	0	$OSC_{in}/8$
1	0	1	$OSC_{in}/16$
1	1	0	$OSC_{in}/8$
1	1	1	$OSC_{in}/16$

C1 — f_VE: Enables the f_V output when set high. When cleared low, the f_V output is forced to a static low level. The bit is cleared low upon power up.

C0 — f_RE: Enables the f_R output when set high. When cleared low, the f_R output is forced to a static low level. The bit is cleared low upon power up.

Figure 14. C Register Access and Format (8 Clock Cycles are Used)

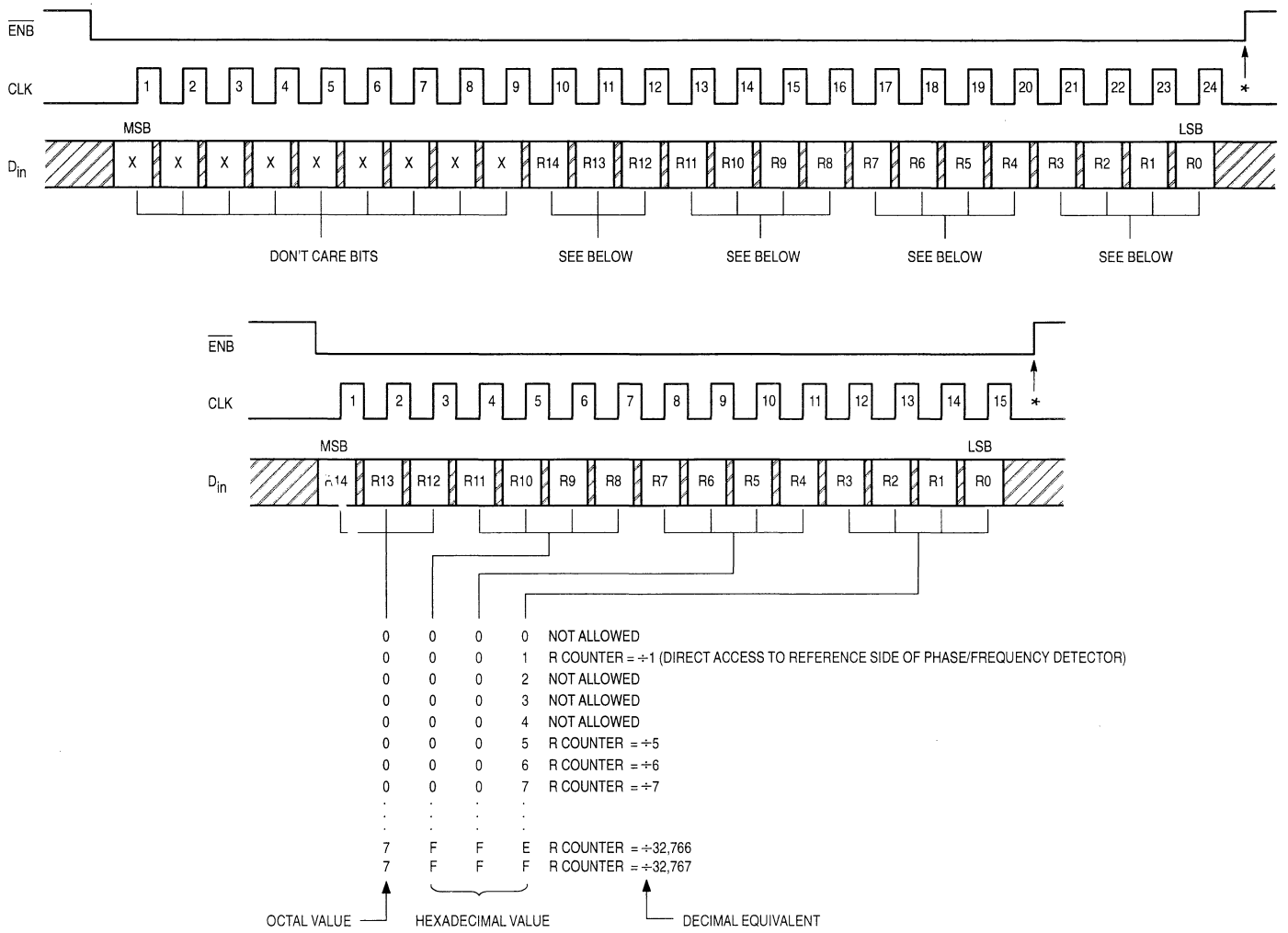
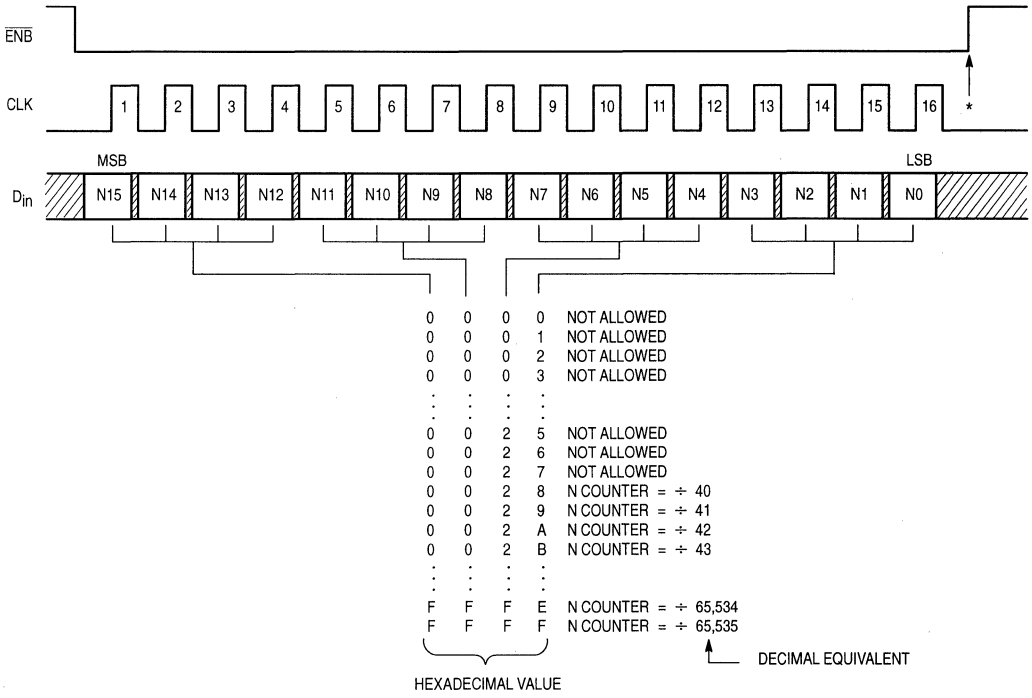


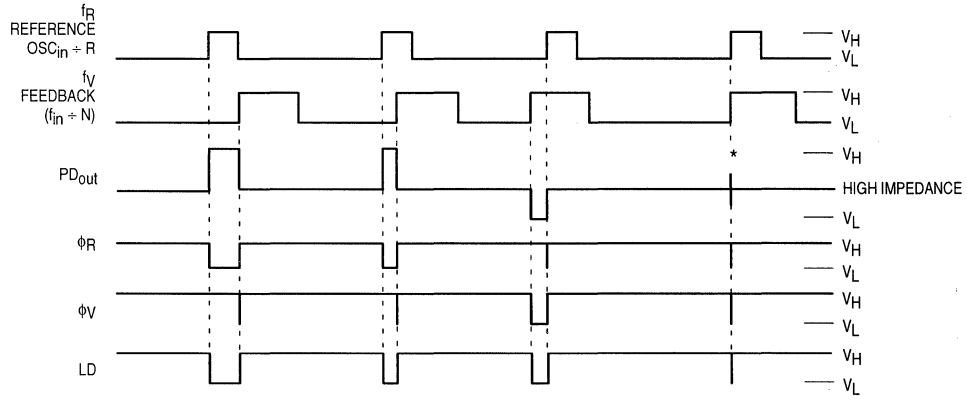
Figure 15. R Register Access and Formats (Either 24 or 15 Clock Cycles Can Be Used)

* At this point, the new data is transferred to the R register and stored. No other registers are affected.



* At this point, the two new bytes are transferred to the N register and stored. No other registers are affected. In addition, the N and R counters are jam–loaded and begin counting down together.

Figure 16. N Register Access and Format (16 Clock Cycles Are Used)



V_H = High voltage level
V_L = Low voltage level
*At this point, when both f_R and f_V are in phase, both the sinking and sourcing output FETs are turned on for a very short interval.
NOTE: The PD_{out} generates error pulses during out–of–lock conditions. When locked in phase and frequency, the output is high impedance and the voltage at that pin is determined by the low–pass filter capacitor. PD_{out}, ϕ_R, and ϕ_V are shown with the polarity bit (POL) = low; see Figure 14 for POL.

Figure 17. Phase/Frequency Detectors and Lock Detector Output Waveforms

DESIGN CONSIDERATIONS

CRYSTAL OSCILLATOR CONSIDERATIONS

The following options may be considered to provide a reference frequency to Motorola's CMOS frequency synthesizers.

Use of a Hybrid Crystal Oscillator

Commercially available temperature–compensated crystal oscillators (TCXOs) or crystal–controlled data clock oscillators provide very stable reference frequencies. An oscillator capable of CMOS logic levels at the output may be direct or dc coupled to OSC_{in}. If the oscillator does not have CMOS logic levels on the outputs, capacitive or ac coupling to OSC_{in} may be used (see Figure 8).

For additional information about TCXOs and data clock oscillators, please consult the latest version of the *eem Electronic Engineers Master Catalog,* the *Gold Book,* or similar publications.

Design an Off–Chip Reference

The user may design an off–chip crystal oscillator using discrete transistors or ICs specifically developed for crystal oscillator applications, such as the MC12061 MECL device. The reference signal from the MECL device is ac coupled to OSC_{in} (see Figure 18). For large amplitude signals (standard CMOS logic levels), dc coupling is used.

Use of the On–Chip Oscillator Circuitry

The on–chip amplifier (a digital inverter) along with an appropriate crystal may be used to provide a reference source frequency. A fundamental mode crystal, parallel resonant at the desired operating frequency, should be connected as shown in Figure 18.

The crystal should be specified for a loading capacitance (C_L) which does not exceed 20 pF when used at the highest operating frequencies listed in the **Loop Specifications** table. Larger C_L values are possible for lower frequencies. Assuming R1 = 0 Ω, the shunt load capacitance (C_L) presented across the crystal can be estimated to be:

$$C_L = \frac{C_{in}C_{out}}{C_{in} + C_{out}} + C_a + C_{stray} + \frac{C1 \bullet C2}{C1 + C2}$$

where

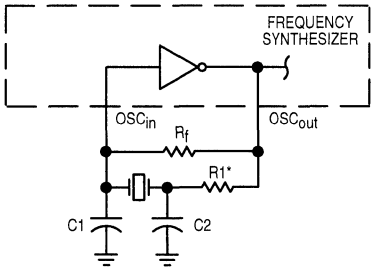
C_{in} = 5 pF (see Figure 19)
C_{out} = 6 pF (see Figure 19)
C_a = 1 pF (see Figure 19)
C1 and C2 = external capacitors (see Figure 18)
C_{stray} = the total equivalent external circuit stray capacitance appearing across the crystal terminals

The oscillator can be "trimmed" on–frequency by making a portion or all of C1 variable. The crystal and associated components must be located as close as possible to the OSC_{in} and OSC_{out} pins to minimize distortion, stray capacitance, stray inductance, and startup stabilization time. Circuit stray capacitance can also be handled by adding the appropriate stray value to the values for C_{in} and C_{out}. For this approach, the term C_{stray} becomes 0 in the above expression for C_L.

Power is dissipated in the effective series resistance of the crystal, R_e, in Figure 20. The maximum drive level specified by the crystal manufacturer represents the maximum stress that the crystal can withstand without damage or excessive shift in operating frequency. R1 in Figure 18 limits the drive level. The use of R1 is not necessary in most cases.

To verify that the maximum dc supply voltage does not cause the crystal to be overdriven, monitor the output frequency at the REF_{out} pin (OSC_{out} is not used because loading impacts the oscillator). The frequency should increase very slightly as the dc supply voltage is increased. An overdriven crystal decreases in frequency or becomes unstable with an increase in supply voltage. The operating supply voltage must be reduced or R1 must be increased in value if the overdriven condition exists. The user should note that the oscillator start–up time is proportional to the value of R1.

Through the process of supplying crystals for use with CMOS inverters, many crystal manufacturers have developed expertise in CMOS oscillator design with crystals. Discussions with such manufacturers can prove very helpful (see Table 2).



* May be needed in certain cases. See text.

Figure 18. Pierce Crystal Oscillator Circuit

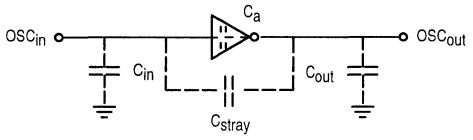
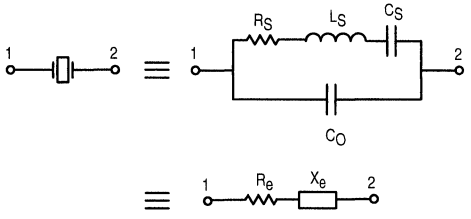


Figure 19. Parasitic Capacitances of the Amplifier and C_{stray}



NOTE: Values are supplied by crystal manufacturer (parallel resonant crystal).

Figure 20. Equivalent Crystal Networks

RECOMMENDED READING

Technical Note TN–24, Statek Corp.

Technical Note TN–7, Statek Corp.

E. Hafner, "The Piezoelectric Crystal Unit–Definitions and Method of Measurement", *Proc. IEEE,* Vol. 57, No. 2, Feb. 1969.

D. Kemper, L. Rosine, "Quartz Crystals for Frequency Control", *Electro–Technology,* June 1969.

P. J. Ottowitz, "A Guide to Crystal Selection", *Electronic Design*, May 1966.

D. Babin, "Designing Crystal Oscillators", *Machine Design*, March 7, 1985.

D. Babin, "Guidelines for Crystal Oscillator Design", *Machine Design*, April 25, 1985.

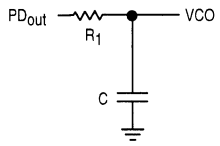
Table 2. Partial List of Crystal Manufacturers

Name	Address	Phone
United States Crystal Corp.	3605 McCart Ave., Ft. Worth, TX 76110	(817) 921–3013
Crystek Crystal	2351 Crystal Dr., Ft. Myers, FL 33907	(813) 936–2109
Statek Corp.	512 N. Main St., Orange, CA 92668	(714) 639–7810
Fox Electronics	5570 Enterprise Parkway, Ft. Myers, FL 33905	(813) 693–0099

NOTE: Motorola cannot recommend one supplier over another and in no way suggests that this is a complete listing of crystal manufacturers.

PHASE–LOCKED LOOP — LOW PASS FILTER DESIGN

(A)

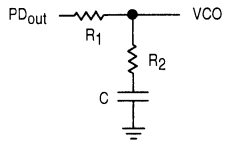


$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NR_1C}}$$

$$\zeta = \frac{N\omega_n}{2K_\phi K_{VCO}}$$

$$F(s) = \frac{1}{R_1sC + 1}$$

(B)

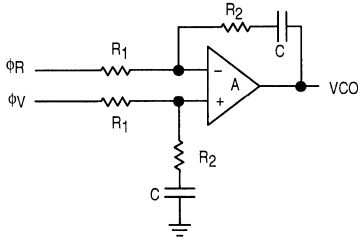


$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NC(R_1 + R_2)}}$$

$$\zeta = 0.5\,\omega_n \left(R_2C + \frac{N}{K_\phi K_{VCO}}\right)$$

$$F(s) = \frac{R_2sC + 1}{(R_1 + R_2)sC + 1}$$

(C)



$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NCR_1}}$$

$$\zeta = \frac{\omega_n R_2 C}{2}$$

ASSUMING GAIN A IS VERY LARGE, THEN:

$$F(s) = \frac{R_2sC + 1}{R_1sC}$$

NOTE:

For (C), R_1 is frequently split into two series resistors; each resistor is equal to R_1 divided by 2. A capacitor C_C is then placed from the midpoint to ground to further filter the error pulses. The value of C_C should be such that the corner frequency of this network does not significantly affect ω_n.

DEFINITIONS:

N = Total Division Ratio in Feedback Loop

K_ϕ (Phase Detector Gain) = $V_{DD}/4\pi$ V/radian for PD_{out}

K_ϕ (Phase Detector Gain) = $V_{DD}/2\pi$ V/radian for ϕ_V and ϕ_R

$$K_{VCO}\text{ (VCO Gain)} = \frac{2\pi\Delta f_{VCO}}{\Delta V_{VCO}}$$

For a nominal design starting point, the user might consider a damping factor $\zeta \approx 0.7$ and a natural loop frequency $\omega_n \approx (2\pi f_R/50)$ where f_R is the frequency at the phase detector input. Larger ω_n values result in faster loop lock times and, for similar sideband filtering, higher f_R–related VCO sidebands.

RECOMMENDED READING:

Gardner, Floyd M., *Phaselock Techniques (second edition).* New York, Wiley–Interscience, 1979.

Manassewitsch, Vadim, *Frequency Synthesizers: Theory and Design (second edition).* New York, Wiley–Interscience, 1980.

Blanchard, Alain, *Phase–Locked Loops: Application to Coherent Receiver Design.* New York, Wiley–Interscience, 1976.

Egan, William F., *Frequency Synthesis by Phase Lock.* New York, Wiley–Interscience, 1981.

Rohde, Ulrich L., *Digital PLL Frequency Synthesizers Theory and Design.* Englewood Cliffs, NJ, Prentice–Hall, 1983.

Berlin, Howard M., *Design of Phase–Locked Loop Circuits, with Experiments.* Indianapolis, Howard W. Sams and Co., 1978.

Kinley, Harold, *The PLL Synthesizer Cookbook.* Blue Ridge Summit, PA, Tab Books, 1980.

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AR254, Phase–Locked Loop Design Articles, Motorola Semiconductor Products, Inc., Reprinted with permission from *Electronic Design,* 1987.

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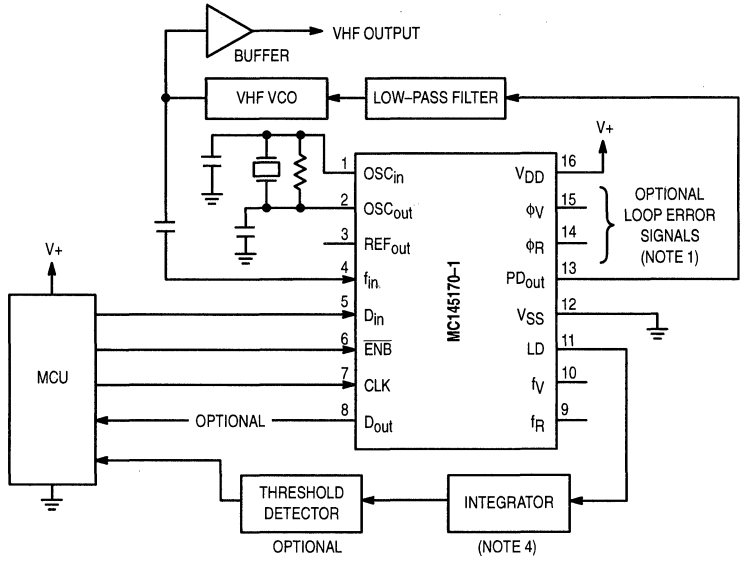
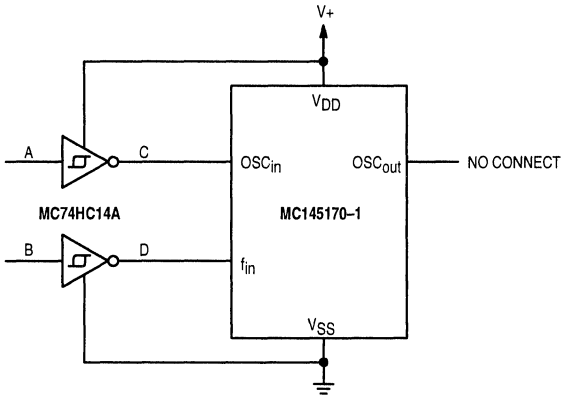


NOTES:

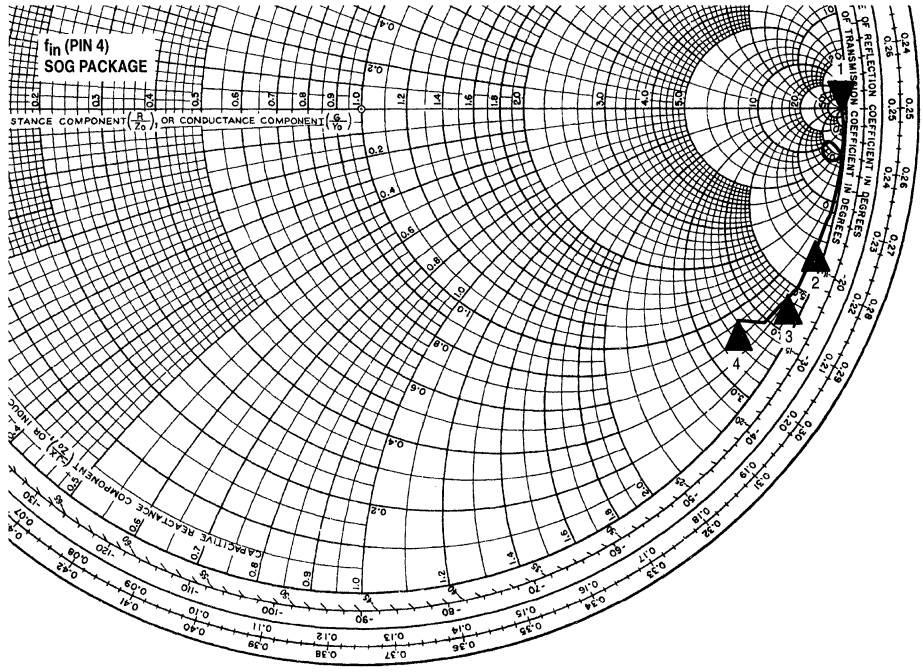
1. The ϕ_R and ϕ_V outputs are fed to an external combiner/loop filter. See the Phase–Locked Loop — Low–Pass Filter Design page for additional information. The ϕ_R and ϕ_V outputs swing rail–to–rail. Therefore, the user should be careful not to exceed the common mode input range of the op amp used in the combiner/loop filter.
2. For optimum performance, bypass the V_{DD} pin to V_{SS} (GND) with one or more low–inductance capacitors.
3. The R counter is programmed for a divide value = OSC_{in}/f_R. Typically, f_R is the tuning resolution required for the VCO. Also, the VCO frequency divided by f_R = N, where N is the divide value of the N counter.
4. May be an R–C low–pass filter.

Figure 21. Example Application



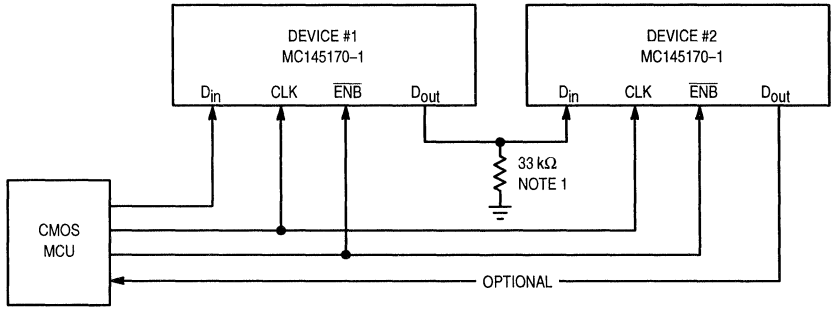
NOTE: The signals at Points A and B may be low–frequency sinusoidal or square waves with slow edge rates or noisy signal edges. At Points C and D, the signals are cleaned up, have sharp edge rates, and rail–to–rail signal swings. With signals as described at Points C and D, the MC145170–1 is guaranteed to operate down to a frequency as low as dc.

Figure 22. Low Frequency Operation Using dc Coupling



Marker	Frequency (MHz)	Resistance (Ω)	Reactance (Ω)	Capacitance (pF)
1	5	2390	– 5900	5.39
2	100	39.2	– 347	4.58
3	150	25.8	– 237	4.48
4	185	42.6	– 180	4.79

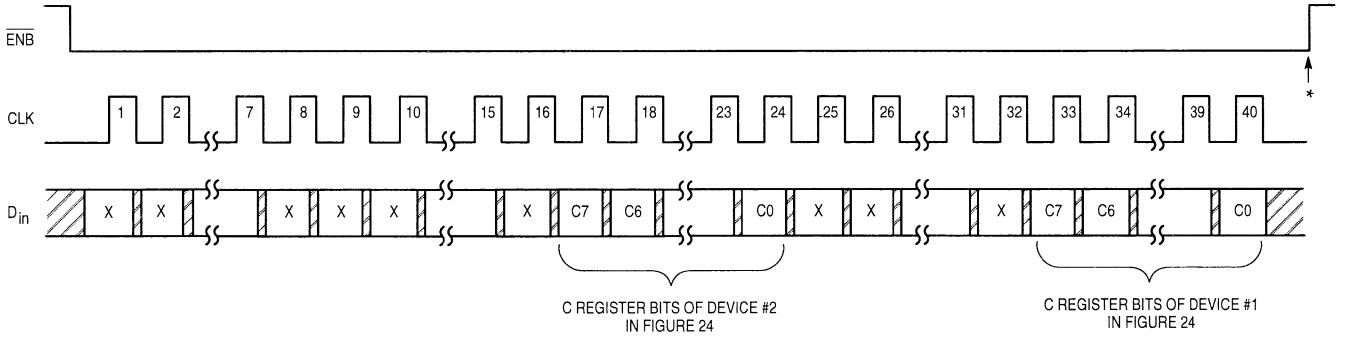
Figure 23. Input Impedance at fin — Series Format (R + jX) (5 MHz to 185 MHz)



NOTES:
1. The 33 kΩ resistor is needed to prevent the D_{in} pin from floating. (The D_{out} pin is a three–state output.)
2. See related Figures 25, 26, and 27.

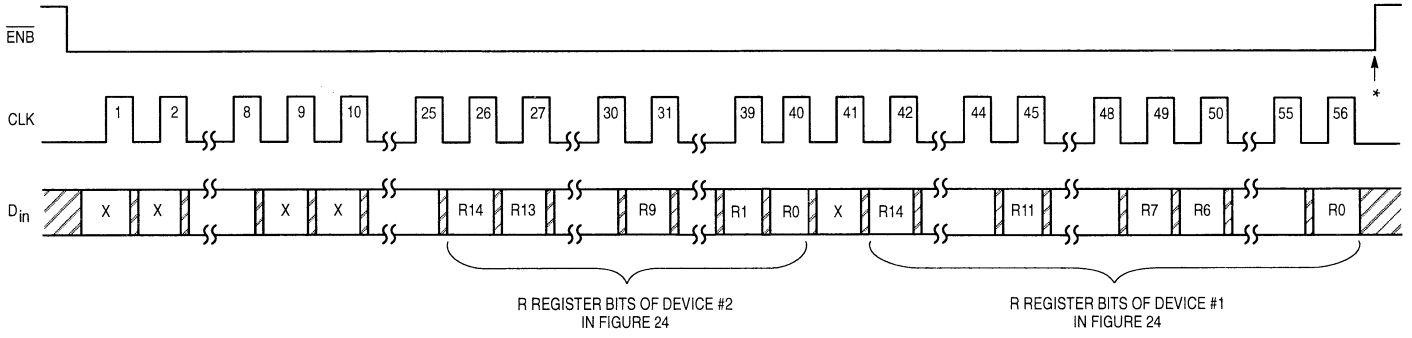
Figure 24. Cascading Two MC145170–1 Devices

Figure 25. Accessing the C Registers of Two Cascaded MC145170–1 Devices



*At this point, the new data is transferred to the C registers of both devices and stored. No other registers are affected.

Figure 26. Accessing the R Registers of Two Cascaded MC145170–1 Devices



*At this point, the new data is transferred to the R registers of both devices and stored. No other registers are affected.

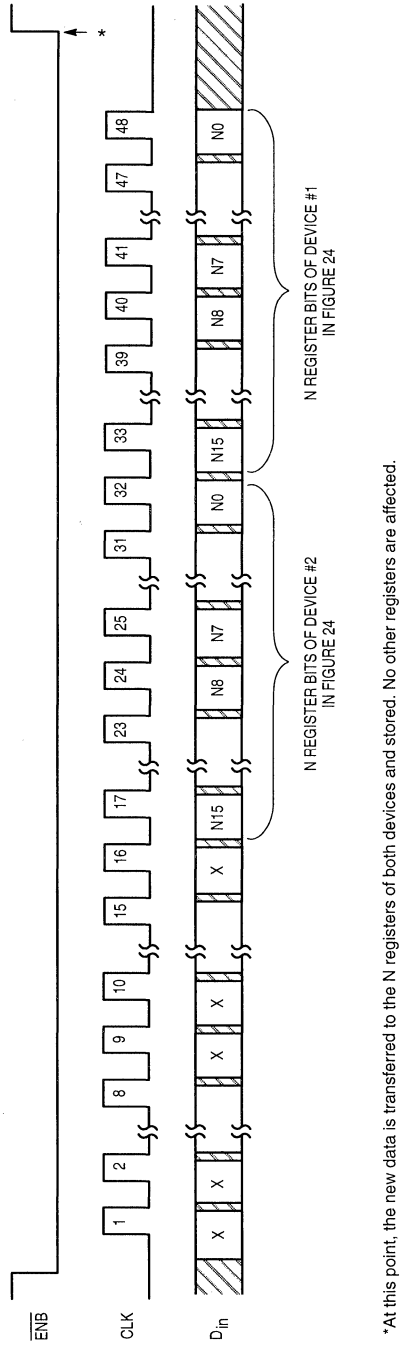
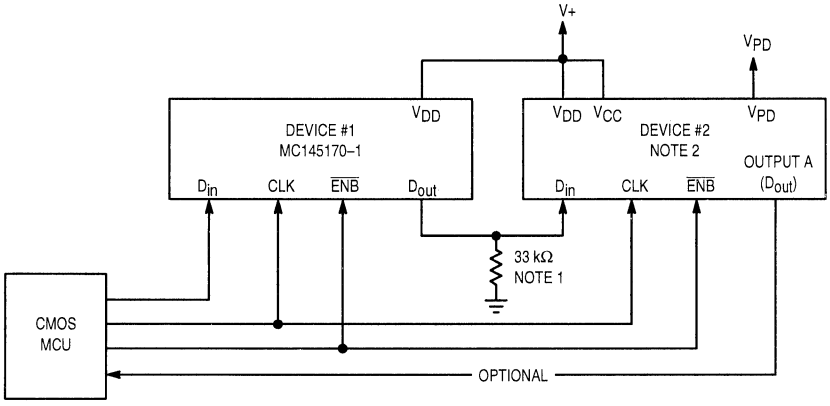


Figure 27. Accessing the N Registers of Two Cascaded MC145170–1 Devices



NOTES:
1. The 33 kΩ resistor is needed to prevent the D_{in} pin from floating. (The D_{out} pin is a three–state output.)
2. This PLL Frequency Synthesizer may be a MC145190, MC145191, MC145192, MC145200, or MC145201.
3. See related Figures 29, 30, and 31.

Figure 28. Cascading Two Different Device Types

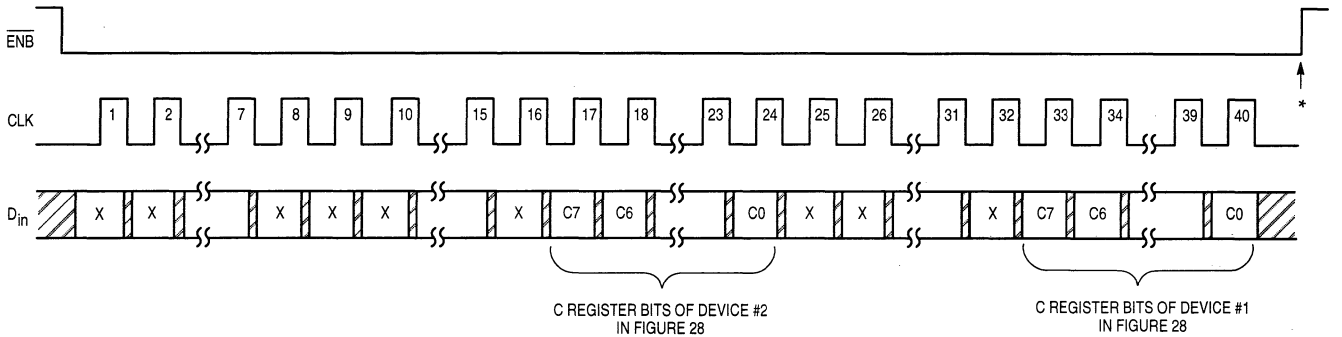


Figure 29. Accessing the C Registers of Two Different Device Types

*At this point, the new data is transferred to the C registers of both devices and stored. No other registers are affected.

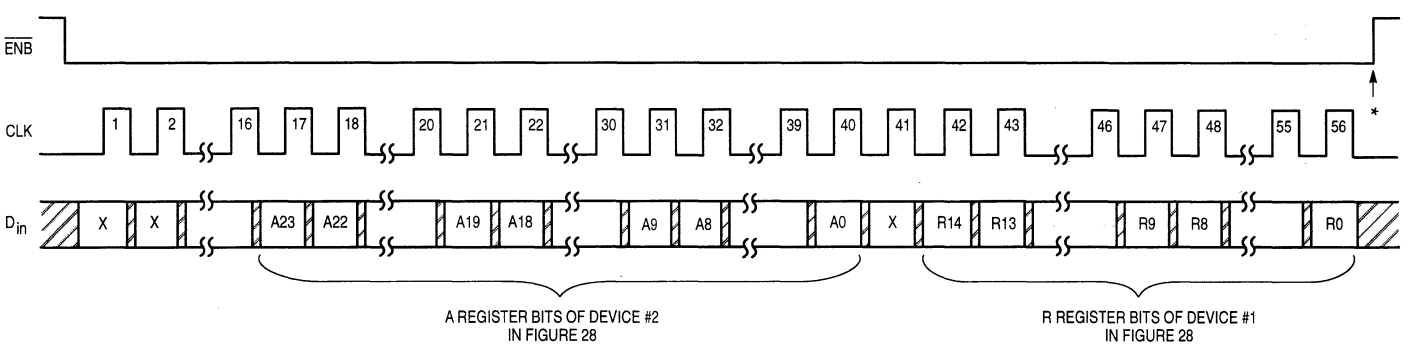


Figure 30. Accessing the A and R Registers of Two Different Device Types

*At this point, the new data is transferred to the A register of Device #2 and R register of Device #1 and stored. No other registers are affected.

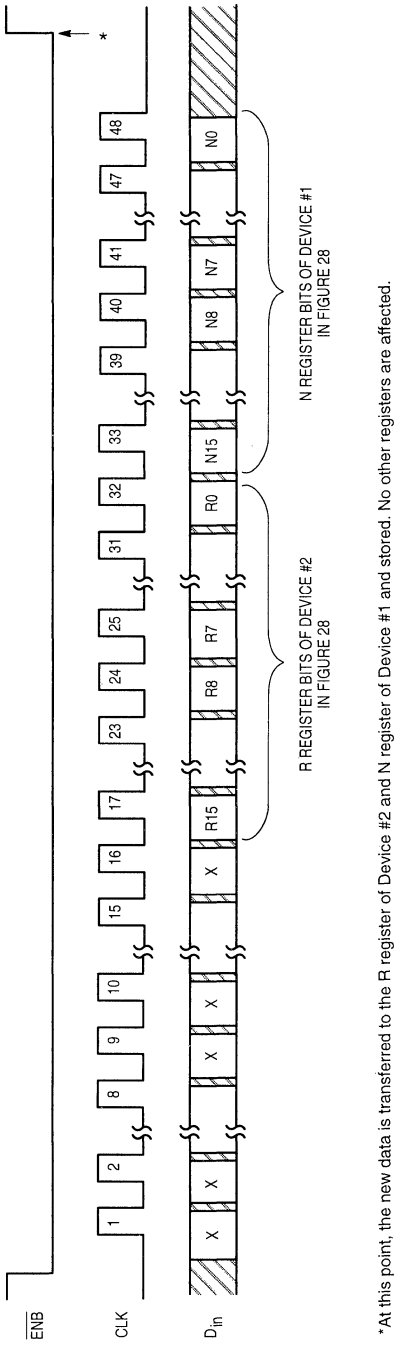


Figure 31. Accessing the R and N Registers of Two Different Device Types

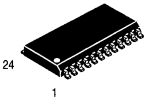
MC145173

2

Advance Information

Dual-Band PLL Frequency Synthesizer with ADC and Frequency Counter

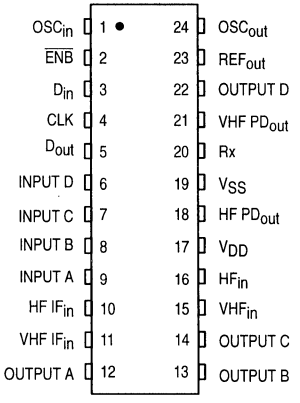
CMOS



DW SUFFIX
SOG PACKAGE
CASE 751E

ORDERING INFORMATION
MC145173DW SOG Package

PIN ASSIGNMENT



The MC145173 is a single–chip CMOS synthesizer with a four–wire serial interface for primary use in AM–FM broadcast receivers. The device also finds use in long–wave (LW) and short–wave (SW) receivers. Two inputs to a single high–speed N counter are provided, along with 2 phase detectors; one for a VHF loop up to 130 MHz, and another for an HF loop up to 40 MHz. The VHF phase detector has a current source/sink output and both detectors feature linear transfer functions (no dead zones). An external crystal ties across on–chip circuitry which drives a completely–programmable reference counter. Thus, a broad range of tuning resolution is possible. The crystal oscillator is buffered and fed to an open–drain output which is active in the HF mode only.

Due to the patented BitGrabber™ registers, address or steering bits are not needed in the serial data stream for random access of the registers. The serial port is byte–oriented to facilitate control via an MCU. Tuning across a band is accomplished with a two–byte transfer to the N register.

The 6–bit analog–to–digital converter (ADC) has two input channels. The converter is read via a one–byte transfer which includes an end–of–conversion (EOC) bit.

A 22–stage frequency counter is provided and accepts two IF (intermediate frequency) signals. Primary use for the frequency counter is for the seek or scan function on broadcast radio receivers. A proper frequency count ensures tuning of valid stations on their center frequencies. Reading the count is accomplished with a three–byte serial transfer which includes a count–complete (CC) bit.

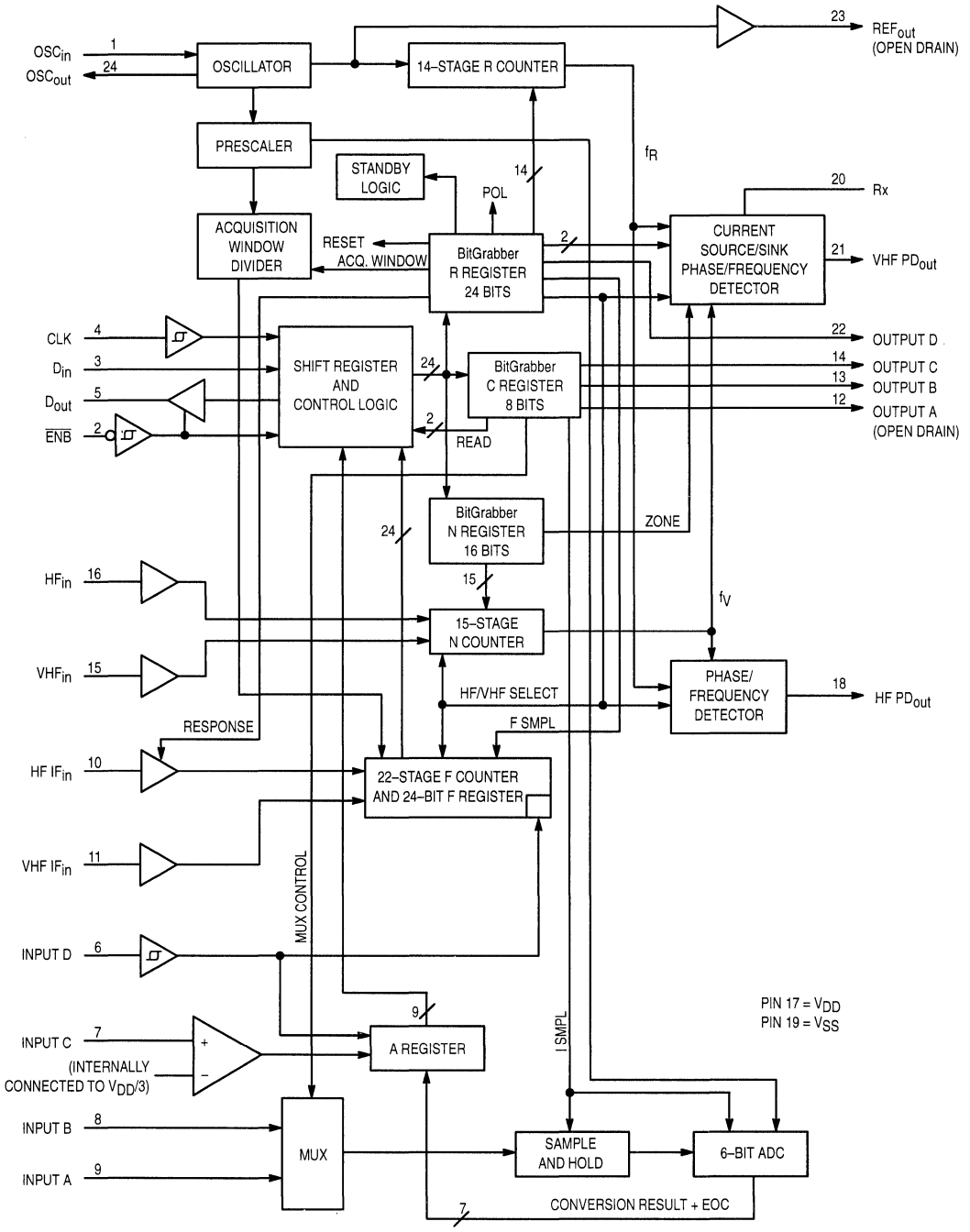
Four general purpose digital outputs are included. One of the outputs is open–drain; the others are totem–pole (push–pull). Two general purpose digital inputs are provided also. One input has a comparator with a switch point at 33% of V_{DD}.

- Operating Voltage Range: 4.5 to 5.5 V
- Maximum Operating Frequency: VHF_{in} = 130 MHz @ 210 mV p–p
  HF_{in} = 40 MHz @ 210 mV p–p
- Maximum Frequency of Reference Counter: 15 MHz
- Maximum Frequency of Frequency Counter: 20 MHz
- Maximum Supply Current: Operating Mode = 12 mA
  Standby Mode = 30 μA
- Approximate ADC Conversion Time: 360 μs
- Operating Temperature Range: – 40 to + 85°C
- R Counter Division Range: 1 and 5 to 16,383
- N Counter Division Range: 40 to 32,767
- Accommodates Downconversion or Upconversion Receiver Design for AM Broadcast Band
- Direct Interface to Motorola SPI Data Port
- Programmer's Guide Included in Datasheet

BitGrabber is a trademark of Motorola, Inc.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	− 0.5 to + 6.0	V
V_{in}	DC Input Voltage	− 0.5 to V_{DD} + 0.5	V
V_{out}	DC Output Voltage	− 0.5 to V_{DD} + 0.5	V
I_{in}	DC Input Current, per Pin	± 10	mA
I_{out}	DC Output Current, per Pin	± 20	mA
I_{DD}	DC Supply Current, V_{DD} and V_{SS} Pins	± 30	mA
P_D	Power Dissipation, per Package	300	mW
T_{stg}	Storage Temperature	− 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 seconds	260	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Descriptions section.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

For proper termination of unused pins, see the Pin Descriptions section.

DC ELECTRICAL CHARACTERISTICS (V_{DD} = 4.5 to 5.5 V, Voltages Referenced to V_{SS}, T_A = −40 to +85°C)

Symbol	Parameter	Test Condition	Guaranteed Limit	Unit
V_{IL}	Maximum Low–Level Input Voltage (D_{in}, CLK, $\overline{ENB}$)		0.25 x V_{DD}	V
V_{IH}	Minimum High–Level Input Voltage (D_{in}, CLK, $\overline{ENB}$)		0.65 x V_{DD}	V
V_{IL}	Maximum Low–Level Input Voltage (Input D, HF IF_{in}, VHF IF_{in}, HF_{in}, VHF_{in}, OSC_{in})	dc coupled	0.3 x V_{DD}	V
V_{IH}	Minimum High–Level Input Voltage (Input D, HF IF_{in}, VHF IF_{in}, HF_{in}, VHF_{in}, OSC_{in})	dc coupled	0.7 x V_{DD}	V
V_{Hys}	Minimum Hysteresis Voltage (CLK, $\overline{ENB}$)		0.3	V
V_{TH}	Threshold Voltage (INPUT C)	V_{in} Ramped Down from V_{DD}	0.28 x V_{DD} to 0.38 x V_{DD}	V
V_{OL}	Maximum Low–Level Output Voltage (D_{out}, OUTPUT A, OUTPUT B, OUTPUT C, OUTPUT D, HF PD_{out})	I_{out} = 20 μA	0.1	V
V_{OH}	Minimum High–Level Output Voltage (D_{out}, OUTPUT B, OUTPUT C, OUTPUT D, HF PD_{out}, REF_{out})	I_{out} = −20 μA	V_{DD} − 0.1	V
I_{OL}	Minimum Low–Level Output Current (HF PD_{out})	V_{out} = 0.4 V	0.36	mA
I_{OH}	Minimum High–Level Output Current (HF PD_{out})	V_{out} = V_{DD} − 0.4 V	− 0.36	mA
I_{OL}	Minimum Low–Level Output Current (D_{out})	V_{out} = 0.4 V	1.6	mA
I_{OH}	Minimum High–Level Output Current (D_{out})	V_{out} = V_{DD} − 0.4 V	− 1.6	mA
I_{OL}	Minimum Low–Level Output Current (OUTPUT B, OUTPUT C, OUTPUT D)	V_{out} = 1.0 V	2.0	mA
I_{OH}	Minimum High–Level Output Current (OUTPUT B, OUTPUT C, OUTPUT D)	V_{out} = V_{DD} − 1.0 V	− 2.0	mA
I_{OL}	Minimum Low–Level Output Current (OUTPUT A)	V_{out} = 1.0 V	2.0	mA
I_{OH}	Minimum High–Level Output Current (REF_{out})	V_{out} = V_{DD} − 1.0 V	− 1.75	mA
I_{in}	Maximum Input Leakage Current (D_{in}, CLK, $\overline{ENB}$, OSC_{in}, INPUT A, INPUT B, INPUT C, INPUT D)	V_{in} = V_{DD} or V_{SS}, Device NOT in Standby**	± 1.0	μA
I_{in}	Maximum Input Current (HF_{in}, VHF_{in}, HF IF_{in}, VHF IF_{in})	V_{in} = V_{DD} or V_{SS}, Device NOT in Standby	± 120	μA
I_{OZ}	Maximum Output Leakage Current (HF PD_{out})	V_{out} = V_{DD} or V_{SS}, Output in High–Impedance State	± 200	nA
I_{OZ}	Maximum Output Leakage Current (VHF PD_{out})	V_{out} = 1.75 or V_{DD} − 1.5 V, Output in High–Impedance State	± 200	nA
I_{OZ}	Maximum Output Leakage Current (REF_{out}, OUTPUT A, D_{out})	V_{out} = V_{DD} or V_{SS}, Output in High–Impedance State	± 2	μA

Continued on next page.

** While in Standby, the OSC_{in} pin is pulled low by a weak on–chip FET.

DC ELECTRICAL CHARACTERISTICS (continued) (V_{DD} = 4.5 to 5.5 V, Voltages Referenced to V_{SS}, T_A = −40 to +85°C)

Symbol	Parameter	Test Condition	Guaranteed Limit	Unit
I_{STBY}	Maximum Standby Supply Current	V_{in} on D_{in}, CLK, INPUT A, INPUT B, INPUT C, INPUT D = V_{DD} or V_{SS}; V_{in} on $\overline{ENB}$ = V_{DD}; V_{in} on OSC_{in}, HF IF_{in}, VHF IF_{in} = V_{SS} or Floating (ac coupled); V_{in} on HF_{in} = V_{DD} or V_{SS} or Floating (ac coupled); V_{in} on VHF_{in} = Floating (ac coupled); D_{out} tied to V_{DD} or V_{SS} through 100 kΩ resistor; Other Outputs Open	30	µA
I_{dd}	Maximum Operating Supply Current	V_{in} on D_{in}, CLK, INPUT A, INPUT B, INPUT C, INPUT D = V_{DD} or V_{SS}; D_{out} tied to V_{DD} or V_{SS} through 100 kΩ resistor; V_{in} on $\overline{ENB}$ = V_{DD}; OSC_{in} = 10.35 MHz @ 1 V p–p; VHF_{in} = 120 MHz @ 210 mV p–p; VHF IF_{in} = 10.7 MHz @ 210 mV p–p	12	mA

ANALOG CHARACTERISTICS — CURRENT SOURCE/SINK OUTPUT — VHF PD_{out}

(I_{out} ≤ 2.5 mA, V_{DD} = 4.5 to 5.5 V, Voltages Referenced to V_{SS})

Parameter	Test Condition	Guaranteed Limit	Unit
Maximum Source Current Variation (Part–to–Part)	V_{out} = 0.5 x V_{DD}	± 20	%
Maximum Sink–vs–Source Mismatch (Note 3)	V_{out} = 0.5 x V_{DD}	12	%
Output Voltage Range (Note 3)	I_{out} variation ≤ 20%	1.25 to V_{DD} – 1.25 V	V

NOTES:
4. Percentages calculated using the following formula: (Maximum Value – Minimum Value)/Maximum Value.
5. See Rx Pin Description for external resistor value.
6. This parameter is guaranteed for any specific temperature within – 40 to +85°C.

ADC CHARACTERISTICS (T_A = – 40 to 85°C, V_{DD} = 4.5 to 5.5 V, f_{OSC} = 9.5 to 10.4 MHz)

Parameter	Test Condition	Guaranteed Limit	Unit
Resolution		6	Bits
Conversion Time	Per Figure 1	3584	OSC_{in} Cycles
Maximum Nonlinearity	V_{in} = V_{SS} + (0.1 x V_{DD}) to V_{DD} – (0.09 x V_{DD})	±1.5	LSBs

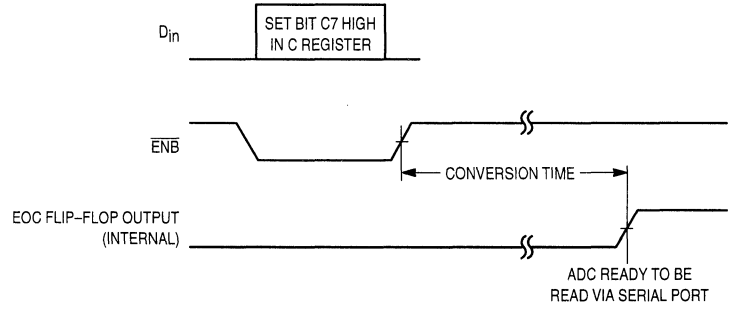


Figure 1.

AC INTERFACE CHARACTERISTICS

(V_{DD} = 4.5 to 5.5 V, T_A = – 40 to + 85°C, C_L = 50 pF, Input $t_r = t_f$ = 10 ns unless otherwise indicated)

Symbol	Parameter	Figure #	Guaranteed Limit	Unit
f_{clk}	Serial Data Clock Frequency (Note: Refer to CLK t_w below)	2	dc to 2.1	MHz
t_{PLH}, t_{PHL}	Maximum Propagation Delay, CLK to D_{out}	2, 8	150	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay, $\overline{ENB}$ to Output B, Output C, Output D	6, 8	300	ns
t_{PLZ}, t_{PZL}	Maximum Propagation Delay, $\overline{ENB}$ to Output A	7, 9	300	ns
t_{PLZ}, t_{PHZ}	Maximum Disable Time, D_{out} Active to High Impedance	3, 9	400	ns
t_{PZL}, t_{PZH}	Access Time, D_{out} High Impedance to Active	3, 9	0 to 200	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, D_{out} CL = 50 pF	2, 8	100	ns
	CL = 200 pF	2, 8	400	ns
C_{in}	Maximum Input Capacitance – D_{in}, $\overline{ENB}$, CLK		10	pF
C_{out}	Maximum Output Capacitance – D_{out}		10	pF

TIMING REQUIREMENTS (T_A = –40 to +85°C, Input $t_r = t_f$ = 10 ns unless otherwise indicated)

Symbol	Parameter	Figure #	Guaranteed Limit	Unit
t_{su}, t_h	Minimum Setup and Hold Times, D_{in} vs CLK	4	100	ns
t_{su}, t_h, t_{rec}	Minimum Setup, Hold, and Recovery Times, $\overline{ENB}$ vs CLK	5	200	ns
$t_{w(H)}$	Minimum Inactive–High Pulse Width, $\overline{ENB}$	5	600	ns
t_w	Minimum Pulse Width, CLK	2	238	ns
t_r, t_f	Maximum Input Rise and Fall Times, CLK (Source Impedance ≤ 5 kΩ)	2	50	µs

AC ELECTRICAL CHARACTERISTICS (V_{DD} = 4.5 to 5.5 V, T_A = –40 to +85°C)

Symbol	Parameter	Test Condition	Figure #	Guaranteed Range		Unit
				Min	Max	
f_{in}	Input Frequency, HF_{in}	V_{in} ≥ 210 mV p–p Sine Wave, N Counter set to divide ratio such that f_V ≤ 1 MHz (Note 1)	10	10 (Note 4)	40	MHz
		V_{in} ≥ 2.2 V p–p Sine Wave, N Counter same as above	10	1	40	MHz
f_{in}	Input Frequency, VHF_{in}	V_{in} ≥ 210 mV p–p Sine Wave, N Counter set to divide ratio such that f_V ≤ 1 MHz (Note 1)	11	40 (Note 4)	130	MHz
f_{in}	Input Frequency, OSC_{in} Externally driven with ac–coupled signal (Note 2)	V_{in} ≥ 1.0 V p–p Sine Wave, R Counter set to divide ratio such that f_R ≤ 1 MHz (Note 3)	12	2 (Note 4)	15	MHz
f_{XTAL}	Crystal Frequency, OSC_{in} and OSC_{out} (Note 2)	C1 ≤ 30 pF, C2 ≤ 30 pF, Includes Stray Capacitance, R Counter set to divide ratio such that f_R ≤ 1 MHz (Note 3)	13	2	15	MHz
f_{in}	Input Frequency, HF IF_{in}	V_{in} ≥ 85 mV p–p Sine Wave, K bit cleared low or set high	10	400	500	kHz
f_{in}	Input Frequency, VHF IF_{in}	V_{in} ≥ 85 mV p–p Sine Wave	10	8 (Note 4)	20	MHz
f_{out}	Output Frequency, REF_{out}	C_L = 20 pF, V_{out} ≥ 1.5 V p–p	14, 15	dc	10.4	MHz

NOTES:

1. f_V is the output signal of the N Counter.
2. The ADC is guaranteed over an OSC_{in} range of 9.5 to 10.4 MHz only.
3. f_R is the output signal of the R Counter.
4. For operation below this frequency, use dc coupling with a signal level of at least V_{IL} to V_{IH}. See Pin Description.

SWITCHING WAVEFORMS

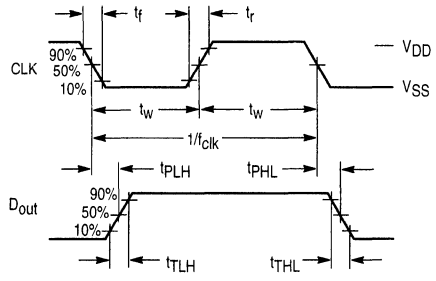


Figure 2.

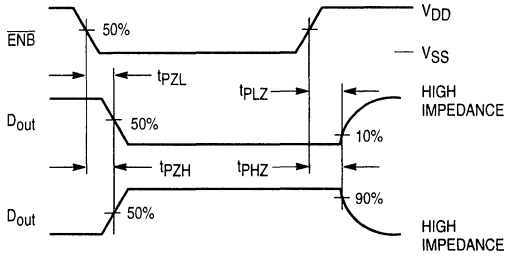


Figure 3.

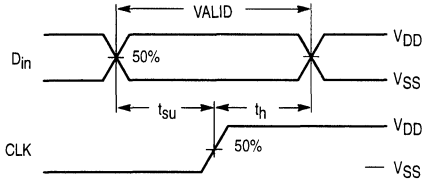


Figure 4.

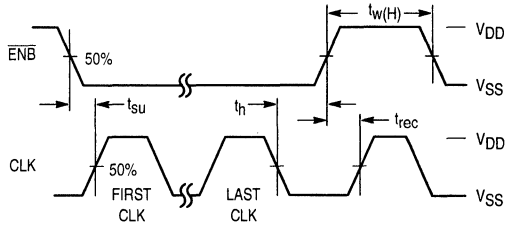


Figure 5.

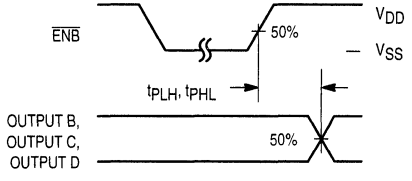


Figure 6.

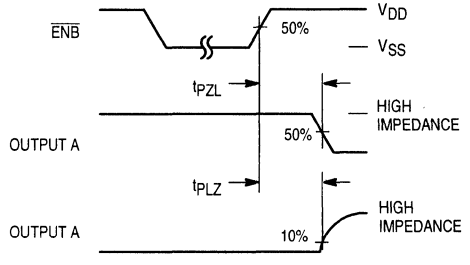
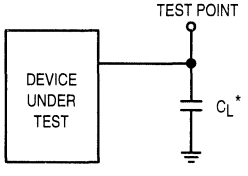
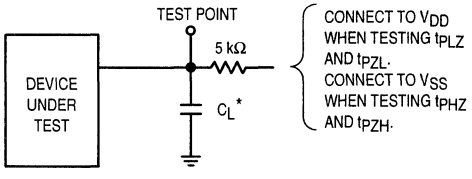


Figure 7.



*Includes all probe and fixture capacitance.

Figure 8. Test Circuit



*Includes all probe and fixture capacitance.

Figure 9. Test Circuit

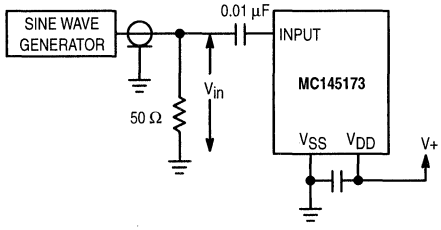


Figure 10. Test Circuit

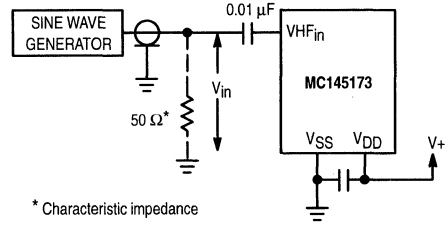


Figure 11. Test Circuit

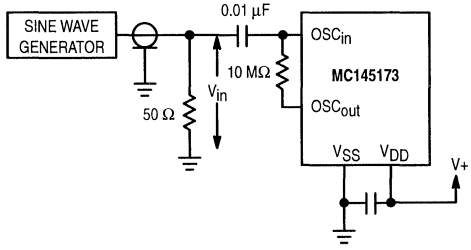


Figure 12. Test Circuit

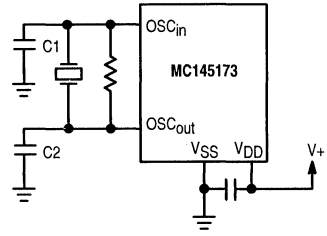


Figure 13. Test Circuit

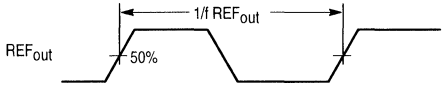


Figure 14. Switching Waveform

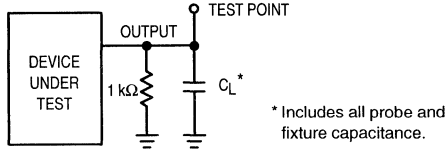


Figure 15. Test Circuit

PIN DESCRIPTIONS

DIGITAL INTERFACE PINS

D_{in}
Serial Data Input (Pin 3)

The bit stream begins with the most significant bit (MSB) and is shifted in on the low–to–high transition of CLK. The bit pattern is 1 byte (8 bits) long to access the C register, 2 bytes (16 bits) to access the N register, or 3 bytes (24 bits) to access the R register. (See Table 1.) The values in the C, N, and R registers do not change during shifting because the transfer of data to the registers is controlled by $\overline{ENB}$.

The bit stream needs neither address nor steering bits due to the innovative BitGrabber registers. Therefore, all bits in the stream are available to be data for the three registers. Random access of any register is provided (i.e., the registers may be accessed in any sequence). Data is retained in the registers over a supply range of 4.5 to 5.5 V. The formats are shown in Figures 17, 18, and 20.

D_{in} typically switches near 45% of V_{DD} for good noise immunity. This input can be directly interfaced to CMOS devices with outputs guaranteed to switch near rail–to–rail. When interfacing to NMOS or TTL devices, either a level shifter (MC74HC14A, MC14504B) or pull–up resistor of 1 to 10 kΩ must be used. Parameters to consider when sizing the resistor are worst–case I_{OL} of the driving device, maximum tolerable power consumption, and maximum data rate.

Table 1Write–Only Registers
(MSBs are shifted in first, C0, N0, and R0 are the LSBs)

Number of Clocks	Accessed Register	Bit Nomenclature
8	C Register	C7, C6, C5, . . ., C0
16	N Register	N15, N14, N13, . . ., N0
24	R Register	R23, R22, R21, . . ., R0
Other Values ≤ 32	Not Allowed	
Values > 32	Not Allowed	

Table 2Read–Only Registers
(MSBs are shifted out first; A7 and F23 are the MSBs)

Number of Clocks	Register	Bit Nomenclature
8, 9, or 16	A Register	A7, A6, A5, . . ., A0, A#
24	F Register	F23, F22, F21, . . ., F0

CLK
Serial Data Clock Input (Pin 4)

Low–to–high transitions on Clock shift bits available at D_{in}, while high–to–low transitions shift bits from D_{out}. The chip's 24–1/2–stage shift register is static, allowing clock rates down to dc in a continuous or intermittent mode.

Eight clock cycles are required to access the C register. Sixteen clock cycles are needed for the N register. 24 cycles are used to access the R register. (See Table 1 and Figures 17, 18, and 20.)

The A register is read using 8, 9, or 16 clock cycles. The F register is read using 24 clocks. (See Table 2 and Figures 21 and 22.)

CLK typically switches near 45% of V_{DD} and has a Schmitt–triggered input buffer. See the last paragraph of **D_{in}** for more information.

NOTE

To guarantee proper operation of the power–on reset (POR) circuit, the CLK pin must be held at the potential of either the V_{SS} or V_{DD} pin during power up. That is, the CLK input should not be floated or toggled while the V_{DD} pin is ramping from 0 to at least 4.5 V. If control of the CLK pin is not practical during power up, then the RST bit in the R Register must be utilized. See the R Register Bits section.

$\overline{ENB}$
Active–Low Enable Input (Pin 2)

This pin is used to activate the serial interface to allow the transfer of data to/from the device. When $\overline{ENB}$ is in an inactive high state, shifting is inhibited, D_{out} is forced to the high–impedance state, and the port is held in the initialized state. To transfer data to and from the device, $\overline{ENB}$ (which must start inactive high) is taken low, a serial transfer is made via D_{in}, D_{out}, and CLK, and $\overline{ENB}$ is taken back high. The low–to–high transition on $\overline{ENB}$ transfers data to the C, N, or R write–only registers depending on the data stream length per Table 1.

To minimize standby current, $\overline{ENB}$ must be high.

CAUTION

Transitions on $\overline{ENB}$ must not be attempted while CLK is high. This puts the device out of synchronization with the microcontroller. Resynchronization occurs when $\overline{ENB}$ is high and CLK is low.

This input is also Schmitt–triggered and switches near 45% of V_{DD}, thereby minimizing the chance of loading erroneous data into the registers. See the last paragraph of **D_{in}** for more information.

D_{out}
Three–State Serial Data Output (Pin 5)

Data is transferred out of the 24–1/2 stage shift register through D_{out} on the high–to–low transition of CLK. The bit stream begins with the MSB. The bit pattern is 1 byte, 9 bits, or 2 bytes long to read the A register. The F register's data is contained in 3 bytes. (See Table 2.)

Before the A register can be read, the Read A bit must be set in the C register. Likewise, the Read F bit must be set to read the F register.

To minimize supply current during the standby state, the D_{out} pin should not be floated. A pull–down resistor to V_{SS} or pull–up resistor to V_{DD} should be used. The value can be 50 kΩ to 100 kΩ.

GENERAL–PURPOSE DIGITAL I/O PINS

Input C
Digital Input (Pin 7)

Input C is a general–purpose digital input which may be used for MCU port expansion. The state of this input is indicated by the In C bit in the A register. (See Figure 21.)

The switch point is precisely controlled by use of a comparator. The reference for the comparator is internally set to approximately 33% of V_{DD}. The input has a small amount of hysteresis voltage (approximately 50 mV).

If not used, this pin should be tied to V_{DD} or V_{SS}.

Input D
Digital Input (Pin 6)

Input D is a general–purpose digital input which may be used for MCU port expansion. The state of this input is indicated by the In D bit in both the A and F registers. That is, the state of the pin may be read from either register. (See Figures 21 and 22.)

This pin is a standard CMOS input with a switch point at approximately 50% of V_{DD}. Input D has a hysteresis voltage of approximately 600 mV.

If not used, this pin should be tied to V_{DD} or V_{SS}.

Output A
Open–Drain Digital Output (Pin 12)

Output A is a general–purpose digital output which may be used for MCU port expansion. An N–channel MOSFET tied to V_{SS} is used to drive this open–drain output. Thus, an external pull–up device is required at this pin. The state of this output is determined by the Out A bit in the C register. (See Figure 17.)

Upon power–up, this pin is low. If not used, Output A should be tied to V_{SS} or floated.

Output B
Digital Output (Pin 13)

Output B is a general–purpose digital output which may be used for MCU port expansion. This is a standard totem–pole (push–pull) CMOS output. The state of this output is determined by the Out B bit in the C register. (See Figure 17.)

Upon power–up, this pin is low. If not used, Output B should be floated.

Output C
Digital Output (Pin 14)

Output C is a general–purpose digital output which may be used for MCU port expansion. This is a standard totem–pole (push–pull) CMOS output. The state of this output is determined by the Out C bit in the C register. (See Figure 17.)

Upon power–up, this pin is low. If not used, Output C should be floated.

Output D
Digital Output (Pin 22)

Output D is a general–purpose digital output which may be used for MCU port expansion. This is a standard totem–pole (push–pull) CMOS output. The state of this output is determined by the Out D bit in the R register. (See Figure 18.)

Upon power–up, this pin is low. If not used, Output D should be floated.

ADC INPUT PINS

Input A, Input B
Analog Inputs (Pins 9, 8)

These are inputs to the 2–channel multiplexer which feeds the 6–bit analog–to–digital converter (ADC). The selected channel is determined by the Chan bit in the C register.

Each pin is a high–impedance input which appears as a mostly–capacitive load of approximately 6 pF.

If not used, these pins should be tied to V_{SS} or V_{DD}.

REFERENCE PINS

OSC_{in}/OSC_{out}
Reference Oscillator Input/Output (Pins 1, 24)

These pins form a reference oscillator when connected to terminals of an external parallel–resonant crystal. Frequency–setting capacitors of appropriate values as recommended by the crystal supplier are connected from each pin to ground (up to a maximum of 30 pF each, including stray capacitance). An external feedback resistor of 1 to 10 MΩ is connected directly across the pins to ensure linear operation of the amplifier. The MC145173 is designed to operate with crystals from 2 to 15 MHz. However, frequencies are restricted to 9.5 to 10.4 MHz when the ADC is utilized. (See Figure 13.)

If desired, an external clock source can be ac coupled to OSC_{in}. A 0.01 µF coupling capacitor is used for measurement purposes and is the minimum size recommended for applications. The input capacitance of the OSC_{in} pin is approximately 6 pF. An external feedback resistor of approximately 10 MΩ is required across the OSC_{in} and OSC_{out} pins in the ac–coupled case. (See Figure 12.) *OSC_{out} is an internal node on the device and should not be used to drive any loads* (i.e., OSC_{out} is unbuffered). However, the buffered REF_{out} is available to drive external loads in the HF mode.

The external signal level must be at least 1 V p–p; the minimum and maximum frequencies are given in the **AC Electrical Characteristics** table. These frequencies apply for R Counter divide ratios as indicated in the table. For very small ratios, the maximum frequency is limited to the divide ratio times 1 MHz (Reason: the phase/frequency detectors are limited to a maximum input frequency of 1 MHz).

If an external source is available which swings from at least the V_{IL} to V_{IH} levels listed in the **DC Electrical Characteristics** table, then dc coupling can be used. In the dc–coupled case, no external feedback resistor is needed. OSC_{out} must be a No Connect to avoid loading an internal node on the MC145173, as noted above. For frequencies below 2 MHz, a signal level of at least V_{IL} and V_{IH} is needed, and dc coupling must be used. The R counter is a static counter and may be operated down to dc. However, wave shaping by a CMOS buffer may be required to ensure fast rise and fall times into the OSC_{in} pin at these low frequencies.

Each rising edge on the OSC_{in} pin causes the R counter to decrement by one. In the standby mode, OSC_{in} is pulled low by an on–chip FET.

REF_{out}
Open–Drain Reference Frequency Output (Pin 23)

This output is the buffered output of the crystal–generated reference frequency or externally provided reference source.

A P–channel MOSFET tied to V_{DD} is used to drive this open–drain output. Thus, an external pull–down device is required at this pin. This output is disabled and assumes the high–impedance state in the VHF mode per bit HF/VHF in the R register. (See Figure 18.)

REF_{out} is capable of operation to 10.4 MHz; see the **AC Electrical Characteristics** table.

If unused, the pin may be floated or tied to V_{DD}.

FREQUENCY COUNTER INPUT PINS

HF IF_{in}
HF Intermediate–Frequency Input (Pin 10)

This pin feeds an on–chip amplifier. The amp drives the F counter when the HF/VHF bit in the R register is low. (See Figure 18.) The signal driving this pin is normally sourced from the IF (intermediate frequency) circuit in the radio and is ac coupled. The input capacitance is approximately 6 pF.

This input is optimized for use with frequencies around 450 kHz. An on–chip low–pass filter is employed to roll off response above 1 MHz. In addition, for further suppression of high–frequency signals, the Kuligowski Acceptor Circuit may be engaged via the K bit in the R register. This is a digital integrator which allows acceptance of frequencies only below the frequency at the OSC_{in} pin divided by 8.

In the standby mode, HF IF_{in} is pulled low by an on–chip FET. If not used, this pin should be tied to V_{SS}.

VHF IF_{in}
VHF Intermediate–Frequency Input (Pin 11)

This pin feeds an on–chip amplifier. The amp drives the F counter when the HF/VHF bit in the R register is high. (See Figure 18.) The signal driving this pin is normally sourced from the IF circuit in the radio and is ac coupled. The input capacitance is approximately 6 pF. Usually, the frequency of the signal driving this pin is about 10.7 MHz.

For signals which swing from at least the V_{IL} to V_{IH} levels listed in the **DC Electrical Characteristics** table, dc coupling may be used. Also, for signals less than the minimum frequencies in the **AC Electrical Characteristics** table, dc coupling with at least V_{IL} and V_{IH} levels is a requirement. The F counter is a static counter and may be operated down to dc. However, wave shaping by a CMOS buffer may be required to ensure fast rise and fall times into the VHF IF_{in} pin.

In the standby mode, VHF IF_{in} is forced to a high–impedence state. If not used, this pin should be tied to V_{SS}.

LOOP PINS

HF_{in}, VHF_{in}
High Frequency Input, Very High Frequency Input (Pins 16, 15)

These pins feed on–chip amplifiers which drive the N counter; the HF/VHF bit in the R register determines which input is selected. (See Figure 18.) These signals are normally sourced from external voltage–controlled oscillators (VCOs), and are ac–coupled. (See Figures 10 and 11.) The input capacitance is approximately 6 pF. For small divide ratios, the maximum frequency is limited to the divide ratio times 1 MHz. (Reason: the phase/frequency detectors are limited to a maximum frequency of 1 MHz.)

For signals which swing from at least the V_{IL} to V_{IH} levels listed in the **DC Electrical Characteristics** table, dc coupling may be used. Also, for signals less than the minimum frequencies in the **AC Electrical Characteristics** table, dc coupling with at least V_{IL} and V_{IH} levels is a requirement. The N counter is a static counter and may be operated down to dc. However, wave shaping by a CMOS buffer may be required to ensure fast rise and fall times into the HF_{in} and VHF_{in} pins.

Each rising edge on these pins cause the N counter to decrement by one.

In the standby mode, HF_{in} is forced to a high–impedence state, and VHF_{in} is pulled low by an on–chip FET. If not used, these pins should be tied to V_{SS}.

HF PD_{out}
Single–Ended Phase/Frequency Detector Output (Pin 18)

This is a three–state output for use as a loop error signal when combined with an external low–pass filter. Through use of a Motorola patented technique, the detector's dead zone has been eliminated. Therefore, the phase/frequency detector is characterized by a linear transfer function. The operation of the phase/frequency detector is described below and is shown in Figure 16.

POL bit (R23) in the R register = low (see Figure 18)
- Frequency of $f_V > f_R$ or Phase of f_V Leading f_R: negative pulses from high impedance
- Frequency of $f_V < f_R$ or Phase of f_V Lagging f_R: positive pulses from high impedance
- Frequency and Phase of $f_V = f_R$: essentially high–impedance state; voltage at pin determined by loop filter

POL bit (R23) = high
- Frequency of $f_V > f_R$ or Phase of f_V Leading f_R: positive pulses from high impedance
- Frequency of $f_V < f_R$ or Phase of f_V Lagging f_R: negative pulses from high impedance
- Frequency and Phase of $f_V = f_R$: essentially high–impedance state; voltage at pin determined by loop filter

This output is enabled and disabled via the HF/VHF bit in the R register. HF PD_{out} is forced to the high–impedance state when disabled. This pin should be floated when it is not used.

VHF PD_{out}
Single–Ended Phase/Frequency Detector Output (Pin 21)

This is a three–state current–source/sink output for use as a loop error signal when combined with an external low–pass filter. The phase/frequency detector is characterized by a linear transfer function. The operation of the phase/frequency detector is described below and is shown in Figure 16.

POL bit (R23) in the R register = low (see Figure 18)
- Frequency of $f_V > f_R$ or Phase of f_V Leading f_R: current–sinking pulses from a floating state
- Frequency of $f_V < f_R$ or Phase of f_V Lagging f_R: current–sourcing pulses from a floating state
- Frequency and Phase of $f_V = f_R$: essentially a floating state; voltage at pin determined by loop filter

POL bit (R23) = high
- Frequency of $f_V > f_R$ or Phase of f_V Leading f_R: current–sourcing pulses from a floating state
- Frequency of $f_V < f_R$ or Phase of f_V Lagging f_R: current–sinking pulses from a floating state

Frequency and Phase of $f_V = f_R$: essentially a floating state; voltage at pin determined by loop filter

This output is enabled and disabled via the HF/VHF bit in the R register. VHF PD_{out} is forced to the floating state when disabled.

If not used, this pin should be a no connect.

Rx
External Resistor (Pin 20)

A resistor is tied between this pin and V_{SS}. This sets a reference current which determines the current delivered (I_{PDout}) at the current source/sink phase/frequency detector output, VHF PD_{out}. For a nominal current of 2.2 mA at the VHF PD_{out} pin, a 15 kΩ resistor is utilized.

In addition, the Rx pin must be bypassed to V_{DD} with a low–inductance 0.1 µF capacitor mounted very close to these pins. Lead lengths on the capacitor should be minimized.

If the VHF PD_{out} pin is not used, the Rx pin may be floated.

POWER SUPPLY

V_{DD}
Most–Positive Supply Potential (Pin 17)

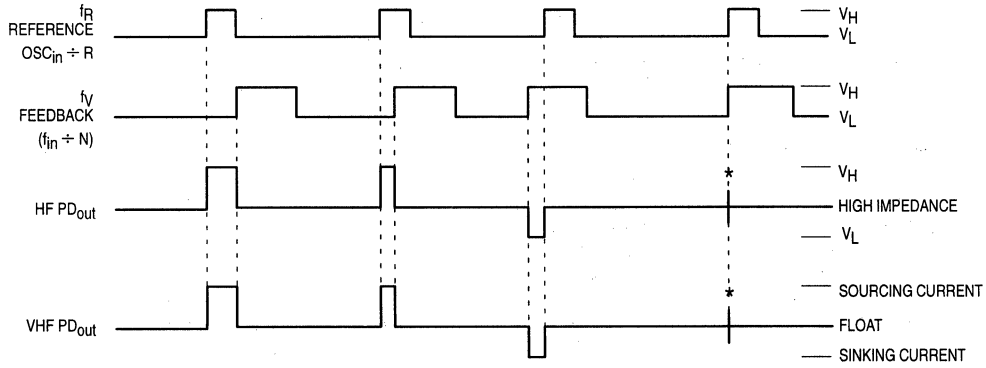
This pin may range from 4.5 to 5.5 V with respect to V_{SS}.

For optimum performance, V_{DD} should be bypassed to V_{SS} using low–inductance capacitor(s) mounted very close to the MC145173. Lead lengths and traces to the capacitor(s) should be minimized. (The very fast switching speed of the device can cause excessive current spikes on the power leads if they are improperly bypassed.)

Power supply ramp up time should be less than 20 ms from 0 to 4.5 V. If the ramp up time exceeds 20 ms, the POR circuit may not function and the outputs will be in an unknown state. The RST bit must be used in this case.

V_{SS}
Most–Negative Supply Potential (Pin 19)

This pin is usually ground.



V_H = High voltage level
V_L = Low voltage level
*At this point, when both f_R and f_V are in phase, both the source and sink drivers are turned on for a short duration. For exceptions, see Figure 19.
NOTE: HF PD_{out} and VHF PD_{out} are shown with the polarity bit (POL) = low; see Figure 18 for POL.

Figure 16. Phase/Frequency Detectors Output Waveforms

C REGISTER BITS

I SMPL
Input Sample (C7)

When the input sample bit is cleared low, the ADC is held in the initialized state. When I SMPL is set high, the ADC converts the input channel selected by bit C4, and holds the conversion value. When the ADC is read via the serial port, I SMPL must remain high. Otherwise, the EOC bit is reset low. The previous converison value is not lost, however.

I SMPL may be set at any time, even if the F SMPL bit in the R register is already set. That is, an A/D conversion may be initiated during an F count. The state of C4 may not be changed simultaneously with C7 being set high.

I SMPL is cleared low upon power up. However, this bit is not automatically cleared low after a conversion and read sequence.

READ A
Read A Register (C6)

Setting the Read A register bit high causes the ADC's value and the states of Inputs C and D to be parallel loaded into the serial port's shift register. $\overline{ENB}$ is then taken low and either 8, 9, or 16 bits are shifted from the D_{out} pin. If only 8 bits are shifted, the state of Input D is not read. To read Input D, use either a 9 or 16 bit shift. (See Figure 21.) Alternatively, Input D may be read from the F Register.

While the Read A bit is set, writing to any register is inhibited. After the read occurs (A register data shifted out), C6 is automatically cleared low. When C6 is low, the shift register is not parallel loaded and any of the registers of Table 1 may be written.

Read A should not be set when Read F is set. If both Read A and Read F are set simultaneously, a *Read A Register* operation is performed and the *Read F Register* request is ignored.

Read A is cleared low at power up.

RESERVED
Reserved Bit (C5)

This bit must be kept low.

CHAN
Channel Select for ADC (C4)

When the channel bit is low, Input A is selected to be converted by the ADC. When the bit is high, Input B is selected. The state of C4 may not be changed simultaneously with the I SMPL bit being set high.

READ F
Read F Register (C3)

Setting the Read F register bit high causes the frequency counter's value and the state of Input D to be parallel loaded into the serial port's shift register. $\overline{ENB}$ is then taken low and 24 bits are shifted from the D_{out} pin. (See Figure 22.)

While the Read F bit is set, writing to any register is inhibited. After the read occurs (F register data shifted out), C3 is automatically cleared low. When C3 is low, the shift register is not parallel loaded and any of the registers of Table 1 may be written.

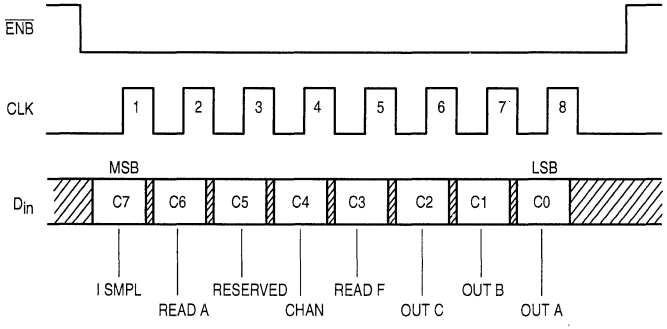
Read F should not be set when Read A is set. If both Read F and Read A are set simultaneously, a *Read A Register* operation is performed and the *Read F Register* request is ignored.

Read F is cleared low at power up.

OUT C, OUT B, OUT A
Output C, Output B, Output A Control (C2, C1, C0)

When Out A, Out B, or Out C is cleared low, the Output A, Output B, or Output C pins are forced low, respectively. When set high, the associated output is forced high, except for Output A which is forced to the high–impedance state.

These bits are cleared low at power up.



NOTE: This is a write–only register.

Figure 17. C Register Access and Format (8 Clock Cycles are Used)

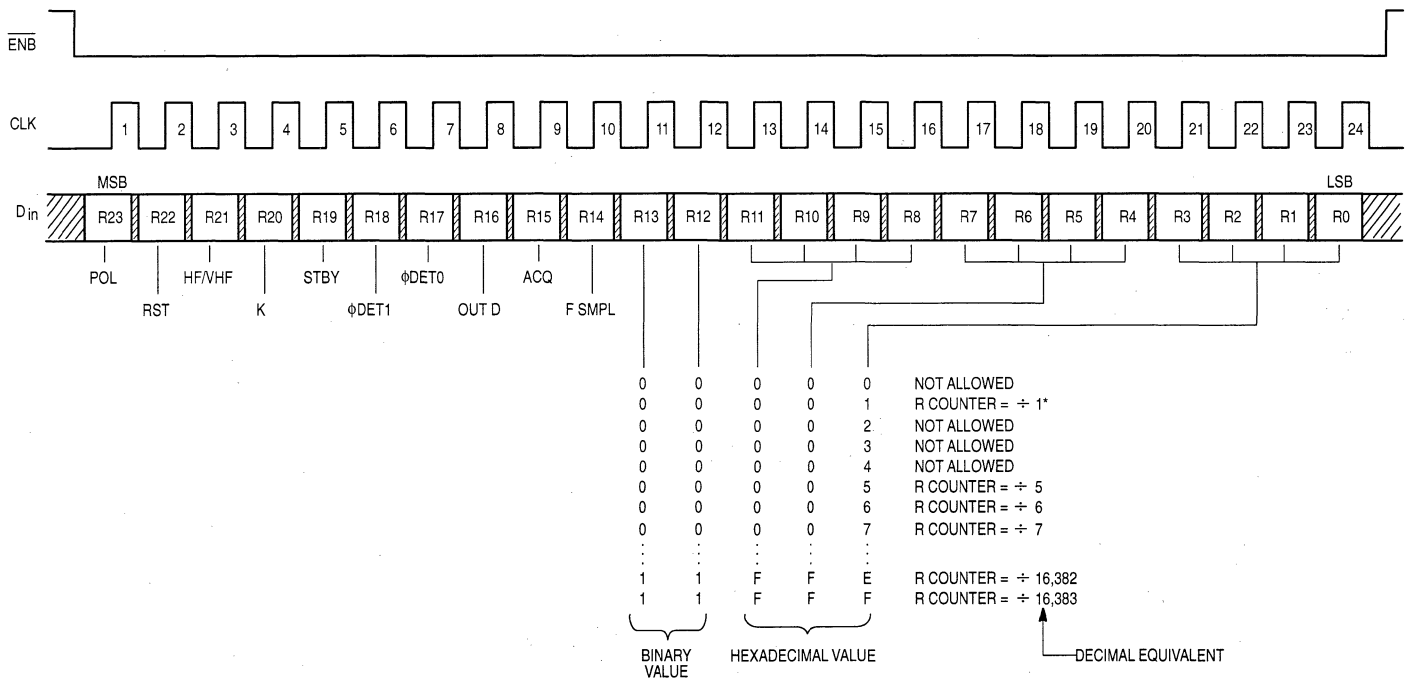


Figure 18. R Register Access and Format (24 Clock Cycles Are Used)

NOTE: This is a write-only register.
*Direct access to reference side of phase/frequency detectors.

Do not attempt to write to the R register when both the F counter and A/D converter are simultaneously active.

POL
Polarity (R23)

The polarity bit controls both phase/frequency detector outputs. When low, the detector outputs are per Figure 16. When R23 is high, the output polarity of both phase/frequency detectors is inverted.

Upon power up, this bit is forced low.

RST
Reset (R22)

When high, this bit resets the device except for the serial port. RST is kept low for normal operation. However, if a power glitch occurs which does not reduce the power supply voltage to 0 volts, the R register should be written twice with the RST bit set high. Also, if the CLK pin is floating upon power up, the RST bit should be written high twice for initialization.

NOTE

The on–chip POR (power–on reset) circuit resets the device during a cold start, if the CLK pin is not floating or toggled during supply ramp up to 4.5 V.

This bit is automatically cleared low after the chip is reset.

HF/VHF
HF/VHF Band Selection (R21)

When this bit is low, the HF_{in} and HF IF_{in} inputs are enabled, along with the HF PD_{out} pin. The VHF PD_{out} pin is forced to the float condition and VHF_{in} is pulled low with an on–chip FET.

When this bit is high, the VHF_{in} and VHF IF_{in} inputs are enabled, along with the VHF PD_{out} pin. Both the HF PD_{out} and HF_{in} pins are forced to the high–impedance state, and REF_{out} is disabled (high–impedance).

K
HF IF_{in} Response (R20)

This bit is used to control the input response of the HF IF_{in} pin.

When the K bit is high, the Kuligowski acceptor circuit is engaged, which allows acceptance of signals only below the frequency at the OSC_{in} pin divided by 8. Use of this digital integrator allows further suppression of high–frequency signals into the HF IF_{in} pin.

In the VHF mode, the K bit should be kept low.

STBY
Standby (R19)

If STBY is low, the chip is in the normal mode of operation.

When this bit is high, the device is placed in the standby state for reduced power consumption. In standby, both phase/frequency detector outputs and the REF_{out} pin are forced to the high–impedance state, the Rx reference current is shut off, and the oscillator is stopped (via an on–chip FET pulling the OSC_{in} pin low). The HF_{in}, VHF_{in}, HF IF_{in}, and VHF IF_{in} inputs are shut off, which inhibits the counters from toggling. Finally, the comparator and ADC are turned off. Data is retained in the C, N, and R registers during standby.

CAUTION

Setting the STBY bit high aborts any frequency count or A/D conversion which may be in progress.

STBY is forced high upon power up.

ϕdet1, ϕdet0
Phase/Frequency Detector Response (R18, R17)

Controls the VHF phase/frequency detector response per Table 3. The HF phase/frequency detector is unaffected.

These bits also control several test modes as shown in Table 4.

Out D
Output D Control (R16)

When cleared low, the Output D pin is forced low. When high, Output D is high.

This bit is cleared low upon power up.

ACQ
Acquisition Window (R15)

This bit determines the frequency counter (F counter) acquisition window. A low level is for a narrow window, and a high is for a wide window.

The formula to determine the window is

$$t = \frac{2^{(19 + 2a)}}{f}$$

where t is the acquisition window in seconds, a is the logic level of the ACQ bit (0 or 1), and f is the frequency at the OSC_{in} pin in hertz.

F SMPL
Frequency Sample (R14)

When this bit is low, the frequency counter (F counter) is initialized to all highs (ones).

When F SMPL is set high, the frequency counter "rolls over" to zero, increments for one acquisition window, and then holds the count. When the frequency counter is read via the serial port, R14 must remain high; otherwise, the frequency counter is initialized and outputs all ones.

F SMPL must not be set high if I SMPL is already high. That is, a frequency count cannot be initiated if an A/D conversion is in progress.

This bit is cleared low upon power up. However, this bit is not automatically cleared low after a frequency count and read sequence.

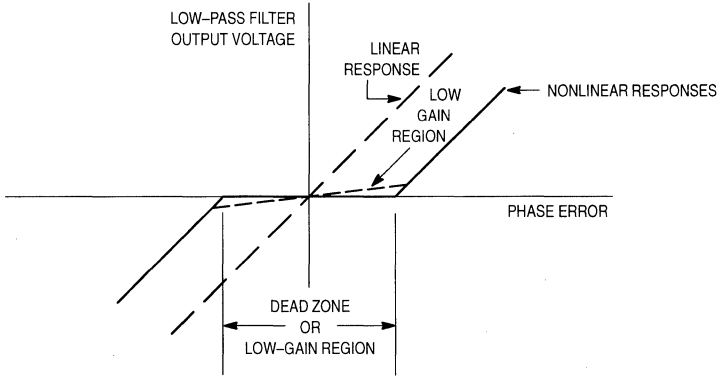
R13 to R0
R Counter Divide Ratio

These bits control the divide ratio of the R counter per Figure 18.

Table 3. VHF PD_{out} Response

N Register Bit	R Register Bits		
N15	R18	R17	VHF Phase Detector Response (Nominal)
L	L	L	Linear response, no low–gain region
L	L	H	Low–gain region, 5 ns wide
L	H	L	Low–gain region, 10 ns wide
L	H	H	Low–gain region, 15 ns wide
H	L	L	Linear response, no dead zone
H	L	H	Dead zone, 5 ns wide
H	H	L	Dead zone, 10 ns wide
H	H	H	Dead zone, 15 ns wide

NOTES:
1. L = Low Level, H = High Level.
2. See Figure 19.



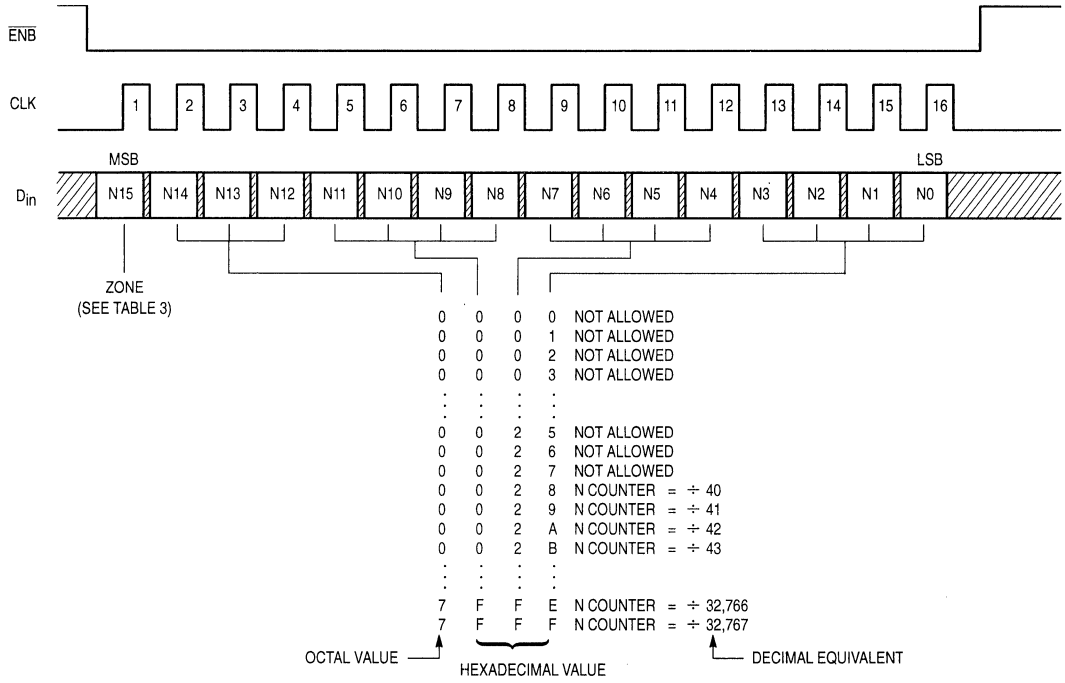
NOTES:
1. Output HF PD_{out} always has a linear transfer characteristic. Therefore, for HF PD_{out}, the Dead Zone = 0 ns.
2. Output VHF PD_{out} has a response which is programmable via bits ϕdet1 (R18), ϕdet0 (R17), and Zone (N15). See Table 3.
3. The gain in the "low–gain region" is reduced to 7% of the gain in the other region.

Figure 19. VHF PD_{out} Transfer Characteristic

Table 4. Test Modes

R Register Bits			Pin Configurations	
R21	R18	R17	Pin 12 — OUTPUT A	Pin 13 — OUTPUT B
L	L	L	OUTPUT A, normal configuration	OUTPUT B, normal configuration
L	L	H	f_V, N counter output — HF_{in} feeds the counter input	OUTPUT B, normal configuration
L	H	L	f_V, N counter output — VHF_{in} feeds the counter input	OUTPUT B, normal configuration
L	H	H	OUTPUT A, normal configuration	f_R, R counter output
H	X	X	OUTPUT A, normal configuration	OUTPUT B, normal configuration

NOTE: L = Low Level, H = High Level, X = Don't Care.



NOTE: This is a write–only register.

Figure 20. N Register Access and Format (16 Clock Cycles Are Used)

A REGISTER BITS

EOC
End of Conversion (A7)

The end of conversion bit is set high when the analog–to–digital conversion is complete. This high level indicates that the A/D conversion value read via the serial port is valid.

EOC is cleared low when the I SMPL bit in the C register is cleared low.

IN C
Input C Level (A6)

In C indicates the state of the Input C pin. A high level on the Input C pin causes the In C bit to be high. A low level on the pin causes a low level to be read on In C. The digital value is stored at the falling edge of $\overline{ENB}$ on the read cycle.

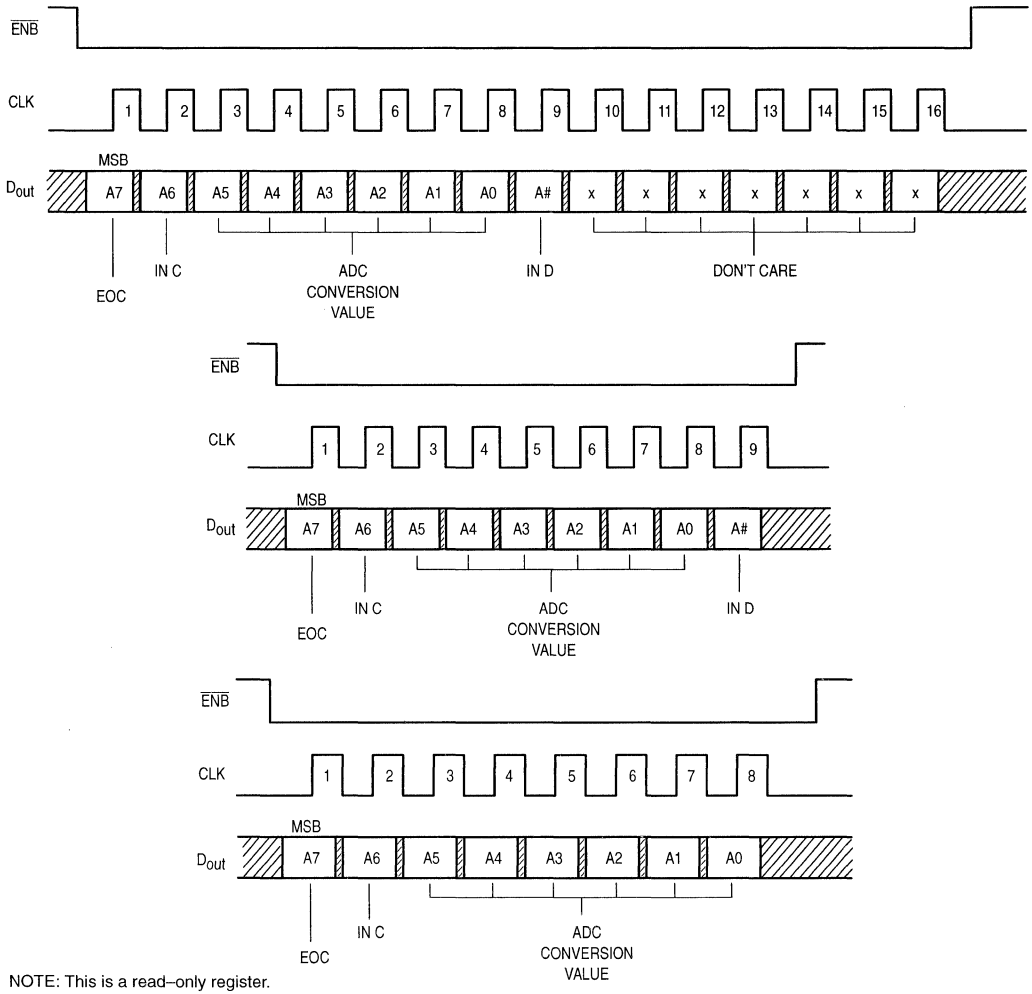
ADC CONVERSION VALUE
A/D Conversion Value (A5 – A0)

These bits contain the analog–to–digital conversion result in binary format. A5 is the MSB of the value; A0 is the LSB.

IN D
Input D Level (A#)

In D indicates the state of the Input D pin. A high level on the Input D pin causes the In D bit to be high. A low level on the pin causes a low level to be read on In D. The digital value is stored at the falling edge of $\overline{ENB}$ on the read cycle.

A 9– or 16–bit shift must be used to read the In D bit from the A register. Optionally, the In D bit may be read from the F register.



NOTE: This is a read–only register.

Figure 21. A Register Formats (8, 9, or 16 Clock Cycles May Be Used)

CC
Count Complete (F23)

The count complete bit is set high when the frequency counter has gone through a count cycle for a complete acquisition window. This high level indicates that the count read via the serial port is valid.

CC is cleared low when the F SMPL bit in the R register is cleared low.

IN D
Input D Level (F22)

In D indicates the state of the Input D pin. A high level on the Input D pin causes the In D bit to be high. A low level on the pin causes a low level to be read on In D.

Optionally, the In D bit may be read from the A register.

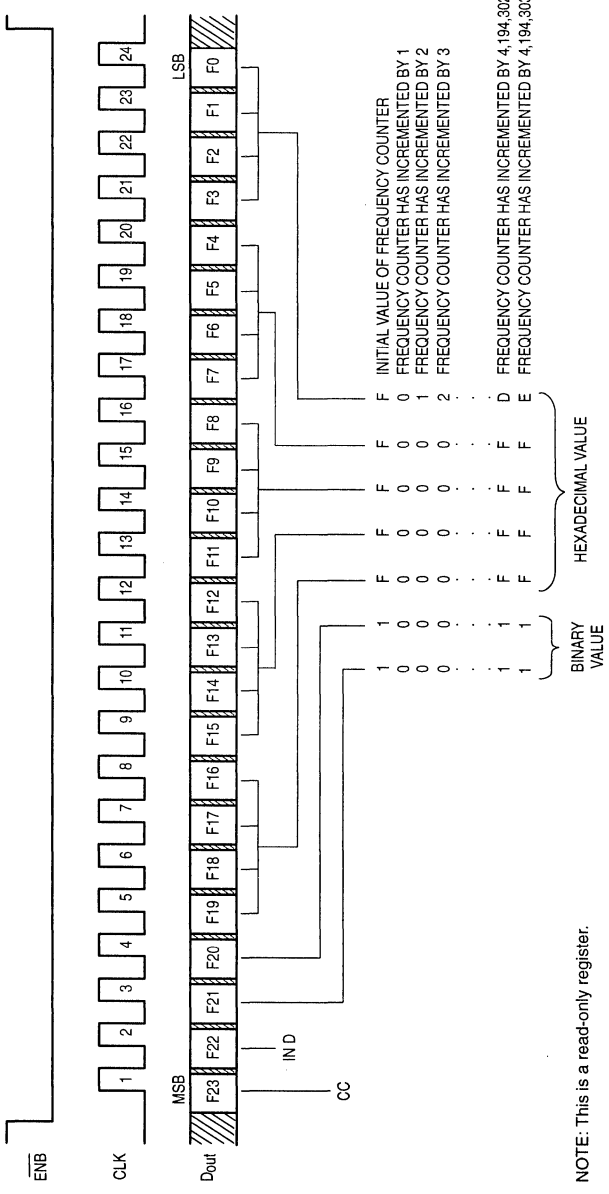


Figure 22. F Register Format (24 Clock Cycles Are Used)

CRYSTAL OSCILLATOR CONSIDERATIONS

The following options may be considered to provide a reference frequency to Motorola's CMOS frequency synthesizers.

Use of a Hybrid Crystal Oscillator

Commercially available temperature–compensated crystal oscillators (TCXOs) or crystal–controlled data clock oscillators provide very stable reference frequencies. An oscillator capable of CMOS logic levels at the output may be direct or dc coupled to OSC_{in}. If the oscillator does not have CMOS logic levels on the outputs, capacitive or ac coupling to OSC_{in} must be used. (See Figure 12.)

For additional information about TCXOs and data clock oscillators, please consult the latest version of the *eem Electronic Engineers Master Catalog,* the *Gold Book,* or similar publications.

Design an Off–Chip Reference

The user may design an off–chip crystal oscillator using discrete transistors or ICs specifically developed for crystal oscillator applications, such as the MC12061 MECL device. The reference signal from the MECL device is ac coupled to OSC_{in}. (See Figure 12.) For large amplitude signals (standard CMOS logic levels), dc coupling may be used.

Use of the On–Chip Oscillator Circuitry

The on–chip amplifier (a digital inverter) along with an appropriate crystal may be used to provide a reference source frequency. A fundamental mode crystal, parallel resonant at the desired operating frequency, should be connected as shown in Figure 23.

The crystal should be specified for a loading capacitance (C_L) which does not exceed 20 pF when used at the highest operating frequency. Larger C_L values are possible for lower frequencies. Assuming R1 = 0 Ω, the shunt load capacitance (C_L) presented across the crystal can be estimated to be:

$$C_L = \frac{C_{in}C_{out}}{C_{in} + C_{out}} + C_a + C_{stray} + \frac{C1 \bullet C2}{C1 + C2}$$

where

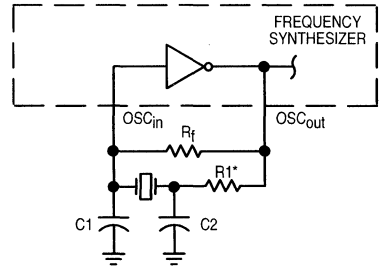
C_{in} = 6 pF (see Figure 24)
C_{out} = 6 pF (see Figure 24)
C_a = 1 pF (see Figure 24)
C1 and C2 = external capacitors (see Figure 23)
C_{stray} = the total equivalent external circuit stray capacitance appearing across the crystal terminals (see Figure 24)

The oscillator can be "trimmed" on–frequency by making a portion or all of C1 variable. The crystal and associated components must be located as close as possible to the OSC_{in} and OSC_{out} pins to minimize distortion, stray capacitance, stray inductance, and startup stabilization time. Circuit stray capacitance can also be handled by adding the appropriate stray value to the values for C_{in} and C_{out}. For this approach, the term C_{stray} becomes 0 in the above expression for C_L.

Power is dissipated in the effective series resistance of the crystal, R_e, in Figure 25. The maximum drive level specified by the crystal manufacturer represents the maximum stress that the crystal can withstand without damage or excessive shift in operating frequency. R1 in Figure 23 limits the drive level. The use of R1 is not necessary in most cases.

To verify that the maximum dc supply voltage does not cause the crystal to be overdriven, monitor the output frequency at the OSC_{out} pin. An active probe should be used to minimize loading. The frequency should increase very slightly as the dc supply voltage is increased. An overdriven crystal decreases in frequency or becomes unstable with an increase in supply voltage. The operating supply voltage must be reduced or R1 must be increased in value if the overdriven condition exists. The user should note that the oscillator start–up time is proportional to the value of R1.

Through the process of supplying crystals for use with CMOS inverters, many crystal manufacturers have developed expertise in CMOS oscillator design with crystals. Discussions with such manufacturers can prove very helpful. (See Table 5)



*May be needed in certain cases. See text.

Figure 23. Pierce Crystal Oscillator Circuit

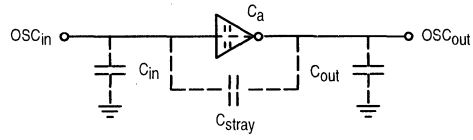
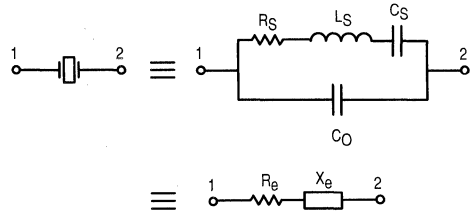


Figure 24. Parasitic Capacitances of the Amplifier and C_{stray}



Note: Values are supplied by crystal manufacturer (parallel resonant crystal).

Figure 25. Equivalent Crystal Networks

Recommended Reading

Technical Note TN–24, Statek Corp.

Technical Note TN–7, Statek Corp.

E. Hafner, "The Piezoelectric Crystal Unit–Definitions and Method of Measurement", *Proc. IEEE,* Vol. 57, No. 2, Feb. 1969.

D. Kemper, L. Rosine, "Quartz Crystals for Frequency Control", *Electro–Technology,* June 1969.

P. J. Ottowitz, "A Guide to Crystal Selection", *Electronic Design*, May 1966.

D. Babin, "Designing Crystal Oscillators", *Machine Design*, March 7, 1985.

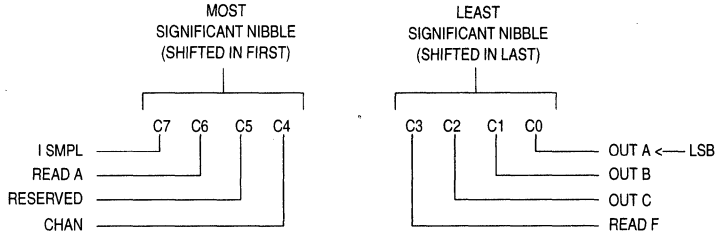
D. Babin, "Guidelines for Crystal Oscillator Design", *Machine Design*, April 25, 1985.

Table 6. Partial List of Crystal Manufacturers

Name	Address	Phone
United States Crystal Corp.	3605 McCart Ave., Ft. Worth, TX 76110	(817) 921–3013
Crystek Crystal	2351 Crystal Dr., Ft. Myers, FL 33907	(813) 936–2109
Statek Corp.	512 N. Main St., Orange, CA 92668	(714) 639–7810
Fox Electronics	5570 Enterprise Parkway, Ft. Myers, FL 33905	(813) 693–0099

NOTE: Motorola cannot recommend one supplier over another and in no way suggests that this is a complete listing of crystal manufacturers.

C REGISTER
Write Only



I SMPL = Analog Input Sample Command
- 0 = Initialize the ADC
- 1 = Sample the voltage on the Input A or B pins (see Chan bit)

Read A = Read A Register Command
- 0 = Allow writes to any registers, normal state
- 1 = Read the Input A or B analog value* and the Input C and D digital values

Reserved = Reserved Bit
- 0 = (Must be in this state)
- 1 = (This state not allowed at this time, reserved)

Chan = Analog Channel Address
- 0 = Input A
- 1 = Input B

*6–bit analog–to–digital converter output value.

Out A = Output A Pin Logic State
- 0 = Pin is forced to a 0 (default)
- 1 = Pin is forced to the high–impedance state

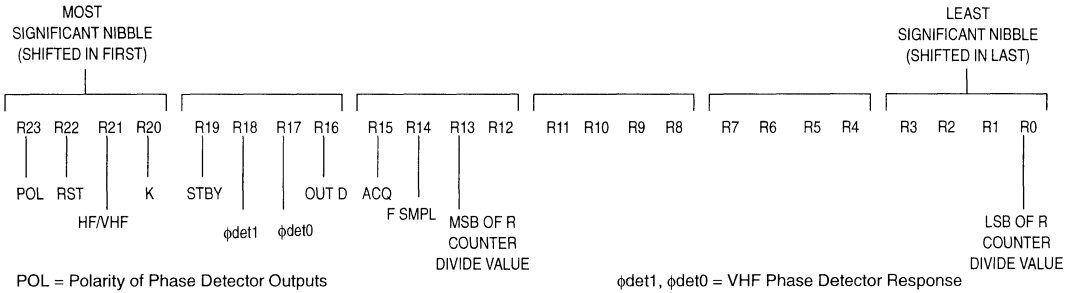
Out B = Output B Pin Logic State
- 0 = Pin is forced to a 0 (default)
- 1 = Pin is forced to a 1

Out C = Output C Pin Logic State
- 0 = Pin is forced to a 0 (default)
- 1 = Pin is forced to a 1

Read F = Read F Register
- 0 = Allow writes to any registers, normal state
- 1 = Read the Frequency Counter's value and Input D state

PROGRAMMER'S GUIDE (continued)

R REGISTER
Write Only



POL = Polarity of Phase Detector Outputs
- 0 = Normal (default)
- 1 = Inverted

RST = Reset
- 0 = Normal
- 1 = Reset the chip (automatically cleared low)
- Suggestion: set to 1 after power glitch

HF/VHF = HF or VHF Band Select
- 0 = HF_{in}, HF IF_{in}, and HF PD_{out} pins are activated (default)
- 1 = VHF_{in}, VHF IF_{in}, and VHF PD_{out} pins are activated

K = HF IF_{in} Input Response
- 0 = Normal (must be 0 when VHF band is selected)
- 1 = Engage Acceptor Circuit

STBY = Standby
- 0 = Normal
- 1 = Low–Power Standby State

φdet1, φdet0 = VHF Phase Detector Response
- 0, 0 = Linear Response
- 0, 1 = Low–Gain Region or Dead Zone – 5 ns wide
- 1, 0 = Low–Gain Region or Dead Zone – 10 ns wide
- 1, 1 = Low–Gain Region or Dead Zone – 15 ns wide

Out D = Output D Pin Logic State
- 0 = Pin is forced to a 0 (default)
- 1 = Pin is forced to a 1

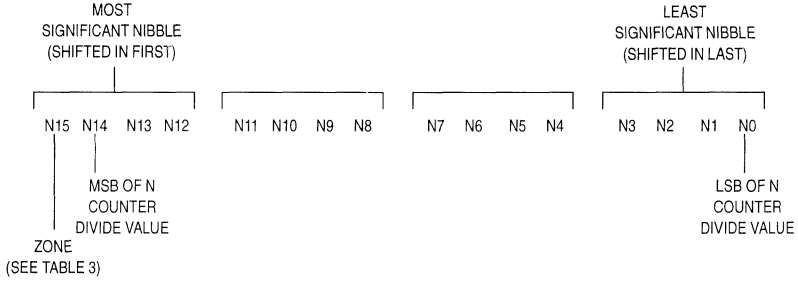
ACQ = Acquisition Window
- 0 = Narrow Sample Window
- 1 = Wide Sample Window

F SMPL = Frequency Counter Sample Command
- 0 = Initialize Counter to all 1's (default)
- 1 = Sample the Frequency at HF IF_{in} or VHF IF_{in} pins

Example:
To program the R Counter to divide by 1000 in decimal, first convert to hexadecimal: $3E8. Then, add leading bits to form 3 bytes (6 nibbles). The leading bits should be adjusted to control the above functions. Finally, load the R Register.

CAUTION:
When both the A/D converter and F Counter are simultaneously active, a write to the R Register causes the F Counter operation to abort.

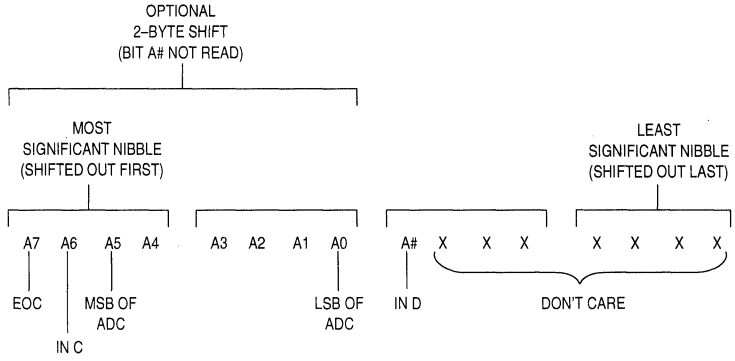
N REGISTER
Write Only



Example:
To program the N Counter to divide by 1000 in decimal, first convert to hexadecimal: $3E8. Then, add leading zeroes to form 2 bytes (4 nibbles): $03E8. Finally, Load the N Register with $03E8.

NOTE:
The chip's VHF PD_{out} is controlled by bit N15 as follows: low = low–gain region, high = dead zone. See Figure 19.

A REGISTER
Read Only



EOC = End of Conversion
0 = Invalid ADC Results (also, this bit is 0 when the ADC is in the initialized state)
1 = A/D Conversion Complete, Results are Valid

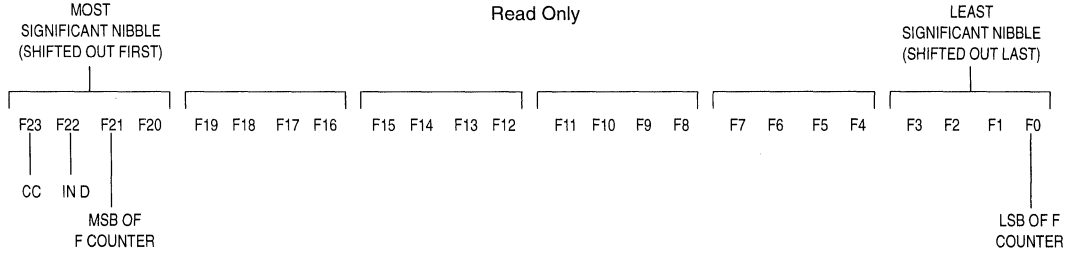
IN C = Input C Pin Status
0 = Pin is a Logic 0
1 = Pin is a Logic 1

MSB to LSB of ADC = Binary Representation of the 6–Bit Conversion value
For example, zero is 000000, full scale is 111111 in binary.

IN D = Input D Pin Status
0 = Pin is a Logic 0
1 = Pin is a Logic 1

Example:
To read just the ADC value, the user may shift out 1 byte. The ADC value is contained in the 6 LSBs. If the MSB is a 1, this indicates that the conversion is complete and the results are valid. The MSB – 1 is the Input C pin value.
A 2–byte shift allows reading the In D bit in addition to the above. (In D is also contained in the F Register.) As illustrated above, the MSB is the EOC bit, and the 7 LSBs are don't care bits. A 9–bit shift also allows reading the In D bit.

F REGISTER
Read Only

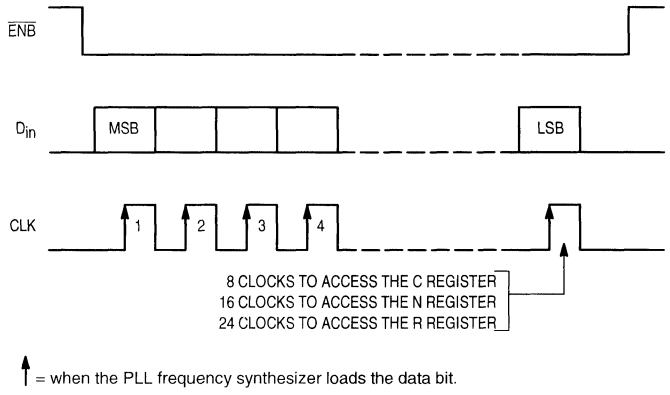


CC = Count Complete Bit
0 = Count NOT Complete, invalid F Count data (also, this bit is 0 when the F Counter is in the initialized state)
1 = Count Complete, valid F Count data

IN D = Input D Pin Status
0 = Pin is a Logic 0
1 = Pin is a Logic 1

MSB to LSB of F Counter = Binary Representation of the Frequency Counter's Value.
For Example, if the Frequency Counter counts to 10,000 in decimal, this is $2710 in hexadecimal. Therefore, the value read, when Input D is at a logic low level, is $802710. Note for this example that the CC bit is set to a 1 which indicates a valid count.

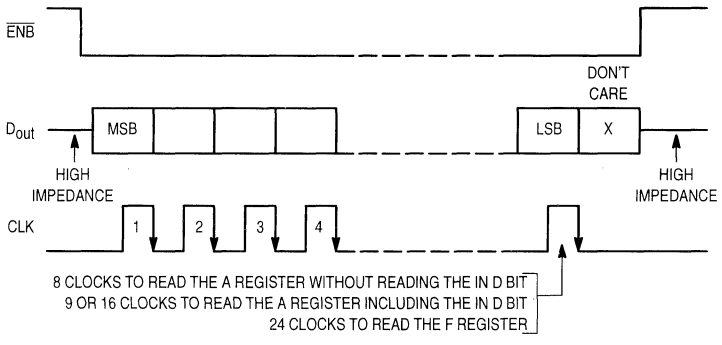
ACCESSING THE WRITE–ONLY REGISTERS



↑ = when the PLL frequency synthesizer loads the data bit.

ACCESSING THE READ–ONLY REGISTERS

The Read F Bit or Read A Bit in the C Register must be set to a 1 prior to the following operation



↓ = when the PLL frequency synthesizer changes the data bit.

CONFIGURING FOR HF AND MF OPERATION

HF = HIGH FREQUENCY: 3 TO 30 MHZ
MF = MEDIUM FREQUENCY 500 kHZ TO 3 MHZ

The write–only registers retain data indefinitely as long as power is applied to the device. Therefore, they do not need to be re–written with the same data when tuning across the band. These registers only need to be written if the contents need to be changed.

Step 1: Load the C Register

The Out A, Out B, and Out C bits must be properly programmed to configure the Output A, Output B, and Output C pins. These outputs switch a few nanoseconds after the C Register is loaded, i.e., after $\overline{ENB}$ makes a low–to–high transition on a C Register access.

Step 2: Load the R Register

This register determines the tuning resolution of the radio by setting the divide ratio of the R Counter. Also, the HF/VHF bit must be cleared low for HF and MF operation.

As an example, assume that the external crystal connected to pins 1 and 24 is 10.25 MHz. Also, assume that the tuning resolution is 10 kHz. Then, the divide ratio needed is 10.25 MHz divided by 10 kHz; this is 1025 decimal. In hexadecimal, this is $401.

Loading the R Register is accomplished with 3 bytes. Therefore, if all other bits are low, the serial data is $000401. For HF and MF operation, the ACQ bit is usually set high for a wide acquisition window. Therefore, it is more likely the data is: $008401.

Tuning the HF or MF Band

To tune across the HF or MF band, the N Register needs to be changed.

For example, if the first I.F. is 10.7 MHz, and 530 kHz needs to be tuned, then the L.O. needs to be running at 10.7 MHz plus 530 kHz for high–side injection; this is 11.23 MHz. The resolution is 10 kHz. Therefore, the ratio required for the N Counter is 11.23 MHz divided by 10 kHz; this is 1123 decimal. In hexadecimal, this is $463.

Loading the N register requires 2 bytes. Therefore, the serial data is $0463.

To tune 1000 kHz, use 1170 decimal or $0492.

To tune 1710 kHz, use 1241 decimal or $04D9.

CONFIGURING FOR VHF OPERATION

VHF = VERY HIGH FREQUENCY: 30 TO 130 MHz

The write–only registers retain data indefinitely as long as power is applied to the device. Therefore, they do not need to be re–written with the same data when tuning across the band. These registers only need to be written if the contents need to be changed.

Step 1: Load the C Register

The Out A, Out B, and Out C bits must be properly programmed to configure the Output A, Output B, and Output C pins. These outputs switch a few nanoseconds after the C Register is loaded; i.e., after $\overline{ENB}$ makes a low–to–high transition on a C Register access.

Step 2: Load the R Register

This register determines the tuning resolution of the radio by setting the divide ratio of the R Counter. Also, the HF/VHF bit must be set high for VHF operation.

As an example, assume that the external crystal connected to pins 1 and 24 is 10.35 MHz. Also, assume that the tuning resolution is 50 kHz. Then, the divide ratio needed is 10.35 MHz divided by 50 kHz; this is 207 decimal. In hexadecimal, this is $CF.

Loading the R Register is accomplished with 3 bytes. Therefore, if all other bits are low, the serial data is $0000CF. For VHF operation, the ACQ bit is usually cleared low for a narrow acquisition window.

Tuning the VHF Band

To tune across the VHF Band, the N Register needs to be changed.

For example, if the I.F. is 10.7 MHz, and 87.5 MHz needs to be tuned, then the L.O. needs to be running at 10.7 MHz plus 87.5 MHz for high–side injection; this is 98.2 MHz. The resolution is 50 kHz. Therefore, the ratio required for the N Counter is 98.2 MHz divided by 50 kHz; this is 1964 decimal. In hexadecimal, this is $7AC.

Loading the N Register requires 2 bytes. Therefore, the serial data is $07AC.

To tune 98.5 MHz, use 2184 decimal or $0888.

To tune 107.9 MHz, use 2372 decimal or $0944.

READING THE A REGISTER

The A Register contains the binary representation of the Analog–to–Digital Converter's value plus the End of Conversion bit (EOC). The EOC bit must be a 1 to indicate a valid conversion. Also, the A Register has bits which indicate the logic levels on the Input C and D pins.

Reading the Logic Levels on the Input C and D Pins

Step 1: Store the Values in the Shift Register

To store the value, set the Read A bit in the C Register to a 1. The digital value present at the Input C and D pins during the falling edge of $\overline{ENB}$ on the read cycle is stored in the shift register.

Step 2: Read the Serial Data

To read the Input C value only, take the $\overline{ENB}$ pin low and shift out 8 bits. The Input C value is contained in the In C bit.

To read both the Input C and D values, take the $\overline{ENB}$ pin low and shift out 9 or 16 bits. The values are in the In C and In D bits.

NOTE: In D may also be read from the F Register.

Reading the Analog–to–Digital Converter Value

Step 1: Initialize

To initialize the converter, clear the I SMPL bit in the C Register to a 0. At this time, the Read A bit in the C Register must be 0. The Chan bit must be 0 to select Input A or 1 to select Input B. The state may not be changed simultaneously with the I SMPL bit being set high.

Step 2: Acquire the Value

To sample the analog input selected, set the I SMPL bit in the C Register to a 1. The Read A bit must not be changed; it must be a 0.

NOTE: I SMPL may be set high, even if F SMPL is already set high. I SMPL is not automatically cleared low.

The length of time required to acquire the data is dependent on the crystal frequency (tied to pins 1 and 24) or OSC_{in} frequency. The formula is: T = 3584/f; where T is the acquisition time in seconds and f is the frequency at OSC_{in} in hertz. After the I SMPL bit is set, the EOC bit is set high after the acquisition time T above, and data is available to be read.

Step 3: Read the Serial Data

To read the ADC value, set the Read A bit in the C Register to a 1. I SMPL must not be changed; it must be a 1.

Take the $\overline{ENB}$ pin low and shift out 8 bits. The value is contained in the least–significant 6 bits. In addition, the EOC bit should be checked to ensure it is a 1; this indicates that the conversion was complete before the data was read. If EOC is a 0, the conversion result is not valid.

The In C bit is valid and indicates the logic level present on the Input C pin. (Alternatively, 9 or 16 bits could be shifted out if the user desires to read both the In C and In D bits.)

NOTE: When the Read A bit is set to a 1, writing to any register is inhibited. After the serial shift which reads the A Register occurs, Read A is automatically cleared to a 0.

CAUTION

If both Read A and Read F are set simultaneously, a *Read A Register* operation is performed and the *Read F Register* request is ignored.

READING THE F REGISTER

The F Register contains the binary representation of the Frequency Counter's value plus the Count Complete flag (CC). The CC bit must be a 1 to indicate a valid count. Also, the F Register has a bit which indicates the logic level on the Input D pin.

Reading the Logic Level on the Input D Pin

Step 1: Store the Value in the Shift Register

To store the value, set the Read F bit in the C Register to a 1. The digital value present at the Input D pin during the falling edge of $\overline{ENB}$ on the read cycle is stored in the shift register.

Step 2: Read the Serial Data

To read the Input D value, take the $\overline{ENB}$ pin low and shift out 24 bits. The Input D value is contained in the In D bit.

NOTE: In D may also be read from the A Register.

Reading the Frequency Counter Value

Step 1: Initialize

To initialize the counter, clear the F SMPL bit in the R Register to a 0. At this time, the Read F bit in the C Register must be 0. The HF/VHF bit in the R Register must be a 0 for HF–MF operation or 1 for VHF operation. The ACQ (Acquisition Window) bit must be a 0 for a narrow acquisition window or a 1 for a wide window. The formula for the window:

$$t = \frac{2^{(19 + 2a)}}{f}$$

where t = acquisition window (in seconds), a = logic level of acquisition bit (0 or 1), f = crystal frequency or OSC_{in} frequency in hertz.

Step 2: Acquire the Count

To sample the frequency, set the F SMPL bit in the R Register to a 1. The Read F bit must not be changed; it must be a 0.

CAUTION

F SMPL must not be set if I SMPL is already set high.

The data is available to be read after the acquisition window time above. The CC bit is set high immediately after the acquisition is complete.

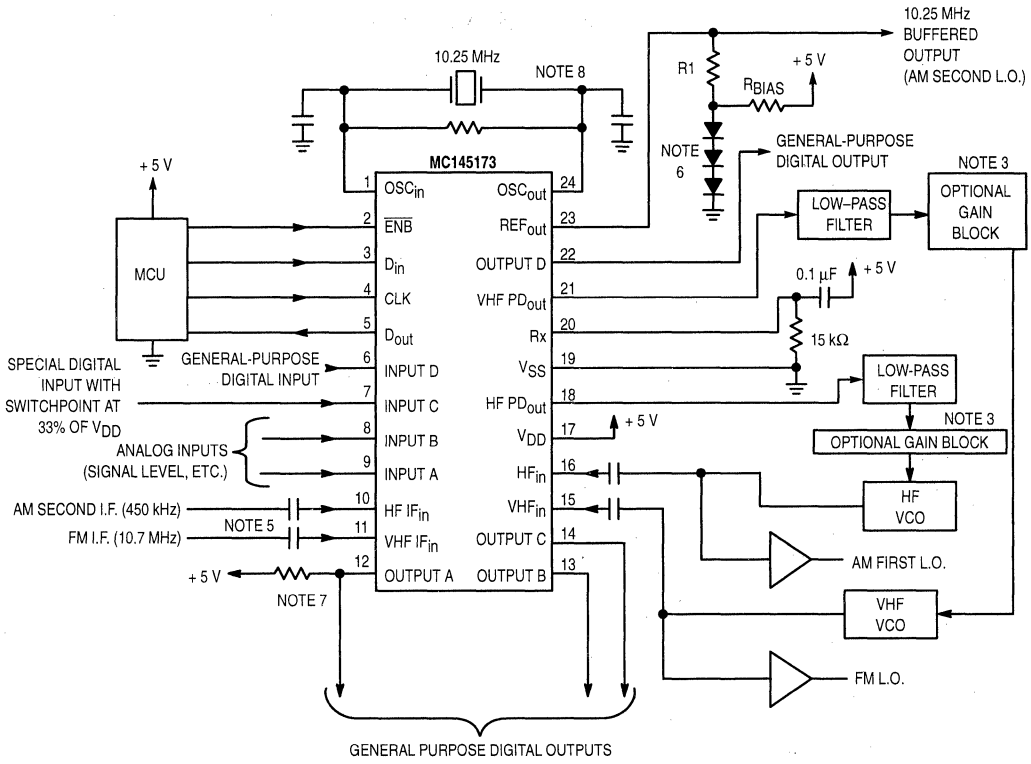
Step 3: Read the Serial Data

To read the F Counter value, set the Read F bit in the C Register to a 1. F SMPL must not be changed; it must be a 1. Take the $\overline{ENB}$ pin low and shift out 24 bits. The value is contained in the least–significant 22 bits. In addition, the CC bit should be checked to ensure it is a 1; this indicates that the count was complete before the data was read. If CC is a 0, the count is not valid. The In D bit is valid and indicates the logic level present on the Input D pin.

NOTE: When the Read F bit is set to a 1, writing to any register is inhibited. After the serial shift which reads the F Register occurs, Read F is automatically cleared to a 0.

CAUTION

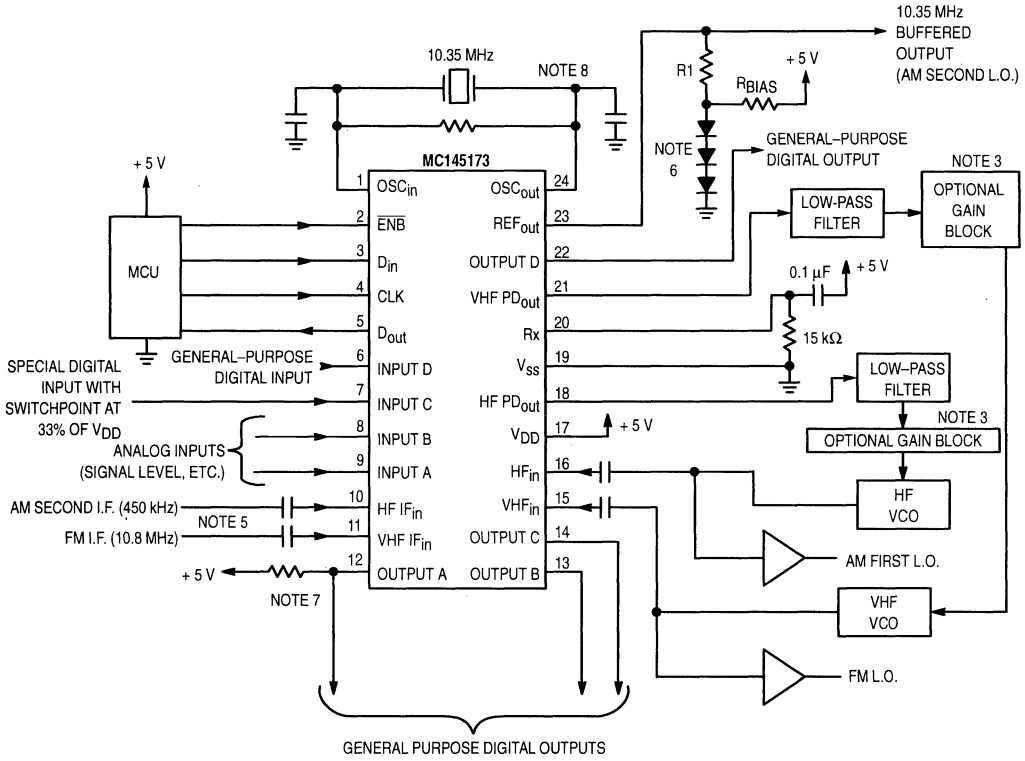
If both Read A and Read F are set simultaneously, a *Read A Register* operation is performed and the *Read F Register* request is ignored.



NOTES:

1. The HF PD_{out} and VHF PD_{out} pins require different low-pass filters. See the Phase-Locked Loop – Low-Pass Filter Design page for more information.
2. For optimum performance, bypass the V_{DD} pin to V_{SS} with a low-inductance capacitor.
3. The gain blocks can be simple one-transistor circuits. See Figures 28 and 29.
4. For the AM band, an R counter divide ratio of 1,025 is used for 10 kHz tuning resolution. The FM band uses an R counter ratio of 205 for 50 kHz tuning resolution.
5. I.F. (intermediate frequency) signals are fed to pins 10 and 11 only if seek or scan feature is included in radio.
6. Diode string is used to limit voltage swing at pin 23; additional or fewer diodes may be used. For full rail-to-rail swing, tie R1 to V_{SS} (GND) and delete the diodes and the R_{BIAS} resistor. **Caution:** this large signal swing may cause a high level of EMI (electromagnetic interference).
7. Pull-up voltage must be at the same potential as the V_{DD} pin or less. Pull-up device other than a resistor may be used.
8. A 10.25 MHz crystal facilitates design of the AM upconversion scheme shown. This results in double conversion for the AM receiver. Optionally, single-conversion designs may be used which offer more flexibility on reference crystal values. For example, a 10.0 MHz crystal could be used which would allow higher-performance 200 kHz tuning resolution for FM.

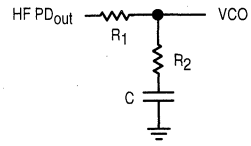
Figure 26. AM-FM Broadcast Receiver Subsystem — USA



NOTES:

1. The HF PD_{out} and VHF PD_{out} pins require different low–pass filters. See the Phase–Locked Loop – Low–Pass Filter Design page for more information.
2. For optimum performance, bypass the V_{DD} pin to V_{SS} with a low–inductance capacitor.
3. The gain blocks can be simple one–transistor circuits. See Figures 28 and 29.
4. For the AM band, an R counter divide ratio of 1,150 is is used for 9 kHz tuning resolution. The FM band uses an R counter ratio of 207 for 50 kHz tuning resolution.
5. I.F. (intermediate frequency) signals are fed to pins 10 and 11 only if seek or scan feature is included in radio.
6. Diode string is used to limit voltage swing at pin 23; additional or fewer diodes may be used. For full rail–to–rail swing, tie R1 to V_{SS} (GND) and delete the diodes and the R_{BIAS} resistor. **Caution:** this large signal swing may cause a high level of EMI (electromagnetic interference).
7. Pull–up voltage must be at the same potential as the V_{DD} pin or less. Pull–up device other than a resistor may be used.
8. A 10.35 MHz crystal facilitates design of the AM upconversion scheme shown. This results in double conversion for the AM receiver. Optionally, single–conversion designs may be used which offer more flexibility on reference crystal values. For example, a 10.0 MHz crystal could be used which would allow higher–performance 100 kHz tuning resolution for FM.

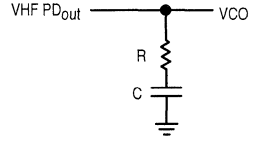
Figure 27. AM–FM Broadcast Receiver Subsystem — Europe



$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NC(R_1 + R_2)}}$$

$$\zeta = 0.5\,\omega_n \left(R_2C + \frac{N}{K_\phi K_{VCO}}\right)$$

$$F(s) = \frac{R_2sC + 1}{(R_1 + R_2)sC + 1}$$



$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NC}}$$

$$\zeta = \frac{R}{2}\sqrt{\frac{K_\phi K_{VCO}C}{N}} = \frac{\omega_n RC}{2}$$

$$Z(s) = \frac{1 + sRC}{sC}$$

NOTE:

For VHF PD_{out}, using K_ϕ in amps per radian with the filter's impedance transfer function, Z(s), maintains units of volts per radian for the detector/ filter combination. Additional sideband filtering can be accomplished by adding a capacitor C′ across R. The corner $\omega_c = 1/RC'$ should be chosen such that ω_n is not significantly affected.

DEFINITIONS:

N = Total Division Ratio in Feedback Loop

K_ϕ (Phase Detector Gain) = $V_{DD}/4\pi$ volts per radian for HF PD_{out}

K_ϕ (Phase Detector Gain) = $I_{PDout}/2\pi$ amps per radian for VHF PD_{out}

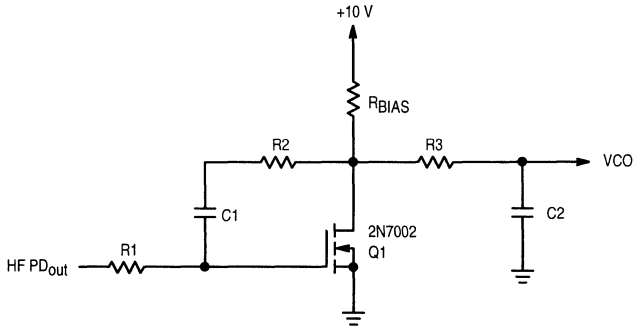
$$K_{VCO}\ (\text{VCO Gain}) = \frac{2\pi\Delta f_{VCO}}{\Delta V_{VCO}}\ \text{radians per volt}$$

For a nominal design starting point, the user might consider a damping factor $\zeta \approx 0.7$ and a natural loop frequency $\omega_n \approx (2\pi f_R/50)$ where f_R is the frequency at the phase detector input. Larger ω_n values result in faster loop lock times and, for similar sideband filtering, higher f_R–related VCO sidebands.

The filters shown above are frequently followed by additional sideband filtering to further attenuate f_R–related VCO sidebands. This additional filtering may be active or passive.

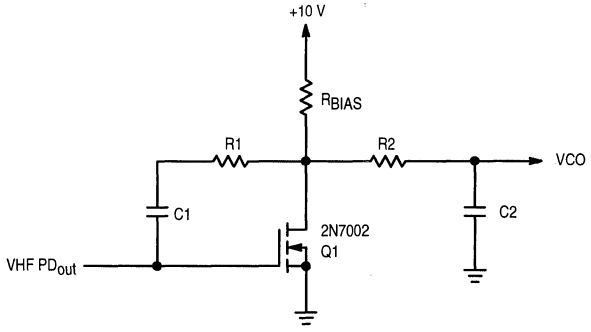
RECOMMENDED READING:

Gardner, Floyd M., *Phaselock Techniques (second edition).* New York, Wiley–Interscience, 1979.
Manassewitsch, Vadim, *Frequency Synthesizers: Theory and Design (second edition).* New York, Wiley–Interscience, 1980.
Blanchard, Alain, *Phase–Locked Loops: Application to Coherent Receiver Design.* New York, Wiley–Interscience, 1976.
Egan, William F., *Frequency Synthesis by Phase Lock.* New York, Wiley–Interscience, 1981.
Rohde, Ulrich L., *Digital PLL Frequency Synthesizers Theory and Design.* Englewood Cliffs, NJ, Prentice–Hall, 1983.
Berlin, Howard M., *Design of Phase–Locked Loop Circuits, with Experiments.* Indianapolis, Howard W. Sams and Co., 1978.
Kinley, Harold, *The PLL Synthesizer Cookbook.* Blue Ridge Summit, PA, Tab Books, 1980.
Seidman, Arthur H., *Integrated Circuits Applications Handbook,* Chapter 17, pp. 538–586. New York, John Wiley & Sons.
Fadrhons, Jan, "Design and Analyze PLLs on a Programmable Calculator," *EDN.* March 5, 1980.
AN535, Phase–Locked Loop Design Fundamentals, Motorola Semiconductor Products, Inc., 1970.
AR254, Phase–Locked Loop Design Articles, Motorola Semiconductor Products, Inc., Reprinted with permission from *Electronic Design* 1987.



NOTES:
1. R1, C1, and R2 form the main filter (determine the loop bandwidth).
2. R3 and C2 are extra filtering; set above loop bandwidth.
3. R1/C1/R2 and R3/C2 are isolated due to Q1. Therefore, there should be minimal interaction.

Figure 28. Active Low–Pass Filter with Gain for HF PD_{out}



NOTES:
1. R1 and C1 form the main filter (determine the loop bandwidth).
2. R2 and C2 are extra filtering; set above loop bandwidth.
3. R1/C1 and R2/C2 are isolated due to Q1. Therefore, there should be minimal interaction.
4. This filter configuration is a concept and has not been examined in the laboratory.

Figure 29. Active Low–Pass Filter with Gain for VHF PD_{out}

MC145190
MC145191

1.1 GHz PLL Frequency Synthesizers

Include On–Board 64/65 Prescalers

2

The MC145190 and MC145191 are single–package synthesizers with serial interfaces capable of direct usage up to 1.1 GHz. A special architecture makes these PLLs very easy to program because a byte–oriented format is utilized. Due to the patented BitGrabber™ registers, no address/steering bits are required for *random access* of the three registers. Thus, tuning can be accomplished via a 3–byte serial transfer to the 24–bit A register. The interface is both SPI and MICROWIRE™ compatible.

Each device features a single–ended current source/sink phase detector output and a double–ended phase detector output. Both phase detectors have linear transfer functions (no dead zones). The maximum current of the single–ended phase detector output is determined by an external resistor tied from the Rx pin to ground. This current can be varied via the serial port.

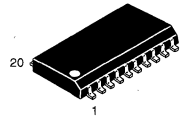
The MC145190 features logic–level converters and high–voltage phase/frequency detectors; the detector supply may range up to 9.5 V. The MC145191 has lower–voltage phase/frequency detectors optimized for single–supply systems of 5 V ±10%.

Each part includes a differential RF input which may be operated in a single–ended mode. Also featured are on–board support of an external crystal and a programmable reference output. The R, A, and N counters are fully programmable. The C register (configuration register) allows the parts to be configured to meet various applications. A patented feature allows the C register to shut off unused outputs, thereby minimizing system noise and interference.

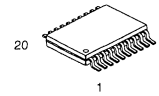
In order to have consistent lock times and prevent erroneous data from being loaded into the counters, on–board circuitry synchronizes the update of the A register if the A or N counters are loading. Similarly, an update of the R register is synchronized if the R counter is loading.

The double–buffered R register allows new divide ratios to be presented to the three counters (R, A, and N) simultaneously.

- Maximum Operating Frequency: 1100 MHz @ V_{in} = 200 mV p–p
- Operating Supply Current: 7 mA Nominal
- Operating Supply Voltage Range (V_{DD} and V_{CC} Pins): 4.5 to 5.5 V
- Operating Supply Voltage Range of Phase Detectors (V_{PD} Pin) —
  MC145190: 8.0 to 9.5 V
  MC145191: 4.5 to 5.5 V
- Current Source/Sink Phase Detector OUTPUT Capability: 2 mA Maximum
- Gain of Current Source/Sink Phase/Frequency Detector Controllable via Serial Port
- Operating Temperature Range: – 40 to + 85°C
- R Counter Division Range: (1 and) 5 to 8191
- Dual–Modulus Capability Provides Total Division up to 262,143
- High–Speed Serial Interface: 4 Mbps
- OUTPUT A Pin, When Configured as Data Out, Permits Cascading of Devices
- Two General–Purpose Digital Outputs — OUTPUT A: Totem–Pole (Push–Pull)
  OUTPUT B: Open–Drain
- Patented Power–Saving Standby Feature with Orderly Recovery for Minimizing Lock Times, Standby Current: 30 μA
- Evaluation Kit Available (Part Numbers MC145190EVK and MC145191EVK). See Evaluation Kit Section



F SUFFIX
SOG PACKAGE
CASE 751J

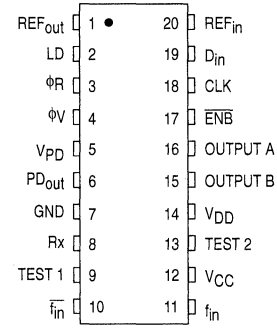


DT SUFFIX
TSSOP
CASE 948D

ORDERING INFORMATION

MC145190F	SOG Package
MC145191F	SOG Package
MC145190DT	TSSOP
MC145191DT	TSSOP

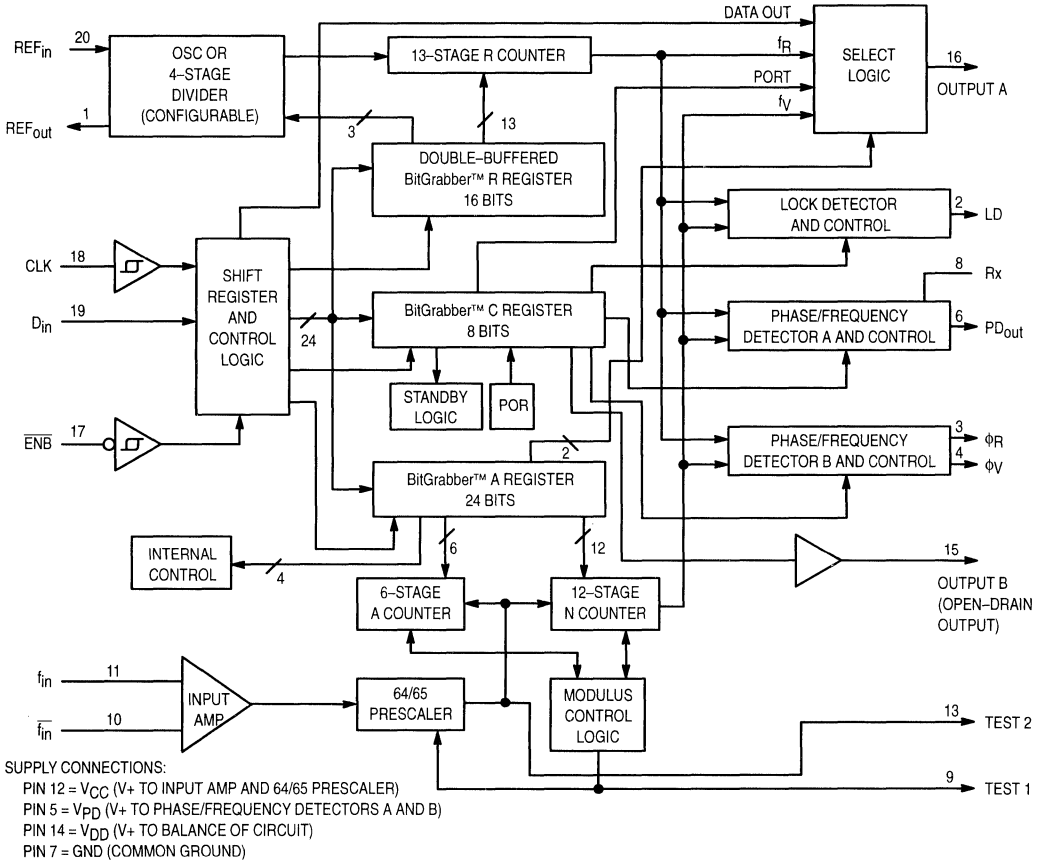
PIN ASSIGNMENT



BitGrabber is a trademark of Motorola Inc. MICROWIRE is a trademark of National Semiconductor Corp.

REV 4
10/95

BLOCK DIAGRAM



MAXIMUM RATINGS* (Voltages Referenced to GND, unless otherwise stated)

Symbol	Parameter	Value	Unit
V_{CC}, V_{DD}	DC Supply Voltage (Pins 12 and 14)	– 0.5 to + 6.0	V
V_{PD}	DC Supply Voltage (Pin 5) MC145190 MC145191	V_{DD} – 0.5 to + 9.5 V_{DD} – 0.5 to + 6.0	V
V_{in}	DC Input Voltage	– 0.5 to V_{DD} + 0.5	V
V_{out}	DC Output Voltage (except OUTPUT B, PD_{out}, ϕR, ϕV)	– 0.5 to V_{DD} + 0.5	V
V_{out}	DC Output Voltage (OUTPUT B, PD_{out}, ϕR, ϕV)	– 0.5 to V_{PD} + 0.5	V
I_{in}, I_{PD}	DC Input Current, per Pin (Includes V_{PD})	± 10	mA
I_{out}	DC Output Current, per Pin	± 20	mA
I_{DD}	DC Supply Current, V_{DD} and GND Pins	± 30	mA
P_D	Power Dissipation, per Package	300	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 seconds	260	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Descriptions section.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit.

ELECTRICAL CHARACTERISTICS

(V_{DD} = V_{CC} = 4.5 to 5.5 V, Voltages Referenced to GND, T_A = −40 to +85°C, unless otherwise stated; MC145190: V_{PD} = 8.0 to 9.5 V; MC145191: V_{PD} = 4.5 to 5.5 V with $V_{DD} \leq V_{PD}$.)

Symbol	Parameter	Test Condition	Guaranteed Limit	Unit
V_{IL}	Maximum Low–Level Input Voltage (D_{in}, CLK, $\overline{ENB}$, REF_{in})	Device in Reference Mode, dc Coupled	0.3 × V_{DD}	V
V_{IH}	Minimum High–Level Input Voltage (D_{in}, CLK, $\overline{ENB}$, REF_{in})	Device in Reference Mode, dc Coupled	0.7 × V_{DD}	V
V_{hys}	Minimum Hysteresis Voltage (CLK, $\overline{ENB}$)		300	mV
V_{OL}	Maximum Low–Level Output Voltage (REF_{out}, OUTPUT A)	I_{out} = 20 µA, Device in Reference Mode	0.1	V
V_{OH}	Minimum High–Level Output Voltage (REF_{out}, OUTPUT A)	I_{out} = –20 µA, Device in Reference Mode	V_{DD} – 0.1	V
I_{OL}	Minimum Low–Level Output Current (REF_{out}, LD, ϕ_R, ϕ_V)	V_{out} = 0.4 V	0.36	mA
I_{OH}	Minimum High–Level Output Current (REF_{out}, LD, ϕ_R, ϕ_V)	V_{out} = V_{DD} – 0.4 V for REF_{out}, LD V_{out} = V_{PD} – 0.4 V for ϕ_R, ϕ_V	– 0.36	mA
I_{OL}	Minimum Low–Level Output Current (OUTPUT A, OUTPUT B)	V_{out} = 0.4 V	1.0	mA
I_{OH}	Minimum High–Level Output Current (OUTPUT A, Only)	V_{out} = V_{DD} – 0.4 V	– 0.6	mA
I_{in}	Maximum Input Leakage Current (D_{in}, CLK, $\overline{ENB}$, REF_{in})	V_{in} = V_{DD} or GND, Device in XTAL Mode	± 1.0	µA
I_{in}	Maximum Input Current (REF_{in})	V_{in} = V_{DD} or GND, Device in Reference Mode	± 150	µA
I_{OZ}	Maximum Output Leakage Current (PD_{out})	V_{out} = V_{PD} – 0.5 V or 0.5 V, Output in High–Impedance State — MC145190 MC145191	± 150 ± 200	nA
I_{OZ}	Maximum Output Leakage Current (OUTPUT B)	V_{out} = V_{PD} or GND, Output in High–Impedance State	± 10	µA
I_{STBY}	Maximum Standby Supply Current (V_{DD} + V_{PD} Pins)	V_{in} = V_{DD} or GND; Outputs Open; Device in Standby Mode, Shut–Down Crystal Mode or REF_{out}–Static–Low Reference Mode; OUTPUT B Controlling V_{CC} per Figure 22	30	µA
I_{PD}	Maximum Phase Detector Quiescent Current (V_{PD} Pin)	Bit C6 = High Which Selects Phase Detector A, PD_{out} = Open, PD_{out} = Static Low or High, Bit C4 = Low Which is ***not*** Standby, I_{Rx} = 113 µA	600	µA
		Bit C6 = Low Which Selects Phase Detector B, ϕ_R and ϕ_V = Open, ϕ_R and ϕ_V = Static Low or High, Bit C4 = Low Which is ***not*** Standby	30	
I_T	Total Operating Supply Current (V_{DD} + V_{PD} + V_{CC} Pins)	f_{in} = 1.1 GHz; REF_{in} = 13 MHz @ 1 V p–p; OUTPUT A = Inactive and No Connect; REF_{out} ÷ 8; ϕ_V, ϕ_R, PD_{out}, LD = No Connect; D_{in}, $\overline{ENB}$, CLK = V_{DD} or GND, Phase Detector B Selected (Bit C6 = Low)	*	mA

* The nominal value = 7 mA. This is not a guaranteed limit.

ANALOG CHARACTERISTICS—CURRENT SOURCE/SINK OUTPUT—PD_{out}

($I_{out} \leq 2$ mA, $V_{DD} = V_{CC} = 4.5$ to 5.5 V, $V_{DD} \leq V_{PD}$. Voltages Referenced to GND)

Parameter	Test Condition	V_{PD}	Guaranteed Limit	Unit
Maximum Source Current Variation (Part–to–Part)	MC145190: $V_{out} = 0.5 \times V_{PD}$	8.0	± 20	%
		9.5	± 20	
	MC145191: $V_{out} = 0.5 \times V_{PD}$	4.5	± 20	%
		5.5	± 20	
Maximum Sink–vs–Source Mismatch (Note 3)	MC145190: $V_{out} = 0.5 \times V_{PD}$	8.0	12	%
		9.5	12	
	MC145191: $V_{out} = 0.5 \times V_{PD}$	4.5	12	%
		5.5	12	
Output Voltage Range (Note 3)	MC145190: I_{out} Variation ≤ 20%	8.0	0.5 to 7.5	V
		9.5	0.5 to 9.0	
	MC145191: I_{out} Variation ≤ 20%	4.5	0.5 to 4.0	V
		5.5	0.5 to 5.0	

NOTES:
1. Percentages calculated using the following formula: (Maximum Value – Minimum Value) / Maximum Value.
2. See Rx Pin Description for external resistor values.
3. This parameter is guaranteed for a given temperature within – 40° to + 85°C.

AC INTERFACE CHARACTERISTICS ($V_{DD} = 4.5$ to 5.5 V, $T_A = -40$ to + 85°C, $C_L = 50$ pF, Input $t_r = t_f = 10$ ns; MC145190: $V_{PD} = 8.0$ to 9.5 V; MC145191: $V_{PD} = 4.5$ to 5.5 V with $V_{DD} \leq V_{PD}$)

Symbol	Parameter	Figure No.	Guaranteed Limit	Unit
f_{clk}	Serial Data Clock Frequency (Note: Refer to Clock t_w below)	1	dc to 4.0	MHz
t_{PLH}, t_{PHL}	Maximum Propagation Delay, CLK to OUTPUT A (Selected as Data Out)	1, 5	105	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay, $\overline{ENB}$ to OUTPUT A (Selected as Port)	2, 5	100	ns
t_{PZL}, t_{PLZ}	Maximum Propagation Delay, $\overline{ENB}$ to OUTPUT B	2, 6	120	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, OUTPUT A and OUTPUT B; t_{THL} ONLY, on OUTPUT B	1, 5, 6	100	ns
C_{in}	Maximum Input Capacitance – D_{in}, $\overline{ENB}$, CLK		10	pF

TIMING REQUIREMENTS

($V_{DD} = V_{CC} = 4.5$ to 5.5 V, $T_A = -40$ to + 85°C, Input $t_r = t_f = 10$ ns unless otherwise indicated)

Symbol	Parameter	Figure No.	Guaranteed Limit	Unit
t_{su}, t_h	Minimum Setup and Hold Times, D_{in} vs CLK	3	20	ns
t_{su}, t_h, t_{rec}	Minimum Setup, Hold and Recovery Times, $\overline{ENB}$ vs CLK	4	100	ns
t_w	Minimum Pulse Width, $\overline{ENB}$	4	*	cycles
t_w	Minimum Pulse Width, CLK	1	125	ns
t_r, t_f	Maximum Input Rise and Fall Times – CLK	1	100	µs

* The minimum limit is 3 REF_{in} cycles or 195 f_{in} cycles, whichever is greater.

SWITCHING WAVEFORMS

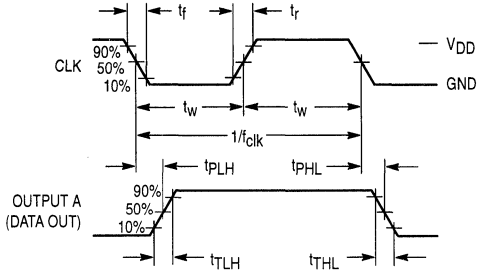


Figure 1.

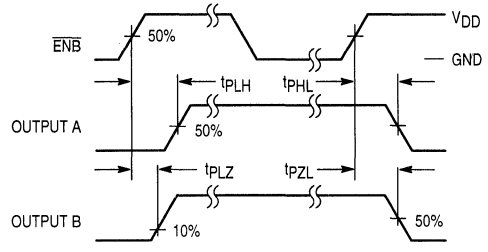


Figure 2.

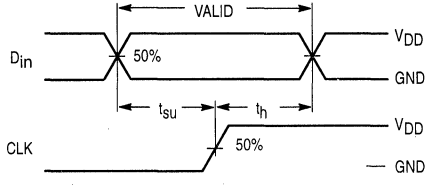


Figure 3.

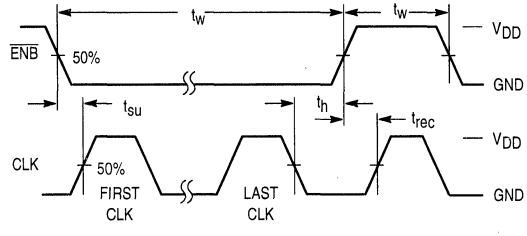
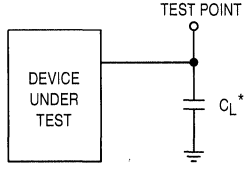
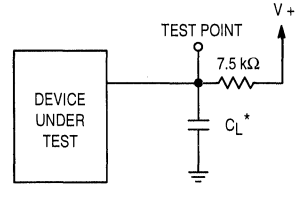


Figure 4.



*Includes all probe and fixture capacitance.

Figure 5. Test Circuit



*Includes all probe and fixture capacitance.

Figure 6. Test Circuit

LOOP SPECIFICATIONS (V_{DD} = V_{CC} = 4.5 to 5.5 V unless otherwise indicated, T_A = – 40 to + 85°C)

Symbol	Parameter	Test Condition	Figure No.	Guaranteed Operating Range		Unit
				Min	Max	
V_{in}	Input Voltage Range, f_{in}	100 MHz ≤ f_{in} < 250 MHz 250 MHz ≤ f_{in} ≤ 1100 MHz	7	400 200	1500 1500	mV p–p
f_{ref}	Input Frequency Range, REF_{in} MC145190 Externally Driven in Reference Mode MC145191	V_{in} = 400 mV p–p V_{in} = 1 V p–p V_{in} = 400 mV p–p V_{in} = 1 V p–p	8	13 6* 12 4.5*	27 27 27 27	MHz
f_{XTAL}	Crystal Frequency, Crystal Mode	C1 ≤ 30 pF, C2 ≤ 30 pF, Includes Stray Capacitance	9	2	15	MHz
f_{out}	Output Frequency, REF_{out}	C_L = 30 pF	10, 12	dc	10	MHz
f	Operating Frequency of the Phase Detectors			dc	2	MHz
t_w	Output Pulse Width, ϕ_R, ϕ_V, LD MC145190 MC145191	f_R in Phase with f_V, C_L = 50 pF, V_{PD} = 5.5 V, V_{DD} = V_{CC} = 5.0 V	11, 12	17	85	ns
t_{TLH}, t_{THL}	Output Transition Times, LD, ϕ_V, ϕ_R — MC145191	C_L = 50 pF, V_{PD} = 5.5 V, V_{DD} = V_{CC} = 5.0 V	11, 12	—	65	ns
C_{in}	Input Capacitance, REF_{in}			—	5	pF

*If lower frequency is desired, use wave shaping or higher amplitude sinusoidal signal.

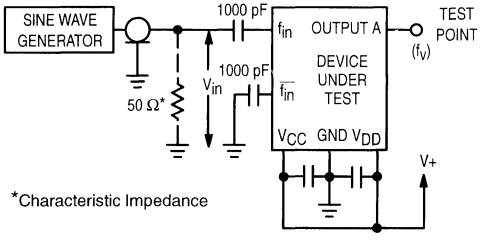


Figure 7. Test Circuit

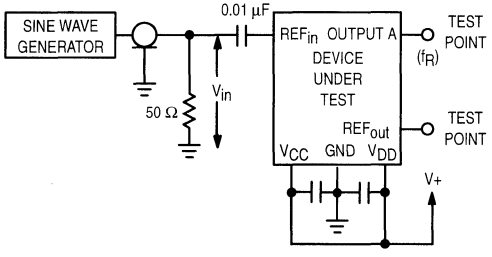


Figure 8. Test Circuit — Reference Mode

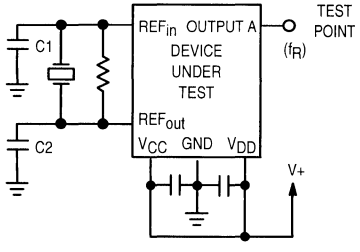


Figure 9. Test Circuit — Crystal Mode

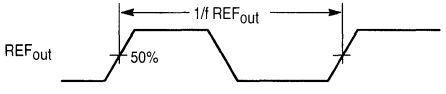


Figure 10. Switching Waveform

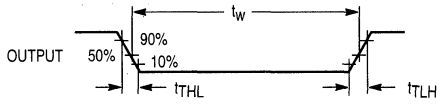


Figure 11. Switching Waveform

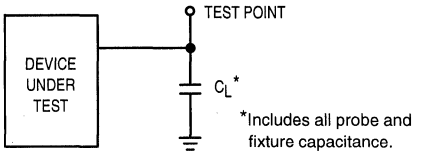
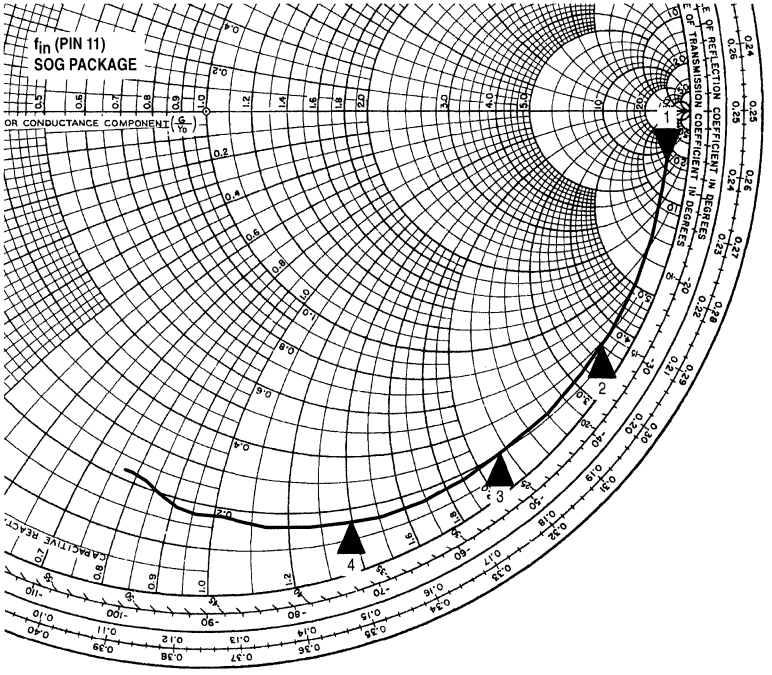


Figure 12. Test Circuit

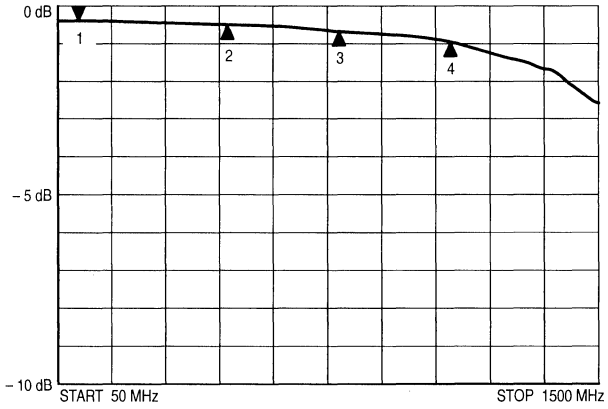
2

NORMALIZED INPUT IMPEDANCE AT f_{in} — SERIES FORMAT (R + jX)
(100 MHz to 1.1 GHz)

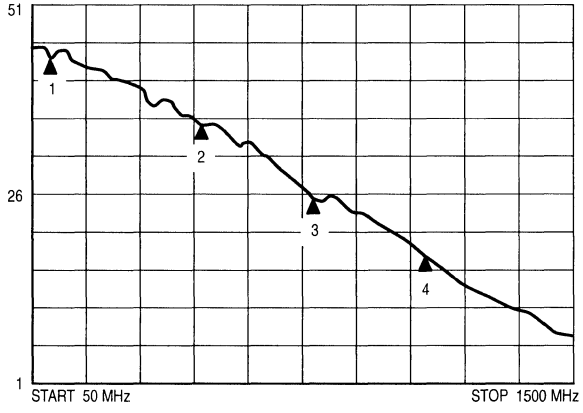


Marker	Frequency (MHz)	Resistance (Ω)	Capacitive Reactance (Ω)	Capacitance (pF)
1	100	338	– 785	2.03
2	500	20.2	– 183	1.74
3	800	11.5	– 109	1.83
4	1100	8.2	– 70.2	2.06

RETURN LOSS AT f_{in}



STANDING WAVE RATIO AT f_{in}



Marker	Frequency (MHz)	SWR	Return Loss (dB)
1	100	43.7	0.40
2	500	34.7	0.48
3	800	25.3	0.68
4	1100	17.9	0.98

PIN DESCRIPTIONS

DIGITAL INTERFACE PINS

D_{in}
Serial Data Input (Pin 19)

The bit stream begins with the most significant bit (MSB) and is shifted in on the low–to–high transition of CLK. The bit pattern is 1 byte (8 bits) long to access the C or configuration register, 2 bytes (16 bits) to access the first buffer of the R register, or 3 bytes (24 bits) to access the A register (see Table 1). The values in the C, R, and A registers do not change during shifting because the transfer of data to the registers is controlled by $\overline{ENB}$.

CAUTION

The value programmed for the N–counter must be greater than or equal to the value of the A–counter.

The 13 least significant bits (LSBs) of the R register are double–buffered. As indicated above, data is latched into the first buffer on a 16–bit transfer. (The 3 MSBs are not double–buffered and have an immediate effect after a 16–bit transfer.) The second buffer of the R register contains the 13 bits for the R counter. This second buffer is loaded with the contents of the first buffer when the A register is loaded (a 24–bit transfer). This allows presenting new values to the R, A, and N counters simultaneously. If this is not required, then the 16–bit transfer may be followed by pulsing $\overline{ENB}$ low with no signal on the CLK pin. This is an alternate method of transferring data to the second buffer of the R register (see Figure 17).

The bit stream needs neither address nor steering bits due to the innovative BitGrabber registers. Therefore, all bits in the stream are available to be data for the three registers. Random access of any register is provided. That is, the registers may be accessed in any sequence. Data is retained in the registers over a supply range of 4.5 to 5.5 V. The formats are shown in Figures 15, 16, and 17.

D_{in} typically switches near 50% of V_{DD} to maximize noise immunity. This input can be directly interfaced to CMOS devices with outputs guaranteed to switch near rail–to–rail. When interfacing to NMOS or TTL devices, either a level shifter (MC74HC14A, MC14504B) or pull–up resistor of 1 kΩ to 10 kΩ must be used. Parameters to consider when sizing the resistor are worst–case I_{OL} of the driving device, maximum tolerable power consumption, and maximum data rate.

Table 1. Register Access
(MSBs are shifted in first; C0, R0, and A0 are the LSBs)

Number of Clocks	Accessed Register	Bit Nomenclature
8	C Register	C7, C6, C5, . . ., C0
16	R Register	R15, R14, R13, . . ., R0
24	A Register	A23, A22, A21, . . ., A0
Other Values ≤ 32	See Figure 13	
Values > 32	See Figures 22 – 25	

CLK
Serial Data Clock Input (Pin 18)

Low–to–high transitions on CLK shift bits available at the D_{in} pin, while high–to–low transitions shift bits from OUTPUT A (when configured as Data Out, see Pin 16). The 24–1/2–stage shift register is static, allowing clock rates down to dc in a continuous or intermittent mode.

Eight clock cycles are required to access the C register. Sixteen clock cycles are needed for the first buffer of the R register. Twenty–four cycles are used to access the A register. See Table 1 and Figures 15, 16, and 17. The number of clocks required for cascaded devices is shown in Figures 24 through 26.

CLK typically switches near 50% of V_{DD} and has a Schmitt–triggered input buffer. Slow CLK rise and fall times are allowed. See the last paragraph of **D_{in}** for more information.

NOTE

To guarantee proper operation of the power–on reset (POR) circuit, the CLK pin must be held at GND (with $\overline{ENB}$ being a don't care) or $\overline{ENB}$ must be held at the potential of the V+ pin (with CLK being a don't care) during power–up. As an alternative, the bit sequence of Figure 13 may be used.

$\overline{ENB}$
Active Low Enable Input (Pin 17)

This pin is used to activate the serial interface to allow the transfer of data to/from the device. When $\overline{ENB}$ is in an inactive high state, shifting is inhibited and the port is held in the initialized state. To transfer data to the device, $\overline{ENB}$ (which must start inactive high) is taken low, a serial transfer is made via D_{in} and CLK, and $\overline{ENB}$ is taken back high. The low–to–high transition on $\overline{ENB}$ transfers data to the C or A registers and first buffer of the R register, depending on the data stream length per Table 1.

NOTE

Transitions on $\overline{ENB}$ must not be attempted while CLK is high. This puts the device out of synchronization with the microcontroller. Resynchronization occurs whenever $\overline{ENB}$ is high and CLK is low.

This input is also Schmitt–triggered and switches near 50% of V_{DD}, thereby minimizing the chance of loading erroneous data into the registers. See the last paragraph of **D_{in}** for more information.

For POR information, see the note for the **CLK pin**.

OUTPUT A
Configurable Digital Output (Pin 16)

OUTPUT A is selectable as f_R, f_V, Data Out, or Port. Bits A22 and A23 in the A register control the selection; see Figure 16.

If A23 = A22 = high, OUTPUT A is configured as f_R. This signal is the buffered output of the 13–stage R counter. The f_R signal appears as normally low and pulses high, and can be used to verify the divide ratio of the R counter. This ratio extends from 5 to 8191 and is determined by the binary value loaded into bits R0–R12 in the R register. Also, direct access to the phase detectors via the REF_{in} pin is allowed by choosing a divide value of 1 (see Figure 17). The maximum frequency at which the phase detectors operate is 2 MHz. Therefore, the frequency of f_R should not exceed 2 MHz.

If A23 = high and A22 = low, OUTPUT A is configured as f_V. This signal is the buffered output of the 12–stage N counter. The f_V signal appears as normally low and pulses high, and can be used to verify the operation of the prescaler,

A counter, and N counter. The divide ratio between the f_{in} input and the f_V signal is $N \times 64 + A$. N is the divide ratio of the N counter and A is the divide ratio of the A counter. These ratios are determined by bits loaded into the A register. See Figure 16. The maximum frequency at which the phase detectors operate is 2 MHz. Therefore, the frequency of f_V should not exceed 2 MHz.

If A23 = low and A22 = high, OUTPUT A is configured as Data Out. This signal is the serial output of the 24–1/2–stage shift register. The bit stream is shifted out on the high–to–low transition of the CLK input. Upon power up, OUTPUT A is automatically configured as Data Out to facilitate cascading devices.

If A23 = A22 = low, OUTPUT A is configured as Port. This signal is a general–purpose digital output which may be used as an MCU port expander. This signal is low when the Port bit (C1) of the C register is low, and high when the Port bit is high.

OUTPUT B
Open–Drain Digital Output (Pin 15)

This signal is a general–purpose digital output which may be used as an MCU port expander. This signal is low when the Out B bit (C0) of the C register is low. When the Out B bit is high, OUTPUT B assumes the high–impedance state. OUTPUT B may be pulled up through an external resistor or active circuitry to any voltage less than or equal to the potential of the V_{PD} pin. **Note**: the maximum voltage allowed on the V_{PD} pin is 9.5 V for the MC145190 and 5.5 V for the MC145191.

Upon power–up, power–on reset circuitry forces OUTPUT B to a low level.

REFERENCE PINS

REF_{in} and REF_{out}
Reference Input and Reference Output (Pins 20 and 1)

Configurable pins for a Crystal or an External Reference. This pair of pins can be configured in one of two modes: the crystal mode or the reference mode. Bits R13, R14, and R15 in the R register control the modes as shown in Figure 17.

In crystal mode, these pins form a reference oscillator when connected to terminals of an external parallel–resonant crystal. Frequency–setting capacitors of appropriate values as recommended by the crystal supplier are connected from each of the two pins to ground (up to a maximum of 30 pF each, including stray capacitance). An external resistor of 1 MΩ to 15 MΩ is connected directly across the pins to ensure linear operation of the amplifier. The device is designed to operate with crystals up to 15 MHz; the required connections are shown in Figure 9. To turn on the oscillator, bits R15, R14, and R13 must have an octal value of one (001 in binary, respectively). This is the active–crystal mode shown in Figure 17. In this mode, the crystal oscillator runs and the R Counter divides the crystal frequency, unless the part is in standby. If the part is placed in standby via the C register, the oscillator runs, but the R counter is stopped. However, if bits R15 to R13 have a value of 0, the oscillator is stopped, which saves additional power. This is the shut–down crystal mode (shown in Figure 17) and can be engaged whether in standby or not.

In the reference mode, REF_{in} (Pin 20) accepts a signal up to 27 MHz from an external reference oscillator, such as a TCXO. A signal swinging from at least the V_{IL} to V_{IH} levels listed in the Electrical Characteristics table may be directly coupled to the pin. If the signal is less than this level, ac coupling must be used as shown in Figure 8. Due to an on–board resistor which is engaged in the reference modes, an external biasing resistor tied between REF_{in} and REF_{out} is not required.

With the reference mode, the REF_{out} pin is configured as the output of a divider. As an example, if bits R15, R14, and R13 have an octal value of seven, the frequency at REF_{out} is the REF_{in} frequency divided by 16. In addition, Figure 17 shows how to obtain ratios of eight, four, and two. A ratio of one–to–one can be obtained with an octal value of three. Upon power up, a ratio of eight is automatically initialized. The maximum frequency capability of the REF_{out} pin is 10 MHz. Therefore, for REF_{in} frequencies above 10 MHz, the one–to–one ratio may not be used. Likewise, for REF_{in} frequencies above 20 MHz, the ratio must be more than two.

If REF_{out} is unused, an octal value of two should be used for R15, R14, and R13 and the REF_{out} pin should be floated. A value of two allows REF_{in} to be functional while disabling REF_{out}, which minimizes dynamic power consumption and electromagnetic interference (EMI).

LOOP PINS

f_{in} and $\overline{f_{in}}$
Frequency Inputs (Pins 11 and 10)

These pins are frequency inputs from the VCO. These pins feed the on–board RF amplifier which drives the 64/65 prescaler. These inputs may be fed differentially. However, they usually are used in a single–ended configuration (shown in Figure 7). Note that f_{in} is driven while $\overline{f_{in}}$ must be tied to ground via a capacitor.

Motorola does not recommend driving $\overline{f_{in}}$ while terminating f_{in} because this configuration is not tested for sensitivity. The sensitivity is dependent on the frequency as shown in the Loop Specifications table.

PD_{out}
Single–Ended Phase/Frequency Detector Output (Pin 6)

This is a three–state current–source/sink output for use as a loop error signal when combined with an external low–pass filter. The phase/frequency detector is characterized by a linear transfer function (no dead zone). The operation of the phase/frequency detector is described below and is shown in Figure 18.

POL bit (C7) in the C register = low (see Figure 15)
- Frequency of $f_V > f_R$ or Phase of f_V Leading f_R: current–sinking pulses from a floating state
- Frequency of $f_V < f_R$ or Phase of f_V Lagging f_R: current–sourcing pulses from a floating state
- Frequency and Phase of $f_V = f_R$: essentially a floating state; voltage at pin determined by loop filter

POL bit (C7) = high
- Frequency of $f_V > f_R$ or Phase of f_V Leading f_R: current–sourcing pulses from a floating state
- Frequency of $f_V < f_R$ or Phase of f_V Lagging f_R: current–sinking pulses from a floating state
- Frequency and Phase of $f_V = f_R$: essentially a floating state; voltage at pin determined by loop filter

This output can be enabled, disabled, and inverted via the C register. If desired, PD_{out} can be forced to the floating state by utilization of the disable feature in the C register (bit C6). This is a patented feature. Similarly, PD_{out} is forced to the

floating state when the device is put into standby (STBY bit C4 = high).

The PD_{out} circuit is powered by V_{PD}. The phase detector gain is controllable by bits C3, C2, and C1: gain (in amps per radian) = PD_{out} current divided by 2π.

ϕ_R and ϕ_V (Pins 3 and 4)
Double–Ended Phase/Frequency Detector Outputs

These outputs can be combined externally to generate a loop error signal. Through use of a Motorola patented technique, the detector's dead zone has been eliminated. Therefore, the phase/frequency detector is characterized by a linear transfer function. The operation of the phase/frequency detector is described below and is shown in Figure 18.

POL bit (C7) in the C register = low (see Figure 15)
Frequency of $f_V > f_R$ or Phase of f_V Leading f_R: ϕ_V = negative pulses, ϕ_R = essentially high
Frequency of $f_V < f_R$ or Phase of f_V Lagging f_R: ϕ_V = essentially high, ϕ_R = negative pulses
Frequency and Phase of $f_V = f_R$: ϕ_V and ϕ_R remain essentially high, except for a small minimum time period when both pulse low in phase
POL bit (C7) = high
Frequency of $f_V > f_R$ or Phase of f_V Leading f_R: ϕ_R = negative pulses, ϕ_V = essentially high
Frequency of $f_V < f_R$ or Phase of f_V Lagging f_R: ϕ_R = essentially high, ϕ_V = negative pulses
Frequency and Phase of $f_V = f_R$: ϕ_V and ϕ_R remain essentially high, except for a small minimum time period when both pulse low in phase

These outputs can be enabled, disabled, and interchanged via C register bits C6 or C4. This is a patented feature. Note that when disabled or in standby, ϕ_R and ϕ_V are forced to their rest condition (high state).

The ϕ_R and ϕ_V output signal swing is approximately from GND to V_{PD}.

LD
Lock Detector Output (Pin 2)

This output is essentially at a high level with narrow low–going pulses when the loop is locked (f_R and f_V of the same phase and frequency). The output pulses low when f_V and f_R are out of phase or different frequencies. LD is the logical ANDing of ϕ_R and ϕ_V (see Figure 18).

This output can be enabled and disabled via the C register. This is a patented feature. Upon power up, on–chip initialization circuitry disables LD to a static low logic level to prevent a false "lock" signal. If unused, LD should be disabled and left open.

The LD output signal swing is approximately from GND to V_{DD}.

Rx
External Resistor (Pin 8)

A resistor tied between this pin and GND, in conjunction with bits in the C register, determines the amount of current that the PD_{out} pin sinks and sources. When bits C2 and C3 are both set high, the maximum current is obtained at PD_{out}; see Tables 2 and 3 for other values of current. To achieve a maximum current of 2 mA, the resistor should be about 47 kΩ when V_{PD} is 9 V or about 18 kΩ when V_{PD} is 5.0 V. See Figure 14 if lower maximum current values are desired.

When the ϕ_R and ϕ_V outputs are used, the Rx pin may be floated.

TEST POINT PINS

TEST 1
Modulus Control Signal (Pin 9)

This pin may be used in conjunction with the Test 2 pin for access to the on–board 64/65 prescaler. When Test 1 is low, the prescaler divides by 65. When high, the prescaler divides by 64.

CAUTION

This pin is an unbuffered output and ***must*** be floated in an actual application. This pin must be attached to an isolated pad with no trace. There is the possibility that the device may be modified and have this lead clipped at the body of the package.

TEST 2
Prescaler Output (Pin 13)

This pin may be used to access to the on–board 64/65 prescaler output.

CAUTION

This pin is an unbuffered output and ***must*** be floated in an actual application. This pin must be attached to an isolated pad with no trace. There is the possibility that the device may be modified and have this lead clipped at the body of the package.

POWER SUPPLY PINS

V_{DD}
Positive Power Supply (Pin 14)

This pin supplies power to the main CMOS digital portion of the device. The voltage range is + 4.5 to + 5.5 V with respect to the GND pin.

For optimum performance, V_{DD} should be bypassed to GND using a low–inductance capacitor mounted very close to these pins. Lead lengths on the capacitor should be minimized.

V_{CC}
Positive Power Supply (Pin 12)

This pin supplies power to the RF amp and 64/65 prescaler. The voltage range is +4.5 to +5.5 V with respect to the GND pin. In the standby mode, the VCC pin still draws a few milliamps from the power supply. This current drain can be eliminated with the use of transistor Q1 as shown in Figure 22.

For optimum performance, VCC should be bypassed to GND using a low–inductance capacitor mounted very close to these pins. Lead lengths on the capacitor should be minimized.

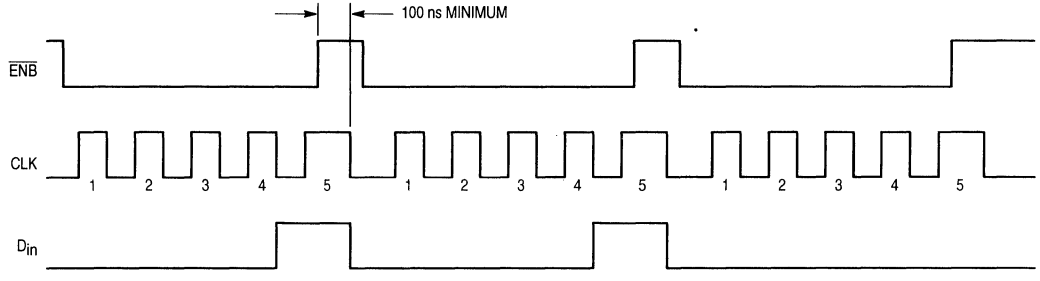
V_{PD}
Positive Power Supply (Pin 5)

This pin supplies power to both phase/frequency detectors A and B. The voltage applied on this pin must be no less than the potential applied to the V_{DD} pin. The maximum voltage can be +9.5 V with respect to the GND pin for the MC145190 and +5.5 V for the MC145191.

For optimum performance, V_{PD} should be bypassed to GND using a low–inductance capacitor mounted very close to these pins. Lead lengths on the capacitor should be minimized.

GND
Ground (Pin 7)

Common ground.



NOTE: It may not be convenient to control the $\overline{ENB}$ or CLK pins during power up per the Pin Descriptions. If this is the case, the part may be initialized through the serial port as shown in the figure above. The sequence is similar to accessing the registers except that the CLK must remain high at least 100 ns after $\overline{ENB}$ is brought high. Note that 3 groups of 5 bits are needed.

Figure 13. Initializing the PLL through the Serial Port

MC145190
Nominal PD_{out} Spurious Current vs f_R Frequency
($1\ V < PD_{out} < V_{PD} - 1\ V$)

f_R (kHz)	Current (RMS nA)
10	1.6
20	5.3
50	22
100	95
200	320

MC145191
Nominal PD_{out} Spurious Current vs f_R Frequency
($1\ V < PD_{out} < V_{PD} - 1\ V$)

f_R (kHz)	Current (RMS nA)
10	3.6
20	4.6
50	17
100	75
200	244

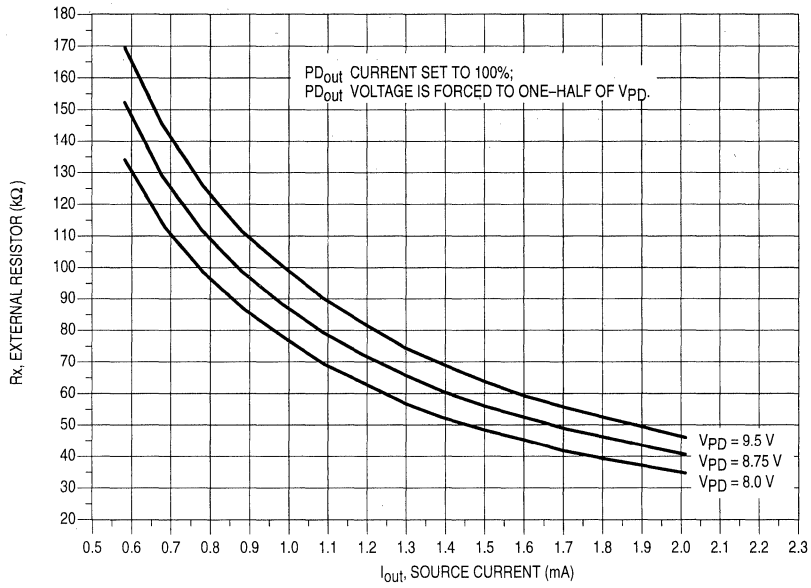
NOTE: For information on spurious current measurement see AN1253/D, "An Improved PLL Design Method Without ω_n and ζ".

Table 2. PD_{out} Current, C1 = Low with OUTPUT A *NOT* Selected as "Port"; Also, Default Mode When OUTPUT A Selected as "Port"

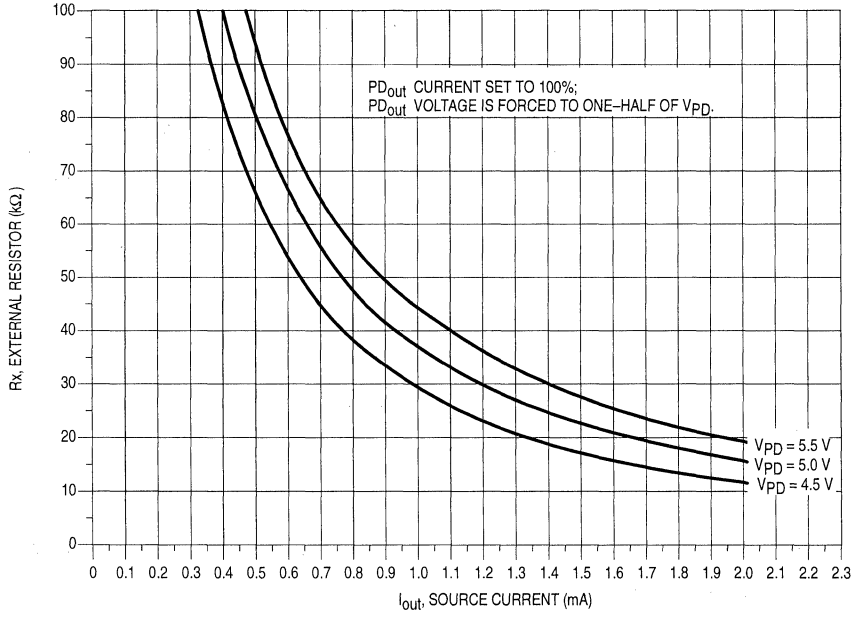
C3	C2	PD_{out} Current
0	0	70%
0	1	80%
1	0	90%
1	1	100%

Table 3. PD_{out} Current, C1 = High with OUTPUT A *NOT* Selected as "Port"

C3	C2	PD_{out} Current
0	0	25%
0	1	50%
1	0	75%
1	1	100%



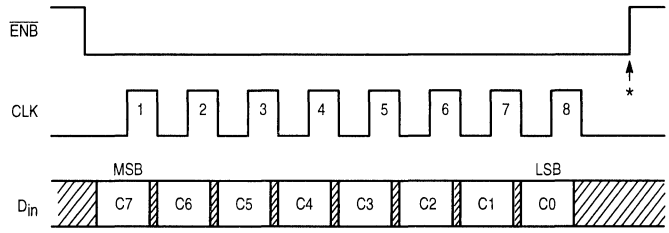
Nominal MC145190 PD_{out} Source Current vs Rx Resistance



Nominal MC145191 PD_{out} Source Current vs Rx Resistance

NOTE: The MC145191 is optimized for Rx values in the 18 kΩ to 40 kΩ range. For example, to achieve 0.3 mA of output current, it is preferable to use a 30–kΩ resistor for Rx and bit settings for 25% (as shown in Table 3).

Figure 14.



* At this point, the new byte is transferred to the C register and stored. No other registers are affected.

C7 — POL: Selects the output polarity of the phase/frequency detectors. When set high, this bit inverts the polarity of PD_{out} and interchanges the ϕ_R function with ϕ_V as depicted in Figure 18. Also see the phase detector output pin descriptions for more information. This bit is cleared low at power up.

C6 — PDA/B: Selects which phase/frequency detector is to be used. When set high, enables the output of phase/frequency detector A (PD_{out}) and disables phase/frequency detector B by forcing ϕ_R and ϕ_V to the static high state. When cleared low, phase/frequency detector B is enabled (ϕ_R and ϕ_V) and phase/frequency detector A is disabled with PD_{out} forced to the high–impedance state. This bit is cleared low at power up.

C5 — LDE: Enables the lock detector output (LD) when set high. When the bit is cleared low, the LD output is forced to a static low level. This bit is cleared low at power up.

C4 — STBY: When set high, places the CMOS section of device, which is powered by the V_{DD} and V_{PD} pins, in the standby mode for reduced power consumption: PD_{out} is forced to the high–impedance state, ϕ_R and ϕ_V are forced high, the A, N, and R counters are inhibited from counting, and the Rx current is shut off. In standby, the state of LD is determined by bit C5. C5 low forces LD low (no change). C5 high forces LD static high. During standby, data is retained in the A, R, and C registers. The condition of REF/OSC circuitry is determined by the control bits in the R register: R13, R14, and R15. However, if REF_{out} = static low is selected, the internal feedback resistor is disconnected and the input is inhibited when in standby; in addition, the REF_{in} input only presents a capacitive load. NOTE: Standby does not affect the other modes of the REF/OSC circuitry.

When C4 is reset low, the part is taken out of standby in 2 steps. First, the REF_{in} (only in one mode) resistor is reconnected, all counters are enabled, and the Rx current is enabled. Any f_R and f_V signals are inhibited from toggling the phase/frequency detectors and lock detector. Second, when the first f_V pulse occurs, the R counter is jam loaded, and the phase/frequency and lock detectors are initialized. Immediately after the jam load, the A, N, and R counters begin counting down together. At this point, the f_R and f_V pulses are enabled to the phase and lock detectors. (Patented feature.)

C3, C2 — I2, I1: Controls the PD_{out} source/sink current per Tables 2 and 3. With both bits high, the maximum current (as set by Rx per Figure 14) is available. Also, see C1 bit description.

C1 — Port: When the OUTPUT A pin is selected as "Port" via bits A22 and A23, C1 determines the state of OUTPUT A. When C1 is set high, OUTPUT A is forced high; C1 low forces OUTPUT A low. When OUTPUT A is NOT selected as "Port," C1 controls whether the PD_{out} step size is 10% or 25%. (See Tables 2 and 3.) When low, steps are 10%. When high, steps are 25%. Default is 10% steps when OUTPUT A is selected as "Port." The Port bit is not affected by the standby mode.

C0 — Out B: Determines the state of OUTPUT B. When C0 is set high, OUTPUT B is high–impedance; C0 low forces OUTPUT B low. The Out B bit is not affected by the standby mode. This bit is cleared low at power up.

Figure 15. C Register Access and Format (8 Clock Cycles are Used)

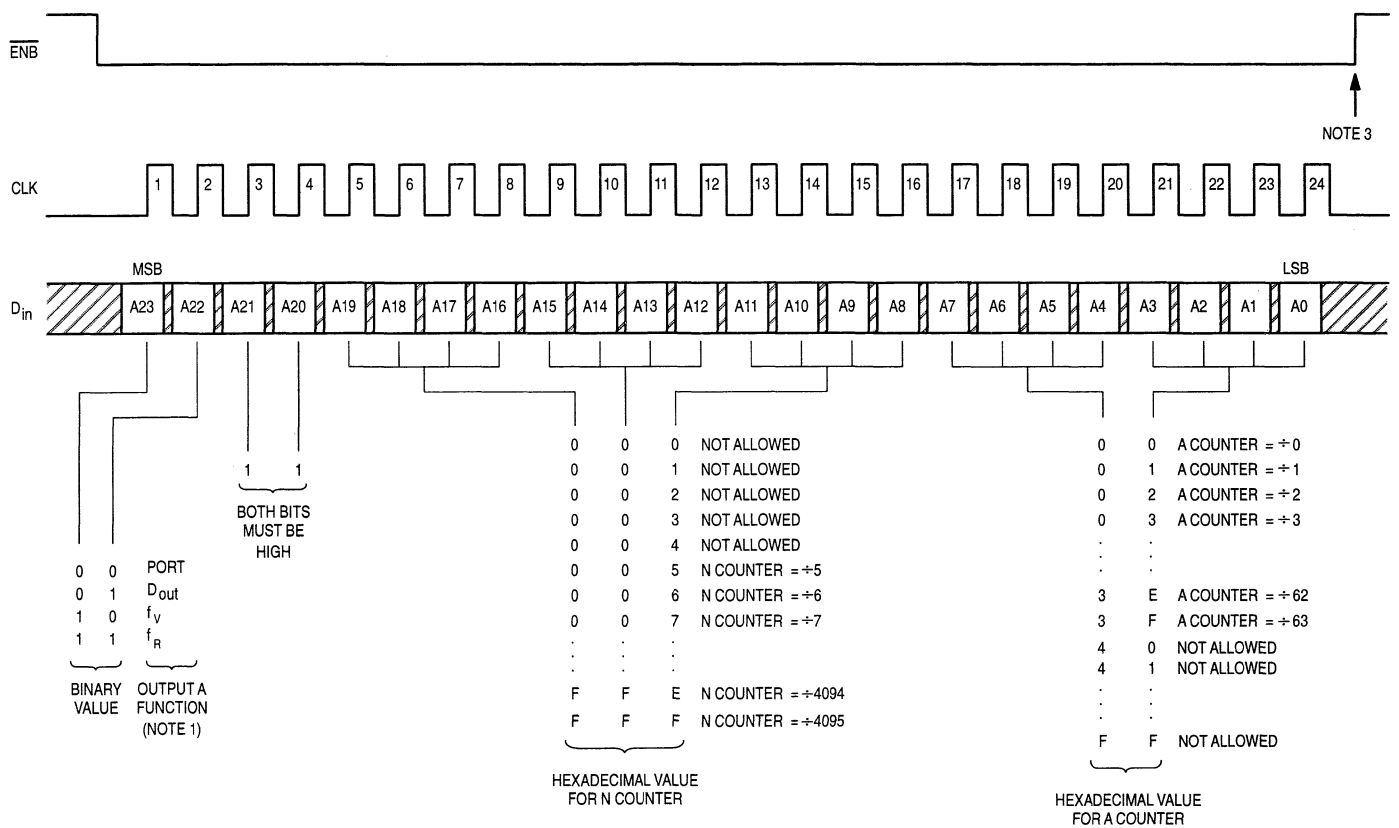
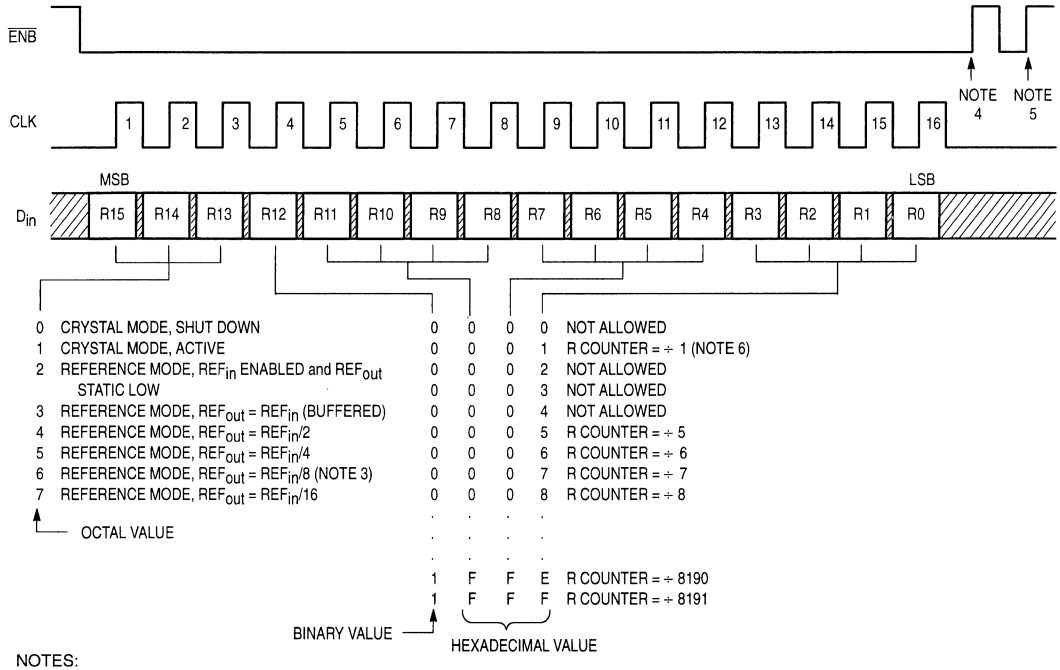


Figure 16. A Register Access and Format (24 Clock Cycles are Used)

NOTES:

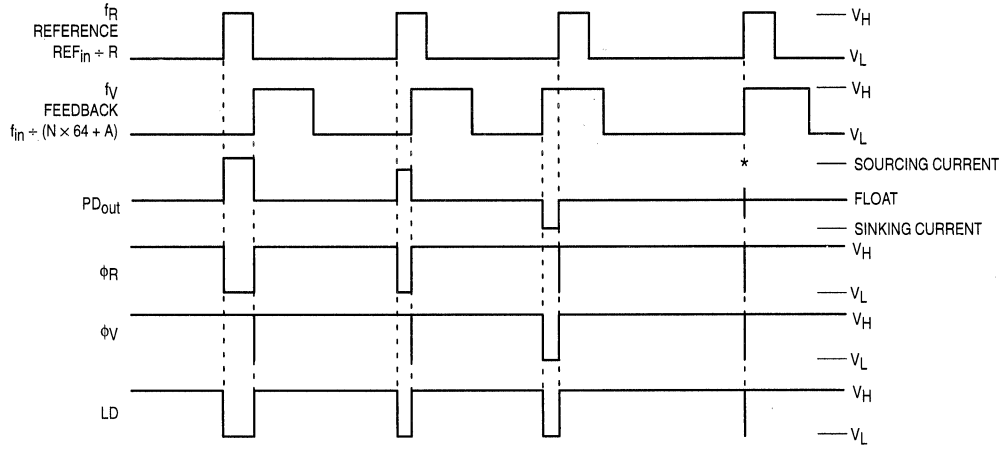
1. A power–on initialize circuit forces the OUTPUT A function to default to Data Out.
2. The values programmed for the N counter must be greater than or equal to the values programmed for the A counter. This results in a total divide value = N x 64 + A.
3. At this point, the three new bytes are transferred to the A register. In addition, the 13 LSBs in the first buffer of the R register are transferred to the R register's second buffer. Thus, the R, N, and A counters can be presented new divide ratios at the same time. The first buffer of the R register is not affected. The C register is not affected.



NOTES:

1. Bits R15 through R13 control the configurable "OSC or 4–stage divider" block (see Block Diagram).
2. Bits R12 through R0 control the "13–stage R counter" block (see Block Diagram).
3. A power–on initialize circuit forces a default REF_{in} to REF_{out} ratio of eight.
4. At this point, bits R13, R14, and R15 are stored and sent to the "OSC or 4–Stage Divider" block in the Block Diagram. Bits R0 through R12 are loaded into the first buffer in the double–buffered section of the R register. Therefore, the R counter divide ratio is not altered yet and retains the previous ratio loaded. The C and A registers are not affected.
5. At this point, bits R0 through R12 are transferred to the second buffer of the R register. The R counter begins dividing by the new ratio after completing the rest of the present count cycle. CLK must be low during the $\overline{ENB}$ pulse, as shown. Also, see note 3 of Figure 16 for an alternate method of loading the second buffer in the R register. The C and A registers are not affected. The first buffer of the R register is not affected.
6. Allows direct access to reference input of phase/frequency detectors.

Figure 17. R Register Access and Format (16 Clock Cycles Are Used)



V_H = High voltage level
V_L = Low voltage level
*At this point, when both f_R and f_V are in phase, the output source and sink circuits are turned on for a short interval.
NOTE: The PD_{out} either sources or sinks current during out–of–lock conditions. When locked in phase and frequency, the output is high impedance and the voltage at that pin is determined by the low–pass filter capacitor. PD_{out}, ϕR, and ϕV are shown with the polarity bit (POL) = low; see Figure 14 for POL.

Figure 18. Phase/Frequency Detectors and Lock Detector Output Waveforms

DESIGN CONSIDERATIONS

CRYSTAL OSCILLATOR CONSIDERATIONS

The following options may be considered to provide a reference frequency to Motorola's CMOS frequency synthesizers.

Use of a Hybrid Crystal Oscillator

Commercially available temperature–compensated crystal oscillators (TCXOs) or crystal–controlled data clock oscillators provide very stable reference frequencies. An oscillator capable of CMOS logic levels at the output may be direct or dc coupled to REF_{in}. If the oscillator does not have CMOS logic levels on the outputs, capacitive or ac coupling to REF_{in} may be used (see Figure 8).

For additional information about TCXOs and data clock oscillators, please consult the latest version of the *eem Electronic Engineers Master Catalog,* the *Gold Book,* or similar publications.

Design an Off–Chip Reference

The user may design an off–chip crystal oscillator using discrete transistors or ICs specifically developed for crystal oscillator applications, such as the MC12061 MECL device. The reference signal from the MECL device is ac coupled to REF_{in} (see Figure 8). For large amplitude signals (standard CMOS logic levels), dc coupling may be used.

Use of the On–Chip Oscillator Circuitry

The on–chip amplifier (a digital inverter) along with an appropriate crystal may be used to provide a reference source frequency. A fundamental mode crystal, parallel resonant at the desired operating frequency, should be connected as shown in Figure 19.

The crystal should be specified for a loading capacitance (C_L) which does not exceed approximately 20 pF when used at the highest operating frequency of 15 MHz. Assuming R1 = 0 Ω, the shunt load capacitance (C_L) presented across the crystal can be estimated to be:

$$C_L = \frac{C_{in}C_{out}}{C_{in}+C_{out}} + C_a + C_{stray} + \frac{C1 \cdot C2}{C1 + C2}$$

where

C_{in} = 5 pF (see Figure 20)
C_{out} = 6 pF (see Figure 20)
C_a = 1 pF (see Figure 20)
C1 and C2 = external capacitors (see Figure 19)
C_{stray} = the total equivalent external circuit stray capacitance appearing across the crystal terminals

The oscillator can be "trimmed" on–frequency by making a portion or all of C1 variable. The crystal and associated components must be located as close as possible to the REF_{in} and REF_{out} pins to minimize distortion, stray capacitance, stray inductance, and startup stabilization time. Circuit stray capacitance can also be handled by adding the appropriate stray value to the values for C_{in} and C_{out}. For this approach, the term C_{stray} becomes 0 in the above expression for C_L.

Power is dissipated in the effective series resistance of the crystal, R_e, in Figure 21. The maximum drive level specified by the crystal manufacturer represents the maximum stress that the crystal can withstand without damage or excessive shift in operating frequency. R1 in Figure 19 limits the drive level. The use of R1 is not necessary in most cases.

To verify that the maximum dc supply voltage does not cause the crystal to be overdriven, monitor the output

frequency (f_R) at OUTPUT A as a function of supply voltage. (REF_{out} is not used because loading impacts the oscillator.) The frequency should increase very slightly as the dc supply voltage is increased. An overdriven crystal decreases in frequency or becomes unstable with an increase in supply voltage. The operating supply voltage must be reduced or R1 must be increased in value if the overdriven condition exists. The user should note that the oscillator start–up time is proportional to the value of R1.

Through the process of supplying crystals for use with CMOS inverters, many crystal manufacturers have developed expertise in CMOS oscillator design with crystals. Discussions with such manufacturers can prove very helpful (see Table 4).

RECOMMENDED READING

Technical Note TN–24, Statek Corp.

Technical Note TN–7, Statek Corp.

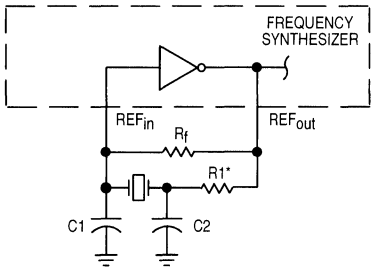
E. Hafner, "The Piezoelectric Crystal Unit–Definitions and Method of Measurement", *Proc. IEEE,* Vol. 57, No. 2, Feb. 1969.

D. Kemper, L. Rosine, "Quartz Crystals for Frequency Control", *Electro–Technology,* June 1969.

P. J. Ottowitz, "A Guide to Crystal Selection", *Electronic Design,* May 1966.

D. Babin, "Designing Crystal Oscillators", *Machine Design,* March 7, 1985.

D. Babin, "Guidelines for Crystal Oscillator Design", *Machine Design,* April 25, 1985.



* May be needed in certain cases. See text.

Figure 19. Pierce Crystal Oscillator Circuit

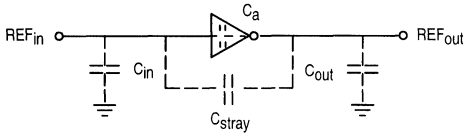
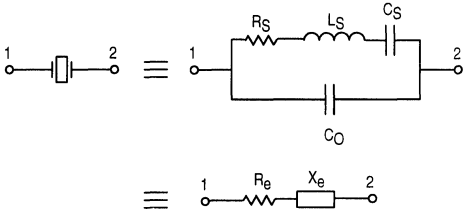


Figure 20. Parasitic Capacitances of the Amplifier and C_{stray}



NOTE: Values are supplied by crystal manufacturer (parallel resonant crystal).

Figure 21. Equivalent Crystal Networks

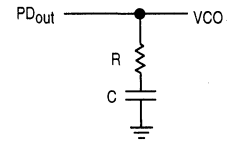
Table 4. Partial List of Crystal Manufacturers

Name	Address	Phone
United States Crystal Corp.	3605 McCart Ave., Ft. Worth, TX 76110	(817) 921–3013
Crystek Crystal	2351 Crystal Dr., Ft. Myers, FL 33907	(813) 936–2109
Statek Corp.	512 N. Main St., Orange, CA 92668	(714) 639–7810
Fox Electronics	5570 Enterprise Parkway, Ft. Myers, FL 33905	(813) 693–0099

NOTE: Motorola cannot recommend one supplier over another and in no way suggests that this is a complete listing of crystal manufacturers.

PHASE–LOCKED LOOP—LOW PASS FILTER DESIGN

(A)



$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NC}}$$

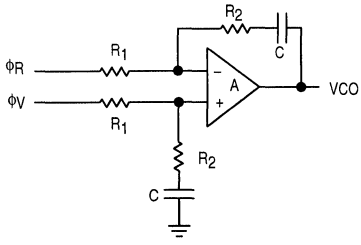
$$\zeta = \frac{R}{2}\sqrt{\frac{K_\phi K_{VCO} C}{N}} = \frac{\omega_n RC}{2}$$

$$Z(s) = \frac{1 + sRC}{sC}$$

2

NOTE:
For (A), using K_ϕ in amps per radian with the filter's impedance transfer function, Z(s), maintains units of volts per radian for the detector/filter combination. Additional sideband filtering can be accomplished by adding a capacitor C′ across R. The corner $\omega_C = 1/RC'$ should be chosen such that ω_n is not significantly affected.

(B)



$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NCR_1}}$$

$$\zeta = \frac{\omega_n R_2 C}{2}$$

ASSUMING GAIN A IS VERY LARGE, THEN:

$$F(s) = \frac{R_2 sC + 1}{R_1 sC}$$

NOTE:
For (B), R_1 is frequently split into two series resistors; each resistor is equal to R_1 divided by 2. A capacitor C_C is then placed from the midpoint to ground to further filter the error pulses. The value of C_C should be such that the corner frequency of this network does not significantly affect ω_n.

* The ϕ_R and ϕ_V outputs are fed to an external combiner/loop filter. The ϕ_R and ϕ_V outputs swing rail–to–rail. Therefore, the user should be careful not to exceed the common mode input range of the op amp used in the combiner/loop filter.

DEFINITIONS:
N = Total Division Ratio in Feedback Loop
K_ϕ (Phase Detector Gain) = $I_{PDout}/2\pi$ amps per radian for PD_{out}
K_ϕ (Phase Detector Gain) = $V_{PD}/2\pi$ volts per radian for ϕ_V and ϕ_R

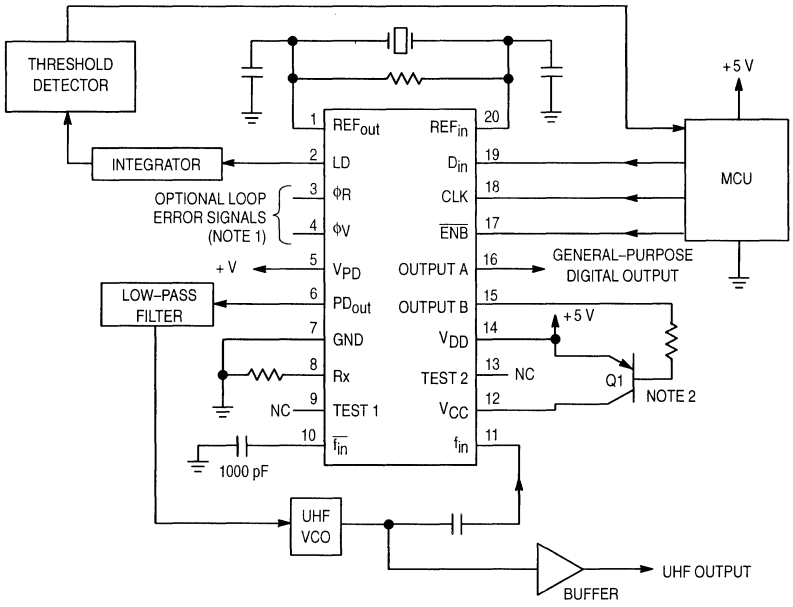
$$K_{VCO}\text{ (VCO Transfer Function)} = \frac{2\pi\Delta f_{VCO}}{\Delta V_{VCO}}\text{ radians per volt}$$

For a nominal design starting point, the user might consider a damping factor $\zeta \approx 0.7$ and a natural loop frequency $\omega_n \approx (2\pi f_R/50)$ where f_R is the frequency at the phase detector input. Larger ω_n values result in faster loop lock times and, for similar sideband filtering, higher f_R–related VCO sidebands.

Either loop filter (A) or (B) is frequently followed by additional sideband filtering to further attenuate f_R–related VCO sidebands. This additional filtering may be active or passive.

RECOMMENDED READING:

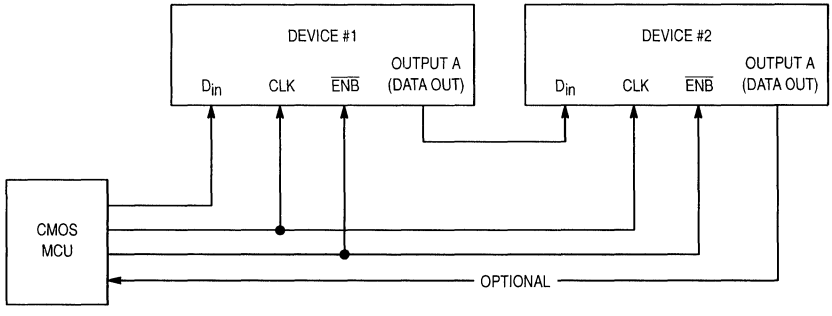
Gardner, Floyd M., *Phaselock Techniques (second edition).* New York, Wiley–Interscience, 1979.
Manassewitsch, Vadim, *Frequency Synthesizers: Theory and Design (second edition).* New York, Wiley–Interscience, 1980.
Blanchard, Alain, *Phase–Locked Loops: Application to Coherent Receiver Design.* New York, Wiley–Interscience, 1976.
Egan, William F., *Frequency Synthesis by Phase Lock.* New York, Wiley–Interscience, 1981.
Rohde, Ulrich L., *Digital PLL Frequency Synthesizers Theory and Design.* Englewood Cliffs, NJ, Prentice–Hall, 1983.
Berlin, Howard M., *Design of Phase–Locked Loop Circuits, with Experiments.* Indianapolis, Howard W. Sams and Co., 1978.
Kinley, Harold, *The PLL Synthesizer Cookbook.* Blue Ridge Summit, PA, Tab Books, 1980.
Seidman, Arthur H., *Integrated Circuits Applications Handbook*, Chapter 17, pp. 538–586. New York, John Wiley & Sons.
Fadrhons, Jan, "Design and Analyze PLLs on a Programmable Calculator," *EDN.* March 5, 1980.
AN535, Phase–Locked Loop Design Fundamentals, Motorola Semiconductor Products, Inc., 1970.
AR254, Phase–Locked Loop Design Articles, Motorola Semiconductor Products, Inc., Reprinted with permission from *Electronic Design,* 1987.
AN1253/D, An Improved PLL Design Method Without ω_n and ζ, Motorola Semiconductor Products, Inc., 1995.



NOTES:

1. When used, the ϕ_R and ϕ_V outputs are fed to an external combiner/loop filter. See the Phase–Locked Loop — Low–Pass Filter Design page for additional information.
2. Transistor Q1 is required only if the standby feature is needed. Q1 permits the bipolar section of the device to be shut down via use of the general–purpose digital pin, OUTPUT B. If the standby feature is not needed, tie Pin 12 directly to the power supply.
3. For optimum performance, bypass the V_{CC}, V_{DD}, and V_{PD} pins to GND with low–inductance capacitors.
4. The R counter is programmed for a divide value = REF_{in}/f_R. Typically, f_R is the tuning resolution required for the VCO. Also, the VCO frequency divided by $f_R = N_T = N \times 64 + A$; this determines the values (N, A) that must be programmed into the N and A counters, respectively.

Figure 22. Example Application



NOTE: See related Figures 24 through 26; these bit streams apply to the MC145190, MC145191, MC145200, and MC145201.

Figure 23. Cascading Two Devices

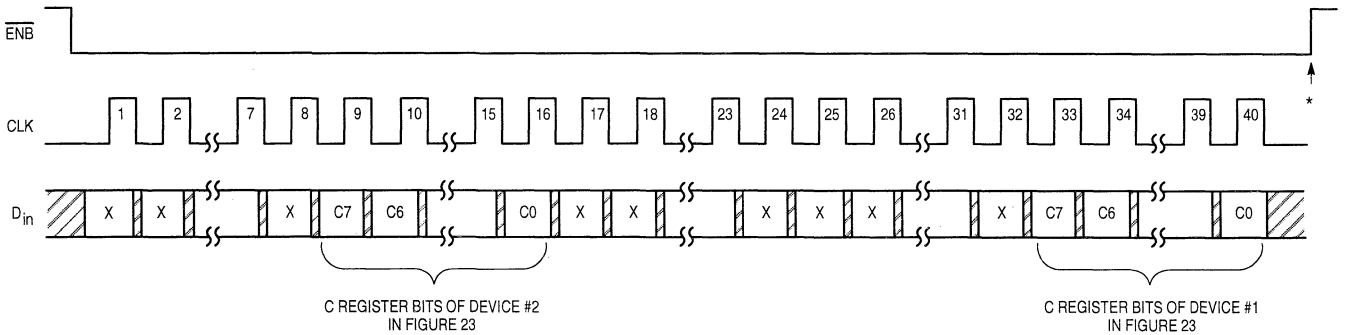


Figure 24. Accessing the C Registers of Two Cascaded Devices

*At this point, the new bytes are transferred to the C registers of both devices and stored. No other registers are affected.

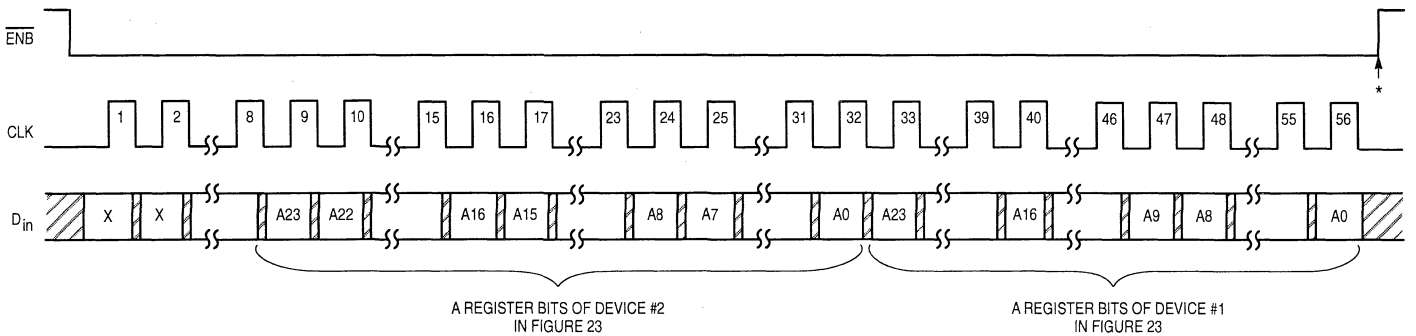


Figure 25. Accessing the A Registers of Two Cascaded Devices

*At this point, the new bytes are transferred to the A registers of both devices and stored. Additionally, for both devices, the 13 LSBs in each of the first buffers of the R registers are transferred to the respective R register's second buffer. Thus, the R, N, and A counters can be presented new divide ratios at the same time. The first buffer of each R register is not affected. Neither C register is affected.

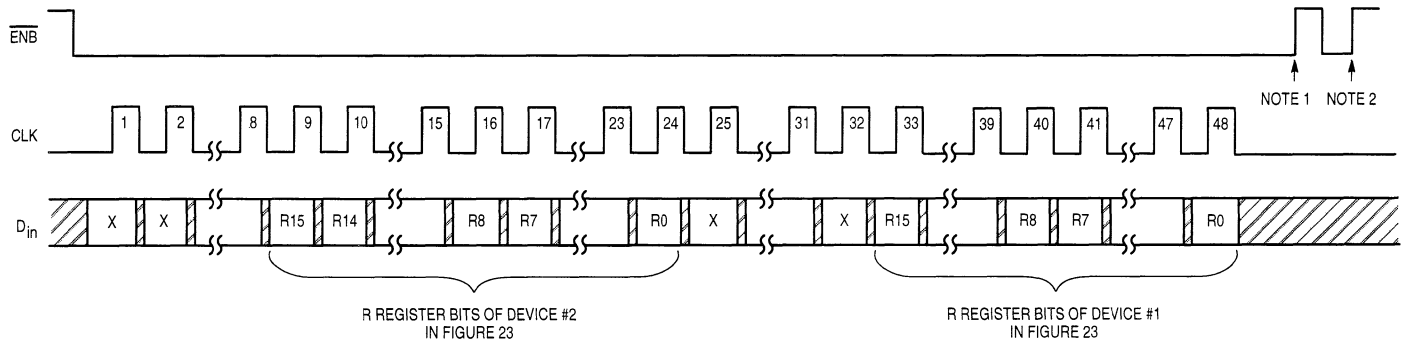


Figure 26. Accessing the R Registers of Two Cascaded Devices

NOTES APPLICABLE TO EACH DEVICE:

1. At this point, bits R13, R14, and R15 are stored and sent to the "OSC or 4-Stage Divider" block in the Block Diagram. Bits R0 through R12 are loaded into the first buffer in the double-buffered section of the R register. Therefore, the R counter divide ratio is not altered yet and retains the previous ratio loaded. The C and A registers are not affected.
2. At this point, the bits R0 through R12 are transferred to the second buffer of the R register. The R counter begins dividing by the new ratio after completing the rest of the present count cycle. CLK must be low during the $\overline{ENB}$ pulse, as shown. Also, see note of Figure 25 for an alternate method of loading the second buffer in the R register. The C and A registers are not affected. The first buffer of the R register is not affected.

MC145192

Low-Voltage 1.1 GHz PLL Frequency Synthesizer

Includes On–Board 64/65 Prescaler

2

The MC145192 is a low–voltage single–package synthesizer with serial interface capable of direct usage up to 1.1 GHz. A special architecture makes this PLL very easy to program because a byte–oriented format is utilized. Due to the patented BitGrabber™ registers, no address/steering bits are required for *random access* of the three registers. Thus, tuning can be accomplished via a 3–byte serial transfer to the 24–bit A register. The interface is both SPI and MICROWIRE™ compatible.

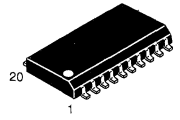
The device features a single–ended current source/sink phase detector A output and a double–ended phase detector B output. Both phase detectors have linear transfer functions (no dead zones). The maximum current of the single–ended phase detector output is determined by an external resistor tied from the Rx pin to ground. This current can be varied via the serial port.

The MC145192 phase/frequency detector B ϕ_R and ϕ_V outputs can be powered from 2.7 to 5.5 V. This is optimized for 3.0 V systems. The phase/frequency detector A PD_{out} output must be powered from 4.5 to 5.5 V, and is optimized for a 5 volt supply.

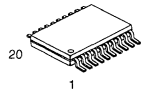
This part includes a differential RF input which may be operated in a single–ended mode. Also featured are on–board support of an external crystal and a programmable reference output. The R, A, and N counters are fully programmable. The C register (configuration register) allows the part to be configured to meet various applications. A patented feature allows the C register to shut off unused outputs, thereby minimizing system noise and interference.

In order to have consistent lock times and prevent erroneous data from being loaded into the counters, on–board circuitry synchronizes the update of the A register if the A or N counters are loading. Similarly, an update of the R register is synchronized if the R counter is loading.

The double–buffered R register allows new divide ratios to be presented to the three counters (R, A, and N) simultaneously.



F SUFFIX
SOG PACKAGE
CASE 751J

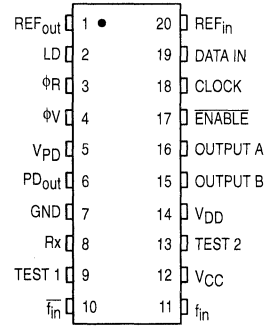


DT SUFFIX
TSSOP
CASE 948D

ORDERING INFORMATION

MC145192F	SOG Package
MC145192DT	TSSOP

PIN ASSIGNMENT



- Maximum Operating Frequency: 1100 MHz @ V_{in} = 200 mV p–p
- Operating Supply Current: 6 mA Nominal at 2.7 V
- Operating Supply Voltage Range (V_{DD} and V_{CC} Pins): 2.7 to 5.0 V
- Operating Supply Voltage Range of Phase Frequency Detector A (V_{PD} Pin) = 4.5 to 5.5 V
- Operating Supply Voltage Range of Phase Detector B (V_{PD} Pin) = 2.7 to 5.5 V
- Current Source/Sink Phase Detector Output Capability: 2 mA Maximum
- Gain of Current Source/Sink Phase/Frequency Detector Controllable via Serial Port
- Operating Temperature Range: – 40° to 85°C
- R Counter Division Range: (1 and) 5 to 8191
- N Counter Division Range: 5 to 4095
- A Counter Division Range: 0 to 63
- Dual–Modulus Capability Provides Total Division up to 262,143
- High–Speed Serial Interface: 2 Megabits per Second
- Output A Pin, When Configured as Data Out, Permits Cascading of Devices
- Two General–Purpose Digital Outputs — Output A: Totem–Pole (Push–Pull) with Four Output Modes
  Output B: Open–Drain
- Power–Saving Standby Feature with Patented Orderly Recovery for Minimizing Lock Times, Standby Current: 30 μA

BitGrabber is a trademark of Motorola Inc. MICROWIRE is a trademark of National Semiconductor Corp.

REV 2
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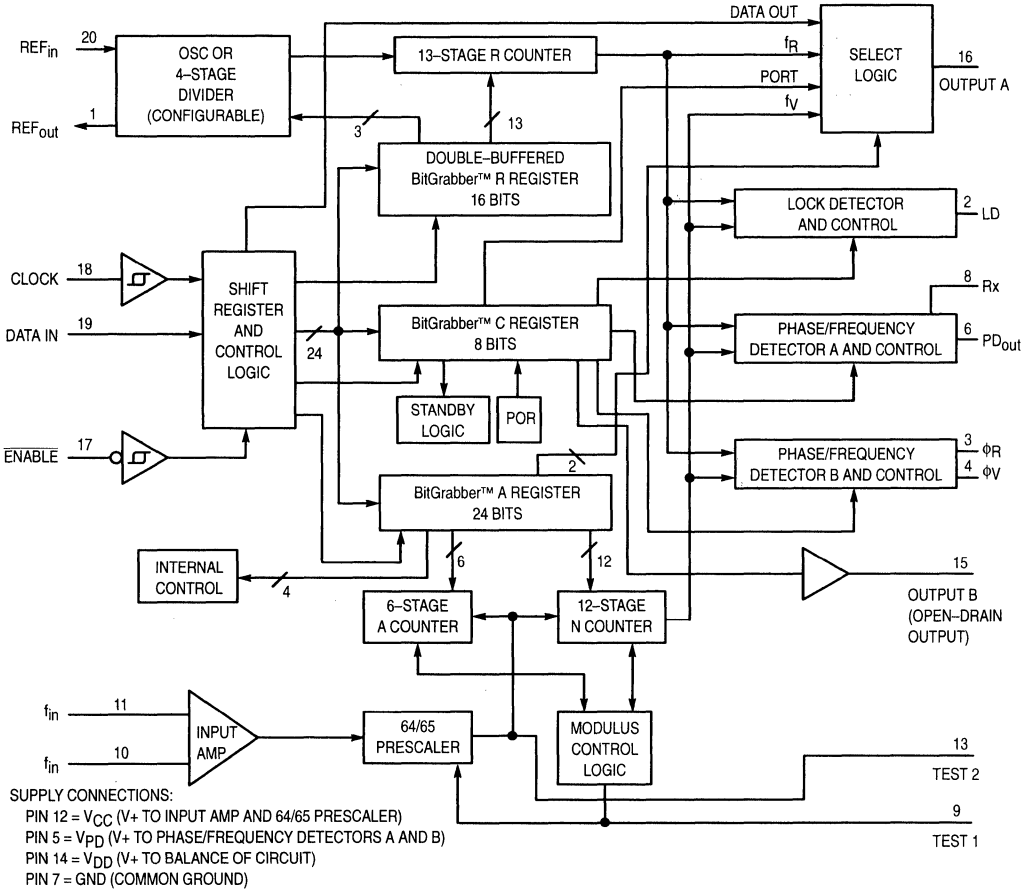
BLOCK DIAGRAM



MAXIMUM RATINGS* (Voltages Referenced to GND, unless otherwise stated)

Symbol	Parameter	Value	Unit
V_{CC}, V_{DD}	DC Supply Voltage (Pins 12 and 14)	– 0.5 to + 6.0	V
V_{PD}	DC Supply Voltage (Pin 5)	V_{DD} – 0.5 to + 6.0	V
V_{in}	DC Input Voltage	– 0.5 to V_{DD} + 0.5	V
V_{out}	DC Output Voltage, except Output B, PD_{out}, ϕR, ϕV Output B, PD_{out}, ϕR, ϕV	 – 0.5 to V_{DD} + 0.5 – 0.5 to V_{PD} + 0.5	V
I_{in}, I_{PD}	DC Input Current, per Pin (Includes V_{PD})	± 10	mA
I_{out}	DC Output Current, per Pin	± 20	mA
I_{DD}	DC Supply Current, V_{DD} and GND Pins	± 30	mA
P_D	Power Dissipation, per Package	300	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds	260	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Descriptions section.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit.

ELECTRICAL CHARACTERISTICS (V_{DD} = V_{CC} = 2.7 to 5.0 V, Voltages Referenced to GND, T_A = – 40° to 85°C, unless otherwise stated; Phase/Frequency Detector A V_{PD} = 4.5 to 5.5 V with $V_{DD} \leq V_{PD}$; Phase/Frequency Detector B V_{PD} = 2.7 to 5.5 V with $V_{DD} \leq V_{PD}$)

Symbol	Parameter	Test Condition	Guaranteed Limit	Unit
V_{IL}	Maximum Low–Level Input Voltage (Data In, Clock, $\overline{\text{Enable}}$, REF_{in})	Device in Reference Mode, DC Coupled	0.2 x V_{DD}	V
V_{IH}	Minimum High–Level Input Voltage (Data In, Clock, $\overline{\text{Enable}}$, REF_{in})	Device in Reference Mode, DC Coupled	0.8 x V_{DD}	V
V_{Hys}	Minimum Hysteresis Voltage (Clock, $\overline{\text{Enable}}$)	V_{DD} = 2.7 V V_{DD} = 5.0 V	100 300	mV
V_{OL}	Maximum Low–Level Output Voltage (REF_{out}, Output A)	I_{out} = 20 µA, Device in Reference Mode	0.1	V
V_{OH}	Minimum High–Level Output Voltage (REF_{out}, Output A)	I_{out} = – 20 µA, Device in Reference Mode	V_{DD} – 0.1	V
I_{OL}	Minimum Low–Level Output Current (REF_{out}, LD)	V_{out} = 0.4 V	0.25	mA
I_{OL}	Minimum Low–Level Output Current (ϕ_R, ϕ_V)	V_{out} = 0.4 V V_{DD}, V_{PD} = 2.7 V	0.36	mA
I_{OL}	Minimum Low–Level Output Current (Output A)	V_{out} = 0.4 V	0.6	mA
I_{OL}	Minimum Low–Level Output Current (Output B)	V_{out} = 0.4 V	1.0	mA
I_{OH}	Minimum High–Level Output Current (REF_{out}, LD)	V_{out} = V_{DD} – 0.4 V	– 0.25	mA
I_{OH}	Minimum High–Level Output Current (ϕ_R, ϕ_V)	V_{out} = V_{PD} – 0.4 V V_{DD}, V_{PD} = 2.7 V	– 0.36	mA
I_{OH}	Minimum High–Level Output Current (Output A Only)	V_{out} = V_{DD} – 0.4 V	– 0.35	mA
I_{in}	Maximum Input Leakage Current (Data In, Clock, $\overline{\text{Enable}}$, REF_{in})	V_{in} = V_{DD} or GND, Device in XTAL Mode	± 1.0	µA
I_{in}	Maximum Input Current (REF_{in})	V_{in} = V_{DD} or GND, Device in Reference Mode	± 150	µA
I_{OZ}	Maximum Output Leakage Current (PD_{out})	V_{out} = V_{PD} – 0.5 V or 0.5 V, Output in High–Impedance State	± 200	nA
	(Output B)	Output in High–Impedance State	± 10	µA
I_{STBY}	Maximum Standby Supply Current (V_{DD} + V_{PD} Pins)	V_{in} = V_{DD} or GND; Outputs Open; Device in Standby Mode, Shut–Down Crystal Mode or REF_{out}–Static–Low Reference Mode; Output B Controlling V_{CC} per Figure 21	30	µA
I_{PD}	Maximum Phase Detector Quiescent Current (V_{PD} Pin)	Bit C6 = High Which Selects Phase Detector A, PD_{out} = Open, PD_{out} = Static Low or High, Bit C4 = Low Which is NOT Standby, I_{Rx} = 113 µA, V_{PD} = 5.5 V	600	µA
		Bit C6 = Low Which Selects Phase Detector B, ϕ_R and ϕ_V = Open, ϕ_R and ϕ_V = Static Low or High, Bit C4 = Low Which is NOT Standby	30	
I_T	Total Operating Supply Current (V_{DD} + V_{PD} + V_{CC} Pins)	f_{in} = 1.1 GHz; REF_{in} = 13 MHz @ 1 V p–p; Output A = Inactive and No Connect; V_{DD} = V_{CC}, REF_{out}, ϕ_V, ϕ_R, PD_{out}, LD = No Connect; Data In, $\overline{\text{Enable}}$, Clock = V_{DD} or GND, Phase Detector A Off	*	mA

* The nominal values are:
6 mA at V_{DD} = 2.7 V and V_{PD} = 2.7 V
9 mA at V_{DD} = 5.0 V and V_{PD} = 5.5 V
These are not guaranteed limits.

ANALOG CHARACTERISTICS — CURRENT SOURCE/SINK OUTPUT — PD_{out}

($I_{out} \leq 2$ mA, $V_{DD} = V_{CC} = 2.7$ to 5.0 V, Voltages Referenced to GND, $V_{DD} = V_{CC} \leq V_{PD}$)

Parameter	Test Condition	V_{PD}	Guaranteed Limit	Unit
Maximum Source Current Variation Part–to–Part	$V_{out} = 0.5 \times V_{PD}$	4.5	± 20	%
		5.5	± 20	
Maximum Sink–versus–Source Mismatch	$V_{out} = 0.5 \times V_{PD}$	4.5	12	%
(Note 3)		5.5	12	
Output Voltage Range	I_{out} variation ≤ 20%	4.5	0.5 to 4.0	V
(Note 3)		5.5	0.5 to 5.0	

NOTES:
1. Percentages calculated using the following formula: (Maximum Value – Minimum Value)/Maximum Value.
2. See Rx Pin Description for external resistor values.
3. This parameter is guaranteed for a given temperature within – 40° to 85°C.

AC INTERFACE CHARACTERISTICS

($V_{DD} = V_{CC} = 2.7$ to 5.0 V, $T_A = -40°$ to 85°C, $C_L = 50$ pF, Input $t_r = t_f = 10$ ns, $V_{PD} = 2.7$ to 5.5 V with $V_{DD} \leq V_{PD}$)

Symbol	Parameter	Guaranteed Limit	Unit
f_{clk}	Serial Data Clock Frequency (Figure 1) NOTE: Refer to Clock t_w below	dc to 2.0	MHz
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Clock to Output A (Selected as Data Out) (Figures 1 and 5)	200	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay, $\overline{\text{Enable}}$ to Output A (Selected as Port) (Figures 2 and 5)	200	ns
t_{PZL}, t_{PLZ}	Maximum Propagation Delay, $\overline{\text{Enable}}$ to Output B (Figures 2 and 6)	200	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Output A and Output B; t_{THL} only, on Output B (Figures 1, 5, and 6)	200	ns
C_{in}	Maximum Input Capacitance — Data In, Clock, $\overline{\text{Enable}}$	10	pF

TIMING REQUIREMENTS ($V_{DD} = V_{CC} = 2.7$ to 5.0 V, $T_A = -40°$ to 85°C, Input $t_r = t_f = 10$ ns unless otherwise indicated)

Symbol	Parameter	Guaranteed Limit	Unit
t_{su}, t_h	Minimum Setup and Hold Times, Data In versus Clock (Figure 3)	50	ns
t_{su}, t_h, t_{rec}	Minimum Setup, Hold and Recovery Times, $\overline{\text{Enable}}$ versus Clock (Figure 4)	100	ns
t_w	Minimum Pulse Width, $\overline{\text{Enable}}$ (Figure 4)	*	cycles
t_w	Minimum Pulse Width, Clock (Figure 1)	250	ns
t_r, t_f	Maximum Input Rise and Fall Times, Clock (Figure 1)	100	µs

* The minimum limit is 3 REF_{in} cycles or 195 f_{in} cycles, whichever is greater.

SWITCHING WAVEFORMS

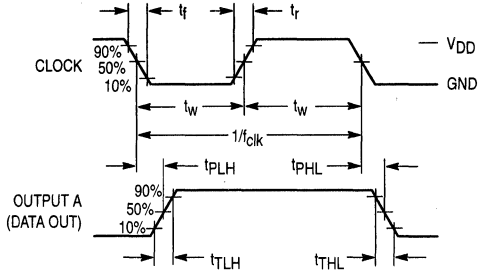


Figure 1.

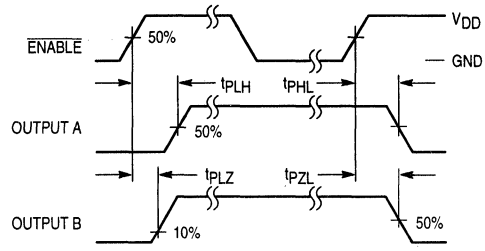


Figure 2.

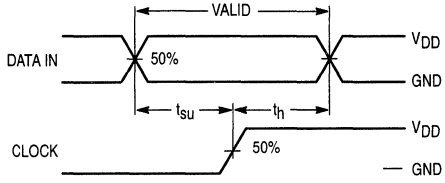


Figure 3.

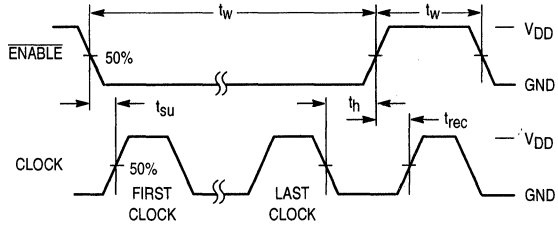
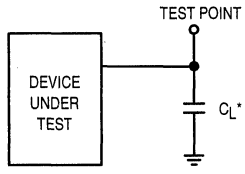
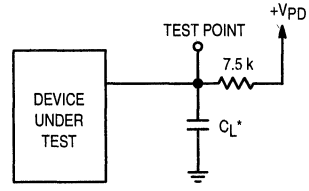


Figure 4.



* Includes all probe and fixture capacitance.

Figure 5. Test Circuit



* Includes all probe and fixture capacitance.

Figure 6. Test Circuit

LOOP SPECIFICATIONS (V_{DD} = V_{CC} = 2.7 to 5.0 V unless otherwise indicated, T_A = – 40° to 85°C)

Symbol	Parameter	Test Condition	Guaranteed Operating Range		Unit
			Min	Max	
V_{in}	Input Voltage Range, f_{in} (Figure 7)	100 MHz ≤ f_{in} < 250 MHz 250 MHz ≤ f_{in} ≤ 1100 MHz	400 200	1500 1500	mV p–p
f_{ref}	Input Frequency, REF_{in} Externally Driven in Reference Mode (Figure 8)	V_{in} = 400 mV p–p V_{DD} = 2.7 V V_{DD} = 3.0 V V_{DD} = 3.5 V V_{DD} = 4.5 to 5 V	 1 4.5 5.5 12	 20 20 20 27	MHz
		V_{in} = 1 V p–p V_{DD} = 2.7 V V_{DD} = 3.0 V V_{DD} = 3.5 V V_{DD} = 4.5 to 5 V	 1 1.5 2 4.5	 20 20 20 27	MHz
f_{XTAL}	Crystal Frequency, Crystal Mode (Figure 9)	C1 ≤ 30 pF, C2 ≤ 30 pF, Includes Stray Capacitance	2	10	MHz
f_{out}	Output Frequency, REF_{out} (Figures 10 and 12)	C_L = 30 pF	dc	5	MHz
f	Operating Frequency of the Phase Detectors		dc	1	MHz
t_w	Output Pulse Width, ϕ_R, ϕ_V, and LD (Figures 11 and 12)	f_R in Phase with f_V, C_L = 50 pF, V_{PD} = 2.7 V, V_{DD} = V_{CC} = 2.7 V	20	140	ns
t_{TLH}, t_{THL}	Output Transition Times, LD, ϕ_V, and ϕ_R (Figures 11 and 12)	C_L = 50 pF, V_{PD} = 2.7 V, V_{DD} = V_{CC} = 2.7 V	—	80	ns
C_{in}	Input Capacitance, REF_{in}		—	5	pF

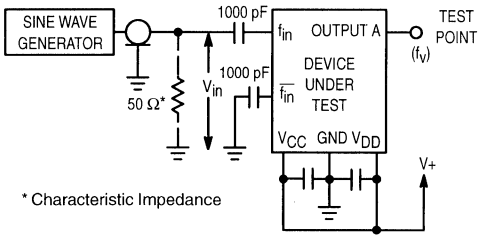


Figure 7. Test Circuit

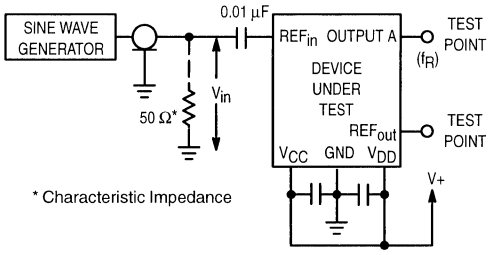


Figure 8. Test Circuit–Reference Mode

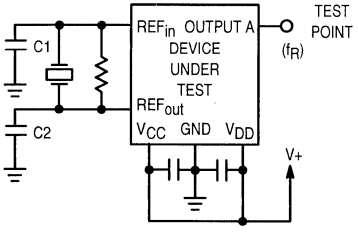


Figure 9. Test Circuit–Crystal Mode

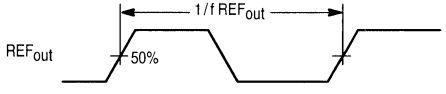


Figure 10. Switching Waveform

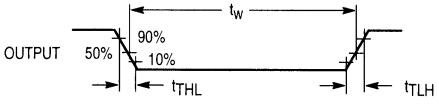


Figure 11. Switching Waveform

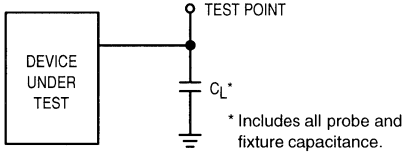
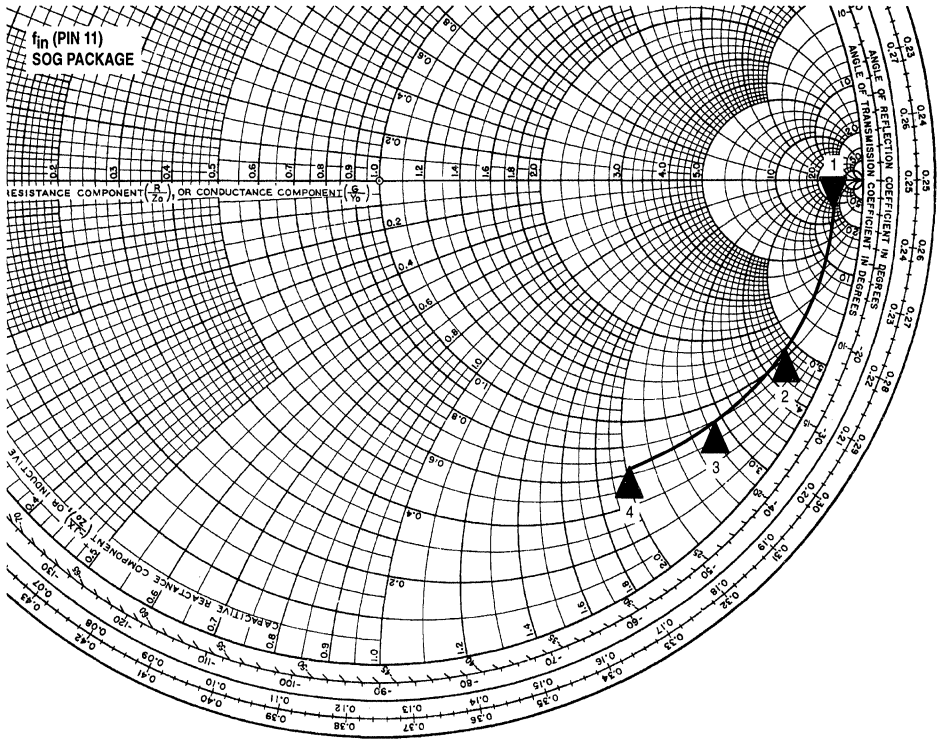


Figure 12. Test Circuit



Marker	Frequency (MHz)	Resistance (Ω)	Capacitive Reactance (Ω)	Capacitance (pF)
1	100	574	– 881	1.81
2	500	57.9	– 242	1.31
3	800	38.3	– 148	1.34
4	1100	31.6	– 103	1.40

Figure 13. Normalized Input Impedance at f_{in} — Series Format (R + jX) (100 MHz to 1100 MHz)

PIN DESCRIPTIONS

DIGITAL INTERFACE PINS

Data In (Pin 19)

Serial Data Input. The bit stream begins with the MSB and is shifted in on the low–to–high transition of Clock. The bit pattern is 1 byte (8 bits) long to access the C or configuration register, 2 bytes (16 bits) to access the first buffer of the R register, or 3 bytes (24 bits) to access the A register (see Table 1). The values in the C, R, and A registers do not change during shifting because the transfer of data to the registers is controlled by $\overline{\text{Enable}}$.

CAUTION

The value programmed for the N–counter must be greater than or equal to the value of the A–counter.

The 13 LSBs of the R register are double–buffered. As indicated above, data is latched into the first buffer on a 16–bit transfer. (The 3 MSBs are not double–buffered and have an immediate effect after a 16–bit transfer.) The second buffer of the R register contains the 13 bits for the R counter. This second buffer is loaded with the contents of the first buffer when the A register is loaded (a 24–bit transfer). This allows presenting new values to the R, A, and N counters simultaneously. If this is not required, then the 16–bit transfer may be followed by pulsing $\overline{\text{Enable}}$ low with no signal on the Clock pin. This is an alternate method of transferring data to the second buffer of the R register. See Figure 16.

The bit stream needs neither address nor steering bits due to the innovative BitGrabber registers. Therefore, all bits in the stream are available to be data for the three registers. Random access of any register is provided. That is, the registers may be accessed in any sequence. Data is retained in the registers over a supply range of 2.7 to 5.0 V. The formats are shown in Figures 14, 15, and 16.

Data In typically switches near 50% of V_{DD} to maximize noise immunity. This input can be directly interfaced to CMOS devices with outputs guaranteed to switch near rail–to–rail. When interfacing to NMOS or TTL devices, either a level shifter (MC74HC14A, MC14504B) or pull–up resistor of 1 kΩ to 10 kΩ must be used. Parameters to consider when sizing the resistor are worst–case I_{OL} of the driving device, maximum tolerable power consumption, and maximum data rate.

Table 1. Register Access

(MSBs are shifted in first, C0, R0, and A0 are the LSBs)

Number of Clocks	Accessed Register	Bit Nomenclature
8	C Register	C7, C6, C5, . . ., C0
16	R Register	R15, R14, R13, . . ., R0
24	A Register	A23, A22, A21, . . ., A0
Other Values ≤ 32	Not Allowed	
Values > 32	See Figures 23 to 26	

Clock (Pin 18)

Serial Data Clock Input. Low–to–high transitions on Clock shift bits available at the Data pin, while high–to–low transitions shift bits from Output A (when configured as Data Out, see Pin 16). The 24–1/2–stage shift register is static, allowing clock rates down to dc in a continuous or intermittent mode.

Eight clock cycles are required to access the C register. Sixteen clock cycles are needed for the first buffer of the R register. Twenty–four cycles are used to access the A register. See Table 1 and Figures 14, 15, and 16. The number of clocks required for cascaded devices is shown in Figures 24 through 26.

Clock typically switches near 50% of V_{DD} and has a Schmitt–triggered input buffer. Slow Clock rise and fall times are allowed. See the last paragraph of **Data In** for more information.

NOTE

To guarantee proper operation of the power–on reset (POR) circuit, the Clock pin must be held at GND (with $\overline{\text{Enable}}$ being a don't care) or $\overline{\text{Enable}}$ must be held at the potential of the V+ pin (with Clock being a don't care) during power–up. As an alternative, the bit sequence of Figure 17 may be used.

$\overline{\text{Enable}}$ (Pin 17)

Active–Low Enable Input. This pin is used to activate the serial interface to allow the transfer of data to/from the device. When $\overline{\text{Enable}}$ is in an inactive high state, shifting is inhibited and the port is held in the initialized state. To transfer data to the device, $\overline{\text{Enable}}$ (which must start inactive high) is taken low, a serial transfer is made via Data In and Clock, and $\overline{\text{Enable}}$ is taken back high. The low–to–high transition on $\overline{\text{Enable}}$ transfers data to the C or A registers and first buffer of the R register, depending on the data stream length per Table 1.

NOTE

Transitions on $\overline{\text{Enable}}$ must not be attempted while Clock is high. This will put the device out of synchronization with the microcontroller. Resynchronization occurs when $\overline{\text{Enable}}$ is high and Clock is low.

This input is also Schmitt–triggered and switches near 50% of V_{DD}, thereby minimizing the chance of loading erroneous data into the registers. See the last paragraph of **Data In** for more information.

For POR information, see the note for the **Clock pin**.

Output A (Pin 16)

Configurable Digital Output. Output A is selectable as f_R, f_V, Data Out, or Port. Bits A22 and A23 in the A register control the selection; see Figure 15.

If A23 = A22 = high, Output A is configured as f_R. This signal is the buffered output of the 13–stage R counter. The f_R signal appears as normally low and pulses high. The f_R signal can be used to verify the divide ratio of the R counter. This ratio extends from 5 to 8191 and is determined by the binary value loaded into bits R0 through R12 in the R register. Also, direct access to the phase detectors via the REF_{in} pin is allowed by choosing a divide value of one. See Figure 16. The maximum frequency at which the phase detectors operate is 1 MHz. Therefore, the frequency of f_R should not exceed 1 MHz.

If A23 = high and A22 = low, Output A is configured as f_V. This signal is the buffered output of the 12–stage N counter.

The f_V signal appears as normally low and pulses high. The f_V signal can be used to verify the operation of the prescaler, A counter, and N counter. The divide ratio between the f_{in} input and the f_V signal is $N \times 64 + A$. N is the divide ratio of the N counter and A is the divide ratio of the A counter. These ratios are determined by bits loaded into the A register. See Figure 15. The maximum frequency at which the phase detectors operate is 1 MHz. Therefore, the frequency of f_V should not exceed 1 MHz.

If A23 = low and A22 = high, Output A is configured as Data Out. This signal is the serial output of the 24–1/2–stage shift register. The bit stream is shifted out on the high–to–low transition of the Clock input. Upon power up, Output A is automatically configured as Data Out to facilitate cascading devices.

If A23 = A22 = low, Output A is configured as Port. This signal is a general–purpose digital output which may be used as an MCU port expander. This signal is low when the Port bit (C1) of the C register is low, and high when the Port bit is high.

Output B (Pin 15)

Open–Drain Digital Output. This signal is a general–purpose digital output which may be used as an MCU port expander. This signal is low when the Out B bit (C0) of the C register is low. When the Out B bit is high, Output B assumes the high–impedance state. Output B may be pulled up through an external resistor or active circuitry to any voltage less than or equal to the potential of the V_{PD} pin. Note: the maximum voltage allowed on the V_{PD} pin is 5.5 V for the MC145192.

Upon power–up, power–on reset circuitry forces Output B to a low level.

REFERENCE PINS

REF_{in} and REF_{out} (Pins 20 and 1)

Configurable Pins for a Crystal or an External Reference. This pair of pins can be configured in one of two modes: the crystal mode or the reference mode. Bits R13, R14, and R15 in the R register control the modes as shown in Figure 16.

In crystal mode, these pins form a reference oscillator when connected to terminals of an external parallel–resonant crystal. Frequency–setting capacitors of appropriate values as recommended by the crystal supplier are connected from each of the two pins to ground (up to a maximum of 30 pF each, including stray capacitance). An external resistor of 1 MΩ to 15 MΩ is connected directly across the pins to ensure linear operation of the amplifier. The device is designed to operate with crystals up to 10 MHz; the required connections are shown in Figure 9. To turn on the oscillator, bits R15, R14, and R13 must have an octal value of one (001 in binary). This is the active–crystal mode shown in Figure 16. In this mode, the crystal oscillator runs and the R Counter divides the crystal frequency, unless the part is in standby. If the part is placed in standby via the C register, the oscillator runs, but the R counter is stopped. However, if bits R15 to R13 have a value of 0, the oscillator is stopped, which saves additional power. This is the shut–down crystal mode shown in Figure 16, and can be engaged whether in standby or not.

In the reference mode, REF_{in} (Pin 20) accepts a signal up to 20 MHz from an external reference oscillator, such as a TCXO. A signal swinging from at least the V_{IL} to V_{IH} levels listed in the Electrical Characteristics table may be directly coupled to the pin. If the signal is less than this level, ac coupling must be used as shown in Figure 8. The ac–coupled signal must be at least 400 mV p–p. Due to an on–board resistor which is engaged in the reference modes, an external biasing resistor tied between REF_{in} and REF_{out} is not required.

With the reference mode, the REF_{out} pin is configured as the output of a divider. As an example, if bits R15, R14, and R13 have an octal value of seven, the frequency at REF_{out} is the REF_{in} frequency divided by 16. In addition, Figure 16 shows how to obtain ratios of eight, four, and two. A ratio of one–to–one can be obtained with an octal value of three. Upon power up, a ratio of eight is automatically initialized. The maximum frequency capability of the REF_{out} pin is 5 MHz for V_{DD} to V_{SS} swing. Therefore, for REF_{in} frequencies above 5 MHz, the one–to–one ratio may not be used for large signal swing requirements. Likewise, for REF_{in} frequencies above 10 MHz, the ratio must be more than two.

If REF_{out} is unused, an octal value of two should be used for R15, R14, and R13 and the REF_{out} pin should be floated. A value of two allows REF_{in} to be functional while disabling REF_{out}, which minimizes dynamic power consumption and electromagnetic interference (EMI).

LOOP PINS

f_{in} and $\overline{f_{in}}$ (Pins 11 and 10)

Frequency Input from the VCO. These pins feed the on–board RF amplifier which drives the 64/65 prescaler. These inputs may be fed differentially. However, they are usually used in a single–ended configuration as shown in Figure 7. Note that f_{in} is driven while $\overline{f_{in}}$ must be tied to ground via a capacitor.

Motorola does not recommend driving $\overline{f_{in}}$ while terminating f_{in} because this configuration is not tested for sensitivity. The sensitivity is dependent on the frequency as shown in the Loop Specifications table.

PD_{out} (Pin 6)

Single–Ended Phase/Frequency Detector Output. This is a 3–state current–source/sink output for use as a loop error signal when combined with an external low–pass filter. The phase/frequency detector is characterized by a linear transfer function. The operation of the phase/frequency detector is described below and is shown in Figure 18.

POL bit (C7) in the C register = low (see Figure 14)
Frequency of $f_V > f_R$ or Phase of f_V Leading f_R: current–sinking pulses from a floating state
Frequency of $f_V < f_R$ or Phase of f_V Lagging f_R: current–sourcing pulses from a floating state
Frequency and Phase of $f_V = f_R$: essentially a floating state; voltage at pin determined by loop filter

POL bit (C7) = high
Frequency of $f_V > f_R$ or Phase of f_V Leading f_R: current–sourcing pulses from a floating state
Frequency of $f_V < f_R$ or Phase of f_V Lagging f_R: current–sinking pulses from a floating state
Frequency and Phase of $f_V = f_R$: essentially a floating state; voltage at pin determined by loop filter

This output can be enabled, disabled, and inverted via the C register. If desired, PD_{out} can be forced to the floating state by utilization of the disable feature in the C register (bit C6). This is a patented feature. Similarly, PD_{out} is forced to the floating state when the device is put into standby (STBY bit C4 = high).

The PD_{out} circuit is powered by V_{PD}. The phase detector gain is controllable by bits C3, C2, and C1: gain (in amps per radian) = PD_{out} current divided by 2π.

ϕ_R and ϕ_V (Pins 3 and 4)

Double–Ended Phase/Frequency Detector Outputs. These outputs can be combined externally to generate a loop error signal. Through use of a Motorola patented technique, the detector's dead zone has been eliminated. Therefore, the phase/frequency detector is characterized by a linear transfer function. The operation of the phase/frequency detector is described below and is shown in Figure 18.

POL bit (C7) in the C register = low (see Figure 14)
Frequency of $f_V > f_R$ or Phase of f_V Leading f_R: ϕ_V = negative pulses, ϕ_R = essentially high
Frequency of $f_V < f_R$ or Phase of f_V Lagging f_R: ϕ_V = essentially high, ϕ_R = negative pulses
Frequency and Phase of $f_V = f_R$: ϕ_V and ϕ_R remain essentially high, except for a small minimum time period when both pulse low in phase

POL bit (C7) = high
Frequency of $f_V > f_R$ or Phase of f_V Leading f_R: ϕ_R = negative pulses, ϕ_V = essentially high
Frequency of $f_V < f_R$ or Phase of f_V Lagging f_R: ϕ_R = essentially high, ϕ_V = negative pulses
Frequency and Phase of $f_V = f_R$: ϕ_V and ϕ_R remain essentially high, except for a small minimum time period when both pulse low in phase

These outputs can be enabled, disabled, and interchanged via C register bits C6 or C4. This is a patented feature. Note that when disabled or in standby, ϕ_R and ϕ_V are forced to their rest condition (high state).

The ϕ_R and ϕ_V output signal swing is approximately from GND to V_{PD}.

LD (Pin 2)

Lock Detector Output. This output is essentially at a high level with narrow low–going pulses when the loop is locked (f_R and f_V of the same phase and frequency). The output pulses low when f_V and f_R are out of phase or different frequencies. LD is the logical ANDing of ϕ_R and ϕ_V. See Figure 18.

This output can be enabled and disabled via the C register. This is a patented feature. Upon power up, on–chip initialization circuitry disables LD to a static low logic level to prevent a false lock signal. If unused, LD should be disabled and left open.

The LD output signal swing is approximately from GND to V_{DD}.

Rx (Pin 8)

External Resistor. A resistor tied between this pin and GND, in conjunction with bits in the C register, determines the amount of current that the PD_{out} pin sinks and sources. When bits C2 and C3 are both set high, the maximum current is obtained at PD_{out}; see Figure 14 for other values of current. To achieve a maximum current of 2 mA, the resistor should be about 22 kΩ when V_{PD} is 5 V.

When the ϕ_R and ϕ_V outputs are used, the Rx pin may be floated.

TEST POINT PINS

Test 1 (Pin 9)

Modulus Control Signal. This pin may be used in conjunction with the Test 2 pin for access to the on–board 64/65 prescaler. When Test 1 is low, the prescaler divides by 65. When high, the prescaler divides by 64.

CAUTION

This pin is an unbuffered output and must be floated in an actual application. This pin may be attached to an isolated pad with no trace. There is the possibility that the device may be modified and have this lead clipped at the body of the package.

Test 2 (Pin 13)

Prescaler Output. This pin may be used to access to the on–board 64/65 prescaler output.

CAUTION

This pin is an unbuffered output and must be floated in an actual application. This pin may be attached to an isolated pad with no trace. There is the possibility that the device may be modified and have this lead clipped at the body of the package.

POWER SUPPLY PINS

V_{DD} (Pin 14)

Positive Supply Potential. This pin supplies power to the main CMOS digital portion of the device. The voltage range is + 2.7 to + 5.0 V with respect to the GND pin.

For optimum performance, V_{DD} should be bypassed to GND using a low–inductance capacitor mounted very close to these pins. Lead lengths on the capacitor should be minimized.

V_{CC} (Pin 12)

Positive Supply Potential. This pin supplies power to the RF amp and 64/65 prescaler. The voltage range is + 2.7 to + 5.0 V with respect to the GND pin. In the standby mode, the V_{CC} pin still draws a few milliamps from the power supply. This current drain can be eliminated with the use of transistor Q1 as shown in Figure 22.

For optimum performance, V_{CC} should be bypassed to GND using a low–inductance capacitor mounted very close to these pins. Lead lengths on the capacitor should be minimized.

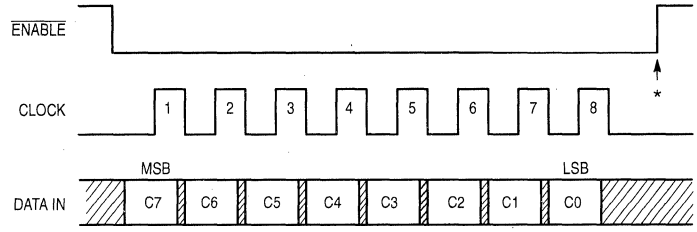
V_{PD} (Pin 5)

Positive Supply Potential. This pin supplies power to both phase/frequency detectors A and B. The voltage applied on this pin must be no less than the potential applied to the V_{DD} pin. The voltage range for V_{PD} is 4.5 to 5.5 V with respect to the GND pin when using PD_{OUT} and 2.7 to 5.5 V when using ϕ_R, ϕ_V outputs.

For optimum performance, V_{PD} should be bypassed to GND using a low–inductance capacitor mounted very close to these pins. Lead lengths on the capacitor should be minimized.

GND (Pin 7)

Common ground.



* At this point, the new byte is transferred to the C register and stored. No other registers are affected.

C7 – POL: Selects the output polarity of the phase/frequency detectors. When set high, this bit inverts PD_{out} and interchanges the ϕ_R function with ϕ_V as depicted in Figure 18. Also see the phase detector output pin descriptions for more information. This bit is cleared low at power up.

C6 – PDA/B: Selects which phase/frequency detector is to be used. When set high, enables the output of phase/frequency detector A (PD_{out}) and disables phase/frequency detector B by forcing ϕ_R and ϕ_V to the static high state. When cleared low, phase/frequency detector B is enabled (ϕ_R and ϕ_V) and phase/frequency detector A is disabled with PD_{out} forced to the high–impedance state. This bit is cleared low at power up.

C5 – LDE: Enables the lock detector output when set high. When the bit is cleared low, the LD output is forced to a static low level. This bit is cleared low at power up.

C4 – STBY: When set high, places the CMOS section of device, which is powered by the V_{DD} and V_{PD} pins, in the standby mode for reduced power consumption: PD_{out} is forced to the high–impedance state, ϕ_R and ϕ_V are forced high, the A, N, and R counters are inhibited from counting, and the Rx current is shut off. In standby, the state of LD is determined by bit C5. C5 low forces LD low (no change). C5 high forces LD static high. During standby, data is retained in the A, R, and C registers. The condition of REF/OSC circuitry is determined by the control bits in the R register: R13, R14, and R15. However, if REF_{out} = static low is selected, the internal feedback resistor is disconnected and the input is inhibited when in standby; in addition, the REF_{in} input only presents a capacitive load. NOTE: Standby does not affect the other modes of the REF/OSC circuitry.
When C4 is reset low, the part is taken out of standby in 2 steps. First, the REF_{in} (only in one mode) resistor is reconnected, all counters are enabled, and the Rx current is enabled. Any f_R and f_V signals are inhibited from toggling the phase/frequency detectors and lock detector. Second, when the first f_V pulse occurs, the R counter is jam loaded, and the phase/frequency and lock detectors are initialized. Immediately after the jam load, the A, N, and R counters begin counting down together. At this point, the f_R and f_V pulses are enabled to the phase and lock detectors. This is a patented feature.

C3, C2 – I2, I1: Controls the PD_{out} source/sink current per Tables 2 and 3. With both bits high, the maximum current (as set by Rx) is available. Also, see C1 bit description.

C1 – Port: When the Output A pin is selected as "Port" via bits A22 and A23, C1 determines the state of Output A. When C1 is set high, Output A is forced high; C1 low forces Output A low. When Output A is not selected as "Port," C1 controls whether the PD_{out} step size is 10% or 25%. (See Tables 2 and 3.) When low, steps are 10%. When high, steps are 25%. Default is 10% steps when Output A is selected as "Port." The Port bit is not affected by the standby mode.

C0 – Out B: Determines the state of Output B. When C0 is set high, Output B is high–impedance; C0 low forces Output B low. The Out B bit is not affected by the standby mode. This bit is cleared low at power up.

Figure 14. C Register Access and Format (8 Clock Cycles Are Used)

Table 2. PD_{out} Current, C1 = Low with Output A NOT Selected as "Port"; Also, Default Mode When Output A Selected as "Port"

C3	C2	PD_{out} Current
0	0	70%
0	1	80%
1	0	90%
1	1	100%

Table 3. PD_{out} Current, C1 = High with Output A NOT Selected as "Port"

C3	C2	PD_{out} Current
0	0	25%
0	1	50%
1	0	75%
1	1	100%

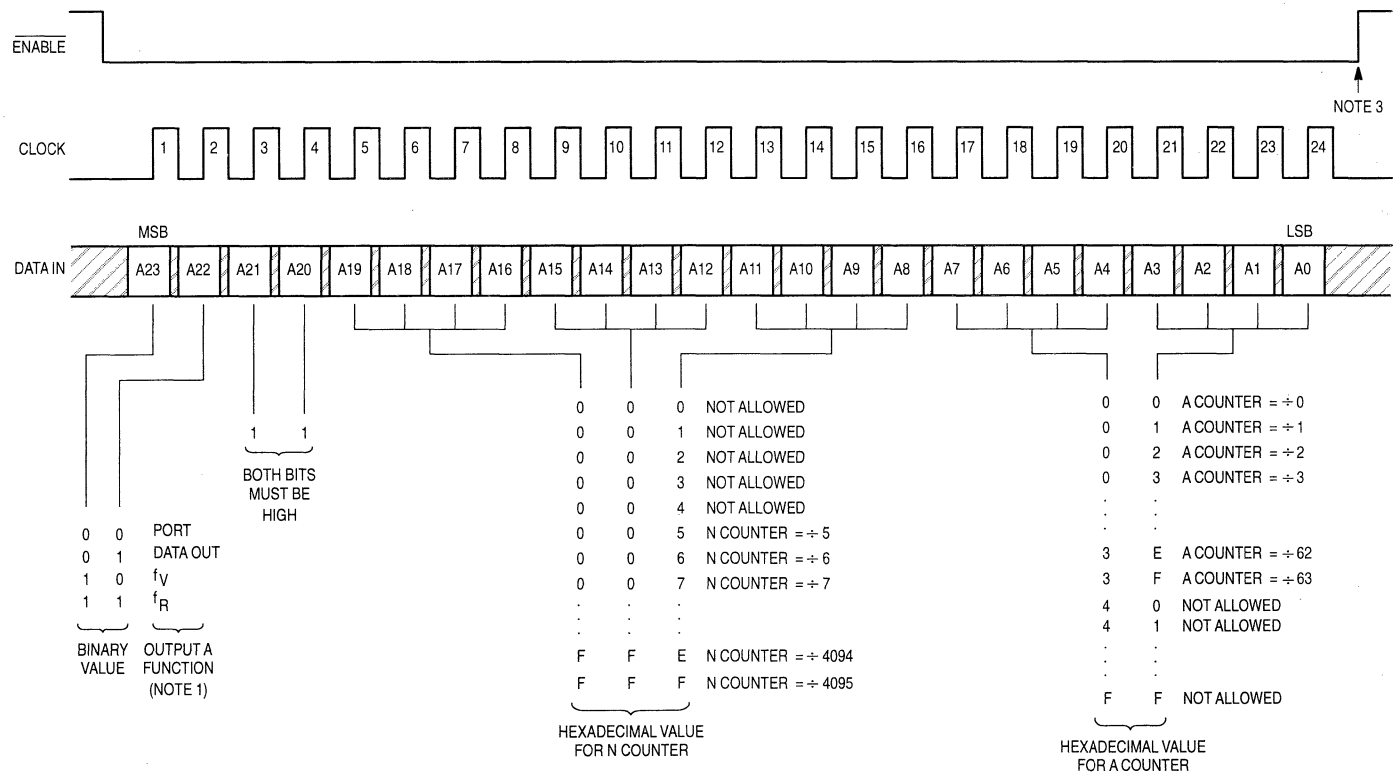
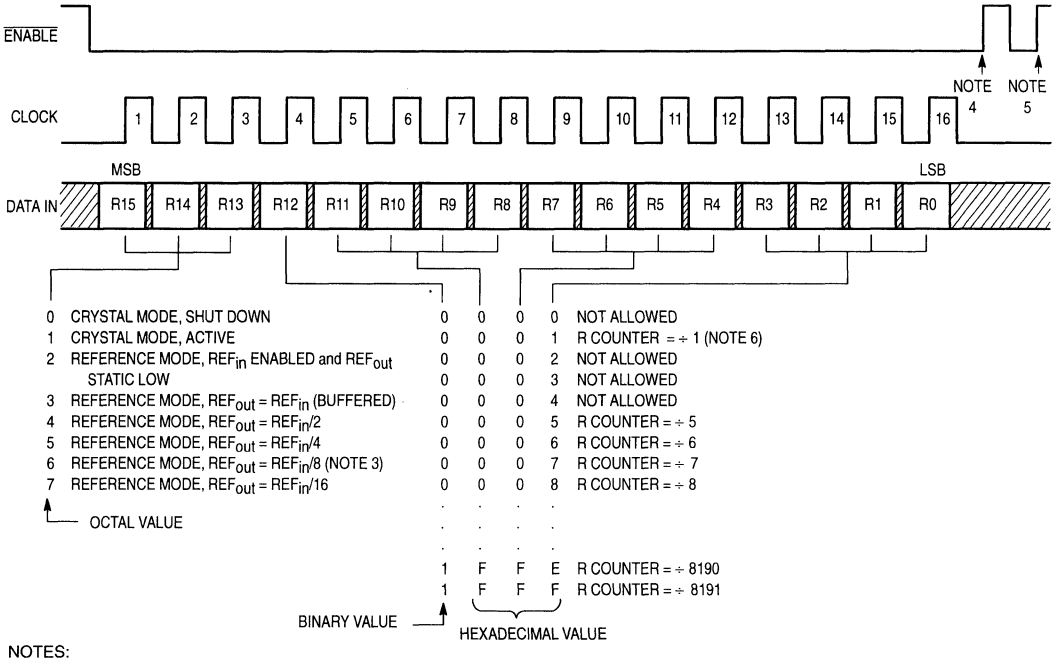


Figure 15. A Register Access and Format (24 Clock Cycles are Used)

NOTES:

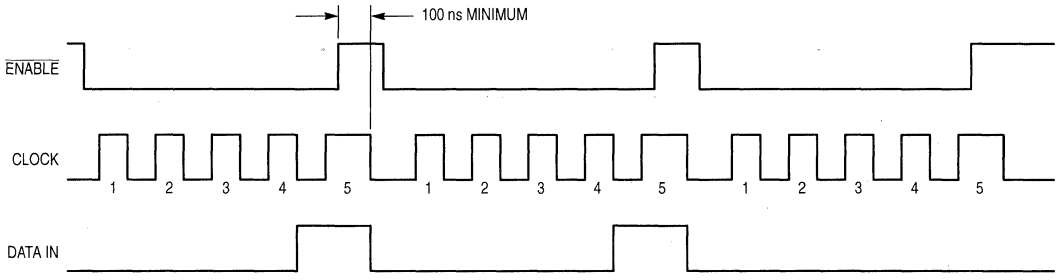
1. A power–on initialize circuit forces the Output A function to default to Data Out.
2. The values programmed for the N counter must be greater than or equal to the values programmed for the A counter. This results in a total divide value = N x 64 + A.
3. At this point, the three new bytes are transferred to the A register. In addition, the 13 LSBs in the first buffer of the R register are transferred to the R register's second buffer. Thus, the R, N, and A counters can be presented new divide ratios at the same time. The first buffer of the R register is not affected. The C register is not affected.



NOTES:

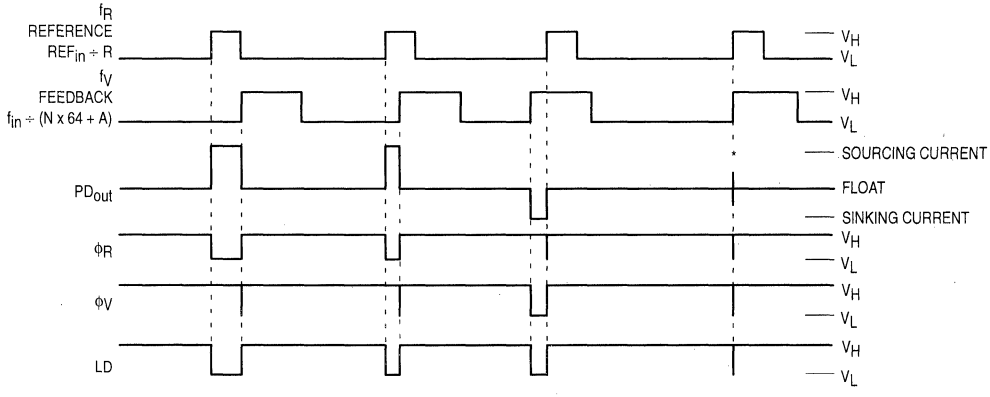
1. Bits R15 through R13 control the configurable "OSC or 4–stage divider" block (see Block Diagram).
2. Bits R12 through R0 control the "13–stage R counter" block (see Block Diagram).
3. A power–on initialize circuit forces a default REF_{in} to REF_{out} ratio of eight.
4. At this point, bits R13, R14, and R15 are stored and sent to the "OSC or 4–Stage Divider" block in the Block Diagram. Bits R0 – R12 are loaded into the first buffer in the double–buffered section of the R register. Therefore, the R counter divide ratio is not altered yet and retains the previous ratio loaded. The C and A registers are not affected.
5. At this point, bits R0 through R12 are transferred to the second buffer of the R register. The R counter begins dividing by the new ratio after completing the rest of the present count cycle. Clock must be low during the $\overline{\text{Enable}}$ pulse, as shown. Also, see note 3 of Figure 15 for an alternate method of loading the second buffer in the R register. The C and A registers are not affected. The first buffer of the R register is not affected.
6. Allows direct access to reference input of phase/frequency detectors.

Figure 16. R Register Access and Format (16 Clock Cycles Are Used)



NOTE: It may not be convenient to control the Enable or Clock pins high during power up per the Pin Descriptions. If this is the case, the part may be initialized through the serial port as shown in the figure above. The sequence is similar to accessing the registers except that the Clock must remain high at least 100 ns after Enable is brought high. Note that 3 groups of 5 bits are needed.

Figure 17. Initializing the PLL through the Serial Port



V_H = High voltage level
V_L = Low voltage level
* At this point, when both f_R and f_V are in phase, the output source and sink circuits are turned on for a short interval.
NOTE: The PD_{out} either sources or sinks current during out–of–lock conditions. When locked in phase and frequency, the output is high impedance and the voltage at that pin is determined by the low pass filter capacitor. PD_{out}, ϕ_R, and ϕ_V are shown with the polarity bit (POL) = low; see Figure 14 for POL.

Figure 18. Phase/Frequency Detectors and Lock Detector Output Waveforms

CRYSTAL OSCILLATOR CONSIDERATIONS

The following options may be considered to provide a reference frequency to Motorola's CMOS frequency synthesizers.

USE OF A HYBRID CRYSTAL OSCILLATOR

Commercially available temperature–compensated crystal oscillators (TCXOs) or crystal–controlled data clock oscillators provide very stable reference frequencies. An oscillator capable of CMOS logic levels at the output may be direct or dc coupled to REF_{in}. If the oscillator does not have CMOS logic levels on the outputs, capacitive or ac coupling to REF_{in} may be used. See Figure 8.

For additional information about TCXOs and data clock oscillators, please consult the latest version of the *eem Electronic Engineers Master Catalog,* the *Gold Book,* or similar publications.

DESIGN AN OFF–CHIP REFERENCE

The user may design an off–chip crystal oscillator using discrete transistors or ICs specifically developed for crystal oscillator applications, such as the MC12061 MECL device. The reference signal from the MECL device is ac coupled to REF_{in}. (See Figure 8.) For large amplitude signals (standard CMOS logic levels), dc coupling may be used.

USE OF THE ON–CHIP OSCILLATOR CIRCUITRY

The on–chip amplifier (a digital inverter) along with an appropriate crystal may be used to provide a reference source frequency. A fundamental mode crystal, parallel resonant at the desired operating frequency, should be connected as shown in Figure 19.

The crystal should be specified for a loading capacitance, C_L, which does not exceed approximately 20 pF when used at the highest operating frequency of 10 MHz. Assuming R1 = 0 Ω, the shunt load capacitance, C_L, presented across the crystal can be estimated to be:

$$C_L = \frac{C_{in}C_{out}}{C_{in} + C_{out}} + C_a + C_{stray} + \frac{C1 \bullet C2}{C1 + C2}$$

where

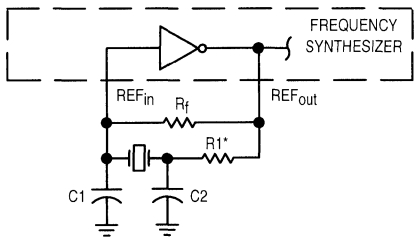
C_{in} = 5 pF (see Figure 20)
C_{out} = 6 pF (see Figure 20)
C_a = 1 pF (see Figure 20)
C1 and C2 = external capacitors (see Figure 19)
C_{stray} = the total equivalent external circuit stray capacitance appearing across the crystal terminals

The oscillator can be "trimmed" on–frequency by making either a portion or all of C1 variable. The crystal and associated components must be located as close as possible to the REF_{in} and REF_{out} pins to minimize distortion, stray capacitance, stray inductance, and startup stabilization time. Circuit stray capacitance can also be handled by adding the appropriate stray value to the values for C_{in} and C_{out}. For this approach, the term C_{stray} becomes zero in the above expression for C_L.

Power is dissipated in the effective series resistance of the crystal, R_e, in Figure 21. The maximum drive level specified by the crystal manufacturer represents the maximum stress that the crystal can withstand without damage or excessive shift in operating frequency. R1 in Figure 19 limits the drive level. The use of R1 is not necessary in most cases.

To verify that the maximum dc supply voltage does not cause the crystal to be overdriven; monitor the output frequency (f_R) at Output A as a function of supply voltage. (REF_{out} is not used because loading impacts the oscillator.) The frequency should increase very slightly as the dc supply voltage is increased. An overdriven crystal decreases in frequency or becomes unstable with an increase in supply voltage. The operating supply voltage must be reduced or R1 must be increased in value if the overdriven condition exists. Note that the oscillator start–up time is proportional to the value of R1.

Through the process of supplying crystals for use with CMOS inverters, many crystal manufacturers have developed expertise in CMOS oscillator design with crystals. Discussions with such manufacturers can prove very helpful. See Table 4.



* May be needed in certain cases. See text.

Figure 19. Pierce Crystal Oscillator Circuit

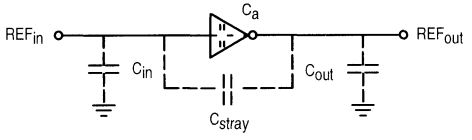
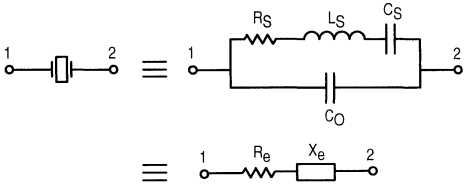


Figure 20. Parasitic Capacitances of the Amplifier and C_{stray}



NOTE: Values are supplied by crystal manufacturer (parallel resonant crystal).

Figure 21. Equivalent Crystal Networks

RECOMMENDED READING

Technical Note TN–24, Statek Corp.

Technical Note TN–7, Statek Corp.

E. Hafner, "The Piezoelectric Crystal Unit–Definitions and Method of Measurement", *Proc. IEEE,* Vol. 57, No. 2, Feb. 1969.

D. Kemper, L. Rosine, "Quartz Crystals for Frequency Control", *Electro–Technology,* June 1969.

P. J. Ottowitz, "A Guide to Crystal Selection", *Electronic Design*, May 1966.

D. Babin, "Designing Crystal Oscillators", *Machine Design*, March 7, 1985.

D. Babin, "Guidelines for Crystal Oscillator Design", *Machine Design*, April 25, 1985.

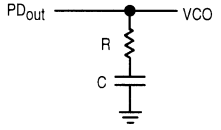
Table 4. Partial List of Crystal Manufacturers

Name	Address	Phone
United States Crystal Corp.	3605 McCart Ave., Ft. Worth, TX 76110	(817) 921–3013
Crystek Crystal	2351 Crystal Dr., Ft. Myers, FL 33907	(813) 936–2109
Statek Corp.	512 N. Main St., Orange, CA 92668	(714) 639–7810
Fox Electronics	5570 Enterprise Parkway, Ft. Myers, FL 33905	(813) 693–0099

NOTE: Motorola cannot recommend one supplier over another and in no way suggests that this is a complete listing of crystal manufacturers.

PHASE–LOCKED LOOP — LOW–PASS FILTER DESIGN

(A)



$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NC}}$$

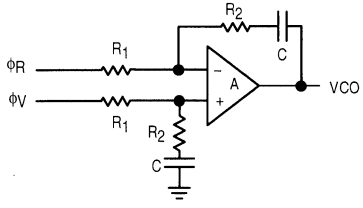
$$\zeta = \frac{R}{2}\sqrt{\frac{K_\phi K_{VCO} C}{N}} = \frac{\omega_n RC}{2}$$

$$Z(s) = \frac{1 + sRC}{sC}$$

NOTE:

For (A), using K_ϕ in amps per radian with the filter's impedance transfer function, Z(s), maintains units of volts per radian for the detector/filter combination. Additional sideband filtering can be accomplished by adding a capacitor C′ across R. The corner $\omega_c = 1/RC'$ should be chosen such that ω_n is not significantly affected.

(B)



$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NCR_1}}$$

$$\zeta = \frac{\omega_n R_2 C}{2}$$

ASSUMING GAIN A IS VERY LARGE, THEN:

$$F(s) = \frac{R_2 sC + 1}{R_1 sC}$$

NOTE:

For (B), R_1 is frequently split into two series resistors; each resistor is equal to R_1 divided by 2. A capacitor C_C is then placed from the midpoint to ground to further filter the error pulses. The value of C_C should be such that the corner frequency of this network does not significantly affect ω_n.

* The ϕ_R and ϕ_V outputs are fed to an external combiner/loop filter. The ϕ_R and ϕ_V outputs swing rail–to–rail. Therefore, the user should be careful not to exceed the common mode input range of the op amp used in the combiner/loop filter.

DEFINITIONS:

N = Total Division Ratio in Feedback Loop

K_ϕ (Phase Detector Gain) = $I_{PDout}/2\pi$ amps per radian for PD_{out}

K_ϕ (Phase Detector Gain) = $V_{PD}/2\pi$ volts per radian for ϕ_V and ϕ_R

K_{VCO} (VCO Transfer Function) = $\frac{2\pi\Delta f_{VCO}}{\Delta V_{VCO}}$ radians per volt

For a nominal design starting point, the user might consider a damping factor $\zeta \approx 0.7$ and a natural loop frequency $\omega_n = (2\pi f_R/50)$ where f_R is the frequency at the phase detector input. Larger ω_n values result in faster loop lock times and, for similar sideband filtering, higher f_R–related VCO sidebands.

Either loop filter (A) or (B) is frequently followed by additional sideband filtering to further attenuate f_R–related VCO sidebands. This additional filtering may be active or passive.

RECOMMENDED READING:

Gardner, Floyd M., *Phaselock Techniques (second edition).* New York, Wiley–Interscience, 1979.

Manassewitsch, Vadim, *Frequency Synthesizers: Theory and Design (second edition).* New York, Wiley–Interscience, 1980.

Blanchard, Alain, *Phase–Locked Loops: Application to Coherent Receiver Design.* New York, Wiley–Interscience, 1976.

Egan, William F., *Frequency Synthesis by Phase Lock.* New York, Wiley–Interscience, 1981.

Rohde, Ulrich L., *Digital PLL Frequency Synthesizers Theory and Design.* Englewood Cliffs, NJ, Prentice–Hall, 1983.

Berlin, Howard M., *Design of Phase–Locked Loop Circuits, with Experiments.* Indianapolis, Howard W. Sams and Co., 1978.

Kinley, Harold, *The PLL Synthesizer Cookbook.* Blue Ridge Summit, PA, Tab Books, 1980.

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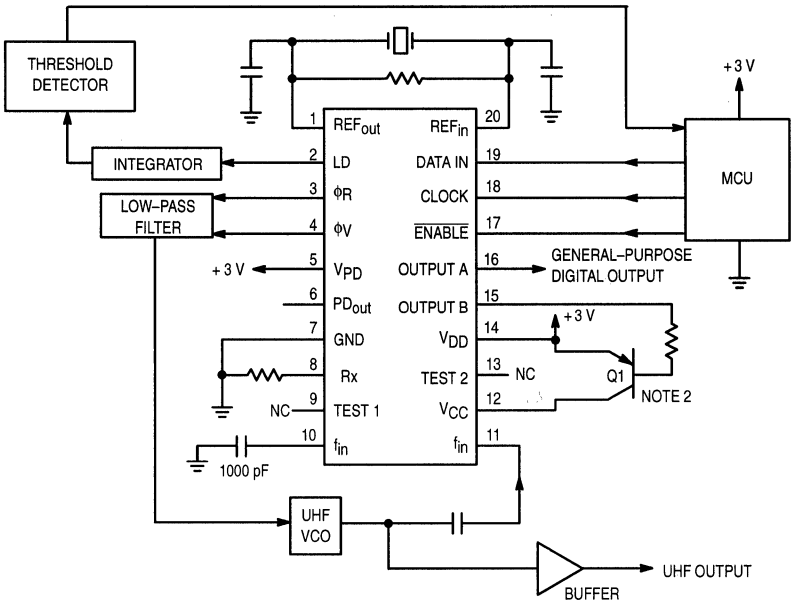
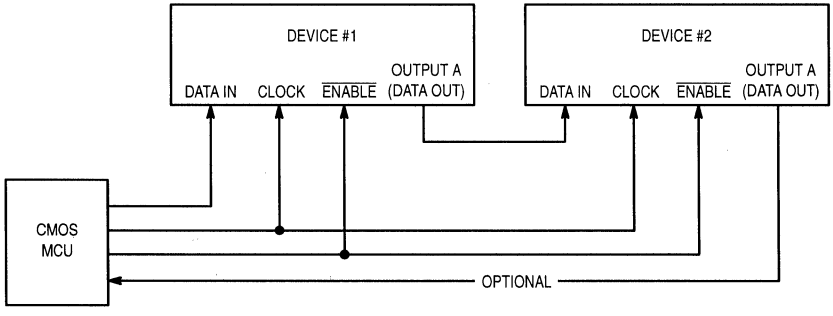
AN1253/D, An Improved PLL Design Method Without ω_n and ζ, Motorola Semiconductor Products, Inc., 1995.



NOTES:

1. When used, the ϕ_R and ϕ_V outputs are fed to an external combiner/loop filter. See the Phase–Locked Loop — Low–Pass Filter Design page for additional information.
2. Transistor Q1 is required only if the standby feature is needed. Q1 permits the bipolar section of the device to be shut down via use of the general–purpose digital pin, Output B. If the standby feature is not needed, tie Pin 12 directly to the power supply.
3. For optimum performance, bypass the V_{CC}, V_{DD}, and V_{PD} pins to GND with low–inductance capacitors.
4. The R counter is programmed for a divide value = REF_{in} / f_R. Typically, f_R is the tuning resolution required for the VCO. Also, the VCO frequency divided by $f_R = N_T = N \times 64 + A$; this determines the values (N, A) that must be programmed into the N and A counters, respectively.

Figure 22. Example Application



NOTE: See related Figures 24, 25, and 26.

Figure 23. Cascading Two Devices

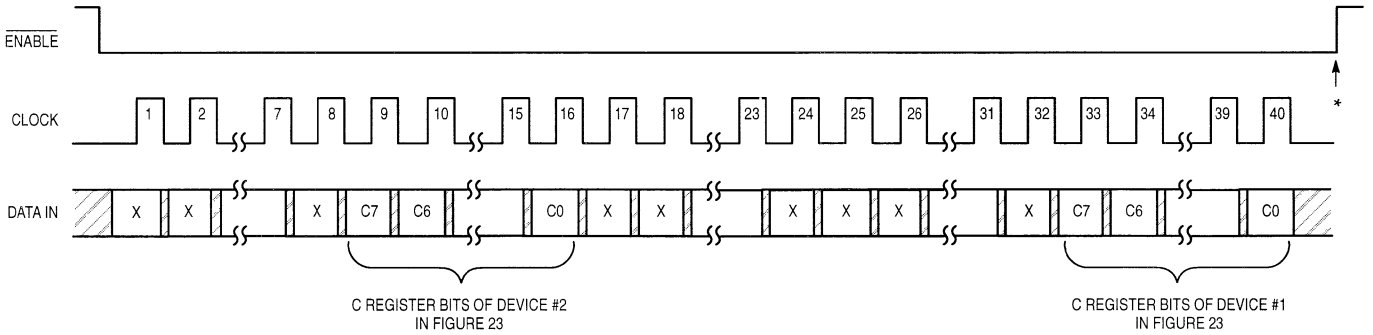


Figure 24. Accessing the C Registers of Two Cascaded Devices

*At this point, the new bytes are transferred to the C registers of both devices and stored. No other registers are affected.

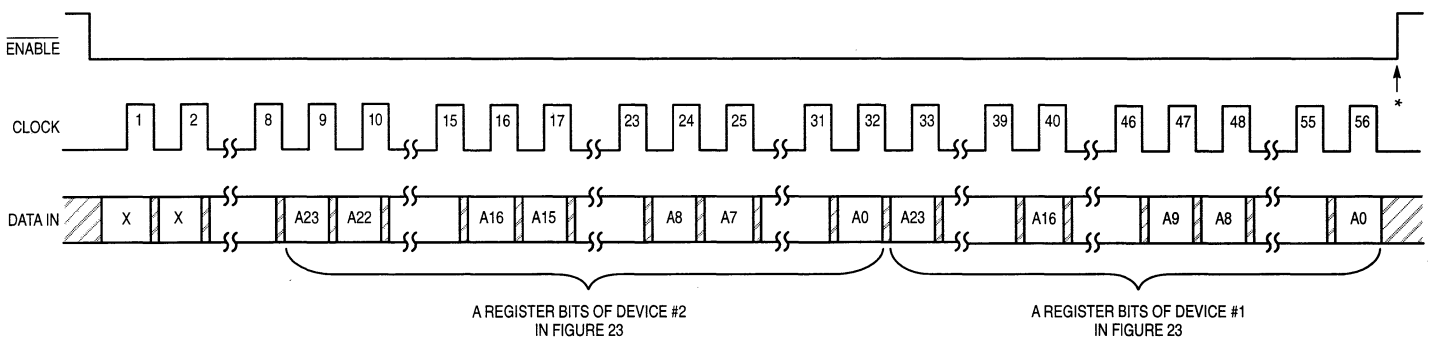


Figure 25. Accessing the A Registers of Two Cascaded Devices

*At this point, the new bytes are transferred to the A registers of both devices and stored. Additionally, for both devices, the 13 LSBs in each of the first buffers of the R registers are transferred to the respective R register's second buffer. Thus, the R, N, and A counters can be presented new divide ratios at the same time. The first buffer of each R register is not affected. Neither C register is affected.

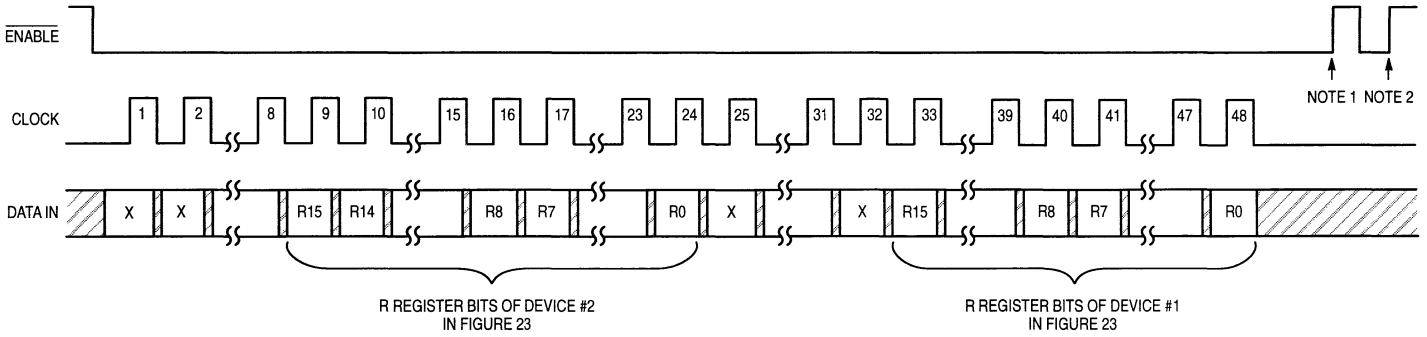


Figure 26. Accessing the R Registers of Two Cascaded Devices

NOTES APPLICABLE TO EACH DEVICE:

1. At this point, bits R13, R14, and R15 are stored and sent to the "OSC or 4–Stage Divider" block in the Block Diagram. Bits R0 through R12 are loaded into the first buffer in the double–buffered section of the R register. Therefore, the R counter divide ratio is not altered yet and retains the previous ratio loaded. The C and A registers are not affected.
2. At this point, the bits R0 through R12 are transferred to the second buffer of the R register. The R counter begins dividing by the new ratio after completing the rest of the present count cycle. Clock must be low during the $\overline{\text{Enable}}$ pulse, as shown. Also, see note of Figure 25 for an alternate method of loading the second buffer in the R register. The C and A registers are not affected. The first buffer of the R register is not affected.

MC145200
MC145201

2.0 GHz PLL Frequency Synthesizers
Include On–Board 64/65 Prescalers

2

The MC145200 and MC145201 are single–package synthesizers with serial interfaces capable of direct usage up to 2.0 GHz. A special architecture makes these PLLs very easy to program because a byte–oriented format is utilized. Due to the patented BitGrabber™ registers, no address/steering bits are required for *random access* of the three registers. Thus, tuning can be accomplished via a 3–byte serial transfer to the 24–bit A register. The interface is both SPI and MICROWIRE™ compatible.

Each device features a single–ended current source/sink phase detector output and a double–ended phase detector output. Both phase detectors have linear transfer functions (no dead zones). The maximum current of the single–ended phase detector output is determined by an external resistor tied from the Rx pin to ground. This current can be varied via the serial port.

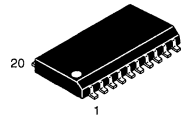
The MC145200 features logic–level converters and high–voltage phase/frequency detectors; the detector supply may range up to 9.5 V. The MC145201 has lower–voltage phase/frequency detectors optimized for single–supply systems of 5 V ±10%.

Each part includes a differential RF input which may be operated in a single–ended mode. Also featured are on–board support of an external crystal and a programmable reference output. The R, A, and N counters are fully programmable. The C register (configuration register) allows the parts to be configured to meet various applications. A patented feature allows the C register to shut off unused outputs, thereby minimizing system noise and interference.

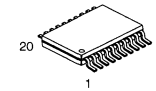
In order to have consistent lock times and prevent erroneous data from being loaded into the counters, on–board circuitry synchronizes the update of the A register if the A or N counters are loading. Similarly, an update of the R register is synchronized if the R counter is loading.

The double–buffered R register allows new divide ratios to be presented to the three counters (R, A, and N) simultaneously.

- Maximum Operating Frequency: 2000 MHz @ V_{in} = 200 mV p–p
- Operating Supply Current: 12 mA Nominal
- Operating Supply Voltage Range (V_{DD} and V_{CC} Pins): 4.5 to 5.5 V
- Operating Supply Voltage Range of Phase Detectors (V_{PD} Pin) —
  MC145200: 8.0 to 9.5 V
  MC145201: 4.5 to 5.5 V
- Current Source/Sink Phase Detector Output Capability: 2 mA Maximum
- Gain of Current Source/Sink Phase/Frequency Detector Controllable via Serial Port
- Operating Temperature Range: – 40 to + 85°C
- R Counter Division Range: (1 and) 5 to 8191
- Dual–Modulus Capability Provides Total Division up to 262,143
- High–Speed Serial Interface: 4 Mbps
- OUTPUT A Pin, When Configured as Data Out, Permits Cascading of Devices
- Two General–Purpose Digital Outputs — OUTPUT A: Totem–Pole (Push–Pull)
  OUTPUT B: Open–Drain
- Power–Saving Standby Feature with Orderly Recovery for Minimizing Lock Times, Standby Current: 30 µA
- Evaluation Kit Available (Part Numbers MC145200EVK and MC145201EVK). See Evaluation Kit Section



F SUFFIX
SOG PACKAGE
CASE 751J

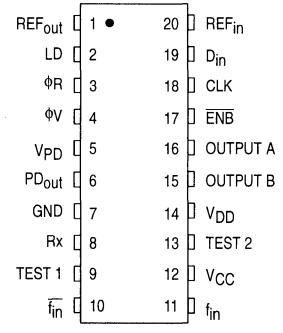


DT SUFFIX
TSSOP
CASE 948D

ORDERING INFORMATION

MC145200F	SOG Package
MC145201F	SOG Package
MC145200DT	TSSOP
MC145201DT	TSSOP

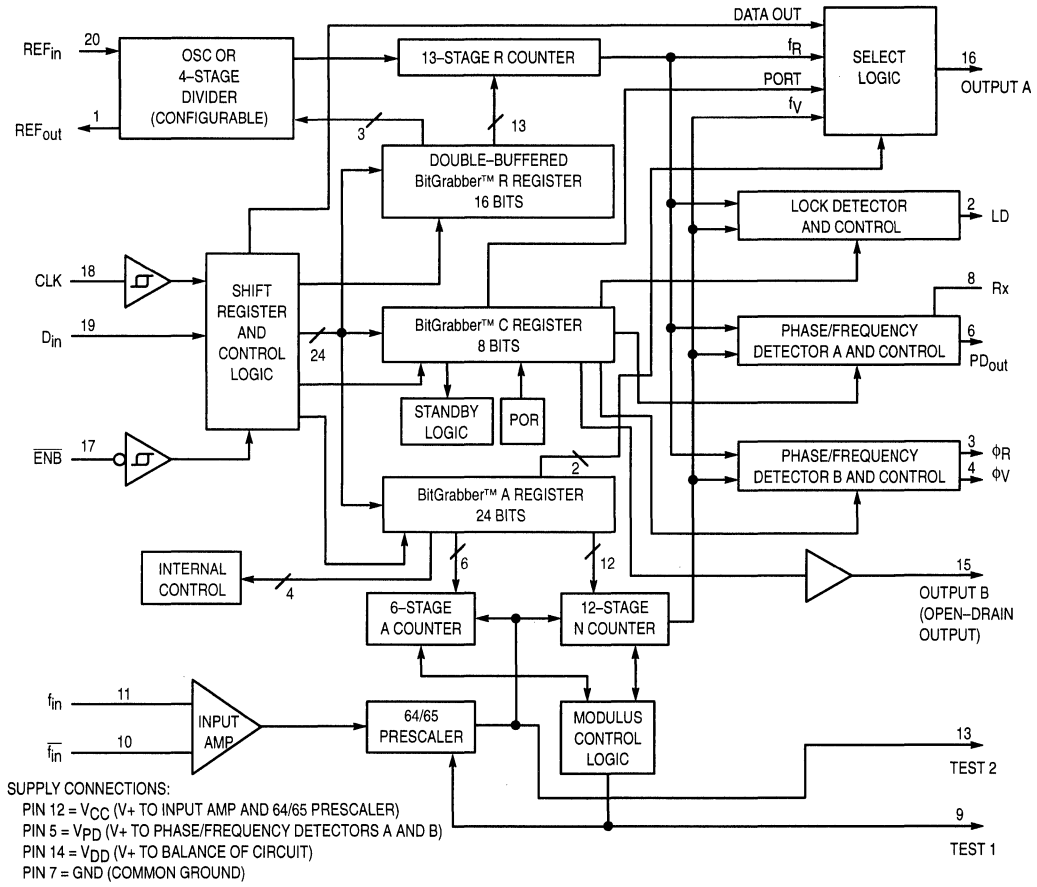
PIN ASSIGNMENT



BitGrabber is a trademark of Motorola, Inc. MICROWIRE is a trademark of National Semiconductor Corp.

REV 3
10/95

BLOCK DIAGRAM



SUPPLY CONNECTIONS:
PIN 12 = V_{CC} (V+ TO INPUT AMP AND 64/65 PRESCALER)
PIN 5 = V_{PD} (V+ TO PHASE/FREQUENCY DETECTORS A AND B)
PIN 14 = V_{DD} (V+ TO BALANCE OF CIRCUIT)
PIN 7 = GND (COMMON GROUND)

MAXIMUM RATINGS* (Voltages Referenced to GND, unless otherwise stated)

Symbol	Parameter		Value	Unit
V_{CC}, V_{DD}	DC Supply Voltage (Pins 12 and 14)		−0.5 to +6.0	V
V_{PD}	DC Supply Voltage (Pin 5)	MC145200 MC145201	V_{DD} −0.5 to +9.5 V_{DD} −0.5 to +6.0	V
V_{in}	DC Input Voltage		−0.5 to V_{DD} +0.5	V
V_{out}	DC Output Voltage (except OUTPUT B, PD_{out}, ϕR, ϕV)		−0.5 to V_{DD} +0.5	V
V_{out}	DC Output Voltage (OUTPUT B, PD_{out}, ϕR, ϕV)		−0.5 to V_{PD} +0.5	V
I_{in}, I_{PD}	DC Input Current, per Pin (Includes V_{PD})		±10	mA
I_{out}	DC Output Current, per Pin		±20	mA
I_{DD}	DC Supply Current, V_{DD} and GND Pins		±30	mA
P_D	Power Dissipation, per Package		300	mW
T_{stg}	Storage Temperature		−65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 seconds		260	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Descriptions section.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit.

ELECTRICAL CHARACTERISTICS

($V_{DD} = V_{CC}$ = 4.5 to 5.5 V, Voltages Referenced to GND, T_A = −40 to +85°C, unless otherwise stated; MC145200: V_{PD} = 8.0 to 9.5 V; MC145201: V_{PD} = 4.5 to 5.5 V with $V_{DD} \leq V_{PD}$.)

Symbol	Parameter	Test Condition	Guaranteed Limit	Unit
V_{IL}	Maximum Low–Level Input Voltage (D_{in}, CLK, $\overline{ENB}$, REF_{in})	Device in Reference Mode, DC Coupled	$0.3 \times V_{DD}$	V
V_{IH}	Minimum High–Level Input Voltage (D_{in}, CLK, $\overline{ENB}$, REF_{in})	Device in Reference Mode, DC Coupled	$0.7 \times V_{DD}$	V
V_{hys}	Minimum Hysteresis Voltage (CLK, $\overline{ENB}$)		300	mV
V_{OL}	Maximum Low–Level Output Voltage (REF_{out}, OUTPUT A)	I_{out} = 20 µA, Device in Reference Mode	0.1	V
V_{OH}	Minimum High–Level Output Voltage (REF_{out}, OUTPUT A)	I_{out} = –20 µA, Device in Reference Mode	$V_{DD} - 0.1$	V
I_{OL}	Minimum Low–Level Output Current (REF_{out}, LD, ϕ_R, ϕ_V)	V_{out} = 0.4 V	0.36	mA
I_{OH}	Minimum High–Level Output Current (REF_{out}, LD, ϕ_R, ϕ_V)	$V_{out} = V_{DD} - 0.4$ V for REF_{out}, LD $V_{out} = V_{PD} - 0.4$ V for ϕ_R, ϕ_V	−0.36	mA
I_{OL}	Minimum Low–Level Output Current (OUTPUT A, OUTPUT B)	V_{out} = 0.4 V	1.0	mA
I_{OH}	Minimum High–Level Output Current (OUTPUT A Only)	$V_{out} = V_{DD} - 0.4$ V	− 0.6	mA
I_{in}	Maximum Input Leakage Current (D_{in}, CLK, $\overline{ENB}$, REF_{in})	$V_{in} = V_{DD}$ or GND, Device in XTAL Mode	± 1.0	µA
I_{in}	Maximum Input Current (REF_{in})	$V_{in} = V_{DD}$ or GND, Device in Reference Mode	± 150	µA
I_{OZ}	Maximum Output Leakage Current (PD_{out})	$V_{out} = V_{PD} - 0.5$ or 0.5 V MC145200 Output in High–Impedance State MC145201	± 150 ± 200	nA
I_{OZ}	Maximum Output Leakage Current (OUTPUT B)	$V_{out} = V_{PD}$ or GND, Output in High–Impedance State	± 10	µA
I_{STBY}	Maximum Standby Supply Current (V_{DD} + V_{PD} Pins)	$V_{in} = V_{DD}$ or GND; Outputs Open; Device in Standby Mode, Shut–Down Crystal Mode or REF_{out}–Static–Low Reference Mode; OUTPUT B Controlling V_{CC} per Figure 22	30	µA
I_{PD}	Maximum Phase Detector Quiescent Current (V_{PD} Pin)	Bit C6 = High Which Selects Phase Detector A, PD_{out} = Open, PD_{out} = Static Low or High, Bit C4 = Low Which is ***not*** Standby, I_{Rx} = 113 µA	600	µA
		Bit C6 = Low Which Selects Phase Detector B, ϕ_R and ϕ_V = Open, ϕ_R and ϕ_V = Static Low or High, Bit C4 = Low Which is ***not*** Standby	30	
I_T	Total Operating Supply Current (V_{DD} + V_{PD} + V_{CC} Pins)	f_{in} = 2.0 GHz; REF_{in} = 13 MHz @ 1 V p–p; OUTPUT A = Inactive and No Connect; REF_{out}, ϕ_V, ϕ_R, PD_{out}, LD = No Connect; D_{in}, $\overline{ENB}$, CLK = V_{DD} or GND, Phase Detector B Enabled (Bit C6 = Low)	*	mA

* The nominal value = 12 mA. This is not a guaranteed limit.

ANALOG CHARACTERISTICS—CURRENT SOURCE/SINK OUTPUT—PD_{out}

($I_{out} \leq 2$ mA, $V_{DD} = V_{CC} = 4.5$ to 5.5 V, $V_{DD} \leq V_{PD}$. Voltages Referenced to GND)

Parameter	Test Condition	V_{PD}	Guaranteed Limit	Unit
Maximum Source Current Variation	MC145200: $V_{out} = 0.5 \times V_{PD}$	8.0	± 20	%
		9.5	± 20	
	MC145201: $V_{out} = 0.5 \times V_{PD}$	4.5	± 20	%
		5.5	± 20	
Maximum Sink–vs–Source Mismatch (Note 3)	MC145200: $V_{out} = 0.5 \times V_{PD}$	8.0	12	%
		9.5	12	
	MC145201: $V_{out} = 0.5 \times V_{PD}$	4.5	12	%
		5.5	12	
Output Voltage Range (Note 3)	MC145200: I_{out} variation ≤ 20%	8.0	0.5 to 7.5	V
		9.5	0.5 to 9.0	
	MC145201: I_{out} variation ≤ 20%	4.5	0.5 to 4.0	V
		5.5	0.5 to 5.0	

NOTES:
1. Percentages calculated using the following formula: (Maximum Value – Minimum Value)/Maximum Value.
2. See Rx Pin Description for external resistor values.
3. This parameter is guaranteed for a given temperature within –40 to +85°C.

AC INTERFACE CHARACTERISTICS

($V_{DD} = 4.5$ to 5.5 V, $T_A = -40$ to +85°C, $C_L = 50$ pF, Input $t_r = t_f = 10$ ns; MC145200: $V_{PD} = 8.0$ to 9.5 V; MC145201: $V_{PD} = 4.5$ to 5.5 V with $V_{DD} \leq V_{PD}$)

Symbol	Parameter	Figure No.	Guaranteed Limit	Unit
f_{clk}	Serial Data Clock Frequency (Note: Refer to Clock t_w below)	1	dc to 4.0	MHz
t_{PLH}, t_{PHL}	Maximum Propagation Delay, CLK to OUTPUT A (Selected as Data Out)	1, 5	105	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay, $\overline{ENB}$ to OUTPUT A (Selected as Port)	2, 5	100	ns
t_{PZL}, t_{PLZ}	Maximum Propagation Delay, $\overline{ENB}$ to OUTPUT B	2, 6	120	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, OUTPUT A and OUTPUT B; t_{THL} only, on OUTPUT B	1, 5, 6	100	ns
C_{in}	Maximum Input Capacitance – D_{in}, $\overline{ENB}$, CLK,		10	pF

TIMING REQUIREMENTS

($V_{DD} = 4.5$ to 5.5 V, $T_A = -40$ to +85°C, Input $t_r = t_f = 10$ ns unless otherwise indicated)

Symbol	Parameter	Figure No.	Guaranteed Limit	Unit
t_{su}, t_h	Minimum Setup and Hold Times, D_{in} vs CLK	3	20	ns
t_{su}, t_h, t_{rec}	Minimum Setup, Hold and Recovery Times, $\overline{ENB}$ vs CLK	4	100	ns
t_w	Minimum Pulse Width, $\overline{ENB}$	4	*	cycles
t_w	Minimum Pulse Width, CLK	1	125	ns
t_r, t_f	Maximum Input Rise and Fall Times, CLK	1	100	µs

* The minimum limit is 3 REF_{in} cycles or 195 f_{in} cycles, whichever is greater.

SWITCHING WAVEFORMS

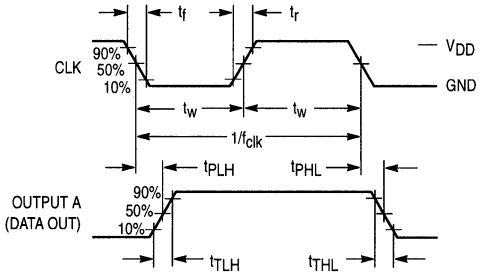


Figure 1.

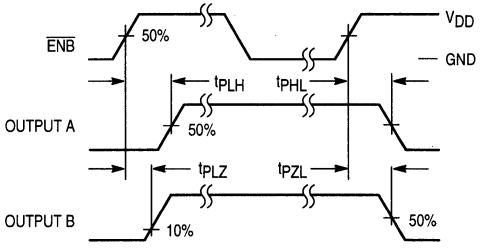


Figure 2.

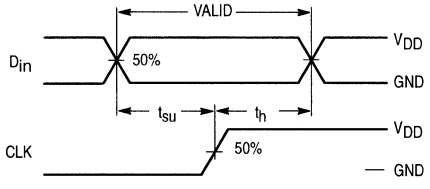


Figure 3.

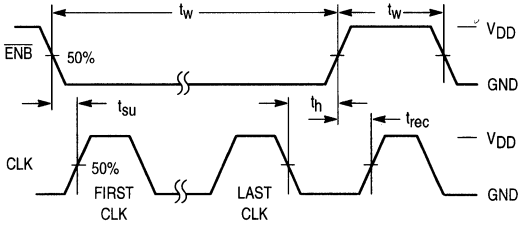
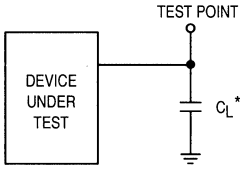
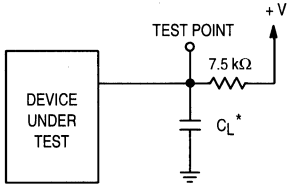


Figure 4.



*Includes all probe and fixture capacitance.

Figure 5. Test Circuit



*Includes all probe and fixture capacitance.

Figure 6. Test Circuit

LOOP SPECIFICATIONS (V_{DD} = V_{CC} = 4.5 to 5.5 V unless otherwise indicated, T_A = −40 to +85°C)

Symbol	Parameter	Test Condition	Figure No.	Guaranteed Operating Range		Unit
				Min	Max	
V_{in}	Input Voltage Range, f_{in}	500 MHz ≤ f_{in} ≤ 2000 MHz	7	200	1500	mV p–p
f_{ref}	Input Frequency, REF_{in} MC145200 Externally Driven in Reference Mode MC145201	V_{in} = 400 mV p–p V_{in} = 1 V p–p V_{in} = 400 mV p–p V_{in} = 1 V p–p	8	13 6* 12 4.5*	27 27 27 27	MHz
f_{XTAL}	Crystal Frequency, Crystal Mode	C1 ≤ 30 pF, C2 ≤ 30 pF, Includes Stray Capacitance	9	2	15	MHz
f_{out}	Output Frequency, REF_{out}	C_L = 30 pF	10, 12	dc	10	MHz
f	Operating Frequency of the Phase Detectors			dc	2	MHz
t_w	Output Pulse Width, LD, ϕ_R, and ϕ_V, — MC145200, MC145201	f_R in Phase with f_V, C_L = 50 pF, V_{PD} = 5.5 V, V_{DD} = V_{CC} = 5.0 V	11, 12	17	85	ns
t_{TLH}, t_{THL}	Output Transition Times, LD, ϕ_V, and ϕ_R — MC145201	C_L = 50 pF, V_{PD} = 5.5 V, V_{DD} = V_{CC} = 5.0 V	11, 12	—	65	ns
C_{in}	Input Capacitance f_{in} REF_{in}			— —	TBD 5	pF

*If lower frequency is desired, use wave shaping or higher amplitude sinusoidal signal.

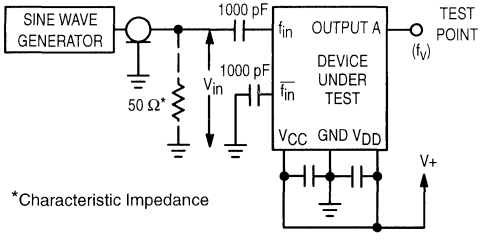


Figure 7. Test Circuit

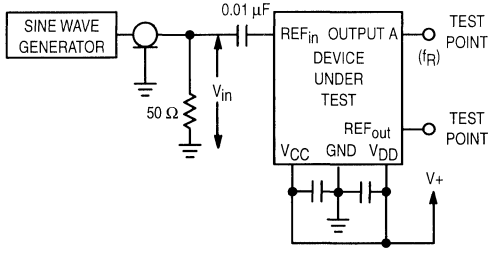


Figure 8. Test Circuit–Reference Mode

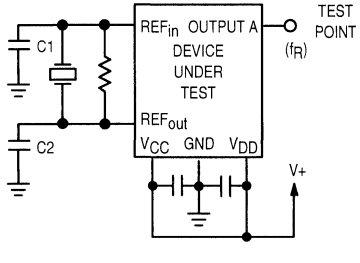


Figure 9. Test Circuit–Crystal Mode

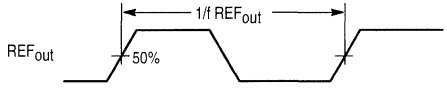


Figure 10. Switching Waveform

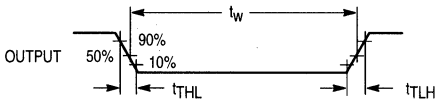


Figure 11. Switching Waveform

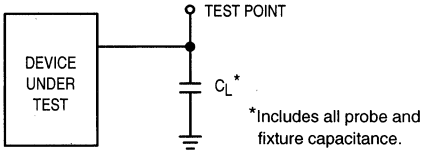
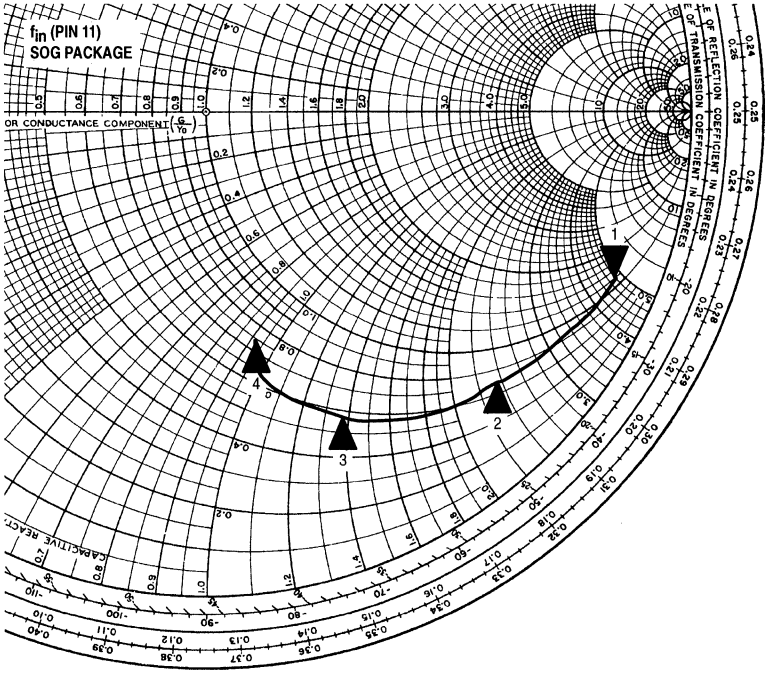


Figure 12. Test Circuit

2

MC145200/MC145201
NORMALIZED INPUT IMPEDANCE AT f_{in} — SERIES FORMAT (R + jX)
(500 MHz to 2 GHz)



Marker	Frequency (GHz)	Resistance (Ω)	Capacitive Reactance (Ω)	Capacitance (pF)
1	0.5	59.0	– 240	1.33
2	1	34.7	– 118	1.35
3	1.5	28.3	– 68.7	1.54
4	2	37.4	– 45.7	1.74

PIN DESCRIPTIONS

DIGITAL INTERFACE PINS

D_{in}
Serial Data Input (Pin 19)

The bit stream begins with the most significant bit (MSB) and is shifted in on the low–to–high transition of CLK. The bit pattern is 1 byte (8 bits) long to access the C or configuration register, 2 bytes (16 bits) to access the first buffer of the R register, or 3 bytes (24 bits) to access the A register (see Table 1). The values in the C, R, and A registers do not change during shifting because the transfer of data to the registers is controlled by $\overline{ENB}$.

CAUTION

The value programmed for the N–counter must be greater than or equal to the value of the A–counter.

The 13 least significant bits (LSBs) of the R register are double–buffered. As indicated above, data is latched into the first buffer on a 16–bit transfer. (The 3 MSBs are not double–buffered and have an immediate effect after a 16–bit transfer.) The second buffer of the R register contains the 13 bits for the R counter. This second buffer is loaded with the contents of the first buffer when the A register is loaded (a 24–bit transfer). This allows presenting new values to the R, A, and N counters simultaneously. If this is not required, then the 16–bit transfer may be followed by pulsing $\overline{ENB}$ low with no signal on the CLK pin. This is an alternate method of transferring data to the second buffer of the R register (see Figure 17).

The bit stream needs neither address nor steering bits due to the innovative BitGrabber registers. Therefore, all bits in the stream are available to be data for the three registers. Random access of any register is provided. That is, the registers may be accessed in any sequence. Data is retained in the registers over a supply range of 4.5 to 5.5 V. The formats are shown in Figures 15, 16, and 17.

D_{in} typically switches near 50% of V_{DD} to maximize noise immunity. This input can be directly interfaced to CMOS devices with outputs guaranteed to switch near rail–to–rail. When interfacing to NMOS or TTL devices, either a level shifter (MC74HC14A, MC14504B) or pull–up resistor of 1 kΩ to 10 kΩ must be used. Parameters to consider when sizing the resistor are worst–case I_{OL} of the driving device, maximum tolerable power consumption, and maximum data rate.

Table 1. Register Access

(MSBs are shifted in first; C0, R0, and A0 are the LSBs)

Number of Clocks	Accessed Register	Bit Nomenclature
8	C Register	C7, C6, C5, . . ., C0
16	R Register	R15, R14, R13, . . ., R0
24	A Register	A23, A22, A21, . . ., A0
Other Values ≤ 32	See Figure 13	
Values > 32	See Figures 22–25	

CLK
Serial Data Clock Input (Pin 18)

Low–to–high transitions on CLK shift bits available at the D_{in} pin, while high–to–low transitions shift bits from OUTPUT A (when configured as Data Out, see Pin 16). The 24–1/2–stage shift register is static, allowing clock rates down to dc in a continuous or intermittent mode.

Eight clock cycles are required to access the C register. Sixteen clock cycles are needed for the first buffer of the R register. Twenty–four cycles are used to access the A register. See Table 1 and Figures 15, 16, and 17. The number of clocks required for cascaded devices is shown in Figures 24 through 26.

CLK typically switches near 50% of V_{DD} and has a Schmitt–triggered input buffer. Slow CLK rise and fall times are allowed. See the last paragraph of **D_{in}** for more information.

NOTE

To guarantee proper operation of the power–on reset (POR) circuit, the CLK pin must be held at GND (with $\overline{ENB}$ being a don't care) or $\overline{ENB}$ must be held at the potential of the V+ pin (with CLK being a don't care) during power–up. As an alternative, the bit sequence of Figure 13 may be used.

$\overline{ENB}$
Active Low Enable Input (Pin 17)

This pin is used to activate the serial interface to allow the transfer of data to/from the device. When $\overline{ENB}$ is in an inactive high state, shifting is inhibited and the port is held in the initialized state. To transfer data to the device, $\overline{ENB}$ (which must start inactive high) is taken low, a serial transfer is made via D_{in} and CLK, and $\overline{ENB}$ is taken back high. The low–to–high transition on $\overline{ENB}$ transfers data to the C or A registers and first buffer of the R register, depending on the data stream length per Table 1.

NOTE

Transitions on $\overline{ENB}$ must not be attempted while CLK is high. This puts the device out of synchronization with the microcontroller. Resynchronization occurs when $\overline{ENB}$ is high and CLK is low.

This input is also Schmitt–triggered and switches near 50% of V_{DD}, thereby minimizing the chance of loading erroneous data into the registers. See the last paragraph of **D_{in}** for more information.

For POR information, see the note for the **CLK pin**.

OUTPUT A
Configurable Digital Output (Pin 16)

OUTPUT A is selectable as f_R, f_V, Data Out, or Port. Bits A22 and A23 in the A register control the selection; see Figure 16.

If A23 = A22 = high, OUTPUT A is configured as f_R. This signal is the buffered output of the 13–stage R counter. The f_R signal appears as normally low and pulses high, and can be used to verify the divide ratio of the R counter. This ratio extends from 5 to 8191 and is determined by the binary value loaded into bits R0 through R12 in the R register. Also, direct access to the phase detectors via the REF_{in} pin is allowed by choosing a divide value of 1 (see Figure 17). The maximum frequency at which the phase detectors operate is 2 MHz. Therefore, the frequency of f_R should not exceed 2 MHz.

If A23 = high and A22 = low, OUTPUT A is configured as f_V. This signal is the buffered output of the 12–stage N counter. The f_V signal appears as normally low and pulses high, and can be used to verify the operation of the prescaler, A counter, and N counter. The divide ratio between the f_{in} input and the f_V signal is $N \times 64 + A$. N is the divide ratio of the N counter and A is the divide ratio of the A counter. These ratios are determined by bits loaded into the A register. See Figure 16. The maximum frequency at which the phase detectors operate is 2 MHz. Therefore, the frequency of f_V should not exceed 2 MHz.

If A23 = low and A22 = high, OUTPUT A is configured as Data Out. This signal is the serial output of the 24–1/2–stage shift register. The bit stream is shifted out on the high–to–low transition of the CLK input. Upon power up, OUTPUT A is automatically configured as Data Out to facilitate cascading devices.

If A23 = A22 = low, OUTPUT A is configured as Port. This signal is a general–purpose digital output which may be used as an MCU port expander. This signal is low when the Port bit (C1) of the C register is low, and high when the Port bit is high.

OUTPUT B
Open–Drain Digital Output (Pin 15)

This signal is a general–purpose digital output which may be used as an MCU port expander. This signal is low when the Out B bit (C0) of the C register is low. When the Out B bit is high, OUTPUT B assumes the high–impedance state. OUTPUT B may be pulled up through an external resistor or active circuitry to any voltage less than or equal to the potential of the V_{PD} pin. **Note**: the maximum voltage allowed on the V_{PD} pin is 9.5 V for the MC145200 and 5.5 V for the MC145201.

Upon power–up, power–on reset circuitry forces OUTPUT B to a low level.

REFERENCE PINS

REF_{in} and REF_{out}
Reference Input and Reference Output (Pins 20 and 1)

Configurable pins for a Crystal or an External Reference. This pair of pins can be configured in one of two modes: the crystal mode or the reference mode. Bits R13, R14, and R15 in the R register control the modes as shown in Figure 17.

In crystal mode, these pins form a reference oscillator when connected to terminals of an external parallel–resonant crystal. Frequency–setting capacitors of appropriate values as recommended by the crystal supplier are connected from each of the two pins to ground (up to a maximum of 30 pF each, including stray capacitance). An external resistor of 1 MΩ to 15 MΩ is connected directly across the pins to ensure linear operation of the amplifier. The device is designed to operate with crystals up to 15 MHz; the required connections are shown in Figure 8. To turn on the oscillator, bits R15, R14, and R13 must have an octal value of one (001 in binary, respectively). This is the active–crystal mode shown in Figure 17. In this mode, the crystal oscillator runs and the R Counter divides the crystal frequency, unless the part is in standby. If the part is placed in standby via the C register, the oscillator runs, but the R counter is stopped. However, if bits R15 to R13 have a value of 0, the oscillator is stopped, which saves additional power. This is the shut–down crystal mode (shown in Figure 17) and can be engaged whether in standby or not.

In the reference mode, REF_{in} (Pin 20) accepts a signal up to 27 MHz from an external reference oscillator, such as a TCXO. A signal swinging from at least the V_{IL} to V_{IH} levels listed in the Electrical Characteristics table may be directly coupled to the pin. If the signal is less than this level, ac coupling must be used as shown in Figure 8. Due to an on–board resistor which is engaged in the reference modes, an external biasing resistor tied between REF_{in} and REF_{out} is not required.

With the reference mode, the REF_{out} pin is configured as the output of a divider. As an example, if bits R15, R14, and R13 have an octal value of seven, the frequency at REF_{out} is the REF_{in} frequency divided by 16. In addition, Figure 17 shows how to obtain ratios of eight, four, and two. A ratio of one–to–one can be obtained with an octal value of three. Upon power up, a ratio of eight is automatically initialized. The maximum frequency capability of the REF_{out} pin is 10 MHz. Therefore, for REF_{in} frequencies above 10 MHz, the one–to–one ratio may not be used. Likewise, for REF_{in} frequencies above 20 MHz, the ratio must be more than two.

If REF_{out} is unused, an octal value of two should be used for R15, R14, and R13 and the REF_{out} pin should be floated. A value of two allows REF_{in} to be functional while disabling REF_{out}, which minimizes dynamic power consumption and electromagnetic interference (EMI).

LOOP PINS

f_{in} and $\overline{f_{in}}$
Frequency Inputs (Pins 11 and 10)

These pins are frequency inputs from the VCO. These pins feed the on–board RF amplifier which drives the 64/65 prescaler. These inputs may be fed differentially. However, they usually are used in a single–ended configuration (shown in Figure 7). Note that f_{in} is driven while $\overline{f_{in}}$ must be tied to ground via a capacitor.

Motorola does not recommend driving $\overline{f_{in}}$ while terminating f_{in} because this configuration is not tested for sensitivity. The sensitivity is dependent on the frequency as shown in the Loop Specifications table.

PD_{out}
Single–Ended Phase/Freq. Detector Output (Pin 6)

This is a three–state current–source/sink output for use as a loop error signal when combined with an external low–pass filter. The phase/frequency detector is characterized by a linear transfer function (no dead zone). The operation of the phase/ frequency detector is described below and is shown in Figure 18.

POL bit (C7) in the C register = low (see Figure 15)
- Frequency of $f_V > f_R$ or Phase of f_V Leading f_R: current–sinking pulses from a floating state
- Frequency of $f_V < f_R$ or Phase of f_V Lagging f_R: current–sourcing pulses from a floating state
- Frequency and Phase of $f_V = f_R$: essentially a floating state; voltage at pin determined by loop filter

POL bit (C7) = high
- Frequency of $f_V > f_R$ or Phase of f_V Leading f_R: current–sourcing pulses from a floating state
- Frequency of $f_V < f_R$ or Phase of f_V Lagging f_R: current–sinking pulses from a floating state

Frequency and Phase of $f_V = f_R$: essentially a floating state; voltage at pin determined by loop filter

This output can be enabled, disabled, and inverted via the C register. If desired, PD_{out} can be forced to a floating state by utilization of the disable feature in the C register (bit C6). This is a patented feature. Similarly, PD_{out} is forced to the floating state when the device is put into standby (STBY bit C4 = high).

The PD_{out} circuit is powered by V_{PD}. The phase detector gain is controllable by bits C3, C2, and C1: gain (in amps per radian) = PD_{out} current divided by 2π.

ϕ_R and ϕ_V (Pins 3 and 4)
Double–Ended Phase/Frequency Detector Outputs

These outputs can be combined externally to generate a loop error signal. Through use of a Motorola patented technique, the detector's dead zone has been eliminated. Therefore, the phase/frequency detector is characterized by a linear transfer function. The operation of the phase/frequency detector is described below and is shown in Figure 18.

POL bit (C7) in the C register = low (see Figure 15)

Frequency of $f_V > f_R$ or Phase of f_V Leading f_R: ϕ_V = negative pulses, ϕ_R = essentially high

Frequency of $f_V < f_R$ or Phase of f_V Lagging f_R: ϕ_V = essentially high, ϕ_R = negative pulses

Frequency and Phase of $f_V = f_R$: ϕ_V and ϕ_R remain essentially high, except for a small minimum time period when both pulse low in phase

POL bit (C7) = high

Frequency of $f_V > f_R$ or Phase of f_V Leading f_R: ϕ_R = negative pulses, ϕ_V = essentially high

Frequency of $f_V < f_R$ or Phase of f_V Lagging f_R: ϕ_R = essentially high, ϕ_V = negative pulses

Frequency and Phase of $f_V = f_R$: ϕ_V and ϕ_R remain essentially high, except for a small minimum time period when both pulse low in phase

These outputs can be enabled, disabled, and interchanged via C register bits C6 or C4. This is a patented feature. Note that when disabled or in standby, ϕ_R and ϕ_V are forced to their rest condition (high state).

The ϕ_R and ϕ_V output signal swing is approximately from GND to V_{PD}.

LD
Lock Detector Output (Pin 2)

This output is essentially at a high level with narrow low–going pulses when the loop is locked (f_R and f_V of the same phase and frequency). The output pulses low when f_V and f_R are out of phase or different frequencies. LD is the logical ANDing of ϕ_R and ϕ_V (see Figure 18).

This output can be enabled and disabled via the C register. This is a patented feature. Upon power up, on–chip initialization circuitry disables LD to a static low logic level to prevent a false "lock" signal. If unused, LD should be disabled and left open.

The LD output signal swing is approximately from GND to V_{DD}.

Rx
External Resistor (Pin 8)

A resistor tied between this pin and GND, in conjunction with bits in the C register, determines the amount of current that the PD_{out} pin sinks and sources. When bits C2 and C3 are both set high, the maximum current is obtained at PD_{out}; see Tables 2 and 3 for other values of current. To achieve a maximum current of 2 mA, the resistor should be about 47 kΩ when V_{PD} is 9 V or about 18 kΩ when V_{PD} is 5.0 V. See Figure 14 if lower maximum current values are desired.

When the ϕ_R and ϕ_V outputs are used, the Rx pin may be floated.

TEST POINT PINS

TEST 1
Modulus Control Signal (Pin 9)

This pin may be used in conjunction with the Test 2 pin for access to the on–board 64/65 prescaler. When Test 1 is low, the prescaler divides by 65. When high, the prescaler divides by 64.

CAUTION

This pin is an unbuffered output and ***must*** be floated in an actual application. This pin must be attached to an isolated pad with no trace. There is the possibility that the device may be modified and have this lead clipped at the body of the package.

TEST 2
Prescaler Output (Pin 13)

This pin may be used to access to the on–board 64/65 prescaler output.

CAUTION

This pin is an unbuffered output and ***must*** be floated in an actual application. This pin must be attached to an isolated pad with no trace. There is the possibility that the device may be modified and have this lead clipped at the body of the package.

POWER SUPPLY PINS

V_{DD}
Positive Power Supply (Pin 14)

This pin supplies power to the main CMOS digital portion of the device. The voltage range is + 4.5 to + 5.5 V with respect to the GND pin.

For optimum performance, V_{DD} should be bypassed to GND using a low–inductance capacitor mounted very close to these pins. Lead lengths on the capacitor should be minimized.

V_{CC}
Positive Power Supply (Pin 12)

This pin supplies power to the RF amp and 64/65 prescaler. The voltage range is + 4.5 to + 5.5 V with respect to the GND pin. In the standby mode, the V_{CC} pin still draws a few milliamps from the power supply. This current drain can be eliminated with the use of transistor Q1 as shown in Figure 22.

For optimum performance, V_{CC} should be bypassed to GND using a low–inductance capacitor mounted very close to these pins. Lead lengths on the capacitor should be minimized.

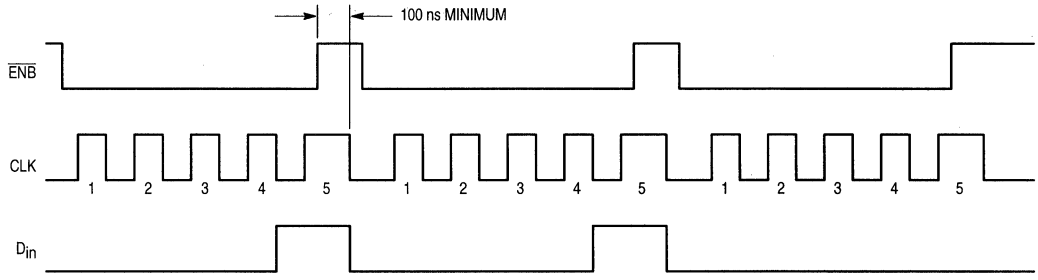
V_{PD}
Positive Power Supply (Pin 5)

This pin supplies power to both phase/frequency detectors A and B. The voltage applied on this pin must be no less than the potential applied to the V_{DD} pin. The maximum voltage can be +9.5 V with respect to the GND pin for the MC145200 and +5.5 V for the MC145201.

For optimum performance, V_{PD} should be bypassed to GND using a low–inductance capacitor mounted very close to these pins. Lead lengths on the capacitor should be minimized.

GND
Ground (Pin 7)

Common ground.



NOTE: It may not be convenient to control the $\overline{ENB}$ or CLK pins during power up per the Pin Descriptions. If this is the case, the part may be initialized through the serial port as shown in the figure above. The sequence is similar to accessing the registers except that the CLK must remain high at least 100 ns after $\overline{ENB}$ is brought high. Note that 3 groups of 5 bits are needed.

Figure 13. Initializing the PLL through the Serial Port

MC145200
Nominal PD_{out} Spurious Current vs f_R Frequency
(1 V < PD_{out} < V_{PD} – 1V)

f_R (kHz)	Current (RMS nA)
10	1.6
20	5.3
50	22
100	95
200	320

MC145201
Nominal PD_{out} Spurious Current vs f_R Frequency
(1 V < PD_{out} < V_{PD} – 1V)

f_R (kHz)	Current (RMS nA)
10	3.6
20	4.6
50	17
100	75
200	244

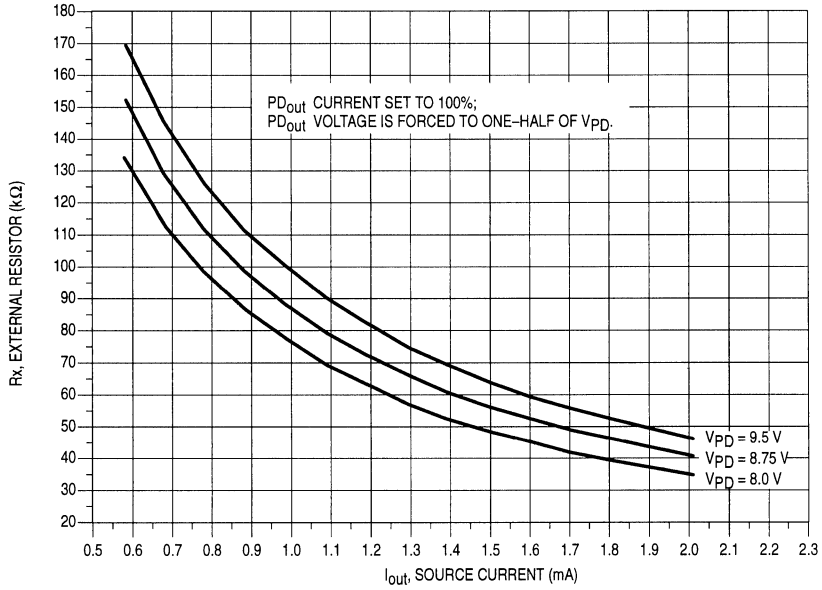
NOTE: For information on spurious current measurement see AN1253/D, "An Improved PLL Design Method Without ω_n and ζ".

Table 2. PD_{out} Current, C1 = Low with OUTPUT A *NOT* Selected as "Port"; Also, Default Mode When OUTPUT A Selected as "Port"

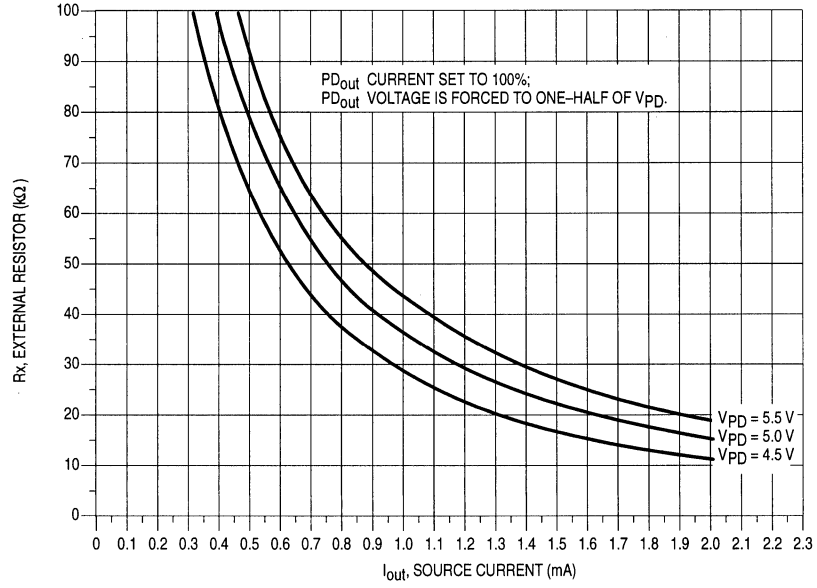
C3	C2	PD_{out} Current
0	0	70%
0	1	80%
1	0	90%
1	1	100%

Table 3. PD_{out} Current, C1 = High with OUTPUT A *NOT* Selected as "Port"

C3	C2	PD_{out} Current
0	0	25%
0	1	50%
1	0	75%
1	1	100%



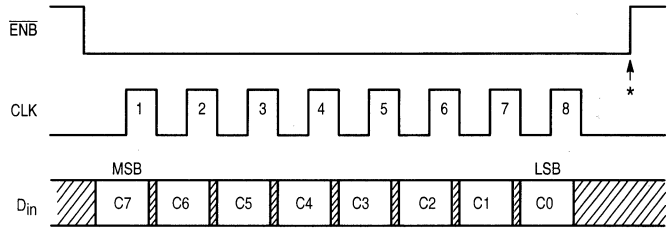
Nominal MC145200 PD_{out} Source Current vs Rx Resistance



Nominal MC145201 PD_{out} Source Current vs Rx Resistance

NOTE: The MC145201 is optimized for Rx values in the 18 kΩ to 40 kΩ range. For example, to achieve 0.3 mA of output current, it is preferable to use a 30–kΩ resistor for Rx and bit settings for 25% (as shown in Table 3).

Figure 14.



* At this point, the new byte is transferred to the C register and stored. No other registers are affected.

2

C7 — POL: Selects the output polarity of the phase/frequency detectors. When set high, this bit inverts the polarity of PD_{out} and interchanges the ϕ_R function with ϕ_V as depicted in Figure 18. Also see the phase detector output pin descriptions for more information. This bit is cleared low at power up.

C6 — PDA/B: Selects which phase/frequency detector is to be used. When set high, enables the output of phase/frequency detector A (PD_{out}) and disables phase/frequency detector B by forcing ϕ_R and ϕ_V to the static high state. When cleared low, phase/frequency detector B is enabled (ϕ_R and ϕ_V) and phase/frequency detector A is disabled with PD_{out} forced to the high–impedance state. This bit is cleared low at power up.

C5 — LDE: Enables the lock detector output (LD) when set high. When the bit is cleared low, the LD output is forced to a static low level. This bit is cleared low at power up.

C4 — STBY: When set high, places the CMOS section of device, which is powered by the V_{DD} and V_{PD} pins, in the standby mode for reduced power consumption: PD_{out} is forced to the high–impedance state, ϕ_R and ϕ_V are forced high, the A, N, and R counters are inhibited from counting, and the Rx current is shut off. In standby, the state of LD is determined by bit C5. C5 low forces LD low (no change). C5 high forces LD static high. During standby, data is retained in the A, R, and C registers. The condition of REF/OSC circuitry is determined by the control bits in the R register: R13, R14, and R15. However, if REF_{out} = static low is selected, the internal feedback resistor is disconnected and the input is inhibited when in standby; in addition, the REF_{in} input only presents a capacitive load. NOTE: Standby does not affect the other modes of the REF/OSC circuitry.

When C4 is reset low, the part is taken out of standby in 2 steps. First, the REF_{in} (only in one mode) resistor is reconnected, all counters are enabled, and the Rx current is enabled. Any f_R and f_V signals are inhibited from toggling the phase/frequency detectors and lock detector. Second, when the first f_V pulse occurs, the R counter is jam loaded, and the phase/frequency and lock detectors are initialized. Immediately after the jam load, the A, N, and R counters begin counting down together. At this point, the f_R and f_V pulses are enabled to the phase and lock detectors. (Patented feature.)

C3, C2 — I2, I1: Controls the PD_{out} source/sink current per Tables 2 and 3. With both bits high, the maximum current (as set by Rx per Figure 14) is available. Also, see C1 bit description.

C1 — Port: When the OUTPUT A pin is selected as "Port" via bits A22 and A23, C1 determines the state of OUTPUT A. When C1 is set high, OUTPUT A is forced high; C1 low forces OUTPUT A low. When OUTPUT A is NOT selected as "Port," C1 controls whether the PD_{out} step size is 10% or 25%. (See Tables 2 and 3.) When low, steps are 10%. When high, steps are 25%. Default is 10% steps when OUTPUT A is selected as "Port." The Port bit is not affected by the standby mode.

C0 — Out B: Determines the state of OUTPUT B. When C0 is set high, OUTPUT B is high–impedance; C0 low forces OUTPUT B low. The Out B bit is not affected by the standby mode. This bit is cleared low at power up.

Figure 15. C Register Access and Format (8 Clock Cycles are Used)

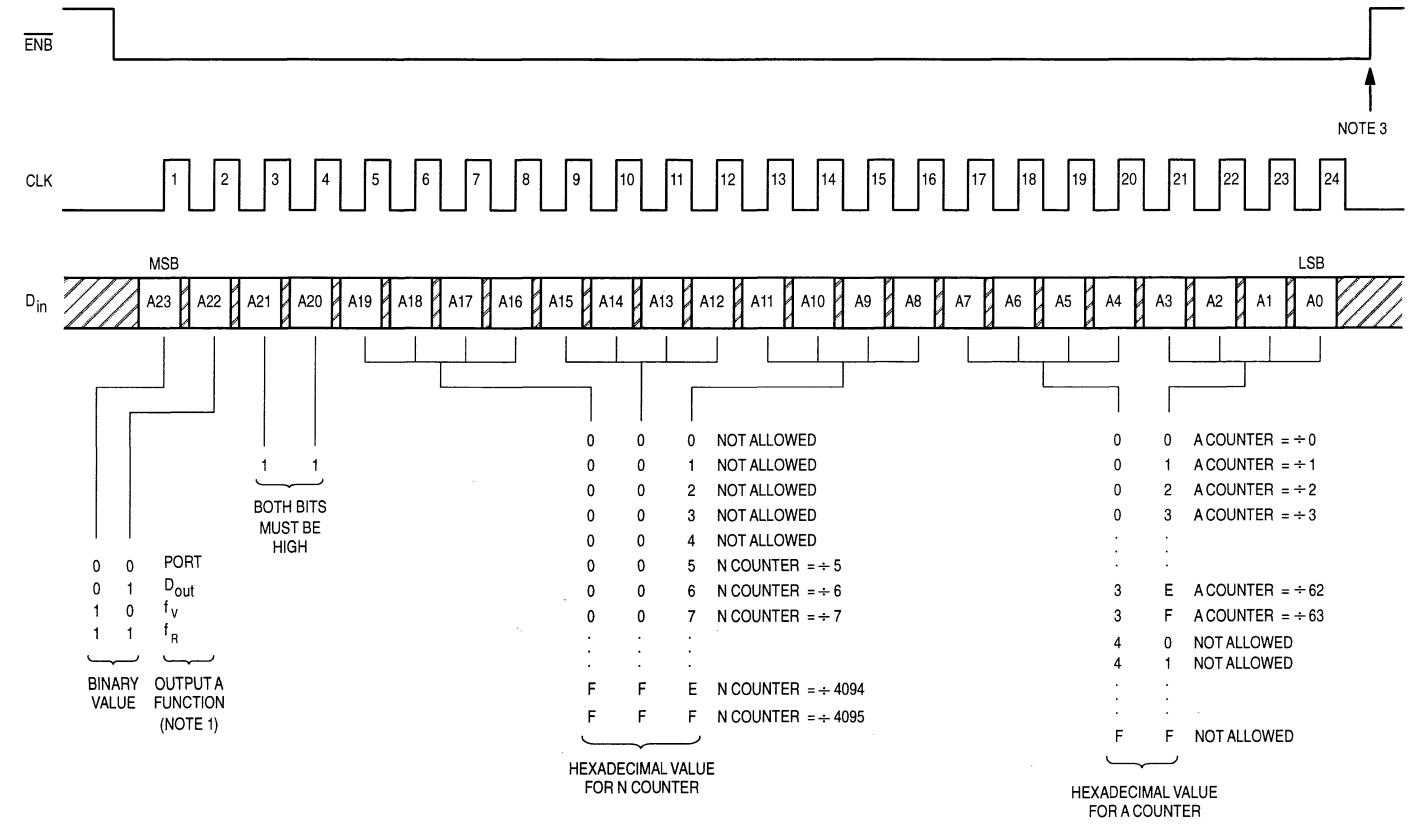
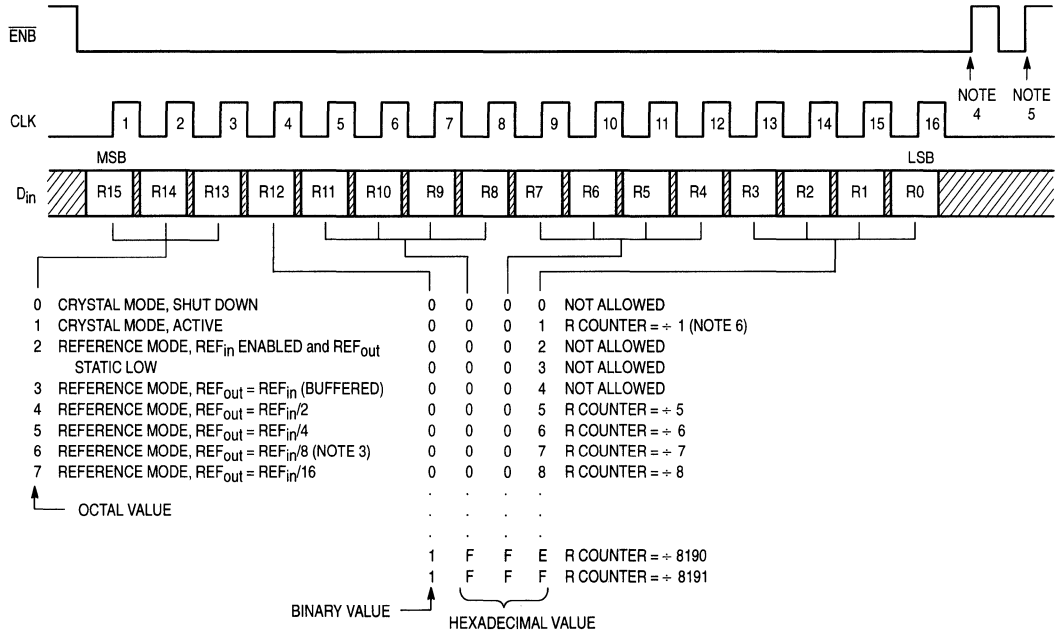


Figure 16. A Register Access and Format (24 Clock Cycles are Used)

NOTES:

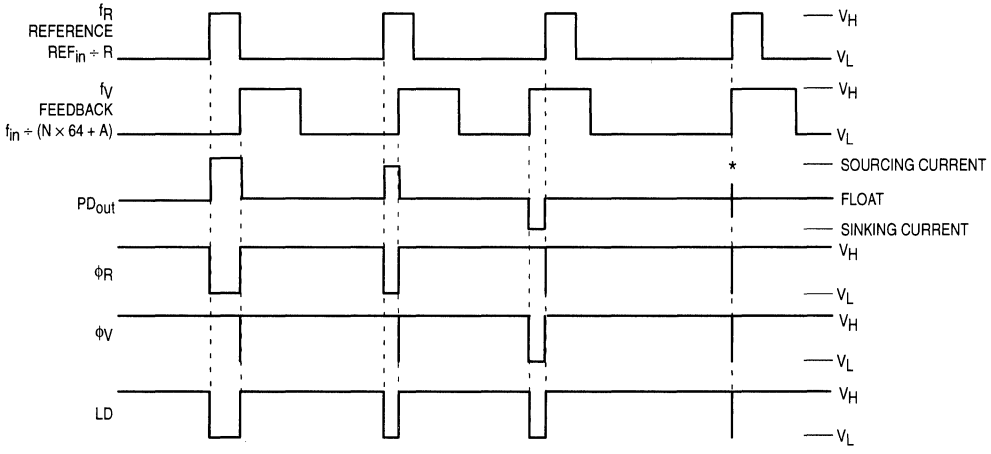
1. A power-on initialize circuit forces the OUTPUT A function to default to Data Out.
2. The values programmed for the N counter must be greater than or equal to the values programmed for the A counter. This results in a total divide value = N x 64 + A.
3. At this point, the three new bytes are transferred to the A register. In addition, the 13 LSBs in the first buffer of the R register are transferred to the R register's second buffer. Thus, the R, N, and A counters can be presented new divide ratios at the same time. The first buffer of the R register is not affected. The C register is not affected.



NOTES:

1. Bits R15 through R13 control the configurable "OSC or 4–stage divider" block (see Block Diagram).
2. Bits R12 through R0 control the "13–stage R counter" block (see Block Diagram).
3. A power–on initialize circuit forces a default REF_{in} to REF_{out} ratio of eight.
4. At this point, bits R13, R14, and R15 are stored and sent to the "OSC or 4–Stage Divider" block in the Block Diagram. Bits R0 through R12 are loaded into the first buffer in the double–buffered section of the R register. Therefore, the R counter divide ratio is not altered yet and retains the previous ratio loaded. The C and A registers are not affected.
5. At this point, bits R0 through R12 are transferred to the second buffer of the R register. The R counter begins dividing by the new ratio after completing the rest of the present count cycle. CLK must be low during the $\overline{ENB}$ pulse, as shown. Also, see note 3 of Figure 16 for an alternate method of loading the second buffer in the R register. The C and A registers are not affected. The first buffer of the R register is not affected.
6. Allows direct access to reference input of phase/frequency detectors.

Figure 17. R Register Access and Format (16 Clock Cycles Are Used)



V_H = High voltage level
V_L = Low voltage level
*At this point, when both f_R and f_V are in phase, the output source and sink circuits are turned on for a short interval.
NOTE: The PD_{out} either sources or sinks current during out–of–lock conditions. When locked in phase and frequency, the output is high impedance and the voltage at that pin is determined by the low–pass filter capacitor. PD_{out}, ϕR, and ϕV are shown with the polarity bit (POL) = low; see Figure 14 for POL.

Figure 18. Phase/Frequency Detectors and Lock Detector Output Waveforms

DESIGN CONSIDERATIONS

CRYSTAL OSCILLATOR CONSIDERATIONS

The following options may be considered to provide a reference frequency to Motorola's CMOS frequency synthesizers.

Use of a Hybrid Crystal Oscillator

Commercially available temperature–compensated crystal oscillators (TCXOs) or crystal–controlled data clock oscillators provide very stable reference frequencies. An oscillator capable of CMOS logic levels at the output may be direct or dc coupled to REF_{in}. If the oscillator does not have CMOS logic levels on the outputs, capacitive or ac coupling to REF_{in} may be used (see Figure 8).

For additional information about TCXOs and data clock oscillators, please consult the latest version of the *eem Electronic Engineers Master Catalog,* the *Gold Book,* or similar publications.

Design an Off–Chip Reference

The user may design an off–chip crystal oscillator using discrete transistors or ICs specifically developed for crystal oscillator applications, such as the MC12061 MECL device. The reference signal from the MECL device is ac coupled to REF_{in} (see Figure 8). For large amplitude signals (standard CMOS logic levels), dc coupling may be used.

Use of the On–Chip Oscillator Circuitry

The on–chip amplifier (a digital inverter) along with an appropriate crystal may be used to provide a reference source frequency. A fundamental mode crystal, parallel resonant at the desired operating frequency, should be connected as shown in Figure 19.

The crystal should be specified for a loading capacitance (C_L) which does not exceed approximately 20 pF when used at the highest operating frequency of 15 MHz. Assuming R1 = 0 Ω, the shunt load capacitance (C_L) presented across the crystal can be estimated to be:

$$C_L = \frac{C_{in}C_{out}}{C_{in}+C_{out}} + C_a + C_{stray} + \frac{C1 \cdot C2}{C1 + C2}$$

where

C_{in} = 5 pF (see Figure 20)
C_{out} = 6 pF (see Figure 20)
C_a = 1 pF (see Figure 20)

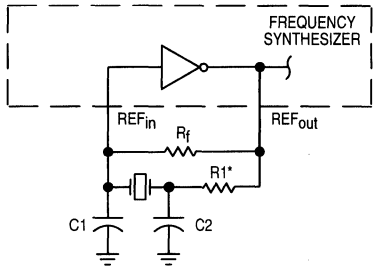
C1 and C2 = external capacitors (see Figure 19)
C_{stray} = the total equivalent external circuit stray capacitance appearing across the crystal terminals

The oscillator can be "trimmed" on–frequency by making a portion or all of C1 variable. The crystal and associated components must be located as close as possible to the REF_{in} and REF_{out} pins to minimize distortion, stray capacitance, stray inductance, and startup stabilization time. Circuit stray capacitance can also be handled by adding the appropriate stray value to the values for C_{in} and C_{out}. For this approach, the term C_{stray} becomes 0 in the above expression for C_L.

Power is dissipated in the effective series resistance of the crystal, R_e, in Figure 21. The maximum drive level specified by the crystal manufacturer represents the maximum stress that the crystal can withstand without damage or excessive shift in operating frequency. R1 in Figure 19 limits the drive level. The use of R1 is not necessary in most cases.

To verify that the maximum dc supply voltage does not cause the crystal to be overdriven, monitor the output frequency (f_R) at OUTPUT A as a function of supply voltage. (REF_{out} is not used because loading impacts the oscillator.) The frequency should increase very slightly as the dc supply voltage is increased. An overdriven crystal decreases in frequency or becomes unstable with an increase in supply voltage. The operating supply voltage must be reduced or R1 must be increased in value if the overdriven condition exists. The user should note that the oscillator start–up time is proportional to the value of R1.

Through the process of supplying crystals for use with CMOS inverters, many crystal manufacturers have developed expertise in CMOS oscillator design with crystals. Discussions with such manufacturers can prove very helpful (see Table 4).



* May be needed in certain cases. See text.

Figure 19. Pierce Crystal Oscillator Circuit

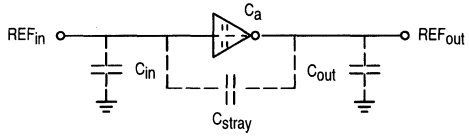
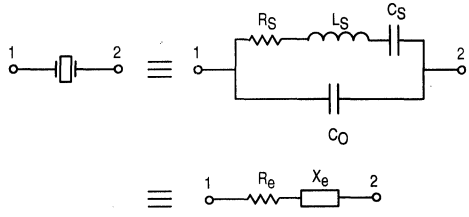


Figure 20. Parasitic Capacitances of the Amplifier and C_{stray}



NOTE: Values are supplied by crystal manufacturer (parallel resonant crystal).

Figure 21. Equivalent Crystal Networks

RECOMMENDED READING

Technical Note TN–24, Statek Corp.

Technical Note TN–7, Statek Corp.

E. Hafner, "The Piezoelectric Crystal Unit–Definitions and Method of Measurement", *Proc. IEEE,* Vol. 57, No. 2, Feb. 1969.

D. Kemper, L. Rosine, "Quartz Crystals for Frequency Control", *Electro–Technology,* June 1969.

P. J. Ottowitz, "A Guide to Crystal Selection", *Electronic Design,* May 1966.

D. Babin, "Designing Crystal Oscillators", *Machine Design,* March 7, 1985.

D. Babin, "Guidelines for Crystal Oscillator Design", *Machine Design,* April 25, 1985.

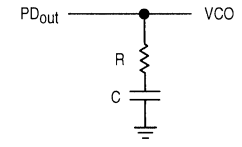
Table 4. Partial List of Crystal Manufacturers

Name	Address	Phone
United States Crystal Corp.	3605 McCart Ave., Ft. Worth, TX 76110	(817) 921–3013
Crystek Crystal	2351 Crystal Dr., Ft. Myers, FL 33907	(813) 936–2109
Statek Corp.	512 N. Main St., Orange, CA 92668	(714) 639–7810
Fox Electronics	5570 Enterprise Parkway, Ft. Myers, FL 33905	(813) 693–0099

NOTE: Motorola cannot recommend one supplier over another and in no way suggests that this is a complete listing of crystal manufacturers.

PHASE–LOCKED LOOP — LOW–PASS FILTER DESIGN

(A)



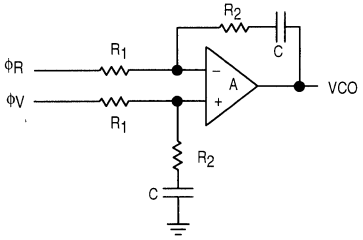
$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NC}}$$

$$\zeta = \frac{R}{2}\sqrt{\frac{K_\phi K_{VCO} C}{N}} = \frac{\omega_n RC}{2}$$

$$Z(s) = \frac{1 + sRC}{sC}$$

NOTE:
For (A), using K_ϕ in amps per radian with the filter's impedance transfer function, Z(s), maintains units of volts per radian for the detector/filter combination. Additional sideband filtering can be accomplished by adding a capacitor C′ across R. The corner $\omega_c = 1/RC'$ should be chosen such that ω_n is not significantly affected.

(B)



$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NCR_1}}$$

$$\zeta = \frac{\omega_n R_2 C}{2}$$

ASSUMING GAIN A IS VERY LARGE, THEN:

$$F(s) = \frac{R_2 sC + 1}{R_1 sC}$$

NOTE:
For (B), R_1 is frequently split into two series resistors; each resistor is equal to R_1 divided by 2. A capacitor C_C is then placed from the midpoint to ground to further filter the error pulses. The value of C_C should be such that the corner frequency of this network does not significantly affect ω_n.

* The ϕ_R and ϕ_V outputs are fed to an external combiner/loop filter. The ϕ_R and ϕ_V outputs swing rail–to–rail. Therefore, the user should be careful not to exceed the common mode input range of the op amp used in the combiner/loop filter.

DEFINITIONS:
N = Total Division Ratio in Feedback Loop
K_ϕ (Phase Detector Gain) = $I_{PDout}/2\pi$ amps per radian for PD_{out}
K_ϕ (Phase Detector Gain) = $V_{PD}/2\pi$ volts per radian for ϕ_V and ϕ_R

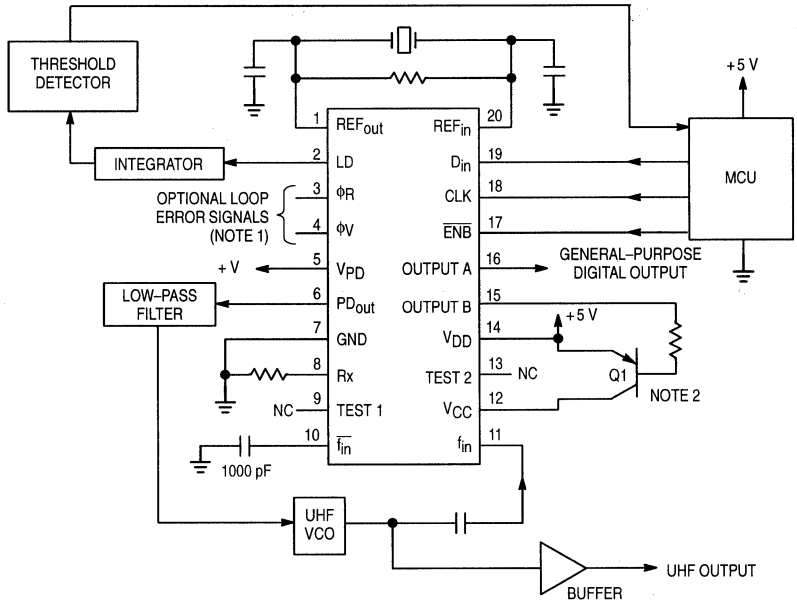
K_{VCO} (VCO Transfer Function) = $\frac{2\pi\Delta f_{VCO}}{\Delta V_{VCO}}$ radians per volt

For a nominal design starting point, the user might consider a damping factor $\zeta \approx 0.7$ and a natural loop frequency $\omega_n \approx (2\pi f_R/50)$ where f_R is the frequency at the phase detector input. Larger ω_n values result in faster loop lock times and, for similar sideband filtering, higher f_R–related VCO sidebands.

Either loop filter (A) or (B) is frequently followed by additional sideband filtering to further attenuate f_R–related VCO sidebands. This additional filtering may be active or passive.

RECOMMENDED READING:

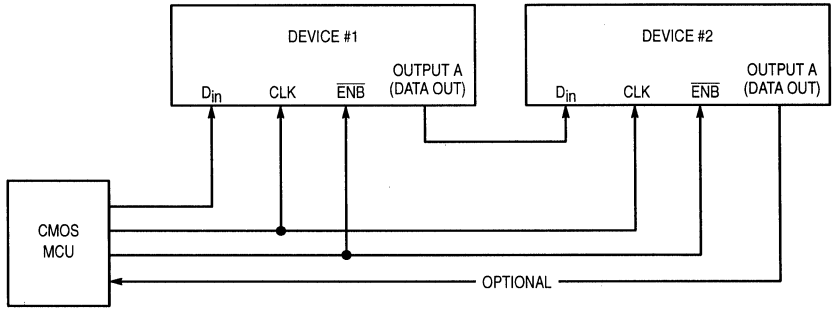
Gardner, Floyd M., *Phaselock Techniques (second edition).* New York, Wiley–Interscience, 1979.
Manassewitsch, Vadim, *Frequency Synthesizers: Theory and Design (second edition).* New York, Wiley–Interscience, 1980.
Blanchard, Alain, *Phase–Locked Loops: Application to Coherent Receiver Design.* New York, Wiley–Interscience, 1976.
Egan, William F., *Frequency Synthesis by Phase Lock.* New York, Wiley–Interscience, 1981.
Rohde, Ulrich L., *Digital PLL Frequency Synthesizers Theory and Design.* Englewood Cliffs, NJ, Prentice–Hall, 1983.
Berlin, Howard M., *Design of Phase–Locked Loop Circuits, with Experiments.* Indianapolis, Howard W. Sams and Co., 1978.
Kinley, Harold, *The PLL Synthesizer Cookbook.* Blue Ridge Summit, PA, Tab Books, 1980.
Seidman, Arthur H., *Integrated Circuits Applications Handbook*, Chapter 17, pp. 538–586. New York, John Wiley & Sons.
Fadrhons, Jan, "Design and Analyze PLLs on a Programmable Calculator," *EDN.* March 5, 1980.
AN535, Phase–Locked Loop Design Fundamentals, Motorola Semiconductor Products, Inc., 1970.
AR254, Phase–Locked Loop Design Articles, Motorola Semiconductor Products, Inc., Reprinted with permission from *Electronic Design,* 1987.
AN1253/D, An Improved PLL Design Method Without ω_n and ζ, Motorola Semiconductor Products, Inc., 1995.



NOTES:

1. When used, the ϕ_R and ϕ_V outputs are fed to an external combiner/loop filter. See the Phase–Locked Loop — Low–Pass Filter Design page for additional information.
2. Transistor Q1 is required only if the standby feature is needed. Q1 permits the bipolar section of the device to be shut down via use of the general–purpose digital pin, OUTPUT B. If the standby feature is not needed, tie Pin 12 directly to the power supply.
3. For optimum performance, bypass the V_{CC}, V_{DD}, and V_{PD} pins to GND with low–inductance capacitors.
4. The R counter is programmed for a divide value = REF_{in}/f_R. Typically, f_R is the tuning resolution required for the VCO. Also, the VCO frequency divided by $f_R = N_T = N \times 64 + A$; this determines the values (N, A) that must be programmed into the N and A counters, respectively.

Figure 22. Example Application



NOTE: See related Figures 24 through 26; these bit streams apply to the MC145190, MC145191, MC145200, and MC145201.

Figure 23. Cascading Two Devices

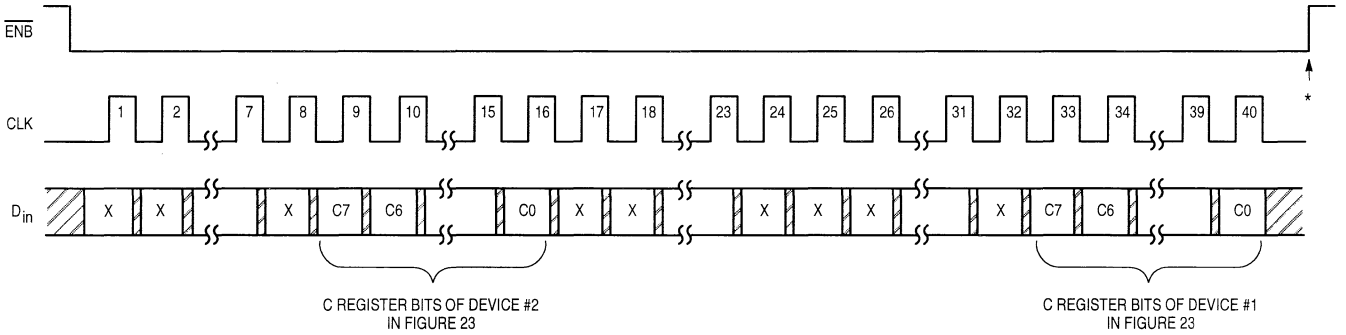


Figure 24. Accessing the C Registers of Two Cascaded Devices

*At this point, the new bytes are transferred to the C registers of both devices and stored. No other registers are affected.

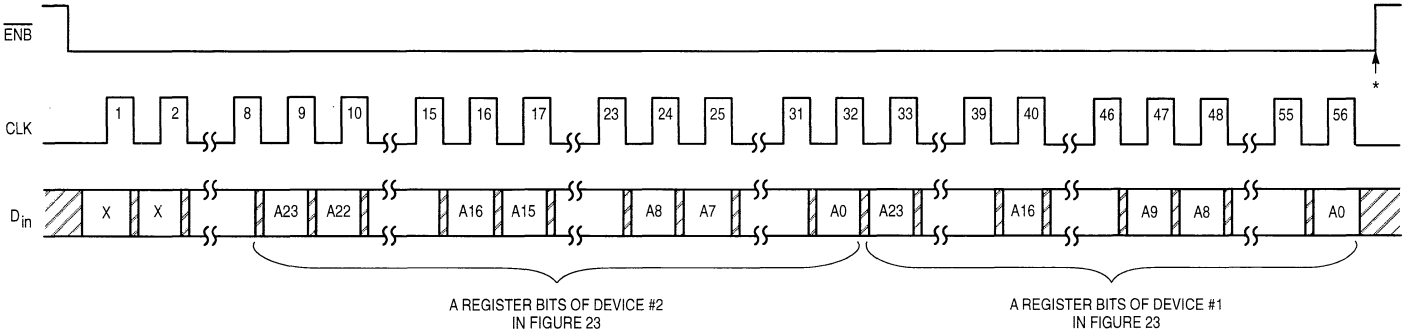


Figure 25. Accessing the A Registers of Two Cascaded Devices

*At this point, the new bytes are transferred to the A registers of both devices and stored. Additionally, for both devices, the 13 LSBs in each of the first buffers of the R registers are transferred to the respective R register's second buffer. Thus, the R, N, and A counters can be presented new divide ratios at the same time. The first buffer of each R register is not affected. Neither C register is affected.

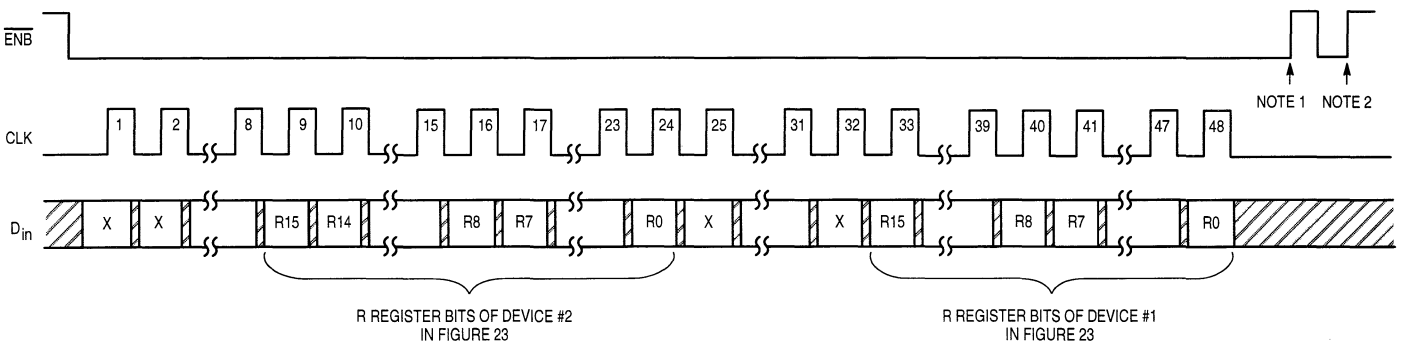


Figure 26. Accessing the R Registers of Two Cascaded Devices

NOTES APPLICABLE TO EACH DEVICE:

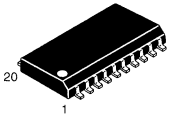
1. At this point, bits R13, R14, and R15 are stored and sent to the "OSC or 4-Stage Divider" block in the Block Diagram. Bits R0 through R12 are loaded into the first buffer in the double-buffered section of the R register. Therefore, the R counter divide ratio is not altered yet and retains the previous ratio loaded. The C and A registers are not affected.
2. At this point, the bits R0 through R12 are transferred to the second buffer of the R register. The R counter begins dividing by the new ratio after completing the rest of the present count cycle. CLK must be low during the $\overline{\text{ENB}}$ pulse, as shown. Also, see note of Figure 25 for an alternate method of loading the second buffer in the R register. The C and A registers are not affected. The first buffer of the R register is not affected.

MC145202

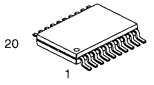
Advance Information

Low-Voltage 2.0 GHz PLL Frequency Synthesizer

Includes On–Board 64/65 Prescaler



F SUFFIX
SOG PACKAGE
CASE 751J

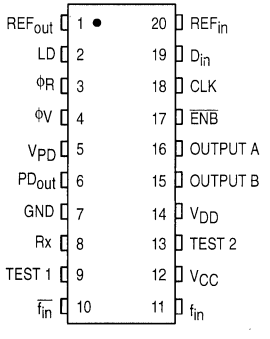


DT SUFFIX
TSSOP
CASE 948D

ORDERING INFORMATION

MC145202F	SOG Package
MC145202DT	TSSOP

PIN ASSIGNMENT



The MC145202 is a low–voltage single–package synthesizer with serial interface capable of direct usage up to 2.0 GHz.

The counters are programmed via a synchronous serial port which is SPI compatible. The serial port is byte-oriented to facilitate control via an MCU. Due to the innovative BitGrabber Plus™ registers, the MC145202 may be cascaded with other peripherals featuring BitGrabber Plus without requiring leading dummy bits or address bits in the serial data stream. In addition, BitGrabber Plus peripherals may be cascaded with existing BitGrabber™ peripherals.

The device features a single–ended current source/sink phase detector A output and a double–ended phase detector B output. Both phase detectors have linear transfer functions (no dead zones). The maximum current of the single–ended phase detector output is determined by an external resistor tied from the Rx pin to ground. This current can be varied via the serial port.

Slew–rate control is provided by a special driver designed for the REF_{out} pin. This minimizes interference caused by REF_{out}.

This part includes a differential RF input that may be operated in a single–ended mode. Also featured are on–board support of an external crystal and a programmable reference output. The R, A, and N counters are fully programmable. The C register (configuration register) allows the part to be configured to meet various applications. A patented feature allows the C register to shut off unused outputs, thereby minimizing system noise and interference.

In order to have consistent lock times and prevent erroneous data from being loaded into the counters, on–board circuitry synchronizes the update of the A register if the A or N counters are loading. Similarly, an update of the R register is synchronized if the R counter is loading.

The double–buffered R register allows new divide ratios to be presented to the three counters (R, A, and N) simultaneously.

- Maximum Operating Frequency: 2000 MHz @ – 10 dBm
- Operating Supply Current: 4 mA Nominal at 3.0 V
- Operating Supply Voltage Range (V_{DD} and V_{CC} Pins): 2.7 to 5.5 V
- Operating Supply Voltage Range of Phase Detectors (V_{PD} Pin): 2.7 to 5.5 V
- Current Source/Sink Phase Detector Output Capability: 1.7 mA @ 5.0 V
  1.0 mA @ 3.0 V
- Gain of Current Source/Sink Phase/Frequency Detector Controllable via Serial Port
- Operating Temperature Range: – 40 to + 85°C
- R Counter Division Range: 1 and 5 to 8191
- Dual–Modulus Capability Provides Total Division up to 262,143
- High–Speed Serial Interface: 4 Mbps
- OUTPUT A Pin, When Configured as Data Out, Permits Cascading of Devices
- Two General–Purpose Digital Outputs — OUTPUT A: Totem–Pole (Push–Pull) with Four Output Modes
  OUTPUT B: Open–Drain
- Patented Power–Saving Standby Feature with Orderly Recovery for Minimizing Lock Times, Standby Current: 30 μA

This document contains information on a new product. Specifications and information herein are subject to change without notice.

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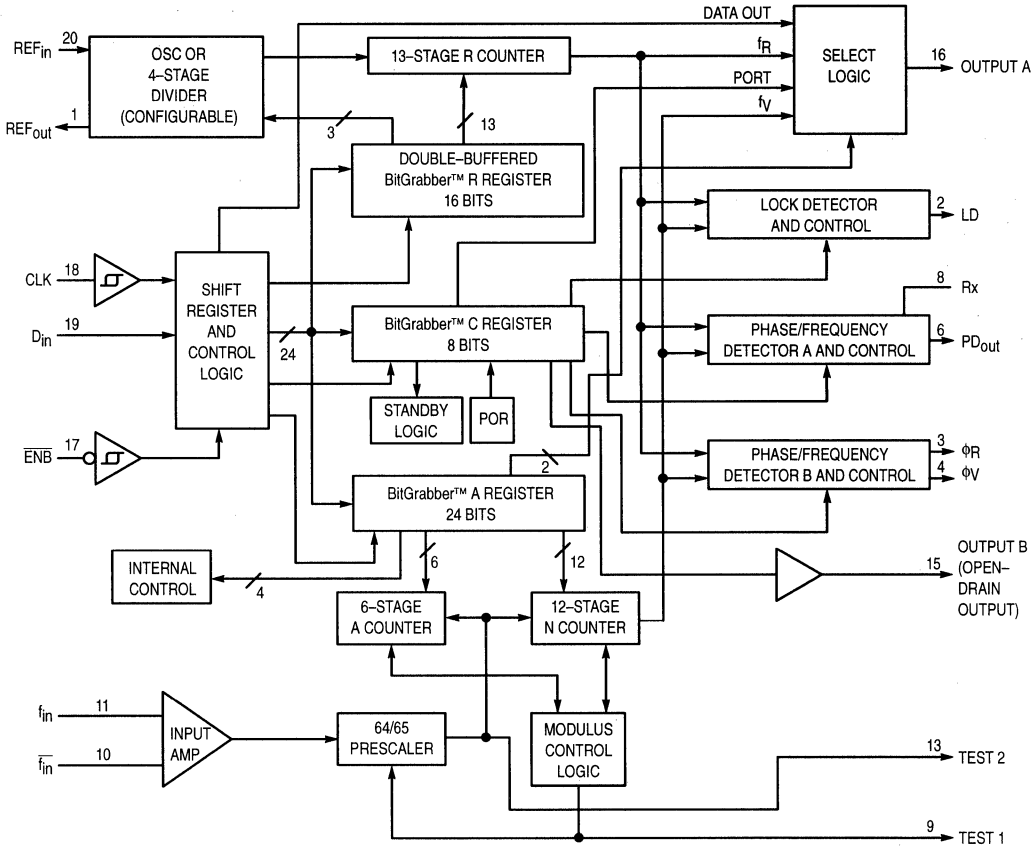
REV 2
10/95

BLOCK DIAGRAM



SUPPLY CONNECTIONS:

PIN 12 = V_{CC} (V+ TO INPUT AMP AND 64/65 PRESCALER)
PIN 5 = V_{PD} (V+ TO PHASE/FREQUENCY DETECTORS A AND B)
PIN 14 = V_{DD} (V+ TO BALANCE OF CIRCUIT)
PIN 7 = GND (COMMON GROUND)

MAXIMUM RATINGS* (Voltages Referenced to GND, unless otherwise stated)

Symbol	Parameter	Value	Unit
V_{CC}, V_{DD}	DC Supply Voltage (Pins 12 and 14)	– 0.5 to + 6.0	V
V_{PD}	DC Supply Voltage (Pin 5)	V_{DD} – 0.5 to + 6.0	V
V_{in}	DC Input Voltage	– 0.5 to V_{DD} + 0.5	V
V_{out}	DC Output Voltage (except OUTPUT B, PD_{out}, ϕ_R, ϕ_V)	– 0.5 to V_{DD} + 0.5	V
V_{out}	DC Output Voltage (OUTPUT B, PD_{out}, ϕ_R, ϕ_V)	– 0.5 to V_{PD} + 0.5	V
I_{in}, I_{PD}	DC Input Current, per Pin (Includes V_{PD})	± 10	mA
I_{out}	DC Output Current, per Pin	± 20	mA
I_{DD}	DC Supply Current, V_{DD} and GND Pins	± 30	mA
P_D	Power Dissipation, per Package	300	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds	260	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Descriptions section.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit.

2

ELECTRICAL CHARACTERISTICS

(V_{DD} = V_{CC} = 2.7 to 5.5 V, Voltages Referenced to GND, unless otherwise stated; V_{PD} = 2.7 to 5.5 V, T_A = – 40 to 85°C)

Symbol	Parameter	Test Condition	Guaranteed Limit	Unit
V_{IL}	Maximum Low–Level Input Voltage (D_{in}, CLK, $\overline{ENB}$)		0.3 x V_{DD}	V
V_{IH}	Minimum High–Level Input Voltage (D_{in}, CLK, $\overline{ENB}$)		0.7 x V_{DD}	V
V_{Hys}	Minimum Hysteresis Voltage (CLK, $\overline{ENB}$)	V_{DD} = 2.7 V V_{DD} = 4.5 V	100 250	mV
V_{OL}	Maximum Low–Level Output Voltage (REF_{out}, OUTPUT A)	I_{out} = 20 µA, Device in Reference Mode	0.1	V
V_{OH}	Minimum High–Level Output Voltage (REF_{out}, OUTPUT A)	I_{out} = – 20 µA, Device in Reference Mode	V_{DD} – 0.1	V
I_{OL}	Minimum Low–Level Output Current (REF_{out}, LD)	V_{out} = 0.3 V	0.36	mA
I_{OL}	Minimum Low–Level Output Current (ϕ_R, ϕ_V)	V_{out} = 0.3 V	0.36	mA
I_{OL}	Minimum Low–Level Output Current (OUTPUT A)	V_{out} = 0.4 V V_{DD} = 4.5 V	1.0	mA
I_{OL}	Minimum Low–Level Output Current (OUTPUT B)	V_{out} = 0.4 V	1.0	mA
I_{OH}	Minimum High–Level Output Current (REF_{out}, LD)	V_{out} = V_{DD} – 0.3 V	– 0.36	mA
I_{OH}	Minimum High–Level Output Current (ϕ_R, ϕ_V)	V_{out} = V_{PD} – 0.3 V	– 0.36	mA
I_{OH}	Minimum High–Level Output Current (OUTPUT A Only)	V_{out} = V_{DD} – 0.4 V V_{DD} = 4.5 V	– 0.6	mA

(continued)

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Condition	Guaranteed Limit	Unit
I_{in}	Maximum Input Leakage Current (D_{in}, CLK, $\overline{ENB}$, REF_{in})	$V_{in} = V_{DD}$ or GND, Device in XTAL Mode	± 1.0	μA
I_{in}	Maximum Input Current (REF_{in})	$V_{in} = V_{DD}$ or GND, Device in Reference Mode	± 100	μA
I_{OZ}	Maximum Output Leakage Current (PD_{out})	$V_{out} = V_{PD}$ or GND, Output in Floating State	± 130	nA
	(OUTPUT B)	$V_{out} = V_{PD}$ or GND, Output in High–Impedance State	± 1	μA
I_{STBY}	Maximum Standby Supply Current (V_{DD} + V_{PD} Pins)	$V_{in} = V_{DD}$ or GND; Outputs Open; Device in Standby Mode, Shut–Down Crystal Mode or REF_{out}–Static–Low Reference Mode; OUTPUT B Controlling V_{CC} per Figure 21	30	μA
I_{PD}	Maximum Phase Detector Quiescent Current (V_{PD} Pin)	Bit C6 = High Which Selects Phase Detector A, PD_{out} = Open, PD_{out} = Static State, Bit C4 = Low Which is ***not*** Standby, I_{Rx} = 170 μA, V_{PD} = 5.5 V	750	μA
		Bit C6 = Low Which Selects Phase Detector B, ϕ_R and ϕ_V = Open, ϕ_R and ϕ_V = Static Low or High, Bit C4 = Low Which is ***not*** Standby	30	
I_T	Total Operating Supply Current (V_{DD} + V_{PD} + V_{CC} Pins)	f_{in} = 2.0 GHz; REF_{in} = 13 MHz @ 1 Vp–p; OUTPUT A = Inactive and No Connect; $V_{DD} = V_{CC}$, REF_{out}, ϕ_V, ϕ_R, PD_{out}, LD = No Connect; D_{in}, $\overline{ENB}$, CLK = V_{DD} or GND, Phase Detector B Selected (Bit C6 = Low)	*	mA

* The nominal values are:
4 mA at V_{DD} = 3.0 V and V_{PD} = 3.0 V
6 mA at V_{DD} = 5.0 V and V_{PD} = 5.0 V
These are not guaranteed limits.

ANALOG CHARACTERISTICS — CURRENT SOURCE/SINK OUTPUT — PD_{out}

($I_{out} \leq$ 1 mA @ V_{DD} = 2.7 V and $I_{out} \leq$ 1.7mA @ $V_{DD} \geq$ 4.5 V, $V_{DD} = V_{CC}$ = 2.7 to 5.5 V, Voltages Referenced to GND)

Parameter	Test Condition	V_{PD}	Guaranteed Limit	Unit
Maximum Source Current Variation (Part–to–Part)	V_{out} = 0.5 x V_{PD}	2.7	± 15	%
		4.5	± 15	
		5.5	± 15	
Maximum Sink–vs–Source Mismatch (Note 3)	V_{out} = 0.5 x V_{PD}	2.7	11	%
		4.5	11	
		5.5	11	
Output Voltage Range (Note 3)	I_{out} Variation ≤ 15%	2.7	0.5 to 2.2	V
	I_{out} Variation ≤ 20%	4.5	0.5 to 3.7	
	I_{out} Variation ≤ 22%	5.5	0.5 to 4.7	

NOTES:
1. Percentages calculated using the following formula: (Maximum Value – Minimum Value)/Maximum Value.
2. See Rx Pin Description for external resistor values.
3. This parameter is guaranteed for a given temperature within – 40 to + 85°C.

AC INTERFACE CHARACTERISTICS

(V_{DD} = V_{CC} = 2.7 to 5.5 V, T_A = – 40 to + 85°C, C_L = 25 pF, Input t_r = t_f = 10 ns; V_{PD} = 2.7 to 5.5 V)

Symbol	Parameter	Figure No.	Guaranteed Limit	Unit
f_{clk}	Serial Data Clock Frequency (Note: Refer to Clock t_w below)	1	dc to 4.0	MHz
t_{PLH}, t_{PHL}	Maximum Propagation Delay, CLK to OUTPUT A (Selected as Data Out)	1, 5	100	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay, $\overline{ENB}$ to OUTPUT A (Selected as Port)	2, 5	150	ns
t_{PZL}, t_{PLZ}	Maximum Propagation Delay, $\overline{ENB}$ to OUTPUT B	2, 6	150	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, OUTPUT A and OUTPUT B; t_{THL} only, on OUTPUT B	1, 5, 6	50	ns
C_{in}	Maximum Input Capacitance – D_{in}, $\overline{ENB}$, CLK		10	pF

TIMING REQUIREMENTS

(V_{DD} = V_{CC} = 2.7 to 5.5 V, T_A = – 40 to + 85°C, Input t_r = t_f = 10 ns, unless otherwise indicated)

Symbol	Parameter	Figure No.	Guaranteed Limit	Unit
t_{su}, t_h	Minimum Setup and Hold Times, D_{in} vs CLK	3	50	ns
t_{su}, t_h, t_{rec}	Minimum Setup, Hold and Recovery Times, $\overline{ENB}$ vs CLK	4	100	ns
t_w	Minimum Pulse Width, $\overline{ENB}$	4	*	cycles
t_w	Minimum Pulse Width, CLK	1	125	ns
t_r, t_f	Maximum Input Rise and Fall Times, CLK	1	100	µs

* The minimum limit is 3 REF_{in} cycles or 195 f_{in} cycles, whichever is greater.

SWITCHING WAVEFORMS

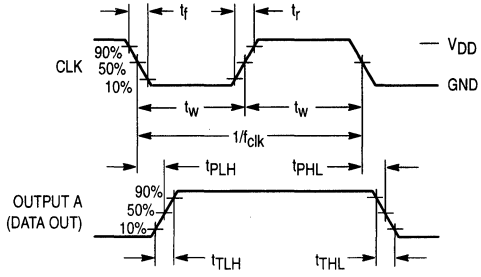


Figure 1.

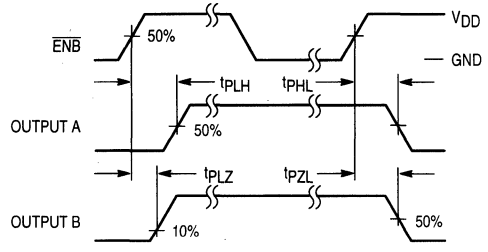


Figure 2.

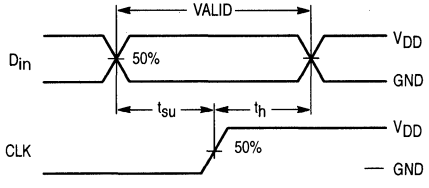


Figure 3.

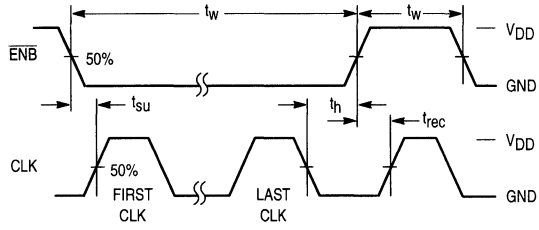
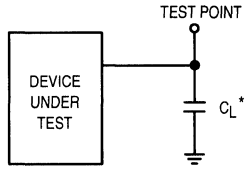
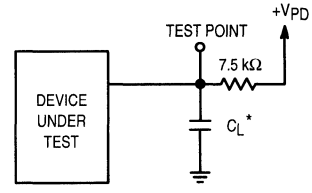


Figure 4.



* Includes all probe and fixture capacitance.

Figure 5.



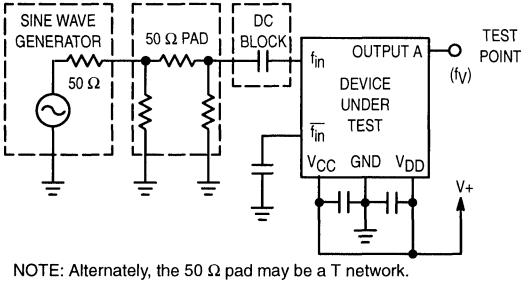
* Includes all probe and fixture capacitance.

Figure 6.

LOOP SPECIFICATIONS (V_{DD} = V_{CC} = 2.7 to 5.5 V unless otherwise indicated, T_A = – 40 to + 85°C)

Symbol	Parameter	Test Condition	Fig. No.	Guaranteed Operating Range		Unit
				Min	Max	
P_{in}	Input Sensitivity Range, f_{in}	500 MHz ≤ f_{in} ≤ 2000 MHz	7	– 10	4	dBm*
f_{ref}	Input Frequency, REF_{in} Externally Driven in Reference Mode	V_{in} ≥ 400 mV p–p 2.7 ≤ V_{DD} < 4.5 V 4.5 ≤ V_{DD} ≤ 5.5 V	8	1.5 1.5	20 30	MHz
f_{XTAL}	Crystal Frequency, Crystal Mode	C1 ≤ 30 pF, C2 ≤ 30 pF, Includes Stray Capacitance	9	2	15	MHz
f_{out}	Output Frequency, REF_{out}	C_L = 20 pF, V_{out} ≥ 1 V p–p	10, 12	dc	10	MHz
f	Operating Frequency of the Phase Detectors			dc	2	MHz
t_w	Output Pulse Width (ϕ_R, ϕ_V, and LD)	f_R in Phase with f_V, C_L = 20 pF, ϕ_R and ϕ_V active for LD measurement, ** V_{PD} = 2.7 to 5.5 V V_{DD} = 2.7 V V_{DD} = 4.5 V V_{DD} = 5.5 V	11, 12	 40 18 14	 120 60 50	ns
t_{TLH}, t_{THL}	Output Transition Times (LD, ϕ_V, and ϕ_R)	C_L = 20 pF, V_{PD} = 2.7 V, V_{DD} = V_{CC} = 2.7 V	11, 12	—	80	ns
C_{in}	Input Capacitance, REF_{in}			—	7	pF

* Power level at the input to the dc block.
** When PD_{out} is active, LD minimum pulse width is approximately 5 ns.



NOTE: Alternately, the 50 Ω pad may be a T network.

Figure 7. Test Circuit

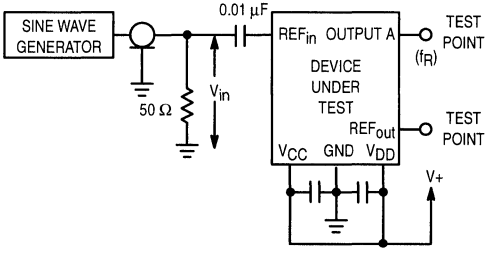


Figure 8. Test Circuit — Reference Mode

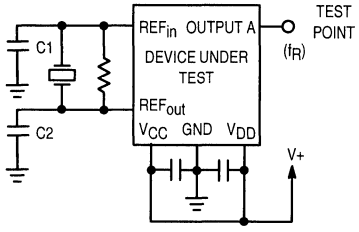


Figure 9. Test Circuit — Crystal Mode

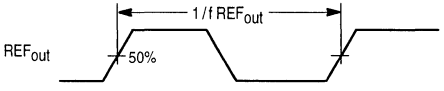


Figure 10. Switching Waveform

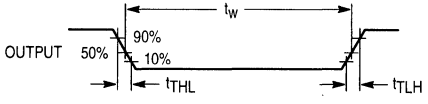


Figure 11. Switching Waveform

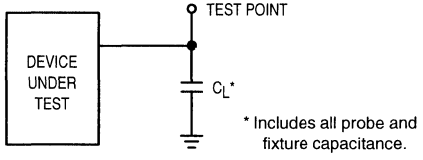


Figure 12. Test Circuit

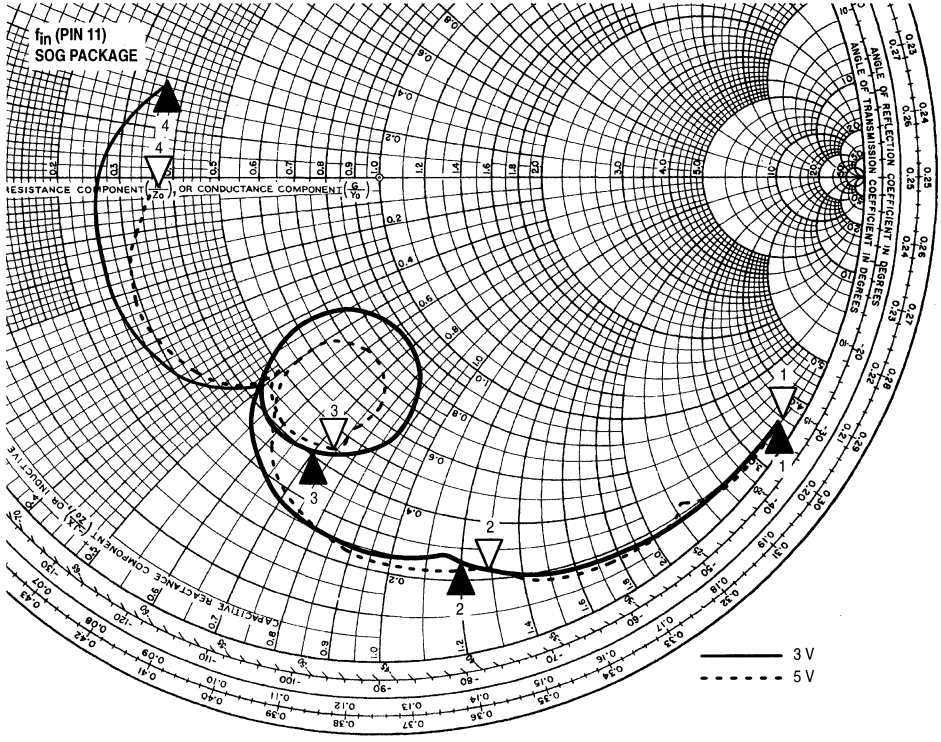


Figure 13. Normalized Input Impedance at f_{in} — Series Format (R + jx)

Table 5. Input Impedence at f_{in} — Series Format (R + jx), V_{CC} = 3 V

Marker	Frequency (GHz)	Resistance (Ω)	Reactance (Ω)	Capacitance
1	0.5	11.4	– 168	1.9 pF
2	1	12.4	– 59.4	2.68 pF
3	1.5	19.8	– 34.9	3.04 pF
4	2	18.1	9.43	751 pH

Table 6. Input Impedence at f_{in} — Series Format (R + jx), V_{CC} = 5 V

Marker	Frequency (GHz)	Resistance (Ω)	Reactance (Ω)	Capacitance
1	0.5	11.8	–175	1.82 pF
2	1	11.5	– 64.4	2.47 pF
3	1.5	22.2	– 36.5	2.91 pF
4	2	18.4	1.14	90.4 pH

PIN DESCRIPTIONS

DIGITAL INTERFACE PINS

D_{in}
Serial Data Input (Pin 19)

The bit stream begins with the most significant bit (MSB) and is shifted in on the low–to–high transition of CLK. The bit pattern is 1 byte (8 bits) long to access the C or configuration register, 2 bytes (16 bits) to access the first buffer of the R register, or 3 bytes (24 bits) to access the A register (see Table 7). The values in the C, R, and A registers do not change during shifting because the transfer of data to the registers is controlled by $\overline{ENB}$.

CAUTION

The value programmed for the N counter must be greater than or equal to the value of the A counter.

The 13 least significant bits (LSBs) of the R register are double–buffered. As indicated above, data is latched into the first buffer on a 16–bit transfer. (The 3 MSBs are not double–buffered and have an immediate effect after a 16–bit transfer.) The second buffer of the R register contains the 13 bits for the R counter. This second buffer is loaded with the contents of the first buffer when the A register is loaded (a 24–bit transfer). This allows presenting new values to the R, A, and N counters simultaneously. If this is not required, then the 16–bit transfer may be followed by pulsing $\overline{ENB}$ low with no signal on the CLK pin. This is an alternate method of transferring data to the second buffer of the R register (see Figure 16).

The bit stream needs neither address nor steering bits due to the innovative BitGrabber Plus registers. Therefore, all bits in the stream are available to be data for the three registers. Random access of any register is provided (i.e., the registers may be accessed in any sequence). Data is retained in the registers over a supply range of 2.7 to 5.5 V. The formats are shown in Figures 14, 15, and 16.

D_{in} typically switches near 50% of V_{DD} to maximize noise immunity. This input can be directly interfaced to CMOS devices with outputs guaranteed to switch near rail–to–rail. When interfacing to NMOS or TTL devices, either a level shifter (MC74HC14A, MC14504B) or pull–up resistor of 1 kΩ to 10 kΩ must be used. Parameters to consider when sizing the resistor are worst–case I_{OL} of the driving device, maximum tolerable power consumption, and maximum data rate.

Table 7. Register Access
(MSBs are shifted in first; C0, R0, and A0 are the LSBs)

Number of Clocks	Accessed Register	Bit Nomenclature
8	C Register	C7, C6, C5, . . ., C0
16	R Register	R15, R14, R13, . . ., R0
24	A Register	A23, A22, A21, . . ., A0
Other Values ≤ 32	Not Allowed	
Values > 32	See Figures 22 – 25	

CLK
Serial Data Clock Input (Pin 18)

Low–to–high transitions on CLK shift bits available at the D_{in} pin, while high–to–low transitions shift bits from OUTPUT A (when configured as Data Out, see Pin 16). The 24–1/2–stage shift register is static, allowing clock rates down to dc in a continuous or intermittent mode.

Eight clock cycles are required to access the C register. Sixteen clock cycles are needed for the first buffer of the R register. Twenty–four cycles are used to access the A register. See Table 7 and Figures 14, 15, and 16. The number of clocks required for cascaded devices is shown in Figures 23 through 25.

CLK typically switches near 50% of V_{DD} and has a Schmitt–triggered input buffer. Slow CLK rise and fall times are allowed. See the last paragraph of **D_{in}** for more information.

NOTE

To guarantee proper operation of the power–on reset (POR) circuit, the CLK pin must be held at GND (with $\overline{ENB}$ being a don't care) or $\overline{ENB}$ must be held at the potential of the V+ pin (with CLK being a don't care) during power–up. Floating, toggling, or having these pins in the wrong state during power–up does not harm the chip, but causes two potentially undesirable effects. First, the outputs of the device power up in an unknown state. Second, if two devices are cascaded, the A Registers must be written twice after power up. After these two accesses, the two cascaded chips perform normally.

$\overline{ENB}$
Active Low Enable Input (Pin 17)

This pin is used to activate the serial interface to allow the transfer of data to/from the device. When $\overline{ENB}$ is in an inactive high state, shifting is inhibited and the port is held in the initialized state. To transfer data to the device, $\overline{ENB}$ (which must start inactive high) is taken low, a serial transfer is made via D_{in} and CLK, and $\overline{ENB}$ is taken back high. The low–to–high transition on $\overline{ENB}$ transfers data to the C or A registers and first buffer of the R register, depending on the data stream length per Table 7.

Transitions on $\overline{ENB}$ must not be attempted while CLK is high. This puts the device out of synchronization with the microcontroller. Resynchronization occurs when $\overline{ENB}$ is high and CLK is low.

This input is also Schmitt–triggered and switches near 50% of V_{DD}, thereby minimizing the chance of loading erroneous data into the registers. See the last paragraph of **D_{in}** for more information.

For POR information, see the note for the **CLK pin**.

OUTPUT A
Configurable Digital Output (Pin 16)

OUTPUT A is selectable as f_R, f_V, Data Out, or Port. Bits A22 and A23 in the A register control the selection; see Figure 15.

If A23 = A22 = high, OUTPUT A is configured as f_R. This signal is the buffered output of the 13–stage R counter. The f_R signal appears as normally low and pulses high. The f_R signal can be used to verify the divide ratio of the R counter. This ratio extends from 5 to 8191 and is determined by the binary value loaded into bits R0–R12 in the R register. Also, direct access to the phase detectors via the REF_{in} pin is allowed by choosing a divide value of 1 (see Figure 16). The maximum frequency at which the phase detectors operate is 2 MHz. Therefore, the frequency of f_R should not exceed 2 MHz.

If A23 = high and A22 = low, OUTPUT A is configured as f_V. This signal is the buffered output of the 12–stage N counter. The f_V signal appears as normally low and pulses high. The f_V signal can be used to verify the operation of the prescaler, A counter, and N counter. The divide ratio between the f_{in} input and the f_V signal is $N \times 64 + A$. N is the divide ratio of the N counter and A is the divide ratio of the A counter. These ratios are determined by bits loaded into the A register. See Figure 15. The maximum frequency at which the phase detectors operate is 2 MHz. Therefore, the frequency of f_V should not exceed 2 MHz.

If A23 = low and A22 = high, OUTPUT A is configured as Data Out. This signal is the serial output of the 24–1/2–stage shift register. The bit stream is shifted out on the high–to–low transition of the CLK input. Upon power up, OUTPUT A is automatically configured as Data Out to facilitate cascading devices.

If A23 = A22 = low, OUTPUT A is configured as Port. This signal is a general–purpose digital output which may be used as an MCU port expander. This signal is low when the Port bit (C1) of the C register is low, and high when the Port bit is high.

OUTPUT B
Open–Drain Digital Output (Pin 15)

This signal is a general–purpose digital output which may be used as an MCU port expander. This signal is low when the Out B bit (C0) of the C register is low. When the Out B bit is high, OUTPUT B assumes the high–impedance state. OUTPUT B may be pulled up through an external resistor or active circuitry to any voltage less than or equal to the potential of the V_{PD} pin. **Note**: the maximum voltage allowed on the V_{PD} pin is 5.5 V.

Upon power–up, power–on reset circuitry forces OUTPUT B to a low level.

REFERENCE PINS

REF_{in} and REF_{out}
Reference Input and Reference Output (Pins 20 and 1)

Configurable pins for a Crystal or an External Reference. This pair of pins can be configured in one of two modes: the crystal mode or the reference mode. Bits R13, R14, and R15 in the R register control the modes as shown in Figure 16.

In crystal mode, these pins form a reference oscillator when connected to terminals of an external parallel–resonant crystal. Frequency–setting capacitors of appropriate values, as recommended by the crystal supplier, are connected from each of the two pins to ground (up to a maximum of 30 pF each, including stray capacitance). An external resistor of 1 MΩ to 15 MΩ is connected directly across the pins to ensure linear operation of the amplifier. The required connections for the components are shown in Figure 9.

To turn on the oscillator, bits R15, R14, and R13 must have an octal value of one (001 in binary, respectively). This is the active–crystal mode shown in Figure 16. In this mode, the crystal oscillator runs and the R Counter divides the crystal frequency, unless the part is in standby. If the part is placed in standby via the C register, the oscillator runs, but the R counter is stopped. However, if bits R15 to R13 have a value of 0, the oscillator is stopped, which saves additional power. This is the shut–down crystal mode (shown in Figure 16) and can be engaged whether in standby or not.

In the reference mode, REF_{in} (Pin 20) accepts a signal from an external reference oscillator, such as a TCXO. A signal swinging from at least the V_{IL} to V_{IH} levels listed in the Electrical Characteristics table may be directly coupled to the pin. If the signal is less than this level, ac coupling must be used as shown in Figure 8. Due to an on–board resistor which is engaged in the reference modes, an external biasing resistor tied between REF_{in} and REF_{out} is not required.

With the reference mode, the REF_{out} pin is configured as the output of a divider. As an example, if bits R15, R14, and R13 have an octal value of seven, the frequency at REF_{out} is the REF_{in} frequency divided by 16. In addition, Figure 16 shows how to obtain ratios of eight, four, and two. A ratio of one–to–one can be obtained with an octal value of three. Upon power up, a ratio of eight is automatically initialized. The maximum frequency capability of the REF_{out} pin is listed in the Loop Specifications table for an output swing of 1 V p–p and 20 pF loads. Therefore, for higher REF_{in} frequencies, the one–to–one ratio may not be used for this magnitude of signal swing and loading requirements. Likewise, for REF_{in} frequencies above two times the highest rated frequency, the ratio must be more than two.

The output has a special on–board driver that has slew–rate control. This feature minimizes interference in the application.

If REF_{out} is unused, an octal value of two should be used for R15, R14, and R13 and the REF_{out} pin should be floated. A value of two allows REF_{in} to be functional while disabling REF_{out}, which minimizes dynamic power consumption.

LOOP PINS

f_{in} and $\overline{f_{in}}$
Frequency Inputs (Pins 11 and 10)

These pins are frequency inputs from the VCO. These pins feed the on–board RF amplifier which drives the 64/65 prescaler. These inputs may be fed differentially. However, they are usually used in a single–ended configuration (shown in Figure 7). Note that f_{in} is driven while $\overline{f_{in}}$ must be tied to ground via a capacitor.

Motorola does not recommend driving $\overline{f_{in}}$ while terminating f_{in} because this configuration is not tested for sensitivity. The sensitivity is dependent on the frequency as shown in the Loop Specifications table.

PD_{out}
Single–Ended Phase/Frequency Detector Output (Pin 6)

This is a three–state current–source/sink output for use as a loop error signal when combined with an external low–pass filter. The phase/frequency detector is characterized by a linear transfer function. The operation of the phase/frequency detector is described below and is shown in Figure 17.

POL bit (C7) in the C register = low (see Figure 14)
Frequency of $f_V > f_R$ or Phase of f_V Leading f_R: current–sinking pulses from a floating state
Frequency of $f_V < f_R$ or Phase of f_V Lagging f_R: current–sourcing pulses from a floating state
Frequency and Phase of $f_V = f_R$: essentially a floating state; voltage at pin determined by loop filter
POL bit (C7) = high
Frequency of $f_V > f_R$ or Phase of f_V Leading f_R: current–sourcing pulses from a floating state
Frequency of $f_V < f_R$ or Phase of f_V Lagging f_R: current–sinking pulses from a floating state
Frequency and Phase of $f_V = f_R$: essentially a floating state; voltage at pin determined by loop filter

This output can be enabled, disabled, and inverted via the C register. If desired, PD_{out} can be forced to the high–impedance state by utilization of the disable feature in the C register (bit C6). This is a patented feature. Similarly, PD_{out} is forced to the high–impedance state when the device is put into standby (STBY bit C4 = high).

The PD_{out} circuit is powered by V_{PD}. The phase detector gain is controllable by bits C3, C2, and C1: gain (in amps per radian) = PD_{out} current divided by 2π.

ϕ_R and ϕ_V (Pins 3 and 4)
Double–Ended Phase/Frequency Detector Outputs

These outputs can be combined externally to generate a loop error signal. Through use of a Motorola patented technique, the detector's dead zone has been eliminated. Therefore, the phase/frequency detector is characterized by a linear transfer function. The operation of the phase/frequency detector is described below and is shown in Figure 17.

POL bit (C7) in the C register = low (see Figure 14)
Frequency of $f_V > f_R$ or Phase of f_V Leading f_R: ϕ_V = negative pulses, ϕ_R = essentially high
Frequency of $f_V < f_R$ or Phase of f_V Lagging f_R: ϕ_V = essentially high, ϕ_R = negative pulses
Frequency and Phase of $f_V = f_R$: ϕ_V and ϕ_R remain essentially high, except for a small minimum time period when both pulse low in phase
POL bit (C7) = high
Frequency of $f_V > f_R$ or Phase of f_V Leading f_R: ϕ_R = negative pulses, ϕ_V = essentially high
Frequency of $f_V < f_R$ or Phase of f_V Lagging f_R: ϕ_R = essentially high, ϕ_V = negative pulses
Frequency and Phase of $f_V = f_R$: ϕ_V and ϕ_R remain essentially high, except for a small minimum time period when both pulse low in phase

These outputs can be enabled, disabled, and interchanged via C register bits C6 or C4. This is a patented feature. Note that when disabled or in standby, ϕ_R and ϕ_V are forced to their rest condition (high state).

The ϕ_R and ϕ_V output signal swing is approximately from GND to V_{PD}.

LD
Lock Detector Output (Pin 2)

This output is essentially at a high level with narrow low–going pulses when the loop is locked (f_R and f_V of the same phase and frequency). The output pulses low when f_V and f_R are out of phase or different frequencies. LD is the logical ANDing of ϕ_R and ϕ_V (see Figure 17).

This output can be enabled and disabled via the C register. This is a patented feature. Upon power up, on–chip initialization circuitry disables LD to a static low logic level to prevent a false "lock" signal. If unused, LD should be disabled and left open.

The LD output signal swing is approximately from GND to V_{DD}.

Rx
External Resistor (Pin 8)

A resistor tied between this pin and GND, in conjunction with bits in the C register, determines the amount of current that the PD_{out} pin sinks and sources. When bits C2 and C3 are both set high, the maximum current is obtained at PD_{out}; see Tables 8 and 9 for other current values. The recommended value for Rx is 3.9 kΩ. A value of 3.9 kΩ provides current at the PD_{out} pin of approximately 1 mA @ V_{DD} = 3 V and approximately 1.7 mA @ V_{DD} = 5 V in the 100% current mode. Note that V_{DD}, not V_{PD}, is a factor in determining the current.

When the ϕ_R and ϕ_V outputs are used, the Rx pin may be floated.

Table 8. PD_{out} Current*, C1 = Low with OUTPUT A *not* Selected as "Port"; Also, Default Mode When OUTPUT A Selected as "Port"

Bit C3	Bit C2	PD_{out} Current*
0	0	70%
0	1	80%
1	0	90%
1	1	100%

* At the time the data sheet was printed, only the 100% current mode was guaranteed. The reduced current modes were for experimentation only.

Table 9. PD_{out} Current*, C1 = High with OUTPUT A *not* Selected as "Port"

Bit C3	Bit C2	PD_{out} Current*
0	0	25%
0	1	50%
1	0	75%
1	1	100%

* At the time the data sheet was printed, only the 100% current mode was guaranteed. The reduced current modes were for experimentation only.

TEST POINT PINS

TEST 1
Modulus Control Signal (Pin 9)

This pin may be used in conjunction with the Test 2 pin for access to the on–board 64/65 prescaler. When Test 1 is low, the prescaler divides by 65. When high, the prescaler divides by 64.

CAUTION

This pin is an unbuffered output and must be floated in an actual application. This pin must be attached to an isolated pad with no trace. There is the possibility that the final production version of the device will have this lead clipped at the body of the package.

TEST 2
Prescaler Output (Pin 13)

This pin may be used to access the on–board 64/65 prescaler output.

CAUTION

This pin is an unbuffered output and must be floated in an actual application. This pin must be attached to an isolated pad with no trace. There is the possibility that the final production version of the device will have this lead clipped at the body of the package.

POWER SUPPLY PINS

V_{DD}
Positive Power Supply (Pin 14)

This pin supplies power to the main CMOS digital portion of the device. Also, this pin, in conjunction with the Rx resistor, determines the internal reference current for the PD_{out} pin. The voltage range is +2.7 to +5.5 V with respect to the GND pin.

For optimum performance, V_{DD} should be bypassed to GND using a low–inductance capacitor mounted very close to these pins. Lead lengths on the capacitor should be minimized.

V_{CC}
Positive Power Supply (Pin 12)

This pin supplies power to the RF amp and 64/65 prescaler. The voltage range is +2.7 to +5.5 V with respect to the GND pin. In standby mode, the V_{CC} pin still draws a few milliamps from the power supply. This current drain can be eliminated with the use of transistor Q1 as shown in Figure 21.

For optimum performance, V_{CC} should be bypassed to GND using a low–inductance capacitor mounted very close to these pins. Lead lengths on the capacitor should be minimized.

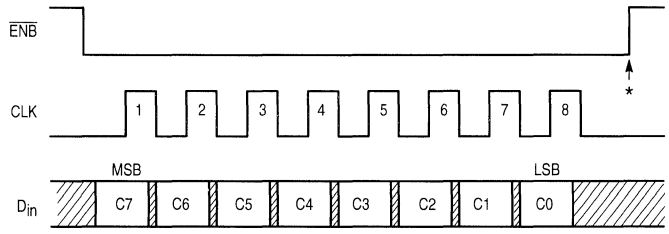
V_{PD}
Positive Power Supply (Pin 5)

This pin supplies power to both phase/frequency detectors A and B. The voltage applied on this pin may be more or less than the potential applied to the V_{DD} and V_{CC} pins. The voltage range for V_{PD} is 2.7 to 5.5 V with respect to the GND pin.

For optimum performance, V_{PD} should be bypassed to GND using a low–inductance capacitor mounted very close to these pins. Lead lengths on the capacitor should be minimized.

GND
Ground (Pin 7)

Common ground.



* At this point, the new byte is transferred to the C register and stored. No other registers are affected.

C7 – POL: Selects the output polarity of the phase/frequency detectors. When set high, this bit inverts PD_{out} and interchanges the ϕ_R function with ϕ_V as depicted in Figure 17. Also see the phase detector output pin descriptions for more information. This bit is cleared low at power up.

C6 – PDA/B: Selects which phase/frequency detector is to be used. When set high, enables the output of phase/frequency detector A (PD_{out}) and disables phase/frequency detector B by forcing ϕ_R and ϕ_V to the static high state. When cleared low, phase/frequency detector B is enabled (ϕ_R and ϕ_V) and phase/frequency detector A is disabled with PD_{out} forced to the high–impedance state. This bit is cleared low at power up.

C5 – LDE: Enables the lock detector output when set high. When the bit is cleared low, the LD output is forced to a static low level. This bit is cleared low at power up.

C4 – STBY: When set, places the CMOS section of device, which is powered by the V_{DD} and V_{PD} pins, in the standby mode for reduced power consumption: PD_{out} is forced to the high–impedance state, ϕ_R and ϕ_V are forced high, the A, N, and R counters are inhibited from counting, and the Rx current is shut off. In standby, the state of LD is determined by bit C5. C5 low forces LD low (no change). C5 high forces LD static high. During standby, data is retained in the A, R, and C registers. The condition of REF/OSC circuitry is determined by the control bits in the R register: R13, R14, and R15. However, if REF_{out} = static low is selected, the internal feedback resistor is disconnected and the input is inhibited when in standby; in addition, the REF_{in} input only presents a capacitive load. NOTE: Standby does not affect the other modes of the REF/OSC circuitry.

When C4 is reset low, the part is taken out of standby in two steps. First, the REF_{in} (only in one mode) resistor is reconnected, all counters are enabled, and the Rx current is enabled. Any f_R and f_V signals are inhibited from toggling the phase/frequency detectors and lock detector. Second, when the first f_V pulse occurs, the R counter is jam loaded, and the phase/frequency and lock detectors are initialized. Immediately after the jam load, the A, N, and R counters begin counting down together. At this point, the f_R and f_V pulses are enabled to the phase and lock detectors. (Patented feature.)

C3, C2 – I2, I1: Controls the PD_{out} source/sink current per Tables 8 and 9. With both bits high, the maximum current is available. Also, see C1 bit description.

C1 – Port: When the OUTPUT A pin is selected as "Port" via bits A22 and A23, C1 determines the state of OUTPUT A. When C1 is set high, OUTPUT A is forced high; C1 low forces OUTPUT A low. When OUTPUT A is ***not*** selected as "Port," C1 controls whether the PD_{out} step size is 10% or 25%. (See Tables 8 and 9.) When low, steps are 10%. When high, steps are 25%. Default is 10% steps when OUTPUT A is selected as "Port." The Port bit is not affected by the standby mode.

C0 – Out B: Determines the state of OUTPUT B. When C0 is set high, OUTPUT B is high–impedance; C0 low forces OUTPUT B low. The Out B bit is not affected by the standby mode. This bit is cleared low at power up.

Figure 14. C Register Access and Format (8 Clock Cycles are Used)

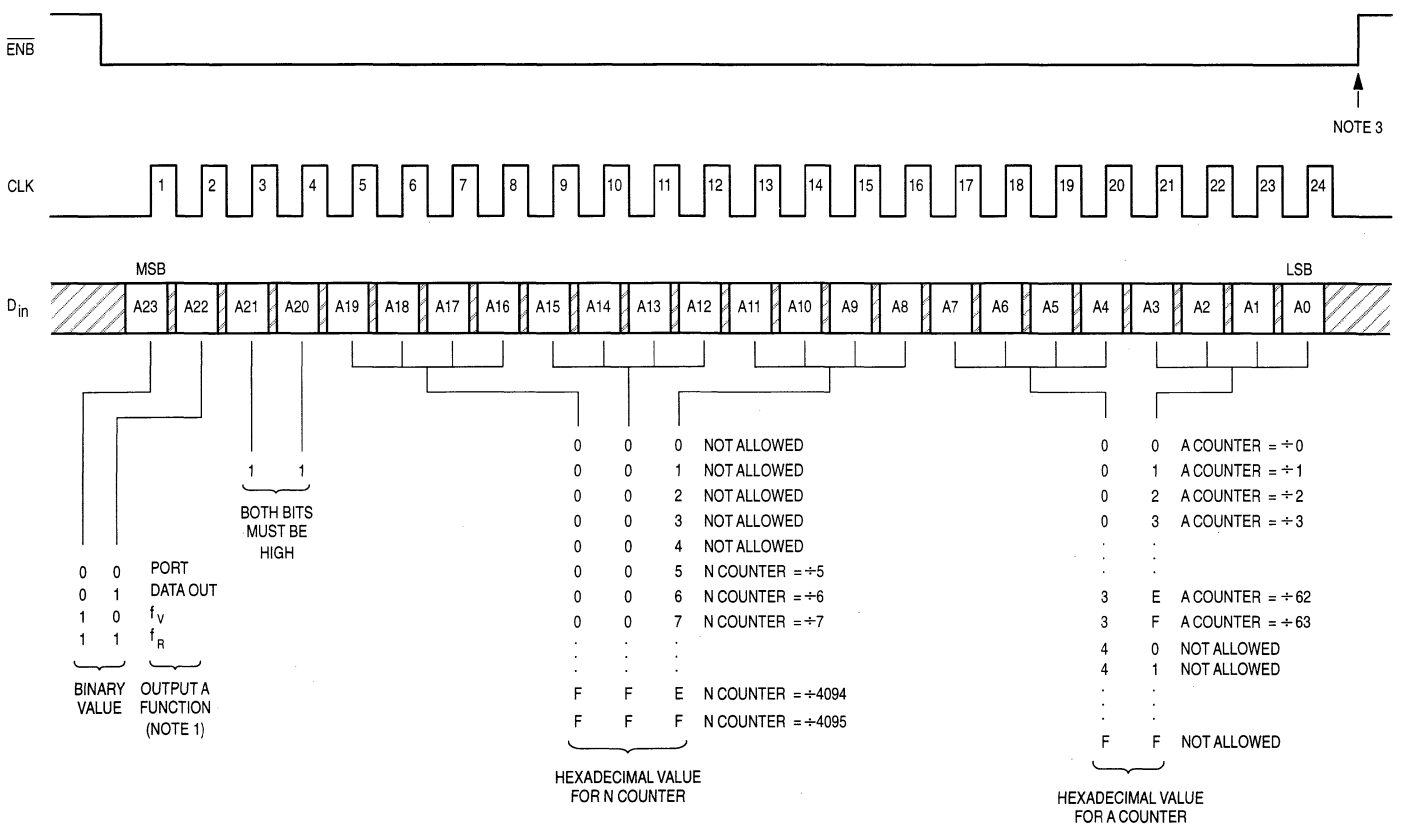
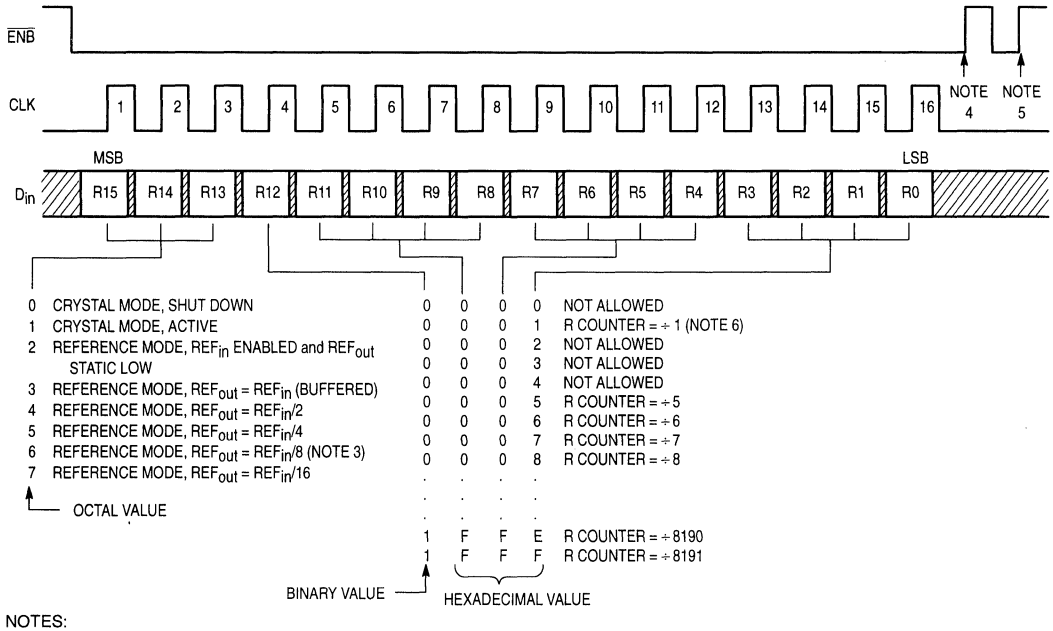


Figure 15. A Register Access and Format (24 Clock Cycles are Used)

NOTES:

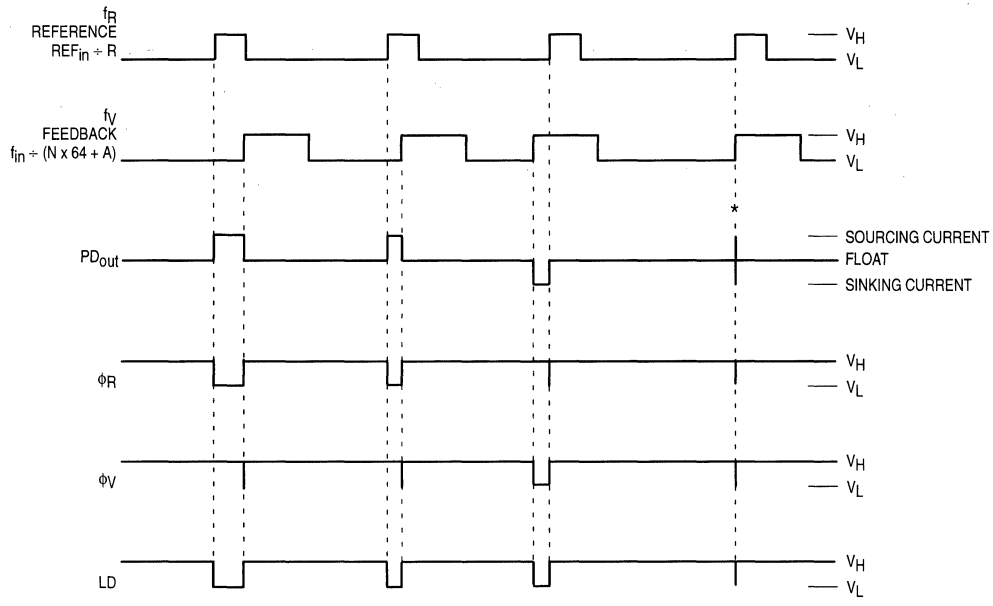
1. A power-on initialize circuit forces the OUTPUT A function to default to Data Out.
2. The values programmed for the N counter must be greater than or equal to the values programmed for the A counter. This results in a total divide value = N x 64 + A.
3. At this point, the three new bytes are transferred to the A register. In addition, the 13 LSBs in the first buffer of the R register are transferred to the R register's second buffer. Thus, the R, N, and A counters can be presented new divide ratios at the same time. The first buffer of the R register is not affected. The C register is not affected.



NOTES:

1. Bits R15 through R13 control the configurable "OSC or 4–stage divider" block (see Block Diagram).
2. Bits R12 through R0 control the "13–stage R counter" block (see Block Diagram).
3. A power–on initialize circuit forces a default REF_{in} to REF_{out} ratio of eight.
4. At this point, bits R13, R14, and R15 are stored and sent to the "OSC or 4–Stage Divider" block in the Block Diagram. Bits R0 – R12 are loaded into the first buffer in the double–buffered section of the R register. Therefore, the R counter divide ratio is not altered yet and retains the previous ratio loaded. The C and A registers are not affected.
5. Optional load pulse. At this point, bits R0 – R12 are transferred to the second buffer of the R register. The R counter begins dividing by the new ratio after completing the rest of the present count cycle. CLK must be low during the $\overline{ENB}$ pulse, as shown. The C and A registers are not affected. The first buffer of the R register is not affected. Also, see note 3 of Figure 15 for an alternate method of loading the second buffer in the R register.
6. Allows direct access to reference input of phase/frequency detectors.

Figure 16. R Register Access and Format (16 Clock Cycles are Used)



V_H = High voltage level
V_L = Low voltage level
*At this point, when both f_R and f_V are in phase, the output source and sink circuits are turned on for a short interval.
NOTE: The PD_{out} either sources or sinks current during out–of–lock conditions. When locked in phase and frequency, the output is in the floating condition and the voltage at that pin is determined by the low–pass filter capacitor. PD_{out}, ϕR, and ϕV are shown with the polarity bit (POL) = low; see Figure 14 for POL.

Figure 17. Phase/Frequency Detectors and Lock Detector Output Waveforms

DESIGN CONSIDERATIONS

CRYSTAL OSCILLATOR CONSIDERATIONS

The following options may be considered to provide a reference frequency to Motorola's CMOS frequency synthesizers.

Use of a Hybrid Crystal Oscillator

Commercially available temperature–compensated crystal oscillators (TCXOs) or crystal–controlled data clock oscillators provide very stable reference frequencies. An oscillator capable of CMOS logic levels at the output may be direct or dc coupled to REF_{in}. If the oscillator does not have CMOS logic levels on the outputs, capacitive or ac coupling to REF_{in} may be used (see Figure 8).

For additional information about TCXOs and data clock oscillators, please consult the latest version of the *eem Electronic Engineers Master Catalog,* the *Gold Book,* or similar publications.

Design an Off–Chip Reference

The user may design an off–chip crystal oscillator using discrete transistors or ICs specifically developed for crystal oscillator applications, such as the MC12061 MECL device. The reference signal from the MECL device is ac coupled to REF_{in} (see Figure 8). For large amplitude signals (standard CMOS logic levels), dc coupling may be used.

Use of the On–Chip Oscillator Circuitry

The on–chip amplifier (a digital inverter) along with an appropriate crystal may be used to provide a reference source frequency. A fundamental mode crystal, parallel resonant at the desired operating frequency, should be connected as shown in Figure 18.

The crystal should be specified for a loading capacitance (C_L) which does not exceed approximately 20 pF when used at the highest operating frequencies listed in the Loop Specifications table. Assuming R1 = 0 Ω, the shunt load capacitance (C_L) presented across the crystal can be estimated to be:

$$C_L = \frac{C_{in}C_{out}}{C_{in} + C_{out}} + C_a + C_{stray} + \frac{C1 \cdot C2}{C1 + C2}$$

where

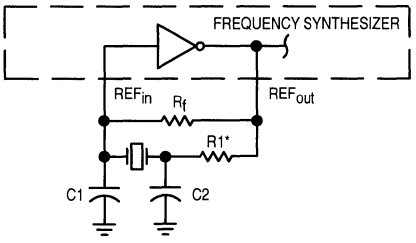
C_{in} = 5 pF (see Figure 19)
C_{out} = 6 pF (see Figure 19)
C_a = 1 pF (see Figure 19)
C1 and C2 = external capacitors (see Figure 18)
C_{stray} = the total equivalent external circuit stray capacitance appearing across the crystal terminals

The oscillator can be "trimmed" on–frequency by making a portion or all of C1 variable. The crystal and associated components must be located as close as possible to the REF_{in} and REF_{out} pins to minimize distortion, stray capacitance, stray inductance, and startup stabilization time. Circuit stray capacitance can also be handled by adding the appropriate stray value to the values for C_{in} and C_{out}. For this approach, the term C_{stray} becomes 0 in the above expression for C_L.

Power is dissipated in the effective series resistance of the crystal, R_e, in Figure 20. The maximum drive level specified by the crystal manufacturer represents the maximum stress that the crystal can withstand without damage or excessive shift in operating frequency. R1 in Figure 18 limits the drive level. The use of R1 is not necessary in most cases.

To verify that the maximum dc supply voltage does not cause the crystal to be overdriven, monitor the output frequency (f_R) at OUTPUT A as a function of supply voltage. (REF_{out} is not used because loading impacts the oscillator.) The frequency should increase very slightly as the dc supply voltage is increased. An overdriven crystal decreases in frequency or becomes unstable with an increase in supply voltage. The operating supply voltage must be reduced or R1 must be increased in value if the overdriven condition exists. The user should note that the oscillator start–up time is proportional to the value of R1.

Through the process of supplying crystals for use with CMOS inverters, many crystal manufacturers have developed expertise in CMOS oscillator design with crystals. Discussions with such manufacturers can prove very helpful (see Table 10).



* May be needed in certain cases. See text.

Figure 18. Pierce Crystal Oscillator Circuit

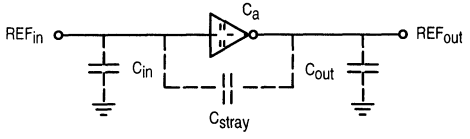
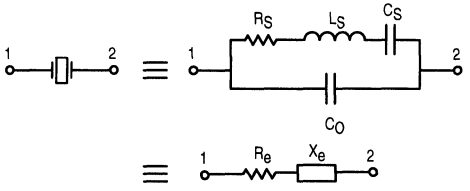


Figure 19. Parasitic Capacitances of the Amplifier and C_{stray}



NOTE: Values are supplied by crystal manufacturer (parallel resonant crystal).

Figure 20. Equivalent Crystal Networks

RECOMMENDED READING

Technical Note TN–24, Statek Corp.

Technical Note TN–7, Statek Corp.

E. Hafner, "The Piezoelectric Crystal Unit–Definitions and Method of Measurement", *Proc. IEEE*, Vol. 57, No. 2, Feb. 1969.

D. Kemper, L. Rosine, "Quartz Crystals for Frequency Control", *Electro–Technology*, June 1969.

P. J. Ottowitz, "A Guide to Crystal Selection", *Electronic Design*, May 1966.

D. Babin, "Designing Crystal Oscillators", *Machine Design*, March 7, 1985.

D. Babin, "Guidelines for Crystal Oscillator Design", *Machine Design*, April 25, 1985.

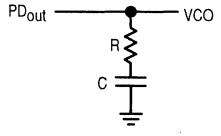
Table 10. Partial List of Crystal Manufacturers

Name	Address	Phone
United States Crystal Corp.	3605 McCart Ave., Ft. Worth, TX 76110	(817) 921–3013
Crystek Crystal	2351 Crystal Dr., Ft. Myers, FL 33907	(813) 936–2109
Statek Corp.	512 N. Main St., Orange, CA 92668	(714) 639–7810
Fox Electronics	5570 Enterprise Parkway, Ft. Myers, FL 33905	(813) 693–0099

NOTE: Motorola cannot recommend one supplier over another and in no way suggests that this is a complete listing of crystal manufacturers.

PHASE–LOCKED LOOP — LOW–PASS FILTER DESIGN

(A)



$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NC}}$$

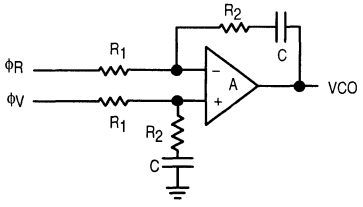
$$\zeta = \frac{R}{2}\sqrt{\frac{K_\phi K_{VCO} C}{N}} = \frac{\omega_n RC}{2}$$

$$Z(s) = \frac{1 + sRC}{sC}$$

NOTE:

For (A), using K_ϕ in amps per radian with the filter's impedance transfer function, Z(s), maintains units of volts per radian for the detector/filter combination. Additional sideband filtering can be accomplished by adding a capacitor C′ across R. The corner $\omega_C = 1/RC'$ should be chosen such that ω_n is not significantly affected.

(B)



$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NCR_1}}$$

$$\zeta = \frac{\omega_n R_2 C}{2}$$

ASSUMING GAIN A IS VERY LARGE, THEN:

$$F(s) = \frac{R_2 sC + 1}{R_1 sC}$$

NOTE:

For (B), R_1 is frequently split into two series resistors; each resistor is equal to R_1 divided by 2. A capacitor C_C is then placed from the midpoint to ground to further filter the error pulses. The value of C_C should be such that the corner frequency of this network does not significantly affect ω_n.

DEFINITIONS:

N = Total Division Ratio in Feedback Loop

K_ϕ (Phase Detector Gain) = $I_{PDout}/2\pi$ amps per radian for PD_{out}

K_ϕ (Phase Detector Gain) = $V_{PD}/2\pi$ volts per radian for ϕ_V and ϕ_R

K_{VCO} (VCO Transfer Function) = $\frac{2\pi\Delta f_{VCO}}{\Delta V_{VCO}}$ radians per volt

For a nominal design starting point, the user might consider a damping factor $\zeta \approx 0.7$ and a natural loop frequency $\omega_n \approx (2\pi f_R/50)$ where f_R is the frequency at the phase detector input. Larger ω_n values result in faster loop lock times and, for similar sideband filtering, higher f_R–related VCO sidebands.

Either loop filter (A) or (B) is frequently followed by additional sideband filtering to further attenuate f_R–related VCO sidebands. This additional filtering may be active or passive.

RECOMMENDED READING:

Gardner, Floyd M., *Phaselock Techniques (second edition).* New York, Wiley–Interscience, 1979.

Manassewitsch, Vadim, *Frequency Synthesizers: Theory and Design (second edition).* New York, Wiley–Interscience, 1980.

Blanchard, Alain, *Phase–Locked Loops: Application to Coherent Receiver Design.* New York, Wiley–Interscience, 1976.

Egan, William F., *Frequency Synthesis by Phase Lock.* New York, Wiley–Interscience, 1981.

Rohde, Ulrich L., *Digital PLL Frequency Synthesizers Theory and Design.* Englewood Cliffs, NJ, Prentice–Hall, 1983.

Berlin, Howard M., *Design of Phase–Locked Loop Circuits, with Experiments.* Indianapolis, Howard W. Sams and Co., 1978.

Kinley, Harold, *The PLL Synthesizer Cookbook.* Blue Ridge Summit, PA, Tab Books, 1980.

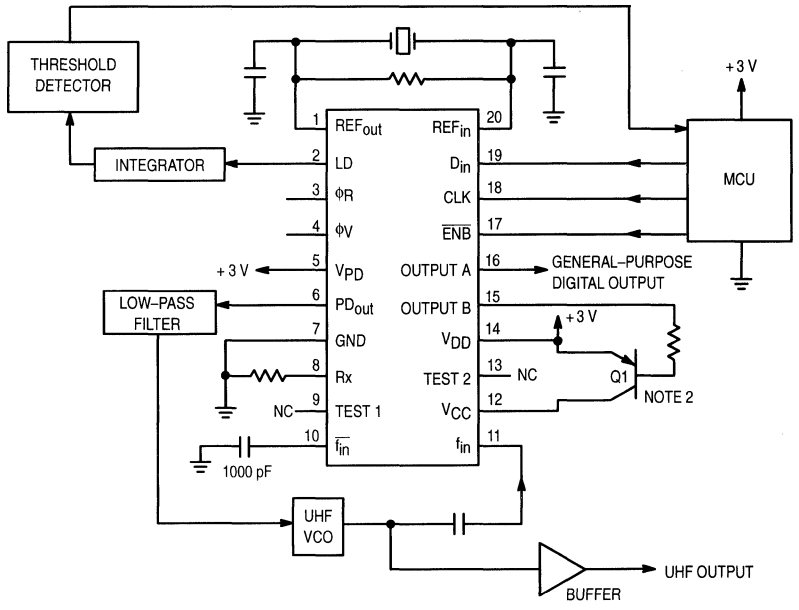
Seidman, Arthur H., *Integrated Circuits Applications Handbook,* Chapter 17, pp. 538–586. New York, John Wiley & Sons.

Fadrhons, Jan, "Design and Analyze PLLs on a Programmable Calculator," *EDN.* March 5, 1980.

AN535, Phase–Locked Loop Design Fundamentals, Motorola Semiconductor Products, Inc., 1970.

AR254, Phase–Locked Loop Design Articles, Motorola Semiconductor Products, Inc., Reprinted with permission from *Electronic Design,* 1987.

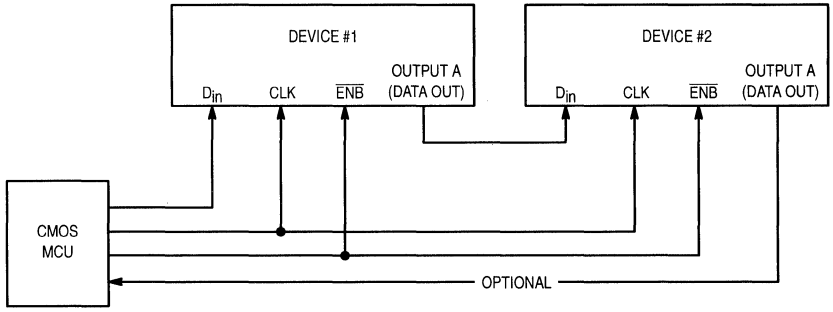
AN1253, An Improved PLL Design Method Without ω_n and ζ, Motorola Semiconductor Products, Inc., 1995.



NOTES:

1. When used, the ϕ_R and ϕ_V outputs are fed to an external combiner/loop filter. See the Phase–Locked Loop — Low–Pass Filter Design page for additional information.
2. Transistor Q1 is required only if the standby feature is needed. Q1 permits the bipolar section of the device to be shut down via use of the general–purpose digital pin, OUTPUT B. If the standby feature is not needed, tie Pin 12 directly to the power supply.
3. For optimum performance, bypass the V_{CC}, V_{DD}, and V_{PD} pins to GND with low–inductance capacitors.
4. The R counter is programmed for a divide value = REF_{in}/f_R. Typically, f_R is the tuning resolution required for the VCO. Also, the VCO frequency divided by $f_R = N_T = N \times 64 + A$; this determines the values (N, A) that must be programmed into the N and A counters, respectively.

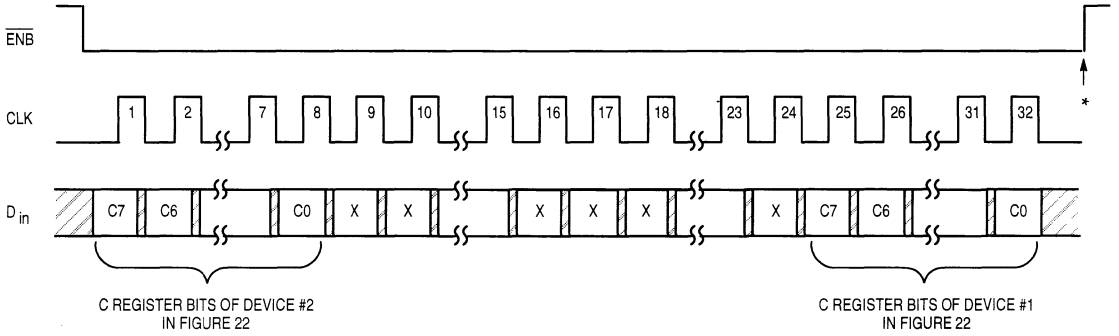
Figure 21. Example Application



NOTE: See related Figures 23, 24, and 25.

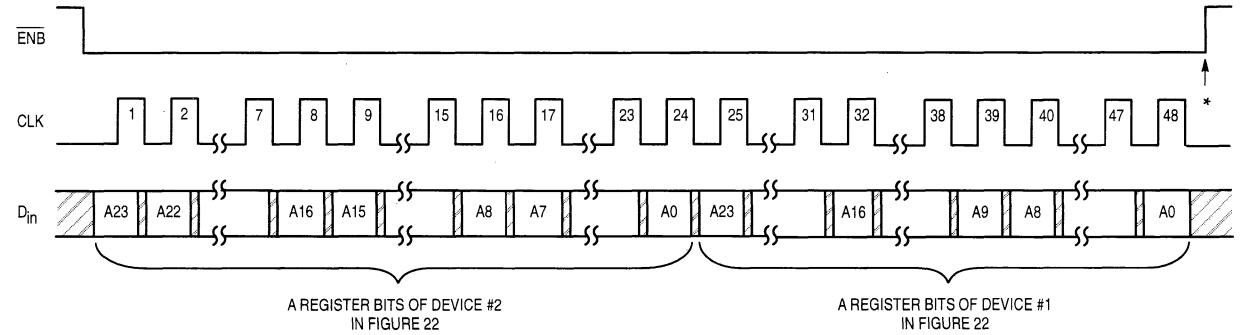
Figure 22. Cascading Two Devices

Figure 23. Accessing the C Registers of Two Cascaded MC145202 Devices



*At this point, the new bytes are transferred to the C registers of both devices and stored. No other registers are affected.

Figure 24. Accessing the A Registers of Two Cascaded MC145202 Devices



* At this point, the new bytes are transferred to the A registers of both devices and stored. Additionally, for both devices, the 13 LSBs in each of the first buffers of the R registers are transferred to the respective R register's second buffer. Thus, the R, N, and A counter can be presented new divide ratios at the same time. The first buffer of each R register is not affected. Neither C register is affected.

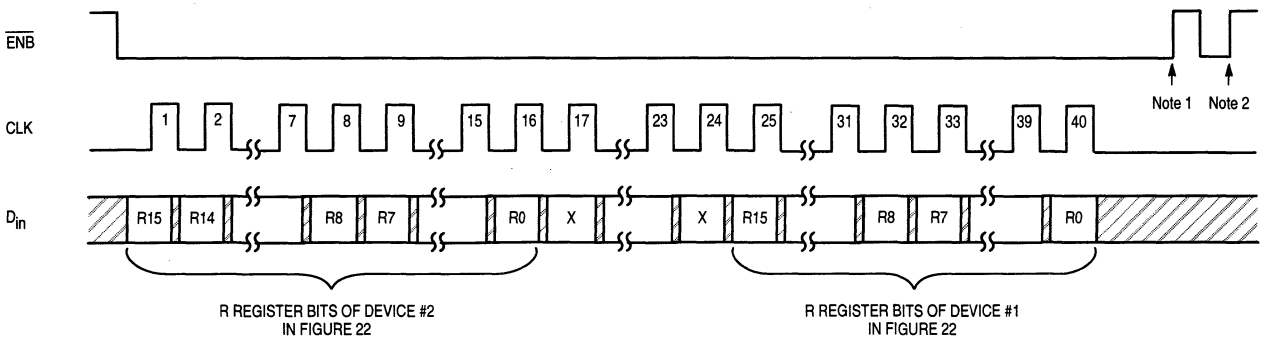


Figure 25. Accessing the R Registers of Two Cascaded MC145202 Devices

NOTES APPLICABLE TO EACH DEVICE:

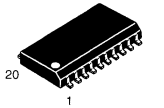
1. At this point, bits R13, R14 and R15 are stored and sent to the "OSC or 4–Stage Divider" block in the Block Diagram. Bits R0 through R12 are loaded into the first buffer in the double–buffered section of the R register. Therfore, the R counter divide is not altered yet and retains the previous ratio loaded. The C and A registers are not affected.
2. Optional load pulse. At this point, the bits R0 through R12 are transfered to the second buffer of the R register. The R counter begins dividing by the new ratio after completing the rest of the present count cycle. CLK must be low during the $\overline{\text{ENB}}$ pulse, as shown. The C and A registers are not affected. The first buffer of the R register is not affected. Also, see note of Figure 24 for an alternate method of loading the second buffer in the R register.

MC145220

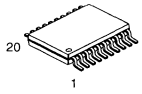
Advance Information

Dual 1.1 GHz PLL Frequency Synthesizer

BiCMOS



F SUFFIX
SOG PACKAGE
CASE 803C

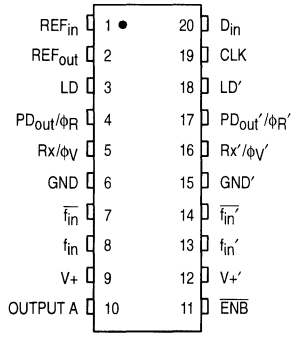


DT SUFFIX
TSSOP
CASE 948D

ORDERING INFORMATION

MC145220F	SOG Package
MC145220DT	TSSOP

PIN ASSIGNMENT



The MC145220 is a low–voltage, single–chip frequency synthesizer with serial interface capable of direct usage up to 1.1 GHz. The device simultaneously supports two loops. The two on–chip dual–modulus prescalers may be independently programmed to divide by either 32/33 or 64/65.

The device consists of two dual–modulus prescalers, two 6–stage A counters, two 12–stage N counters, two fully programmable 13–stage R (reference) counters, and two lock detectors. Four phase/frequency detectors are included: two with current source/sink outputs and two with double–ended outputs.

The counters are programmed via a synchronous serial port which is SPI compatible. The serial port is byte–oriented to facilitate control via an MCU. Due to the innovative BitGrabber Plus™ registers, the MC145220 may be cascaded with other peripherals featuring BitGrabber Plus without requiring leading dummy bits or multiple address bits in the serial data stream. In addition, BitGrabber Plus peripherals may be cascaded with existing BitGrabber™ peripherals. Because this device is a dual synthesizer, a single steering bit is used in the serial data stream to direct the data to either side of the chip.

The phase/frequency detectors have linear transfer functions (no dead zones). The current delivered by the current source/sink outputs is controllable via the serial port.

Also featured are low–power standby for either one or both loops and on–board support of an external crystal. In addition, the part may be configured such that the REF_{in} pin accepts an external reference signal. In this configuration, the REF_{out} pin may be programmed to output the REF_{in} frequency divided by 1, 2, 4, 8, or 16.

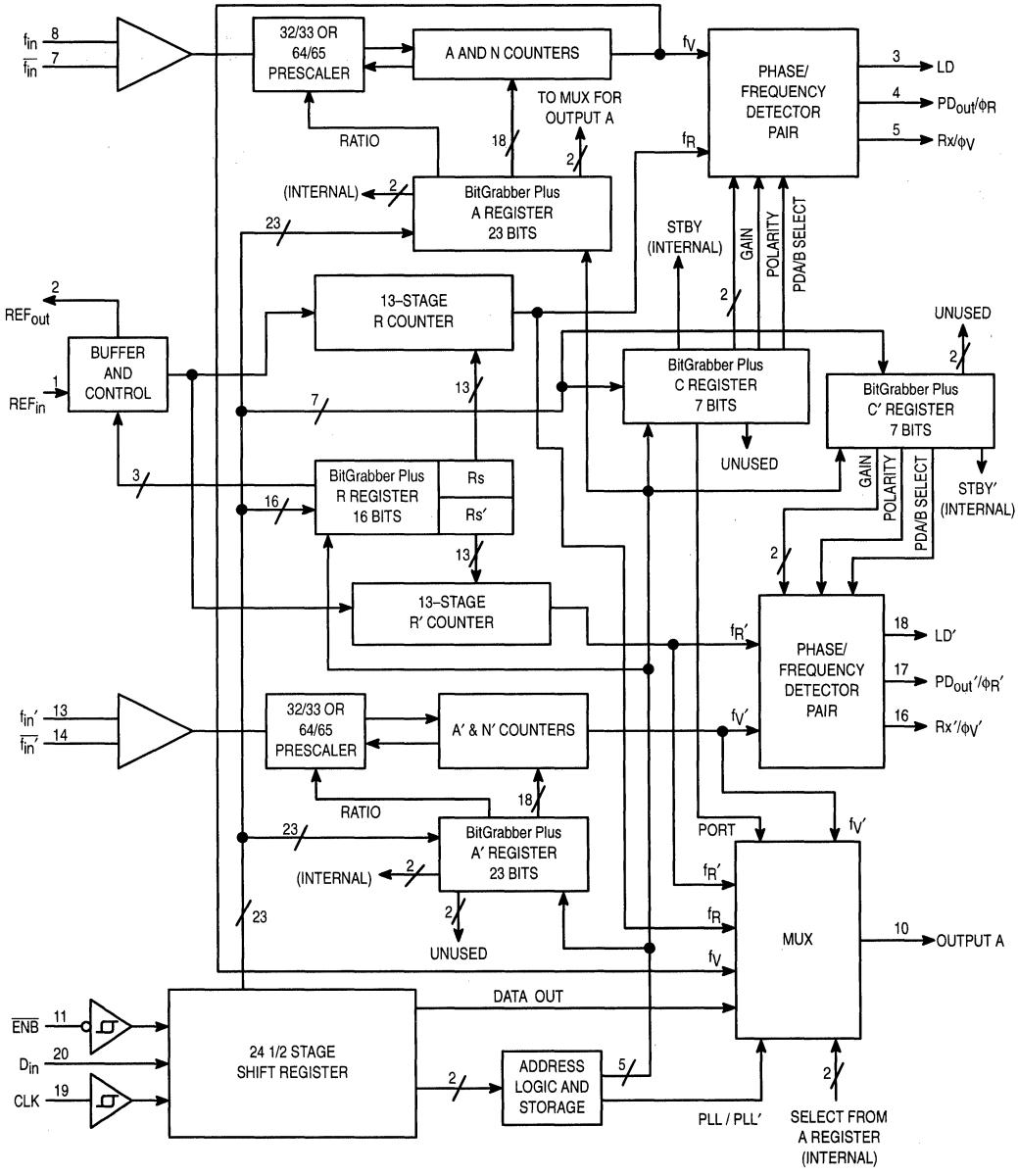
Applications include full–duplex radios, such as UHF cordless and cellular phones. Radio designs requiring two UHF loops or a UHF and VHF loop are accommodated.

- Operating Frequency: 40 to 1100 MHz
- Operating Supply Voltage Range: 2.7 to 5.5 V
- Supply Current: Both PLLs Operating — 12 mA Nominal
  One PLL Operating, One on Standby — 6.5 mA Nominal
  Both PLLs on Standby — 100 μA Maximum
- Phase Detector Output Current: Up to 2 mA @ 5 V
  Up to 1 mA @ 3 V
- Operating Temperature Range: – 40 to 85°C
- Independent R Counters Allow Use of Different Step Sizes for Each Loop
- R Counter Division Range: 1 and 10 to 8,191
- Dual–Modulus Capability Provides Total Division of the VCO Frequency up to 262,143
- Direct Interface to Motorola SPI Data Port

NOTE: This product is being evaluated for operation over a wider range than 40 MHz to 1.1 GHz. If your design requires a wider frequency range, contact your local Motorola representative for further information.

REV 3
10/95

BLOCK DIAGRAM



PIN 9 = V+ (Positive Power to the main PLL, Reference Circuit, and a portion of the Serial Port)
PIN 6 = GND (Ground to the main PLL, Reference Circuit, and a portion of the Serial Port)
PIN 12 = V+′ (Positive Power to PLL′ and a portion of the Serial Port)
PIN 15 = GND′ (Ground to PLL′ and a portion of the Serial Port)

MAXIMUM RATINGS* (Voltages Referenced to GND, unless otherwise stated)

Symbol	Parameter	Value	Unit
V+, V+′	DC Supply Voltage	– 0.5 to + 6.0	V
V_{in}	DC Input Voltage	– 0.5 to V+ + 0.5	V
V_{out}	DC Output Voltage	– 0.5 to V+ + 0.5	V
I_{in}	DC Input Current, per Pin	± 10	mA
I_{out}	DC Output Current, per Pin	± 20	mA
I	DC Supply Current, V+, V+′, GND, and GND′ Pins	30	mA
P_D	Power Dissipation, per Package	300	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds	260	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Descriptions section.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit.

2

ELECTRICAL CHARACTERISTICS

(V+ = V+′ = 2.7 to 5.5 V, GND = GND′, Voltages Referenced to GND, T_A = – 40 to 85°C, unless otherwise stated)

Symbol	Parameter	Test Condition	Guaranteed Limit	Unit
V_{IL}	Maximum Low–Level Input Voltage (D_{in}, CLK, $\overline{ENB}$, REF_{in})	Device in Reference Mode, dc Coupled	0.3 x V+	V
V_{IH}	Minimum High–Level Input Voltage (D_{in}, CLK, $\overline{ENB}$, REF_{in})	Device in Reference Mode, dc Coupled	0.7 x V+	V
V_{Hys}	Minimum Hysteresis Voltage (CLK, $\overline{ENB}$)		100	mV
V_{OL}	Maximum Low–Level Output Voltage (LD, LD′, REF_{out}, Output A)	I_{out} = 20 µA, Device in Reference Mode; Output A Not Selected as Port	0.1	V
V_{OH}	Minimum High–Level Output Voltage (REF_{out}, Output A)	I_{out} = – 20 µA, Device in Reference Mode; Output A Not Selected as Port	V+ – 0.1	V
I_{OL}	Minimum Low–Level Output Current (REF_{out})	V_{out} = 0.3 V	0.5	mA
I_{OL}	Minimum Low–Level Output Current (PD_{out}/ϕ_R, PD_{out}'/ϕ_R', Rx/ϕ_V, Rx′/ϕ_V′)	V_{out} = 0.3 V; Phase/Frequency Detectors Configured with ϕ_R, ϕ_V Outputs	0.5	mA
I_{OL}	Minimum Low–Level Output Current (Output A)	V_{out} = 0.3 V	0.5	mA
I_{OL}	Minimum Low–Level Output Current (LD, LD′)	V_{out} = 0.3 V	0.5	mA
I_{OH}	Minimum High–Level Output Current (REF_{out})	V_{out} = V+ – 0.3 V	– 0.4	mA
I_{OH}	Minimum High–Level Output Current (PD_{out}/ϕ_R, PD_{out}'/ϕ_R', Rx/ϕ_V, Rx′/ϕ_V′)	V_{out} = V+ – 0.3 V; Phase/Frequency Detectors Configured with ϕ_R, ϕ_V Outputs	– 0.4	mA
I_{OH}	Minimum High–Level Output Current (Output A)	V_{out} = V+ – 0.3 V; Output A Not Selected as Port	– 0.4	mA
I_{in}	Maximum Input Leakage Current (D_{in}, CLK, $\overline{ENB}$, REF_{in})	V_{in} = V+ or GND; Device in XTAL Mode	± 1.0	µA
I_{in}	Maximum Input Current (REF_{in})	V_{in} = V+ or GND; Device in Reference Mode	± 150	µA
I_{OZ}	Maximum Output Leakage Current (PD_{out}/ϕ_R, PD_{out}'/ϕ_R')	V_{out} = V+ or GND; Phase/Frequency Detectors Configured with PD_{out} Output, Output in High–Impedance State	± 150	nA
I_{OZ}	Maximum Output Leakage Current (Output A, LD, LD′)	V_{out} = V+ or GND; Output A Selected as Port; Output in High–Impedance State	± 5	µA
I_{STBY}	Maximum Standby Supply Current	V_{in} = V+ or GND; Outputs Open; Both PLLs in Standby Mode, Shut–Down Crystal Mode or REF_{out}–Static–Low Reference Mode	100	µA
I_T	Total Operating Supply Current	f_{in} = f_{in}' = 1.1 GHz; both loops active; REF_{in} = 13 MHz @ 1 V p–p; Output A = Inactive; All Outputs = No Connect; D_{in}, $\overline{ENB}$, CLK = V+ or GND; Phase/Frequency Detectors Configured with ϕ_R, ϕ_V Outputs	*	mA

* The nominal value is 12 mA. This is not a guaranteed limit.

ANALOG CHARACTERISTICS — CURRENT SOURCE/SINK OUTPUTS — $PD_{out}/\phi R$ AND $PD_{out}'/\phi R'$

(Phase/Frequency Detectors Configured with PD_{out} Outputs, $I_{out} \leq 2$ mA @V+ = V+′ = 4.5 to 5.5 V, $I_{out} \leq 1$ mA @V+ = V+′ = 2.7 to 4.4 V, GND = GND′, Voltages Referenced to GND)

Parameter		Test Condition	Guaranteed Limit	Unit
Maximum Source Current Variation Part–to–Part	(Notes 3 and 4)	V_{out} = 0.5 x V+	± 20	%
Maximum Sink–versus–Source Mismatch	(Note 3)	V_{out} = 0.5 x V+	12	%
Output Voltage Range	(Note 3)	I_{out} variation ≤ 20%	0.5 to V+ – 0.5 V	V

NOTES:

5. Percentages calculated using the following formula: (Maximum Value – Minimum Value)/Maximum Value.
6. See Rx Pin Description for external resistor values.
7. This parameter is guaranteed for a given temperature within – 40 to 85°C and given supply voltage within 2.7 to 5.5 V.
8. Applicable for the $Rx/\phi V$ or $Rx'/\phi V'$ reference pin tied to the GND or GND′ pin through a resistor. See Pin Descriptions for suggested resistor values.

2

AC INTERFACE CHARACTERISTICS

(V+ = V+′ = 2.7 to 5.5 V, GND = GND′, T_A = – 40 to 85°C, C_L = 25 pF, Input $t_r = t_f$ = 10 ns)

Symbol	Parameter	Guaranteed Limit	Unit
f_{clk}	Serial Data CLK Frequency (Figure 1) NOTE: Refer to Clock t_w below	dc to 2.0	MHz
t_{PLH}, t_{PHL}	Maximum Propagation Delay, CLK to Output A (Selected as Data Out) (Figures 1 and 5)	200	ns
t_{PZL}, t_{PLZ}	Maximum Propagation Delay, $\overline{ENB}$ to Output A (Selected as Port) (Figures 2 and 6)	200	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Output A; t_{THL} only, on Output A when Selected as Port (Figures 1, 5, and 6)	200	ns
C_{in}	Maximum Input Capacitance — D_{in}, CLK, $\overline{ENB}$	10	pF

TIMING REQUIREMENTS (V+ = V+′ = 2.7 to 5.5 V, GND = GND′, T_A = – 40 to 85°C, Input $t_r = t_f$ = 10 ns unless otherwise indicated)

Symbol	Parameter	Guaranteed Limit	Unit
t_{su}, t_h	Minimum Setup and Hold Times, D_{in} versus CLK (Figure 3)	50	ns
t_{su}, t_h, t_{rec}	Minimum Setup, Hold, and Recovery Times, $\overline{ENB}$ versus CLK (Figure 4)	100	ns
t_w	Minimum Pulse Width, $\overline{ENB}$ (Figure 4)	*	cycles
t_w	Minimum Pulse Width, CLK (Figure 1)	250	ns
t_r, t_f	Maximum Input Rise and Fall Times — CLK (Figure 1)	100	µs

* The minimum limit is 3 REF_{in} cycles or 195 f_{in} cycles with selection of a 64/65 prescale ratio or 99 f_{in} cycles with selection of a 32/33 prescale ratio, whichever is greater.

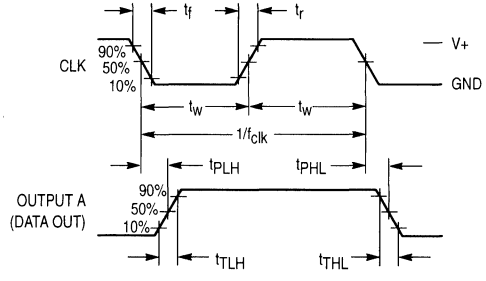


Figure 1.

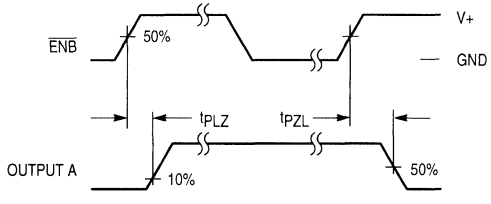


Figure 2.

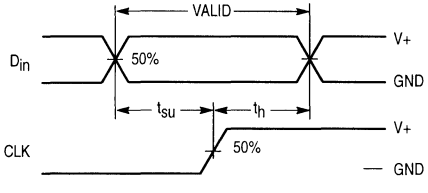


Figure 3.

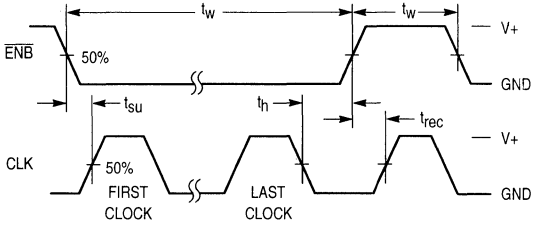
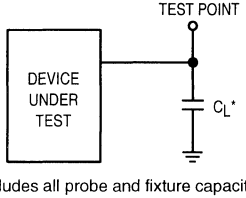
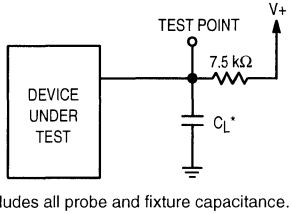


Figure 4.



* Includes all probe and fixture capacitance.

Figure 5.



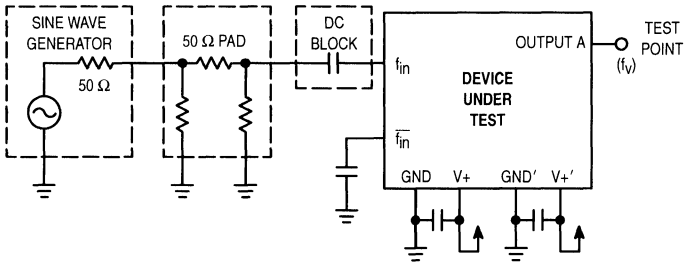
* Includes all probe and fixture capacitance.

Figure 6.

LOOP SPECIFICATIONS ($V+ = V+' = 2.7$ to 5.5 V unless otherwise indicated, GND = GND′, $T_A = -40$ to 85°C)

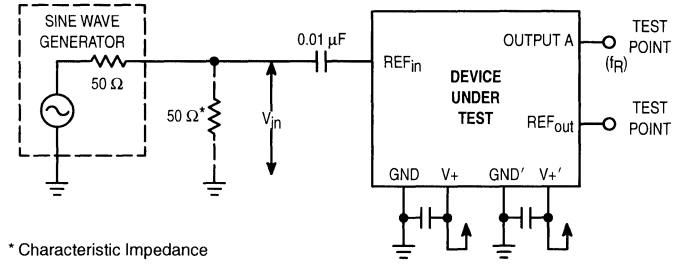
Symbol	Parameter	Test Condition	Guaranteed Operating Range		Unit
			Min	Max	
P_{in}	Input Sensitivity Range, f_{in} or f_{in}' (Figure 7)	40 MHz ≤ frequency < 300 MHz 300 MHz ≤ frequency < 700 MHz 700 MHz ≤ frequency < 1100 MHz	– 2 – 5 – 16	8 6 4	dBm*
ΔP_{in}	Difference Allowed Between f_{in} and f_{in}'			10	dB
—	Isolation Between f_{in} and f_{in}'		15		dB
f_{ref}	Input Frequency, REF_{in} Externally Driven in Reference Mode (Figure 8)	V_{in} = 400 mV p–p, R Counter set to divide ratio such that $f_R \leq 1$ MHz, REF Counter set to divide ratio such that $REF_{out} \leq 5$ MHz V+ = 2.7 V V+ = 4.5 V V+ = 5.5 V	 4 5 5	 15 27 27	MHz
f_{XTAL}	Crystal Frequency, Crystal Mode (Figure 9)	C1 ≤ 30 pF, C2 ≤ 30 pF, Includes Stray Capacitance; R Counter and REF Counter same as above V+ = 2.7 V V+ = 3.5 V V+ = 4.5 V V+ = 5.5 V	 2 2 2 2	 10 13 15 15	MHz
f_{out}	Output Frequency, REF_{out} (Figures 10 and 12)	C_L = 25 pF	dc	5	MHz
f	Operating Frequency of the Phase Detectors		dc	1	MHz
t_w	Output Pulse Width, ϕ_R, ϕ_V, ϕ_R', ϕ_V' (Figures 11 and 12)	f_R in Phase with f_V, C_L = 25 pF	16	125	ns
C_{in}	Input Capacitance, REF_{in}		—	5	pF

* Power level at the input to the dc block.



NOTE: Alternately, the 50 Ω pad may be a T network.

Figure 7. Test Circuit



* Characteristic Impedance

Figure 8. Test Circuit — Reference Mode

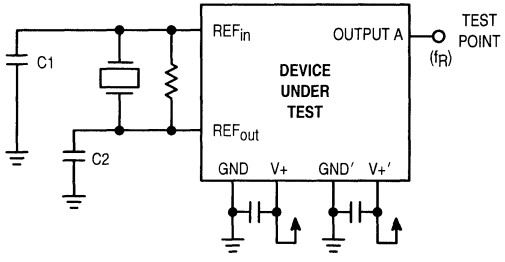


Figure 9. Test Circuit — Crystal Mode

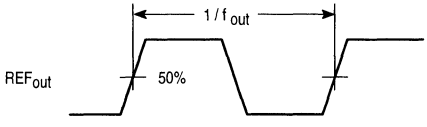


Figure 10. Switching Waveform

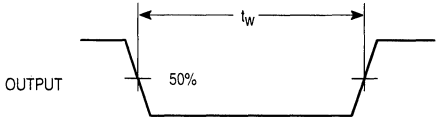
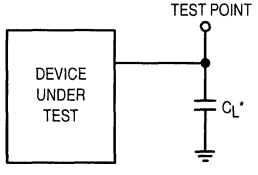
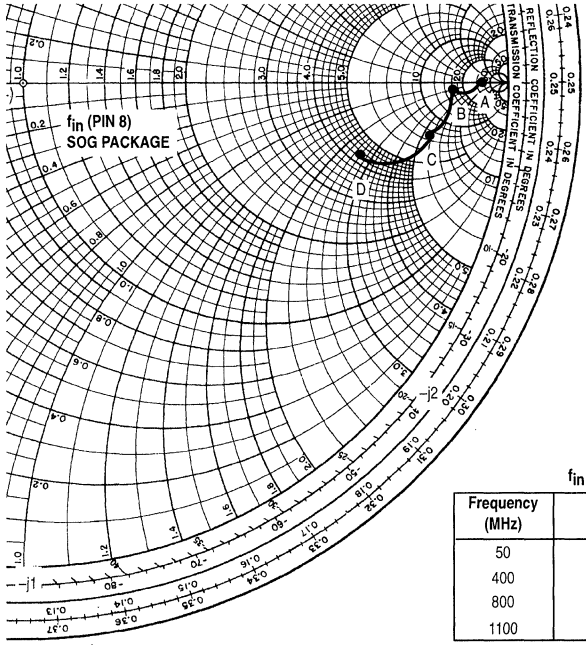


Figure 11. Switching Waveform



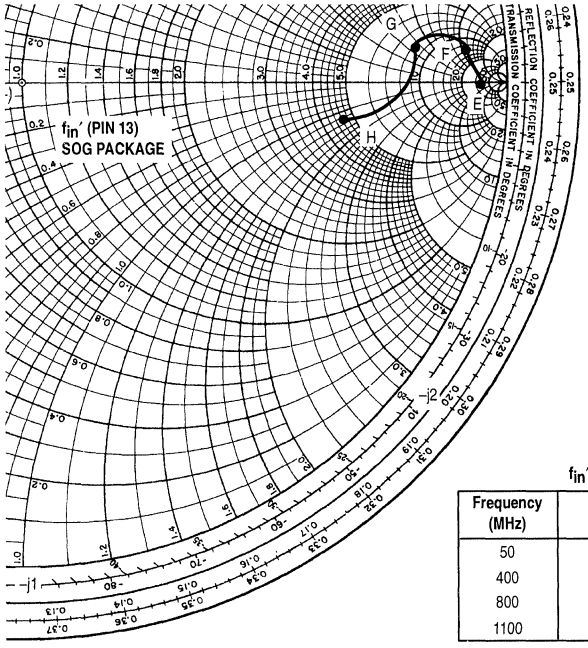
* Includes all probe and fixture capacitance.

Figure 12. Test Circuit



f_{in} (PIN 8) – SOG PACKAGE

Frequency (MHz)	Point	Impedance (Ω)	
		3 V Supply	5 V Supply
50	A	1900 – j 157	1970 – j 102
400	B	1440 – j 228	1510 + j 19
800	C	552 – j 380	671 – j 334
1100	D	196 – j 141	223 – j 147



f_{in}' (PIN 13) – SOG PACKAGE

Frequency (MHz)	Point	Impedance (Ω)	
		3 V Supply	5 V Supply
50	E	1900 + j 149	1930 + j 214
400	F	878 + j 703	746 + j 741
800	G	705 + j 208	626 + j 327
1100	H	215 – j 69.3	243 – j 61.3

Figure 13. Nominal Input Impedance of f_{in} and f_{in}' — Series Format (R + jX) (50 – 1100 MHz)

PIN DESCRIPTIONS

DIGITAL INTERFACE PINS

D_{in}
Serial Data Input (Pin 20)

The bit stream begins with the MSB and is shifted in on the low–to–high transition of CLK. The bit pattern is 1 byte (8 bits) long to access the C or configuration registers, 2 bytes (16 bits) to access the first buffer of the R registers, or 3 bytes (24 bits) to access the A registers (see Table 1). The values in the registers do not change during shifting because the transfer of data to the registers is controlled by $\overline{ENB}$.

NOTE

The value programmed for the N counter must be greater than or equal to the value of the A counter.

The 13 LSBs of the R registers are double–buffered. As indicated above, data is latched into the first buffer on a 16–bit transfer. (The 3 MSBs are not double–buffered and have an immediate effect after a 16–bit transfer.) The two second buffers of the R register contain the two 13–bit divide ratios for the R counters. These second buffers are loaded with the contents of the first buffer as follows. Whenever the A register is loaded, the Rs (second) buffer is loaded from the R (first) buffer. Similarly, whenever the A′ register is loaded, the Rs′ (second) buffer is updated from the R (first) buffer. This allows presenting new values to the R, A, and N counters simultaneously. Note that two different R counter divide ratios may be established: one for the main PLL and another for PLL′.

The bit stream does not need address bits due to the innovative BitGrabber Plus registers. A steering bit is used to direct data to either the main PLL or PLL′ section of the chip. Data is retained in the registers over a supply range of 2.7 to 5.5 V. The formats are shown in Figures 14, 15, and 16.

D_{in} typically switches near 50% of V+ to maximize noise immunity. This input can be directly interfaced to CMOS devices with outputs guaranteed to switch near rail–to–rail. When interfacing to NMOS or TTL devices, either a level shifter (MC74HC14A, MC14504B) or pull–up resistor of 1 kΩ to 10 kΩ must be used. Parameters to consider when sizing the resistor are worst–case I_{OL} of the driving device, maximum tolerable power consumption, and maximum data rate.

Table 1. Register Access

(MSBs are shifted in first; C0, R0, and A0 are the LSBs)

Number of Clocks	Accessed Register	Bit Nomenclature
8	C Registers	C7, C6, C5, . . ., C0
16	R Register, First Buffer	R15, R14, R13, . . ., R0
24	A Registers	A23, A22, A21, . . ., A0
Other Values ≤ 32	Not Allowed	
Values > 32	See Figures 24 to 27	

CLK
Serial Data Clock Input (Pin 19)

Low–to–high transitions on CLK shift bits available at the D_{in} pin, while high–to–low transitions shift bits from Output A (when configured as Data Out, see Pin 10). The 24–1/2 stage shift register is static, allowing clock rates down to dc in a continuous or intermittent mode.

Eight clock cycles are required to access the C registers. Sixteen clock cycles are needed for the first buffer of the R register. Twenty–four cycles are used to access the A registers. See Table 1 and Figures 14, 15, and 16. The number of clocks required for cascaded devices is shown in Figures 25 through 27.

CLK typically switches near 50% of V+ and has a Schmitt–triggered input buffer. Slow CLK rise and fall times are allowed. See the last paragraph of **D_{in}** for more information.

NOTE

To guarantee proper operation of the power–on reset (POR) circuit, the CLK pin must be held at GND (with $\overline{ENB}$ being a don't care) or $\overline{ENB}$ must be held at the potential of the V+ pin (with CLK being a don't care) during power–up. Floating, toggling, or having these pins in the wrong state during power–up does not harm the chip, but causes two potentially undesirable effects. First, the outputs of the device power up in an unknown state. Second, if two devices are cascaded, the A Registers must be written twice after power up. After these two accesses, the two cascaded chips perform normally.

$\overline{ENB}$
Active–Low Enable Input (Pin 11)

This pin is used to activate the serial interface to allow the transfer of data to/from the device. When $\overline{ENB}$ is in an inactive high state, shifting is inhibited and the port is held in the initialized state. To transfer data to the device, $\overline{ENB}$ (which must start inactive high) is taken low, a serial transfer is made via D_{in} and CLK, and $\overline{ENB}$ is taken back high. The low–to–high transition on $\overline{ENB}$ transfers data to the C or A registers and first buffer of the R register, depending on the data stream length per Table 1.

NOTE

Transitions on $\overline{ENB}$ must not be attempted while CLK is high. This puts the device out of synchronization with the microcontroller. Resynchronization occurs whenever $\overline{ENB}$ is high and CLK is low.

This input is Schmitt–triggered and switches near 50% of V+, thereby minimizing the chance of loading erroneous data into the registers. See the last paragraph of **D_{in}** for more information.

For POR information, see the note for the **CLK pin**.

OUTPUT A
Configurable Digital Output (Pin 10)

Output A is selectable as f_R, f_V, f_R', f_V', Data Out, or Port. Bits A21 and A22 and the steering bit (A23) control the selection; see Figure 15. When selected as Port, the pin becomes an open–drain N–channel MOSFET output. As such, a pullup device is needed for pin 10. With all other selections, the pin is a totem–pole (push–pull) output.

If A22 = A21 = high, Output A is configured as f_R when the steering bit is low and f_R' when the bit is high. These signals are the buffered outputs of the 13–stage R counters. The signals appear as normally low and pulse high. The signals can be used to verify the divide ratios of the R counters. These ratios extend from 10 to 8191 and are determined by the binary value loaded into bits R0 – R12 in the R register. Also, direct access to the phase detectors via the REF_{in} pin is allowed by choosing a divide value of one. See Figure 16. The maximum frequency at which the phase detectors operate is 1 MHz. Therefore, the frequency of f_R and f_R' should not exceed 1 MHz.

If A22 = high and A21 = low, Output A is configured as f_V when the steering bit is low and f_V' when the bit is high. These signals are the buffered outputs of the 12–stage N counters. The signals appear as normally low and pulse high. The signals can be used to verify the operation of the prescalers, A counters, and N counters. The divide ratio between the f_{in} or f_{in}' input and the f_V or f_V' signal is N x P + A. N is the divide ratio of the N counter, P is 32 with a 32/33 prescale ratio or 64 with a 64/65 prescale ratio, and A is the divide ratio of the A counter. These ratios are determined by bits loaded into the A registers. See Figure 15. The maximum frequency at which the phase detectors operate is 1 MHz. Therefore, the frequency of f_V and f_V' should not exceed 1 MHz.

If A22 = low and A21 = high, Output A is configured as Data Out. This signal is the serial output of the 24–1/2 stage shift register. The bit stream is shifted out on the high–to–low transition of the CLK input. Upon power up, Output A is automatically configured as Data Out to facilitate cascading devices.

If A22 = A21 = low, Output A is configured as Port. This signal is a general–purpose digital output which may be used as an MCU port expander. This signal is low when the Port bit (C1) of the C register is low, and high impedance when the Port bit is high. See Figure 14.

REFERENCE PINS

REF_{in} and REF_{out}
Reference Oscillator Input and Output (Pins 1 and 2)

Configurable Pins for a Crystal or an External Reference. This pair of pins can be configured in one of two modes: the crystal mode or the reference mode. Bits R13, R14, and R15 in the R register control the modes as shown in Figure 16.

In the crystal mode, these pins form a reference oscillator when connected to terminals of an external parallel–resonant crystal. Frequency–setting capacitors of appropriate values, as recommended by the crystal supplier, are connected from each of the two pins to ground (up to a maximum of 30 pF each, including stray capacitance). An external resistor of 1 MΩ to 15 MΩ is connected directly across the pins to ensure linear operation of the amplifier. The required connections for the crystal are shown in Figure 9. To turn on the oscillator, bits R15, R14, and R13 must have an octal value of one (001 in binary). This is the active–crystal mode shown in Figure 16. In this mode, the crystal oscillator runs and the R Counter divides the crystal frequency, unless the part is in standby. If the part is placed in standby via the C or C′ register, the oscillator runs, but the R or R′ counter is stopped, respectively. However, if bits R15 to R13 have a value of 0, the oscillator is stopped, which saves additional power. This is the shut–down crystal mode shown in Figure 16, and can be engaged whether in standby or not.

In the reference mode, REF_{in} (pin 1) accepts a signal from an external reference oscillator, such as a TCXO. A signal swinging from at least the V_{IL} to V_{IH} levels listed in the **Electrical Characteristics** table may be directly coupled to the pin. If the signal is less than this level, ac coupling must be used as shown in Figure 8. The ac–coupled signal must be at least 400 mV p–p. Due to an on–board resistor which is engaged in the reference modes, an external biasing resistor tied between REF_{in} and REF_{out} is not required.

With the reference mode, the REF_{out} pin is configured as the output of a divider. As an example, if bits R15, R14, and R13 have an octal value of seven, the frequency at REF_{out} is the REF_{in} frequency divided by 16. In addition, Figure 16 shows how to obtain ratios of eight, four, and two. A ratio of one–to–one can be obtained with an octal value of three. Upon power up, a ratio of eight is automatically initialized. The maximum frequency capability of the REF_{out} pin is 5 MHz for large output swings (V_{OH} to V_{OL}) and 25 pF loads. Therefore, for REF_{in} frequencies above 5 MHz, the one–to–one ratio may not be used for these large signal swing and large C_L requirements. Likewise, for REF_{in} frequencies above 10 MHz, the ratio must be more than two.

If REF_{out} is unused, an octal value of two should be used for R15, R14, and R13 and the REF_{out} pin should be floated. A value of two allows REF_{in} to be functional while disabling REF_{out}, which minimizes dynamic power consumption and electromagnetic interference (EMI).

LOOP PINS

f_{in}, $\overline{f_{in}}$ and f_{in}', $\overline{f_{in}'}$
Frequency Inputs (Pins 8, 7 and 13, 14)

These pins feed the onboard RF amplifiers which drive the prescalers. These inputs may be fed differentially. However, they usually are used in single–ended configurations (shown in Figure 7). Note that f_{in} is driven while $\overline{f_{in}}$ must be tied to ac ground (via capacitor). The signal sources driving these pins originate from external VCOs.

Motorola does not recommend driving $\overline{f_{in}}$ while terminating f_{in} because this configuration is not tested for sensitivity. The sensitivity is dependent on the frequency as shown in the **Loop Specifications** table.

PD_{out}/ϕ_R, PD_{out}'/ϕ_R'
Single–Ended Phase/Frequency Detector Outputs (Pins 4 and 17)

When the C2 bits in the C or C′ registers are low, these pins are independently configured as single–ended outputs PD_{out} or PD_{out}', respectively. As such, each pin is a three–state current–source/sink output for use as a loop error signal when combined with an external low–pass filter. The phase/frequency detector is characterized by a linear transfer function. The operation of the phase/frequency detector is described below and is shown in Figure 17.

POL bit (C0) in the C register = low (see Figure 14)
- Frequency of $f_V > f_R$ or Phase of f_V Leading f_R: current–sinking pulses from a floating state
- Frequency of $f_V < f_R$ or Phase of f_V Lagging f_R: current–sourcing pulses from a floating state
- Frequency and Phase of $f_V = f_R$: essentially a floating state; voltage at pin determined by loop filter

POL bit (C0) = high
- Frequency of $f_V > f_R$ or Phase of f_V Leading f_R: current–sourcing pulses from a floating state
- Frequency of $f_V < f_R$ or Phase of f_V Lagging f_R: current–sinking pulses from a floating state
- Frequency and Phase of $f_V = f_R$: essentially a floating state; voltage at pin determined by loop filter

These outputs can be enabled, disabled, and inverted via the C and C′ registers. If desired, these pins can be forced to the floating state by utilization of the standby feature in the C or C′ registers (bit C6). This is a patented feature.

The phase detector gain is controllable by bits C4 and C5: gain (in amps per radian) = PD_{out} current in amps divided by 2π.

PD_{out}/ϕ_R, Rx/ϕ_V and PD_{out}'/ϕ_R', Rx'/ϕ_V'
Double–Ended Phase/Frequency Detector Outputs (Pins 4, 5 and 17, 16)

When the C2 bits in the C or C′ registers are high, these two pairs of pins are independently configured as double–ended outputs ϕ_R, ϕ_V or ϕ_R', ϕ_V', respectively. As such, these outputs can be combined externally to generate a loop error signal. Through use of a Motorola patented technique, the detector's dead zone has been eliminated. Therefore, the phase/frequency detector is characterized by a linear transfer function. The operation of the phase/frequency detectors are described below and are shown in Figure 17.

POL bit (C0) in the C register = low (see Figure 14)
- Frequency of $f_V > f_R$ or Phase of f_V Leading f_R: ϕ_V = negative pulses, ϕ_R = essentially high
- Frequency of $f_V < f_R$ or Phase of f_V Lagging f_R: ϕ_V = essentially high, ϕ_R = negative pulses
- Frequency and Phase of $f_V = f_R$: ϕ_V and ϕ_R remain essentially high, except for a small minimum time period when both pulse low in phase

POL bit (C0) = high
- Frequency of $f_V > f_R$ or Phase of f_V Leading f_R: ϕ_R = negative pulses, ϕ_V = essentially high
- Frequency of $f_V < f_R$ or Phase of f_V Lagging f_R: ϕ_R = essentially high, ϕ_V = negative pulses
- Frequency and Phase of $f_V = f_R$: ϕ_V and ϕ_R remain essentially high, except for a small minimum time period when both pulse low in phase

These outputs can be enabled, disabled, or interchanged via C register bits C6 or C0. This is a patented feature. Note that when disabled in standby, these outputs are forced to their rest condition (high state). See Figure 14.

The ϕ_R and ϕ_V output signals swing from approximately GND to V+.

LD and LD′
Lock Detector Outputs (Pins 3 and 18)

Each output is essentially at a high–impedance state with very narrow low–going pulses of a few nanoseconds when the respective loop is locked (f_R and f_V of the same phase and frequency). The output pulses low when f_V and f_R are out of phase or different frequencies. LD is the logical ANDing of ϕ_R and ϕ_V, while LD′ is the logical ANDing of ϕ_R' and ϕ_V'. See Figure 17.

Upon power up, on–chip initialization circuitry forces LD and LD′ to the high–impedance state. These pins are low during standby. If unused, LD should be tied to GND and LD′ should be tied to GND′.

These outputs have open–drain N–channel MOSFET drivers. This facilitates a wired–OR function. See Figure 21.

Rx/ϕ_V and Rx'/ϕ_V'
External Current Setting Resistors (Pins 5 and 16)

When the C2 bits in the C or C′ registers are low, these two pins are independently configured as current setting pins Rx or Rx′, respectively. As such, resistors tied between each of these pins and GND and GND′, in conjunction with bits C4 and C5 in the C and C′ registers, determine the amount of current that the PD_{out} pins sink and source. When bits C4 and C5 are both set high, the maximum current is obtained; see Table 2 for other values of current.

Table 2. PD_{out} or PD_{out}' Current

C5	C4	Current
0	0	5%
0	1	50%
1	0	80%
1	1	100%

The formula for determining the value of Rx or Rx′ is as follows.

$$R = \frac{V1 - V2}{I}$$

where Rx is the value of external resistor in ohms, V1 is the supply voltage, V2 is 1.5 V for a reference current through Rx of 100 μA or 1.745 V for a reference current of 200 μA, and I is the reference current flowing through Rx or Rx′.

The reference current flowing through Rx or Rx′ is multiplied by a factor of approximately 10 (in the 100% current mode) and delivered by the PD_{out} or PD_{out}' pin, respectively. To achieve a maximum phase detector output current of 1 mA, the resistor should be about 15 kΩ when a 3 V supply is employed. See Table 3.

Table 3. Rx Values

Supply Voltage	Rx	PD_{out} or PD_{out}' Current in 100% Mode
3 V	15 kΩ	1 mA
5 V	16 kΩ	2 mA

Do not use a decoupling capacitor on the Rx or Rx′ pin. Use of a capacitor causes undesirable current spikes to appear on the phase detector output when invoking the standby mode.

POWER SUPPLY PINS

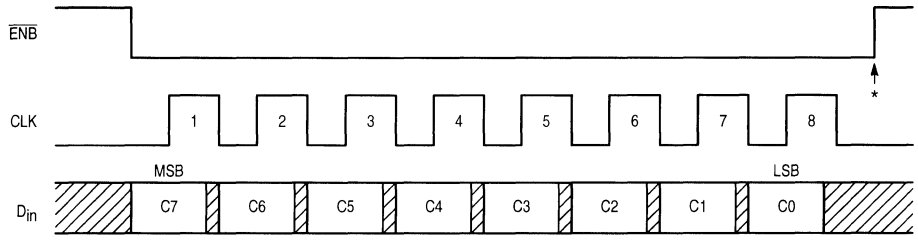
V+ and V+′
Positive Supply Potentials (Pins 9 and 12)

V+ supplies power to the main PLL, reference circuit, and a portion of the serial port. V+′ supplies power to PLL′ and a portion of the serial port. Both V+ and V+′ must be at the same voltage level and may range from 2.7 V to 5.5 V with respect to the GND and GND′ pins.

For optimum performance, V+ should be bypassed to GND and V+′ bypassed to GND′ using separate low–inductance capacitors mounted very close to the MC145220. Lead lengths and printed circuit board traces to the capacitors should be minimized. (The very fast switching speed of the device can cause excessive current spikes on the power leads if they are improperly bypassed.)

GND and GND′
Grounds (Pins 6 and 15)

The GND pin is the ground for the main PLL and GND′ is the ground for PLL′.



* At this point, the new byte is transferred to the C or C′ register and stored. No other registers are affected.

C7 – Steer: Used to direct the data to either the C or C′ register. A low level directs data to the C register; a high level is for the C′ register.

C6 – Standby: When set high, places both the main PLL and PLL′ (when C6 is set in the C register) or PLL′ only (when C6 is set in the C′ register) in the standby mode for reduced power consumption. The associated PD_{out} is forced to the floating state, the associated counters (A, N, and R) are inhibited from counting, the associated Rx current is shut off, and the associated prescaler stops counting and is placed in a low current mode. The associated double–ended phase/frequency detector outputs are forced to a high level. In standby, the associated LD output is placed in the low–state, thus indicating "not locked" (open loop). During standby, data is retained in all registers and any register may be accessed.

In standby, the condition of the REF/OSC circuitry is determined by bits R13, R14, and R15 in the R register per Figure 16. However, if REF_{out} = *static low* is selected, the internal feedback resistor is disconnected and the REF_{in} is inhibited when both PLL and PLL′ are placed in standby via the C register. Thus, the REF_{in} only presents a capacitive load. **Note**: PLL/PLL′ standby does not affect the other modes of the REF/OSC circuitry as determined by bits R13, R14, and R15 in the R register. The PLL′ standby mode (controlled from the C′ register) has no effect on the REF/OSC circuit.

When C6 is reset low, the associated PLL (or PLLs) is (are) taken out of standby in two steps. First, the REF_{in} (only in 1 mode, PLL/PLL′ in standby) resistor is reconnected, REF_{in} (only 1 mode) is gated on, all counters are enabled, and the Rx current is enabled. Any f_R and f_V signals are inhibited from toggling the phase/frequency detectors and lock detectors. Second, when the appropriate f_R pulse occurs, the A and N counters are jam loaded, the prescaler is gated on, and the phase/frequency and lock detectors are initialized. Immediately after the jam load, the A, N, and R counters begin counting down together. At this point, the f_R and f_V pulses are enabled to the phase and lock detectors. (Patented feature.)

C5, C4 – I2, I1: Independently controls the PD_{out} or PD_{out}' source/sink current per Table 2. With both bits high, the maximum current (as set by Rx or Rx′) is available. POR forces C5 and C4 to high levels.

C3 – Spare: Unused

C2 – PDA/B: Independently selects which phase/frequency detector is to be used. When set high, the double–ended detector is selected with outputs ϕ_R and ϕ_V or ϕ_R' and ϕ_V'. When reset low, the current source/sink detector is selected with outputs PD_{out} or PD_{out}'. In the second case, the appropriate Rx or Rx′ pin is tied to an external resistor. POR forces C2 low.

C1 – Port: When the Output A pin is selected as "Port" via bits A22 and A21, C1 of the C register determines the state of Output A. When C1 is set high, Output A is forced to the high–impedance state; C1 low forces Output A low. The Port bit is not affected by the standby mode. **Note**: C1 of the C′ register is not used in any mode.

C0 – POL: Selects the output polarity of the associated phase/frequency detectors. When set high, this bit inverts the associated current source/sink output and interchanges the associated double–ended output relative to the waveforms in Figure 17. Also, see the phase detector output pin descriptions for more information. This bit is cleared low at power up.

Figure 14. C and C′ Register Accesses and Format (8 Clock Cycles are Used)

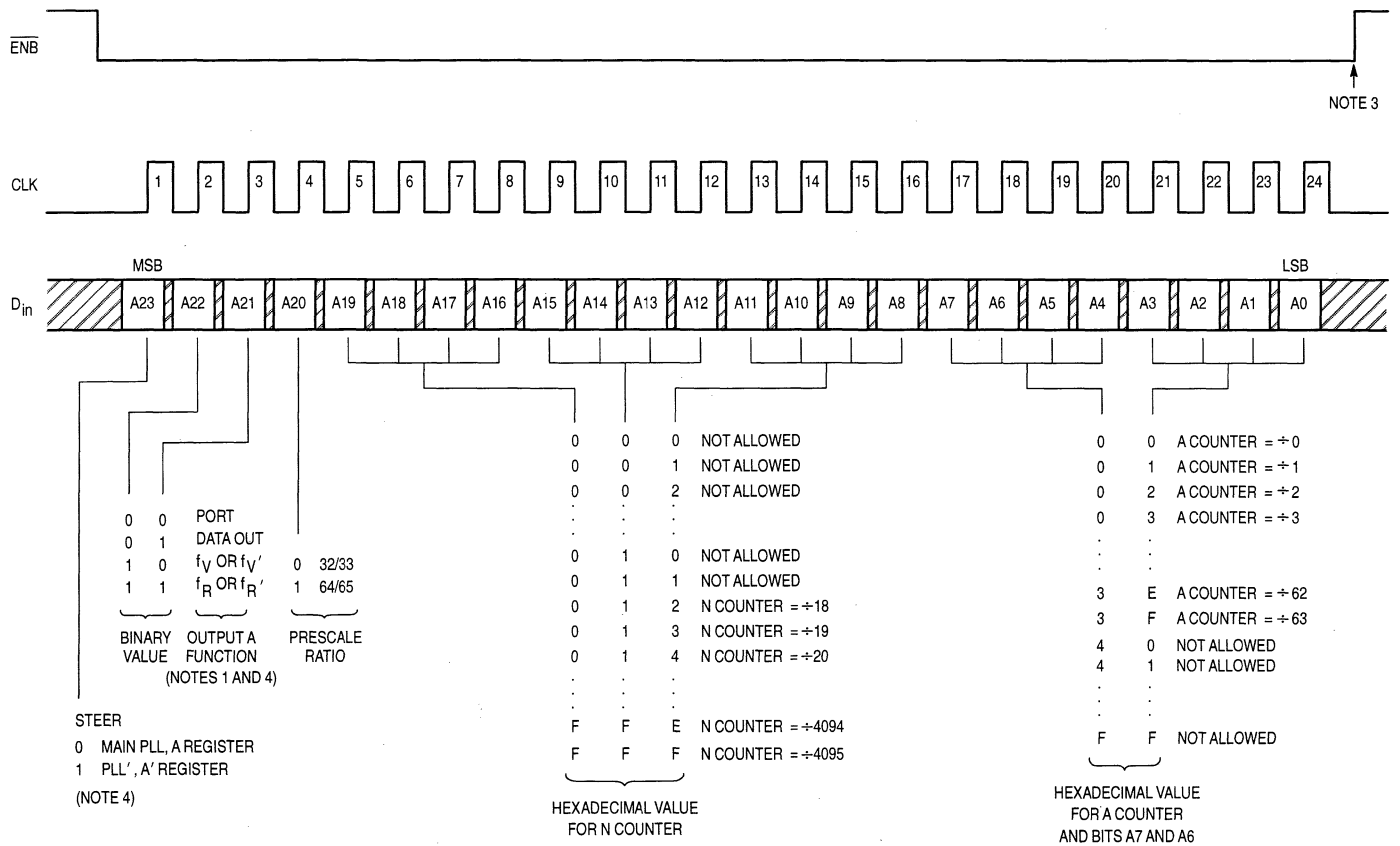
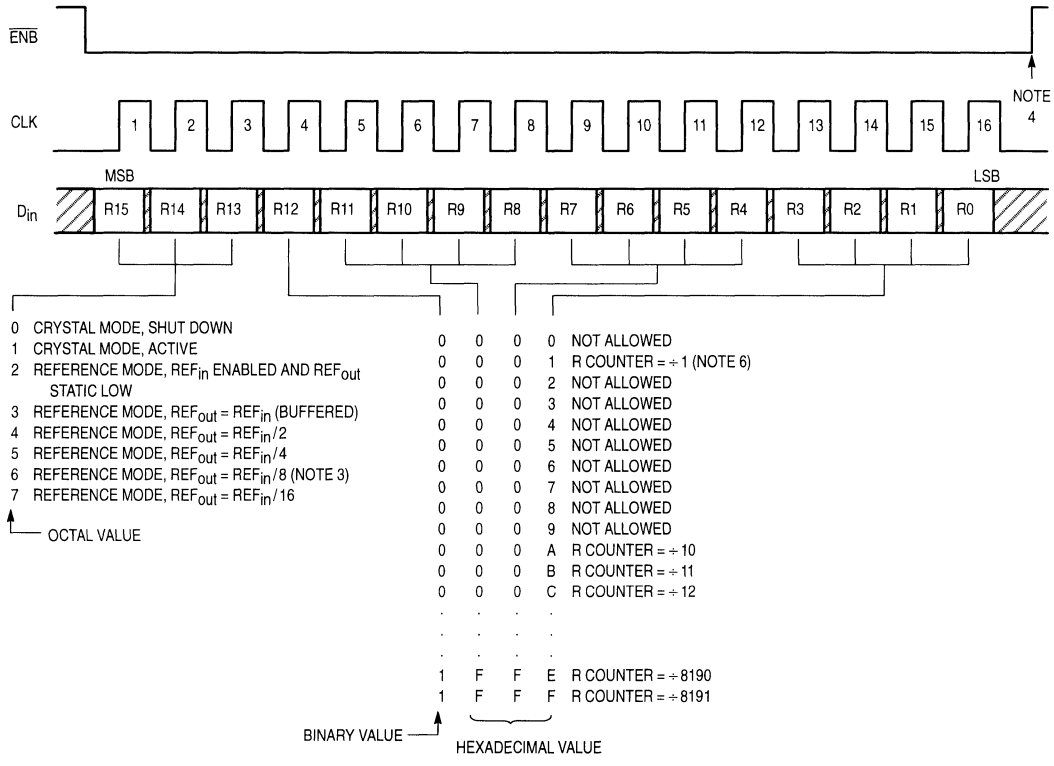


Figure 15. A and A′ Register Accesses and Format (24 Clock Cycles are Used)

NOTES:

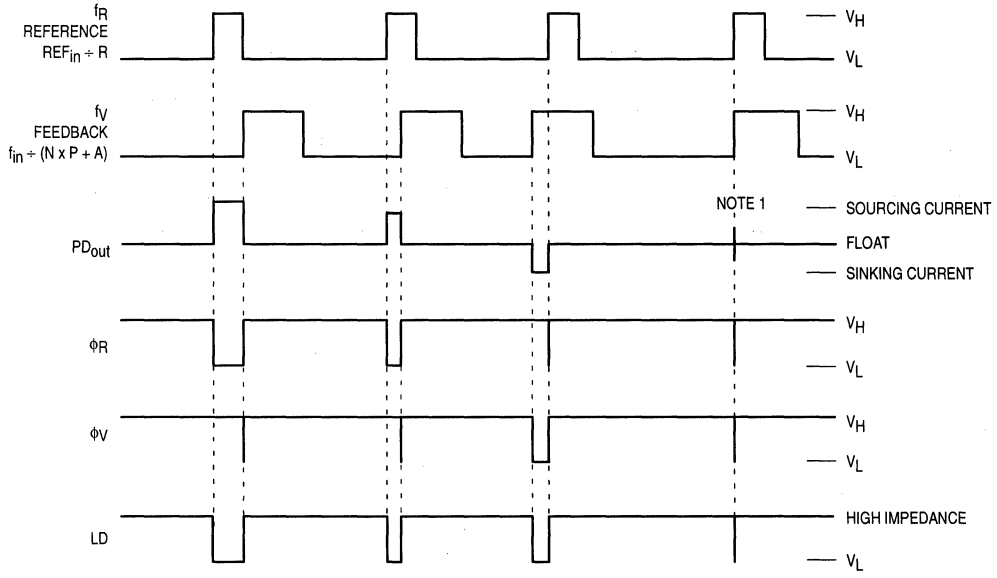
1. A power-on initialize circuit forces the Output A function to default to Data Out.
2. The values programmed for the N counter must be greater than or equal to the values programmed for the A counter. This results in a total divide value = N x P + A where N is the value programmed for the N counter, P is 32 if bit A20 is low or 64 if A20 is high, and A is the value programmed for the A counter.
3. At this point, the three new bytes are transferred to the A register if bit A23 is a "0" or A′ register if A23 is a "1". In addition, the 13 LSBs in the first buffer of the R register are transferred to the R register's relative second buffer, Rs or Rs′. Thus, the R, N, and A (or R′, N′, and A′) counters can be presented new divide ratios at the same time. The first buffer of the R register is not affected. The C or C′ registers are not affected.
4. A "0" for the Steering bit allows selection of f_R, f_V, Data Out, or Port by bits A21 and A22. A "1" for the Steering bit allows selection of $f_{R'}$, $f_{V'}$, Data Out, or Port.



NOTES:

1. Bits R15 – R13 control the configurable "Buffer and Control" block (see Block Diagram).
2. Bits R12 – R0 control the "13–stage R counter" blocks (see Block Diagram).
3. A power–on initialize circuit forces a default REF_{in} to REF_{out} ratio of eight.
4. At this point, bits R13, R14, and R15 are stored and sent to the "Buffer and Control" block in the Block Diagram. Bits R0 – R12 are loaded into the first buffer in the double–buffered section of the R register. Therefore, the R or R′ counter divide ratio is not altered yet and retains the previous ratio loaded. The C, C′, A, and A′ registers are not affected.
5. Bits R0 – R12 are transferred to the second buffer of the R register (Rs in the Block Diagram) on a subsequent 24–bit write to the A register. The bits are transferred to Rs′ on a subsequent 24–bit write to the A′ register. The respective R counter begins dividing by the new ratio after completing the rest of its present count cycle.
6. Allows direct access to reference input of phase/frequency detectors.

Figure 16. R Register Access and Format (16 Clock Cycles are Used)



NOTES:
1. At this point, when both f_R and f_V are in phase, the output source and sink circuits are turned on for a short interval.
2. The PD_{out} either sources or sinks current during out–of–lock conditions. When locked in phase and frequency, the output is mostly in a floating condition and the voltage at that pin is determined by the low–pass filter capacitor. PD_{out}, ϕR, and ϕV are shown with the polarity bit (POL) = low; see Figure 14 for POL.
3. V_H = High voltage level, V_L = Low voltage level.
4. The waveforms are applicable to both the main PLL and PLL′.

Figure 17. Phase/Frequency Detectors and Lock Detector Output Waveforms

CRYSTAL OSCILLATOR CONSIDERATIONS

The following options may be considered to provide a reference frequency to Motorola's CMOS frequency synthesizers.

Use of a Hybrid Crystal Oscillator

Commercially available temperature–compensated crystal oscillators (TCXOs) or crystal–controlled data clock oscillators provide very stable reference frequencies. An oscillator capable of CMOS logic levels at the output may be direct or dc coupled to REF_{in}. If the oscillator does not have CMOS logic levels on the outputs, capacitive or ac coupling to REF_{in} must be used. See Figure 8.

For additional information about TCXOs and data clock oscillators, please consult the latest version of the *eem Electronic Engineers Master Catalog,* the *Gold Book,* or similar publications.

Design an Off–Chip Reference

The user may design an off–chip crystal oscillator using discrete transistors or ICs specifically developed for crystal oscillator applications, such as the MC12061 MECL device. The reference signal from the MECL device is ac coupled to REF_{in}. (See Figure 8.) For large amplitude signals (standard CMOS logic levels), dc coupling may be used.

Use of the On–Chip Oscillator Circuitry

The on–chip amplifier (a digital inverter) along with an appropriate crystal may be used to provide a reference source frequency. A fundamental mode crystal, parallel resonant at the desired operating frequency, should be connected as shown in Figure 18.

The crystal should be specified for a loading capacitance, C_L, which does not exceed approximately 20 pF when used near the highest operating frequency of the MC145220. Assuming R1 = 0 Ω, the shunt load capacitance, C_L, presented across the crystal can be estimated to be:

$$C_L = \frac{C_{in}C_{out}}{C_{in} + C_{out}} + C_a + C_{stray} + \frac{C1 \cdot C2}{C1 + C2}$$

where

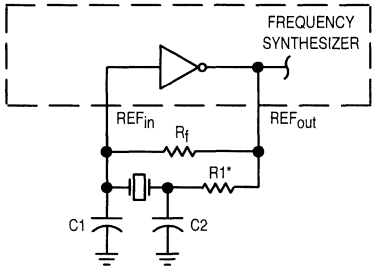
C_{in} = 5 pF (see Figure 19)
C_{out} = 6 pF (see Figure 19)
C_a = 1 pF (see Figure 19)
C1 and C2 = external capacitors (see Figure 18)
C_{stray} = the total equivalent external circuit stray capacitance appearing across the crystal terminals

The oscillator can be "trimmed" on–frequency by making either a portion or all of C1 variable. The crystal and associated components must be located as close as possible to the REF_{in} and REF_{out} pins to minimize distortion, stray capacitance, stray inductance, and startup stabilization time. Circuit stray capacitance can also be handled by adding the appropriate stray value to the values for C_{in} and C_{out}. For this approach, the term C_{stray} becomes zero in the above expression for C_L.

Power is dissipated in the effective series resistance of the crystal, R_e, in Figure 20. The maximum drive level specified by the crystal manufacturer represents the maximum stress that the crystal can withstand without damage or excessive shift in operating frequency. R1 in Figure 18 limits the drive level. The use of R1 is not necessary in most cases.

To verify that the maximum dc supply voltage does not cause the crystal to be overdriven, monitor the output frequency (f_R) at Output A as a function of supply voltage. (REF_{out} is not used because loading impacts the oscillator.) The frequency should increase very slightly as the dc supply voltage is increased. An overdriven crystal decreases in frequency or becomes unstable with an increase in supply voltage. The operating supply voltage must be reduced or R1 must be increased in value if the overdriven condition exists. Note that the oscillator start–up time is proportional to the value of R1.

Through the process of supplying crystals for use with CMOS inverters, many crystal manufacturers have developed expertise in CMOS oscillator design with crystals. Discussions with such manufacturers can prove very helpful. See Table 4.



* May be needed in certain cases. See text.

Figure 18. Pierce Crystal Oscillator Circuit

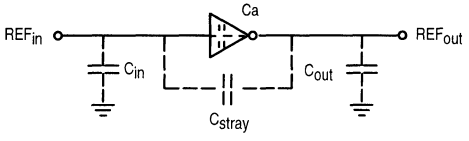
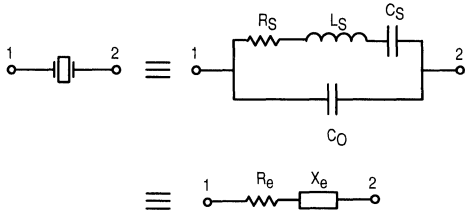


Figure 19. Parasitic Capacitances of the Amplifier and C_{stray}



NOTE: Values are supplied by crystal manufacturer (parallel resonant crystal).

Figure 20. Equivalent Crystal Networks

RECOMMENDED READING

Technical Note TN–24, Statek Corp.

Technical Note TN–7, Statek Corp.

E. Hafner, "The Piezoelectric Crystal Unit – Definitions and Method of Measurement", *Proc. IEEE,* Vol. 57, No. 2, Feb. 1969.

D. Kemper, L. Rosine, "Quartz Crystals for Frequency Control", *Electro–Technology,* June 1969.

P. J. Ottowitz, "A Guide to Crystal Selection", *Electronic Design*, May 1966.

D. Babin, "Designing Crystal Oscillators", *Machine Design*, March 7, 1985.

D. Babin, "Guidelines for Crystal Oscillator Design", *Machine Design*, April 25, 1985.

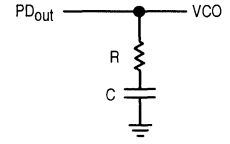
Table 4. Partial List of Crystal Manufacturers

Name	Address	Phone
United States Crystal Corp.	3605 McCart Ave., Ft. Worth, TX 76110	(817) 921–3013
Crystek Crystal	2351 Crystal Dr., Ft. Myers, FL 33907	(813) 936–2109
Statek Corp.	512 N. Main St., Orange, CA 92668	(714) 639–7810
Fox Electronics	5570 Enterprise Parkway, Ft. Myers, FL 33905	(813) 693–0099

NOTE: Motorola cannot recommend one supplier over another and in no way suggests that this is a complete listing of crystal manufacturers.

PHASE–LOCKED LOOP — LOW–PASS FILTER DESIGN

(A)



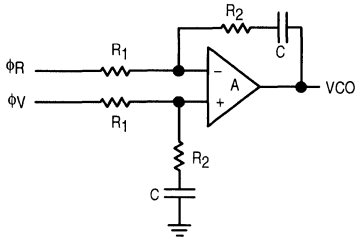
$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NC}}$$

$$\zeta = \frac{R}{2}\sqrt{\frac{K_\phi K_{VCO} C}{N}} = \frac{\omega_n RC}{2}$$

$$Z(s) = \frac{1 + sRC}{sC}$$

NOTE:
For (A), using K_ϕ in amps per radian with the filter's impedance transfer function, Z(s), maintains units of volts per radian for the detector/filter combination. Additional sideband filtering can be accomplished by adding a capacitor C′ across R. The corner $\omega_c = 1/RC'$ should be chosen such that ω_n is not significantly affected.

(B)



$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NCR_1}}$$

$$\zeta = \frac{\omega_n R_2 C}{2}$$

ASSUMING GAIN A IS VERY LARGE, THEN:

$$Z(s) = \frac{R_2 sC + 1}{R_1 sC}$$

NOTE:
For (B), R_1 is frequently split into two series resistors; each resistor is equal to R_1 divided by 2. A capacitor C_C is then placed from the midpoint to ground to further filter the error pulses. The value of C_C should be such that the corner frequency of this network does not significantly affect ω_n.

DEFINITIONS:
N = Total Division Ratio in Feedback Loop
K_ϕ (Phase Detector Gain) = $I_{PDout}/2\pi$ amps per radian for PD_{out}
K_ϕ (Phase Detector Gain) = $V+/2\pi$ volts per radian for ϕV and ϕR

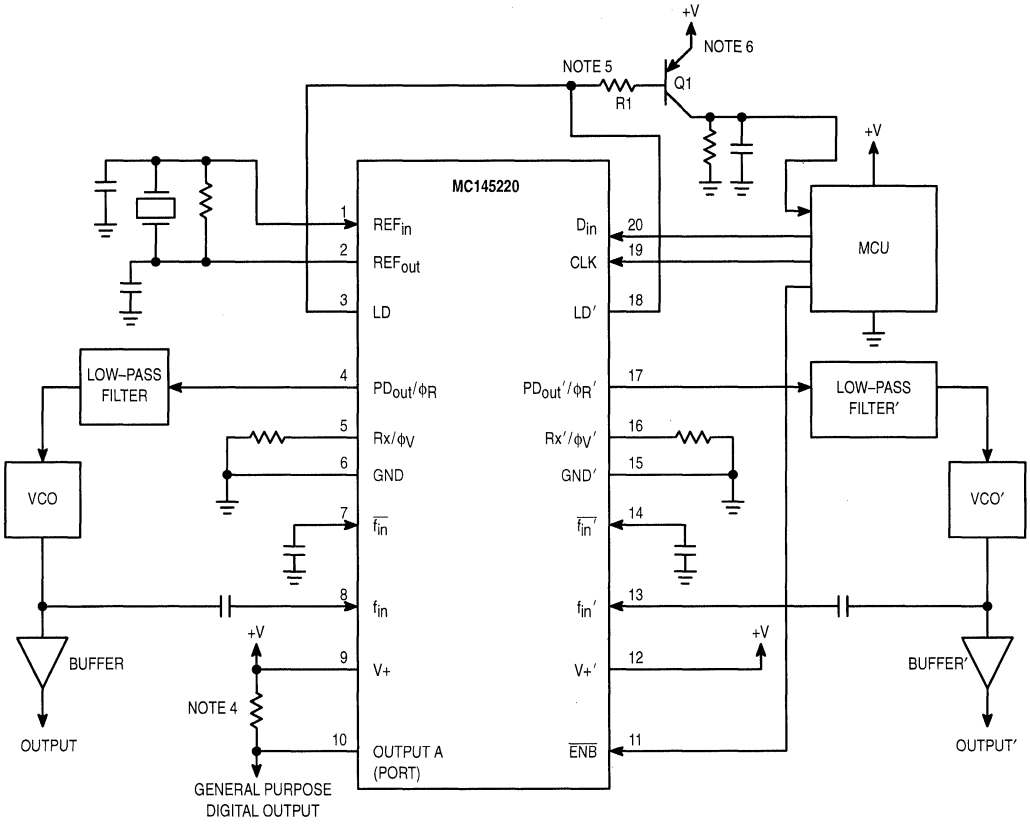
K_{VCO} (VCO Transfer Function) = $\frac{2\pi\Delta f_{VCO}}{\Delta V_{VCO}}$ radians per volt

For a nominal design starting point, the user might consider a damping factor $\zeta \approx 0.7$ and a natural loop frequency $\omega_n \approx (2\pi f_R/50)$ where f_R is the frequency at the phase detector input. Larger ω_n values result in faster loop lock times and, for similar sideband filtering, higher f_R–related VCO sidebands.

Either loop filter (A) or (B) is frequently followed by additional sideband filtering to further attenuate f_R–related VCO sidebands. This additional filtering may be active or passive.

RECOMMENDED READING:

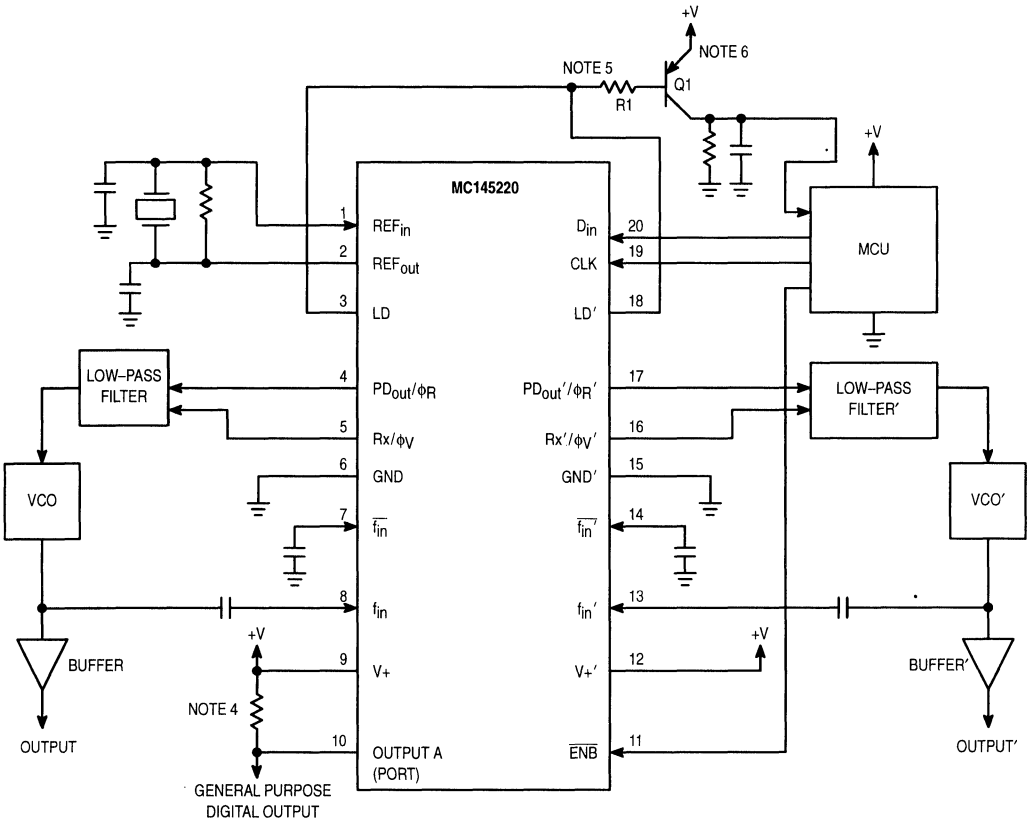
Gardner, Floyd M., *Phaselock Techniques (second edition).* New York, Wiley–Interscience, 1979.
Manassewitsch, Vadim, *Frequency Synthesizers: Theory and Design (second edition).* New York, Wiley–Interscience, 1980.
Blanchard, Alain, *Phase–Locked Loops: Application to Coherent Receiver Design.* New York, Wiley–Interscience, 1976.
Egan, William F., *Frequency Synthesis by Phase Lock.* New York, Wiley–Interscience, 1981.
Rohde, Ulrich L., *Digital PLL Frequency Synthesizers Theory and Design.* Englewood Cliffs, NJ, Prentice–Hall, 1983.
Berlin, Howard M., *Design of Phase–Locked Loop Circuits, with Experiments.* Indianapolis, Howard W. Sams and Co., 1978.
Kinley, Harold, *The PLL Synthesizer Cookbook.* Blue Ridge Summit, PA, Tab Books, 1980.
Seidman, Arthur H., *Integrated Circuits Applications Handbook*, Chapter 17, pp. 538–586. New York, John Wiley & Sons.
Fadrhons, Jan, "Design and Analyze PLLs on a Programmable Calculator," *EDN.* March 5, 1980.
AN535, Phase–Locked Loop Design Fundamentals, Motorola Semiconductor Products, Inc., 1970.
AR254, Phase–Locked Loop Design Articles, Motorola Semiconductor Products, Inc., Reprinted with permission from *Electronic Design,* 1987.
AN1253, An Improved PLL Design Method Without ω_n and ζ, Motorola Semiconductor Products, Inc., 1995.



NOTES:

1. The PD_{out} output is fed to an external loop filter. See the Phase–Locked Loop — Low–Pass Filter Design page for additional information.
2. For optimum performance, bypass the V+ and V+′ pins to GND and GND′ with low–inductance capacitors.
3. The R counter is programmed for a divide value = REF_{in} /f_R. Typically, f_R is the tuning resolution required for the VCO. Also, the VCO frequency divided by $f_R = N_T = N \bullet P + A$; this determines the values (N, A) that must be programmed into the N and A counters, respectively. P is the lower divide ratio of the dual–modulus prescaler (i.e., 32 or 64).
4. Pull–up voltage must be at the same potential as the V+ pin or less. Pull–up device other than a resistor may be used. (Pull–up device not required when Output A is configured as f_R, f_R′, f_V, f_V′ DATA OUT.)
5. LD and LD′ are open–drain outputs. This allows the wired–OR configuration shown. Note that R1 and Q1 form the "pull–up device".
6. Use of Q1 is optional and depends on loading.

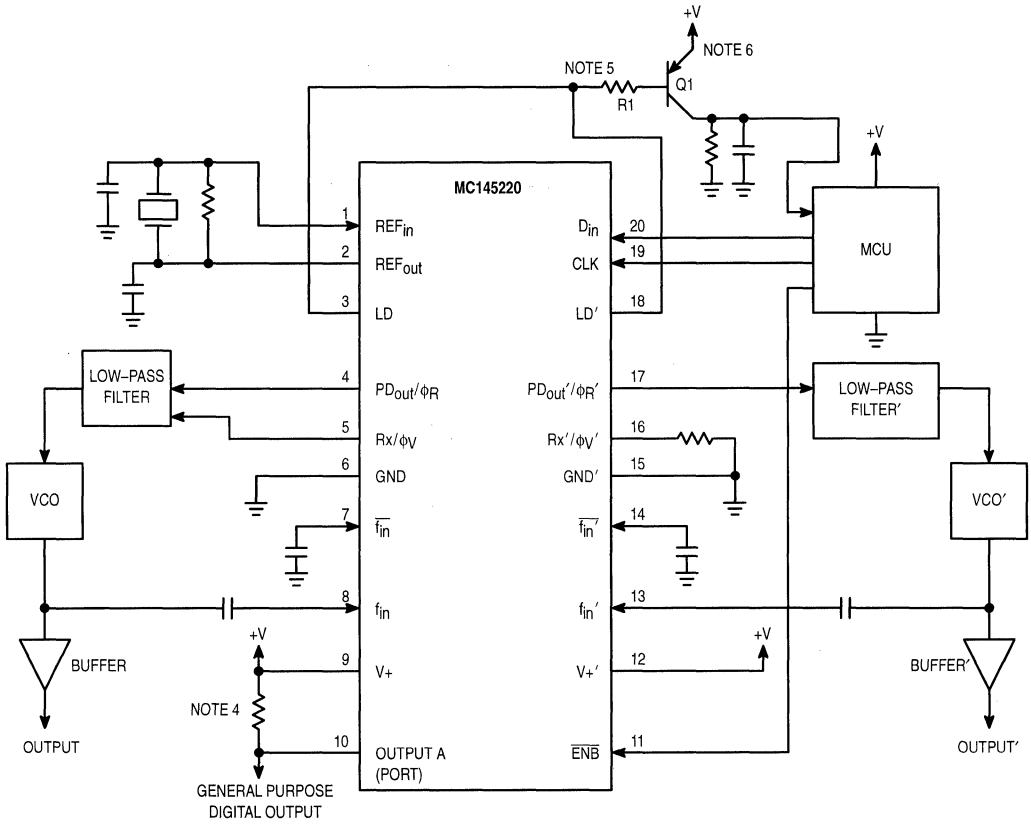
Figure 21. Application Showing Use of the Two Single–Ended Phase/Frequency Detectors



NOTES:

1. The ϕ_R and ϕ_V outputs are fed to an external combiner/loop filter. See the Phase–Locked Loop — Low–Pass Filter Design page for additional information. The ϕ_R and ϕ_V outputs swing rail–to–rail. Therefore, the user should be careful not to exceed the common mode input range of the op amp used in the combiner/loop filter.
2. For optimum performance, bypass the V+ and V+′ pins to GND and GND′ with low–inductance capacitors.
3. The R counter is programmed for a divide value = REF_{in} /f_R. Typically, f_R is the tuning resolution required for the VCO. Also, the VCO frequency divided by $f_R = N_T = N \bullet P + A$; this determines the values (N, A) that must be programmed into the N and A counters, respectively. P is the lower divide ratio of the dual–modulus prescaler (i.e., 32 or 64).
4. Pull–up voltage must be at the same potential as the V+ pin or less. Pull–up device other than a resistor may be used. (Pull–up device not required when Output A is configured as f_R, f_R′, f_V, f_V′ DATA OUT.)
5. LD and LD′ are open–drain outputs. This allows the wired–OR configuration shown. Note that R1 and Q1 form the "pull–up device".
6. Use of Q1 is optional and depends on loading.

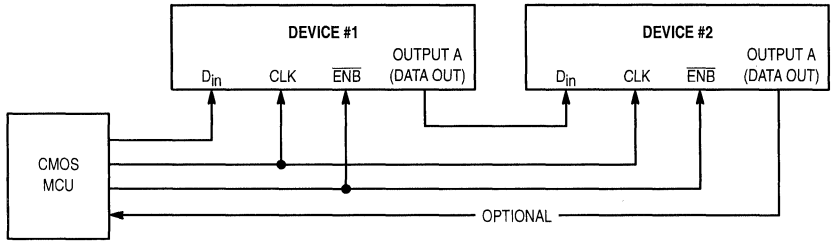
Figure 22. Application Showing Use of the Two Double–Ended Phase/Frequency Detectors



NOTES:

1. See the Phase–Locked Loop — Low–Pass Filter Design page for additional information.
2. For optimum performance, bypass the V+ and V+′ pins to GND and GND′ with low–inductance capacitors.
3. The R counter is programmed for a divide value = REF_{in} /f_R. Typically, f_R is the tuning resolution required for the VCO. Also, the VCO frequency divided by $f_R = N_T = N \bullet P + A$; this determines the values (N, A) that must be programmed into the N and A counters, respectively. P is the lower divide ratio of the dual–modulus prescaler (i.e., 32 or 64).
4. Pull–up voltage must be at the same potential as the V+ pin or less. Pull–up device other than a resistor may be used. (Pull–up device not required when Output A is configured as f_R, $f_{R'}$, f_V, $f_{V'}$ DATA OUT.)
5. LD and LD′ are open–drain outputs. This allows the wired–OR configuration shown. Note that R1 and Q1 form the "pull–up device".
6. Use of Q1 is optional and depends on loading.

Figure 23. Application Showing Use of Both the Single– and Double–Ended Phase/Frequency Detectors



NOTE: See related Figures 25, 26, and 27.

Figure 24. Cascading Two Devices

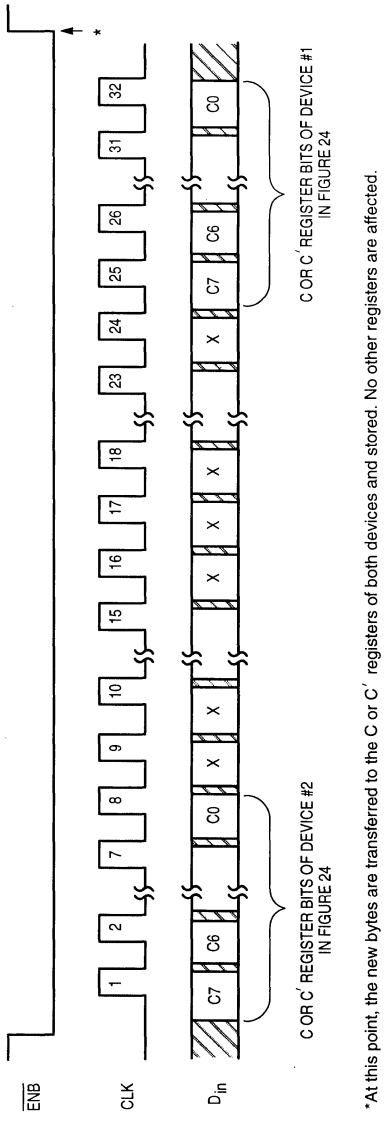
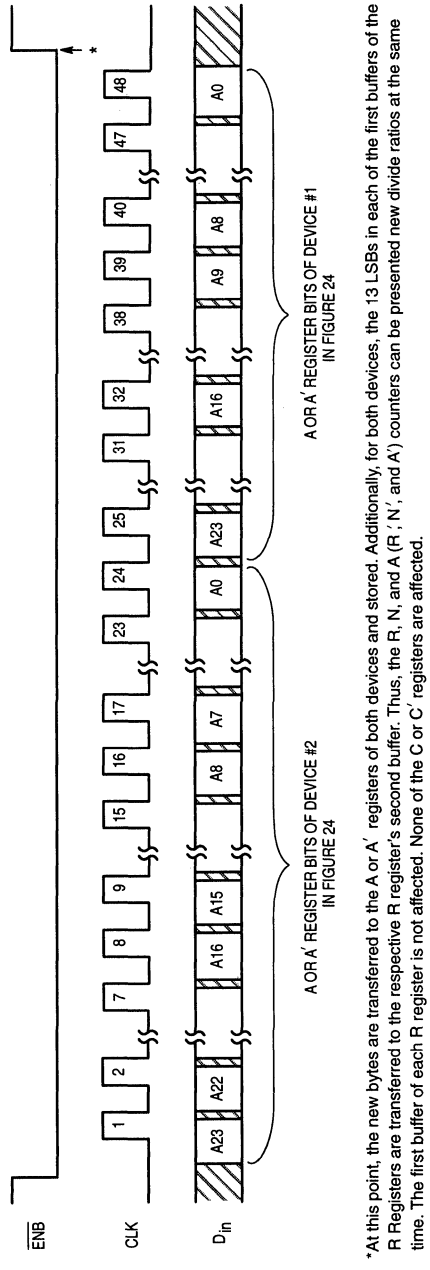


Figure 25. Accessing the C or C′ Registers of Two Cascaded MC145220 Devices (32 Clock Cycles are Used)



*At this point, the new bytes are transferred to the A or A′ registers of both devices and stored. Additionally, for both devices, the 13 LSBs in each of the first buffers of the R Registers are transferred to the respective R register's second buffer. Thus, the R, N, and A (R′, N′, and A′) counters can be presented new divide ratios at the same time. The first buffer of each R register is not affected. None of the C or C′ registers are affected.

Figure 26. Accessing the A or A′ Registers of Two Cascaded MC145220 Devices (48 Clock Cycles are Used)

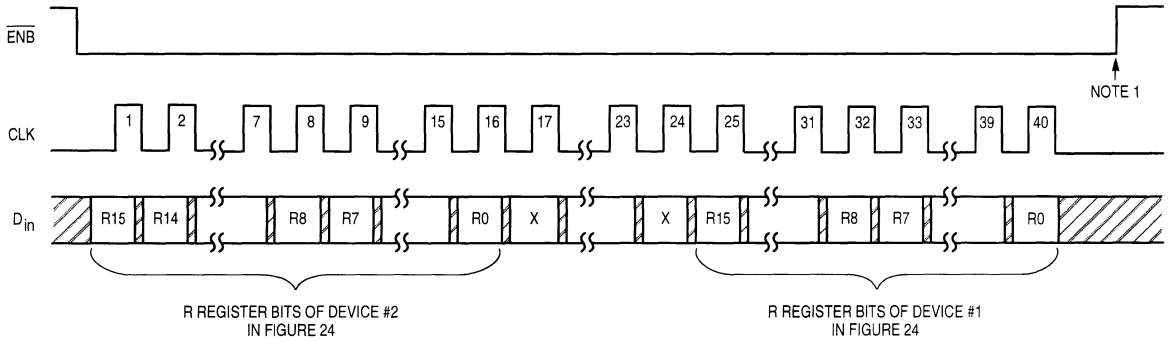


Figure 27. Accessing the R Registers of Two Cascaded MC145220 Devices (40 Clock Cycles are Used)

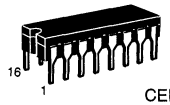
NOTES APPLICABLE TO EACH DEVICE:

1. At this point, bits R13, R14, and R15 are stored and sent to the Buffer and Control block in the Block Diagram. Bits R0 through R12 are loaded into the first buffer in the double–buffered section of the R register. Therefore, the R and R′ counter divide ratios are not altered yet and retain the previous ratios loaded. The other registers are not affected.
2. See note of Figure 26 for the method of loading the second buffers in the R register to achieve new divide ratios.

MC145402

Advance Information

Serial 13-Bit Linear Codec (A/D and D/A)



L SUFFIX
CERAMIC PACKAGE
CASE 620

ORDERING INFORMATION

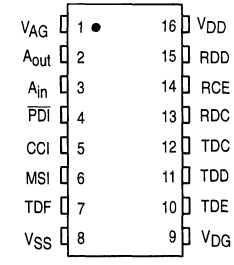
MC145402L Ceramic Package

2

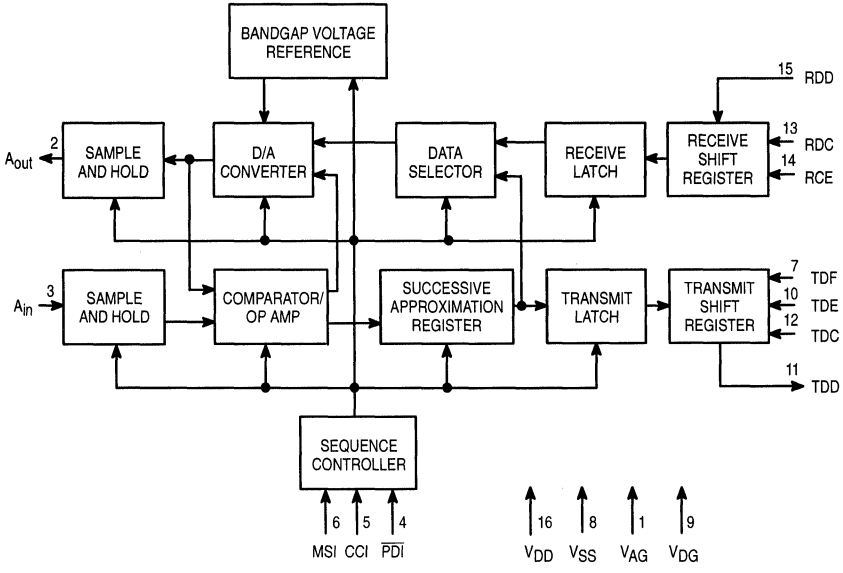
The MC145402 is a 13–bit linear monotonic digital–to–analog and analog–to–digital converter implemented in a single silicon–gate CMOS IC. Potential applications include analog interface for Digital Signal Processor (DSP) applications, high speed modems, telephone systems, SONAR, Adaptive Differential Pulse Code Modulation (ADPCM) converters, echo cancellers, repeaters, voice synthesizers, and music synthesizers.

- 60 dB Signal–to–(Noise Plus Distortion) Ratio Typical
- On–Chip Precision Voltage Reference
- Serial Data Ports
- Two's Complement Coding
- ± 5 V Supply Operation
- Sample Rates from 100 Hz to 16 kHz (Both A/D and D/A), 100 Hz to 21.3 kHz (A/D Only), and 100 Hz to 64 kHz (D/A Only)
- Input Sample and Hold Provided On–Chip
- 5 V CMOS Inputs; Outputs Capable of Driving Two LSTTL Loads
- Available in a 16–Pin DIP
- Low Power Consumption: 50 mW Typical, 1 mW Power–Down

PIN ASSIGNMENT



BLOCK DIAGRAM



This document contains information on a new product. Specifications and information herein are subject to change without notice.

ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	$V_{DD} - V_{SS}$	– 0.5 to 11	V
Voltage, Any Pin to VSS	V	– 0.5 to V_{DD} + 0.5	V
DC Current Drain per Pin (Excluding V_{DD}, V_{SS})	I	10	mA
Operating Temperature Range	T_A	– 40 to + 85	°C
Storage Temperature Range	T_{stg}	– 85 to + 150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electrical fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$ on analog inputs/outputs and $V_{DG} \le (V_{in}$ or $V_{out}) \le V_{DD}$ on digital inputs/outputs. Reliability of operation is enhanced if unused digital inputs are tied to an appropriate logic voltage level (e.g., either V_{DG} or V_{DD}) and unused analog Inputs are tied to V_{AG}.

2

RECOMMENDED OPERATING CONDITIONS

Parameter		Pins	0 to 70°C Min	25°C Typ	0 to 70°C Max	Unit
DC Supply Voltage		V_{DD} to V_{SS}	9.5	10	10.5	V
Power Dissipation, $\overline{PDI}$ = 1		V_{DD} to V_{SS}	—	50	80	mW
Power Dissipation, $\overline{PDI}$ = 0		V_{DD} to V_{SS}	—	1	5	mW
Conversion Rate	Full Cycle A/D and D/A	MSI	0.1	—	16	kHz
	Short Cycle A/D		0.1	—	21.3	
	Short Cycle D/A		0.1	—	64	
Conversion Sequence Rate		CCI	3.2	—	512	kHz
Data Rate		TDC, RDC	16 x f_{MSI}	—	4096	kHz
Full Scale Analog Levels (Referenced to 600 Ω)		AI, AO	—	3.27	—	Vp
			—	9.5	—	dBm

DIGITAL ELECTRICAL CHARACTERISTICS (V_{DD} = 5 V, V_{SS} = – 5 V, V_{AG} = V_{DG} = 0 V, T_A = 0 to 70°C)

Characteristic			Symbol	Min	Max	Unit
High Level Input Voltage			V_{IH}	3.5	—	V
Low Level Input Voltage			V_{IL}	—	1.5	V
Input Current			I_{in}	—	± 1.0	μA
Input Capacitance			C_{in}	—	10	pF
High Level Output Voltage	TDD	I_{out} = – 20 μA	V_{OH}	4.9	—	V
		I_{out} = – 1 mA		4.3	—	
Low Level Output Voltage	TDD	I_{out} = – 20 μA	V_{OL}	—	0.1	V
		I_{out} = – 1 mA		—	0.4	

CODER AND DECODER PERFORMANCE (V_{DD} = 5 V ± 5%, V_{SS} = – 5 V ± 5%, V_{AG} = V_{DG} = 0 V,
0 dBm0 = 1.60 Vrms = 6.30 dBm (600 Ω), T_A = 0 to 70°C, MSI = TDE = RCE = 8 kHz, TDC = RDC = 2.048 MHz, CCI = 256 kHz)

Characteristic		Coder (A/D)			Decoder (D/A)			Unit
		Min	Typ	Max	Min	Typ	Max	
Resolution		13	—	13	13	—	13	Bits
Conversion Time	Full Cycle A/D and D/A	62.5	—	10,000	62.5	—	10,000	µs
	Short Cycle A/D	46.9	—	10,000	—	—	—	
	Short Cycle D/A	—	—	—	15.6	—	10,000	
Differential Nonlinearity		—	—	± 1	—	—	± 1	LSB
Gain Error		– 0.35	—	+ 0.35	– 0.35	—	+ 0.35	dB
Offset		– 15	—	+ 15	—	—	—	LSB
		—	—	—	– 20	—	+ 20	mV
Idle Channel Noise, 3 kHz Low–Pass		—	– 75	—	—	– 79	—	dBm0
Signal–to–Noise	3.2 dBm0	—	61	—	—	62	—	dB
(Referenced to 1.02 kHz through	0 dBm0	—	60	—	—	60	—	
a f_{MSI}/2 Low–Pass Filter)	– 10 dBm0	—	57	—	—	59	—	
	– 20 dBm0	—	50	—	—	52	—	
	– 30 dBm0	—	40	—	—	42	—	
	– 40 dBm0	—	30	—	—	32	—	
	– 50 dBm0	—	20	—	—	22	—	

ANALOG ELECTRICAL CHARACTERISTICS (V_{DD} = 5 V ± 5%, V_{SS} = – 5 V ± 5%, V_{AG} = V_{DG} = 0 V,
0 dBm0 = 1.60 Vrms = 6.30 dBm (600 Ω), T_A = 0 to 70°C, MSI = TDE = RCE = 8 kHz, TDC = RDC = 2.048 MHz, CCI = 256 kHz)

Characteristic	Pin	Symbol	Min	Typ	Max	Unit
Input Current	AI	I_{in}	—	0.01	± 1	µA
AC Input Impedance	AI	Z_{in}	0.5	—	—	MΩ
Input Capacitance	AI	C_{in}	—	—	15	pF
Output Voltage Range	AO	V_{out}	– 3.4	—	3.4	V
Power Supply Rejection Ratio (100 mV RMS on V_{DD} or V_{SS}, 0 – 50 kHz)	AO, TDD	PSRR	—	40	—	dB
Crosstalk, A_{in} to A_{out} and RDD to TDD Referenced to 0 dBm0 @ 1.02 kHz	AO, TDD	—	—	– 90	– 75	dB
Slew Rate	AO	SR	1.5	3	—	V/µs
Settling Time (Full Scale)	AO	t_{settle}	—	8	—	µs

SWITCHING CHARACTERISTICS

(V_{DD} = + 5 V ± 5%, V_{SS} = – 5 V ± 5%, V_{AG} = V_{DG} = 0 V, T_A = 0 to 70°C, C_L = 50 pF, See Figure 1)

Characteristic		Symbol	Min	Max	Unit
Input Rise Time	RCE, RDC, TDC, TDE, CCI, MSI	t_r	—	100	ns
Input Fall Time	RCE, RDC, TDC, TDE, CCI, MSI	t_f	—	100	ns
Output Rise Time	TDD	t_r	—	80	ns
Output Fall Time	TDD	t_f	—	80	ns
Pulse Width High	RDC, MSI, CCI, TDC, RCE	t_{wH}	100	—	ns
Pulse Width Low	TDE, MSI, TDC, RCE, RDC	t_{wL}	100	—	ns
CCI Pulse Width Low		t_{wL}	500	—	ns
MSI Clock Frequency		f_{MSI}	0.1	64	kHz
CCI Clock Frequency		f_{CCI}	3.2	512	kHz
TDC and RDC Clock Frequency		f_{DC}	16 x f_{MSI}	4.1	MHz
TDC Rising Edge to TDD Data Valid During TDE High		t_{p1}	—	150	ns
TDE Rising Edge to TDD Data Valid During TDC High		t_{p2}	—	150	ns
TDE Rising Edge to TDD Low–Impedance Propagation Delay		t_{p3}	0	100	ns
TDE Falling Edge to TDD High–Impedance Propagation Delay		t_{p4}	—	40	ns
TDE Rising Edge to TDC Falling Edge Setup Time		t_{su1} t_{su2}	20 100	— —	ns
RDC Bit 0 Falling Edge to Last CCI Falling Edge Prior to MSI		t_{su3}	20	—	ns
MSI Rising Edge to CCI Falling Edge Setup Time		t_{su4} t_{su5}	20 100	— —	ns
Last CCI Rising Edge (Prior to MSI) to TDE Rising Edge		t_{su6}	100	—	ns
Last CCI Rising Edge (Prior to MSI) to First TDC Rising Edge		$t_{su6'}$	100	—	ns
First TDC Falling Edge to Last CCI Rising Edge Prior to MSI		t_{su7}	0	—	ns
RCE Rising Edge to RDC Falling Edge Setup Time		t_{su8} t_{su9}	20 100	— —	ns
RDD Valid to RDC Falling Edge Setup Time		t_{su10}	60	—	ns
RDD Hold Time from RDC Falling Edge		t_h	100	—	ns

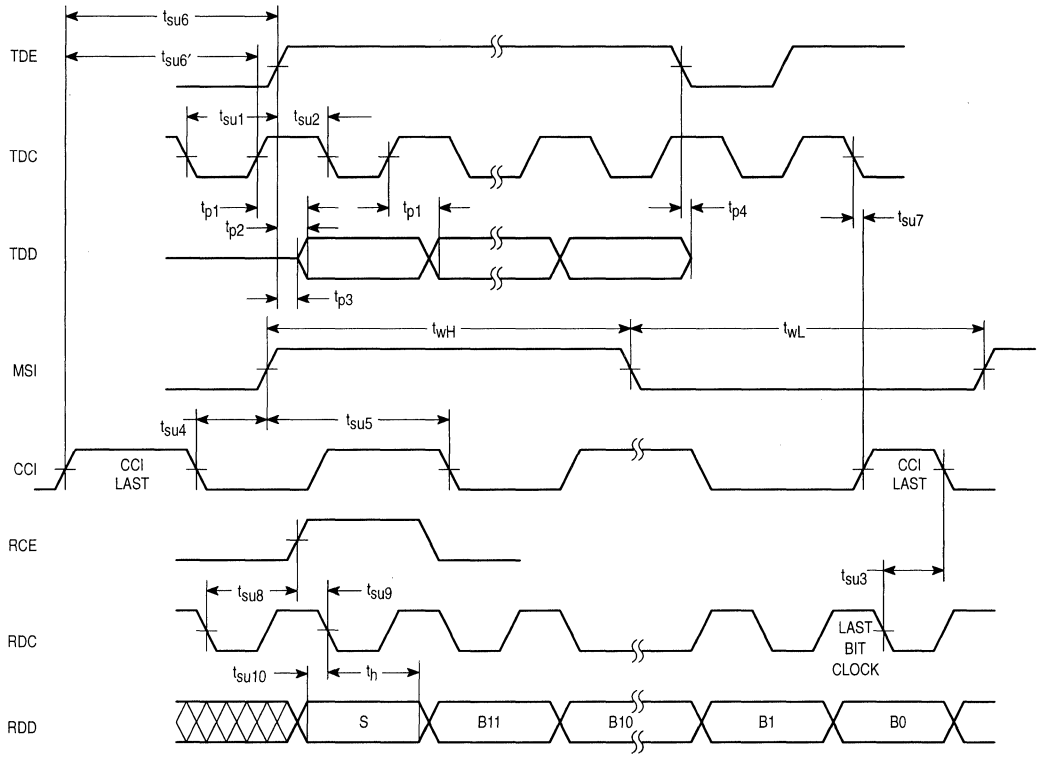


Figure 1. AC Timing Diagram

PIN DESCRIPTIONS

V_{DD}
Positive Supply (Pin 16)

The most positive power supply, typically + 5 V in split power supply configurations, or + 10 V in single supply systems.

V_{SS}
Negative Supply (Pin 8)

The most negative power supply, typically – 5 V in split power supply configurations, or 0 V in single supply systems.

V_{AG}
Analog Ground (Pin 1)

This is the analog signal reference point. This pin is normally tied to 0 V in split supply operation or $V_{DD}/2$ in single supply systems.

V_{DG}
Digital Ground (Pin 9)

This is the ground reference for all of the digital input and output pins. CMOS compatible logic signals swing from V_{DG} to V_{DD} where V_{DG} can be established anywhere from V_{DD} – 4.75 V to V_{SS}.

A_{out}
Analog Output (Pin 2)

This is the output of the decoder's sample and hold circuit and is a 100% duty cycle analog output of the last digital word received and decoded by the decoder. A_{out} is updated approximately 60 ns after the rising edge of the last CCI prior to MSI (see Figure 2). A_{out} is capable of driving a 10 kΩ, 50 pF load.

A_{in}
Analog Input (Pin 3)

This is the high–impedance input to the coder. An A/D cycle begins on the first falling edge of CCI following the rising edge of MSI. A_{in} is sampled approximately 50 ns after the rising edge of CCI prior to the start of the A/D cycle.

$\overline{PDI}$
Power–Down Input (Pin 4)

In normal operation this Input should be tied high. A logic low on this input puts the device into a minimum power dissipation mode. During power–down, all functions stop. Two complete MSI conversion cycles are required to establish normal operation after leaving the power–down mode.

CCI
Convert Clock Input (Pin 5)

This input controls the complete conversion sequence during one MSI cycle and must receive a clock which is 32 times the frequency of MSI. The only exception to 32 times the frequency of MSI is during short–cycle operation. See **General Modes of Operation** section. CCI must be synchronous and approximately rising edge aligned with MSI.

MSI
Master Sync Input (Pin 6)

This pin determines the conversion rate for both the coder and the decoder. One A/D and D/A conversion takes place during each period of the digital clock applied to this input (except in short–cycle operation, see **General Modes of Operation** section). MSI must be synchronous and approximately rising edge aligned with CCI.

TDC
Transmit Data Clock (Pin 12)

Digital data from the coder is serially transmitted from TDD on rising TDC edges whenever TDE is a logic high. TDC must be approximately rising edge aligned with TDE. Generally, if TDC is low when TDE rises, the first rising edge of TDC clocks the first data bit. If TDC is high when TDE rises, the first bit will be clocked by TDE and the first rising edge of TDC after TDE rises will clock out the second data bit.

TDE
Transmit Data Enable (Pin 10)

This pin is used to initiate the serial transfer of data from the coder and provides three–state control of the TDD pin. The rising edge of TDE (or TDC if it follows TDE) signals the start of data transfer from the TDD pin. A resulting high logic level on TDE also releases TDD from its high–impedance state. TDE must remain high throughout the data transfer to keep TDD in the low–impedance state and must return to a low state prior to each data transfer. If TDE remains high for more than 16 TDC clocks, the 16 bits of TDD data will be recirculated. (Note: The A/D cycle begins on the first falling edge of CCI after the rising edge of MSI. The internal transmit latch is updated one and one half CCI periods prior to the start of the A/D cycle. A pulse generated by the logical AND of TDE and the first TDC transfers data to the transmit shift register, and this pulse must not occur when the transmit latch is updated. See Figure 2 and see t_{su6}, $t_{su6'}$, and t_{su7} of Figure 1.

TDD
Transmit Digital Data (Pin 11)

This is the three–state output data pin from the coder and is controlled by the TDE and TDC pins. TDD is in the high–impedance state whenever TDE is a logic low. The first data bit is output from TDD on the rising edge of TDE (or TDC if it follows TDE) and each subsequent bit is output on rising edges of TDC. Two output data formats are available as described in the TDF pin description below.

TDF
Transmit Data Format (Pin 7)

The 13–bit digital output of the coder is available in one of two 16–bit two's complement formats as determined by the state of this pin. A logic 0 at this pin causes the data from TDD to be in a 16–bit sign–extended format as follows: SSSSM ... L where S, M, and L represent the sign, most significant bit, and the least significant bit, respectively. A logic 1 on this pin formats the data as follows: SM ... LSSS (see Figure 3). RDD data is not affected by the state of this pin and if a "digital loopback" is needed (TDD data looped back into RDD), this pin should be high.

RDC
Receive Data Clock (Pin 13)

Receive digital data is accepted by the decoder on the first 13 falling edges of RDC after an RCE rising edge.

RCE
Receive Clock Enable (Pin 14)

This pin identifies the beginning of a data transfer into the RDD pin of the decoder. The first 13 falling edges of RDC after an RCE rising edge will clock data into the decoder data input, RDD. RCE must return low prior to each data transfer. Since receive data is latched into the receive latch on the last CCI falling edge prior to MSI, data transfers may not span this falling edge of CCI without loss of data.

RDD
Receive Digital Data (Pin 15)

This pin is the data input to the decoder and is controlled by the RDC and RCE pins described above. Two's complement data are loaded in the following sequence: SM ... L where S, M, and L represent the sign, most significant bit, and the least significant bit, respectively. Only the first 13 bits clocked by RDC after RCE rises will be accepted for decoding. Any additional bits will be ignored (see Figure 3).

GENERAL INFORMATION

GENERAL MODES OF OPERATION

The MC145402 has three modes of operation; a "full" cycle mode and two "short" cycle modes. The full cycle mode allows simultaneous analog–to–digital (A/D) and digital–to–analog (D/A) operation. The short cycle modes allow either A/D only or D/A only operation. Two MSI cycles are required for the MC145402 to detect which operating mode has been selected. See Figure 2 for full versus short cycle clocking.

Full Cycle Operation

When operating in the full cycle mode, the MC145402 performs a 13–bit A/D conversion followed by a 13–bit D/A conversion. Full cycle operation is selected by using a CCI frequency that is 32 times the frequency of MSI. MSI is the sample rate frequency.

Short Cycle Analog–to–Digital Operation

If CCI is 24 times the frequency of MSI, short cycle analog–to–digital operation is selected. This allows a 13–bit A/D conversion only. In this mode, the D/A is not operational and any data applied to the RDD input is ignored.

Short Cycle Digital–to–Analog Operation

Short cycle digital–to–analog operation is selected by using a CCI clock frequency that is eight times the MSI sample rate. During short cycle D/A operation, A/D operation is disabled and digital data read from TDD is not valid.

CLOCKING RECOMMENDATIONS

For optimum differential nonlinearity performance, all data transitions on TDD and RDD should be limited to the first four CCI cycles following the rising edge of MSI. This may be achieved by setting MSI = TDE = RCE having a duration of 16 data clock cycles, and TDC = RDC ≥ 4 x CCI clock frequency. Figure 6 shows a circuit that generates this clocking configuration; see **Application Circuits** section.

SIGNAL TO DISTORTION RATIO

Figures 4 and 5 show graphs of typical signal to distortion ratios versus signal level for the MC145402. The presented data is referenced to a 1020 Hz input sinusoidal frequency with signal levels referenced to 600 Ω and transmission level point adjusted (e.g., 0 dBm0 at 600 Ω with a TLP of 6.30 dB is 4.53 V peak–to–peak). For comparison, ideal signal to noise ratios for 9–, 10–, 11–, 12–, and 13–bit A/D and D/A converters are also shown. The equation used for an ideal RMS to RMS signal to distortion ratio is:

$$S/D = N \times 6\ dB + 1.76\ dB$$

where N is the number of bits of resolution, 6 dB per bit, and $1.76 = 20\log(\sqrt{3}/\sqrt{2})$.

$(\sqrt{3}/\sqrt{2})$ is approximately the RMS to RMS ratio of a sine wave to white noise.

The signal to noise plus distortion ratio is measured through a brickwall low–pass filter set to the Nyquist frequency of the A/D and D/A sample rate. For an 8 kHz sample rate, the low–pass filter is set to block all signals above 4 kHz.

APPLICATION CIRCUITS

Figure 6 shows a typical circuit for generating the clock frequencies for the MC145402. This circuit uses an MC74HC4040 and a 2.048 MHz crystal to generate the 256 kHz frequency for internal sequencing, 1.024 MHz for the date clocks, and an 8 kHz sample frequency. A 4.096 MHz crystal could be used for a sample rate of 16 kHz.

Figure 7 shows the MC145402 interfaced to the DSP56000 digital signal processor. The DSP56000 can internally generate the clocks for the MC145402 using the SSI serial interface. SCK provides the sequencing and data clocks (non–gated continuous dock) and SC2 (setup as the Frame Sync Out, FSL = 0) provides the sample rate and data enables for the MC145402. The divide–by–four circuit to generate the CCI clock is recommended for optimum MC145402 performance, and allows the DSP56000 to clock data in and out of the MC145402 quickly, leaving time available for processing by the DSP before another sample is available. SC0 and SC1 could be used to gate the enables to select up to four devices on the SSI bus.

TELEPHONE SYSTEM TRANSMISSION LEVEL POINT FOR A LINEAR A/D OR D/A CONVERTER REFERENCED TO MU–LAW COMPANDING

Mu–Law companding, as specified by AT&T and CCITT, requires 8159 quantization levels to implement both A/D and D/A conversion schemes. This is to be mirrored about signal ground for the negative part of the wave form.

To implement a 13–bit (± 12–bit) linear converter scheme requires 8192 quantization levels mirrored about signal ground. To specify this converter such that it can be used to interface with, or as an alternative to, telephony based Mu–Law applications, the following is an explanation of the gain translation.

A 13–bit linear converter scheme has 8192 quantization levels. The goal is to be able to convert between these two encoding schemes with minimal distortion. This dictates setting the LSBs to the same level. For this to be achieved requires the reference voltage of the linear converter to be

8192/8159 times the reference voltage of the Mu–Law converter. The peak amplitude of a Mu–Law converter is 3.17 dBm0. The peak level of the linear converter will be 8192/8159 times the peak level of the Mu–Law converter, which is 8192/8159 x 3.17 dBm0. However, you cannot multiply a gain factor by a dBm value without using common term units and math (i.e., we must convert this gain factor to a dB equivalent), which is:

$$20 \log_{10} (8192/8159) = 0.03 \text{ dB}$$

With the gain factor in dB, we can add it to the Mu–Law peak level:

$$3.17 \text{ dBm0} + 0.03 \text{ dB} = 3.20 \text{ dBm0}$$

Therefore, the linear converter peak level is 3.20 dBm0.

This is another way of saying the 0 dBm0 level for the linear converter is 3.20 dB below the maximum amplitude.

To determine the absolute 0 dBm0 level for the linear converter from the peak level, we calculate the peak level in dBm by:

$$10 \log_{10} \frac{3.27 \text{ VpK} / \sqrt{2}) / (600\ \Omega)}{1 \text{ mW}} = 9.50 \text{ dBm } (600\ \Omega)$$

and 3.20 dB below this level is the 0 dBm0 absolute amplitude, which is

$$9.50 \text{ dBm} - 3.20 \text{ dB} = 6.30 \text{ dBm } (600\ \Omega)$$

Therefore, the calibration level, or transmission level point (TLP), for this part is 6.30 dBm (600 Ω), which is 1.6 Vrms based on the reference voltage of 3.27 V.

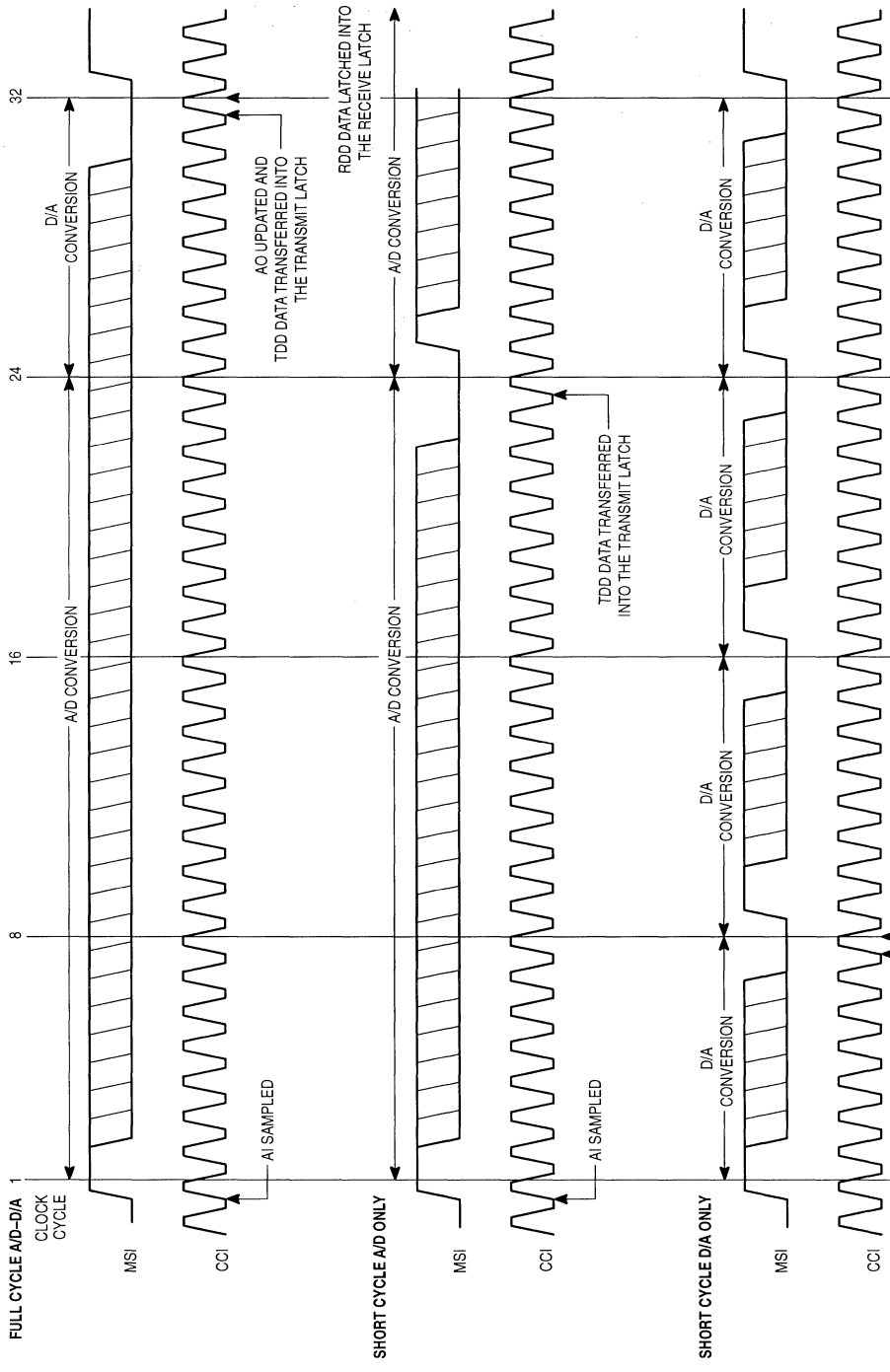


Figure 2. MC145402 Full and Short Cycle Timing

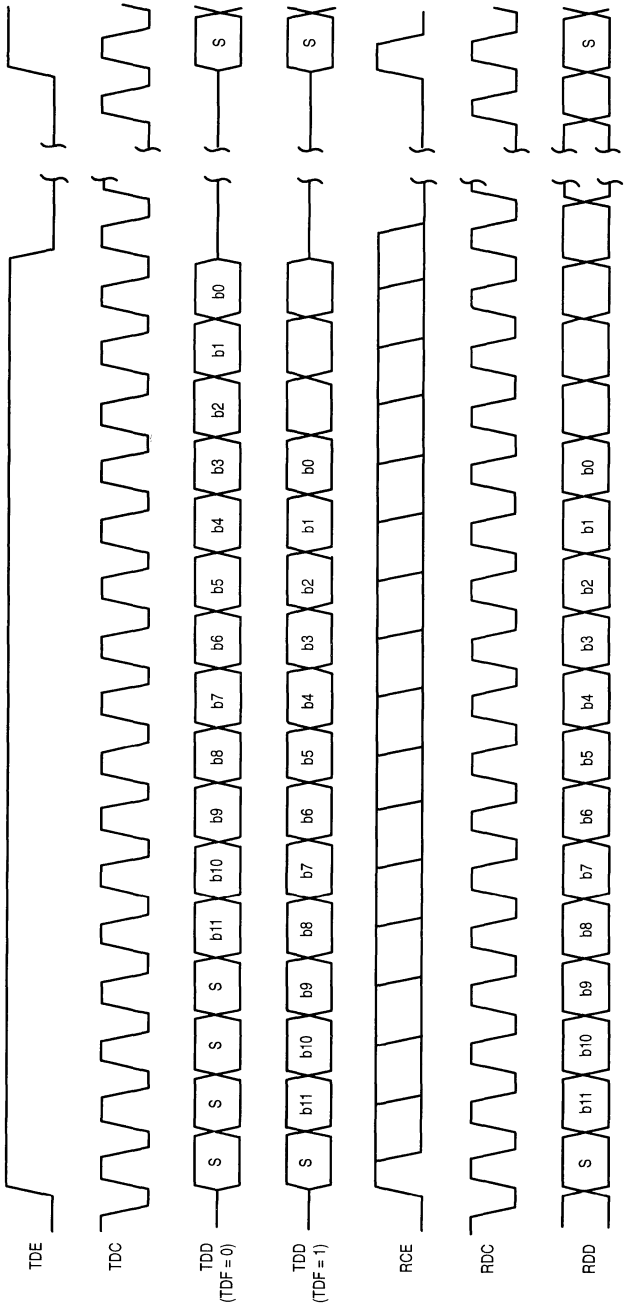


Figure 3. MC145402 Digital Data Timing

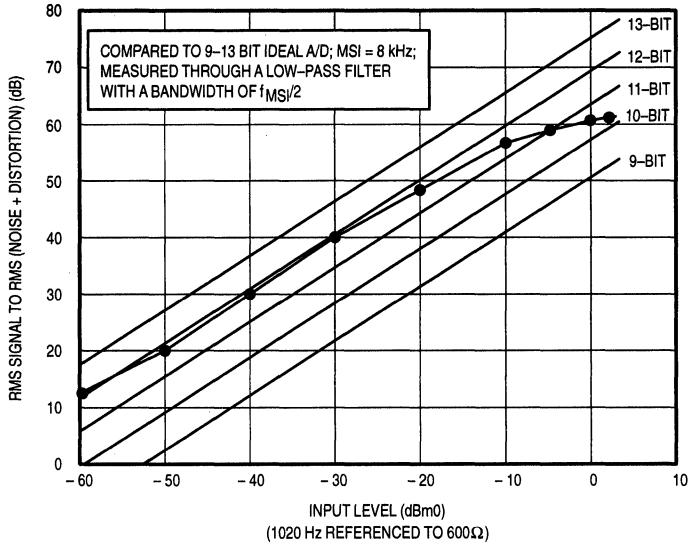


Figure 4. MC145402 Encoder (A/D) Signal to Noise Plus Distortion Ratio

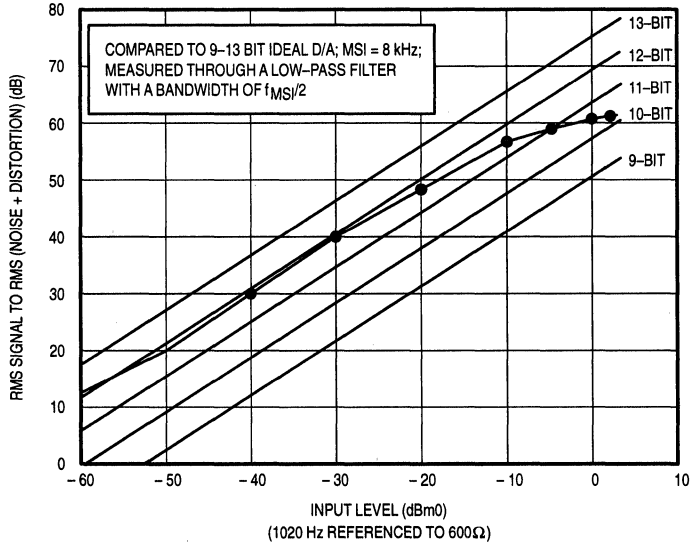


Figure 5. MC145402 Decoder (D/A) Signal to Noise Plus Distortion Ratio

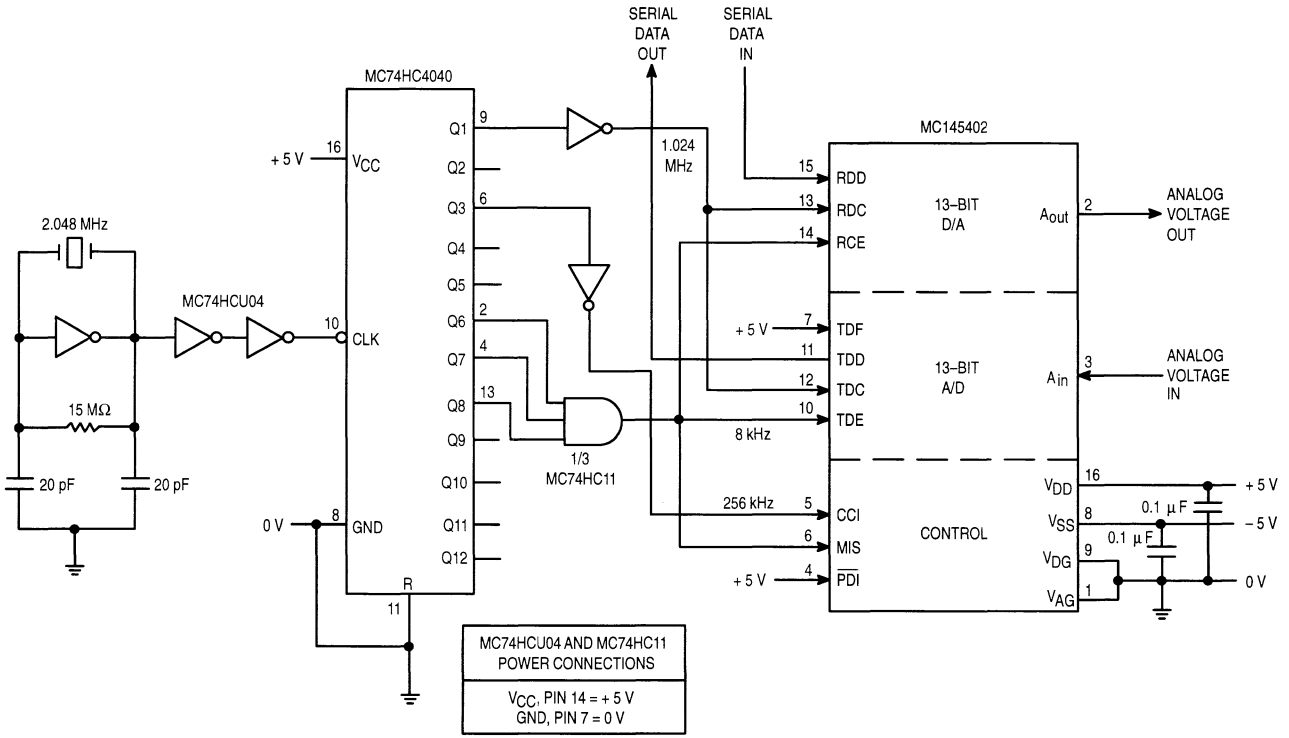


Figure 6. Typical MC145402 Configuration

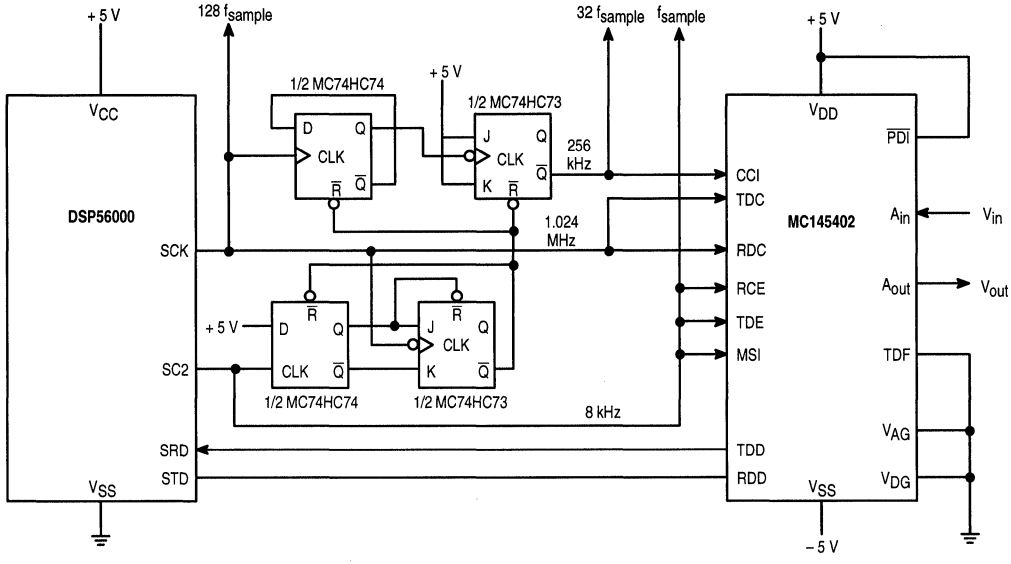


Figure 7. The MC145402, 13–Bit Linear Codec, Interfaced to a Motorola DSP56000, Digital Signal Processor, SSI Port

MC145403
MC145404
MC145405
MC145408

Drivers/Receivers
EIA–232–E and CCITT V.28

These devices are silicon gate CMOS ICs that combine both the transmitter and receiver to fulfill the electrical specifications of EIA Standard 232–E and CCITT V.28. The drivers feature true TTL input compatibility, slew rate limiting outputs, 300 Ω power–off source impedance, and output typically switching to within 25% of the supply rails. The receivers can handle up to ± 25 V while presenting 3 to 7 kΩ impedance. Hysteresis in the receivers aid in the reception of noisy signals. By combining both drivers and receivers in a single CMOS chip, these devices provide efficient, low–power solutions for both EIA–232–E and V.28 applications.

These devices offer the following performance features:

Drivers

- ± 5 to ± 12 V Supply Range
- 300 Ω Power–Off Source Impedance
- Output Current Limiting
- TTL and CMOS Compatible Inputs
- Driver Slew Rate Range Limited to 30 V/µs Maximum

Receivers

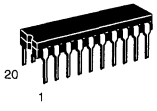
- ± 25 V Input Range
- 3 to 7 kΩ Input Impedance
- 0.8 V of Hysteresis for Enhanced Noise Immunity
- TTL and CMOS Compatible Outputs

Available Driver/Receiver Combinations

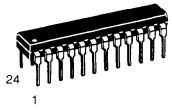
Device	Drivers	Receivers	Figure	No. of Pins
MC145403	3	5	1	20
MC145404	4	4	2	20
MC145405	5	3	3	20
MC145408	5	5	4	24

Alternative EIA–232 devices to consider are:

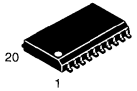
Three Supply	Single Supply
MC145406 (3 x 3)	MC145407 (3 x 3)
	MC145705 (2 x 3) with Power Down
	MC145706 (3 x 2) with Power Down
	MC145707 (3 x 3) with Power Down



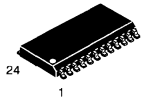
P SUFFIX
PLASTIC DIP
CASE 738



P SUFFIX
PLASTIC DIP
CASE 724



DW SUFFIX
SOG PACKAGE
CASE 751D



DW SUFFIX
SOG PACKAGE
CASE 751E

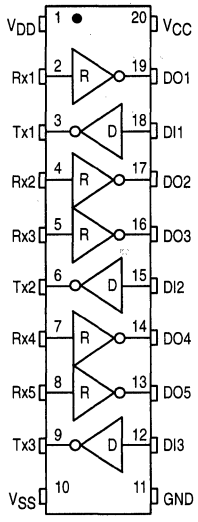
ORDERING INFORMATION

MC145403P	Plastic DIP
MC145404P	Plastic DIP
MC145405P	Plastic DIP
MC145408P	Plastic DIP
MC145403DW	SOG Package
MC145404DW	SOG Package
MC145405DW	SOG Package
MC145408DW	SOG Package

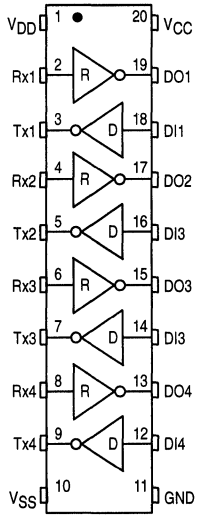
REV 1
10/95

PIN ASSIGNMENTS
(DIP AND SOG)

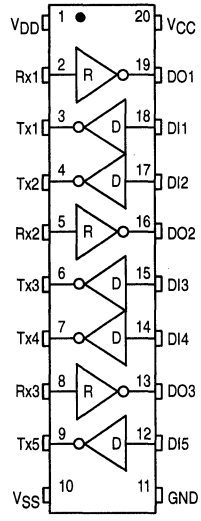
MC145403
3 DRIVERS/5 RECEIVERS



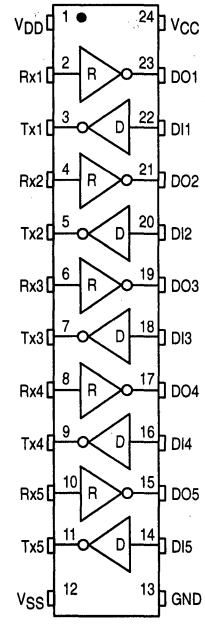
MC145404
4 DRIVERS/4 RECEIVERS



MC145405
5 DRIVERS/3 RECEIVERS

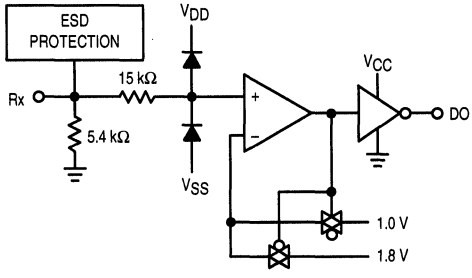


MC145408
5 DRIVERS/5 RECEIVERS

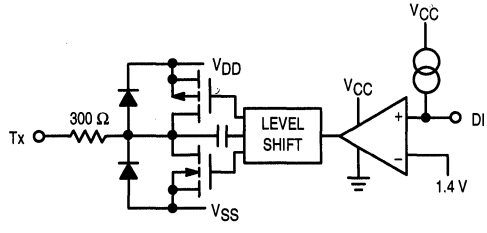


FUNCTIONAL DIAGRAM

RECEIVER



DRIVER



ABSOLUTE MAXIMUM RATINGS

(Voltages referenced to GND, except where noted)

Rating	Symbol	Value	Unit
DC Supply Voltage ($V_{DD} \geq V_{CC}$)	V_{DD} V_{SS} V_{CC}	− 0.5 to + 13.5 + 0.5 to − 13.5 − 0.5 to + 6.0	V
Input Voltage Range Rx1 − Rx*n* DI1 − DI*n*	V_{IR}	 V_{SS} − 15 to V_{DD} + 15 0.5 to V_{CC} + 15	V
DC Current Drain per Pin	I	± 00	mA
Power Dissipation	P_D	1	W
Operating Temperature Range	T_A	− 40 to + 85	°C
Storage Temperature Range	T_{stg}	− 85 to + 150	°C

This device contains circuitry to protect the inputs and outputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high impedance circuit.

For proper operation it is recommended that V_{out} and V_{in} be constrained to the ranges described as follows:

Digital I/O: Driver Inputs (DI):
($GND \leq V_{DI} \leq V_{CC}$).
Receiver Outputs (DO):
($GND \leq V_{DO} \leq V_{CC}$).
EIA–232 I/O: Driver Outputs (Tx):
($V_{SS} \leq V_{Tx1 - Txn} \leq V_{DD}$).
Receiver Inputs (Rx):
V_{SS} − 15 V ≤ $V_{Rx1 - Rxn} \leq V_{DD}$ + 15 V).

Reliability of operation is enhanced if unused outputs are tied off to an appropriate logic voltage level (e.g., either GND or V_{CC} for DI, and GND for Rx).

DC ELECTRICAL CHARACTERISTICS (All polarities referenced to GND = 0 V, T_A = − 40 to + 85°C)

Parameter		Symbol	Min	Typ	Max	Unit
DC Supply Voltage		V_{DD} V_{SS} V_{CC}	4.5 − 4.5 4.5	5 to 12 − 5 to − 12 5	13.2 − 13.2 5.5	V
Quiescent Supply Current (Outputs Unloaded, Inputs Low)	V_{DD} = + 12 V V_{SS} = − 12 V V_{CC} = + 5 V	I_{DD} I_{SS} I_{CC}	— — —	425 − 400 110	635 − 600 200	µA

RECEIVER ELECTRICAL SPECIFICATIONS

(Voltage polarities referenced to GND = 0 V, V_{DD} = + 12 V, V_{SS} = − 12 V, T_A = − 40 to + 85°C, V_{CC} = + 5 V, ± 10%)

Characteristic		Symbol	Min	Typ	Max	Unit
Input Turn–On Threshold $V_{DO} = V_{OL}$	Rx1 − Rx*n*	V_{on}	1.35	1.8	2.35	V
Input Turn–Off Threshold $V_{DO} = V_{OH}$	Rx1 − Rx*n*	V_{off}	0.75	1	1.25	V
Input Threshold Hysteresis $\Delta = V_{on} - V_{off}$		V_{hys}	0.6	0.8	—	V
Input Resistance (V_{SS} − 15 V) ≤ V Rx1 − Rx*n* ≤ (V_{DD} + 15 V)		R_{in}	3	5.4	7	kΩ
High Level Output Voltage V_{Rx} = − 3 to − 25 V* (DO1 − DO*n*)	I_{out} = − 20 µA I_{out} = − 1.0 mA	V_{OH}	4.9 3.8	4.9 4.3	— —	V
Low Level Output Voltage V_{Rx} = + 3 to + 25 V* (DO1 − DO*n*)	I_{out} = + 2 mA I_{out} = + 4 mA	V_{OL}	— —	0.02 0.5	0.5 0.7	V

* This is the range of input voltages as specified by EIA–232–E to cause a receiver to be in the high or low.

DRIVER ELECTRICAL SPECIFICATIONS

(Voltage Polarities Referenced to GND = 0 V, V_{DD} = + 12 V, V_{SS} = – 12 V, T_A = – 40 to + 85°C, V_{CC} = + 5 V, ± 10%)

Characteristic		Symbol	Min	Typ	Max	Unit
Digital Input Voltage	DI1 – DI*n*					V
Logic 0		V_{IL}	—	—	0.8	
Logic 1		V_{IH}	2	—	—	
Input Current	DI1 – DI*n*					μA
V_{DI} = GND		I_{IL}	—	7	—	
V_{DI} = V_{CC}		I_{IH}	—	—	± 1.0	
Output High Voltage	Tx1 – Tx*n*	V_{OH}				V
V_{DI} = Logic 0, R_L = 3 kΩ						
V_{DD} = + 5.0 V, V_{SS} = – 5.0 V			3.5	3.9	—	
V_{DD} = + 6.0 V, V_{SS} = – 6.0 V			4.3	4.7	—	
V_{DD} = + 12.0 V, V_{SS} = – 12.0 V			9.2	9.5	—	
Output Low Voltage*	Tx1 – Tx*n*	V_{OL}				V
V_{DI} = Logic 1, R_L = 3 kΩ						
V_{DD} = + 5.0 V, V_{SS} = – 5.0 V			– 4	– 4.3	—	
V_{DD} = + 6.0 V, V_{SS} = – 6.0 V			– 4.5	– 5.2	—	
V_{DD} = + 12.0 V, V_{SS} = – 12.0 V			– 10	– 10.3	—	
Input Current (Figure 5)	Tx1 – Tx*n*	Z_{off}	300	—	—	Ω
Output Short Circuit Current	Tx1 – Tx*n*	I_{SC}				mA
V_{DD} = + 12 V, V_{SS} = – 12 V						
Tx Shorted to GND**			—	± 22	± 60	
Tx Shorted to ± 15 V***			—	± 60	± 100	

* Voltage specifications are in terms of absolute values.

** Specification is for one Tx output pin to be shorted at a time. Should all three driver outputs be shorted simultaneously, device power dissipation limits will be exceeded.

*** This condition could exceed package limitations.

SWITCHING CHARACTERISTICS (V_{CC} = + 5 V, ± 10%, V_{DD} = + 12 V, V_{SS} = – 12 V, T_A = – 40 to + 85°C; See Figures 2 and 3)

Characteristic	Symbol	Min	Typ	Max	Unit
Drivers					
Propagation Delay Time Tx	t_{PLH}				ns
Low–to–High					
R_L = 3 kΩ, C_L = 50 pF		—	500	1000	
High–to–Low	t_{PHL}				
R_L = 3 kΩ, C_L = 50 pF		—	700	1000	
Output Slew Rate	SR				V/μs
Minimum Load					
R_L = 7 kΩ, C_L = 0 pF (V_{DD} = 6 to 12 V, V_{SS} = – 6 to – 12 V)		—	± 6	± 30	
Maximum Load					
R_L = 3 kΩ, C_L = 2500 pF (V_{DD} = 12 V, V_{SS} = – 12 V, V_{CC} = 5 V)		4	—	—	
Receivers (C_L = 50 pF)					
Propagation Delay Time	t_{PLH}				ns
Low–to–High		—	360	610	
High–to–Low	t_{PHL}	—	130	610	
Output Rise Time	t_r	—	250	400	ns
Output Fall Time	t_f	—	40	100	ns

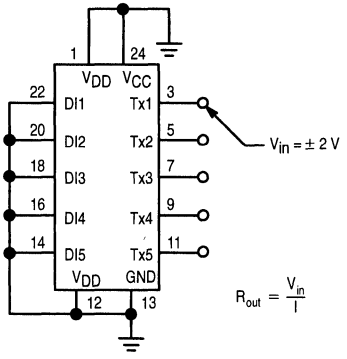


Figure 1. Power–Off Source Resistance Illustrated for MC145408

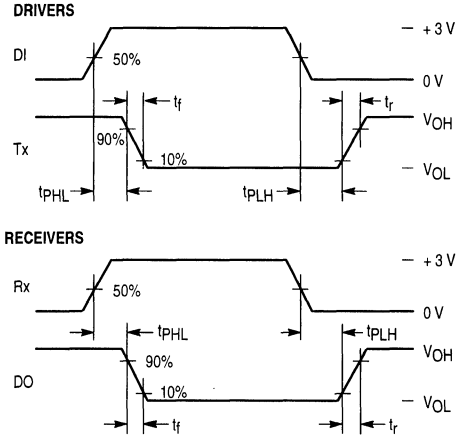


Figure 2. Switching Characteristics

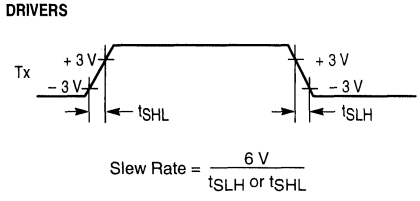


Figure 3. Slew Rate Characteristics

PIN DESCRIPTIONS

V_{CC}
Digital Power Supply

The digital supply pin, which is connected to the logic power supply (+ 5.5 V maximum).

GND
Ground

Ground return pin is typically connected to the signal ground pin of the EIA–232–E connector (Pin 7) as well as to the logic power supply ground.

V_{DD}
Most Positive Device Pin

The most positive power supply pin, which is typically + 5 to + 12 V.

V_{SS}
Most Negative Device Pin

The most negative power supply pin, which is typically – 5 to – 12 V.

Rx1 – Rx*n*
Receive Data Input Pins

These are the EIA–232–E receive signal inputs. A voltage between + 3 and + 25 V is decoded as a space, and causes the corresponding DO pin to swing to ground (0 V). A voltage between – 3 and – 25 V is decoded as a mark, and causes the corresponding DO pin to swing to V_{CC}.

DO1 – DO*n*
Data Output Pins

These are the receiver digital output pins which swing from V_{CC} to GND. Each output pin is capable of driving one LSTTL input load.

DI1 – DI*n*
Data Input Pins

These are the high impedance digital input pins to the drivers. Input voltage levels on these pins are LSTTL compatible and must be between V_{CC} and GND. A weak pull–up on each input sets all unused DI pins to V_{CC}, causing the corresponding unused driver outputs to be at V_{SS}.

Tx1 – TX*n*
Transmit Data Output Pins

These are the EIA–232–E transmit signal output pins, which swing from V_{DD} to V_{SS}. A logic 1 at the DI input causes the corresponding Tx output to swing to V_{SS}. A logic 0 at the DI input causes the corresponding Tx out to swing to V_{DD}. The actual levels and slew rate achieved will depend on the output loading ($R_L \parallel C_L$).

APPLICATION INFORMATION

POWER SUPPLY CONSIDERATIONS

Figure 4 shows a technique to guard against excessive device current.

The diode D1 prevents excessive current from flowing through an internal diode from the V_{CC} pin to the V_{DD} pin when $V_{DD} < V_{CC}$ by approximately 0.6 V or greater. This high current condition can exist for a short period of time during power up/down. Additionally, if the + 12 V supply is switched off while the + 5 V is on and the off supply is a low impedance to ground, the diode D1 will prevent current flow through the internal diode.

The diode D2 is used as a voltage clamp, to prevent V_{SS} from drifting positive to V_{CC}, in the event that power is removed from V_{SS} (Pin 12). If V_{SS} power is removed, and the impedance from the V_{SS} pin to ground is greater than approximately 3 kΩ, this pin will be pulled to V_{CC} by internal circuitry causing excessive current in the V_{CC} pin.

If by design, neither of the above conditions are allowed to exist, then the diodes D1 and D2 are not required.

ESD PROTECTION

ESD protection on IC devices that have their pins accessible to the outside world is essential. High static voltages applied to the pins when someone touches them either directly or indirectly can cause damage to gate oxides and transistor junctions by coupling a portion of the energy from the I/O pin to the power supply buses of the IC. This coupling will usually occur through the internal ESD protection diodes. The key to protecting the IC is to shunt as much of the energy to ground as possible before it enters the IC. Figure 4 shows a technique which will clamp the ESD voltage at approximately ± 15 V using the MMBZ15VDLT1. Any residual voltage which appears on the supply pins is shunted to ground through the capacitors C1 – C3. This scheme has provided protection to the interface part up to ± 10 kV, using the human body model test.

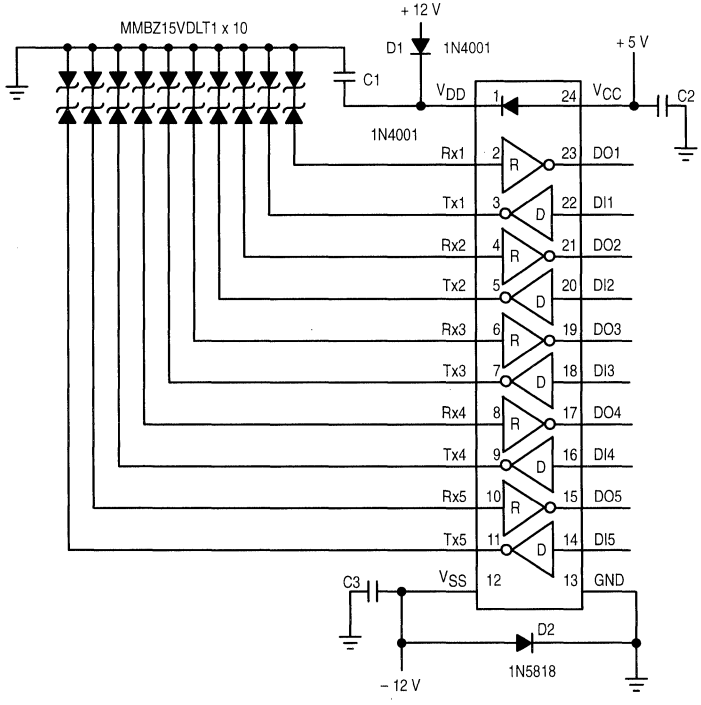


Figure 4.

MC145406

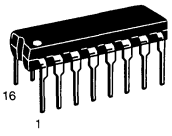
Driver/Receiver

EIA–232–E and CCITT V.28 (Formerly RS–232–D)

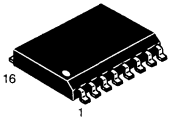
The MC145406 is a silicon–gate CMOS IC that combines three drivers and three receivers to fulfill the electrical specifications of standards EIA–232–E and CCITT V.28. The drivers feature true TTL input compatibility, slew–rate–limited output, 300–Ω power–off source impedance, and output typically switching to within 25% of the supply rails. The receivers can handle up to ±25 V while presenting 3 to 7 kΩ impedance. Hysteresis in the receivers aids reception of noisy signals. By combining both drivers and receivers in a single CMOS chip, the MC145406 provides efficient, low–power solutions for EIA–232–E and V.28 applications.

Drivers
- ± 5 V to ±12 V Supply Range
- 300–Ω Power–Off Source Impedance
- Output Current Limiting
- TTL Compatible
- Maximum Slew Rate = 30 V/μs

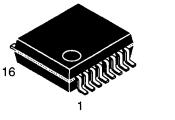
Receivers
- ± 25 V Input Voltage Range When V_{DD} = 12 V, V_{SS} = – 12 V
- 3 to 7 kΩ Input Impedance
- Hysteresis on Input Switchpoint



P SUFFIX
PLASTIC DIP
CASE 648

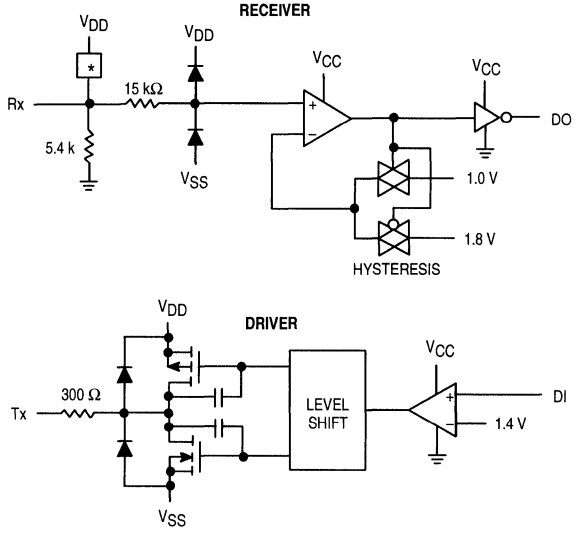


DW SUFFIX
SOG PACKAGE
CASE 751G



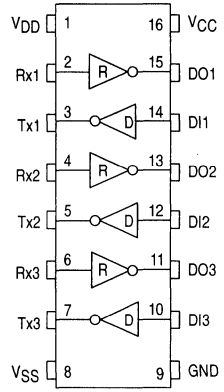
SD SUFFIX
SSOP
CASE 940B

BLOCK DIAGRAM



*Protection circuit

PIN ASSIGNMENT



D = DRIVER
R = RECEIVER

MAXIMUM RATINGS (Voltage polarities referenced to GND)

Rating	Symbol	Value	Unit
DC Supply Voltages ($V_{DD} \geq V_{CC}$)	V_{DD} V_{SS} V_{CC}	− 0.5 to + 13.5 + 0.5 to − 13.5 − 0.5 to + 6.0	V
Input Voltage Range Rx1–3 Inputs DI1–3 Inputs	V_{IR}	 (V_{SS} − 15) to (V_{DD} + 15) − 0.5 to (V_{CC} + 0.5)	V
DC Current Per Pin		± 100	mA
Power Dissipation	P_D	1.0	W
Operating Temperature Range	T_A	− 40 to + 85	°C
Storage Temperature Rate	T_{stg}	− 85 to + 150	°C

This device contains protection circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation, it is recommended that the voltages at the DI and DO pins be constrained to the range $GND \leq V_{DI} \leq V_{CC}$ and $GND \leq V_{DO} \leq V_{CC}$. Also, the voltage at the Rx pin should be constrained to (V_{SS} − 15 V) ≤ V_{Rx1-3} ≤ (V_{DD} + 15 V), and Tx should be constrained to $V_{SS} \leq V_{Tx1-3} \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., GND or V_{CC} for DI and Ground for Rx.)

DC ELECTRICAL CHARACTERISTICS (All polarities referenced to GND = 0 V, T_A = − 40 to +85°C)

Parameter	Symbol	Min	Typ	Max	Unit
DC Supply Voltage					V
V_{DD}	V_{DD}	4.5	5 to 12	13.2	
V_{SS}	V_{SS}	−4.5	−5 to − 12	−13.2	
V_{CC} ($V_{DD} \geq V_{CC}$)	V_{CC}	4.5	5.0	5.5	
Quiescent Supply Current (Outputs unloaded, inputs low)					µA
V_{DD} = + 12 V	I_{DD}	—	140	400	
V_{SS} = − 12 V	I_{SS}	—	340	600	
V_{CC} = + 5 V	I_{CC}	—	300	450	

RECEIVER ELECTRICAL SPECIFICATIONS

(Voltage polarities referenced to GND = 0 V, V_{DD} = + 5 to + 12 V, V_{SS} = − 5 to − 12 V, $V_{DD} \geq V_{CC}$, T_A = − 40 to + 85°C)

Characteristic		Symbol	Min	Typ	Max	Unit
Input Turn–on Threshold $V_{DO1-DO3} = V_{OL}$, V_{CC} = 5.0 V ± 5%	Rx1–Rx3	V_{on}	1.35	1.80	2.35	V
Input Turn–off Threshold $V_{DO1-DO3} = V_{OH}$, V_{CC} = 5.0 V ± 5%	Rx1–Rx3	V_{off}	0.75	1.00	1.25	V
Input Threshold Hysteresis V_{CC} = 5.0 V ± 5%	Rx1–Rx3	V_{on}–V_{off}	0.6	0.8	—	V
Input Resistance (V_{SS} − 15 V) ≤ $V_{Rx1-Rx3}$ ≤ (V_{DD} + 15 V)	Rx1–Rx3	R_{in}	3.0	5.4	7.0	kΩ
High–Level Output Voltage ($V_{Rx1-Rx3}$ = − 3 V to (V_{SS} − 15 V))*	DO1–DO3	V_{OH}				V
I_{OH} = − 20 µA, V_{CC} = + 5.0 V			4.9	4.9	—	
I_{OH} = −1 mA, V_{CC} = + 5.0 V			3.8	4.3	—	
Low–Level Output Voltage ($V_{Rx1-Rx3}$ = + 3 V to (V_{DD} + 15 V))*	DO1–DO3	V_{OL}				V
I_{OL} = + 20 µA, V_{CC} = + 5.0 V			—	0.01	0.1	
I_{OL} = + 2 mA, V_{CC} = + 5.0 V			—	0.02	0.5	
I_{OL} = + 4 mA, V_{CC} = + 5.0 V			—	0.5	0.7	

* This is the range of input voltages as specified by EIA–232–E to cause a receiver to be in the high or low logic state.

ELECTRICAL SPECIFICATIONS (Voltage polarities referenced to GND = 0 V, V_{CC} = + 5 V ± 5%, T_A = – 40 to + 85°C)

Characteristic	Symbol	Min	Typ	Max	Unit
Digital Input Voltage DI1–DI3					V
Logic 0	V_{IL}	—	—	0.8	
Logic 1	V_{IH}	2.0	—	—	
Input Current DI1–DI3	I_{in}	—	—	± 1.0	μA
$V_{DI1–DI3} = V_{CC}$					
Output High Voltage ($V_{DI1–3}$ = Logic 0, R_L = 3.0 kΩ) Tx1–Tx3	V_{OH}				V
V_{DD} = + 5.0 V, V_{SS} = – 5.0 V		3.5	3.9	—	
V_{DD} = + 6.0 V, V_{SS} = – 6.0		4.3	4.7	—	
V_{DD} = + 12.0 V, V_{SS} = – 12.0 V		9.2	9.5	—	
Output Low Voltage* ($V_{DI1–3}$ = Logic 1, R_L = 3.0 kΩ) Tx1–Tx3	V_{OL}				V
V_{DD} = + 5.0 V, V_{SS} = – 5.0 V		– 4.0	– 4.3	—	
V_{DD} = + 6.0 V, V_{SS} = – 6.0 V		– 4.5	– 5.2	—	
V_{DD} = + 12.0 V, V_{SS} = – 12.0 V		– 10.0	– 10.3	—	
Off Source Resistance (Figure 1) Tx1–Tx3		300	—	—	Ω
$V_{DD} = V_{SS} = GND = 0$ V, $V_{Tx1–Tx3}$ = ± 2.0 V					
Output Short–Circuit Current (V_{DD} = + 12.0 V, V_{SS} = – 12.0 V) Tx1–Tx3	I_{SC}				mA
Tx1–Tx3 shorted to GND**		—	± 22	± 60	
Tx1–Tx3 shorted to ± 15.0 V***		—	± 60	± 100	

* The voltage specifications are in terms of absolute values.

** Specification is for one Tx output pin to be shorted at a time. Should all three driver outputs be shorted simultaneously, device power dissipation limits will be exceeded.

*** This condition could exceed package limitations.

SWITCHING CHARACTERISTICS (V_{CC} = + 5 V ± 5%, T_A = – 40 to + 85°C; See Figures 2 and 3)

Drivers

Characteristic	Symbol	Min	Typ	Max	Unit
Propagation Delay Time Tx1–Tx3					ns
Low–to–High					
R_L = 3 kΩ, C_L = 50 pF	t_{PLH}	—	300	500	
High–to–Low	t_{PHL}				
R_L = 3 kΩ C_L = 50 pF		—	300	500	
Output Slew Rate Tx1–Tx3	SR				V/μs
Minimum Load					
R_L = 7 kΩ, C_L = 0 pF, V_{DD} = + 6 to + 12 V, V_{SS} = – 6 to – 12 V		—	± 9	± 30	
Maximum Load					
R_L = 3 kΩ, C_L = 2500 pF					
V_{DD} = + 12 V, V_{SS} = – 12 V		4	—	—	
V_{DD} = + 5 V, V_{SS} = – 5 V		—	—	—	

Receivers (C_L = 50 pF)

Characteristic	Symbol	Min	Typ	Max	Unit
Propagation Delay Time DO1–DO3					ns
Low–to–High	t_{PLH}	—	150	425	
High–to–Low	t_{PHL}	—	150	425	
Output Rise Time DO1–DO3	t_r	—	250	400	ns
Output Fall Time DO1–DO3	t_f	—	40	100	ns

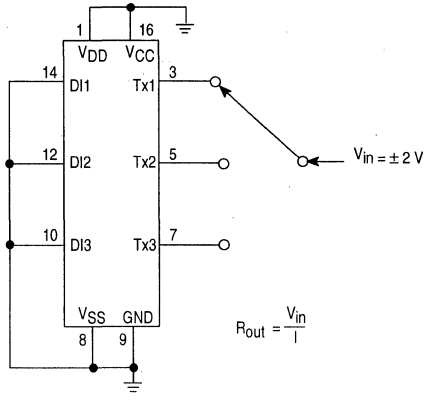
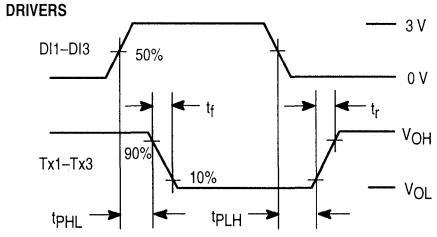


Figure 1. Power–Off Source Resistance (Drivers)



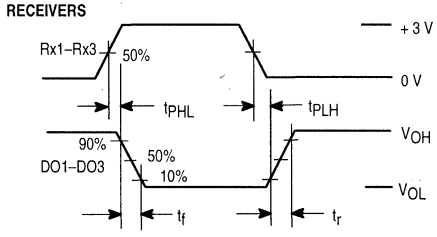


Figure 2. Switching Characteristics

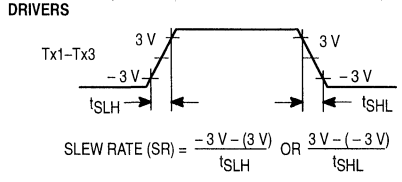


Figure 3. Slew–Rate Characterization

PIN DESCRIPTIONS

V_{DD}
Positive Power Supply (Pin 1)

The most positive power supply pin, which is typically + 5 to + 12 V.

V_{SS}
Negative Power Supply (Pin 8)

The most negative power supply pin, which is typically – 5 to – 12 V.

V_{CC}
Digital Power Supply (Pin 16)

The digital supply pin, which is connected to the logic power supply (maximum + 5.5 V). V_{CC} ***must*** be less than or equal to V_{DD}.

GND
Ground (Pin 9)

Ground return pin is typically connected to the signal ground pin of the EIA–232–E connector (Pin 7) as well as to the logic power supply ground.

Rx1, Rx2, Rx3
Receive Data Input (Pins 2, 4, 6)

These are the EIA–232–E receive signal inputs whose voltages can range from (V_{DD} + 15 V) to (V_{SS} – 15 V). A voltage between + 3 and (V_{DD} + 15 V) is decoded as a space and causes the corresponding DO pin to swing to ground (0 V); a voltage between – 3 and (V_{DD} – 15 V) is decoded as a mark and causes the DO pin to swing up to V_{CC}. The actual turn–on input switchpoint is typically biased at 1.8 V above ground, and includes 800 mV of hysteresis for noise rejection. The nominal input impedance is 5 kΩ. An open or grounded input pin is interpreted as a mark, forcing the DO pin to V_{CC}.

DO1, DO2, DO3
Data Output (Pins 11, 13, 15)

These are the receiver digital output pins, which swing from V_{CC} to GND. A space on the Rx pin causes DO to produce a logic 0; a mark produces a logic 1. Each output pin is capable of driving one LSTTL input load.

DI1, DI2, DI3
Data Input (Pins 10, 12,14)

These are the high–impedance digital input pins to the drivers. TTL compatibility is accomplished by biasing the input switchpoint at 1.4 V above GND. However, 5–V CMOS compatibility is maintained as well. Input voltage levels on these pins must be between V_{CC} and GND.

Tx1, Tx2, Tx3
Transmit Data Output (Pins 3, 5, 7)

These are the EIA–232–E transmit signal output pins, which swing toward V_{DD} and V_{SS}. A logic 1 at a DI input causes the corresponding Tx output to swing toward V_{SS}. A logic 0 causes the output to swing toward V_{DD} (the output voltages will be slightly less than V_{DD} or V_{SS} depending upon the output load). Output slew rates are limited to a maximum of 30 V per μs. When the MC145406 is off (V_{DD} = V_{SS} = V_{CC} = GND), the minimum output impedance is 300 Ω.

APPLICATIONS INFORMATION

The MC145406 has been designed to meet the electrical specifications of standards EIA–232–E and CCITT V.28. EIA–232–E defines the electrical and physical interface between Data Communication Equipment (DCE) and Data Terminal Equipment (DTE). A DCE is connected to a DTE using a cable that typically carries up to 25 leads. These leads, referred to as interchange circuits, allow the transfer of timing, data, control, and test signals. Electrically this transfer requires level shifting between the TTL/CMOS logic levels of the computer or modem and the high voltage levels of EIA–232–E, which can range from ±3 to ± 25 V. The MC145406 provides the necessary level shifting as well as meeting other aspects of the EIA–232–E specification.

DRIVERS

As defined by the specification, an EIA–232–E driver presents a voltage of between ± 5 to ± 15 V into a load of between 3 to 7 kΩ. A logic 1 at the driver input results in a voltage of between – 5 to – 15 V. A logic 0 results in a voltage between + 5 to + 15 V. When operating V_{DD} and V_{SS} at ± 7 to ± 12 V, the MC145406 meets this requirement. When operating at ± 5 V, the MC145406 drivers produce less than ± 5 V at the output (when terminated), which does not meet EIA–232–E specification. However, the output voltages when using a ± 5 V power supply are high enough (around ± 4 V) to permit proper reception by an EIA–232–E receiver, and can be used in applications where strict compliance to EIA–232–E is not required.

Another requirement of the MC145406 drivers is that they withstand a short to another driver in the EIA–232–E cable. The worst–case condition that is permitted by EIA–232–E is a ± 15 V source that is current limited to 500 mA. The MC145406 drivers can withstand this condition momentarily. In most short circuit conditions the source driver will have a series 300 Ω output impedance needed to satisfy the EIA–232–E driver requirements. This will reduce the short circuit current to under 40 mA which is an acceptable level for the MC145406 to withstand.

Unlike some other drivers, the MC145406 drivers feature an internally–limited output slew–rate that does not exceed 30 V per μs.

RECEIVERS

The job of an EIA–232–E receiver is to level–shift voltages in the range of – 25 to + 25 V down to TTL/CMOS logic levels (0 to + 5 V). A voltage of between – 3 and – 25 V on Rx1 is defined as a mark and produces a logic 1 at DO1. A voltage between + 3 and + 25 V is a space and produces a logic zero. While receiving these signals, the Rx inputs must present a resistance between 3 and 7 kΩ. Nominally, the input resistance of the Rx1–Rx3 inputs is 5.4 kΩ.

The input threshold of the Rx1–Rx3 inputs is typically biased at 1.8 V above ground (GND) with typically 800 mV of hysteresis included to improve noise immunity. The 1.8 V bias forces the appropriate DO pin to a logic 1 when its Rx input is open or grounded as called for in the EIA–232–E specification. Notice that TTL logic levels can be applied to the Rx inputs in lieu of normal EIA–232–E signal levels. This might be helpful in situations where access to the modem or computer through the EIA–232–E connector is necessary with TTL devices. However, it is important not to connect the EIA–232–E outputs (Tx1–Tx3) to TTL inputs since TTL operates off + 5 V only, and may be damaged by the high output voltage of the MC145406.

The DO outputs are to be connected to a TTL or CMOS input (such as an input to a modem chip). These outputs will swing from V_{CC} to ground, allowing the designer to operate the DO and DI pins from digital power supply. The Tx and Rx sections are independently powered by V_{DD} and V_{SS} so that one may run logic at + 5 V and the EIA–232–E signals at ± 12 V.

POWER SUPPLY CONSIDERATIONS

Figure 4 shows a technique to guard against excessive device current.

The diode D1 prevents excessive current from flowing through an internal diode from the V_{CC} pin to the V_{DD} pin when $V_{DD} < V_{CC}$ by approximately 0.6 V. This high current condition can exist for a short period of time during power up/down. Additionally, if the + 12 V supply is switched off while the + 5 V is on and the off supply is a low impedance to ground, the diode D1 will prevent current flow through the internal diode.

The diode D2 is used as a voltage clamp, to prevent V_{SS} from drifting positive to V_{CC}, in the event that power is removed from V_{SS} (Pin 12). If V_{SS} power is removed, and the impedance from the V_{SS} pin to ground is greater than approximately 3 kΩ, this pin will be pulled to V_{CC} by internal circuitry causing excessive current in the V_{CC} pin.

If by design, neither of the above conditions are allowed to exist, then the diodes D1 and D2 are not required.

ESD PROTECTION

ESD protection on IC devices that have their pins accessible to the outside world is essential. High static voltages applied to the pins when someone touches them either directly or indirectly can cause damage to gate oxides and transistor junctions by coupling a portion of the energy from the I/O pin to the power supply buses of the IC. This coupling will usually occur through the internal ESD protection diodes. The key to protecting the IC is to shunt as much of the energy to ground as possible before it enters the IC. Figure 4 shows a technique which will clamp the ESD voltage at approximately ± 15 V using the MMBZ15VDLT1. Any residual voltage which appears on the supply pins is shunted to ground through the capacitors C1–C3. This scheme has provided protection to the interface part up to ± 10 kV, using the human body model test.

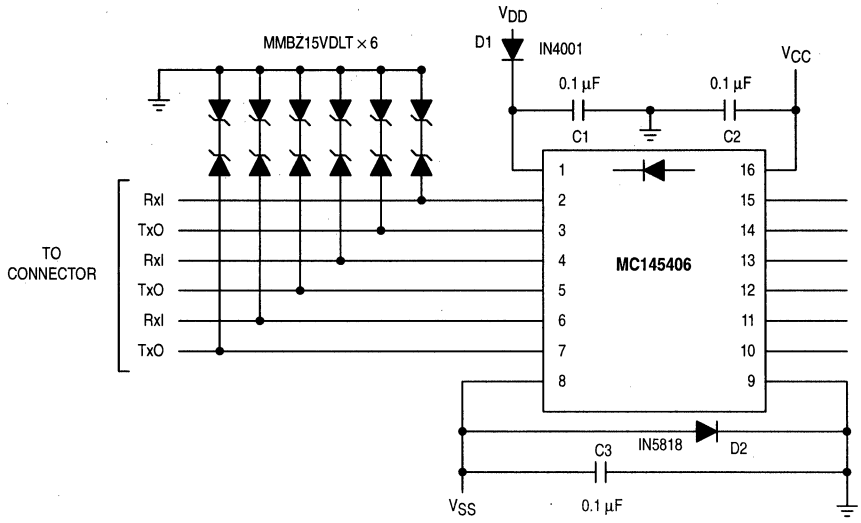
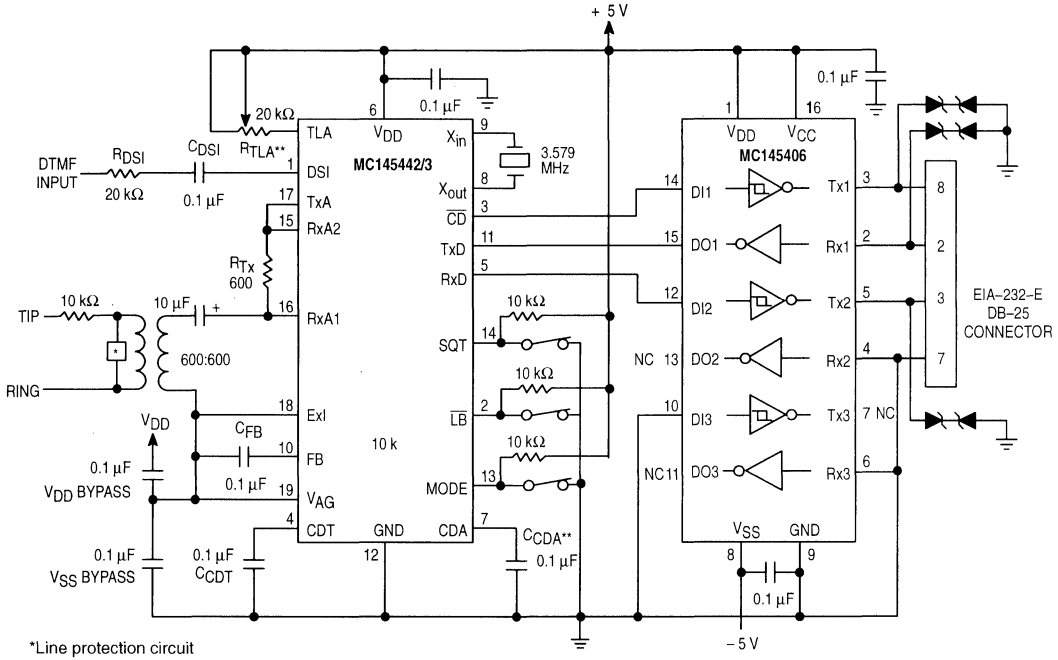


Figure 4. ESD and Power Supply Networks



*Line protection circuit

**Refer to the applications information for values of C_{CDA} and R_{TLA}

Figure 5. 5–V 300–Baud Modem with EIA–232–E Interface

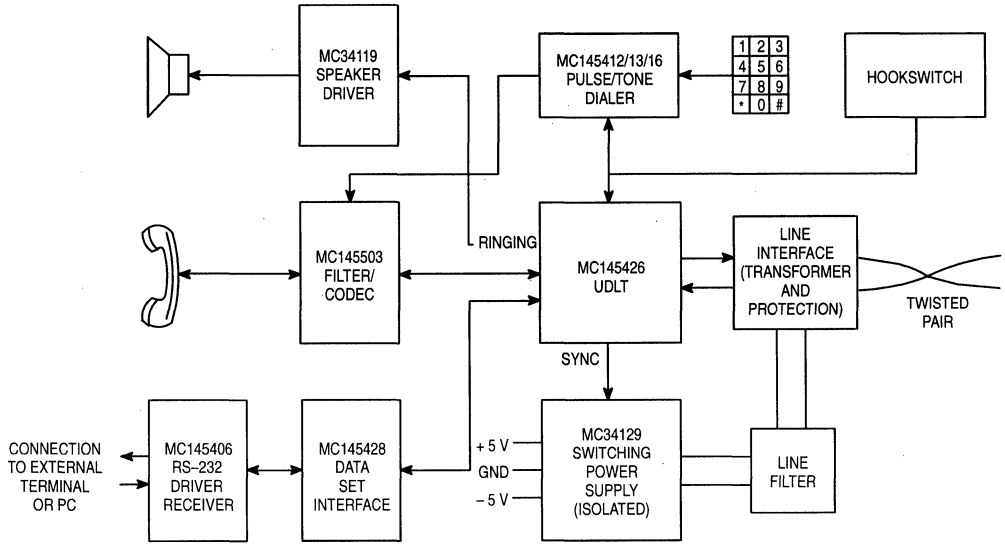


Figure 6. Line–Powered Voice/Data Telephone with Electrically Isolated EIA–232–E Interface

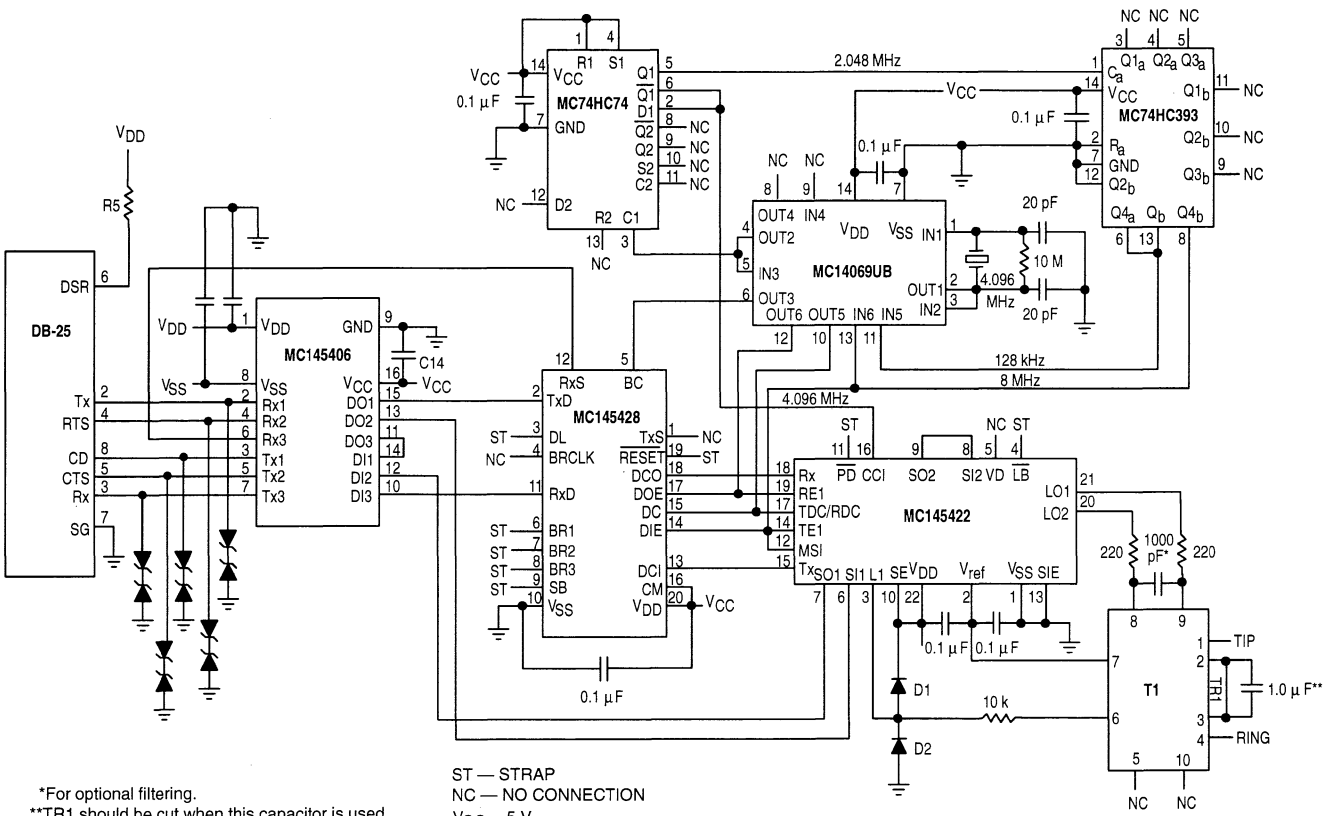


Figure 7. 80–kbps Limited Distance Modem with EIA–232–E Interface (Master)

MC145407

Advance Information

5 Volt Only Driver/Receiver

EIA–232–E and CCITT V.28

2

The MC145407 is a silicon–gate CMOS IC that combines three drivers and three receivers to fulfill the electrical specifications of EIA–232–E and CCITT V.28 while operating from a single + 5 V power supply. A voltage doubler and inverter convert the + 5 V to ± 10 V. This is accomplished through an on–board 20 kHz oscillator and four inexpensive external electrolytic capacitors. The three drivers and three receivers of the MC145407 are virtually identical to those of the MC145406. Therefore, for applications requiring more than three drivers and/or three receivers, an MC145406 can be powered from an MC145407, since the MC145407 charge pumps have been designed to guarantee ± 5 V at the output of up to six drivers. Thus, the MC145407 provides a high–performance, low–power, stand–alone solution or, with the MC145406, a + 5 V only, high–performance two–chip solution.

Drivers

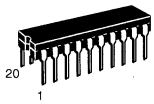
- ± 7.5 V Output Swing
- 300 Ω Power–Off Impedance
- Output Current Limiting
- TTL and CMOS Compatible Inputs
- Slew Rate Range Limited from 4 V/μs to 30 V/μs

Receivers

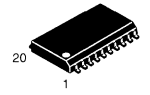
- + 25 V Input Range
- 3 to 7 kΩ Input Impedance
- 0.8 V Hysteresis for Enhanced Noise Immunity

Charge Pumps

- + 5 V to ± 10 V Dual Charge Pump Architecture
- Supply Outputs Capable of Driving Three On–Chip Drivers and Three Drivers on the MC145406 Simultaneously
- Requires Four Inexpensive Electrolytic Capacitors
- On–Chip 20 kHz Oscillator



P SUFFIX
PLASTIC DIP
CASE 738

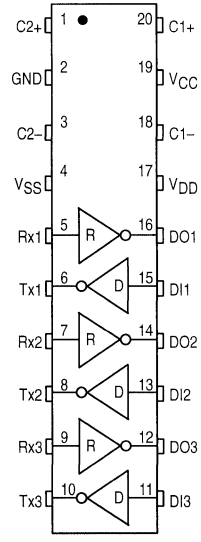


DW SUFFIX
SOG PACKAGE
CASE 751D

ORDERING INFORMATION

MC145407P	Plastic DIP
MC145407DW	SOG Package

PIN ASSIGNMENT

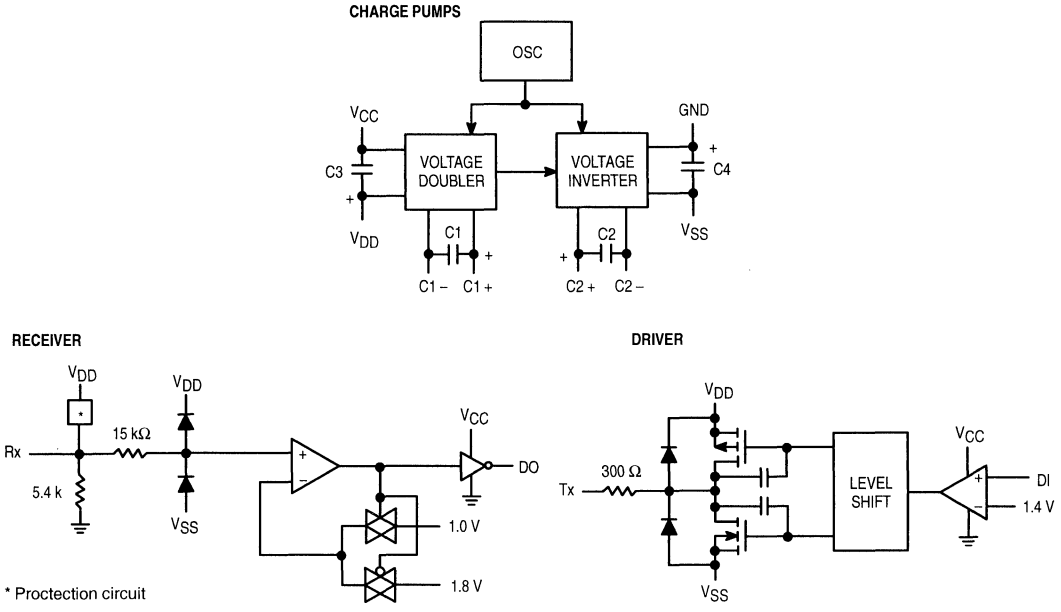


D = DRIVER
R = RECEIVER

This document contains information on a new product. Specifications and information herein are subject to change without notice.

REV 1
10/95

FUNCTION DIAGRAM



MAXIMUM RATINGS (Voltage polarities referenced to GND)

Rating	Symbol	Value	Unit
DC Supply Voltages	V_{CC}	– 0.5 to + 6.0	V
Input Voltage Range Rx1 – Rx3 Inputs DI1 – DI3 Inputs	V_{IR}	 V_{SS} – 15 to V_{DD} + 15 – 0.5 to (V_{CC} + 0.5)	V
DC Current per Pin	I	± 100	mA
Power Dissipation	P_D	1	W
Operating Temperature Range	T_A	– 40 to + 85	°C
Storage Temperature Range	T_{stg}	– 85 to + 150	°C

This device contains protection circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation, it is recommended that the voltages at the DI and DO pins be constrained to the range GND ≤ V_{DI} ≤ V_{CC} and GND ≤ V_{DO} ≤ V_{CC}. Also, the voltage at the Rx pin should be constrained to (V_{SS} – 15 V) ≤ $V_{Rx1 - Rx3}$ ≤ (V_{DD} + 15 V), and Tx should be constrained to V_{SS} ≤ $V_{Tx1 - Tx3}$ ≤ V_{DD}.

Unused inputs must always be tied to appropriate logic voltage level (e.g., GND or V_{CC} for DI, and GND for Rx).

DC ELECTRICAL CHARACTERISTICS (All polarities referenced to GND = 0 V; C1, C2, C3, C4 = 10 µF; T_A = – 40 to + 85°C)

Parameter		Symbol	Min	Typ	Max	Unit
DC Supply Voltage		V_{CC}	4.5	5	5.5	V
Quiescent Supply Current (Outputs unloaded, inputs low)		I_{CC}	—	1.2	3.0	mA
Output Voltage	I_{load} = 0 mA	V_{DD}	8.5	10	11	V
	I_{load} = 5 mA		7.5	9.5	—	
	I_{load} = 10 mA		6	9	—	
	I_{load} = 0 mA	V_{SS}	– 8.5	– 10	–11	
	I_{load} = 5 mA		– 7.5	– 9.2	—	
	I_{load} = 10 mA		– 6	– 8.6	—	

RECEIVER ELECTRICAL SPECIFICATIONS

(Voltage polarities referenced to GND = 0 V; V_{CC} = + 5 V ± 10%; C1, C2, C3, C4 = 10 µF; T_A = – 40 to + 85°C)

Characteristic		Symbol	Min	Typ	Max	Unit
Input Turn–on Threshold $V_{DO1 - DO3} = V_{OL}$	Rx1 – Rx3	V_{on}	1.35	1.8	2.35	V
Input Turn–off Threshold $V_{DO1 - DO3} = V_{OH}$	Rx1 – Rx3	V_{off}	0.75	1.0	1.25	V
Input Threshold Hysteresis ($V_{on} - V_{off}$)	Rx1 – Rx3	V_{hys}	0.6	0.8	—	V
Input Resistance	Rx1 – Rx3	R_{in}	3.0	5.4	7.0	kΩ
High–Level Output Voltage $V_{Rx1 - Rx3}$ = – 3 V to – 25 V I_{OH} = – 20 µA I_{OH} = – 1 mA	DO1 – DO3	V_{OH}	 V_{CC} – 0.1 V_{CC} – 0.7	 — 4.3	 — —	V
Low–Level Output Voltage $V_{Rx1 - Rx3}$ = + 3 V to + 25 V I_{OL} = + 20 µA I_{OL} = + 1.6 mA	DO1 – DO3	V_{OL}	 — —	 0.01 0.5	 0.1 0.7	V

DRIVER ELECTRICAL SPECIFICATIONS

(Voltage polarities referenced to GND = 0 V: V_{CC} = +5 V ±10%; C1, C2, C3, C4 = 10 μF; T_A = −40 to +85°C)

Characteristic		Symbol	Min	Typ	Max	Unit
Digital Input Voltage	DI1 – DI3					V
Logic 0		V_{IL}	—	—	0.8	
Logic 1		V_{IH}	2.0	—	—	
Input Current	DI1 – DI3	I_{in}	—	—	± 1.0	μA
$GND \le V_{DI1 - DI3} \le V_{CC}$						
Output High Voltage	Tx1 – Tx3	V_{OH}	6	7.5	—	V
$V_{DI1 - DI3}$ = Logic 0, R_L = 3.0 kΩ	Tx1 – Tx6*		5	6.5	—	
Output Low Voltage	Tx1 – Tx3	V_{OL}	− 6	− 7.5	—	V
$V_{DI1 - DI3}$ = Logic 1, R_L = 3.0 kΩ	Tx1 – Tx6*		− 5	− 6.5	—	
Off Source Impedance (Figure 1)	Tx1 – Tx3	Z_{off}	300	—	—	Ω
Output Short–Circuit Current	Tx1 – Tx3	I_{SC}				mA
V_{CC} = + 5.5 V	Tx1 – Tx3 shorted to GND**		—	—	± 60	
	Tx1 – Tx3 shorted to ± 15 V***		—	—	± 100	

* Specifications for an MC145407 powering an MC145406 with three additional drivers/receivers.

** Specification is for one Tx output pin to be shorted at a time. Should all three driver outputs be shorted simultaneously, device power dissipation limits could be exceeded.

*** This condition could exceed package limitations.

SWITCHING CHARACTERISTICS (V_{CC} = + 5 V ± 10%; C1, C2, C3, C4 = 10 μF; T_A = − 40 to + 85°C; See Figures 2 and 3)

Characteristic		Symbol	Min	Typ	Max	Unit
Drivers						
Propagation Delay Time	Tx1 – Tx3	t_{PLH}				μs
Low–to–High						
R_L = 3 kΩ, C_L = 50 pF or 2500 pF			—	0.5	1	
High–to–Low		t_{PHL}				
R_L = 3 kΩ, C_L = 50 pF or 2500 pF			—	0.5	1	
Output Slew Rate	Tx1 – Tx3	SR				V/μs
Minimum Load: R_L = 7 kΩ, C_L = 0 pF			—	9.0	± 30	
Maximum Load: R_L = 3 kΩ, C_L = 2500 pF			4.0	—	—	
Receivers (C_L = 50 pF)						
Propagation Delay Time	DO1 – DO3					μs
Low–to–High		t_{PLH}	—	—	1	
High–to–Low		t_{PHL}	—	—	1	
Output Rise Time	DO1 – DO3	t_r	—	250	400	ns
Output Fall Time	DO1 – DO3	t_f	—	40	100	ns

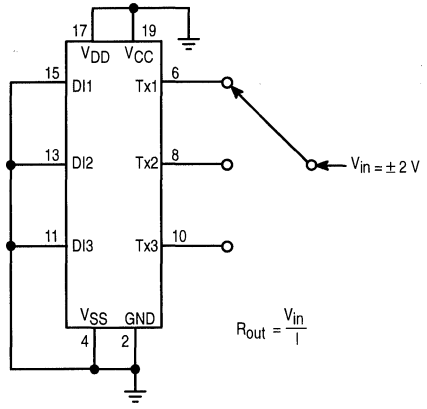


Figure 1. Power–Off Source Resistance

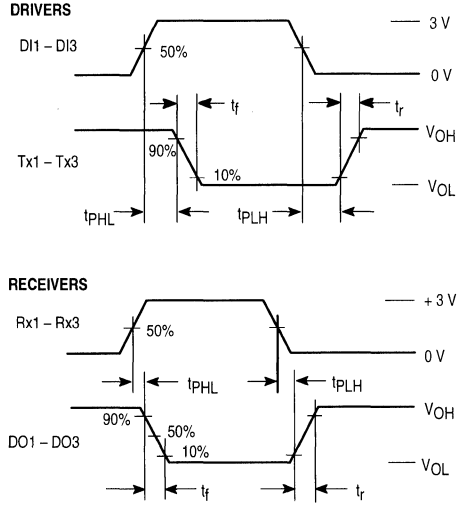


Figure 2. Switching Characteristics

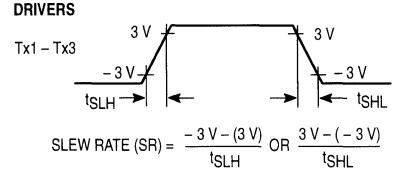


Figure 3. Slew Rate Characterization

PIN DESCRIPTIONS

V_{CC}
Digital Power Supply (Pin 19)

The digital supply pin, which is connected to the logic power supply. This pin should have a 0.33 μF capacitor to ground.

GND
Ground (Pin 2)

Ground return pin is typically connected to the signal ground pin of the EIA–232–E connector (Pin 7) as well as to the logic power supply ground.

V_{DD}
Positive Power Supply (Pin 17)

This is the positive output of the on–chip voltage doubler and the positive power supply input of the driver/receiver sections of the device. This pin requires an external storage capacitor to filter the 50% duty cycle voltage generated by the charge pump.

V_{SS}
Negative Power Supply (Pin 4)

This is the negative output of the on–chip voltage doubler/inverter and the negative power supply input of the driver/receiver sections of the device. This pin requires an external storage capacitor to filter the 50% duty cycle voltage generated by the charge pump.

C2+, C2–, C1–, C1+
Voltage Doubler and Inverter (Pins 1, 3, 18, 20)

These are the connections to the internal voltage doubler and inverter, which generate the V_{DD} and V_{SS} voltages.

Rx1, Rx2, Rx3
Receive Data Input (Pins 5, 7, 9)

These are the EIA–232–E receive signal inputs. A voltage between + 3 and + 25 V is decoded as a space and causes the corresponding DO pin to swing to ground (0 V). A voltage between – 3 and – 25 V is decoded as a mark, and causes the DO pin to swing up to V_{CC}.

DO1, DO2, DO3
Data Output (Pins 16, 14, 12)

These are the receiver digital output pins, which swing from V_{CC} to GND. Each output pin is capable of driving one LSTTL input load.

DI1, DI2, DI3
Data Input (Pins 15, 13, 11)

These are the high impedance digital input pins to the drivers. Input voltage levels on these pins must be between V_{CC} and GND.

Tx1, Tx2, Tx3
Transmit Data Output (Pins 6, 8, 10)

These are the EIA–232–E transmit signal output pins, which swing toward V_{DD} and V_{SS}. A logic 1 at a DI input causes the corresponding Tx output to swing toward V_{SS}. A logic 0 causes the output to swing toward V_{DD}. The actual levels and slew rate achieved will depend on the output loading ($R_L \parallel C_L$).

APPLICATIONS INFORMATION

ESD CONSIDERATIONS

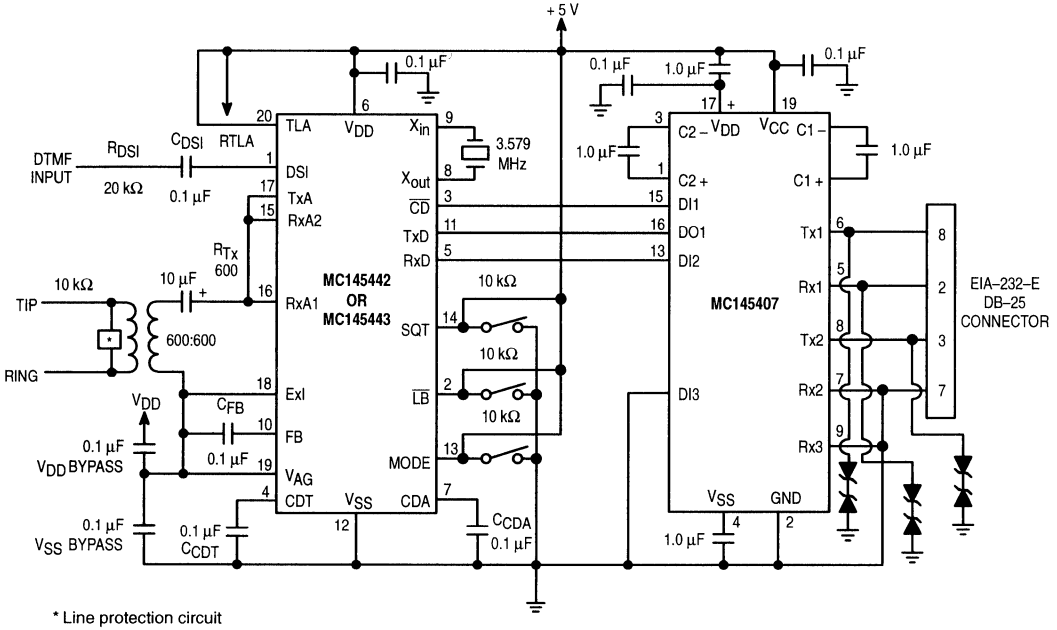
ESD protection on IC devices that have their pins accessible to the outside world is essential. High static voltages applied to the pins when someone touches them either directly or indirectly can cause damage to gate oxides and transistor junctions by coupling a portion of the energy from the I/O pin to the power supply busses of the IC. This coupling will usually occur through the internal ESD protection diodes. The key to protecting the IC is to shunt as much of the energy to ground as possible before it enters the IC. Figure 7 shows a technique which will clamp the ESD voltage at approximately + 15 V using the MMBZ15VDLT1. Any residual voltage which appears on the supply pins is shunted to ground through the 0.1 μF capacitors.

OPERATION WITH SMALLER VALUE CHARGE PUMP CAPS

The MC145407 is characterized in the electrical tables using 10 μF charge pump caps to illustrate its capability in driving a companion MC145406 or MC145403. If there is no requirement to support a second interface device and/or the charge pump is not being used to power any other components, the MC145407 is capable of complying with EIA–232–E and V.28 with smaller value charge pump caps. Table 1 summarizes driver performance with both 2.2 μF and 1.0 μF charge pump caps.

Table 1. Typical Performance

Parameter	2.2 μF	1.0 μF
Tx V_{OH} @ 25°C	7.3	7.2
Tx V_{OH} @ 85°C	7.2	7.1
Tx V_{OL} @ 25°C	– 6.5	– 6.4
Tx V_{OL} @ 85°C	– 6.1	– 6.0
Tx Slew Rate @ 25°C	8.0 V/μs	8.0 V/μs
Tx Slew Rate @ 85°C	7.0 V/μs	7.0 V/μs



* Line protection circuit

Figure 4. 5 V, 300 Baud Modem with EIA–232–E Interface

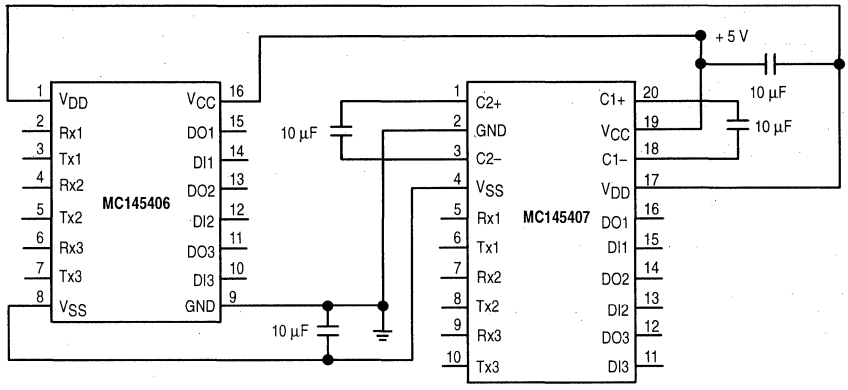


Figure 5. MC145406/MC145407 5 V Only Solution for up to Six EIA–232–E Drivers and Receivers

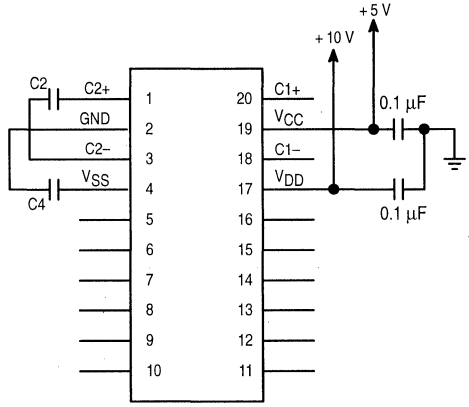


Figure 6. Two Supply Configuration (MC145407 Generates V_{SS} Only)

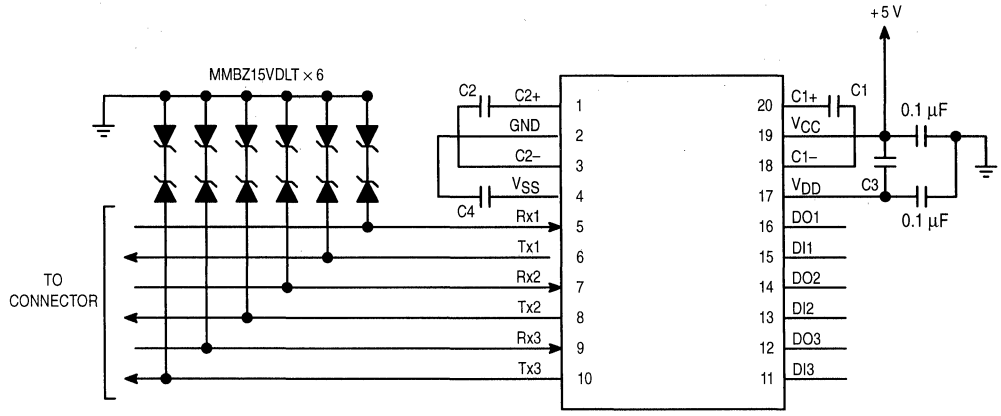
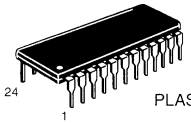


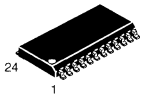
Figure 7. ESD Protection Scheme

MC145421
MC145425

ISDN Universal Digital Loop Transceivers II
(UDLT II)



P SUFFIX
PLASTIC PACKAGE
CASE 709



DW SUFFIX
SOG PACKAGE
CASE 751E

ORDERING INFORMATION

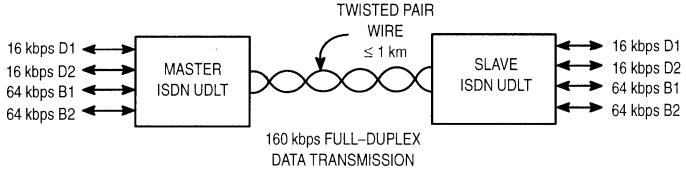
MC145421P	Plastic Package
MC145425P	Plastic Package
MC145421DW	SOG Package
MC145425DW	SOG Package

The MC145421 and MC145425 UDLTs are high–speed data transceivers capable of providing 160 kbps full–duplex data communication over 26 AWG and larger twisted–pair cable up to 1 km in length. These devices are primarily used in digital subscriber voice and data telephone systems. In addition, the devices meet and exceed the CCITT recommendations for data transfer rates of ISDNs on a single twisted pair. The devices utilize a 512 kbaud MDPSK burst modulation technique to supply the 160 kbps full–duplex data transfer rates. The 160 kbps rate is provided through four channels. There are two B channels, which are 64 kbps each. In addition, there are two D channels which are 16 kbps each.

The MC145421 and MC145425 UDLTs are designed for upward compatibility with the existing MC145422 and MC145426 80 kbps UDLTs, as well as compatibility with existing and evolving telephone switching hardware and software architectures.

The MC145421 (Master) UDLT is designed for use at the telephone switch line card while the MC145425 (Slave) UDLT is designed for use at the remote digital telset or data terminal.

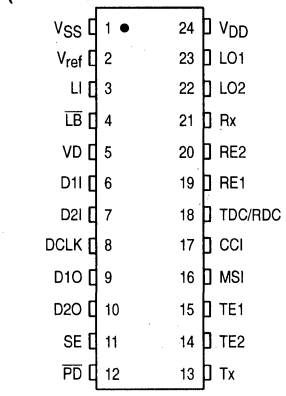
- Employs CMOS Technology in Order to Take Advantage of Its Proven Capability for Complex Analog and Digital LSI Functions
- Provides Synchronous Full–Duplex 160 kbps Voice and Data Communication in a 2B+2D Format for ISDN Compatibility
- Provides the CCITT Basic Access Data Transfer Rate (2B+D) for ISDNs on a Single Twisted Pair Up to 1 km
- Compatible with Existing and Evolving Telephone Switch Architectures and Call Signaling Schemes
- Protocol Independent
- Single + 5 V Power Supply
- MC145421EVK is Available



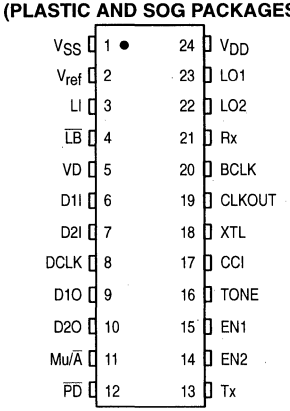
REV 2 (Replaces ADI1251)
9/95

PIN ASSIGNMENTS

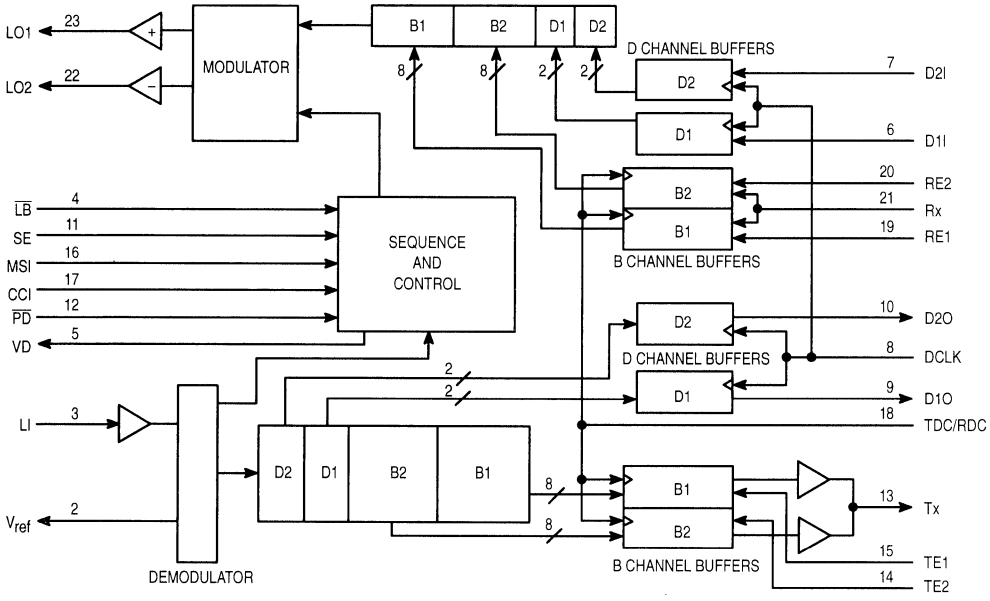
MC145421 — MASTER
(PLASTIC AND SOG PACKAGES)



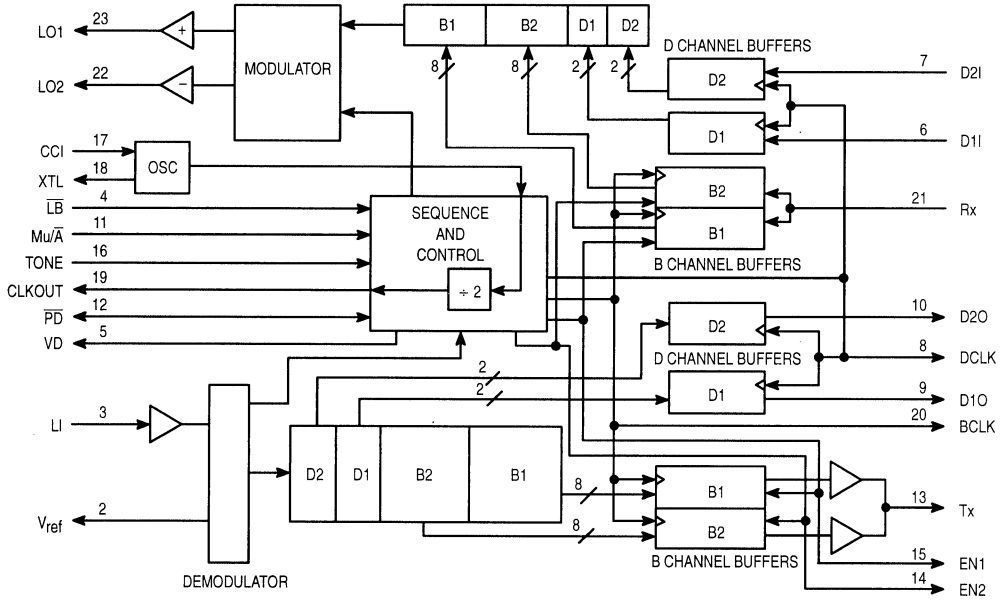
MC145425 — SLAVE
(PLASTIC AND SOG PACKAGES)



MC145421 MASTER ISDN BLOCK DIAGRAM



MC145425 SLAVE ISDN BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Voltage Referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	$V_{DD} - V_{SS}$	– 0.5 to 6.5	V
Voltage Any Pin to V_{SS}	V	– 0.5 to V_{DD} + 0.5	V
DC Current, Any Pin (Excluding V_{DD}, V_{SS})	I	± 10	mA
Operating Temperature	T_A	– 40 to + 85	°C
Storage Temperature	T_{stg}	– 85 to + 150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

2

RECOMMENDED OPERATING CONDITIONS (T_A = – 40 to + 85°C)

Parameter	Pins	Min	Typ	Max	Unit
DC Supply Voltage	V_{DD}	4.5	5.0	5.5	V
Frame Rate MC145421 (See Note)	MSI	—	8.0	—	kHz
MC145421/25 Frame Slip Rate (See Note)	—	—	—	0.25	%
CCI Clock Frequency	—	—	8.192	8.29	MHz
TDC/RDC Data Clocks (for Master)	—	0.128	—	4.1	MHz
DCLK	—	0.016	—	4.1	MHz
Modulation Baud Rate (CCI/16)	LO1, LO2	—	512	—	kHz

NOTE: The slave's crystal frequency divided by 1024 must equal the master's MSI frequency ± 0.25% for optimum operation. Also, the 8.192 MHz input at the master divided by 1024 must be within 0.048% of the master's 8 kHz MSI clock frequency.

DIGITAL CHARACTERISTICS (V_{DD} = 5 V, T_A = – 40 to + 85°C)

Parameter		Min	Max	Unit
Input High Level		3.5	—	V
Input Low Level		—	1.5	V
Input Current, V_{DD}		—	15	mA
Input Current (Digital Pins)		—	5	µA
Input Capacitance		—	10	pF
Output High Current (Except Tx on Master and Slave, and $\overline{PD}$ on the Slave)	V_{OH} = 2.5 V_{OH} = 4.6	– 1.7 – 0.36	— —	mA
Tx Output High Current	V_{OH} = 2.5 V_{OH} = 4.6	– 3.4 – 0.7	— —	mA
$\overline{PD}$ (Slave) Output High Current (See Note)	V_{OH} = 2.5	—	– 90	µA
Output Low Current (Except Tx on Master and Slave, and $\overline{PD}$ on Slave)	V_{OL} = 0.4 V_{OL} = 0.8	0.36 0.8	— —	mA
Tx Output Low Current	V_{OL} = 0.4 V_{OL} = 0.8	1.7 3.5	— —	mA
$\overline{PD}$ (Slave) Output Low Current (See Note)	V_{OL} = 0.4	30	60	µA
Tx Three–State Impedance		100	—	kΩ
XTL Output High Current	V_{OH} = 4.6	—	– 450	µA
XTL Output Low Current	V_{OH} = 0.4	450	—	µA

NOTE: To overdrive $\overline{PD}$ from a low level to 3.5 V, or a high level to 1.5 V requires a minimum of ± 800 µA drive capability.

ANALOG CHARACTERISTICS (V_{DD} = 5 V, T_A = 0 to 70°C)

Parameter	Min	Max	Unit
Modulation Differential Amplitude RL = 880 Ω (LO1 – LO2)	4.6	—	Vpeak
Modulation Differential DC Offset	—	40	mV
V_{ref} Voltage (Typically 9/20 • ($V_{DD} - V_{SS}$))	2.0	2.5	V
PCM Tone Level	– 22	– 18	dBm
Demodulator Input Amplitude	50	—	mVpeak
Demodulator Input Impedance (LI to V_{ref})	75	300	kΩ

MC145421 MASTER PIN DESCRIPTIONS

V_{DD}
Positive Supply (Pin 24)

The most positive power supply pin, normally + 5 V with respect to V_{SS}.

V_{SS}
Negative Supply (Pin 1)

The most negative supply pin and logic ground, normally 0 V.

V_{ref}
Reference Output (Analog Ground) (Pin 2)

This pin is the output of the internal reference supply and should be bypassed to V_{DD} and V_{SS} with 0.1 μF capacitors. This pin usually serves as an analog ground reference for transformer coupling of the device's incoming bursts from the line. No external dc load should be placed on this pin.

LI
Line Input (Pin 3)

This pin is an input to the demodulator for the incoming bursts. The input has an internal 240 kΩ resistor tied to the V_{ref} pin, so an external capacitor or line transformer may be used to couple the input signal to the device with no dc offset.

LO1, LO2
Line Driver Outputs (Pins 23, 22)

These push–pull outputs drive the twisted pair transmission line with a 512 kHz modified DPSK (MDPSK) burst each 125 μs, in other words at an 8 kHz rate. When not modulating the line, these pins are driven to the active high state — being the same potential, they create an ac short. When used in conjunction with feed resistors, proper line termination is maintained.

SE
Signal Enable Input (Pin 11)

At the time of a negative transition on this pin, an internal latch stores the states of $\overline{LB}$ and $\overline{PD}$ for as long as SE is held low. During this time, the VD, DO1, and DO2 outputs are driven to the high–impedance state. When SE is high, all pins function normally.

$\overline{LB}$
Loopback Control (Pin 4)

A low level on this pin ties the internal modulator output to the internal demodulator input, which loops the entire burst for testing purposes. During the loopback operation, the LI input is ignored and the LO1 and LO2 drivers are driven to the active high level. The state of this pin is internally latched if the SE pin is held low. This feature is only active when the $\overline{PD}$ input is high.

$\overline{PD}$
Power–Down Input (Pin 12)

When held low the ISDN UDLT powers down, except the circuitry that is necessary to demodulate an incoming burst and to output VD, B, and D channel data bits. When $\overline{PD}$ is brought high, the ISDN UDLT powers up. Then, it begins transmitting every MSI period to the slave device, shortly after the rising edge of MSI. The state of this pin is latched if the SE pin is held low.

VD
Valid Data Output (Pin 5)

A high level on this pin indicates that a valid line transmission has been demodulated. A valid transmission burst is determined by proper synchronization and the absence of detected bit errors. VD changes state on the rising edge of MSI when $\overline{PD}$ is high. When $\overline{PD}$ is low, VD changes state at the end of demodulation of a transmission burst and does not change again until three MSI rising edges have occurred, at which time it goes low, or until the next demodulation of a burst. VD is a standard B–series CMOS output and is high impedance when SE is low.

MSI
Master Sync Input (Pin 16)

This pin is the master, 8 kHz frame reference input. The rising edge of MSI loads B and D channel data which had been input during the previous frame into the modulator section of the device and initiates the outbound burst onto the twisted–pair cable. The rising edge of MSI also initiates the buffering of the B and D channel data demodulated during the previous frame. MSI should be approximately leading edge aligned with the TDC/RDC data clock input pin.

CCI
High–Speed Clock Input (Pin 17)

An 8.192 MHz clock should be supplied to this input. The 8.192 MHz input should be 50% duty cycle. However, it may free–run with respect to all other clocks without performance degradation.

D1I, D2I
D Channel Signaling Bit Inputs (Pins 6, 7)

These inputs are 16 kbps serial data inputs. Two bits should be clocked into each of these inputs between the rising edges of the MSI frame reference clock. The first bit of each D channel is clocked into an intermediate buffer on the first falling edge of the DCLK following the rising edge of MSI. The second bit of each D channel is clocked in on the next negative transition of the DCLK. If further DCLK negative edges occur, new information is serially clocked into the buffer replacing the previous data one bit at a time. Buffered D channel data bits are burst to the slave device on the next rising edge of the MSI frame reference clock.

D1O, D2O
D Channel Signal Outputs (Pins 9, 10)

These serial outputs provide the 16 kbps D channel signaling information from the incoming burst. Two data bits should be clocked out of each of these outputs between the rising edges of the MSI frame reference clock. The rising edge of MSI produces the first bit of each D channel on its respective pin. Circuitry then searches for a negative D channel clock edge. This tells the D channel data shift register to produce the second D channel bit on the next rising edge of the DCLK. Further positive edges of the DCLK recirculate the D channel output buffer information.

DCLK
D Channel Clock Input (Pin 8)

This input is the transmit and receive data clock for both D channels. D channel input and output operation is described in the D1O, D2O pin description.

Tx
Transmit Data Output (Pin 13)

This pin is high impedance when both TE1 and TE2 are low. This pin serves as an output for B channel information received from the slave device. The B channel data is under the control of TE1, TE2, and TDC/RDC. (See TE1, TE2 description.)

Rx
Receive Data Input (Pin 21)

B channel data is input on this pin and is controlled by the RE1, RE2, and TDC/RDC pins. (See RE1, RE2 description.)

TE1, TE2
Transmit Data Enable Input (Pins 14, 15)

These two pins control the output of data for their respective B channel on the Tx output pin. When both TE1 and TE2 are low, the Tx pin is high impedance. The rising edge of the respective enable produces the first bit of the selected B channel data on the Tx pin. Internal circuitry then scans for the next negative transition of the TDC/RDC clock. Following this event, the next seven bits of the selected B channel data are output on the next seven rising edges of the TDC/RDC data clock. When TE1 and TE2 are high simultaneously, data on the Tx pin is undefined. TE1 and TE2 should be approximately leading–edge aligned with the TDC/RDC data clock signal. In order to keep the Tx pin out of the high–impedance state, these enable lines should be high while the respective B channel data is being output.

RE1, RE2
Receive Data Enable Inputs (Pins 19, 20)

These inputs control the input of B channel data on the Rx pin of the device. The rising edge of the respective enable signal causes the device to load the selected receive data buffer with data from the Rx pin on the next eight falling edges of the TDC/RDC clock input. The RE1 and RE2 enables should be roughly leading–edge aligned with the TDC/RDC data clock input. These enables are rising edge sensitive and need not be high for the entire B channel input period.

TDC/RDC
Transmit/Receive Data Clock Input (Pin 18)

This input is the transmit and receive data clock for the B channel data. As described in the TE1/TE2 and the RE1/RE2 sections, output data changes state on the rising edge of this signal, and input data is read on the falling edges of this signal. TDC/RDC should be roughly leading–edge aligned with the TE1, TE2, RE1, and RE2 enables, as well as the MSI frame reference signal.

MC145425 SLAVE PIN DESCRIPTIONS

V_{DD}
Positive Supply (Pin 24)

The most positive power supply pin, normally + 5 V with respect to V_{SS}.

V_{SS}
Negative Supply (Pin 1)

The most negative supply pin and logic ground, normally 0 V.

V_{ref}
Reference Output (Analog Ground) (Pin 2)

This pin is the output of the internal reference supply and should be bypassed to V_{DD} and V_{SS} with 0.1 μF capacitors. This pin usually serves as an analog ground reference for transformer coupling of the device's incoming bursts from the line. No external dc load should be placed on this pin.

LI
Line Input (Pin 3)

This pin is an input to the demodulator for the incoming bursts. The input has an internal 240 kΩ resistor tied to the V_{ref} pin, an external capacitor or line transformer may be used to couple the input signal to the device with no dc offset.

LO1, LO2
Line Driver Outputs (Pins 23, 22)

These push–pull outputs drive the twisted pair transmission line with a 512 kHz modified DPSK (MDPSK) burst each 125 μs; in other words at an 8 kHz frame rate. When not modulating the line, these pins are driven to the active high state — being the same potential, they create an ac short. When used in conjunction with feed resistors, proper line termination is maintained.

CLK OUT
Clock Output (Pin 19)

This pin serves as a buffered output of the crystal frequency divided by two. This clock is provided for systems using the MC145428 Data Set Interface asynchronous/synchronous terminal adaptor device.

$\overline{LB}$
Loopback Control Input (Pin 4)

When this pin is low, the incoming B channels from the master are burst back to the master — instead of the Rx B channel input data. The B channel data from the master continues to be output at the slave's Tx pin during loopback. If the TONE and the loopback function are active simultaneously, the loopback function overrides the TONE function. D channel data is not affected by $\overline{LB}$.

VD
Valid Data Output (Pin 5)

A high on this pin indicates that a valid transmission burst has been demodulated. A valid burst is determined by proper synchronization and the absence of detected bit errors. If no transmissions from the master have been received in the last 250 μs, as determined by an internal oscillator, VD will go low.

Mu/$\overline{A}$
Tone Format Input (Pin 11)

This pin determines the PCM code for the 500 Hz square wave tone generated when the TONE input is high — Mu–Law (Mu/$\overline{A}$ = 1) or CCITT A–Law (Mu/$\overline{A}$ = 0) format.

TONE
Tone Enable Input (Pin 16)

A high on this pin causes a 500 Hz square wave PCM tone to be inserted in place of the demodulated B channel data on B channel 1. This feature allows the designer to provide audio feedback for telset keyboard operations.

$\overline{PD}$
Power Down Input/Output (Pin 12)

This is a bidirectional pin with a weak output driver so that it can be externally overdriven. When held low, the ISDN UDLT is powered down, and the only active circuitry is that which is necessary for demodulation, generation of EN1, EN2, BCLK, and DCLK, and outputting of the data bits and VD. When held high, the ISDN UDLT is powered up and transmits normally in response to received bursts from the master. If the ISDN UDLT is powered up for 250 µs — which is derived from an internal oscillator and no bursts from the master have occurred — the ISDN slave UDLT generates a free–running set of EN1, EN2, BCLK, and DCLK signals and sends a burst to the master device every other 125 µs frame. This is a wake–up signal to the master.

When $\overline{PD}$ is floating and a burst from the master is demodulated, the weak output drivers will try to force $\overline{PD}$ high. It will try to force $\overline{PD}$ low if 250 µs have elapsed without a burst from the master being successfully demodulated. This allows the slave device to self power up and down in demand–powered loop systems.

CCI
Crystal Input (Pin 17)

Normally, an 8.192 MHz crystal is tied between this pin and the XTL pin. A 10 MΩ resistor between CCI and XTL and 25 pF capacitors from CCI and XTL to V_{SS} are required to ensure stability and start–up. CCI may also be driven with an external 8.192 MHz signal if a crystal is not desired.

XTL
Crystal Output (Pin 18)

This pin is capable of driving one external CMOS input and 15 pF of additional load capacitance.

D1I, D2I
D Channel Inputs (Pins 6, 7)

These two pins are inputs for the 16 kbps D data channels. The D channel data bits are clocked in serially on the negative edge of the 16 kbps DCLK output pin.

D1O, D2O
D Channel Outputs (Pins 9, 10)

These two pins are outputs for the 16 kbps D data channels. These pins are updated on the rising edges of the slave DCLK output pin.

Tx
Transmit Data Output (Pin 13)

This line is an output for the B channel data received from the master. B channel 1 data is output on the first eight cycles of the BCLK output when EN1 is high. B channel 2 data is output on the next eight cycles of the BCLK, when EN2 is high. B channel data bits are clocked out on the rising edge of the BCLK output pin.

DCLK
D Channel Clock Output (Pin 8)

This output is the transmit and receive data clock for both D channels. It starts upon demodulation of a burst from the master device. This signal is rising edge aligned with the EN1 and BCLK signals. After the demodulation of a burst, the DCLK line completes two cycles and then remains low until another burst from the master is demodulated. In this manner synchronization with the master is established and any clock slip between master and slave is absorbed each frame.

Rx
Receive Data Input (Pin 21)

This pin is an input for the B channel data. B channel 1 data is clocked in on the first eight falling edges of the BCLK output following the rising edge of the EN1 output. B channel 2 data is clocked in on the next eight falling edges of the BCLK following the rising edge of the EN2 output.

EN1
B Channel 1 Enable Output (Pin 15)

This line is an 8 kHz enable signal for the input and output of the B channel 1 data. While EN1 is high, B channel 1 data is clocked out on the Tx pin on the first eight rising edges of the BCLK. During this same time, B channel 1 input data is clocked in on the Rx pin on the first eight falling edges of the BCLK. The VD pin is also updated on the rising edge of the EN1 signal. EN1 serves as the slave device's 8 kHz frame reference signal.

EN2
B Channel 2 Enable Output (Pin 14)

This pin is the logical inverse of the EN1 output and is used to signal the time slot for the input and output of data for the B channel 2 data.

BCLK
B Channel Data Clock Output (Pin 20)

This is a standard B series output which provides the data clock for the B channel data. This clock signal is 128 kHz and begins operating upon the successful demodulation of a burst from the master. At this time, EN1 goes high and BCLK starts toggling. BCLK remains active for 16 periods, at the end of which time it remains low until another burst is received from the master. In this manner synchronization between the master and slave is established and any clock slippage is absorbed each frame.

BACKGROUND

The MC145421 and the MC145425 ISDN UDLTs provide an economical means of sending and receiving two B channels (64 kbps each) of voice/data and two D channels (16 kbps each) of signal data in a two–wire configuration at distances up to one kilometer. There are two ISDN UDLTs, master and slave. The master UDLT is compatible with existing and evolving PABX architectures. This device transmits 2B+2D channels of data to the remote slave. At the remote end, the slave device presents a replica of the PBX backplane to the terminal devices.

These devices permit existing digital PBX architectures to remain unchanged and provide enhanced voice/data communication services throughout the PBX service area by simply replacing a subscriber's line card and telset.

All operations occur within the boundaries of an 8 kHz frame (125 μs). In the master, the frame sequence begins on the rising edge of MSI. In the slave, the frame begins after the demodulation of a burst from the master. The slave initializes its timing controls at this point to stay synchronized with the master.

During one 125 μs frame four main activities are performed:

1. Previously buffered 2B+2D channel data is burst to the other end.
2. New 2B+2D channel data is accepted for the next frame's transmission.
3. An incoming burst is demodulated and stored.
4. 2B+2D channel data from the previous demodulated frame is output.

The bursts are 20 bits long, composed of two 8–bit B channels and two 2–bit D channels. Bursts are encoded using a modified DPSK method at 512 kHz. Since a single wire pair is used, half–duplex operation is used. A 512 kHz burst is sent from end to end in a ping–pong fashion. This method provides apparent full–duplex 160 kbps transmission of data at distances up to one kilometer.

GENERAL

The ISDN UDLT consists of a modulator, a demodulator, intermediate data registers, receive and transmit data registers, and sequencing and control logic. The Rx and Tx buffers interface digitally to the line card backplane signals, while the modulator and demodulator interface to the twisted pair transmission media. Intermediate data registers buffer data between these main components. The ISDN UDLT is intended to operate with a 5 V power supply and can be driven by CMOS or TTL logic.

MASTER OPERATION

In the master, the rising edge of MSI initiates the 125 μs frame. B channel data is clocked into the Rx registers under control of TDC/RDC, RE1, and RE2. This data is combined with the D channel data clocked in on pins D1I and D2I by the DCLK. The resulting 20–bit packet is stored for the next frame transmission to the slave UDLT.

The burst output to the slave consists of the 2B+2D data loaded during the previous frame. The burst received from the slave is demodulated and stored for outputting in the following frame.

B channel bits demodulated in the previous frame are output on the Tx pin under control of TDC/RDC, TE1, and TE2. Demodulated D channel bits are output on the D1O and D2O output pins. The indication of a valid burst demodulation is the VD output, which is updated at the start of every frame.

SLAVE OPERATION

In normal slave operation, the main synchronizing event is completion of demodulating a burst from the master UDLT. This action initializes the 125 μs frame boundary of the slave. During the slave frame, B channel data is loaded and stored under control of the BCLK, EN1, and EN2 outputs. D channel data is loaded at D1I and D21 under control of the DCLK output.

The demodulated burst from the master is separated into its D channel and B channel components and output on the D1O, D2O, and Tx pins. The return burst to the master consisting of previously loaded 2B+2D data is transmitted eight bauds after the completion of demodulation of the master's burst. This provides a period for line transients to diminish.

The start of the slave frame initiates two cycles of the 16 kHz DCLK, and one cycle each of the 8 kHz EN1 and EN2 enables. After completing their cycles, these outputs remain low until another demodulation signals the start of a new slave frame. In this manner, clock slip between the master and slave UDLTs is absorbed each frame.

POWER–DOWN OPERATION

When $\overline{PD}$ is low in the master, the ISDN UDLT is powered down and only that circuitry necessary to demodulate incoming bursts is active. No transmissions to the slave occur during power down. If the master is receiving bursts from the slave, the VD pin will change state upon completion of the demodulation.

When the $\overline{PD}$ input pin is driven high, the master ISDN UDLT is powered up. In this mode, the master bursts to the slave every frame. B and D channel data can be loaded and unloaded and VD is updated on the MSI rising edge.

If no bursts are received by the master, whether powered up or not, the B channel data is unknown and the D channel bits will remain at their last known values.

The $\overline{PD}$ pin on the slave UDLT is bidirectional with a weak output driver that can be overdriven externally. When low, either externally or internally derived, the slave is powered down. No bursts to the master can be transmitted. EN1, EN2, BCLK, and DCLK outputs are inactive during power down except when TONE is high or a burst has been received from the master. B and D channel data can be loaded and unloaded, and VD is updated upon completion of demodulation of an incoming burst from the master. Input B and D channel data is not transmitted until the slave is powered up, in which case the first burst contains the most recently loaded data.

When the $\overline{PD}$ pin is high, the slave is powered up and transmits every frame, the data enables and clocks are output, and data can be loaded and unloaded.

TIME–OUT OPERATION

Time–out is an operating state in both the UDLT master and slave devices. This state indicates that no incoming bursts have been demodulated, forcing the VD pin low. An internal counter is incremented for each frame that does not contain an incoming burst. The counter is reset upon demodulating a burst from the far end. Time–out can occur whether the device is powered up or down.

In the master, time–out begins on the rising edge of the third MSI following the last received burst. This is equivalent to two MSI frames. The VD output is forced low during time–out. The B channel output data will be unknown, but the D channel bits will remain at their last values. Successful demodulation of a burst from the slave will result in leaving the time–out state on the next rising MSI edge.

When the $\overline{PD}$ pin is used as an output on the slave UDLT, time–out controls the pin. Time–out forces the $\overline{PD}$ output low to indicate that the device has powered itself down. In this case, the slave will not transmit to the master. However, when a valid burst is received, time–out ends and the $\overline{PD}$ pin is driven high to indicate power up. This feature allows the slave UDLT to self–power–up and down in demand–powered loop systems.

NOTE

The slave uses a free running clock during time–out. After a long period without a burst from the master, the timing between master and slave could be such that more than one burst will be needed to resync the two devices.

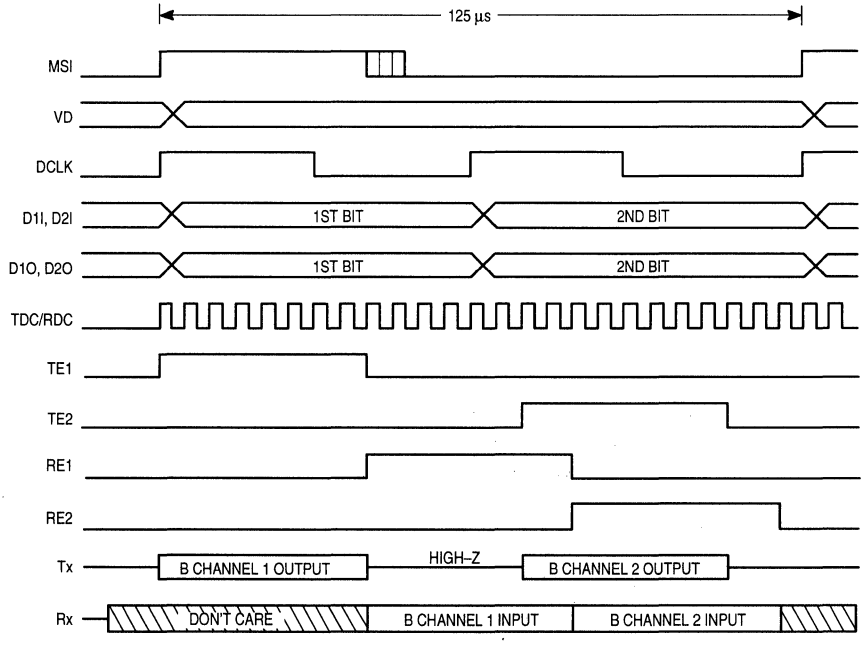


Figure 1. Typical MC145421 Master ISDN UDLT Timing

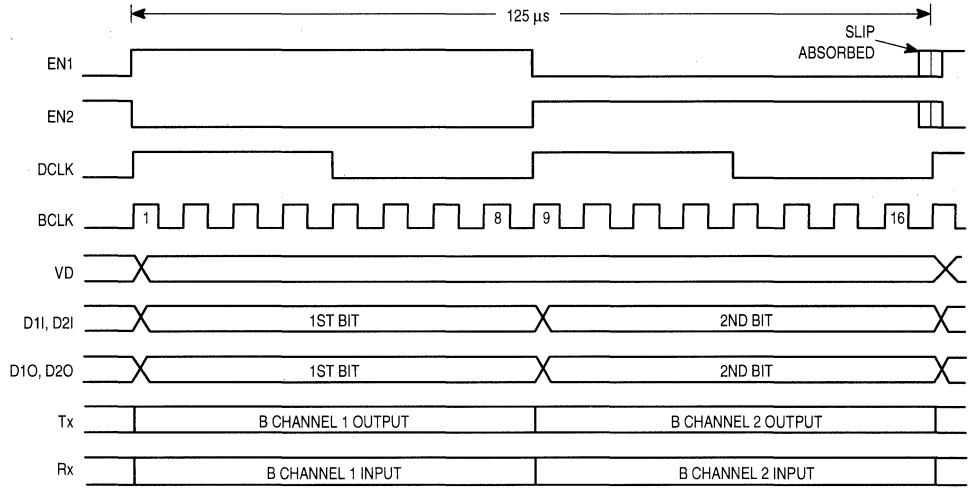
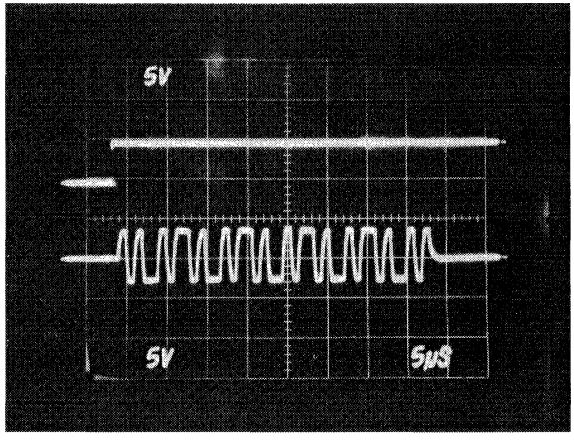


Figure 2. MC145425 Slave ISDN UDLT Timing



Top Trace: MSI
Bottom Trace: Outgoing burst measured at LI (with respect to V_{ref})

Figure 3. Master Burst

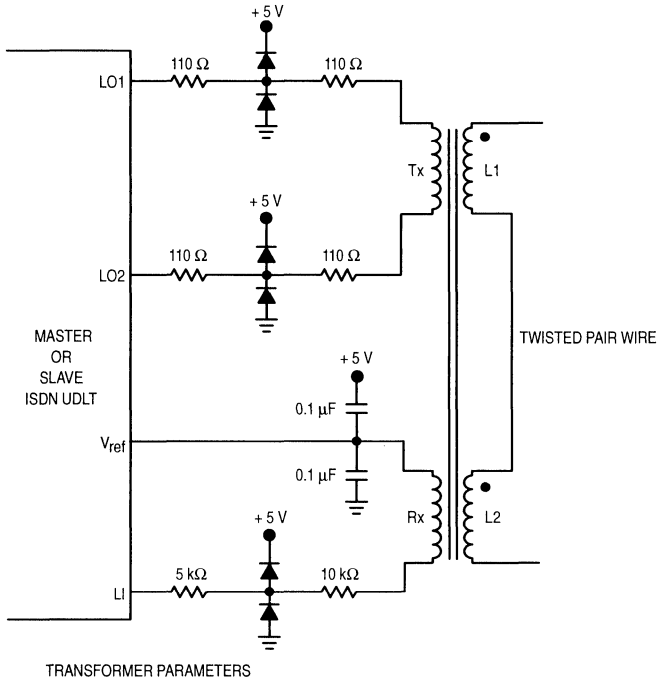


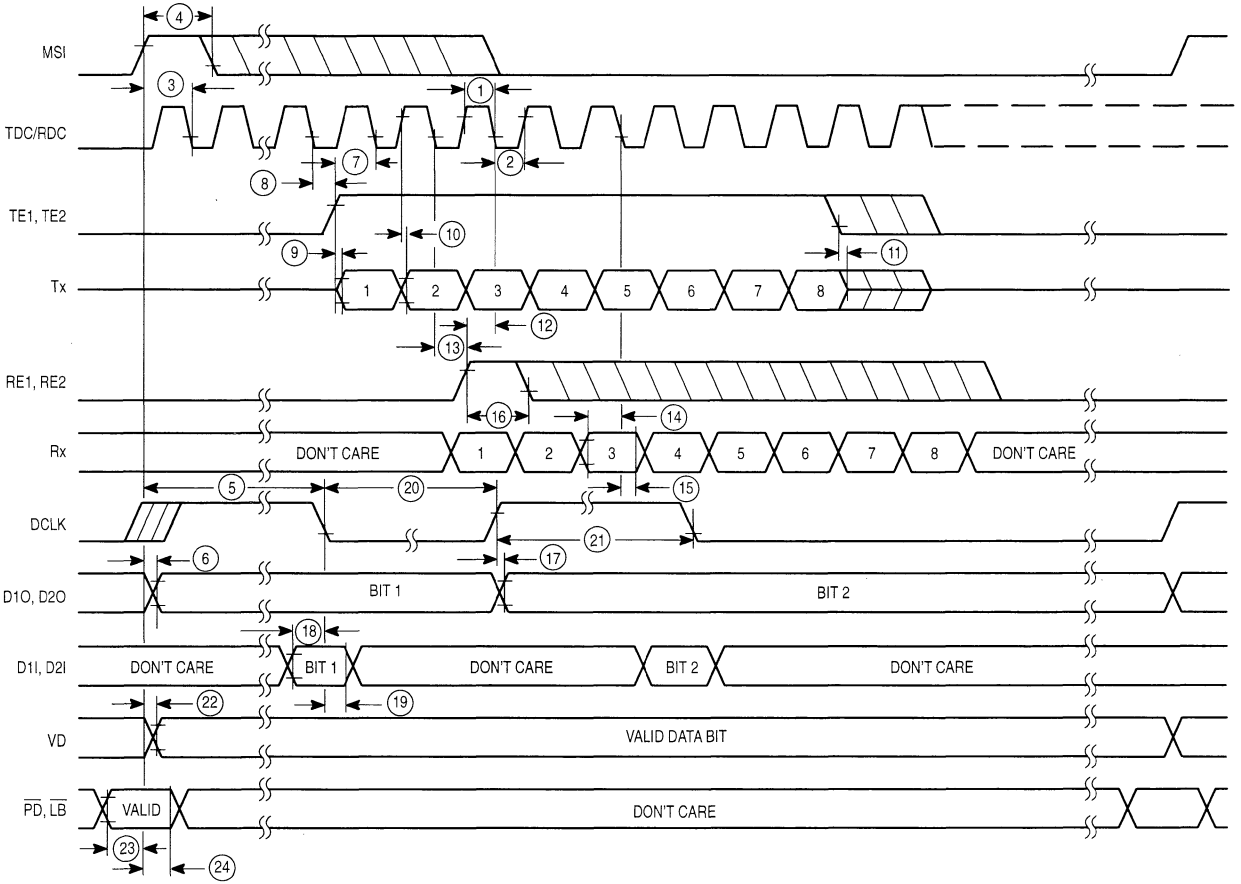
Figure 4. Interface to Twisted Pair Wire

SWITCHING CHARACTERISTICS (V_{DD} = 5 V, T_A = 0 to 70°C; C_{Load} = 50 pF)

No.*	Parameter	Min	Max	Unit
Master Timing				
1	TDC/RDC Pulse Width High	110	—	ns
2	TDC/RDC Pulse Width Low	110	—	ns
3	MSI Rising Edge to TDC/RDC Falling Edge	90	—	ns
4	MSI Pulse Width	200	—	ns
5	MSI Rising Edge to First DCLK Falling Edge	90	—	ns
6	MSI Rising Edge to First D1O, D2O Bit Valid	—	100	ns
7	TE1, TE2 Rising Edge to TDC/RDC Falling Edge	110	—	ns
8	TDC/RDC Falling Edge to TE1, TE2 Rising Edge	20	—	ns
9	TE1, TE2 Rising Edge to First Tx Data Bit Valid	—	50	ns
10	TDC/RDC Rising Edge to Tx Data Bits 2 Through 8 Valid	—	50	ns
11	TE1, TE2 Falling Edge to Tx High–Impedance	—	70	ns
12	REI, RE2 Rising Edge to TDC/RDC Falling Edge	110	—	ns
13	TDC/RDC Falling Edge to RE1, RE2 Rising Edge	20	—	ns
14	Rx Data Setup (Data Valid Before TDC/RDC Falling Edge)	50	—	ns
15	Rx Data Hold (Data Valid After TDC/RDC Falling Edge)	20	—	ns
16	RE1, RE2 Pulse Width	220	—	ns
17	DCLK Rising Edge to D1O, D2O Bit Valid	—	135	ns
18	D1I, D2I Data Setup (Data Valid Before DCLK Falling Edge)	50	—	ns
19	D1I, D2I Data Hold (Data Valid After DCLK Falling Edge)	20	—	ns
20	DCLK Pulse Width Low	110	—	ns
21	DCLK Pulse Width High	110	—	ns
22	MSI Rising Edge to VD Valid	—	150	ns
23	$\overline{PD}$, $\overline{LB}$ Setup ($\overline{PD}$, $\overline{LB}$ Valid Before MSI Rising Edge)	50	—	ns
24	$\overline{PD}$, $\overline{LB}$ Hold ($\overline{PD}$, $\overline{LB}$ Valid After MSI Rising Edge)	20	—	ns
Slave Timing				
25	BCLK Pulse Width High (CCI = 8.192 MHz)	3.66	4.15	µs
26	BCLK Pulse Width Low (CCI = 8.192 MHz)	3.66	4.15	µs
27	EN1 or EN2 Rising Edge to BCLK Rising Edge	75	175	ns
28	EN1 or EN2 Rising Edge to DCLK Rising Edge	—	± 50	ns
29	EN1 or EN2 Rising Edge to First Tx Data Bit Valid	—	50	ns
30	BCLK Rising Edge to Tx Data Bits 2 Through 8 Valid	—	– 75	ns
31	DCLK Pulse Width High (CCI = 8.192 MHz)	31.0	31.5	µs
32	DCLK Pulse Width Low (CCI = 8.192 MHz)	31.0	31.5	µs
33	DCLK Rising Edge to D1O, D2O Bits Valid	—	50	ns
34	Rx Setup (Rx Data Valid Before BCLK Falling Edge)	175	—	ns
35	Rx Hold (Rx Data Valid After BCLK Falling Edge)	20	—	ns
36	D1I, D2I Setup (D1I, D2I Valid Before DCLK Falling Edge)	50	—	ns
37	D1I, D2I Hold (D1I, D2I Valid After DCLK Falling Edge)	20	—	ns
38	EN1 Rising Edge to VD Valid	—	50	ns
SE Pin Timing				
39	$\overline{LB}$, $\overline{PD}$ Hold ($\overline{LB}$, $\overline{PD}$ Valid After SE Falling Edge)	20	—	ns
40	D1O, D2O, VD High Impedance After SE Falling Edge	—	70	ns
41	D1O, D2O, VD Valid After SE Rising Edge	60	—	ns
42	$\overline{LB}$, $\overline{PD}$ Setup ($\overline{LB}$, $\overline{PD}$ Valid Before SE Rising Edge)	50	—	ns

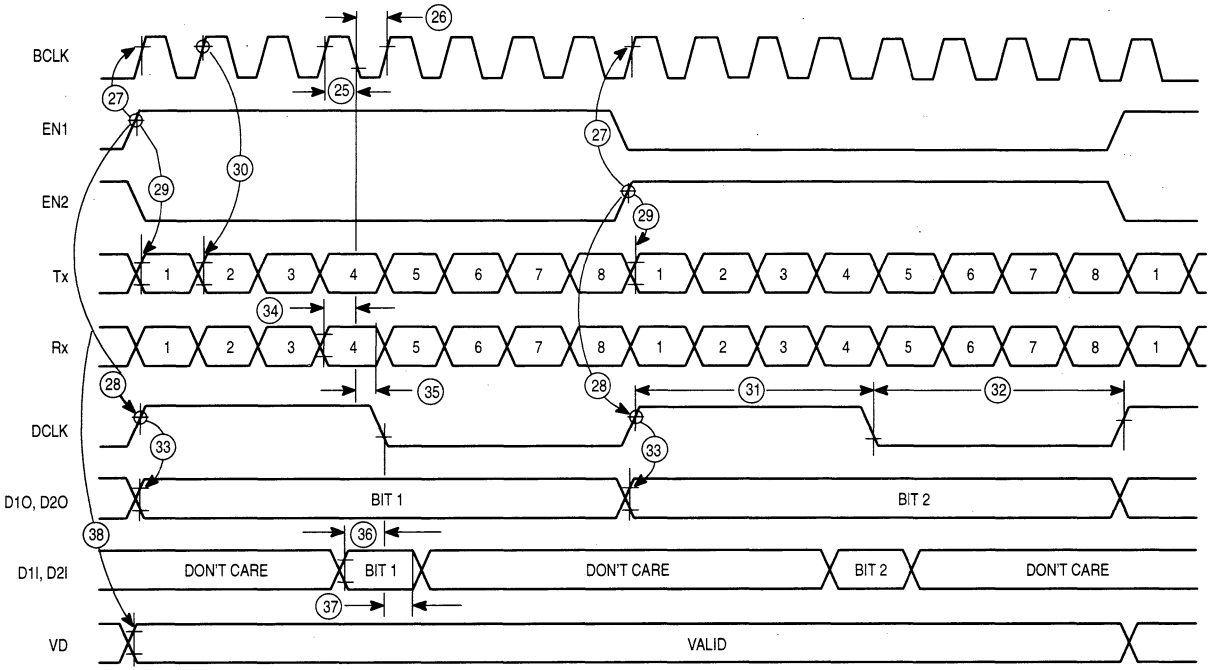
* See Switching Characteristics waveforms.

MASTER SWITCHING CHARACTERISTICS

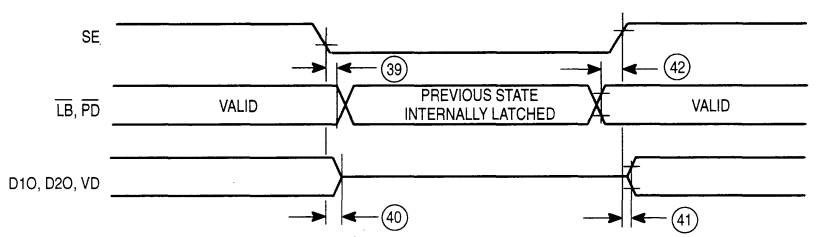


NOTE: All measurement thresholds are 30% or 70% of V_{DD}.

SLAVE SWITCHING CHARACTERISTICS



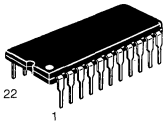
MASTER SE PIN TIMING



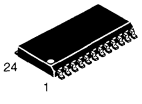
Note: All measurement thresholds are 30% or 70% of V_{DD}.

MC145422
MC145426

Universal Digital-Loop Transceivers (UDLT)



P SUFFIX
PLASTIC DIP
CASE 708



DW SUFFIX
SOG PACKAGE
CASE 751E

ORDERING INFORMATION

MC145422P	Plastic DIP
MC145426P	Plastic DIP
MC145422DW	SOG Package
MC145426DW	SOG Package

The MC145422 and MC145426 UDLTs are high–speed data transceivers that provide 80 kbps full–duplex data communication over 26 AWG and larger twisted–pair cable up to two kilometers in distance. Intended primarily for use in digital subscriber voice/data telephone systems, these devices can also be used in remote data acquisition and control systems. These devices utilize a 256 kilobaud modified differential phase shift keying burst modulation technique for transmission to minimize RFI/ EMI and crosstalk. Simultaneous power distribution and duplex data communication can be obtained using a single twisted–pair wire.

These devices are designed for compatibility with existing, as well as evolving, telephone switching hardware and software architectures.

The UDLT chip–set consists of the MC145422 Master UDLT for use at the telephone switch linecard and the MC145426 Slave UDLT for use at the remote digital telset and/or data terminal.

The devices employ CMOS technology in order to take advantage of their reliable low–power operation and proven capability for complex analog/digital LSI functions.

- Provides Full–Duplex Synchronous 64 kpbs Voice/Data Channel and Two 8 kbps Signaling Data Channels Over One 26 AWG Wire Pair Up to Two Kilometers
- Compatible with Existing and Evolving Telephone Switch Architectures and Call Signaling Schemes
- Automatic Detection Threshold Adjustment for Optimum Performance Over Varying Signal Attenuations
- Protocol Independent
- Single 5 V Power Supply
- 22–Pin PDIP, 24–Pin SOG Packages
- Application Notes AN943, AN949, AN968, AN946, and AN948

MC145422 Master UDLT

- Pin Controlled Power–Down and Loopback Features
- Signaling and Control I/O Capable of Sharing Common Bus Wiring with Other UDLTs
- Variable Data Clock — 64 kHz to 2.56 MHz
- Pin Controlled Insertion/Extraction of 8 kbps Channel into LSB of 64 kbps Channel for Simultaneous Routing of Voice and Data Through PCM Voice Path of Telephone Switch

MC145426 Slave UDLT

- Compatible with MC145500 Series PCM Codec–Filters
- Pin Controlled Loopback Feature
- Automatic Power–Up/Power–Down Feature
- On–Chip Data Clock Recovery and Generation
- Pin Controlled 500 Hz D3 or CCITT Format PCM Tone Generator for Audible Feedback Applications

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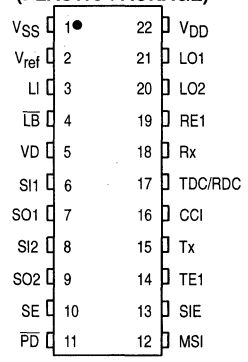
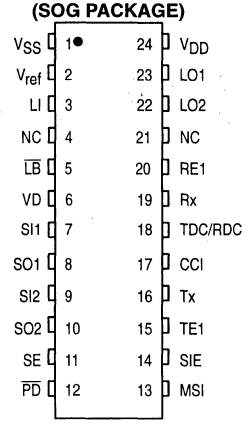
PIN ASSIGNMENTS

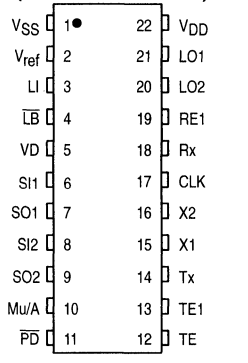
MC145422 — MASTER (PLASTIC PACKAGE)



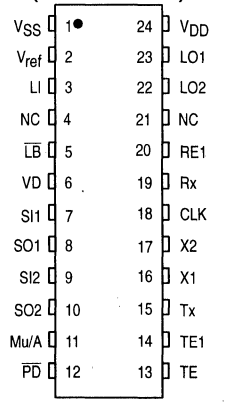
MC145422 — MASTER (SOG PACKAGE)



MC145426 — SLAVE (PLASTIC PACKAGE)

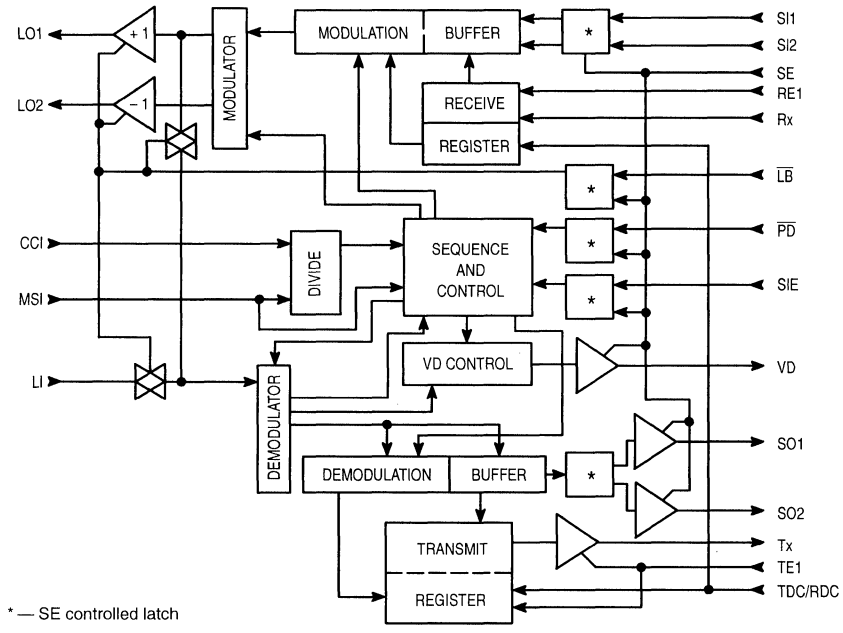


MC145426 — SLAVE (SOG PACKAGE)



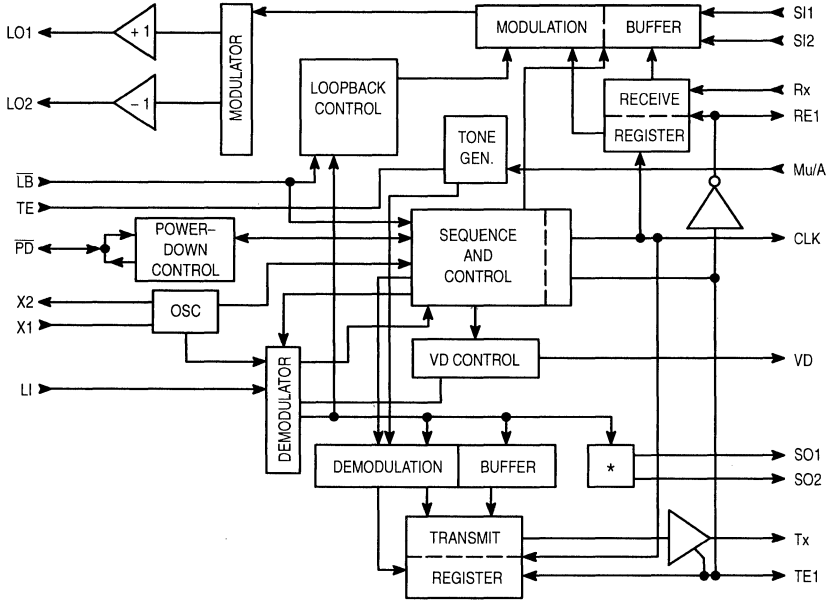
NC = NO CONNECTION

MC145422 MASTER UDLT BLOCK DIAGRAM



* — SE controlled latch

MC145426 SLAVE UDLT BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Voltage Referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	$V_{DD} - V_{SS}$	− 0.5 to + 9.0	V
Voltage, Any Pin to V_{SS}	V	− 0.5 to V_{DD} + 0.5	V
DC Current, Any Pin (Excluding V_{DD}, V_{SS})	I	± 10	mA
Operating Temperature	T_A	− 40 to + 85	°C
Storage Temperature	T_{stg}	− 85 to + 150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

2

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to 70°C)

Parameter	Pins	Min	Max	Unit
DC Supply Voltage	V_{DD}	4.5	5.5	V
Power Dissipation ($\overline{PD}$ = V_{DD}, V_{DD} = 5 V)	V_{DD}	—	80	mW
Power Dissipation ($\overline{PD}$ = V_{SS}, TE = V_{SS})	V_{DD}	—	75	mW
MC145422 Frame Rate	MSI	7.9	8.1	kHz
MC145422 — MC145426 Frame Rate Slip (See Note 1)	—	—	0.25	%
CCI Clock Frequency (MSI = 8 kHz)	CCI	—	2.048	MHz
Data Clock Rate MC145422	TDC, RDC	64	2560	kHz
Modulation Baud Rate (See Note 2)	LO1, LO2	—	256	kHz

NOTES:
1. The MC145426 crystal frequency divided by 512 must equal the MC145422 MSI Frequency ± 0.25% for optimum operation.
2. Assumes crystal frequency of 4.096 MHz for the MC145426 and 2.048 MHz CCI for the MC145422.

DIGITAL CHARACTERISTICS (V_{DD} = 5 V, T_A = 0 to 70°C)

Parameter		Min	Max	Unit
Input High Level		3.5	—	V
Input Low Level		—	1.5	V
Input Current	Except LI LI	− 1.0 − 100	1.0 100	µA
Input Capacitance		—	7.5	pF
Output High Current (Except Tx on MC145422 and Tx and $\overline{PD}$ on MC145426)	V_{OH} = 2.5 V V_{OH} = 4.6 V	− 1.7 − 0.36	— —	mA
Output Low Current (Except Tx on MC145422 and Tx and $\overline{PD}$ on MC145426)	V_{OL} = 0.4 V V_{OL} = 0.8 V	0.36 0.8	— —	mA
$\overline{PD}$ Output High Current (MC145426) (See Note 1)	V_{OH} = 2.5 V V_{OH} = 4.6 V	− 90 − 10	— —	µA
$\overline{PD}$ Output Low Current (MC145426) (See Note 1)	V_{OL} = 0.4 V V_{OL} = 0.8 V	60 100	— —	µA
Tx Output High Current	V_{OH} = 2.5 V V_{OH} = 4.6 V	− 3.4 − 0.7	— —	mA
Tx Output Low Current	V_{OL} = 0.4 V V_{OL} = 0.8 V	1.7 3.5	— —	mA
Tx Input Impedance (TE1 = V_{SS}, MC145422)		100	—	kΩ
Crystal Frequency (MC145426, Note 2)		4.0	4.4	MHz
PCM Tone (TE = V_{DD}, MC145426)		− 22	− 18	dBm0
Three–State Current (SO1, SO2, VD, Tx on MC145422, Tx on MC145426)		—	± 1	µA
V_{ref} Voltage (See Note 3)		2	3	V
X2 — Oscillator Output High Drive Current (MC145426) (See Note 4)	V_{OH} = 4.6 V	− 450	—	µA
X2 — Oscillator Output Low Drive Current (MC145426) (See Note 4)	V_{OL} = 0.4 V	450	—	µA

NOTES:
1. To overdrive $\overline{PD}$ from a low level to 3.5 V or a high level to 1.5 V requires a minimum of ± 800 µA drive capability.
2. The MC145426 crystal frequency divided by 512 must equal the MC145422 MSI frequency ± 0.25% for optimum performance.
3. V_{ref} typically (9/20 V_{DD} − V_{SS}).
4. Output drive when X1 is being driven from an external clock.

ANALOG CHARACTERISTICS (V_{DD} = 5 V, T_A = 0 to 70°C)

Parameter		Min	Max	Unit
Modulation Differential Amplitude (R_L = 440 Ω)	LO1 to LO2	4.5	6.0	V p–p
Modulation Differential DC Offset		0	300	mV
Demodulator Input Amplitude (See Note)		0.050	2.5	V peak
Demodulator Input Impedance		50	150	kΩ

NOTE: The input level into the demodulator to reliably demodulate incoming bursts. Input referenced to V_{ref}.

MC145422 SWITCHING CHARACTERISTICS (V_{DD} = 5 V, T_A = 25°C, C_L = 50 pF)

Parameter		Figure No.	Symbol	Min	Max	Unit
Input Rise Time	All Digital Inputs	1	t_r	—	4	µs
Input Fall Time	All Digital Inputs	1	t_f	—	4	µs
Pulse Width	TDC/RDC, RE1, MSI	1	t_w(H,L)	90	—	ns
CCI Duty Cycle		1	t_w(H,L)	45	55	%
Data Clock Frequency	TDC/RDC	—	t_{DC}	64	2560	kHz
Propagation Delay Time	MSI to SO1, SO2 VD ($\overline{PD}$ = V_{DD}) TDC to Tx	2 3	t_{PLH}, t_{PHL}	— —	90 90	ns
MSI to TDC/RDC Setup Time		4	t_{su3} t_{su4}	90 40	— —	ns
TE1/RE1 to TDC/RDC Setup Time		4	t_{su3} t_{su4}	90 40	— —	ns
Rx to TDC/RDC Setup Time		5	t_{su5}	60	—	ns
Rx to TDC/RDC Hold Time		5	t_{h1}	60	—	ns
SI1, SI2 to MSI Setup Time		6	t_{su6}	60	—	ns
SI1, SI2 to MSI Hold Time		6	t_{h2}	60	—	ns

MC145426 SWITCHING CHARACTERISTICS (V_{DD} = 5 V, T_A = 25°C, C_L = 50 pF)

Parameter		Figure No.	Symbol	Min	Max	Unit
Input Rise Time	All Digital Inputs	1	t_r	—	4	µs
Input Fall Time	All Digital Inputs	1	t_f	—	4	µs
Clock Output Pulse Width	CLK	1	t_w(H,L)	3.8	4.0	µs
Crystal Frequency		—	f_{X1}	4.086	4.1	MHz
Propagation Delay Times	TE1 Rising to CLK (TE = V_{DD}) TE1 Rising to CLK (TE = V_{SS}) CLK to TE1 Falling CLK to RE1 Rising RE1 Falling to CLK (TE = V_{DD}) RE1 Falling to CLK (TE = V_{SS}) CLK to Tx TE1 to SO1, SO2	7 7 7 8 8 8 9 9	t_{p1} t_{p1} t_{p2} t_{p3} t_{p4} t_{p4} t_{p5} t_{p6}	– 50 438 — — – 50 438 — —	50 538 40 40 50 538 90 90	ns
Rx to CLK Setup Time		5	t_{su5}	60	—	ns
Rx to CLK Hold Time		5	t_{h1}	60	—	ns
SI1, SI2 to TE1 Setup Time		6	t_{su6}	60	—	ns
SI1, SI2 to TE1 Hold Time		6	t_{h2}	60	—	ns

SWITCHING WAVEFORMS

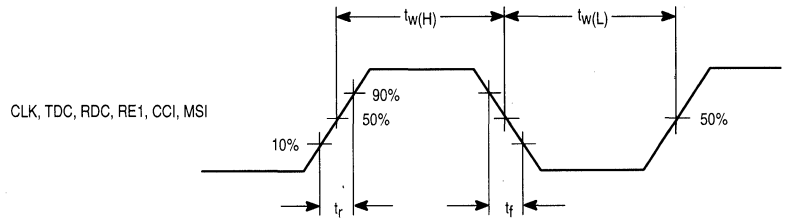


Figure 1.

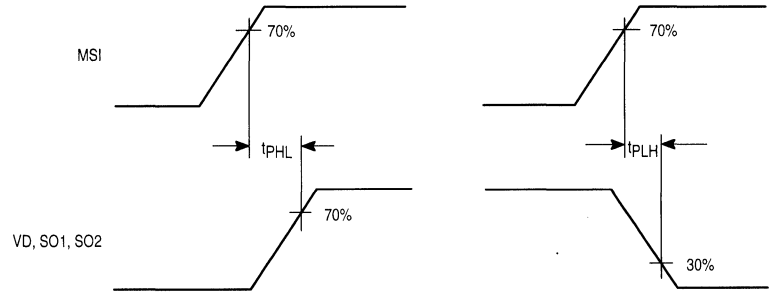


Figure 2.

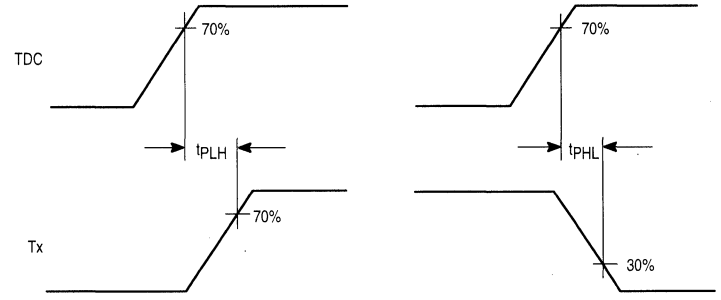


Figure 3.

SWITCHING WAVEFORMS (continued)

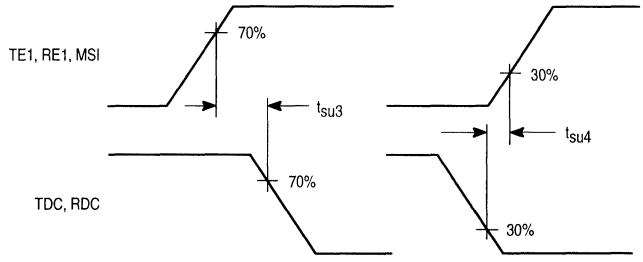


Figure 4.

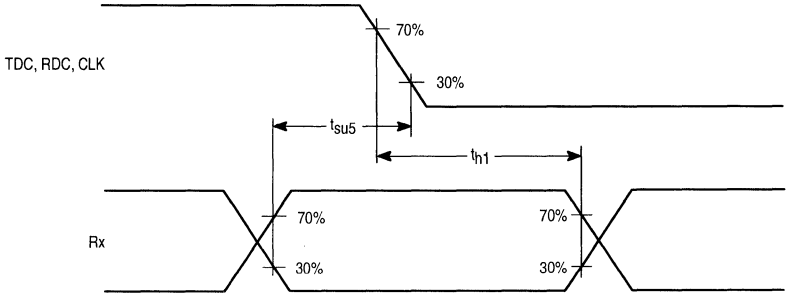


Figure 5.

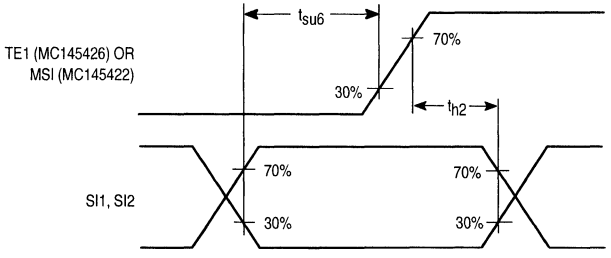


Figure 6.

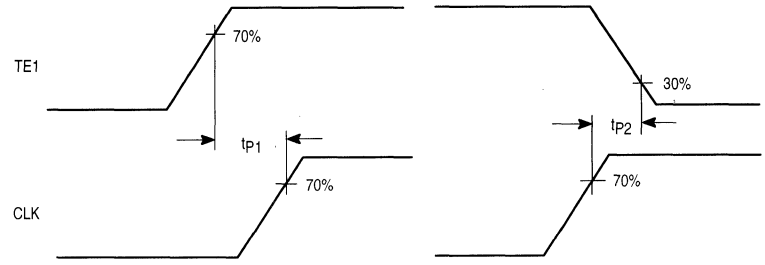


Figure 7.

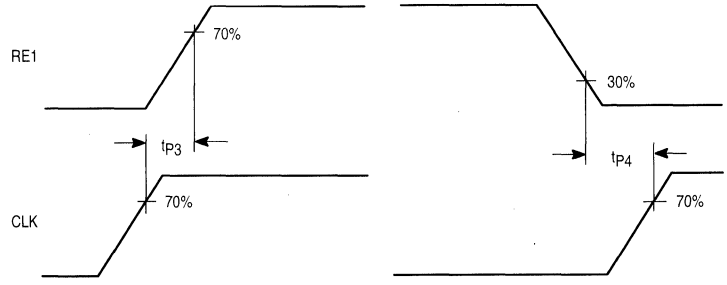


Figure 8.

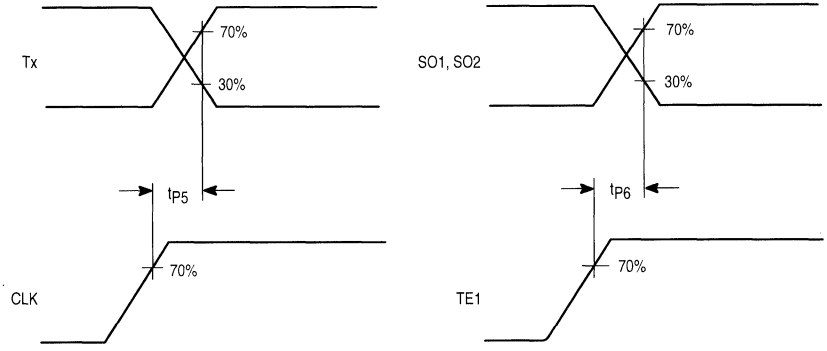


Figure 9.

MC145422 MASTER UDLT PIN DESCRIPTIONS

V_{DD}
Positive Supply

Normally 5 V.

V_{SS}
Negative Supply

This pin is the most negative supply pin, normally 0 V.

V_{ref}
Reference Output

This pin is the output of the internal reference supply and should be bypassed to V_{DD} and V_{SS} by 0.1 μF capacitors. No external dc load should be placed on this pin.

LI
Line Input

This input to the demodulator circuit has an internal 100 kΩ resistor tied to the internal reference node so that an external capacitor and/or line transformer may be used to couple the input signal to the part with no dc offset.

$\overline{LB}$
Loopback Control

A low on this pin disconnects the LI pin from internal circuitry, drives LO1, LO2 to V_{ref} and internally ties the modulator output to the demodulator input which loops the part on itself for testing in the system. The state of this pin is internally latched if the $\overline{SE}$ pin is brought and held low. Loopback is active only when $\overline{PD}$ Is high.

VD
Valid Data Output

A high on this pin indicates that a valid line transmission has been demodulated. A valid transmission is determined by proper sync and the absence of detected bit errors. VD changes state on the leading edge of MSI when $\overline{PD}$ is high. When $\overline{PD}$ is low, VD changes state at the end of demodulation of a line transmission. VD is a standard B–series CMOS output and is high impedance when SE is held low.

SI1, SI2
Signaling Bit Inputs

Data on these pins is loaded on the rising edge of MSI for transmission to the slave. The state of these pins is internally latched if SE is held low.

SO1, SO2
Signaling Bit Outputs

These outputs are received signaling bits from the slave UDLT and change state on the rising edge of MSI if $\overline{PD}$ is high, or at the completion of demodulation if $\overline{PD}$ is low. These outputs have standard B–series CMOS drive capability and are high impedance if the SE pin is held low.

SE
Signal Enable Input

If held high, the $\overline{PD}$, $\overline{LB}$, SI1, SI2, and SIE inputs and the SO1, SO2, and VD outputs function normally. If held low, the state of these inputs is latched and held internally while the outputs are high impedance. This allows these pins to be bussed with those of other UDLTs to a common controller.

$\overline{PD}$
Power–Down Input

If held low, the UDLT ceases modulation. In power–down, the only active circuit is that which is necessary to demodulate an incoming burst and output the signal and valid data bits. Internal data transfers to the transmit and receive registers cease. When brought high, the UDLT powers up, and waits three positive MSI edges or until the end of an incoming transmission from the slave UDLT and begins transmitting every MSI period to the slave UDLT on the next rising edge of the MSI.

MSI
Master Sync Input

This pin is the system sync and initiates the modulation on the twisted pair. MSI should be approximately leading–edge aligned with TDC/RDC.

SIE
Signal Insert Enable

This pin, when held high, inserts signal bit 2 received from the slave into the LSB of the outgoing PCM word at Tx and will ignore the SI2 pin and use in place the LSB of the incoming PCM word at Rx for transmission to the slave. The PCM word to the slave will have LSB forced low in this mode. In this manner, signal bit 2 to/from the slave UDLT is inserted in to the PCM words the master sends and receives from the backplane for routing through the PABX for simultaneous voice/data communication. The state of this pin is internally latched if the SE pin is brought and held low.

TE1
Transmit Data Enable 1 Input

This pin controls the outputting of data on the Tx pin. While TE1 is high, the Tx data is presented on the eight rising edges of TDC/RDC. TE1 is also a high–impedance control of the Tx pin. If MSI occurs during this period, new data will be transferred to the Tx output register in the ninth high period of TDC/RDC after TE1 rises; otherwise, it will transfer on the rising edge of MSI. TE1 and TDC/RDC should be approximately leading–edge aligned.

Tx
Transmit Data Output

This three–state output presents new voice data during the high periods of TDC/RDC when TE1 is high (see TE1).

CCI
Convert Clock Input

A 2.048 MHz clock signal should be applied to this pin. The signal is used for internal sequencing and control. This signal should be coherent with MSI for optimum performance but may be asynchronous if slightly worse error rate performance can be tolerated.

TDC/RDC
Transmit/Receive Data Clock

This pin is the transmit and receive data clock and can be 64 kHz to 2.56 MHz. Data is output at the Tx pin while TE1 is high on the eight rising edges of TDC/RDC after the rising edge of TE1. Data on the Rx pin is loaded into the receive register of the UDLT on the eight falling edges of TDC/RDC after a positive transition on RE1. This clock should be approximately leading–edge aligned with MSI.

Rx
Receive Data

Voice data is clocked into the UDLT from this pin on the falling edges of TDC/RDC under the control of RE1.

RE1
Receive Data Enable 1 Input

A rising edge on this pin will enable data on the Rx pin to be loaded into the receive data register on the next eight falling edges of the data dock, TDC/RDC. RE1 and TDC/RDC should be approximately leading–edge aligned.

2

LO1, LO2
Line Driver Outputs

These outputs drive the twisted pair line with 256 kHz modified DPSK bursts each frame and are push–pull. These pins are driven to V_{ref} when not modulating the line.

MC145426 SLAVE UDLT PIN DESCRIPTIONS

V_{DD}
Positive Supply

Normally 5 V.

V_{SS}
Negative Supply

This pin is the most negative supply pin, normally 0 V.

V_{ref}
Reference Output

This pin is the output of the internal reference supply and should be bypassed to V_{DD} and V_{SS} by 0.1 µF capacitors. No external dc load should be placed on this pin.

LI
Line Input

This input to the demodulator circuit has an internal 100 kΩ resistor tied to the internal reference node (V_{ref}) so that an external capacitor and/or line transformer may be used to couple the signal to this part with no dc offset.

$\overline{LB}$
Loopback Control

When this pin is held low and $\overline{PD}$ is high (the UDLT is receiving transmissions from the master), the UDLT will use the 8 bits of demodulated PCM data in place of the 8 bits of Rx data in the return burst to the Master, thereby looping the part back on itself for system testing. SI1 and SI2 operate normally in this mode. CLK will be held low during loopback operation.

VD
Valid Data Output

A high on this pin indicates that a valid line transmission has been demodulated. A valid transmission is determined by proper sync and the absence of detected bit errors.VD changes state on the leading edge of TE1. If no transmissions from the master have been received in the last 250 µs (derived from the internal oscillator), VD will go low without TE1 rising since TE1 is not generated in the absence of received transmissions from the master (see TE pin description for the one exception to this).

SI1, SI2
Signaling Bit Inputs

Data on these pins is loaded on the rising edge of TE1 for transmission to the master. If no transmissions from the master are being received and $\overline{PD}$ is high, data on these pins will be loaded into the part on an internal signal. Therefore, data on these pins should be steady until synchronous communication with the master has been established, as indicated by the high on VD.

SO1, SO2
Signaling Bit Outputs

These outputs are received signaling bits from the master UDLT and change state on the rising edge of TE1. These outputs have standard B–series CMOS output drive capability.

$\overline{PD}$
Power–Down Input/Output

This is a bidirectional pin with weak output drivers such that it can be overdriven externally. When held low, the UDLT is powered down and the only active circuitry is that which is necessary for demodulation, TE1/RE1/CLK generation upon demodulation, the outputting of data received from the master, and updating of VD status. When held high, the UDLT is powered up and transmits in response to transmissions from the master. If no received bursts from the master have occurred when powered up for 250 µs (derived from the internal oscillator frequency), the UDLT will generate a free running 125 µs internal clock from the internal oscillator and will burst a transmission to the master every other internal 125 µs clock using data on the SI1 and SI2 pins and the last data word loaded into the receive register. The weak output drivers will try to force $\overline{PD}$ high when a transmission from the master is demodulated and will try to force it low if 250 µs have passed without a transmission from the master. This allows the slave UDLT to self power–up and down in demand powered loop systems.

TE
Tone Enable

A high on this pin generates a 500 Hz square wave PCM tone and inserts it in place of the demodulated voice PCM word from the master for outputting to the Tx pin to the telset mono–circuit. A high on TE will generate TE1 and CLK from the internal oscillator when the slave is not receiving bursts from the master so that the PCM square wave can be loaded into the codec–filter. This feature allows the user to provide audio feedback for the telset keyboard depressions except during loopback. During loopback of the slave UDLT, CLK is defeated so a tone cannot be generated in this mode.

TE1
Transmit Data Enable 1 Output

This is a standard B–series CMOS output which goes high after the completion of demodulation of an incoming transmission from the master. It remains high for 8 CLK periods and then low until the next burst from the master is demodulated. While high, the voice data just demodulated is output on the first eight rising edges of CLK at the Tx pin. The signaling data just demodulated is output on SO1 and SO2 on TE1's rising edge, as is VD.

Tx
Transmit Data Output

This is a standard B–series CMOS output. Voice data is output on this pin on the rising edges of CLK while TE1 is high and is high impedance when TE1 is low.

X1
Crystal Input

A 4.096 MHz crystal is tied between this pin and X2. A 10 MΩ resistor across X1 and X2 and 25 pF capacitors from X1 and X2 to V_{SS} are required for stability and to ensure startup. X1 may be driven by an external CMOS clock signal if X2 is left open.

X2
Crystal Output

This pin is capable of driving one external CMOS input and 15 pF of additional capacitance (see X1 pin description).

CLK
Clock Output

This is a standard B–series CMOS output which provides the data clock for the telset codec–filter. It is generated by dividing the oscillator down to 128 kHz and starts upon the completion of demodulation of an incoming burst from the master. At this time, CLK begins and TE1 goes high. CLK will remain active for 16 periods, at the end of which it will remain low until another transmission from the master is demodulated. In this manner, sync from the master is established in the slave and any clock slip between the master and the slave is absorbed each frame. CLK is generated in response to an incoming burst from the master, however, if TE is brought high, then CLK and TE1/RE1 are generated from the internal oscillator until TE is brought low or an incoming burst from the master is received. CLK is disabled when $\overline{LB}$ is held low.

Rx
Receive Data Input

Voice data from the telset codec–filter is input on this pin on the first eight falling edges of CLK after RE1 goes high.

Mu/A
Tone Digital Format Input

This pin determines if the PCM code of the 500 Hz square wave tone, when TE is high, is Mu–Law (Mu/A = 1) or A–Law (Mu/A = 0) format.

RE1
Receive Data Enable 1 Output

This is a standard B–series CMOS output which is the inverse of TE1 (see TE1 pin description).

LO1, LO2
Line Driver Outputs

These outputs drive the twisted pair line with 256 kHz modified DPSK bursts each frame and are push–pull. These pins are driven to V_{ref} when the device is not modulating.

BACKGROUND

The MC145422 master and MC145426 slave UDLT transceiver ICs main application is to bidirectionally transmit the digital signals present at a codec–filter digital–PABX backplane interface over normal telephone wire pairs. This allows the remoting of the codec–filter in a digital telephone set and enables each set to have a high speed data access to the PABX switching facility. In effect, the UDLT allows each PABX subscriber direct access to the inherent 64 kbps data routing capabilities of the PABX.

The UDLT provides a means for transmitting and receiving 64 kbits of voice data and 16 kbps of signaling data in two–wire format over normal telephone pairs. The UDLT is a two–chip set consisting of a master and a slave. The master UDLT replaces the codec–filter and SLIC on the PABX line card, and transmits and receives data over the wire pair to the teleset. The UDLT appears to the linecard and backplane as if it were a PCM Codec–Filter and has almost the same digital interface features as the MC145500 series codec–filters. The slave UDLT is located in the telset and interfaces the codec–filter to the wire pair. By hooking two UDLTs back–to–back, a repeater can also be formed. The master and slave UDLTs operate in a frame synchronous manner, sync being established at the slave by the timing of the master's transmission. The master's sync is derived from the PABX frame sync.

The UDLT operates using one twisted pair. Eight bits of voice data and two bits of signaling data are transmitted and received each frame in a half–duplex manner (i.e., the slave waits until the transmission from the master is completely received before transmitting back to the master). Transmission occurs at 256 kHz bit rate using a modified form of DPSK. This "ping– pong" mode will allow transmission of data at distances up to two kilometers before turnaround delay becomes a problem. The UDLT is so defined as to allow this data to be handled by the linecard, backplane, and PABX as if it were just another voice conversation. This allows existing PABX hardware and software to be unchanged and yet provides switched 64 kbps voice or data communications throughout its service area by simply replacing a subscriber's linecard and teleset. A feature in the master allows one of the two signaling bits to be inserted and extracted from the backplane PCM word to allow simultaneous voice and data transmission through the PABX. Both UDLTs have a loop-back feature by which the device can be tested in the user system.

The slave UDLT has the additional feature of providing a 500 Hz Mu–Law or A–Law coded square wave to the codec–filter when the TE pin is brought high. This can be used to provide audio feedback in the telset during keyboard depressions.

CIRCUIT DESCRIPTION

GENERAL

The UDLT consists of a modulator, demodulator, two intermediate data buffers, sequencing and control logic, and transmit and receive data registers. The data registers interface to the linecard or codec–filter digital interface signals, the modulator and demodulator interface the twisted pair transmission medium, while the intermediate data registers buffer data between these two sections. The UDLT is

intended to operate on a single 5 V supply and can be driven by TTL or CMOS logic.

MASTER OPERATION

In the master, data from the linecard is loaded into the receive register each frame from the Rx pin under the control of the TDC/RDC clock and the receive data enable, RE1. RE1 controls loading of eight serial bits, henceforth referred to as the voice data word. Each MSI, these words are transferred out of the receive register to the modulation buffer for subsequent modulation onto the line. The modulation buffer takes the receive voice data word and the two signaling data input bits on SI1 and SI2 loaded on the MSI transition and formats the 10 bits into a specific order. This data field is then transmitted in a 256 kHz modified DPSK burst onto the line to the remote slave UDLT.

Upon demodulating the return burst from the slave, the decoded data is transferred to the demodulation buffer and the signaling bits are stripped ready to be output on SO1 and SO2 at the next MSI. The voice data word is loaded into the transmit register as described in the TE1 pin description for outputting via the Tx pin at the TDC/RDC data clock rate under the control of TE1. VD is output on the rising edge of MSI. Timing diagrams for the master are shown in Figure 10.

SLAVE OPERATION

In the slave, the synchronizing event is the detection of an incoming line transmission from the master as indicated by the completion of demodulation. When an incoming burst from the master is demodulated, several events occur. As in the master, data is transferred from the demodulator to the demodulation buffer and the signaling bits are stripped for outputting at SO1 and SO2. Data in the receive register is transferred to the modulation buffer. TE1 goes high loading in data at SI1 and SI2, which will be used in the transmission burst to the master along with the data in the transmit data buffer, and outputting SO1, SO2, and VD. Modulation of the burst begins four 256 kHz periods after the completion of demodulation.

While TE1 is high, voice data is output on Tx to the telset codec–filter on the rising edges of the data clock output on the CLK pin. On the ninth rising edge of CLK, TE1 goes low, RE1 goes high, and voice data from the codec–filter is input to the receiver register from the Rx pin on the next eight falling edges of CLK. RE1 is TE1 inverted and is provided to facilitate interface to the codec–filter.

The CLK pin 128 kHz output is formed by dividing down the 4.096 MHz crystal frequency by 32. Slippage between the frame rate of the master (as represented by the completion of demodulation of an incoming transmission from the master) and the crystal frequency is absorbed by holding the 16th low period of CLK until the next completion of demodulation. This is shown in the slave UDLT timing diagram of Figure 11.

POWER–DOWN OPERATION

In the master when $\overline{PD}$ is low, the UDLT stops modulating and only that circuitry necessary to demodulate the incoming bursts and output the signaling and VD data bits is active. In this mode, if the UDLT receives a burst from the slave, the SO1, SO2, and VD pins will change state upon completion of the demodulation instead of the the rising edge of MSI. The state of these pins will not change until either three rising MSI edges have occurred without the reception of a burst from the slave or until another burst is demodulated, whichever occurs first.

When $\overline{PD}$ is brought high, the master UDLT will wait either three rising MSI edges or until the MSI rising edge following the demodulation of an incoming burst before transmitting to the slave. The data for the first transmission to the slave after power–up is loaded into the UDLT during the RE1 period prior to the burst in the case of voice, and on the present rising edge of MSI for signaling data.

In the slave, $\overline{PD}$ is a bidirectional pin with weak output drivers such that it can be overdriven externally. When held low, the UDLT slave is powered–down and only that circuitry necessary for demodulation, TE1/RE1/CLK generation upon demodulation, and the outputting of voice and signaling bits is active. When held high, the UDLT slave is powered–up and transmits normally in response to transmissions from the master. If no bursts have been received from the master within 250 µs after power–up (derived from the internal oscillator frequency), the UDLT generates an internal 125 µs free–running clock from the internal oscillator. The slave UDLT then bursts a transmission to the master UDLT every other 125 µs clock period using data loaded into the Rx pin during the last RE1 period and SI1, SI2 data loaded in on the internal 125 µs clock edge. The weak output drivers will try to force $\overline{PD}$ high when a transmission from the master is demodulated and will try to force it low if 250 µs have passed without a transmission from the master. This allows the slave UDLT to self power–up and down in demand power–loop systems.

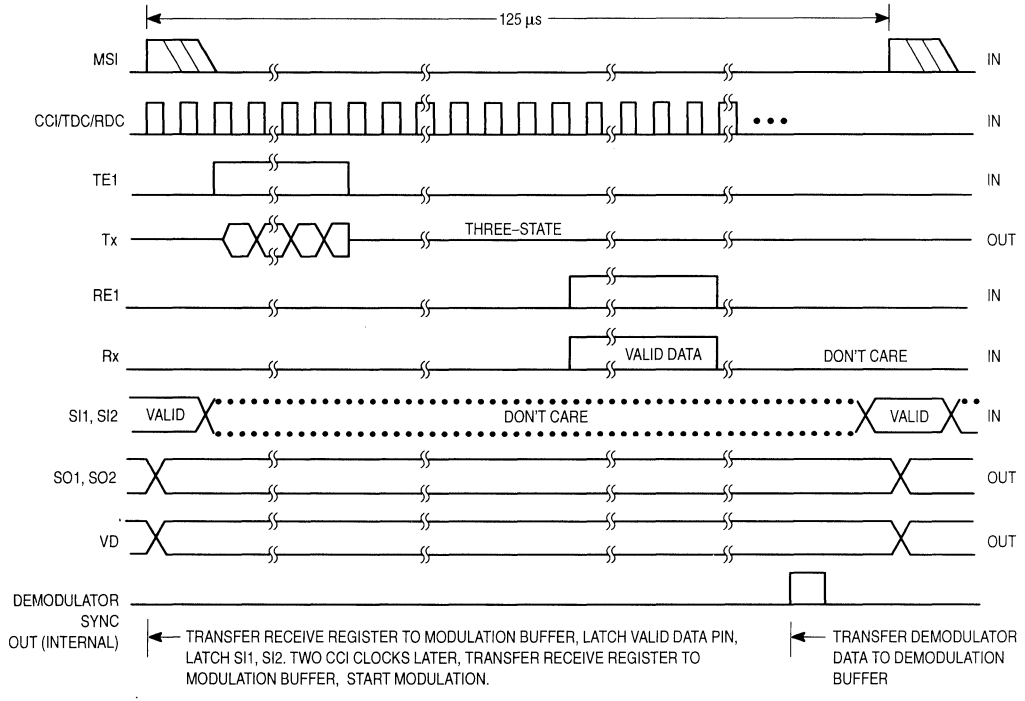
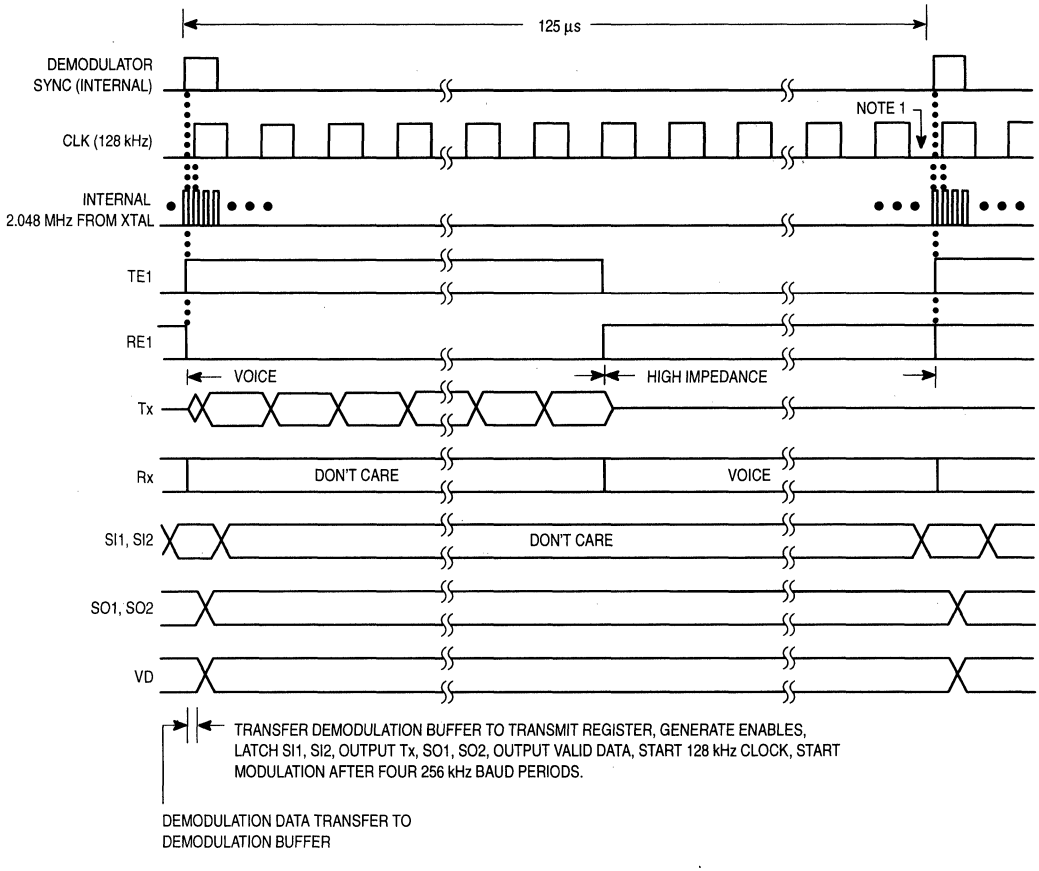


Figure 10. Master UDLT Timing



NOTE: 1. Slip between master and slave is taken up in this period.

Figure 11. Slave UDLT Timing

Both the Differential–Phase Shift Keying and the Modified Differential–Phase–Shift Keying waveforms are shown in Figures 12 thru 14. The DPSK encodes data as phase reversals of a 256 kHz carrier. A 0 is indicated by a 180° phase shift between bit boundaries, while the signal continues in phase to indicate a 1. This method needs no additional bits to indicate the start of the burst.

The modified DPSK waveform actually used in the transceivers is a slightly modified form of DPSK, as shown in Figure 12. The phase–reversal cusps of the DPSK waveform have been replaced by a 128 kHz half–cycle to lower the spectral content of the waveform, which, save for some key differences, appears quite similar to frequency shift keying. The burst always begins and ends with a half–cycle of 256 kHz, which helps locate bit boundaries.

The bit pattern shown in Figure 13a shows a stable waveform due to the even number of phase changes or zeros. The waveform shown in Figure 13b shows random data patterns being modulated.

Figure 14 shows the "ping–pong" signals on 3000 feet of 26 AWG twisted–pair wire as viewed at LI of the master UDLT and the slave UDLT.

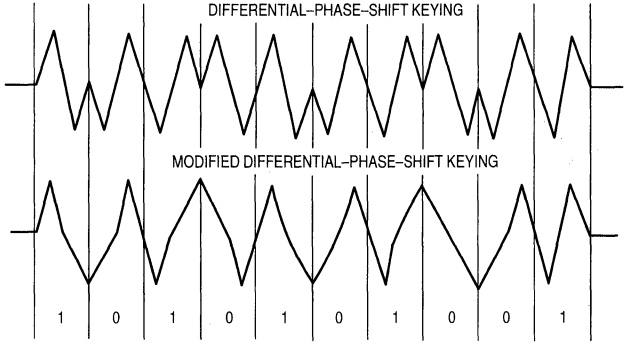
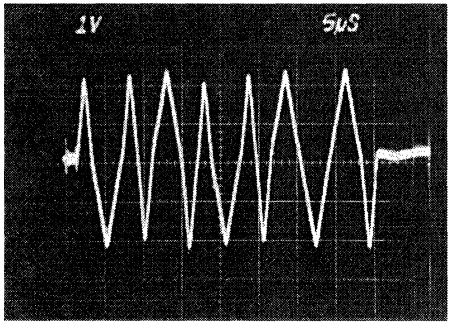
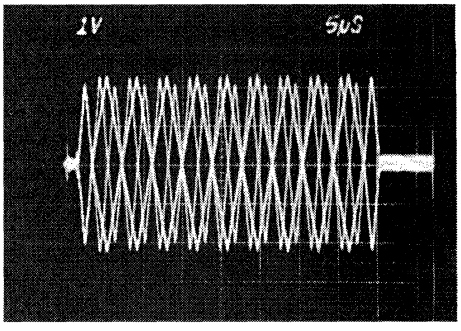


Figure 12. Modified Differential Phase Shift Keying



13a. Bit Pattern — 1010101000



13b. Bit Pattern — Random

Figure 13. Typical Signal Waveforms at Demodulator

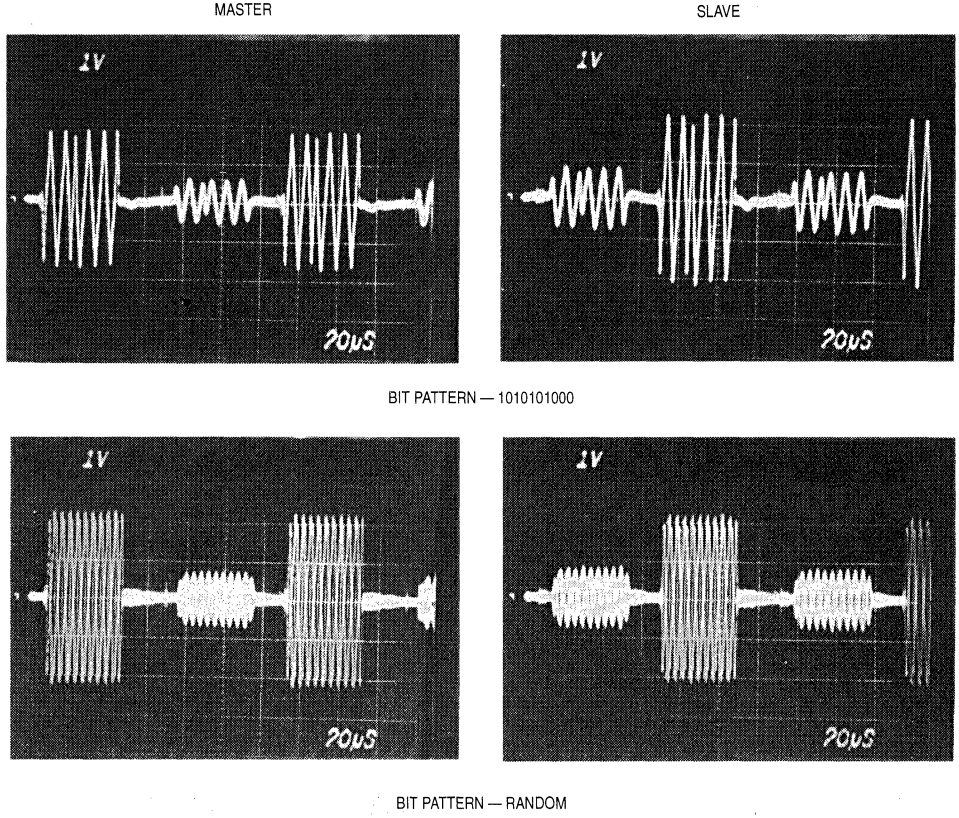


Figure 14. Typical Signal Waveforms at Demodulator

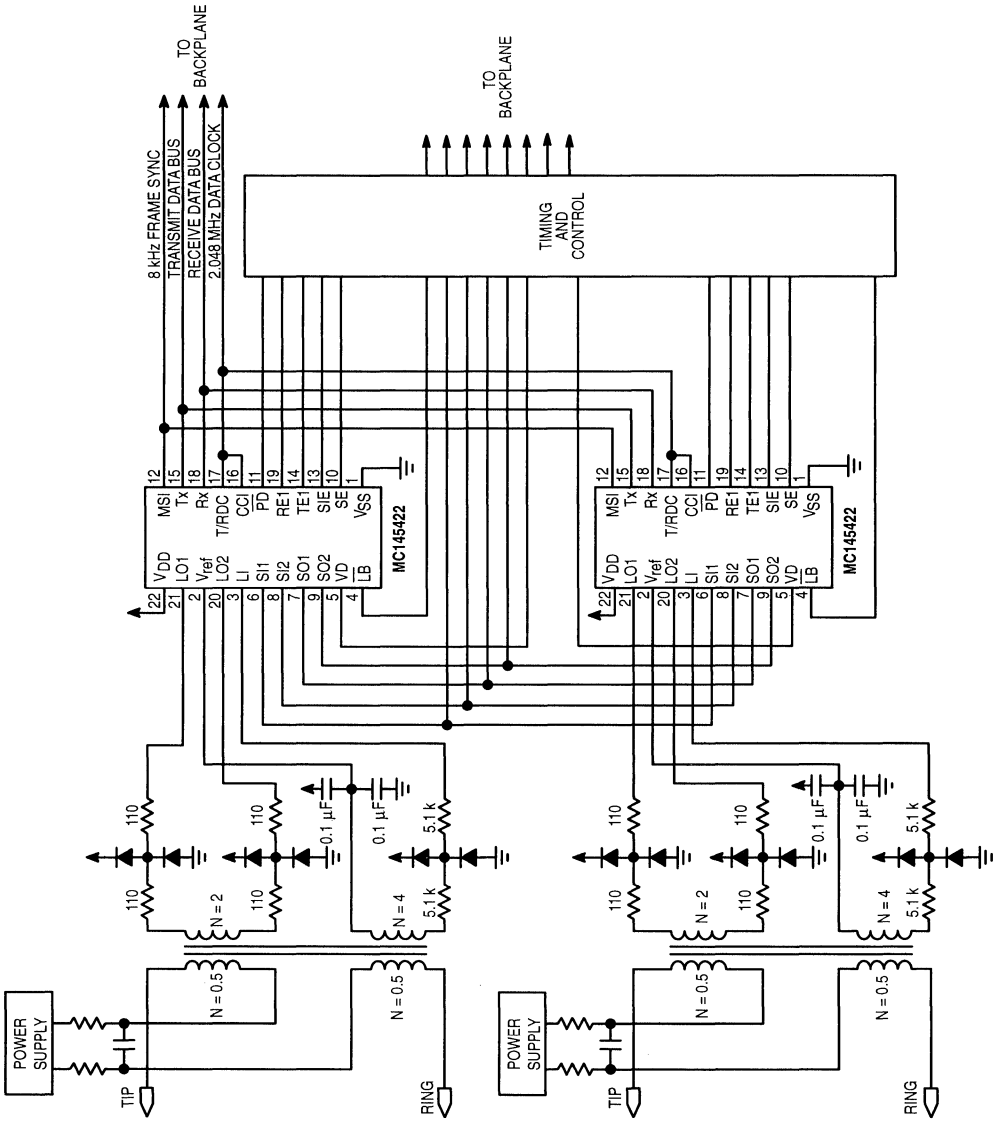


Figure 15. Typical Multichannel Digital Line Card

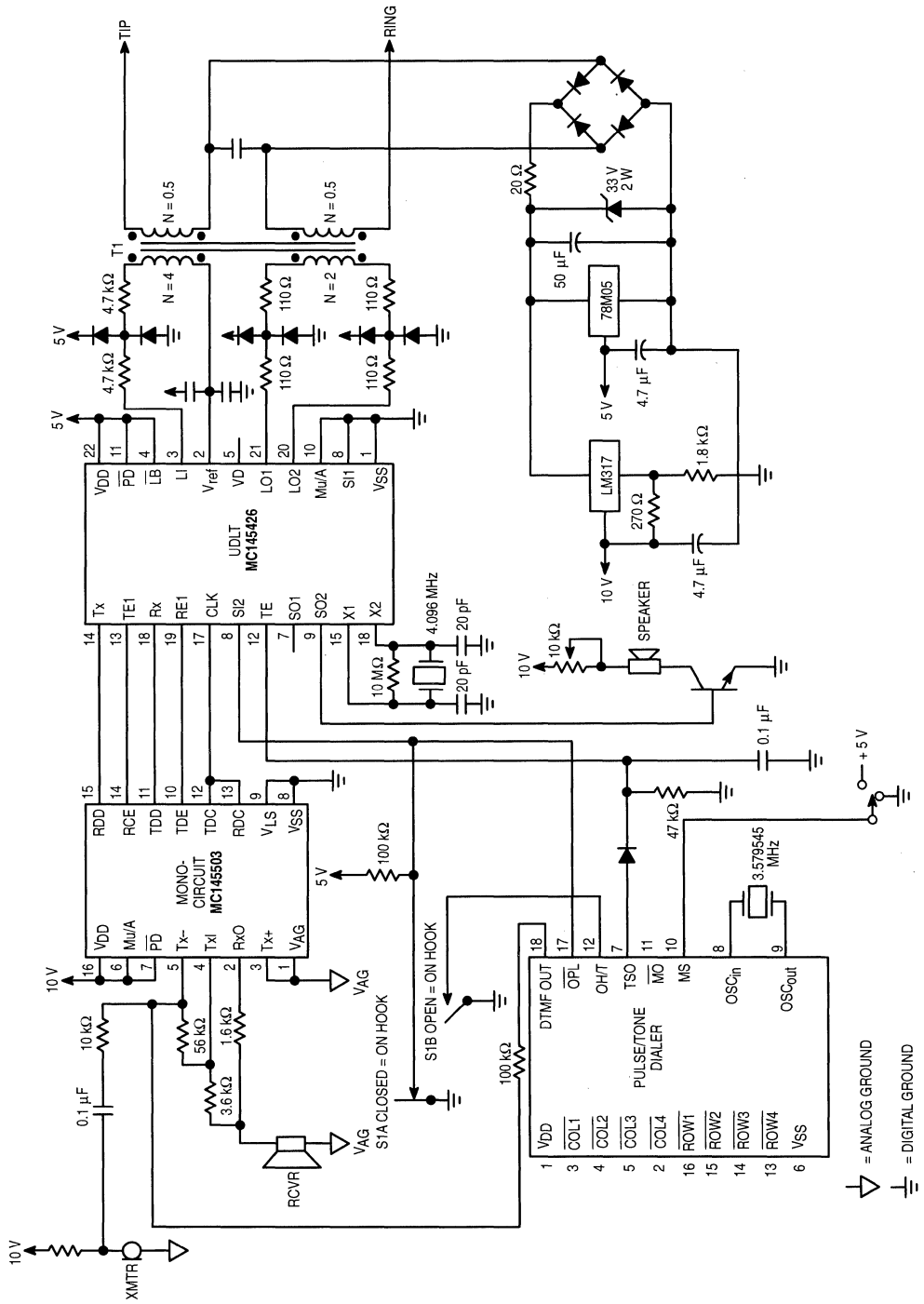


Figure 16. Basic Digital Telset

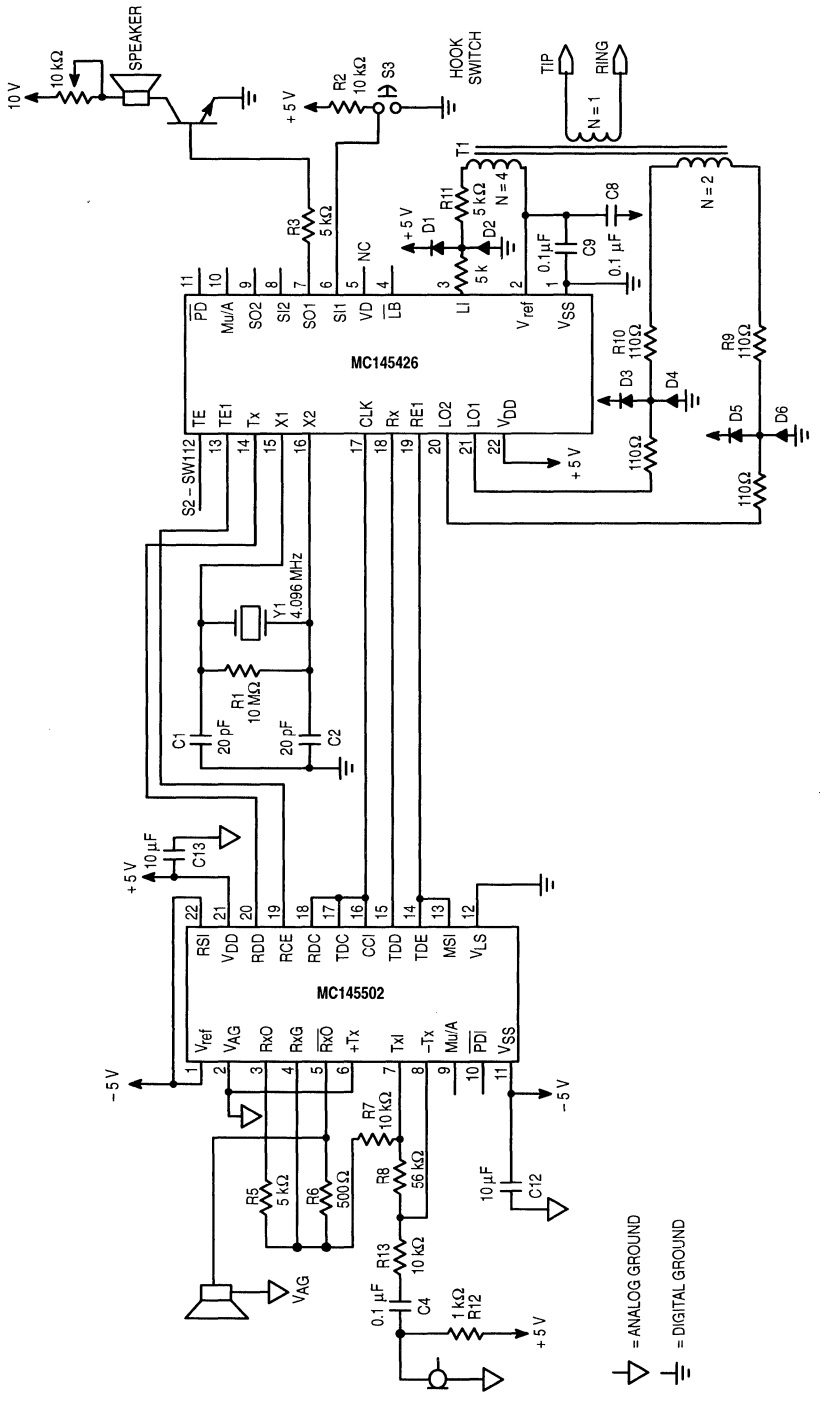


Figure 17. Full–Featured Digital Telset

MC145436A

Advance Information

Low-Power Dual Tone Multiple Frequency Receiver

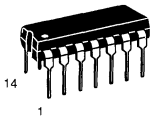
2

The MC145436A is a low–power and improved input sensitivity version of the MC14LC5436.

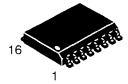
The MC145436A is a silicon gate CMOS LSI device containing the filter and decoder for detection of a pair of tones conforming to the DTMF standard with outputs in hexadecimal. Switched capacitor filter technology is used together with digital circuitry for the timing control and output circuits. The MC145436A provides excellent power line noise and dial tone rejection and is suitable for applications in central office equipment, PABX, and keyphone systems, remote control equipment and consumer telephony products.

The MC145436A offers the following performance features:

- Single + 5 V Power Supply
- Detects All 16 Standard Digits
- Uses Inexpensive 3.58 MHz Crystal
- Provides Guard Time Controls to Improve Speech Immunity
- Output in 4–Bit Hexadecimal Code
- Built–In 60 Hz and Dial Tone Rejection
- Pin Compatible with SSI–204, MC145436, and MC14LC5436
- Functional and Applicational Compatible with MC145436 and MC14LC5436



P SUFFIX
PLASTIC DIP
CASE 646



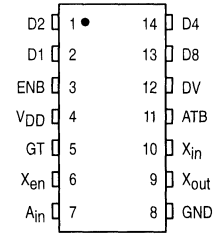
DW SUFFIX
SOG PACKAGE
CASE 751G

ORDERING INFORMATION

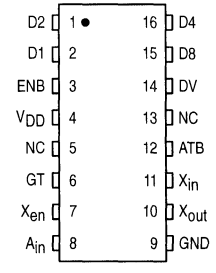
MC145436AP	Plastic DIP
MC145436ADW	SOG Package

PIN ASSIGNMENTS

PDIP



SOG

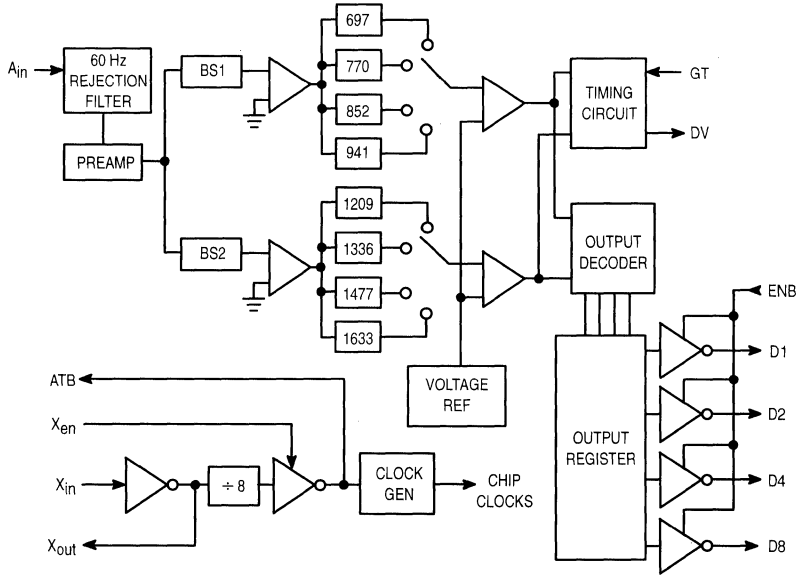


NC = NO CONNECTION

This document contains information on a new product. Specifications and information herein are subject to change without notice.

REV 0
7/95

BLOCK DIAGRAM



MAXIMUM RATINGS (Voltages Referenced to GND Unless Otherwise Noted)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	– 0.5 to + 6.0	V
Input Voltage, Any Pin Except A_{in}	V_{in}	– 0.5 to V_{DD} + 0.5	V
Input Voltage, A_{in}	V_{in}	V_{DD} – 10 to V_{DD} + 0.5	V
DC Current Drain per Pin	I	± 10	mA
Power Dissipation	P_D	100	mW
Operating Temperature Range	T_A	– 40 to + 85	°C
Storage Temperature Range	T_{stg}	– 65 to + 150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than the maximum rated voltages to this high impedance circuit.

For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$. Reliability of operation is enhanced if unused inputs are tied to and appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

2

ELECTRICAL CHARACTERISTICS

(All Polarities Referenced to V_{SS} = 0 V, V_{DD} = 5.0 V ± 10%, T_A = – 40 to + 85°C, Unless Otherwise Noted)

Parameter		Symbol	Min	Typ	Max	Unit
DC Supply Voltage		V_{DD}	4.5	5	5.5	V
Supply Current (f_{CLK} = 3.58 MHz)		I_{DD}	—	5	8	mA
Input Current	GT ENB, X_{in}, X_{en}	I_{in}	— —	— —	450 ± 1	µA
Input Voltage Low	ENB, GT, X_{en}	V_{IL}	—	—	1.5	V
Input Voltage High	ENB, GT, X_{en}	V_{IH}	3.5	—	—	V
I_{out} Data and DV Pins: V_{out} = 4.5 V (Source)		I_{OH}	800	—	—	µA
I_{out} Data and DV Pins: V_{out} = 0.4 V (Sink)		I_{OL}	1.0	—	—	mA
Input Impedance	A_{in}	R_{in}	90	100	—	kΩ
Fanout	ATB	F_{out}	—	—	10	
Input Capacitance	X_{en}, ENB	C_{in}	—	6	—	pF

ANALOG CHARACTERISTICS (V_{DD} = 5.0 V ± 10%, T_A = – 40 to + 85°C, Unless Otherwise Noted)

Parameter	Min	Typ	Max	Unit
Signal Level for Detection (A_{in})	– 35	—	– 2	dBm
Twist = High Tone/Low Tone	– 10	—	10	dB
Frequency Detect Bandwidth	± (1.5 + 2 Hz)	± 2.5	± 3.5	% f_O
60 Hz Tolerance	—	—	0.8	Vrms
Dial Tone Tolerance (Note 1) (Dial Tone 330 + 440)	—	—	0	dB
Noise Tolerance (Notes 1 and 2)	—	—	– 12	dB
Power Supply Noise (Wide Band)	—	—	10	mV p–p
Talk Off (Mitel Tape #CM7290)	—	2	—	Hits

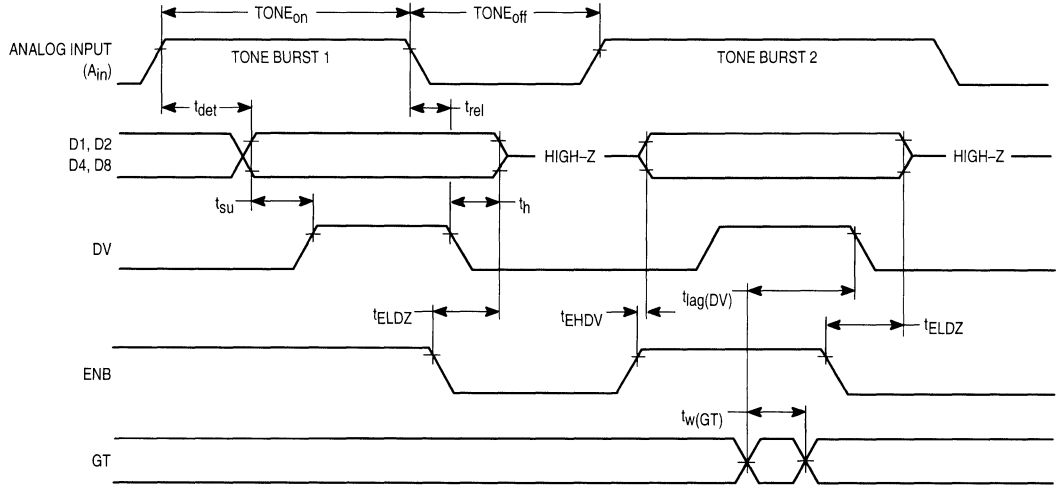
NOTES:
1. Referenced to lower amplitude tone.
2. Bandwidth limited (0 to 3.4 kHz) Gaussian Noise.

AC CHARACTERISTICS (V_{DD} = 5.0 V ± 10%, T_A = – 40 to + 85°C)

Characteristic		Symbol	Min	Typ	Max	Unit
Tone On Time	For Detection For Rejection	$TONE_{on}$	40 —	— —	— 20	ms
Pause Time	For Detection For Rejection	$TONE_{off}$	40 —	— —	— 20	ms
Detect Time	GT = 0 GT = 1	t_{det}	22 32	— —	40 50	ms
Release Time	GT = 0 GT = 1	t_{rel}	28 18	— —	40 30	ms
Data Setup Time		t_{su}	7	—	—	µs
Data Hold Time		t_h	4.2	4.6	5	ms
Pulse Width	GT	$t_{w(GT)}$	18	—	—	µs
DV Reset Lag Time		$t_{lag(DV)}$	—	—	5	ms
ENB High to Output DV*		t_{EHDV}	—	120	500	ns
ENB Low to Output High–Z*		t_{ELDZ}	—	110	300	ns

* Data out: C_L = 35 pF || R_L = 500 Ω.

TIMING DIAGRAM



PIN DESCRIPTIONS

V_{DD}
Positive Power Supply (PDIP, SOG — Pin 4)

The digital supply pin, which is connected to the positive side of the power supply.

V_{SS}
Ground (PDIP — Pin 8, SOG — Pin 9)

Ground return pin is typically connected to the system ground.

D1, D2, D4, D8
Data Output (PDIP — Pins 2, 1, 14, 13; SOG — Pins 2, 1, 16, 15)

These digital outputs provide the hexadecimal codes corresponding to the detected digit. The digital outputs become valid after a tone pair has been detected and are cleared when a valid pause is timed. See Table 1 for hexadecimal codes.These output pins are high impedance when the enable pin is at logic 0.

ENB
Enable (PDIP, SOG — Pin 3)

Outputs D1, D2, D4, D8 are enabled when ENB is at a logic 1, and high impedance (disabled) when ENB is at a logic 0.

GT
Guard Time (PDIP — Pin 5, SOG — Pin 6)

The guard time control input provides two sets of detected time and release time, both within the allowed ranges of tone on and tone off (see Figure 1). A longer tone detect time rejects signals too short to be considered valid. With GT = 1, talk off performance is improved, since it reduces the probability that tones simulated by speech will maintain signal conditions long enough to be accepted. In addition, a shorter release time reduces the probability that a pause simulated by an interrupt in speech will be detected as a valid pause. On the other hand, a shorter tone detect time with a long release time would be appropriate for an extremely noisy environment where fast acquisition time and immunity to dropouts would be required. In general, the tone signal time generated by a telephone is 100 ms, nominal, followed by a pause of about 100 ms. A high–to–low or low–to–high transition on the GT pin resets the internal logic and the MC145436A is immediately ready to accept a new tone input.

Table 1. Hexadecimal Codes

Digit	Output Code			
	D8	D4	D2	D1
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
0	1	0	1	0
*	1	0	1	1
#	1	1	0	0
A	1	1	0	1
B	1	1	1	0
C	1	1	1	1
D	0	0	0	0

X_{en}
Oscillator Enable (PDIP — Pin 6, SOG — Pin 7)

A logic 1 on X_{en} enables the on–chip crystal oscillator. When using alternate time base from the ATB pin, X_{en} should be tied to V_{SS}.

A_{in}
Analog Input (PDIP — Pin 7, SOG — Pin 8)

This pin accepts the analog input and is internally biased so that the input signal may be ac coupled. The input may be dc coupled so long as it does not exceed the positive supply (see Figure 2).

X_{in}/X_{out}
Oscillator In and Oscillator Out (PDIP — Pins 10, 9; SOG — Pins 11, 10)

These pins connect to an internal crystal oscillator. In operation, a parallel resonant crystal is connected from X_{in} to X_{out}, as well as a 1 MΩ resistor in parallel with the crystal. When using the alternate clock source from ATB, X_{in} should be tied to V_{DD}.

ATB
Alternate Time Base (PDIP — Pin 11, SOG — Pin 12)

This pin serves as a frequency reference when more than one MC145436A is used, so that only one crystal is required for multiple MC145436As. When doing so, all ATB pins should be tied together as shown in Figure 3. When only one MC145436A is used, this pin should be left unconnected. The output frequency of ATB is 447.4 kHz.

DV
Data Valid (PDIP — Pin 12, SOG — Pin 14)

DV signals a detection by going high after a valid tone pair is sensed and decoded at output pins D1, D2, D4, D8. DV remains high until a loss of the current DTMF signal occurs or until a transition in GT occurs.

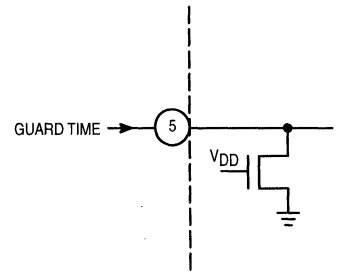


Figure 1. Guard Time

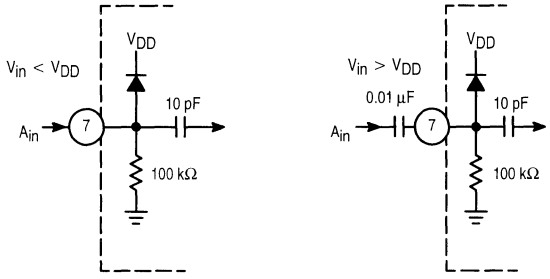


Figure 2. Analog Input (Operational Information Based on PDIP Package)

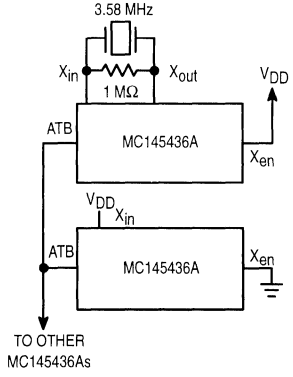


Figure 3. Multiple MC145436As

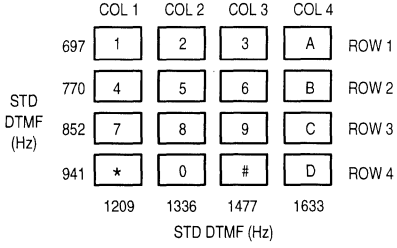


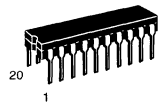
Figure 4. 4 × 4 Keyboard Matrix

MC145442
MC145443

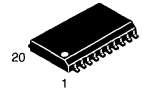
Single-Chip 300-Baud Modem

The MC145442 and MC145443 silicon–gate CMOS single–chip low–speed modems contain a complete frequency shift keying (FSK) modulator, demodulator, and filter. These devices are with CCITT V.21 (MC145442) and Bell 103 (MC145443) specifications. Both devices provide full–duplex or half–duplex 300–baud data communication over a pair of telephone lines. They also include a carrier detect circuit for the demodulator section and a duplexer circuit for direct operation on a telephone line through a simple transformer.

- MC145442 Compatible with CCITT V.21
- MC145443 Compatible with Bell 103
- Low–Band and High–Band Band–Pass Filters On–Chip
- Simplex, Half–Duplex, and Full–Duplex Operation
- Originate and Answer Mode
- Analog Loopback Configuration for Self Test
- Hybrid Network Function On–Chip
- Carrier Detect Circuit On–Chip
- Adjustable Transmit Level and $\overline{CD}$ Delay Timing
- On–Chip Crystal Oscillator (3.579 MHz)
- Single + 5 V Power Supply Operation
- Internal Mid–Supply Generator
- Power–Down Mode
- Pin Compatible with MM74HC943
- Capable of Driving – 9 dBm into a 600 Ω Load



P SUFFIX
PLASTIC DIP
CASE 738

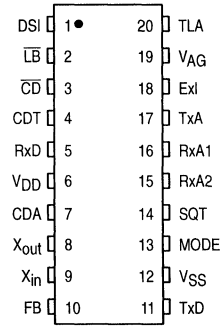


DW SUFFIX
SOG PACKAGE
CASE 751D

ORDERING INFORMATION

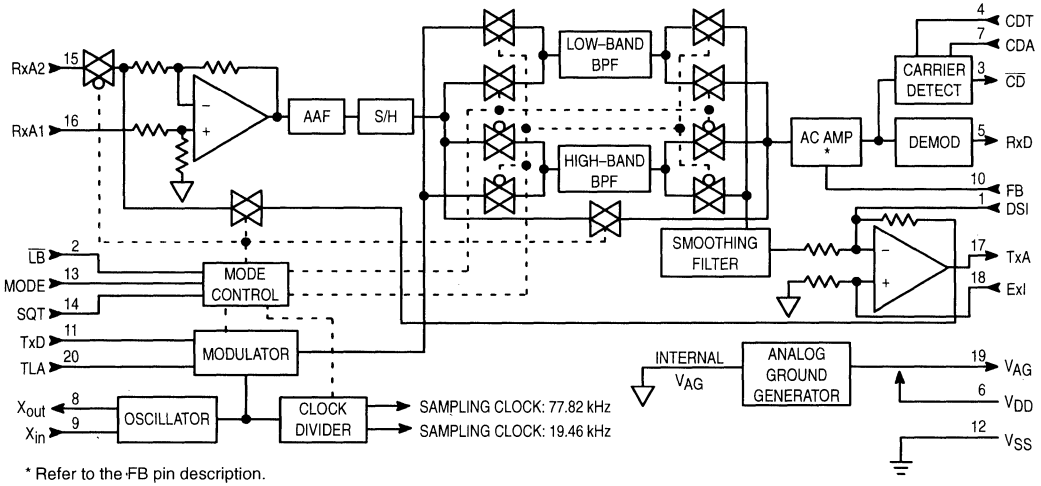
MC145442P	Plastic DIP
MC145443P	Plastic DIP
MC145442DW	SOG Package
MC145443DW	SOG Package

PIN ASSIGNMENT



REV 1
8/95

BLOCK DIAGRAM



* Refer to the FB pin description.

ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to V_{SS})

Rating	Symbol	Value	Unit
Supply Voltage	V_{DD}	– 0.5 to + 7.0	V
DC Input Voltage	V_{in}	– 0.5 to V_{DD} + 0.5	V
DC Output Voltage	V_{out}	– 0.5 to V_{DD} + 0.5	V
Clamp Diode Current, per Pin	I_{IK}, I_{OK}	± 20	mA
DC Output Current, per Pin	I_{out}	± 28	mA
Power Dissipation	P_D	500	mW
Operating Temperature Range	T_A	– 40 to + 85	°C
Storage Temperature Range	T_{stg}	– 65 to + 150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$).

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{DD}	4.5	5.5	V
DC Input or Output Voltage	V_{in}, V_{out}	0	V_{DD}	V
Input Rise or Fall Time	t_r, t_f	—	500	ns
Crystal Frequency*	$f_{crystal}$	3.2	5.0	MHz

* Changing the crystal frequency from 3.579 MHz will change the output frequencies. The change in output frequency will be proportional to the change in crystal frequency.

DC ELECTRICAL CHARACTERISTICS (V_{DD} = 5.0 V ± 10%, T_A = – 40 to + 85°C)

Characteristic		Symbol	Min	Typ	Max	Unit
High–Level Input Voltage	$\overline{LB}$	V_{IH}	V_{DD} – 0.8	—	—	V
	X_{in}, TxD, Mode, SQT		3.15	—	—	
Low–Level Input Voltage	$\overline{LB}$	V_{IL}	—	—	0.8	V
	X_{in}, TxD, Mode, SQT		—	—	1.1	
High–Level Output Voltage		V_{OH}				V
I_{OH} = 20 µA	$\overline{CD}$, RxD		V_{DD} – 0.1	—	—	
I_{OH} = 2 mA	$\overline{CD}$, RxD		3.7	—	—	
I_{OH} = 20 µA	X_{out}		—	V_{DD} – 0.05	—	
Low–Level Output Voltage		V_{OL}				V
I_{OL} = 20 µA	$\overline{CD}$, RxD		—	—	0.1	
I_{OL} = 2 mA	$\overline{CD}$, RxD		—	—	0.4	
I_{OL} = 20 µA	X_{out}		—	0.05	—	
Input Current	$\overline{LB}$, TxD, Mode, SQT	I_{in}	—	—	± 1.0	µA
	RxA1, RxA2		—	10	± 12	
	X_{in}		—	—	± 10	
Quiesent Supply Current (X_{in} or $f_{crystal}$ = 3.579 MHz)		I_{DD}	—	7	10	mA
Power–Down Supply Current			—	200	300	µA
Input Capacitance	X_{in}	C_{in}	—	10	—	pF
	All Other Inputs		—	—	10	
V_{AG} Output Voltage (I_O = ± 10 µA)		V_{AG}	2.4	2.5	2.6	V
CDA Output Voltage (I_O = ± 10 µA)		V_{CDA}	1.1	1.2	1.3	V
Line Driver Feedback Resistor		R_f	10	20	30	kΩ

AC ELECTRICAL CHARACTERISTICS

(V_{DD} = 5.0 V ± 10%, T_A = – 40 to + 85°C, Crystal Frequency = 3.579 MHz ± 0.1%; See Figure 1)

Characteristic	Min	Typ	Max	Unit
TRANSMITTER				
Power Output on TxA				dBm
R_L = 1.2 kΩ, R_{TLA} = ∞	– 13	– 12	– 11	
R_L = 1.2 kΩ, R_{TLA} = 5.5 kΩ	– 10	– 9	– 8	
Second Harmonic Power R_L = 1.2 kΩ	—	– 56	—	dBm
RECEIVE FILTER AND HYBRID				
Hybrid Input Impedance RxA1, RxA2	40	50	—	kΩ
FB Output Impedance	—	16	—	kΩ
Adjacent Channel Rejection	– 48	—	—	dBm
DEMODULATOR				
Receive Carrier Amplitude	– 48	—	– 12	dBm
Dynamic Range	—	36	—	dB
Bit Jitter (S/N = 30 dB, Input = – 38 dBm, Bit Rate = 300 baud)	—	100	—	µs
Bit Bias	—	5	—	%
Carrier Detect Threshold — On to Off	—	– 44	—	dBm
(CDA = 1.2 V or CDA grounded through a 0.1 µF capacitor) — Off to On	—	– 47	—	

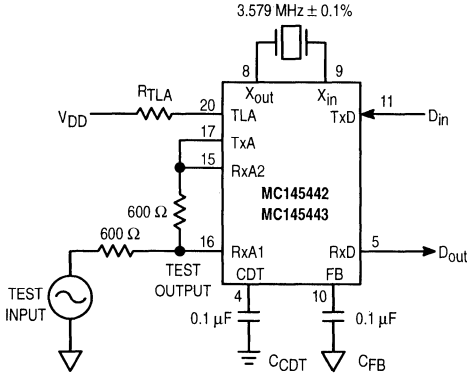


Figure 1. AC Characteristics Evaluation Circuit

PIN DESCRIPTIONS

V_{DD}
Positive Power Supply (Pin 6)

This pin is normally tied to 5.0 V.

V_{SS}
Negative Power Supply (Pin 12)

This pin is normally tied to 0 V.

V_{AG}
Analog Ground (Pin 19)

Analog ground is internally biased to $(V_{DD} - V_{SS})/2$. This pin must be decoupled by a capacitor from V_{AG} to V_{SS} and a capacitor from V_{AG} to V_{DD}. Analog ground is the common bias line used in the switched capacitor filters, limiter, and slicer in the demodulation circuitry.

TLA
Transmit Level Adjust (Pin 20)

This pin is used to adjust the transmit level. Transmit level adjustment range is typically from – 12 dBm to – 9 dBm. (See Applications Information.)

TxD
Transmit Data (Pin 11)

Binary information is input to the transmit data pin. Data entered for transmission is modulated using FSK techniques. A logic high input level represents a mark and a logic low represents a space (see Table 1).

TxA
Transmit Carrier (Pin 17)

This is the output of the line driver amplifier. The transmit carrier is the digitally synthesized sine wave output of the modulator derived from a crystal oscillator reference. When a 3.579 MHz crystal is used the frequency outputs shown in Table 1 apply. (See ***Applications Information***.)

Table 1. Bell 103 and CCITT V.21 Frequency Characteristics

Data	Originate Mode		Answer Mode	
	Transmit	Receive	Transmit	Receive
Bell 103 (MC145443)				
Space	1070 Hz	2025 Hz	2025 Hz	1070 Hz
Mark	1270 Hz	2225 Hz	2225 Hz	1270 Hz
CCITT V.21 (MC145442)				
Space	1180 Hz	1850 Hz	1850 Hz	1180 Hz
Mark	980 Hz	1650 Hz	1850 Hz	980 Hz

NOTE: Actual frequencies may be ± 5 Hz assuming 3.579545 MHz crystal is used.

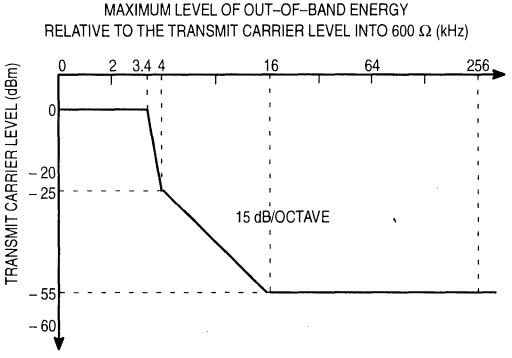


Figure 2. Out–of–Band Energy

EXI
External Input (Pin 18)

The external input is the non–inverting input to the line driver. It is provided to combine an auxiliary audio signal or speech signal to the phone line using the line driver. This pin should be connected to V_{AG} if not used. The average level must be the same as V_{AG} to maintain proper operation. (See ***Applications Information***.)

DSI
Driver Summing Input (Pin 1)

The driver summing input may be used to connect an external signal, such as a DTMF dialer, to the phone line. A series resistor, R_{DSI}, is needed to define the voltage gain A_V (see ***Applications Information*** and Figure 6). When applying a signal to do DSI pin, the modulator should be squelched by bringing SQT (Pin 14) to a logic high level. The voltage gain, A_V, is calculated by the formula $A_V = -R_f/R_{DSI}$ (where $R_f \approx 20$ kΩ). For example, a 20 kΩ resistor for R_{DSI} will provide unity gain ($A_V = -20$ kΩ/20 kΩ $= -1$). This pin **must** be left **open** if not used.

RxD
Receive Data (Pin 6)

The receive data output pin presents the digital binary data resulting from the demodulation of the receive carrier. If no carrier is present, $\overline{CD}$ high, the receive data output (RxD) is clamped high.

RxA2, RxA1
Receive Carrier (Pins 15, 16)

The receive carrier is the FSK input to the demodulator through the receive band–pass filter. RxA1 is the non–inverting input and RxA2 is the inverting input of the receive hybrid (duplexer) operational amplifier.

$\overline{LB}$
Analog Loopback (Pin 2)

When a high level is applied to this pin (SQT must be low), the analog loopback test is enabled. The analog loopback test connects the TxA pin to the RxA2 pin and the RxA1 to analog ground. In loopback, the demodulator frequencies are switched to the modulation frequencies for the selected mode. (See Tables 1 and 2 and Figures 4c and 4d.)

When $\overline{LB}$ is connected to analog ground (V_{AG}), the modulator generates an echo cancellation tone of 2100 Hz for MC145442 CCITT V.21 and 2225 Hz for MC145443 Bell 103 systems. For normal operation, this pin should be at a logic low level (V_{SS}).

The power–down mode is enabled when both $\overline{LB}$ and SQT are connected to a logic high level (see Table 2).

Table 2. Functional Table

MODE Pin 13	SQT Pin 14	$\overline{LB}$ Pin 2	Operating Mode
1	0	0	Originate Mode
0	0	0	Answer Mode
X	0	V_{AG} (V_{DD}/2)	Echo Tone
X	0	1	Analog Loopback
X	1	0	Squelch Mode
X	1	V_{AG} (V_{DD}/2)	Squelch Mode
X	1	1	Power Down

MODE
Mode (Pin 13)

This input selects the pair of transmit and frequencies used during modulation and demodulation. When a logic high level is placed on this input, originate (Bell) or channel 1 (CCITT) is selected. When a low level is placed on this input, answer (Bell) or channel 2 (CCITT) is selected. (See Tables 1 and 2 and Figure 4.)

CDT
Carrier Detect Timing (Pin 4)

A capacitor on this pin to V_{SS} sets the amount of time the carrier must be present before $\overline{CD}$ goes low (see ***Applications Information*** for the capacitor values).

$\overline{CD}$
Carrier Detect Output (Pin 3)

This output is used to indicate when a carrier has been sensed by the carrier detect circuit. This output goes to a logic low level when a valid signal above the maximum threshold level (defined by CDA, Pin 7) is maintained on the input to the hybrid circuit longer then the response (defined by CDT, Pin 4). This pin is held at the logic low level until the signal falls below the maximum threshold level for longer than the turn off time. (See ***Applications Information*** and Figure 5.)

CDA
Carrier Detect Adjust (Pin 7)

An external voltage may be applied to this pin to adjust the carrier detect threshold. The threshold hysteresis is internally fixed at 3 dB (see ***Applications Information***).

X_{out}, X_{in}
Crystal Oscillator (Pins 8, 9)

A crystal reference oscillator is formed when a 3.579 MHz crystal is connected between these two pins. X_{out} (Pin 8) is the output of the oscillator circuit, and X_{in} (Pin 9) is the input to the oscillator circuit. When using an external clock, apply the clock to the X_{in} (Pin 9) pin and leave X_{out} (Pin 8) open. An internal 10 MΩ resistor and internal capacitors, typically 10 pF on X_{in} and 16 pF on X_{out}, allow the crystal to be connected without any other external components. Printed circuit board layout should keep external stray capacitance to a minimum.

FB
Filter Bias (Pin 10)

This is the negative input to the ac amplifier. In normal operation, this pin is connected to analog ground through a 0.1 µF bypass capacitor in order to cancel the input offset voltage of the limiter. It has a nominal input impedance of 16 kΩ. (see Figure 3).

SQT
Transmit Squelch (Pin 14)

When this input pin is at a logic high level, the modulator is disabled. The line driver remains active if $\overline{LB}$ is at a logic low level (see Table 2) .

When both $\overline{LB}$ and SQT are connected to a logic high level, see Table 2, the entire chip is in a power down state and all circuitry except the crystal oscillator is disabled. Total power supply current decreases from 10 mA (Max) to 300 µA (Max).

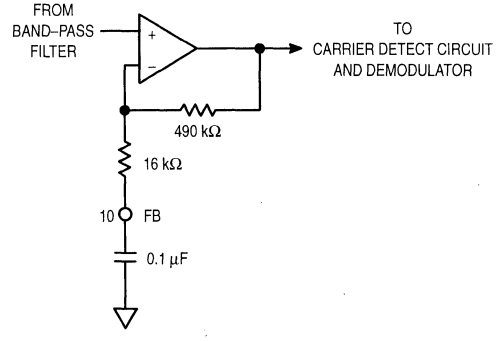


Figure 3. ac Amplifier Circuit

GENERAL DESCRIPTION

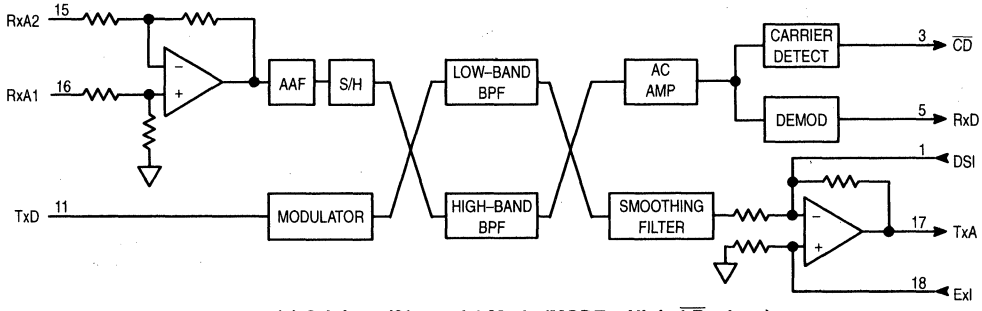
The MC145442 and MC145443 are full–duplex low–speed modems. They provide a 300–baud FSK signal for bidirectional data transmission over the telephone network. They can be operated in one of four basic configurations as determined by the state of MODE (Pin 13) and $\overline{LB}$ (Pin 2). The normal (non–loopback) and self test (loopback) modes in both answer and originate modes will be discussed.

For an originate or channel 1 mode, a logic high level is placed on MODE (Pin 13) and a logic low level is placed on $\overline{LB}$ (Pin 2). In this mode, transmit data is input on TxD, where it is converted to a FSK signal and routed through a low–band band–pass filter. The filtered output signal is then buffered by the Tx op–amp line driver, which is capable of driving – 9 dBm onto a 600 Ω line. The receive signal is connected through a hybrid duplexer circuit on Pins 15 and 16, RxA2 and RxA1. The signal then passes through the anti–aliasing filter, the sample–and–hold circuit, is switched into the high–band band–pass filter, and then switched into the ac amplifier circuit. The output of the ac amplifier circuit is routed to the demodulator circuit and demodulated. The resulting digital data is then output through RxD (Pin 5). The carrier detect circuit receives its signal from the output of the ac amplifier circuit and goes low when the incoming signal is detected (see Figure 4a).

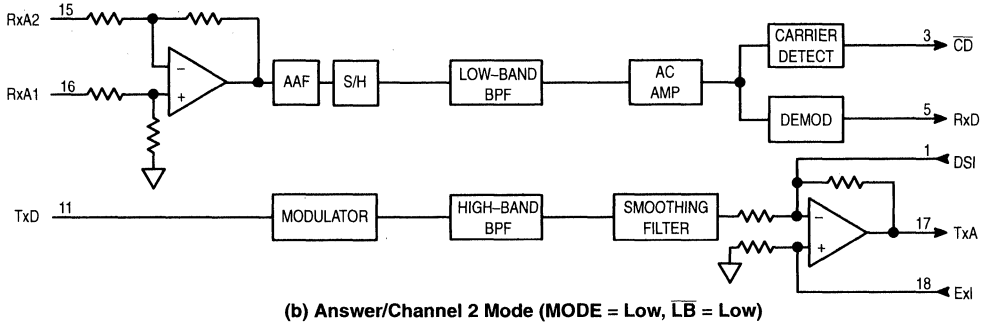
In the answer or channel 2 mode, a logic low level is placed on MODE (Pin 13) and on $\overline{LB}$ (Pin 2). In this mode, the data follows the same path except the FSK signal is routed to the high–band band–pass filter and the sample–and–hold signal is routed through the low–band band–pass filter. (See Figure 4b.)

In the analog loopback originate or channel 1 mode, a logic high level is placed on MODE (Pin 13) and on $\overline{LB}$ (Pin 2). This mode is used for a self check of the modulator, demodulator, and low–band pass–band filter circuit. The modulator side is configured exactly like the originate mode above except the line driver output (TxA, Pin 17) is switched to the negative input of the hybrid op–amp. The RxA2 input pin is open in this mode and the non–inverting input of the hybrid circuit is connected to V_{AG}. The sample–and–hold output bypasses the filter so that the demodulator receives the modulated Tx data (see Figure 4c). This test checks all internal device components except the high–band band–pass filter, which can be checked in the answer or channel 2 mode test.

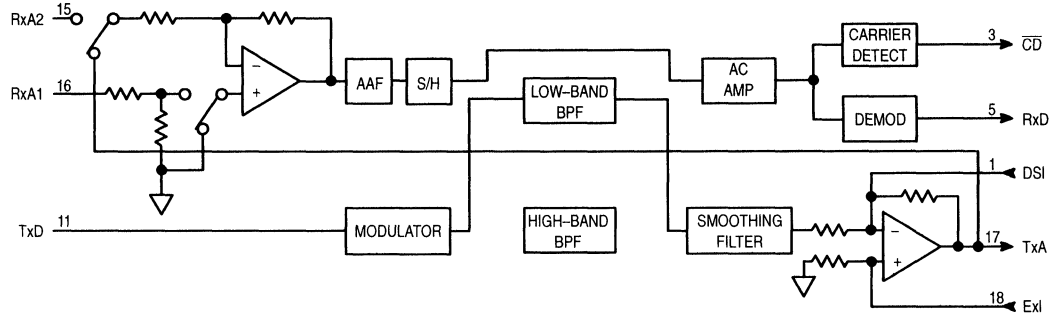
In the analog loopback or channel 2 mode, a logic low level is placed on MODE (Pin 13) and a logic high level on LB (Pin 2). This mode is used for a self check of the modulator, demodulator, and high–band pass–band filter circuit. This configuration is exactly like the originate loopback mode above, except the signal is routed through the high–band pass–band filter (see Figure 4d).



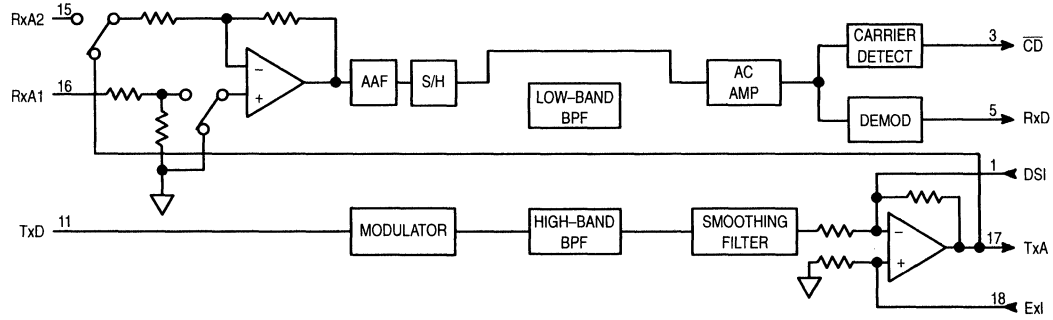
(a) Originate/Channel 1 Mode (MODE = High, $\overline{LB}$ = Low)



(b) Answer/Channel 2 Mode (MODE = Low, $\overline{LB}$ = Low)



(c) Originate/Channel 1 Mode and Analog Loopback State (MODE = High, $\overline{LB}$ = Low)



(d) Answer/Channel 2 Mode and Analog Loopback State (MODE = Low, $\overline{LB}$ = Low)

Figure 4. Basic Operating Modes

APPLICATIONS INFORMATION

CARRIER DETECT TIMING ADJUSTMENT

The value of a capacitor, C_{CDT} at CDT (Pin 4) determines how long a received modem signal must be present above the minimum threshold level before $\overline{CD}$ (Pin 3) goes low. The C_{CDT} capacitor also determines how long the $\overline{CD}$ pin stays low after the received modem signal goes below the minimum threshold. The $\overline{CD}$ pin is used to distinguish a strong modem signal from random noise. The following equations show the relationship between t_{CDL}, the time in seconds required for $\overline{CD}$ to go low; t_{CDH}, the time in seconds required for $\overline{CD}$ to go high; and C_{CDT}, the capacitor value in μF.

Valid signal to $\overline{CD}$ response time: $t_{CDL} \approx 6.4 \times C_{CDT}$

Invalid signal to $\overline{CD}$ off time: $t_{CDH} \approx 0.54 \times C_{CDT}$

Example: $t_{CDL} \approx 6.4 \times 0.1\ \mu F \approx 0.64$ seconds
$t_{CDH} \approx 0.54 \times 0.1\ \mu F \approx 0.054$ seconds

CARRIER DETECT THRESHOLD ADJUSTMENT

The carrier detect threshold is set by internal resistors to activate $\overline{CD}$ with a typical – 44 dBm (into 600 Ω) signal and deactivate $\overline{CD}$ with a typical – 47 dBm signal applied to the input of the hybrid circuit. The carrier detect threshold level can be adjusted by applying an external voltage on CDA (Pin 7). The following equations may be used to find the CDA voltage required for a given threshold voltage. (V_{on} and V_{off} are in Vrms.)

$$V_{CDA} = 244 \times V_{on}$$
$$V_{CDA} = 345 \times V_{off}$$

Example (Internally Set)

$V_{on} = 4.9$ mV ≈ – 44 dBm: $V_{CDA} = 244 \times 4.9$ mV = 1.2 V
$V_{off} = 3.5$ mV ≈ – 47 dBm: $V_{CDA} = 345 \times 3.5$ mV = 1.2 V

Example (Externally Set)

$V_{on} = 7.7$ mV ≈ – 40 dBm: $V_{CDA} = 244 \times 7.7$ mV = 1.9 V
$V_{off} = 5.4$ mV ≈ – 43 dBm: $V_{CDA} = 345 \times 5.4$ mV = 1.9 V

The CDA pin has an approximate Thevenin equivalent voltage of 1.2 V and an output impedance of 100 kΩ. When using the internal 1.2 V reference a 0.1 μF capacitor should be connected between this pin and V_{SS} (see Figure 5).

TRANSMIT LEVEL ADJUSTMENT

The power output at TxA (Pin 17) is determined by the value of resistor R_{TLA} that is connected between TLA (Pin 20) to V_{DD} (Pin 6). Table 3 shows the R_{TLA} values and the corresponding power output for a 600 Ω load. The voltage at TxA is twice the value of that at ring and tip because TxA feeds the signal through a 600 Ω resistor R_{TX} to a 600 Ω line transformer (see Figure 7). When choosing resistor R_{TLA}, keep in mind that – 9 dBm is the maximum output level allowed from a modem onto the telephone line (in the U.S.). In addition, keep in mind that maximizing the power output from the modem optimizes the signal–to–noise ratio, improving accurate data transmission.

Table 3. Transmit Level Adjust

Output Transmit Level (Typical into 600 Ω)	R_{TLA}
– 12 dBm	∞
– 11 dBm	19.8 kΩ
– 10 dBm	9.2 kΩ
– 9 dBm	5.5 kΩ

THE LINE DRIVER

The line driver is a power amplifier used for driving the telephone line. Both the inverting and noninverting input to the line driver are available for transmitting externally generated tones.

Exl (Pin 18) is the noninverting input to the line driver and gives a fixed gain of 2 (R_i = 50 kΩ). The average signal level must be the same as V_{AG} to maintain proper operation. This pin should be connected to V_{AG} if not used.

The driver summing input (DSI, Pin 1) may be used to connect an external signal, such as a DTMF dialer, to the phone line. When applying a signal to the DSI pin, the modulator should be squelched by bringing SQT (Pin 14) to a logic high level. DSI ***must*** be left ***open*** if not used.

In addition, the DSI pin is the inverting side of the line driver and allows adjustable gain with a series resistor R_{DSI} (see Figure 6). The voltage gain, A_V, is determined by the equation:

$$A_V = -\frac{R_f}{R_{DSI}}$$

where $R_f \approx 20$ kΩ.

Example: A resistor value of 20 kΩ for RDSI will provide unity gain.

$$A_V = -(20\ k\Omega / 20\ k\Omega) = -1$$

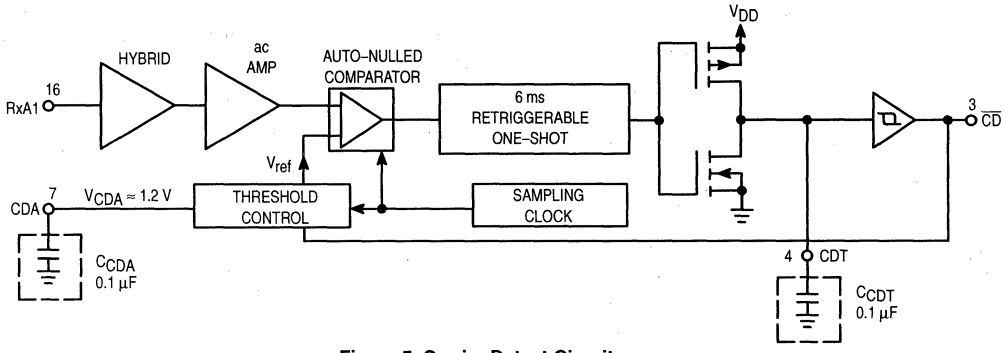


Figure 5. Carrier Detect Circuit

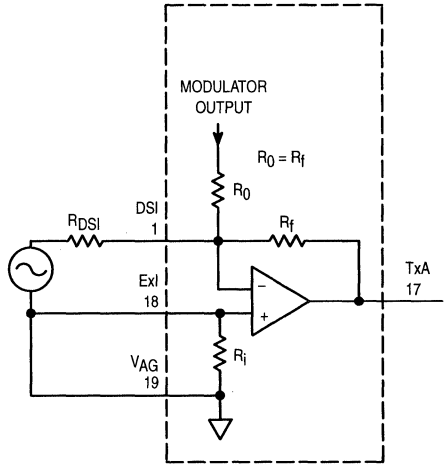


Figure 6. Line Driver Using the DSI Input

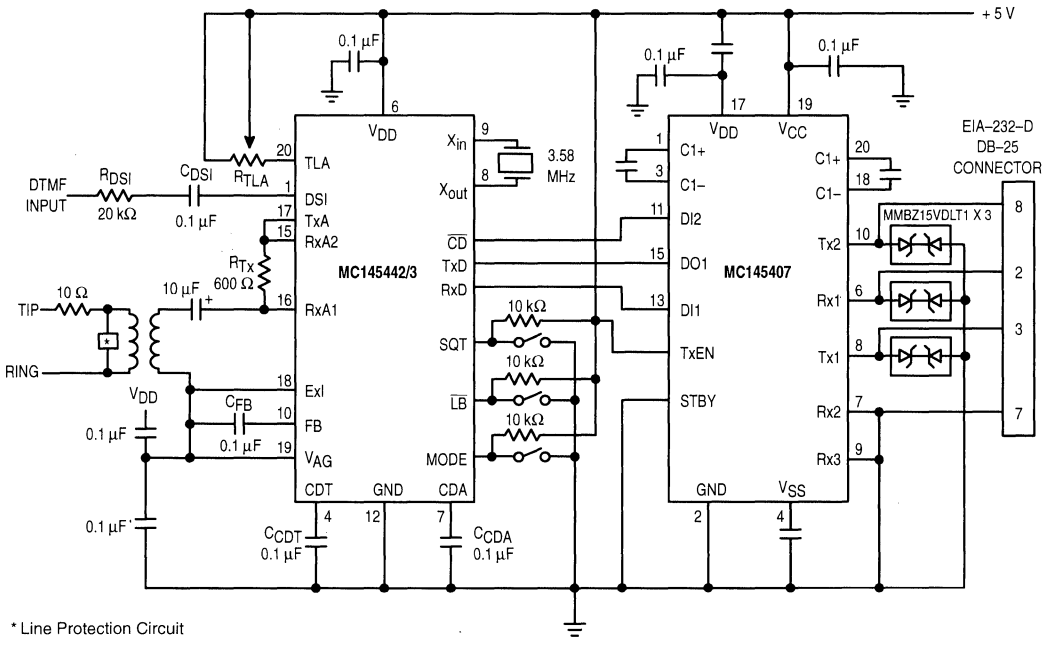


Figure 7. Typical MC145442/MC145443 Applications Circuit

MC145444

Advance Information

Single-Chip 300-Baud Modem

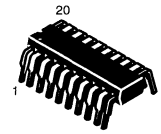
MC145444 is a silicon gate CMOS frequency shift keying (FSK) modem intended for use with telemeter systems or remote control systems over the telephone network.

This device is compatible with CCITT V.21 and contains the entire circuit that provides a full–duplex or half–duplex 300–baud data communication over a pair of telephone lines. This device also includes the DTMF generator and call progress tone detector (CPTD).

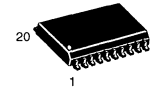
The differential line driver has the capability of driving 0 dBm into a 600 Ω load with a single + 5 V power supply.

The transmit level is controlled by the programmable attenuator in 1 dB steps. Devices functions are controlled through a 3–wire serial interface.

- Capable of Driving 0 dBm into a 600 Ω Load
- DTMF Generator On–Chip
- Imprecise Call Progress Detector On–Chip
- A Transmit Attenuator Programmable in 1 dB Steps
- 3–Wire Serial Interface
- Compatible with CCITT V.21
- 2100 Hz Answer Tone Generator On–Chip
- Analog Loopback Configuration for Self Test
- Simplex, Half–Duplex, and Full–Duplex Operation



H SUFFIX
PLASTIC DIP
CASE 804

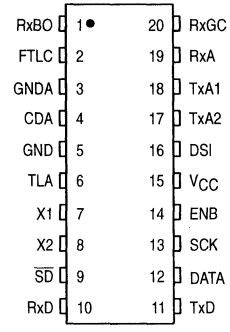


DW SUFFIX
SOG PACKAGE
CASE 751D

ORDERING INFORMATION

MC145444P	Plastic DIP
MC145444DW	SOG Package

PIN ASSIGNMENT



This document contains information on a new product. Specifications and information herein are subject to change without notice.

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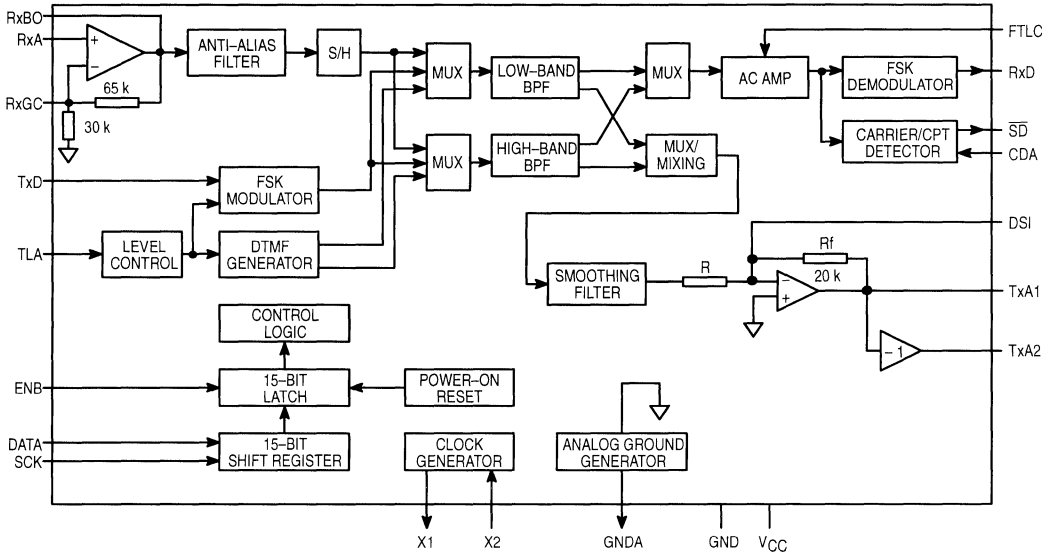
BLOCK DIAGRAM



MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{CC}	– 0.5 to + 7.0	V
DC Input Voltage	V_{in}	– 0.5 to V_{CC} + 0.5	V
DC Output Voltage	V_{out}	– 0.5 to V_{CC} + 0.5	V
Clamp Diode Current per Pin	I_{IK}, I_{OK}	± 20	mA
DC Current per Pin	I_{out}	± 25	mA
Power Dissipation	P_D	500	mW
Storage Temperature Range	T_{stg}	– 65 to + 150	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
DC Supply Voltage	V_{CC}	4.5	5	5.5	V
DC Input Voltage	V_{in}	0	—	V_{CC}	V
DC Output Voltage	V_{out}	0	—	V_{CC}	V
Input Rise Time	t_r	0	—	500	ns
Input Fall Time	t_f	0	—	500	ns
Crystal Frequency	f_{osc}	—	3.579545	—	MHz
Operating Temperature Range	T_A	– 20	25	70	°C

DC ELECTRICAL CHARACTERISTICS (V_{CC} = + 5.0 V ± 10%, T_A = – 20 to + 70°C)

Characteristic		Symbol	Conditions	Min	Typ	Max	Unit
Input Voltage	H Level	V_{IH}		3.15	—	—	V
	L Level	V_{IL}		—	—	1.1	
Output Voltage	H Level	V_{OH}	I_{OH} = 20 µA	V_{CC} – 0.1	V_{CC} – 0.01	—	V
	L Level	V_{OL}	I_{OL} = 20 µA I_{OL} = 2 mA	— —	0.01 —	0.1 0.4	
Input Current DATA, SCK, E, TxD		I_{in}	V_{in} = V_{CC} or GND	—	± 1.0	± 10.0	µA
Quiescent Supply Current		I_{CC}	FSK Mode	—	8	—	mA
Power–Down Supply Current		I_{CC}	Power–Down Mode 1	—	—	300	µA
		I_{CC}	Power–Down Mode 2	—	—	1	µA

TRANSMIT CARRIER CHARACTERISTICS (V_{CC} = + 5.0 V ± 10%, T_A = – 20 to + 70°C)

Characteristic		Symbol	Conditions	Min	Typ	Max	Unit
Carrier Frequency Channel 1	Mark "1"	f_{1M}	Crystal Frequency 3.579545 MHz	974	980	986	Hz
	Space "0"	f_{1S}		1174	1180	1186	
Carrier Frequency Channel 2	Mark "1"	f_{2M}		1644	1650	1656	
	Space "0"	f_{2S}		1844	1850	1856	
Answer Tone		f_{ans}		2094	2100	2106	
Transmit Carrier Level		V_O*	Attenuator = 0 dB RTLA = ∞	—	6	—	dBm
Second Harmonic Energy		V_{2h}*		—	– 46	—	dBm
Out–of–Band Energy		V_{OE}*		Figure 1			dBm

* $V_{TXA1} - V_{TXA2}$, R_L = 1.2 kΩ

TRANSMIT ATTENUATOR CHARACTERISTICS (V_{CC} = + 5.0 V ± 10%, T_A = – 20 to + 70°C)

Characteristic	Symbol	Conditions	Min	Typ	Max	Unit
Attenuator Range	A_{RNG}		0	—	15	dB
Attenuator Accuracy	A_{ACC}		– 0.5	—	+ 0.5	dB

RECEIVER CHARACTERISTICS (Includes Hybrid, Demodulator and Carrier Detector)
(V_{CC} = + 5.0 V ± 10%, T_A = – 20 to + 70°C)

Characteristic		Symbol	Conditions	Min	Typ	Max	Unit
Input Impedance		R_{IRX}	RxA Pin (Pin 19)	50	—	—	kΩ
Receiver Carrier Amplitude		V_{IRX}		– 48	—	– 12	dBm
Carrier Detect	OFF to ON	V_{CDON}	CDA = 1.2 V f_{in} = 1.0 kHz	—	– 44	—	dBm
Threshold	ON to OFF	V_{CDOF}		—	– 47	—	
Hysterisis ($V_{CDON} - V_{CCDOF}$)		H_{VS}		2	—	—	dB
Carrier Detect Timing	OFF to ON	T_{CDON}	CD1 = 0, CD0 = 0	—	450	—	ms
			CD1 = 0, CD0 = 1	—	15	—	
			CD1 = 0, CD1 = 1	—	15	—	
			CD1 = 1, CD0 = 1	—	80	—	
	ON to OFF	T_{CDOFF}	CD1 = 0, CD0 = 0	—	30	—	
			CD1 = 0, CD0 = 1	—	30	—	
			CD1 = 0, CD0 = 1	—	15	—	
			CD1 = 1, CD0 = 1	—	10	—	

BAND–PASS FILTER CHARACTERISTICS (RxA to FTLC) (V_{CC} = + 5.0 V ± 10%, T_A = – 20 to + 70°C)

Characteristic	Symbol	Conditions	Min	Typ	Max	Unit
FTLC Output Impedance	R_{OFT}		10	—	50	kΩ
Adjacent Channel Rejection	REJ	V_{RXA} = – 12 dBm	—	50	—	dB
Pass–Band Gain	G_{PAS}		—	10	—	dB
Group Delay		Low–Band Filter 930 – 1230 Hz	—	700	—	µs
		High–Band Filter 1600 – 1900 Hz	—	800	—	

DTMF CHARACTERISTICS (V_{CC} = + 5.0 V ± 10%, T_A = – 20 to + 70°C)

Characteristic		Symbol	Conditions	Min	Typ	Max	Unit
Tone Output Level	Low Group	V_{fl}*		—	3	—	dBm
	High Group	V_{fh}*		—	4	—	
High Group Pre Emphasis		P_E	Attenuator = 0 dB RTLA = ∞ Crystal Frequency 3.579545 MHz	0	—	3	dB
DTMF Distortion		DIST		—	5	—	%
DTMF Frequency Variation		Δf_V		– 1	—	1	%
Out–of–Band Energy		V_{OE}*		Figure 1			dB
Setup Time		t_{osc}		—	4	—	ms

* $V_{TXA1} - V_{TXA2}$, R_L = 1.2 kΩ

CPTD CHARACTERISTICS (V_{CC} = + 5.0 V ± 10%, T_A = – 20 to + 70°C)

Characteristic		Symbol	Conditions	Min	Typ	Max	Unit
Band–Pass Filter Center Frequency		f_c		—	400	—	Hz
Band–Pass Filter – 3 dB Band Width		Δ_{BW}		—	140	—	Hz
Tone Detect Level	OFF to ON	V_{TDON}	CDA = 1.2 V f_{in} = 400 Hz	—	– 44	—	dBm
	ON to OFF	V_{TDOF}		—	– 47	—	
Tone Detect Timing	OFF to ON	T_{TDON}		—	10	—	ms
	ON to OFF	T_{TDOF}		—	25	—	

DEMODULATOR CHARACTERISTICS (V_{CC} = + 5.0 V ± 10%, T_A = – 20 to + 70°C)

Characteristic	Symbol	Conditions	Min	Typ	Max	Unit
Bit Bias	ID	Input Level = – 24 dBm	—	5	—	%
Bit Error Rate	BER	Input Level = – 24 dBm CCITT Line Simulation 511 Bit Pattern S/N = 5 dB	—	0.00001	—	—

SWITCHING CHARACTERISTICS (V_{CC} = + 5.0 V ± 10%, T_A = – 20 to + 70°C)

Characteristic		Symbol	Conditions	Min	Typ	Max	Unit
Setup Times	DATA to SCK	t_{su}		50	—	—	ns
	SCK to ENB			50	—	—	ns
Hold Time	SCK to DATA	t_h		50	—	—	ns
Recovery Time	ENB to SCK	t_{rec}		50	—	—	ns
Input Rise Time		t_r		—	—	2	µs
Input Fall Time		t_f		—	—	2	µs
Input Pulse Width	ENB, SCK	t_w		50	—	—	ns

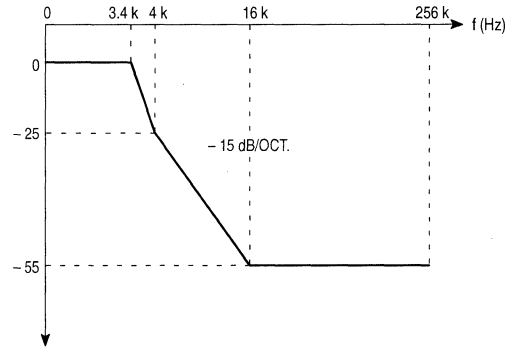


Figure 1. Out–of–Band Energy

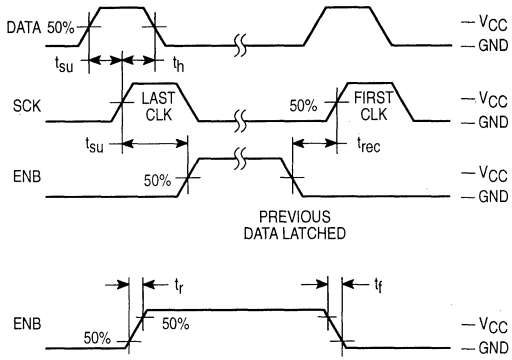


Figure 2. Switching Characteristics

PIN DESCRIPTION

V_{CC}
Positive Power Supply (Pin 15)

This pin is normally tied to the + 5.0 V. A 0.1 μF decoupling capacitor should be used.

GND
Ground Pin (Pin 5)

This pin is normally tied to 0 V.

GNDA
Analog Ground (Pin 3)

Analog ground is internally biased to $(V_{CC} - V_{SS})/2$. It should be tied to ground through a 0.1 μF and 100 μF capacitor.

X1
Crystal Oscillator Output (Pin 7)

Connecting a 3.579545 MHz ± 0.1% crystal between X1 and X2 will cause the transmit frequencies to be within ± 64 MHz of nominal. X1 is capable of driving several CMOS gates. An external clock may be applied to X2. X1 should then be left open.

X2
Crystal Oscillator Input (Pin 8)

Refer to X1.

SCK
Shift Resister Clock Input (Pin 13)

This pin is the clock input for the 15–bit shift register. Serial data is loaded into the shift register on the rising edge of this clock.

DATA
Serial Data Input (Pin 12)

This pin is the 15–bit serial data input. This data determines the mode, DTMF signal, transmit attenuation, carrier detect time, channel, and transmit squelch.

ENB
Enable Input (Pin 14)

Data is loaded into the 15–bit shift register when this pin is at a logic low. When this pin transitions from a logic high to low, the data is transferred to the internal latch on the falling edge of ENB. New data loaded into the shift register will not affect the device operation until this pin transitions from high to low. (See Figure 2.)

TxD
Transmit Data Input (Pin 11)

This pin is the transmit data input, The mark frequency is generated when this pin is at the logic high level. The space frequency is generated when the pin is at a logic low.

RxD
Receive Data Output (Pin 10)

This pin is the receive data output. A high logic level of this pin indicates that the mark carrier frequency has been received, and a low logic level indicates the space carrier frequency has been received.

$\overline{SD}$
Carrier/Call Progress Tone Detect (Pin 9)

This pin is the output from the carrier detector or call progress tone detector. This pin works as a carrier detector in the FSK mode and as the call progress tone detector in the CPTD mode. The output goes to a logic low level when the input signal reaches the minimum threshold of the detect level that is adjusted by the CDA voltage. When $\overline{SD}$ = H, the receive data output (RxD) is clamped high to avoid errors that may occur with loop noise. The $\overline{SD}$ pin is also clamped high in the other modes except during the power–down mode.

TxA1
Non–Inverting Transmit Analog Carrier Output (Pin 18)

This pin is the line driver non–inverting output of the FSK and tone transmit analog signals. A + 6 dBm (max) differential output voltage can be obtained by connecting a 1.2 kΩ load resistor between Tx1 and Tx2. Attention must be set so as not to exceed this level when an external input is added to the DSI pin. A telephone line (600 Ω) is driven through an external 600 Ω resistor. In this case, the output level becomes about half of differential output.

TxA2
Inverting Transmit Analog Carrier Output (Pin 17)

This pin is the line driver inverting output. The signal is equal in magnitude, but 180° out of phase with the TxA1 (refer to TxA1).

RxA
Receive Signal Input (Pin 19)

This pin is the receive signal input. The pin has an input impedance of 50 kΩ (min).

RxGC
Receive Gain Adjust (Pin 20)

This pin is used to adjust the receive buffer gain. To adjust the gain, the signal from the RxBO through a divider is added as a feedback. This pin may be held open when the gain adjustment is not needed.

RxBO
Receiver Buffer Output (Pin 1)

This pin is the receive buffer output.

DSI
Driver Summing Input (Pin 16)

This pin is the inverting input of the line driver. An external signal is transmitted through an external series resistor R_{DSI}. The differential gain $G_{DSI} = (V_{TXA1} - V_{TXA2})/V_{DSI}$ is determined by the following equation.

$$G_{DSI} = -2Rf / R_{DSI}, Rf \approx 20\ k\Omega$$

DSI should be left open when not used.

CDA
Carrier Detect Level/CPTD Level Control (Pin 4)

The carrier/call progress tone detect level is programmed with a CDA pin voltage.

When this pin is held open, the CDA voltage is set to 1.2 V with an internal divider. The detect level is set at – 44 dBm (typ) for off to on, and – 47 dBm (typ) for on to off. The minimum hysteresis is 2 dB. This pin has a very high input impedance so it should be connected to GND with a 0.1 μF capacitor to keep it well regulated. An external voltage may be applied to this pin to adjust the carrier detect threshold. The following equations may be used to find the CDA voltage required for a given threshold voltage.

$$V_{CDA} = 245 \times V_{on}$$
$$V_{CDA} = 347 \times V_{off}$$

FTLC
Filter Test (Pin 2)

This pin is a high–impedance filter output. It may be used to check the receive filter. This pin also may be used as a demodulator input. In normal operation, this pin is connected to the GNDA through a 0.1 μF bypass capacitor. This pin handles very small signals so care must be used with the capacitor's wiring.

TLA
Transmit Carrier Level Adjust (Pin 6)

This pin is used to adjust the transmit carrier level that is determined by the value of the resistor (RTLA) connected between this pin and GND. The maximum transmit level is obtained when this pin is connected to GND (RTLA = 0).

SERIAL INTERFACE

The following six functions are set up with the 15–bit serial data.

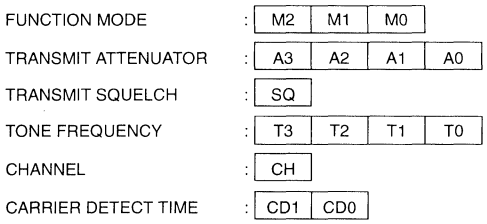


Figure 3 presents the 15–bit serial data timing, starting with the carrier detect time, CD1, followed by the channel, the tone frequency, the transmit squelch, the transmit attenuator, and the function mode. This data is loaded into the internal shift register at the rising edge of the SCK signal and latched at the falling edge of the ENB signal.

FUNCTION MODE

Modes are selected from the following 3–bit data (M2 – M0, see Table 1).

Table 1. Function Mode Truth Table

M2	M1	M0	Function Mode
0	0	0	FSK
0	0	1	Analog Loopback
0	1	0	CPTD
0	1	1	Answer Tone
1	0	0	DTMF
1	0	1	Single Tone
1	1	0	Power–Down 1
1	1	1	Power–Down 2

The following paragraphs describe each function. Table 2 presents each output status.

FSK Mode

The transmitter and the receiver work as a FSK modulator/demodulator. The $\overline{SD}$ pin output is the carrier's detect signal.

Analog Loopback Mode

TxA1 connects to the receiver internally and FSK signals are demodulated. The frequency of the receiver is set up with the same frequency as the transmitter. The $\overline{SD}$ pin output is the carrier detect signal. An IC self test is supported with this function.

CPTD Mode

The receiver detects a 400 Hz call progress tone. The detect signal comes from the $\overline{SD}$ pin. The transmitter is disabled.

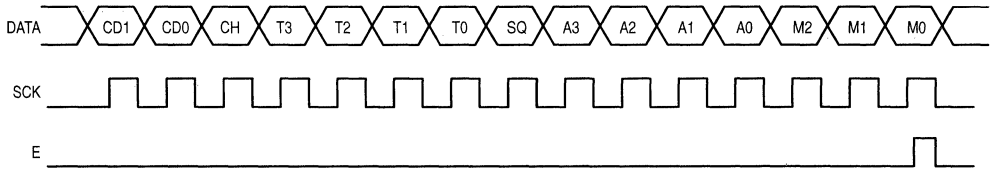


Figure 3. Serial Data Timing

2

Table 2. Output Status

Function Mode	Output		
	RxD	$\overline{SD}$	TxA1, TxA2
FSK	Received Digital Data	Carrier Detect	FSK
Analog Loopback			
CPTD	H	CPTD	$V_{CC}/2$
Answer Tone	H	H	Answer Tone
DTMF	H	H	DTMF Tone
Single Tone	H	H	Single Tone
Power–Down 1, 2	High–Z	High–Z	High–Z

Answer Tone Mode

The transmitter works as 2100 Hz answer tone generator. The receiver is disabled.

DTMF Mode

The transmitter works as a DTMF tone generator. The receiver is disabled.

Single Tone Mode

The transmitter output is one of the DTMF eight frequencies. The receiver is disabled.

Power–Down Mode 1

Internal circuits except the oscillator are disabled, and all outputs except the X1 pin go to the high impedance state. The supply current decreases to 300 μA (max).

Power–Down Mode 2

All circuits including the oscillator stop working and all outputs go to the high impedance state. The supply current decreases to 1.0 μA (max).

Transmit Attenuator

Four–bit serial data (A3 – A0) sets up the analog transmit level in the FSK, answer tone, DTMF, analog loopback, and single tone mode. The range of the transmit attenuator is 0 – 15 dB in 1 dB steps. The external signal (DSI) is not affected by this attenuator.

TONE FREQUENCY

The DTMF tones or the single tone mode is selected by the 4–bit serial data (T3 – T0).

Table 3. Transmit Attenuator Truth Table

A3	A2	A1	A0	Attenuation (dB)
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	11
1	1	0	0	12
1	1	0	1	13
1	1	1	0	14
1	1	1	1	15

Table 4. Tone Frequency Truth Table

				Tone Frequency (Hz)			
				DTMF Mode			
T3	T2	T1	T0	Low Group	High Group	Keyboard Equivalent	Single Tone Mode
0	0	0	0	941	1633	D	941
0	0	0	1	697	1209	1	697
0	0	1	0	697	1336	2	697
0	0	1	1	697	1477	3	697
0	1	0	0	770	1209	4	770
0	1	0	1	770	1336	5	770
0	1	1	0	770	1477	6	770
0	1	1	1	852	1209	7	852
1	0	0	0	852	1336	8	1336
1	0	0	1	852	1477	9	1477
1	0	1	0	941	1336	0	1336
1	0	1	1	941	1209	*	1209
1	1	0	0	941	1477	#	1477
1	1	0	1	697	1633	A	1633
1	1	1	0	770	1633	B	1633
1	1	1	1	852	1633	C	1633

TRANSMIT SQUELCH

The 1–bit serial data (SQ) controls the transmit analog signal. The FSK signal, DTMF tones, single tone, and answer tone are disabled. The external signal to the DSI will be transmitted at that time. The internal line driver works at all times except during the power–down mode.

SQ	Squelch
1	Enable
0	Disable

2

CHANNEL

The transmit and receive channel is set up with a 1–bit serial data (CH) when the function mode is either in FSK or analog loopback.

When the function mode is either on the FSK or analog loopback mode, the transmit and receive channel is set up with a 1–bit serial data (CH).

CH	Channel
1	1 (Originate)
0	2 (Answer)

CARRIER DETECT TIME

The carrier detect time (see Figure 4 and Table 5) is set by 2–bit serial data (CD1, CD0). t_{on} indicates the amount of time the carrier is greater than V_{on} threshold must be present before $\overline{SD}$ goes low.

t_{off}, on the other hand, indicates the amount of delay time $\overline{SD}$ goes high after the carrier level becomes lower than V_{off} threshold.

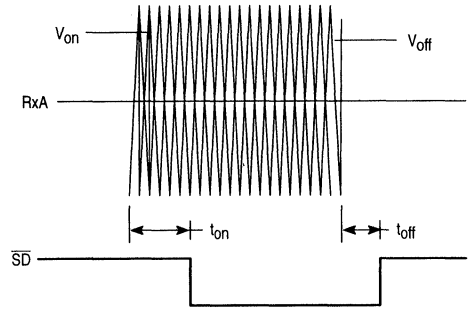


Figure 4. Carrier Detect Timing

Table 5. Carrier Detect Time Truth Table

CD1	CD0	Carrier Detect Time (Typ)	
		t_{on} (ms)	t_{off} (ms)
0	0	450	30
0	1	15	30
1	0	15	15
1	1	80	10

POWER–ON RESET

When the power is switched on, this device has the following conditions.

Function Mode	FSK
Transmit Attenuator	0 dB
Transmit Squelch	Enable
Channel	1 (Originate)

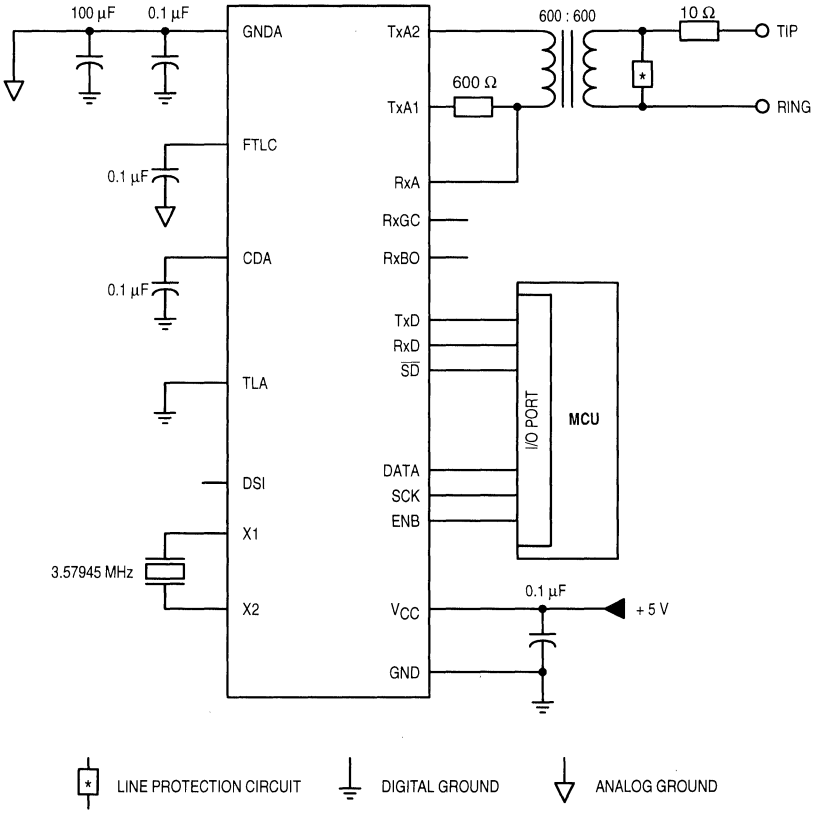
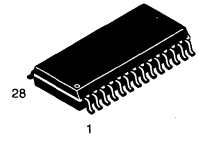


Figure 5. Application Circuit

MC145446A

Product Preview

Multi-Function 300-Baud Modem



FW SUFFIX
SOP
CASE 751M

ORDERING INFORMATION

MC145446AFW	SOP

The MC145446A is a silicon gate CMOS frequency shift keying (FSK) modem intended for use with telemeter systems or remote control systems over the telephone network. It replaces the MC145446.

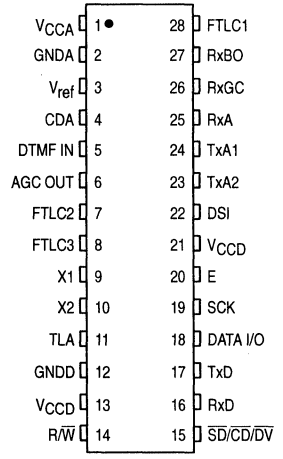
This device is compatible with CCITT V.21 and contains the entire circuit that provides a full–duplex or half–duplex 300–baud data communication over a pair of telephone lines. This device also includes the DTMF generator/receiver and call progress tone detector (CPTD).

The differential line driver has the capability of driving 0 dBm into a 600 Ω load with a single 5 V power supply. The transmit level is controlled by the programmable attenuator in 1 dB steps.

This device also includes a serial control interface and internal control and status registers that permit a CPU to exercise the following built–in features.

- Single 5 V Power Supply
- Compatible with CCITT V.21
- DTMF Generator and Receiver for All 16 Standard Digits
- Capable of Driving 0 dBm into a 600 Ω Load (V_{CC} = 5 V)
- AGC (Auto Gain Control) Amplifier for DTMF Receiver
- Imprecise Call Progress Tone (400 Hz) Detector
- A Transmit Attenuator Programmable in 1 dB Steps
- 2100 Hz Answer Tone Generator
- Serial Control Interface
- Analog Loopback Configuration for Self Test
- Power–Down Mode, Less than 1 μA

PIN ASSIGNMENT



This document contains information on a new product. Specifications and information herein are subject to change without notice.

REV 0
10/95

MC145447

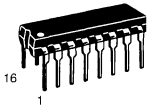
Calling Line Identification (CLID) Receiver with Ring Detector

The MC145447 is a silicon gate HCMOS IC designed to demodulate Bell 202 and V.23 1200–baud FSK asynchronous data. The primary application for this device is in products that will be used to receive and display the calling number, or message waiting indicator sent to subscribers from participating central office facilities of the public switched network. The device also contains a carrier detect circuit and ring detector which may be used to power up the device.

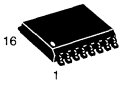
Applications for this device include adjunct boxes, answering machines, feature phones, fax machines, and computer interface products.

The MC145447 offers the following performance features.

- Ring Detector On–Chip
- Ring Detect Output for MCU Interrupt
- Power–Down Mode, Less than 1 μA
- Single Supply: + 3.5 to + 6.0 V
- Pin Selectable Clock Frequencies: 3.68 MHz, 3.58 MHz, or 455 kHz
- Two Stage Power–Up for Power Management Control
- Demodulates Bell 202 and V.23



P SUFFIX
PLASTIC DIP
CASE 648

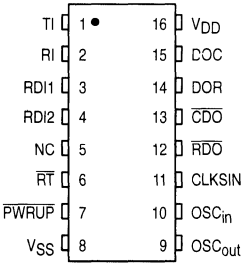


DW SUFFIX
SOG PACKAGE
CASE 751G

ORDERING INFORMATION

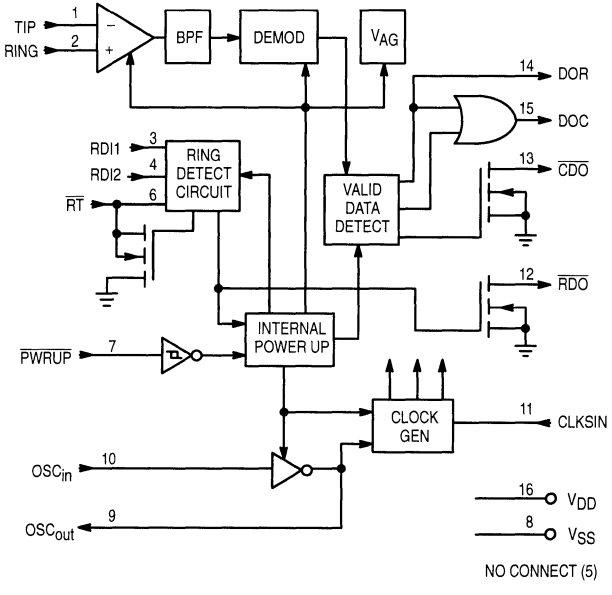
MC145447P	Plastic DIP
MC145447DW	SOG Package

PIN ASSIGNMENT



NC = NO CONNECTION

BLOCK DIAGRAM



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8/95

ABSOLUTE MAXIMUM RATINGS

(Voltages referenced to GND, except where noted)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	– 0.5 to + 6.0	V
Input Voltage, All Pins	V_{in}	– 0.5 to V_{DD} + 0.5	V
DC Current Drain Per Pin	I	± 10	mA
Power Dissipation	P_D	20	mW
Operating Temperature Range	T_A	0 to + 70	°C
Storage Temperature Range	T_{stg}	– 40 to + 150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

2

ELECTRICAL CHARACTERISTICS

(All polarities referenced to V_{SS} = 0 V, V_{DD} = + 5 V ± 10%, unless otherwise noted, T_A = 0 to + 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
DC Supply Voltage	V_{DD}	3.5	5	6	V
Supply Current (All Output Pins Unloaded) (See Figure 1) $\overline{RT}$ = 0, $\overline{PWRUP}$ = 1, XTAL = 3.58 MHz	I_{DD}	—	2.4	3	mA
Supply Current (All Output Pins Unloaded) (See Figure 1) $\overline{PWRUP}$ = 0, $\overline{RT}$ = Don't Care, XTAL = 3.58 MHz	I_{DD}	—	6.2	8	mA
Standby Current (All Output Pins Unloaded) (See Figure 1) $\overline{RT}$ = 1, $\overline{PWRUP}$ = 1	I_{STBY}	—	—	1	µA
Input Voltage 0 Level (CLKSIN, OSC_{in})	V_{IL}	—	—	V_{DD} x 0.3	V
Input Voltage 1 Level (CLKSIN, OSC_{in})	V_{IH}	V_{DD} x 0.7	—	—	V
Output Voltage High: V_{DD} = 5 V (DOR, DOC, OSC_{out}) I_{OH} = 40 µA $I_{OH} \le$ 1 µA	V_{OH}	 2.4 4.95	—	—	V
Output Voltage Low: V_{DD} = 5 V (DOR, DOC, OSC_{out}) I_{OL} = 1.6 mA $I_{OL} \le$ 1 µA	V_{OL}	—	—	 0.4 0.05	V
Input Leakage Current (OSC_{in}, CLKSIN, $\overline{PWRUP}$, $\overline{RT}$, RDI1, and RDI2)	I_{in}	—	—	±1	µA
Output Voltage Low: V_{DD} = 5 V ($\overline{RDO}$, $\overline{RT}$, $\overline{CDO}$) I_{OL} = 2.0 mA	V_{OL}	—	—	0.4	V
Input Threshold Voltage Positive Going: V_{DD} = 5 V (RDI1, $\overline{RT}$, $\overline{PWRUP}$) (See Figure 3)	V_{T+}	2.5	2.75	3.0	V
Input Threshold Voltage Negative Going: V_{DD} = 5 V (RDI1, $\overline{RT}$, $\overline{PWRUP}$) (See Figure 3)	V_{T-}	2.0	2.3	2.6	V
RDI2 Threshold	$R_{D2}V_T$	1.0	1.1	1.2	V
TIP/RING Input dc Resistance	R_{in}	—	500	—	kΩ

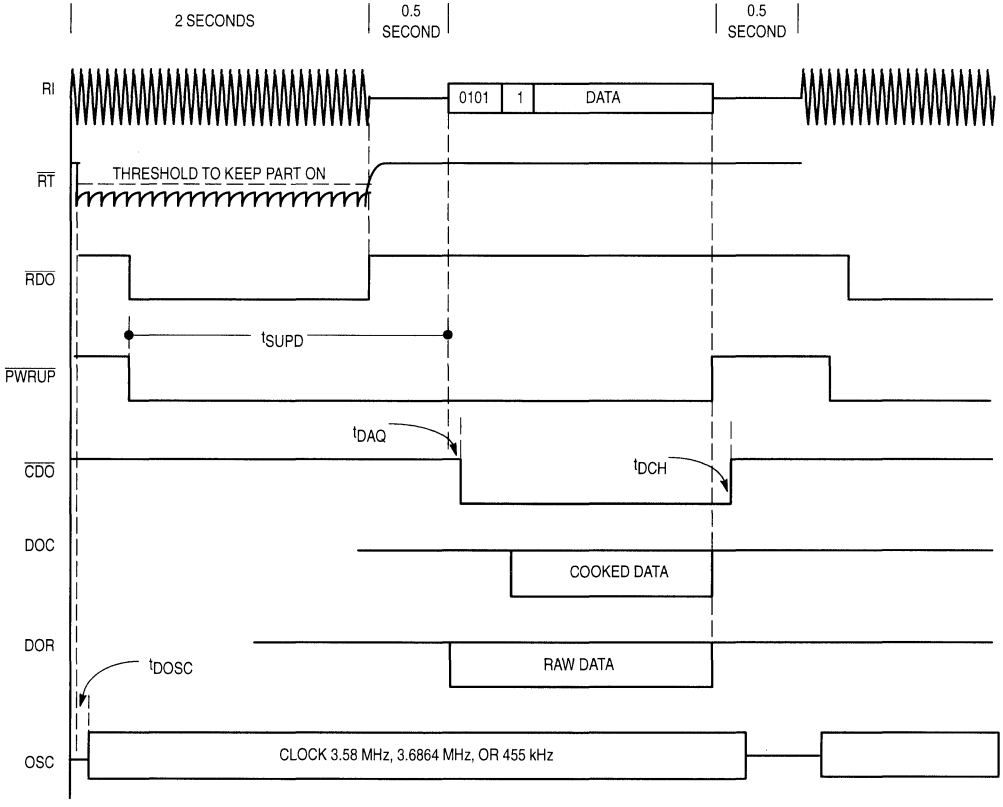
ANALOG CHARACTERISTICS (V_{DD} = + 5 V, T_A = + 25°C, unless otherwise noted, 0 dBm = 0.7746 Vrms @ 600 Ω)

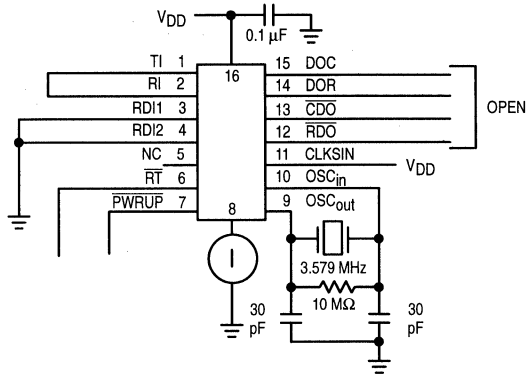
Characteristic		Min	Typ	Max	Unit
Input Sensitivity: TIP and RING (Pins 1 and 2, V_{DD} = + 5 V)		– 40	– 45	—	dBm
Band–Pass Filter (BPF)					dB
Frequency Response (Relative to 1700 Hz @ 0 dBm)	60 Hz	—	– 64	—	
	500 Hz	—	– 4	—	
	2700 Hz	—	– 3	—	
	≥ 3300 Hz	—	– 34	—	
Carrier Detect Sensitivity		—	– 48	—	dBm

SWITCHING CHARACTERISTICS (V_{DD} = + 5 V, C_L = 50 pF, T_A = + 25°C)

Description	Symbol	Min	Typ	Max	Unit
OSC Startup	t_{DOSC}	—	2	—	ms
Power–Up Low to FSK (Setup Time)	t_{SUPD}	15	—	—	ms
Carrier Detect Acquisition Time	t_{DAQ}	—	14	—	ms
End of Data to Carrier Detect High	t_{DCH}	8	—	—	ms

TIMING DIAGRAM





RT	PWRUP	I_{DD}	OSC_{in}
1	1	1 µA MAX	DISABLE
0	1	2.4 mA TYP	ENABLE
X	0	6.2 mA TYP	ENABLE

Figure 1. I_{DD} Test Circuit

PIN DESCRIPTIONS

TI
Tip Input (Pin 1)

This input pin is normally connected to the tip side of the twisted pair. It is internally biased to 1/2 supply voltage when the device is in the power–up mode. This pin must be dc isolated from the line.

RI
Ring Input (Pin 2)

This input is normally connected to the ring side of the twisted pair. It is internally biased to 1/2 supply voltage when the device is in the power–up mode. This pin must be dc isolated from the line.

RDI1
Ring Detect Input 1 (Pin 3)

This input is normally coupled to one of the twisted pair wires through an attenuating network. It detects energy on the line and enables the oscillator and precision ring detection circuitry.

RDI2
Ring Detect Input 2 (Pin 4)

This input to the precision ring detection circuit is normally coupled to one of the twisted pair wires through an attenuating network. A valid ring signal as determined from this input sends the $\overline{RDO}$ (Pin 12) to a logic 0.

$\overline{RT}$
Ring Time (Pin 6)

An RC network may be connected to this pin. The RC time constant is chosen to hold this pin voltage below 2.2 V between the peaks of the ringing signal. $\overline{RT}$ is an internal power–up control and activates only the circuitry necessary to determine if the incoming ring is valid.

$\overline{PWRUP}$
Power Up (Pin 7)

A logic 0 on the $\overline{PWRUP}$ input causes the device to be in the active mode ready to demodulate incoming data. A logic 1 on this pin causes the device to be in the standby mode, if the $\overline{RT}$ input pin is at a logic 1. This pin may be controlled by $\overline{RDO}$ and $\overline{CDO}$ for auto power–up operation. For other applications, this pin may be controlled externally.

V_{SS}
Ground (Pin 8)

Ground return pin is typically connected to the system ground.

OSC_{out}
Oscillator Output (Pin 9)

This pin will have either a crystal or a ceramic resonator tied to it with the other end connected to OSC_{in}.

OSC_{in}
Oscillator Input (Pin 10)

This pin will have either a crystal or a ceramic resonator tied to it with the other end connected to OSC_{out}. OSC_{in} may also be driven directly from an appropriate external source.

CLKSIN
Clock Select Input (Pin 11)

A logic 1 on this input configures the device to accept either a 3.579 MHz or 3.6864 MHz crystal. A logic 0 on this pin configures the part to operate with a 455 kHz resonator.

For crystal and resonator specifications see Table 1.

$\overline{RDO}$
Ring Detect Out (Pin 12)

This open–drain output goes low when a valid ringing signal is detected. $\overline{RDO}$ remains low as long as the ringing signal remains valid. This signal can be used for auto power–up, when connected to Pin 7.

$\overline{CDO}$
Carrier Detect Output (Pin 13)

When low, this open drain output indicates that a valid carrier is present on the line. $\overline{CDO}$ remains low as long as the carrier remains valid. An 8 ms hysteresis is built in to allow for a momentary drop out of the carrier. $\overline{CDO}$ may be used in the auto power–up configuration when connected to $\overline{PWRUP}$.

DOR
Data Out Raw (Pin 14)

This pin presents the output of the demodulator whenever $\overline{CDO}$ is low. This data stream includes the alternate 1 and 0 pattern, and the 150 ms of marking, which precedes the data. At all other times, DOR is held high.

DOC
Data Out Cooked (Pin 15)

This output presents the output of the demodulator whenever $\overline{CDO}$ is low, and when an internal validation sequence has been successfully passed. The output does not include the alternate 1 and 0 pattern. At all other times, DOC is held high.

V_{DD}
Positive Power Supply (Pin 16)

The digital supply pin, which is connected to the positive side of the power supply.

APPLICATIONS INFORMATION

The MC145447 has been designed to be one of the main functional blocks in products targeted for the CLASS (Custom Local Area Signaling Service) market. CLASS is a set of subscriber features now being presented to the consumer by the RBOCs (Regional Bell Operating Companies) and independent TELCOs. Among CLASS features, such as distinctive ringing and selective call forwarding, the subscriber will also have available a service known as Calling Number Delivery (CND) and message waiting. With these services, a subscriber will have the ability to display at a minimum, a message containing the phone number of the calling party, the date, and the time. A message containing only this information is known as a single format message, as shown in Figure 9. An extended message, known as multiple format message, can contain additional information as shown in Figure 10.

The interface should be arranged to allow simplex data transmission from the terminating central office, to the CPE (Customer Premises Equipment), only when the CPE is in an on–hook state. The data will be transmitted in the silent period between the first and second power ring after a voice path has been established.

The data signaling interface should conform to Bell 202, which is described as follows:

- Analog, phase coherent, frequency shift keying
- Logical 1 (Mark) = 1200 ± 12 Hz
- Logical 0 (Space) = 2200 ± 22 Hz
- Transmission rate = 1200 bps
- Application of data = serial, binary, asynchronous

The transmission level from the terminating C.O. will be – 13.5 dBm ± 1.0. The expected worst case attenuation through the loop is expected to be – 20 dB. The receiver therefore, should have a sensitivity of approximately – 34.5 dBm to handle the worst case installations.

Additional information on CLASS services can be obtained from:

BELLCORE CUSTOMER SVS.
1–800–521–2673
201–699–5800 FOREIGN CALLS
201–699–0936 FAX

The document number is: TA–NWT–000030
Title: "Voice Band Data Transmission Interface Generic Requirements"

Figure 7 is a conceptual design of how the MC145447 can be implemented into a product which will retrieve the incoming message and convert it to EIA–232 levels for transmission to the serial port of a PC. With this message and appropriate software, the PC can be used to look up the name and any additional information associated with the caller that had been previously stored.

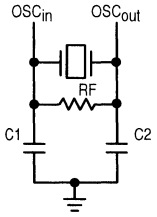
Figure 8 is a conceptual design of an adjunct unit in parallel with an existing phone. This arrangement gives the subscriber CND service without having to replace existing equipment.

Table 1. Oscillator Specifications

Clock Select Pin 11 = 1

Crystal Mode	Parallel
Frequency	3.579 MHz or 3.6864 MHz
R_f	10 MΩ
C1 and C2	30 pF

Source:
Fox Electronics
5570 Enterprise Pkwy.
Ft. Myers, FL 33905
Tel. 813–693–0099



Clock Select Pin 11 = 0

Resonator	#CSB455J
Frequency	455 kHz ± 0.5%
R_f	1.0 MΩ
C1 and C2	100 pF

Source:
Murata Manufacturing Co. Ltd.
2200 Lake Park Dr.
Smyma, GA 30080
Tel. 404–436–1300

NOTE: Motorola cannot recommend one supplier over another and in no way suggests that this is a complete listing.

FULL–TIME POWER–UP APPLICATION WITH RING DETECTOR CIRCUIT DISABLED

Some MC145447 applications require that the Calling Line Identification Receiver be constantly powered. To ensure that the device is properly reset, a Logic 1 must be applied to $\overline{PWRUP}$ (Pin 7) for a minimum of 10 µs after V_{DD} has reached its full value. It is also necessary that the $\overline{RT}$ pin (Pin 6) be high while $\overline{PWRUP}$ is high. This may be accomplished with an external ring detect signal or MCU generated signal applied to $\overline{PWRUP}$. Alternatively, a power on reset RC network may be used as shown in Figure 6. Rpu and Cpu must be chosen such that the voltage at $\overline{PWRUP}$ meets the logic 1 input threshold requirements for 10 µs after V_{DD} has reached its full value. The power supply rise time on V_{DD} (Pin 16) must also be taken into account when determining Rpu and Cpu. See Figure 3 for a description of the change in input thresholds (V_{T+} and V_{T-}) with respect to V_{DD} for $\overline{PWRUP}$. Also, some applications may not require the ring detect function. In this case, RDI1 (Pin 3) and RDI2 (Pin 4) should be tied to V_{SS} and $\overline{RT}$ tied to V_{DD} as shown in Figure 6.

DESIGN INFORMATION

The circuit in Figure 2 illustrates in greater detail the relationship between Pins 3, 4, 6, and 7.

The external component values shown in Figure 2 are the same as those shown in Figures 7 and 8. When V_{DD} is applied to the circuit in these two figures, the RC network will charge cap C1 to V_{DD} holding $\overline{RT}$ (Pin 6) off. If the $\overline{PWRUP}$ (Pin 7) is also held at V_{DD}, the MC145447 will be in a power–down mode, and will consume 1 μA of supply current (max).

The resistor network (R2 – R4) attenuates the incoming power ring applied to the top of R2. The values given have been chosen to provide a sufficient voltage at RDI1 (Pin 3) to turn on the Schmitt–trigger input with approximately a 40 Vrms or greater power ring input from tip and ring. When V_{T+} of the Schmitt is exceeded, Q1 will be driven to saturation discharging cap C1 on $\overline{RT}$. This will initialize a partial power–up, with only the portions of the part involved with the ring signal analysis enabled, including RDI2 (Pin 4). At this time the MC145447 power consumption is increased to approximately 2.4 mA (typ).

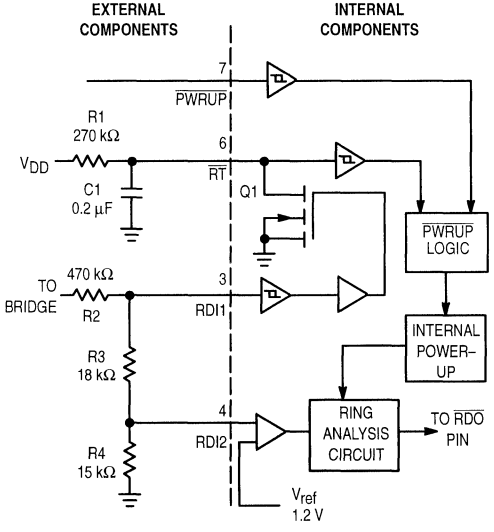


Figure 2.

The value of R1 and C1 must be chosen to hold the $\overline{RT}$ pin voltage below the V_{T+} of the $\overline{RT}$ Schmitt between the individual cycles of the power ring. The values shown will work for ring frequencies of 15.3 Hz (min).

With RDI2 now enabled, a portion of the power ring above 1.2 V is fed to the ring analysis circuit. This circuit is a digital integrator which looks at the duty cycle of the incoming signal. When the input to RDI2 is above 1.2 V, the integrator is counting up at an 800 Hz rate. When the input to RDI2 falls below 1.2 V, the integrator counts down at a 400 Hz rate.

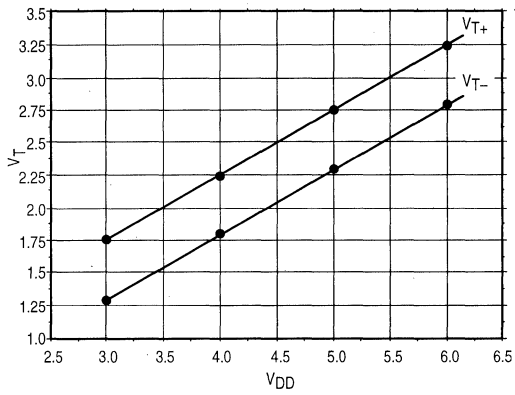


Figure 3. V_{DD} versus V_{T+} and V_{T-}

A ring is qualified when an internal count of binary 48 is reached. The ring is disqualified when the count drops to a binary 32. The number of ring cycles required to qualify the signal will depend on the amplitude of the voltage presented to RDI2. The shortest amount of time needed to do the qualification is approximately 60 ms. The shortest amount of time required for dequalification will be approximately 40 ms.

Once the ring signal is qualified, the $\overline{RDO}$ pin will be sent low. This can be fed back to $\overline{PWRUP}$ as shown in Figure 7, or with a pull–up resistor, can be used as an interrupt to an MCU as shown in Figure 8. In either case, once the $\overline{PWRUP}$ pin is below V_{T-}, the part will be fully powered up, and ready to receive FSK. During this mode, the device current will increase to approximately 6.2 mA (typ). The state of the $\overline{RT}$ pin is now a "don't care" as far as the part is concerned. Normally, however, this pin will be allowed to return to V_{DD}.

After the FSK message has been received, the $\overline{PWRUP}$ pin can be allowed to return to V_{DD} and the part will return to the standby mode, consuming less than 1 μA of supply current. The part is now ready to repeat the same sequence for the next incoming message.

TYPICAL DEMODULATOR PERFORMANCE

The following describes the performance of the MC145447 demodulator in the presence of noise over a simulated Bell 3002 telephone loop.

The Bell 3002 loop represents a worst case local telephone loop in North America. The characteristics of this loop, which affect performance, are high frequency attenuation and Envelope Delay Distortion (EDD) or group delay.

The minimum receiver sensitivity of the MC145447 under these conditions is typically – 45 dBm.

The MC145447 achieves a Bit Error Rate (BER) of 1×10^{-5} at a Signal–to–Noise Ratio (SNR) of 15 dB in V.23 operation and at an SNR of 18 dB in Bell 202 operation (see Figures 4 and 5).

All measurements in dBm are referenced to 600 Ω: 0 dBm = 0.7746 Vrms.

All measurements were taken using the MC145460EVK evaluation board.

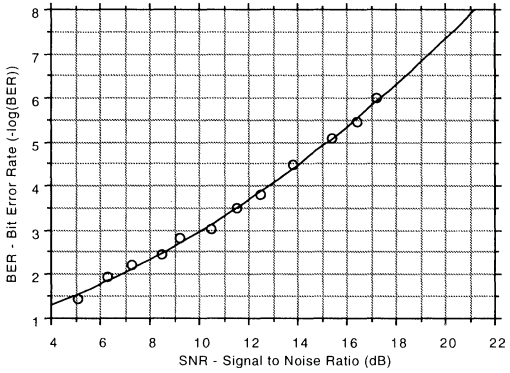


Figure 4. MC145447 V.23 Operation (Typical BER vs SNR)

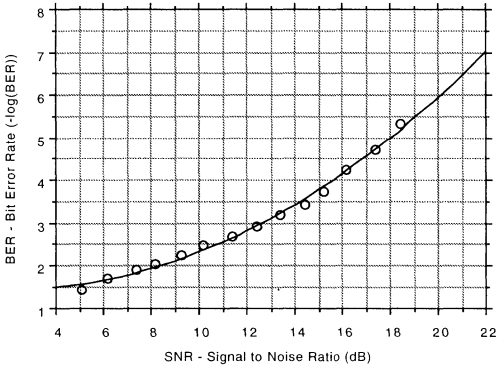


Figure 5. MC145447 Bell 202 Operation (Typical BER vs SNR)

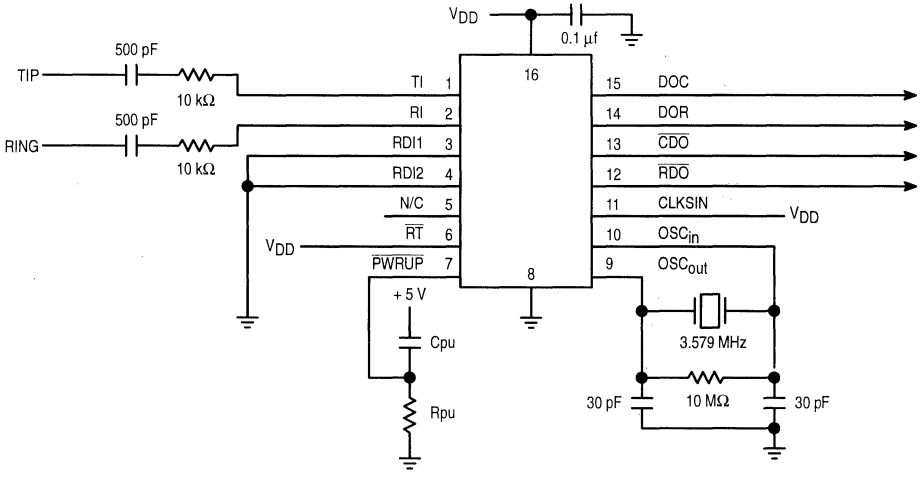


Figure 6.

APPLICATION CIRCUIT

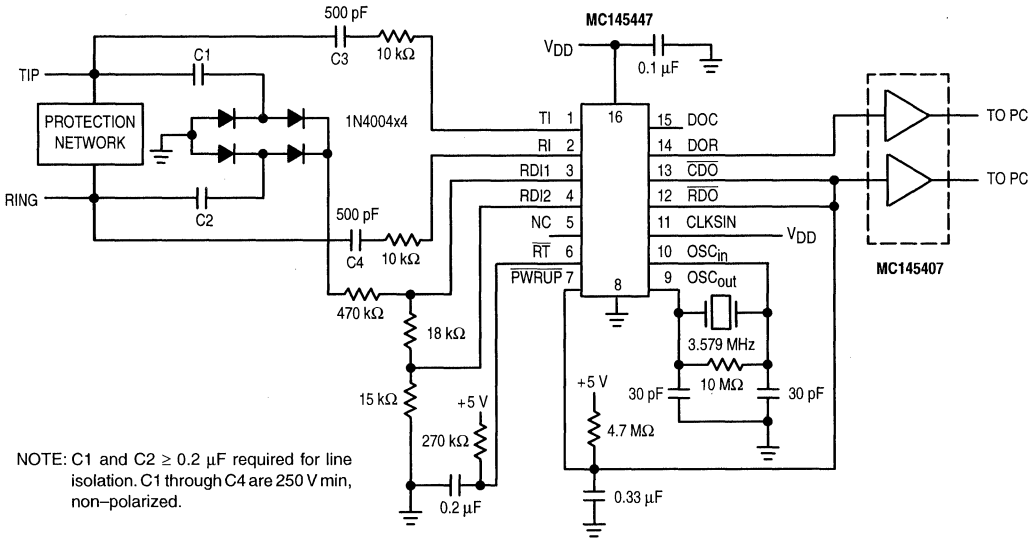
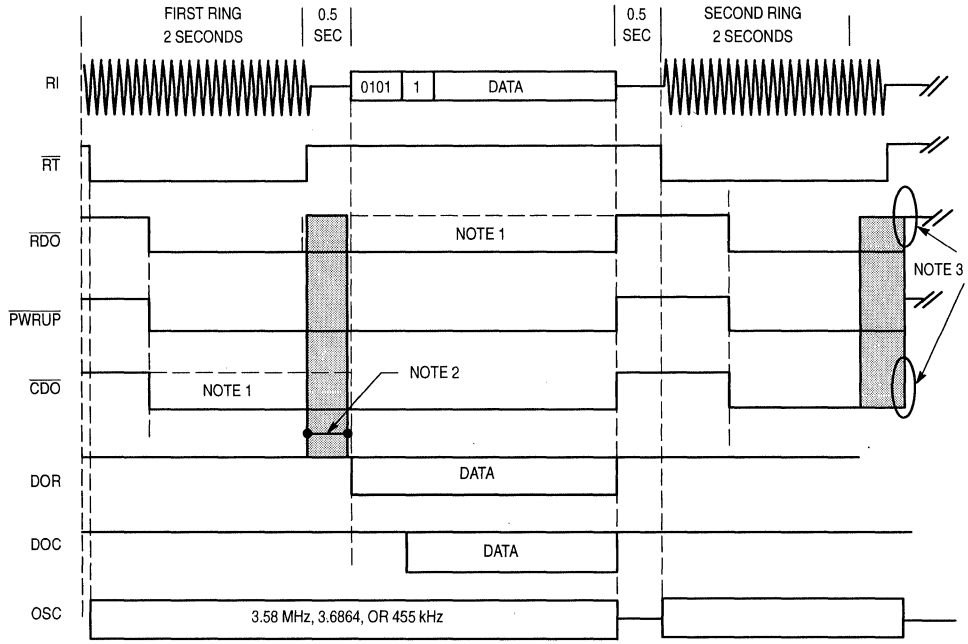


Figure 7. Partial Implementation of PC Interface to Tip and Ring



NOTES:
1. Wired 'OR' RDO with CDO.
2. Overlap of RDO edge with CDO edge to ensure part stays in PWRUP determined by RC time constant on RDO, PWRUP, and CDO pin.
3. Part reverts to PWR ON, on rising edge of RDO since there is no CDO.

Timing Diagram for Figure 7

APPLICATION CIRCUIT

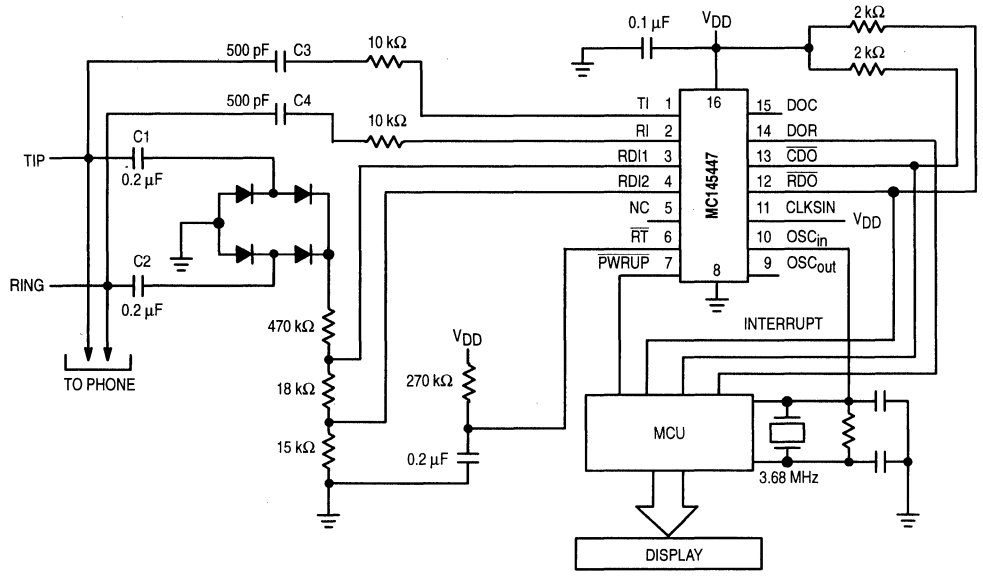
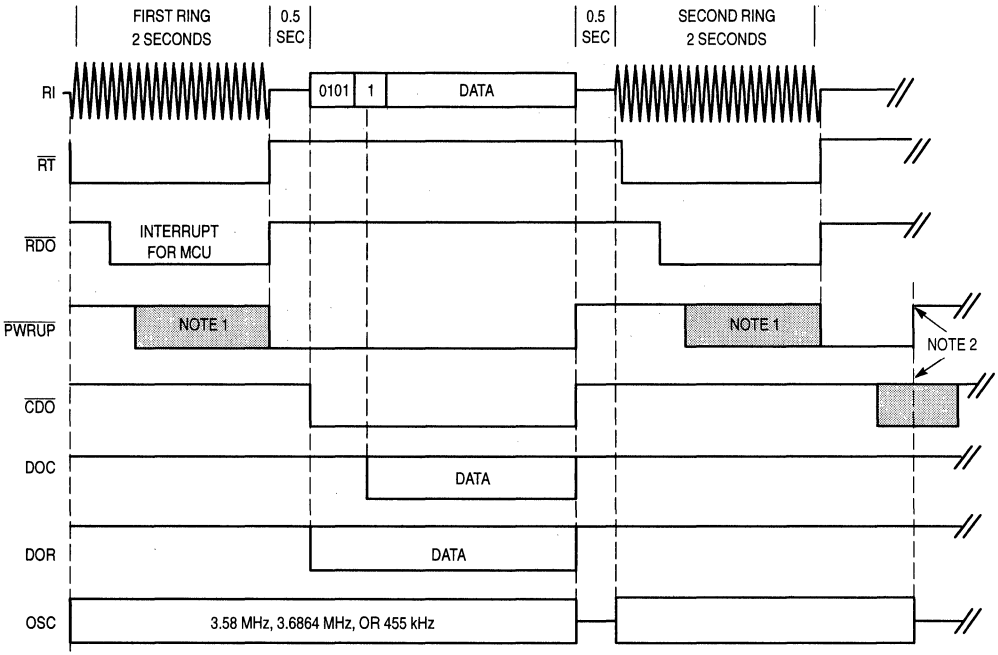


Figure 8. Adjunct Box Concept for Calling Number Display



NOTES:
1. MCU must assert $\overline{\text{PWRUP}}$ to MC145447.
2. No data detected, MCU powers down the MC145447.

Timing Diagram for Figure 8

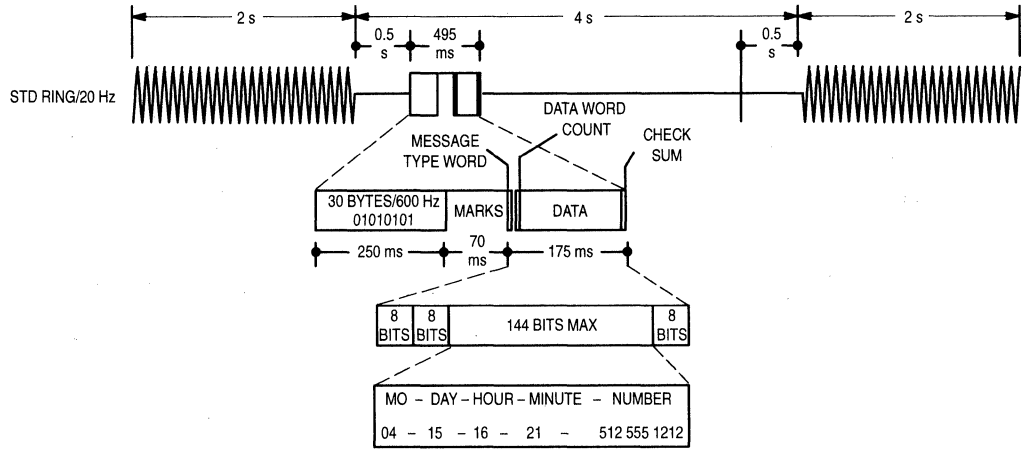


Figure 9. Single Message Format

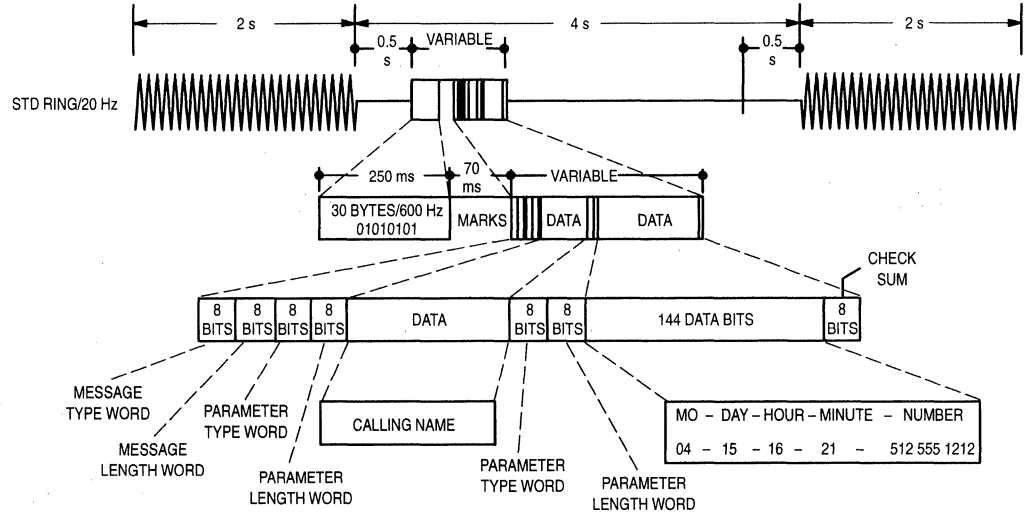


Figure 10. Multiple Message Format

MC145472
MC14LC5472

Technical Summary
U-Interface Transceiver

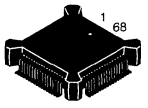
This technical summary provides a brief description of the MC145472 and MC14LC5472 U–Interface Transceivers. A complete data book for the MC145472 and MC14LC5472 is available and can be ordered from your local Motorola sales office. The data book number is MC145472/D.

The MC145472 U–Interface Transceiver is a single chip device intended for the ISDN Basic Access Interface and conforms to the American National Standard known as ANSI T1.601–1992. The MC145472 can be configured for LT or NT applications and performs all necessary Layer 1 functions while utilizing 2B1Q line coding.

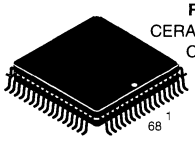
The customer data crossing the U Reference Point consists of two 64 kbps B channels and one 16 kbps D channel in each direction. This data is input to and output from the MC145472 via the industry standard Interchip Digital Link (IDL).

The MC145472 can operate in many different modes. The control of these various modes is provided via special purpose pins and the Serial Control Port (SCP). The SCP conforms to the Motorola Serial Peripheral Interface standard, an industry standard serial microprocessor interface.

The MC14LC5472 supercedes the MC145472. The MC14LC5472 has 500 mW power consumption when activated. In all other respects, it is the same as the MC145472. In this technical summary, MC145472 and MC14LC5472 are used interchangeably.



FU SUFFIX
PQFP
CASE 847

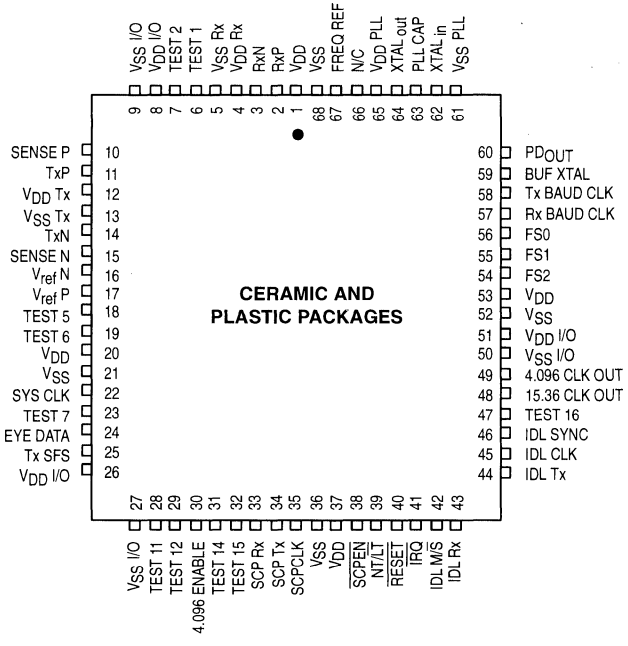


FE SUFFIX
CERAMIC PACKAGE
CASE 847B

ORDERING INFORMATION

MC145472FE	Ceramic Package
MC14LC5472FE	Ceramic Package
MC14LC5472FU	PQFP

PIN ASSIGNMENT



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Also, the MC14LC5472 is available in a 68–lead Plastic Quad Flat Package (PQFP). Both the MC145472 and MC14LC5472 are available in a 68–lead Ceramic Quad Flat Package. The 68–lead PQFP for the MC14LC5472 has a considerably smaller printed circuit board footprint than the 68–lead Ceramic Quad Flat Package. This permits more MC14LC5472s to be placed on a circuit board than would be the case if the MC145472 was used.

Information regarding the generic 2B1Q U–Interface requirement is readily available in standards documents such as ANSI T1.601–1992 and therefore has not been included in this document. The U–Interface equipment designer will find the ANSI document to be a useful reference.

Key features of the MC14LC5472 U–Interface Transceiver include:

- Single Chip 2B1Q Echo Canceling Adaptively Equalized Transceiver
- Conforms to ANSI T1.601–1992, Integrated Services Digital Network (ISDN) Basic Access Interface for Use on Metallic Loops for Application on the Network Side of the NT (Layer 1 Specification) of the American National Standards Institute, Inc.
- Warm Start Capability
- NT Synchronizes to and Operates with 80 kHz ± 32 ppm Received Signal from LT
- IDL Interface Supports Master, Slave, and Slave–Slave Timing Modes
- On–Chip FIFOs for Transmit and Receive Directions
- MC14LC5472 Power Consumption is 500 mW Maximum When Activated
- 2B + D Customer Data Provided by the Industry Standard IDL Interface
- Control, Status, and Extended Maintenance Functions Provided through the SCP
- On–Chip Conformance with Activation and Deactivation as Specified in the American National Standard T1.601
- Automatic Handling of Basic Maintenance Functions
- Automatic Internal Compliance with the Embedded Operations Channel (eoc) Protocol as Specified in the American National Standard
- Extended Maintenance Functions Provided through the SCP
- Complete Set of Loopbacks for Both the IDL and U Reference Point Directions
- Pin Selectable for Line Termination (LT) or Network Termination (NT) Applications
- On–Chip 2.5 V Transmit Driver Meeting 1992 Requirement
- Eight Different Choices of Reference Frequency Input in LT Mode
- High Performance CMOS Process Technology
- 5 V Power Supply
- The MC14LC5494EVK is the Evaluation Platform for the MC14LC5472

ISDN BASIC ACCESS SYSTEM OVERVIEW

ISDN Reference Model

The ISDN Reference Model is shown in Figure 1. This is a general model which can be adapted to many different implementations of the ISDN. The diagram indicates the position of the U Reference Point between the Line Termination (LT) and the Network Termination 1 (NT1) blocks in the model.

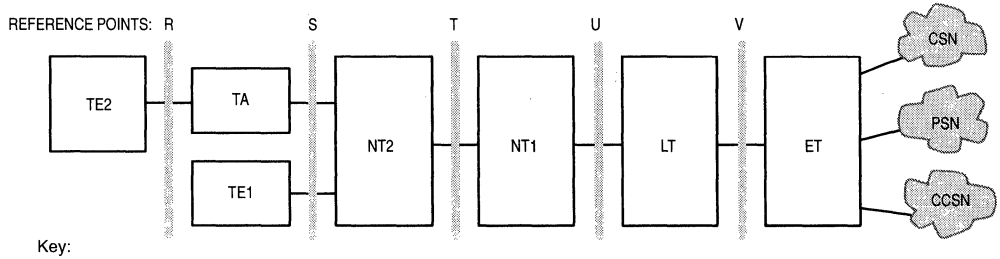
The U–Interface is the physical point of access to the ISDN at the U Reference Point defined in the Reference Model. This interface is a single twisted wire pair supporting full–duplex transmission of digital information at a rate of 160 kbps. The twisted wire pair can extend up to 18,000 feet and may include bridge taps. This interface is often referred to as a Digital Subscriber Line.

U–Interface Transceiver Applications

Some typical ISDN applications of the MC145472 U–Interface Transceiver are shown in Figure 2. This figure shows how Motorola ISDN devices can be configured with other Motorola MCUs and Codecs to implement ISDN equipment such as terminal adapters, NT1s, terminal equipment, line cards, and U–Interface terminals.

A typical non–ISDN pair gain application is shown in Figures 3 and 4. Pair gain is a technique to multiplex two or more analog phone lines over a digital line and recreate them at the customer location.

Figure 5 details how to connect two MC145472 U–Interface transceivers as a U–Repeater.



Key:

CCSN: Common Channel Signalling Network
CSN: Circuit Switched Network
ET: Exchange Termination (C.O. Switch)
LT: Line Termination (Line Card)
NT1: Network Termination 1 (OSI Layer 1 Only)
NT2: Network Termination 2 (OSI Layers 2 and 3)
PSN: Packet Switched Network
TA: Terminal Adapter
TE1: Terminal Equipment 1 (ISDN Terminal)
TE2: Terminal Equipment 2 (Non–ISDN Terminal)

Figure 1. ISDN Reference Model

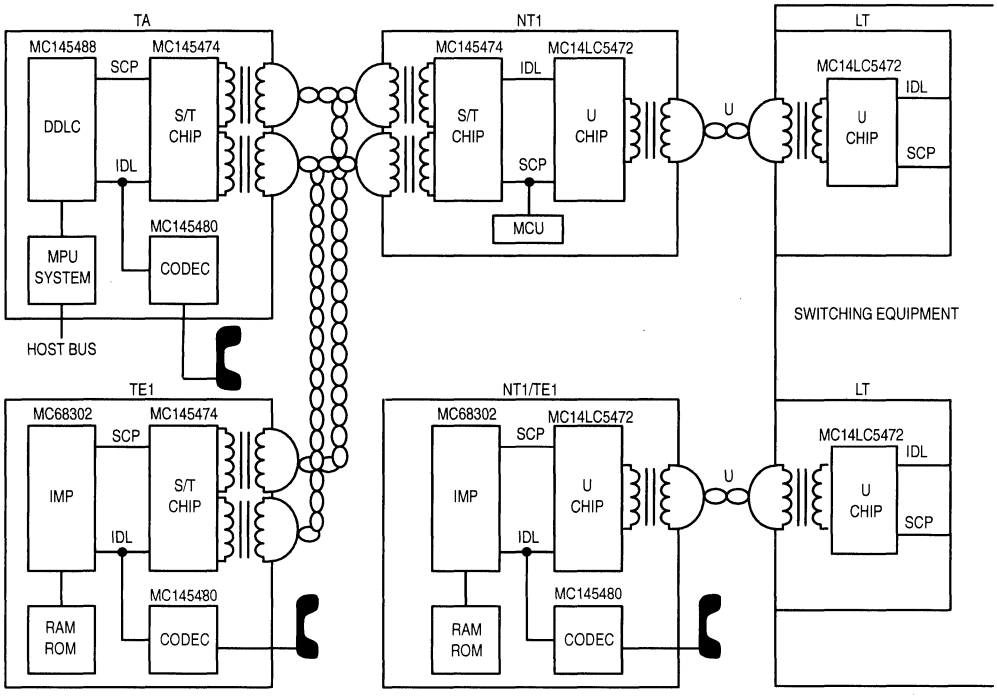


Figure 2. MC14LC5472 Typical ISDN Applications

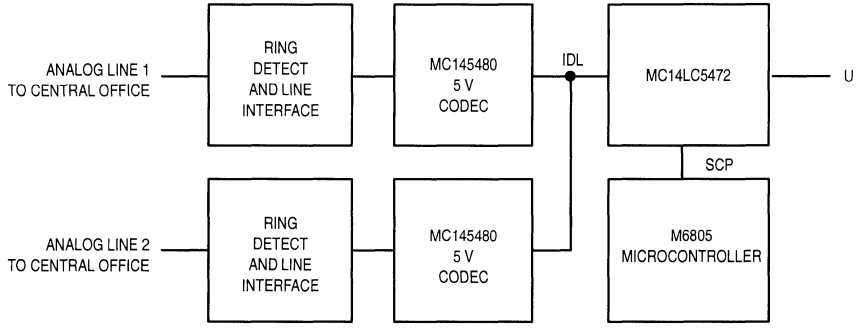


Figure 3. Pair Gain Application, Central Office Terminal

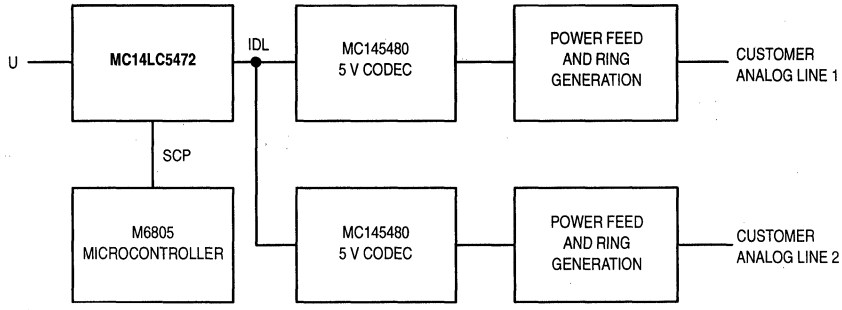
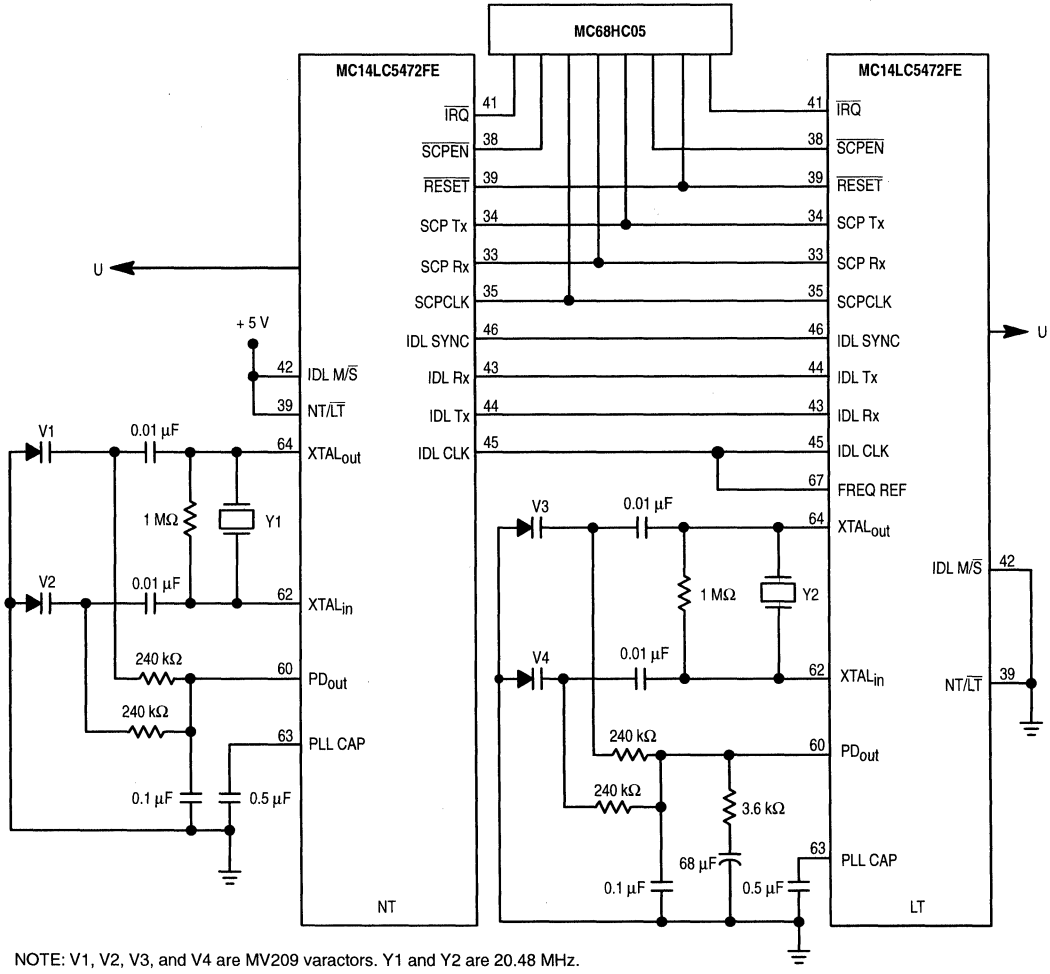


Figure 4. Pair Gain Application, Remote Terminal



NOTE: V1, V2, V3, and V4 are MV209 varactors. Y1 and Y2 are 20.48 MHz.

Figure 5. U Repeater Showing Clock and IDL Connections

DEVICE DESCRIPTION

FUNCTIONAL DESCRIPTION

A functional block diagram of the MC145472 U–Interface Transceiver is shown in Figure 6. The MC14572 utilizes mixed analog and digital signal processing circuit technology to implement an adaptively equalized echo canceling full–duplex transmitter/receiver or transceiver.

2B+D data is input to the device at the IDL Rx input. This data is passed through a FIFO prior to being formatted and scrambled in the Superframe Framer. The resulting 160 kbps binary data stream is converted to an 80 kbaud dibit stream which is subsequently converted to four analog amplitudes by the DAC (digital–to–analog converter). The resulting pulse amplitude modulated signal is band–limited by the Tx Filter prior to entering the Tx Driver which differentially drives the line coupling circuit to the twisted wire pair.

From the twisted wire pair, information from the far end U–Interface Transceiver is coupled through the external line interface circuit to the differential receiver inputs RxP and RxN. (In this two–wire environment, the transmitted signal is also coupled into the receiver inputs.) This combined analog signal is converted to a digital word in a sigma–delta, analog–to–digital converter. After filtering, an adaptively generated replica of the transmitted signal, calculated by the echo canceler, is subtracted from the combined signal leaving only the far end signal. In addition, phase dispersion present in the far end signal is corrected by the Decision Feedback Equalizer. The resulting four level signal is decoded by the slicer to produce a 160 kbps data stream. Timing information is also recovered from the far end signal. The Superframe Deframer descrambles and disassembles the received superframes and passes the received 2B+D data through a FIFO to the IDL Interface where it is available at the IDL Tx output.

Control and status of the device is handled via the SCP, a standard serial microcontroller interface. The SCP provides access to the 4 kbps Maintenance Channel in the U–Interface superframe. In addition, activation and deactivation are handled by an Automatic Activation Controller and the eoc portion of the M channel can be handled automatically with the Automatic eoc Processor.

A crystal oscillator and analog Phase–Locked Loop (PLL) are provided to ease clocking requirements for the device.

U–INTERFACE DATA FORMAT

The data transmitted on the U–Interface is organized into a 12 ms long superframe. This superframe consists of eight basic frames each of 1.5 ms in duration. The first nine bauds of each frame are a synchronization word. The next 108 bauds consists of 12 × 2B+D data. The last three bauds consist of maintenance channel data including a cyclic redundancy check. The first frame of the superframe is identified by its sync word being inverted.

The U–Interface Transceiver transmits a four level 2B1Q, (two binary, one quaternary), line code. Two bits are encoded into each baud. Each basic frame consists of 120 bauds or 240 bits of data. The baud symbols are called + 3, + 1, – 1, and – 3. The B and D channel data is scrambled before being transmitted. Figure 7 gives an example of the 2B1Q line code. Tables 1 and 2 detail the U–Interface superframe formats.

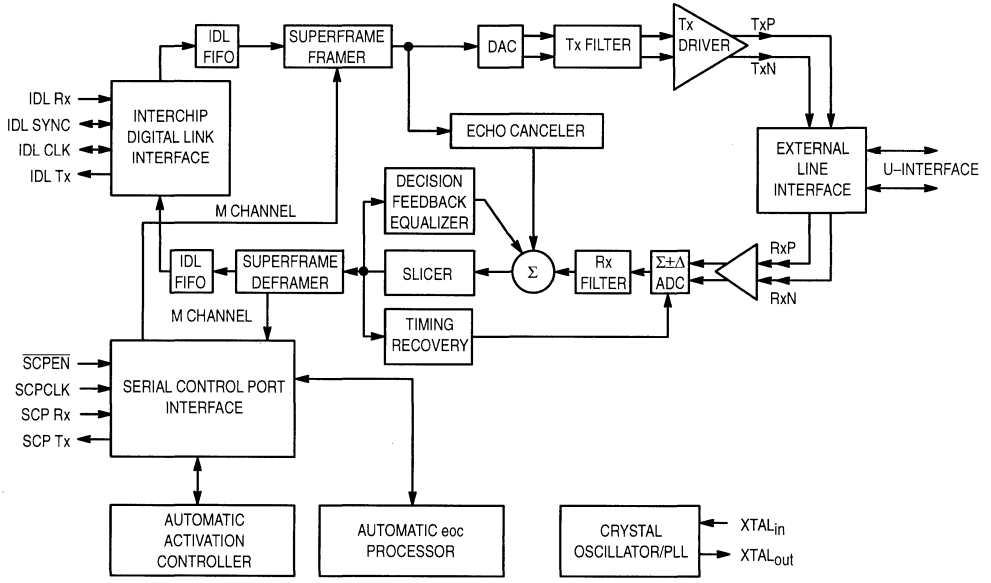


Figure 6. MC14LC5472 Functional Block Diagram

Table 1. Superframe Data Format, LT NT

	Framing	2B+D	Overhead Bits (M – M6)					
QUAT Positions	1 – 9	10 – 117	118s	118m	119s	119m	120s	120m
Bit Positions	1 – 18	19 – 234	235	236	237	238	239	240
Basic Frame #	**Sync Word**	**2B+D**	**M1**	**M2**	**M3**	**M4**	**M5**	**M6**
1	ISW	12 x 2B+D	eoc a1	eoc a2	eoc a3	act	1	1
2	SW	12 x 2B+D	eoc dm	eoc i1	eoc i2	dea	1	febe
3	SW	12 x 2B+D	eoc i3	eoc i4	eoc i5	1	crc1	crc2
4	SW	12 x 2B+D	eoc i6	eoc i7	eoc i8	1	crc3	crc4
5	SW	12 x 2B+D	eoc a1	eoc a2	eoc a3	1	crc5	crc6
6	SW	12 x 2B+D	eoc dm	eoc i1	eoc i2	1	crc7	crc8
7	SW	12 x 2B+D	eoc i3	eoc i4	eoc i5	uoa	crc9	crc10
8	SW	12 x 2B+D	eoc i6	eoc i7	eoc i8	aib	crc11	crc12

act = start up bit, set = 1 during start up
aib = alarm indication bit (set = 0 to indicate interruption)
crc = cyclic redundancy check: covers 2B+D + M4
dea = turn off bit (set = 0 to indicate turn off)
febe = far end block error
uoa = U–only–activation
1 = reserved bit for future standard (set = 1)
eoc = embedded operations channel
a = address bit
dm = data/message indicator (0 = data, 1 = message)
i = information bit

Table 2. Superframe Data Format, NT LT

	Framing	2B+D	Overhead Bits (M1 – M6)					
QUAT Positions	1 – 9	10 – 117	118s	118m	119s	119m	120s	120m
Bit Positions	1 – 18	19 – 234	235	236	237	238	239	240
Basic Frame #	**Sync Word**	**2B+D**	**M1**	**M2**	**M3**	**M4**	**M5**	**M6**
1	ISW	12 x 2B+D	eoc a1	eoc a2	eoc a3	act	1	1
2	SW	12 x 2B+D	eoc dm	eoc i1	eoc i2	ps1	1	febe
3	SW	12 x 2B+D	eoc i3	eoc i4	eoc i5	ps2	crc1	crc2
4	SW	12 x 2B+D	eoc i6	eoc i7	eoc i8	ntm	crc3	crc4
5	SW	12 x 2B+D	eoc a1	eoc a2	eoc a3	cso	crc5	crc6
6	SW	12 x 2B+D	eoc dm	eoc i1	eoc i2	1	crc7	crc8
7	SW	12 x 2B+D	eoc i3	eoc i4	eoc i5	sai	crc9	crc10
8	SW	12 x 2B+D	eoc i6	eoc i7	eoc i8	1	crc11	crc12

act = start up bit, set = 1 during start up.
crc = cyclic redundancy check: covers 2B+D + M4
cso = cold start only (set = 1 for cold start only)
febe = far end block error
ntm = NT in test mode bit (set = 0 to indicate test mode)
sai = S–active indicator bit (optional, set = 1 for S/T activity)
1 = reserved bit for future standard (set = 1)
eoc = embedded operations channel
a = address bit
dm = data/message indicator (0 = data, 1 = message)
i = information bit
ps1, ps2 = power status bits (set = 0 to indicate power problems)

PIN FUNCTIONALITY

Tables 3 through 7 list the MC145472 pins in functional groups and provide brief pin descriptions. For more detailed information, refer to the MC145472 data book.

MODE SELECTION

These pins are used to select the operating mode of the MC145472 U–Interface Transceiver.

The RESET pin is a Schmitt–trigger input and holds the MC145472 in a hardware reset condition when at logic 0.

The NT/$\overline{LT}$ input pin selects the operating mode of the MC145472. When at logic 1 the U–Interface Transceiver is in NT mode. When at logic 0 the U–Interface Transceiver is in LT mode.

Figures 8 and 9 show typical LT and NT mode connections, respectively.

INTERCHIP DIGITAL LINK (IDL) INTERFACE

The IDL Interface consists of five pins: IDL M/$\overline{S}$, IDL SYNC, IDL CLK, IDL Tx, and IDL Rx. With the IDL M/$\overline{S}$ pin the IDL Interface can be configured as an IDL Master (IDL SYNC and IDL CLK are outputs) or an IDL Slave (IDL SYNC and IDL CLK are inputs). The IDL Interface receives 2B+D data on the IDL Rx pin and buffers it through a FIFO to the Superframe Framer (See Figure 6). Simultaneously, this block accepts 2B+D data from the Superframe Deframer, buffers it through a FIFO, and transmits it out the IDL Tx pin. Figure 10 shows the IDL data formats.

Table 3. Quick Reference to Power Supply and Mode Selection Pins

Power Supply Pins		
Pin Name	**Pin No.**	**Pin Description**
V_{DD}	1, 20, 37, 53	Positive power supply, nominally + 5 V.
V_{SS}	21, 36, 52, 68	Negative power supply, nominally ground.
V_{DD} Rx	4	Positive power supply for analog receive circuits, nominally + 5 V.
V_{SS} Rx	5	Negative power supply for analog receive circuits, nominally ground.
V_{DD} Tx	12	Positive power supply for analog transmit circuits, nominally + 5 V.
V_{SS} Tx	13	Negative power supply for analog transmit circuits, nominally ground.
V_{DD} I/O	8, 26, 51	Positive power supply for input and output circuits, nominally + 5 V.
V_{SS} I/O	9, 27, 50	Negative power supply for input and output circuits, nominally ground.
V_{DD} PLL	65	Positive power supply for phase–locked loop circuits, nominally + 5 V.
V_{SS} PLL	61	Negative power supply for phase–locked loop circuits, nominally ground.
Mode Selection Pins		
Pin Name	**Pin No.**	**Pin Description**
RESET	40	Hardware reset when at a logic low, normal operation when at a logic high. This pin has a Schmitt–trigger input.
NT/$\overline{LT}$	39	Hardware selection of LT (logic low) and NT (logic high) operating mode.

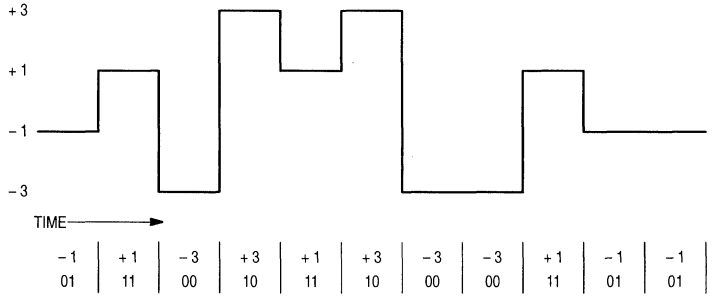


Figure 7. 2B1Q Line Code

Table 4. Quick Reference to IDL and SCP Pins

Interchip Digital Link (IDL) Interface Pins		
Pin Name	**Pin No.**	**Pin Description**
IDL M/$\overline{S}$	42	Selects between IDL Master (IDL CLK and IDL SYNC are outputs) and IDL Slave (IDL CLK and IDL SYNC are inputs) modes. Logic high selects IDL Master mode and logic low selects IDL Slave mode.
IDL SYNC	46	8 kHz IDL frame synchronization input (IDL Slave mode) or output (IDL Master mode).
IDL CLK	45	Bit clock input (IDL Slave mode) or output (IDL Master mode) for serial transfer of 2B+D data at IDL Tx and IDL Rx.
IDL Tx	44	This is the IDL output for the 2B+D data.
IDL Rx	43	This is the IDL input for the 2B+D data.
Serial Control Port (SCP) Interface Pins		
Pin Name	**Pin No.**	**Pin Description**
$\overline{SCPEN}$	38	SCP Enable Input held low selects the device for a read or write operation to the SCP.
SCPCLK	35	SCP Clock is an input which clocks the SCP data.
SCP Tx	34	SCP data output.
SCP Rx	33	SCP data input.
$\overline{IRQ}$	41	Open–drain output held low during an interrupt condition.

Table 5. Quick Reference to 2B1Q Interface Pins

2B1Q Interface Pins		
Pin Name	**Pin No.**	**Pin Description**
TxP	11	Positive output of the differential transmit driver.
TxN	14	Negative output of the differential transmit driver.
SENSE P	10	This pin senses the amplitude of the positive transmit driver output.
SENSE N	15	This pin senses the amplitude of the negative transmit driver output.
RxP	2	Positive input to the differential receive circuit.
RxN	3	Negative input to the differential receive circuit.
V_{ref} P	17	Positive input for off chip voltage reference. Connect a 0.1 μF ceramic capacitor between this pin and V_{ref} N.
V_{ref} N	16	Negative input for off chip voltage reference. Connect a 0.1 μF ceramic capacitor between this pin and V_{ref} P.
Tx BAUD CLK	58	This pin provides an 80 kHz clock output corresponding to the transmitted 2B1Q bauds.
Rx BAUD CLK	57	This pin provides an 80 kHz clock output corresponding to the received 2B1Q bauds.
EYE DATA	24	Once per received baud period, this pin outputs at a rate of 10.24 Mbps a serial digital word which represents the recovered 2B1Q signal or eye pattern.
SYS CLK	22	A 10.24 MHz clock output derived from the 20.48 MHz crystal oscillator which may be used to sample EYE DATA.
Tx SFS	25	Generates an output pulse once every transmitted superframe.

Table 6. Quick Reference to Phase–Locked Loop and Test Pins

Phase–Locked Loop and Clock Pins		
Pin Name	**Pin No.**	**Pin Description**
FREQ REF	67	In LT mode this input accepts one of eight possible stable input frequencies which is frequency multiplied to 20.48 MHz, the device's master clock frequency. Connect this pin high or low in NT mode. This pin has a Schmitt–trigger input.
FS0 FS1 FS2	56 55 54	The state of these three inputs indicates the frequency being applied to the FREQ REF pin. Connect these pins low or high in NT mode.
$XTAL_{in}$	62	This is the input of the 20.48 MHz crystal oscillator amplifier.
$XTAL_{out}$	64	This is the output of the 20.48 MHz crystal oscillator amplifier.
BUF XTAL	59	Buffered 20.48 MHz square wave output.
PD_{out}	60	Output of the PLL phase detector.
PLL CAP	63	Connect a 0.1 μF ceramic capacitor from this pin to ground.
15.36 CLK OUT	48	Buffered 15.36 MHz output.
4.096 CLK OUT	49	Buffered 4.096 MHz output.
4.096 ENABLE	30	When tied high this input enables the buffered 4.096 MHz clock output.

Table 7. Quick Reference to Test Pins

Test Pins		
Pin Name	**Pin No.**	**Pin Description**
TEST 5, 7, 11, 12, 14, 15, 16	18, 23, 28, 29, 31, 32, 47	Test pins for Motorola use. These pins should be connected to ground for normal operation.
TEST 1, 2, 6	6, 7, 19	Test pins for Motorola use. These pins should be left open circuit for normal operation.

The IDL interface can operate in IDL slave mode or IDL master mode. This is independent of the transceiver being in LT or NT mode. Normally, IDL slave mode is used when the MC145472 is configured as an LT and IDL master mode is used when the MC145472 is configured as an NT. The MC145472 can be used in slave–slave applications. Refer to the complete MC145472 data book for further details.

SERIAL CONTROL PORT (SCP) INTERFACE

The MC145472 is equipped with an industry standard SCP Interface. The SCP is used by an external controller, such as an MC6805 family microcontroller, MC145488 Dual Data Link Controller, or MC68302 Integrated Multiprotocol Processor, to communicate with the U–Interface Transceiver.

The SCP is a full–duplex, four–wire interface with control and status information passed to and from the U–Interface Transceiver. The SCP Interface consists of a transmit output, a receive input, a data clock, and an enable signal. These device pins are known as SCP Tx, SCP Rx, SCP CLK, and $\overline{SCPEN}$, respectively. The SCP Clock determines the rate of exchange of data in both the transmit and receive directions, and the SCP Enable signal governs when this exchange is to take place. The four–wire SCP Interface is supplemented with an interrupt request line, $\overline{IRQ}$, for external microcontroller notification of an event requiring service.

The operation and configuration of the MC145472 is controlled by setting the state of its control registers and monitoring its status registers. The control, status, and M channel data registers reside in six 4–bit wide Nibble Registers, one 12–bit wide "Nibble Register", and sixteen 8–bit wide Byte Registers. Figures 11 and 12 are examples of how data is transferred over the SCP.

2B1Q INTERFACE

Figure 13 shows the recommended 2B1Q interface network for connection to the U–Interface and component specifications are shown in Table 8.

NOTE

Motorola continues to qualify several third party sources for the 2B1Q Interface transformer. Contact your local Motorola representative or the Motorola factory applications staff for the latest information regarding component sourcing.

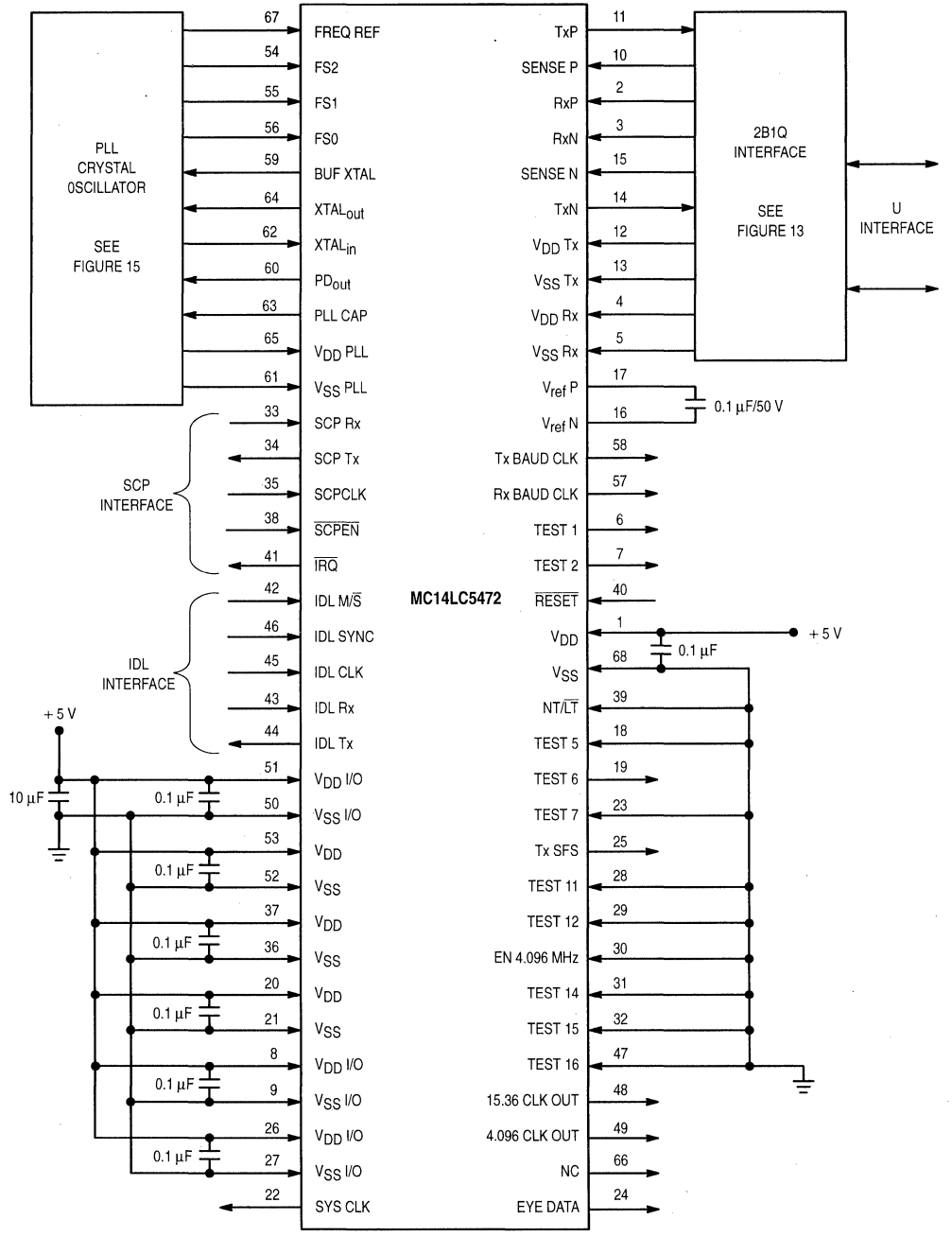


Figure 8. Typical LT Mode Connections

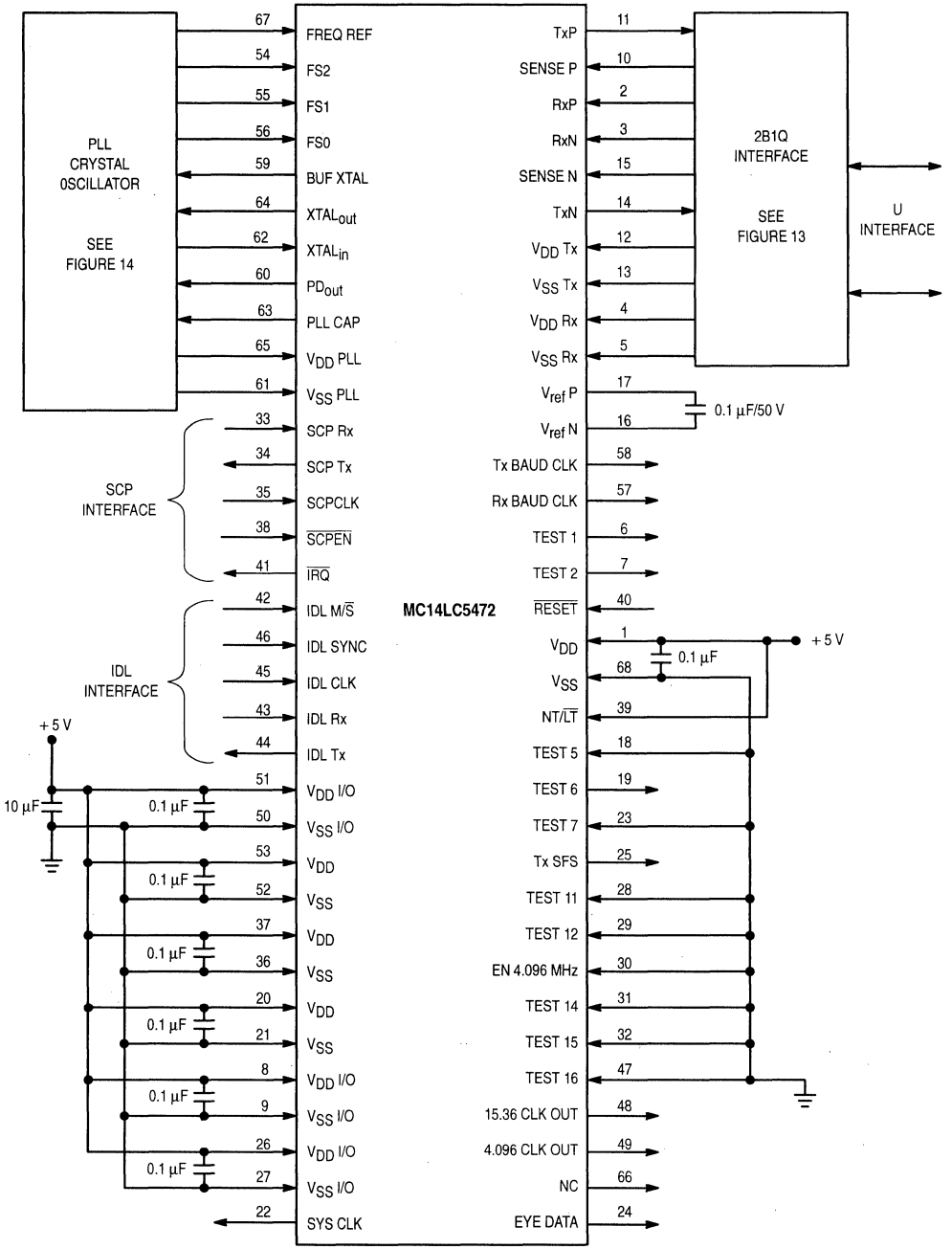
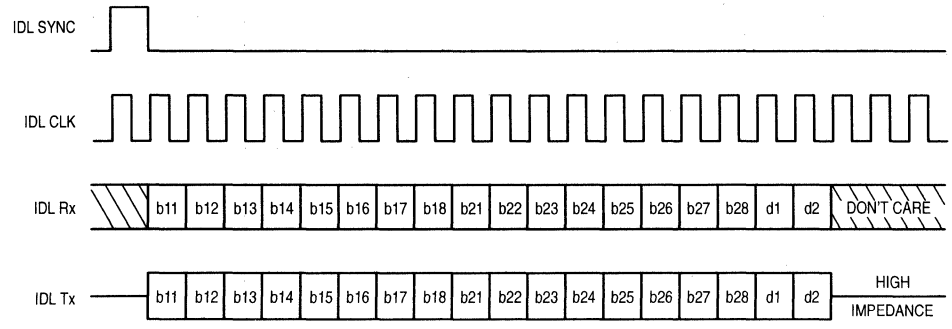
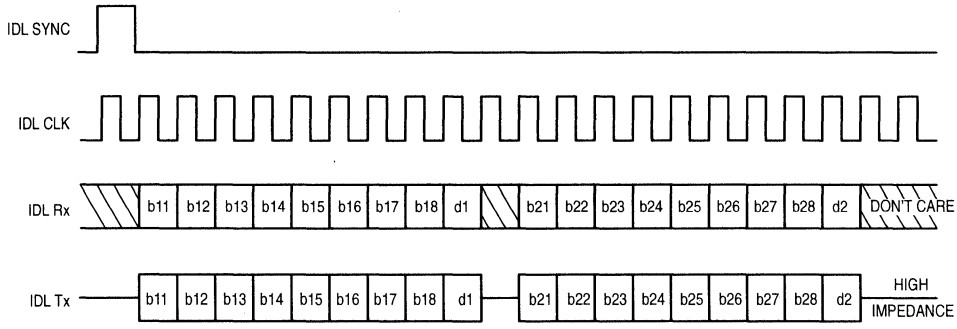


Figure 9. Typical NT Mode Connections



a. IDL Interface Timing in 8–Bit Mode



b. IDL Interface Timing in 10–Bit Mode

Figure 10. IDL Interface Data Formats

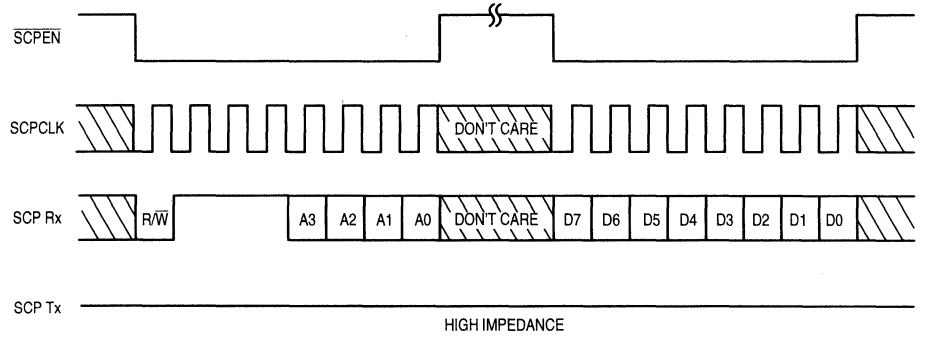


Figure 11. SCP Byte Register Write Operation Using Double 8–Bit Transfer

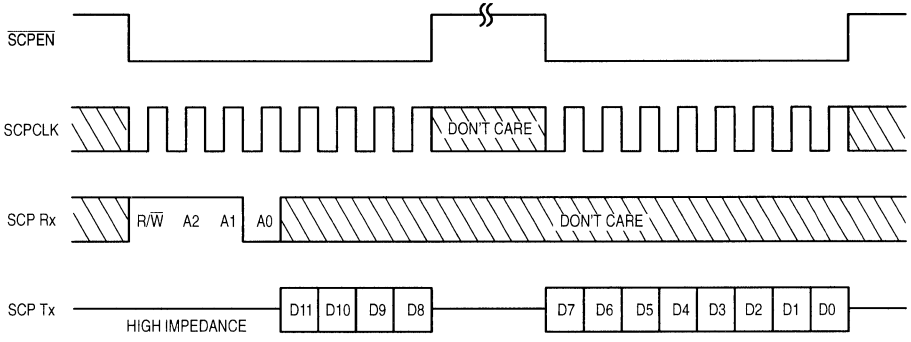


Figure 12. SCP Register R6 Read Operation

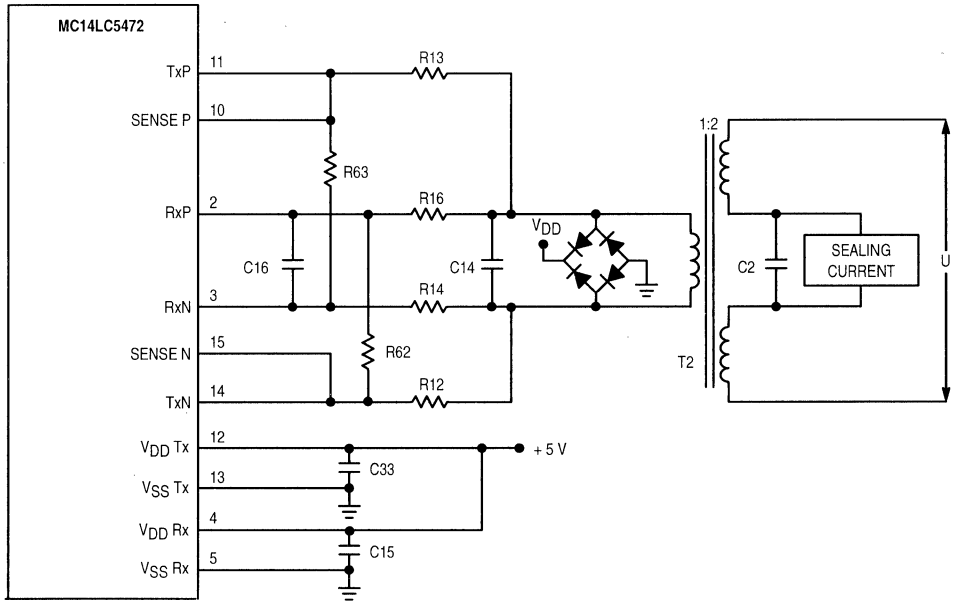


Figure 13. Typical 2B1Q Interface Schematic

Table 8. Line Interface Component Values

Component	Description
C2	1.0 µF, 100 V, 10%, low distortion capacitor
C14	0.033 µF, 50 V, 10%, low distortion capacitor
C15	0.1 µF ceramic, 50 V
C16	270 pF, or nearest commercial value, 10%, silver mica or other low distortion, high quality capacitor
C33	0.1 µF ceramic, 50 V
R12	14.3 Ω, 1%, metal film or other high quality low distortion resistor
R13	14.3 Ω, 1%, metal film or other high quality low distortion resistor
R14	1.00 kΩ, 1% metal film or other high quality low distortion resistor
R16	1.00 kΩ, 1% metal film or other high quality low distortion resistor
R62	1.69 kΩ, 1% metal film or other high quality low distortion resistor
R63	1.69 kΩ, 1% metal film or other high quality low distortion resistor
T2	Pulse transformer, 1:2 turns ratio
Diode Bridge	4 x 1N4001

NOTE: R12, R13, C14, and C16 are specific to Dale transformer part number PT–200–02. Motorola does not warrant this transformer, and in no way suggests that this is the only appropriate transformer.

Crystal Oscillator Or Phase–Locked Loop (PLL)

These pins provide access to the phase detector and crystal oscillator portions of the U–Interface Transceiver PLL. A 15.36 MHz and a 4.096 MHz clock output are available for other devices.

In the LT mode, the PLL synchronizes a 20.48 MHz crystal oscillator to one of eight possible reference frequencies supplied by the switching equipment. This phase–locked clock assures that the transmitted 2B1Q signal is synchronized to the frequency reference supplied at the FREQ REF pin. In addition, the very low frequency response (≈ 1 Hz) of the PLL loop filter limits jitter present in the frequency reference. Refer to Figures 14 and 15 for details of the loop filter network and voltage controlled crystal oscillator and Table 11 for suggested component values.

In the NT mode there is both an analog and a digital PLL. The analog PLL synchronizes the 20.48 MHz crystal oscillator to the recovered 2B1Q signal. The digital PLL synchronizes the IDL clock to the recovered 2B1Q signal and also updates the analog PLL on a regular basis. This ensures that the recovered timing is synchronized to the signal received from the LT. In NT mode the U–Interface Transceiver can lock to 80 kbaud ± 32 ppm receive signals when the recommended VCXO circuit is used.

The FREQ REF pin is a Schmitt–trigger digital input which provides the reference frequency for the phase–locked loop in LT mode. The eight possible frequencies include: 2.048, 2.560, 4.096, 7.680, 8.192, 10.24, 15.36, and 20.48 MHz.

The three frequency select inputs (FS0 – FS2) are used to select one of the eight possible reference frequencies which may be used to drive the Frequency Reference Input when the device is in the LT mode.

$XTAL_{in}$ and $XTAL_{out}$ are the oscillator pins. A 20.48 MHz pullable crystal and other components may be connected to $XTAL_{in}$ and $XTAL_{out}$ to form a voltage controlled crystal oscillator in the LT or NT modes.

PD_{out} is the output of the on–chip phase detector of the PLL. PD_{out} is a current source output of approximately 15 µA and connects to the PLL filter network.

PLL CAP must have a 0.1 µF capacitor connected between it and ground.

Clock Outputs

BUF XTAL is the buffered output from the 20.48 MHz oscillator and can be used to drive the $XTAL_{in}$ pin of other MC145472 devices in the same system. BUF XTAL must not be used as a microprocessor clock since it is turned off after a reset.

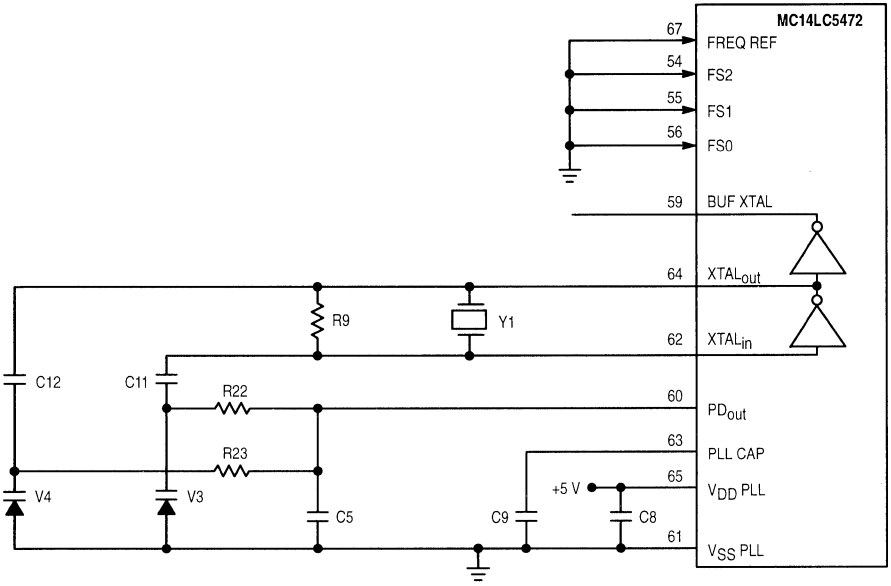
15.36 CLKOUT provides a buffered 15.36 MHz clock output that can be used for the MC145474/75 S/T transceiver clock. This clock is a 20.48 MHz clock with every fourth clock tick removed. Figure 16 shows the 15.36 MHz clock waveform. There may be applications where this clock is inadequate.

4.096 CLKOUT provides a buffered 4.096 MHz clock output that can be used for a microcontroller clock. The 4.096 Enable input, (Pin 30), must be high to enable this clock.

Test Pins

The following input pins are utilized by Motorola to test the functionality of the MC145472 during the manufacturing process. These pins should be connected to ground for normal operation:

TEST 5, TEST 7, TEST 11, TEST 12, TEST 14, TEST 15, and TEST 16



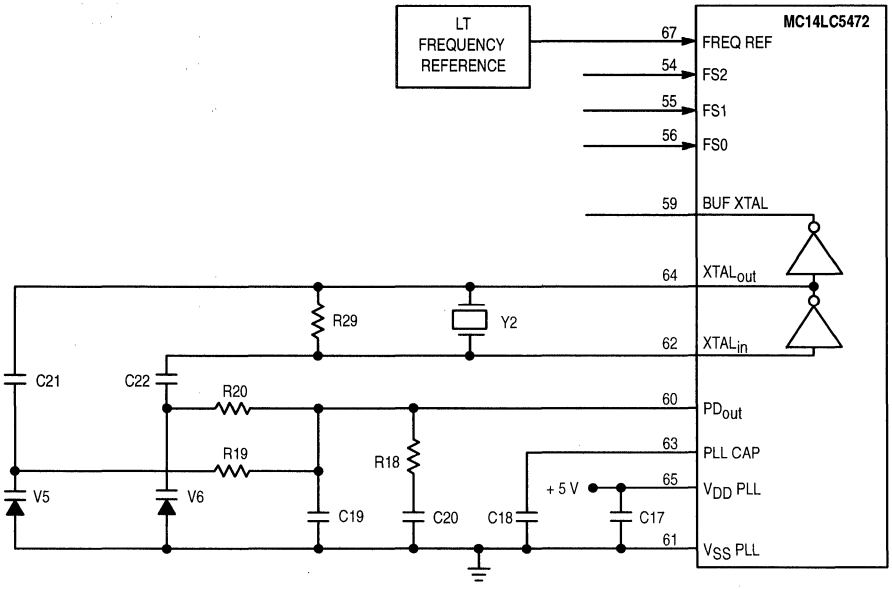
NOTE: See Table 9 for component values.

Figure 14. Typical NT Mode Voltage Controlled Crystal Oscillator Schematic

Table 9. NT Mode Crystal Oscillator Component Values

Component	Description
C5	0.1 µF ceramic, 50 V
C8	0.1 µF ceramic, 50 V
C9	0.1 µF ceramic, 50 V
C11, C12	0.01 µF to 0.1 µF ceramic, 50 V
R22, R23	270 kΩ, 5%
R9	0.5 MΩ to 1.5 MΩ, 5%
V3, V4	MV209 varactor. See complete MC145472 data book for sourcing and specification information.
Y1	20.48 MHz ± 40 ppm, 18 pF, pullable between 240 to 300 ppm over a capacitance range of 12 to 22 pF. See complete MC145472 data book for sourcing.

NOTE: V3, V4 may be combined into a single package.



NOTE: See Table 10 for component values.

Figure 15. Typical LT Mode PLL Crystal Oscillator Schematic

Table 10. LT Mode PLL Crystal Oscillator Component Values

Component	Description
C17	0.1 µF ceramic, 50 V
C18	0.1 µF ceramic, 50 V
C19	0.1 µF ceramic, 50 V
C20	See Table 11 for reference frequency dependent value.
C21	0.01 µF to 0.1 µF ceramic, 50 V
C22	0.01 µF to 0.1 µF ceramic, 50 V
R18	See Table 11 for reference frequency dependent value.
R19	270 kΩ, 5%
R20	270 kΩ, 5%
R29	0.5 MΩ to 1.5 MΩ, 5%
R_B	1 kΩ
R_C	47 kΩ
V5, V6	MV209 varactor diode. See complete MC145472 data book for sourcing and specification information.
Y2	20.48 MHz ± 40 ppm, 18 pF, pullable between 240 to 300 ppm over a capacitance range of 12 to 22 pF. See complete MC145472 data book for sourcing.

The following output pins are utilized by Motorola to test the functionality of the MC145472 during the manufacturing process. These pins should be left open circuit for normal operation.

TEST 1, TEST 2, TEST 6

SCP HIDOM

The MC145472 U–Interface Transceiver has the capability of forcing all outputs (both analog and digital) to the high impedance state. This feature, known as "the serial control port high impedance digital output mode" is provided to allow "in circuit" testing of other circuits or devices resident on the same PCB without requiring the removal of the MC145472.

TEST AND DEBUG

The MC145472 permits an external microcontroller to take control of the transmit framer by writing to control bits in Byte Register 8. This is very useful for debugging prototypes since the MC145472 can be forced to transmit a variety of signals regardless of the presence or lack of presence of a signal on the receive pins. Table 12 summarizes these signals and the control bits.

Table 11. LT PLL Frequency Select Options and Component Values

Reference Frequency (MHz)	FS2	FS1	FS0	R18 (Ω, 5%)	C20 (μF)
15.36	0	0	0	1800	150
10.24	0	0	1	910	330
8.192	0	1	0	2200	150
7.68	0	1	1	3300	100
4.096	1	0	0	2200	150
2.56	1	0	1	3300	100
2.048	1	1	0	3600	68
20.48	1	1	1	360	680

Table 12. Frame Control Modes

Frame Steering	Frame Control 2:0			Superframe Framer Mode of Operation	
b7	b6	b5	b4	NT	LT
1	0	0	0	SN0	SL0
1	0	0	1	Six frames of 10 kHz tone followed by SN1	SL1
1	0	1	0	SN2	SL2
1	0	1	1	SN3	SL3
1	1	0	0	10 kHz tone	
1	1	0	1	40 kHz tone	
1	1	1	0	Generates a single quat every basic frame which alternates over all four of the 2B1Q symbols.	
1	1	1	1	Superframe Framer free runs the scrambler with no synchronization words.	
0	Don't Care			The Superframe Framer output is determined by the state of the Automatic Activation Controller.	

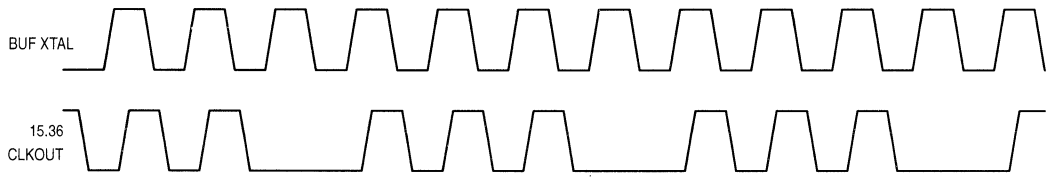


Figure 16. Waveform for 15.36 MHz Clock Output

SERIAL CONTROL PORT REGISTERS

INTRODUCTION

This section summarizes all of the MC145472 U–Interface Transceiver control and status registers available via the SCP Interface. Tables 13 through 15 summarize the registers.

The MC145472 SCP Interface is pin–for–pin identical to that of the MC145474/75 S/T–Interface Transceiver. Using the same interface as the MC145474/75 provides a common interface for applications utilizing both the MC145472 and the MC145474/75 such as an NT1 and for applications which can use either interface device such as line cards or terminal equipment.

In addition to being pin–for–pin compatible, the architecture of the nibble register map and the operation of the SCP Interface is similar to that of the MC145474/75. This is intended to simplify the code development effort and minimize device driver code size for a microcontroller.

See the MC145472 data book for a complete description of the bits in the register map.

The Register Map consists of six 4–bit Nibble Registers, one 12–bit Register, and sixteen 8–bit Byte Registers, designated as NR0 – NR5, R6 (see Tables 13 and 14), and BR0 – BR15 (see Table 15), respectively. Register R6 appears in the nibble register memory map but is a 12–bit register and is used to access the embedded operations channel.

NIBBLE REGISTER DESCRIPTIONS

This section briefly describes the U–chip nibble registers and their uses. The embedded operations channel register R6 appears in the nibble register map even though it is a 12–bit register.

NR0

This register contains read/write control bits. All bits are cleared on Hardware Reset ($\overline{\text{RESET}}$, Pin 40), but are unaffected by Software Reset (NR0(b3)). This register is write only when the U–Interface Transceiver is in Absolute Power–Down mode (NR0(b1)).

NR1

This register contains device activation status. All bits are cleared on Software Reset or Hardware Reset. If any bit in this register changes from 0 to a 1, or if Linkup, Superframe Sync, or Transparent/Activation in Progress change from a one to a zero, an IRQ 3 (NR3(b3)) is generated.

NR2

Register NR2 contains activation and deactivation control bits. All bits are cleared on Software Reset or Hardware Reset.

NR3

This is the interrupt status register. The register is read only. All bits are cleared on Software Reset or Hardware Reset. Each interrupt status bit in the register operates the same. If it is a 1, and its corresponding interrupt enable is a 1 in Register NR4, the $\overline{\text{IRQ}}$ pin on the chip will become active. IRQ 3 has the highest priority while IRQ 0 has the lowest.

NR4

This is the interrupt mask register. All bits are cleared on Software Reset or Hardware Reset. Each bit operates the same. For example, if bit Enable IRQ 1 is set to 1 by the external microcontroller and the IRQ 1 interrupt bit is set to 1 in NR3, the $\overline{\text{IRQ}}$ pin (Pin 41) becomes active.

NR5

This register contains control bits for the IDL Interface. More IDL controls are in Registers BR6 and BR7. All bits are cleared on Software Reset or Hardware Reset.

Table 13. Nibble Registers Map

	b3	b2	b1	b0
NR0	SOFTWARE RESET	POWER DOWN ENABLE	ABSOLUTE POWER DOWN	RETURN TO NORMAL
NR1	LINKUP	ERROR INDICATION	SUPERFRAME SYNC	TRANSPARENT/ACTIVATION IN PROGRESS
NR2	ACTIVATION REQUEST	DEACTIVATION REQUEST	SUPERFRAME UPDATE DISABLE	CUSTOMER ENABLE
NR3	IRQ 3	IRQ 2	IRQ 1	IRQ 0
NR4	ENABLE IRQ 3	ENABLE IRQ 2	ENABLE IRQ 1	ENABLE IRQ 0
NR5	RESERVED	BLOCK B1	BLOCK B2	SWAP B1/B2

Table 14. Register R6 Map

	b22	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
R6	eoc a1	eoc a2	eoc a3	eoc dm	eoc i1	eoc i2	eoc i3	eoc i4	eoc i5	eoc i6	eoc i7	eoc i8

Table 15. Byte Register Map, BR0 – BR15A

	b7	b6	b5	b4	b3	b2	b1	b0
BR0	M40	M41	M42	M43	M44	M45	M46	M47
BR1	M40	M41	M42	M43	M44	M45	M46	M47
BR2	M50	M60	M51	febe INPUT	RESERVED	RESERVED	RESERVED	RESERVED
BR3	M50	M60	M51	RECEIVED febe	COMPUTED nebe	VERIFIED act	VERIFIED dea	SUPERFRAME DETECT
BR4	febe COUNTER 7	febe COUNTER 6	febe COUNTER 5	febe COUNTER 4	febe COUNTER 3	febe COUNTER 2	febe COUNTER 1	febe COUNTER 0
BR5	nebe COUNTER 7	nebe COUNTER 6	nebe COUNTER 5	nebe COUNTER 4	nebe COUNTER 3	nebe COUNTER 2	nebe COUNTER 1	nebe COUNTER 0
BR6	U–LOOP B1	U–LOOP B2	U–LOOP 2B+D	U–LOOP TRANSPARENT	IDL–LOOP B1	IDL–LOOP B2	IDL–LOOP 2B+D	IDL–LOOP TRANSPARENT
BR7	BR15A SELECT	RESERVED	RESERVED	IDL INVERT	IDL FREE RUN	IDL SPEED	IDL M/S INVERT	IDL 8/10
BR8	FRAME STEERING	FRAME CONTROL 2	FRAME CONTROL 1	FRAME CONTROL 0	crc CORRUPT	MATCH SCRAMBLER	RECEIVE WINDOW DISABLE	NT/LT INVERT
	FRAME STATE 3	FRAME STATE 2	FRAME STATE 1	FRAME STATE 0	RESERVED	RESERVED	RESERVED	NT/LT MODE
BR9	eoc CONTROL 1	eoc CONTROL 0	M4 CONTROL 1	M4 CONTROL 0	M5/M6 CONTROL 1	M5/M6 CONTROL 0	febe/nebe CONTROL	RESERVED
BR10	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
BR11	ACTIVATION CONTROL 6	ACTIVATION CONTROL 5	ACTIVATION CONTROL 4	ACTIVATION CONTROL 3	ACTIVATION CONTROL 2	ACTIVATION CONTROL 1	ACTIVATION CONTROL 0	ACTIVATION TIMER DISABLE
	ACTIVATION STATE 6	ACTIVATION STATE 5	ACTIVATION STATE 4	ACTIVATION STATE 3	ACTIVATION STATE 2	ACTIVATION STATE 1	ACTIVATION STATE 0	ACTIVATION TIMER EXPIRE
BR12	ACTIVATION CONTROL STEER	INTERPOLATE ENABLE	LOAD ACTIVATION STATE	STEP ACTIVATION STATE	HOLD ACTIVATION STATE	JUMP SELECT	RESERVED	FORCE LINKUP
	EPI 18	EPI 17	EPI 16	EPI 15	EPI 14	EPI 13	EPI 12	EPI 11
BR13	ENABLE MEC UPDATES	ACCUM EC OUTPUT	ENABLE EC UPDATES	FAST EC BETA	ACCUM DFE OUTPUT	ENABLE DFE UPDATES	FAST DFE/ARC BETA	CLEAR ALL COEFF'S
	EPI 10	EPI 9	EPI 8	EPI 7	EPI 6	EPI 5	EPI 4	EPI 3
BR14	RESERVED	ro/wo TO r/w	RESERVED	FRAMER TO DEFRAMER LOOP	± 1 TONES	RESERVED	RESERVED	ENABLE CLKs
BR15	RESERVED	RESERVED	RESERVED	MASK 4	MASK 3	MASK 2	MASK 1	MASK 0
BR15A	FREQ ADAPT	JUMP DISABLE	RESERVED	RESERVED	ENABLE Tx SFS	ENABLE 15.36 MHz	ENABLE 20.48 MHz	ENABLE EYE DATA AND BAUD CLK
				RESERVED	RESERVED	RESERVED	RESERVED	RESERVED

R6

This register is 12 bits long to match the length of the eoc message. Operation of Register R6 depends on the setting of the eoc control bits in BR9(b7:b6) and BR14(b6). This register is double buffered.

In the default mode (BR14(b6) is 0), R6 performs as a read only/write only register. Data that is read from R6 by the external microcontroller is the eoc message that the Superframe Deframer stores according to the eoc Control register, BR9(b7:b6). Data that is written to R6 is stored in a latch contained in the Superframe Framer and is subsequently transmitted beginning on the next transmit eoc frame boundary. The Superframe Framer latches are set to ones on hardware or software resets.

BYTE REGISTER DESCRIPTIONS

This section briefly describes the U–chip byte registers and their uses.

BR0

This register contains the M4 channel bits that are framed and sent by the Superframe Framer. The bits that are written to this register are sent out on the next transmit superframe boundary. This register is double buffered. All bits are set to 1s following a Hardware Reset ($\overline{\text{RESET}}$, Pin 40) or Software Reset (NR0(b3)).

BR1

By reading this register, the external microcontroller obtains a buffered copy of the M4 bits that are parsed from the received superframe by the Superframe Deframer. The values in the register are valid when Superframe Sync, NR1(b1), is a one. BR1 is updated based on the mode set in Register BR9(b5:b4). This register is double buffered. The receive M4 channel byte can be read at any time during the Superframe prior to the next update.

BR2

This register contains the reserved M5 and M6 bits that are sent by the Superframe Framer. The bits that are written to the register are sent out on the next transmit superframe boundary, provided Superframe Updated Disable (NR2(b1)) is set to 0. All bits are set to 1s following a Hardware Reset or Software Reset. The febe input bit is used to indicate how the returning febe bit is calculated. Bits b7, b6, and b5 are double buffered. The state of the Reserved bits BR2(b3:b0) is inconsequential.

BR3

This register contains the ANSI T1.601–1992 reserved M5 and M6 bits that are received by the Superframe Deframer, occurring in basic frames 1 and 2 of the superframe, and four other Superframe Deframer status bits. The M5 and M6 values in the register are valid when the Superframe Sync bit (NR1(b1)) is a 1. M50, M51, and M60 are updated based on the mode set in Register BR9(b3:b2). Bits b7, b6, b5 are double buffered. They can be read at any time during the superframe prior to the next update.

BR4

This register contains the current febe count. The counter is not cleared by a software or hardware reset. The register can be preset to any value by writing to it. If the febe bit is active in a superframe, the counter will increment at the end of the received superframe. The count does not wrap around from FF to 00 The counter will not increment unless Superframe Sync (NR1(b1)) and Linkup (NR1(b3)) are both 1s.

BR5

This register contains the current nebe count. A nebe occurs whenever the received crc message does not match the computed crc or when Linkup (NR1(b3)) is a 1 and Superframe Sync (NR1(b1)) is a 0. Superframe timing to increment the nebe counter during times when Superframe Sync is a 0 is maintained by the Superframe Framer. The counter is not cleared by a software or hardware reset. The register can be preset to any value by writing to it. If the Superframe Deframer detects a crc error in the received superframe, the counter will increment at the end of that superframe. The count does not wrap around from FF to 00.

BR6

This register contains the loopback controls. Loopbacks can be directed towards the U–Interface or towards the IDL interface. For normal (no loopback) operation all bits should be 0. BR6 is cleared by a Software Reset, Hardware Reset, or when the Return to Normal bit (NR0(b0)) is set. When a bit is set to a 1 the appropriate loopback is enabled.

BR7

This register is used to configure the IDL interface. By setting bits in this register the IDL interface can be configured as master or slave, 8– or 10–bit data format, or the IDL clock rate can be selected when in master mode. BR7 is cleared on Hardware Reset or Software Reset. All bits in this register are read/write.

BR8

This register contains controls that are used for maintenance operations such as external loopbacks, Superframe Framer Control and State information, and NT/$\overline{\text{LT}}$ mode control. All write capable bits are cleared on a Software Reset or Hardware Reset. Bits b7 – b4, and b0, are read only/write only. To read the write only bits, it is necessary to set BR14(b6) to a one.

BR9

This register contains mode control over the Deframer's updating of the received maintenance bits. The register is cleared on Software Reset or Hardware Reset.

BR10

This register is RESERVED.

BR11

This register contains activation state and control data. All the bits are cleared on Hardware Reset and Software Reset. The register is a read only/write only register. Setting BR14(b6) to a 1 permits the external microcontroller to read back the write portion of the register.

BR12

This register is read only/write only. The write only portion controls the U–Interface Transceiver's Central Processing Unit (CPU) and activation controller. The read portion contains the eight most significant bits of the Error Power Indicator (EPI) register in the CPU. By setting BR14(b6) to a 1, the external microcontroller can read back the setting of the control bits. These bits are cleared on a Hardware Reset or Software Reset.

BR13

This register contains several bits that control the internal operation of the U–Interface Transceiver. These bits are cleared on a Hardware Reset or Software Reset.

BR14

This register is used for setting various diagnostic modes. This register is cleared on a Hardware Reset or Software Reset. When all of these bits are 0, the register map is in the default mode.

BR15

This register contains the revision number of the particular U–Interface Transceiver device in bits 0 – 4. BR15 is accessed by an SCP transfer when BR7(b7) is a 0 and the byte address in the SCP transfer is 15.

BR15A

This register is used to enable clock and test data outputs. All writeable bits in this register are cleared to 0 after a reset. BR15A is accessed by an SCP transfer when BR7(b7) is a 1 and the byte address in the SCP transfer is 15.

ACTIVATION AND DEACTIVATION

INTRODUCTION

Activation or start–up is the process that U–Interface Transceivers use to initiate a robust full–duplex communications channel. This process, which may be initiated from either the LT or the NT mode U–Interface Transceiver, is a well–defined sequence of procedures during which the training of the equalizers and echo cancelers at each end of the transmission line takes place. Two types of activation, cold start or warm start, may occur. The MC145472 is capable of automatically supporting both types.

Deactivation is the process used to gracefully end communication between the U–Interface Transceivers at each end of the transmission line. Only the LT mode U–Interface Transceiver may initiate a deactivation procedure.

The internal register set of the MC145472 is detailed in Tables 13 through 15.

ACTIVATION SIGNALS FOR NT MODE

When configured as an NT, the U–Interface Transceiver can transmit any of the signals shown in Table 16. The actual procedure undertaken by the device using these five signals is described later in this section.

ACTIVATION SIGNALS FOR LT MODE

When configured as an LT, the U–Interface Transceiver can transmit any of the signals shown in Table 17. The actual procedure undertaken by the device using these five signals is described later in this section.

Table 16. NT Mode Activation Signals

Information Station	Description
TN	A 10 kHz tone consisting of alternating four + 3 quats followed by four – 3 quats for a time period of 6 frames.
SN0	No signal transmitted.
SN1	Synchronization word present, no superframe synchronization word (ISW), and 2B+D+M = 1.
SN2	Synchronization word present, no superframe synchronization word (ISW), and 2B+D+M = 1.
SN3	Synchronization word present, superframe synchronization word (ISW) present. M channel bits active. Transmitted 2B+D data operational when M4 act bit = 1. When M4 act = 0, transmitted 2B+D data = 1.

Table 17. LT Mode Activation Signals

Information Station	Description
TL	A 10 kHz tone consisting of alternating four + 3 quats followed by four – 3 quats for a time period of 2 frames.
SL0	No signal transmitted.
SL1	Synchronization word present, no superframe synchronization word (ISW), and 2B+D+M = 1.
SL2	Synchronization word present, superframe synchronization word (ISW) present, 2B+D = 0, and M channel bits active.
SL3	Synchronization word present, superframe synchronization word (ISW) present. M channel bits active. Transmitted 2B+D data operational when M4 act bit = 1. When M4 act = 0, transmitted 2B + D data = 0.

ACTIVATION INITIATION

The U–Interface Transceiver can be activated in either of two ways. The external microcontroller can explicitly set the Activation Request bit, NR2(b3), to a 1 or the transceiver can detect an incoming 10 kHz wake–up tone from the far end.

An LT configured U–Interface Transceiver looks for an NT sending the TN wake–up tone. An NT configured U–Interface Transceiver looks for an LT sending the TL wake–up tone. In either case, Activation Request being set or a wake–up tone being detected, the U–Interface Transceiver proceeds with activation automatically and signals the result of the activation to the external microcontroller by setting status bits in NR1.

ACTIVATION INDICATION

The activation status is indicated in Nibble Register 1. This register indicates whether the MC145472 is not activated, is in the process of activating or fully activated. This register also is used to provide error status.

LT DEACTIVATION PROCEDURES

ANSI T1.601–1992 specifies that only the LT can deactivate the U–Interface. This is done in the MC145472 by setting Deactivation Request (NR2(b2)) to 1.

NT DEACTIVATION PROCEDURES

ANSI T1.601–1992 specifies that the NT cannot initiate deactivation. The MC145472 deactivates to a warm start condition when Deactivation Request (NR2(b2)) is set to 1 prior to the LT deactivating the U–Interface. This should be done in response to the M4 dea bit changing from a 1 to a 0 at the NT when the loop is active.

2

M CHANNEL BITS

The eoc, M4, M5, and M6 channel bits are available at the SCP Interface once activation has been attained. All of the maintenance channel bits appear in the register map of the MC145472. These bits can be programmed by an external microcontroller to operate as defined in the ANSI T1.601 specification. The MC145472 has several operating modes for the M channel bits including a mode that automatically implements the embedded operations channel function in NT mode. Due to the M channel bits being register accessible they can also be redefined for proprietary applications.

SCP INTERFACE INDICATION OF TRANSMIT STATES

The four SCP bits, FS3 – FS0 BR8(b7:b4), indicate the current state of the Superframe Framer. See Table 12 for frame control modes.

MAINTENANCE CHANNEL

INTRODUCTION

The MC145472 provides a very flexible interface to the 4 kbps Maintenance Channel (M channel) defined in ANSI T1.601–1992. The M channel consists of 48 bits sent by both the LT and NT configured U–Interface Transceivers during the course of a superframe. These 48 bits are divided into six channels designated M1 – M6, each consisting of eight bits per superframe. The Embedded Operations Channel (eoc) consists of M1, M2, and M3. The overhead bits, such as crc, febe, act, and dea, are contained in channels M4, M5, and M6.

An external microcontroller can read from or write to the M channel via the SCP Interface. Interrupts to an external microcontroller can be enabled when an eoc, M4, M5, or M6 channel register is updated. M channel registers can be configured to update when a new value is detected between successive superframes, when a bit changes, or when two or three successive superframes of a new value are detected. The M4 channel act bit (BR1(b7)) can also be configured to automatically enable or disable customer data when in NT or LT mode of operation. The M4 channel dea bit (BR1(b6)) can also be configured to automatically issue a deactivation request in NT mode of operation. The M channel registers are updated only when Superframe Sync (NR1(b1)) is set to 1.

Figures 17 and 18 detail Maintenance Channel interrupt times with respect to the U–Interface for both NT and LT modes.

EMBEDDED OPERATIONS CHANNEL (eoc)

The eoc consumes 2 kbps of the 4 kbps Maintenance Channel (M4 channel). The eoc channel is used by the central office (LT) to initiate maintenance operations at the NT. The MC145472 can be configured to automatically perform the standard ANSI T1.601 eoc operations when in NT mode. The MC145472 can also be configured to permit an external microcontroller to service eoc commands. This permits extensions of the eoc command set to be implemented as the ANSI T1.601 standard is changed or proprietary solutions can be implemented for non–ISDN applications. Byte Register BR9 is used to configure the operating mode of the eoc. An interrupt is generated when the eoc register R6 is updated and Enable IRQ 2 (NR4(b2)) is set to 1.

M4 CHANNEL

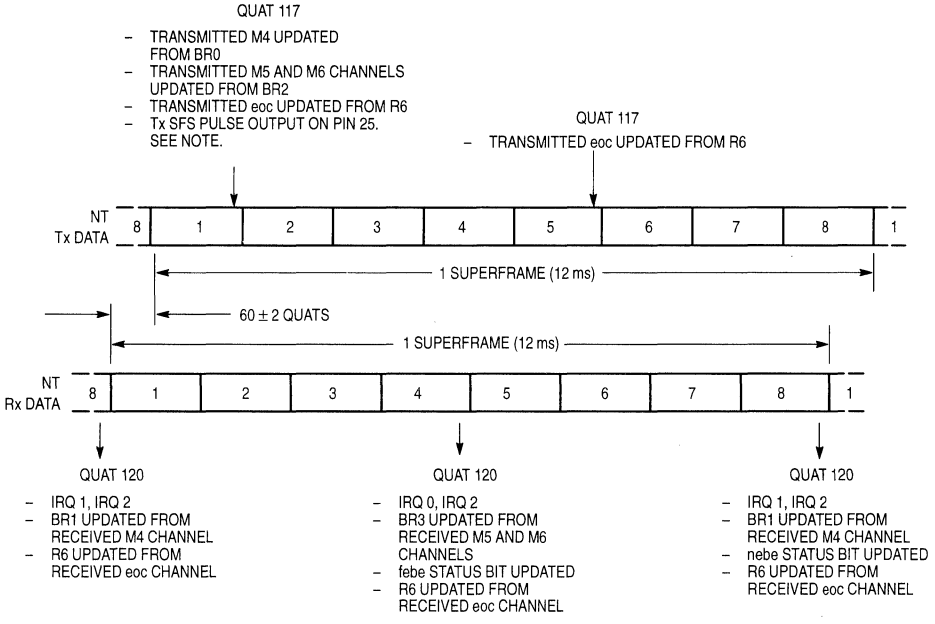
The M4 channel is used for signaling maintenance and system status between the NT and the LT. Typical information will be power status sent from the NT to the LT or the LT letting the NT know that the LT will deactivate the loop. The MC145472 provides four different modes that the M4 channel can operate in. A system designer can select whichever mode best fits the application. The received M4 data from the Superframe Deframer is available in BR0. The transmitted M4 channel data is written to Byte Register BR1. Byte Register BR9 is used to configure the operating mode of the M4 channel. An interrupt is generated when BR0 is updated and Enable IRQ 1, NR4(b1), is set to 1.

M5 AND M6 CHANNELS

The M5 and M6 channels are similar to the M4 channel. At this time the ANSI T1.601 specification defines all bits in these two channels as reserved bits. The MC145472 provides full access to these channels so they can be used in non–ISDN applications. The received M5 and M6 data from the Superframe Deframer is available in BR2. The transmitted M5/M6 channel data is written to Byte Register BR3. Register BR9 is used to configure the operating mode of the M5/M6 channels. These channels are configured as a pair. An interrupt is generated when BR2 is updated and Enable IRQ 0 (NR4(b0)) is set to 1.

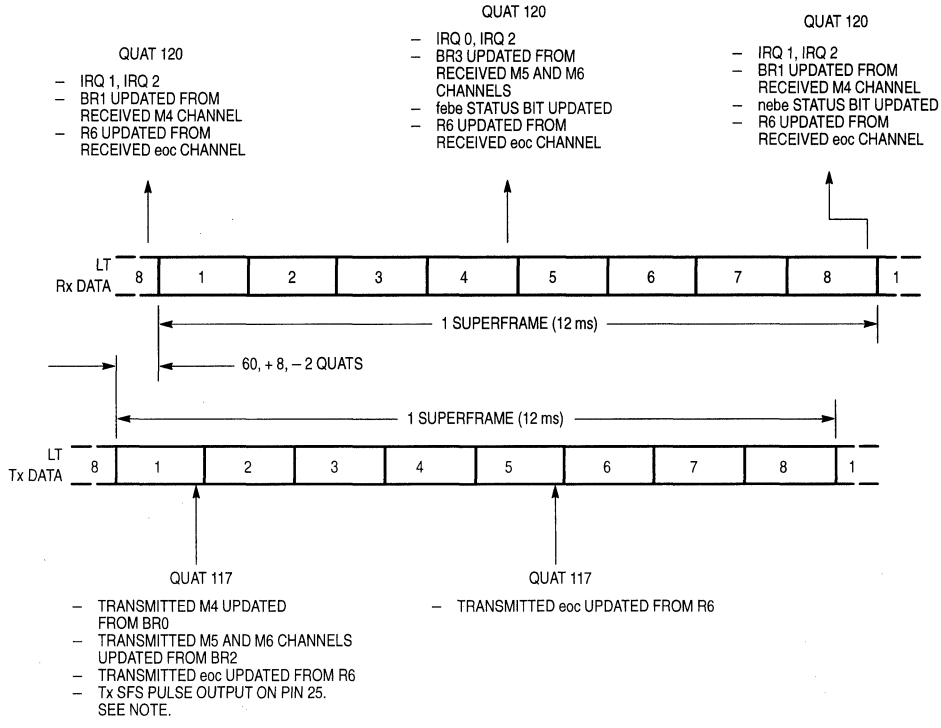
febe AND nebe BITS

The MC145472 has extensive febe (Far End Block Error) and nebe (Near End Block Error) maintenance capabilities. The state of the received computed nebe and of the received febe is available through the SCP Interface. Also, independent febe and nebe counters are available for performance monitoring purposes.



NOTE: Due to internal superframe delays the actual sync word marker on the TxP and TxN pins occurs 8 quats prior to the Tx SFS pulse. This causes the Tx SFS pulse to appear during Quat 113 at pin 25. Internal to the MC145472 the Tx SFS pulse is generated during Quat 117.

Figure 17. NT Mode Maintenance Channel Updates



NOTE: Due to internal superframe delays the actual sync word marker on the TxP and TxN pins occurs 8 quats prior to the Tx SFS pulse. This causes the Tx SFS pulse to appear during Quat 113 ± 1 at pin 25. Internal to the MC145472 the Tx SFS pulse is generated during Quat 117.

Figure 18. LT Mode Maintenance Channel Updates

LOOPBACK MODES

INTRODUCTION

The MC145472 U–Interface Transceiver supports four different loopback types, each having various modes. The four types are: 1) U–Interface Loopback, 2) IDL Interface Loopback, 3) Superframe Framer–to–Deframer Loopback, and 4) External Analog Loopback. Each of these loopback modes is selected by setting bits in the appropriate SCP register(s). Any combination of loopbacks may be invoked, including simultaneous loopbacks toward the U–interface and toward the IDL Interface. These loopbacks are available with transparency or non–transparency. "Transparent" means that a loopback passes the data on through to the other side as well as looping it back and "non–transparent" means that the data is blocked from being passed downstream and is replaced with the idle code (all 1s).

U–INTERFACE LOOPBACK

U–Interface Loopback is shown in Figure 19. As the shaded portion of the block diagram shows, this loopback mode exercises virtually the entire U–Interface Transceiver. 2B1Q symbols are received from the far end transmitter, recovered, passed through the IDL Interface block, and transmitted back to the far end receiver.

IDL INTERFACE LOOPBACK

IDL Interface Loopback is shown in Figure 20. As the shaded portion of the block diagram shows, this loopback mode takes B and D channel data in at the IDL Rx pin and sends the same data back out the IDL Tx pin.

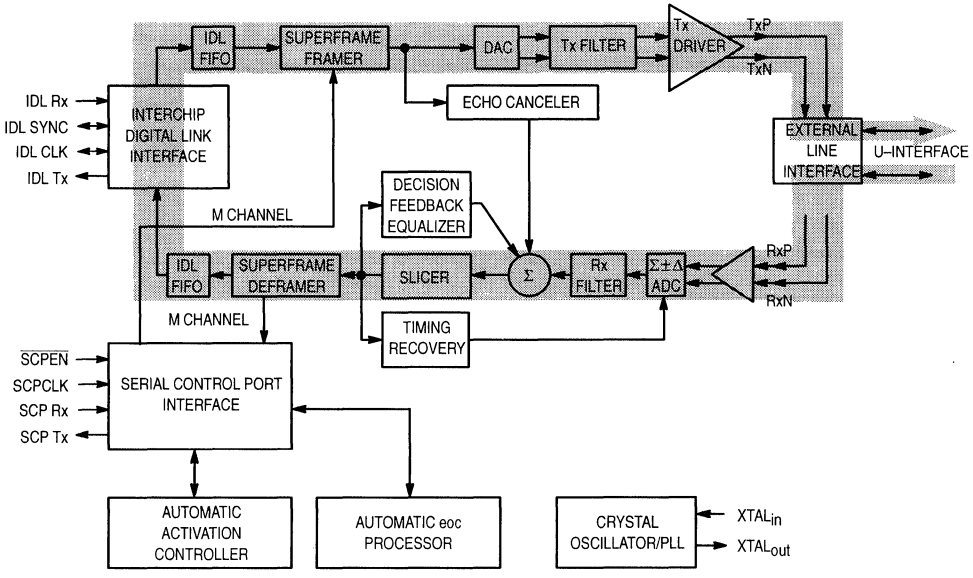


Figure 19. U–Interface Loopback Block Diagram

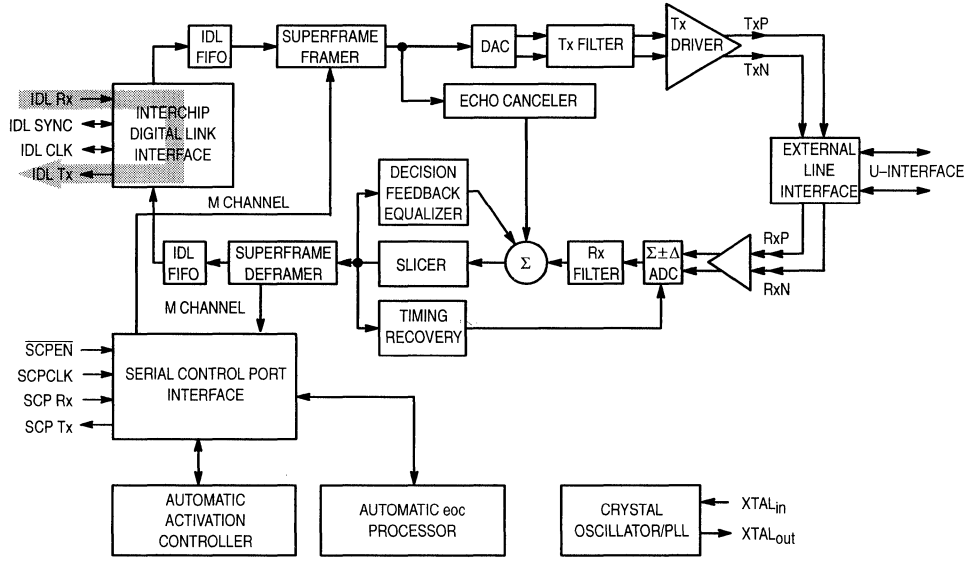


Figure 20. IDL Interface Loopback Block Diagram

Superframe Framer–to–Deframer Loopback

Superframe Framer–to–Deframer Loopback is shown in Figure 21. As the shaded portion of the block diagram shows, this loopback mode takes B and D channel data in at the IDL Rx pin and M channel data via the SCP, performs all of the superframe framing and subsequent deframing functions, and sends the same data back out the IDL Tx pin and SCP. This loopback mode is intended primarily for diagnostic purposes.

External Analog Loopback

External Analog Loopback is shown in Figure 22. As the shaded portion of the block diagram shows, this loopback mode takes B and D channel data in at the IDL Rx pin and transmits the data out the Tx Driver pins. The 2B1Q signal passes through the external line interface circuitry and back into the receiver input pins. The signal is then recovered and sent out the IDL Tx pin. Note that the external line interface has been physically disconnected from the U–Interface twisted wire pair.

Since the entire 2B1Q superframe is being looped back, loopback data includes the 2B+D channels and all of the M channels. For instance, data written by an external microcontroller to the eoc, M4, and M5/M6 registers, (R6, BR0, and BR2), is looped back and can be read from the eoc, M4, and M5/M6 registers, (R6, BR1, and BR3).

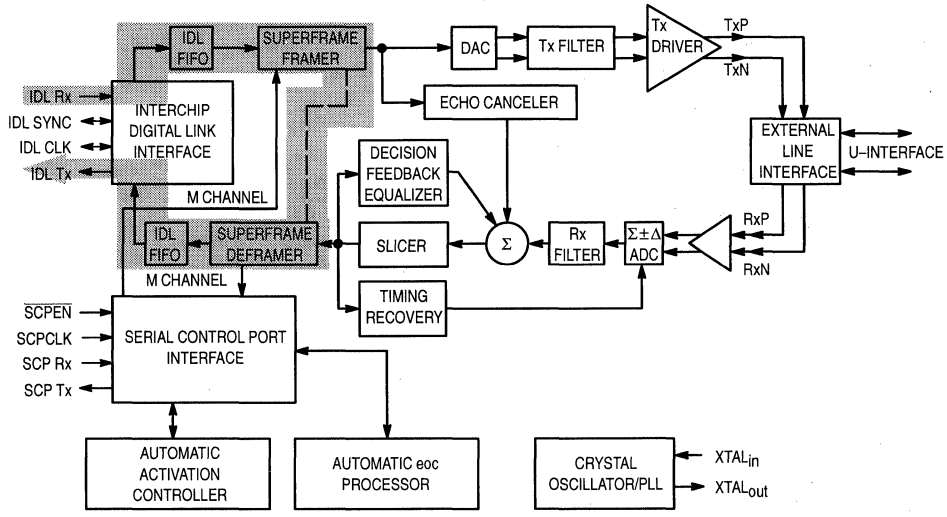


Figure 21. Superframe Framer–to–Deframer Loopback Block Diagram

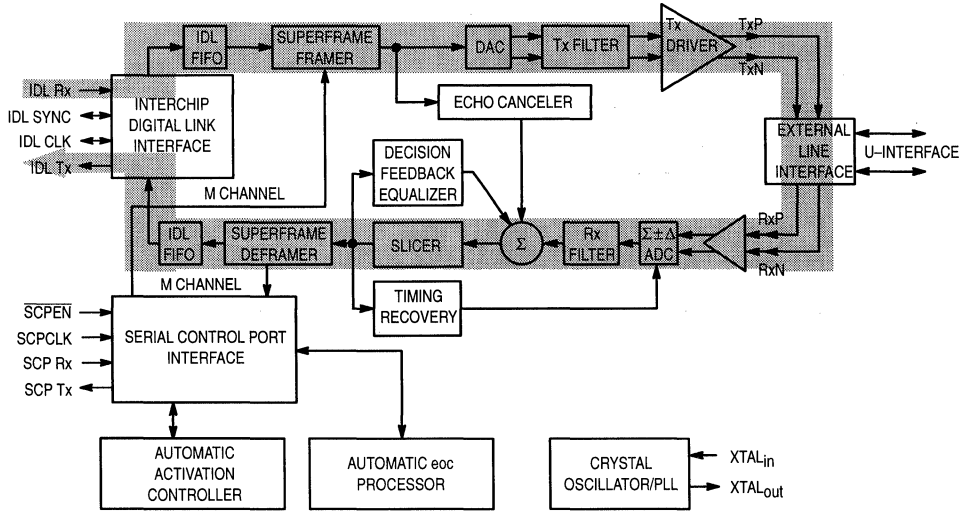


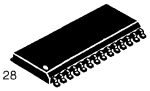
Figure 22. External Analog Loopback Block Diagram

MC145474
MC145475

Technical Summary

ISDN S/T-Interface Transceiver

P SUFFIX
PLASTIC DIP
CASE 736B



DW SUFFIX
SOG PACKAGE
CASE 751F

ORDERING INFORMATION

MC145474P	Plastic DIP
MC145475DW	SOG Package

This technical summary provides a brief description of the MC145474 and MC145475 S/T–Interface Transceivers. A complete data book for the MC145474/75 is available and can be ordered from your local Motorola Semiconductor Sales Office (order number MC145474/D).

The MC145474/75 ISDN S/T–Transceiver provides an economical VLSI Layer 1 interface for the transportation of two 64 kpbs B channels and one 16 kpbs D channel between the network termination or NT and terminal equipment applications or TEs. Both the MC145474 and the MC145475 conform to CCITT I.430 and ANSI TI.605 specifications.

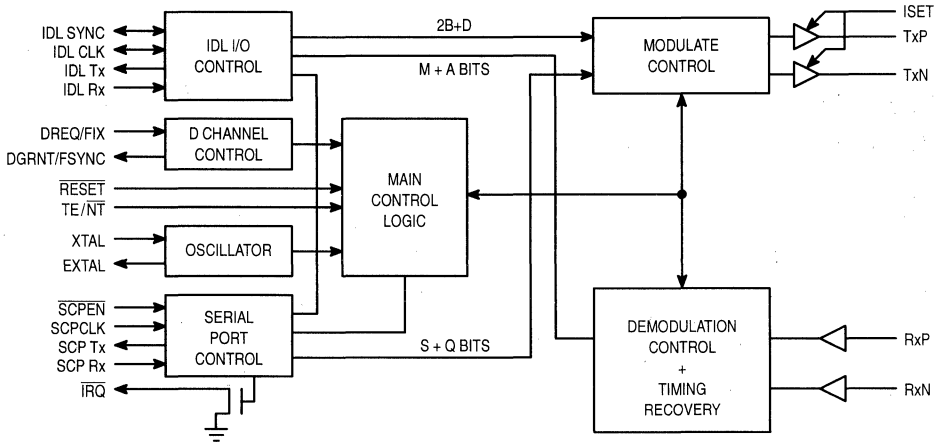
The MC145474/75 provides the modulation/line drive and demodulation/line receive functions required of the interface. In addition, the MC145474/75 provides the activation/deactivation, error monitoring, framing, bit, and octet timing. The MC145474/75 provides the control signals for the interface to the Layer 2 devices. Complete multiframe capability is provided.

The MC145474/75 features to Interchip Digital Link (IDL) for the exchange of 2B+D channel information between ISDN components and systems. The MC145474/75 provides an industry standard serial control port (SCP) to program the operation of the transceiver.

- Conforms to CCITT I.430 and ANSI T1.605 Specifications
- Detects Far–End Code Violations (FECVs) in the NT Mode
- Incorporates the IDL Interface
- Pin Selectable NT or TE Modes of Operation
- Industry Standard Microprocessor SCP Interface
- Supports 1:1 Transformers for Transmit and Receive
- Exceeds the Recommended Range of Operation in All Configurations
- Complete Multiframing Capability Supported (SC1 – SC5 and Q Channel)
- Optional B Channel Idle, Invert, or Exchange
- Supports Full Range of S/T and IDL Loopbacks
- Supports Transmit Power Down and Absolute Minimum Power Mode
- Supports Crystal or External Clock Input Modes
- MC145475 Bonded Out for NT1 Star Mode of Operation
- CMOS Design for Low Power Operation
- The MC14LC5494EVK May Be Used to Evaluate the MC145474

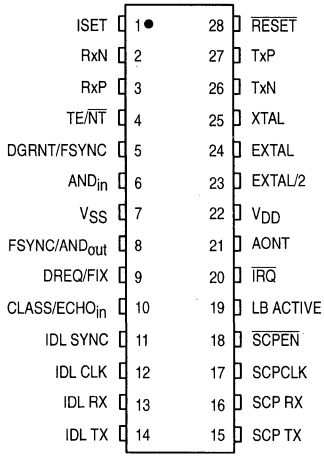
REV 2
8/95

BLOCK DIAGRAM

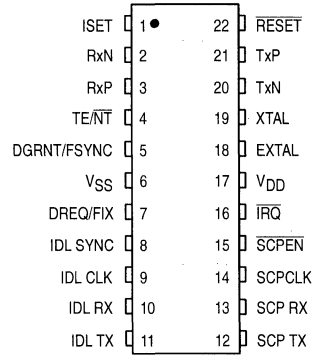


PIN ASSIGNMENTS

MC145475
SOG PACKAGE



MC145474
PLASTIC PACKAGE



ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{DD}	– 0.3 to + 7.0	V
Input Voltage (any pin to V_{SS})	V_{in}	– 0.3 to V_{DD} + 0.3	V
DC Current, any pin (excluding V_{DD}, V_{SS}, TxP, and TxN)	I	± 10	mA
Operating Temperature	T_A	– 40 to + 85	°C
Storage Temperature	T_{stg}	– 85 to + 150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electrical fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \ge V_{DD}$.

Reliability of operation is enhanced if unused digital inputs are tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

2

DIGITAL DC ELECTRICAL CHARACTERISTICS (CMOS MODE, BR13(6) = 0)

(T_A = – 40 to + 85°C, V_{DD} = 5.0 V ± 10%, Voltages referenced to V_{SS})

Characteristics	Symbol	Min	Max	Unit
Input High Voltage	V_{IH}	3.5	—	V
Input Low Voltage	V_{IL}	– 0.3	1.5	V
Input Leakage Current @ 5.5 V	I_{in}	—	5	µA
High–Impedance Input Current @ 4.5/0.5 V	$I_{lkg(Z)}$	—	10	µA
Input Capacitance	C_{in}	—	10	pF
Output High Voltage (I_{OH} = – 400 µA)	V_{OH}	2.4	—	V
Output Low Voltage (I_{OL} = 5.0 mA)	V_{OL}	—	0.5	V
XTAL Input High Level	$V_{IH(X)}$	3.5	—	V
XTAL Input Low Level	$V_{IL(X)}$	—	0.5	V
EXTAL Output Current (V_{OH} = 4.6 V)	$I_{OH(X)}$	—	– 400	µA
EXTAL Output Current (V_{OL} = 0.4 V)	$I_{OL(X)}$	—	400	µA
$\overline{IRQ}$ Output Low Current (V_{OL} = 0.4 V)		—	1.7	mA
$\overline{IRQ}$ Output Off–State Impedance		100	—	kΩ

DIGITAL DC ELECTRICAL CHARACTERISTICS (TTL MODE, BR13(6) = 1)

(T_A = – 40 to + 85°C, V_{DD} = 5.0 V ± 10%, Voltages referenced to V_{SS})

Characteristics	Symbol	Min	Max	Unit
Input High Voltage	V_{IH}	2.0	—	V
Input Low Voltage	V_{IL}	– 0.3	0.8	V

NOTE: The MC145474/75 can be programmed to accept TTL levels on all digital input pins (this does not include XTAL and EXTAL). The MC145474/75 is configured for TTL mode by writing a 1 to BR13(6). Programming the MC145474/75 for TTL mode has no effect on either the digital output pins, the crystal circuit, TxP/TxN, or RxP/RxN. Thus, the only dc electrical characteristics that differ, when operating in the CMOS mode, are the input voltages accepted on the digital inputs.

ANALOG CHARACTERISTICS (T_A = – 40 to + 85°C, V_{DD} = 5.0 V ± 10%, Voltages referenced to V_{SS})

Characteristics		Min	Typ	Max	Unit
TxP/TxN Drive Current	R_L = 50 Ω	13.5	15	16.5	mA
(TxP – TxN) Voltage Limit		—	—	1.17	V p–p
Input Amplitude (RxP – RxN)		35	—	—	mV p–p

POWER DISSIPATION (T_A = – 40 to + 85°C, V_{DD} = 5.0 V ± 10%, Voltages referenced to V_{SS})

Characteristics	Min	Typ	Max	Unit	Notes
DC Supply Voltage (V_{DD})	4.5	5.0	5.5	V	
Worst Case Power Consumption	—	—	175	mW	1
Transmit Power–Down (NR1(2) = 1)	—	—	75	mW	2
Absolute Minimum Power (NR1(1) = 1)	—	—	40	mW	2

NOTES:
1. The worst case power consumption occurs when the MC145474/75 is transmitting a 96 kHz test tone (BR11(0) = 1) into a 50 Ω load resistor. The 15.36 MHz clock is being provided by the crystal as depicted in Figure 1.
2. The power consumption figures for transmit power–down and absolute minimum power are both determined with the crystal circuit as depicted in Figure 1 still connected and operational.

2

IDL TIMING CHARACTERISTICS (NT MODE, IDL SLAVE) (T_A = – 40 to + 85°C, V_{DD} = 5.0 V ± 10%, Voltages referenced to V_{SS})

Ref. No.	Characteristics	Min	Max	Unit
1	Time Between Successive IDL SYNCs	Note 1		
2	IDL SYNC Active After IDL CLK Falling Edge (Hold Time)	30	—	ns
3	IDL SYNC Active Before IDL CLK Falling Edge (Setup Time)	30	—	ns
4	IDL CLK Period	Note 2		
5	IDL CLK Width High	70	—	ns
6	IDL CLK Width Low	70	—	ns
7	IDL Rx Valid Before IDL CLK Falling Edge (Setup Time)	30	—	ns
8	IDL Rx Valid After IDL CLK Falling Edge (Hold Time)	30	—	ns
9	IDL Tx Time to High Impedance	—	30	ns
10	IDL Tx High Impedance to Active State	—	70	ns
11	IDL CLK to IDL Tx Active	—	70	ns

NOTES:
1. IDL SYNC is an 8 kHz signal. The phase relationship between IDL SYNC and IDL CLK is as described earlier.
2. IDL CLK input frequency can be run at 1.536 MHz, 1.544 MHz, 2.046 MHz, 2.56 MHz, or 4.098 MHz.

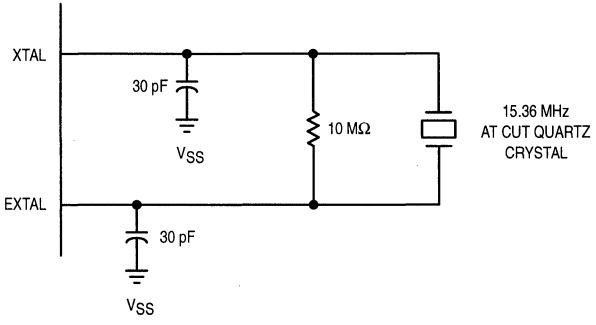


Figure 1. Crystal Circuit

IDL TIMING CHARACTERISTICS (NT MODE IDL MASTER OR TE MODE WITH THE IDL CLK RATE SET TO 2.56 MHz)

(T_A = – 40 to + 85°C, V_{DD} = 5.0 V ± 10%, Voltages referenced to V_{SS})

Ref. No.	Characteristics	Min	Max	Unit
1	Time Between Successive IDL SYNCs		Note 1	
2	IDL SYNC Active After IDL CLK Falling Edge (Hold Time)	160	230	ns
3	IDL SYNC Active Before IDL CLK Falling Edge (Setup Time)	160	230	ns
4	IDL CLK Period		Note 2	
5	IDL CLK Width High		Note 2	
6	IDL CLK Width Low		Note 2	
7	IDL Rx Valid Before IDL CLK Falling Edge (Setup Time)	30	—	ns
8	IDL Rx Valid After IDL CLK Falling Edge (Hold Time)	30	—	ns
9	IDL Tx Time to High Impedance	0	30	ns
10	IDL Tx High Impedance to Active State	—	45	ns
11	IDL CLK to IDL Tx Active	—	45	ns

NOTES:
1. IDL SYNC is an 8 kHz signal. The phase relationship between IDL SYNC and IDL CLK is as described earlier.
2. In NT Mode IDL Master or TE Mode, the IDL CLK is generated internally in the MC145474/75. When configured for 2.56 MHz operation, IDL CLK is the crystal frequency divided by 6 and has a 50% duty cycle.

IDL TIMING CHARACTERISTICS (NT MODE IDL MASTER OR TE MODE WITH THE IDL CLK RATE SET TO 2.048 MHz)

(T_A = – 40 to + 85°C, V_{DD} = 5.0 V ± 10%, Voltages referenced to V_{SS})

Ref. No.	Characteristics	Min	Max	Unit
1	Time Between Successive IDL SYNCs		Note 1	
2	IDL SYNC Active After IDL CLK Falling Edge (Hold Time)	210	280	ns
3	IDL SYNC Active Before IDL CLK Falling Edge (Setup Time)	210	280	ns
4	IDL CLK Period		Note 2	
5	IDL CLK Width High		Note 2	
6	IDL CLK Width Low		Note 2	
7	IDL Rx Valid Before IDL CLK Falling Edge (Setup Time)	30	—	ns
8	IDL Rx Valid After IDL CLK Falling Edge (Hold Time)	30	—	ns
9	IDL Tx Time to High Impedance	0	30	ns
10	IDL Tx High Impedance to Active State	—	45	ns
11	IDL CLK to IDL Tx Active	—	45	ns

NOTES:
1. IDL SYNC is an 8 kHz signal. The phase relationship between IDL SYNC and IDL CLK is as described earlier.
2. In NT Mode IDL Master or TE Mode, the IDL CLK is generated internally in the MC145474/75. When configured for 2.048 MHz operation, IDL CLK is the crystal frequency divided by 7.5 and has a 53.3% duty cycle.

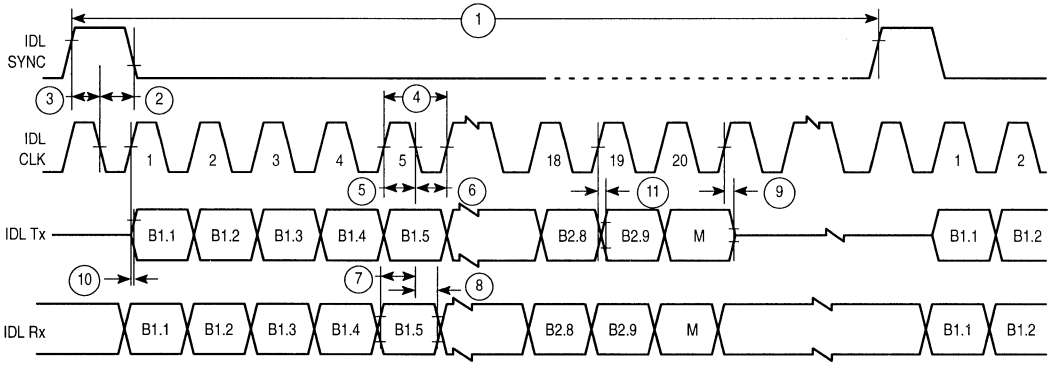
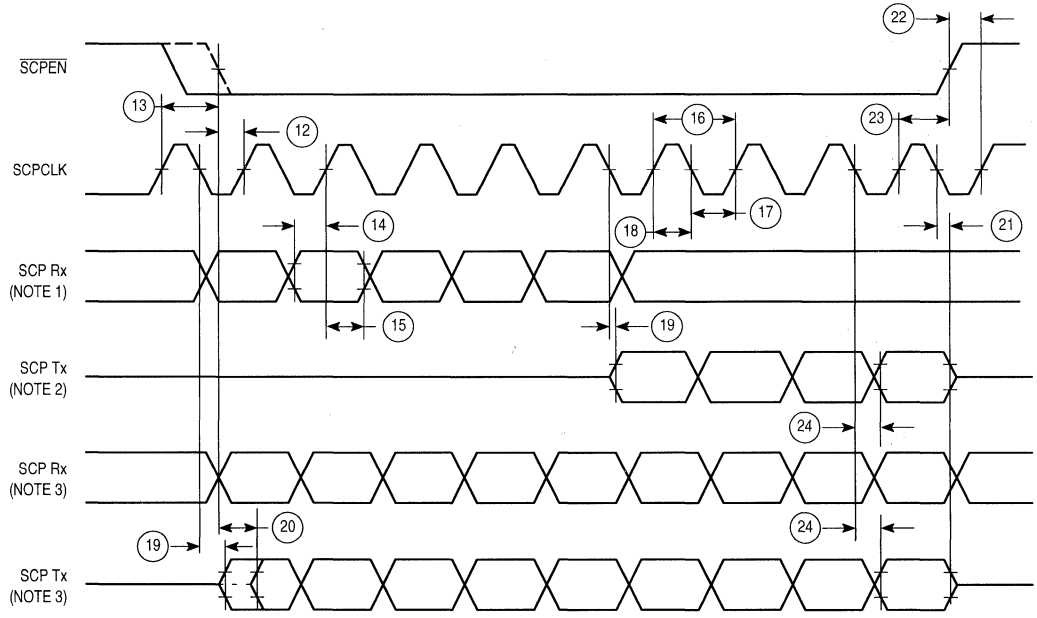


Figure 2. IDL Timing Characteristics

SCP TIMING CHARACTERISTICS

Ref. No.	Characteristics	Min	Max	Unit
12	$\overline{\text{SCPEN}}$ Active Before Rising Edge of SCPCLK	50	—	ns
13	SCPCLK Rising Edge Before $\overline{\text{SCPEN}}$ Active	50	—	ns
14	SCP Rx Valid Before SCPCLK Rising Edge (Setup Time)	35	—	ns
15	SCP Rx Valid After SCPCLK Rising Edge (Hold Time)	20	—	ns
16	SCPCLK Period (See Note 1)	244	—	ns
17	SCPCLK Width (Low)	30	—	ns
18	SCPCLK Width (High)	30	—	ns
19	SCP Tx Active Delay	0	50	ns
20	$\overline{\text{SCPEN}}$ Active to SCP Tx Active	0	50	ns
21	SCPCLK Falling Edge to SCP Tx High Impedance	—	30	ns
22	$\overline{\text{SCPEN}}$ Inactive Before SCPCLK Rising Edge	50	—	ns
23	SCPCLK Rising Edge Before $\overline{\text{SCPEN}}$ Active	50	—	ns
24	SCPCLK Falling Edge to SCP Tx Valid Data	0	50	ns

NOTE:
1. Maximum SCPCLK frequency is 4.096 MHz.



NOTES:
1. During a nibble read, four bits are presented on SCP Rx.
2. During a nibble read, SCP Tx will be active for the duration of the 4–bit transmission as shown.
3. A byte transaction consists of two 8–bit exchanges. During the first exchange, whether a read or a write, 8 bits (the byte register address) are presented on SCP Rx. In the second exchange, 8 bits are presented on SCP Tx during a byte read. During a byte write, the second exchange consists of 8 bits presented to SCP Rx.

Figure 3. SCP Timing Characteristics

NT1 STAR MODE TIMING CHARACTERISTICS

Ref. No.	Characteristics	Min	Max	Unit
25	Propagation Delay from AND_{in} to AND_{out}, while receiving INFO 0	—	30	ns

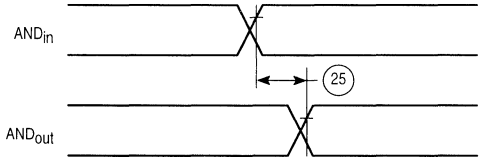


Figure 4. NT1 Star Mode

D CHANNEL TIMING CHARACTERISTICS (TE Mode)

Ref. No.	Characteristics	Min	Max	Unit
26	DREQ Valid Before Falling Edge of IDL SYNC	30	—	ns
27	DREQ Valid After Falling Edge of IDL SYNC	30	—	ns
28	DGRNT Valid Before Falling Edge of IDL SYNC	390	—	ns

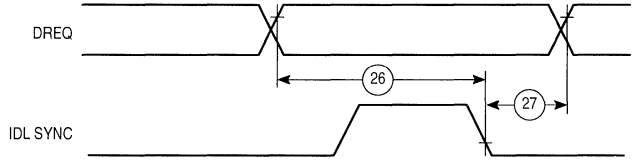


Figure 5. D Channel Timing

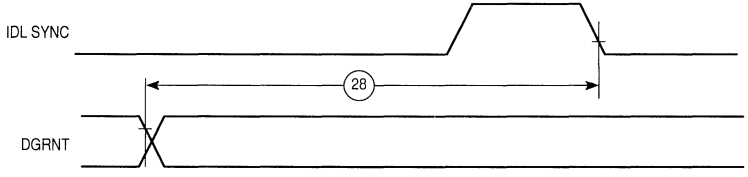


Figure 6. D Channel Timing

PIN DESCRIPTIONS

ISET
Current Set

A current programming resistor is connected between this pin and ground.

RxP, RxN
Receive Positive, Receive Negative

The S/T–Interface pseudo–ternary signal is input through these pins.

2

TE/$\overline{NT}$
Terminal Equipment/Network Termination

This pin is an input and selects the TE or NT mode of operation.

DGRANT/FSYNC
D Channel Grant/Frame Synchronization

This pin is a dual function output and operates as DGRANT when TE mode is selected, and FSYNC when NT mode is selected.

DGRANT: The DGRANT output is asserted when the MC145474/75 has determined that it can access the D channel.

FSYNC: FSYNC is asserted when the MC145474/75 has achieved frame synchronization.

AND_{in}
NT1 Star Mode D Channel AND Gate Input

This pin is an input to the MC145475 and is used in NT1 star mode.

V_{SS}
Negative Power Supply

This pin is the most negative power supply pin and digital logic ground. It is normally 0 V.

FSYNC/AND_{out}
Frame Synchronization/
NT1 Star D Mode Channel AND Gate Output

This pin is a dual function output and operates as FSYNC when TE mode is selected and AND_{out} when NT mode is selected. This pin is available only on the MC145475.

FSYNC: FSYNC is asserted when the MC145475 has achieved frame synchronization.

AND_{out}: This pin is an output from the MC145475 and is used in NT1 star mode.

DREQ/FIX
D Channel Request/
Fixed/Adaptive Timing Select

This pin is a dual function input and operates as DREQ when TE mode is selected and FIX when NT mode is selected.

DREQ: The DREQ input should be asserted when access to the D channel is desired

FIX: This input is used to select fixed or adaptive timing mode in an NT configured MC145474/75.

CLASS/$ECHO_{in}$
D Channel Class Selection/
NT1 Star Mode Echo Channel Input

This pin is a dual function input and operates as CLASS when TE mode is selected and $ECHO_{in}$ when NT mode is selected. This pin is available only on the MC145475.

CLASS: This pin selects the desired class or priority to be used when transmitting data on the D channel.

$ECHO_{in}$: This pin is an input to the MC145475 and is used in NT1 star mode.

IDL SYNC
IDL Frame Synchronization Signal

The 8 kHz IDL frame synchronization signal is transmitted or received through this pin. When the MC145474/75 is operating as an IDL slave, this pin is an input to the device. Conversely, when the device is operating as an IDL master, this pin is an output.

IDL CLK
IDL Clock Signal

The IDL clock signal is transmitted through this pin. When the MC145474/75 is operating as an IDL slave, this pin is an input to the device. Conversely, when the device is operating as an IDL master, this pin is an output.

IDL Rx
IDL Receive Input

This pin is an input to the MC145474/75. 2B+D data is received through this pin and then modulated onto the S/T–Interface.

IDL Tx
IDL Transmit Output

This pin is an output from the MC145474/75. Demodulated 2B+D data from the S/T–Interface is transmitted through this pin.

SCP Rx
SCP Receive Input

The serial control port receive line is used to input control, status, and data information into the MC145474/75 S/T–Transceiver.

SCP Tx
SCP Transmit Output

The serial control port (SCP) transmit line is used to output control, status, and data information from the MC145474/75 S/T–Transceiver.

SCPCLK
SCP Clock Signal

The serial control port clock is used to clock control, status, and data information into and out of the MC145474/75 S/T–Transceiver.

$\overline{SCPEN}$
SCP Enable Signal

This signal when held low selects the SCP for the transfer of control, status, and data information into and out of the MC145474/75 S/T–Transceiver.

LB ACTIVE
Loopback Active

This pin is always an output from the device. If any of the loopbacks are invoked, or any combination of the loopbacks are invoked, then this pin will be held high.

$\overline{IRQ}$
Interrupt Request Line

The interrupt request active low pin is an active low open drain output used to signal MPU or MCU devices that an interrupt condition exists in the MC145474/75 S/T–Transceiver.

AONT
Active Only NT

This pin is always an input to the device. The active only NT feature is applicable only to the NT mode of operation and is available as an output pin on the MC145475 and as an SCP control bit (BR7(6)) in both versions of the device.

V_{DD}
Positive Power Supply

This pin is the positive power supply input to the MC145474/75 and is 5.0 V ± 10% with respect to V_{SS}.

XTAL/2
7.68 MHz Clock Output

This pin is always an output from the device. The MC145474/75 S/T–Transceiver's 15.36 MHz clock is internally divided by two and the output of this divider (7.68 MHz) presents itself on the XTAL/2 pin.

XTAL and EXTAL
Crystal Input and Crystal Output

The MC145474/75 S/T–Transceiver requires a 15.36 MHz clock source for operation. This can be provided by a 15.36 MHz resonant crystal circuit using XTAL and EXTAL as the terminals of the circuit, or an external 15.36 MHz clock source can be input to the device via the XTAL pin. An inverter is internally connected between XTAL and EXTAL with XTAL as the input to the inverter and EXTAL as the output.

TxP, TxN
Transmit Positive, Transmit Negative

These pins act as differential current limited voltage source drive pairs for creating the logical line signals.

$\overline{RESET}$
MC145474/75 Reset

When low, a hardware reset is applied to the MC145474/75.

WIRING CONFIGURATIONS

INTRODUCTION

The MC145474/75 ISDN S/T–Transceiver conforms to CCITT I.430 and ANSI T1.605 specifications. It is a Layer 1 S/T–Transceiver designed for use at the S and T reference points. It is designed for both point–to–point and multipoint operation. The S/T–Transceiver is designed for use in either the network terminating (NT) mode or in terminal equipment (TE) applications. Two 64 kpbs B channels and one 16 kpbs D channel are transmitted in a full–duplex fashion across the interface.

Suggested wiring configurations follow. These configurations are deemed to be the most common but by no means the only wiring configurations. Note that when operating in the TE mode, only one TE has the 100 Ω termination resistors in the transmit and receive paths. Figures 7 through 10 illustrate where to connect the termination resistors for the described loop configurations.

POINT–TO–POINT OPERATION

In the point–to–point mode of operation one NT communicates with one TE. As such, 100 Ω termination resistors must be connected across the transmit and receive paths of both the NT and TE transceivers. Figure 7 illustrates this wiring configuration.

When using the MC145474/75 in this configuration, the NT must be in adaptive timing. This is accomplished by holding the DREQ/FIX pin low (i.e., connecting it to VSS). CCITT I.430 and ANSI T1.605 specify that the S/T–Transceiver must be able to operate up to a distance of 1 km in the point–to–point mode. This is the distance D1, shown in Figure 7.

SHORT PASSIVE BUS OPERATION

The short passive bus is intended for use when up to eight TEs are required to communicate with one NT. TEs can be distributed at any point along the passive bus, the only requirement being that the termination resistors be located at the end of the passive bus. Figure 8 illustrates this wiring configuration. CCITT I.430 and ANSI T1.605 specify a maximum operational distance from the NT of 200 meters. This corresponds to the distance D2, as shown in Figure 8.

EXTENDED PASSIVE BUS OPERATION

A wiring configuration whereby the TEs are restricted to a grouping at the far end of the cable, distant from the NT, is shown as the "Extended Passive Bus." This configuration is as illustrated in Figure 9. The termination resistors are to be positioned as illustrated in the diagram.

The essence of this configuration is that a restriction is placed on the distance between the TEs. The distance D3, as illustrated in Figure 9, corresponds to the maximum distance between the grouping of TEs. CCITT I.430 and ANSI T1.605 specify a distance of 25 to 50 meters for the separation between the TEs, and a distance of 500 meters for the total length. These distances correspond to the distances D3 and D4, as shown in Figure 9.

Note that the "NT configured" MC145474/75 should be placed in the adaptive timing mode for this configuration. This is achieved by holding the DREQUEST/FIX pin low.

BRANCHED PASSIVE BUS OPERATION

A wiring configuration which has somewhat similar characteristics to those of the "Extended Passive Bus" is known as the "Branched Passive Bus" and is illustrated in Figure 10. In this configuration the branching occurs at the end of the bus. The branching occurs after a distance D1 from the NT. The distance D5 corresponds to the maximum separation between the TEs.

NT1 STAR MODE OF OPERATION

A wiring configuration which may be used to support multiple T interfaces is known as the "NT1 Star Mode of Operation." This mode of operation is supported by the MC145475. This mode is described later. Note that the NT1 Star mode contains multiple NTs. Each of these NTs can be connected to either a passive bus (short, extended, or branched) or to a single TE.

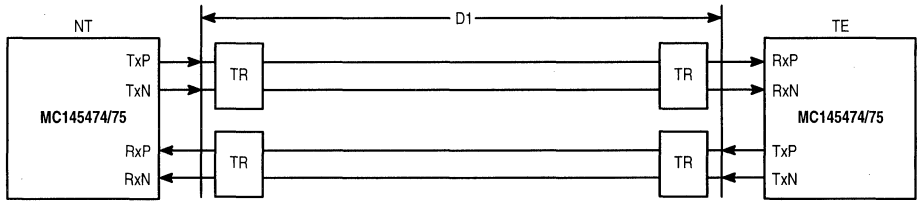


Figure 7. Point–to–Point

2

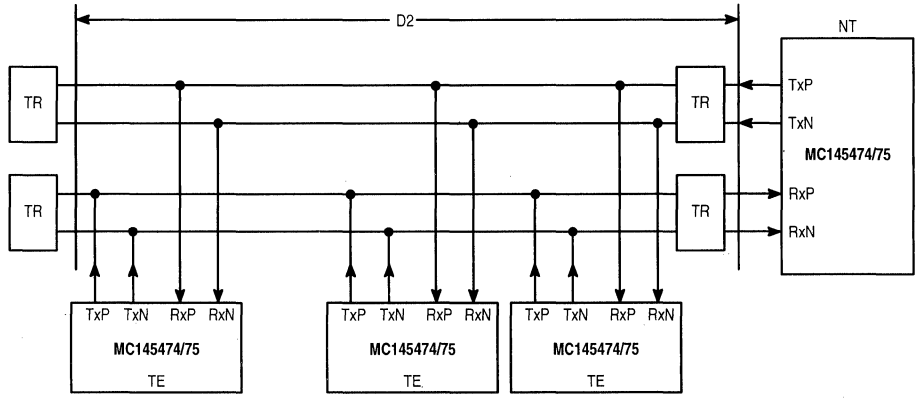


Figure 8. Short Passive Bus

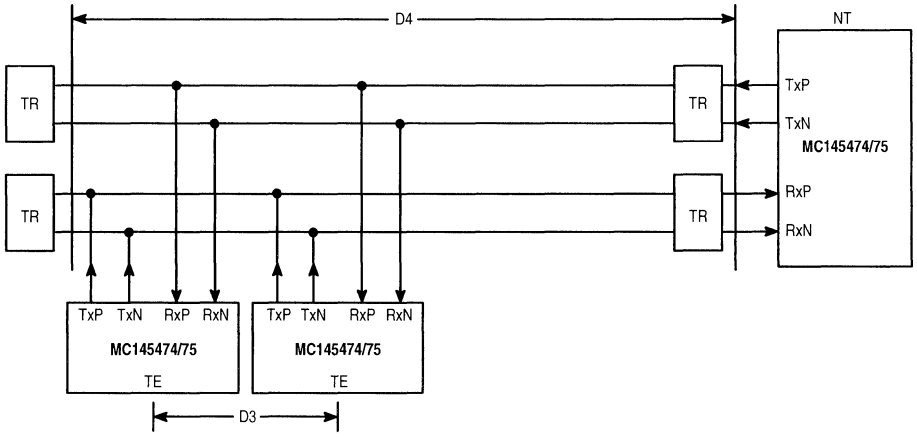


Figure 9. Extended Passive Bus

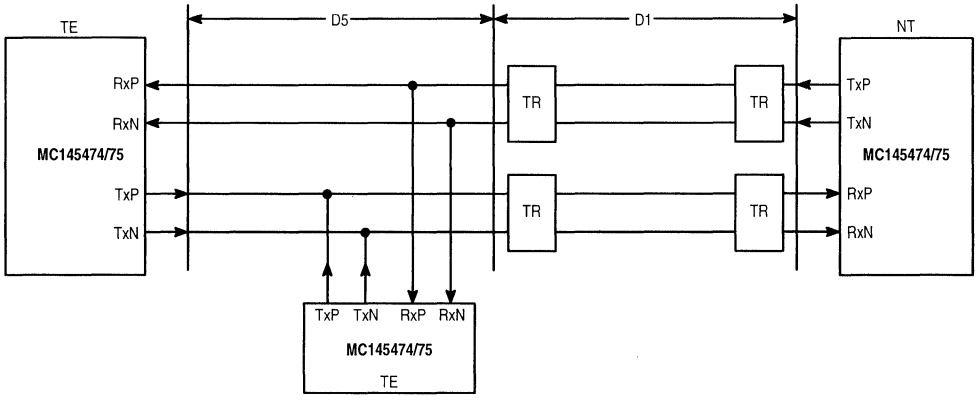


Figure 10. Branched Passive Bus

ACTIVATION/DEACTIVATION OF S/T–TRANSCEIVER

INTRODUCTION

CCITT I.430 and ANSI T1.605 define five information states for the S/T–Transceiver. When the NT is in the fully operational state it transmits INFO 4. When the TE is in the fully operational state it transmits INFO 3. INFO 1 is transmitted by the TE when it wants to wake up the NT. INFO 2 is transmitted by the NT when it wants to wake up the TE, or in response to the TEs transmitted INFO 1. These states cause unique patterns of symbols to be transmitted over the S/T–Interface. Only when the S/T loop is in the fully activated state are the 2B+D channels of data transmitted over the interface.

2

TRANSMISSION STATES FOR NT MODE S/T TRANSCEIVER

When configured as an NT, an S/T–Transceiver can be in any of the following transmission states shown in Table 1.

Table 1. NT Mode Transmission States

Information State	Description
INFO 0	The NT transmits 1s in every bit position. This corresponds to no signal being transmitted.
INFO 2	The NT sets its B1, B2, D, and E channels to 0. The A bit is set to 0.
INFO 4	INFO 4 corresponds to frames containing operational data on the B1, B2, D, and E channels. The A bit is set to 1.

TRANSMISSION STATES FOR TE MODE S/T–TRANSCEIVER

When configured as a TE, an S/T–Transceiver can be in any of the following transmission states shown in Table 2.

ACTIVATION OF S/T LOOP BY NT

The NT activates the loop by transmitting INFO 2 to the TE or TEs. This is accomplished in the MC145474/75 by setting NR2(3) to a 1. Note that this bit is internally reset to 0 after the internal activation state machine has recognized its active transition.

Table 2. TE Mode Transmission States

Information State	Description
INFO 0	The TE transmits 1s in every bit position. This corresponds to no signal being transmitted.
INFO 1	The TE transmits a continuous signal with the following pattern: positive zero, negative zero, six ones. This signal is asynchronous to the NT.
INFO 3	INFO 3 corresponds to frames containing operational data on the B1, B2, and D channels. If INFO 4 or INFO 2 is being received, INFO 3 will be synchronized to it.

The TE or TEs on receiving INFO 2 will synchronize to it and transmit back INFO 3 to the NT. The NT on receiving INFO 3 from the TE will respond with INFO 4, thus activating the loop.

ACTIVATION OF S/T LOOP BY TE

The TE can activate an inactive loop by transmitting INFO 1 to the NT. This is accomplished in the MC145474/75 by setting NR2(3) to a 1. Note that this bit is internally reset to 0 after the internal activation state machine has recognized its active transition.

The NT upon detecting INFO 1 from the TE will respond with INFO 2. The TE upon receiving a signal from the NT will cease transmission of INFO 1, reverting to an INFO 0 state. After synchronizing to the received signal and having fully verified that it is INFO 2, the TE will respond with INFO 3, thus activating the loop.

FULL ACTIVATION

When the S/T–Interface is fully activated, INFO 3 is transmitted by the TE and INFO 4 by the NT. Figure 11 shows the binary organization and phase relationship of these signals from the TE's perspective.

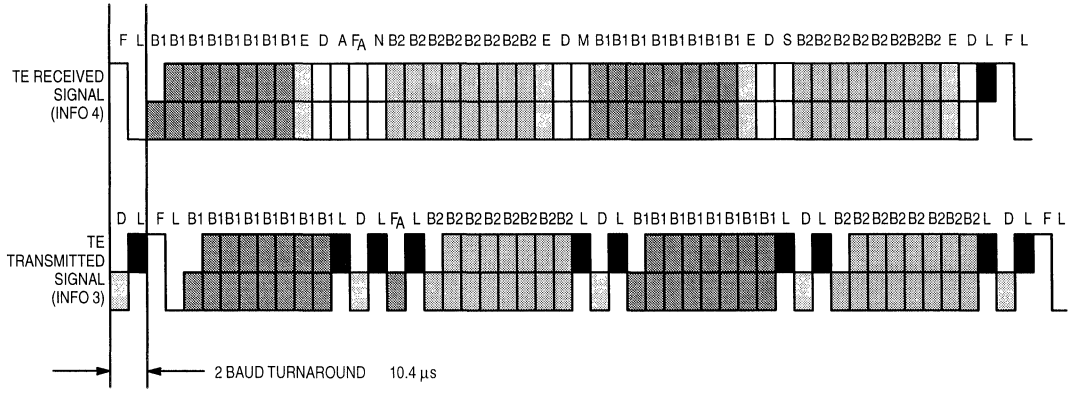


Figure 11. Two Baud Turnaround in TE

THE INTERCHIP DIGITAL LINK

The interchip digital link (IDL) is a four–wire interface used for full–duplex communication between ICs on the board–level. The interface consists of a transmit path, a receive path, an associated clock and a sync signal. These signals are known as IDL Tx, IDL Rx, IDL CLK, and IDL SYNC, respectively. The clock determines the rate of exchange of data in both the transmit and receive directions, and the sync signal controls when this exchange is to take place. Five channels of data are exchanged in a 20–bit package every 8 kHz. These channels consist of two 64 kbps B channels and one 16 kbps D channel used for full–duplex communication between the NT and TE. Figure 12 shows phase alignment and order of transmission.

In addition to these 2B + D channels there are two 8 kbps channels. These two additional channels, known as the IDL A and IDL M channels, are for local communication only (i.e., they are not transmitted from NT to TE or vice versa). Use of these channels is optional. The IDL A and IDL M channels have no effect on the operation of the S/T–Transceiver. There are two modes of operation for an IDL device: IDL master and IDL slave. If an IDL device is configured as an IDL master, then IDL SYNC and IDL CLK are outputs from the device. Conversely, if an IDL device is configured as an IDL slave, then IDL SYNC and IDL CLK are inputs to the device. Ordinarily the MC145474/75 is configured as an IDL slave when acting as an NT, and as an IDL master when acting as a TE. The exception to this rule is the option to configure the NT as an IDL master. Note that an NT configured MC145474/75 comes out of reset in the IDL slave mode.

THE SERIAL CONTROL PORT

INTRODUCTION

The MC145474/75 is equipped with a serial control port (SCP). This SCP is used by external devices (such as an MC145488 DDLC) to communicate with the S/T–Transceiver. The SCP is an industry standard serial control port and is compatible with Motorola's SPI used on several single chip MCUs.

The SCP is a four–wire bus with control and status bits as well as data being passed to and from the S/T–Transceiver in a full–duplex fashion. The SCP interface consists of a transmit path, a receive path, an associated clock, and an enable signal. These signals are known as SCP Tx, SCP Rx, SCPCLK, and $\overline{\text{SCPEN}}$. The clock determines the rate of exchange of data in both the transmit and receive directions, and the enable signal governs when this exchange is to take place.

The operation/configuration of the S/T–Transceiver is programmed by setting the state of the control bits within the S/T–Transceiver. The control, status, and data information reside in eight 4–bit wide nibble registers and sixteen 8–bit wide byte registers. The nibble registers are accessed via an 8–bit SCP bus transaction. The 16–byte wide registers are accessed by first writing to a pointer register within the eight 4–bit wide nibble registers. This pointer register (NR(7)) will then contain the address of the byte wide register to be read from or written to, on the following SCP transaction. Thus, an SCP byte access is in essence a 16–bit operation. Note that this 16–bit operation can take place by means of two 8–bit accesses or a single 16–bit access.

SCP TRANSACTIONS

There are four types of SCP transactions. These are:

1. SCP nibble read
2. SCP nibble write
3. SCP byte read
4. SCP byte write

SCP Nibble Read

A nibble read is an 8–bit SCP transaction. Figure 13 illustrates this process. To initiate an SCP nibble, read the $\overline{\text{SCPEN}}$ pin must be brought low. Following this, a Read/$\overline{\text{Write}}$ (R/$\overline{\text{W}}$) bit followed by three primary address bits (A0 – A3), are shifted (MSB first) into an intermediate buffer register on the first four rising edges of SCPCLK, following the high–to–low transition of $\overline{\text{SCPEN}}$. If a read operation is to be performed then R/$\overline{\text{W}}$ should be a 1. The three address bits clocked in after the R/$\overline{\text{W}}$ bit select which nibble register is to be read. The contents of this nibble register are shifted out on SCP Tx on the subsequent four falling edges of SCPCLK (i.e., the four falling edges of SCPCLK after the rising edge of SCPCLK which clocked in the last address bit, LSB). $\overline{\text{SCPEN}}$ should be brought back high after the transaction, before another falling edge of SCPCLK is encountered. Note that SCP Rx is ignored during the time that SCP Tx is being driven. Also note that SCP Tx comes out of high impedance only when it is transmitting data.

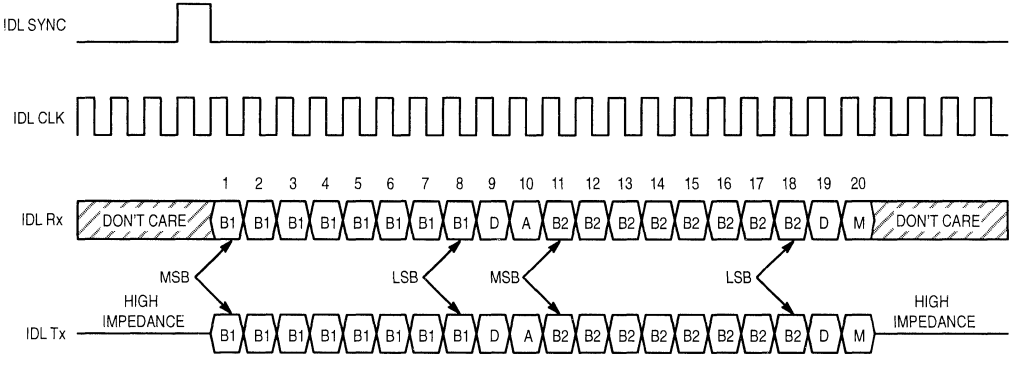
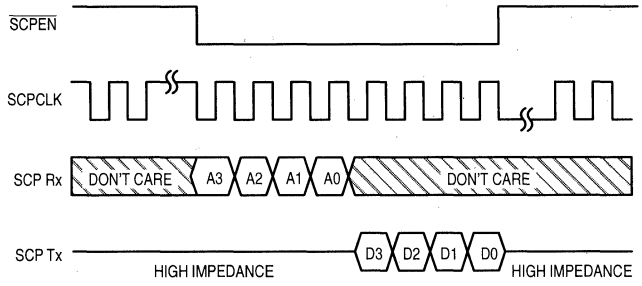


Figure 12. Interchip Digital Link



NOTES:
1. R/$\overline{W}$ = 1 for a read operation.
2. Data is shifted out on SCP Tx on the falling edges of SCPCLK, MSB first.
3. Data is shifted into the chip from SCP Rx on the rising edges of SCPCLK, MSB first.

Figure 13. Serial Control Port Nibble Read Operation

SCP Nibble Write

A nibble write is an 8–bit SCP transaction. Figure 14 illustrates this process. To initiate an SCP nibble write the $\overline{SCPEN}$ pin must be brought low. Following this an R/$\overline{W}$ bit followed by three primary address bits are shifted (MSB first) into an intermediate buffer register on the first four rising edges of SCPCLK following the high to low transition of $\overline{SCPEN}$. If a write operation is to be performed then R/$\overline{W}$ should be a 0. The three address bits clocked in after the R/$\overline{W}$ bit select the nibble register to be written to. The data shifted in on the next four rising edges of SCPCLK is then written to the selected register. Throughout this whole operation the SCP Tx pin remains in high–impedance state. Note that if a selected register or bit in a selected register is "read only" then a write operation has no effect.

SCP Byte Read

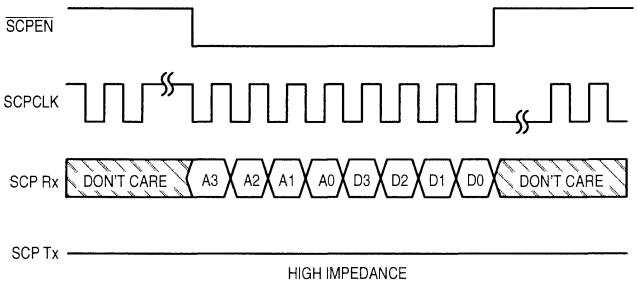
A byte read is a 16–bit SCP transaction. Figure 15 illustrates this process. To initiate an SCP byte read the $\overline{SCPEN}$ must be brought low. Following this an R/$\overline{W}$ bit is shifted in from SCP Rx on the next rising edge of SCPCLK. This bit determines the operation to be performed, read or write. If R/$\overline{W}$ is a 1 then a read operation is selected. Conversely, if R/$\overline{W}$ is a 0 then a write operation is selected. The next three bits shifted in from SCP Rx on the three subsequent rising edges of SCPCLK are primary address bits as mentioned previously. If all three bits are 1, then nibble register 7 is selected (NR7). This is a pointer register, selection of which informs the device that a byte operation is to be performed. When NR7 is selected, the following four bits shifted in from SCP Rx on the following four rising edges of SCPCLK, are automatically written to NR7. These four bits are the address bits for the byte operation. In a read operation the next eight falling edges of SCPCLK will shift out the data from the selected byte register on SCP Tx.

As mentioned previously, an SCP byte access is a 16–bit transaction. This can take place in one 16–bit exchange (Figure 15) or two 8–bit exchanges (Figure 16). If the transaction is performed in two 8–bit exchanges the $\overline{SCPEN}$ should be returned high after the first eight bits have been shifted into the part. When $\overline{SCPEN}$ comes low again the MSB of the selected byte will present itself on SCP Tx. The following eight falling edges of SCPCLK will shift out the remaining eight bits of the byte register. Note that the order in which data is written into the part and read out of the part is independent of whether the byte access is done in one 16–bit exchange or in two 8–bit exchanges.

SCP Byte Write

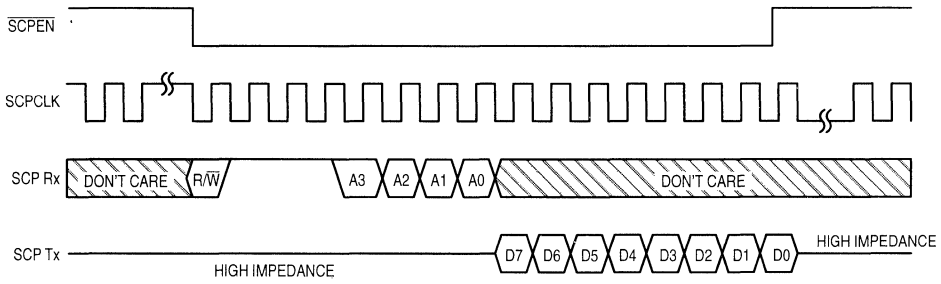
A byte write is also a 16–bit SCP transaction. Figure 17 illustrates this process. To initiate an SCP byte write the $\overline{SCPEN}$ must be brought low. As before, the next bit determines whether the operation is to be read or write. If the first bit is a 0 then a write operation is selected. Again the next three bits read in from SCP Rx on the subsequent three rising edges of SCPCLK must all be 1 in order to select the pointer nibble register (NR7). The following four bits shifted in are automatically written into NR7. As in an SCP byte read these bits are the address bits for the selected byte register operation. The next eight rising edges of SCPCLK shift in the data from the SCP Rx. This data is then stored in the selected byte register. Throughout this operation SCP Tx will be in a high–impedance state. Note that if the selected byte is **read only**, then this operation will have no effect.

As mentioned previously, an SCP byte access is a 16–bit transaction. This can take place in one 16–bit exchange (Figure 17) or two 8–bit exchanges (Figure 18). If the transaction is performed in two 8–bit exchanges, then $\overline{SCPEN}$ should be returned high after the first eight bits have been shifted into the part. When $\overline{SCPEN}$ comes low again, the next eight rising edges of SCPCLK shift data in from SCP Rx. This data is then stored in the selected byte. Figure 18 illustrates this process.



NOTES:
1. R/$\overline{W}$ = 0 for a write operation.
2. Data is shifted out on SCP Tx on the falling edges of SCPCLK, MSB first.
3. Data is shifted into the chip from SCP Rx on the rising edges of SCPCLK, MSB first.

Figure 14. Serial Control Port Nibble Write Operation



NOTES:
1. R/$\overline{W}$ = 1 for a read operation.
2. Data is shifted out on SCP Tx on the falling edges of SCPCLK, MSB first.
3. Data is shifted into the chip from SCP Rx on the rising edges of SCPCLK, MSB first.

Figure 15. Serial Control Port Byte Read Operation

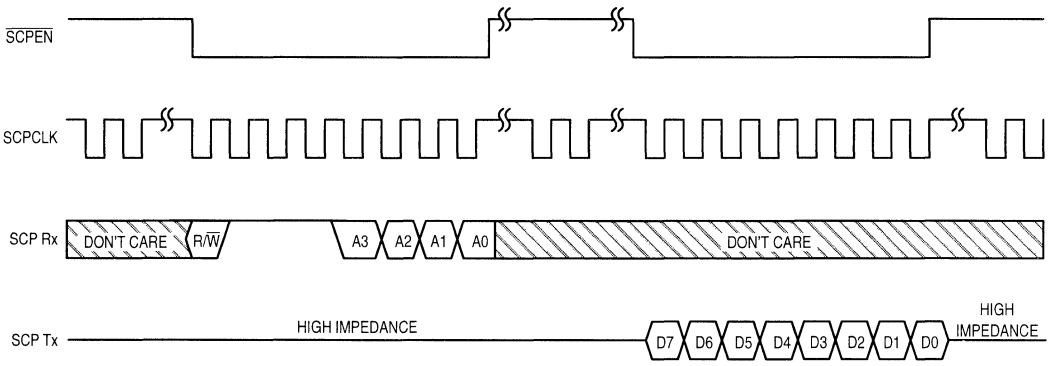
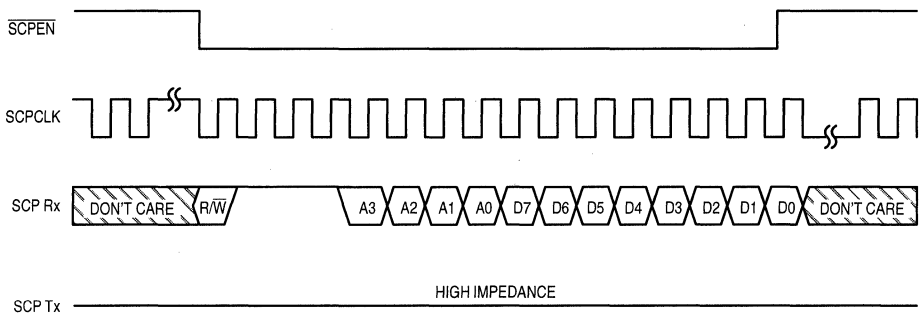


Figure 16. Serial Control Port Byte Read Operation (Double 8–Bit Transaction)



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NOTES:
1. R/$\overline{W}$ = 0 for a write operation.
2. Data is shifted out on SCP Tx on the falling edges of SCPCLK, MSB first.
3. Data is shifted into the chip from SCP Rx on the rising edges of SCPCLK, MSB first.

Figure 17. Serial Control Port Byte Write Operation

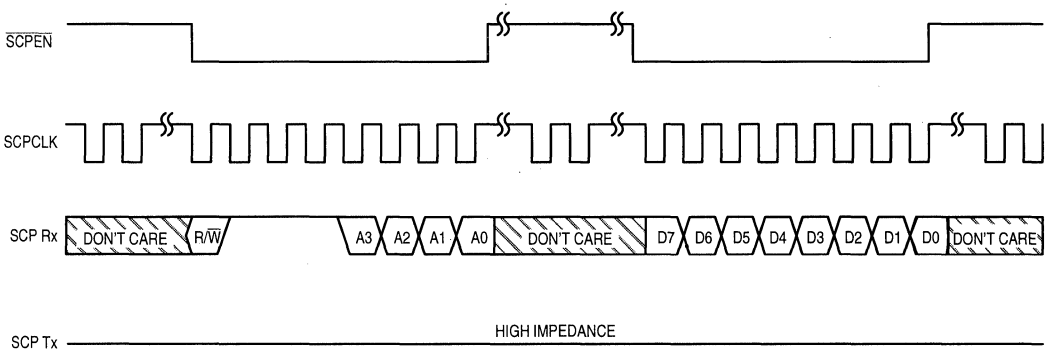


Figure 18. Serial Control Port Byte Write Operation (Double 8–Bit Transaction)

NIBBLE MAP DEFINITION

There are eight nibble registers (NR0 through NR7) in the MC145474/75. Control and status information reside in these nibble registers. These nibble registers are accessed via the SCP (see Tables 3 and 4).

BYTE MAP DESCRIPTION

There are sixteen byte registers (BR0 through BR15) in the MC145474/75. Control, status, and maintenance information reside in these byte registers. These byte registers are accessed via the SCP (see Tables 5 and 6).

Table 3. SCP Nibble Map for NT Operation

	(3)	(2)	(1)	(0)
NR0	Software Reset	Transmit Power Down	Absolute Minimum Power	Return to Normal
NR1	Activation Indication (AI)	Error Indication (EI)		Frame Sync (FS)
NR2	Activation Request (AR)	Deactivate Request (DR)	Activation Timer #1 Expire	
NR3	IRQ #3 Change in Rx INFO	IRQ #2 Multiframe Reception	IRQ #6 FECV Detection	
NR4	IRQ #3 Enable	IRQ #2 Enable	IRQ #6 Enable	
NR5	Idle B1 Channel on S/T Loop	Idle B2 Channel on S/T Loop	Invert B1 Channel	Invert B2 Channel
NR6	2B+D IDL Non–Transparent Loopback	Activate IDL M FIFO	Activate IDL A FIFO	Exchange B1 & B2 at IDL

Table 4. SCP Nibble Map for TE Operation

	(3)	(2)	(1)	(0)
NR0	Software Reset	Transmit Power Down	Absolute Minimum Power	Return to Normal
NR1	Activation Indication (AI)	Error Indication (EI)	Multiframing Detect	Frame Sync (FS)
NR2	Activation Request (AR)		Activation Timer #3 Expire	Class
NR3	IRQ #3 Change in Rx INFO	IRQ #2 Multiframe Reception	IRQ #1 D Channel Collision	
NR4	IRQ #3 Enable	IRQ #2 Enable	IRQ #1 Enable	
NR5	Enable B1 Channel on S/T Loop	Enable B2 Channel on S/T Loop	Invert B1 Channel	Invert B2 Channel
NR6	2B+D IDL Non–Transparent Loopback	Activate IDL M FIFO	Activate IDL A FIFO	Exchange B1 & B2 at IDL

Table 5. SCP Byte Map for NT Operation

	(7)	(6)	(5)	(4)	(3)	(2)	(1)	(0)
BR0	M7	M6	M5	M4	M3	M2	M1	M0
BR1	A7	A6	A5	A4	A3	A2	A1	A0
BR2	SC1.1 to Loop	SC1.2 to Loop	SC1.3 to Loop	SC1.4 to Loop				
BR3	Q1 from Loop	Q2 from Loop	Q3 from Loop	Q4 from Loop	Q Bit Quality Indicate	INT Every M. Frame		
BR4	Fr. Viol. Count B7	Fr. Viol. Count B6	Fr. Viol. Count B5	Fr. Viol. Count B4	Fr. Viol. Count B3	Fr. Viol. Count B2	Fr. Viol. Count B1	Fr. Viol. Count B0
BR5	BPV Count B7	BPV Count B6	BPV Count B5	BPV Count B4	BPV Count B3	BPV Count B2	BPV Count B1	BPV Count B0
BR6	B1 S/T LB Transparent	B1 S/T LB Non–Trans.	B2 S/T LB Transparent	B2 S/T LB Non–Trans.	IDL B1 LB Transparent	IDL B1 LB Non–Trans.	IDL B2 LB Transparent	IDL B2 LB Non–Trans.
BR7	Act. Proc. Disabled	Reserved	Enable Multiframing	Invert E Channel	IDL Master Mode	IDL CLK Speed LSB		Act. Timer #2
BR8	IDL M FIFO ≤ 1/2 Full	IDL A FIFO ≤ 1/2 Full	Act. IDL M FIFO HOZ	Act. IDL A FIFO HOZ	Enable IRQ #4	Enable IRQ #5	IRQ #4 IDL A FIFO	IRQ #5 IDL M FIFO
BR9	SC2.1 to Loop	SC2.2 to Loop	SC2.3 to Loop	SC2.4 to Loop	SC3.1 to Loop	SC3.2 to Loop	SC3.3 to Loop	SC3.4 to Loop
BR10	SC4.1 to Loop	SC4.2 to Loop	SC4.3 to Loop	SC4.4 to Loop	SC5.1 to Loop	SC5.2 to Loop	SC5.3 to Loop	SC5.4 to Loop
BR11	Do Not React to INFO 1	Do Not React to INFO 3	Rx INFO State B1	Rx INFO State B0	Tx INFO State B1	Tx INFO State B0	EXT S/T Loopback	Tx 96 kHz Test Signal
BR12	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
BR13	NT1 Star Mode	TTL Input Levels	IDL CLK Speed MSB	Mute B2 on IDL	Mute B1 on IDL	Force E to Zero		
BR14					Reserved	Reserved	Reserved	Reserved
BR15	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

Table 6. SCP Byte Map for TE Operation

	(7)	(6)	(5)	(4)	(3)	(2)	(1)	(0)
BR0	M7	M6	M5	M4	M3	M2	M1	M0
BR1	A7	A6	A5	A4	A3	A2	A1	A0
BR2	Q1 to Loop	Q2 to Loop	Q3 to Loop	Q4 to Loop				
BR3	SC1.1 from Loop	SC1.2 from Loop	SC1.3 from Loop	SC1.4 from Loop		INT Every M Frame		
BR4	Fr. Viol. Count B7	Fr. Viol. Count B6	Fr. Viol. Count B5	Fr. Viol. Count B4	Fr. Viol. Count B3	Fr. Viol. Count B2	Fr. Viol. Count B1	Fr. Viol. Count B0
BR5	BPV Count B7	BPV Count B6	BPV Count B5	BPV Count B4	BPV Count B3	BPV Count B2	BPV Count B1	BPV Count B0
BR6	B1 S/T LB Transparent	B1 S/T LB Non–Trans.	B2 S/T LB Transparent	B2 S/T LB Non–Trans.	IDL B1 LB Transparent	IDL B1 LB Non–Trans.	IDL B2 LB Transparent	IDL B2 LB Non–Trans.
BR7	Act. Proc. Ignored	D Channel Proc. Ignored		Map E to IDL on D Channel	IDL Free Run	IDL CLK Speed LSB	LAPD Pol. Cont.	
BR8	IDL M FIFO ≤ 1/2 Full	IDL A FIFO ≤ 1/2 Full	Act. IDL M FIFO HOZ	Act. IDL A FIFO HOZ	Enable IRQ #4	Enable IRQ #5	IRQ #4 IDL A FIFO	IRQ #5 IDL M FIFO
BR9	SC2.1 from Loop	SC2.2 from Loop	SC2.3 from Loop	SC2.4 from Loop	SC3.1 from Loop	SC3.2 from Loop	SC3.3 from Loop	SC3.4 from Loop
BR10	SC4.1 from Loop	SC4.2 from Loop	SC4.3 from Loop	SC4.4 from Loop	SC5.1 from Loop	SC5.2 from Loop	SC5.3 from Loop	SC5.4 from Loop
BR11			Rx INFO State B1	Rx INFO State B0	Tx INFO State B1	Tx INFO State B0	EXT S/T Loopback	Tx 96 kHz Test Signal
BR12	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
BR13		TTL Input Levels	IDL CLK Speed MSB	Mute B2 on IDL	Mute B1 on IDL		Force IDL Transmit	
BR14					Reserved	Reserved	Reserved	Reserved
BR15	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

D CHANNEL OPERATION

INTRODUCTION

The S/T–Interface is designed for full duplex transmission of two 64 kbps B channels and one 16 kbps D channel, between one NT device and one or more TEs. The TEs gain access to the B channels by sending Layer 2 frames to the network over the D channel. CCITT I.430 and ANSI T1.605 specify a D channel access algorithm for TEs to gain access to the D channel. The MC145474/75 S/T–Transceiver is fully compliant with the D channel access algorithm as defined in CCITT I.430 and ANSI T1.605. The SCP bits and pins directly pertaining to D channel operation are shown in Tables 7 and 8.

D channel data is clocked into the MC145474/75 via IDL Rx on the falling edges of IDL CLK. Data is clocked out onto IDL Tx on the rising edges of IDL CLK. This is in accordance with the IDL specification as outlined earlier.

GAINING ACCESS TO THE D CHANNEL IN TE MODE

The pins DREQ and DGRANT are used in the TE mode of operation to request and grant access to the D channel. An external device wishing to send a Layer 2 frame should bring DREQ high, and maintain it high for the duration of the Layer 2 frame. DGRANT is an output signal used to indicate to an external device that the D channel is clear. Note that the DGRANT signal actually goes high one received E echo bit prior to the programmed priority class selection. DGRANT goes high at a count of (n – 1) to accommodate the delay between the input of D channel data via the IDL interface and the line transmission of those bits towards the NT. If at the time of the IDL SYNC pulse falling edge, the DGRANT and the DREQ signals are both detected high, the TE mode transceiver will begin FIFO buffering of the input D channel bits from the IDL interface. This FIFO is four bits deep. Note that DGRANT goes high on the boundaries of the demodulated E bits. In order for the contention algorithm to work on the D channel, HDLC data must be used. The MC145474/75 modulates the D channel data onto the S/T bus in the form that it is received from the IDL bus. Thus, the data must be presented to it in HDLC format. Note that one of the applications of the MC145488 DDLC is for use with the MC145474/75 in the terminal mode. The MC145488 will perform the HDLC conversion and perform the necessary D channel handshaking.

Note that the active polarity of the DREQ and DGRANT signals may be reversed by setting the LAPD polarity control bit (BR7(1)) in the SCP. When BR7(1) is a 0 the active polarity is as described above. Conversely, when BR7(1) is a 1 the MC145474/75 will drive DGRANT to a logic 0 when DGRANT is active and to a logic 1 when DGRANT is inactive. Also, when BR7(1) is 1, DREQ will be considered to be active low.

Table 7. D Channel SCP Bit Description

MC145474/75 NT Mode		MC145474/75 TE Mode	
SCP Bit	**Description**	**SCP Bit**	**Description**
BR7(4)	Invert the Echo Channel	NR2(0)	Class
BR13(2)	Force the Echo Channel to '0'	NR3(1)	Interrupt on D Channel Collision
BR13(7)	NT1 Star Mode	NR4(1)	Interrupt Enable for NR3(1)
		BR7(1)	LAPD Polarity Control
		BR7(4)	Map Echo Bits to D Timeslots on IDL Tx
		BR7(6)	D Channel Procedures Ignored

Table 8. D Channel Operation Pin Description

Pin No.	MC145474	MC145475
5	DGRANT	DGRANT
7	DREQ	AND_{in}
8		AND_{out}
9		DREQ
10		CLASS/ECHOin

GAINING ACCESS TO THE D CHANNEL IN NT MODE

When configured as an NT the MC145474/75 has automatic access to the D channel. This is because the S/T–Interface is designed for communication between a single NT and one or more TEs. As such, the NT does not have to compete for access to the D channel. Thus, there are no DREQ or DGRANT functions associated with the NT mode of operation. Data present in the D bit positions of the IDL frame on IDL Rx are modulated onto the D bit timeslots on the S/T loop. Demodulated D channel data from the TE/TEs is transmitted onto IDL Tx in accordance with the IDL specification. The ECHO function of an NT configured S/T–Transceiver is performed internally in the MC145474/75. To assist in testing an S/T loop the MC145474/75 features the SCP test bits BR7(4) and BR13(2). Setting BR7(4) in the NT mode will invert the E echo channel (i.e., the logical inverse of the demodulated D channel data from the TE/TEs is transmitted in the E channel). Setting BR13(2) to a 1 will force the E channel to all 0s. Refer to Section 8 for a more detailed description of these test bits. Setting BR13(7) to a 1 puts the "NT configured" MC145474/75 S/T–Transceiver into the NT1 Star mode of operation. In this mode, the bits to be ECHOed back to the TE/TEs are obtained from the $ECHO_{in}$ pin.

MULTIFRAMING

A Layer 1 signalling channel between the NT and TE is provided in the MC145474/75 in accordance with CCITT I.430 and ANSI T1.605. In the NT to TE direction, this Layer 1 channel is the S channel. In the TE to NT direction it is the Q channel. The S channel is subdivided into five subchannels: SC1, SC2, SC3, SC4, and SC5. The MC145474/75 is capable of transmitting and receiving data in all S subchannels as well as the Q channel by simply reading or writing to the appropriate SCP registers. Interrupts are also available to indicate the reception of multiframe information. See the MC145474/75 data book for a complete description.

NT1 STAR MODE OPERATION

Appendix B of ANSI T1.605 describes an example of an NT that will support multiple T interfaces. This is to accommodate multipoint operation with more than eight TEs. The MC145475 can be configured for NT1 Star mode of operation. This mode is for use in wire ORing multiple NT configured S/T chips on the IDL side. Each NT has a common IDL SYNC, IDL CLK, IDL Tx, and IDL Rx, as shown in Figure 19. Each NT is then connected to its own individual S/T loop containing either a single TE or a group of TEs. As such, the contention for either of the B channels or for the D channel is now extended from a single passive bus to a grouping of passive busses.

ISDN employs the use of HDLC data on the D channel. Access to either of the B channels is requested and either granted or denied by the user sending Layer 2 frames on the D channel. In normal operation where there is only one NT, the TEs are granted access to the D channel in accordance with their priority and class. By counting the required number of E channel echo bits being 1, the TEs know when the D channel is clear. Thus in the NT1 Star mode of operation, where there are multiple passive busses competing for the same B1, B2, and D channels, the same E echo channel must be transmitted from each NT to its passive bus. This is accomplished in the MC145475 by means of the AND_{in}, AND_{out}, and $ECHO_{in}$ pins.

Figure 19 shows how to connect the multiple number of NTs in the NT1 Star mode. Successive connection of the AND_{out} (this is the output of an internal AND gate whose inputs are the demodulated D bits and the data on the AND_{in} pin) and AND_{in} pins, and the common connections of the $ECHO_{in}$ pins, succeeds in sending the same E echo channel to each group of TE/TEs. To configure a series of NTs for NT1 Star mode, BR13(7) must be set to 1 in each NT. Data transmitted on IDL Tx in NT1 Star mode, will have the following format: a logic 0 is V_{SS}, a logic 1 causes IDL Tx to go to a high–impedance state. This then permits the series wire ORing of the IDL bus. Note that one of the NTs must have its AND_{in} pin pulled high.

TRANSMISSION LINE INTERFACE CIRCUITRY

The MC145474/75 is an ISDN S/T–Transceiver fully compliant with CCITT I.430 and ANSI T1.605. As such it is designed to interface with a four–wire transmission medium, one pair being the transmit path, the other pair the receive path. TxP and TxN, a fully differential output transmit pair from the MC145474/75, are designed to interface to the transmit pair of the transmission medium via auxiliary discrete components and a 1:1 turns ratio transformer. RxP and RxN are a high–impedance differential input pair used for coupling the receive line signal through a 1:1 turns ratio transformer (see Figures 20 and 21).

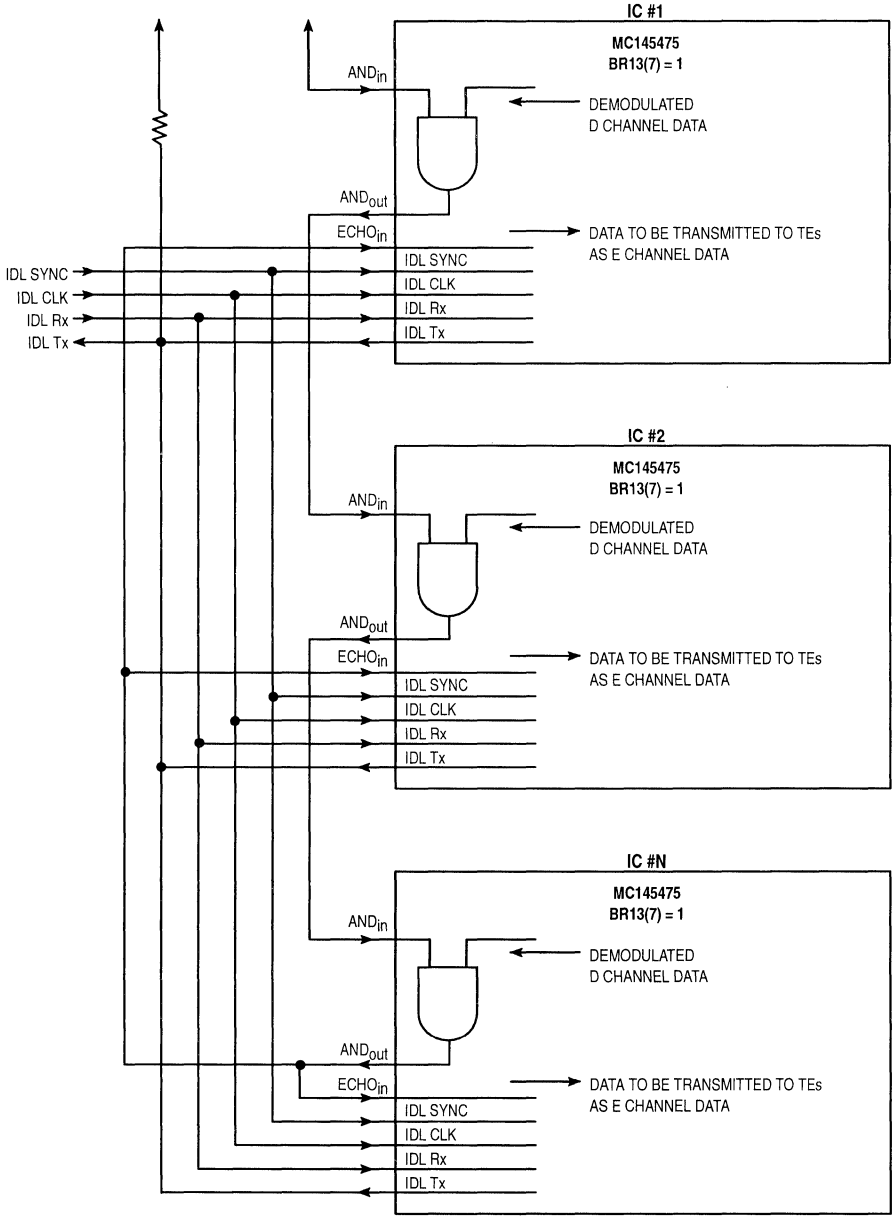
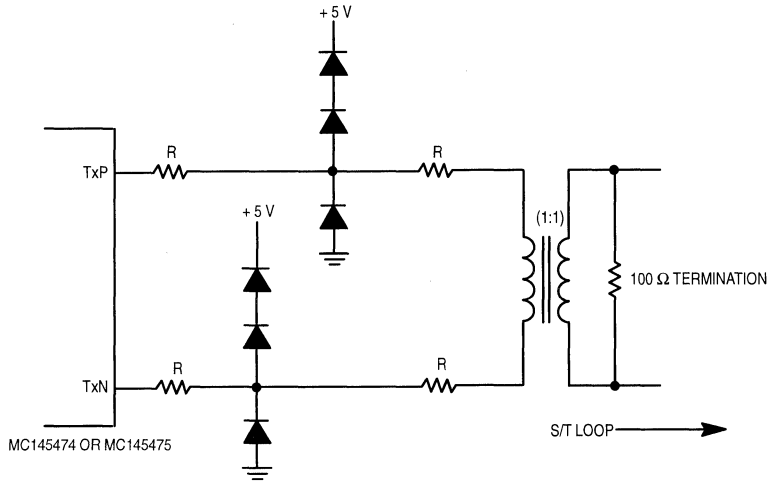


Figure 19. NT1 Star Mode of Operation



NOTE: 4R + winding resistance = 26.4 Ω.

Figure 20. Transmit Line Interface Circuit

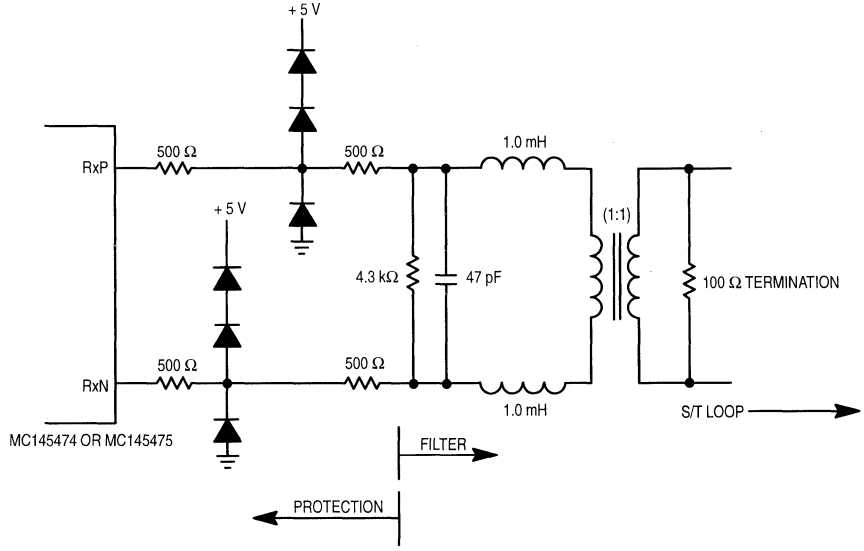
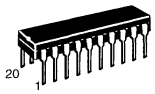


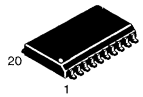
Figure 21. Receive Line Interface Circuit

MC145480

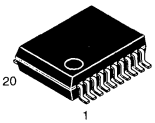
5 V PCM Codec-Filter



P SUFFIX
PLASTIC DIP
CASE 738



DW SUFFIX
SOG PACKAGE
CASE 751D



VF SUFFIX
SSOP
CASE 940C

ORDERING INFORMATION

MC145480P	Plastic DIP
MC145480DW	SOG Package
MC145480VF	SSOP

The MC145480 is a general purpose per channel PCM Codec–Filter with pin selectable Mu–Law or A–Law companding, and is offered in 20–pin DIP, SOG, and SSOP packages. This device performs the voice digitization and reconstruction as well as the band limiting and smoothing required for PCM systems. This device is designed to operate in both synchronous and asynchronous applications and contains an on–chip precision reference voltage.

This device has an input operational amplifier whose output is the input to the encoder section. The encoder section immediately low–pass filters the analog signal with an active R–C filter to eliminate very high frequency noise from being modulated down to the passband by the switched capacitor filter. From the active R–C filter, the analog signal is converted to a differential signal. From this point, all analog signal processing is done differentially. This allows processing of an analog signal that is twice the amplitude allowed by a single–ended design, which reduces the significance of noise to both the inverted and non–inverted signal paths. Another advantage of this differential design is that noise injected via the power supplies is a common–mode signal that is cancelled when the inverted and non–inverted signals are recombined. This dramatically improves the power supply rejection ratio.

After the differential converter, a differential switched capacitor filter band–passes the analog signal from 200 Hz to 3400 Hz before the signal is digitized by the differential compressing A/D converter.

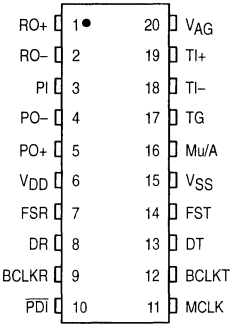
The decoder accepts PCM data and expands it using a differential D/A converter. The output of the D/A is low–pass filtered at 3400 Hz and sinX/X compensated by a differential switched capacitor filter. The signal is then filtered by an active R–C filter to eliminate the out–of–band energy of the switched capacitor filter.

The MC145480 PCM Codec–Filter accepts a variety of clock formats, including Short Frame Sync, Long Frame Sync, IDL, and GCI timing environments. This device also maintains compatibility with Motorola's family of Telecommunication products, including the MC14LC5472 U–Interface Transceiver, MC145474/75 S/T–Interface Transceiver, MC145532 ADPCM Transcoder, MC145422/26 UDLT–1, MC145421/25 UDLT–2, and MC3419/MC33120 SLIC.

The MC145480 PCM Codec–Filter utilizes CMOS due to its reliable low–power performance and proven capability for complex analog/digital VLSI functions.

- Single 5 V Power Supply
- Typical Power Dissipation of 23 mW, Power–Down of 0.01 mW
- Fully–Differential Analog Circuit Design for Lowest Noise
- Transmit Band–Pass and Receive Low–Pass Filters On–Chip
- Active R–C Pre–Filtering and Post–Filtering
- Mu–Law and A–Law Companding by Pin Selection
- On–Chip Precision Reference Voltage (1.575 V)
- Push–Pull 300 Ω Power Drivers with External Gain Adjust
- MC145536EVK is the Evaluation Kit that Also Includes the MC145532 ADPCM Transcoder

PIN ASSIGNMENT



REV 2
9/95

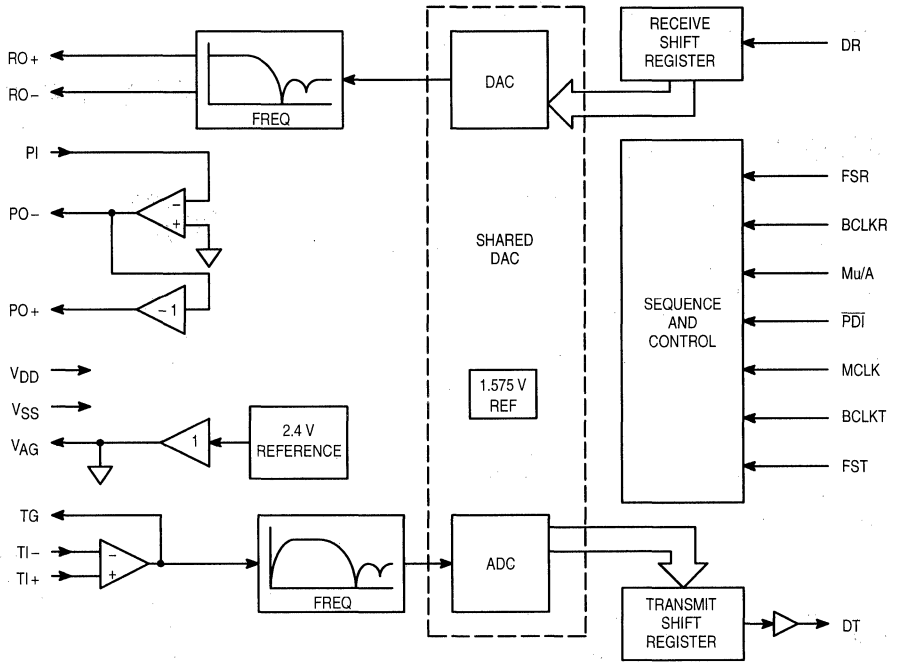


Figure 1. MC145480 PCM Codec–Filter Block Diagram

DEVICE DESCRIPTION

A PCM Codec–Filter is used for digitizing and reconstructing the human voice. These devices are used primarily for the telephone network to facilitate voice switching and transmission. Once the voice is digitized, it may be switched by digital switching methods or transmitted long distance (T1, microwave, satellites, etc.) without degradation. The name codec is an acronym from "COder" for the analog–to–digital converter (ADC) used to digitize voice, and "DECoder" for the digital–to–analog converter (DAC) used for reconstructing voice. A codec is a single device that does both the ADC and DAC conversions.

To digitize intelligible voice requires a signal–to–distortion ratio of about 30 dB over a dynamic range of about 40 dB. This may be accomplished with a linear 13–bit ADC and DAC, but will far exceed the required signal–to–distortion ratio at larger amplitudes than 40 dB below the peak amplitude. This excess performance is at the expense of data per sample. Two methods of data reduction are implemented by compressing the 13–bit linear scheme to companded pseudo–logarithmic 8–bit schemes. The two companding schemes are: Mu–255 Law, primarily in North America and Japan; and A–Law, primarily used in Europe. These companding schemes are accepted world wide. These companding schemes follow a segmented or "piecewise–linear" curve formatted as sign bit, three chord bits, and four step bits. For a given chord, all sixteen of the steps have the same voltage weighting. As the voltage of the analog input increases, the four step bits increment and carry to the three chord bits which increment. When the chord bits increment, the step bits double their voltage weighting. This results in an effective resolution of six bits (sign + chord + four step bits) across a 42 dB dynamic range (seven chords above 0, by 6 dB per chord).

In a sampling environment, Nyquist theory says that to properly sample a continuous signal, it must be sampled at a frequency higher than twice the signal's highest frequency component. Voice contains spectral energy above 3 kHz, but its absence is not detrimental to intelligibility. To reduce the digital data rate, which is proportional to the sampling rate, a sample rate of 8 kHz was adopted, consistent with a bandwidth of 3 kHz. This sampling requires a low–pass filter to limit the high frequency energy above 3 kHz from distorting the in–band signal. The telephone line is also subject to 50/60 Hz power line coupling, which must be attenuated from the signal by a high–pass filter before the analog–to–digital converter.

The digital–to–analog conversion process reconstructs a staircase version of the desired in–band signal, which has spectral images of the in–band signal modulated about the sample frequency and its harmonics. These spectral images are called aliasing components, which need to be attenuated to obtain the desired signal. The low–pass filter used to attenuate these aliasing components is typically called a reconstruction or smoothing filter.

The MC145480 PCM Codec–Filter has the codec, both presampling and reconstruction filters, a precision voltage reference on–chip, and requires no external components.

PIN DESCRIPTIONS

POWER SUPPLY

V_{DD}
Positive Power Supply (Pin 6)

This is the most positive power supply and is typically connected to + 5 V. This pin should be decoupled to V_{SS} with a 0.1 μF ceramic capacitor.

V_{SS}
Negative Power Supply (Pin 15)

This is the most negative power supply and is typically connected to 0 V.

V_{AG}
Analog Ground Output (Pin 20)

This output pin provides a mid–supply analog ground regulated to 2.4 V. This pin should be decoupled to V_{SS} with a 0.01 μF to 0.1 μF ceramic capacitor. All analog signal processing within this device is referenced to this pin. If the audio signals to be processed are referenced to V_{SS}, then special precautions must be utilized to avoid noise between V_{SS} and the V_{AG} pin. Refer to the applications information in this document for more information. The V_{AG} pin becomes high impedance when this device is in the powered down mode.

CONTROL

Mu/A
Mu/A Law Select (Pin 16)

This pin controls the compression for the encoder and the expansion for the decoder. Mu–Law companding is selected when this pin is connected to V_{DD} and A–Law companding is selected when this pin is connected to V_{SS}.

$\overline{PDI}$
Power–Down Input (Pin 10)

This pin puts the device into a low power dissipation mode when a logic 0 is applied. When this device is powered down, all of the clocks are gated off and all bias currents are turned off, which causes RO+, RO–, PO–, PO+, TG, V_{AG}, and DT to become high impedance. The device will operate normally when a logic 1 is applied to this pin. The device goes through a power–up sequence when this pin is taken to a logic 1 state, which prevents the DT PCM output from going low impedance for at least two FST cycles. The filters must settle out before the DT PCM output or the RO+ or RO– receive analog outputs will represent a valid analog signal.

ANALOG INTERFACE

TI+
Transmit Analog Input (Non–Inverting) (Pin 19)

This is the non–inverting input of the transmit input gain setting operational amplifier. This pin accommodates a differential to single–ended circuit for the input gain setting op amp. This allows input signals that are referenced to the V_{SS} pin to be level shifted to the V_{AG} pin with minimum noise. This pin may be connected to the V_{AG} pin for an inverting amplifier configuration if the input signal is already referenced to the V_{AG} pin. The common mode range of the TI+ and TI– pins is from 1.2 V, to V_{DD} minus 2 V. This is an FET gate input. Connecting both TI+ and TI– pins to V_{DD} will place this amplifier's output (TG) into a high–impedance state, thus allowing the TG pin to serve as a high–impedance input to the transmit filter.

TI–
Transmit Analog Input (Inverting) (Pin 18)

This is the inverting input of the transmit gain setting operational amplifier. Gain setting resistors are usually connected from this pin to TG and from this pin to the analog signal source. The common mode range of the TI+ and TI– pins is from 1.2 V to V_{DD} – 2 V. This is an FET gate input. Connecting both TI+ and TI– pins to V_{DD} will place this amplifier's output (TG) into a high–impedance state, thus allowing the TG pin to serve as a high–impedance input to the transmit filter.

TG
Transmit Gain (Pin 17)

This is the output of the transmit gain setting operational amplifier and the input to the transmit band–pass filter. This op amp is capable of driving a 2 kΩ load. Connecting both TI+ and TI– pins to V_{DD} will place this amplifier's output (TG) into a high–impedance state, thus allowing the TG pin to serve as a high–impedance input to the transmit filter. All signals at this pin are referenced to the V_{AG} pin. This pin is high impedance when the device is in the powered down mode.

RO+
Receive Analog Output (Non–Inverting) (Pin 1)

This is the non–inverting output of the receive smoothing filter from the digital–to–analog converter. This output is capable of driving a 2 kΩ load to 1.575 V peak referenced to the V_{AG} pin. This pin is high impedance when the device is in the powered down mode.

RO–
Receive Analog Output (Inverting) (Pin 2)

This is the inverting output of the receive smoothing filter from the digital–to–analog converter. This output is capable of driving a 2 kΩ load to 1.575 V peak referenced to the V_{AG} pin. This pin is high impedance when the device is in the powered down mode.

PI
Power Amplifier Input (Pin 3)

This is the inverting input to the PO– amplifier. The non–inverting input to the PO– amplifier is internally tied to the V_{AG} pin. The PI and PO– pins are used with external resistors in an inverting op amp gain circuit to set the gain of the PO+ and PO– push–pull power amplifier outputs. Connecting PI to V_{DD} will power down the power driver amplifiers and the PO+ and PO– outputs will be high impedance.

PO–
Power Amplifier Output (Inverting) (Pin 4)

This is the inverting power amplifier output, which is used to provide a feedback signal to the PI pin to set the gain of the push–pull power amplifier outputs. This pin is capable of driving a 300 Ω load to PO+. The PO+ and PO– outputs are differential (push–pull) and capable of driving a 300 Ω load to 3.15 V peak, which is 6.3 V peak–to–peak. The bias voltage and signal reference of this output is the V_{AG} pin. The V_{AG}

pin cannot source or sink as much current as this pin, and therefore low impedance loads must be between PO+ and PO–. Connecting PI to V_{DD} will power down the power driver amplifiers and the PO+ and PO– outputs will be high impedance. This pin is also high impedance when the device is powered down by the $\overline{PDI}$ pin.

PO+
Power Amplifier Output (Non–Inverting) (Pin 5)

This is the non–inverting power amplifier output, which is an inverted version of the signal at PO–. This pin is capable of driving a 300 Ω load to PO–. Connecting PI to V_{DD} will power down the power driver amplifiers and the PO+ and PO– outputs will be high impedance. This pin is also high impedance when the device is powered down by the $\overline{PDI}$ pin. See PI and PO– for more information.

2

DIGITAL INTERFACE

MCLK
Master Clock (Pin 11)

This is the master clock input pin. The clock signal applied to this pin is used to generate the internal 256 kHz clock and sequencing signals for the switched–capacitor filters, ADC, and DAC. The internal prescaler logic compares the clock on this pin to the clock at FST (8 kHz) and will automatically accept 256, 512, 1536, 1544, 2048, 2560, or 4096 kHz. For MCLK frequencies of 256 and 512 kHz, MCLK must be synchronous and approximately rising edge aligned to FST. For optimum performance at frequencies of 1.536 MHz and higher, MCLK should be synchronous and approximately rising edge aligned to the rising edge of FST. In many applications, MCLK may be tied to the BCLKT pin.

FST
Frame Sync, Transmit (Pin 14)

This pin accepts an 8 kHz clock that synchronizes the output of the serial PCM data at the DT pin. This input is compatible with various standards including IDL, Long Frame Sync, Short Frame Sync, and GCI formats. If both FST and FSR are held low for several 8 kHz frames, the device will power down.

BCLKT
Bit Clock, Transmit (Pin 12)

This pin controls the transfer rate of transmit PCM data. In the IDL and GCI modes it also controls the transfer rate of the receive PCM data. This pin can accept any bit clock frequency from 64 to 4096 kHz for Long Frame Sync and Short Frame Sync timing. This pin can accept clock frequencies from 256 kHz to 4.096 MHz in IDL mode, and from 512 kHz to 6.176 MHz for GCI timing mode.

DT
Data, Transmit (Pin 13)

This pin is controlled by FST and BCLKT and is high impedance except when outputting PCM data. When operating in the IDL or GCI mode, data is output in either the B1 or B2 channel as selected by FSR. This pin is high impedance when the device is in the powered down mode.

FSR
Frame Sync, Receive (Pin 7)

When used in the Long Frame Sync or Short Frame Sync mode, this pin accepts an 8 kHz clock, which synchronizes the input of the serial PCM data at the DR pin. FSR can be asynchronous to FST in the Long Frame Sync or Short Frame Sync modes. When an ISDN mode (IDL or GCI) has been selected with BCLKR, this pin selects either B1 (logic 0) or B2 (logic 1) as the active data channel.

BCLKR
Bit Clock, Receive (Pin 9)

When used in the Long Frame Sync or Short Frame Sync mode, this pin accepts any bit clock frequency from 64 to 4096 kHz. When this pin is held at a logic 1, FST, BCLKT, DT, and DR become IDL Interface compatible. When this pin is held at a logic 0, FST, BCLKT, DT, and DR become GCI Interface compatible.

DR
Data, Receive (Pin 8)

This pin is the PCM data input, and when in a Long Frame Sync or Short Frame Sync mode is controlled by FSR and BCLKR. When in the IDL or GCI mode, this data transfer is controlled by FST and BCLKT. FSR and BCLKR select the B channel and ISDN mode, respectively.

FUNCTIONAL DESCRIPTION

ANALOG INTERFACE AND SIGNAL PATH

The transmit portion of this device includes a low–noise, three–terminal op amp capable of driving a 2 kΩ load. This op amp has inputs of TI+ (Pin 19) and TI– (Pin 18) and its output is TG (Pin 17). This op amp is intended to be configured in an inverting gain circuit. The analog signal may be applied directly to the TG pin if this transmit op amp is independently powered down by connecting the TI+ and TI– inputs to the V_{DD} power supply. The TG pin becomes high impedance when the transmit op amp is powered down. The TG pin is internally connected to a 3–pole anti–aliasing pre–filter. This pre–filter incorporates a 2–pole Butterworth active low–pass filter, followed by a single passive pole. This pre–filter is followed by a single–ended to differential converter that is clocked at 512 kHz. All subsequent analog processing utilizes fully–differential circuitry. The next section is a fully–differential, 5–pole switched–capacitor low–pass filter with a 3.4 kHz frequency cutoff. After this filter is a 3–pole switched–capacitor high–pass filter having a cutoff frequency of about 200 Hz. This high–pass stage has a transmission zero at dc that eliminates any dc coming from the analog input or from accumulated op amp offsets in the preceding filter stages. The last stage of the high–pass filter is an autozeroed sample and hold amplifier.

One bandgap voltage reference generator and digital–to–analog converter (DAC) are shared by the transmit and receive sections. The autozeroed, switched–capacitor bandgap reference generates precise positive and negative reference voltages that are virtually independent of temperature and power supply voltage. A binary–weighted capacitor array (CDAC) forms the chords of the companding structure, while a resistor string (RDAC) implements the linear steps within each chord. The encode process uses the DAC, the voltage reference, and a frame–by–frame autozeroed

comparator to implement a successive–approximation conversion algorithm. All of the analog circuitry involved in the data conversion (the voltage reference, RDAC, CDAC, and comparator) are implemented with a differential architecture.

The receive section includes the DAC described above, a sample and hold amplifier, a 5–pole, 3400 Hz switched capacitor low–pass filter with sinX/X correction, and a 2–pole active smoothing filter to reduce the spectral components of the switched capacitor filter. The output of the smoothing filter is buffered by an amplifier, which is output at the RO+ and RO– pins. These outputs are capable of driving a 4 kΩ load differentially or a 2 kΩ load to the V_{AG} pin. The MC145480 also has a pair of power amplifiers that are connected in a push–pull configuration. The PI pin is the inverting input to the PO– power amplifier. The non–inverting input is internally tied to the V_{AG} pin. This allows this amplifier to be used in an inverting gain circuit with two external resistors. The PO+ amplifier has a gain of minus one, and is internally connected to the PO– output. This complete power amplifier circuit is a differential (push–pull) amplifier with adjustable gain that is capable of driving a 300 Ω load to +12 dBm. The power amplifier may be powered down independently of the rest of the chip by connecting the PI pin to V_{DD}.

POWER–DOWN

There are two methods of putting this device into a low power consumption mode, which makes the device nonfunctional and consumes virtually no power. $\overline{PDI}$ is the power–down input pin which, when taken low, powers down the device. Another way to power the device down is to hold both the FST and FSR pins low. When the chip is powered down, the V_{AG}, TG, RO+, RO–, PO+, PO–, and DT outputs are high impedance. To return the chip to the power–up state, $\overline{PDI}$ must be high and either the FST or the FSR frame sync pulse must be present. The DT output will remain in a high–impedance state for at least two FST pulses after power–up.

MASTER CLOCK

Since this codec–filter design has a single DAC architecture, the MCLK pin is used as the master clock for all analog signal processing including analog–to–digital conversion, digital–to–analog conversion, and for transmit and receive filtering functions of this device. The clock frequency applied to the MCLK pin may be 256 kHz, 512 kHz, 1.536 MHz, 1.544 MHz, 2.048 MHz, 2.56 MHz, or 4.096 MHz. This device has a prescaler that automatically determines the proper divide ratio to use for the MCLK input, which achieves the required 256 kHz internal sequencing clock. The clocking requirements of the MCLK input are independent of the PCM data transfer mode (i.e., Long Frame Sync, Short Frame Sync, IDL mode, or GCI mode).

DIGITAL I/O

The MC145480 is pin selectable for Mu–Law or A–Law. Table 1 shows the 8–bit data word format for positive and negative zero and full scale for both companding schemes (see Tables 3 and 4 at the end of this document for a complete PCM word conversion table). Table NO TAG shows the series of eight PCM words for both Mu–Law and A–Law that correspond to a digital milliwatt. The digital mW is the 1 kHz calibration signal reconstructed by the DAC that defines the absolute gain or 0 dBm0 Transmission Level Point (TLP) of the DAC. The 0 dBm0 level for Mu–Law is 3.17 dB below the maximum level for an unclipped tone signal. The 0 dBm0 level for A–Law is 3.14 dB below the maximum level for an unclipped tone signal. The timing for the PCM data transfer is independent of the companding scheme selected. Refer to Figure NO TAG for a summary and comparison of the four PCM data interface modes of this device.

Table 1. PCM Codes for Zero and Full Scale

Level	Mu–Law			A–Law		
	Sign Bit	Chord Bits	Step Bits	Sign Bit	Chord Bits	Step Bits
+ Full Scale	1	0 0 0	0 0 0 0	1	0 1 0	1 0 1 0
+ Zero	1	1 1 1	1 1 1 1	1	1 0 1	0 1 0 1
– Zero	0	1 1 1	1 1 1 1	0	1 0 1	0 1 0 1
– Full Scale	0	0 0 0	0 0 0 0	0	0 1 0	1 0 1 0

Table 2. PCM Codes for Digital mW

Phase	Mu–Law			A–Law		
	Sign Bit	Chord Bits	Step Bits	Sign Bit	Chord Bits	Step Bits
π/8	0	0 0 1	1 1 1 0	0	0 1 1	0 1 0 0
3π/8	0	0 0 0	1 0 1 1	0	0 1 0	0 0 0 1
5π/8	0	0 0 0	1 0 1 1	0	0 1 0	0 0 0 1
7π/8	0	0 0 1	1 1 1 0	0	0 1 1	0 1 0 0
9π/8	1	0 0 1	1 1 1 0	1	0 1 1	0 1 0 0
11π/8	1	0 0 0	1 0 1 1	1	0 1 0	0 0 0 1
13π/8	1	0 0 0	1 0 1 1	1	0 1 0	0 0 0 1
15π/8	1	0 0 1	1 1 1 0	1	0 1 1	0 1 0 0

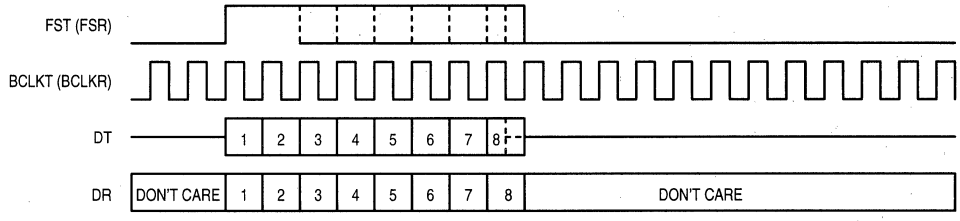


Figure NO TAGa. Long Frame Sync (Transmit and Receive Have Individual Clocking)

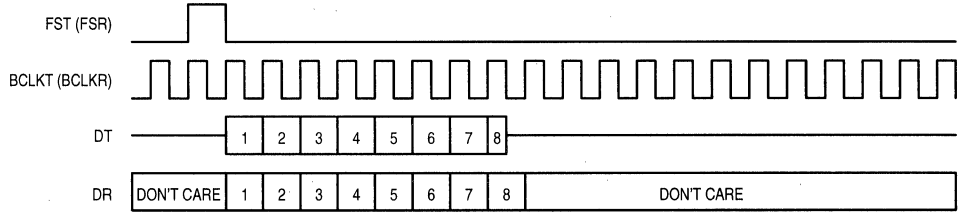


Figure NO TAGb. Short Frame Sync (Transmit and Receive Have Individual Clocking)

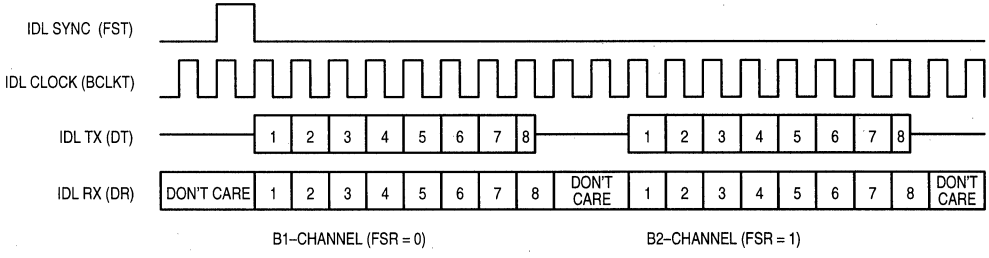


Figure NO TAGc. IDL Interface — BCLKR = 1 (Transmit and Receive Have Common Clocking)

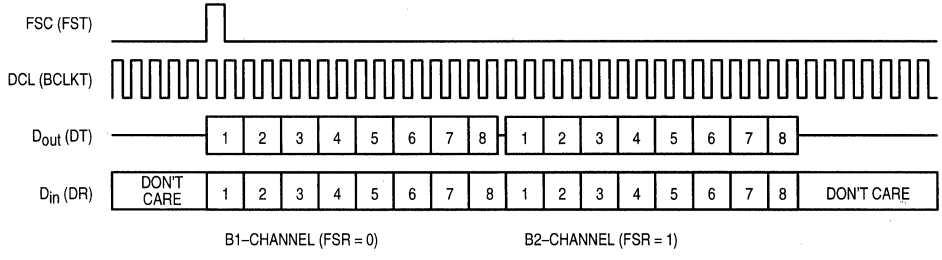


Figure NO TAGd. GCI Interface — BCLKR = 0 (Transmit and Receive Have Common Clocking)

Figure 2. Digital Timing Modes for the PCM Data Interface

Long Frame Sync

Long Frame Sync is the industry name for one type of clocking format that controls the transfer of the PCM data words. (Refer to Figure NO TAGa.) The "Frame Sync" or "Enable" is used for two specific synchronizing functions. The first is to synchronize the PCM data word transfer, and the second is to control the internal analog–to–digital and digital–to–analog conversions. The term "Sync" refers to the function of synchronizing the PCM data word onto or off of the multiplexed serial PCM data bus, which is also known as a PCM highway. The term "Long" comes from the duration of the frame sync measured in PCM data clock cycles. Long Frame Sync timing occurs when the frame sync is used directly as the PCM data output driver enable. This results in the PCM output going low impedance with the rising edge of the transmit frame sync, and remaining low impedance for the duration of the transmit frame sync.

The implementation of Long Frame Sync has maintained compatibility and been optimized for external clocking simplicity. This optimization includes the PCM data output going low impedance with the logical AND of the transmit frame sync (FST) with the transmit data bit clock (BCLKT). The optimization also includes the PCM data output (DT) remaining low impedance until the middle of the LSB (seven and a half PCM data clock cycles) or until the FST pin is taken low, whichever occurs last. This requires the frame sync to be approximately rising edge aligned with the initiation of the PCM data word transfer, but the frame sync does not have a precise timing requirement for the end of the PCM data word transfer. The device recognizes Long Frame Sync clocking when the frame sync is held high for two consecutive falling edges of the transmit data clock. The transmit logic decides on each frame sync whether it should interpret the next frame sync pulse as a Long or a Short Frame Sync. This decision is used for receive circuitry also. The device is designed to prevent PCM bus contention by not allowing the PCM data output to go low impedance for at least two frame sync cycles after power is applied or when coming out of the powered down mode.

The receive side of the device is designed to accept the same frame sync and data clock as the transmit side and to be able to latch its own transmit PCM data word. Thus the PCM digital switch needs to be able to generate only one type of frame sync for use by both transmit and receive sections of the device.

The logical AND of the receive frame sync with the receive data clock tells the device to start latching the 8–bit serial word into the receive data input on the falling edges of the receive data clock. The internal receive logic counts the receive data clock cycles and transfers the PCM data word to the digital–to–analog converter sequencer on the ninth data clock rising edge.

This device is compatible with four digital interface modes. To ensure that this device does not reprogram itself for a different timing mode, the BCLKR pin must change logic state no less than every 125 µs. The minimum PCM data bit clock frequency of 64 kHz satisfies this requirement.

Short Frame Sync

Short Frame Sync is the industry name for the type of clocking format that controls the transfer of the PCM data words (refer to Figure NO TAGb). The "Frame Sync" or "Enable" is used for two specific synchronizing functions. The first is to synchronize the PCM data word transfer, and the second is to control the internal analog–to–digital and digital–to–analog conversions. The term "Sync" refers to the function of synchronizing the PCM data word onto or off of the multiplexed serial PCM data bus, which is also known as a PCM highway. The term "Short" comes from the duration of the frame sync measured in PCM data clock cycles. Short Frame Sync timing occurs when the frame sync is used as a "pre–synchronization" pulse that is used to tell the internal logic to clock out the PCM data word under complete control of the data clock. The Short Frame Sync is held high for one falling data clock edge. The device outputs the PCM data word beginning with the following rising edge of the data clock. This results in the PCM output going low impedance with the rising edge of the transmit data clock, and remaining low impedance until the middle of the LSB (seven and a half PCM data clock cycles).

The device recognizes Short Frame Sync clocking when the frame sync is held high for one and only one falling edge of the transmit data clock. The transmit logic decides on each frame sync whether it should interpret the next frame sync pulse as a Long or a Short Frame Sync. This decision is used for receive circuitry also. The device is designed to prevent PCM bus contention by not allowing the PCM data output to go low impedance for at least two frame sync cycles after power is applied or when coming out of the powered down mode.

The receive side of the device is designed to accept the same frame sync and data clock as the transmit side and to be able to latch its own transmit PCM data word. Thus the PCM digital switch needs to be able to generate only one type of frame sync for use by both transmit and receive sections of the device.

The falling edge of the receive data clock latching a high logic level at the receive frame sync input tells the device to start latching the 8–bit serial word into the receive data input on the following eight falling edges of the receive data clock. The internal receive logic counts the receive data clock cycles and transfers the PCM data word to the digital–to–analog converter sequencer on the rising data clock edge after the LSB has been latched into the device.

This device is compatible with four digital interface modes. To ensure that this device does not reprogram itself for a different timing mode, the BCLKR pin must change logic state no less than every 125 µs. The minimum PCM data bit clock frequency of 64 kHz satisfies this requirement.

Interchip Digital Link (IDL)

The Interchip Digital Link (IDL) Interface is one of two standard synchronous 2B+D ISDN timing interface modes with which this device is compatible. In the IDL mode, the device can communicate in either of the two 64 kbps B channels (refer to Figure NO TAGc for sample timing). The IDL mode is selected when the BCLKR pin is held high for two or more FST (IDL SYNC) rising edges. The digital pins that control the transmit and receive PCM word transfers are reprogrammed to accommodate this mode. The pins affected are FST, FSR, BCLKT, DT, and DR. The IDL Interface consists of four pins: IDL SYNC (FST), IDL CLK (BCLKT), IDL TX (DT), and IDL RX (DR). The IDL interface mode provides access to both the transmit and receive PCM data words with common control clocks of IDL Sync and IDL Clock. In this mode, the

FSR pin controls whether the B1 channel or the B2 channel is used for both transmit and receive PCM data word transfers. When the FSR pin is low, the transmit and receive PCM words are transferred in the B1 channel, and for FSR high the B2 channel is selected. The start of the B2 channel is ten IDL CLK cycles after the start of the B1 channel.

The IDL SYNC (FST, Pin 14) is the input for the IDL frame synchronization signal. The signal at this pin is nominally high for one cycle of the IDL Clock signal and is rising edge aligned with the IDL Clock signal. (Refer to Figure 4 and the IDL Timing specifications for more details.) This event identifies the beginning of the IDL frame. The frequency of the IDL Sync signal is 8 kHz. The rising edge of the IDL SYNC (FST) should be aligned approximately with the rising edge of MCLK. MCLK must be one of the clock frequencies specified in the Digital Switching Characteristics table, and is typically tied to IDL CLK (BCLKT).

The IDL CLK (BCLKT, Pin 12) is the input for the PCM data clock. All IDL PCM transfers and data control sequencing are controlled by this clock following the IDL SYNC. This pin accepts an IDL data clock frequency of 256 kHz to 4.096 MHz.

The IDL TX (DT, Pin 13) is the output for the transmit PCM data word. Data bits are output for the B1 channel on sequential rising edges of the IDL CLK signal beginning after the IDL SYNC pulse. If the B2 channel is selected, then the PCM word transfer starts on the eleventh IDL CLK rising edge after the IDL SYNC pulse. The IDL TX pin will remain low impedance for the duration of the PCM word until the LSB after the falling edge of IDL CLK. The IDL TX pin will remain in a high impedance state when not outputting PCM data or when a valid IDL Sync signal is missing.

The IDL RX (DR, Pin 8) is the input for the receive PCM data word. Data bits are input for the B1 channel on sequential falling edges of the IDL CLK signal beginning after the IDL SYNC pulse. If the B2 channel is selected, then the PCM word is latched in starting on the eleventh IDL CLK falling edge after the IDL SYNC pulse.

General Circuit Interface (GCI)

The General Circuit Interface (GCI) is the second of two standard synchronous 2B+D ISDN timing interface modes with which this device is compatible. In the GCI mode, the device can communicate in either of the two 64 kbps B–channels. (Refer to Figure 2d for sample timing.) The GCI mode is selected when the BCLKR pin is held low for two or more FST (FSC) rising edges. The digital pins that control the transmit and receive PCM word transfers are reprogrammed to accommodate this mode. The pins affected are FST, FSR, BCLKT, DT, and DR. The GCI Interface consists of four pins: FSC (FST), DCL (BCLKT), D_{out} (DT), and D_{in} (DR). The GCI interface mode provides access to both the transmit and receive PCM data words with common control clocks of FSC (frame synchronization clock) and DCL (data clock). In this mode, the FSR pin controls whether the B1 channel or the B2 channel is used for both transmit and receive PCM data word transfers. When the FSR pin is low, the transmit and receive PCM words are transferred in the B1 channel, and for FSR high the B2 channel is selected. The start of the B2 channel is 16 DCL cycles after the start of the B1 channel.

The FSC (FST, Pin 14) is the input for the GCI frame synchronization signal. The signal at this pin is nominally rising edge aligned with the DCL clock signal. (Refer to Figure 6 and the GCI Timing specifications for more details.) This event identifies the beginning of the GCI frame. The frequency of the FSC synchronization signal is 8 kHz. The rising edge of the FSC (FST) should be aligned approximately with the rising edge of MCLK. MCLK must be one of the clock frequencies specified in the Digital Switching Characteristics table, and is typically tied to DCL (BCLKT).

The DCL (BCLKT, Pin 12) is the input for the clock that controls the PCM data transfers. The clock applied at the DCL input is twice the actual PCM data rate. The GCI frame begins with the logical AND of the FSC with the DCL. This event initiates the PCM data word transfers for both transmit and receive. This pin accepts a GCI data clock frequency of 512 kHz to 6.176 MHz for PCM data rates of 256 kHz to 3.088 MHz.

The GCI D_{out} (DT, Pin 13) is the output for the transmit PCM data word. Data bits are output for the B1 channel on alternate rising edges of the DCL clock signal, beginning with the FSC pulse. If the B2 channel is selected, then the PCM word transfer starts on the seventeenth DCL rising edge after the FSC rising edge. The D_{out} pin will remain low impedance for 15–1/2 DCL clock cycles. The D_{out} pin becomes high impedance after the second falling edge of the DCL clock during the LSB of the PCM word. The D_{out} pin will remain in a high–impedance state when not outputting PCM data or when a valid FSC signal is missing.

The D_{in} (DR, Pin 8) is the input for the receive PCM data word. Data bits are latched in for the B1 channel on alternate rising edges of the DCL clock signal, beginning with the second DCL clock after the rising edge of the FSC pulse. If the B2 channel is selected then the PCM word is latched in starting on the eighteenth DCL rising edge after the FSC rising edge.

PRINTED CIRCUIT BOARD LAYOUT CONSIDERATIONS

The MC145480 is manufactured using high–speed CMOS VLSI technology to implement the complex analog signal processing functions of a PCM Codec–Filter. The fully–differential analog circuit design techniques used for this device result in superior performance for the switched capacitor filters, the analog–to–digital converter (ADC) and the digital–to–analog converter (DAC). Special attention was given to the design of this device to reduce the sensitivities of noise, including power supply rejection and susceptibility to radio frequency noise. This special attention to design includes a fifth order low–pass filter, followed by a third order high–pass filter whose output is converted to a digital signal with greater than 75 dB of dynamic range, all operating on a single 5 V power supply. This results in a Mu–Law LSB size for small audio signals of about 386 μV. The typical idle channel noise level of this device is less than one LSB. In addition to the dynamic range of the codec–filter function of this device, the input gain–setting op amp has the capability of greater than 35 dB of gain intended for an electret microphone interface.

This device was designed for ease of implementation, but due to the large dynamic range and the noisy nature of the environment for this device (digital switches, radio telephones, DSP front–end, etc.) special care must be taken to assure optimum analog transmission performance.

PC BOARD MOUNTING

It is recommended that the device be soldered to the PC board for optimum noise performance. If the device is to be used in a socket, it should be placed in a low parasitic pin inductance (generally, low–profile) socket.

POWER SUPPLY, GROUND, AND NOISE CONSIDERATIONS

This device is intended to be used in switching applications which often require plugging the PC board into a rack with power applied. This is known as "hot–rack insertion." In these applications care should be taken to limit the voltage on any pin from going positive of the V_{DD} pins, or negative of the V_{SS} pins. One method is to extend the ground and power contacts of the PCB connector. The device has input protection on all pins and may source or sink a limited amount of current without damage. Current limiting may be accomplished by series resistors between the signal pins and the connector contacts.

The most important considerations for PCB layout deal with noise. This includes noise on the power supply, noise generated by the digital circuitry on the device, and cross coupling digital or radio frequency signals into the audio signals of this device. The best way to prevent noise is to:

1. Keep digital signals as far away from audio signals as possible.
2. Keep radio frequency signals as far away from the audio signals as possible.
3. Use short, low inductance traces for the audio circuitry to reduce inductive, capacitive, and radio frequency noise sensitivities.
4. Use short, low inductance traces for digital and RF circuitry to reduce inductive, capacitive, and radio frequency radiated noise.
5. Bypass capacitors should be connected from the V_{DD} and V_{AG} pins to V_{SS} with minimal trace length. Ceramic monolithic capacitors of about 0.1 μF are acceptable to decouple the device from its own noise. The V_{DD} capacitor helps supply the instantaneous currents of the digital circuitry in addition to decoupling the noise which may be generated by other sections of the device or other circuitry on the power supply. The V_{AG} decoupling capacitor helps to reduce the impedance of the V_{AG} pin to V_{SS} at frequencies above the bandwidth of the V_{AG} generator, which reduces the susceptibility to RF noise.
6. Use a short, wide, low inductance trace to connect the V_{SS} ground pin to the power supply ground. The V_{SS} pin is the digital ground and the most negative power supply pin for the analog circuitry. All analog signal processing is referenced to the V_{AG} pin, but because digital and RF circuitry will probably be powered by this same ground, care must be taken to minimize high frequency noise in the V_{SS} trace. Depending on the application, a double–sided PCB with a V_{SS} ground plane connecting all of the digital and analog V_{SS} pins together would be a good grounding method. A multilayer PC board with a ground plane connecting all of the digital and analog V_{SS} pins together would be the optimal ground configuration. These methods will result in the lowest resistance and the lowest inductance in the ground circuit. This is important to reduce voltage spikes in the ground circuit resulting from the high speed digital current spikes. The magnitude of digitally induced voltage spikes may be hundreds of times larger than the analog signal the device is required to digitize.
7. Use a short, wide, low inductance trace to connect the V_{DD} power supply pin to the 5 V power supply. Depending on the application, a double–sided PCB with V_{DD} bypass capacitors to the V_{SS} ground plane, as described above, may complete the low impedance coupling for the power supply. For a multilayer PC board with a power plane, connecting all of the V_{DD} pins to the power plane would be the optimal power distribution method. The integrated circuit layout and packaging considerations for the 5 V V_{DD} power circuit are essentially the same as for the V_{SS} ground circuit.
8. The V_{AG} pin is the reference for all analog signal processing. In some applications the audio signal to be digitized may be referenced to the V_{SS} ground. To reduce the susceptibility to noise at the input of the ADC section, the three–terminal op amp may be used in a differential to single–ended circuit to provide level conversion from the V_{SS} ground to the V_{AG} ground with noise cancellation. The op amp may be used for more than 35 dB of gain in microphone interface circuits, which will require a compact layout with minimum trace lengths as well as isolation from noise sources. It is recommended that the layout be as symmetrical as possible to avoid any imbalances which would reduce the noise cancelling benefits of this differential op amp circuit. Refer to the application schematics for examples of this circuitry.

   If possible, reference audio signals to the V_{AG} pin instead of to the V_{SS} pin. Handset receivers and telephone line interface circuits using transformers may be audio signal referenced completely to the V_{AG} pin. Refer to the application schematics for examples of this circuitry. The V_{AG} pin cannot be used for ESD or line protection.
9. For applications using multiple MC145480 PCM Codec–Filters, the V_{AG} pins cannot be tied together. The V_{AG} pins are capable of sourcing and sinking current and will each be driving the node, which will result in large contention currents, crosstalk susceptibilities, and increased noise.
10. The MC145480 is fabricated with advanced high–speed CMOS technology that is capable of responding to noise pulses on the clock pins of 1 ns or less. It should be noted that noise pulses of such short duration may not be seen with oscilloscopes that have less bandwidth than 600 MHz. The most often encountered sources of clock noise spikes are inductive or capacitive coupling of high–speed logic signals, and ground bounce. The best solution for addressing clock spikes from coupling is to separate the traces and use short low inductance PC board traces. To address ground bounce problems, all integrated circuits should have high frequency bypass capacitors directly across their power supply pins, with low inductance traces for ground and power supply. A less than optimum solution may be to limit the bandwidth of the trace by adding series resistance and/or capacitance at the input pin.

MAXIMUM RATINGS (Voltages Referenced to V_{SS} Pin)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	– 0.5 to 6	V
Voltage on Any Analog Input or Output Pin		V_{SS} – 0.3 to V_{DD} + 0.3	V
Voltage on Any Digital Input or Output Pin		V_{SS} – 0.3 to V_{DD} + 0.3	V
Operating Temperature Range	T_A	– 40 to + 85	°C
Storage Temperature Range	T_{stg}	– 85 to +150	°C

POWER SUPPLY (T_A = – 40 to + 85°C)

Characteristics		Min	Typ	Max	Unit
DC Supply Voltage		4.75	5.0	5.25	V
Active Power Dissipation	(No Load, PI ≥ V_{DD} – 0.5 V) (No Load, PI ≤ V_{DD} – 1.5 V)	— —	23 25	33 35	mW
Power–Down Dissipation (V_{IH} for Logic Levels Must be ≥ 3.0 V)	$\overline{PDI}$ = V_{SS} FST and FSR = V_{SS}, $\overline{PDI}$ = V_{DD}	— —	0.01 0.1	0.5 1.0	mW

DIGITAL LEVELS (V_{DD} = + 5 V ± 5%, V_{SS} = 0 V, T_A = – 40 to + 85°C)

Characteristics	Symbol	Min	Max	Unit
Input Low Voltage	V_{IL}	—	0.6	V
Input High Voltage	V_{IH}	2.2	—	V
Output Low Voltage (DT Pin, I_{OL}= 2.5 mA)	V_{OL}	—	0.4	V
Output High Voltage (DT Pin, I_{OH} = – 2.5 mA)	V_{OH}	V_{DD} – 0.5	—	V
Input Low Current (V_{SS} ≤ V_{in} ≤ V_{DD})	I_{IL}	– 10	+ 10	μA
Input High Current (V_{SS} ≤ V_{in} ≤ V_{DD})	I_{IH}	– 10	+ 10	μA
Output Current in High Impedance State (V_{SS} ≤ DT ≤ V_{DD})	I_{OZ}	– 10	+ 10	μA
Input Capacitance of Digital Pins (Except DT)	C_{in}	—	10	pF
Input Capacitance of DT Pin when High–Z	C_{out}	—	15	pF

ANALOG ELECTRICAL CHARACTERISTICS (V_{DD} = + 5 V ± 5%, V_{SS} = 0 V, T_A = – 40 to + 85°C)

Characteristics		Min	Typ	Max	Unit
Input Current	TI+, TI–	—	± 0.1	± 1.0	mA
AC Input Impedance to V_{AG} (1 kHz)	TI+, TI–	—	1.0	—	MΩ
Input Capacitance	TI+, TI–	—	—	10	pF
Input Offset Voltage of TG Op Amp	TI+, TI–	—	—	± 5	mV
Input Common Mode Voltage Range	TI+, TI–	1.2		V_{DD} – 2.0	V
Input Common Mode Rejection Ratio	TI+, TI–	—	60	—	dB
Gain Bandwidth Product (10 kHz) of TG Op Amp ($R_L \geq$ 10 kΩ)		—	3000	—	kHz
DC Open Loop Gain of TG Op Amp ($R_L \geq$ 10 kΩ)		—	95	—	dB
Equivalent Input Noise (C–Message) Between TI+ and TI– at TG		—	– 30	—	dBrnC
Output Load Capacitance for TG Op Amp		0	—	100	pF
Output Voltage Range for TG (R_L = 10 kΩ to V_{AG}) (R_L = 2 kΩ to V_{AG})		 0.5 1.0	 — —	 V_{DD} – 0.5 V_{DD} – 1.0	V
Output Current (0.5 V ≤ $V_{out} \leq V_{DD}$ – 0.5 V)	TG, RO+, RO–	± 1.0	—	—	mA
Output Load Resistance to V_{AG}	TG, RO+, and RO–	2	—	—	kΩ
Output Impedance (0 to 3.4 kHz)	RO+ or RO–	—	1	—	Ω
Output Load Capacitance	RO+ or RO–	0	—	500	pF
DC Output Offset Voltage of RO+ or RO– Referenced to V_{AG}		—	—	± 25	mV
V_{AG} Output Voltage Referenced to V_{SS} (No Load)		2.2	2.4	2.6	V
V_{AG} Output Current with ± 25 mV Change in Output Voltage		± 2.0	± 10	—	mA
Power Supply Rejection Ratio (0 to 100 kHz @100 mVrms Applied to V_{DD}, C–Message Weighting, All Analog Signals Referenced to V_{AG} Pin)	Transmit Receive	50 50	80 75	— —	dBC
Power Drivers PI, PO+, PO–					
Input Current (V_{AG} – 0.5 V ≤ PI ≤ V_{AG} + 0.5 V)	PI	—	± 0.05	± 1.0	mA
Input Resistance (V_{AG} – 0.5 V ≤ PI ≤ V_{AG} + 0.5 V)	PI	10	—	—	MΩ
Input Offset Voltage	PI	—	—	± 20	mV
Output Offset Voltage of PO+ Relative to PO– (Inverted Unity Gain for PO–)		—	—	± 50	mV
Output Current (V_{SS} + 0.7 V ≤ PO+ or PO– ≤ V_{DD} – 0.7 V)		± 10	—	—	mA
PO+ or PO– Output Resistance (Inverted Unity Gain for PO–)		—	1	—	Ω
Gain Bandwidth Product (10 kHz, Open Loop for PO–)		—	1000	—	kHz
Load Capacitance (PO+ or PO– to V_{AG}, or PO+ to PO–)		0	—	1000	pF
Gain of PO+ Relative to PO– (R_L = 300 Ω, + 3 dBm0, 1 kHz)		– 0.2	0	+ 0.2	dB
Total Signal to Distortion at PO+ and PO– with a 300 Ω Differential Load		45	60	—	dBC
Power Supply Rejection Ratio (0 to 25 kHz @ 100 mVrms Applied to V_{DD}. PO– Connected to PI. Differential or Measured Referenced to V_{AG} Pin.)	0 to 4 kHz 4 to 25 kHz	40 —	55 40	— —	dB

ANALOG TRANSMISSION PERFORMANCE

(V_{DD} = + 5 V ± 5%, V_{SS} = 0 V, All Analog Signals Referenced to V_{AG}, 0 dBm0 = 0.775 Vrms = + 0 dBm @ 600 Ω, FST = FSR = 8 kHz, BCLKT = MCLK = 2.048 MHz Synchronous Operation, T_A = – 40 to + 85°C, Unless Otherwise Noted)

Characteristics	End–to–End		A/D		D/A		Units
	Min	Max	Min	Max	Min	Max	
Absolute Gain (0 dBm0 @ 1.02 kHz, T_A = 25°C, V_{DD} = 5.0 V)	—	—	– 0.25	+ 0.25	– 0.25	+ 0.25	dB
Absolute Gain Variation with Temperature 0 to + 70°C	—	—	—	± 0.03	—	± 0.03	dB
– 40 to + 85°C	—	—	—	± 0.05	—	± 0.05	
Absolute Gain Variation with Power Supply (T_A = 25°C)	—	—	—	± 0.03	—	± 0.04	dB
Gain vs Level Tone (Mu–Law, Relative to – 10 dBm0, 1.02 kHz)							dB
+ 3 to – 40 dBm0 @ 0 to + 85°C	—	—	– 0.25	+ 0.25	– 0.20	+ 0.20	
+ 3 to – 40 dBm0 @ – 40 to 0°C	—	—	– 0.25	+ 0.25	– 0.25	+ 0.25	
– 40 to – 50 dBm0 @ 0 to + 85°C	—	—	– 0.8	+ 0.8	– 0.5	+ 0.5	
– 40 to – 50 dBm0 @ – 40 to 0°C	—	—	– 0.8	+ 0.8	– 0.9	+ 0.9	
– 50 to – 55 dBm0 @ 0 to + 85°C	—	—	– 1.3	+ 1.3	– 1.0	+ 1.0	
– 50 to – 55 dBm0 @ – 40 to 0°C	—	—	– 1.3	+ 1.3	– 1.8	+ 1.8	
Gain vs Level Pseudo Noise, CCITT G.712 – 10 to – 40 dBm0	—	—	– 0.25	+ 0.25	– 0.25	+ 0.25	dB
(A–Law, Relative to – 10 dBm0) – 40 to – 50 dBm0	—	—	– 0.60	+ 0.30	– 0.30	+ 0.30	
– 50 to – 55 dBm0	—	—	– 1.00	+ 0.45	– 0.45	+ 0.45	
Total Distortion, 1.02 kHz Tone (Mu–Law, C–Message Weighting)							dBC
+ 3 dBm0	—	—	34	—	34	—	
0 to – 30 dBm0	—	—	36	—	36	—	
– 40 dBm0 @ 0 to + 85°C	—	—	30	—	30	—	
– 40 dBm0 @ – 40 to 0°C	—	—	28.5	—	28.5	—	
– 45 dBm0	—	—	25	—	25	—	
Total Distortion, Pseudo Noise, CCITT G.714 (A–Law) – 3 dBm0	—	—	30.0	—	30.0	—	dB
– 6 to – 27 dBm0	—	—	35.0	—	36.0	—	
– 34 dBm0	—	—	34.0	—	34.5	—	
– 40 dBm0 @ 0 to + 85°C	—	—	28.5	—	29.5	—	
– 40 dBm0 @ – 40 to 0°C	—	—	28.0	—	28.5	—	
– 55 dBm0	—	—	13.5	—	14.5	—	
Idle Channel Noise (For End–to–End and A/D, See Note 1)							
(Mu–Law, C–Message Weighted)	—	—	—	18	—	11	dBrnc0
(A–Law, Psophometric Weighted)	—	—	—	– 68	—	– 78	dBm0p
Frequency Response (Relative to 1.02 kHz @ 0 dBm0) 15 Hz	—	—	—	– 40	– 0.5	0	dB
50 Hz	—	—	—	– 30	– 0.5	0	
60 Hz	—	—	—	– 26	– 0.5	0	
200 Hz	—	—	– 1.0	– 0.4	– 0.5	0	
300 to 3000 Hz	—	—	– 0.20	+ 0.15	– 0.15	+ 0.15	
3300 Hz	—	—	– 0.35	+ 0.15	– 0.35	+ 0.15	
3400 Hz	—	—	– 0.8	0	– 0.8	0	
4000 Hz	—	—	—	– 14	—	– 14	
4600 Hz to 100 kHz	—	—	—	– 32	—	30	
In–Band Spurious (1.02 kHz @ 0 dBm0, Transmit and Receive)							dB
300 to 3000 Hz	—	– 48	—	– 48	—	– 48	
Out–of–Band Spurious at RO+ (300 to 3400 Hz @ 0 dBm0 in)							dB
4600 to 7600 Hz	—	– 30	—	—	—	– 30	
7600 to 8400 Hz	—	– 40	—	—	—	– 40	
8400 to 100,000 Hz	—	– 30	—	—	—	– 30	
Idle Channel Noise Selective (8 kHz, Input = V_{AG}, 30 Hz Bandwidth)	—	– 70	—	—	—	– 70	dBm0
Absolute Delay (1600 Hz)	—	—	—	315	—	205	µs
Group Delay Referenced to 1600 Hz 500 to 600 Hz	—	—	—	210	– 40	—	µs
600 to 800 Hz	—	—	—	130	– 40	—	
800 to 1000 Hz	—	—	—	70	– 40	—	
1000 to 1600 Hz	—	—	—	35	– 30	—	
1600 to 2600 Hz	—	—	—	70	—	85	
2600 to 2800 Hz	—	—	—	95	—	110	
2800 to 3000 Hz	—	—	—	145	—	175	
Crosstalk of 1020 Hz @ 0 dBm0 from A/D or D/A (Note 2)	—	—	—	– 75	—	– 70	dB
Intermodulation Distortion of Two Frequencies of Amplitudes (– 4 to – 21 dBm0 from the Range 300 to 3400 Hz)	—	– 41	—	– 41	—	– 41	dB

NOTES:
1. Extrapolated from a 1020 Hz @ – 50 dBm0 distortion measurement to correct for encoder enhancement.
2. Selectively measured while stimulated with 2667 Hz @ – 50 dBm0.

DIGITAL SWITCHING CHARACTERISTICS, LONG FRAME SYNC AND SHORT FRAME SYNC

(V_{DD} = + 5 V ± 5%, V_{SS} = 0 V, All Digital Signals Referenced to V_{SS}, T_A = – 40 to + 85°C, C_L = 150 pF, Unless Otherwise Noted)

Ref. No.	Characteristics	Min	Typ	Max	Unit
1	Master Clock Frequency for MCLK	— — — — — — —	256 512 1536 1544 2048 2560 4096	— — — — — — —	kHz
1	MCLK Duty Cycle for 256 kHz Operation	45	—	55	%
2	Minimum Pulse Width High for MCLK (Frequencies of 512 kHz or Greater)	50	—	—	ns
3	Minimum Pulse Width Low for MCLK (Frequencies of 512 kHz or Greater)	50	—	—	ns
4	Rise Time for All Digital Signals	—	—	50	ns
5	Fall Time for All Digital Signals	—	—	50	ns
6	Setup Time from MCLK Low to FST High	50	—	—	ns
7	Setup Time from FST High to MCLK Low	50	—	—	ns
8	Bit Clock Data Rate for BCLKT or BCLKR	64	—	4096	kHz
9	Minimum Pulse Width High for BCLKT or BCLKR	50	—	—	ns
10	Minimum Pulse Width Low for BCLKT or BCLKR	50	—	—	ns
11	Hold Time from BCLKT (BCLKR) Low to FST (FSR) High	20	—	—	ns
12	Setup Time for FST (FSR) High to BCLKT (BCLKR) Low	80	—	—	ns
13	Setup Time from DR Valid to BCLKR Low	0	—	—	ns
14	Hold Time from BCLKR Low to DR Invalid	50	—	—	ns
	LONG FRAME SPECIFIC TIMING				
15	Hold Time from 2nd Period of BCLKT (BCLKR) Low to FST (FSR) Low	50	—	—	ns
16	Delay Time from FST or BCLKT, Whichever is Later, to DT for Valid MSB Data	—	—	60	ns
17	Delay Time from BCLKT High to DT for Valid Chord and Step Bit Data	—	—	60	ns
18	Delay Time from the Later of the 8th BCLKT Falling Edge, or the Falling Edge of FST to DT Output High Impedance	10	—	60	ns
19	Minimum Pulse Width Low for FST or FSR	50	—	—	ns
	SHORT FRAME SPECIFIC TIMING				
20	Hold Time from BCLKT (BCLKR) Low to FST (FSR) Low	50	—	—	ns
21	Setup Time from FST (FSR) Low to MSB Period of BCLKT (BCLKR) Low	50	—	—	ns
22	Delay Time from BCLKT High to DT Data Valid	10	—	60	ns
23	Delay Time from the 8th BCLKT Low to DT Output High Impedance	10	—	60	ns

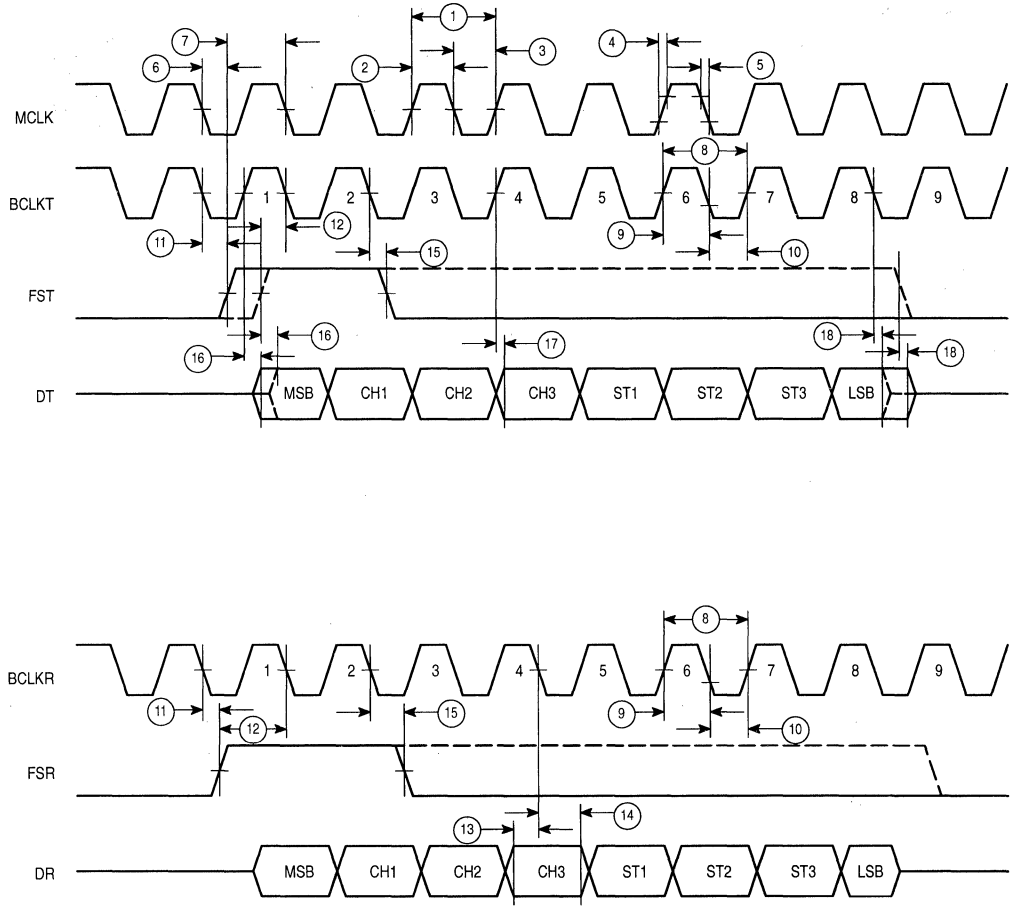


Figure 3. Long Frame Sync Timing

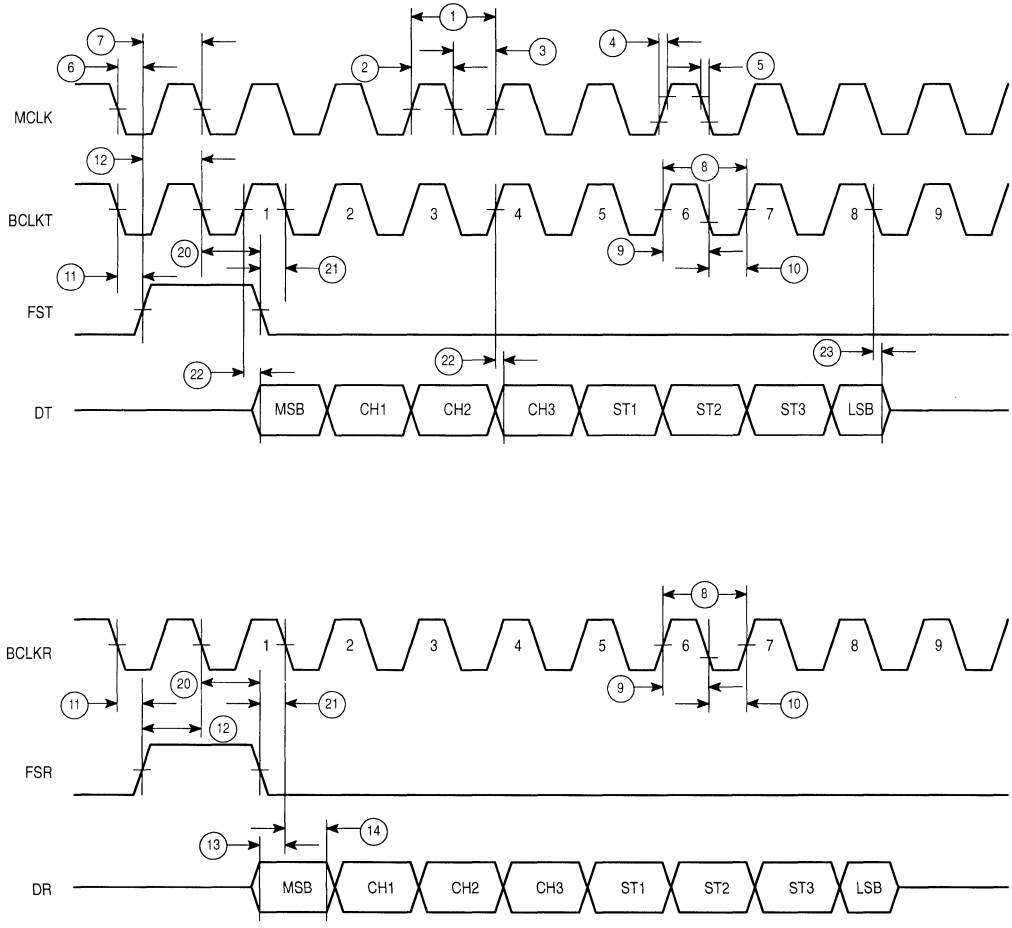


Figure 4. Short Frame Sync Timing

DIGITAL SWITCHING CHARACTERISTICS FOR IDL MODE

(V_{DD} = 5.0 V ± 5%, T_A = – 40 to + 85°C, C_L = 150 pF, See Figure 5 and Note 1)

Ref. No.	Characteristics	Min	Max	Unit
31	Time Between Successive IDL Syncs	Note 2		
32	Hold Time of IDL SYNC After Falling Edge of IDL CLK	20	—	ns
33	Setup Time of IDL SYNC Before Falling Edge IDL CLK	60	—	ns
34	IDL Clock Frequency	256	4096	kHz
35	IDL Clock Pulse Width High	50	—	ns
36	IDL Clock Pulse Width Low	50	—	ns
37	Data Valid on IDL RX Before Falling Edge of IDL CLK	20	—	ns
38	Data Valid on IDL RX After Falling Edge of IDL CLK	75	—	ns
39	Falling Edge of IDL CLK to High–Z on IDL TX	10	50	ns
40	Rising Edge of IDL CLK to Low–Z and Data Valid on IDL TX	10	60	ns
41	Rising Edge of IDL CLK to Data Valid on IDL TX	—	50	ns

NOTES:

1. Measurements are made from the point at which the logic signal achieves the guaranteed minimum or maximum logic level.
2. In IDL mode, both transmit and receive 8–bit PCM words are accessed during the B1 channel, or both transmit and receive 8–bit PCM words are accessed during the B2 channel as shown in Figure 5. IDL accesses must occur at a rate of 8 kHz (125 µs interval).

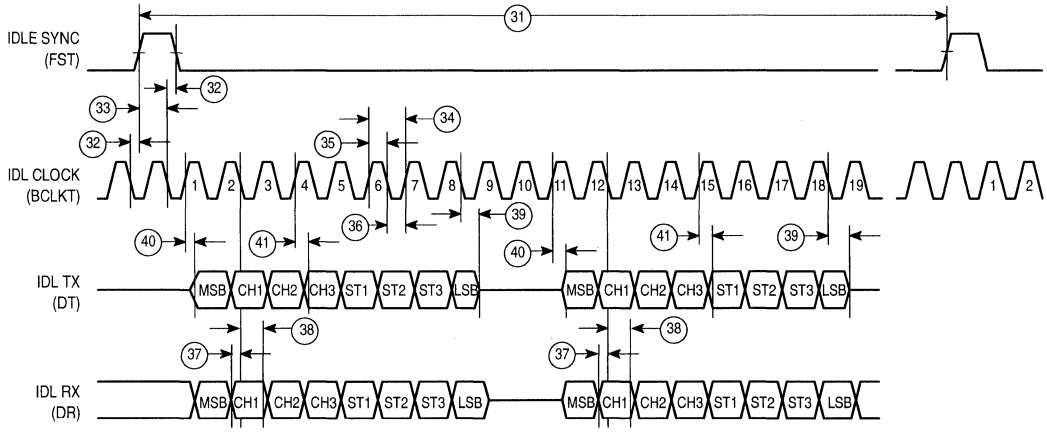


Figure 5. IDL Interface Timing

DIGITAL SWITCHING CHARACTERISTICS FOR GCI MODE

(V_{DD} = 5.0 V ± 5%, T_A = – 40 to + 85°C, C_L = 150 pF, See Figure 6 and Note 1)

Ref. No.	Characteristics	Min	Max	Unit
42	Time Between Successive FSC Pulses	Note 2		
43	DCL Clock Frequency	512	6176	kHz
44	DCL Clock Pulse Width High	50	—	ns
45	DCL Clock Pulse Width Low	50	—	ns
46	Hold Time of FSC After Falling Edge of DCL	20	—	ns
47	Setup Time of FSC to DCL Falling Edge	60	—	ns
48	Rising Edge of DCL (After Rising Edge of FSC) to Low Impedance and Valid Data of D_{out}	—	60	ns
49	Rising Edge of FSC (While DCL is High) to Low Impedance and Valid Data of D_{out}	—	60	ns
50	Rising Edge of DCL to Valid Data on D_{out}	—	60	ns
51	Second DCL Falling Edge During LSB to High Impedance of D_{out}	10	50	ns
52	Setup Time of D_{in} Before Rising Edge of DCL	20	—	ns
53	Hold Time of D_{in} After DCL Rising Edge	—	60	ns

NOTES:
1. Measurements are made from the point at which the logic signal achieves the guaranteed minimum or maximum logic level.
2. In GCI mode, both transmit and receive 8–bit PCM words are accessed during the B1 channel, or both transmit and receive 8–bit PCM words are accessed during the B2 channel as shown in Figure 6. GCI accesses must occur at a rate of 8 kHz (125 µs interval).

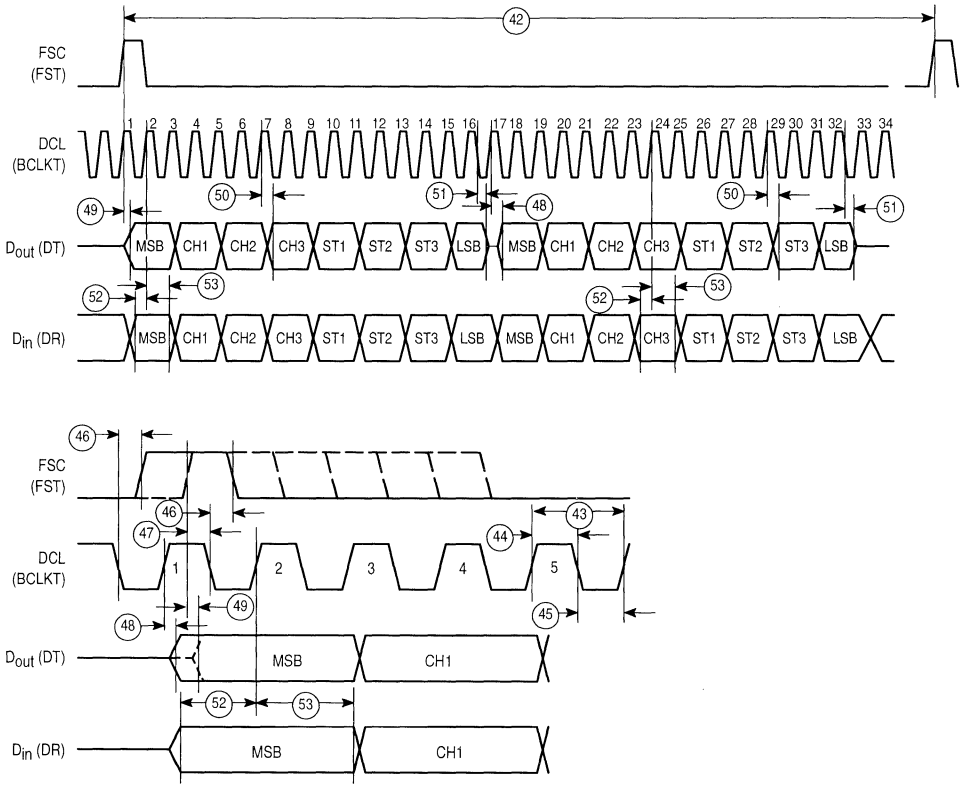


Figure 6. GCI Interface Timing

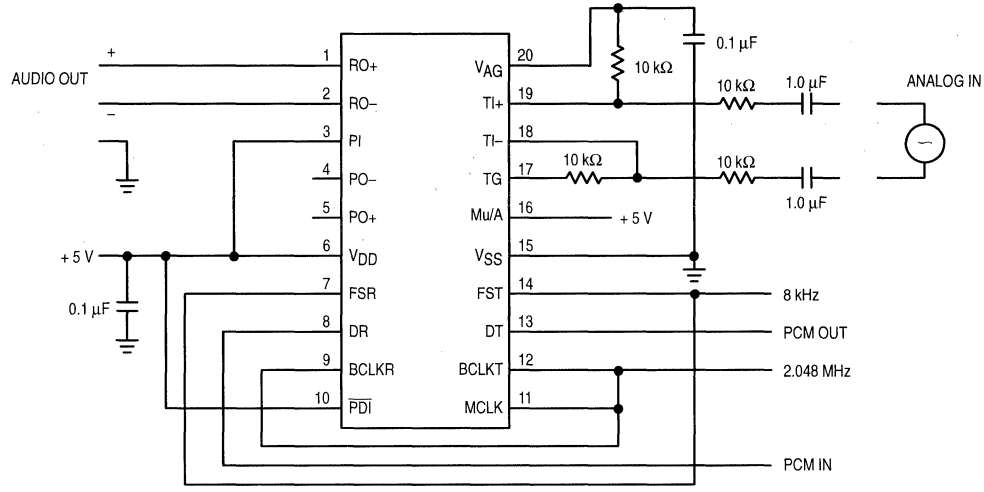


Figure 7. MC145480 Test Circuit with Differential Input and Output

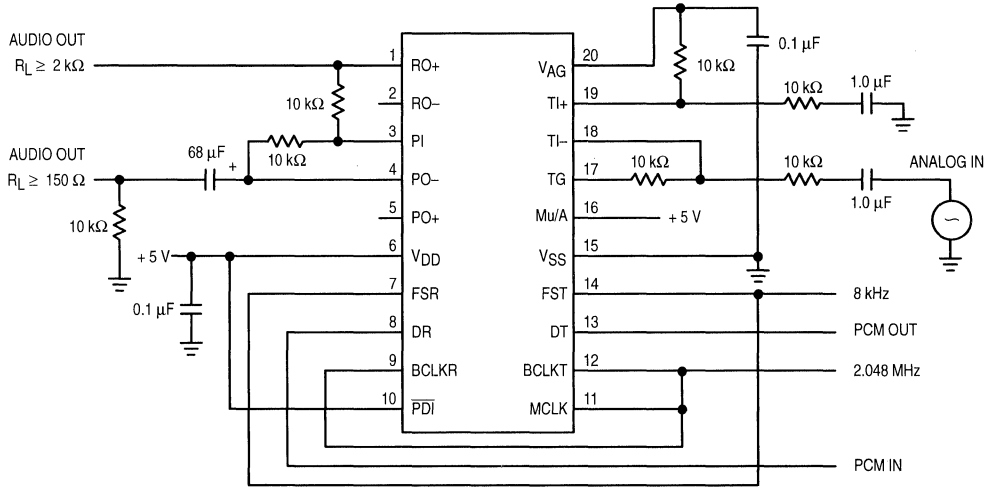


Figure 8. MC145480 Test Circuit with Input and Output Referenced to V_{SS}

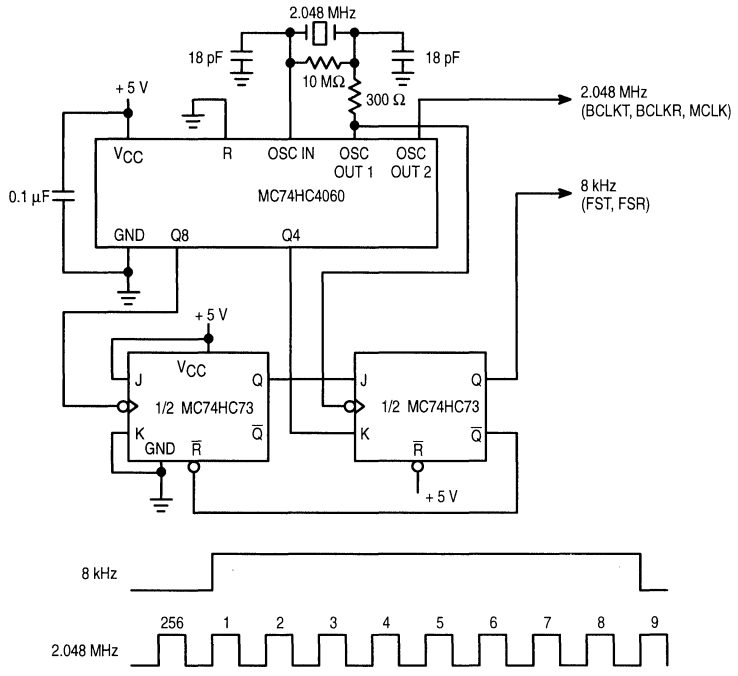


Figure 9. Long Frame Sync Clock Circuit for 2.048 MHz

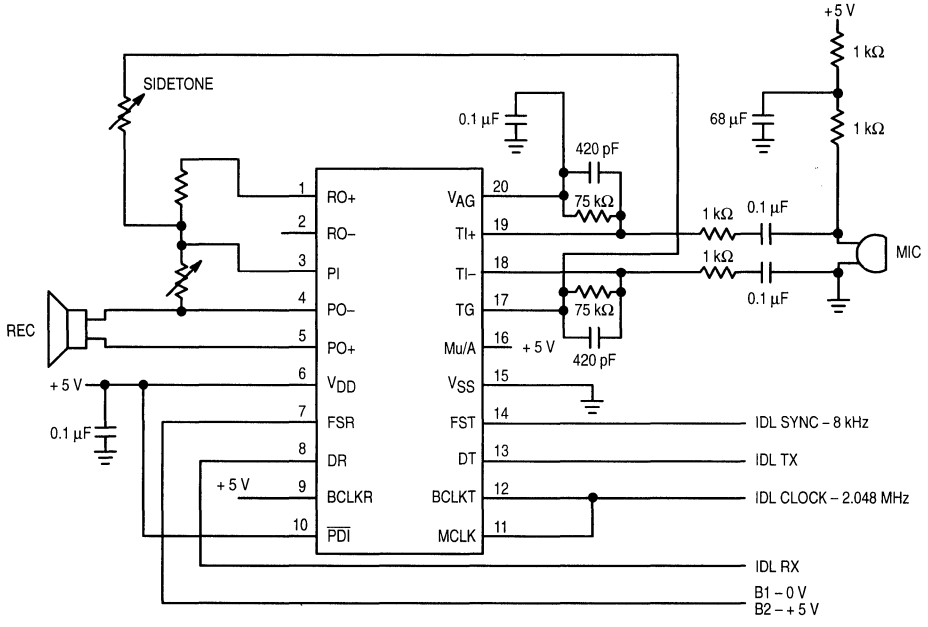


Figure 10. MC145480 Analog Interface to Handset with IDL Clocking

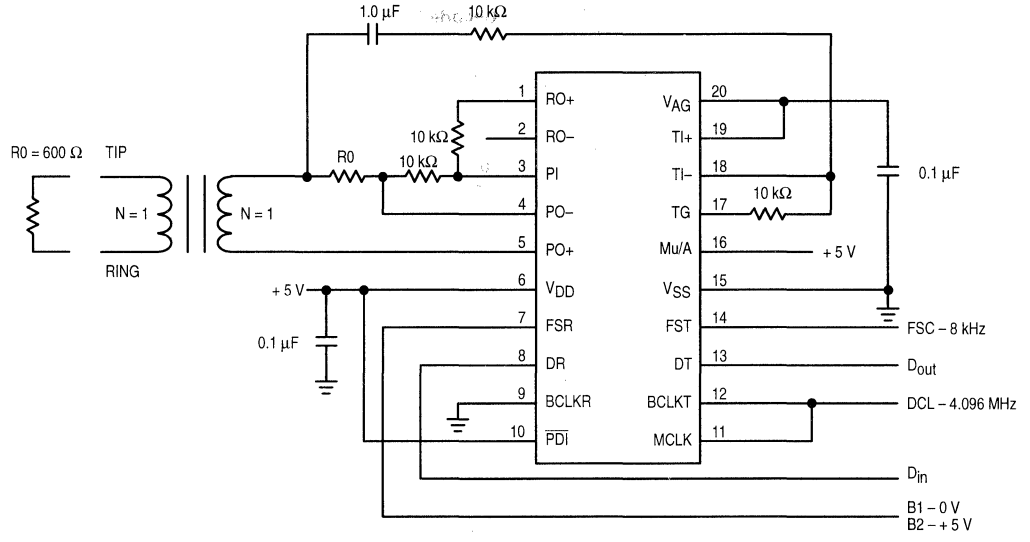


Figure 11. MC145480 Transformer Interface to 600 Ω Telephone Line with GCI Clocking

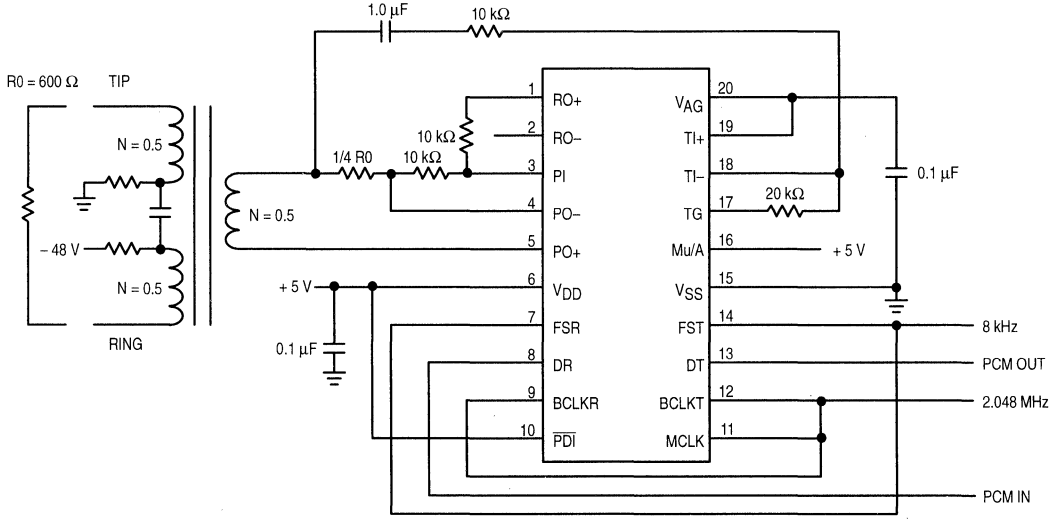


Figure 12. MC145480 Step–Up Transformer Interface to 600 Ω Telephone Line

Table 3. Mu–Law Encode–Decode Characteristics

Chord Number	Number of Steps	Step Size	Normalized Encode Decision Levels	Digital Code 1 Sign	2 Chord	3 Chord	4 Chord	5 Step	6 Step	7 Step	8 Step	Normalized Decode Levels
			8159									
				1	0	0	0	0	0	0	0	8031
8	16	256	7903									
			⋮					⋮				⋮
			4319									
				1	0	0	0	1	1	1	1	4191
			4063									
			⋮					⋮				⋮
7	16	128	2143									
				1	0	0	1	1	1	1	1	2079
			2015									
			⋮					⋮				⋮
6	16	64	1055									
				1	0	1	0	1	1	1	1	1023
			991									
			⋮					⋮				⋮
5	16	32	511									
				1	0	1	1	1	1	1	1	495
			479									
			⋮					⋮				⋮
4	16	16	239									
				1	1	0	0	1	1	1	1	231
			223									
			⋮					⋮				⋮
3	16	8	103									
				1	1	0	1	1	1	1	1	99
			95									
			⋮					⋮				⋮
2	16	4	35									
				1	1	1	0	1	1	1	1	33
			31									
			⋮					⋮				⋮
1	15	2	3									
				1	1	1	1	1	1	1	0	2
	1	1	1									
				1	1	1	1	1	1	1	1	0
			0									

NOTES:
1. Characteristics are symmetrical about analog zero with sign bit = 0 for negative analog values.
2. Digital code includes inversion of all magnitude bits.

Table 4. A–Law Encode–Decode Characteristics

Chord Number	Number of Steps	Step Size	Normalized Encode Decision Levels	Digital Code 1 Sign	2 Chord	3 Chord	4 Chord	5 Step	6 Step	7 Step	8 Step	Normalized Decode Levels
			4096									
7	16	128	3968	1	0	1	0	1	0	1	0	4032
			⋮					⋮				⋮
			2176									
			2048	1	0	1	0	0	1	0	1	2112
6	16	64	⋮					⋮				⋮
			1088									
			1024	1	0	1	1	0	1	0	1	1056
5	16	32	⋮					⋮				⋮
			544									
			512	1	0	0	0	0	1	0	1	528
4	16	16	⋮					⋮				⋮
			272									
			256	1	0	0	1	0	1	0	1	264
3	16	8	⋮					⋮				⋮
			136									
			128	1	1	1	0	0	1	0	1	132
2	16	4	⋮					⋮				⋮
			68									
			64	1	1	1	1	0	1	0	1	66
1	32	2	⋮					⋮				⋮
			2									
			0	1	1	0	1	0	1	0	1	1

NOTES:
1. Characteristics are symmetrical about analog zero with sign bit = 0 for negative analog values.
2. Digital code includes inversion of all even numbered bits.

MC145481

Product Preview

3 V PCM Codec-Filter

The MC145481 is a general purpose per channel PCM Codec–Filter with pin selectable Mu–Law or A–Law companding, and is offered in 20–pin DIP, SOG, and SSOP packages. This device performs the voice digitization and reconstruction as well as the band limiting and smoothing required for PCM systems. This device is designed to operate in both synchronous and asynchronous applications and contains an on–chip precision reference voltage.

This device has an input operational amplifier whose output is the input to the encoder section. The encoder section immediately low–pass filters the analog signal with an active R–C filter to eliminate very high frequency noise from being modulated down to the passband by the switched capacitor filter. From the active R–C filter, the analog signal is converted to a differential signal. From this point, all analog signal processing is done differentially. This allows processing of an analog signal that is twice the amplitude allowed by a single–ended design, which reduces the significance of noise to both the inverted and non–inverted signal paths. Another advantage of this differential design is that noise injected via the power supplies is a common–mode signal that is cancelled when the inverted and non–inverted signals are recombined. This dramatically improves the power supply rejection ratio.

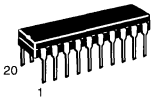
After the differential converter, a differential switched capacitor filter bandpasses the analog signal from 200 Hz to 3400 Hz before the signal is digitized by the differential compressing A/D converter.

The decoder accepts PCM data and expands it using a differential D/A converter. The output of the D/A is low–pass filtered at 3400 Hz and sinX/X compensated by a differential switched capacitor filter. The signal is then filtered by an active R–C filter to eliminate the out of band energy of the switched capacitor filter.

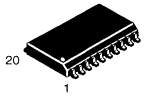
The MC145481 PCM Codec–Filter accepts a variety of clock formats, including Short Frame Sync, Long Frame Sync, IDL, and GCI timing environments.

The MC145481 PCM Codec–Filter utilizes CMOS due to its reliable low–power performance and proven capability for complex analog/digital VLSI functions.

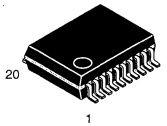
- Single 3 V Power Supply
- Typical Power Dissipation of 12 mW, Power–Down of 0.01 mW
- Fully Differential Analog Circuit Design for Lowest Noise
- Transmit Band–Pass and Receive Low–Pass Filters On–Chip
- Active R–C Pre–Filtering and Post–Filtering
- Mu–Law and A–Law Companding by Pin Selection
- On–Chip Precision Reference Voltage (0.886 V) for a –5 dBm TLP @ 600 Ω
- Push–Pull 300 Ω Power Drivers with External Gain Adjust



P SUFFIX
PLASTIC DIP
CASE 738



DW SUFFIX
SOG PACKAGE
CASE 751D

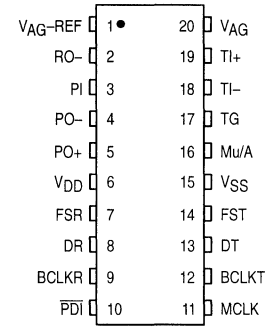


SD SUFFIX
SSOP
CASE 940C

ORDERING INFORMATION

MC145481P	Plastic DIP
MC145481DW	SOG Package
MC145481SD	SSOP

PIN ASSIGNMENT



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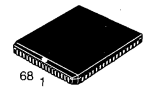
MC145488



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2

Technical Summary
Dual Data Link Controller

This technical summary gives a brief overview of the MC145488 Dual Data Link Controller. The MC145488 is a two–channel ISDN LAPD controller with an on–chip direct memory access (DMA) controller. It is intended for ISDN terminal and switch applications where one or two channels of data will use HDLC–type protocols. The DDLC can also be used in local area, wide area network, and bridge router applications. Each serial interface can be clocked at data rates up to 10 Mbps. The DDLC can operate with microprocessors using clock frequencies up to 20.5 MHz.

The DDLC is ideally suited for use with the MC145474 S/T–Transceiver. The interchip digital link (IDL) easily connects the chips together, providing a powerful layer one/layer two ISDN solution. A serial control port is provided to efficiently control the MC145474 or other ISDN family devices. The DDLC is compatible with 68000 and 80186 bus structures.

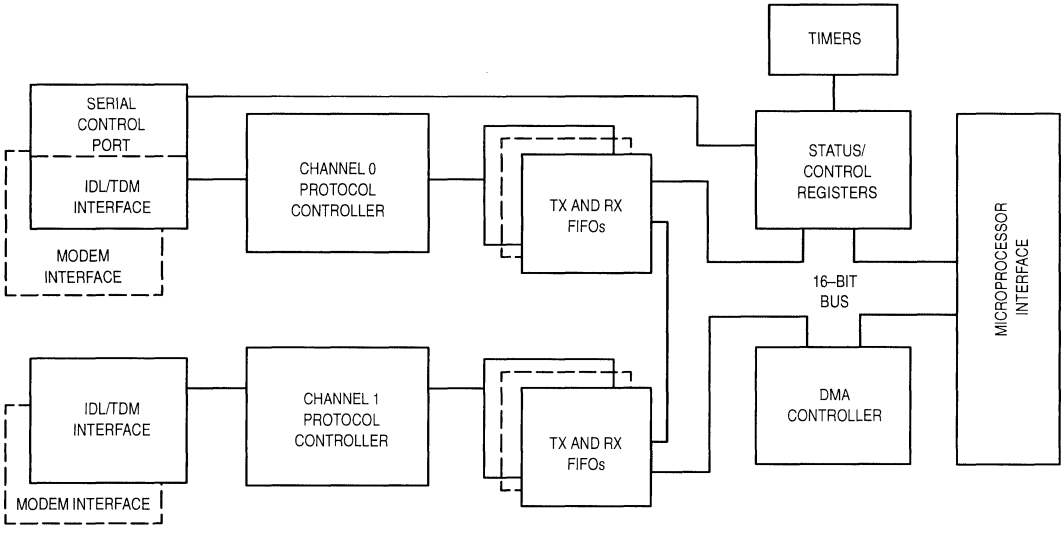
NOTE

This document is a summary of principal features and operation of the DDLC. Please refer to the MC145488 DDLC data book for the complete description and electrical specifications. It can be ordered from your local Motorola sales office or from the Motorola Literature Distribution Center as MC145488/D.

- Two Independent Full–Duplex Bit–Oriented Protocol Controllers Support HDLC, SDLC, CCITT X.25, CCITT Q.921 (LAPD), and V.120 at Basic and Primary Rates
- Four–Channel On–Chip DMA Controller
  - — 64 kbyte Address Range with Expansion Control
  - — Internal Programmable Wait–State Generator
  - — Two Buffer Descriptors for Each Receiver Channel
- Compatible with 68000 and 80186 Bus Structures
  - — Non–Multiplexed 16– or 8–Bit Data Bus
  - — Frame Sizes up to 4096 bytes
- Bit–Level HDLC Processing Including:
  - — Flag Generation/Detection
  - — Abort Generation/Detection
  - — Zero Insertion/Deletion
  - — CRC–CCITT Generation/Checking
  - — Residue Bit Handler
- TEI/SAPI Address Comparison
  - — Three Address Comparisons
  - — Wildcard Bits for Block Comparisons
- Transparent Mode for Codec Compatibility
- Programmable Interrupt Vector Generation
- Two Independent Timers Configurable as a Watchdog Timer
- Flexible Serial Interface with:
  - — IDL Interface for Connection to Other ISDN Family Devices
  - — Timeslot Interface for Connection to PBX–Type Backplanes
  - — Modem Interface for Other Applications
- Supports CCITT Specification 1.460
- Supports DMI Specification 3.1 Modes 0, 1, 2, and 3
- Serial Control Port for ISDN Family Device Control
- Low–Power CMOS with Automatic Power–Down
- Serial Data Rates up to 10 Mbps
- DDLC Master Clock up to 20.5 MHz

MICROWIRE is a trademark of National Semiconductor, Inc.

BLOCK DIAGRAM



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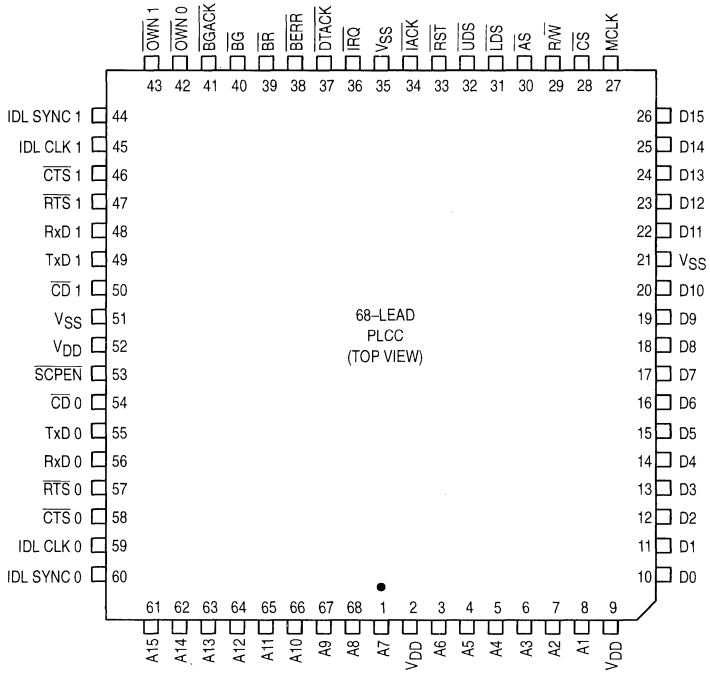


GENERAL DESCRIPTION

DDLC OVERVIEW

The MC145488 Dual Data Link Controller (DDLC) is a high–performance two–channel protocol controller with an on–chip direct memory access controller (DMAC). Each channel has a full–duplex transceiver with independent protocol controllers to handle the bit–level tasks of HDLC–type bit–oriented protocols, including LAPB and LAPD. Each channel also has dedicated DMA controllers for transmit and receive. A transparent mode is provided which bypasses the protocol circuitry so that serial data may be directly transferred between the host processor's memory and the serial interface. The DDLC's microprocessor interface is configurable to 68000 or 80186 systems and may be used in 8–bit or 16–bit bus modes. The DDLC's master clock can be obtained from microprocessor clocks up to 20.5 MHz.

Each channel has a serial data interface which operates up to and above T1 or E1 primary rate speeds in three modes: IDL, Timeslot, and Modem. In the IDL (Interchip Digital Link) mode for ISDN applications, the IDL bus is supported. When in the IDL D channel mode, the DREQ and DGRNT access control lines to the ISDN D channel, through the MC145474 S/T transceiver, are enabled. The timeslot mode is used to connect the DDLC to PBX–type PCM highway backplanes. Both long–frame and short–frame timing are supported as well as synchronous transmit and receive. In the modem mode, each channel has its own separate transmit and receive clock inputs along with modem control lines (RTS, CTS, and CD). The two channels are independent and may be in different interface modes.

A serial control port (SCP) is provided to pass control information to other devices in a system. The SCP is compatible with Motorola's Serial Peripheral Interface (SPI) and National Semiconductor's MICROWIRE™ Plus. Two internal timers may be used for general purpose, low resolution timing of HDLC–type protocols. One of the timers may be configured as a watchdog timer to reset the entire system in the event of a hardware or software failure.

Power consumption is an important aspect of ISDN terminal designs, and the DDLC was designed to use the minimum power possible while maintaining maximum functionality. The DDLC keeps power consumption to a minimum with an automatic power–down feature that turns off sections of circuitry that are not being used. Only those circuits that are actually used (e.g., when the $\overline{CS}$ pin is activated for a register read/write or when the DMA controller performs a bus transaction) enter the normal power state for the duration of the access and for any time required for internal processing.

Two internal loopback functions and special chip and system test modes are available. The loopbacks are controlled by the host for on–line maintenance. The test modes are activated by bits in the master control register and provide access to the internal state machines.

HDLC PROTOCOL OVERVIEW

HDLC (High–Level Data Link Control) and its descendants, LAPB (Link Access Protocol–Balanced) and LAPD (Link Access Protocol for the D channel), are bit–oriented synchronous protocols which are widely used in data communications systems. LAPB and LAPD share the basic format of HDLC but differ in minor aspects (see Figure 1).

In the packet mode, the DDLC transmits and receives data in a format called a frame or packet. All frames start with an opening flag and end with a closing flag. Between the flags, a frame contains an address field, control field, information field, and a cyclic redundancy check field (CRC).

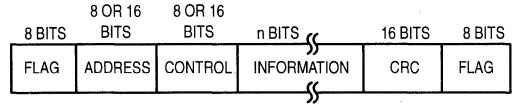


Figure 1. HDLC Frame Format

Flag

The flag is the unique binary pattern (01111110). It provides the frame boundary and a reference for the position of each field of the frame.

Address Field

The 8 or 16 bits following the opening flag comprise the address field. The address field is used to distinguish between the various devices in a network. The DDLC has address recognition circuitry included, which relieves the host from this task.

Control Field

The 8 or 16 bits following the address field are the control field. Commands and responses between the devices in a network are exchanged in this field.

Information Field

This field follows the control field and precedes the CRC field. The information field contains the data to be transferred and may be a null field.

Cycle Redundancy Check Field

The 16 bits preceding the closing flag are the Cycle Redundancy Check (CRC) field. This field detects bit errors in the address, control, and information fields. Checking is with the standard CCITT polynominal $x^{16} x^{12} x^5 + 1$ for both the transmitter and receiver. The transmitter calculates the CRC on all bits of the frame (except for the flags) and transmits the complement of the resulting remainder as the CRC field. The receiver performs the similar computation on all bits (except for the flags) and compares the result to F0B8.

Zero Insertion and Deletion

Zero insertion and deletion, which allows the content of the frame to be transparent, is automatically performed by the DDLC. A binary 0 is inserted by the transmitter after any succession of five 1s within a frame (between flags). This eliminates the possibility of data imitating a flag character. The receiver deletes all 0s that were inserted by the transmitter to regenerate the original data.

Abort

The function of prematurely terminating a data frame is called an abort. The transmitter aborts a frame by sending between seven and fourteen consecutive 1s. When the receiver detects an abort character, it responds by clearing the FIFO and clearing the buffer in memory. It then begins searching for a new frame.

In–Frame, Inter–Frame Time Fill, and Idle

For LAPB and other applications, there are three states that the data link may be in: in–frame, inter–frame time fill, and idle. In–frame is the period from the beginning of an opening flag and the end of a closing flag. Inter–frame time fill is the period between frames when continuous flags are transmitted. Idle is an out–of–frame period when continuous 1s are on the link. In LAPD, on the D channel, there are only two states: in–frame and idle. Continuous flags are not transmitted between frames.

BLOCK DIAGRAM DESCRIPTION

This section is a brief overview of the internal blocks of the DDLC. The blocks include two protocol controllers that handle the bit–level aspects of HDLC–like packet protocols and four FIFOs that buffer the data, a four–channel DMA controller, and a microprocessor interface block that connects the DDLC to the host system. Figure 3 is a simplified block diagram of the DDLC. While the DDLC has two data transceivers, only one is shown for simplicity.

TRANSMIT BIT HANDLER

Two identical bit–level protocol transmitters are provided which perform HDLC–type framing. This section describes the operation of only one transmitter, but it applies to both.

Packet Operation

The transmitter is designed to operate with as little intervention from the host processor as possible. To transmit a frame of data, the host merely informs the DDLC of the starting address of the data frame in memory and the length of the frame in bytes. The DDLC then transmits an opening flag and the data (LSB first) from memory. When the transmitter detects that the end of the data buffer has been reached, a CRC field and a closing flag are appended. The transmitter generates an abort character if the FIFO underruns. During inter–frame periods, the DDLC can be configured to transmit either continuous flags (7E hex) or continuous marks (FF hex).

State Diagram

Figure 2 is the state diagram for the transmitter in packet operation.

Abort

The DDLC can be configured to transmit a standard HDLC abort character. It can also transmit an abort character which is compatible with DMI 3.1 modes 2 or 3 for restricted B–channel applications. An abort character will be transmitted when the TX Fifo underruns, when the Force Abort bit is set in the Transmit Control Register, or when the CTS pin is deasserted.

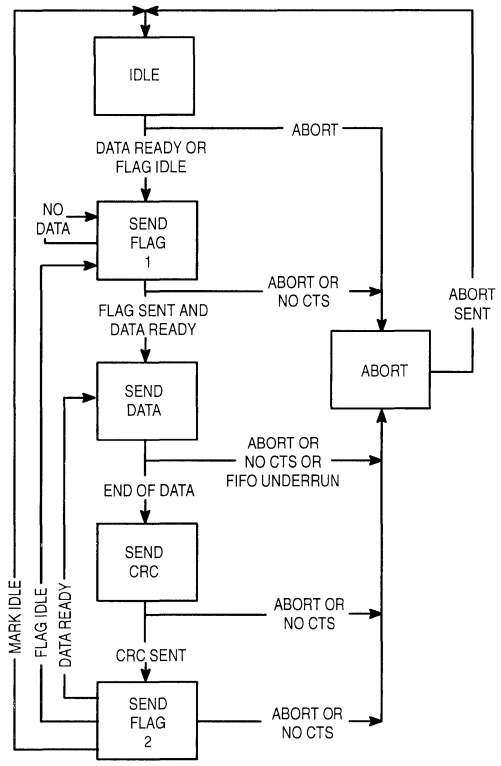


Figure 2. Transmitter State Diagram
HDLC Operation

Flow Control Mechanisms

The DDLC provides two flow control mechanisms: one for basic rate ISDN applications and the other for standard modem applications. The following paragraphs describe the operation of the two schemes.

ISDN D Channel Contention

When the DDLC is operating on the D channel with the companion MC145474 S/T transceiver, the DREQ and DGRNT lines must be used to comply with the basic rate D channel contention algorithm. When the DDLC has a data frame to transmit, it asserts DREQ (high). When DGRNT is detected high from the MC145474 transmission from the DDLC begins in the IDL D–bit time slots when DREQ and DGRNT are both active. If DGRNT is deasserted (goes low) in the middle of a frame, the DDLC automatically aborts the frame in progress and prepares to retransmit the entire frame when the D channel becomes available again. This is done without interrupting the host.

Modem Flow Control

The transmitter indicates to a modem that it has data ready to transmit with signals similar to D channel operation. In this mode, Request–To–Send ($\overline{RTS}$) is directly controlled by the Transmit Enable (TE) bit. When TE is high, the $\overline{RTS}$ pin is asserted (low). During inter–frame periods, either flags or

marks (as selected) are transmitted but the $\overline{RTS}$ pin remains asserted until the user negates the TE bit. Transmission of a frame, if one is ready, actually begins when the modem asserts Clear–to–Send ($\overline{CTS}$ low). If $\overline{CTS}$ is negated for more than one Tx CLK period while a frame is in transmission, the frame is aborted and the DMA pointers are reset so that the frame can be retransmitted without interrupting the host.

Interrupts

There is one interrupt generated by the transmitter state machine. Transmit Frame Complete indicates that an entire frame and its closing flag have been successfully transmitted. Ordinarily, this interrupt is used for basic rate ISDN D channel operation. Two other interrupts associated with the transmitter are generated by the DMA controller and are discussed in the section describing the DMA controller.

Transmit FIFO

The transmitter has a FIFO which buffers it from the DMA controller. It is four characters deep and nine bits wide. The ninth bit is a Tag bit which is set when the the last byte of a frame is read from memory by the DMA controller. After the tagged byte, the DDLC sends a closing CRC and flag sequence.

Transparent Operation

The transmitter has the capability of operating with unframed data such as PCM–encoded voice or proprietary protocols. Raw data may be transmitted from memory with byte alignment maintained through the FIFO and transmitter. Byte alignment signals must be provided. In the modem mode, the alignment signal is externally generated. In IDL and timeslot operation, it is internally generated but user programmable. The DDLC transmits data continuously as long as there is data to transmit.

Inter–Frame Time Fill

The bit sequence that is transmitted between frames is determined by the value of the ITF bit in the Transmit Control register. The inter–frame time fill can be either the X.25 flag character (7E hex) or the LAPD marks (1) idle.

RECEIVE BIT HANDLER

The receiver provides the complementary functions to the transmitter. This section describes the operation of one receiver, but it applies to both receivers.

Packet Operation

The receiver is reset and idle until the Receive Enable bit is set, at which time it begins searching for a flag character. When a flag is found, the selected address field of the frame, if desired, is checked and if a match is found, the DDLC passes the frame of data to the allocated buffer in memory. If no address match is found, the DDLC clears the FIFO, resets the DMA pointers, and searches for a new frame. Zeros inserted by the transmitter are removed from the data before placing the bytes in memory. When the closing flag is detected, the CRC field is checked and if found to be correct, the DDLC queues an interrupt indicating that a good data frame has been received and is in memory. If the CRC is found to be in error, the DDLC automatically resets the buffer pointers to the start of the buffer and searches for a new frame.

Each receiver has two receive buffers, A and B. This permits one buffer to be actively receiving a frame while software is obtaining the data from and reinitializing the other buffer. If an incoming frame is longer than the length defined for the active receive buffer, the DDLC will switch to the second buffer if it is enabled.

If an abort character is found, the buffer pointers in the DMA controller are reset and the aborted frame is ignored. The FIFO is cleared and the receiver begins searching for a flag. No interrupt is generated.

State Diagram

Figure 4 shows the state diagram of the receiver.

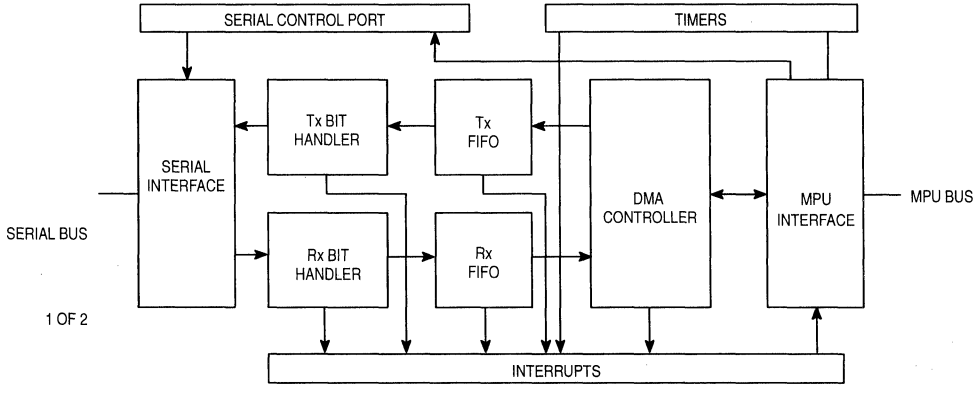


Figure 3. DDLC Block Diagram (One Transceiver Shown)

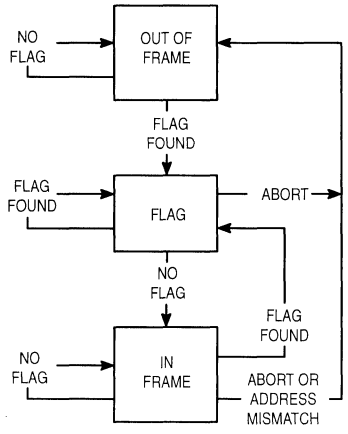


Figure 4. Receiver State Diagram HDLC Operation

Non–Octet Aligned Packets

The receiver has the capability of operating in non–octet aligned packet systems. The residue bit count indicating the number of orphan data bits at the end of the information field is placed in the RC bits of the Receive Status register. These bits are valid until overwritten by another frame. In non–octet aligned systems, the software should check the residue count soon after receiving a Receive Buffer Complete Interrupt to ensure that the residue count is not overwritten by the next frame. Orphan bits are LSB justified in memory. Note: The DDLC does not transmit non–octet aligned frames.

Address Recognition (Filtering)

The receiver can filter received frames by comparing their address fields to user programmable addresses. Two addresses may be programmed with another (broadcast, FF hex) hardwired into the receiver. Address filtering may be performed on either the first OR second octet following the opening flag of a frame. Typically, in ISDN terminal applications, the TEI address (second) field will be of interest. In network applications, the SAPI (first) field will be checked. A separate Wildcard register allows selected bits of Compare Address 0 to be ignored during the comparison procedure. If received frames are rejected by address recognition, the receiver is reset and searches for a new frame. Address recognition may be disabled by clearing the Address Compare Enable bit to 0.

Receive FIFO

The receiver has a FIFO that is similar to the transmitter's. It is four characters deep and ten bits wide (eight bits for data and two bits for the Tag). Serial bytes are produced by the receiver and converted to parallel. As each byte is formed, it is pushed into the FIFO. A comparator in the controller keeps track of the occupancy of the FIFO and requests that the DMA controller place a word of data (16 bits) in memory when there are two or more bytes in the FIFO. In 8–bit operation, the FIFO requests service when one or more bytes of data read are ready to be placed in memory. If the FIFO overruns because the DMA controller did not service a request, an interrupt is queued. When a receiver is operating at 64 kbps in the 16–bit mode, DMA requests from that FIFO occur at approximately 250 μs intervals.

Transparent Operation

The DDLC receiver provides a transparent operation mode for passing raw octet–aligned serial data to memory via DMA. This feature is useful for storing PCM voice or proprietary protocols in memory. When using the DDLC to pass PCM voice to memory, maximum buffer size of 4096 bytes should be used. The Receive Buffer Overrun Interrupt is used in conjunction with Receive Buffers A and B that are available for each channel when transparent mode is used. Because the transparent mode requires that data be in eight–bit quantities, synchronization procedures for defining octet boundaries are required. In the modem mode, the sync signal is externally generated and input on the $\overline{CD}$ pin. In IDL mode timeslot operation, the sync signal is internally generated but user programmable. Once byte alignment is obtained in the receiver, it is maintained through the DMA controller into memory.

Interrupts

There are two interrupts generated by the receiver. The receiver queues an interrupt when a frame has been successfully received. The receive idle interrupt indicates that 15 or more consecutive 1s were received. This interrupt is considered normal operation. The current status of receive idle and carrier detect is available in the Receive Status register, but the user must remember that they can change immediately after being read. The carrier detect pin also generates an interrupt when it changes state.

DMA CONTROLLER

In order to relieve the host software from critically timed data transfers to or from the protocol controllers, the DDLC provides four DMA channels, one for each transmitter and receiver.

DMA Operation

When the DMA controller detects a service request from one of the FIFOs, it prepares the address and data from the transfer then requests ownership of the system bus from the host. When ownership is granted, the DMA controller assumes control of the bus and transfers data either to or from memory. Transfers are 16 bits or 8 bits, depending on the selected bus width. When the number of bytes in a received frame is odd, the last byte is placed in the most significant byte of the last word. The least significant byte contains unknown data. The receive byte count contains the correct number of bytes received (including the CRC). When odd length frames are transmitted, the last word read from memory has the last byte transmitted in the most significant byte, and the least significant byte of that word is discarded.

The DMA controller uses a round robin strategy to service internal DMA requests. A channel that was just serviced is not polled again until all other channels have been polled and serviced, if needed. The DDLC services one DMA request per bus arbitration cycle. The DDLC does not perform burst DMAs, so other devices can have access to the microprocessor bus. This type of operation improves system performance and guarantees that the DDLC is well behaved.

It is impossible to precisely predict what the DDLC bus occupancy will be, but worst case with both channels operating full–duplex at 64 kbps (aggregate rate of 256 kbps) in a 16–bit 68000 system with a 12 MHz MCLK, approximately 0.66% of the host bus bandwidth is consumed by the DDLC. Bus occupancy increases linearly with data rate. At very high data rates, latency from the bus request to the bus grant and interrupt service latency become the limiting factors. It must also be kept in mind that the DDLC can generate interrupts quickly, especially with a large number of small data packets at a high clock rate.

2

Buffer Descriptors

As previously stated, the DDLC has four DMA channels. Pointer registers and counters are required so that the DMA controller knows where to place or fetch data in memory.

Transmit Buffer Descriptors

When the host has a frame of data to transmit, it informs the DMA controller where the data resides in memory. A 16–bit register, the Transmit Base Address register, points to the first word of the transmitted frame and provides a 64 kbyte address range. The host programs the address of the first word to be transmitted into this register. The length of the data frame must also be given to the DMA controller, so a 12–bit Transmit Frame Length register is used to indicate the length of the frame in bytes. Frames of up to 4096 bytes in length may be transmitted.

Back to back frames can be transmitted by updating the transmit buffers when the Transmit DMA Complete interrupt is generated.

NOTE

Once a transmit buffer descriptor has been prepared, it must not be disturbed until the transmit DMA complete or transmit frame complete interrupts are generated.

Receive Buffer Descriptors

The receive buffer descriptors have a 16–Bit Receive Buffer Base Address register, a 12–Bit Buffer Length register, and a 12–Bit Frame Length register. The 16–Bit Base Address register provides 64 kbyte address range and contains the address of the first word of the data buffer to accept a data frame. The 12–Bit Frame Length register indicates the length of the memory buffer in bytes. Buffers of up to 4096 bytes may be built. The DMA controller never places data outside of the boundaries set–up by these two registers. The Frame Length register indicates the number of bytes (including the CRC) received.

Each channel has a pair of buffer descriptors. These may be used alternately so that while one buffer is filling, another buffer is ready–in–waiting. If back–to–back data frames are received, after the first buffer has been closed the second is immediately ready for the next frame. There must be at least one buffer ready to accept data when the Rx Enable bit is set. Figure 6 describes the activity of the receiver with four buffers in memory.

If a packet is being received and no buffers are ready, the receive FIFO will overrun, the Receiver Enable bit is reset, and an interrupt is queued indicating the overrun. If both descriptors are ready, then Buffer A is filled first. If a received frame is larger than a buffer, the Buffer (A or B) Overrun Interrupt is queued, but the receiver continues to receive and the DMA controller places the data in the alternate buffer (if it is available). If an alternate buffer is not ready, the Rx FIFO Overrun Interrupt is generated and the receiver is reset.

Once a data frame has been completely received, the number of bytes received is indicated in the Frame Length register. The number in this register is valid only when the Receive DMA Complete bit (Buffer A or Buffer B) in the Receive Status register is set to '1'.

NOTE

As with the transmitter, once a receive buffer descriptor has been prepared, it must not be disturbed until the closing flag has been found and DMA activity on the buffer has stopped.

Address Expansion

The DDLC provides signals for expansion of the 64 kbyte address space. The $\overline{OWN}$ pins are activated with timing identical to the address pins to enable external address expansion circuitry onto the address bus. Using the $\overline{OWN}$ pins with the R/$\overline{W}$ pin, the transmit and receive buffers may all be on separate 64 kbyte pages in memory.

Transmit Channel Operation

Figure 5 is a simplified state diagram of the DMA controller's operation when a transmit channel requests service.

Four interrupts are produced by the transmitter DMA channel. Transmit DMA Complete indicates that the last byte of data has been transferred from the buffer into the transmit FIFO. FIFO Underrun indicates the DMA requests were not serviced and the FIFO underran. Bus Error is generated when the $\overline{BERR}$ pin is activated during a DMA cycle. Address Error is generated when either $\overline{IACK}$ or $\overline{CS}$ are activated during a DMA cycle.

Receive Channel Operation

Figure 7 is a simplified state diagram for operation of the DMA controller when a receive channel requests service.

MICROPROCESSOR INTERFACE

The microprocessor block interfaces the internal 16–bit bus to the host 8– or 16–bit bus. The block also performs all timing conversion and buffering. This block has three modes of operation described in this section: system slave, system master, and interrupt generator.

System Slave Mode

When the DDLC is in this mode, it appears as fast memory to the host processor. The host can read from or write to the registers in the DDLC. This mode is entered when the $\overline{CS}$ pin is activated. Internal address decoding circuitry is selected and the desired register is connected to the internal bus for access by the host.

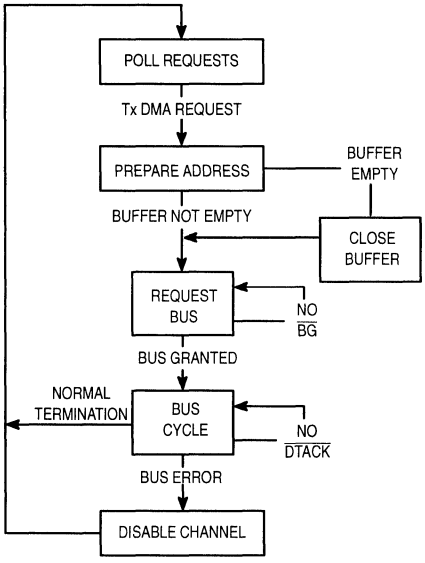


Figure 5. Transmit DMA State Diagram

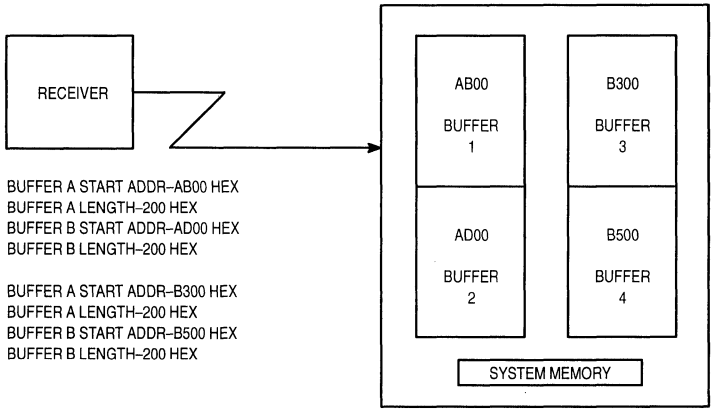


Figure 6. Alternate Receive Buffer Operation

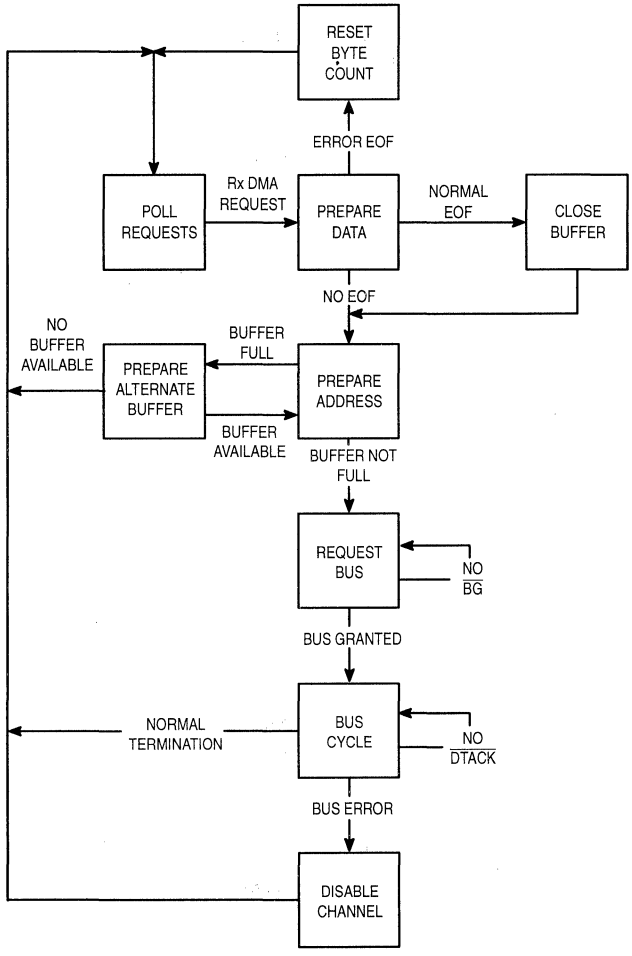


Figure 7. Receive DMA State Diagram

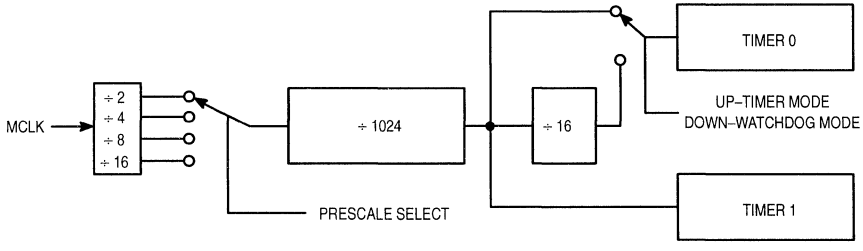


Figure 8. Timer Clock Selection

System Master (DMA) Mode

During DMA operation, the DDLC becomes a system master and controls the system bus. When one of the internal FIFOs requests a DMA transfer, the DDLC negotiates with the system host for ownership of the bus. After successful negotiation, one DMA request is serviced, and then the bus is relinquished. The DDLC has the capability of reading or writing data from or to memory. If the memory system is slow, the DDLC inserts wait states (user selectable) until the memory is ready to complete the access. The DDLC has the capability of recovering from system faults such as address or bus errors.

Interrupt Operation

The DDLC has 27 vectored interrupt sources to inform the host of its status. One group of interrupts is normal operation interrupts. These inform the host that a particular task was completed and that new tasks are desired. Another group is bit handler faults, which inform the host that a DDLC channel detected a fault from which it cannot recover without assistance from the host. A third group is the timer and SCP interrupts. The last group of interrupts is the system faults. These include DMA bus and address errors. The interrupts are presented to the host as a vector number in an interrupt acknowledge cycle. The interrupts are encoded into the low four bits so the DDLC vector space consumes 16 out of 256 locations. Software can program the base vector number, so the DDLC vectors can be located anywhere within the vector table. For applications not using vectored interrupts, the equivalent vector number is accessible in the Master Status register.

SERIAL INTERFACE

The serial interface block has a variety of configurations that make it compatible with most common interfaces. Each serial interface is independent, so two different configurations may be active simultaneously. The serial interface has an IDL mode, a timeslot mode, and a general purpose modem mode. The serial interface supports long frame and short frame timing. It also supports subrate multiplexing. The serial mode is selected by programming the appropriate bits in the Serial Interface Control register.

A full set of serial interface control and handshake pins are provided. The name and functionality change to reflect the serial mode of operation. Separate receive and transmit clock inputs are provided for all modes except IDL and timeslot modes.

The serial interface also supports transfer of transparent data. Depending on which type of serial interface is used, an external synchronization signal must be provided to maintain byte alignment. In IDL mode, the byte synchronization is programmed by the microprocessor.

SERIAL CONTROL PORT

A Serial Control Port, similar to the Serial Peripheral Interface (SPI) on Motorola single–chip microprocessors, is provided to communicate with external devices via a serial link. The SCP functions are multiplexed onto other serial pins so when the SCP is enabled, certain modem control features are lost. Please refer to the MC145488/D Data Book for complete details.

TIMERS

Two timers are provided for general purpose low–resolution protocol uses. The clock to the timer is derived from the Master MPU Clock (MCLK). The baud rate generator in the SCP block is used to drive the timer divide chain. This clock is then divided by 1024 and applied to an eight–bit down–counter. The counter is readable and writable by the host and may be set to any value. The counter counts down toward zero from the current value. A non–maskable interrupt is generated when the counter underflows from FF to FE. The timers continue counting down after reaching FE. The status bit from the previous interrupt must be cleared before a new interrupt is generated. The timer function and interrupt are enabled by setting the Timer Enable bit in the Timer register to one. The timer interrupt status bits must be read while set before they can be cleared. The timers are intended for low accuracy uses such as protocol timers. Figure 8 describes the clock selection choices for the timers.

Watchdog Timer

Timer 0 may be configured as a watchdog timer for the entire host system. When the Watchdog Enable bit is set, an extra divide–by–16 is added to the clock input of the counter. When the counter underflows from FF to FE, the Reset pin becomes an output for 16 MCLK cycles and a logic low is output. This provides a system reset to the host. The host can write any value (except FE hex) to the Timer register to setup any timeout. Timeouts of up to 5.6 seconds are available with a 12 MHz MCLK.

POWER CONSUMPTION

The DDLC is designed utilizing high–performance CMOS technology. As as result, average power consumption is very low. However, because there are wide address and data buses, peak currents may exceed 150 mA for short periods of time (less than 20 ns) while the drivers are charging or discharging the buses.

REGISTER SET

The DDLC has many user accessible registers. These registers control the blocks or indicate status. Other registers, used by the DMA section, are used as buffer descriptors and counters. For a more detailed description, please refer to the DDLC data book. The address for each register is the hexadecimal offset from the base address of the chip select. The registers may be accessed as 8–bit registers or 16–bit registers. Table 1 is a map of the registers and their principal function.

Table 1. Register Memory Map

00	SYSTEM CONTROL	
02	MASTER STATUS	
04	INTERRUPT ENABLE	
06	DATA BUS SIZE SELECT	
10	SCP REGISTER	
12	CH 0 TIMER	
14	CH 1 TIMER	
20	CHANNEL 0 SERIAL INTERFACE CONTROL	CHANNEL 0 REGISTERS
22	CHANNEL 0 Tx CONTROL	
24	CHANNEL 0 Rx CONTROL	
26	CHANNEL 0 Tx STATUS	
28	CHANNEL 0 Rx STATUS	
2A	CHANNEL 0 ADDRESS COMPARE	
2C	CHANNEL 0 ADDRESS WILDCARD BITS	
2E	CHANNEL 0 CRC ERROR COUNT	
30	CHANNEL 0 Tx FRAME LENGTH	
32	CHANNEL 0 Tx BASE ADDRESS	
34	CHANNEL 0 Tx BYTE COUNT	
36	CHANNEL 0 Rx BUFFER LENGTH	
38	CHANNEL 0 Rx BUFFER A BASE ADDRESS	
3A	CHANNEL 0 Rx BUFFER A BYTE COUNT	
3C	CHANNEL 0 Rx BUFFER B BASE ADDRESS	
3E	CHANNEL 0 Rx BUFFER B BYTE COUNT	
40	CHANNEL 1 SERIAL INTERFACE CONTROL	CHANNEL 1 REGISTERS
42	CHANNEL 1 Tx CONTROL	
44	CHANNEL 1 Rx CONTROL	
46	CHANNEL 1 Tx STATUS	
48	CHANNEL 1 Rx STATUS	
4A	CHANNEL 1 ADDRESS COMPARE	
4C	CHANNEL 1 ADDRESS WILDCARD BITS	
4E	CHANNEL 1 CRC ERROR COUNT	
50	CHANNEL 1 Tx FRAME LENGTH	
52	CHANNEL 1 Tx BASE ADDRESS	
54	CHANNEL 1 Tx BYTE COUNT	
56	CHANNEL 1 Rx BUFFER LENGTH	
58	CHANNEL 1 Rx BUFFER A BASE ADDRESS	
5A	CHANNEL 1 Rx BUFFER A BYTE COUNT	
5C	CHANNEL 1 Rx BUFFER B BASE ADDRESS	
5E	CHANNEL 1 Rx BUFFER B BYTE COUNT	

PCM Codec-Filter Mono-Circuit

MC145500
MC145501
MC145502
MC145503
MC145505

The MC145500, MC145501, MC145502, MC145503, and MC145505 are all per channel PCM Codec–Filter mono–circuits. These devices perform the voice digitization and reconstruction as well as the band limiting and smoothing required for PCM systems. The MC145500 and MC145503 are general purpose devices that are offered in a 16–pin package. They are designed to operate in both synchronous and asynchronous applications and contain an on–chip precision reference voltage. The MC145501 is offered in an 18–pin package and adds the capability of selecting from three peak overload voltages (2.5, 3.15, and 3.78 V). The MC145505 is a synchronous device offered in a 16–pin DIP and wide body SOIC package intended for instrument use. The MC145502 is the full–featured device which presents all of the options of the chip. This device is packaged in a 22–pin DIP and a 28–pin chip carrier package and contains all the features of the MC145500 and MC145501 plus several more. Most of these features can be made available in a lower pin count package tailored to a specific user's application. Contact the factory for further details.

These devices are pin–for–pin replacements for Motorola's first generation of MC14400/01/02/03/05 PCM mono–circuits and are upwardly compatible with the MC14404/06/07 codecs and other industry standard codecs. They also maintain compatibility with Motorola's family of MC33120 and MC3419 SLIC products.

The MC145500 family of PCM Codec–Filter mono–circuits utilizes CMOS due to its reliable low–power performance and proven capability for complex analog/digital VLSI functions.

MC145500 (This Device is Not Recommended for New Designs)

- 16–Pin Package
- Transmit Bandpass and Receive Low–Pass Filter On–Chip
- Pin Selectable Mu–Law/A–Law Companding with Corresponding Data Format
- On–Chip Precision Reference Voltage (3.15 V)
- Power Dissipation of 50 mW, Power–Down of 0.1 mW at ± 5 V
- Automatic Prescaler Accepts 128 kHz, 1.536, 1.544, 2.048, and 2.56 MHz for Internal Sequencing

MC145501 — All of the Above Plus:
(This Device is Not Recommended for New Designs)

- 18–Pin Package
- Selectable Peak Overload Voltages (2.5, 3.15, 3.78 V)
- Access to the Inverting Input of the TxI Input Operational Amplifier

MC145502 — All of the Above Plus:

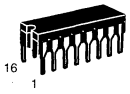
- 22–Pin and 28–Pin Packages
- Variable Data Clock Rates (64 kHz to 4.1 MHz)
- Complete Access to the Three Terminal Transmit Input Operational Amplifiers
- An External Precision Reference May Be Used

MC145503 — All of the Above Features of the MC145500 Plus:

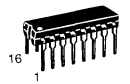
- 16–Pin Package
- Complete Access to the Three Terminal Transmit Input Operational Amplifiers

MC145505 — Same as MC145503 Except:

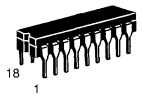
- 16–Pin Package
- Common 64 kHz to 4.1 MHz Transmit/Receive Data Clock



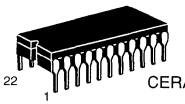
L SUFFIX
CERAMIC PACKAGE
CASE 620
MC145500/03/05



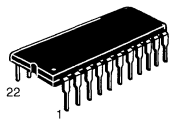
P SUFFIX
PLASTIC DIP
CASE 648
MC145503/05



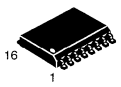
L SUFFIX
CERAMIC PACKAGE
CASE 726
MC145501



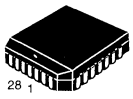
L SUFFIX
CERAMIC PACKAGE
CASE 736
MC145502



P SUFFIX
PLASTIC DIP
CASE 708
MC145502



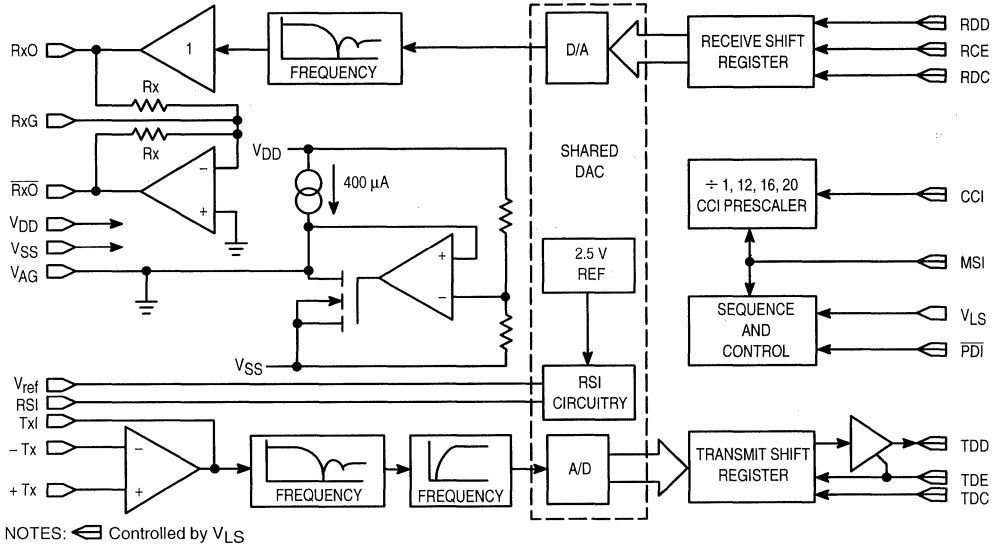
DW SUFFIX
SOG PACKAGE
CASE 751G
MC145503/05



FN SUFFIX
PLCC PACKAGE
CASE 776
MC145502

REV 1
9/95 (Replaces ADI1287)

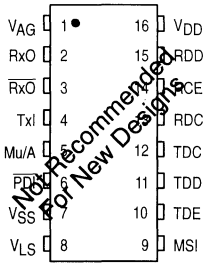
MC145500/01/02/03/05 PCM CODEC–FILTER MONO–CIRCUIT BLOCK DIAGRAM



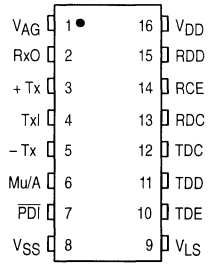
NOTES: ⊲ Controlled by V_{LS}
Rx ≈ 100 kΩ (internal resistors)

PIN ASSIGNMENTS
(DRAWINGS DO NOT REFLECT RELATIVE SIZE)

MC145500L



MC145503L, P



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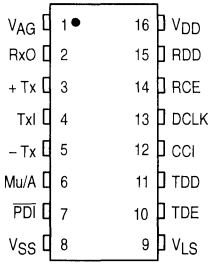
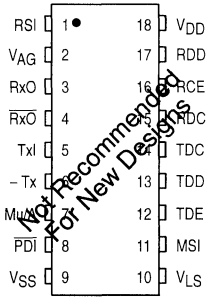
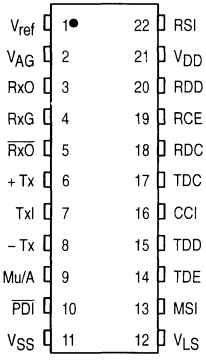


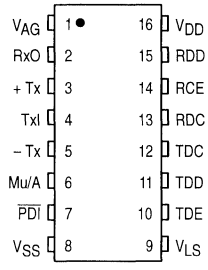
MC145501L



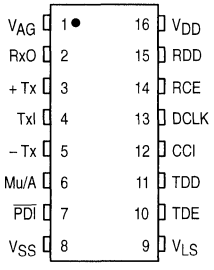
MC145502L, P



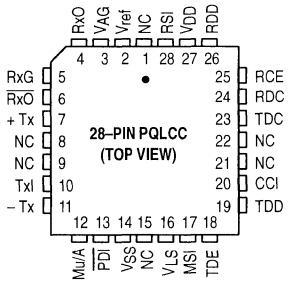
MC145503DW



MC145505DW



MC145502FN



NC = NO CONNECTION

2

ABSOLUTE MAXIMUM RATINGS (Voltage Referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}, V_{SS}	– 0.5 to 13	V
Voltage, Any Pin to V_{SS}	V	– 0.5 to V_{DD} + 0.5	V
DC Drain Per Pin (Excluding V_{DD}, V_{SS})	I	10	mA
Operating Temperature Range	T_A	– 40 to + 85	°C
Storage Temperature Range	T_{stg}	– 85 to + 150	°C

This device contains circuitry to protect against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., V_{SS}, V_{DD}, V_{LS}, or V_{AG}).

2

RECOMMENDED OPERATING CONDITIONS (T_A = – 40 to + 85°C)

Characteristic		Min	Typ	Max	Unit
DC Supply Voltage					V
Dual Supplies: V_{DD} = – V_{SS}, (V_{AG} = V_{LS} = 0 V)		4.75	5.0	6.3	
Single Supply: V_{DD} to V_{SS} (V_{AG} is an Output, V_{LS} = V_{DD} or V_{SS})					
MC145500, MC145501, MC145502, MC145503, MC145505 (Using Internal 3.15 V Reference)		8.5	—	12.6	
MC145501, MC145502 Using Internal 2.5 V Reference		7.0	—	12.6	
MC145501, MC145502 Using Internal 3.78 V Reference		9.5	—	12.6	
MC145502 Using External 1.5 V Reference, Referenced to V_{AG}		4.75	—	12.6	
Power Dissipation					mW
CMOS Logic Mode (V_{DD} to V_{SS} = 10 V, V_{LS} = V_{DD})		—	40	70	
TTL Logic Mode (V_{DD} = + 5 V, V_{SS} = – 5 V, V_{LS} = V_{AG} = 0 V)		—	50	90	
Power Down Dissipation		—	0.1	1.0	mW
Frame Rate Transmit and Receive		7.5	8.0	8.5	kHz
Data Rate		—	128	—	kHz
MC145500, MC145501, MC145503		—	1536	—	
Must Use One of These Frequencies, Relative to MSI Frequency of 8 kHz		—	1544	—	
		—	2048	—	
		—	2560	—	
Data Rate for MC145502, MC145505		64	—	4096	kHz
Full Scale Analog Input and Output Level					Vp
MC145500, MC145503, MC145505		—	3.15	—	
MC145501, MC145502 (V_{ref} = V_{SS})	RSI = V_{DD}	—	3.78	—	
	RSI = V_{SS}	—	3.15	—	
	RSI = V_{AG}	—	2.5	—	
MC145502 Using an External Reference Voltage Applied at V_{ref} Pin	RSI = V_{DD}	—	1.51 x V_{ref}	—	
	RSI = V_{SS}	—	1.26 x V_{ref}	—	
	RSI = V_{AG}	—	V_{ref}	—	

DIGITAL LEVELS (V_{SS} to V_{DD} = 4.75 V to 12.6 V, T_A = – 40 to + 85°C)

Characteristic		Symbol	Min	Max	Unit
Input Voltage Levels (TDE, TDC, RCE, RDC, RDD, DC, MSI, CCI, $\overline{PDI}$)					V
CMOS Mode (V_{LS} = V_{DD}, V_{SS} is Digital Ground)	"0"	V_{IL}	—	0.3 x V_{DD}	
	"1"	V_{IH}	0.7 x V_{DD}	—	
TTL Mode ($V_{LS} \le V_{DD}$ – 4.0 V, V_{LS} is Digital Ground)	"0"	V_{IL}	—	V_{LS} + 0.8 V	
	"1"	V_{IH}	V_{LS} + 2.0 V	—	
Output Current for TDD (Transmit Digital Data)					mA
CMOS Mode (V_{LS} = V_{DD}, V_{SS} = 0 V and is Digital Ground)					
(V_{DD} = 5 V, V_{out} = 0.4 V)		I_{OL}	1.0	—	
(V_{DD} = 10 V, V_{out} = 0.5 V)			3.0	—	
(V_{DD} = 5 V, V_{out} = 4.5 V)		I_{OH}	– 1.0	—	
(V_{DD} = 10 V, V_{out} = 9.5 V)			– 3.0	—	
TTL Mode ($V_{LS} \le V_{DD}$ – 4.75 V, V_{LS} = 0 V and is Digital Ground)	(V_{OL} = 0.4 V)	I_{OL}	1.6	—	
	(V_{OH} = 2.4 V)	I_{OH}	– 0.2	—	

ANALOG TRANSMISSION PERFORMANCE

(V_{DD} = + 5 V ± 5%, V_{SS} = − 5 V ± 5%, V_{LS} = V_{AG} = 0 V, V_{ref} = RSI = V_{SS} (Internal 3.15 V Reference), 0 dBm0 = 1.546 Vrms = + 6 dBm @ 600 Ω, T_A = − 40 to + 85°C, TDC = RDC = CC = 2.048 MHz, TDE = RCE = MSI = 8 kHz, Unless Otherwise Noted)

Characteristic	End–to–End		A/D		D/A		Unit
	Min	Max	Min	Max	Min	Max	
Absolute Gain (0 dBm0 @ 1.02 kHz, T_A = 25°C, V_{DD} = 5 V, V_{SS} = − 5 V)	—	—	− 0.30	+ 0.30	− 0.30	+ 0.30	dB
Absolute Gain Variation with Temperature 0 to + 70°C	—	—	—	± 0.03	—	± 0.03	dB
Absolute Gain Variation with Temperature − 40 to + 85°C	—	—	—	± 0.1	—	± 0.1	dB
Absolute Gain Variation with Power Supply (V_{DD} = 5 V, V_{SS} = − 5 V, 5%)	—	—	—	± 0.02	—	± 0.02	dB
Gain vs Level Tone (Relative to − 10 dBm0, 1.02 kHz) + 3 to − 40 dBm0	− 0.4	+ 0.4	− 0.2	+ 0.2	− 0.2	+ 0.2	dB
− 40 to − 50 dBm0	− 0.8	+ 0.8	− 0.4	+ 0.4	− 0.4	+ 0.4	
− 50 to − 55 dBm0	− 1.6	+ 1.6	− 0.8	+ 0.8	− 0.8	+ 0.8	
Gain vs Level Pseudo Noise (A–Law Relative to − 10 dBm0)							dB
CCITT G.714 − 10 to − 40 dBm0	—	—	− 0.25	+ 0.25	− 0.25	+ 0.25	
− 40 to − 50 dBm0	—	—	− 0.30	+ 0.30	− 0.30	+ 0.30	
− 50 to − 55 dBm0	—	—	− 0.45	+ 0.45	− 0.45	+ 0.45	
Total Distortion − 1.02 kHz Tone (C–Message) 0 to − 30 dBm0	35	—	36	—	36	—	dBC
− 40 dBm0	29	—	29	—	30	—	
− 45 dBm0	24	—	24	—	25	—	
Total Distortion With Pseudo Noise (A–Law) − 3 dBm0	27.5	—	28	—	28.5	—	dB
CCITT G.714 − 6 to − 27 dBm0	35	—	35.5	—	36	—	
− 34 dBm0	33.1	—	33.5	—	34.2	—	
− 40 dBm0	28.2	—	28.5	—	30.0	—	
− 55 dBm0	13.2	—	13.5	—	15.0	—	
Idle Channel Noise (For End–End and A/D, See Note 1)							
Mu–Law, C–Message Weighted	—	15	—	15	—	9	dBrnC0
A–Law, Psophometric Weighted	—	− 69	—	− 69	—	− 78	dBm0p
Frequency Response (Relative to 1.02 kHz @ 0 dBm0) 15 to 60 Hz	—	− 23	—	− 23	—	0.15	dB
300 to 3000 Hz	− 0.3	+ 0.3	− 0.15	+ 0.15	− 0.15	+ 0.15	
3400 Hz	− 1.6	0	− 0.8	0	− 0.8	0	
4000 Hz	—	− 28	—	− 14	—	− 14	
≥ 4600 Hz	—	− 60	—	− 32	—	− 30	
Inband Spurious (1.02 kHz @ 0 dBm0, Transmit and RxO)	—	—	—	− 43	—	− 43	dBm0
300 to 3000 Hz							
Out–of–Band Spurious at RxO (300 − 3400 Hz @ 0 dBm0 In)							dB
4600 to 7600 Hz	—	− 30	—	—	—	− 30	
7600 to 8400 Hz	—	− 40	—	—	—	− 40	
8400 to 100,000 Hz	—	− 30	—	—	—	− 30	
Idle Channel Noise Selective @ 8 kHz, Input = V_{AG}, 30 Hz Bandwidth	—	− 70	—	—	—	− 70	dBm0
Absolute Delay @ 1600 Hz (TDC = 2.048 MHz, TDE = 8 kHz)	—	—	—	310	—	180	µs
Group Delay Referenced to 1600 Hz (TDC = 2048 kHz,							µs
TDE = 8 kHz) 500 to 600 Hz	—	—	—	200	− 40	—	
600 to 800 Hz	—	—	—	140	− 40	—	
800 to 1000 Hz	—	—	—	70	− 30	—	
1000 to 1600 Hz	—	—	—	40	− 20	—	
1600 to 2600 Hz	—	—	—	75	—	90	
2600 to 2800 Hz	—	—	—	110	—	120	
2800 to 3000 Hz	—	—	—	170	—	160	
Crosstalk of 1020 Hz @ 0 dBm0 From A/D or D/A (Note 2)	—	—	—	− 75	—	− 80	dB
Intermodulation Distortion of Two Frequencies of Amplitudes − 4 to − 21 dBm0 from the Range 300 to 3400 Hz	—	—	—	− 41	—	− 41	dB

NOTES:
1. Extrapolated from a 1020 Hz @ − 50 dBm0 distortion measurement to correct for encoder enhancement.
2. Selectively measured while the A/D is stimulated with 2667 Hz @ − 50 dBm0.

ANALOG ELECTRICAL CHARACTERISTICS ($V_{DD} = -V_{SS} = 5$ V to 6 V ± 5%, $T_A = -40$ to + 85°C)

Characteristic		Symbol	Min	Typ	Max	Unit
Input Current	+Tx, –Tx (TxI for MC145500)	I_{in}	—	± 0.01	± 0.2	µA
AC Input Impedance to V_{AG} (1 kHz)	+Tx, –Tx TxI for MC145500	Z_{in}	5 0.1	10 0.2	— —	MΩ
Input Capacitance	+Tx, –Tx		—	—	10	pF
Input Offset Voltage of TxI Op Amp			—	< ± 30	—	mV
Input Common Mode Voltage Range	+Tx, –Tx	V_{ICR}	V_{SS} + 1.0	—	V_{DD} – 2.0	V
Input Common Mode Rejection Ratio	+Tx, –Tx	CMRR	—	70	—	dB
TxI Unity Gain Bandwidth	$R_L \geq 10$ kΩ	BW_p	—	1000	—	kHz
TxI Open Loop Gain	$R_L \geq 10$ kΩ	A_{VOL}	—	75	—	dB
Equivalent Input Noise (C–Message) Between +Tx and –Tx, at TxI			—	– 20	—	dBrnC0
Output Load Capacitance for TxI Op Amp			0	—	100	pF
Output Voltage Range TxI Op Amp, RxO or $\overline{RxO}$ $R_L = 10$ kΩ to V_{AG} $R_L = 600$ Ω to V_{AG}		V_{out}	 V_{SS} + 0.8 V_{SS} + 1.5	 — —	 V_{DD} – 1.0 V_{DD} – 1.5	V
Output Current TxI, RxO, $\overline{RxO}$	$V_{SS} + 1.5\ V \leq V_{out} \leq V_{DD} - 1.5\ V$		± 5.5	—	—	mA
Output Impedance RxO, $\overline{RxO}$*	0 to 3.4 kHz	Z_{out}	—	3	—	Ω
Output Load Capacitance for RxO and $\overline{RxO}$*			0	—	200	pF
Output dc Offset Voltage Referenced to V_{AG} Pin	RxO $\overline{RxO}$*		— —	— —	± 100 ± 150	mV
Internal Gainsetting Resistors for RxG to RxO and $\overline{RxO}$			62	100	225	kΩ
External Reference Voltage Applied to V_{ref} (Referenced to V_{AG})			0.5	—	V_{DD} – 1.0	V
V_{ref} Input Current			—	—	20	µA
V_{AG} Output Bias Voltage			—	0.53 V_{DD} + 0.47 V_{SS}	—	V
V_{AG} Output Current	Source Sink	I_{VAG}	0.4 10.0	— —	0.8 —	mA
Output Leakage Current During Power Down for the TxI Op Amp, V_{AG}, RxO, and $\overline{RxO}$			—	—	± 30	µA
Positive Power Supply Rejection Ratio, 0 – 100 kHz @ 250 mV, C–Message Weighting	Transmit Receive		45 55	50 65	— —	dBC
Negative Power Supply Rejection Ratio, 0 – 100 kHz @ 250 mV, C–Message Weighting	Transmit Receive		50 50	55 60	— —	dBC

* Assumes that RxG is not connected for gain modifications to $\overline{RxO}$.

MODE CONTROL LOGIC (V_{SS} to V_{DD} = 4.75 V to 12.6 V, T_A = – 40 to + 85°C)

Characteristic	Min	Typ	Max	Unit
V_{LS} Voltage for TTL Mode (TTL Logic Levels Referenced to V_{LS})	V_{SS}	—	V_{DD} – 4.0	V
V_{LS} Voltage for CMOS Mode (CMOS Logic Levels of V_{SS} to V_{DD})	V_{DD} – 0.5	—	V_{DD}	V
Mu/A Select Voltage				V
Mu–Law Mode	V_{DD} – 0.5	—	V_{DD}	
Sign Magnitude Mode	V_{AG} – 0.5	—	V_{AG} + 0.5	
A–Law Mode	V_{SS}	—	V_{SS} + 0.5	
RSI Voltage for Reference Select Input (MC145501 and MC145502) 3.78 V Mode	V_{DD} – 0.5	—	V_{DD}	V
2.5 V Mode	V_{AG} – 0.5	—	V_{AG} + 0.5	
3.15 V Mode	V_{SS}	—	V_{SS} + 0.5	
V_{ref} Voltage for Internal or External Reference (MC145502 Only)				V
Internal Reference Mode	V_{SS}	—	V_{SS} + 0.5	
External Reference Mode	V_{AG} + 0.5	—	V_{DD} – 1.0	
Analog Test Mode Frequency, MS = CCI (MC145500, MC145501, MC145502 Only) See Pin Description; Test Modes	—	128	—	kHz

SWITCHING CHARACTERISTICS (V_{SS} to V_{DD} = 9.5 V to 12.6 V, T_A = – 40 to + 85°C, C_L = 150 pF, CMOS or TTL Mode)

Characteristic		Symbol	Min	Typ	Max	Unit
Output Rise Time	TDD	t_{TLH}	—	30	80	ns
Output Fall Time		t_{THL}	—	30	80	
Input Rise Time	TDE, TDC, RCE, RDC, DC, MSI, CCI	t_{TLH}	—	—	4	µs
Input Fall Time		t_{THL}	—	—	4	
Pulse Width	TDE Low, TDC, RCE, RDC, DC, MSI, CCI	t_W	100	—	—	ns
DCLK Pulse Frequency (MC145502/05 Only)	TDC, RDC, DC	f_{CL}	64	—	4096	kHz
CCI Clock Pulse Frequency (MSI = 8 kHz)		f_{CL1}	—	128	—	kHz
CCI is internally tied to TDC on the MC145500/01/03, therefore, the		f_{CL2}	—	1536	—	
transmit data clock must be one of these frequencies. This pin will accept		f_{CL3}	—	1544	—	
one of these discrete clock frequencies and will compensate to produce		f_{CL4}	—	2048	—	
internal sequencing.		f_{CL5}	—	2560	—	
Propagation Delay Time						ns
TDE Rising to TDD Low Impedance	TTL	t_{P1}	—	90	180	
	CMOS		—	90	150	
TDE Falling to TDD High Impedance	TTL	t_{P2}	—	—	55	
	CMOS		—	—	40	
TDC Rising Edge to TDD Data, During TDE High	TTL	t_{P3}	—	90	180	
	CMOS		—	90	150	
TDE Rising Edge to TDD Data, During TDC High	TTL	t_{P4}	—	90	180	
	CMOS		—	90	150	
TDC Falling Edge to TDE Rising Edge Setup Time		t_{su1}	20	—	—	ns
TDE Rising Edge to TDC Falling Edge Setup Time		t_{su2}	100	—	—	ns
TDE Falling Edge to TDC Rising Edge to Preserve the Next TDD Data		t_{su8}	20	—	—	ns
RDC Falling Edge to RCE Rising Edge Setup Time		t_{su3}	20	—	—	ns
RCE Rising Edge to RDC Falling Edge Setup Time		t_{su4}	100	—	—	ns
RDD Valid to RDC Falling Edge Setup Time		t_{su5}	60	—	—	ns
CCI Falling Edge to MSI Rising Edge Setup Time		t_{su6}	20	—	—	ns
MSI Rising Edge to CCI Falling Edge Setup Time		t_{su7}	100	—	—	ns
RDD Hold Time from RDC Falling Edge		t_h	100	—	—	ns
TDE, TDC, RCE, RDC, RDD, DC, MSI, CCI Input Capacitance			—	—	10	pF
TDE,TDC, RCE, RDC, RDD, DC, MSI, CCI Input Current			—	± 0.01	± 10	µA
TDD Capacitance During High Impedance (TDE Low)			—	12	15	pF
TDD Input Current During High Impedance (TDE Low)			—	± 0.1	± 10.0	µA

DEVICE DESCRIPTIONS

A codec–filter is a device which is used for digitizing and reconstructing the human voice. These devices were developed primarily for the telephone network to facilitate voice switching and transmission. Once the voice is digitized, it may be switched by digital switching methods or transmitted long distance (T1, microwave, satellites, etc.) without degradation. The name codec is an acronym from "Coder" for the A/D used to digitize voice, and "Decoder" for the D/A used for reconstructing voice. A codec is a single device that does both the A/D and D/A conversions.

To digitize intelligible voice requires a signal to distortion of about 30 dB for a dynamic range of about 40 dB. This may be accomplished with a linear 13–bit A/D and D/A, but will far exceed the required signal to distortion at amplitudes greater than 40 dB below the peak amplitude. This excess performance is at the expense of data per sample. Two methods of data reduction are implemented by compressing the 13–bit linear scheme to companded 8–bit schemes. These companding schemes follow a segmented or "piecewise–linear" curve formatted as sign bit, three chord bits, and four step bits. For a given chord, all 16 of the steps have the same voltage weighting. As the voltage of the analog input increases, the four step bits increment and carry to the three chord bits which increment. With the chord bits incremented, the step bits double their voltage weighting. This results in an effective resolution of 6–bits (sign + chord + four step bits) across a 42 dB dynamic range (7 chords above zero, by 6 dB per chord). There are two companding schemes used; Mu–255 Law specifically in North America, and A–Law specifically in Europe. These companding schemes are accepted world wide. The tables show the linear quantization levels to PCM words for the two companding schemes.

In a sampling environment, Nyquist theory says that to properly sample a continuous signal, it must be sampled at a frequency higher than twice the signal's highest frequency component. Voice contains spectral energy above 3 kHz, but its absence is not detrimental to intelligibility. To reduce the digital data rate, which is proportional to the sampling rate, a sample rate of 8 kHz was adopted, consistent with a bandwidth of 3 kHz. This sampling requires a low–pass filter to limit the high frequency energy above 3 kHz from distorting the inband signal. The telephone line is also subject to 50/60 Hz power line coupling which must be attenuated from the signal by a high–pass filter before the A/D converter.

The D/A process reconstructs a staircase version of the desired inband signal which has spectral images of the inband signal modulated about the sample frequency and its harmonics. These spectral images are called aliasing components which need to be attenuated to obtain the desired signal. The low–pass filter used to attenuate filter aliasing components is typically called a reconstruction or smoothing filter.

The MC145500 series PCM Codec–Filters have the codec, both presampling and reconstruction filters, a precision voltage reference on chip, and require no external components. There are five distinct versions of the Motorola MC145500 Series.

MC145500

The MC145500 PCM Codec–Filter is intended for standard byte interleaved synchronous and asynchronous applications. The TDC pin on this device is the input to both the TDC and CCI functions in the pin description. Consequently, for MSI = 8 kHz, TDC can be one of five discrete frequencies. These are 128 kHz (40 to 60% duty cycle) 1.536, 1.544, 2.048, or 2.56 MHz. (For other data clock frequencies, see MC145502 or MC145505.) The internal reference is set for 3.15 V peak full scale, and the full scale input level at TxI and output level at RxO is 6.3 V peak–to–peak. This is the + 3 dBm0 level of the PCM Codec–Filter. All other functions are described in the pin description.

MC145501

The MC145501 PCM Codec–Filter offers the same features and is for the same application as the MC145500, but offers two additional pins and features. The reference select input allows the full scale level of the device to be set at 2.5 Vp, 3.15 Vp, or 3.78 Vp. The –Tx pin allows for external transmit gain adjust and simplifies the interface to the MC3419 SLIC. Otherwise, it is identical to MC145500.

MC145502

The MC145502 PCM Codec–Filter is the full feature 22–pin device. It is intended for use in applications requiring maximum flexibility. The MC145502 contains all the features of the MC145500 and MC145501. The MC145502 is intended for bit interleaved or byte interleaved applications with data clock frequencies which are nonstandard or time varying. One of the five standard frequencies (listed above) is applied to the CCI input, and the data clock inputs can be any frequency between 64 kHz and 4.096 MHz. The V_{ref} pin allows for use of an external shared reference or selection of the internal reference. The RxG pin accommodates gain adjustments for the inverted analog output. All three pins of the input gain–setting operational amplifier are present, providing maximum flexibility for the analog interface.

MC145503

The MC145503 PCM Codec–Filter is intended for standard byte interleaved synchronous or asynchronous applications. TDC can be one of five discrete frequencies. These are 128 kHz (40 to 60% duty cycle), 1.536, 1.544, 2.048, or 2.56 MHz. (For other data clock frequencies, see MC145502 or MC145505.) The internal reference is set for 3.15 V peak full scale, and the full scale input level at TxI and output level at RxO is 6.3 V peak–to–peak. This is the + 3 dBm0 level of the PCM Codec–Filter. The +Tx and –Tx inputs provide maximum flexibility for analog interface. All other functions are described in the pin description.

MC145505

The MC145505 PCM Codec–Filter is intended for byte interleaved synchronous applications. The MC145505 has all the features of the MC145503 but internally connects TDC and RDC (see pin description) to the DC pin. One of the five standard frequencies (listed above) should be applied to

CCI. The data clock input (DC) can be any frequency between 64 kHz and 4.096 MHz.

PIN DESCRIPTIONS

DIGITAL

V_{LS}
Logic Level Select input and TTL Digital Ground

V_{LS} controls the logic levels and digital ground reference for all digital inputs and the digital output. These devices can operate with logic levels from full supply (V_{SS} to V_{DD}) or with TTL logic levels using V_{LS} as digital ground. For V_{LS} = V_{DD}, all I/O is full supply (V_{SS} to V_{DD} swing) with CMOS switch points. For $V_{SS} < V_{LS} < (V_{DD} - 4\ V)$, all inputs and outputs are TTL compatible with V_{LS} being the digital ground. The pins controlled by V_{LS} are inputs MSI, CCI, TDE, TDC, RCE, RDC, RDD, $\overline{PDI}$, and output TDD.

MSI
Master Synchronization Input

MSI is used for determining the sample rate of the transmit side and as a time base for selecting the internal prescale divider for the convert clock input (CCI) pin. The MSI pin should be tied to an 8 kHz clock which may be a frame sync or system sync signal. MSI has no relation to transmit or receive data timing, except for determining the internal transmit strobe as described under the TDE pin description. MSI should be derived from the transmit timing in asynchronous applications. In many applications MSI can be tied to TDE. (MSI is tied internally to TDE in MC145503/05.)

CCI
Convert Clock Input

CCI is designed to accept five discrete clock frequencies. These are 128 kHz, 1.536 MHz, 1.544 MHz, 2.048 MHz, or 2.56 MHz. The frequency at this input is compared with MSI and prescale divided to produce the internal sequencing clock at 128 kHz (or 16 times the sampling rate). The duty cycle of CCI is dictated by the minimum pulse width except for 128 kHz, which is used directly for internal sequencing and must have a 40 to 60% duty cycle. In asynchronous applications, CCI should be derived from transmit timing. (CCI is tied internally to TDC in MC145500/01/03.)

TDC
Transmit Data Clock Input

TDC can be any frequency from 64 kHz to 4.096 MHz, and is often tied to CCI if the data rate is equal to one of the five discrete frequencies. This clock is the shift clock for the transmit shift register and its rising edges produce successive data bits at TDD. TDE should be derived from this clock. (TDC and RDC are tied together internally in the MC145505 and are called DC.) CCI is internally tied to TDC on the MC145500/ 01/03. Therefore, TDC must satisfy CCI timing requirements also.

TDE
Transmit Data Enable Input

TDE serves three major functions. The first TDE rising edge following an MSI rising edge generates the internal transmit strobe which initiates an A/D conversion. The internal transmit strobe also transfers a new PCM data word into the transmit shift register (sign bit first) ready to be output at TDD. The TDE pin is the high impedance control for the transmit digital data (TDD) output. As long as this pin is high, the TDD output stays low impedance. This pin also enables the output shift register for clocking out the 8–bit serial PCM word. The logical AND of the TDE pin with the TDC pin clocks out a new data bit at TDD. TDE should be held high for eight consecutive TDC cycles to clock out a complete PCM word for byte interleaved applications. The transmit shift register feeds back on itself to allow multiple reads of the transmit data. If the PCM word is clocked out once per frame in a byte interleaved system, the MSI pin function is transparent and may be connected to TDE.

The TDE pin may be cycled during a PCM word for bit interleaved applications. TDE controls both the high impedance state of the TDD output and the internal shift clock. TDE must fall before TDC rises (t_{su8}) to ensure integrity of the next data bit. There must be at least two TDC falling edges between the last TDE rising edge of one frame and the first TDE rising edge of the next frame. MSI must be available separate from TDE for bit interleaved applications.

TDD
Transmit Digital Data Output

The output levels at this pin are controlled by the V_{LS} pin. For V_{LS} connected to V_{DD}, the output levels are from V_{SS} to V_{DD}. For a voltage of V_{LS} between $V_{DD} - 4$ V and V_{SS}, the output levels are TTL compatible with V_{LS} being the digital ground supply. The TDD pin is a three–state output controlled by the TDE pin. The timing of this pin is controlled by TDC and TDE. When in TTL mode, this output may be made high–speed CMOS compatible using a pull–up resistor. The data format (Mu–Law, A–Law, or sign magnitude) is controlled by the Mu/A pin.

RDC
Receive Data Clock Input

RDC can be any frequency from 64 kHz to 4.096 MHz. This pin is often tied to the TDC pin for applications that can use a common clock for both transmit and receive data transfers. The receive shift register is controlled by the receive clock enable (RCE) pin to clock data into the receive digital data (RDD) pin on falling RDC edges. These three signals can be asynchronous with all other digital pins. The RDC input is internally tied to the TDC input on the MC145505 and called DC.

RCE
Receive Clock Enable Input

The rising edge of RCE should identify the sign bit of a receive PCM word on RDD. The next falling edge of RDC, after a rising RCE, loads the first bit of the PCM word into the receive register. The next seven falling edges enter the remainder of the PCM word. On the ninth rising edge, the receive PCM word is transferred to the receive buffer register and the A/D sequence is interrupted to commence the decode process. In asynchronous applications with an 8 kHz transmit sample rate, the receive sample rate should be between 7.5 and 8.5 kHz. Two receive PCM words may be decoded and analog summed each transmit frame to allow on–chip conferencing. The two PCM words should be clocked in as two single PCM words, a minimum of 31.25 μs apart, with a receive data clock of 512 kHz or faster.

RDD
Receive Digital Data Input

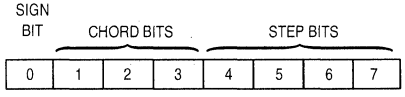
RDD is the receive digital data input. The timing for this pin is controlled by RDC and RCE. The data format is determined by the Mu/A pin.

Mu/A
Select

This pin selects the companding law and the data format at TDD and RDD.

Mu/A = V_{DD}; Mu–255 Companding D3 Data Format with Zero Code Suppress
Mu/A = V_{AG}; Mu–255 Companding with Sign Magnitude Data Format
Mu/A = V_{SS}; A–Law Companding with CCITT Data Format Bit Inversions

Code	Sign/ Magnitude	Mu–Law	A–Law (CCITT)
+ Full Scale	1111 1111	1000 0000	1010 1010
+ Zero	1000 0000	1111 1111	1101 0101
– Zero	0000 0000	0111 1111	0101 0101
– Full Scale	0111 1111	0000 0010	0010 1010



NOTE: Starting from sign magnitude, to change format:
To Mu–Law —
MSB is unchanged (sign)
Invert remaining seven bits
If code is 0000 0000, change to 0000 0010 (for zero code suppression)
To A–Law —
MSB is unchanged (sign)
Invert odd numbered bits
Ignore zero code suppression

$\overline{PDI}$
Power Down Input

The power down input disables the bias circuitry and gates off all clock inputs. This puts the V_{AG}, TxI, RxO, $\overline{RxO}$, and TDD outputs into a high–impedance state. The power dissipation is reduced to 0.1 mW when $\overline{PDI}$ is a low logic level. The circuit operates normally with $\overline{PDI}$ = V_{DD} or with a logic high as defined by connection at V_{LS}. TDD will not come out of high impedance for two MSI cycles after $\overline{PDI}$ goes high.

DCLK
Data Clock Input

In the MC145505, TDC and RDC are internally connected to DCLK.

ANALOG

V_{AG}
Analog Ground Input/Output Pin

V_{AG} is the analog ground power supply input/output. All analog signals into and out of the device use this as their ground reference. Each version of the MC145500 PCM Codec–Filter family can provide its own analog ground supply internally. The dc voltage of this internal supply is 6% positive of the midway between V_{DD} and V_{SS}. This supply can sink more than 8 mA but has a current source limited to 400 μA. The output of this supply is internally connected to the analog ground input of the part. The node where this supply and the analog ground are connected is brought out to the V_{AG} pin. In symmetric dual supply systems (± 5, ± 6, etc.), V_{AG} may be externally tied to the system analog ground supply. When RxO or $\overline{RxO}$ drive low impedance loads tied to V_{AG}, a pull–up resistor to V_{DD} will be required to boost the source current capability if V_{AG} is not tied to the supply ground. All analog signals for the part are referenced to V_{AG}, including noise; therefore, decoupling capacitors (0.1 μF) should be used from V_{DD} to V_{AG} and V_{SS} to V_{AG}.

V_{ref}
Positive Voltage Reference Input (MC145502 Only)

The V_{ref} pin allows an external reference voltage to be used for the A/D and D/A conversions. If V_{ref} is tied to V_{SS}, the internal reference is selected. If $V_{ref} > V_{AG}$, then the external mode is selected and the voltage applied to V_{ref} is used for generating the internal converter reference voltage. In either internal or external reference mode, the actual voltage used for conversion is multiplied by the ratio selected by the RSI pin. The RSI pin circuitry is explained under its pin description below. Both the internal and external references are inverted within the PCM Codec–Filter for negative input voltages such that only one reference is required.

External Mode — In the external reference mode ($V_{ref} > V_{AG}$), a 2.5 V reference like the MC1403 may be connected from V_{ref} to V_{AG}. A single external reference may be shared by tying together a number of V_{ref} pins and V_{AG} pins from different codec–filters. In special applications, the external reference voltage may be between 0.5 and 5 V. However, the reference voltage gain selection circuitry associated with RSI must be considered to arrive at the desired codec–filter gain.

Internal Mode — In the internal reference mode ($V_{ref} = V_{SS}$), an internal 2.5 V reference supplies the reference voltage for the RSI circuitry. The V_{ref} pin is functionally connected to V_{SS} for the MC145500, MC145501, MC145503, and MC145505 pinouts.

RSI
Reference Select Input (MC145501/02 Only)

The RSI input allows the selection of three different overload or full–scale A/D and D/A converter reference voltages independent of the internal or external reference mode. The RSI pin is a digital input that senses three different logic states: V_{SS}, V_{AG}, and V_{DD}. For RSI = V_{AG}, the reference voltage is used directly for the converters. The internal reference is 2.5 V. For RSI = V_{SS}, the reference voltage is multiplied by the ratio of 1.26, which results in an internal converter reference of 3.15 V. For RSI = V_{DD}, the reference voltage is multiplied by 1.51, which results in an internal converter reference of 3.78 V. The device requires a minimum of 1.0 V of headroom between the internal converter reference to V_{DD}. V_{SS} has this same absolute valued minimum, also measured from V_{AG} pin. The various modes of operation are summarized in Table 2. The RSI pin is functionally connected to V_{SS} for the MC145500, MC145503, and MC145505 pinouts.

RxO, $\overline{\text{RxO}}$
Receive Analog Outputs

These two complimentary outputs are generated from the output of the receive filter. They are equal in magnitude and out of phase. The maximum signal output of each is equal to the maximum peak–to–peak signal described with the reference. If a 3.15 V reference is used with RSI tied to V_{AG} and a + 3 dBm0 sine wave is decoded, the RxO output will be a 6.3 V peak–to–peak signal. $\overline{\text{RxO}}$ will also have an inverted signal output of 6.3 V peak–to–peak. External loads may be connected from RxO to $\overline{\text{RxO}}$ for a 6 dB push–pull signal gain or from either RxO or $\overline{\text{RxO}}$ to V_{AG}. With a 3.15 V reference each output will drive 600 Ω to + 9 dBm. With RSI tied to V_{DD}, each output will drive 900 Ω to + 9 dBm.

RxG
Receive Output Gain Adjust (MC145502 Only)

The purpose of the RxG pin is to allow external gain adjustment for the $\overline{\text{RxO}}$ pin. If RxG is left open, then the output signal at RxO will be inverted and output at $\overline{\text{RxO}}$. Thus the push–pull gain to a load from RxO to $\overline{\text{RxO}}$ is two times the output level at RxO. If external resistors are applied from RxO to RxG (RI) and from RxG to $\overline{\text{RxO}}$ (RG), the gain of $\overline{\text{RxO}}$ can be set differently from inverting unity. These resistors should be in the range of 10 kΩ. The RxO output level is unchanged by the resistors and the $\overline{\text{RxO}}$ gain is approximately equal to minus RG/RI. The actual gain is determined by taking into account the internal resistors which will be in parallel to these external resistors. The internal resistors have a large tolerance, but they match each other very closely. This matching tends to minimize the effects of their tolerance on external gain configurations. The circuit for RxG and $\overline{\text{RxO}}$ is shown in the block diagram.

TxI
Transmit Analog Input

TxI is the input to the transmit filter. It is also the output of the transmit gain amplifiers of the MC145501/02/03/05. The input impedance is greater than 100 kΩ to V_{AG} in the MC145500. The TxI input has an internal gain of 1.0, such that a +3 dBm0 signal at TxI corresponds to the peak converter reference voltage as described in the V_{ref} and RSI pin descriptions. For 3.15 V reference, the + 3 dBm0 input should be 6.3 V peak–to–peak.

+Tx / –Tx
Positive Tx Amplifier Input (MC145502/03/05 Only) / Negative Tx Amplifier Input (MC145501/02/03/05 Only)

The TxI pin is the input to the transmit band–pass filter. If +Tx or –Tx is available, then there is an internal amplifier preceding the filter whose pins are +Tx, –Tx, and TxI. These pins allow access to the amplifier terminals to tailor the input gain with external resistors. The resistors should be in the range of 10 kΩ. If +Tx is not available, it is internally tied to V_{AG}. If –Tx and +Tx are not available, the TxI is a unity gain high–impedance input.

POWER SUPPLIES

V_{DD}
Most Positive Power Supply

V_{DD} is typically 5 to 12 V.

V_{SS}
Most Negative Power Supply

V_{SS} is typically 10 to 12 V negative of V_{DD}.

For a ± 5 V dual–supply system, the typical power supply configuration is V_{DD} = + 5 V, V_{SS} = – 5 V, V_{LS} = 0 V (digital ground accommodating TTL logic levels), and V_{AG} = 0 V being tied to system analog ground.

For single–supply applications, typical power supply configurations include:

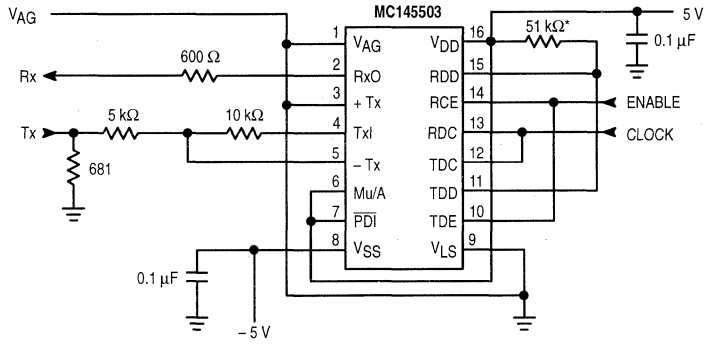
V_{DD} = 10 V to 12 V
V_{SS} = 0 V

V_{AG} generates a mid supply voltage for referencing all analog signals.

V_{LS} controls the logic levels. This pin should be connected to V_{DD} for CMOS logic levels from V_{SS} to V_{DD}. This pin should be connected to digital ground for true TTL logic levels referenced to V_{LS}.

TESTING CONSIDERATIONS (MC145500/01/02 ONLY)

An analog test mode is activated by connecting MSI and CCI to 128 kHz. In this mode, the input of the A/D (the output of the Tx filter) is available at the $\overline{\text{PDI}}$ pin. This input is direct coupled to the A/D side of the codec. The A/D is a differential design. This results in the gain of this input being effectively attenuated by half. If monitored with a high–impedance buffer, the output of the Tx low–pass filter can also be measured at the $\overline{\text{PDI}}$ pin. This test mode allows independent evaluation of the transmit low–pass filter and A/D side of the codec. The transmit and receive channels of these devices are tested with the codec–filter fully functional.



* To define RDD when TDD is high Z.

Figure 1. Test Circuit

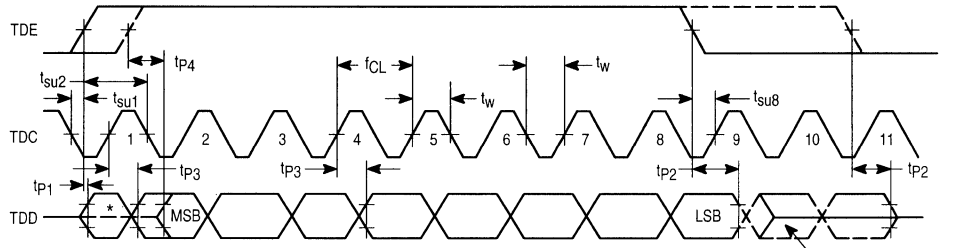
Table 1. Options Available by Pin Selection

RSI* Pin Level	V_{ref}* Pin Level	Peak–to–Peak Overload Voltage (Txl, RxO)
V_{DD}	V_{SS}	7.56 V p–p
V_{DD}	$V_{AG} + V_{EXT}$	(3.02 x V_{EXT}) V p–p
V_{AG}	V_{SS}	5 V p–p
V_{AG}	$V_{AG} + V_{EXT}$	(2 x V_{EXT}) V p–p
V_{SS}	V_{SS}	6.3 V p–p
V_{SS}	$V_{AG} + V_{EXT}$	(2.52 x V_{EXT}) V p–p

* On MC145500/03/05, RSI and V_{ref} tied internally to V_{SS}. On MC145501, V_{ref} tied internally to V_{SS}.

Table 2. Summary of Operation Conditions User Programmed Through Pins V_{DD}, V_{AG}, and V_{SS}

Pin Programmed / Logic Level	Mu/A	RSI Peak Overload Voltage	V_{LS}
V_{DD}	Mu–Law Companding Curve and D3/D4 Digital Formats with Zero Code Suppress	3.78	CMOS Logic Levels
V_{AG}	Mu–Law Companding Curve and Sign Magnitude Data Format	2.50	TTL Levels V_{AG} Up
V_{SS}	A–Law Companding Curve and CCITT Digital Format	3.15	TTL Levels V_{SS} Up



* Data output during this time will vary depending on TDC rate and TDE timing.

Figure 2. Transmit Timing Diagram

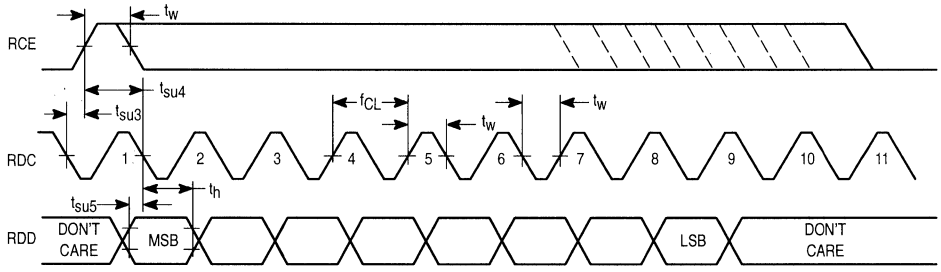


Figure 3. Receive Timing Diagram

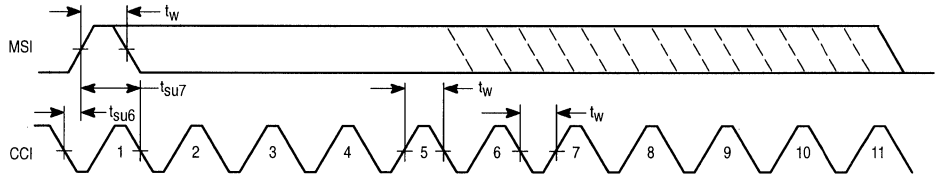


Figure 4. MSI/CCI Timing Diagram

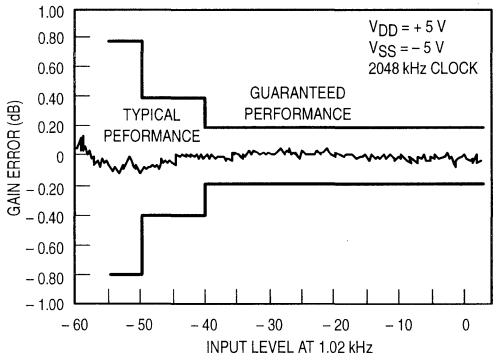


Figure 5. MC145502 Gain vs Level Mu–Law Transmit

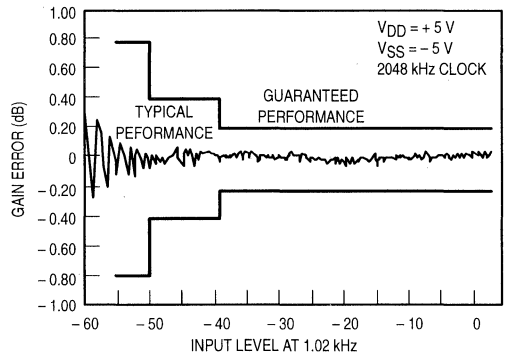


Figure 6. MC145502 Gain vs Level Mu–Law Receive

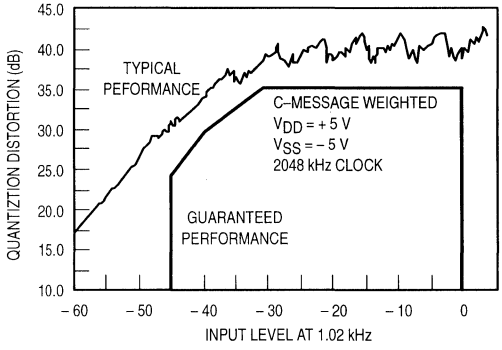


Figure 7. MC145502 Quantization Distortion Mu–Law Transmit

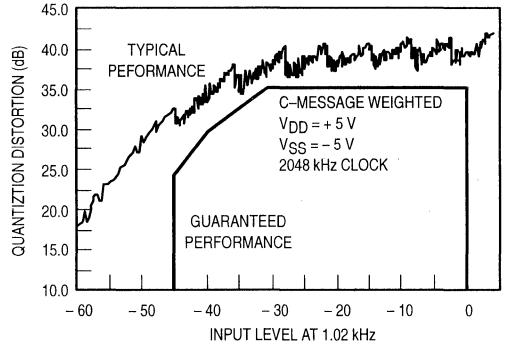


Figure 8. MC145502 Quantization Distortion Mu–Law Receive

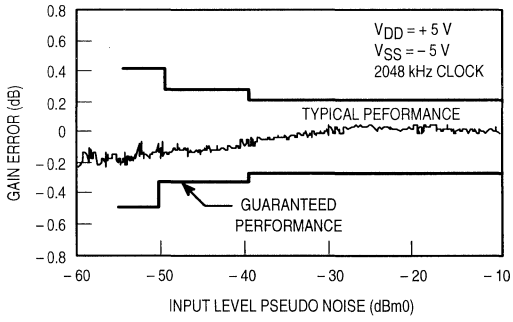


Figure 9. MC145502 Gain vs Level A–Law Transmit

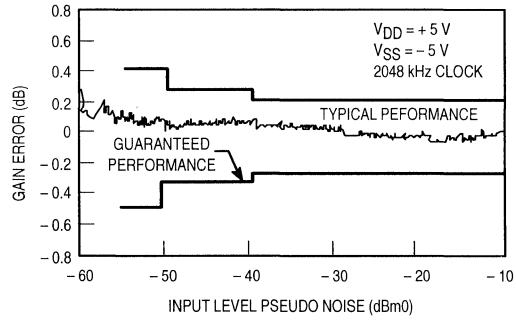


Figure 10. MC145502 Gain vs Level A–Law Receive

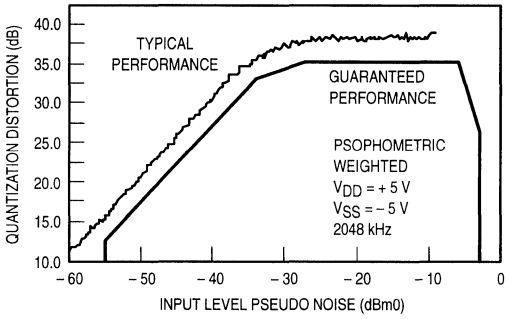


Figure 11. MC145502 Quantization Distortion A–Law Transmit

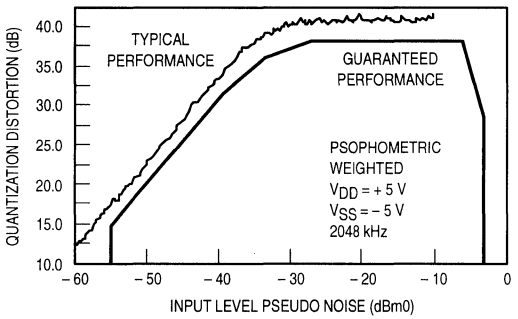


Figure 12. MC145502 Quantization Distortion A–Law Receive

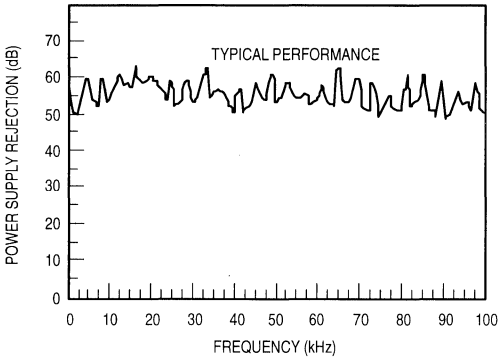


Figure 13. MC145502 Power Supply Rejection Ratio Positive Transmit VAC = 250 mVrms, C–Message Weighted

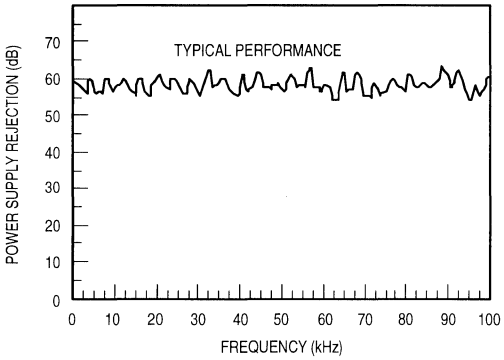


Figure 14. MC145502 Power Supply Rejection Ratio Negative Transmit VAC = 250 mVrms, C–Message Weighted

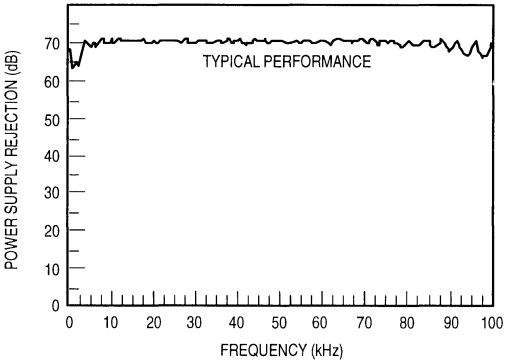


Figure 15. MC145502 Power Supply Rejection Ratio Positive Receive VAC = 250 mVrms, C–Message Weighted

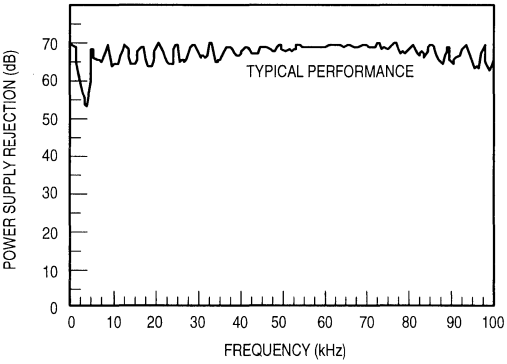


Figure 16. MC145502 Power Supply Rejection Ratio Negative Receive VAC = 250 mVrms, C–Message Weighted

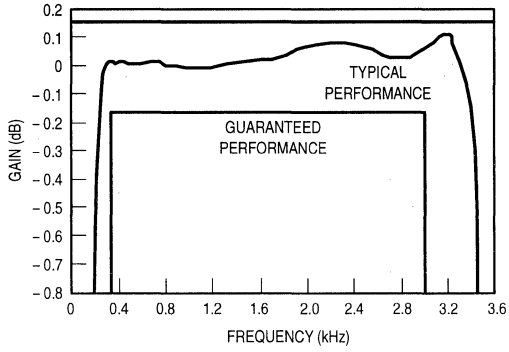


Figure 17. MC145502 Pass–Band Filter Response Transmit

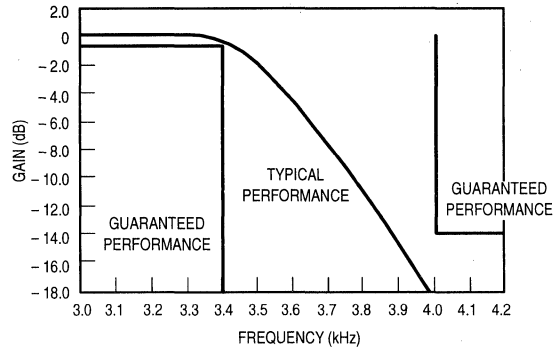


Figure 18. MC145502 Low–Pass Filter Response Transmit

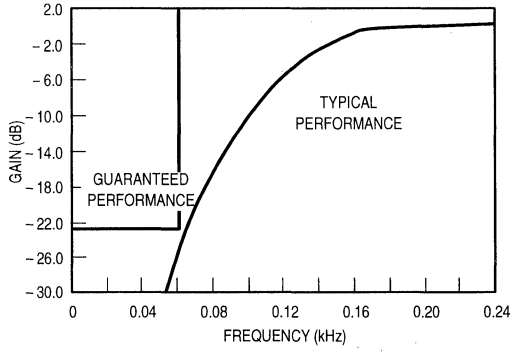


Figure 19. MC145502 High–Pass Filter Response Transmit

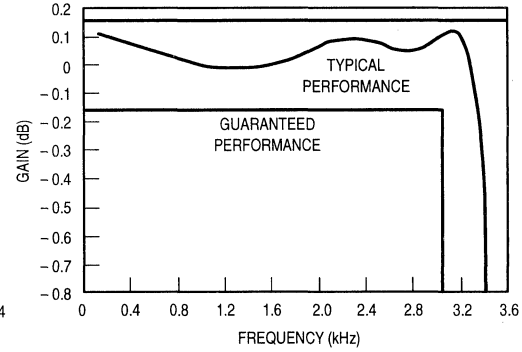


Figure 20. MC145502 Pass–Band Filter Response Receive

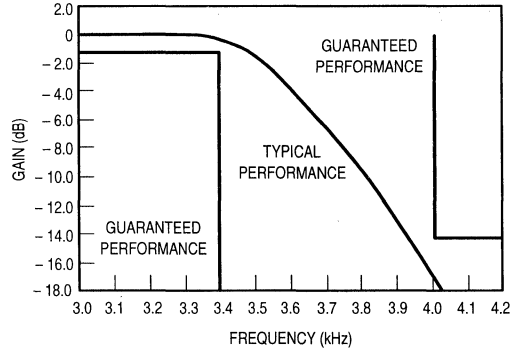
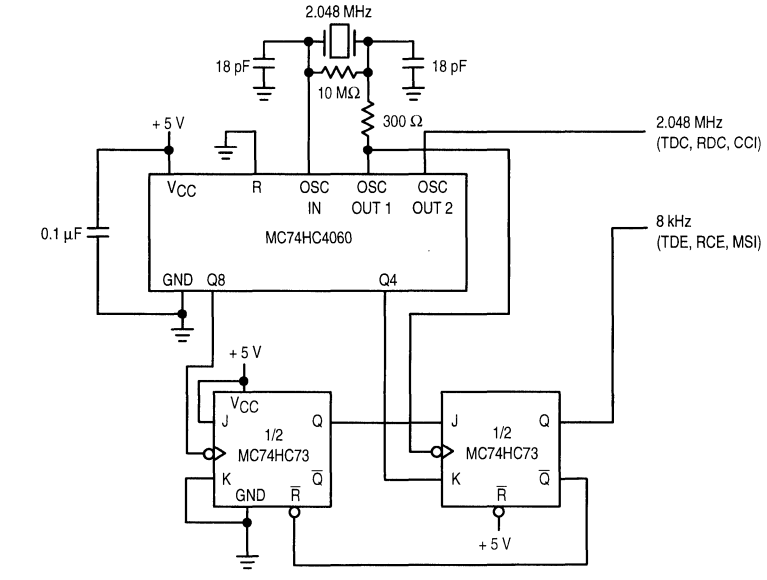


Figure 21. MC145502 Low–Pass Filter Response Receive



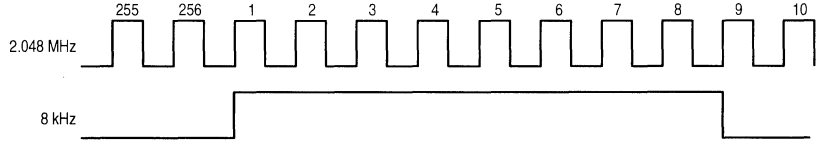
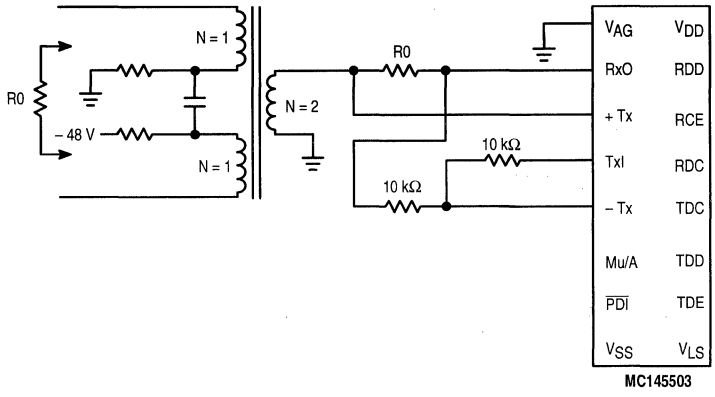
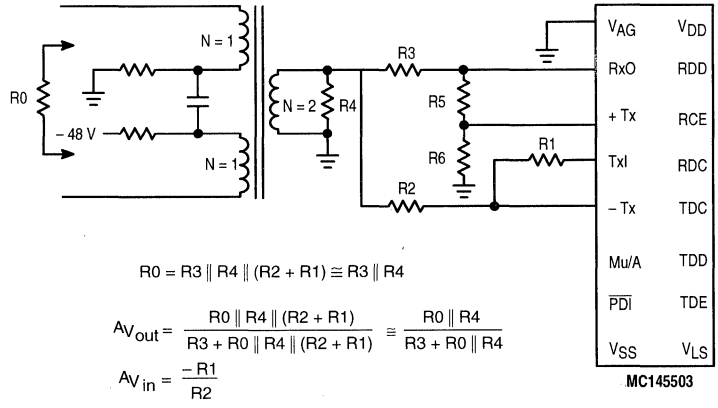


Figure 22. Simple Clock Circuit for Driving MC145500/01/02/03/05 Codec–Filters



23a. Simplified Transformer Hybrid Using MC145503



$$R0 = R3 \parallel R4 \parallel (R2 + R1) \cong R3 \parallel R4$$

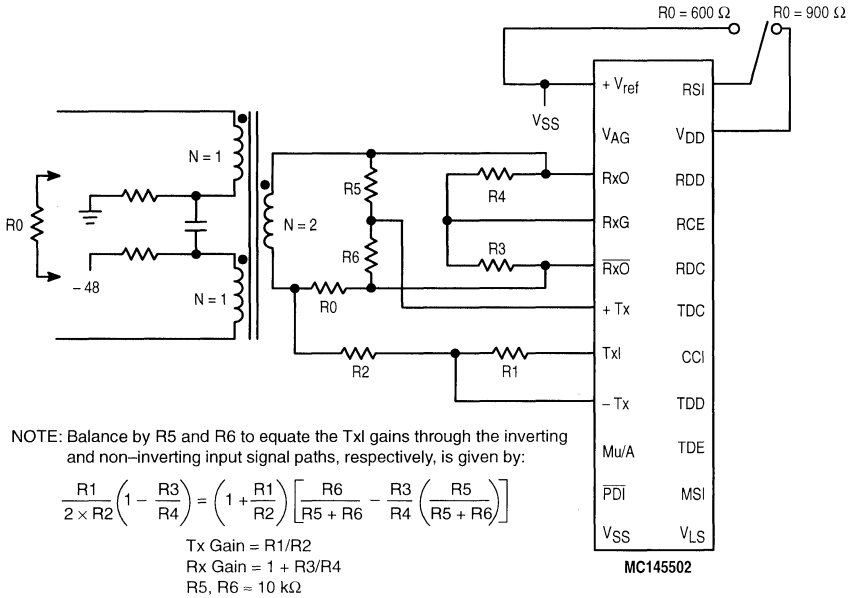
$$A_{V_{out}} = \frac{R0 \parallel R4 \parallel (R2 + R1)}{R3 + R0 \parallel R4 \parallel (R2 + R1)} \cong \frac{R0 \parallel R4}{R3 + R0 \parallel R4}$$

$$A_{V_{in}} = \frac{-R1}{R2}$$

NOTE: Hybrid Balance by R5 and R6 to equate the RxO signal gain at TxI through the inverting and non–inverting signal paths.

23b. Universal Transformer Hybrid Using MC145503

Figure 23. Hybrid Interfaces to the MC145503 PCM Codec–Filter Mono–Circuit

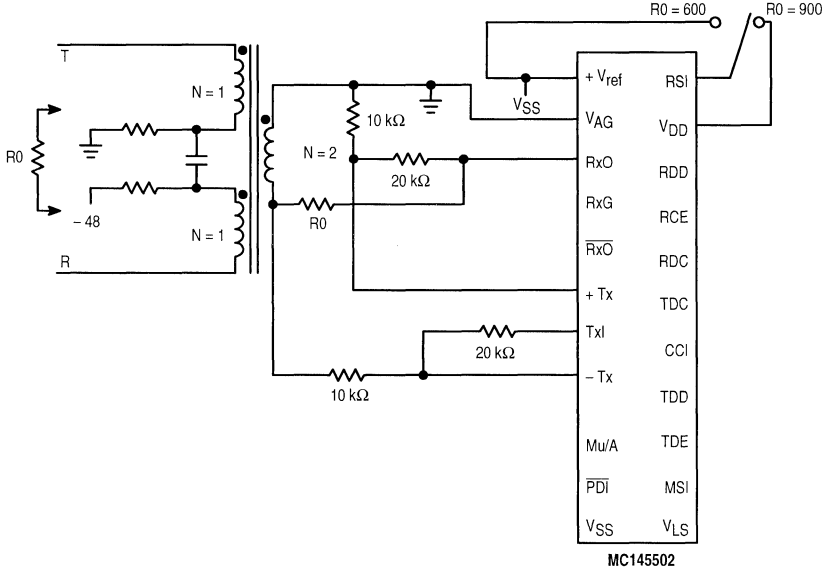


NOTE: Balance by R5 and R6 to equate the Txl gains through the inverting and non–inverting input signal paths, respectively, is given by:

$$\frac{R1}{2 \times R2}\left(1 - \frac{R3}{R4}\right) = \left(1 + \frac{R1}{R2}\right)\left[\frac{R6}{R5 + R6} - \frac{R3}{R4}\left(\frac{R5}{R5 + R6}\right)\right]$$

Tx Gain = R1/R2
Rx Gain = 1 + R3/R4
R5, R6 ≈ 10 kΩ
Adjust Rx Gain with R3
Adjust Tx Gain with R1

24a. Universal Transformer Hybrid Using MC145502



24b. Single–Ended Hybrid Using MC145502

Figure 24. Hybrid Interfaces to the MC145502 PCM Codec–Filter Mono–Circuit

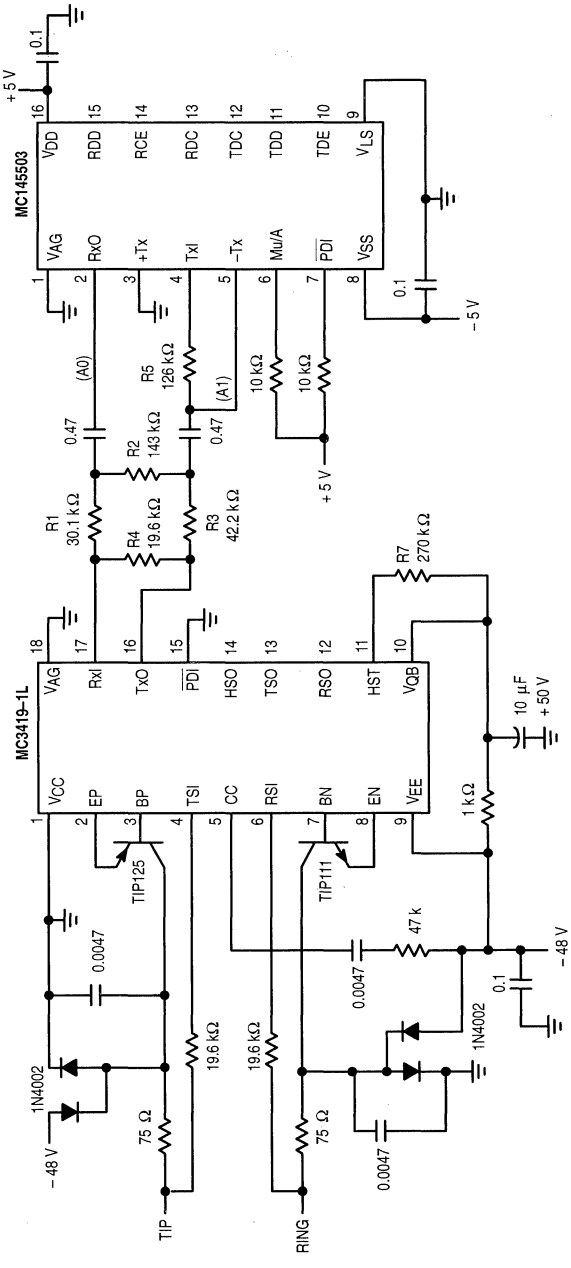


Figure 25. A Complete Single Party Channel Unit Using MC3419 SLIC and MC145503 PCM Mono–Circuit

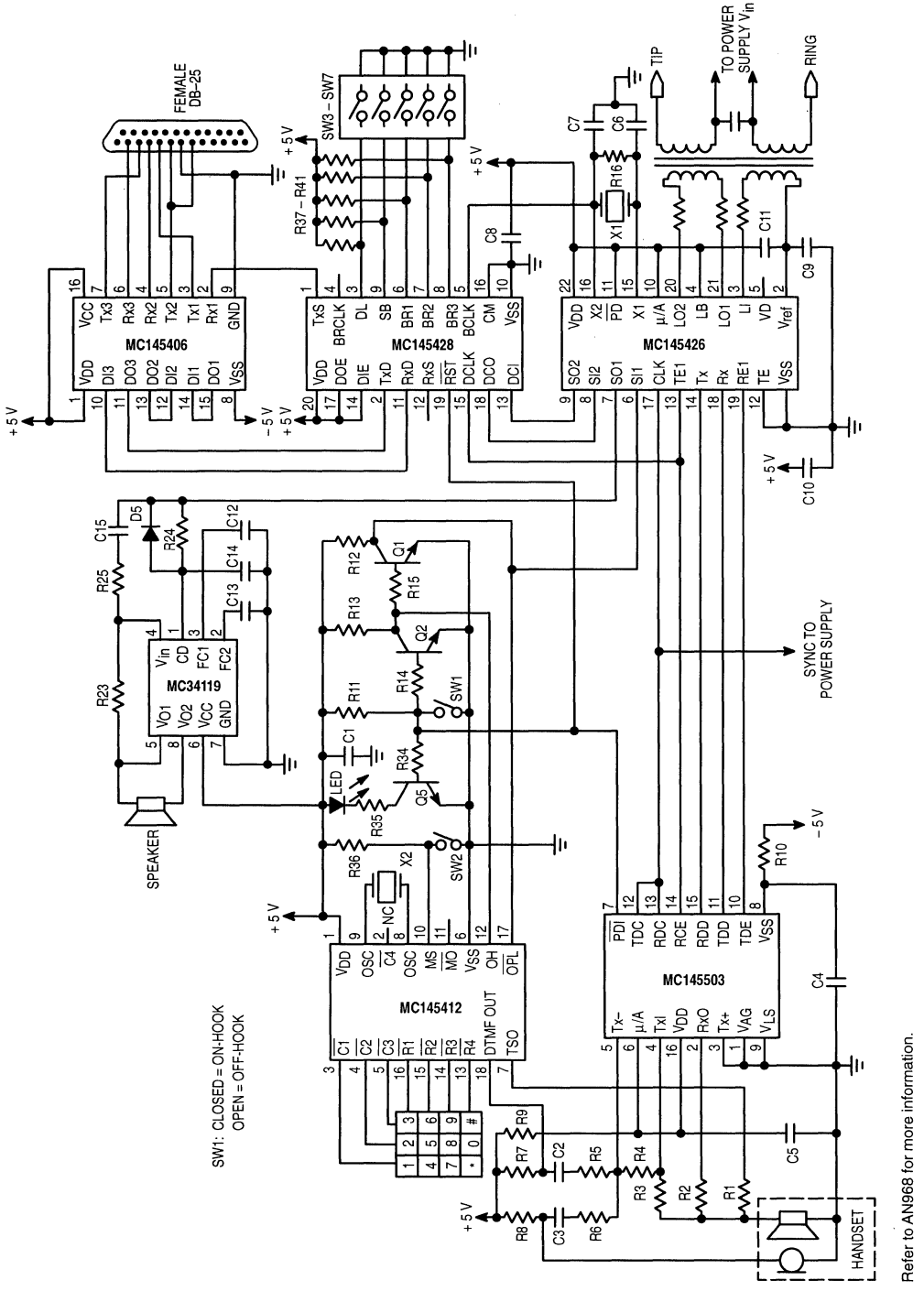


Figure 26. Digital Telephone Schematic

Table 3. Mu–Law Encode–Decode Characteristics

Chord Number	Number of Steps	Step Size	Normalized Encode Decision Levels	Digital Code 1 Sign	2 Chord	3 Chord	4 Chord	5 Step	6 Step	7 Step	8 Step	Normalized Decode Levels
			8159									
8	16	256		1	0	0	0	0	0	0	0	8031
			7903									
			⋮					⋮				⋮
			4319									
				1	0	0	0	1	1	1	1	4191
			4063									
7	16	128	⋮					⋮				⋮
			2143									
				1	0	0	1	1	1	1	1	2079
			2015									
			⋮					⋮				⋮
6	16	64	1055									
				1	0	1	0	1	1	1	1	1023
			991									
			⋮					⋮				⋮
5	16	32	511									
				1	0	1	1	1	1	1	1	495
			479									
			⋮					⋮				⋮
4	16	16	239									
				1	1	0	0	1	1	1	1	231
			223									
			⋮					⋮				⋮
3	16	8	103									
				1	1	0	1	1	1	1	1	99
			95									
			⋮					⋮				⋮
2	16	4	35									
				1	1	1	0	1	1	1	1	33
			31									
			⋮					⋮				⋮
1	15	2	3									
				1	1	1	1	1	1	1	0	2
			1									
	1	1		1	1	1	1	1	1	1	1	0
			0									

NOTES:
1. Characteristics are symmetrical about analog zero with sign bit = 0 for negative analog values.
2. Digital code includes inversion of all magnitude bits.

Table 4. A–Law Encode–Decode Characteristics

Chord Number	Number of Steps	Step Size	Normalized Encode Decision Levels	Digital Code 1 Sign	2 Chord	3 Chord	4 Chord	5 Step	6 Step	7 Step	8 Step	Normalized Decode Levels
			4096									
				1	0	1	0	1	0	1	0	4032
			3968									
7	16	128	⋮					⋮				⋮
			2176									
				1	0	1	0	0	1	0	1	2112
			2048									
6	16	64	⋮					⋮				⋮
			1088									
				1	0	1	1	0	1	0	1	1056
			1024									
5	16	32	⋮					⋮				⋮
			544									
				1	0	0	0	0	1	0	1	528
			512									
4	16	16	⋮					⋮				⋮
			272									
				1	0	0	1	0	1	0	1	264
			256									
3	16	8	⋮					⋮				⋮
			136									
				1	1	1	0	0	1	0	1	132
			128									
2	16	4	⋮					⋮				⋮
			68									
				1	1	1	1	0	1	0	1	66
			64									
1	32	2	⋮					⋮				⋮
			2									
				1	1	0	1	0	1	0	1	1
			0									

NOTES:
1. Characteristics are symmetrical about analog zero with sign bit = 0 for negative analog values.
2. Digital code includes alternate bit inversion, as specified by CCITT.

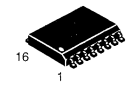
MC145532

ADPCM Transcoder

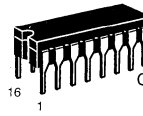
Conforms to G.721–1988 and T1.301–1987

The MC145532 Adaptive Differential Pulse Code Modulation (ADPCM) Transcoder provides a low–cost, full–duplex, single–channel transcoder to (from) a 64 kbps PCM channel from (to) either a 16 kbps, 24 kbps, 32 kbps, or 64 kbps channel.

- Complies with CCITT Recommendation G.721–1988
- Complies with the American National Standard (T1.301–1987)
- Full–Duplex, Single–Channel Operation
- Mu–Law or A–Law Coding is Pin Selectable
- Synchronous or Asynchronous Operation
- Easily Interfaces with Any Member of Motorola's PCM Codec–Filter Mono–Circuit Family or Other Industry Standard Codec
- Serial PCM and ADPCM Data Transfer Rate from 64 kbps to 5.12 Mbps
- Power–Down Capability for Low Current Consumption
- The Reset State, an Option Specified in the Standards, is Automatically Initiated When the RESET Pin is Released
- Simple Time Slot Assignment Timing for Transcoder Applications
- Single 5 V Power Supply
- 16–Pin Package
- The MC145536EVK is the Evaluation Platform for the MC145532 and Also Includes the MC145480 5 V PCM Codec–Filter



DW SUFFIX
SOG PACKAGE
CASE 751G

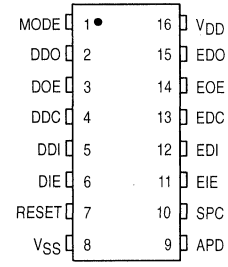


L SUFFIX
CERAMIC PACKAGE
CASE 620

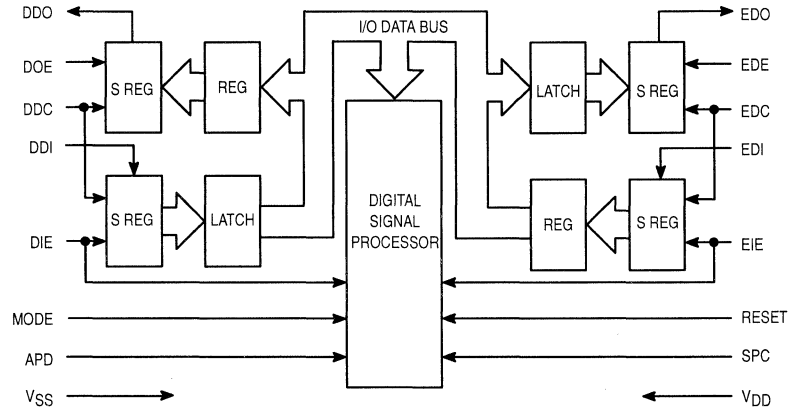
ORDERING INFORMATION

MC145532DW	SOG Package
MC145532L	Ceramic Package

PIN ASSIGNMENT



BLOCK DIAGRAM



REV 1
9/95 (Replaces NP470)

DEVICE DESCRIPTION

An Adaptive Differential PCM (ADPCM) transcoder is used to reduce the data rate required to transmit a PCM encoded voice signal while maintaining the voice fidelity and intelligibility of the PCM signal.

The transcoder is used on 64 kbps data streams which represent either voice or voice band data signals that have been digitized by a codec (e.g., MC145557). The transcoder uses a filter to attempt to predict the next PCM input value based on previous PCM input values. The error between the predicted and the true PCM input value is the information that is sent to the other end of the line. Hence the word differential, since the ADPCM data stream is the difference between the true PCM input value and the predicted value. The term "adaptive" applies to the filter that is performing the prediction. It is adaptive in that its transfer function changes based on the PCM input data. That is, it adapts to the statistics of the signals presented to it.

PIN DESCRIPTIONS

ENCODER INPUT

EDI
Encoder Data Input (Pin 12)

PCM data to be encoded are applied to this input pin which operates synchronously with EDC and EIE to enter the data in a serial format.

EDC
Encoder Data Clock (Pin 13)

Data applied to EDI are latched into the transcoder on a falling edge of EDC and data are output from EDO on a rising edge of this input pin. The frequency of EDC may be as low as 64 kHz or as high as 5.12 MHz.

EIE
Encoder Input Enable (Pin 11)

The beginning of a new PCM word is indicated to the transcoder by a rising edge applied to this input. The frequency of EIE may not exceed 8 kHz.

ENCODER OUTPUT

EDO
Encoder Data Output (Pin 15)

ADPCM data are available in a serial format from this output, which operates synchronously with EDC and EOE. EDO is a three–state output which remains in a high–impedance state, except when presenting data.

EOE
Encoder Output Enable (Pin 14)

Each ADPCM word is requested by a rising edge on this input, which causes the EDO pin to provide the data when clocked by EDC. One EOE must occur for each EIE.

DECODER INPUT

DDI
Decoder Data Input (Pin 5)

ADPCM data to be decoded are applied to this input pin, which operates in conjunction with DDC and DIE to enter the data in a serial format.

DDC
Decoder Data Clock (Pin 4)

Data applied to DDI are latched into the transcoder on the falling edge of DDC and data are output from DDO on the rising edge of DDC. The frequency of DDC may be as low as 64 kHz or as high as 5.12 MHz.

DIE
Decoder Input Enable (Pin 6)

The beginning of a new ADPCM word is indicated by a rising edge applied to this input. Data are serially clocked into DDI on the subsequent falling edges of DDC following the DIE rising edge. The frequency of DIE may not exceed 8 kHz.

DECODER OUTPUT

DDO
Decoder Data Output (Pin 2)

PCM data are available in a serial format from this output, which operates in conjunction with DDC and DOE. DDO is a three–state output that remains at a high–impedance state except when presenting data.

DOE
Decoder Output Enable (Pin 3)

Each ADPCM word is requested by a rising edge on this input which causes the DDO pin to provide the data when clocked by DDC. One DOE must occur for each DIE.

CONTEXT

MODE
Mode Select (Pin 1)

A logic 0 applied to this input makes the transcoder compatible with Mu–255 companding and D3 data format. A logic 1 applied to this pin makes the transcoder compatible with A–Law companding with even bit inversion data format.

SPC
Signal Processor Clock (Pin 10)

This input is typically clocked with a 20.48 MHz clock signal which is used as the digital signal processor master clock. This pin has a CMOS compatible input.

RESET
Reset (Pin 7)

A logic 0 applied to this input forces the transcoder into a low power dissipation mode. A rising edge on this pin causes power to be restored and the optional transcoder RESET state (specified in the standards) to be forced. Valid data is available at the output pins four input enables after a rising edge on this pin. This pin has a CMOS compatible input.

APD
Absolute Power Down (Pin 9)

A logic 1 applied to this input forces the transcoder into a power saving mode. This pin has a CMOS compatible input.

POWER SUPPLY

V_{DD}
Positive Power Supply (Pin 16)

The most positive power supply pin, normally 5 V.

V_{SS}
Negative Power Supply (Pin 8)

The most negative power supply pin, normally 0 V.

FUNCTIONAL DESCRIPTION

ENCODING/DECODING RATES

The MC145532 allows for the encoding and decoding of data at one of four rates on a sample–by–sample basis. Each data sample that is provided to the part is accompanied by an indication of the rate at which it is to be encoded or decoded. The width of the enable pulse determines the encoding/decoding rate chosen for each sample.

The 64 kbps rate allows for PCM data to be passed directly through the part. The 32 kbps rate is either the G.721–1988 or the T1.301–1987 standard, depending on the state of the mode pin. The 24 kbps encoding rate is compliant with CCITT G.723–1988 and G.726. The 16 kbps rate is a modified quantizer from the 32 kbps technique and is not a standard.

TIMING

Figures 1 through 8 show the timing of the input and output pins. The MC145532 determines the mode of the timing signals, either short or long frame, for each enable, independent of the mode of any previous enables. A transition from short frame to long frame mode or vice versa will cause at least one frame of data to be destroyed. Each of the four sets of I/O pins determines its mode independent of the other sets. Thus the encoder input could be operating with long frame timing and the output could be operating with short frame timing. Note that the short frame timing on the input enables can only be used with the 32 kbps transcoding rate. The number of data clock falling edges enclosed by the input enable line (EIE or DIE) determines both the short frame or long frame mode and the transcoding rate. The mode of the input or output is determined each frame. In all modes, the data is captured by the MC145532 on the falling edge of either EDC or DDC.

ENCODER INPUT — SHORT FRAME

Figure 1 shows the timing of the encoder data clock (EDC), the encoder input enable (EIE), and the encoder data input (EDI) pins in short frame operation.

The determination of short frame mode is made by the MC145532 based on one falling EDC edge while EIE is high. Note that only a 32 kbps encoding rate can be specified when using short frame mode on the encoder input.

ENCODER INPUT — LONG FRAME

Figure 2 shows the clock, enable, and data signals for the encoder input in long frame mode. In this mode, the data is captured by the MC145532 on the falling edge of EDC.

The determination of the encoding rate is made based on the number of falling EDC edges seen by the MC145532 while EIE is high. Four edges implies a 32 kbps encoding rate, three edges implies a 24 kbps encoding rate, two edges implies a 16 kbps rate, and from five to eight inclusive imply a 64 kbps rate. The encoding rate may be changed on a frame–by–frame basis. The encoded word is available at EDO (via EOE and EDC) from 250 μs to 375 μs after it is requested.

ENCODER OUTPUT — SHORT FRAME

Figure 3 shows the timing of the encoder output in short frame mode. The length of the LSB is always one half of an EDC cycle.

The EDO will provide the correct number of bits for the encoding rate that was selected for this frame of data on the encoder input pins. The data is loaded into the MC145532 during one frame, encoded on the next frame, and read during the third frame.

ENCODER OUTPUT — LONG FRAME

Figure 4 shows the timing of the encoder output in long frame mode. The enable must be wider than two falling edges of the EDC to be in long frame mode. If the enable falls before the correct number of bits have been presented to the output (EDO), the transcoder will complete the presentation of the bits to the output with the LSB being one half of an EDC period wide. If the enable falls after the one half EDC period of the LSB, then the LSB will be extended up to the full EDC clock period and the subsequent data will be a recirculation of the previous data, which repeats until the enable pin falls. This is shown on the second enable for the 16 kbps encoding rate example in Figure 4.

DECODER INPUT — SHORT FRAME

Figure 5 shows the timing of the decoder data clock, the decoder input enable, and the decoder data input pins in short frame operation. Note that in this mode only a 32 kbps decoding rate can be selected.

DECODER INPUT — LONG FRAME

Figure 6 shows the clock, enable, and data signals for the decoder input in long frame mode.

The determination of the decoding rate is made based on the number of falling DDC edges seen by the MC145532 while DIE is high. Four edges implies a 32 kbps decoding rate, three edges implies a 24 kbps decoding rate, two edges implies a 16 kbps rate, and from five to eight edges inclusive imply a 64 kbps rate. The decoding rate may be changed on a frame–by–frame basis.

DECODER OUTPUT — SHORT FRAME

Figure 7 shows the timing of the decoder output in short frame mode.

The DDO will provide the 8–bit PCM word for the decoding rate that was selected for this frame of data on the decoder input pins. The data is loaded into the MC145532 during one frame, decoded on the next frame, and read during the third frame.

DECODER OUTPUT — LONG FRAME

Figure 8 shows the timing of the decoder output in long frame mode. Note that at least eight bits are presented to the output, provided that at least two falling edges of DDC are seen while DOE is high. The enable can be used to extend the LSB to a full DDC period and/or cause the eight bits of data to be recirculated to the output pin until the enable falls.

STANDARDS INFORMATION

The following standards apply to the MC145532:

T1.301–1987 — 32 kbps ADPCM
T1.303–1988 — 24 kbps ADPCM
CCITT G.721–1988, G.723–1988, and G.726 — 32 kbps and 24 kbps

CCITT, ITU–T, TIA, and EIA documents may be obtained by contacting Global Engineering Documents in the USA at (800) 854–7179, or internationally at (303) 397–7956.

2

ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	– 0.5 to + 7.0	V
Voltage, Any Pin to V_{SS}	V	– 0.5 to V_{DD} + 0.5	V
DC Current, Any Pin	I_{in}	± 10	mA
Operating Temperature	T_A	– 40 to + 85	°C
Storage Temperature	T_{stg}	– 85 to + 150	°C

This device contains circuitry to protect against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

RECOMMENDED OPERATING CONDITIONS (T_A = – 40 to + 85°C)

Parameter	Symbol	Min	Max	Unit
DC Supply Voltage	V_{DD}	4.50	5.50	V
Power Dissipation	P_D	—	0.28	W

DIGITAL CHARACTERISTICS (V_{DD} = 5.0 V, T_A = – 40 to + 85°C)

Parameter		Symbol	Min	Max	Unit
High Level Input Voltage	Mode, DOE, DDC, DDI, DIE, EIE, EDI, EDC, EOE	V_{IH}	2.0	—	V
Low Level Input Voltage	Mode, DOE, DDC, DDI, DIE, EIE, EDI, EDC, EOE	V_{IL}	—	0.8	V
High Level Input Voltage	RESET, APD, SPC	V_{IH}	0.7 V_{DD}	—	V
Low Level Input Voltage	RESET, APD, SPC	V_{IL}	—	0.3 V_{DD}	V
Input Current		I_{in}	—	± 1.0	µA
Input Capacitance		C_{in}	—	10	pF
High Level Output Voltage (I_{OH} = – 2.0 mA)	DDO, EDO	V_{OH}	4.6	—	V
Low Level Output Voltage (I_{OL} = 2.0 MA)	DDO, EDO	V_{OL}	—	0.4	V
Output Leakage Current (V_{DD} = 5.5 V)	DDO, EDO	I_{lkg}	—	± 5.0	µA

SWITCHING CHARACTERISTICS (V_{DD} = 5.0 V, T_A = – 40 to + 85°C)

Parameter	Min	Max	Unit
SPC Frequency	19.990	23	MHz
SPC Duty Cycle	45	55	%

ENCODER INPUT — SHORT FRAME (V_{DD} = 5.0 V, T_A = – 40 to + 85°C)

Parameter	Symbol	Min	Max	Unit
Enable Low Setup Time	$t_{su(EIE)L}$	15	—	ns
Enable Low Hold Time	$t_{h(EIE)H}$	30	—	ns
Enable Valid Time	$t_{V(EIE)}$	15	—	ns
Enable Hold Time	$t_{h(EIE)}$	15	—	ns
Data Valid Time	$t_{v(EDI)}$	15	—	ns
Data Hold Time	$t_{h(EDI)}$	15	—	ns

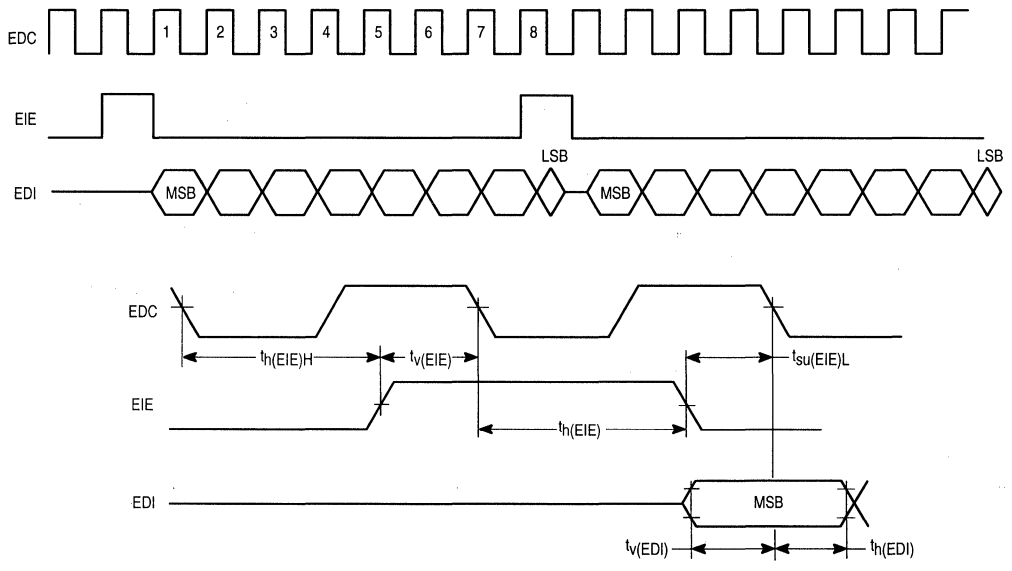


Figure 1. Encoder Input Timing — Short Frame

ENCODER INPUT — LONG FRAME (V_{DD} = 5.0 V, T_A = – 40 to + 85°C)

Parameter	Symbol	Min	Max	Unit
Enable Low Hold Time	$t_{h(EIE)L}$	30	—	ns
Enable Valid Time	$t_{v(EIE)}$	15	—	ns
Data Valid Time	$t_{v(EDI)}$	15	—	ns
Data Hold Time	$t_{h(EDI)}$	15	—	ns

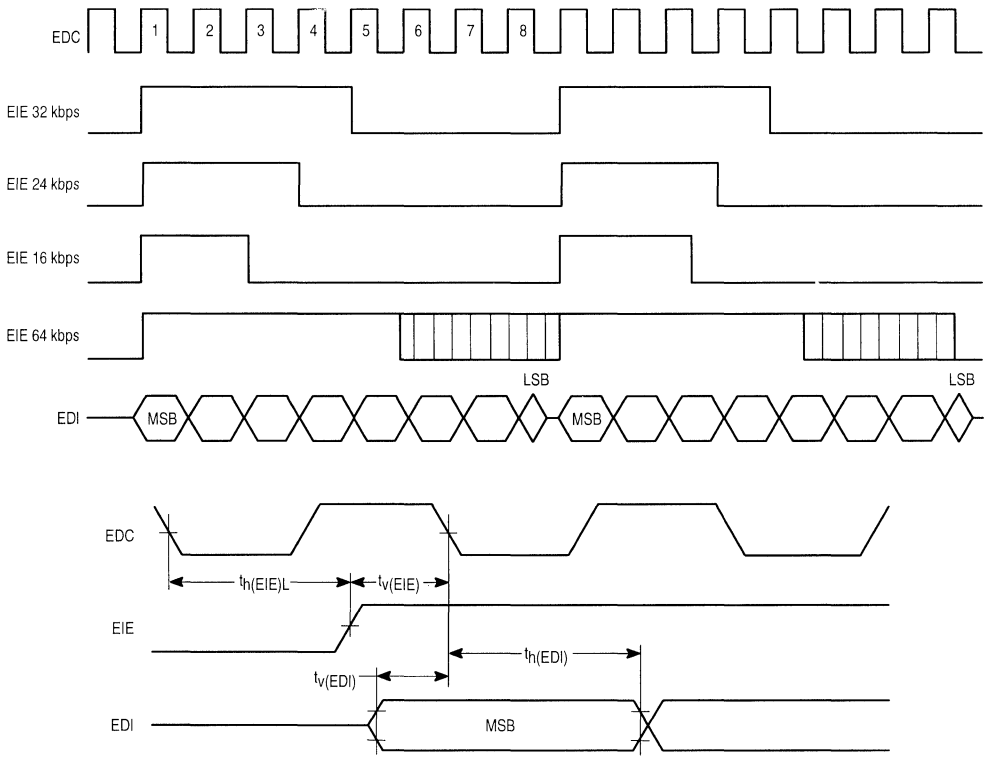


Figure 2. Encoder Input Timing — Long Frame

ENCODER OUTPUT — SHORT FRAME (V_{DD} = 5.0 V, T_A = – 40 to + 85°C)

Parameter	Symbol	Min	Max	Unit
Enable Low Hold Time	$t_{h(EOE)L}$	30	—	ns
Enable Valid Time	$t_{v(EOE)}$	15	—	ns
Enable Hold Time	$t_{h(EOE)}$	15	—	ns
Data Valid Time	$t_{v(EDO)}$	—	40	ns
Data Three–State Time (with 150 pF Load)	$t_{z(EDO)}$	1	30	ns

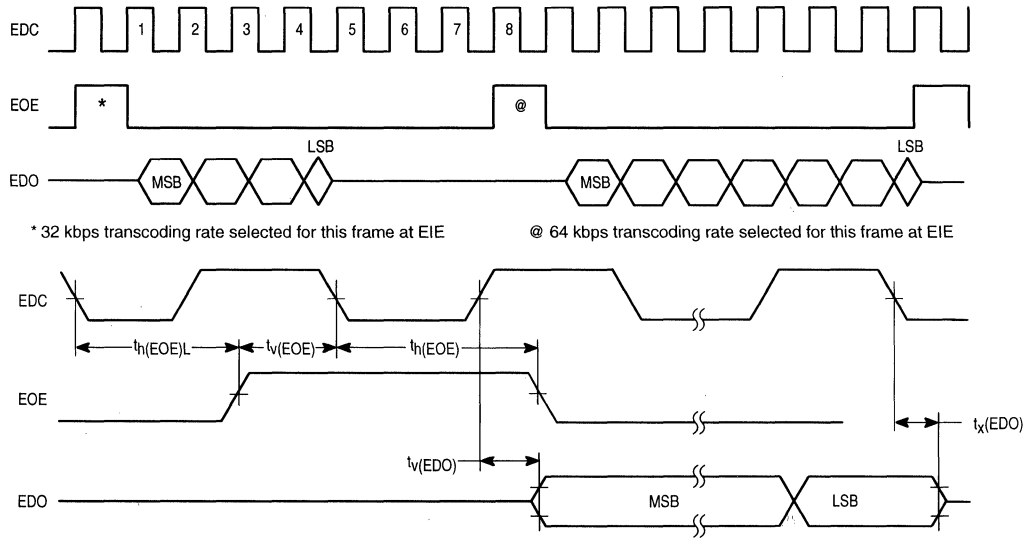
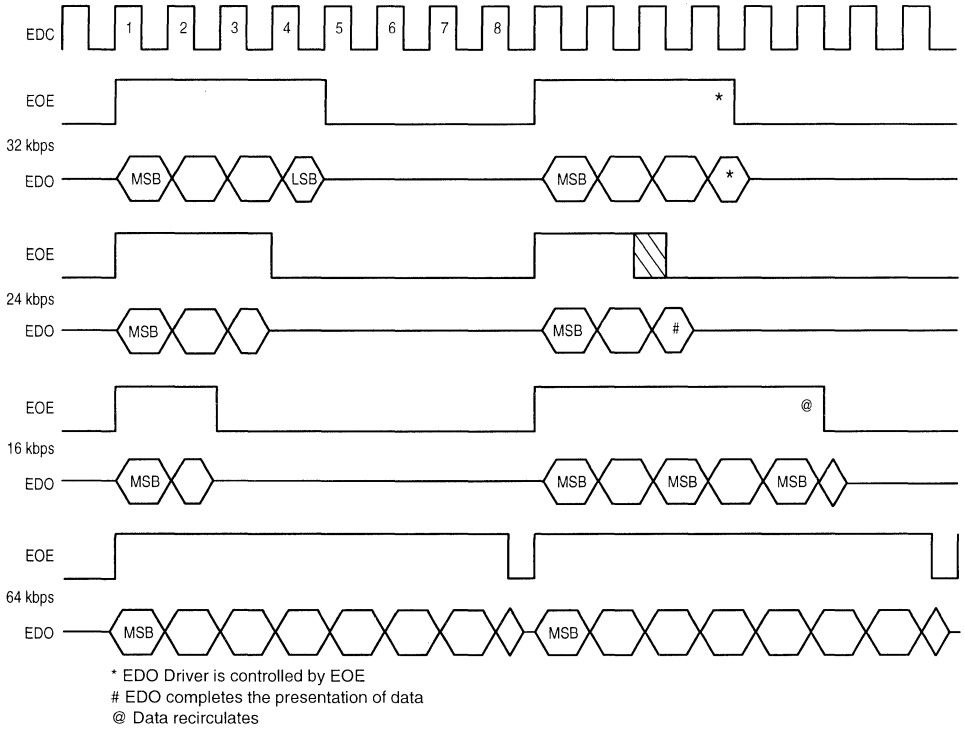


Figure 3. Encoder Output Timing — Short Frame

ENCODER OUTPUT — LONG FRAME (V_{DD} = 5.0 V, T_A = – 40 to + 85°C)

Parameter	Symbol	Min	Max	Unit
Enable Low Hold Time	$t_{h(EOE)L}$	30	—	ns
Enable Valid Time	$t_{v(EOE)}$	15	—	ns
Enable to Data Time (Whichever Edge Occurs Last)	$t_{EOE-EDO}$	—	40	ns
Clock to Data Time (Whichever Edge Occurs Last)	$t_{EDC-EDO}$	—	45	ns



* EDO Driver is controlled by EOE
\# EDO completes the presentation of data
@ Data recirculates

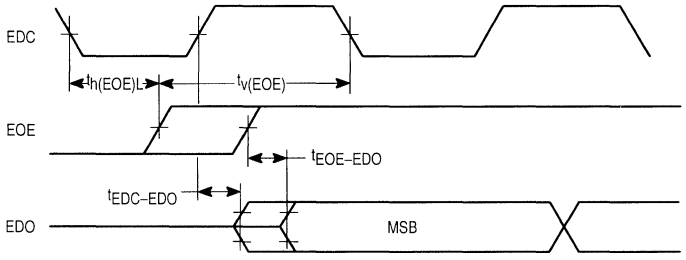


Figure 4. Encoder Output Timing — Long Frame

DECODER INPUT — SHORT FRAME (V_{DD} = 5.0 V, T_A = – 40 to + 85°C)

Parameter	Symbol	Min	Max	Unit
Enable Low Setup Time to Falling DDC	$t_{su(DIE)L}$	15	—	ns
Enable Low Hold Time from Falling DDC	$t_{h(DIE)H}$	30	—	ns
Enable Valid Time to Falling DDC	$t_{v(DIE)}$	15	—	ns
Enable Hold Time from Falling DDC	$t_{h(DIE)}$	15	—	ns
Data Valid Time Before Falling DDC	$t_{v(DDI)}$	15	—	ns
Data Hold Time from Falling DDC	$t_{h(DDI)}$	15	—	ns

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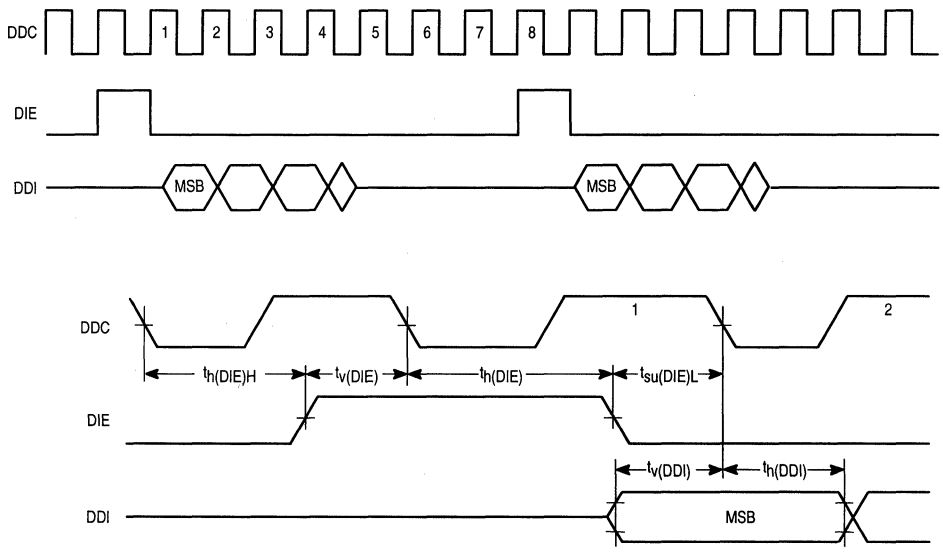


Figure 5. Decoder Input Timing — Short Frame

DECODER INPUT — LONG FRAME (V_{DD} = 5.0 V, T_A = – 40 to + 85°C)

Parameter	Symbol	Min	Max	Unit
Enable Hold Time from Falling DDC	$t_{h(DIE)}$	30	—	ns
Enable Valid Time to Falling DDC	$t_{v(DIE)}$	15	—	ns
Data Valid Time to Falling DDC	$t_{v(DDI)}$	15	—	ns
Data Hold Time from Falling DDC	$t_{h(DDI)}$	15	—	ns

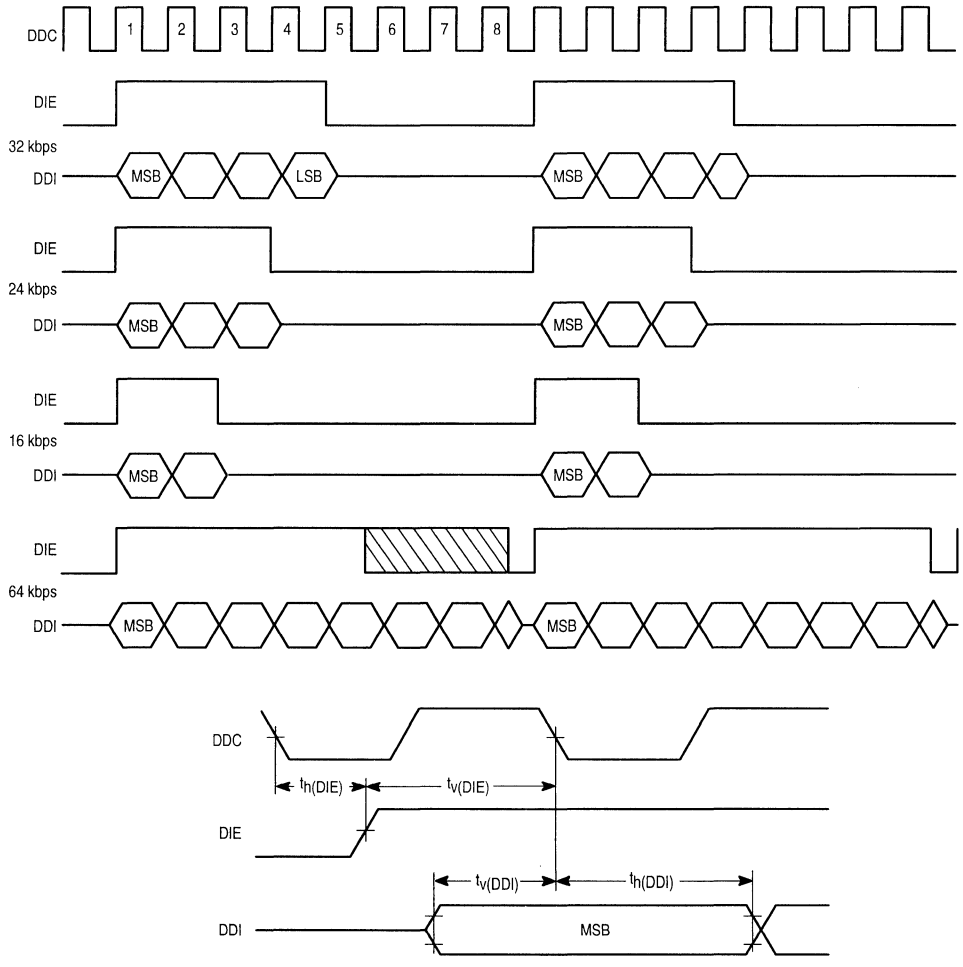


Figure 6. Decoder Input Timing — Long Frame

DECODER OUTPUT — SHORT FRAME (V_{DD} = 5.0 V, T_A = – 40 to + 85°C)

Parameter	Symbol	Min	Max	Unit
Enable Low Hold Time	$t_{h(DOE)L}$	30	—	ns
Enable Valid Time	$t_{v(DOE)}$	15	—	ns
Enable Hold Time	$t_{h(DOE)}$	15	—	ns
Rising Edge of DDC to Valid DDO	$t_{v(DDO)}$	—	40	ns
Delay Time from 8th DDC Low to DDO Output Disabled	$t_{z(DDO)}$	—	30	ns

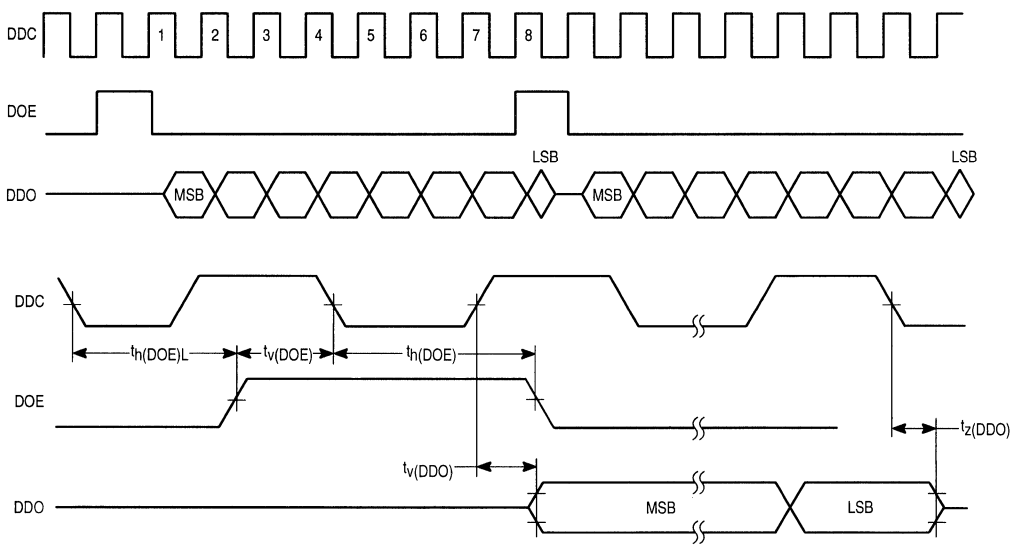


Figure 7. Decoder Output Timing — Short Frame

DECODER OUTPUT — LONG FRAME (V_{DD} = 5.0 V, T_A = – 40 to + 85°C)

Parameter	Symbol	Min	Max	Unit
Enable Low Hold Time	$t_{h(DOE)L}$	30	—	ns
Enable Valid Time	$t_{v(DOE)}$	15	—	ns
Rising Edge of DDE to Valid DDO (When DDC is High)	$t_{DOE-DDO}$	—	40	ns
Rising Edge of DDC to Valid DDO (When DOE is High)	$t_{DDC-DDO}$	—	45	ns
Delay Time from 8th DDC Low or DOE Low to DDO Output Disabled	$t_{z(DDO)}$	0	30	ns

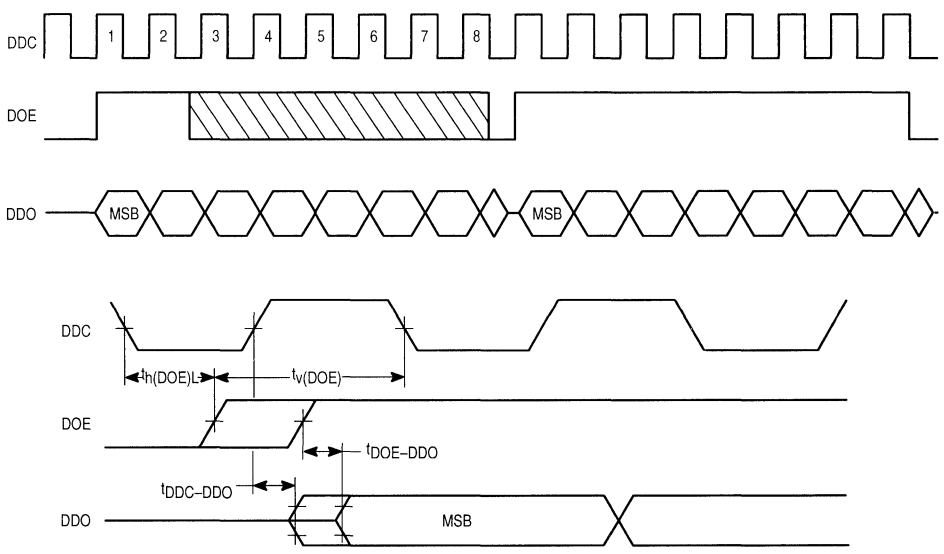


Figure 8. Decoder Output Timing — Long Frame

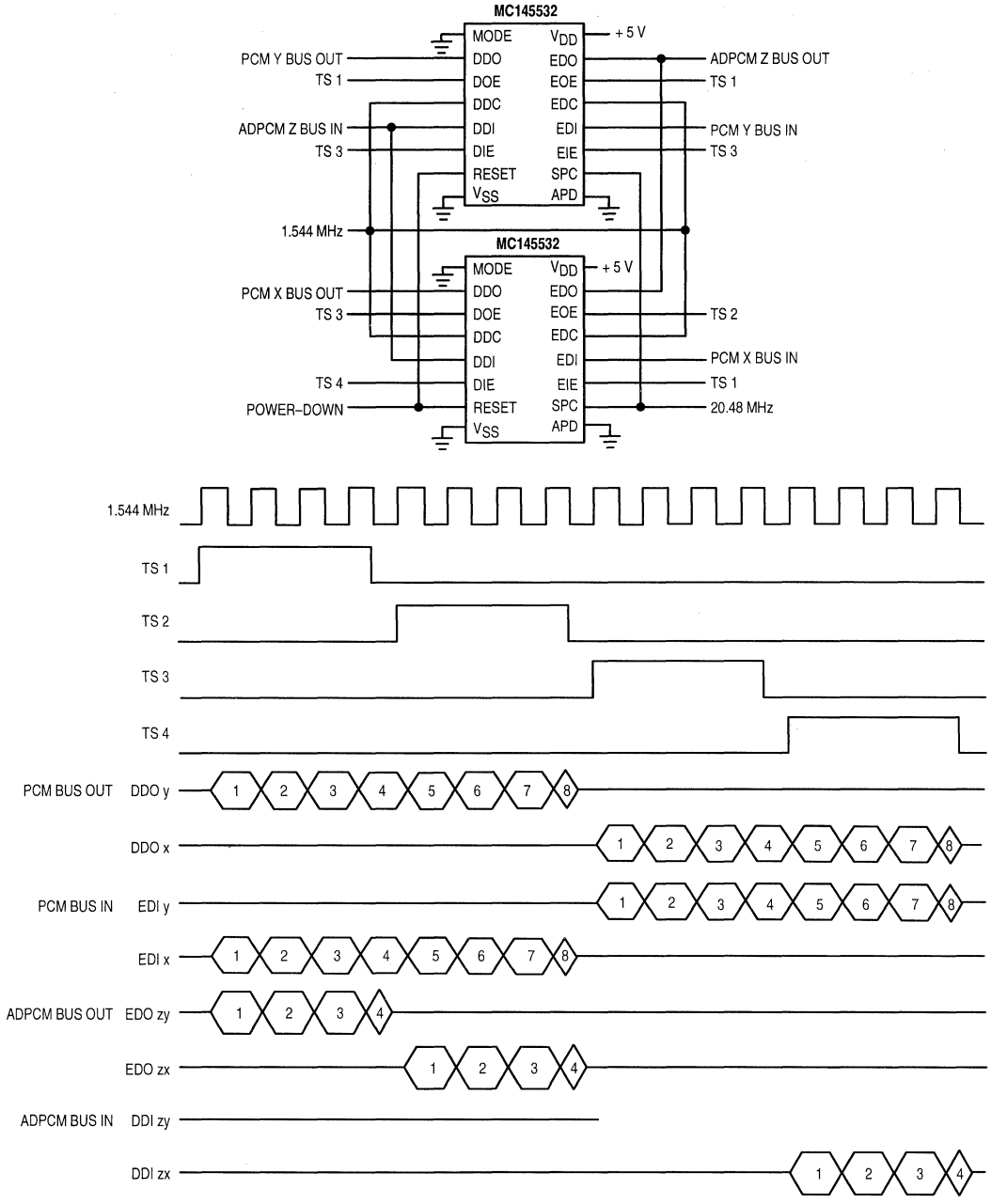


Figure 9. ADPCM Transcoder Application

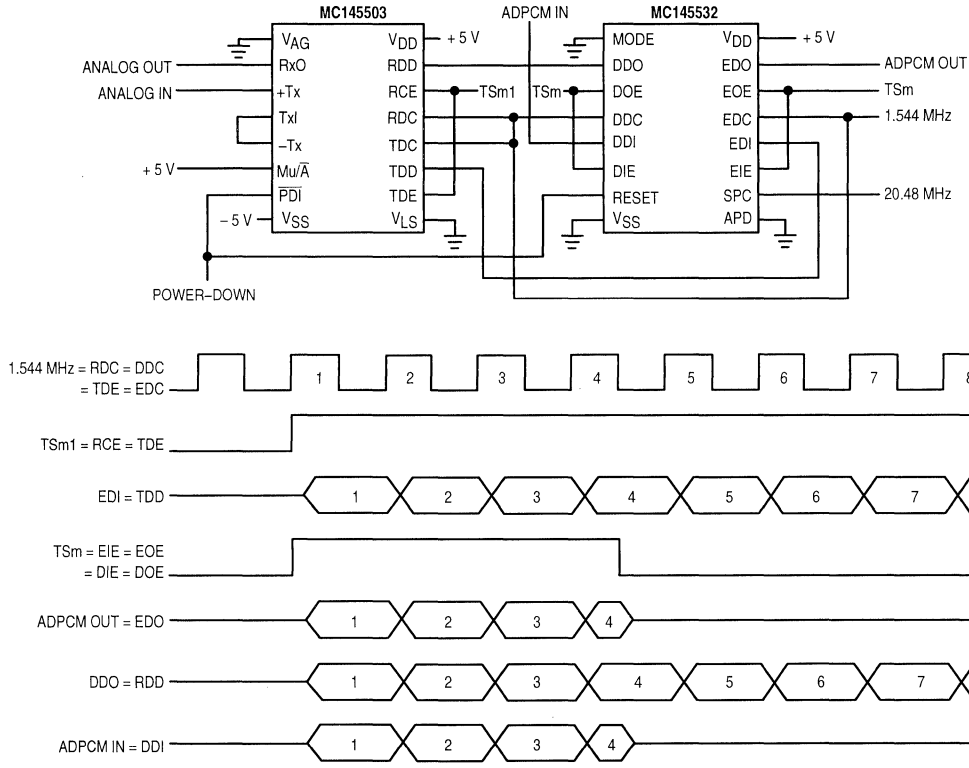
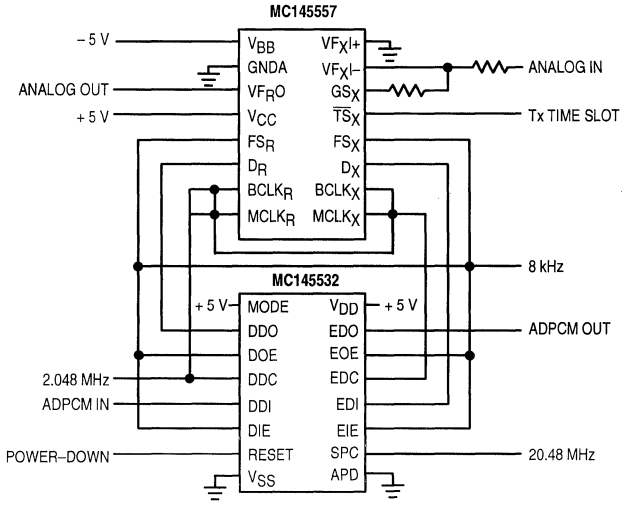


Figure 10. ADPCM Transcoder/Codec Application



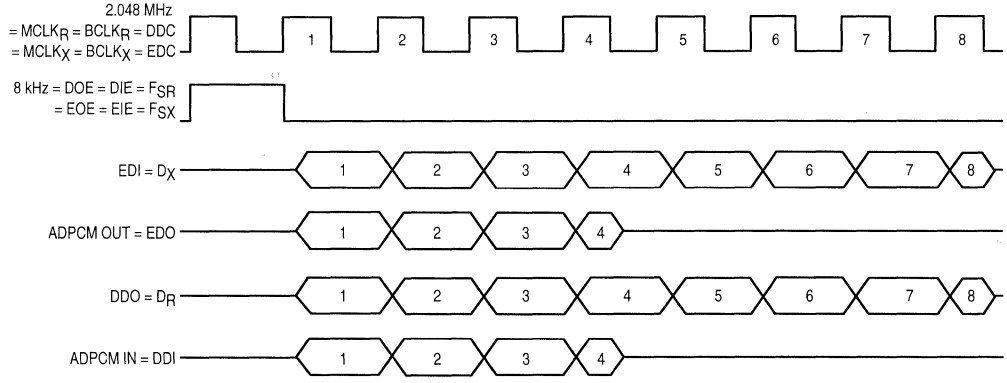


Figure 11. ADPCM Transcoder/Codec Application (A–Law)

MC145540

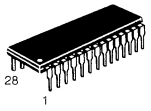
Technical Summary
ADPCM Codec

This technical summary provides a brief description of the MC145540 ADPCM Codec. A complete data book for the MC145540 is available and can be ordered from your local Motorola sales office. The data book number is MC145540/D.

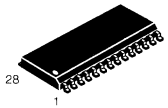
The MC145540 ADPCM Codec is a single chip implementation of a PCM Codec–Filter and an ADPCM encoder/decoder, and therefore provides an efficient solution for applications requiring the digitization and compression of voiceband signals. This device is designed to operate over a wide voltage range, 2.7 to 5.25 V and, as such, is ideal for battery powered as well as ac powered applications. The MC145540 ADPCM Codec also includes a serial control port and internal control and status registers that permit a microcomputer to exercise many built–in features.

The ADPCM Codec is designed to meet the 32 kbps ADPCM conformance requirements of CCITT Recommendation G.721–1988 and ANSI T1.301. It also meets ANSI T1.303 and CCITT Recommendation G.723–1988 for 24 kbps ADPCM operation, and the 16 kbps ADPCM standard, CCITT Recommendation G.726. This device also meets the PCM conformance specification of the CCITT G.714 Recommendation.

- Single 2.7 to 5.25 V Power Supply
- Typical 2.3 V Power Dissipation of 43 mW, Power–Down of 15 μW
- Differential Analog Circuit Design for Lowest Noise
- Complete Mu–Law and A–Law Companding PCM Codec–Filter
- ADPCM Transcoder for 64, 32, 24, and 16 kbps Data Rates
- Universal Programmable Dual Tone Generator
- Programmable Transmit Gain, Receive Gain, and Sidetone Gain
- Low Noise, High Gain, Three Terminal Input Operational Amplifier for Microphone Interface
- Push–Pull, 300 Ω Power Drivers with External Gain Adjust for Receiver Interface
- Push–Pull, 300 Ω Auxiliary Output Drivers for Ringer Interface
- Voltage Regulated Charge Pump to Power the Analog Circuitry in Low Voltage Applications
- Receive Noise Burst Detect Algorithm
- Order Complete Document as MC145540/D
- Device Supported by MC145537EVK ADPCM Codec Evaluation Kit



P SUFFIX
PLASTIC DIP
CASE 710

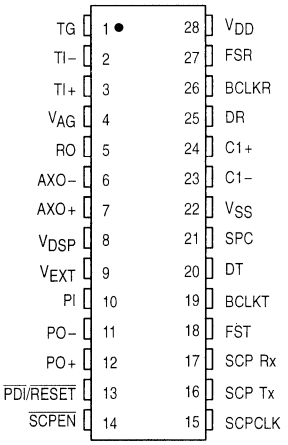


DW SUFFIX
SOG PACKAGE
CASE 751F

ORDERING INFORMATION

MC145540P	Plastic DIP
MC145540DW	SOG Package

PIN ASSIGNMENT



MC14LC5540

2

Technical Summary
ADPCM Codec

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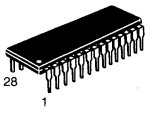
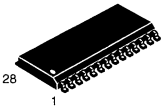
- Single 2.7 to 5.25 V Power Supply
- Typical 2.3 V Power Dissipation of 43 mW, Power–Down of 15 μW
- Differential Analog Circuit Design for Lowest Noise
- Complete Mu–Law and A–Law Companding PCM Codec–Filter
- ADPCM Transcoder for 64, 32, 24, and 16 kbps Data Rates
- Universal Programmable Dual Tone Generator
- Programmable Transmit Gain, Receive Gain, and Sidetone Gain
- Low Noise, High Gain, Three Terminal Input Operational Amplifier for Microphone Interface
- Push–Pull, 300 Ω Power Drivers with External Gain Adjust for Receiver Interface
- Push–Pull, 300 Ω Auxiliary Output Drivers for Ringer Interface
- Voltage Regulated Charge Pump to Power the Analog Circuitry in Low Voltage Applications
- Receive Noise Burst Detect Algorithm
- Order Complete Document as MC145540/D
- Device Supported by MC145537EVK ADPCM Codec Evaluation Kit



P SUFFIX
PLASTIC DIP
CASE 710

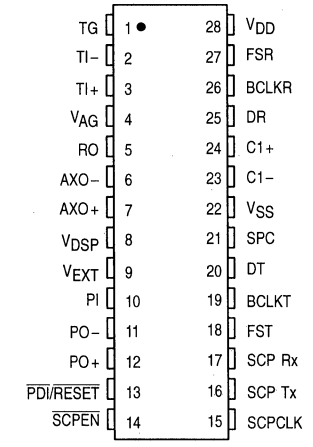


DW SUFFIX
SOG PACKAGE
CASE 751F

ORDERING INFORMATION

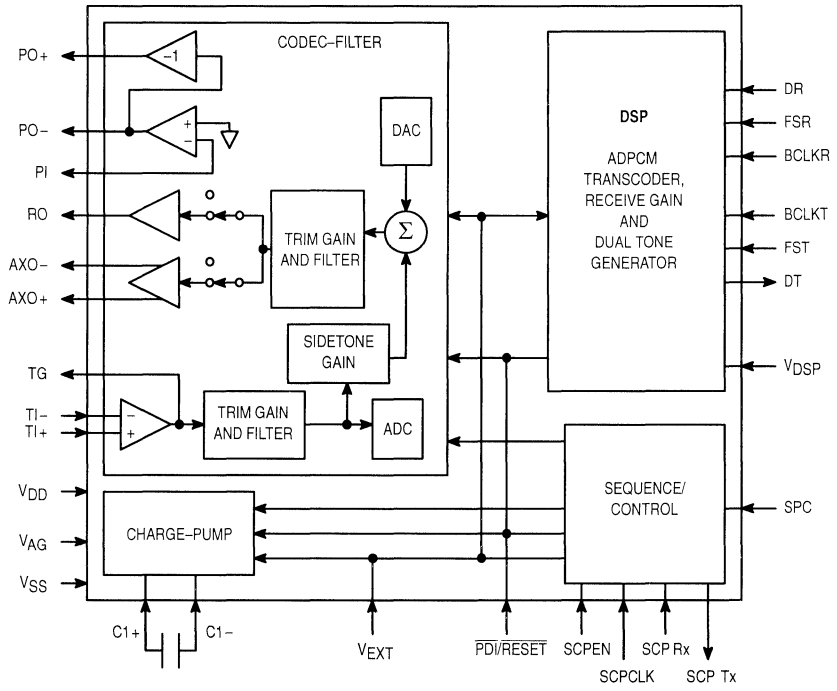
MC14LC5540P	Plastic DIP
MC14LC5540DW	SOG Package

PIN ASSIGNMENT



REV 1
9/95

BLOCK DIAGRAM



PIN DESCRIPTIONS

Power Supply Pins

V_{SS}
Negative Power Supply (Pin 22)

This is the most negative power supply and is typically connected to 0 V.

V_{EXT}
External Power Supply Input (Pin 9)

This power supply input pin must be between 2.70 and 5.25 V. Internally, it is connected to the input of the V_{DSP} voltage regulator, the 5 V regulated charge pump, and all digital I/O including the Serial Control Port and the ADPCM Serial Data Port. This pin is also connected to the analog output drivers (PO+, PO–, AXO+, and AXO–). This pin should be decoupled to V_{SS} with a 0.1 μF ceramic capacitor. This pin is internally connected to the V_{DD} and V_{DSP} pins when the device is powered down.

V_{DSP}
Digital Signal Processor Power Supply Output (Pin 8)

This pin is connected to the output of the on–chip V_{DSP} voltage regulator which supplies the positive voltage to the DSP circuitry and to the other digital blocks of the ADPCM Codec. This pin should be decoupled to V_{SS} with a 0.1 μF ceramic capacitor. This pin cannot be used for powering external loads. This pin is internally connected to the V_{EXT} pin during power–down to retain memory.

V_{DD}
Positive Power Supply Input/Output (Pin 28)

This is the positive output of the on–chip voltage regulated charge pump and the positive power supply input to the analog sections of the device. Depending on the supply voltage available, this pin can function in one of two different operating modes:

1. When V_{EXT} is supplied from a regulated 5 V (± 5%) power supply, V_{DD} is an input and should be externally connected to V_{EXT}. Charge pump capacitor C1 should not be used and the charge pump should be disabled in BR0(b2). In this case V_{EXT} and V_{DD} can share the same 0.1 μF ceramic decoupling capacitor to V_{SS}.
2. When V_{EXT} is supplied from 2.70 to 5.25 V, such as battery powered applications, the charge pump should be used. In this case, V_{DD} is the output of the on–chip voltage regulated charge pump and must **not** be connected to V_{EXT}. V_{DD} should be decoupled to V_{SS} with a 1.0 μF ceramic capacitor. This pin cannot be used for powering external loads in this operating mode. This pin is internally connected to the V_{EXT} pin when the charge pump is turned off or the device is powered down.

V_{AG}
Analog Ground Output (Pin 4)

This output pin provides a mid–supply analog ground regulated to 2.4 V. All analog signal processing within this device

is referenced to this pin. This pin should be decoupled to V_{SS} with a 0.01 to 0.1 μF ceramic capacitor. If the audio signals to be processed are referenced to V_{SS}, then special precautions must be utilized to avoid noise between V_{SS} and the V_{AG} pin. Refer to the applications information in this document for more information. The V_{AG} pin becomes high impedance when in analog power–down mode.

C1–, C1+
Charge Pump Capacitor Pins (Pin 23 And 24)

These are the capacitor connections to the internal voltage regulated charge pump that generates the V_{DD} supply voltage. A 0.1 μF capacitor should be placed between these pins. Note that if an external V_{DD} is supplied, this capacitor should not be in the circuit.

2

ANALOG INTERFACE PINS

TG
Transmit Gain (Pin 1)

This is the output of the transmit gain setting operational amplifier and the input to the transmit band–pass filter. This op amp is capable of driving a 2 kΩ load to the V_{AG} pin. When TI– and TI+ are connected to V_{DD}, the TG op amp is powered down and the TG pin becomes a high–impedance input to the transmit filter. All signals at this pin are referenced to the V_{AG} pin. This pin is high impedance when the device is in the analog power–down mode. This op amp is powered by the V_{DD} pin.

TI–
Transmit Analog Input (Inverting) (Pin 2)

This is the inverting input of the transmit gain setting operational amplifier. Gain setting resistors are usually connected from this pin to TG and from this pin to the analog signal source. The common mode range of the TI+ and TI– pins is from 1.0 V, to V_{DD} – 2 V. Connecting this pin and TI+ (Pin 3) to V_{DD} will place this amplifier's output (TG) in a high–impedance state, thus allowing the TG pin to serve as a high–impedance input to the transmit filter.

TI+
Transmit Analog Input (Non–Inverting) (Pin 3)

This is the non–inverting input of the transmit input gain setting operational amplifier. This pin accommodates a differential to single–ended circuit for the input gain setting op amp. This allows input signals that are referenced to the V_{SS} pin to be level shifted to the V_{AG} pin with minimum noise. This pin may be connected to the V_{AG} pin for an inverting amplifier configuration if the input signal is already referenced to the V_{AG} pin. The common mode range of the TI+ and TI– pins is from 1.0 V to V_{DD} – 2 V. Connecting this pin and TI– (Pin 2) to V_{DD} will place this amplifier's output (TG) in a high–impedance state, thus allowing the TG pin to serve as a high–impedance input to the transmit filter.

RO
Receive Analog Output (Pin 5)

This is the non–inverting output of the receive smoothing filter from the digital–to–analog converter. This output is capable of driving a 2 kΩ load to 1.575 V peak referenced to the V_{AG} pin. This pin may be dc referenced to either the V_{AG} pin or a voltage of half of V_{EXT} by BR2 (b7). This pin is high impedance when the device is in the analog power–down mode. This pin is high impedance except when it is enabled for analog signal output.

AXO–
Auxiliary Audio Power Output (Inverting) (Pin 6)

This is the inverting output of the auxiliary power output drivers. The Auxiliary Power Driver is capable of differentially driving a 300 Ω load. This power amplifier is powered from V_{EXT} and its output can swing to within 0.5 V of V_{SS} and V_{EXT}. This pin may be dc referenced to either the V_{AG} pin or a voltage of half of V_{EXT} by BR2 (b7). This pin is high impedance in power down. This pin is high impedance except when it is enabled for analog signal output.

AXO+
Auxiliary Audio Power Output (Non–Inverting) (Pin 7)

This is the non–inverting output of the auxiliary power output drivers. The Auxiliary Power Driver is capable of differentially driving a 300 Ω load. This power amplifier is powered from V_{EXT} and its output can swing to within 0.5 V of V_{SS} and V_{EXT}. This pin may be dc referenced to either the V_{AG} pin or a voltage of half of V_{EXT} by BR2 (b7). This pin is high impedance in power down. This pin is high impedance except when it is enabled for analog signal output.

PI
Power Amplifier Input (Pin 10)

This is the inverting input to the PO– amplifier. The non–inverting input to the PO– amplifier may be dc referenced to either the V_{AG} pin or a voltage of half of V_{EXT} by BR2 (b7). The PI and PO– pins are used with external resistors in an inverting op amp gain circuit to set the gain of the PO+ and PO– push–pull power amplifier outputs. Connecting PI to V_{DD} will power down these amplifiers and the PO+ and PO– outputs will be high impedance.

PO–
Power Amplifier Output (Inverting) (Pin 11)

This is the inverting power amplifier output that is used to provide a feedback signal to the PI pin to set the gain of the push–pull power amplifier outputs. This power amplifier is powered from V_{EXT} and its output can swing to within 0.5 V of V_{SS} and V_{EXT}. This should be noted when setting the gain of this amplifier. This pin is capable of driving a 300 Ω load to PO+ independent of supply voltage. The PO+ and PO– outputs are differential (push–pull) and capable of driving a 300 Ω load to 3.15 V peak, which is 6.3 V peak–to–peak when a nominal 5 V power supply is used for V_{EXT}. The bias voltage and signal reference for this pin may be dc referenced to either the V_{AG} pin or a voltage of half of V_{EXT} by BR2 (b7). Low impedance loads must be between PO+ and PO–. This pin is high impedance when the device is in the analog power–down mode. This pin is high impedance except when it is enabled for analog signal output.

PO+
Power Amplifier Output (Non–Inverting) (Pin 12)

This is the non–inverting power amplifier output that is an inverted version of the signal at PO–. This power amplifier is powered from V_{EXT} and its output can swing to within 0.5 V of V_{SS} and V_{EXT}. This pin is capable of driving a 300 Ω load to PO–. This pin may be dc referenced to either the V_{AG} pin or a voltage of half of V_{EXT} by BR2 (b7). This pin is high

impedance when the device is in the analog power–down mode. See **PI** and **PO–** for more information. This pin is high impedance except when it is enabled for analog signal output.

ADPCM/PCM SERIAL INTERFACE PINS

FST
Frame Sync, Transmit (Pin 18)

When used in the Long Frame Sync or Short Frame Sync mode, this pin accepts an 8 kHz clock that synchronizes the output of the serial ADPCM data at the DT pin.

BCLKT
Bit Clock, Transmit (Pin 19)

When used in the Long Frame Sync or Short Frame Sync mode, this pin accepts any bit clock frequency from 64 to 5120 kHz.

DT
Data, Transmit (Pin 20)

This pin is controlled by FST and BCLKT and is high impedance except when outputting data.

SPC
Signal Processor Clock (Pin 21)

This input requires a 20.48 or 20.736 MHz clock signal that is used as the DSP engine master clock. Internally the device divides down this clock to generate the 256 kHz clock required by the PCM Codec. (This clock may be optionally specified for higher frequencies; contact the factory for more information.)

DR
Data, Receive (Pin 25)

ADPCM data to be decoded are applied to this input, which operates synchronously with FSR and BCLKR to enter the data in a serial format.

BCLKR
Bit Clock, Receive (Pin 26)

When used in the Long Frame Sync or Short Frame Sync mode, this pin accepts any bit clock frequency from 64 to 5120 kHz. This pin may be used for applying an external 256 kHz clock for sequencing the analog signal processing functions of this device. This is selected by the SCP port at BR0 (b7).

FSR
Frame Sync, Receive (Pin 27)

When used in the Long Frame Sync or Short Frame Sync mode, this pin accepts an 8 kHz clock that synchronizes the input of the serial ADPCM data at the DR pin. FSR can operate asynchronous to FST in the Long Frame Sync or Short Frame Sync mode.

SERIAL CONTROL PORT INTERFACE PINS

$\overline{\text{PDI/RESET}}$
Power–Down Input/Reset (Pin 13)

A logic 0 applied to this input forces the device into a low–power dissipation mode. A rising edge on this pin causes power to be restored and the ADPCM Reset state (specified in the standards) to be forced.

$\overline{\text{SCPEN}}$
Serial Control Port Enable Input (Pin 14)

This pin, when held low, selects the Serial Control Port (SCP) for the transfer of control and status information into and out of the MC14LC5540 ADPCM Codec. This pin should be held low for a total of 16 periods of the SCPCLK signal in order for information to be transferred into or out of the MC14LC5540 ADPCM Codec. The timing relationship between $\overline{\text{SCPEN}}$ and SCPCLK is shown in Figures 6 through 9.

SCPCLK
Serial Control Port Clock Input (Pin 15)

This input to the device is used for controlling the rate of transfer of data into and out of the SCP Interface. Data are clocked into the MC14LC5540 ADPCM Codec from SCP Rx on rising edges of SCPCLK. Data are shifted out of the device on SCP Tx on falling edges of SCPCLK. SCPCLK can be any frequency from 0 to 4.096 MHz. An SCP transaction takes place when $\overline{\text{SCPEN}}$ is brought low. Note that SCPCLK is ignored when $\overline{\text{SCPEN}}$ is high (i.e., it may be continuous or it can operate in a burst mode).

SCP Tx
Serial Control Port Transmit Output (Pin 16)

SCP Tx is used to output control and status information from the MC14LC5540 ADPCM Codec. Data are shifted out of SCP Tx on the falling edges of SCPCLK, most significant bit first.

SCP Rx
Serial Control Port Receive Input (Pin 17)

SCP Rx is used to input control and status information to the MC14LC5540 ADPCM Codec. Data are shifted into the device on rising edges of SCPCLK. SCP Rx is ignored when data are being shifted out of SCP Tx or when $\overline{\text{SCPEN}}$ is high.

ADPCM/PCM SERIAL INTERFACE TIMING DIAGRAMS

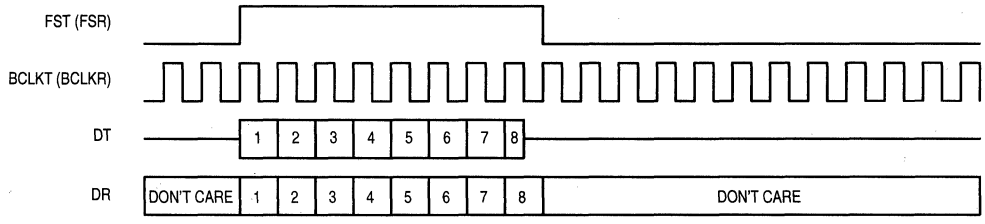


Figure 1. Long Frame Sync (64 kbps PCM Data Timing)

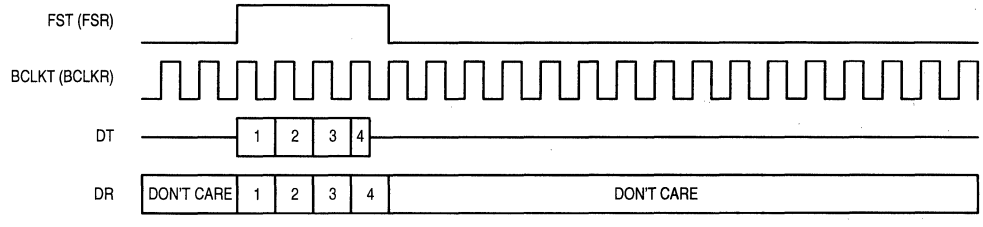


Figure 2. Long Frame Sync (32 kbps ADPCM Data Timing)

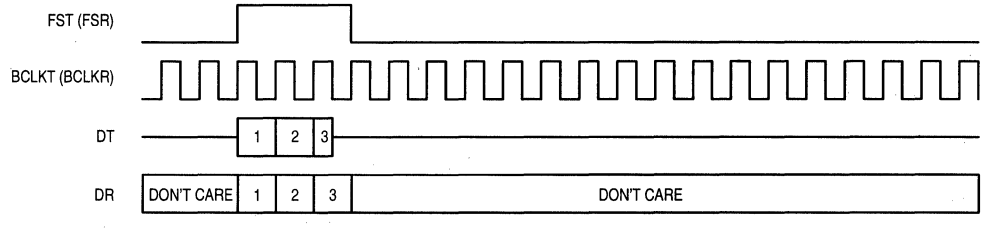


Figure 3. Long Frame Sync (24 kbps ADPCM Data Timing)

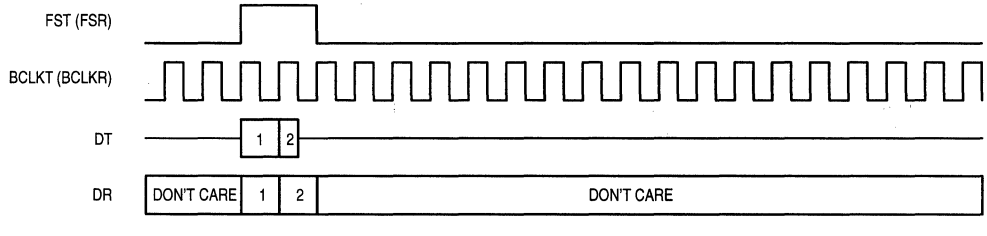


Figure 4. Long Frame Sync (16 kbps ADPCM Data Timing)

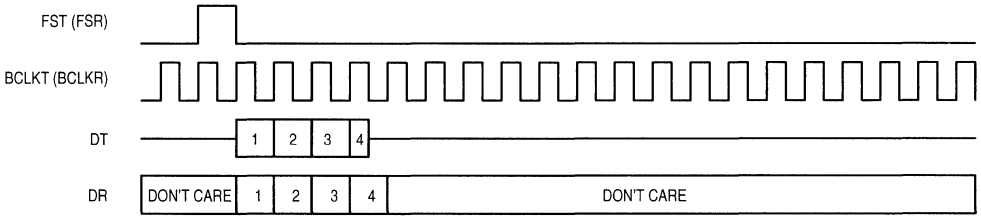


Figure 5. Short Frame Sync (32 kbps ADPCM Data Timing)

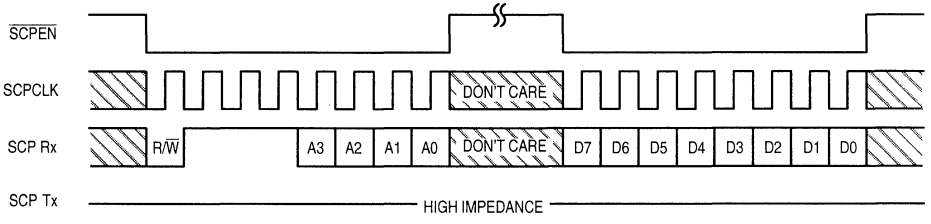


Figure 6. SCP Byte Register Write Operation Using Double 8–Bit Transfer

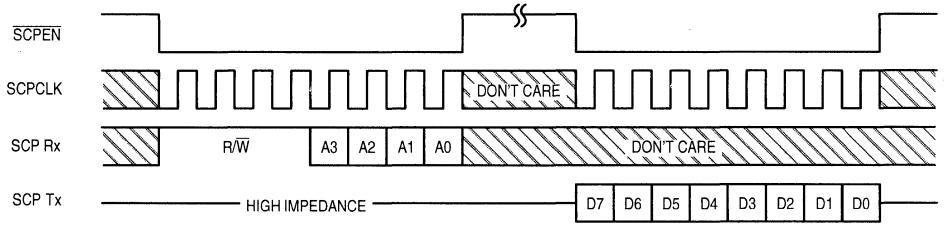


Figure 7. SCP Byte Register Read Operation Using Double 8–Bit Transfer

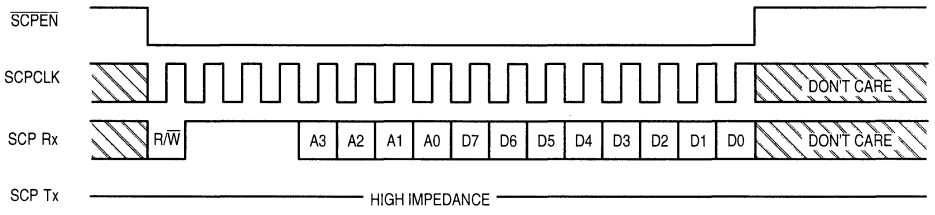


Figure 8. SCP Byte Register Write Operation Using Single 16–Bit Transfer

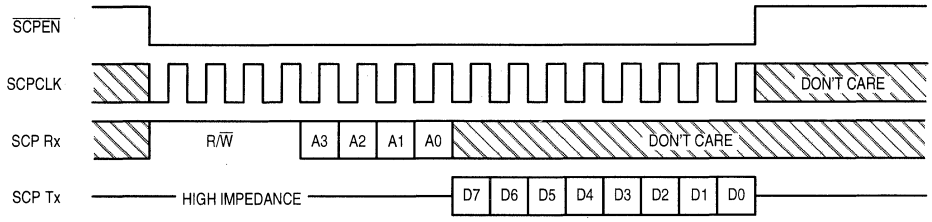


Figure 9. SCP Byte Register Read Operation Using Single 16–Bit Transfer

2

SERIAL CONTROL PORT (SCP) INTERFACE

The MC14LC5540 is equipped with an industry standard Serial Control Port (SCP) Interface. The SCP is used by an external controller, such as an M68HC05 family microcontroller, to communicate with the MC14LC5540 ADPCM Codec.

The SCP is a full–duplex, four–wire interface used to pass control and status information to and from the ADPCM Codec. The SCP Interface consists of a transmit output, a receive input, a data clock, and an enable signal. These device pins are known as SCP Tx, SCP Rx, SCPCLK, and $\overline{\text{SCPEN}}$, respectively. The SCPCLK determines the rate of exchange of data in both the transmit and receive directions, and the $\overline{\text{SCPEN}}$ signal governs when this exchange is to take place.

The operation and configuration of the ADPCM Codec is controlled by setting the state of the control and status registers within the MC14LC5540 and then monitoring these control and status registers. The control and status registers reside in sixteen 8–bit wide Byte Registers, BR0 – BR15. A complete register map can be found in the **Serial Control Port Registers** section.

BYTE REGISTER OPERATIONS

The sixteen byte registers are addressed by addressing a four–bit byte register address (A3:A0) as shown in Figures 6 and 7. A second 8–bit operation transfers the data word (D7:D0). Alternatively, these registers can be accessed with a single 16–bit operation as shown in Figures 8 and 9.

ADPCM CODEC DEVICE DESCRIPTION

The MC14LC5540 is a single channel Mu–Law or A–Law companding PCM Codec–Filter with an ADPCM encoder/decoder operating on a single voltage power supply from 2.7 to 5.25 V.

The MC14LC5540 ADPCM Codec is a complete solution for digitizing and reconstructing voice in compliance with CCITT G.714, G.721–1988, G.723–1988, G.726, and ANSI T1.301 and T1.303 for 64, 32, 24, and 16 kbps. This device satisfies the need for high–quality, low–power, low data rate voice transmission, and storage applications and is offered in 28–pin Plastic DIP and SOG packages.

Referring to Figure 10, the main functional blocks of the MC14LC5540 are the switched capacitor technology PCM Codec–Filter, the DSP based ADPCM encoder/decoder, and the voltage regulated charge pump. As an introduction to the functionality of the ADPCM Codec, a basic description of these functional blocks follows.

PCM CODEC–FILTER BLOCK DESCRIPTION

A PCM Codec–Filter is a device used for digitizing and reconstructing the human voice. These devices were developed primarily for the telephone network to facilitate voice switching and transmission. Once the voice is digitized, it may be switched by digital switching methods or transmitted long distance (T1, microwave, fiber optics, satellites, etc.) without degradation. The name codec is an acronym from "COder" for the analog–to–digital converter (ADC) used to digitize voice, and "DECoder" for the digital–to–analog converter (DAC) used for reconstructing voice. A codec is a single device that does both the ADC and DAC conversions.

To digitize voice intelligibly requires a signal to distortion of about 30 dB for a dynamic range of about 40 dB. This may be accomplished with a linear 13–bit ADC and DAC, but will far exceed the required signal to distortion at amplitudes greater than 40 dB below the peak amplitude. This excess performance is at the expense of bits of data per sample. Two methods of data reduction are implemented by compressing the 13–bit linear scheme to companded 8–bit schemes. These companding schemes follow a segmented or "piecewise–linear" curve formatted as sign bit, three chord bits, and four step bits. For a given chord, all 16 of the steps have the same voltage weighting. As the voltage of the analog input increases, the four step bits increment and carry to the three chord bits, which increment. When the chord bits increment, the step bits double their voltage weighting. This results in an effective resolution of six bits (sign + chord + four step bits) across a 42 dB dynamic range (seven chords above 0, by 6 dB per chord). There are two companding schemes used: Mu–255 Law specifically in North America and A–Law specifically in Europe. These companding schemes are accepted world wide.

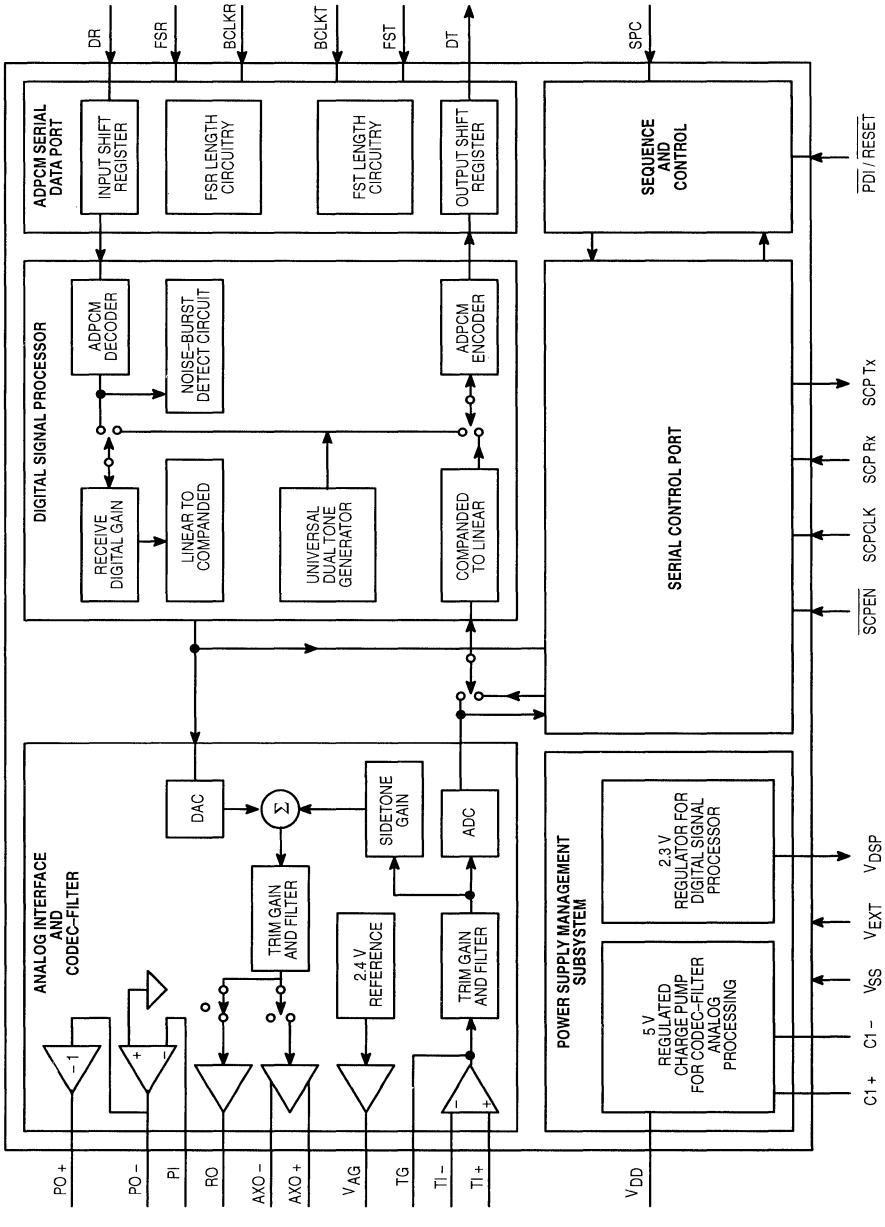


Figure 10. ADPCM Codec Block Diagram

In a sampling environment, Nyquist theory says that to properly sample a continuous signal, it must be sampled at a frequency higher than twice the signal's highest frequency component. Voice contains spectral energy above 3 kHz, but its absence is not detrimental to intelligibility. To reduce the digital data rate, which is proportional to the sampling rate, a sample rate of 8 kHz was adopted, consistent with a bandwidth of 3 kHz. This sampling requires a low–pass filter to limit the high frequency energy above 3 kHz from distorting the inband signal. The telephone line is also subject to 50/60 Hz power line coupling, which must be attenuated from the signal by a high–pass filter before the analog–to–digital converter.

2

The digital–to–analog conversion process reconstructs a staircase version of the desired inband signal which has spectral images of the inband signal modulated about the sample frequency and its harmonics. These spectral images are called aliasing components which need to be attenuated to obtain the desired signal. The low–pass filter used to attenuate these aliasing components is typically called a reconstruction or smoothing filter.

The MC14LC5540 ADPCM Codec incorporates this codec function as one of its main functional blocks.

ADPCM TRANSCODER BLOCK DESCRIPTION

An Adaptive Differential PCM (ADPCM) transcoder is used to reduce the data rate required to transmit a PCM encoded voice signal while maintaining the voice fidelity and intelligibility of the PCM signal.

The ADPCM transcoder is used on both Mu–Law and A–Law 64 kbps data streams which represent either voice or voice band data signals that have been digitized by a PCM Codec–Filter. The PCM to ADPCM encoder section of this transcoder has a type of linear predicting digital filter which is trying to predict the next PCM sample based on the previous history of the PCM samples. The ADPCM to PCM decoder section implements an identical linear predicting digital filter. The error or difference between the predicted and the true PCM input value is the information that is sent from the encoder to the decoder as an ADPCM word. The characteristics of this ADPCM word include the number of quantized steps (this determines the number of bits per ADPCM word) and the actual meaning of this word is a function of the predictor's output value, the error signal and the statistics of the history of PCM words. The term "adaptive" applies to the transfer function of the filter that generates the ADPCM word which adapts to the statistics of the signals presented to it. This means that an ADPCM word "3" does not have the same absolute error voltage weighting for the analog signal when the channel is quiet as it does when the channel is processing a speech signal. The ADPCM to PCM decoder section has a reciprocating filter function which interprets the ADPCM word for proper reconstruction of the PCM sample.

The adaptive characteristics of the ADPCM algorithm make it difficult to analyze and quantify the performance of the ADPCM code sequence. The 32 kbps algorithm was optimized for both voice and moderate speed modems ($\leq$ 4800 baud). This optimization includes that the algorithm supports the voice frequency band of 300 – 3400 Hz with minimal degradation for signal–to–distortion, gain–versus–level, idle channel noise, and other analog transmission performance. This algorithm has also been subjected to audibility testing with many languages for Mean Opinion Score (MOS) ratings and performed well when compared to 64 kbps PCM. The standards committees have specified multiple 16000 word test vectors for the encoder and for the decoder to verify compliance. To run these test vectors, the device must be initialized to the reference state by resetting the device.

In contrast to 64 kbps PCM, the ADPCM words appear as random bit activity on an oscilloscope display whether the audio channel is processing speech or a typical PCM idle channel with nominal bit activity. The ADPCM algorithm does not support dc signals with the exception of digital quiet, which will result in all ones in the ADPCM channel. All digital processing is performed on 13–bit linearizations of the 8–bit PCM companded words, whether the words are Mu–Law or A–Law. This allows an ADPCM channel to be intelligibly decoded into a Mu–Law PCM sequence or an A–Law PCM sequence irrespective of whether it was originally digitized as Mu–Law or A–Law. There will be additional quantizing degradation if the companding scheme is changed because the ADPCM algorithm is trying to reconstruct the original 13–bit linear codes, which included companding quantization.

CHARGE PUMP

The charge pump is the functional block that allows the analog signal processing circuitry of the MC14LC5540 to operate with a power supply voltage as low as 2.7 V. This analog signal processing circuitry includes the PCM Codec–Filter function, the transmit trim gain, the receive trim gain, the sidetone gain control, and the transmit input operational amplifier. This circuitry does not dissipate much current but it does require a nominal voltage of 5 V for the V_{DD} power supply.

The charge pump block is a regulated voltage doubler which takes twice the current it supplies from the voltage applied to the V_{EXT} power supply pin which may range from 2.7 to 5.25 V and generates the required 5 V V_{DD} supply. The charge pump block receives as inputs the V_{EXT} supply voltage, the same 256 kHz clock that sequences the analog signal processing circuitry, and the Charge Pump Enable signal from the SCP block. It also makes use of the capacitor connected to the C1+ and C1– pins and the decoupling capacitor connected to the V_{DD} pin.

FUNCTIONAL DESCRIPTION

POWER SUPPLY CONFIGURATION

Analog Signal Processing Power Supply

All analog signal processing is powered by the V_{DD} pin at 5 V. This voltage may be applied directly to the V_{DD} pin or 5 V may be obtained by the on–chip 5 V regulated charge pump which is powered from the V_{EXT} pin. The V_{EXT} pin is the main positive power supply pin for this device.

For applications that are not 5 V regulated, the on–chip 5 V regulated charge pump may be turned on and C1 will be required. V_{DD} will require a 1.0 μF decoupling capacitor to filter the voltage spikes of the charge pump. This allows the V_{EXT} power supply to be from 2.7 to 5.25 V. This mode of operation is intended for hand held applications where three NiCad cells or three dry cells would be the power supply.

The on–chip 5 V regulated charge pump is a single stage charge pump that effectively series regulates the amount of voltage it generates and internally applies this regulated voltage to the V_{DD} pin. This 5 V voltage is developed by

connecting the external 0.1 μF capacitor (C1) between the V_{EXT} power supply pin and the power supply ground pin, V_{SS}. This puts a charge of as much as 2.7 V on C1. The charge pump circuitry then connects the negative lead of C1 to the V_{EXT}, pin which sums the voltage of C1 with the voltage at V_{EXT} for a minimum potential voltage of 5.4 V. The charge voltage on C1 is regulated such that the summing of voltages is regulated to 5 V. This limits all of the voltages on the device to safe levels for this IC fabrication technology. This charge pumped voltage is then stored on the 1.0 μF capacitor connected at V_{DD} and V_{SS}, which filters and serves as a reservoir for power. The clock period for this charge pump is the same 256 kHz as the analog sequencing clock, minimizing noise problems.

For applications with a regulated 5 V (± 5%) power supply, the V_{DD} pin and the V_{EXT} pin are connected to the 5 V power supply. These pins may share one decoupling capacitor in this configuration as a function of external noise on the power supply. The on–chip, 5 V regulated charge pump should be turned off via the SCP port at register 0. The external capacitor (C1) should not be populated for these applications.

Digital Signal Processing Power Supply

This device has an on–chip series regulator which limits the voltage of the Digital Signal Processing (DSP) circuitry to about 2.3 V. This reduces the maximum power dissipation of this circuitry. From the V_{EXT} power supply pin, the DSP circuitry appears as a constant current load instead of a resistive ($CV^2/2$) load for a constant clock frequency. This series regulator is designed to have a low drop–out voltage, which allows the DSP circuitry to work when the V_{EXT} voltage is as low as 2.7 V. The output of this regulator is brought out to the V_{DSP} pin for a 0.1 μF decoupling capacitor. This regulator is not designed to power any loads external to the device.

ANALOG INTERFACE AND SIGNAL PATH

Transmit Analog

The transmit analog portion of this device includes a low–noise, three terminal operational amplifier capable of driving a 2 kΩ load. This op amp has inputs of TI+ and TI– and its output is TG. This op amp is intended to be configured in an inverting gain circuit. The analog signal may be applied directly to the TG pin if this transmit op amp is independently powered down. Power–down may be achieved by connecting both the TI+ and TI– inputs to the V_{DD} pin. The TG pin becomes high impedance when the transmit op amp is powered down. The TG pin is internally connected to a time continuous three–pole anti–aliasing pre–filter. This pre–filter incorporates a two–pole Butterworth active low–pass filter, followed by a single passive pole. This pre–filter is followed by a single–ended to differential converter that is clocked at 512 kHz. All subsequent analog processing utilizes fully differential circuitry. The output of the differential converter is followed by the transmit trim gain stage. This stage is intended to compensate for gain tolerances of external components such as microphones. The amount of gain control is 0–7 dB in 1 dB steps. This stage only accommodates positive gain because the maximum signal levels of the output of the input op amp are the same as the transmit filter and ADC, which should nominally be next to the clip levels of this device's circuitry. Any requirement for attenuation of the output of the input op amp would mean that it is being overdriven. The gain is programmed via the SCP port in BR1 (b2:b0). The next section is a fully–differential, 5–pole switched–capacitor low–pass filter with a 3.4 kHz frequency cutoff. After this filter is a 3–pole switched–capacitor high–pass filter having a cutoff frequency of about 200 Hz. This high–pass stage has a transmission zero at dc that eliminates any dc coming from the analog input or from accumulated op amp offsets in the preceding filter stages. (This high–pass filter may be removed from the signal path under control of the SCP port BR8 (b4).) The last stage of the high–pass filter is an autozeroed sample and hold amplifier.

One bandgap voltage reference generator and digital–to–analog converter (DAC) are shared by the transmit and receive sections. The autozeroed, switched–capacitor bandgap reference generates precise positive and negative reference voltages that are virtually independent of temperature and power supply voltage. A binary–weighted capacitor array (CDAC) forms the chords of the companding structure, while a resistor string (RDAC) implements the linear steps within each chord. The encode process uses the DAC, the voltage reference, and a frame–by–frame autozeroed comparator to implement a successive–approximation analog–to–digital conversion (ADC) algorithm. All of the analog circuitry involved in the data conversion (the voltage reference, RDAC, CDAC, and comparator) are implemented with a differential architecture.

The nonlinear companded Mu–Law transfer curve of the ADC may be changed to 8–bit linear by BR8 (b5).

The input to the ADC is normally connected to the output of the transmit filter section, but may be switched to measure the voltage at the V_{EXT} pin for battery voltage monitoring. This is selected by the I/O Mode in BR0 (b4:b3). In this mode, the ADC is programmed to output a linear 8–bit PCM word for the voltage at V_{EXT} which is intended to be read in BR9 (b7:b0). The data format for the ADC output is a "Don't Care" for the sign bit and seven magnitude bits. The scaling for the ADC is for 6.3 V at V_{EXT} equals full scale (BIN X111 1111). The ADPCM algorithm does not support dc signals.

Transmit Digital

The Digital Signal Processor (DSP) section of this device is a custom designed, interrupt driven, microcoded machine optimized for implementing the ADPCM algorithms. In the full–duplex speech mode, the DSP services one encode interrupt and one decode interrupt per frame (125 μs). The encode algorithm (i.e., 16 kbps, 24 kbps, or 32 kbps ADPCM, or 64 kbps PCM) is determined by the length of the transmit output enable at the FST pin. The length of the FST enable measured in transmit data clock (BCLKT) cycles tells the device which encoding rate to use. This enable length information is used by the encoder each frame. The transmit ADPCM word corresponding to this request will be computed during the next frame and will be available a total of two frames after being requested. This transmit enable length information can be delayed by the device an additional four frames corresponding to a total of six frames. These six frames of delay allow the device to be clocked with the same clocks for both transmit (encode) and receive (decode), and to be frame aligned for applications that require every sixth frame signaling. It is important to note that the enable length information is delayed and not the actual ADPCM (PCM) sample word. The amount of delay for the FST enable length

is controlled in BR7 (b5). If the FST enable goes low before the falling edge of BCLKT during the last bit of the ADPCM word, the digital data output circuitry counts BCLKT cycles to keep the data output (DT pin) low impedance for the duration of the ADPCM data word (2, 3, 4, or 8 BCLKT cycles) minus one half of a BCLKT cycle.

Receive Digital

The receive digital section of this device accepts serial ADPCM (PCM) words at the DR pin under the control of the BCLKR and FSR pins. The FSR enable duration, measured in BCLKR cycles, tells the device which decode algorithm (i.e., 16 kbps, 24 kbps, or 32 kbps ADPCM, or 64 kbps PCM) the DSP machine should use for the word that is being received at the DR pin. This algorithm may be changed on a frame by frame basis.

The DSP machine receives an interrupt when an ADPCM word has been received and is waiting to be decoded into a PCM word. The DSP machine performs a decode and an encode every frame when the device is operating in its full duplex conversation mode. The DSP machine decodes the ADPCM word according to CCITT G.726 for 32 kbps, 24 kbps, and 16 kbps. This decoding includes the correction for the CCITT/ANSI Sync function, except when the receive digital gain is used. The receive digital gain is anticipated to be user adjustable gain control in handset applications where as much as 12 dB of gain or more than 12 dB of attenuation may be desirable. The receive digital gain is a linear multiply performed on the 13–bit linear data before it is converted to Mu–Law or A–Law, and is programmed via the SCP port in BR3 (b7:b0). The decoded PCM word may be read via the SCP port in BR10 (b7:b0).

Receive Analog Signal Processing

The receive analog signal processing section includes the DAC described above, a sample and hold amplifier, a trim gain stage, a 5–pole, 3400 Hz switched capacitor low–pass filter with sinX/X correction, and a 2–pole active smoothing filter to reduce the spectral components of the switched capacitor filter. (The receive low–pass smoothing filter may be removed from the signal path for the additional spectral components for applications using the on–chip tone generator function described below. This low–pass filter performs the sinX/X compensation. The receive filter is removed from the circuit via the SCP in BR2 (b4).) The input to the smoothing filter is the output to the receive trim gain stage. This stage is intended to compensate for gain tolerances of external components such as handset receivers. This stage is capable of 0 to 7 dB of attenuation in 1–dB steps. This stage only accommodates attenuation because the nominal signal levels of the DAC should be next to the clip levels of this device's circuitry and any positive gain would overdrive the outputs. The gain is programmed via the SCP port in BR2 (b2:b0).The output of the 2–pole active smoothing filter is buffered by an amplifier which is output at the RO pin. This output is capable of driving a 2 kΩ load to the V_{AG} pin.

Receive Analog Output Drivers and Power Supply

The high current analog output circuitry (PO+, PO–, PI, AXO+, AXO–) is powered by the V_{EXT} power supply pin. Due to the wide range of V_{EXT} operating voltages for this device, this circuitry and the RO pin have a programmable reference point of either V_{AG} (2.4 V) or $V_{EXT}/2$. In applications where this device is powered with 5 V, it is recommended that the dc reference for this circuitry be programmed to V_{AG}. This allows maximum output signals for driving high power telephone line transformer interfaces and loud speaker/ringers. For applications that are battery powered, V_{AG} pin will still be 2.4 V, but the receive analog output circuitry will be powered from as low as 2.7 V. To optimize the output power, this circuitry should be referenced to one half of the battery voltage, $V_{EXT}/2$. The RO pin is powered by the V_{DD} pin, but its dc reference point is programmed the same as the high current analog output circuitry.

This device has two pairs of power amplifiers that are connected in a push–pull configuration. These push–pull power driver pairs have similar drive capabilities, but have different circuit configurations and different intended uses. The PO+ and PO– power drivers are intended to accommodate large gain ranges with precise adjustment by two external resistors for applications such as driving a telephone line or a handset receiver. The PI pin is the inverting input to the PO– power amplifier. The non–inverting input is internally tied to the same reference as the RO output. This allows this amplifier to be used in an inverting gain circuit with two external resistors. The PO+ amplifier has a gain of – 1, and is internally connected to the PO– output. This complete power amplifier circuit is a differential (push–pull) amplifier with adjustable gain which is capable of driving a 300 Ω load to + 12 dBm when V_{EXT} is 5 V. The PO+ and PO– outputs are intended to drive loads differentially and not to V_{SS} or V_{AG}. The PO+ and PO– power amplifiers may be powered down independently of the rest of the chip by connecting the PI pin to V_{DD} or in BR2 (b5).

The other paired power driver outputs are the AXO+ and AXO– Auxiliary outputs. These push–pull output amplifiers are intended to drive a ringer or loud speaker with impedance as low as 300 Ω to + 12 dBm when V_{EXT} is 5 V. The AXO+ and AXO– outputs are intended to drive loads differentially and not to V_{SS} or V_{AG}. The AXO+ and AXO– power amplifiers may be powered down independently of the rest of the chip via the SCP port in BR2 (b6).

SIDETONE

The Sidetone function of this device allows a controlled amount of the output from the transmit filter to be summed with the output of the DAC at the input to the receive low–pass filter. The sidetone component has gains of –8.5 dB, –10.5 dB, –12.0 dB, –13.5 dB, –15.0 dB, –18.0 dB, –21.5 dB, and ≤ – 70 dB. The sidetone function is controlled by the SCP port in BR1 (b6:b4).

UNIVERSAL TONE GENERATOR

The Universal Dual Tone Generator function supports both the transmit and the receive sides of this device. When the tone generator is being used, the decoder function of the DSP circuit is disabled. The output of the tone generator is made available to the input of the receive digital gain function for use at the receive analog outputs. In handset applications, this could be used for generating DTMF, distinctive ringing or call progress feedback signals. In telephone line interface applications, this tone generator could be used for signaling on the line. The tone generator output is also available for the input to the encoder function of the DSP machine for outputting at the DT pin. This function is useful in

handset applications for non–network signaling such as information services, answering machine control, etc. At the network interface side of a cordless telephone application, this function could be used for dialing feedback or call progress to the handset. The tone generator function is controlled by the SCP port in BR4, BR5, and BR7. The tone generator does not work when the device is operated in 64 kbps mode, except when analog loopback is enabled at BR0 (b5).

POWER–DOWN AND RESET

There are two methods of putting all of this device into a low power consumption mode that makes the device nonfunctional and consumes virtually no power. $\overline{\text{PDI/RESET}}$ is the power–down input and reset pin which, when taken low, powers down the device. Another way to power the device down is by the SCP port at BR0. BR0 allows the analog section of this device to be powered down individually and/or the digital section of this device to be powered down individually. When the chip is powered down, the V_{AG}, TG, RO, PO+, PO–, AXO+, AXO–, DT and SCP Tx outputs are high impedance. To return the chip to the power–up state, $\overline{\text{PDI/RESET}}$ must be high and the SPC clock and the FST or the FSR frame sync pulses must be present. The ADPCM algorithm is reset to the CCITT initial state following the reset transition from low to high logic states. The DT output will remain in a high–impedance state for at least two FST pulses after power–up. This device is functional after being reset for full–duplex voice coding with the charge pump active.

SIGNAL PROCESSING CLOCK (SPC)

This is the clock that sequences the DSP circuit. This clock may be asynchronous to all other functions of this device. Clock frequencies of 20.48 MHz or 20.736 MHz are recommended. This clock is also used to drive a digitally phase–locked prescaler that is referenced to FST (8 kHz) and automatically determines the proper divide ratio to use for achieving the required 256 kHz internal sequencing clock for all analog signal processing, including analog–to–digital conversion, digital–to–analog conversion, transmit filtering, receive filtering and analog gain functions of this device, and the charge pump.

The analog sequencing function of the SPC clock may be eliminated by reprogramming the device to use the BCLKR pin as the direct input for the required 256 kHz analog sequencing clock. The 256 kHz clock applied at BCLKR must be an integer 32 times the FST 8 kHz clock and be approximately rising edge aligned with the FST rising edge. This mode requires that the transmit and receive ADPCM transfers be controlled by the BCLKT pin. This is reprogrammed via the SCP port in BR0(b7).

DIGITAL I/O

The MC14LC5540 is programmable for Mu–Law or A–Law. The timing for the PCM data transfer is independent of the companding scheme selected. Table 1 shows the 8–bit data word format for positive and negative zero and full scale for both 64 kbps companding schemes (see Figures 1 through 5 for a summary and comparison of the five PCM data interface modes of this device).

Long Frame Sync

Long Frame Sync is the industry name for one type of clocking format which controls the transfer of the ADPCM or PCM data words (see Figures 1 through 4). The "Frame Sync" or "Enable" is used for two specific synchronizing functions. The first is to synchronize the PCM data word transfer, and the second is to control the internal analog–to–digital and digital–to–analog conversions. The term "Sync" refers to the function of synchronizing the PCM data word onto or off of the multiplexed serial PCM data bus, also known as a PCM highway. The term "Long" comes from the duration of the frame sync measured in PCM data clock cycles. Long Frame Sync timing occurs when the frame sync is used directly as the PCM data output driver enable. This results in the PCM output going low impedance with the rising edge of the transmit frame sync, and remaining low impedance for the duration of the transmit frame sync.

The implementation of Long Frame Sync for this device has maintained industry compatibility and been optimized for external clocking simplicity. The PCM data output goes low impedance with the rising edge of the FST pin but the MSB of the data is clocked out due to the logical AND of the transmit frame sync (FST pin) with the transmit data clock (BCLKT pin). This allows either the rising edge of the FST enable or the rising edge of the BCLKT data clock to be first. This implementation includes the PCM data output remaining low impedance until the middle of the LSB (seven and a half data clock cycles for 64 kbps PCM, three and a half data clock cycles for 32 kbps ADPCM, etc.). This allows the frame sync to be approximately rising edge aligned with the initiation of the PCM data word transfer but the frame sync does not have a precise timing requirement for the end of the PCM data word transfer. This prevents bus contention between similar devices on a common bus. The device recognizes Long Frame Sync clocking when the frame sync is held high for two consecutive falling edges of the transmit data clock.

In the full–duplex speech mode, the DSP services one encode interrupt and one decode interrupt per frame (125 μs). The encode algorithm (i.e., 16 kbps, 24 kbps, or 32 kbps ADPCM or 64 kbps PCM) is determined by the length of the transmit output enable at the FST pin. The length of the FST enable measured in transmit data clock (BCLKT) cycles tells the device which encoding rate to use. This enable length information is used by the encoder each frame. The transmit ADPCM word corresponding to this request will be computed during the next frame and be available a total of two frames after being requested. This transmit enable length information can be delayed by the device an additional four frames corresponding to a total of six frames. This six frames of delay allows the device to be clocked with the same clocks for both transmit (encode) and receive (decode), and to be frame aligned for applications that require every sixth frame signaling. It is important to note that the enable length information is delayed and not the actual ADPCM (PCM) sample word. The amount of delay for the FST enable length is controlled by the SCP port at BR7 (b5). The digital data output circuitry counts BCLKT cycles to keep the data output (DT pin) low impedance for the duration of the ADPCM data word (2, 3, 4, or 8 BCLKT cycles) minus one half of a BCLKT cycle.

Table 1. PCM Full Scale and Zero Words

Level	Mu–Law			A–Law		
	Sign Bit	Chord Bits	Step Bits	Sign Bit	Chord Bits	Step Bits
+ Full Scale	1	0 0 0	0 0 0 0	1	0 1 0	1 0 1 0
+ Zero	1	1 1 1	1 1 1 1	1	1 0 1	0 1 0 1
– Zero	0	1 1 1	1 1 1 1	0	1 0 1	0 1 0 1
– Full Scale	0	0 0 0	0 0 0 0	0	0 1 0	1 0 1 0

The length of the FST enable tells the DSP what encoding algorithm to use. The transmit logic decides on each frame sync whether it should interpret the next frame sync pulse as a Long or a Short Frame Sync. The device is designed to prevent PCM bus contention by not allowing the PCM data output to go low impedance for at least two frame sync cycles after power is applied or when coming out of the power–down mode.

The receive side of the device is designed to accept the same frame sync and data clock as the transmit side and to be able to latch its own transmit PCM data word. Thus the PCM digital switch only needs to be able to generate one type of frame sync for use by both transmit or receive sections of the device.

The logical AND of the receive frame sync with the receive data clock tells the device to start latching the serial word into the receive data input on the falling edges of the receive data clock. The internal receive logic counts the receive data clock falling edges while the FSR enable is high and transfers the enable length and the PCM data word into internal registers for access by the DSP machine which also sets the DSP's decoder interrupt.

The receive digital section of this device accepts serial ADPCM (PCM) words at the DR pin under the control of the BCLKR and FSR pins. The FSR enable duration measured in BCLKR cycles, tells the device which decode algorithm (i.e., 16 kbps, 24 kbps, or 32 kbps ADPCM, or 64 kbps PCM) the DSP machine should use for the word that is being received at the DR pin. This algorithm may be changed on a frame by frame basis.

When the device is programmed to be in the PCM Codec mode by BR0 (4:3), the device will output and input the complete 8–bit PCM words using the Long Frame Sync clocking format as though the FST and FSR pulses were held high for 8 data clock cycles.

The DSP machine receives an interrupt when an ADPCM word has been received and is waiting to be decoded into a PCM word. The DSP machine performs a decode and an encode every frame when the device is operating in its full–duplex conversation mode. The DSP machine decodes the ADPCM word according to CCITT G.726 for 32 kbps, 24 kbps, and 16 kbps.

Short Frame Sync

Short Frame Sync is the industry name for this type of clocking format which controls the transfer of the ADPCM data words (see Figure 5). This device uses Short Frame Sync timing for 32 kbps ADPCM only. The "Frame Sync" or "Enable" is used for two specific synchronizing functions. The first is to synchronize the ADPCM data word transfer, and the second is to control the internal analog to digital and digital to analog conversions. The term "Sync" refers to the function of synchronizing the ADPCM data word onto or off of the multiplexed serial ADPCM data bus, also known as a PCM highway. The term "Short" comes from the duration of the frame sync measured in PCM data clock cycles. Short Frame Sync timing occurs when the frame sync is used as a "pre–synchronization" pulse that is used to tell the internal logic to clock out the ADPCM data word under complete control of the data clock. The Short Frame Sync is held high for one falling data clock edge. The device outputs the ADPCM data word beginning with the following rising edge of the data clock. This results in the ADPCM output going low impedance with the rising edge of the transmit data clock, and remaining low impedance until the middle of the LSB (three and a half PCM data clock cycles).

The device recognizes Short Frame Sync clocking when the frame sync is held high for one and only one falling edge of the transmit data clock. The transmit logic decides on each frame sync whether it should interpret the next frame sync pulse as a Long or a Short Frame Sync. It is not recommended to switch between Long Frame Sync and Short Frame Sync clocking without going through a power–down cycle due to bus contention problems. The device is designed to prevent PCM bus contention by not allowing the ADPCM data output to go low impedance for at least two frame sync cycles after power is applied or when coming out of a powered down mode.

The receive side of the device is designed to accept the same frame sync and data clock as the transmit side and to be able to latch its own transmit ADPCM data word. Thus the PCM digital switch only needs to be able to generate one type of frame sync for use by both transmit or receive sections of the device.

The falling edge of the receive data clock (BCLKR) latching a high logic level at the receive frame sync (FSR) input tells the device to start latching the 4–bit ADPCM serial word into the receive data input on the following four falling edges of the receive data clock. The internal receive logic counts the receive data clock cycles and transfers the ADPCM data word to a register for access by the DSP.

When the device is programmed to be in the PCM Codec mode by BR0 (4:3), the device will output the complete 8–bit PCM word using the Short Frame Sync clocking format. The 8–bit PCM word will be clocked out (or in) the same way that the 4–bit ADPCM word would be, except that the fourth bit will be valid for the full BCLKT period and the eighth bit will be valid for only one half of the BCLKT period.

SERIAL CONTROL PORT REGISTER MAP

The SCP register map consists of 16 byte registers. Registers BR0 – BR5 and BR7 – BR10 provide external control of and status of the part. Register BR15 holds the value of the mask number for the particular MC14LC5540. BR6 and BR11 – BR14 are not defined and as such are presently reserved.

Table 2. Byte Register Map

Byte	b7	b6	b5	b4	b3	b2	b1	b0
BR0	Ext 256 kHz CLK	Mu–/A–Law Select	Analog Loopback	I/O Mode (1)	I/O Mode (0)	Charge Pump Disable	Analog Power Down	Digital Power Down
BR1	Reserved	Sidetone Gain (2)	Sidetone Gain (1)	Sidetone Gain (0)	Transmit Mute	Transmit Gain (2)	Transmit Gain (1)	Transmit Gain (0)
BR2	RO Reference Select	AXO Enable	PO Disable	Receive Filter Disable	RO Mute	Analog Receive Gain (2)	Analog Receive Gain (1)	Analog Receive Gain (0)
BR3	Digital Rx Gain Enable	Digital Rx Gain (6)	Digital Rx Gain (5)	Digital Rx Gain (4)	Digital Rx Gain (3)	Digital Rx Gain (2)	Digital Rx Gain (1)	Digital Rx Gain (0)
BR4	N.B. Time / Tone Param. (7)	N.B. Time / Tone Param. (6)	N.B. Time / Tone Param. (5)	N.B. Time / Tone Param. (4)	N.B.Time / Tone Param. (3)	N.B. Time / Tone Param. (2)	N.B. Time / Tone Param. (1)	N.B. Time / Tone Param. (0)
BR5	N.B. Threshold (7) / Address Param. (1)	N.B. Threshold (6) / Address Param. (0)	N.B. Threshold (5) / Don't Care	N.B. Threshold (4) / Don't Care	N.B. Threshold (3) / Tone Param. (11)	N.B. Threshold (2) / Tone Param. (10)	N.B. Threshold (1) / Tone Param. (9)	N.B. Threshold (0) / Tone Param. (8)
BR6	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
BR7	Tone Param. Status	N.B. Detect Enable	2/6 Delay	G.726/ Motorola 16 kbps	Tone Enable	Reserved	Tone 1 Enable	Tone 2 Enable
BR8	Software Encoder Reset	Software Decoder Reset	Linear Codec Mode	Highpass Disable	Reserved	Reserved	Reserved	Reserved
BR9	Encoder PCM (7)	Encoder PCM (6)	Encoder PCM (5)	Encoder PCM (4)	Encoder PCM (3)	Encoder PCM (2)	Encoder PCM (1)	Encoder PCM (0)
BR10	D/A PCM (7)	D/A PCM (6)	D/A PCM (5)	D/A PCM (4)	D/A PCM (3)	D/A PCM (2)	D/A PCM (1)	D/A PCM (0)
BR11	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
BR12	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
BR13	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
BR14	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
BR15	Reserved	Reserved	Reserved	Reserved	Mask (3)	Mask (2)	Mask (1)	Mask (0)

NOTE: "Setting" a bit corresponds to writing a 1 to the register and "clearing" a bit corresponds to writing a 0 to the register.

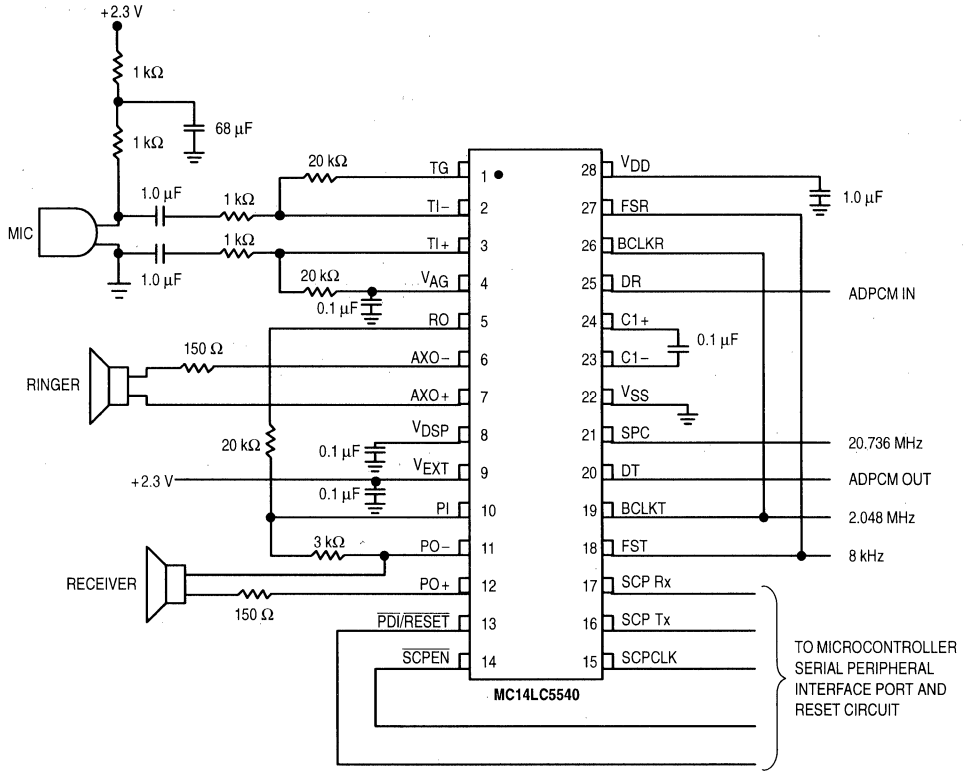


Figure 11. MC14LC5540 Handset Application

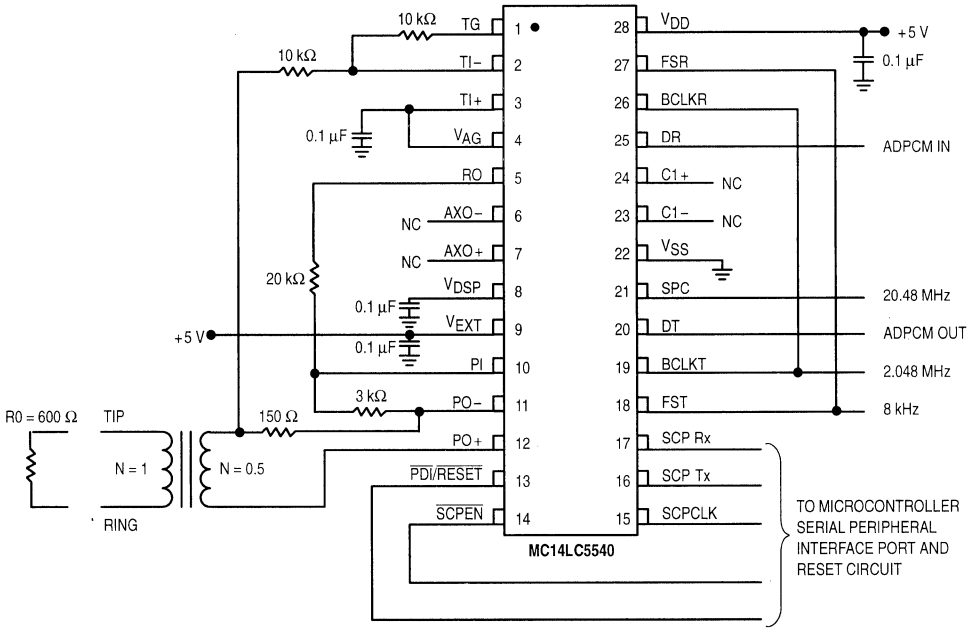


Figure 12. MC14LC5540 Transformer Application

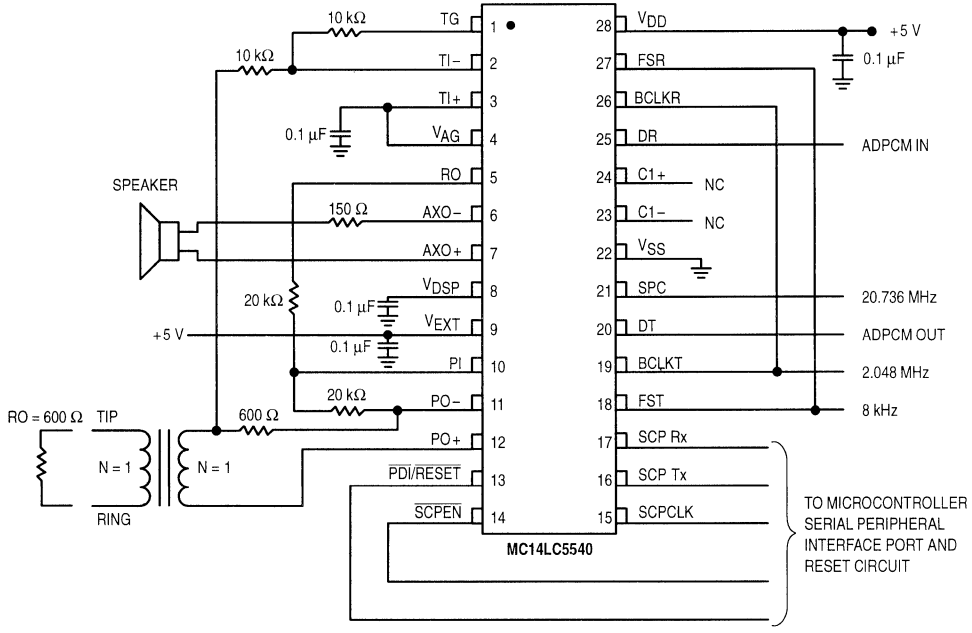


Figure 13. MC14LC5540 Transformer + Speaker Application

MC145541

Product Preview

2 V ADPCM Codec

2

The MC145541 ADPCM Codec is a single chip implementation of a PCM Codec–Filter and an ADPCM encoder/decoder. This device provides an efficient solution for applications requiring the digitization and compression of voiceband signals. The MC145541 is designed to operate over the voltage range 1.8 to 3.6 V, and is ideal for battery–powered as well as ac–powered applications. The MC145541 ADPCM Codec also includes a serial control port and internal control and status registers that permit a microcontroller to exercise many built–in features. The MC145541 ADPCM Codec is designed to meet the 32 kbps ADPCM conformance requirements of CCITT Recommendation G.721–1988 and ANSI T1.301–1987. It also meets ANSI T1.303 and CCITT Recommendation G.723–1988 for 24 kbps ADPCM operation, and the 16 kbps ADPCM standard of CCITT Recommendation G.726. This device also meets the PCM conformance specification of the CCITT G.714 Recommendation.

The MC145541 package is a 44–pin 10 mm body, Thin Quad Flat Package (TQFP).

- Single 1.8 to 3.6 V Power Supply
- Typical Active Power Dissipation at 3.0 V of 20 mW
- ADPCM Transcoding Rates of 32, 24, and 16 kbps
- Independent Access to the 64 kbps PCM Data
- Complete Mu–Law or A–Law Companding PCM Codec–Filter
- Transmit VOX Function to Determine if Speech is Present
- Comfort Noise Generator for Receive Side
- Receive Noise Burst Detect Circuit
- Universal Dual Tone Generator

REV 0
9/95

PCM Codec-Filter

MC145554
MC145557
MC145564
MC145567

The MC145554, MC145557, MC145564, and MC145567 are all per channel PCM Codec–Filters. These devices perform the voice digitization and reconstruction as well as the band limiting and smoothing required for PCM systems. They are designed to operate in both synchronous and asynchronous applications and contain an on–chip precision voltage reference. The MC145554 (Mu–Law) and MC145557 (A–Law) are general purpose devices that are offered in 16–pin packages. The MC145564 (Mu–Law) and MC145567 (A–Law), offered in 20–pin packages, add the capability of analog loopback and push–pull power amplifiers with adjustable gain.

These devices have an input operational amplifier whose output is the input to the encoder section. The encoder section immediately low–pass filters the analog signal with an active R–C filter to eliminate very–high–frequency noise from being modulated down to the pass band by the switched capacitor filter. From the active R–C filter, the analog signal is converted to a differential signal. From this point, all analog signal processing is done differentially. This allows processing of an analog signal that is twice the amplitude allowed by a single–ended design, which reduces the significance of noise to both the inverted and non–inverted signal paths. Another advantage of this differential design is that noise injected via the power supplies is a common–mode signal that is cancelled when the inverted and non–inverted signals are recombined. This dramatically improves the power supply rejection ratio.

After the differential converter, a differential switched capacitor filter band passes the analog signal from 200 Hz to 3400 Hz before the signal is digitized by the differential compressing A/D converter.

The decoder accepts PCM data and expands it using a differential D/A converter. The output of the D/A is low–pass filtered at 3400 Hz and sinX/X compensated by a differential switched capacitor filter. The signal is then filtered by an active R–C filter to eliminate the out–of–band energy of the switched capacitor filter.

These PCM Codec–Filters accept both long–frame and short–frame industry standard clock formats. They also maintain compatibility with Motorola's family of TSACs and MC3419/MC34120 SLIC products.

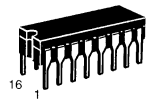
The MC145554/57/64/67 family of PCM Codec–Filters utilizes CMOS due to its reliable low–power performance and proven capability for complex analog/digital VLSI functions.

MC145554/57 (16–Pin Package)

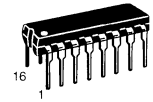
- Fully Differential Analog Circuit Design for Lowest Noise
- Performance Specified for Extended Temperature Range of – 40 to + 85°C
- Transmit Band–Pass and Receive Low–Pass Filters On–Chip
- Active R–C Pre–Filtering and Post–Filtering
- Mu–Law Companding MC145554
- A–Law Companding MC145557
- On–Chip Precision Voltage Reference (2.5 V)
- Typical Power Dissipation of 40 mW, Power Down of 1.0 mW at ± 5 V

MC145564/67 (20–Pin Package) — All of the Features of the MC145554/57 Plus:

- Mu–Law Companding MC145564
- A–Law Companding MC145567
- Push–Pull Power Drivers with External Gain Adjust
- Analog Loopback



L SUFFIX
CERAMIC PACKAGE
CASE 620
MC145554/57



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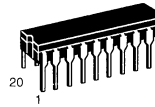
PLASTIC DIP
CASE 648
MC145554/57

DW SUFFIX
SOG PACKAGE
CASE 751G
MC145554/57



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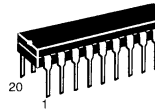
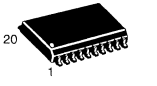
CASE 732
MC145564/67



P SUFFIX
PLASTIC DIP
CASE 738
MC145564/67

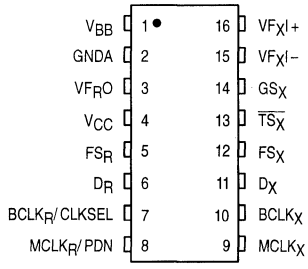


DW SUFFIX
SOG PACKAGE
CASE 751D
MC145564/67

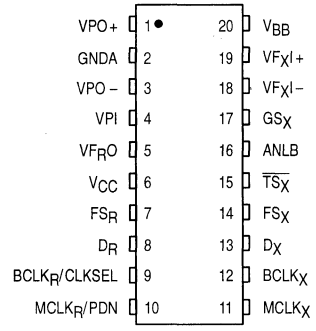
REV 1
9/95 (Replaces ADI1517)

PIN ASSIGNMENTS

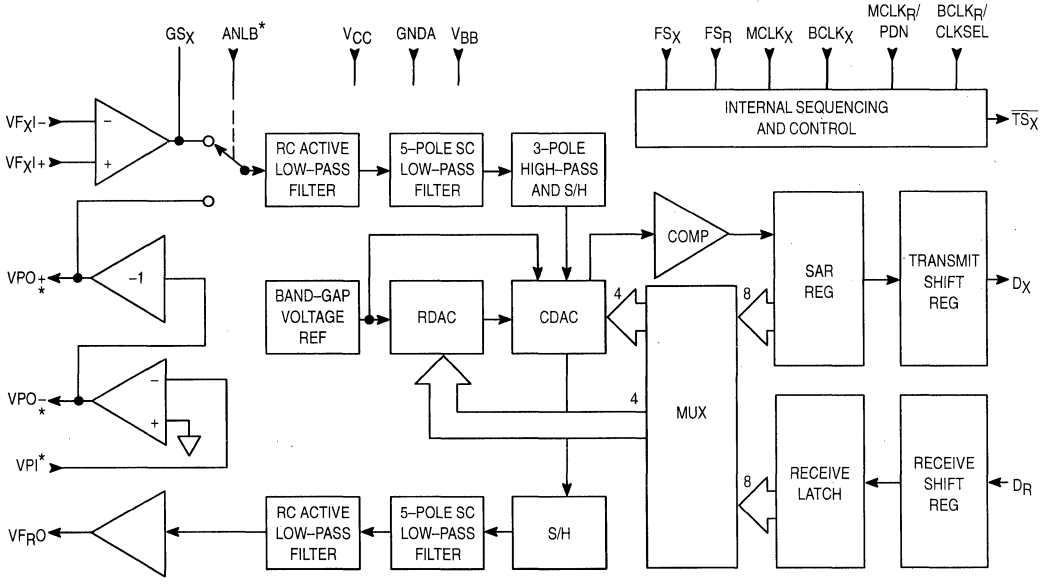
MC145554, MC145557



MC145564, MC145567



FUNCTIONAL BLOCK DIAGRAM



* MC145564 and MC145567 only.

DEVICE DESCRIPTION

A codec–filter is used for digitizing and reconstructing the human voice. These devices were developed primarily for the telephone network to facilitate voice switching and transmission. Once the voice is digitized, it may be switched by digital switching methods or transmitted long distance (T1, microwave, satellites, etc.) without degradation. The name codec is an acronym from "COder" (for the A/D used to digitize voice) and "DECoder" (for the D/A used for reconstructing voice). A codec is a single device that does both the A/D and D/A conversions.

To digitize intelligible voice requires a signal–to–distortion ratio of about 30 dB over a dynamic range of about 40 dB. This can be accomplished with a linear 13–bit A/D and D/A, but will far exceed the required signal–to–distortion ratio at amplitudes greater than 40 dB below the peak amplitude. This excess performance is at the expense of data per sample. Methods of data reduction are implemented by compressing the 13–bit linear scheme to companded 8–bit schemes. There are two companding schemes used: Mu–255 Law specifically in North America, and A–Law specifically in Europe. These companding schemes are accepted world wide. These companding schemes follow a segmented or "piecewise–linear" curve formatted as sign bit, three chord bits, and four step bits. For a given chord, all sixteen of the steps have the same voltage weighting. As the voltage of the analog input increases, the four step bits increment and carry to the three chord bits which increment. When the chord bits increment, the step bits double their voltage weighting. This results in an effective resolution of six bits (sign + chord + four step bits) across a 42 dB dynamic range (seven chords above zero, by 6 dB per chord). Tables 3 and 4 show the linear quantization levels to PCM words for the two companding schemes.

In a sampling environment, Nyquist theory says that to properly sample a continuous signal, it must be sampled at a frequency higher than twice the signal's highest frequency component. Voice contains spectral energy above 3 kHz, but its absence is not detrimental to intelligibility. To reduce the digital data rate, which is proportional to the sampling rate, a sample rate of 8 kHz was adopted, consistent with a bandwidth of 3 kHz. This sampling requires a low–pass filter to limit the high frequency energy above 3 kHz from distorting the in–band signal. The telephone line is also subject to 50/60 Hz power line coupling, which must be attenuated from the signal by a high–pass filter before the A/D converter.

The D/A process reconstructs a staircase version of the desired in–band signal, which has spectral images of the in–band signal modulated about the sample frequency and its harmonics. These spectral images, called aliasing components, need to be attenuated to obtain the desired signal. The low–pass filter used to attenuate these aliasing components is typically called a reconstruction or smoothing filter.

The MC145554/57/64/67 PCM Codec–Filters have the codec, both presampling and reconstruction filters, and a precision voltage reference on–chip, and require no external components.

PIN DESCRIPTION

DIGITAL

FS_R
Receive Frame Sync

This is an 8 kHz enable that must be synchronous with $BCLK_R$. Following a rising FS_R edge, a serial PCM word at D_R is clocked by $BCLK_R$ into the receive data register. FS_R also initiates a decode on the previous PCM word. In the absence of FS_X, the length of the FS_R pulse is used to determine whether the I/O conforms to the Short Frame Sync or Long Frame Sync convention.

D_R
Receive Digital Data Input

$BCLK_R$/CLKSEL
Receive Data Clock and Master Clock Frequency Selector

If this input is a clock, it must be between 128 kHz and 4.096 MHz, and synchronous with FS_R. In synchronous applications this pin may be held at a constant level; then $BCLK_X$ is used as the data clock for both the transmit and receive sides, and this pin selects the assumed frequency of the master clock (see Table 1 in **Functional Description**).

$MCLK_R$/PDN
Receive Master Clock and Power–Down Control

Because of the shared DAC architecture used on these devices, only one master clock is needed. Whenever FS_X is clocking, $MCLK_X$ is used to derive all internal clocks, and the $MCLK_R$/PDN pin merely serves as a power–down control. If $MCLK_R$/PDN pin is held low or is clocked (and at least one of the frame syncs is present), the part is powered up. If this pin is held high, the part is powered down. If FS_X is absent but FS_R is still clocking, the device goes into receive half–channel mode, and $MCLK_R$ (if clocking) generates the internal clocks.

$MCLK_X$
Transmit Master Clock

This clock is used to derive the internal sequencing clocks; it must be 1.536 MHz, 1.544 MHz, or 2.048 MHz.

$BCLK_X$
Transmit Data Clock

$BCLK_X$ may be any frequency between 128 kHz and 4.096 MHz, but it should be synchronous with $MCLK_X$.

D_X
Transmit Digital Data Output

This output is controlled by FS_X and $BCLK_X$ to output the PCM data word; otherwise this pin is in a high–impedance state.

FS_X
Transmit Frame Sync

This is an 8 kHz enable that must be synchronous with $BCLK_X$. A rising FS_X edge initiates the transmission of a

serial PCM word, clocked by $BCLK_X$, out of D_X. If the FS_X pulse is high for more than eight $BCLK_X$ periods, the D_X and $\overline{TS_X}$ outputs will remain in a low–impedance state until FS_X is brought low. The length of the FS_X pulse is used to determine whether the transmit and receive digital I/O conforms to the Short Frame Sync or to the Long Frame Sync convention.

$\overline{TS_X}$
Transmit Time Slot Indicator

This is an open–drain output that goes low whenever the D_X output is in a low–impedance state (i.e., during the transmit time slot when the PCM word is being output) for enabling a PCM bus driver.

ANLB
Analog Loopback Control Input (MC145564/67 Only)

When held high, this pin causes the input of the transmit RC active filter to be disconnected from GS_X and connected to VPO+ for analog loopback testing. This pin is held low in normal operation.

ANALOG

GS_X
Gain–Setting Transmit

This output of the transmit gain–adjust operational amplifier is internally connected to the encoder section of the device. It must be used in conjunction with VF_XI- and VF_XI+ to set the transmit gain for a maximum signal amplitude of 2.5 V peak. This output can drive a 600 Ω load to 2.5 V peak.

VF_XI-
Voice–Frequency Transmit Input (Inverting)

This is the inverting input of the transmit gain–adjust operational amplifier.

VF_XI+
Voice–Frequency Transmit Input (Non–Inverting)

This is the non–inverting input of the transmit gain–adjust operational amplifier.

VF_RO
Voice–Frequency Receive Output

This receive analog output is capable of driving a 600 Ω load to 2.5 V peak.

VPI
Voltage Power Input (MC145564/67 Only)

This is the inverting input to the first receive power amplifier. Both of the receive power amplifiers can be powered down by connecting this input to V_{BB}.

VPO–
Voltage Power Output (Inverted) (MC145564/67 Only)

This inverted output of the receive push–pull power amplifiers can drive 300 Ω to 3.3 V peak.

VPO+
Voltage Power Output (Non–Inverted) (MC145554/67 Only)

This non–inverted output of the receive push–pull power amplifier pair can drive 300 Ω to 3.3 V peak.

POWER SUPPLY

GNDA
Analog Ground

This terminal is the reference level for all signals, both analog and digital. It is 0 V.

V_{CC}
Positive Power Supply

V_{CC} is typically 5 V.

V_{BB}
Negative Power Supply

V_{BB} is typically – 5 V.

FUNCTIONAL DESCRIPTION

ANALOG INTERFACE AND SIGNAL PATH

The transmit portion of these codec–filters includes a low–noise gain setting amplifier capable of driving a 600 Ω load. Its output is fed to a three–pole anti–aliasing pre–filter. This pre–filter incorporates a two–pole Butterworth active low–pass filter, and a single passive pole. This pre–filter is followed by a single ended–to–differential converter that is clocked at 256 kHz. All subsequent analog processing utilizes fully differential circuitry. The next section is a fully–differential, five–pole switched capacitor low–pass filter with a 3.4 kHz passband. After this filter is a 3–pole switched–capacitor high–pass filter having a cutoff frequency of about 200 Hz. This high–pass stage has a transmission zero at dc that eliminates any dc coming from the analog input or from accumulated operational amplifier offsets in the preceding filter stages. The last stage of the high–pass filter is an auto-zeroed sample and hold amplifier.

One bandgap voltage reference generator and digital–to–analog converter (DAC) are shared by the transmit and receive sections. The autozeroed, switched–capacitor bandgap reference generates precise positive and negative reference voltages that are independent of temperature and power supply voltage. A binary–weighted capacitor array (CDAC) forms the chords of the companding structure, while a resistor string (RDAC) implements the linear steps within each chord. The encode process uses the DAC, the voltage reference, and a frame–by–frame autozeroed comparator to implement a successive–approximation conversion algorithm. All of the analog circuitry involved in the data conversion — the voltage reference, RDAC, CDAC, and comparator — are implemented with a differential architecture.

The receive section includes the DAC described above, a sample and hold amplifier, a five–pole 3400 Hz switched capacitor low–pass filter with sinX/X correction, and a two–pole active smoothing filter to reduce the spectral components of the switched capacitor filter. The output of the smoothing filter is a power amplifier that is capable of driving a 600 Ω load. The MC145564 and MC145567 add a pair of power amplifiers that are connected in a push–pull configuration; two external resistors set the gain of both of the

complementary outputs. The output of the second amplifier may be internally connected to the input of the transmit anti–aliasing filter by bringing the ANLB pin high. The power amplifiers can drive unbalanced 300 Ω loads or a balanced 600 Ω load; they may be powered down independent of the rest of the chip by tying the VPI pin to V_{BB}.

MASTER CLOCKS

Since the codec–filter design has a single DAC architecture, only one master clock is used. In normal operation (both frame syncs clocking), the $MCLK_X$ is used as the master clock, regardless of whether the $MCLK_R$/PDN pin is clocking or low. The same is true if the part is in transmit half–channel mode (FS_X clocking, FS_R held low). But if the codec–filter is in the receive half–channel mode, with FS_R clocking and FS_X held low, $MCLK_R$ is used for the internal master clock if it is clocking; if MCLKR is low, then $MCLK_X$ is still used for the internal master clock. Since only one of the master clocks is used at any given time, they need not be synchronous.

The master clock frequency must be 1.536 MHz, 1.544 MHz, or 2.048 MHz. The frequency that the codec–filter expects depends upon whether the part is a Mu–Law or an A–Law part, and on the state of the $BCLK_R$/CLKSEL pin. The allowable options are shown In Table 1. When a level (rather than a clock) is provided for $BCLK_R$/CLKSEL, $BCLK_X$ is used as the bit clock for both transmit and receive.

Table 1. Master Clock Frequency Determination

	Master Clock Frequency Expected	
$BCLK_R$/CLKSEL	MC145554/64	MC145557/67
Clocked, 1, or Open	1.536 MHz 1.544 MHz	2.048 MHz
0	2.048 MHz	1.536 MHz 1.544 MHz

FRAME SYNCS AND DIGITAL I/O

These codec–filters can accommodate both of the industry standard timing formats. The Long Frame Sync mode is used by Motorola's MC145500 family of codec–filters and the UDLT family of digital loop transceivers. The Short Frame Sync mode is compatible with the IDL (Interchip Digital Link) serial format used in Motorola's ISDN family and by other companies in their telecommunication devices. These codec–filters use the length of the transmit frame sync (FS_X) to determine the timing format for both transmit and receive unless the part is operating in the receive half–channel mode.

In the Long Frame Sync mode, the frame sync pulses must be at least three bit clock periods long. The D_X and $\overline{TS_X}$ outputs are enabled by the logical ANDing of FS_X and $BCLK_X$; when both are high, the sign bit appears at the D_X output. The next seven rising edges of $BCLK_X$ clock out the remaining seven bits of the PCM word. The D_X and $\overline{TS_X}$ outputs return to a high impedance state on the falling edge of the eighth bit clock or the falling edge of FS_X, whichever comes later. The receive PCM word is clocked into D_R on the eight falling $BCLK_R$ edges following an FS_R rising edge.

For Short Frame Sync operation, the frame sync pulses must be one bit clock period long. On the first $BCLK_X$ rising edge after the falling edge of $BCLK_X$ has latched FS_X high, the D_X and $\overline{TS_X}$ outputs are enabled and the sign bit is presented on D_X. The next seven rising edges of $BCLK_X$ clock out the remaining seven bits of the PCM word; on the eighth $BCLK_X$ falling edge, the D_X and $\overline{TS_X}$ outputs return to a high impedance state. On the second falling $BCLK_R$ edge following an FS_R rising edge, the receive sign bit is clocked into D_R. The next seven $BCLK_R$ falling edges clock in the remaining seven bits of the receive PCM word.

Table 2 shows the coding format of the transmit and receive PCM words.

HALF–CHANNEL MODES

In addition to the normal full–duplex operating mode, these codec–filters can operate in both transmit and receive half–channel modes. Transmit half–channel mode is entered by holding FS_R low. The VF_RO output goes to analog ground but remains in a low impedance state (to facilitate a hybrid interface); PCM data at D_R is ignored. Holding FS_X low while clocking FS_R puts these devices in the receive half–channel mode. In this state, the transmit input operational amplifier continues to operate, but the rest of the transmit circuitry is disabled; the D_X and $\overline{TS_X}$ outputs remain in a high impedance state. $MCLK_R$ is used as the internal master clock if it is clocking. If $MCLK_R$ is not clocking, then $MCLK_X$ is used for the internal master clock, but in that case it should be synchronous with FS_R. If $BCLK_R$ is not clocking, $BCLK_X$ will be used for the receive data, just as in the full–channel operating mode. In receive half–channel mode only, the length of the FS_R pulse is used to determine whether Short Frame Sync or Long Frame Sync timing is used at D_R.

POWER–DOWN

Holding both FS_X and FS_R low causes the part to go into the power–down state. Power–down occurs approximately 2 ms after the last frame sync pulse is received. An alternative way to put these devices in power–down is to hold the $MCLK_R$/PDN pin high. When the chip is powered down, the D_X, $\overline{TS_X}$, and GS_X outputs are high impedance, the VF_RO, VPO–, and VPO+ operational amplifiers are biased with a trickle current so that their respective outputs remain stable at analog ground. To return the chip to the power–up state, $MCLK_R$/PDN must be low or clocking and at least one of the frame sync pulses must be present. The D_X and $\overline{TS_X}$ outputs will remain in a high–impedance state until the second FS_X pulse after power–up.

Table 2. PCM Data Format

	Mu–Law (MC145554/64)			A–Law (MC145557/67)		
Level	Sign Bit	Chord Bits	Step Bits	Sign Bit	Chord Bits	Step Bits
+ Full Scale	1	000	0000	1	010	1010
+ Zero	1	111	1111	1	101	0101
– Zero	0	111	1111	0	101	0101
– Full Scale	0	000	0000	0	010	1010

MAXIMUM RATINGS (Voltage Referenced to GNDA)

Rating	Symbol	Value	Unit
DC Supply Voltage V_{CC} to V_{BB} V_{CC} to GNDA V_{BB} to GNDA		– 0.5 to + 13 – 0.3 to + 7.0 – 7.0 to + 0.3	V
Voltage on Any Analog Input or Output Pin		V_{BB} – 0.3 to V_{CC} + 0.3	V
Voltage on Any Digital Input or Output Pin		GNDA – 0.3 to V_{CC} + 0.3	V
Operating Temperature Range	T_A	– 40 to + 85	°C
Storage Temperature Range	T_{stg}	– 85 to + 150	°C

This device contains circuitry to protect against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., V_{BB}, GNDA, or V_{CC}).

2

POWER SUPPLY (T_A = – 40 to + 85°C)

Characteristic		Min	Typ	Max	Unit
DC Supply Voltage	V_{CC} V_{BB}	4.75 – 4.75	5.0 – 5.0	5.25 – 5.25	V
Active Power Dissipation (No Load)	MC145554/57 MC145564/67 MC145564/67, VPI = V_{BB}	— — —	40 45 40	60 70 60	mW
Power–Down Dissipation (No Load)	MC145554/57 MC145564/67 MC145564/67, VPI = V_{BB}	— — —	1.0 2.0 1.0	3.0 5.0 3.0	mW

DIGITAL LEVELS (V_{CC} = 5 V ± 5%, V_{BB} = – 5 V ± 5%, GNDA = 0 V, T_A = – 40 to + 85°C)

Characteristic		Symbol	Min	Max	Unit
Input Low Voltage		V_{IL}	—	0.6	V
Input High Voltage		V_{IH}	2.2	—	V
Output Low Voltage	D_X or $\overline{TS_X}$, I_{OL} = 3.2 mA	V_{OL}	—	0.4	V
Output High Voltage	D_X, I_{OH} = – 3.2 mA I_{OH} = – 1.6 mA	V_{OH}	2.4 V_{CC} – 0.5	— —	V
Input Low Current	GNDA ≤ $V_{in} \le V_{CC}$	I_{IL}	– 10	+ 10	µA
Input High Current	GNDA ≤ $V_{in} \le V_{CC}$	I_{IH}	– 10	+ 10	µA
Output Current in High Impedance State	GNDA ≤ $D_X \le V_{CC}$	I_{OZ}	– 10	+ 10	µA

ANALOG ELECTRICAL CHARACTERISTICS

(V_{CC} = +5 V ± 5%, V_{BB} = – 5 V ± 5%, VF_XI – Connected to GS_X, T_A = – 40 to + 85°C)

Characteristic		Min	Typ	Max	Unit
Input Current (– 2.5 ≤ V_{in} ≤ + 2.5 V)	VF_XI+, VF_XI-	—	± 0.05	± 0.2	µA
AC Input Impedance to GNDA (1 kHz)	VF_XI+, VF_XI-	10	20	—	MΩ
Input Capacitance	VF_XI+, VF_XI-	—	—	10	pF
Input Offset Voltage of GS_X Op Amp	VF_XI+, VF_XI-	—	—	± 25	mV
Input Common Mode Voltage Range	VF_XI+, VF_XI-	– 2.5	—	2.5	V
Input Common Mode Rejection Ratio	VF_XI+, VF_XI-	—	65	—	dB
Unity Gain Bandwidth of GS_X Op Amp (R_{load} ≥ 10 kΩ)		—	1000	—	kHz
DC Open Loop Gain of GS_X Op Amp (R_{load} ≥ 10 kΩ)		75	—	—	dB
Equivalent Input Noise (C–Message) Between VF_XI+ and VF_XI- at GS_X		—	–20	—	dBrnC0
Output Load Capacitance for GS_X Op Amp		0	—	100	pF
Output Voltage Range for GS_X	R_{load} = 10 kΩ to GNDA R_{load} = 600 Ω to GNDA	– 3.5 – 2.8	— —	+ 3.5 + 2.8	V
Output Current (– 2.8 V ≤ V_{out} ≤ + 2.8 V)	GS_X, VF_RO	± 5.0	—	—	mA
Output Impedance VF_RO (0 to 3.4 kHz)		—	1	—	Ω
Output Load Capacitance for VF_RO		0	—	500	pF
VF_RO Output DC Offset Voltage Referenced to GNDA		—	—	± 100	mV
Transmit Power Supply Rejection	Positive, 0 to 100 kHz, C–Message Negative, 0 to 100 kHz, C–Message	45 45	— —	— —	dBC
Receive Power Supply Rejection	Positive, 0 to 100 kHz, C–Message Positive, 4 kHz to 25 kHz Positive, 25 kHz to 50 kHz Negative, 0 to 100 kHz, C–Message Negative, 4 kHz to 25 kHz Negative, 25 kHz to 50 kHz	50 50 43 50 45 38	— — — — — —	— — — — — —	dBC dB dB dBC dB dB

MC145564/67 Power Drivers

Input Current (– 1 V ≤ VPI ≤ + 1 V)	VPI	—	±0.05	±0.5	µA
Input Resistance (– 1 V ≤ VPI ≤ + 1 V)	VPI	5	10	—	MΩ
Input Offset Voltage (VPI Connected to VPO–)	VPI	—	—	±50	mV
Output Resistance, Inverted Unity Gain	VPO+ or VPO–	—	1	—	Ω
Unity Gain Bandwidth, Open Loop	VPO–	—	400	—	kHz
Load Capacitance (∞ Ω ≥ R_{load} ≥ 300 Ω)	VPO+ or VPO– to GNDA	0	—	1000	pF
Gain from VPO– to VPO+ (R_{load} = 300 Ω, VPO+ to GNDA Level at VPO– = 1.77 Vrms, +3 dBm0)		—	–1	—	V/V
Maximum 0 dBm0 Level for Better than ± 0.1 dB Linearity Over the Range – 10 dBm0 to + 3 dBm0 (For R_{load} between VPO+ and VPO–)	R_{load} = 600 Ω R_{load} = 1200 Ω R_{load} = 10 kΩ	3.3 3.5 4.0	— — —	— — —	Vrms
Power Supply Rejection of V_{CC} or V_{BB} (VPO– Connected to VPI) VPO+ or VPO– to GNDA	0 to 4 kHz 4 to 50 kHz	55 35	— —	— —	dB
Differential Power Supply Rejection of V_{CC} or V_{BB} (VPO– Connected to VPI)	VPO+ to VPO–, 0 to 50 kHz	50	—	—	dB

ANALOG TRANSMISSION PERFORMANCE

(V_{CC} = + 5 V ± 5%, V_{BB} = – 5 V ± 5%, GNDA = 0 V, 0 dBm0 = 1.2276 Vrms = + 4 dBm @ 600 Ω, FS_X = FS_R = 8 kHz, $BCLK_X$ = $MCLK_X$ = 2.048 MHz Synchronous Operation, VF_XI – Connected to GS_X, T_A = – 40 to + 85°C Unless Otherwise Noted)

Characteristic		End–to–End Min	End–to–End Max	A/D Min	A/D Max	D/A Min	D/A Max	Unit
Absolute Gain (0 dBm0 @ 1.02 kHz, T_A = 25°C, V_{CC} = 5 V, V_{BB} = – 5 V)		—	—	–0.25	– 0.25	– 0.25	+ 0.25	dB
Absolute Gain Variation with Temperature	0 to 70°C	—	—	—	± 0.03	—	± 0.03	dB
	– 40 to + 85°C	—	—	—	± 0.06	—	± 0.06	
Absolute Gain Variation with Power Supply (V_{CC} = 5 V, ± 5%, V_{BB} = – 5 V, ± 5%)		—	—	—	± 0.02	—	± 0.02	dB
Gain vs Level Tone (Relative to – 10 dBm0, 1.02 kHz)	+ 3 to – 40 dBm0	– 0.4	+ 0.4	– 0.2	+ 0.2	– 0.2	+ 0.2	dB
	– 40 to – 50 dBm0	– 0.8	+ 0.8	– 0.4	+ 0.4	– 0.4	+ 0.4	
	– 50 to – 55 dBm0	– 1.6	+ 1.6	– 0.8	+ 0.8	– 0.8	+ 0.8	
Gain vs Level Pseudo Noise CCITT G.712 (MC145557/67 A–Law Relative to – 10 dBm0)	– 10 to – 40 dBm0	—	—	– 0.25	+ 0.25	– 0.25	+ 0.25	dB
	– 40 to – 50 dBm0	—	—	– 0.30	+ 0.30	– 0.30	+ 0.30	
	– 50 to – 55 dBm0	—	—	– 0.45	+ 0.45	– 0.45	+ 0.45	
Total Distortion, 1.02 kHz Tone (C–Message)	+ 3 dBm0	33	—	33	—	33	—	dBC
	0 to – 30 dBm0	35	—	36	—	36	—	
	– 40 dBm0	29	—	30	—	30	—	
	– 45 dBm0	24	—	25	—	25	—	
	– 55 dBm0	15	—	15	—	15	—	
Total Distortion With Pseudo Noise CCITT G.714 (MC145557/67 A–Law)	– 3 dBm0	27.5	—	28	—	28.5	—	dB
	– 6 to – 27 dBm0	35	—	35.5	—	36	—	
	– 34 dBm0	33.1	—	33.5	—	34.2	—	
	– 40 dBm0	28.2	—	28.5	—	30	—	
	– 55 dBm0	13.2	—	13.5	—	15	—	
Idle Channel Noise (For End–End and A/D, Note 1)								
(MC145554/64 Mu–Law, C–Message Weighted)		—	15	—	15	—	7	dBrnC0
(MC145557/67 A–Law, Psophometric Weighted)		—	–70	—	– 70	—	– 83	dBm0p
Frequency Response (Relative to 1.02 kHz @ 0 dBm0)	15 Hz	—	– 40	—	– 40	– 0.15	0	dB
	50 Hz	—	– 30	—	– 30	– 0.15	0	
	60 Hz	—	– 26	—	– 26	– 0.15	0	
	200 Hz	—	—	– 1.0	– 0.4	– 0.15	0	
	300 to 3000 Hz	– 0.3	0.3	– 0.15	+ 0.15	– 0.15	+ 0.15	
	3300 Hz	– 0.70	+ 0.3	– 0.35	+ 0.15	– 0.35	+ 0.15	
	3400 Hz	– 1.6	0	– 0.8	0	– 0.8	0	
	4000 Hz	—	– 28	—	– 14	—	– 14	
	4600 Hz	—	– 60	—	– 32	—	– 30	
In–Band Spurious (1.02 kHz @ 0 dBm0, Transmit and Receive)	300 to 3000 Hz	—	–48	—	– 48	—	– 48	dBm0
Out–of–Band Spurious at VF_RO (300 – 3400 Hz @ 0 dBm0 In)								dB
	4600 to 7600 Hz	—	– 30	—	—	—	– 30	
	7600 to 8400 Hz	—	– 40	—	—	—	– 40	
	8400 to 100,000 Hz	—	– 30	—	—	—	– 30	
Idle Channel Noise Selective (8 kHz, Input = GNDA, 30 Hz Bandwidth)		—	–70	—	—	—	– 70	dBm0
Absolute Delay (1600 Hz)		—	—	—	315	—	215	µs
Group Delay Referenced to 1600 Hz	500 to 600 Hz	—	—	—	220	– 40	—	µs
	600 to 800 Hz	—	—	—	145	– 40	—	
	800 to 1000 Hz	—	—	—	75	– 40	—	
	1000 to 1600 Hz	—	—	—	40	– 30	—	
	1600 to 2600 Hz	—	—	—	75	—	90	
	2600 to 2800 Hz	—	—	—	105	—	125	
	2800 to 3000 Hz	—	—	—	155	—	175	
Crosstalk of 1020 Hz @ 0 dBm0 from A/D or D/A (Note 2)		—	—	—	– 75	—	– 75	dB
Intermodulation Distortion of Two Frequencies of Amplitudes – 4 to – 21 dBm0 from the Range 300 to 3400 Hz		—	– 41	—	– 41	—	– 41	dB

NOTES:

3. Extrapolated from a 1020 Hz @ – 50 dBm0 distortion measurement to correct for encoder enhancement.
4. Selectively measured while the A/D is stimulated with 2667 Hz @ – 50 dBm0.

DIGITAL SWITCHING CHARACTERISTICS

(V_{CC} = 5 V ± 5%, V_{BB} = – 5 V ± 5%, GNDA = 0 V, All Signals Referenced to GNDA; T_A = – 40 to + 85°C, C_{load} = 150 pF Unless Otherwise Noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Master Clock Frequency	$MCLK_X$ or $MCLK_R$	f_M	— — —	1.536 1.544 2.048	— — —	MHz
Minimum Pulse Width High or Low	$MCLK_X$ or $MCLK_R$	$t_{w(M)}$	100	—	—	ns
Minimum Pulse Width High or Low	$BCLK_X$ or $BCLK_R$	$t_{w(B)}$	50	—	—	ns
Minimum Pulse WIdth Low	FS_X or FS_R	$t_{w(FL)}$	50	—	—	ns
Rise Time for all Digital Signals		t_r	—	—	50	ns
Fall Time for all Digital Signals		t_f	—	—	50	ns
Bit Clock Data Rate	$BCLK_X$ or $BCLK_R$	f_B	128	—	4096	kHz
Setup Time from $BCLK_X$ Low to $MCLK_R$ High		$t_{su(BRM)}$	50	—	—	ns
Setup Time from $MCLK_X$ High to $BCLK_X$ Low		$t_{su(MFB)}$	20	—	—	ns
Hold Time from $BCLK_X$ ($BCLK_R$) Low to FS_X (FS_R) High		$t_{h(BF)}$	20	—	—	ns
Setup Time for FS_X (FS_R) High to $BCLK_X$ ($BCLK_R$) Low for Long Frame		$t_{su(FB)}$	80	—	—	ns
Delay Time from $BCLK_X$ High to D_X Data Valid		$t_{d(BD)}$	20	60	140	ns
Delay Time from $BCLK_X$ High to $\overline{TS_X}$ Low		$t_{d(BTS)}$	20	50	140	ns
Delay Time from the 8th $BCLK_X$ Low of FS_X Low to D_X Output Disabled		$t_{d(ZC)}$	50	70	140	ns
Delay Time to Valid Data from FS_X or $BCLK_X$, Whichever is Later		$t_{d(ZF)}$	20	60	140	ns
Setup Time from D_R Valid to $BCLK_X$ Low		$t_{su(DB)}$	0	—	—	ns
Hold Time from $BCLK_R$ Low to D_R Invalid		$t_{h(BD)}$	50	—	—	ns
Setup Time from FS_X (FS_R) High to $BCLK_X$ ($BCLK_R$) Low in Short Frame		$t_{su(F)}$	50	—	—	ns
Hold Time from $BCLK_X$ ($BCLK_R$) Low to FS_X (FS_R) Low in Short Frame		$t_{h(F)}$	50	—	—	ns
Hold Time from 2nd Period of $BCLK_X$ ($BCLK_R$) Low to FS_X (FS_R) Low in Long Frame		$t_{h(BFI)}$	50	—	—	ns

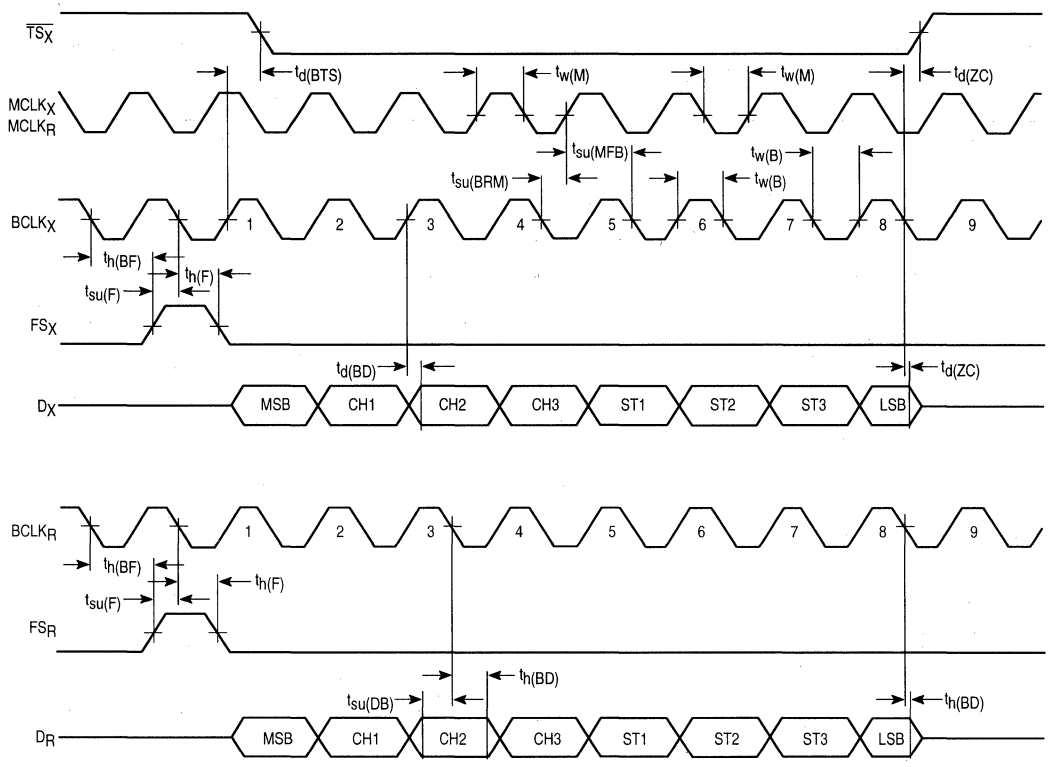


Figure 1. Short Frame Sync Timing

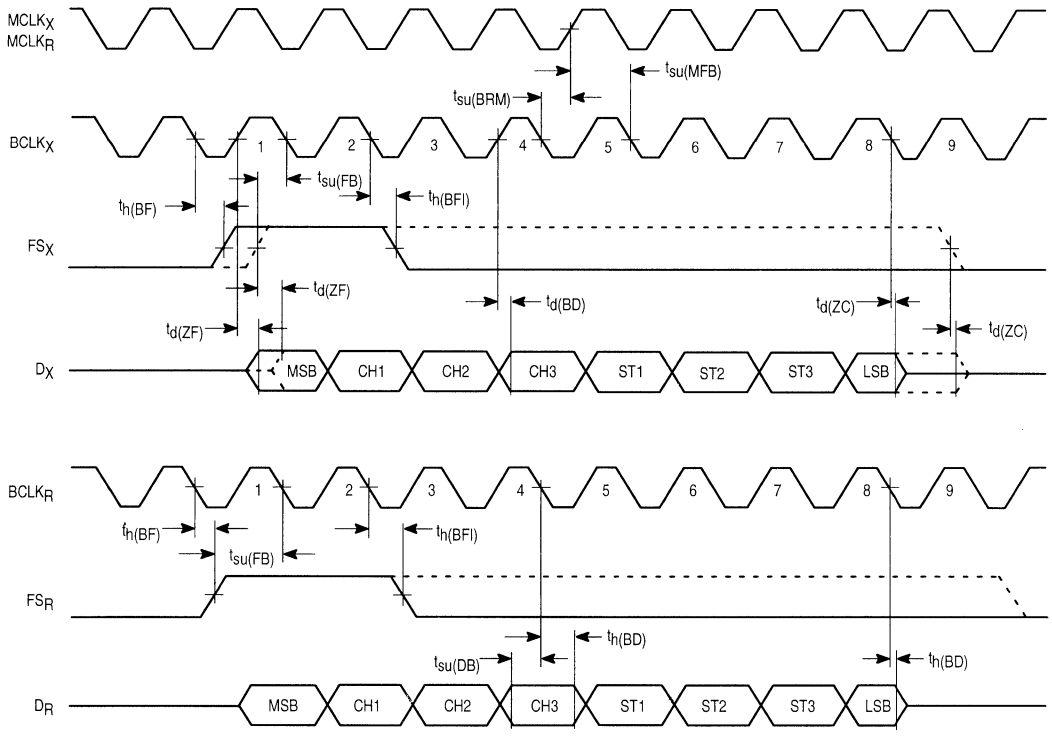


Figure 2. Long Frame Sync Timing

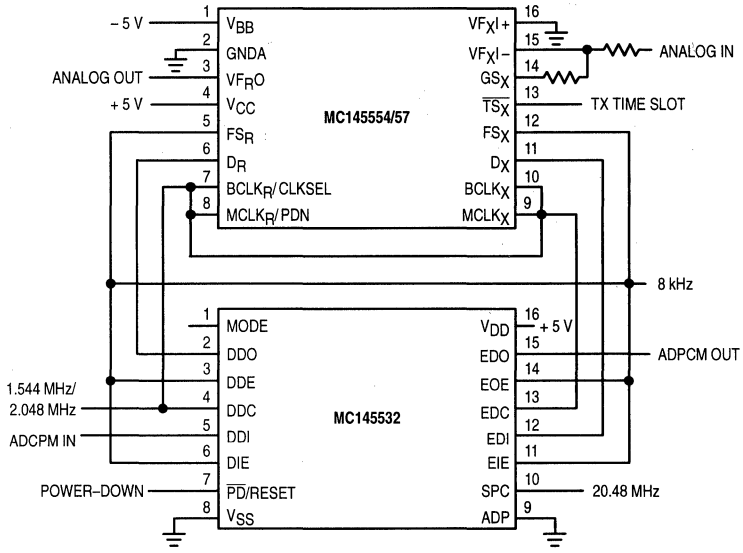
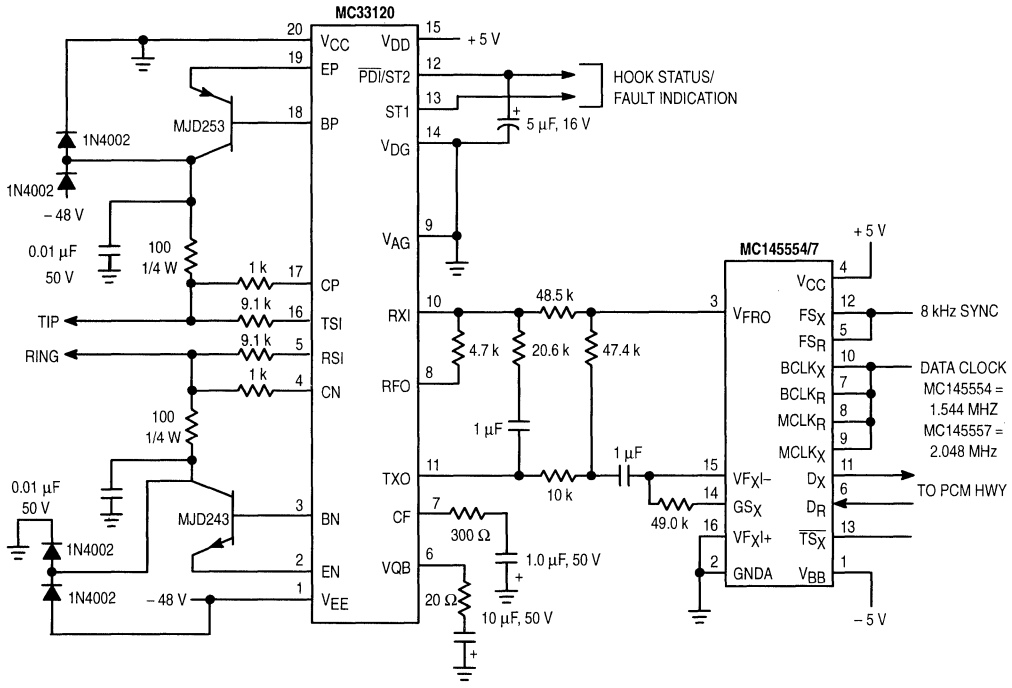


Figure 3. ADPCM Transcoder Application



NOTE: Six resistors and two capacitors on the two–wire side can be 5% tolerance.

Figure 4. A Complete Single Party Channel Unit Using MC145554/57 PCM Codec–Filter and MC33120 SLIC

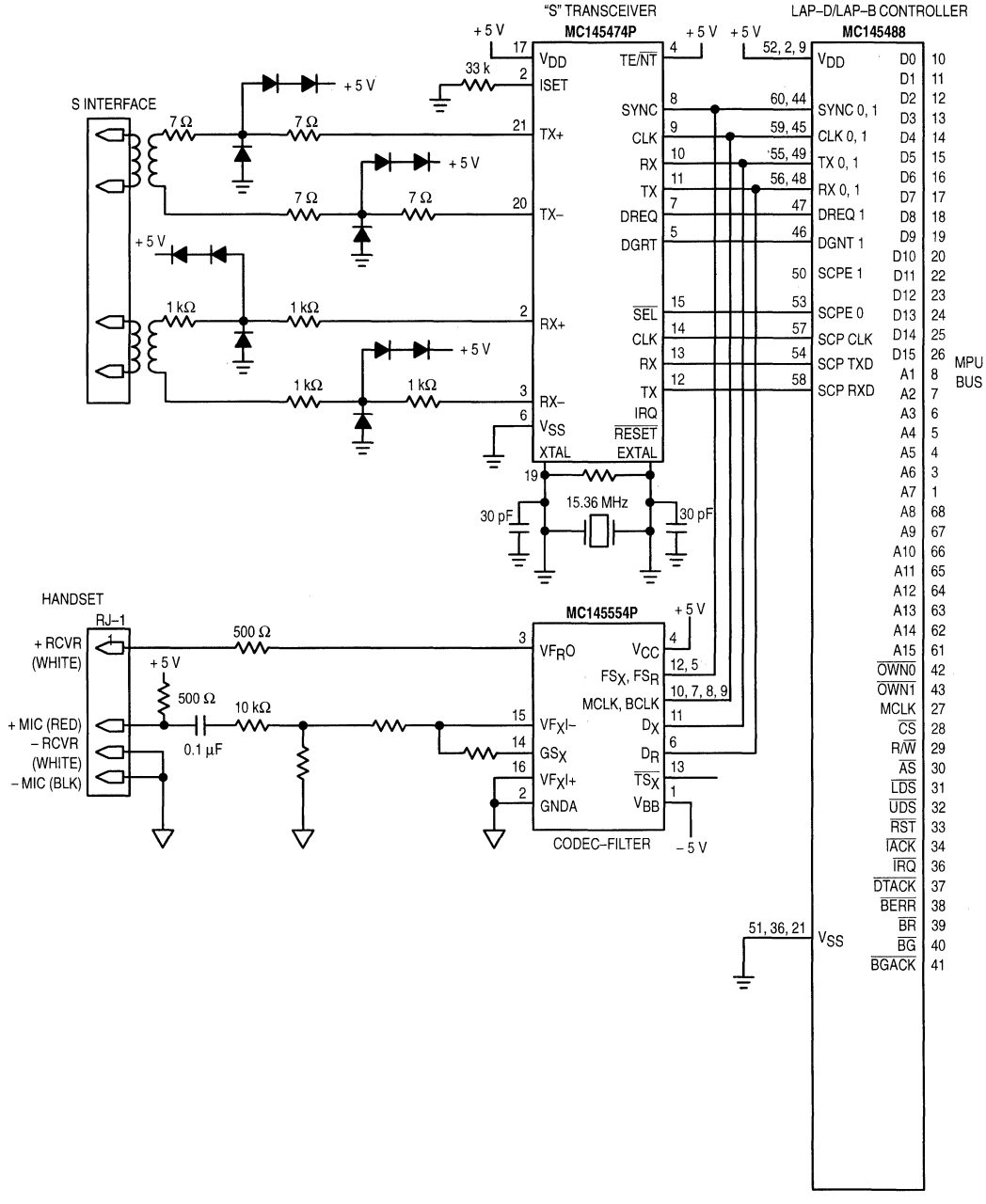


Figure 5. ISDN Voice/Data Terminal

Table 3. Mu–Law Encode–Decode Characteristics

Chord Number	Number of Steps	Step Size	Normalized Encode Decision Levels	Digital Code 1 Sign	2 Chord	3 Chord	4 Chord	5 Step	6 Step	7 Step	8 Step	Normalized Decode Levels
			8159									
				1	0	0	0	0	0	0	0	8031
			7903									
8	16	256	⋮					⋮				⋮
			4319									
				1	0	0	0	1	1	1	1	4191
			4063									
			⋮					⋮				⋮
7	16	128	2143									
				1	0	0	1	1	1	1	1	2079
			2015									
			⋮					⋮				⋮
6	16	64	1055									
				1	0	1	0	1	1	1	1	1023
			991									
			⋮					⋮				⋮
5	16	32	511									
				1	0	1	1	1	1	1	1	495
			479									
			⋮					⋮				⋮
4	16	16	239									
				1	1	0	0	1	1	1	1	231
			223									
			⋮					⋮				⋮
3	16	8	103									
				1	1	0	1	1	1	1	1	99
			95									
			⋮					⋮				⋮
2	16	4	35									
				1	1	1	0	1	1	1	1	33
			31									
			⋮					⋮				⋮
1	15	2	3									
				1	1	1	1	1	1	1	0	2
	1	1	1									
				1	1	1	1	1	1	1	1	0
			0									

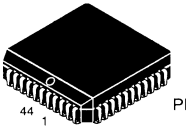
NOTES:
1. Characteristics are symmetrical about analog zero with sign bit = 0 for negative analog values.
2. Digital code includes inversion of all magnitude bits.

Table 4. A–Law Encode–Decode Characteristics

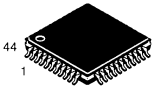
Chord Number	Number of Steps	Step Size	Normalized Encode Decision Levels	Digital Code 1 Sign	2 Chord	3 Chord	4 Chord	5 Step	6 Step	7 Step	8 Step	Normalized Decode Levels
			4096									
				1	0	1	0	1	0	1	0	4032
7	16	128	3968 ⋮ 2176					⋮				⋮
				1	0	1	0	0	1	0	1	2112
6	16	64	2048 ⋮ 1088					⋮				⋮
				1	0	1	1	0	1	0	1	1056
5	16	32	1024 ⋮ 544					⋮				⋮
				1	0	0	0	0	1	0	1	528
4	16	16	512 ⋮ 272					⋮				⋮
				1	0	0	1	0	1	0	1	264
3	16	8	256 ⋮ 136					⋮				⋮
				1	1	1	0	0	1	0	1	132
2	16	4	128 ⋮ 68					⋮				⋮
				1	1	1	1	0	1	0	1	66
1	32	2	64 ⋮ 2					⋮				⋮
				1	1	0	1	0	1	0	1	1
			0									

NOTES:
1. Characteristics are symmetrical about analog zero with sign bit = 0 for negative analog values.
2. Digital code includes alternate bit inversion, as specified by CCITT.

MC145572



FN SUFFIX
PLCC PACKAGE
CASE 777



PB SUFFIX
TQFP
CASE 824D

ORDERING INFORMATION

MC145572FN	PLCC Package
MC145572PB	TQFP

2

Technical Summary

ISDN U-Interface Transceiver

This technical summary provides an overview of the MC145572 U–Interface Transceiver. A complete data booklet with comprehensive technical information is available and can be ordered through your Motorola Sales office.

The MC145572 U–Interface Transceiver is a single chip device for Integrated Services Digital Network Basic Access Interface that conforms to the American National Standard ANSI T1.601–1992. The device, which can be configured for LT (Line Termination) or NT (Network Termination) applications, performs all necessary Layer 1 functions while utilizing 2B1Q line coding.

The MC145572 is a redesign of the MC145472 and MC14LC5472 U–Interface Transceivers. The internal signal processing algorithms are the same as for the original MC145472 to maintain its industry–leading performance. The control and time division multiplex interfaces have been significantly enhanced to serve the needs of the growing ISDN marketplace. The use of the latest process technologies permits the MC145572 to be made available in 44–lead PLCC and PQFP packages.

The MC145572 is designed to be easily retrofit into existing MC145472/MC14LC5472 designs with no software changes and few hardware changes. New designs can take advantage of enhanced digital interface features of the MC145572, such as the timeslot assigner and the availability of superframe alignment signals.

The MC145572 can operate in many different modes. The control of these various modes is provided via special purpose pins and the Serial Control Port (SCP) or the Parallel Control Port (PCP). The SCP conforms to the Motorola Serial Control Peripheral Interface standard, an industry standard serial microprocessor interface. The PCP is a standard microprocessor bus port. The designer may choose between using GCI or the Motorola IDL–type time division 2B+D data interface. A timeslot assigner is also provided on the MC145572.

The customer data crossing the U Reference Point consists of two 64 kbps B channels and one 16 kbps D channel in each direction. Maintenance and framing overhead is also included for a total 160 kbps data (80 Kbaud signaling) rate.

Features

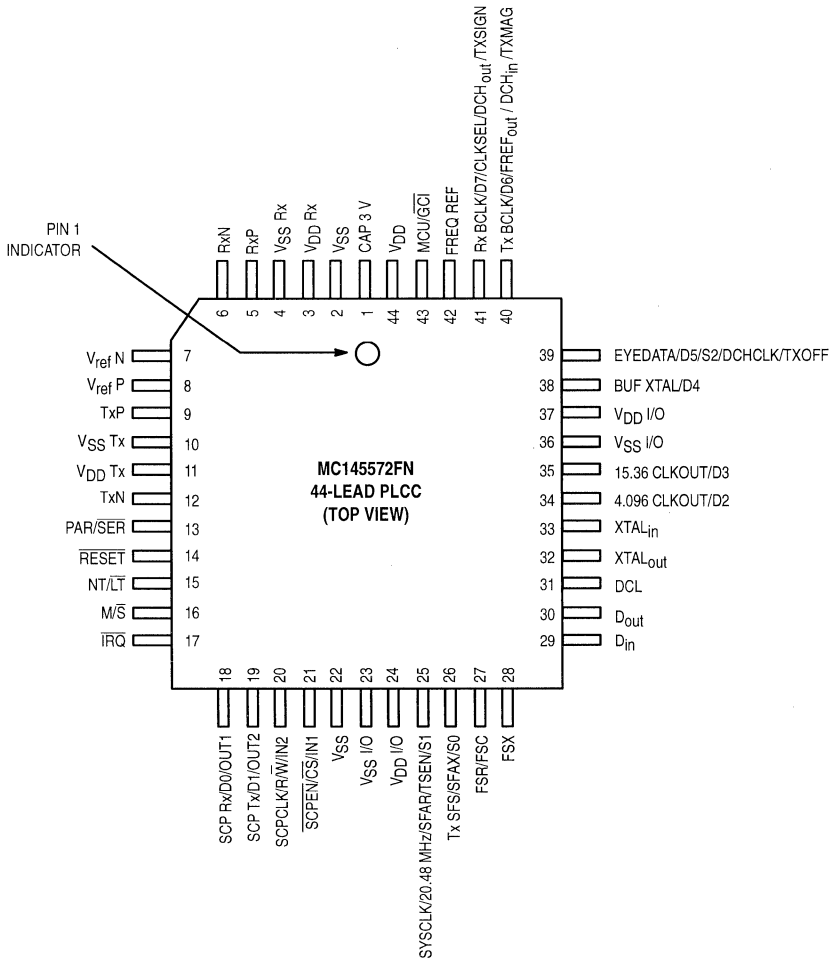
- Single Chip 2B1Q Echo Canceling Adaptively Equalized Transceiver
- Conforms to ANSI T1.601–1992, *Integrated Services Digital Network (ISDN)–Basic Access Interface for Use on Metallic Loops for Application on the Network Side of the NT (Layer 1 Specification)* of the American National Standards Institute
- Warm Start Capability
- NT Synchronizes to and Operates with 80 kHz ± 32 ppm Received Signal from LT
- Supports Master–Slave, and Slave–Slave Timing Modes
- On–Chip FIFOs for Transmit and Receive Directions
- 2B+D Customer Data Provided by the Industry Standard Interchip Digital Link
- General Circuit Interface (GCI)
- Timeslot Assigner
- Control, Status, and Extended Maintenance Functions Provided through the Serial Control Port (SCP)
- Microprocessor Bus Compatible Parallel Port Available as Pin Selectable Option

REV 1
10/95

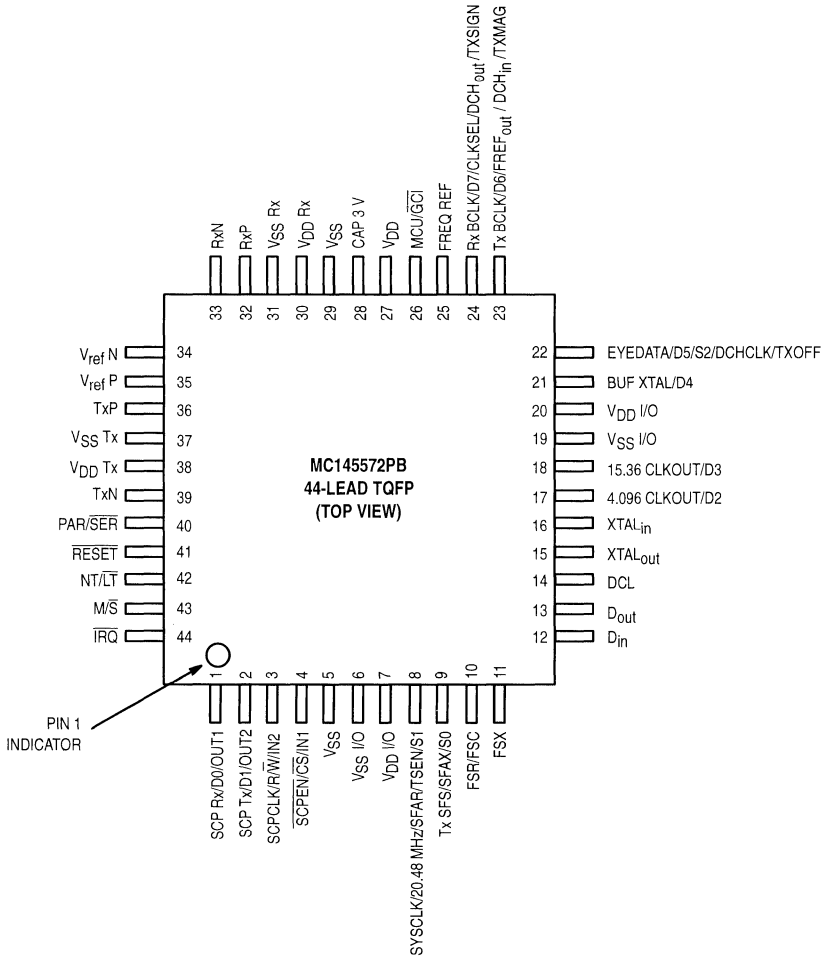
- On–Chip Conformance with Activation and Deactivation as Specified in ANSI T1.601
- Automatic Handling of Basic Maintenance Functions
- Automatic Internal Compliance with the Embedded Operations Channel (eoc) Protocol as Specified in the American National Standard
- Complete Set of Loop–Backs for Both the IDL and U–Reference Point Directions
- Pin Selectable for Line Termination or Network Termination Applications
- On–Chip 2.5 V Transmit Driver Meeting 1992 Requirement
- 8 kHz Reference Frequency in LT Mode
- High Performance CMOS Process Technology
- 5 V Power Supply

2

MC145572FN PIN ASSIGNMENT



MC145572PB PIN ASSIGNMENT



MAXIMUM RATINGS (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	– 0.5 to 7.0	V
V_{in}	Voltage, Any Pin to V_{SS}	– 0.3 to V_{DD} + 0.3	V
I_{in}	DC Current, Any Pin (Except for V_{DD}, V_{SS}, TxP, and TxN)	± 10	mA
T_A	Operating Temperature	– 40 to 85	°C
T_{stg}	Storage Temperature	– 85 to 150	°C

This device contains circuitry to protect against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., V_{SS}, V_{DD}, V_{LS}, or V_{AG}).

2

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS}, T_A = – 40 to 85°C)

Parameter	Pins	Min	Typ	Max	Unit
DC Supply Voltage	V_{DD}	4.75	5.0	5.25	V
Current Sourced from CAP 3 V pin @ 2.7 V	CAP 3V	—	—	5	mA

POWER CONSUMPTION (Voltages referenced to V_{SS}, T_A = – 40 to 85°C)

Parameter	Pins	Min	Typ	Max	Unit
DC Supply Voltage	V_{DD}	4.75	5.0	5.25	V
Power Consumption, Activated		—	225	275	mW
Power Consumption, Absolute Power Down		—	—	5	mW

PERFORMANCE (V_{DD} = 5.0 V ± 5%, T_A = – 40 to + 85°C)

Parameter	Min	Typ	Max	Unit
Cold Start Time, LT Mode	—	9	—	s
Cold Start Time, NT Mode	—	4	—	s
Warm Start Time, LT and NT Modes	—	200	—	ms
Transmit Linearity	45	—	—	dB
Bit Error Rate, 16,500k ft of 26 AWG, 1500 ft of 24AWG, +1 dB NEXT Margin, ANSI T1.601–1992 (see Note)	—	—	10^{-7}	
Differential Receiver Sensitivity		15	20	mV

NOTE: Bit error rate performance depends significantly on the characteristics of the line interface circuit used to couple the MC145572 to the transmission line. This parameter is provided for informational purposes only.

DC ELECTRICAL CHARACTERISTICS (V_{DD} = 5.0 V + 5%, T_A = – 40 to 85°C)

Parameter	Test Conditions	Symbol	Min	Max	Unit
High–Level Input Voltage, except FREQREF and $\overline{RESET}$		V_{IH}	2.0	—	V
Low–Level Input Voltage, except FREQREF and $\overline{RESET}$		V_{IL}	– 0.3	0.8	V
High–Level Input Voltage, FREQREF and $\overline{RESET}$		V_{IH}	3.75	—	V
Low–Level Input Voltage, FREQREF and $\overline{RESET}$		V_{IL}	—	1.25	V
High–Level Output Voltage (I_{OH} = – 400 µA)		V_{OH}	2.4		V
Low–Level Output Voltage (I_{OL} = 5 mA)		V_{OL}		.5	V
High–Level Input Current		I_{IH}	—	TBD	µA
Low–Level Input Current		I_{IL}	—	TBD	µA
High–Level Output Current	$V_{OH} = V_{DD} - 0.5$ V	I_{OH}	TBD	—	mA
Low–Level Output Current	V_{OL} = 0.4 V	I_{OL}	TBD	—	mA
$\overline{IRQ}$ Output Current	V_{OL} = 0.4 V	I_{IRQ}	TBD	—	mA
$\overline{IRQ}$ High Impedance		$R_{IRQ\ off}$	TBD	—	kΩ
Input Capacitance, Digital Pins		C_{in}	—	10	pF
$XTAL_{in}$ High–Level Input			TBD	—	V
$XTAL_{in}$ Low–Level Input			—	TBD	V
$XTAL_{out}$ Output Current	V_{OH} = 3.2 V		TBD	—	mA
	V_{OL} = 1 V		TBD	—	mA

NOTE: All digital outputs except $XTAL_{out}$ are three–stateable regardless of their normal operating condition.

2B1Q INTERFACE ELECTRICAL CHARACTERISTICS

PINS TxP AND TxN (V_{DD} = 5.0 V ± 5%, T_A = – 40 to 85°C, R_L = 60 Ω from TxP to TxN)

Parameter	Min	Typ	Max	Unit
Output Resistance — Full Power Mode	—	—	0.05	Ω
Output Resistance — Power Down Mode	—	10	30	Ω
Output Resistance — Absolute Power Down Mode	—	10	30	Ω
Output Peak Voltage from TxP to TxN	—	± 4.0	—	V_{pk} $-V_{pk}$
Output Load Capacitance	—	—	47	nF
Power Supply Rejection	—	60	—	dB
Peak Current	—	75	—	mA

PINS TxP AND TxN (V_{DD} = 5.0 V ± 5%, T_A = – 40 to 85°C)

Parameter	Min	Max	Unit
Input Resistance — Full Power Mode	1	—	MΩ
Input Resistance — Power Down Mode	1	—	MΩ
Input Resistance — Absolute Power Down Mode	1	—	MΩ
Input Capacitance	—	TBD	pF
Power Supply Rejection	—	TBD	dB
Input Voltage Range for RxP or RxN	$((V_{DD} - V_{SS})/2) - 0.5$	$((V_{DD} - V_{SS})/2) + 0.5$	V

IDL2 MASTER SHORT FRAME SYNC TIMING, 8/10 BIT AND TSAC FORMATS

Ref. No.	Parameter		Min	Typ	Max	Unit	Note
1	FSR or FSX Period		125	125	—	µs	1
2	Delay From the Rising Edge of DCL to the Rising Edge of FSX or FSR		—		30	ns	
3	Delay From the Rising Edge of DCL to the Falling Edge of FSX or FSR		—		30	ns	
4	DCL Clock Period		391		1953	ns	2
5	DCL Pulse Width High	512 kHz	878		1074	ns	3
		2.048 MHz	210		265		
		2.56 MHz	170		215		
	DCL Clock 249 Pulse Width High	2.048 MHz	160		315		
		2.56 MHz	120		265		
	DCL Clock 59 Pulse Width High	512 kHz	825		1120		
6	DCL Pulse Width Low		45		55	% of DCL Period	4
7	Delay From Rising Edge of DCL to Low–Z and Valid Data on D_{out}		—		30	ns	
8	Delay From Rising Edge of DCL to Data Valid on D_{out}		5		30	ns	
9	Delay From Rising Edge of DCL to Hi–Z on D_{out}		—		30	ns	
10	Data Valid on D_{in} Before Falling Edge of DCL (D_{in} Setup Time)		25		—	ns	
11	Data Valid on D_{in} After Falling Edge of DCL (D_{in} Hold Time)		25		—	ns	
12	Delay From Rising Edge of DCL to TSEN Low		—		30	ns	5
13	Delay From Falling Edge of DCL to TSEN High		—		30	ns	

NOTES:

1. FSR or FSX occur on average every 125 µs.
2. The DCL Frequency may be 512 kHz, 2.048 MHz, or 2.56 MHz.
3. The duty cycle of DCL is between 45% and 55% when operated in master timing mode. This duty cycle is guaranteed for all DCL clocks except the clock that is used for making timing adjustments in order to maintain synchronization with the received signal when operating in NT mode. In NT master mode the MC145572 conveys timing adjustments over the DCL clock of the device. This is done by adding or subtracting a single 20.48 MHz clock period of 48 ns to the high phase of DCL clock on two successive IDL frames once per U–Interface basic frame. The total adjustment is 96 ns distributed over the two IDL frames. When DCL is configured for 2.048 MHz or 2.56 MHz the adjustment occurs during clock pulse number 249 after FSX/FSR. The count starts at clock pulse 0 for the DCL clock immediately following FSX/FSR. When DCL is configured for 512 kHz the adjustment occurs during DCL pulse number 59. It is important to remember this when using the timeslot assigner since it is possible to program it to transfer 2B or D data during the clock period where the timing adjustment is being made and this may affect setup and hold times for other components in a system.
4. The pulse width during the low phase of the clock varies between 45% and 55% of the nominal frequency. Timing adjustments are not made during the low phase of DCL.
5. In IDL 8 and 10 bit formats, TSEN can be valid during the B1, B2, and D channel timeslots.

ISDN BASIC ACCESS SYSTEM OVERVIEW

ISDN REFERENCE MODEL

The Integrated Services Digital Network (ISDN) Reference Model is shown in Figure 1. This is a general model that can be adapted to many different implementations of the ISDN. The diagram indicates the position of the U–Reference Point between the Line Termination (LT) and the Network Termination 1 (NT1) blocks in the model.

The U–Interface is the physical access point to the ISDN at the U–Reference Point. This interface is a single twisted wire pair supporting full–duplex transmission of digital information at a rate of 160 kbps. The twisted wire pair can extend up to 18,000 feet and may include bridge taps. This interface is often referred to as a Digital Subscriber Line.

U–INTERFACE TRANSCEIVER ISDN APPLICATIONS

Figure 2 shows some typical ISDN applications of the MC145572 U–Interface Transceiver as well as related ISDN applications for S/T–Interface terminal equipment using Motorola semiconductor solutions.

The LT example shows the U–Interface Transceiver in a line card environment. This line card can be located in an ISDN central office switch or other ISDN compatible switching equipment, including a remote switch or carrier terminal. In this application, the Interchip Digital Link (IDL) and Serial Control Port (SCP) of the MC145572 are interfaced to the backplane of the switching equipment as required for the particular switch architecture.

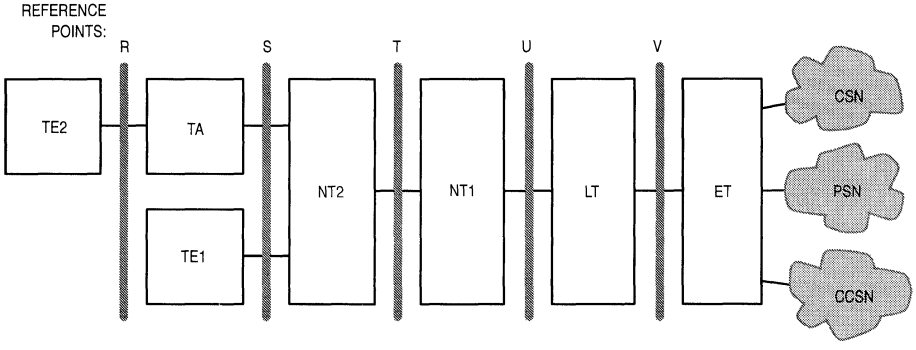
The NT1 converts the 2–wire U–Interface to the 4–wire S/T–Interface as shown. By combining an MC145572 with a Motorola MC145574 S/T–Interface Transceiver, an NT1 can be readily implemented.

Also shown is a highly integrated U–Interface ISDN terminal, designated NT1/TE1, which implements a complete voice and data terminal with a U–Interface for immediate and cost effective access to the ISDN. The MC145572 is shown interfaced to the M68000 core based MC68302 Integrated Multiprotocol Processor (IMP), which handles Layers 2 – 7 of the OSI Reference Model. Voice is supported with a conventional codec–filter device such as the MC145480.

The network is completed with a Terminal Adaptor (TA) and an S/T–interface ISDN Terminal (TE1). Two different architectures are shown: the TA is implemented with the MC145488 Dual Data Link Controller and a host MCU system, and the TE1 is shown implemented with the MC68302 IMP.

NON–ISDN U–INTERFACE TRANSCEIVER APPLICATIONS

A typical non–ISDN pair gain application block diagram is shown in Figures 3 and 4. Pair gain is a technique to multiplex two or more analog phone lines over a single twisted pair.



Key:

CCSN:	Common Channel Signalling Network	NT2:	Network Termination 2 (OSI Layers 2 and 3)
CSN:	Circuit Switched Network	PSN:	Packet Switched Network
ET:	Exchange Termination (C.O. Switch)	TA:	Terminal Adapter
LT:	Line Termination (Line Card)	TE1:	Terminal Equipment 1 (ISDN Terminal)
NT1:	Network Termination 1 (OSI Layer 1 Only)	TE2:	Terminal Equipment 2 (Non–ISDN Terminal)

Figure 1. ISDN Reference Model

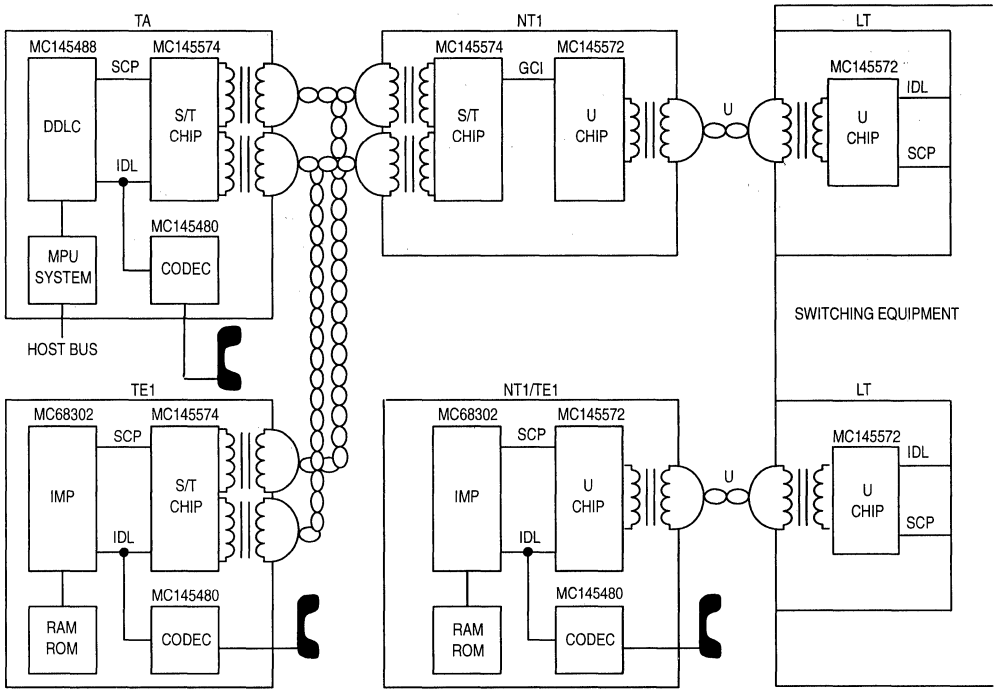


Figure 2. MC145572 Typical ISDN Applications

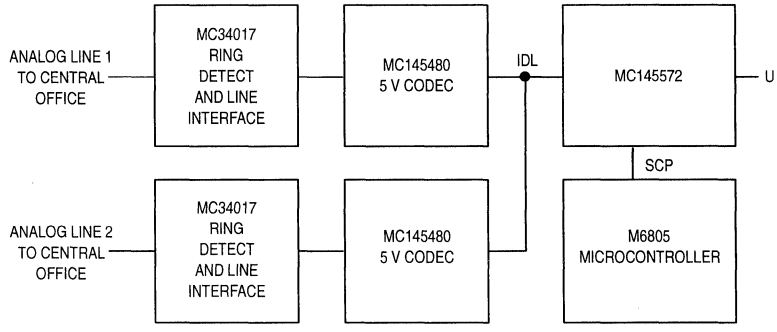


Figure 3. Pair Gain Application, Central Office Terminal

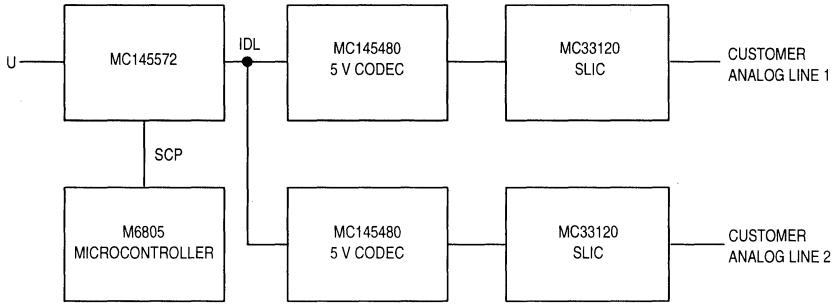


Figure 4. Pair Gain Application, Remote Terminal

FUNCTIONAL OVERVIEW

A functional block diagram of the MC145572 U–Interface Transceiver is shown in Figure 5. This device utilizes mixed analog and digital signal processing circuit technology to implement an adaptively equalized echo canceling full–duplex transmitter/receiver or transceiver.

The 2B+D data is input to the device at the D_{in} pin of the time division multiplexed data interface. This data is passed through a three frame deep FIFO prior to being formatted and scrambled in the Superframe Framer. The resulting 160 kbps binary data stream is converted to an 80 kbaud dibit stream which is subsequently converted to four analog amplitudes by the DAC (digital–to–analog converter). The resulting pulse amplitude modulated signal is band limited by the Tx Filter prior to entering the Tx Driver which differentially drives the line coupling circuit to the twisted wire pair.

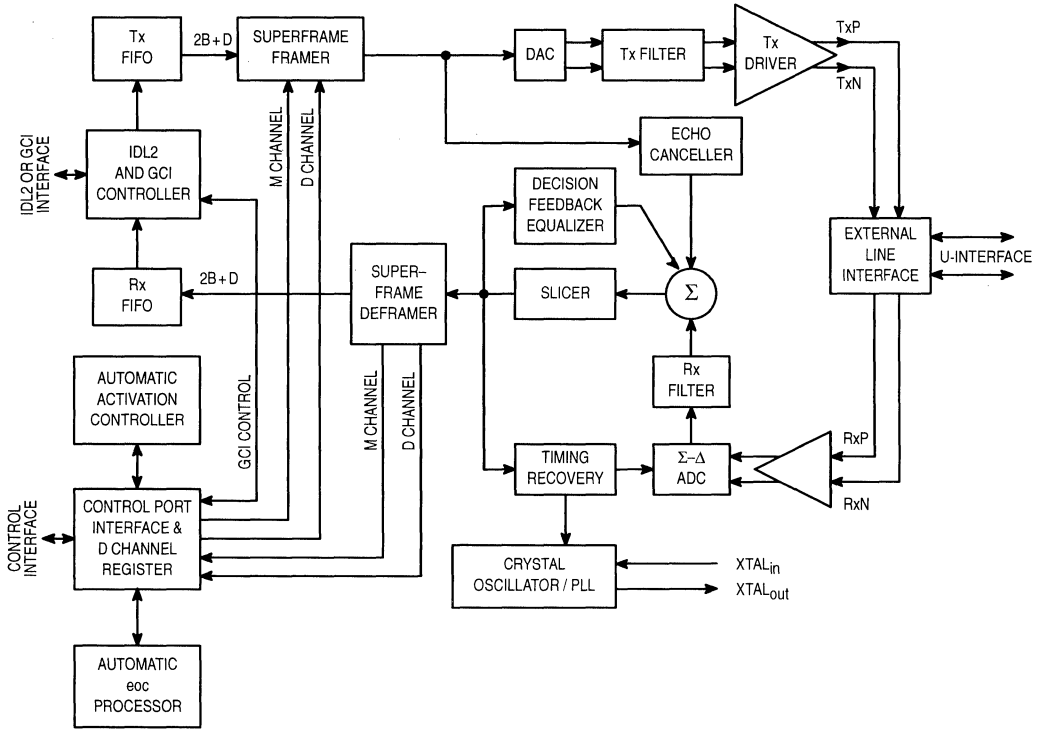


Figure 5. MC145572 Functional Block Diagram

From the twisted wire pair, information from the far end U–Interface Transceiver is coupled through the external line interface circuit to the differential receiver inputs RxP and RxN. (In this two wire environment, the transmitted signal is also coupled into the receiver inputs.) This combined analog signal is converted to a digital word in the Σ–Δ (sigma–delta) ADC (analog–to–digital converter). After filtering, an adaptively generated replica of the transmitted signal, calculated by the echo canceler, is subtracted from the combined signal leaving only the far end signal. In addition, phase distortion present in the far end signal is corrected by the Decision Feedback Equalizer. The resulting four level signal is decoded by the slicer to produce a 160 kbps data stream. Timing information is also recovered from the far end signal. The Superframe Deframer descrambles and disassembles the received superframes and passes the received 2B+D data through a three IDL frame deep FIFO to the IDL Interface where it is available at the D_{out} pin of the time division multiplexed data interface.

The MC145572 permits the designer to select one of three options for control of the device and access to its register set. When operating in MCU mode the MC145572 can be configured for either Serial Control Port or Parallel Control Port mode of operation. In Serial Control Port mode control and status of the device is handled via the Serial Control Port (SCP), a standard four wire serial microcontroller interface. In Parallel Control Port mode the MC145572 is configured to provide an eight bit wide data port with a chip select and read/write pin. In either case the internal register set of the MC145572 gives an external microcontroller access to the 4 kbps Maintenance Channel provided across the U–interface.

When the MC145572 is configured for GCI mode the Command/Indicate channel of the GCI interface is used for control and status messages. The GCI Monitor channel is used to send and receive maintenance channel messages. The Monitor channel also permits the internal registers of the MC145572 to be read from or written to if it is desired to bypass the normal operation of the GCI interface.

The Embedded Operations Channel (eoc) portion of the M–channel can be handled automatically with the internal Automatic eoc Processor. In addition, activation and deactivation of the MC145572 is handled by an Automatic Activation Controller.

The MC145572 requires a single 20.48000 MHz pullable crystal connected between the $XTAL_{in}$ and $XTAL_{out}$ pins. No other external components are required for the crystal oscillator. Internal crystal pulling circuitry adjusts the crystal frequency in both the LT and NT modes of operation.

MC145572/MC14LC5472 COMPATIBILITY

After either a hardware or software reset the MC145572 maintains basic pin function and register compatibility with the MC14LC5472 U–Interface Transceiver when configured for MCU mode and using the Serial Control Port interface. There are differences between the MC14LC5472 and the MC145572 in exact signal requirements and outputs for these pins.

Most software written for the MC14LC5472 will operate the MC145572 without requiring any modifications. The MC145572 has an extended register set which provides access to the on chip timeslot assigner, I/O pin configuration bits, the D Channel, and internal parameters of the device. The extended registers are accessed by setting bits in register BR10 that were reserved bits for the MC14LC5472. The new registers then overlay the original registers and are referred to in this document as Overlay Registers OR0 through OR9, OR12, and OR13. Register BR10 is common to both register sets permitting software to switch between the basic register set and the overlay register set as required.

PIN DESCRIPTION QUICK REFERENCE

Tables 1 through 5 list the MC145572 pins in functional groups and provide brief pin descriptions. For more detailed information, refer to the section indicated in the title.

Table 1. Power Supply and Mode Selection Pins

Pin Name	Pin No.		Pin Description
	TQFP	PLCC	
Power Supply Pins			
V_{DD}	27	44	Positive power supply, nominally + 5 V.
V_{SS}	29, 5	2, 22	Negative power supply, nominally ground.
V_{DD} Rx, V_{DD} Tx	30, 38	3, 11	Positive power supply for analog circuits, nominally + 5 V.
V_{SS} Rx, V_{SS} Tx	31, 37	4, 10	Negative power supply for analog circuits, nominally ground.
V_{DD} I/O	7, 20	24, 37	Positive power supply for input and output circuits, nominally + 5 V.
V_{SS} I/O	6, 19	23, 36	Negative power supply for input and output circuits, nominally ground.
CAP 3V	28	1	Connection for internal 3 V regulator decoupling capacitor.
Mode Selection Pins			
$\overline{RESET}$	41	14	Hardware reset when at a logic low, normal operation when at a logic high. This pin has a Schmitt trigger input.
NT/$\overline{LT}$	42	15	Hardware selection of $\overline{LT}$ (logic low) and NT (logic high) operating mode.
MCU/$\overline{GCI}$	26	43	MCU mode versus GCI mode select input.
PAR/$\overline{SER}$	40	13	Parallel versus serial control port selection. PAR/$\overline{SER}$ = 1 (logic high) for a parallel port. PAR/$\overline{SER}$ = 0 (logic low) for serial control port interfacing.

Table 2. Time Division Multiplex Interface Pins

Pin Name	Pin No.		Pin Description
	TQFP	PLCC	
Time Division Multiplex Data Interface			
M/$\overline{S}$	43	16	Master/Slave mode select input for the IDL2 or GCI interface. Master mode for M/$\overline{S}$=1 (logic high).
FSR/$\overline{FSC}$	10	27	The MCU 8 kHz Frame Sync for data transmitted on the D_{out} pin. In GCI operation, this pin serves as the FSC pin.
FSX	11	28	The MCU 8 kHz frame sync for data input to the D_{in} pin. This pin is not used in GCI mode.
DCL	14	31	MCU bit clock, or GCI 2x bit clock.
D_{out}	13	30	Serial data out of MCU or GCI interface.
D_{in}	12	29	Serial data into MCU or GCI interface.

Table 3. Digital Data Interface Pins

Pin Name			Pin No.		Pin Description
MCU/SCP Mode	MCU/PCP Mode	GCI Mode	TQFP	PLCC	
SCPEN	CS	IN1	4	21	In serial port, MCU mode, $\overline{SCPEN}$ is the active low SCP enable input. In parallel port, MCU mode, $\overline{CS}$ is the active low chip select. In full GCI mode, defined when MCU/$\overline{GCI}$ = 0, this input is IN1.
SCPCLK	R/$\overline{W}$	IN2	3	20	In serial port, MCU mode, SCPCLK is the serial control port clock input. In parallel port, MCU mode, R/$\overline{W}$ is the read versus write indication to the parallel port. In full GCI mode, defined when MCU/$\overline{GCI}$ = 0, this input is IN2.
SCP Rx	D0	OUT1	1	18	In serial port, MCU mode, SCP Rx is the serial control port data input. In parallel port, MCU mode, D0 is the LSB of the parallel data bus. In full GCI mode, defined by MCU/$\overline{GCI}$ = 0, OUT1 is an output reflecting the state of bit 5 as set in BR7.
SCP Tx	D1	OUT2	2	19	In serial port, MCU mode, SCP Tx is the serial control port data output. In parallel port, MCU mode, this is signal D1 of the parallel data bus. In full GCI mode, defined by MCU/$\overline{GCI}$ = 0, OUT2 is an output reflecting the state of bit 6 as set in BR7
IRQ	IRQ	—	44	17	Open–drain active low output for microcontroller interrupt.
4.096 CLKOUT	D2	4.096 CLKOUT	17	34	4.096 MHz clock out. In parallel port, MCU mode, this is signal D2 of the parallel data bus.
15.36 CLKOUT	D3	15.36 CLKOUT	18	35	15.36 MHz clock out. Not synchronized to recovered clock in the NT mode. In parallel port, MCU mode, this is signal D3 of the parallel data bus.
BUF XTAL	D4	BUF XTAL	21	38	This is a square wave output from the 20.48 MHz oscillator and it is not synchronized to the recovered clock in the NT mode. In parallel port, MCU mode, this is signal D4 of the parallel data bus.
EYEDATA DCHCLK	D5	S2	22	39	In serial port MCU mode, this pin may carry either EYEDATA or DCHCLK. In parallel port MCU mode, this is signal D5 of the parallel data bus. In full GCI mode, this pin is the S2 input.
TXBCLK DCH_{in}	D6	$FREF_{out}$	23	40	In serial port MCU mode, this pin may carry either TXBCLK or DCH_{in}. TXBCLK is an 80 kHz clock output, aligned and synchronized to the transmitted baud. DCH_{in} is the D channel port serial data input. In parallel port MCU mode, this is signal D6 of the parallel data bus. In full GCI mode, operating as a GCI slave, this pin provides 2.048 MHz or 512 kHz synchronized clock output.
RXBCLK DCH_{out}	D7	CLKSEL	24	41	In serial port MCU mode, this pin may carry either RXBCLK or DCH_{out}. RXBCLK is an 80 kHz clock output, aligned and synchronized to the received baud. DCH_{out} is the D channel port serial data output. In parallel port MCU mode, D7 is the MSB of the parallel data bus. In full GCI mode, operating as a GCI master, CLKSEL selects between 512 kHz and 2.048 MHz for DCL. CLKSEL = 1 selects 2.048 MHz.
SYSCLK 20.48 MHz SFAR $\overline{TSEN}$	SYSCLK 20.48 MHz SFAR $\overline{TSEN}$	S1	8	25	In either MCU mode, this pin may carry either SYSCLK, 20.48 MHz, SFAR, or $\overline{TSEN}$ outputs. SYSCLK is a 10.24 MHz clock for sampling EYEDATA. SFAR is the receive data superframe alignment output in the NT and LT modes. $\overline{TSEN}$ is an active low open–drain buffer enable output, used for enabling a bus driver to buffer MCU data out from the MC145572, onto a PCM highway. $\overline{TSEN}$ is active only when D_{out} is active. In full GCI mode, this pin is the S1 input.
Tx SFS SFAX	Tx SFS SFAX	S0	9	26	In either MCU mode, this pin may carry either Tx SFS output, or SFAX input/output. When this pin is unused connect a 100 kΩ resistor to V_{SS} in LT mode. Tx SFS is provided for compatibility to the MC145472, which provides an absolute transmit superframe reference. SFAX is the transmit data superframe alignment input in the LT mode, or superframe alignment out put in the NT mode. In LT mode SFAX can also be an output. In full GCI mode, this pin is the S0 input.

Table 4. 2B1Q Interface Pins

Pin Name	Pin No.		Pin Description
	TQFP	PLCC	
TxP, TxN	36, 39	9, 12	Positive and negative outputs of the differential transmit driver.
RxP, RxN	32, 33	5, 6	Positive and negative inputs to the differential receive circuit.
V_{ref} P. V_{ref} N	35, 34	8, 7	Positive and negative signals for internal voltage reference. Connect a 0.1 μF ceramic capacitor between V_{ref}P and V_{ref}N.

Table 5. Phase–Locked Loop and Clock Pins

Pin Name	Pin No.		Pin Description
	TQFP	PLCC	
FREQREF	25	42	LT mode: 8 kHz reference clock input (Schmitt trigger input). NT mode: optional synchronized clock output, selected by control register in the MCU mode (MCU/$\overline{GCI}$ = 1).
$XTAL_{in}$, $XTAL_{out}$	16, 15	33, 32	Input and output signals of the 20.48 MHz crystal oscillator amplifier.

CONTROL INTERFACES

When operated in MCU mode the MC145572 has two configurations that provide MCU access to its internal register set. The Serial Control Port mode is a four wire serial interface that clocks data into or out of the MC145572 at data rates up to 4 Mbps. The Parallel Control Port mode configures the MC145572 to have an eight bit parallel data port that can be located anywhere in processor memory.

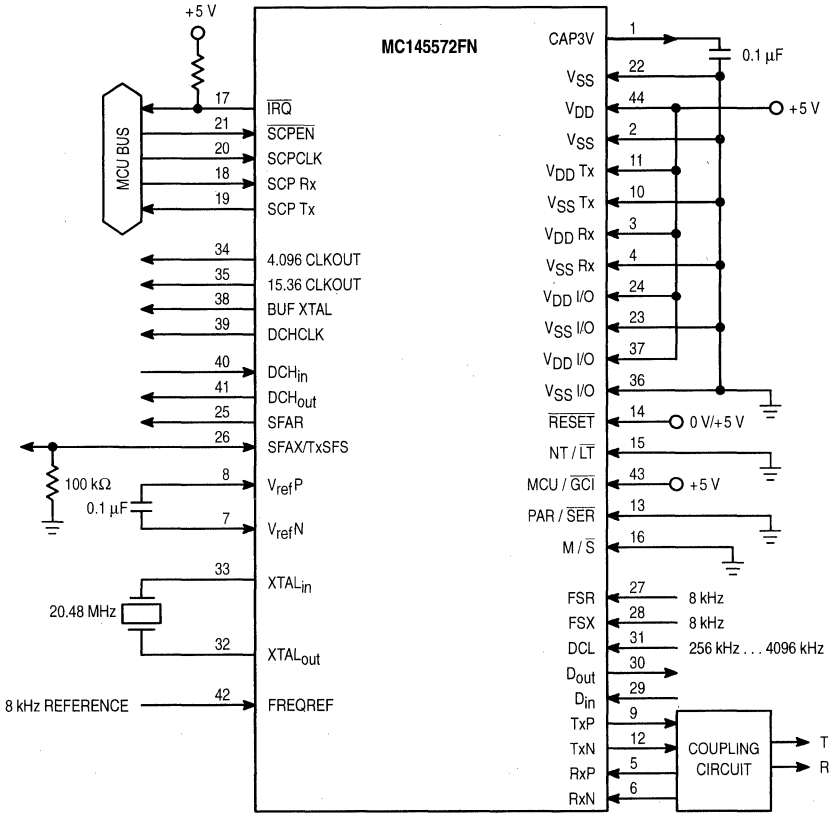
SERIAL CONTROL PORT MODE

The MC145572 is equipped with an industry standard Serial Control Port Interface. The Serial Control Port (SCP) is used by an external controller, such as an M68HC05 family microcontroller, MC145488 Dual Data Link Controller, or MC68302 Integrated Multiprotocol Processor, to communicate with the U–Interface Transceiver.

The SCP is a full–duplex four wire interface with control and status information passed to and from the U–Interface Transceiver. The Serial Control Port Interface consists of a transmit output, a receive input, a data clock, and an enable signal. These device pins are known as SCP Tx, SCP Rx, SCPCLK, and $\overline{SCP\ EN}$, respectively. The SCP Clock determines the rate of exchange of data in both the transmit and receive directions, and the SCP Enable signal governs when this exchange is to take place. The four wire SCP Interface is supplemented with an interrupt request line, $\overline{IRQ}$, for external microcontroller notification of an event requiring service.

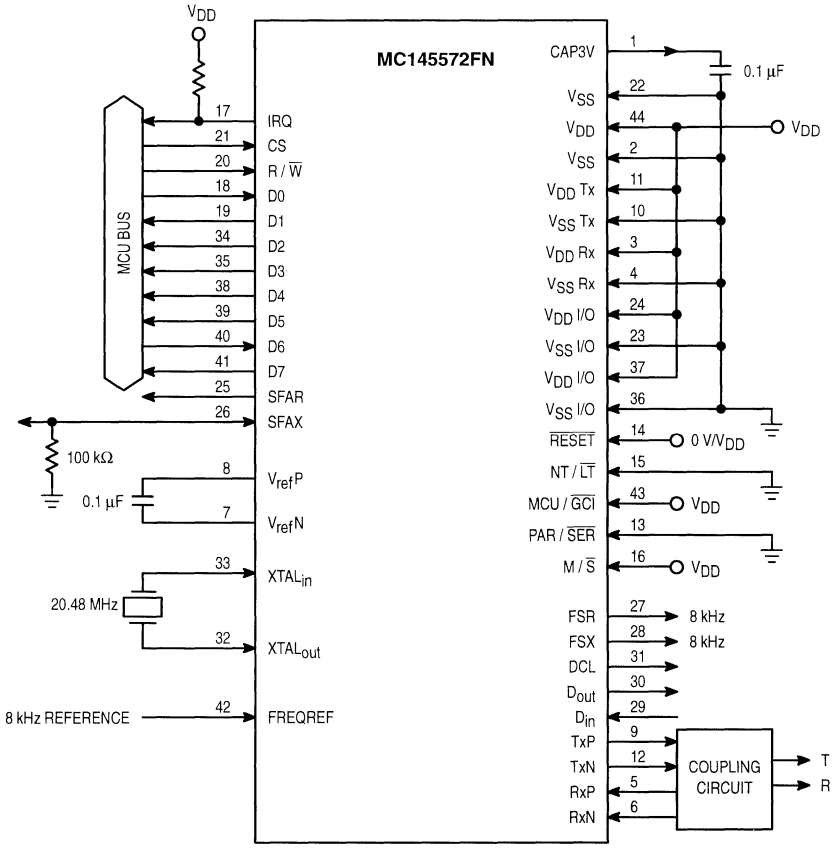
PARALLEL CONTROL PORT MODE

In the Parallel Control Port mode the MC145572 is configured to have a single address /byte wide data port for access to the internal register set. A read/write pin (R/$\overline{W}$) and chip select pin ($\overline{CS}$) are provided to enable read or write accesses to the data port. For an external microcontroller such as the MC68302 to access an individual nibble, byte or overlay register a sequence of write and read operations is required. The first access is always a write cycle that writes a pointer and internal read/write indicator to the MC145572. The pointer byte contains the Nibble or Byte Register address and for the case of Nibble Register writes the data to be written. This initial write may be followed by up to two read accesses or one write access. An open drain $\overline{IRQ}$ output pin is provided for interrupting an external MCU when a change of status is detected by the MC145572. Figure 7 shows pin configurations to operate the MC145572 in MCU mode using the Parallel Control Port for access to the register set.



NOTE: In LT mode the 100 kΩ resistor on SFAX/TxSFS is required when none of these pin functions is enabled.

Figure 6. MCU Mode with Serial Control Port Configuration



NOTE: In LT mode the 100 kΩ resistor on SFAX/TxSFS is required when none of these pin functions is enabled.

Figure 7. MCU Mode with Parallel Control Port Configuration

MCU MODE REGISTER DESCRIPTION REFERENCE

This section describes all of the MC145572 U–Interface Transceiver control and status registers available via the Serial and Parallel Control Ports. Tables 6 through 8 contain Register Maps.

The internal registers of the MC145572 are used when the device is in MCU mode. When in GCI mode, MCU/$\overline{GCI}$ = 0, the MC145572 is controlled via the C/I and monitor channels, and it is not necessary to access the registers in normal applications.

The MC145572 provides a Parallel Control Port interface mode that provides access to all control registers.

The register map for the MC145572 is nearly identical to that for the MC145472 after a hardware or software reset. Reserved bits in the MC145472 register map have been redefined to permit access to new registers in the MC145572. Most software developed for the MC145472 will work for the MC145572 without modifications.

The MC145572 Serial Control Port (SCP) Interface is pin–for–pin identical to that of the MC145474/75 S/T–Interface Transceiver. Using the same interface as the MC145474/75 provides a common interface for applications utilizing both the MC145572 and the MC145474/75 and for applications that can use either device, such as line cards or terminal equipment.

In addition to being pin–for–pin compatible, the architecture of the register map and the SCP Interface is nearly identical to that of the MC145474/75. This simplifies the code development effort and minimizes device driver code size for the microcontroller.

Table 6. Nibble Registers and R6 Map (NR0 – NR5; R6)

	b3	b2	b1	b0
NR0	SOFTWARE RESET	POWER DOWN ENABLE	ABSOLUTE POWER DOWN	RETURN TO NORMAL
NR1	LINKUP	ERROR INDICATION	SUPERFRAME SYNC	TRANSPARENT/ ACTIVATION IN PROGRESS
NR2	ACTIVATION REQUEST	DEACTIVATION REQUEST	SUPERFRAME UPDATE DISABLE	CUSTOMER ENABLE
NR3	IRQ3	IRQ2	IRQ1	IRQ0
NR4	ENABLE IRQ3	ENABLE IRQ2	ENABLE IRQ1	ENABLE IRQ0
NR5	RESERVED	BLOCK B1	BLOCK B2	SWAP B1/B2

	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
R6	eoc a1	eoc a2	eoc a3	eoc dm	eoc i1	eoc i2	eoc i3	eoc i4	eoc i5	eoc i6	eoc i7	eoc i8

Table 7. Byte Register Map (BR0 – BR15A)

	b7	b6	b5	b4	b3	b2	b1	b0
BR0	M40	M41	M42	M43	M44	M45	M46	M47
BR1	M40	M41	M42	M43	M44	M45	M46	M47
BR2	M50	M60	M51	febe INPUT	RESERVED	RESERVED	RESERVED	RESERVED
BR3	M50	M60	M51	RECEIVED febe	COMPUTED nebe	VERIFIED act	VERIFIED dea	SUPERFRAME DETECT
BR4	febe COUNTER 7	febe COUNTER 6	febe COUNTER 5	febe COUNTER 4	febe COUNTER 3	febe COUNTER 2	febe COUNTER 1	febe COUNTER 0
BR5	nebe COUNTER 7	nebe COUNTER 6	nebe COUNTER 5	nebe COUNTER 4	nebe COUNTER 3	nebe COUNTER 2	nebe COUNTER 1	nebe COUNTER 0
BR6	U–LOOP B1	U–LOOP B2	U–LOOP 2B+D	U–LOOP TRANSPAR-ENT	IDL2–LOOP B1	IDL2–LOOP B2	IDL2–LOOP 2B+D	IDL2–LOOP TRANSPARENT
BR7	BR15A SELECT	**GCI IN2**	**GCI IN1**	IDL2 INVERT	IDL2 FREE RUN	IDL2 SPEED	IDL2 M/S INVERT	IDL2 8/10
		OUT2	**OUT1**					
BR8	FRAME STEERING	FRAME CONTROL 2	FRAME CONTROL 1	FRAME CONTROL 0	crc CORRUPT	MATCH SCRAM-BLER	RECEIVE WINDOW DISABLE	NT/LT INVERT
	FRAME STATE 3	FRAME STATE 2	FRAME STATE 1	FRAME STATE 0	RESERVED	RESERVED	RESERVED	NT/LT MODE
BR9	eoc CONTROL 1	eoc CONTROL 0	M4 CONTROL 1	M4 CONTROL 0	M5/M6 CONTROL 1	M5/M6 CONTROL 0	febe/nebe CONTROL	RESERVED
BR11	ACTIVATION CONTROL 6	ACTIVATION CONTROL 5	ACTIVATION CONTROL 4	ACTIVATION CONTROL 3	ACTIVATION CONTROL 2	ACTIVATION CONTROL 1	ACTIVATION CONTROL 0	ACTIVATION TIMER DISABLE
	ACTIVATION STATE 6	ACTIVATION STATE 5	ACTIVATION STATE 4	ACTIVATION STATE 3	ACTIVATION STATE 2	ACTIVATION STATE 1	ACTIVATION STATE 0	ACTIVATION TIMER EXPIRE
BR12	ACTIVATION CONTROL STEER	INTERPO-LATE ENABLE	LOAD ACTIVATION STATE	STEP ACTIVATION STATE	HOLD ACTIVATION STATE	JUMP SELECT	RESERVED	FORCE LINKUP
	EPI 18	EPI 17	EPI 16	EPI 15	EPI 14	EPI 13	EPI 12	EPI 11
BR13	ENABLE MEC UPDATES	ACCUM EC OUTPUT	ENABLE EC UPDATES	FAST EC BETA	ACCUM DFE OUTPUT	ENABLE DFE UPDATES	FAST DFE/ARC BETA	CLEAR ALL COEFF'S
	EPI 10	EPI 9	EPI 8	EPI 7	EPI 6	EPI 5	EPI 4	EPI 3
BR14	RESERVED	ro/wo TO r/w	RESERVED	FRAMER TO DEFRAMER LOOP	± 1 TONES	RESERVED	RESERVED	ENABLE CLKs
BR15	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
	MASK 7	**MASK 6**	**MASK 5**	MASK 4	MASK 3	MASK 2	MASK 1	MASK 0
BR15A	FREQ ADAPT	JUMP DISABLE	RESERVED	RESERVED	ENABLE Tx SFS	RESERVED	RESERVED	EYE DATA ENABLE
				RESERVED	RESERVED	RESERVED	RESERVED	RESERVED

NOTE: Bits in bold type were reserved bits in the MC145472/MC14LC5472 register map.

Table 8. Overlay Register Map (OR0 – OR13)

INIT GROUP REGISTER OVERLAY REGISTERS OR0–OR9, OR11, AND OR12								
	b7	**b6**	**b5**	**b4**	**b3**	**b2**	**b1**	**b0**
OR0	D_{out} B1 CHANNEL TIME SLOT BITS (7:0)							
OR1	D_{out} B2 CHANNEL TIME SLOT BITS (7:0)							
OR2	D_{out} D CHANNEL TIME SLOT BITS (7:0)							
OR3	D_{in} B1 CHANNEL TIME SLOT BITS (7:0)							
OR4	D_{in} B2 CHANNEL TIME SLOT BITS (7:0)							
OR5	D_{in} D CHANNEL TIME SLOT BITS (7:0)							
						GCI Slot (2:0)		
OR6	TSA B1 ENABLE	TSA B2 ENABLE	TSA D ENABLE	GCI SELECT M4–OR0	GCI MODE ENABLE	RESERVED	RESERVED	RESERVED
OR7	RESERVED	RESERVED	$\overline{\text{TSEN}}$ DCH ENABLE	IDL2 RATE2	IDL2 LONGFRAME MODE	CRC CORRUPT MODE	febe/nebe ROLLOVER	M4 TRINAL MODE
OR8	D/R MODE 1	D/R MODE 0	SFAX OUTPUT ENABLE	FREQREF OUTPUT ENABLE	$\overline{\text{TSEN}}$ ENABLE B1, B2	RESERVED	SFAX SFAR ENABLE	D CHANNEL PORT ENABLE
OR9	RESERVED	OPEN FEEDBACK SWITCHES	ANALOG LOOPBACK	CLKOUT 2048	4096 HIRATE	2048 DISABLE	1536 DISABLE	4096 DISABLE
BR10	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	**SELECT DUMP ACCESS**	**SELECT DCH ACCESS**	**SELECT INIT GROUP**
D CHANNEL ACCESS SELECT OVERLAY								
OR12	D CHANNEL TRANSMIT BITS (7:0)							
	D CHANNEL RECEIVE BITS (7:0)							
DUMP/RESTORE ACCESS SELECT OVERLAY								
OR13	DUMP REGISTER WRITE ACCESS (7:0)							
	DUMP REGISTER READ ACCESS (7:0)							

IDL2 TIME DIVISION BUS INTERFACE

The IDL2 Interface consists of six pins: M/$\overline{S}$, FSX, FSR, DCL, D_{in}, and D_{out}. With the M/$\overline{S}$ pin, the IDL2 Interface can be configured as a timing Master (FSR, FSX, and DCL are outputs) or a timing Slave (FSR, FSX, and DCL are inputs). Master or Slave configuration is independent of NT or LT mode selection. The IDL2 Interface receives 2B+D data on the D_{in} pin and buffers it through a FIFO to the U–Interface Superframe Framer. Simultaneously, this block accepts 2B+D data from the U–Interface Superframe Deframer, buffers it through a FIFO, and transmits it out the D_{out} pin. Refer to Figure 5 for a block diagram of the MC145572.

2B+D Data is transferred over the IDL2 interface at an 8 kHz rate. Each IDL2 2B+D frame contains 8 bits of B1 channel data, 8 bits of B2 channel data, and 2 bits of D channel data. The IDL2 interface supports five different frame formats and a time slot assigner. The frame formats are long frame and short frame synchronization each with either 8–bit or 10–bit 2B+D data formats. The fifth frame format is the IDL2 GCI Electrical frame format. In this format only the 2B+D data bits of the GCI interface are accessible by the MC145572. Either the Serial Control Port or the Parallel Control Port must be used for access to the internal register set of the MC145572 when IDL2 operation is enabled.

SHORT FRAME OPERATION

Short frame operation is the same as the IDL interface used on the MC145472 and MC14LC5472 U–Interface Transceivers with one exception. The MC145572 provides for two 8 kHz frame sync pins, FSX and FSR, when operated in IDL2 mode. The FSX pin is used to indicate IDL2 frame synchronization for data input into the D_{in} pin for transmission onto the U–Interface. The FSR pin is used to indicate IDL2 frame synchronization for data recovered from the U–Interface and output to the D_{out} pin. When configured for master mode, the MC145572 drives FSR and FSX simultaneously. When configured for IDL2 slave operation, the MC145572 FSX and FSR inputs can be driven independently. In slave mode, both FSX and FSR can be connected together so a single synchronization signal can be used to drive both inputs.

LONG FRAME OPERATION

When configured for long frame mode the 8 kHz frame sync is active during the 2B+D data transfer. The FSX pin is

used to indicate frame synchronization for data input into the D_{in} pin for transmission onto the U–Interface. The FSR pin is used to indicate frame synchronization for data recovered from the U–Interface and output to the D_{out} pin. When configured for master mode, the MC145572 drives FSR and FSX simultaneously. When configured for IDL2 slave operation, the MC145572 FSX and FSR inputs can be driven independently. In slave mode, both FSX and FSR can be connected together so a single synchronization signal can be used to drive both inputs.

GCI 2B+D OPERATION

By setting OR6(b3), GCI Mode Enable, to a '1' the IDL2 interface is configured to accept GCI interface timing. In this mode only 2B+D data is transferred between the MC145572 and the GCI interface. The other bits in the GCI frame are ignored. Four signal pins are available in this mode: DCL, FSC, D_{in}, and D_{out}. Control and status information for the MC145572 is provided through the Serial Control Port or the Parallel Control Port. DCL is a 2X bit clock, D_{in} accepts data from the IDL2 interface to be transmitted onto the U–Interface, D_{out} transmits data received from the U–Interface onto the IDL2 interface, and FSC is the 8 kHz frame synchronization pulse. D_{out} is driven only when 2B+D data is output from the MC145572. During all other bit times of the GCI frame D_{out} is high impedance. For applications having a multiplexed GCI frame structure, overlay register OR5 bits 2:0 are used to program the active GCI channel in the multiplex.

MCU MODE ACTIVATION AND DEACTIVATION

Activation or start–up is the process U–Interface Transceivers use to initiate a robust full–duplex communications channel. This process, which may be initiated from either the LT or the NT mode U–Interface Transceiver, is a well–defined sequence of procedures during which the training of the equalizers and echo cancelers at each end of the transmission line takes place. Two types of activation, cold start or warm start, may occur. The MC145572 is capable of automatically supporting both types.

Deactivation is the process used to gracefully end communication between the U–Interface Transceivers at each end of the transmission line. Only the LT mode U–Interface Transceiver may initiate a deactivation procedure.

ACTIVATION SIGNALS FOR NT MODE

When configured as an NT, the MC145572 U–Interface Transceiver can transmit any of the signals shown in Table 9.

ACTIVATION SIGNALS FOR LT MODE

When configured as an LT, the MC145572 U–Interface Transceiver can transmit any of the signals shown in Table 10.

ACTIVATION INITIATION

The MC145572 U–Interface Transceiver can be activated in either of two ways. The external microcontroller can explicitly issue Activation Request (NR2(b3) = 1) or the transceiver detects an incoming 10 kHz wake–up tone. An LT configured U–Interface Transceiver searches for an NT sending the TN wake–up tone. An NT configured U–Interface Transceiver searches for an LT sending the TL wake–up tone. In IDL2 mode the Activation in Progress status bit (NR1(b0)) is set to a 1 when an incoming 10 kHz wake–up tone is detected. In either case, Activation Request being set or a wake–up tone being detected, the U–Interface Transceiver proceeds with activation automatically and signals the result of the activation to the external microcontroller by setting status bits in NR1 to $B.

Table 9. NT Mode Activation Signals

Information Station	Description
TN	A 10 kHz tone consisting of alternating four +3 quats followed by four –3 quats for a time period of 6 frames.
SN0	No signal transmitted.
SN1	Synchronization word present, no superframe synchronization word (ISW), and 2B+D+M = 1.
SN2	Synchronization word present, no superframe synchronization word (ISW), and 2B+D+M = 1.
SN3	Synchronization word present, superframe synchronization word (ISW) present. M channel bits active. Transmitted 2B+D data operational when act n M4 bit = 1. When act n M4 = 0, transmitted 2B+D data = 1.

Table 10. LT Mode Activation Signals

Information Station	Description
TL	A 10 kHz tone consisting of alternating four + 3 quats followed by four – 3 quats for a time period of 2 frames.
SL0	No signal transmitted.
SL1	Synchronization word present, no superframe synchronization word (ISW), and 2B+D+M = 1.
SL2	Synchronization word present, superframe synchronization word (ISW) present, 2B+D = 0, and M = Normal.
SL3	Synchronization word present, superframe synchronization word (ISW) present. M channel bits active. Transmitted 2B+D data operational when M4 act bit = 1. When M4 act = 0, transmitted 2B+D data = 0.

NT DEACTIVATION PROCEDURES AND WARM START

ANSI T1.601 specifies that the NT cannot initiate deactivation. The MC145572 deactivates to a warm start condition when Deactivation Request (NR2(b2)) is set to 1 prior to the LT deactivating the U–Interface. This should be done in response to the M4 channel dea bit being received as 0 by the NT when the loop is active. If Deactivation Request (NR2(b2)) is not set to 1 before the LT deactivates the U–Interface, the MC145572 deactivates to a cold start condition and gives an error indication interrupt. Deactivation Request is automatically set if the M4 maintenance bits are operated with automatic verification of activation and deactivation. See BR9(b5:b4) and OR7(b0) for more information.

LT DEACTIVATION PROCEDURES

ANSI T1.601 specifies that only the LT can deactivate the U–Interface. This is done in the MC145572 by setting Deactivation Request (NR2(b2)) to 1.

Prior to deactivating, the LT should notify the NT of the pending deactivation by clearing the M4 channel dea bit towards the NT for at least three superframes. Then, deactivate the LT by setting Deactivation Request (NR2(b2)) to a 1.

MCU MODE MAINTENANCE CHANNEL OPERATION

When configured for MCU mode operation the MC145572 provides a very flexible interface to the 4 kbps maintenance channel (M–channel) defined in ANSI T1.601–1992. The M–channel consists of 48 bits sent by both the LT and NT configured U–Interface Transceivers during the course of a superframe. These 48 bits are divided into six subchannels designated M1 through M6, each consisting of eight bits per superframe. The Embedded Operations Channel (eoc) consists of M1, M2, and M3. The overhead bits, such as crc, febe, act, and dea, are contained in subchannels M4, M5, and M6.

An external microcontroller can read from or write to the M–channel via the SCP or PCP Interfaces. Interrupts to an external microcontroller can be enabled when an eoc, M4, M5, or M6 channel register is updated. M–channel registers can be configured to update when a new value is detected between successive superframes, when a bit changes, or when two or three successive superframes of a new value are detected. The M4 channel act bit, BR1(b7), can also be configured to automatically enable or disable customer data when in NT or LT mode of operation. The M4 channel dea bit, BR1(b6), can also be configured to automatically issue a deactivation request in NT mode of operation. The M–channel registers are updated only when Superframe Sync, NR1(b1), is set to 1.

GCI MODE FUNCTIONAL DESCRIPTION

The MC145572 is configurable for General Circuit Interface or GCI operation. GCI is a time divison multiplex bus that combines the ISDN 2B+D data and control/status information onto four signal pins. There are two clocks per data bit and a single frame synchronization pulse, FSC.

In GCI mode the MC145572 supports the full set of commands and indications over the Command/Indicate channel. The monitor channel is used for sending and receiving maintenance channel messages and accessing the internal MC145572 registers.

As a GCI slave the MC145572 accepts clock frequencies between 512 kHz and 8.192 MHz. As a GCI master the MC145572 operates at either 512 kHz or 2.048 MHz. Figure 8 is a typical configuration for the MC145572 in GCI mode. The MC145572 is configured for GCI operation when the MCU/GCI pin is tied low. The PAR/SER pin is a don't care but must be tied either high or low.

Table 11. C/I Channel Commands and Indications

C/I Codeword				LT Mode	LT Mode	NT Mode	NT Mode
b4	b3	b2	b1	Command	Indication	Command	Indication
0	0	0	0	DR	–	–	DR
0	0	0	1	RES	DEAC	RES	–
0	0	1	0	LTD2	–	NTD2	–
0	0	1	1	LTD1	–	NTD1	–
0	1	0	0	–	RSY	–	RSY
0	1	0	1	–	EI2	–	EI2
0	1	1	0	–	–	–	–
0	1	1	1	UAR	UAI	–	–
1	0	0	0	AR	AR	AR	AR
1	0	0	1	–	–	–	–
1	0	1	0	ARL	–	–	ARL
1	0	1	1	–	–	–	–
1	1	0	0	–	AI	AI	AI
1	1	0	1	–	–	–	–
1	1	1	0	–	–	–	AIL
1	1	1	1	DC	DI	DI	DC

NOTES:

AI Activation indication
ARL Activation request with local analog loopback
DEAC Deactivation request accepted
DR Deactivation request
LTD1 (LT mode), NTD1 (NT mode) Sets pin "OUT1" high when command is active.
RES Reset
UAI U–Only activation indication
AR Activation request
DC Deactivation confirm
DI Deavtivation indication
EI2 Error indication
LTD2 (LT mode), NTD2 (NT mode) Set pin "OUT2" high when command is active.
RSY Loss of sync – resync. requested
UAR U–Only activation request

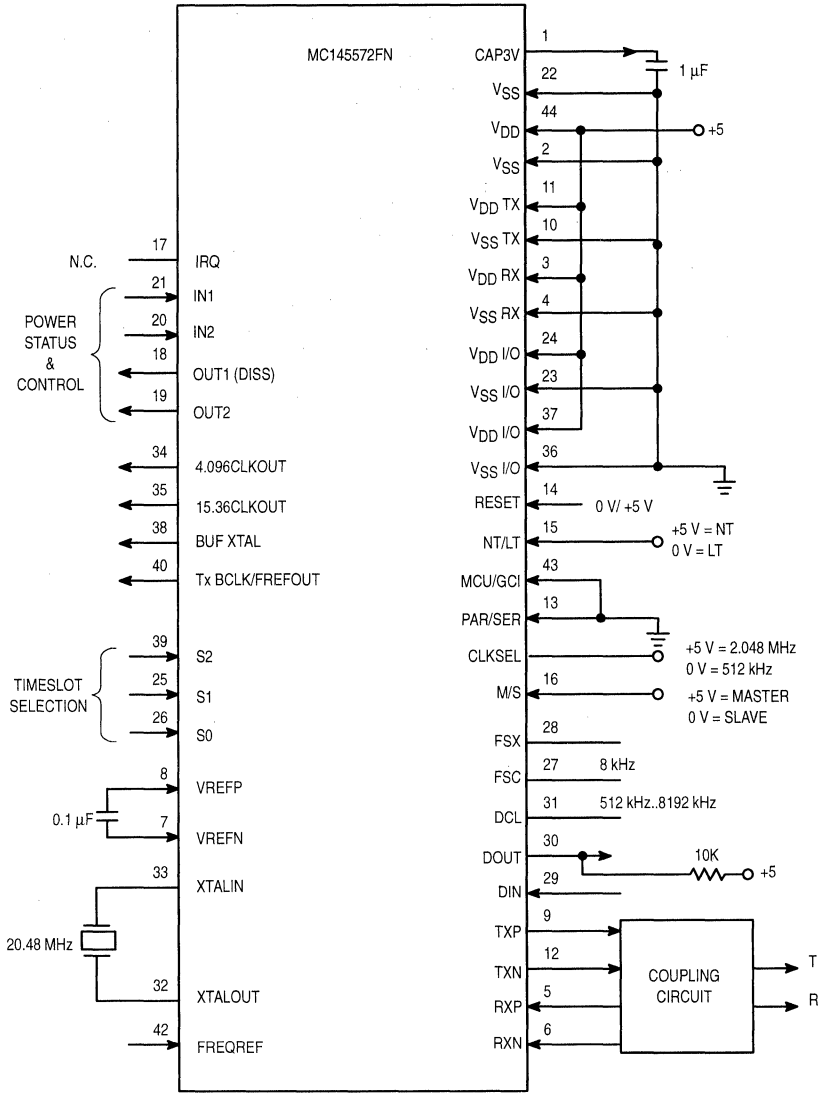
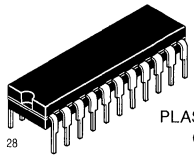


Figure 8. MC145572 Configuration for GCI Operation

MC145574



P SUFFIX
PLASTIC PACKAGE
CASE 736B

FTB SUFFIX
TQFP
CASE 837A

ORDERING INFORMATION

MC145574P	Plastic Package
MC145574FTB	TQFP

2

Technical Summary

ISDN S/T Interface Transceiver

This technical summary provides an overview of the MC145574 S/T interface transceiver. A complete data booklet with comprehensive technical information is available and can be ordered through your Motorola Sales Office.

The MC145574 is Motorola's second generation S/T transceiver and is a follow–on to the MC145474/75 transceiver. It is intended to provide the improved interfacing capabilities and reduced power consumption required by today's ISDN applications while maintaining the functionality and extended range performance of the MC145474/75.

The MC145574 provides an economical VLSI layer 1 interface for the transportation of two 64 kbps B channels and one 16 kbps D channel between the network termination (NT) and terminal equipment applications (TEs). The MC145574 conforms to CCITT I.430 and ANSI T1.605 specifications. The MC145574 provides the modulation/line drive and demodulation/line receive functions required of the interface. In addition, the MC145574 provides the activation/deactivation, error monitoring, framing, bit, and octet timing. The MC145574 provides the control signals for the interface to the layer 2 devices. Complete multiframe capability is provided.

The MC145574 features the interchip digital link (IDL2) for the exchange of the 2B+D channel information between ISDN components and systems. The MC145574 provides an industry standard serial control port (SCP) to program the operation of the transceiver. As an alternative to IDL+SCP combination, the general circuit interface (GCI) is provided.

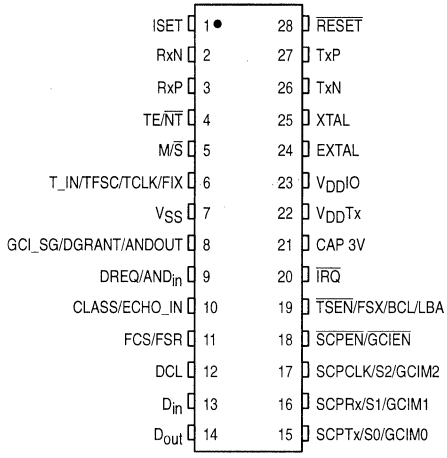
The MC145574 is not pin compatible with the MC145474/75 but it is intended to have a compatible register set and be fully compatible with current application software; however, to make full use of the additional MC145574 features software, modifications will be required.

- Three Selectable Resolutions: 320 (CGA), 480 (EGA), or 640 (VGA) Dots per Line
- Conforms to CCITT I.430 and ANSI T1.605 Specifications
- Register/Software Compatible with the First Generation MC145474/75
- Pin Selectable NT or TE Modes of Operation
- Incorporates the IDL2, with Timeslot Assigner
- Industry Standard Microprocessor SCP
- Features GCI Interface
- Supports 2.5:1 Transformers for Transmit and Receive
- Exceeds the Recommended Range of Operation in all Configurations
- Complete Multiframing Capability Supported (SC1 – SC5 and Q Channel)
- Optional B Channel Idle, Invert, or Exchange
- Supports Full Range of S/T and IDL Loopbacks
- Supports Transmit Power Down, Listening, and Absolute Minimum Power Mode
- Supports Crystal or External Clock Input Mode
- NT Star and NT Terminal Modes Supported
- Low Power Consumption
- Compatible with 3 V Devices

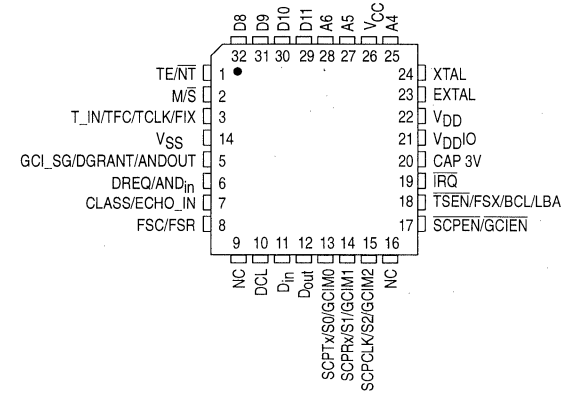
REV 0
10/95

PIN ASSIGNMENTS

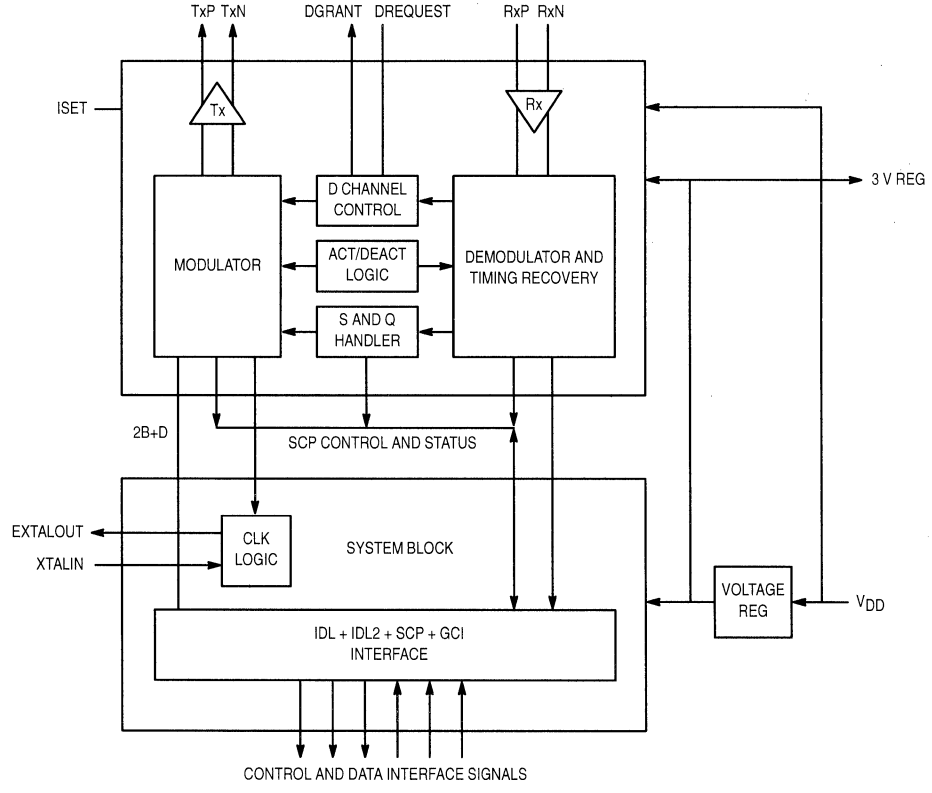
MC145574
PDIP PACKAGE



MC145574
TQFP



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	– 0.5 to + 7	V
V_{in}	Input Voltage	V_{SS} – 0.3 to V_{DD} + 0.3	V
I	DC Current (Any Pin Excluding V_{DD}, $V_{DD}IO$, CAP 3V, V_{SS}, TxP, and TxN)	± 10	mA
T_A	Operating Temperature Range	– 40 to + 85	°C
T_{stg}	Storage Temperature Range	– 85 to + 150	°C

NOTE: Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description section.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

2

DIGITAL DC ELECTRICAL CHARACTERISTICS (T_A = – 40 to + 85°C, V_{DD} = 5.0 V ± 5%, Voltages referenced to V_{SS})

Characteristic	Symbol	Min	Max	Unit
Input High Voltage	V_{IH}	2.0	—	V
Input Low Voltage	V_{IL}	—	0.8	V
Input Leakage Current @ 5.25 V	I_{in}	—	5	µA
High Impedance Input Current @ 4.5/0.5 V	Ilkg(Z)	—	10	µA
Input Capacitance	C_{in}	—	10	pF
Output High Voltage (I_{OH} = – 400 µA)	V_{OH}	2.4	—	V
Output Low Voltage (I_{OL} = 5.0 mA)	V_{OL}	—	0.4	V
XTAL Input High level	$V_{IH(X)}$	3.0	—	V
XTAL Input Low level	$V_{IL(X)}$	—	0.5	V
EXTAL Output Current (V_{OH} = 4.6 V)	$I_{OH(X)}$	—	– 400	µA
EXTAL Output Current (V_{OL} = 0.4 V)	$I_{OL(X)}$	—	400	µA
IRQ Output Low Current (V_{OL} = 0.4 V)		—	2	mA
IRQ Output Off State Impedance		100	—	kΩ

ANALOG CHARACTERISTICS (T_A = – 40 to + 85°C, V_{DD} = 5.0 V ± 5%, Voltages referenced to V_{SS})

Characteristic	Min	Typ	Max	Unit
TxP/TxN Drive Current: R_L = 50 Ω	5.4	6.0	6.6	mA
(TxP – TxN) Voltage Limit	—	—	1.17	Vpeak
Rx Input Sensitivity, Normal Mode (RxP – RxN)	90	—	—	mVpeak
Rx Input Sensitivity, Sleep Mode (RxP – RxN)	220	—	—	mVpeak
Voltage Regulator	3.0	3.2	3.4	V

POWER DISSIPATION (T_A = – 40 to + 85°C, V_{DD} = 5.0 V ± 5%, Voltages referenced to V_{SS} and $V_{DD}IO$ connected to V_{DD})

Characteristic	Min	Typ	Max	Unit
DC Supply Voltage	4.75	5	5.25	V
Worst Case Power Consumption	—	—	90	mW
Transmit Power Down	—	—	70	mW
Sleep Mode	—	—	4	mW
Absolute Minimum Power Down	—	—	2	mW

IDL TIMING CHARACTERISTICS (IDL SLAVE) (T_A = – 40 to + 85°C, V_{DD} = 5.0 V ± 5%, Voltages referenced to V_{SS})

Reference Number	Characteristic	Min	Max	Unit
1	Time Between Successive FSRs	Note 1		
2	FSR Active After DCL Falling Edge (Hold Time)	30	—	ns
3	FSR Active Before DCL Falling Edge (Setup Time)	30	—	ns
4	DCL Period	Note 2		
5	DCL Width High	45	55	% of DCL Period
6	DCL Width Low	45	55	% of DCL Period
7	DIN Valid Before DCL Falling Edge (Setup Time)	30	—	ns
8	DIN Valid After DCL Falling Edge (Hold Time)	30	—	ns
9	DOUT Time to High–Impedance	—	30	ns
10	DOUT High–Impedance to Active State	—	70	ns
11	DCL to DOUT Active	—	70	ns

NOTES:
1. FSR is an 8 kHz signal.
2. DCL input frequency can be run from 512 kHz to 4.096 MHz.

IDL TIMING CHARACTERISTICS (IDL MASTER WITH THE IDL DCL RATE SET TO 2.56 MHz)
(T_A = – 40 to + 85°C, V_{DD} = 5.0 V ± 5%, Voltages referenced to V_{SS})

Reference Number	Characteristic	Min	Max	Unit
1	Time Between Successive FSRs	Note 1		
2	FSR Active After DCL Falling Edge (Hold Time)	—	30	ns
3	FSR Active Before IDL DCL Falling Edge (Setup Time)	—	30	ns
4	DCL Period	Note 2		
5	DCL Width High	Note 2		
6	DCL Width Low	Note 2		
7	DIN Valid Before DCL Falling Edge (Setup Time)	30	—	ns
8	DIN Valid After DCL Falling Edge (Hold Time)	30	—	ns
9	DOUT Time to High–Impedance	0	30	ns
10	DOUT High–Impedance to Active State	—	45	ns
11	DCL to DOUT Active	—	45	ns

NOTES:
1. FSR is an 8 kHz signal.
2. DCL output frequency can be programmed at 512 kHz, 2.048 MHz, or 2.56 MHz.

SCP TIMING CHARACTERISTICS (T_A = – 40 to + 85°C, V_{DD} = 5.0 V ± 5%, Voltages referenced to V_{SS})

Reference Number	Characteristic	Min	Max	Unit
12	$\overline{\text{SCP EN}}$ Active Before Rising Edge of SCP CLK	50	—	ns
13	SCP Rising Edge Before $\overline{\text{SCP EN}}$ Active	50	—	ns
14	SCP Rx Valid Before SCP CLK Rising Edge (Setup Time)	20	—	ns
15	SCP Rx Valid After SCP CLK Rising Edge (Hold Time)	20	—	ns
16	SCP CLK Period (Note 1)	244	—	ns
17	SCP CLK Width (Low)	30	—	ns
18	SCP CLK Width (High)	30	—	ns
19	SCP Tx Active Delay	—	50	ns
20	$\overline{\text{SCP EN}}$ Active to SCP Tx Active	—	50	ns
21	SCP CLK Falling Edge to SCP Tx High–Impedance	—	40	ns
22	$\overline{\text{SCP EN}}$ Inactive Before SCP CLK Rising Edge	50	—	ns
23	SCP CLK Rising Edge Before $\overline{\text{SCP EN}}$ Inactive	50	—	ns
24	SCP CLK Falling Edge to SCP Tx Valid Data	—	50	ns

NOTE:
1. Maximum SCP Clock Frequency is 4.096 MHz.

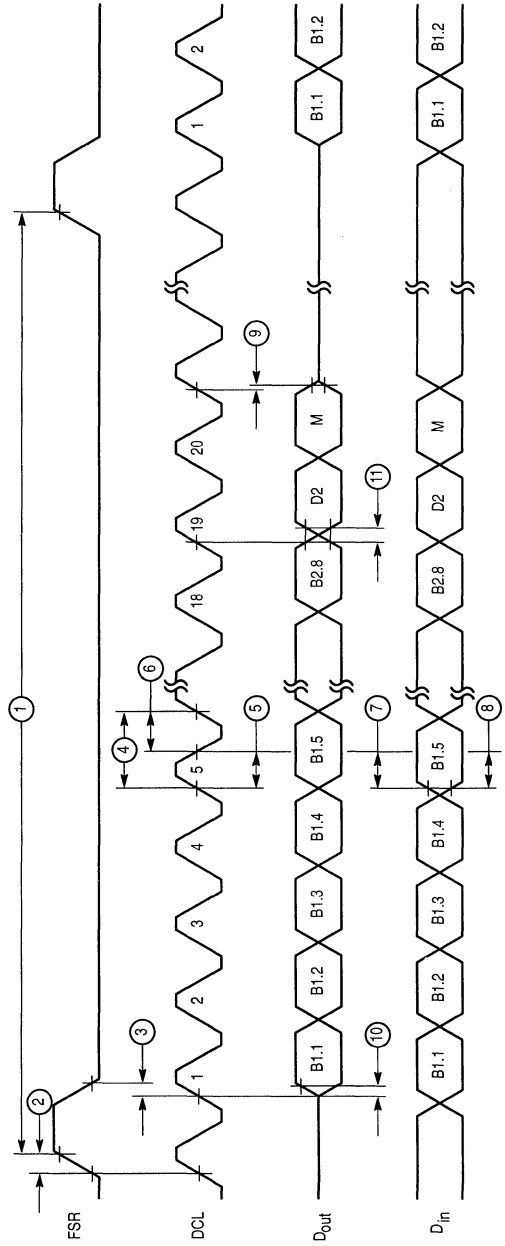
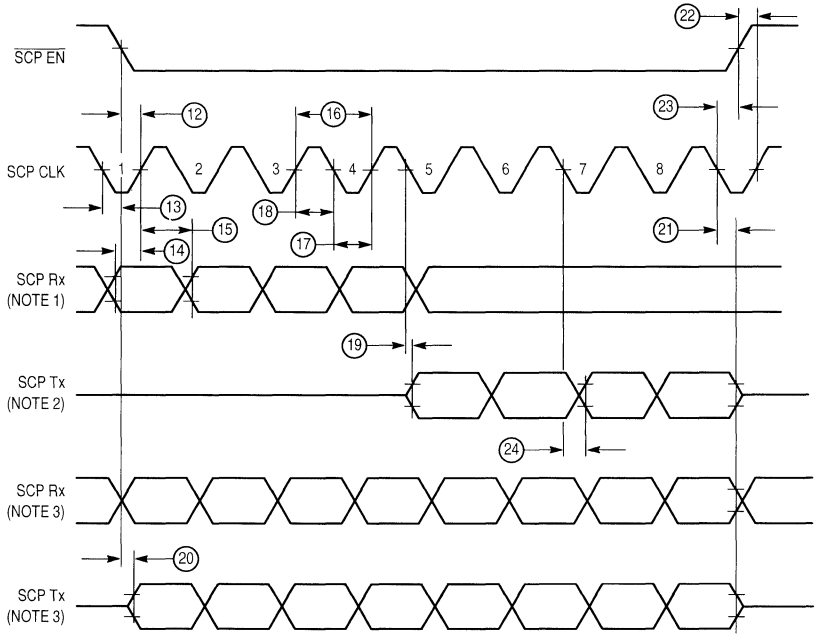


Figure 1. IDL Timing Characteristics



NOTES:

1. During a nibble read, four bits are presented on SCP Rx.
2. During a nibble read, SCP Tx will be active for the duration of the 4–bit transmission as shown.
3. During a byte read, eight bits are presented on SCP Rx. A byte transaction consists of two 8–bit exchanges. During the second 8–bit exchange, data is either written to the byte from SCP Rx or is read from the byte. If the operation is a read operation, then data is presented onto SCP Tx. Refer to "The Serial Control Port" section for a detailed description.

Figure 2. SCP Timing Characteristics

GCI TIMING CHARACTERISTICS (GCI SLAVE) (T_A = – 40 to + 85°C, V_{DD} = 5.0 V ± 5%, Voltages referenced to V_{SS})

Reference Number	Characteristic	Min	Max	Unit
1	Time Between Successive FSCs	Note 1		
2	FSC Active After DCL Falling Edge (Hold Time)	30	—	ns
3	FSC Active Before DCL Falling Edge (Setup Time)	70	—	ns
4	DCL Period	Note 2		
5	DCL Width High	45	55	% of DCL Period
6	DCL Width Low	45	55	% of DCL Period
7	DIN Valid Before DCL Falling Edge (Setup Time)	30	—	ns
8	DIN Valid After DCL Falling Edge (Hold Time)	50	—	ns
11	DCL to DOUT Active	—	70	ns

NOTES:
1. FSC is an 8 kHz signal.
2. DCL input frequency can be run from 512 kHz to 4.096 MHz.

GCI TIMING CHARACTERISTICS (GCI MASTER WITH THE GCI DCL RATE SET TO 2.048 MHz)
(T_A = – 40 to + 85°C, V_{DD} = 5.0 V ± 5%, Voltages referenced to V_{SS})

Reference Number	Characteristic	Min	Max	Unit
1	Time Between Successive FSCs	Note 1		
2	FSC Active After DCL Falling Edge (Hold Time)	—	30	ns
3	FSC Active Before DCL Falling Edge (Setup Time)	—	30	ns
4	DCL Period	Note 2		
5	DCL Width High	Note 2		
6	DCL Width Low	Note 2		
7	DIN Valid Before DCL Falling Edge (Setup Time)	30	—	ns
8	DIN Valid After DCL Falling Edge (Hold Time)	50	—	ns
11	DCL to DOUT Active	—	70	ns

NOTES:
1. FSC is an 8 kHz signal.
2. DCL output frequency can be programmed at 512 kHz, 1.536 MHz, or 2.048 MHz.

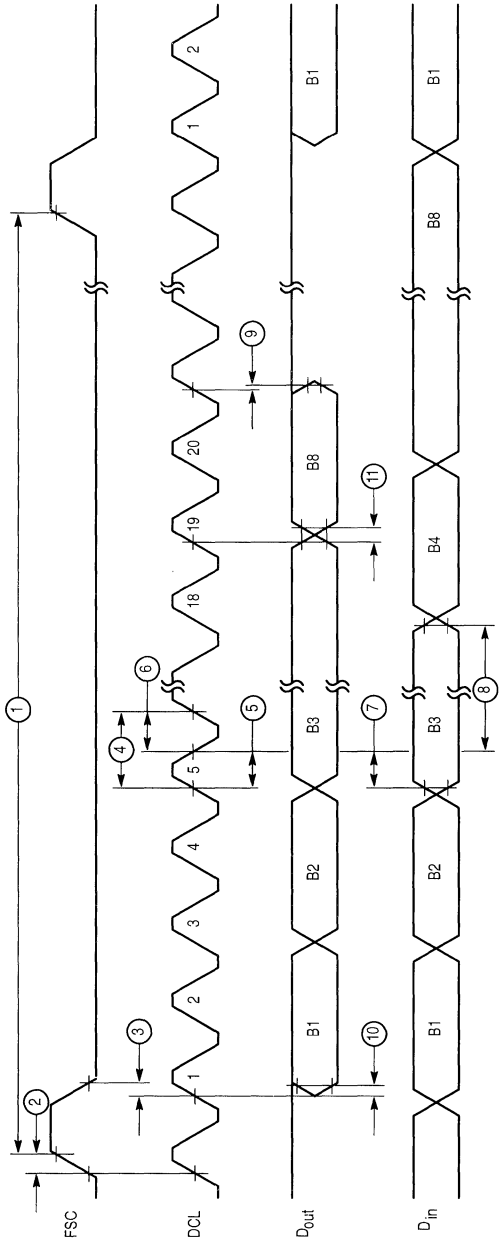


Figure 3. GCI Timing Characteristics

NT1 STAR MODE TIMING CHARACTERISTICS

NT1 STAR MODE OF OPERATION

A wiring configuration which may be used to support multiple T interfaces is known as the "NT1 Star Mode of Operation." This mode of operation is supported by the MC145574. Note that the NT1 Star mode contains multiple NTs. Each of these NTs can be connected to either a passive bus (short, extended, or branched) or to a single TE.

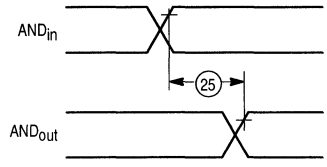


Figure 4. NT1 Star Mode

2

Table 1. D Channel Timing Characteristics (IDL Mode)

Reference Number	Characteristic	Min	Max	Unit
25	Propagation Delay from AND_{in} to AND_{out}	—	30	ns
26	DREQUEST Valid Before Falling Edge of FSR	30	—	ns
27	DREQUEST Valid After Falling Edge of FSR	30	—	ns
28	DGRANT Valid Before Falling Edge of FSR	390	—	ns

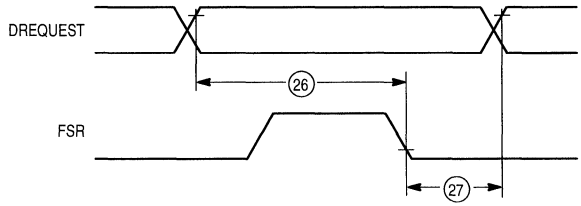


Figure 5. D Channel Request Timing

PIN DESCRIPTIONS

$V_{SS(A)}$ (Pin 1)

This pin provides the signal ground to the PLL circuitry. Analog ground for PLL is separated from digital ground for optimal performance.

ISET

This pin normally performs the ISET function and should have an external resistor connected to ground. The resistor should have a value of 30 kΩ ± 5%.

RxN, RxP

These two pins form the differential receiver for the S/T Interface. They are connected to the S/T loop via a transformer.

TE/$\overline{NT}$

This pin allows the external selection of NT or TE mode. When this pin is held low NT mode is selected and when held high TE mode.

This pin is OR'd with an SCP register bit enabling TE/NT selection to be made in software.

M/$\overline{S}$

This pin allows the external selection of mode for the IDL and GCI interface. This pin functions in both NT and TE modes. When this pin is held low, SLAVE mode is selected and when held high, MASTER mode.

This pin is OR'd with an SCP register bit enabling MASTER/SLAVE selection to be made in software.

T_IN/TFSC/TCLK/FIX

This pin performs four functions dependent on the mode of operation. In all NT modes, except NT Terminal mode, this pin is the FIX input and enables the device to differentiate between fixed and adaptive timing modes. When this pin is held low, ADAPTIVE timing is selected and when held high, FIXED timing. This pin is OR'd with an SCP register bit enabling FIXED/ADAPTIVE selection to be made in software.

In the NT terminal mode this pin is the T_IN input. T_IN is an IDL input port that will accept B1, B2, and D Data. Please refer to the NT Terminal section for further details. In the NT Terminal mode, the FIX function is controlled via an SCP register bit.

In TE SLAVE mode this pin outputs TFSC. TFSC is an 8 kHz frame clock that is synchronized to the received S/T Interface and can be used as the synchronization source in the NT–2 slave–slave mode. Alternatively, this pin can output TCLK, selected via the SCP. TCLK is a clock, whose frequency can be chosen via the SCP, which is synchronized to the received S/T Interface. TCLK can be used as an alternative to TFSC in NT–2 slave–slave mode.

V_{SS}

This is the most negative power supply and digital logic ground. It is normally 0 V.

GCI_SG/DGRANT/AND_{out}

This pin performs three functions dependent on the mode of operation. In NT Star mode it is the AND_{out} output function for use in NT Star applications.

In the TE Master and NT Terminal modes, this pin is the DGRANT output function used for gaining D–Channel access.

In GCI TE Master, this pin is GCI_SG and indicates Stop/Go access to the D–Channel.

DREQUEST/AND_{in}

This pin performs three functions dependent on the mode of operation. In NT Star mode, it is the AND_{in} input function for use in NT Star applications.

In the TE Master and NT Terminal modes, this pin is the DREQUEST input used for requesting D–Channel access.

In all other modes, this input has no defined function and should be tied to V_{SS}.

CLASS/ECHO_IN

This pin performs two functions dependent on the mode of operation. In NT Star mode, it is the ECHO_IN input function for use in NT Star applications.

In the TE Master mode, this pin is the CLASS input used to determine the D–Channel access class.

In all other modes, this input has no defined function and should be tied to V_{SS}.

FSR/FSC

This pin is bidirectional, the direction depending on whether the device is to be a timing master or slave to the IDL/GCI interface. In either case, this pin should be driven with or drive an 8 kHz frame sync signal. In GCI mode this pin is called FSC. In IDL mode this pin is called FSR.

This pin is also the frame sync signal for the IDL receive direction (FSR) when independent frame sync's have been enabled via the SCP interface.

DCL

This pin is the clock pin for the IDL/GCI interface and will be either an input or an output depending on whether the interface is operating as a slave or a master.

D_{in}

This pin is the data input pin for the IDL/GCI.

D_{out}

This pin is the data output pin for the IDL/GCI.

SCPTx/GCI_S0/GCI_M0

This pin has three functions. It is the data output pin, SCPTx, in SCP mode. It is a time slot select input pin, GCI_S0, in GCI slave mode. It is a mode select pin, GCI_M0, in GCI master mode.

SCPRx/GCI_S1/GCI_M1

This pin has three functions. It is the data input pin, SCPRx, in SCP mode. In GCI slave mode it is a time slot select input pin, GCI_S1, and it is a mode select pin, GCI_M1, in GCI master mode

SCPCLK/GCI_S2/GCI_M2

This pin has three functions. It is the clock input pin, SCPCLK, in SCP mode. In GCI Slave mode, it is a time slot select input pin, GCI_S2. In GCI Master mode, it is a mode select pin, GCI_M2.

$\overline{SCPEN}$/GCIEN

This pin has two functions. It is the SCP enable pin, $\overline{SCPEN}$, in SCP mode. In GCI mode, it is the GCI enable pin,

$\overline{\text{GCIEN}}$. Please refer to the section on GCI for details on how the device enters GCI mode.

$\overline{\text{TSEN}}$/FSX/BCL/LBA

This pin is initially high impedance but can be programmed to have three separate functions. The $\overline{\text{TSEN}}$ signal is enabled via the SCP. This pin then becomes an open drain output that pulls low when data is being output from DOUT. This signal can then be used to enable an external driver in applications where the IDL data goes off board, PBX's, etc.

In IDL mode it can also be used as the 8 kHz frame sync, FSX, for the transmit path. In this mode the pin is bidirectional, the direction depending on whether the device is an IDL master or slave. FSX only operates when dual frame sync mode has been enabled via the SCP.

In GCI mode this pin is an output clock, BCL. BCL is a bit rate clock that is half the frequency of the DCL clock and is synchronous with FSC. This clock can be used as the data clock for standard devices such as a codec.

LBA is the default function for both the IDL and GCI modes. This pin is initially an output, LBA, Loopback Active. The LBA pin is normally low but when a loopback is activated within the device, this pin will toggle transition to a high during the time that the loopback is enabled. This pin can be redefined by writing to internal registers within the device.

$\overline{\text{IRQ}}$

This pin is an open drain output that pulls low when the device wants to inform the µP that a status change has occurred. This pin returns to high impedance after clearing the interrupt condition via the SCP.

CAP 3V

This pin is the 3 V regulated supply output used to power the internal digital circuitry.

V_{DDIO}

This is the positive supply pin for the output drivers. This pin should be connected to V_{DD} if 5 V drivers are required or the 3 V regulator output, CAP 3V, if 3 V drivers are required. For further information, refer to the section on Power Supply Strategy.

V_{DD}

This is the positive supply pin and is normally 5 V ± 5%.

This pin should have a capacitor of 100 nF connected to ground. For further information refer to section on Power Supply Strategy.

EXTAL

This pin should be connected to the external 15.36 MHz crystal using the circuit defined in the T1 specification.

XTAL

This pin should be connected to an external 15.36 MHz crystal using the circuit defined in the T1 specification or alternatively, it can be driven by a 15.36 MHz clock source.

TxN, TxP

These two pins form a differential output driver that will connect to the S/T interface via a transformer.

$\overline{\text{RESET}}$

This pin is always an input and is the reset pin for the device and is active low. When this pin is held low, a hardware reset is applied and the device is held in the deactivated state. At the initial application of power, the T2 should be reset. This pin is a Schmitt–trigger input and could have an external RC circuit connected to perform the power on reset function.

ADDITIONAL NOTES

Input Levels

The MC145574 S/T transceiver is always TTL/CMOS level compatible on all digital input pins.

SCP HIDOM

The MC145574 S/T transceiver has the capability of forcing all outputs (both analog and digital) to the high impedance state. This feature, known as the "serial control port high impedance digital output mode," is provided to allow "in circuit" testing of other circuits or devices resident on the same PCB without requiring the removal of the MC145574.

The SCP HIDOM mode is entered by holding $\overline{\text{SCPEN}}$ low for a minimum of 33 consecutive rising edges of the SCP CLK while SCP Rx is high. If $\overline{\text{SCPEN}}$ goes high, or if SCP Rx goes low, the device will exit the SCP HIDOM mode and return to normal operation.

WIRING CONFIGURATIONS

INTRODUCTION

The MC145574 ISDN S/T transceiver conforms to CCITT I.430 and ANSI T1.605 specifications. It is a layer 1 S/T transceiver designed for use at the S and T reference points. It is designed for both point–to–point and multipoint operation. The S/T transceiver is designed for use in either the network terminating (NT) mode or in terminal endpoint (TE) applications. Two 64 kbps B channels and one 16 kbps D channel are transmitted in a full duplex fashion across the interface.

The configurations described in this document are deemed to be the most common, but by no means the only wiring configurations. Note that when operating in the TE mode, only one TE has the 100 Ω termination resistors in the transmit and receive paths. Figures 6 through 9 illustrate where to connect the termination resistors for the described loop configurations.

A description of the most commonly used loop configurations is as described below.

POINT–TO–POINT OPERATION

In the point–to–point mode of operation one NT communicates with one TE. As such, 100 Ω termination resistors must be connected across the transmit and receive paths of both the NT and TE transceivers. Figure 6 illustrates this wiring configuration.

When using the MC145574 in this configuration, the NT must be in adaptive timing. This is accomplished by holding the FIX pin low, i.e., connecting it to V_{SS}. CCITT I.430 and ANSI T1.605 specify that the S/T transceiver must be able to operate up to a distance of 1 km in the point–to–point mode. This is the distance D1 as shown in Figure 6.

SHORT PASSIVE BUS OPERATION

The short passive bus is intended for use when up to eight TEs are required to communicate with one NT. TEs can be distributed at any point along the passive bus, the only requirement being that the termination resistors be located at the end of the passive bus. Figure 7 illustrates this wiring configuration. CCITT I.430 and ANSI T1.605 specify a maximum operational distance from the NT of 200 meters. This corresponds to the distance D2 as shown in Figure 7.

EXTENDED PASSIVE BUS OPERATION

A wiring configuration whereby the TEs are restricted to a grouping at the far end of the cable, distant from the NT, is shown as the "Extended Passive Bus." This configuration is as illustrated in Figure 8. The termination resistors are to be positioned as illustrated in the diagram.

The essence of this configuration is that a restriction is placed on the distance between the TEs. The distance D3 as illustrated in Figure 8 corresponds to the maximum distance between the grouping of TEs. CCITT I.430 and ANSI T1.605 specify a distance of 25 to 50 meters for the separation between the TEs, and a distance of 500 meters for the total length. These distances correspond to the distances D3 and D4 as shown in Figure 8.

Note that the "NT configured" MC145574 should be placed in the adaptive timing mode for this configuration. This is achieved by holding the FIX pin low.

BRANCHED PASSIVE BUS OPERATION

A wiring configuration which has somewhat similar characteristics to those of the "Extended Passive Bus" is known as the "Branched Passive Bus" and is illustrated in Figure 9. In this configuration, the branching occurs at the end of the bus. The branching occurs after a distance D1 from the NT. The distance D5 corresponds to the maximum separation between the TEs.

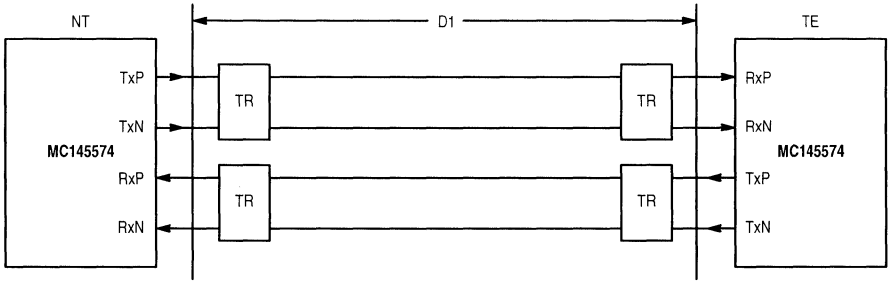


Figure 6. Point–to–Point

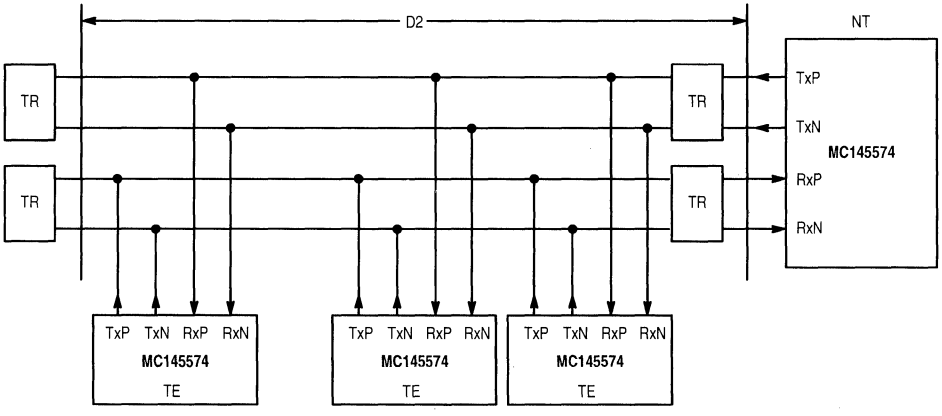


Figure 7. Short Passive Bus

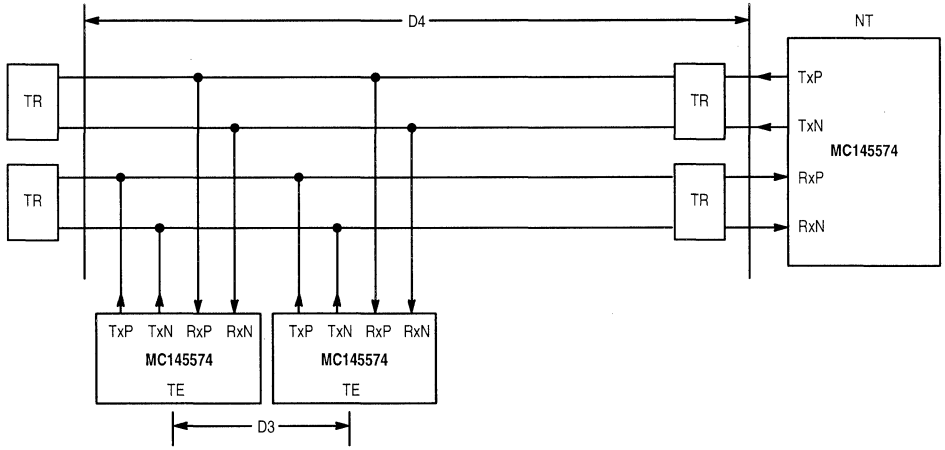


Figure 8. Extended Passive Bus

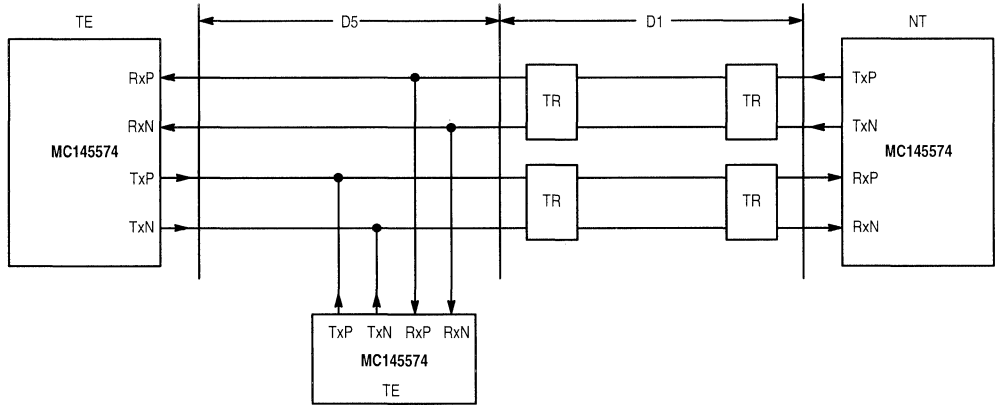


Figure 9. Branched Passive Bus

ACTIVATION/DEACTIVATION OF S/T TRANSCEIVER

INTRODUCTION

CCITT I.430 and ANSI T1.605 define five information states for the S/T transceiver. When the NT is in the fully operational state, it transmits INFO 4. When the TE is in the fully operational state, it transmits INFO 3. INFO 1 is transmitted by the TE when it wants to wake up the NT. INFO 2 is transmitted by the NT when it wants to wake up the TE, or in response to the TEs transmitted INFO 1. These states cause unique patterns of symbols to be transmitted over the S/T interface. Only when the S/T loop is in the fully activated state are the 2B+D channels of data transmitted over the interface.

ACTIVATION OF S/T LOOP BY NT

The NT activates the loop by transmitting INFO 2 to the TE or TEs. This is accomplished in the MC145574 by setting NR2(3) to a "1". Note that this bit is internally reset to "0" after the internal activation state machine has recognized its active transition.

The TE and TEs, on receiving INFO 2, will synchronize to it and transmit back INFO 3 to the NT. The NT, on receiving INFO 3 from the TE, will respond with INFO 4, thus activating the loop.

ACTIVATION OF S/T LOOP BY TE

The TE can activate an inactive loop by transmitting INFO 1 to the NT. This is accomplished in the MC145574 by setting NR2(3) to a "1". Note that this bit is internally reset to "0" after the internal activation state machine has recognized its active transition.

The NT, upon detecting INFO 1 from the TE, will respond with INFO 2. The TE, upon receiving a signal from the NT, will cease transmission of INFO 1, reverting to an INFO 0 state. After synchronizing to the received signal and having

fully verified that it is INFO 2, the TE will respond with INFO 3, thus activating the loop.

ACTIVATION PROCEDURES IGNORED

The MC145574 has the capability of being forced into the highest transmission state. This is accomplished by setting BR7(7) to a "1". Thus when this bit is set in the NT, it will force the NT to transmit INFO 4. Correspondingly, in the TE, setting this bit to "1" will force the TE to transmit INFO 3.

Note that CCITT I.430 and ANSI T1.605 specifications allow a TE to be activated by reception of INFO 4, without having to go through the intermediate handshaking. This is to allow for the situation where a TE is connected to an already active loop.

An NT, however, cannot be activated by a TE sending it INFO 3, without going through the intermediate INFO 1, INFO 2, INFO 3, and INFO 4 states.

This "Activation Procedures Ignored" feature is provided for test purposes, allowing the NT to forcibly activate the TE or TEs. In the TE, the forced transmission of INFO 3 enables verification of the TEs operation.

THE INTERCHIP DIGITAL LINK

INTRODUCTION

The Interchip Digital Link of the MC145574, IDL2, is backwards compatible with the IDL of the MC145474/75 S/T transceiver of first generation. But in addition to the standard operating mode, this enhanced interface features some new modes that are programmable through the SCP.

The IDL2 is a four–wire interface used for full–duplex communication between ICs on the board–level. The interface consists of a transmit path, a receive path, an associated clock, and a sync signal. These signals are known as DOUT, DIN, DCL, and FSR, respectively. The clock determines the rate of exchange of data in both the transmit and receive directions, and the sync signal controls when this exchange is to take place. Three channels of data are exchanged every 8 kHz. These channels consist of two 64 kbps B channels and one 16 kbps D channel used for full duplex communication between the NT and TE.

There are two modes of operation for an IDL device: IDL master and IDL slave. If an IDL device is configured as an IDL master, then FSR and DCL are outputs from the device. Conversely, if an IDL device is configured as an IDL slave, then FSR and DCL are inputs to the device. Ordinarily the MC145574 should be configured as an IDL slave when acting as an NT, and as an IDL master when acting as a TE. The exception to this rule is the option to configure the NT as an IDL master. The TE configured MC145574 also features the new option of operating in IDL slave mode.

THE SERIAL CONTROL PORT

The MC145574 is equipped with a serial control port (SCP). This SCP is used by external devices (such as an MC145488 DDLC) to communicate with the S/T transceiver. The SCP is an industry standard serial control port and is compatible with Motorola's SPI used on several single–chip MCUs.

The SCP is a five–wire bus with control and status bits, data being passed to and from the S/T transceiver in a full–duplex fashion, and an indicator of the interrupt status register.

The SCP interface consists of a transmit path, a receive path, an associated clock, an enable signal, and an interrupt indicate.These signals are known as SCPTx, SCPRx, SCPCLK, $\overline{\text{SCPEN}}$, and $\overline{\text{IRQ}}$.

The clock determines the rate of exchange of data in both the transmit and receive directions, the enable signal governs when this exchange is to take place, and the interrupt signal indicates that an interrupt condition exists and a read operation of the interrupt status register, NR3, is required.

The operation/configuration of the S/T transceiver is programmed by setting the state of the control bits within the S/T transceiver. The control, status, and data information reside in eight 4–bit wide nibble registers, sixteen 8–bit wide byte registers, and sixteen 8–bit wide overlay registers. The nibble registers are accessed via an 8–bit SCP bus transaction. The 16–byte wide registers are accessed by first writing to a pointer register within the eight 4–bit wide nibble registers. This pointer register (NR(7)) will then contain the address of the byte wide register to be read from or written to, on the following SCP transaction. Thus, an SCP byte access is in essence a 16–bit operation. Note that this 16–bit operation can take place by means of two 8–bit accesses or a single 16–bit access.

SCP TRANSACTIONS

There are six types of SCP transactions. These are:

1. SCP nibble read.
2. SCP nibble write.
3. SCP byte read.
4. SCP byte write.
5. SCP merged read.
6. SCP merged write.

SCP Nibble Read

A nibble read is an 8–bit SCP transaction. Figure 10 illustrates this process. To initiate an SCP nibble read the $\overline{\text{SCPEN}}$ pin must be brought low. Following this, a Read/$\overline{\text{Write}}$ (R/$\overline{\text{W}}$) bit followed by three primary address bits (A0 – A3), are shifted (MSB first) into an intermediate buffer register on the first four rising edges of SCPCLK, following the high to low transition of $\overline{\text{SCPEN}}$. If a read operation is to be performed, then R/$\overline{\text{W}}$ should be a "1". The three address bits clocked in after the R/$\overline{\text{W}}$ bit select which nibble register is to be read. The contents of this nibble register are shifted out on SCPTx on the subsequent four falling edges of SCPCLK, i.e., the four falling edges of SCPCLK after the rising edge of SCPCLK which clocked in the last address bit (LSB). $\overline{\text{SCPEN}}$ should be brought back high after the transaction, before another falling edge of SCPCLK is encountered. Note that SCP Rx is ignored during the time that SCPTx is being driven. Also note that SCPTx comes out of high impedance only when it is transmitting data.

SCP Nibble Write

A nibble write is an eight bit SCP transaction. To initiate an SCP nibble write the $\overline{\text{SCPEN}}$ pin must be brought low. Following this, a R/$\overline{\text{W}}$ bit followed by three primary address bits are shifted (MSB first) into an intermediate buffer register on the first four rising edges of SCPCLK following the high to

low transition of $\overline{SCPEN}$. If a write operation is to be performed then R/$\overline{W}$ should be a "0". The three address bits clocked in after the R/$\overline{W}$ bit select the nibble register to be written to. The data shifted in on the next four rising edges of SCPCLK is then written to the selected register. Throughout this whole operation the SCPTx pin remains in high–impedance state. Note that if a selected register or bit in a selected register is "read only" then a write operation has no effect.

SCP Byte Read

A byte read is a 16–bit SCP transaction. To initiate an SCP byte read, the $\overline{SCPEN}$ must be brought low. Following this, an R/$\overline{W}$ bit is shifted in from SCPRx on the next rising edge of SCPCLK. This bit determines the operation to be performed, read or write.

If R/$\overline{W}$ is a "1" then a read operation is selected. Conversely, if R/$\overline{W}$ is a "0" then a write operation is selected. The next three bits shifted in from SCPRx on the three subsequent rising edges of SCPCLK are primary address bits as mentioned previously. If all three bits are "1" then nibble register 7 is selected (NR7). This is a pointer register, selection of which informs the device that a byte operation is to be performed. When NR7 is selected, the following four bits shifted in from SCP Rx on the following four rising edges of SCPCLK are automatically written to NR7. These four bits are the address bits for the byte operation. In a read operation, the next eight falling edges of SCPCLK will shift out the data from the selected byte register on SCPTx.

As mentioned previously, an SCP byte access is a 16–bit transaction. This can take place in one 16–bit exchange or two 8–bit exchanges. If the transaction is performed in two 8–bit exchanges the $\overline{SCPEN}$ should be returned high after the first eight bits have been shifted into the part.

When $\overline{SCPEN}$ comes low again, the MSB of the selected byte will present itself on SCPTx. The following seven falling edges of SCPCLK will shift out the remaining seven bits of the byte register. Note that the order in which data is written into the part and read out of the part is independent of whether the byte access is done in one 16–bit exchange or in two 8–bit exchanges.

SCP Byte Write

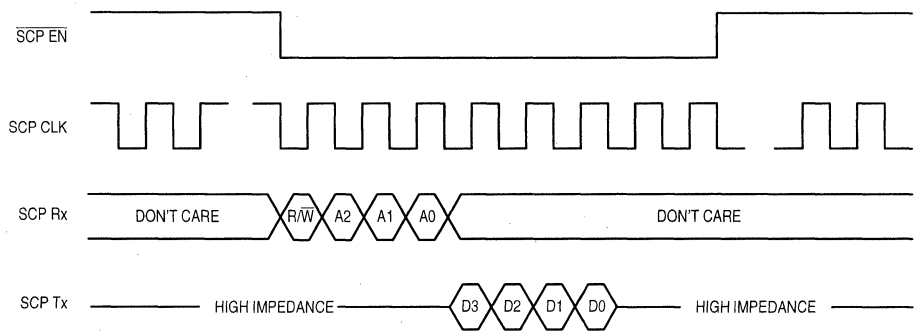
A byte write is also a 16–bit SCP transaction. To initiate an SCP byte write the $\overline{SCP\ EN}$ must be brought low. As before, the next bit determines whether the operation is to be read or write. If the first bit is a "0" then a write operation is selected. Again, the next three bits read in from SCP Rx on the subsequent three rising edges of SCPCLK must all be "1" in order to select the pointer nibble register (NR7). The following four bits shifted in are automatically written into NR7. As in an SCP byte read, these bits are the address bits for the selected byte register operation. The next eight rising edges of SCPCLK shift in the data from the SCPRx. This data is then stored in the selected byte register. Throughout this operation SCPTx will be in a high–impedance state. Note that if the selected byte is "read only," then this operation will have no effect.

As mentioned previously, an SCP byte access is a 16–bit transaction. This can take place in one 16–bit exchange or two 8–bit exchanges. If the transaction is performed in two 8–bit exchanges, then $\overline{SCPEN}$ should be returned high after the first eight bits have been shifted into the part.

When $\overline{SCPEN}$ comes low again, the next eight rising edges of SCPCLK shift data in from SCPRx. This data is then stored in the selected byte.

SCP Merged Read/Write

Merged operations are accomplished by not taking $\overline{SCPEN}$ high between separate SCP instructions. The SCP bytes/nibbles are strung together in a continuous bit stream and can be a mux or read/write command. The device is able to extract the separate instructions and provide the appropriate response. The $\overline{SCPEN}$ signal goes low at the start of the bit stream and goes high again at the end. SCPCLK should only be active during valid bit times while $\overline{SCPEN}$ is low.



NOTES:
1. R/$\overline{W}$ = 1 for a read operation.
2. Data is shifted out on SCP Tx on the falling edges of SCP CLK, MSB first.
3. Data is shifted into the chip from SCP Rx on the rising edges of SCP CLK, MSB first.

Figure 10. Serial Control Port Nibble Read Operation

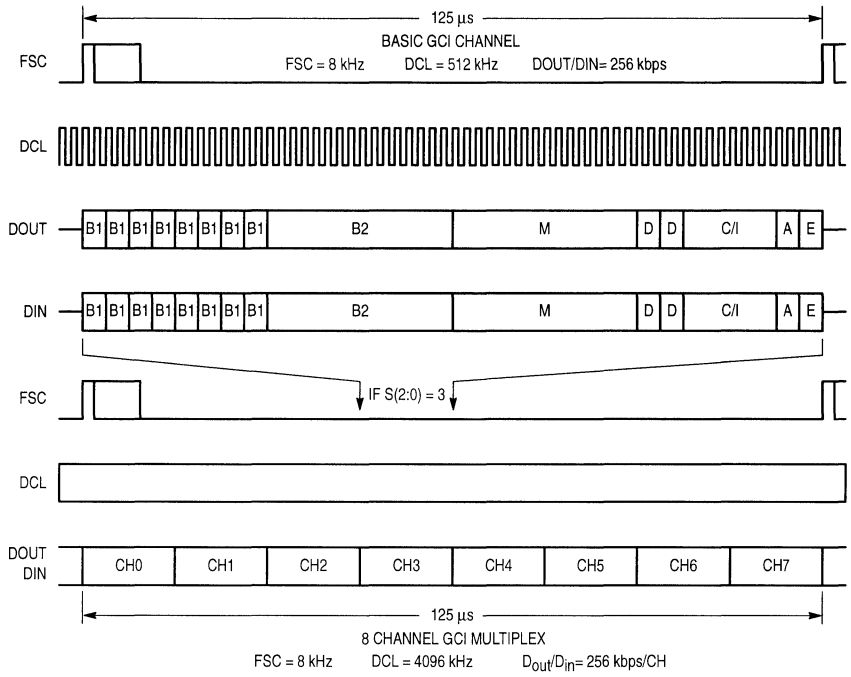


Figure 11.

GENERAL CIRCUIT INTERFACE

The MC145574 is able to work with a general circuit interface port (GCI). This GCI is a standard four–wire interface between devices for the subscriber access in ISDN and analog environments. The principle use, in the these applications, is to control the subscriber line interface circuitry.

Some of the benefits of the General Circuit Interface are:

- Operation and maintenance features.
- Activation and deactivation facilities (via C/I channel).
- Well defined transmission protocols to ensure correct information transfer between GCI compatible devices.
- Point–to–Point and Multipoint communication links.
- Multiplexed mode of operation where up to eight GCI channels can be combined to form a single data stream.

The GCI interface consists of a transmit path, a receive path, an associated clock, and a frame sync signal. These signals are known as D_{out}, D_{in}, DCL, and FSC.

The clock determines the rate of exchange of data in both the transmit and receive directions, and the frame sync signal indicates when this exchange will start.

GCI FRAME STRUCTURE

In a GCI channel, information is in a four byte time–division based structure with a repetition rate of 8 kHz. The four bytes are B1 and B2 channels, a Monitor (M) channel, and a Control/Indication (C/I) channel.

The two independent B channels are used to carry subscriber voice and data information.

The M channel is used for operation and maintenance facilities.

The C/I channel is further subdivided into two bits for the D channel information, four bits for the C/I channel and two bits for the A and E channels that are used to control the transfer of information on the monitor channel.

Figure 11 shows the relative positions of these channels.

NIBBLE MAP DEFINITION

INTRODUCTION

There are seven nibble register (NR0 through NR6) in the MC145574. Control and status information reside in these nibble registers. These nibble registers are accessed via the SCP. The nomenclature used in this data sheet is such that NR2(3) refers to nibble register 2, bit 3.

The MC145574 nibble register map is compatible to the MC145474/475 nibble register map, the only modification being the removal of bits NR6(2) and NR6(1) related to the IDL A/M FIFOs and the addition of bits (NR2(0), NR3(0), and NR4(0) for NT mode only).

Tables 2 and 3 show an SCP nibble map for NT and TE operations, respectively.

Table 2. SCP Nibble Map for NT Operation

	(3)	(2)	(1)	(0)
NR0	Software Reset	Transmit Power Down	Absolute Minimum Power	Return to Normal
NR1	Act Ind (AI)	Error Ind (EI)		Frame Sync (FS)
NR2	Act Req (AR)	Deact Req (DR)	Act Timer T1 Expire	NT Term Class
NR3	IRQ#3 Δ Rx Info	IRQ#2 Multiframe Reception	IRQ#6 FECV Detection	IRQ#7 NT Term D Col
NR4	IRQ#3 Enable	IRQ#2 Enable	IRQ#6 Enable	IRQ#7 Enable
NR5	Idle B1 Channel on S/T Loop	Idle B2 Channel on S/T Loop	Invert B1 Channel	Invert B2 Channel
NR6	2B+D IDL Transparent Loopback			Exchange B1 and B2 at IDL

Table 3. SCP Nibble Map for TE Operation

	(3)	(2)	(1)	(0)
NR0	Software Reset	Transmit Power Down	Absolute Minimum Power	Return to Normal
NR1	Act Ind (AI)	Error Ind (EI)	Multiframing Detection	Frame Sync (FS)
NR2	Act Req (AR)		Act Timer T3 Expire	Class
NR3	IRQ#3 Δ Rx Info	IRQ#2 Multiframe Reception	IRQ#1 D Channel Collision	
NR4	IRQ#3 Enable	IRQ#2 Enable	IRQ#1 Enable	
NR5	En B1 S/T Loopback on S/T Loop	En B2 S/T Loopback on S/T Loop	Invert B1 Channel	Invert B2 Channel
NR6	2B+D IDL Transparent Loopback			Exchange B1 and B2 at IDL

BYTE MAP DESCRIPTION

INTRODUCTION

There are sixteen byte registers (BR0 through BR15) in the MC145574. Control, status, and maintenance information reside in these byte registers. These byte registers are accessed via the SCP. The nomenclature used in this data sheet is such that BR2(3) refers to byte register 2, bit 3.

The byte register map is fully compatible with the byte register map of the MC145474, exceptions are:

1. The functions that were related to the IDL A/M FIFO's have been removed, writing to these registers will have no effect and reading them will return FFH.
2. The TTL Input Level bit BR13 (6) has been removed. The digital inputs are both CMOS and TTL compatible. Writing to this bit has no effect on the circuit, and reading it returns "0" or "1" depending on what value, if any, has been written.
3. The only addition to the byte register map is the bit BR15 (0), used for enabling the overlay registers.

Tables 4 and 5 show the byte map for NT and TE modes of operation, respectively.

OVERLAY MAP DEFINITION

INTRODUCTION

There are ten nibble register (OR0 through OR8 and OR15) in the MC145574. The overlay registers are a second bank of registers available when the overlay register control bit BR15(7) is set to a logic "1". These overlay registers are in the IDL2 TSA mode used to assign the timeslot used by each channel (B1,B2 and D) for transmission and reception: (OR0 through OR5), OR6, OR7 and OR8 are control registers used in the GCI indirect mode and OR15 gives the Revision number of the S/T chip. See Table 6 for the overlay register map.

Table 4. Byte Map for NT Mode of Operation

	(7)	(6)	(5)	(4)	(3)	(2)	(1)	(0)
BR0								
BR1								
BR2	SC1.1	SC1.2	SC1.3	SC1.4				
BR3	Q.1	Q.2	Q.3	Q.4	Q Qual	MF Int		
BR4	FV7	FV6	FV5	FV4	FV3	FV2	FV1	FV0
BR5	BPV7	BPV6	BPV5	BPF4	BPV3	BP32	BPV1	BPV0
BR6	B1 S/T LB TP	B1 S/T LB NTP	B2 S/T LB TP	B2 S/T LB NTP	IDL B1 LB TP	IDL B1 LB NTP	IDL B2 LB TP	IDL B2 LB NTP
BR7	ACT PR Disabled	AONT	Enable MFrame	Invert E Channel	IDL MS Mode	IDL CLK SPD 0	LAPD Pol Cont	ACT T2 EXP
BR8								
BR9	TXSC2.1	TXSC2.2	TXSC2.3	TXSC2.4	TXSC3.1	TXSC3.2	TXSC3.3	TXSC3.4
BR10	TXSC4.1	TXSC4.2	TXSC4.3	TXSC4.4	TXSC5.1	TXSC5.2	TXSC5.3	TXSC5.4
BR11	Do Not React to INFO 1	Do Not React to INFO 2	Rx INFO St Bit 1	Rx INFO St Bit 0	Tx INFO St Bit 1	Tx INFO St Bit 0	Ext S/T Loopback	Tx 96K Test Signal
BR12	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
BR13	NT1 Star		IDL CLK SPD1	Mute B2 to IDL Tx	Mute B1 to IDL Tx	Force E to Zero		
BR14	IDL ADJ En	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
BR15	Overlay Reg En		Rev 5	Rev 4	Rev 3	Rev 2	Rev 1	Rev 0

Table 5. Byte Map for TE Mode of Operation

	(7)	(6)	(5)	(4)	(3)	(2)	(1)	(0)
BR0								
BR1								
BR2	Q.1	Q.2	Q.3	Q.4				
BR3	SC1.1	SC1.2	SC1.3	SC1.4	MF Detect	MF Int		
BR4	FV7	FV6	FV5	FV4	FV3	FV2	FV1	FV0
BR5	BPV7	BPV6	BPV5	BPF4	BPV3	BP32	BPV1	BPV0
BR6	B1 S/T LB TP	B1 S/T LB NTP	B2 S/T LB TP	B2 S/T LB NTP	IDL B1 LB TP	IDL B1 LB NTP	IDL B2 LB TP	IDL B2 LB NTP
BR7	ACT PR Disabled	D Chan Proc Ignored		Map E to D	IDL Free Run	IDL CLK SPD 0	LAPD Pol Cont	
BR8								
BR9	RXSC2.1	RXSC2.2	RXSC2.3	RXSC2.4	RXSC3.1	RXSC3.2	RXSC3.3	RXSC3.4
BR10	RXSC4.1	RXSC4.2	RXSC4.3	RXSC4.4	RXSC5.1	RXSC5.2	RXSC5.3	RXSC5.4
BR11			Rx INFO St Bit 1	Rx INFO St Bit 0	Tx INFO St Bit 1	Tx INFO St Bit 0	Ext S/T Loopback	Tx 96K Test Signal
BR12	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
BR13			IDL CLK SPD1	Mute B2 to IDL Tx	Mute B1 to IDL Tx		Force IDL Tx	
BR14	IDL ADJ En	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
BR15	Overlay Reg En		Rev 5	Rev 4	Rev 3	Rev 2	Rev 1	Rev 0

Table 6. Overlay Registers Map

	(7)	(6)	(5)	(4)	(3)	(2)	(1)	(0)
OR0	D_{out} B1 CHANNEL TIME SLOT BITS (7:0)							
OR1	D_{out} B2 CHANNEL TIME SLOT BITS (7:0)							
OR2	D_{out} D CHANNEL TIME SLOT BITS (7:0)							
OR3	D_{in} B1 CHANNEL TIME SLOT BITS (7:0)							
OR4	D_{in} B2 CHANNEL TIME SLOT BITS (7:0)							
OR5	D_{in} D CHANNEL TIME SLOT BITS (7:0)							
OR5	(GCI Indirect Mode)					S1	S2	S3
OR6	TSA B1 EN	TSA B2 EN	TSA D EN			GCI_IND EN	CLK1	CLK0
OR7	Disable 3 V Reg	Enable S/G Bit	Enable TCLK	Dual Fr Sync's	Long Frame	8/10 Bits Select	TSEN	TSEN D_EN
OR8			DIS Stal	TE En	MS En	FIX En	NTTerm	Sleep Enable
OR15	Overlay Reg EN		Rev 5	Rev 4	Rev 3	Rev 2	Rev 1	Rev 0

D CHANNEL OPERATION

INTRODUCTION

The S/T interface is designed for full duplex transmission of two 64 kbps B channels and one 16 kbps D channel, between one NT device and one or more TEs. The TEs gain access to the B channels by sending layer 2 frames to the network over the D channel. CCITT I.430 and ANSI T1.605 specify a D channel access algorithm for TEs to gain access to the D channel. The MC145574 S/T transceiver is fully compliant with the D channel access algorithm as defined in CCITT I.430 and ANSI T1.605. The D channel operation is handled through the SCP when using the S/T Interface either in IDL or GCI indirect mode, and handled through the C/I channel when using the S/T Interface GCI direct mode.

The various bits and pins directly pertaining to D channel operation are shown in Tables 7 and 8.

D channel data is clocked into the MC145574 via DOUT on the falling edges of DCL. Data is clocked out onto DOUT on the rising edges of DCL in either GCI or IDL2 modes of operation.

IDL2 D CHANNEL OPERATION

Gaining Access to the D Channel in the TE Mode

The pins DREQUEST and DGRANT are used in the TE mode of operation to request and grant access to the D channel. An external device wishing to send a layer 2 frame should bring DREQUEST high, and maintain it high for the duration of the layer 2 frame. DGRANT is an output signal used to indicate to an external device that the D channel is clear. Note that the DGRANT signal actually goes high once received E echo bit prior to the programmed priority class selection. DGRANT goes high at a count of (n – 1) to accommodate the delay between the input of D channel data via the IDL interface and the line transmission of those bits towards the NT. If at the time of the FSR pulse falling edge, the DGRANT and the DREQUEST signals are both detected high, the TE mode transceiver will begin FIFO buffering of the input D channel bits from the IDL interface. This FIFO is four bits deep. Note that DGRANT goes high on the boundaries of the demodulated E bits. In order for the contention algorithm to work on the D channel, HDLC data must be used. The MC145574 modulates the D channel data onto the S/T bus in the form that it is received from the IDL bus. Thus, the data must be presented to it in HDLC format. Note that one of the applications of the MC145488 DDLC is for use with the MC145574 in the terminal mode. The MC145488 will perform the HDLC conversion and perform the necessary D channel handshaking.

Setting the Class for TE Mode of Operation

Recommendation CCITT I.430 and ANSI T1.605 specifications mandate two classes of operation for a TE, with respect to D channel operation. These two classes of operation are class 1 and class 2. Each of these classes have two associated priorities, high priority and low priority. These classes and their associated priorities pertain to the number of demodulated E bits required to be "1", before the D channel is deemed to be clear for use. Using the MC145574 in the TE mode of operation, the user programs the device for class 1 or class 2 operation by either NR2(0) or pin 10.

Table 9 illustrates how to configure the MC145574 for either class 1 or class 2 operation. This table also illustrates when DGRANT goes high. Note that although DGRANT goes high one E bit before the required count, data will not be modulated onto the D bit timeslots in the S/T frame until the required number of E bits = "1" are received. Thus, data gets modulated onto the D channel if the E bit following the low to high transition of DGRANT is "1".

The device will automatically switch from high to low priority and back, within each class of operation, in accordance with CCITT I.430 and ANSI T1.605.

MULTIFRAMING

INTRODUCTION

A layer 1 signalling channel between the NT and TE is provided in the MC145574 in accordance with CCITT I.430 and

ANSI T1.605. In the NT and TE direction, this layer 1 channel is the S channel. In the TE to NT direction it is the Q channel. The S channel is subdivided into five subchannels: SC1, SC2, SC3, SC4, and SC5. In normal operation the NT sets its Fa bit (bit 14) to a binary zero every frame. The "wrapping" action of the TE/TEs, as outlined in CCITT I.430 and ANSI T1.605, causes the Fa bit of the TE/TEs to be a "0" also. This is to ensure the existence of two–line code violations per frame, enabling fast synchronization.

Multiframing is activated by the NT by setting the M bit (bit 26) in the NT and TE frame to a binary one, once every 20 frames. In addition to this, the Fa bit (bit 14) in the NT to TE direction is set to a binary one, once every five frames. When multiframing is enabled, the NT sends its S channel data (SC1 through SC5) in the S timeslot (bit 37) every frame. Table 10 shows the order in which the S channel data is transmitted. Note that the M bit = "1" sets the multiframe boundary. Once every five frames the Fa bit is set to "1" in the NT to TE direction. This serves as a Q bit identifier for the TE/TEs, which send their Q data in their Fa bit position in the corresponding frames. In order to avoid Q data collision, those TEs which have not been addressed for multiframing, must send '1s' in the Q bit timeslots.

DEVICE CONFIGURATIONS

The MC145574 can be configured in several different modes for different applications.

NT CONFIGURATIONS

To select NT mode, pin 4 (TE/$\overline{NT}$) must be held low. The NT device can operate in a mixture of different configurations. How each aspect of the NT's operation is selected will be discussed separately in the following sections. However for a broad view of the NT's various flavors, the NT family tree is shown below.

NT Fixed or Adaptive Timing

The receiver/demodulator of the NT can operate in two different modes depending on the type of loop that the device is connected to. These modes are called FIXED and ADAPTIVE Timing modes. The mode of operation is chosen by the state of Pin 6. When this pin is held low, the device is in adaptive mode and when held high, the device is in fixed timing mode. The choice of mode is dependent on the loop characteristics. The intention is that fixed timing should be used for short passive bus configurations and adaptive timing used for all others. However, the performance of the timing recovery circuit employed in the MC145474/75 and hence, also in the MC145574 allows the use of adaptive timing in all loop configurations. Thus, it is recommended that adaptive timing be used in all configurations.

It is also possible to select fixed timing mode via the SCP control bit OR8(2), the FIX pin is internally OR'd with this SCP bit, and one should note that in the NTTerm mode this is the only way to select fixed timing.

NT Master or Slave

In NT mode, the IDL or GCI interface can be selected either as a master or a slave. This selection is made with Pin 5. When held low slave mode is selected and when held high master mode is selected.

In slave mode the IDL/GCI interface frame sync and clock are inputs and the S/T loop interface timing is slaved to these inputs. In master mode the IDL/GCI interface frame sync and clock are outputs, these signals being derived from the 15.36 MHz XTAL oscillator. The S/T loop interface timing, however, is always slaved to the IDL/GCI frame sync.

Therefore, in NT mode the S/T loop interface timing is always slaved to the IDL/GCI frame sync. The source of this timing can be selected to be from the IDL/GCI driver (Slave mode) or from the NT device itself (Master mode).

NT Master mode will be referred to as NTM, likewise NT Slave mode will be NTS.

It is also possible to select NTM by writing to the SCP control bit BR7(3). Or alternatively in TE or NT mode, master selection can be made via OR8(3), the M/$\overline{S}$ pin is internally OR'd with these SCP bits.

NT STAR and NT Terminal Modes

In NT mode two further mode extensions can be selected via control bits accessible through the SCP. These NT mode extensions have no effect on the IDL/GCI interface but alter the operation of other pins to perform the desired functions. These two modes are called NT Star and NT Term.

NT Star Mode

Appendix B of ANSI T1.605 describes an example of an NT that will support multiple T interfaces. This is to accommodate multipoint operation with more than eight TEs. The MC145574 can be configured for NT Star mode of operation. This mode is for use in wire ORing multiple NT configured S/T chips on the IDL side. Each NT has a common FSR, DCL, D_{out}, and D_{in}. Each NT is then connected to its own individual S/T loop containing either a single TE or a group of TEs. As such, the contention for either of the B channels or for the D channel is now extended from a single passive bus to a grouping of passive busses.

ISDN employs the use of HDLC data on the D channel. Access to either of the B channels is requested and either granted or denied by the user sending layer 2 frames on the D channel. In normal operation where there is only one NT, the TEs are granted access to the D channel in accordance with their priority and class. By counting the required number of E channel echo bits being "1", the TEs know when the D channel is clear. Thus, in the NT Star mode of operation, where there are multiple passive busses competing for the same B1, B2, and D channels, the same E echo channel must be transmitted from each NT to its passive bus. This is accomplished in the MC145574 by means of the AND_{in}, AND_{out}, and ECHO IN pins.

Figure 12 shows how to connect the multiple number of NTs in the NT Star mode. Successive connection of the AND_{out} (this is the output of an internal AND gate whose inputs are the demodulated D bits and the data on the AND_{in} pin) and AND_{in} pins, and the common connections of the ECHO IN pins, succeeds in sending the same E echo channel to each group of TE/TEs. To configure a series of NTs for NT Star mode, BR13(7) must be set to "1" in each NT. Data transmitted on IDL Tx in NT Star mode, will have the following format: a logic "0" is V_{SS}, a logic "1" causes IDL_D_{out} to go to a high–impedance state. This then permits the series wire ORing of the IDL bus. Note that one of the NTs must have its AND_{in} pin pulled high.

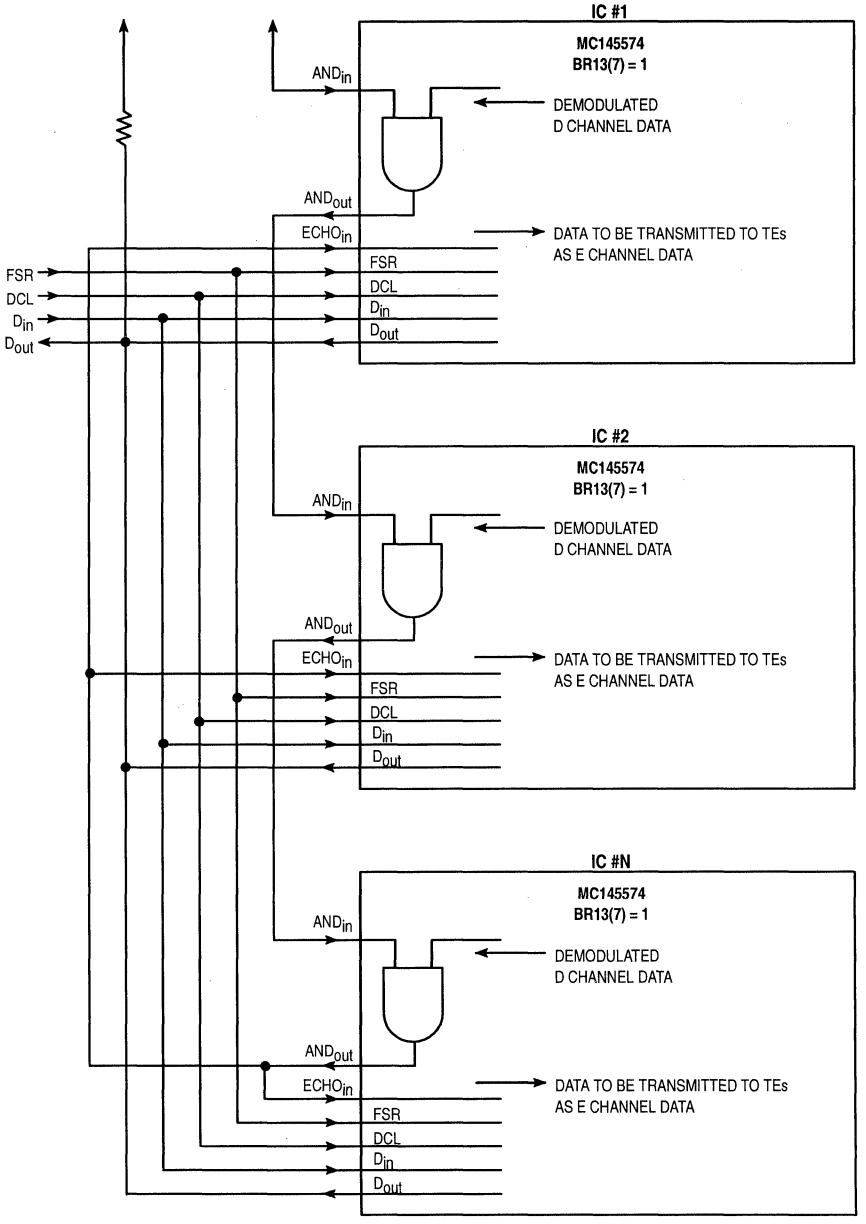


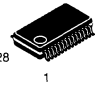
Figure 12. NT Star Mode of Operation

MC145583

Product Preview

3.3 Volt Only Driver/Receiver with an Integrated Standby Mode

EIA–232–E and CCITT V.28



VF SUFFIX
SSOP
CASE 940J

ORDERING INFORMATION

MC145583VF	SSOP

2

The MC145583 is a CMOS transceiver composed of three drivers and five receivers that fulfills the electrical specifications of EIA–232–E, EIA–562, and CCITT V.28 while operating from a single + 3.3 or + 5.0 V power supply. This transceiver is a high–performance, low–power consumption device that is equipped with a standby function.

A voltage tripler and inverter converts the + 3.3 V to ± 8.8 V, or a voltage doubler and inverter converts the + 5.0 V to ± 8.8 V. This is accomplished through an on–chip 40 kHz oscillator and five inexpensive external capacitors.

Drivers:

- ± 5 V Minimum Output Swing at 3.3 or 5.0 V Power Supply
- 300 Ω Power–Off Impedance
- Output Current Limiting
- Three–State Outputs During Standby Mode

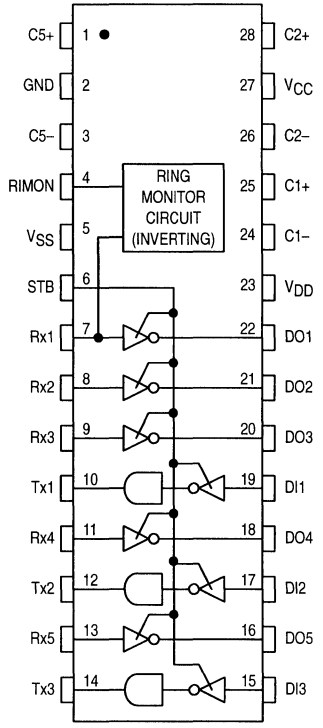
Receivers:

- ± 25 V Input Range
- 3 to 7 kΩ Input Impedance
- 0.8 V Hysteresis for Enhanced Noise Immunity
- Three–State Outputs During Standby Mode

Ring Monitor Circuit:

- Invert the Input Level on Rx1 to Logic Output Level on RIMON at Standby Mode

PIN ASSIGNMENT

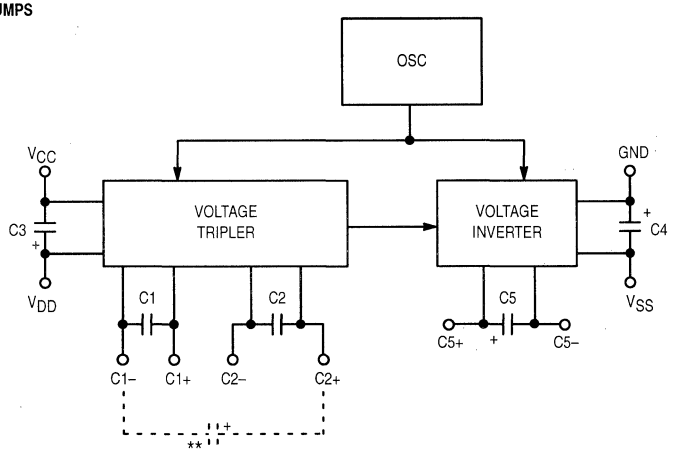


This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

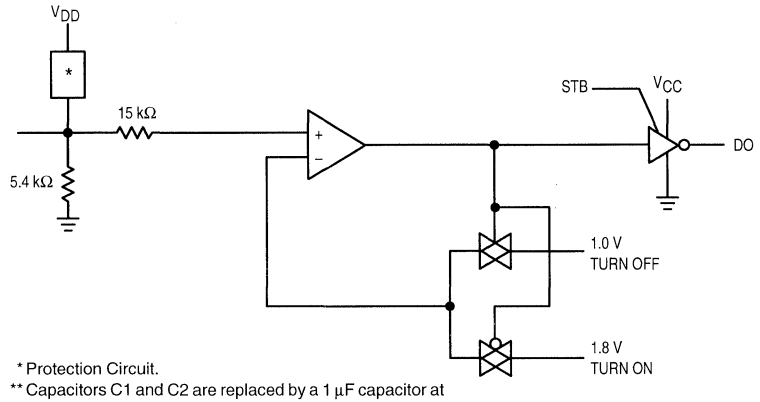
REV 2
10/95

FUNCTION DIAGRAM

CHARGE PUMPS

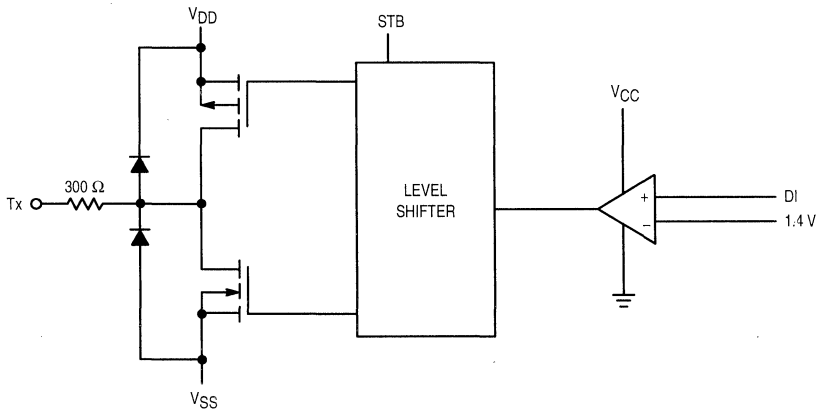


RECEIVER



* Protection Circuit.
** Capacitors C1 and C2 are replaced by a 1 μF capacitor at V_{CC} = 5.0 V supply.

DRIVER



MAXIMUM RATINGS (Voltage polarities referenced to GND)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{CC}	– 0.5 to + 6.0	V
Input Voltage Rx1 – Rx5 Inputs DI1 – DI3 Inputs	V_{IR}	V_{SS} – 15 to V_{DD} + 15 – 0.5 to V_{CC} + 0.5	V
DC Current per Pin	I	± 100	mA
Power Dissipation	P_D	1	W
Operating Temperature Range	T_A	– 40 to + 85	°C
Storage Temperature Range	T_{stg}	– 85 to + 150	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, it is recommended that the voltage at the DI and DO pins be constrained to the range GND ≤ V_{DI} ≤ V_{CC} and GND ≤ V_{DO} ≤ V_{CC}. Also, the voltage at the Rx pin should be constrained to (V_{SS} – 15 V) ≤ $V_{Rx1 – Rx5}$ ≤ (V_{DD} + 15 V), and Tx should be constrained to V_{SS} ≤ $V_{Tx1 – Tx3}$ ≤ V_{DD}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., GND or V_{CC} for DI, and GND for Rx).

2

RECOMMENDED OPERATING LIMITS

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply	V_{CC} V_{CC}*	3.0 4.5	3.3 5.0	3.6 5.5	V
Operating Temperature Range	T_A	– 40	—	85	°C

* Capacitors C1 and C2 are replaced by a 1 µF capacitor at V_{CC} = 5 V.

DC ELECTRICAL CHARACTERISTICS (Voltage polarities referenced to GND = 0 V; C1 – C5 = 1 µF; T_A = 25°C)

Parameter	Symbol	Min	Typ	Max	Unit
DC Power Supply	V_{CC}	3.0	3.3	3.6	V
Quiescent Supply Current (Output Unloaded, Input Low)	I_{CC}	—	2.8	6.0	mA
Quiescent Supply Current (Standby Mode; STB = 1, Output Unloaded)	$I_{CC(STB)}$	—	< 5	10	µA
Control Signal Input Voltage (STB)	V_{IL} V_{IH}	— V_{CC} – 0.5	— —	0.5 —	V
Control Signal Input Current (STB)	I_{IL} I_{IH}	— —	— —	10 10	µA
Charge Pumps Output Voltage (V_{CC} = 3 V; C1, C2, C3, C4, C5 = 1 µF)					V
Output Voltage (V_{DD}) I_{load} = 0 mA	V_{DD}	8.5	8.8	—	
Output Voltage (V_{DD}) I_{load} = 6 mA		7.5	7.9	—	
Output Voltage (V_{SS}) I_{load} = 0 mA	V_{SS}	—	– 8.8	– 8.5	
Output Voltage (V_{SS}) I_{load} = 6 mA		—	– 7.8	– 7.0	

RECEIVER ELECTRICAL SPECIFICATIONS

(Voltage polarities referenced to GND = 0 V; V_{CC} = + 3.3 V ± 10%; C1 – C5 = 1 µF; T_A = 25°C)

Parameter		Symbol	Min	Typ	Max	Unit
Input Turn–On Threshold ($V_{DO1 – DO5}$ = V_{OL}; Rx1 – Rx5)	3.3 V	V_{on}	1.35	1.8	2.35	V
	5.0 V		2.00	2.5	3.10	
Input Turn–Off Threshold ($V_{DO1 – DO5}$ = V_{OH}; Rx1 – Rx5)	3.3 V	V_{off}	0.75	1.0	1.25	V
	5.0 V		1.20	1.5	1.80	
Input Resistance		R_{in}	3	5.4	7	kΩ
High–Level Output Voltage (DO1 – DO5) I_{out} = – 20 µA		V_{OH}	V_{CC} – 0.1	—	—	V
$V_{Rx1 – Rx5}$ = – 3 to – 25 V I_{out} = – 1 mA			V_{CC} – 0.6	2.7	—	
Low–Level Output Voltage (DO1 – DO5) I_{out} = + 20 µA		V_{OL}	—	0.01	0.1	V
$V_{Rx1 – Rx5}$ = + 3 to + 25 V I_{out} = + 1.6 mA			—	0.5	0.7	
Ring Monitor Circuit (Input Threshold)		V_{TH}	—	1.1	—	V
High–Level Output Voltage (RIMON) I_{out} = – 20 µA		V_{OH}	V_{CC} – 0.1	—	—	V
I_{out} = – 1 mA			V_{CC} – 0.6	2.7	—	
Low–Level Output Voltage (RIMON) I_{out} = + 20 µA		V_{OL}	—	0.01	0.1	V
I_{out} = + 1.6 mA			—	0.5	0.7	

DRIVER ELECTRICAL SPECIFICATIONS

(Voltage polarities referenced to GND = 0 V; V_{CC} = + 3.3 V or + 5.0 V ± 10%; C1 – C5 = 1 µF; T_A = 25°C)

Parameter		Symbol	Min	Typ	Max	Unit
Digital Input Voltage	DI1 – DI3					V
Logic Low		V_{IL}	—	—	0.7	
Logic High		V_{IH}	1.8	—	—	
Digital Input Current	DI1 – DI3					µA
V_{DI} = GND		I_{IL}	—	7	—	
V_{DI} = V_{CC}		I_{IH}	—	—	± 1.0	
Output High Voltage		V_{OH}				V
Load on All Tx1 – Tx3, R_L = 3 kΩ; C_P = 2500 pF, $V_{DI1 – DI3}$ = Logic Low			5.0	7.0	—	
No Load			8.5	8.8	—	
Output Low Voltage		V_{OL}				V
Load on All Tx1 – Tx3, R_L = 3 kΩ; C_P = 2500 pF, $V_{DI1 – DI3}$ = Logic High			—	– 7.0	– 5.0	
No Load			—	– 8.8	– 8.5	
Ripple (Refer to $V_{DD} – V_{SS}$ Value) ***		V_{RF}	—	—	± 5%	
Off Source Impedance	Tx1 – Tx3	Z_{off}	300	—	—	Ω
Output Short Circuit Current (V_{CC} = 3.3 V or 5.5 V)		I_{SC}				mA
Tx1 – Tx3 Shorted to GND*			—	—	± 60	
Tx1 – Tx3 Shorted to ± 15 V**			—	—	± 100	

* Specification is for one Tx output to be shorted at a time. Should all three driver outputs be shorted simultaneously, device power dissipation limits could be exceeded.

** This condition could exceed package limitations.

*** Ripple V_{RF} would not exceed ± 5% of ($V_{DD} – V_{SS}$).

SWITCHING CHARACTERISTICS (V_{CC} = + 3.3 V or + 5 V, ± 10%; C1 – C5 = 1 µF; T_A = 25°C)

Parameter		Symbol	Min	Typ	Max	Unit
Drivers						
Propagation Delay Time	Tx1 – Tx3	t_{DPLH}				µs
Low–to–High (R_L = 3 kΩ, C_L = 50 pF or 2500 pF)			—	0.5	1	
High–to–Low (R_L = 3 kΩ, C_L = 50 pF or 2500 pF)		t_{DPHL}	—	0.5	1	
Output Slew Rate (Source R = 300 Ω) Loading: R_L = 3 – 7 kΩ; C_L = 2500 pF	Tx1 – Tx3	SR	± 4	—	± 30	V/µs
Output Disable Time*		t_{DAZ}	—	4	10	µs
Output Enable Time*		t_{DZA}	—	25	50	ms
Receivers						
Propagation Delay Time	DO1 – DO5					µs
Low–to–High		t_{RPLH}	—	—	1	
High–to–Low		t_{RPHL}	—	—	1	
Output Rise Time	DO1 – DO5	t_r	—	120	200	ns
Output Fall Time	DO1 – DO5	t_f	—	40	100	ns
Output Disable Time*		t_{RAZ}	—	4	10	µs
Output Enable Time*		t_{RZA}	—	25	50	ms

* Including the charge pump setup time.

TRUTH TABLES

Drivers

DI	STB	Tx
X	H	Z*
H	L	L
L	L	H

* $V_{SS} \le V_{Tx} \le V_{DD}$ X = Don't Care

Receivers

Rx	STB	DO
X	H	Z*
H	L	L
L	L	H

* GND ≤ $V_{DO} \le V_{CC}$ X = Don't Care

PIN DESCRIPTIONS

V_{CC}
Digital Power Supply (Pin 27)

This digital supply pin is connected to the logic power supply. This pin should have a not less than 0.33 µF capacitor GND.

GND
Ground (Pin 2)

Ground return pin is typically connected to the signal ground pin of the EIA–232–E connector (Pin 7) as well as to the logic power supply ground.

V_{DD}
Positive Power Supply (Pin 23)

This is the positive output of the on–chip voltage tripler and the positive power supply input of the driver/receiver sections of the device. This pin requires an external storage capacitor to filter the 50% duty cycle voltage generated by the charge pump.

V_{SS}
Negative Power Supply (Pin 5)

This is the negative output of the on–chip voltage tripler/inverter and the negative power supply input of the driver/ receiver sections of the device. This pin requires an external storage capacitor to filter the 50% duty cycle voltage generated by the charge pump.

RIMON
Ring Monitor Circuit (Pin 4)

The Ring Monitor Circuit will convert the input level on Rx1 pin at standby mode and output on the RIMON pin.

STB
Standby Mode (Pin 6)

The device enters the standby mode while this pin is connected to the logic high level. During the standby mode, driver and receiver output pins become high–impedance state. In this condition, supply current I_{CC} is below 5 µA (typ).

C5+, C5–, C2+, C2–, C1+, C1–
Voltage Tripler and Inverter (Pins 1, 3, 28, 26, 25, 24)

These are the connections to the internal voltage tripler and inverter, which generate the V_{DD} and V_{SS} voltages.

Rx1, Rx2, Rx3, Rx4, Rx5
Receive Data Inputs (Pins 7, 8, 9, 11, 13)

These are the EIA–232–E receive signal inputs. A voltage between + 3 and + 25 V is decoded as a space, and causes the corresponding DO pin to swing to GND (0 V). A voltage between – 3 and – 25 V is decoded as a mark, and causes the DO pin to swing up to V_{CC}.

DO1, DO2, DO3, DO4, DO5
Data Outputs (Pins 22, 21, 20, 18, 16)

These are the receiver digital output pins, which swing from V_{CC} to GND. Output level of these pins is high impedance while in standby mode.

DI1, DI2, DI3
Data Inputs (Pins 19, 17, 15)

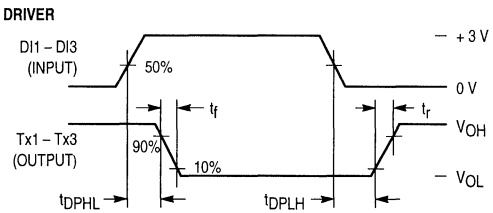
These are the high impedance digital input pins to the drivers. Input voltage levels on these pins must be between V_{CC} and GND.

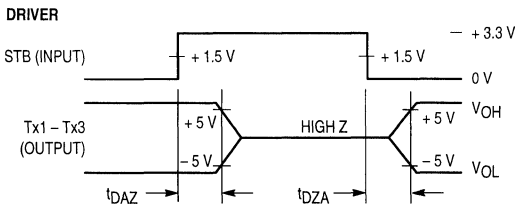
Tx1, Tx2, Tx3
Transmit Data Output (Pins 10, 12, 14)

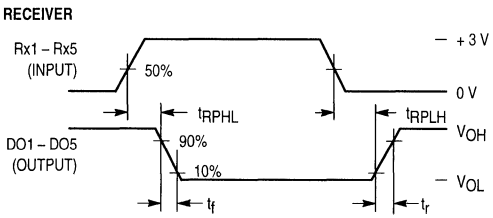
These are the EIA–232–E transmit signal output pins, which swing toward V_{DD} and V_{SS}. A logic 1 at a DI input causes the corresponding Tx output to swing toward V_{SS}. The actual levels and slew rate achieved will depend on the output loading (R_L/C_L).

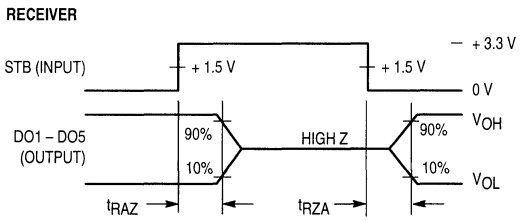
The minimum output impedance is 300 Ω when turned off.

SWITCHING CHARACTERISTICS









ESD PROTECTION

ESD protection on IC devices that have their pins accessible to the outside world is essential. High static voltages applied to the pins when someone touches them either directly or indirectly can cause damage to gate oxides and transistor junctions by coupling a portion of the energy from the I/O pin to the power supply buses of the IC. This coupling will usually occur through the internal ESD protection diodes which are designed to do just that. The key to protecting the IC is to shunt as much of the energy to ground as possible before it enters the IC. Figure 1 shows a technique which will clamp the ESD voltage at approximately ± 15 V using the MMBZ15VDLT1. Any residual voltage which appears on the supply pins is shunted to ground through the capacitors C1 and C2.

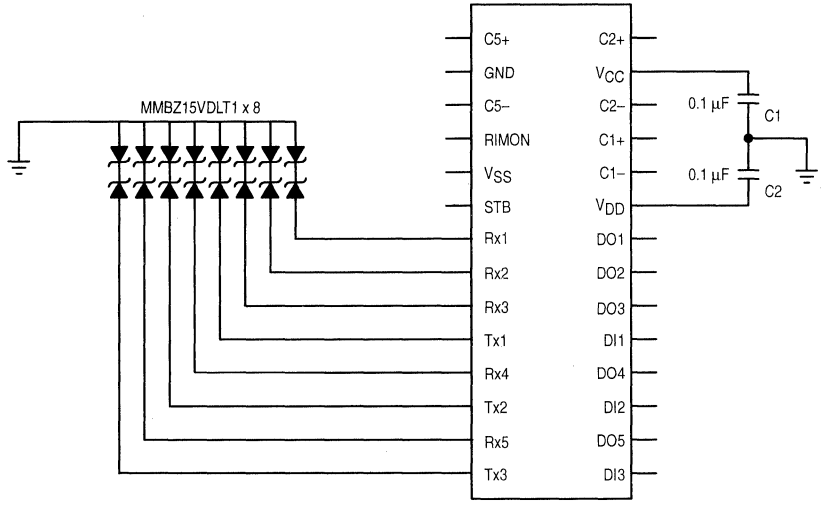


Figure 1. ESD Protection Scheme

MC145705
MC145706
MC145707

Product Preview

5 Volt Only Driver/Receiver with an Integrated Standby Mode

EIA–232–E and CCITT V.28

The MC145705/06/07 are a series of silicon–gate CMOS transceiver ICs that fulfill the electrical specifications of EIA–232–E and CCITT V.28 while operating from a single + 5 V power supply. These transceiver series are high performance and low power consumption devices that are equipped with standby and output enable function.

A voltage doubler and inverter convert the + 5 V to ± 10 V. This is accomplished through an on–board 20 kHz oscillator and four inexpensive external electrolytic capacitors.

The MC145705 is composed of two drivers and three receivers, the MC145706 has three drivers and two receivers, and the MC145707 has three drivers and three receivers. These drivers and receivers are virtually identical to those of the MC145407.

Available Driver/Receiver Combinations

Device	Drivers	Receivers	No. of Pins
MC145705	2	3	20
MC145706	3	2	20
MC145707	3	3	24

Drivers:

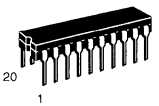
- ± 7.5 Output Swing
- 300 Ω Power–Off Impedance
- Output Current Limiting
- TTL and CMOS Compatible Inputs
- Three–State Outputs During Standby Mode
- Hold Output OFF (MARK) State by TxEN Pin

Receivers:

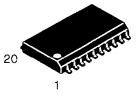
- ± 25 V Input Range
- 3 to 7 kΩ Input Impedance
- 0.8 V Hysteresis for Enhanced Noise Immunity
- Three–State Outputs During Standby Mode

Charge Pumps:

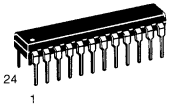
- + 5 to ± 10 V Dual Charge Pump Architecture
- Supply Outputs Capable of Driving Three Drivers on the MC145403/06 Simultaneously
- Requires Four Inexpensive Electrolytic Capacitors
- On–Chip 20 kHz Oscillators



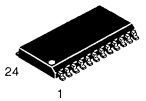
P SUFFIX
PLASTIC DIP
CASE 738



DW SUFFIX
SOG PACKAGE
CASE 751D



P SUFFIX
PLASTIC DIP
CASE 724



DW SUFFIX
SOG PACKAGE
CASE 751E

ORDERING INFORMATION

MC145705P	Plastic DIP
MC145706P	Plastic DIP
MC145707P	Plastic DIP
MC145705DW	SOG Package
MC145706DW	SOG Package
MC145707DW	SOG Package

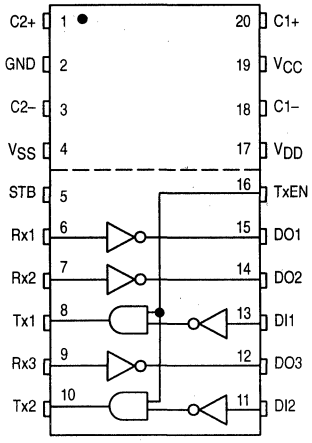
2

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

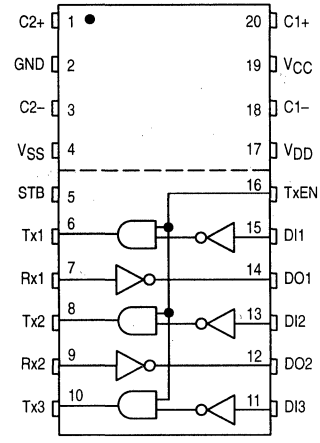
REV 1
8/95

PIN ASSIGNMENTS

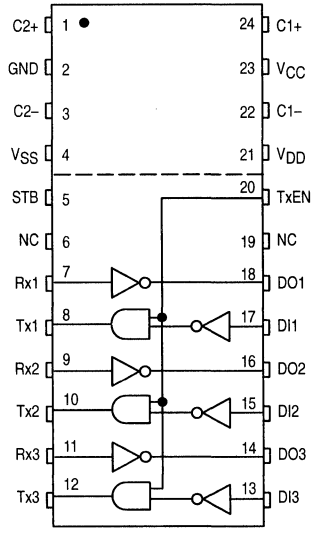
MC145705
2 DRIVERS/3 RECEIVERS



MC145706
3 DRIVERS/2 RECEIVERS



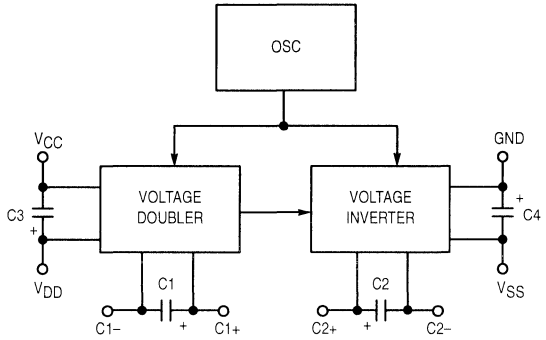
MC145707
3 DRIVERS/3 RECEIVERS



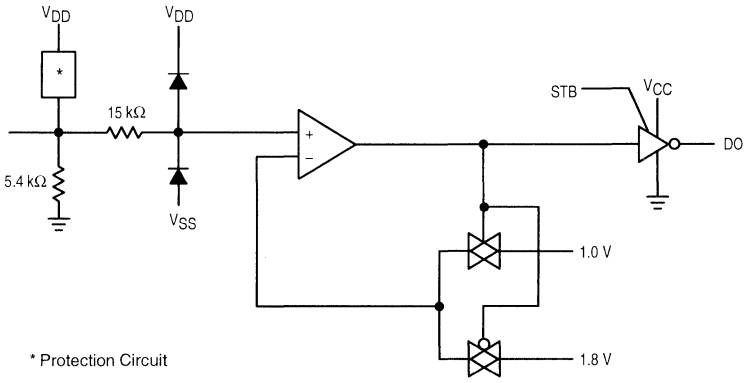
NC = NO CONNECTION

FUNCTION DIAGRAM

CHARGE PUMPS

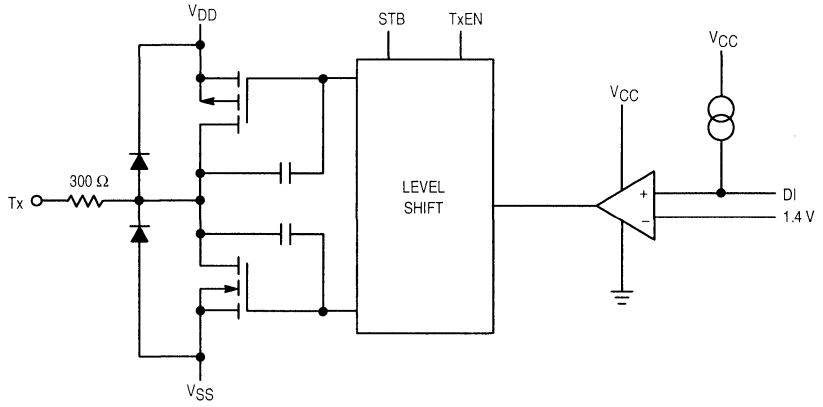


RECEIVER



* Protection Circuit

DRIVER



MAXIMUM RATINGS (Voltage Polarities Referenced to GND)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{CC}	– 0.5 to + 6.0	V
Input Voltage Rx1 – Rx3 Inputs DI1 – DI3 Inputs	V_{IR}	V_{SS} – 15 to V_{DD} + 15 0.5 to V_{CC} + 15	V
DC Current per Pin	I	± 100	mA
Power Dissipation	P_D	1	W
Operating Temperature Range	T_A	– 40 to + 85	°C
Storage Temperature Range	T_{stg}	– 85 to + 150	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, it is recommended that the voltage at the DI and DO pins be constrained to the range $GND \le V_{DI} \le V_{DD}$ and $GND \le V_{DO} \le V_{CC}$. Also, the voltage at the Rx pin should be constrained to $(V_{SS} - 15\ V) \le V_{Rx1 - Rx3} \le (V_{DD} + 15\ V)$, and Tx should be constrained to $V_{SS} \le V_{Tx1 - Tx3} \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., GND or V_{CC} for DI, and GND for Rx).

RECOMMENDED OPERATING LIMITS

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply	V_{CC}	4.5	5	5.5	V
Operating Temperature Range	T_A	– 40	—	85	°C

DC ELECTRICAL CHARACTERISTICS (Voltage polarities referenced to GND = 0 V; C1 – C4 = 10 µF; T_A = – 40 to + 85°C)

Parameter		Symbol	Min	Typ	Max	Unit
DC Power Supply		V_{CC}	4.5	5	5.5	V
Quiescent Supply Current (Output Unloaded, Input Low)		I_{CC}	—	1.7	3.5	mA
Quiescent Supply Current (Standby Mode) (Output Unloaded, Input Open)		$I_{CC(STB)}$	—	< 10	20	µA
Control Signal Input Voltage (STB, TxEN)	Logic Low Logic High	V_{IL} V_{IH}	— V_{CC} – 0.5	— —	0.5 —	V
Control Signal Input Current	Logic Low (TxEN) Logic High (STB)	I_{IL} I_{IH}	— —	— —	– 10 10	µA
Charge Pumps Output Voltage (C1, C2, C3, C4 = 10 µF)						V
Output Voltage (V_{DD})	I_{load} = 0 mA I_{load} = 5 mA I_{load} = 10 mA	V_{DD}	8.5 7.5 6.0	10.0 9.5 9.0	11 — —	
Output Voltage (V_{SS})	I_{load} = 0 mA I_{load} = 5 mA I_{load} = 10 mA	V_{SS}	– 8.5 – 7.5 – 6.0	– 10.0 – 9.2 – 8.6	– 11 — —	

RECEIVER ELECTRICAL SPECIFICATIONS

(Voltage polarities referenced to GND = 0 V; V_{CC} = + 5 V ± 10%; C1 – C4 = 10 µF; T_A = – 40 to + 85°C)

Parameter		Symbol	Min	Typ	Max	Unit
Input Turn–On Threshold ($V_{DO1 - DO3} = V_{OL}$)	Rx1 – Rx3	V_{on}	1.35	1.8	2.35	V
Input Turn–Off Threshold ($V_{DO1 - DO3} = V_{OH}$)	Rx1 – Rx3	V_{off}	0.75	1	1.25	V
Input Threshold Hysteresis ($V_{on} = V_{off}$)	Rx1 – Rx3	V_{hys}	0.6	0.8	—	V
Input Resistance		R_{in}	3	5.4	7	kΩ
High–Level Output Voltage (DO1 – DO3) $V_{Rx1 - Rx3}$ = – 3 to – 25 V	I_{out} = – 20 µA I_{out} = – 1 mA	V_{OH}	V_{CC} – 0.1 V_{CC} – 0.7	— 4.3	— —	V
Low–Level Output Voltage (DO1 – DO3) $V_{Rx1 - Rx3}$ = + 3 to + 25 V	I_{out} = + 20 µA I_{out} = + 1.6 mA	V_{OL}	— —	0.01 0.5	0.1 0.7	V

DRIVER ELECTRICAL SPECIFICATIONS

(Voltage polarities referenced to GND = 0 V; V_{CC} = + 5 V ± 10%; C1 – C4 = 10 µF; T_A = – 40 to + 85°C)

Parameter		Symbol	Min	Typ	Max	Unit
Digital Input Voltage	DI1 – DI3					V
Logic Low		V_{IL}	—	—	0.8	
Logic High		V_{IH}	2	—	—	
Input Current	DI1 – DI3					µA
V_{DI} = GND		I_{IL}	—	7	—	
V_{DI} = V_{CC}		I_{IH}	—	—	± 1.0	
Output High Voltage	Tx1 – Tx3	V_{OH}	6	7.5	—	V
($V_{DI1 – DI3}$ = Logic Low, R_L = 3 kΩ)	Tx1 – Tx6*		5	6.5	—	
Output Low Voltage	Tx1 – Tx3	V_{OL}	– 6	– 7.5	—	V
($V_{DI1 – DI3}$ = Logic High, R_L = 3 kΩ)	Tx1 – Tx6*		– 5	– 6.5	—	
Off Source Impedance	Tx1 – Tx3	Z_{off}	300	—	—	Ω
Output Short Circuit Current (V_{CC} = 5.5 V)		I_{SC}				mA
Tx1 – Tx3 Shorted to GND**			—	—	± 60	
Tx1 – Tx3 Shorted to ± 15 V***			—	—	± 100	

* Specifications for a MC14570X powering a MC145406 or MC145403 with three additional drivers/receivers.

** Specification is for one Tx output to be shorted at a time. Should all three driver outputs be shorted simultaneously, device power dissipation limits could be exceeded.

*** This condition could exceed package limitations.

SWITCHING CHARACTERISTICS (V_{CC} = + 5 V, ± 10%; C1 – C4 = 10 µF; T_A = – 40 to + 85°C)

Parameter		Symbol	Min	Typ	Max	Unit
Drivers						
Propagation Delay Time	Tx1 – Tx3	t_{PLH}				µs
Low–to–High (R_L = 3 kΩ, C_L = 50 pF or 2500 pF)			—	0.5	1	
High–to–Low (R_L = 3 kΩ, C_L = 50 pF or 2500 pF)		t_{PHL}	—	0.5	1	
Output Slew Rate	Tx1 – Tx3	SR				V/µs
Minimum Load (R_L = 7 kΩ, C_L = 0 pF)			—	± 6	± 30	
Maximum Load (R_L = 3 kΩ, C_L = 2500 pF)			—	± 5	—	
Output Disable Time		t_{DAZ}	—	4	10	µs
Output Enable Time		t_{DZA}	—	25	50	ms
Receivers						
Propagation Delay Time	DO1 – DO3	t_{PLH}				µs
Low–to–High			—	—	1	
High–to–Low		t_{PHL}	—	—	1	
Output Rise Time	DO1 – DO3	t_r	—	250	400	ns
Output Fall Time	DO1 – DO3	t_f	—	40	100	ns
Output Disable Time		t_{RAZ}	—	4	10	µs
Output Enable Time		t_{RZA}	—	25	50	ms

TRUTH TABLE

Drivers

DI	TxEN	STB	Tx
X	X	H	Z*
X	L	L	L
H	H	L	L
L	H	L	H

* $V_{SS} \leq V_{Tx} \leq V_{DD}$ X = Don't Care

Receivers

Rx	STB	DO
X	H	Z*
H	L	L
L	L	H

* GND ≤ V_{DO} ≤ V_{CC} X = Don't Care

PIN DESCRIPTIONS

V_{CC}
Digital Power Supply

This digital supply pin is connected to the logic power supply. This pin should have a 0.33 µF capacitor to ground.

GND
Ground

Ground return pin is typically connected to the signal ground pin of the EIA–232–D connector (Pin 7) as well as to the logic power supply ground.

V_{DD}
Positive Power Supply

This is the positive output of the on–chip voltage doubler and the positive power supply input of the driver/receiver sections of the device. This pin requires an external storage capacitor to filter the 50% duty cycle voltage generated by the charge pump.

V_{SS}
Negative Power Supply

This is the negative output of the on–chip voltage doubler/inverter and the negative power supply input of the driver/receiver sections of the device. This pin requires an external storage capacitor to filter the 50% duty cycle voltage generated by the charge pump.

TxEN
Output Enable

This is the driver output enable pin. When this pin is in logic low level, the condition of the driver outputs (Tx1 – Tx3) are in keep OFF (mark) state.

STB
Standby

The device enters the standby mode while this pin is connected to the logic high level. During the standby mode, driver and receiver output pins become high impedance state. In this condition, supply current I_{CC} is below 10 µA (Typ) and can be operated with low current consumption.

C2+, C2–, C1+, C1–
Voltage Doubler and Inverter

These are the connections to the internal voltage doubler and inverter, which generate the V_{DD} and V_{SS} voltages.

Rx1, Rx2 (Rx3)
Receive Data Input

These are the EIA–232–E receive signal inputs. A voltage between + 3 and + 25 V is decoded as a space, and causes the corresponding DO pin to swing to ground (0 V). A voltage between – 3 and – 25 V is decoded as a mark, and causes the DO pin to swing up to V_{CC}.

DO1, DO2 (DO3)
Data Output

These are the receiver digital output pins, which swing from V_{CC} to GND. Each output pin is capable of driving one LSTTL input load.

Output level of these pins is high impedance while in standby mode.

DI1, DI2 (DI3)
Data Input

These are the high impedance digital input pins to the drivers. Input voltage levels on these pins must be between V_{CC} and GND.

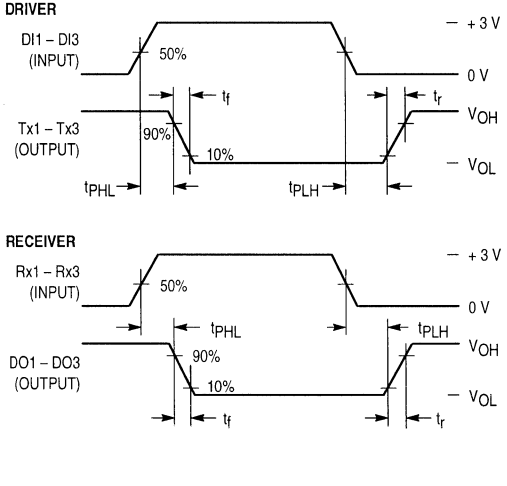
The level of these input pins are TTL/CMOS compatible.

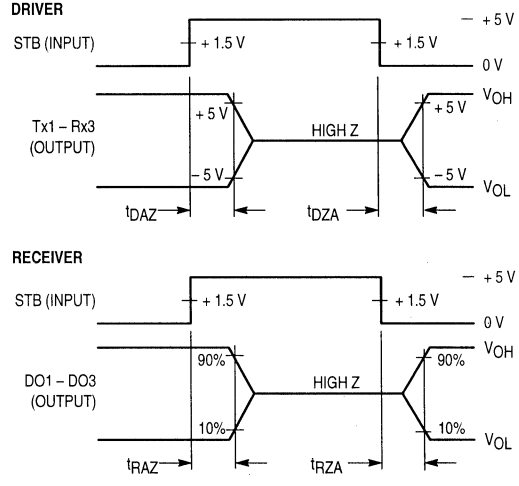
Tx1, Tx2 (Tx3)
Transmit Data Output

These are the EIA–232–E transmit signal output pins, which swing toward V_{DD} and V_{SS}. A logic 1 at a DI input causes the corresponding Tx output to swing toward V_{SS}. The actual levels and slew rate achieved will depend on the output loading (RL/CL).

The minimum output impedance is 300 Ω when turned off.

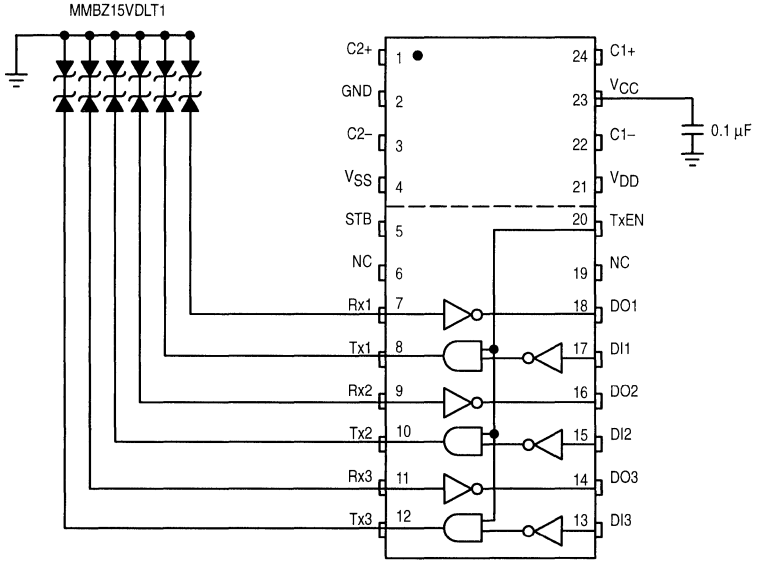
SWITCHING CHARACTERISTICS



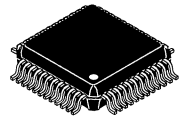


ESD PROTECTION

ESD protection on IC devices that have their pins accessible to the outside world is essential. High static voltages applied to the pins when someone touches them either directly or indirectly can cause damage to gate oxides and transistor junctions by coupling a portion of the energy from the I/O pin to the power supply buses of the IC. This coupling will usually occur through the internal ESD protection diodes which are designed to do just that. The key to protecting the IC is to shunt as much of the energy to ground as possible before it enters the IC. The figure below shows a technique which will clamp the ESD voltage at approximately ± 15 V using the MMBZ15VDLT1. Any residual voltage which appears on the supply pins is shunted to ground through the capacitors C1 and C2.



MC145750



VFU SUFFIX
PLASTIC VQFP
CASE 932

ORDERING INFORMATION
MC145750VFU VQFP

2

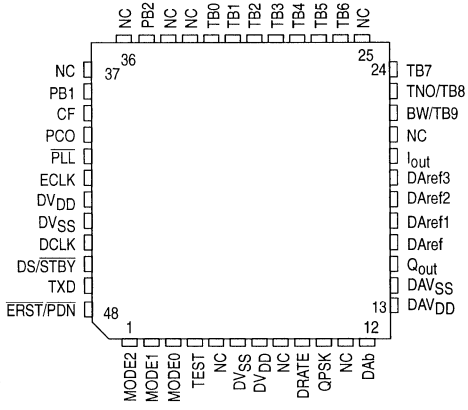
Product Preview

QPSK Encoder

The MC145750 is a silicon gate HCMOS device designed to encode π/4–shift QPSK baseband signals. The device contains two 10–bit DACs for the I/Q signal, Root–Nyquist digital filtering, and burst rising and falling edge processing for digital RF communication equipment. Primary applications for this device are in products that will be used in PHS (384 kbps) and PDC (42 kbps). It will perform up to 800 kbps data rate. It also contains PN511 random pattern generator and timing generator with PLL.

- Root–Nyquist Digital Filtering (Coefficient = 0.5)
- Burst Edge Processing Circuitry (Ramp–Up and –Down)
- Two 10–Bit DACs for I/Q Output
- Operating Voltage Range: 2.7 to 5.5 V
- PN511 Random Pattern Generator
- Conformance to RCR Standard for PHS, PDC
- Variable Data Transmission Rate up to 800 kbps (V_{DD} = 5 V)
- Timing Generator with PLL
- QPSK Mode, Burst, and Continuous I/Q Signal Output is Performed
- Companion Device is MRFIC0001

PIN ASSIGNMENT

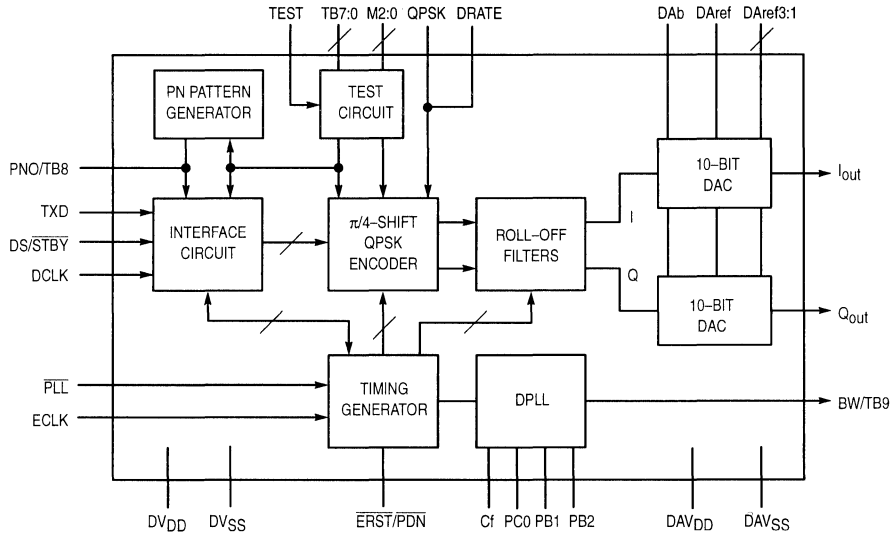


NC = NO CONNECTION

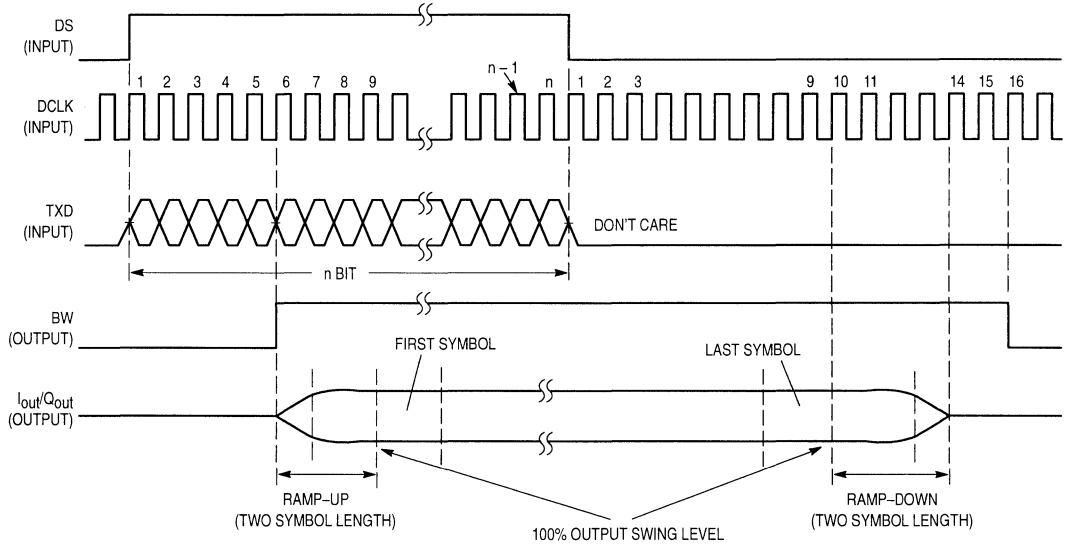
This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

REV 2
10/95

BLOCK DIAGRAM



INPUT/OUTPUT TIMING RELATIONS



MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	– 0.5 to + 7	V
DC Input Voltage	V_{in}	– 0.5 to V_{DD} + 0.5	V
Power Dissipation	P_D	500	mW
Storage Temperature	T_{stg}	– 65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

2

Parameter	Symbol	Min	Typ	Max	Unit
DC Supply Voltage	V_{DD}	2.7	3.3	5.5	V
DC Input Voltage	V_{in}	0	—	V_{DD}	V
Operating Temperature Range	T_A	– 20	25	85	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C, TXD = L, Normal Mode)

Parameters		Symbol	Condition	Min	Typ**	Max	Unit
DC Supply Current V_{DD} = 3 V		I_{dd1}	$\overline{ERST}$ = L	—	0.25	0.5	mA
	DRATE = L	I_{dd2}	DS = L	—	5.0	6.0	
	DRATE = H	I_{dd3}		—	1.5	1.8	
	DRATE = L	I_{dd4}	DS = Burst Input*	—	5.0	6.0	
	DRATE = H	I_{dd5}		—	1.5	1.8	
	DRATE = L	I_{dd6}	DS = Continual Input	—	8.0	10.0	
	DRATE = H	I_{dd7}		—	2.0	2.6	
DC Supply Current V_{DD} = 5 V		I_{dd1}	$\overline{ERST}$ = L	—	0.5	3.0	mA
	DRATE = L	I_{dd2}	DS = L	—	27.0	33.0	
	DRATE = H	I_{dd3}		—	17.0	19.0	
	DRATE = L	I_{dd4}	DS = Burst Input*	—	30.0	33.0	
	DRATE = H	I_{dd5}		—	18.0	20.0	
	DRATE = L	I_{dd6}	DS = Continual Input	—	33.0	37.0	
	DRATE = H	I_{dd7}		—	18.0	20.0	

*625 µs burst/5 ms period (DRATE = L) at DCLK = 384 kHz.
6.6 ms burst/20 ms period (DRATE = H) at DCLK = 42 kHz.
**Typical numbers are not guaranteed.

ANALOG CHARACTERISTICS (T_A = 25°C)

Parameters		Symbol	Condition	Min	Typ**	Max	Unit
Output Swing Level I/Q Out	V_{DD} = 3 V	V_{out}	RL = kΩ, TXD = L Normal Mode	500	550	600	mV p–p
	V_{DD} = 5 V			520	570	620	
Output Swing Imbalance		ΔV_{out}		– 0.5	0	0.5	dB
Output DC Level I/Q Out	V_{DD} = 3 V	V_{out}	DS = L	800	820	840	mV
	V_{DD} = 5 V			780	800	820	
Output Swing Imbalance		ΔV_{DD}		—	—	20	
Out–of–Band Noise Level	V_{DD} = 5 V	V_{in}	600 kHz	—	– 50	—	dB
			900 kHz	—	– 55	—	
DC Output Resistance		R_{out}	I_{out}/Q_{out}	—	50	100	Ω

*DAref1 = H at V_{DD} = 3 V, DAref3 = H at V_{DD} = 5 V
**Typical numbers are not guaranteed.

SWITCHING CHARACTERISTICS (T_A = 25°C)

Parameters		Symbol	Condition	Min	Typ*	Max	Unit
Input Voltage	High–Level	V_{IH}		V_{DD} x 0.7	—	—	V
	Low–Level	V_{IL}		—	—	V_{DD} x 0.3	
Output Voltage	High–Level	V_{OH}	BW, PNO	V_{DD} x 0.9	—	—	
	Low–Level	V_{OL}		—	—	V_{DD} x 0.1	
Data Set–Up Time		t_{su}	TXD, DS, STBY	10	—	—	ns
Data Hold Time		t_h	TXD, DS, STBY	10	—	—	
Data Output Propagation Delay		t_{pd}	BW, PNO	—	1.5	3	µs
I/Q Output Propagation Delay		T_D	I_{out}, Q_{out}	—	4	6	
Data Rate	V_{DD} = 3 V		DRATE = L	—	—	450	kbps
			DRATE = H	—	—	55	
	V_{DD} = 5 V		DRATE = L	—	—	800	
			DRATE = H	—	—	100	
Clock Input Duty Cycle		DCLK		45	50	55	%
VCO Oscillation Frequency	V_{DD} = 3 V	f_{VCO1}		—	—	20	MHz
	V_{DD} = 5 V	f_{VCO2}		—	—	32	

* Typical numbers are not guaranteed.

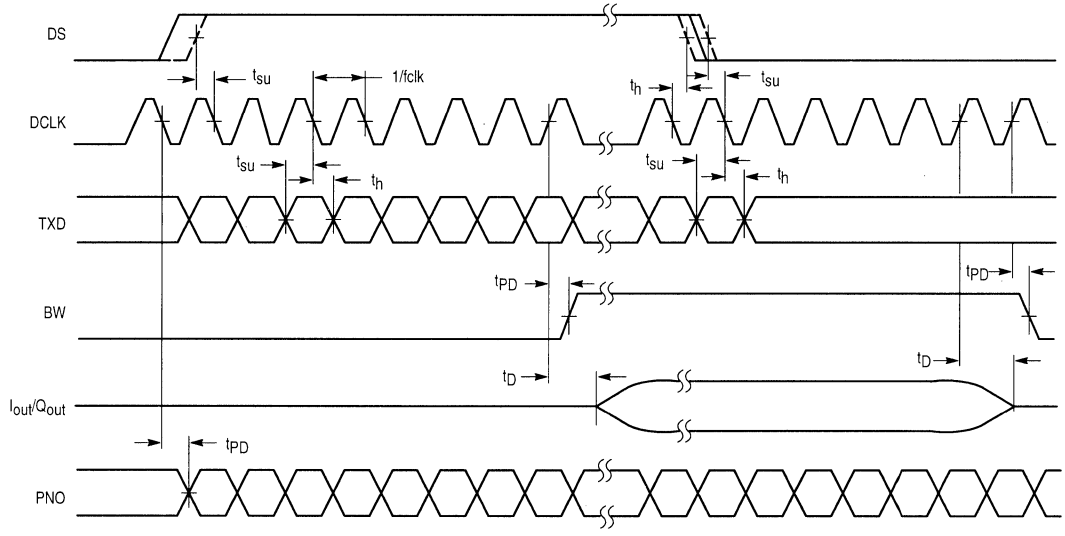


Figure 1. Timing Diagram

PIN DESCRIPTIONS

POWER SUPPLY

V_{SS}
Digital Ground (Pins 6, 44)

These are the negative power supply input pins to the digital portion of the device and are connected to ground (0 V).

V_{DD}
Positive Power Supply Input (Pins 7, 43)

These are the positive power supply input pins to the digital portion of the device. Typical operating voltage range is 3.3 V at DAref3 = H, 5.0 V at DAref1 = H. Power should be fed simultaneously with DAV_{DD} pin in order to avoid any possible damage to the device.

DAV_{DD}
Positive Power Supply Input for DACs (Pin 13)

This is the positive power supply input pin to the analog portion of the device. Typical operating voltage range is 2.7 V to 5.5 V.

DAV_{SS}
Analog Ground for DACs (Pin 14)

This is the negative power supply pin to the analog portion of the device and is connected to ground.

MODE CONTROL AND TEST

MODE0 – MODE2
Normal/Test Mode Select (Pins 1, 2, 3)

These pins must be connected to ground for normal operation. For system test, PN pattern generation mode will be performed when MODE0 = H and MODE1, MODE2 = L. PN511 signal is fed to the encoder instead of input data from TXD pin. Data shift timing is the same as the normal operation mode and burst timing indicated by DS pin is still valid for the device. The PN511 signal is monitored at the PNO pin.

TEST
Test Mode (Pin 4)

The device operates normally while this pin is held low. When this signal is high, the device enters into factory test mode. Only one mode is allowed to be enacted by user for PN Mode.

DRATE
Data–Rate Select (Pin 9)

This pin can select high data rate when it is low, such as in PHS applications.

QPSK
(D)QPSK/π/4–Shift QPSK Mode Select (Pin 10)

The device operates as a π/4–QPSK Encoder when this pin is held high. By making this pin low, it functions as non–shift differential QPSK Encoder. All of the functions are the same in both modes.

PN0/TB8
PN511 Test Pattern Output/Test Bus 8 (Pin 23)

This is the output data of PN511 test–pattern in normal mode. When the PN pattern generator outputs to this pin, it can be output I/Q pins and data from TXD pin may be ignored. If the DS signal is L, I/Q pins stop but PN data stream may be output.

TB0 – TB7
Test Bus (Pins 24, 26 – 32)

These pins are used in factory test and should be connected to ground for normal operation.

PLL
Int/Ext PLL Clock Select (Pin 41)

When this pin is connected to ground, the PLL is active and timing will be generated internally. When this pin is connected to V_{DD}, timing should be applied to the ECLK pin.

DIGITAL INTERFACE PINS

BW/TB9
Burst Window Output/Test Bus 9 (Pin 22)

This output indicates when modulated baseband I/Q signals are output from this device. This pin is used as the transmission control signal for saving power for RF.

ECLK
External Clock Input (Pin 42)

When the internal timing generator with PLL is not used in the system, this pin must have 15.36 MHz applied as a system clock for this device. This pin is connected to ground for normal operation.

DCLK
Data Shift Clock Input (Pin 45)

This is the shift clock input for the transmit data input and is typically 384 kHz for the PHS (DRATE Pin = L) and 42 kHz for the PDC (DRATE Pin = H) application. The data input occurs at the rising edge of the DCLK. For burst–type systems such as the TDMA data transmission applications, this signal must be synchronized with the rising/falling edge of the DS pin (Data Slot Timing Input).

DS/$\overline{\text{STBY}}$
Data Slot Timing/Standby Input (Pin 46)

For burst–type, this input signal indicates when transmit data are valid for the device. Its duration must be equal with the number of input data to the device, and its transition must be aligned with the rising edge of the DCLK signal.

When a logic L is applied to this pin, all digital portions except the timing generator are not clocked and the device is in a low power dissipation mode. When a logic H is applied continuously, all input data are encoded as valid data.

TXD
Transmit Data Input (Pin 47)

Data bit streams to be transmitted are input to this pin. The data is valid only when the DS (Pin 46) is asserted (high). Its transition should be synchronized with rising edge of the DCLK (Pin 45).

$\overline{\text{ERST/PDN}}$
External Reset/Power Down Input (Pin 48)

When a logic L is applied to this pin, it forces a complete power down. When at start up, V_{DD} goes high, it is recommended that a logic L. then a logic H be applied to this pin to start up and reset all digital portions.

ANALOG INTERFACE PINS

Q_{out}
Filtered Quadrature–Phase Output (Pin 15)

This is the modulated quadrature–phase signal output and the amplitude is typically 550 mV p–p at V_{DD} = 3 V in PN test mode. The output dc resistance is approximately 50 Ω.

I_{out}
Filtered In–Phase Output (Pin 20)

This is the modulated in–phase signal output and amplitude is typically 500 mV p–p at V_{DD} = 3 V in PN test mode. The output dc resistance is approximately 50 Ω.

DAC AND PLL SETTING

DAb
Reference Bias Setting Pin to DACs (Pin 12)

A resistor connected to ground from this pin determines the reference current value for internal DACs. This resistor's value is 200 kΩ typically.

DAref
Ripple Filter Capacitor (Pin 16)

A capacitor connected to ground from this pin acts as a ripple filter for the internal DACs' reference voltage. This capacitor's value is 0.1μF, typically.

DAref1 – DAref3
Reference Bias Setting to DACs (Pin 17 – 19)

These pins determine the reference voltage for internal DACs in conjunction with DAb pin. At 3 V operation, DAref1 pin should be connected to V_{DD}. DAref2 pin should be connected to V_{DD} at 3.3 V. DAref3 pin should be connected to V_{DD} at 5 V. The two other pins for the respective cases must be left open.

PB1, PB2
PLL Bias (Pins 35, 38)

This pin determines the bias of the PLL. Its recommended values are shown in Table 1 and it depends on operating voltage.

Cf
Loop Filter Capacitor (Pin 39)

Input from Cf pin is fed directly as the internal VCO control signal.

PCO
Phase Comparator Output (Pin 40)

Connect an LPF as loop filter for the PLL. Refer to the application figure for recommended values.

Table 7. Function Table

Pin		L	H	Remarks
3	MODE0	Normal Mode	PN Pattern	These settings are independent of power supply.
10	QPSK	Non–Shift	/4–Shift	
9	DRATE	High Speed	Low Speed	To be determined setting high or low speed data rate.
17	DAref1	—	V_{DD} = 5 V	These pins should be held high depending on power supply voltage and others should be left open.
18	DAref2	—	V_{DD} 3.3 V	
19	DAref3	—	V_{DD} 3.0 V	
41	$\overline{\text{PLL}}$	PLL Operation Mode	Ext Clock Mode	In case of external clock mode, TX data rate must be set to a frequency of 1/40 when DRATE = L, and must be set to a frequency of 1/320 when DRATE = H. Max data rate is limited by power supply.
48	$\overline{\text{ERST/PDN}}$	Power Down	Normal Operation	Digital circuits reset condition will be released by rising edge of this input.

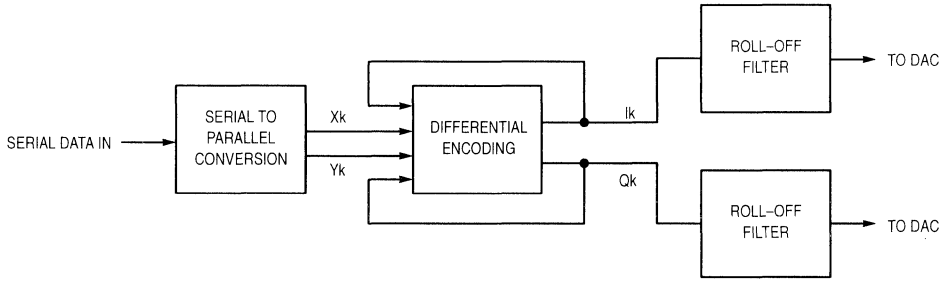


Figure 2. DQPSK Baseband Signal Generation

DEVICE DESCRIPTION

π/4–Shift QPSK Encoding

RCR standard (STD–28) specifies the basic configuration of this modulation scheme as shown in Figure 2. First, serial data input is converted to Xk/Yk parallel streams. Then its value is compared with one previous symbol Ik/Qk, respectively, whether or not there is a change of polarity. If there is a change, result is coded as 1. This two–bit πr (di–bit) is called symbol, hence symbol rate is just half of the data input rate to be modulated.

Phase transitions are determined as shown in Figure 3, with respect to four di–bit values of Xk, Yk. (As is shown, there should be at least π/4 of phase shift in each symbol timing unlike plain QPSK.) Actual in–phase outputs are fed to a quadrature modulator circuit, and it is recommended that a 2– to 3–order LPF be used, which may be used as a level shifter and dc offset compensation circuitry at the same time.

The reference voltage for the DACs is given by connecting either of DAref1:3 to V_{DD} according to the operating voltage used. It is preferable not to have this voltage vary, since I/Q output levels are affected.

Timing Generator

The PLL is intended in order to generate all required timing signals for the devices. The VCO oscillating at the PN511 pattern rate is utilized when some characteristics are measured. By pulling MODE0 pin high, the device generates this sequence. It is a useful simple measurement for the occupied power bandwidth and the out–of–band power level. The sequence itself can also be monitored at the PNO pin.

This circuit is reset by an external reset signal while the low–state of DS is not valid for initializing the generator.

START–UP SEQUENCE

To ensure stability and to initialize the internal ROM and encoder, the start–up sequence should be done at power–up. Refer to Figure 4.

Di–Bit Input

Xk	Yk	Phase Shift
0	0	π/4
0	1	3π/4
1	0	– π/4
1	1	– 3π/4

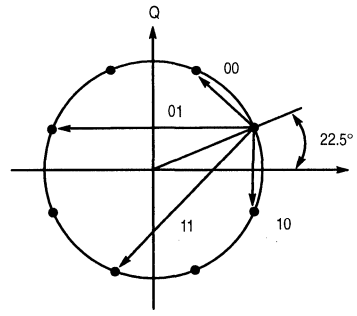


Figure 3. Phase Diagram

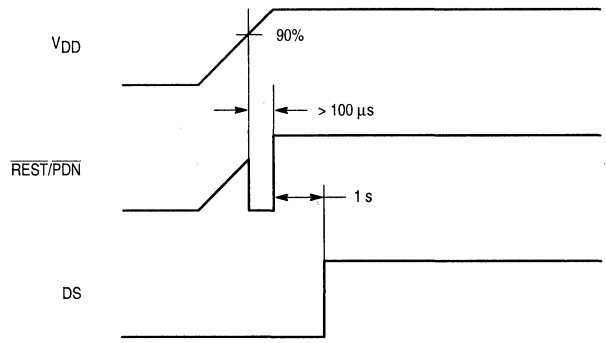


Figure 4. Start–Up Sequence

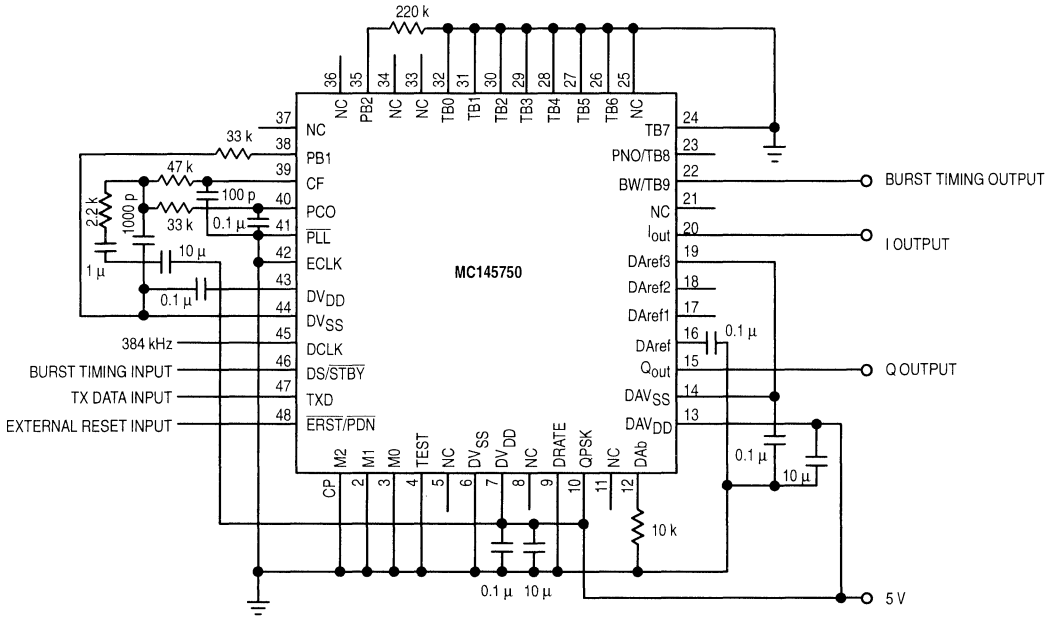


Figure 5. DRATE Equals L: 5 V Operation

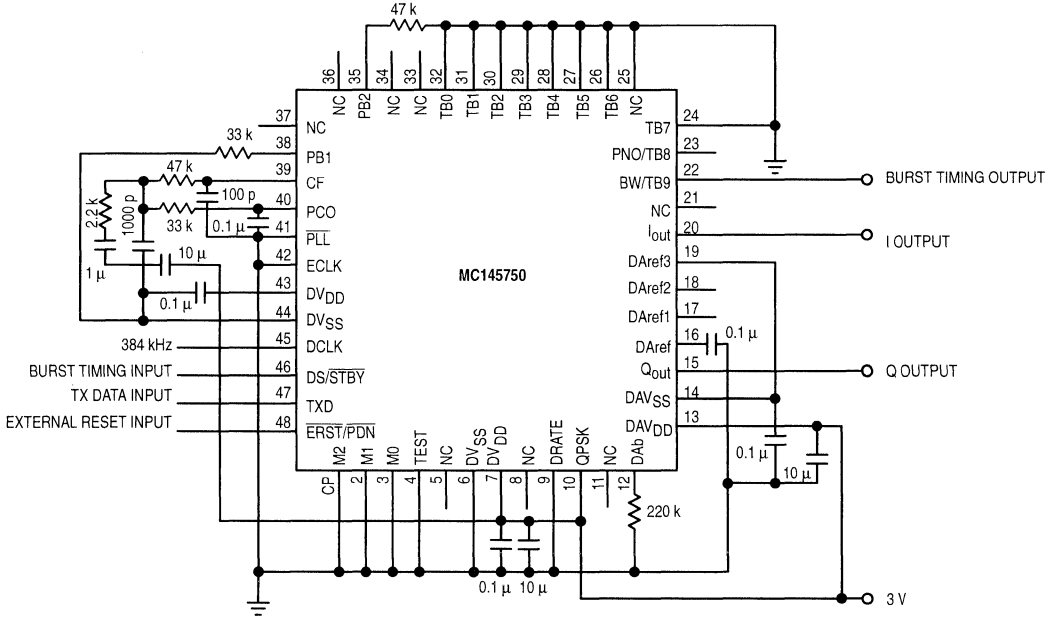


Figure 6. DRATE Equals H: 3 V Operation

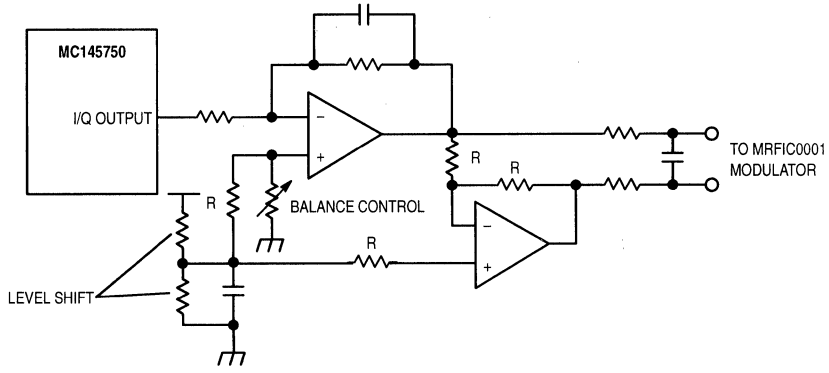


Figure 7. I/Q Output Interface Circuit 1

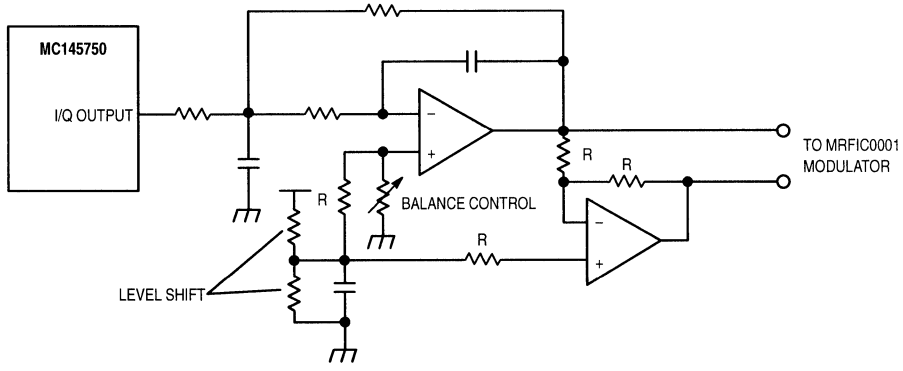
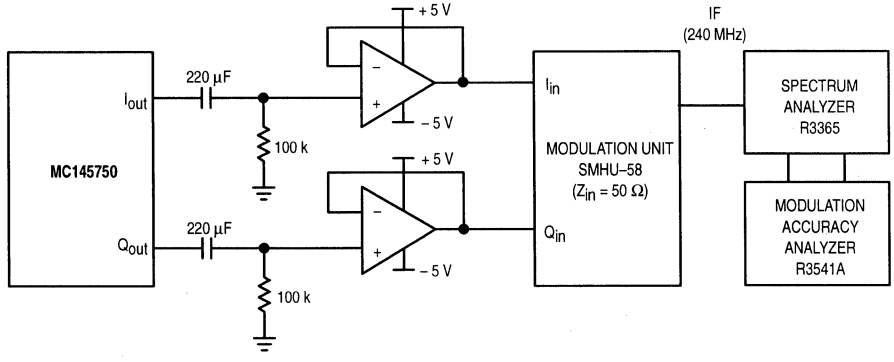


Figure 8. I/Q Output Interface Circuit 2



Measurement Equipment: Advantest Spectrum Analyzer R3365
Advantest Modulation Accuracy Analyzer R3541A
Rohde & Schwarz Modulation Unit SMHU–58

Conditions: Internal PLL mode, 384 kbps (PHS), T_A = 25°C

Motorola cannot recommend one supplier over another and in no way suggests that this is a complete listing of measurement equipment suppliers.

Figure 9. Modulation Accuracy Measurement Schematic

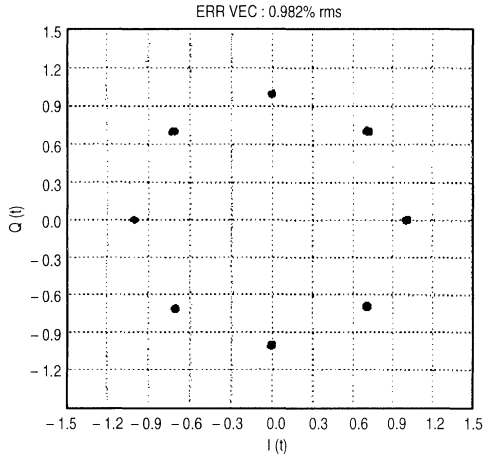


Figure 10. I–Q Pattern

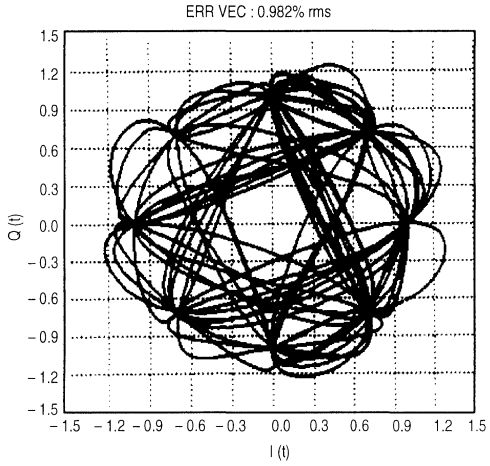


Figure 11. I–Q Pattern

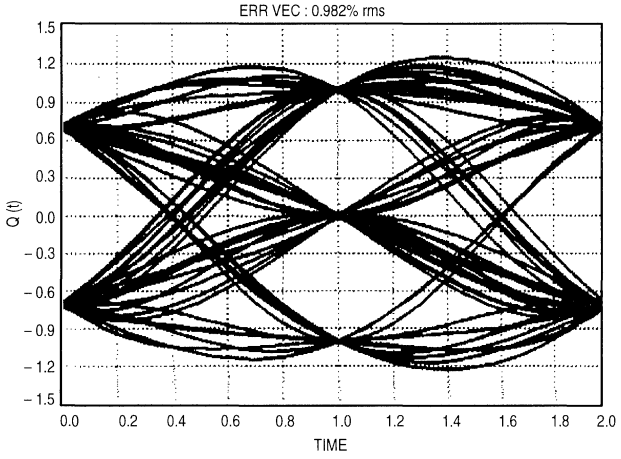


Figure 12. Q–Eye Pattern

MC68HC68T1

Real-Time Clock plus RAM with Serial Interface

CMOS

2

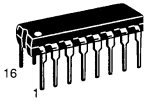
The MC68HC68T1 HCMOS Clock/RAM peripheral contains a real–time clock/calendar, a 32K x 8 static RAM, and a synchronous, serial, three–wire interface for communication with a microcomputer. Operating in a burst mode, successive Clock/RAM locations can be read or written using only a single starting address. An on–chip oscillator allows acceptance of a selectable crystal frequency or the device can be programmed to accept a 50/60 Hz line input frequency.

The LINE and system voltage (V_{SYS}) pins give the MC68HC68T1 the capability for sensing power–up/power–down conditions, a capability useful for battery–backup systems. The device has an interrupt output capable of signaling a microcontroller of an alarm, periodic interrupt, or power sense condition. An alarm can be set for comparison with the seconds, minutes, and hours registers. This alarm can be used in conjunction with the power supply enable (PSE) output to initiate a system power–up sequence if the V_{SYS} pin is powered to the proper level.

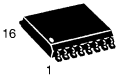
A software power–down sequence can be initiated by setting a bit in the interrupt control register. This applies a reset to the CPU via the $\overline{CPUR}$ pin, sets the clock out (CLKOUT) and PSE pins low, and disables the serial interface. This condition is held until a rising edge is sensed on the V_{SYS} input pin, signaling system power coming on, or by activation of a previously enabled interrupt if the V_{SYS} pin is powered up.

A watchdog circuit can be enabled that requires the microcomputer to toggle the slave select (SS) pin of the MC68HC68T1 periodically without performing a serial transfer. If this condition is not sensed, the $\overline{CPUR}$ line resets the CPU.

- Full Clock Features — Seconds, Minutes, Hours (AM/PM), Day–of–Week, Date, Month, Year (0 – 99), Auto Leap Year
- 32–Byte General Purpose RAM
- Direct Interface to Motorola SPI and National MICROWIRE™ Serial Data Ports
- Minimum Timekeeping Voltage: 2.2 V
- Burst Mode for Reading/Writing Successive Addresses in Clock/RAM
- Selectable Crystal or 50/60 Hz Line Input Frequency
- Clock Registers Utilize BCD Data
- Buffered Clock Output for Driving CPU Clock, Timer, Colon, or LCD Backplane
- Power–On Reset with First Time–Up Bit
- Freeze Circuit Eliminates Software Overhead During a Clock Read
- Three Independent Interrupt Modes — Alarm, Periodic, or Power–Down
- CPU Reset Output — Provides Orderly Power–Up/Power–Down
- Watchdog Circuit
- Pin–for–Pin Replacement for CDP68HC68T1
- Chip Complexity: 8500 FETs or 2125 Equivalent Gates
- Also See Application Notes ANE425, AN457, and AN1065



P SUFFIX
PLASTIC DIP
CASE 648

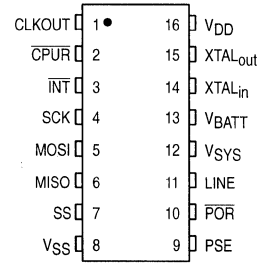


DW SUFFIX
SOG PACKAGE
CASE 751G

ORDERING INFORMATION

MC68HC68T1P	Plastic DIP
MC68HC68T1DW	SOG Package

PIN ASSIGNMENT



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REV 1 (Supercedes DL130)
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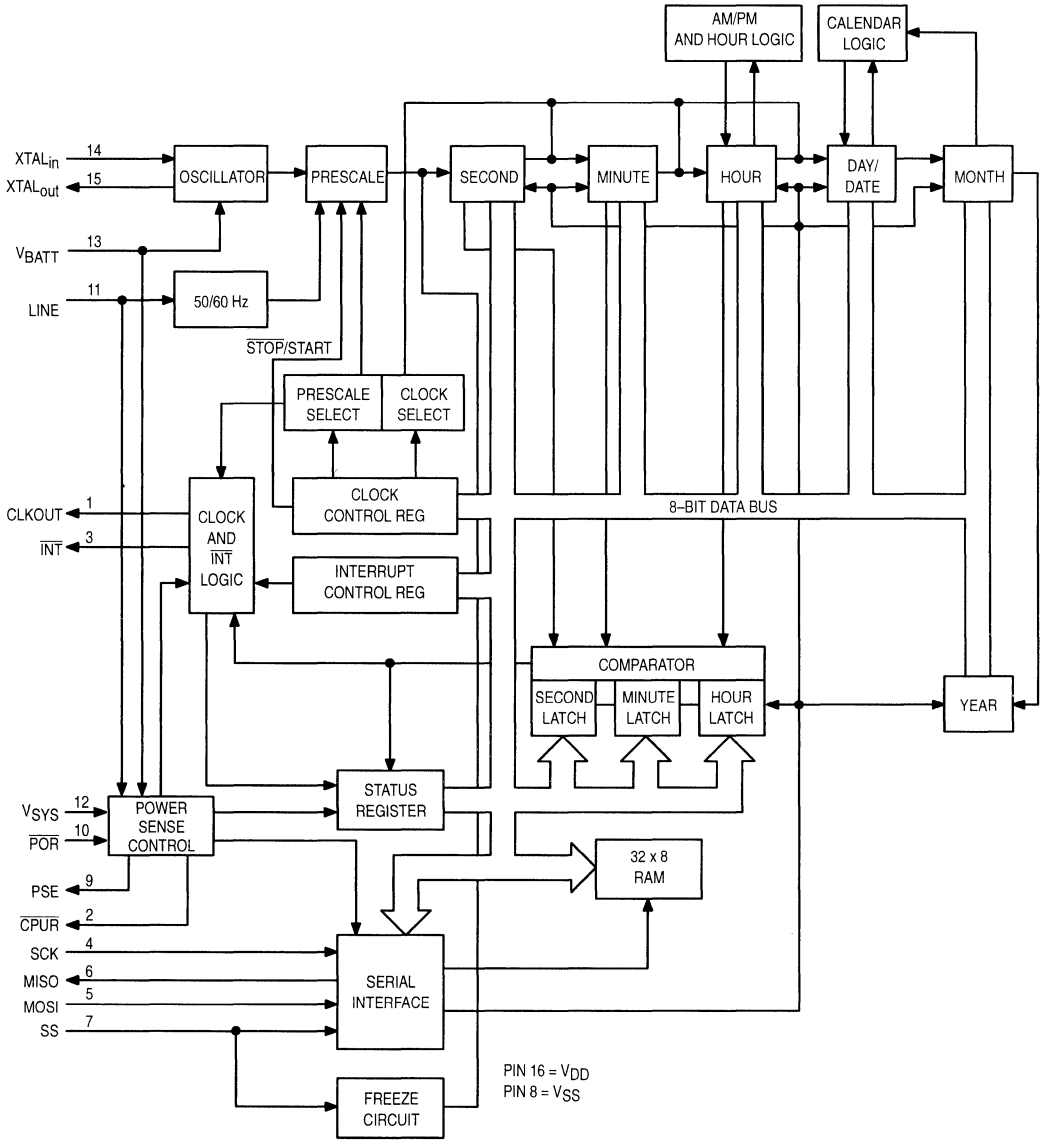
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	– 0.5 to + 7.0	V
V_{in}	DC Input Voltage (except Line Input**)	– 0.5 to V_{DD} + 0.5	V
V_{out}	DC Output Voltage	– 0.5 to V_{DD} + 0.5	V
I_{in}	DC Input Current, per Pin	± 10	mA
I_{out}	DC Output Current, per Pin	± 10	mA
I_{DD}	DC Supply Current, V_{DD} and V_{SS} Pins	± 30	mA
P_D	Power Dissipation, per Package***	500	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature (10–Second Soldering)	260	°C

* Maximum Ratings are those values beyond which damage to the device may occur.
** See Electrical Characteristics Table.
*** Power Dissipation Temperature Derating: — 12 mW/°C from 65 to 85°C.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{OI} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

ELECTRICAL CHARACTERISTICS (T_A = – 40 to + 85°C, Voltages Referenced to V_{SS})

Symbol	Parameter	Test Condition	V_{DD} V	Guaranteed Limit	Unit
V_{DD}	Power Supply Voltage Range		—	3.0 to 6.0	V
$V_{(stdby)}$	Minimum Standby (Timekeeping) Voltage*		—	2.2	V
V_{IL}	Maximum Low–Level Input Voltage		3.0 4.5 6.0	0.9 1.35 1.8	V
V_{IH}	Minimum High–Level Input Voltage		3.0 4.5 6.0	2.1 3.15 4.2	V
V_{in}	Maximum Input Voltage, Line Input	Power Sense Mode	5.0	12	V p–p
V_{OL}	Maximum Low–Level Output Voltage	I_{out} = 0 μA I_{out} = 1.6 mA	4.5	0.1 0.4	V
V_{OH}	Minimum High–Level Output Voltage	I_{out} = 0 μA I_{out} = 1.6 mA	4.5	4.4 3.7	V
I_{in}	Maximum Input Current, Except SS	$V_{in} = V_{DD}$ or V_{SS}	6.0	± 1	μA
I_{IL}	Maximum Low–Level Input Current, SS	$V_{in} = V_{SS}$	6.0	– 1.0	μA
I_{IH}	Maximum Pull–Down Current, SS	$V_{in} = V_{DD}$	6.0	100	μA
I_{OZ}	Maximum Three–State Leakage Current	$V_{out} = V_{DD}$ or V_{SS}	6.0	± 10	μA
I_{DD}	Maximum Quiescent Supply Current	$V_{in} = V_{DD}$ or V_{SS}, All Input; I_{out} = 0 μA	6.0	50	μA
I_{DD}	Maximum RMS Operating Supply Current Crystal Operation	I_{out} = 0 μA, $V_{in} = V_{DD}$ or V_{ss}, all inputs except $XTAL_{in}$, Clock Out Disabled, No Serial Access Cycles; $f_{XTAL_{in}}$ = 32 kHz / 1 MHz / 2 MHz / 4 MHz	5.0	0.1 0.6 0.84 1.2	mA
	Maximum RMS Operating Supply Current External Frequency Source Driving $XTAL_{in}$, $XTAL_{out}$ Open	I_{out} = 0 μA, $V_{in} = V_{DD}$ or V_{ss}, Clock Out Disabled, No Serial Access Cycles; $f_{XTAL_{in}}$ = 32 kHz / 1 MHz / 2 MHz / 4 MHz	5.0	0.024 0.12 0.24 0.5	
I_{batt}	Maximum RMS Standby Current Crystal Operation	V_{BATT} = 3.0 V, V_{SYS} = 0.0 V, V_{DD} = 0.0 V, I_{out} = 0 μA, V_{in} = Don't Care, all inputs except $XTAL_{in}$, Clock Out Disabled, No Serial Access Cycles; $f_{XTAL_{in}}$ = 32 kHz / 1 MHz / 2 MHz / 4 MHz	0.0	25 250 360 600	μA

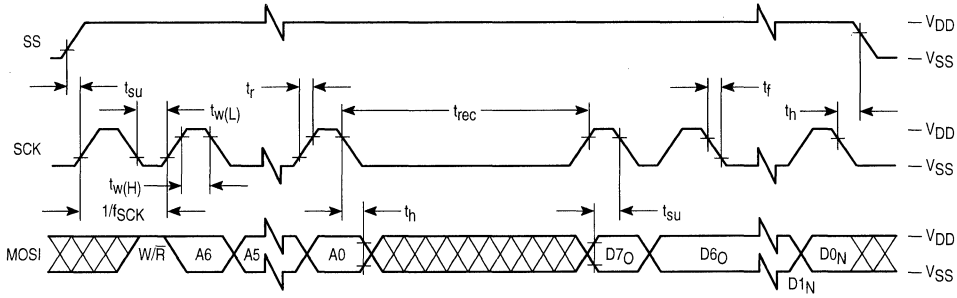
* Timekeeping function only, no read/write accesses. Data in the registers and RAM retained.

AC ELECTRICAL CHARACTERISTICS (T_A = – 40 to + 85°C, C_L = 200 pF, Input $t_r = t_f$ = 6 ns, Voltages Referenced to V_{SS})

Symbol	Parameter	Figure No.	V_{DD} V	Guaranteed Limit	Unit
f_{SCK}	Maximum Clock Frequency (Refer to SCK t_w, below)	1, 2, 3	3.0 4.5 6.0	— 2.1 2.1	MHz
t_{PLH}, t_{PHL}	Maximum Propagation Delay, SCK to MISO	2, 3	3.0 4.5 6.0	200 100 100	ns
t_{PLZ}, t_{PHZ}	Maximum Propagation Delay, SS to MISO	2, 4	3.0 4.5 6.0	200 100 100	ns
t_{PZL}, t_{PZH}	Maximum Propagation Delay, SCK to MISO	2, 4	3.0 4.5 6.0	200 100 100	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Measured Between 70% V_{DD} and 20% V_{DD})	2, 3	3.0 4.5 6.0	200 100 100	ns
C_{in}	Maximum Input Capacitance		—	10	pF

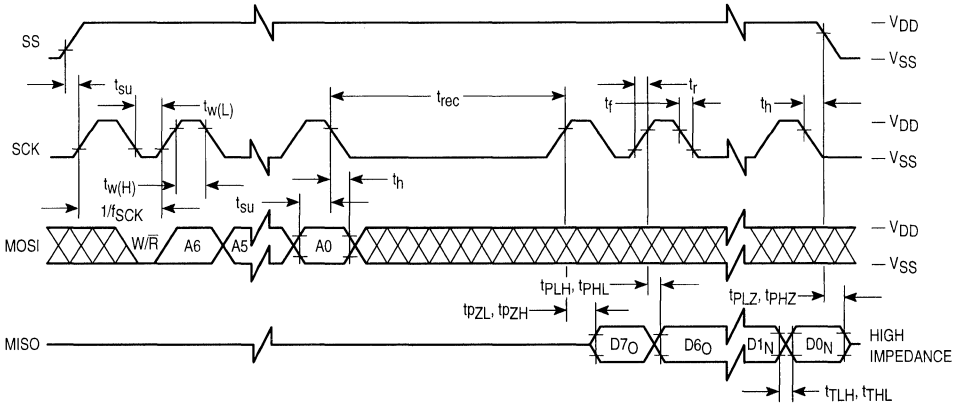
TIMING REQUIREMENTS (T_A = – 40 to + 85°C, Input $t_r = t_f$ = 6 ns, Voltages Referenced to V_{SS})

Symbol	Parameter	Figure No.	V_{DD} V	Guaranteed Limit	Unit
t_{su}	Minimum Setup Time, SS to SCK	1, 2	3.0 4.5 6.0	200 100 100	ns
t_{su}	Minimum Setup Time, MOSI to SCK	1, 2	3.0 4.5 6.0	200 100 100	ns
t_h	Minimum Hold Time, SCK to SS	1, 2	3.0 4.5 6.0	250 125 125	ns
t_h	Minimum Hold Time, SCK to MOSI	1, 2	3.0 4.5 6.0	200 100 100	ns
t_{rec}	Minimum Recovery Time, SCK	1, 2	3.0 4.5 6.0	200 200 200	ns
$t_{w(H)}$, $t_{w(L)}$	Minimum Pulse Width, SCK	1, 2	3.0 4.5 6.0	400 200 200	ns
t_w	Minimum Pulse Width, $\overline{POR}$		3.0 4.5 6.0	— 100 100	ns
t_r, t_f	Maximum Input Rise and Fall Times (Except $XTAL_{in}$ and $\overline{POR}$) (Measured Between 70% V_{DD} and 20% V_{DD})	1, 2	3.0 4.5 6.0	— 2 2	μs



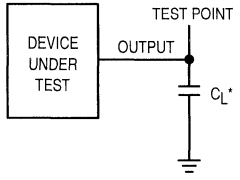
NOTE: Measurement points are V_{IL} and V_{IH} unless otherwise noted on the **AC Electrical Characteristics** table.

Figure 1. Write Cycle



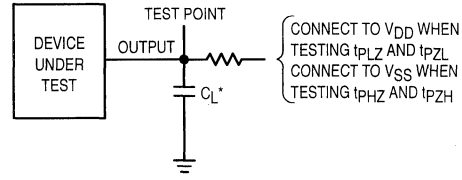
NOTE: Measurement points are V_{OL}, V_{OH}, V_{IL}, and V_{IH} unless otherwise noted on the **AC Electrical Characteristics** table.

Figure 2. Read Cycle



* Includes all probe and fixture capacitance.

Figure 3. Test Circuit



* Includes all probe and fixture capacitance.

Figure 4. Test Circuit

OPERATING CHARACTERISTICS

The real–time clock consists of a clock/calendar and a 32K x 8 RAM (see Figure 5). Communication with the device may be established via a serial peripheral interface (SPI) or MICROWIRE bus. In addition to the clock/calendar data from seconds to years, and systems flexibility provided by the 32–byte RAM, the clock features computer handshaking with an interrupt output and a separate square–wave clock output that can be one of seven different frequencies. An alarm circuit is available that compares the alarm latches with the seconds, minutes, and hours time counters and activates the interrupt output when they are equal. The clock is specifically designed to aid in power–up/power–down applications and offers several pins to aid the designer of battery–backup systems.

CLOCK/CALENDAR

The clock/calendar portion of this device consists of a long string of counters that is toggled by a 1 Hz input. The 1 Hz input is derived from the on–chip oscillator that utilizes one of four possible external crystals or that can be driven by an external frequency source. The 1 Hz trigger to the counters can also be supplied by a 50 or 60 Hz source that is connected to the LINE input pin.

The time counters offer seconds, minutes, and hours data in 12– or 24–hour format. An AM/PM indicator is available that once set, toggles at 12:00 AM and 12:00 PM. The calendar counters consist of day of week, date of month, month, and year information. Data in the counters is in BCD format. The hours counter utilizes BCD for hours data plus bits for 12/24 hour and AM/PM modes. The seven time counters are read serially at addresses $20 through $26. The time counters are written to at addresses $A0 through $A6. (See Figures 5 and 6 and Table 1.)

32 x 8 GENERAL–PURPOSE RAM

The real–time clock also has a static 32 x 8 RAM. The RAM is read at addresses $00 through $1F and written to at addresses $80 through $9F (see Figure 5).

ALARM

The alarm is set by accessing the three alarm latches and loading the desired data. (See **Serial Peripheral Interface**.) The alarm latches consist of seconds, minutes, and hours registers. When their outputs equal the values of the seconds, minutes, and hours time counters, an interrupt is generated. The interrupt output goes low if the alarm bit in the status register is set and the interrupt output is activated after an alarm time is sensed (see **Pin Descriptions, $\overline{\text{INT}}$ Pin**). To preclude a false interrupt when loading the time counters, the alarm interrupt bit in the interrupt control register should be reset. This procedure is not required when the alarm time is being loaded.

WATCHDOG FUNCTION

When Watchdog (bit 7) in the interrupt control register is set high, the clock's slave select pin must be toggled at regular intervals without a serial data transfer. If SS is not toggled, the MC68HC68T1 supplies a CPU reset pulse at Pin 2 and Watchdog (bit 6) in the status register is set (see Figure 7). Typical service and reset times are shown in Table 2.

CLOCK OUT

The value in the three least significant bits of the clock control register selects one of seven possible output frequencies. (See **Clock Control Register**.) This square–wave signal is available at the CLKOUT pin. When the power–down operation is initialized, the output is reset low.

CONTROL REGISTER AND STATUS REGISTER

The operation of the real–time clock is controlled by the clock control and interrupt control registers, which are read/write registers. Another register, the status register, is available to indicate the operating conditions. The status register is a read–only register.

MODE SELECT

The voltage level that is present at the V_{SYS} input pin at the end of power–on reset selects the device to be in the single–supply mode or battery–backup mode.

Single–Supply Mode

If V_{SYS} is powered up when power–on reset is completed; CLKOUT, PSE, and $\overline{\text{CPUR}}$ are enabled high and the device is completely operational. $\overline{\text{CPUR}}$ is placed low if the voltage level at the V_{SYS} pin subsequently goes low. If CLKOUT, PSE, and $\overline{\text{CPUR}}$ are reset low due to a power–down instruction, V_{SYS} brought low and then powered high enables these outputs.

An example of the single–supply mode is where only one supply is available and V_{DD}, V_{BATT}, and V_{SYS} are tied together to the supply.

Battery–Backup Mode

If V_{SYS} is not powered up at the end of power–on reset, CLKOUT, PSE, $\overline{\text{CPUR}}$, and SS are disabled (CLKOUT, PSE, and $\overline{\text{CPUR}}$ low). This condition is held until V_{SYS} rises to a threshold (approximately 0.7 V) above V_{BATT}. CLKOUT, PSE, and $\overline{\text{CPUR}}$ are then enabled and the device is operational. If V_{SYS} falls below a threshold above V_{BATT}, the outputs CLKOUT, PSE, and $\overline{\text{CPUR}}$ are reset low.

An example of battery–backup operation occurs if V_{SYS} is tied to V_{DD} and V_{DD} is not receiving voltage from a supply. A rechargeable battery is connected to the V_{BATT} pin. The device retains data and keeps time down to a minimum V_{BATT} voltage of 2.2 V.

POWER CONTROL

Power control is composed of two operations, power–sense and power–down/power–up. Two pins are involved in power sensing, the LINE input pin and the $\overline{\text{INT}}$ output pin. Two additional pins, PSE and V_{SYS}, are utilized during power–down/power–up operation.

FREEZE FUNCTION

The freeze function prevents an increment of the time counters, if any of the registers are being read. Also, alarm operation is delayed if the registers are being read.

POWER SENSING

When power sensing is enabled (Power Sense Bit in the interrupt control register), ac/dc transitions are sensed at the LINE input pin. Threshold detectors determine when transitions cease. After a delay of 2.68 to 4.64 ms plus the external input RC circuit time constant, an interrupt true bit is set high in the status register. This bit can then be sampled to see if system power has turned back on (see Figure 8).

The power–sense circuitry operates by sensing the level of the voltage present at the LINE input pin. This voltage is centered around V_{DD}, and as long as the voltage is either plus or minus a threshold (approximately 0.7 V) from V_{DD}, a power sense failure is not indicated. With an ac signal present, remaining in this V_{DD} window longer than a maximum of 4.64 ms activates the power–sense circuit. The larger the amplitude of the signal, the less likely a power failure would be detected. A 50 or 60 Hz, 10 V p–p sine–wave voltage is an acceptable signal to present at the LINE input pin to set up the power–sense function. When ac power fails, an internal circuit pulls the voltage at the line pin within the detection window.

Power–Down

Power–down is a processor–directed operation. The power–down bit is set in the interrupt control register to initiate power–down operation. During power–down, the power supply enable (PSE) output, normally high, is placed low. The CLKOUT pin is placed low. The $\overline{CPUR}$ output, connected to the processor reset input pin, is also placed low. In addition, the serial interface (MOSI and MISO) is disabled (see Figure 9).

Power–Up

There are four methods that can initiate the power–up mode. Two of the methods require an interrupt to the microcomputer by programming the interrupt control register. The interrupts can be generated by the alarm circuit by setting the alarm bit and the appropriate alarm registers. Also, an interrupt can be generated by programming the periodic interrupt bits in the interrupt control register. V_{SYS} must be at 5 volts for this operation to occur.

The third method is by initiating the power sense circuit with the power sense bit in the interrupt control register set to sense power loss along with the V_{SYS} pin to sense subsequent power–up condition (see Figure 10). (Reference Figure 19 for application circuit for third method.)

The fourth method that initiates power–up occurs when the level on the V_{SYS} pin rises 0.7 V above the level of the V_{BATT} pin, after previously falling to the level of V_{BATT} while in the battery–backup mode. An interrupt is not generated when the fourth method is utilized.

While in the single–supply mode, power–up is initiated when the V_{SYS} pin loses power and then returns high. There is no interrupt generated when using this method (see Figure 11).

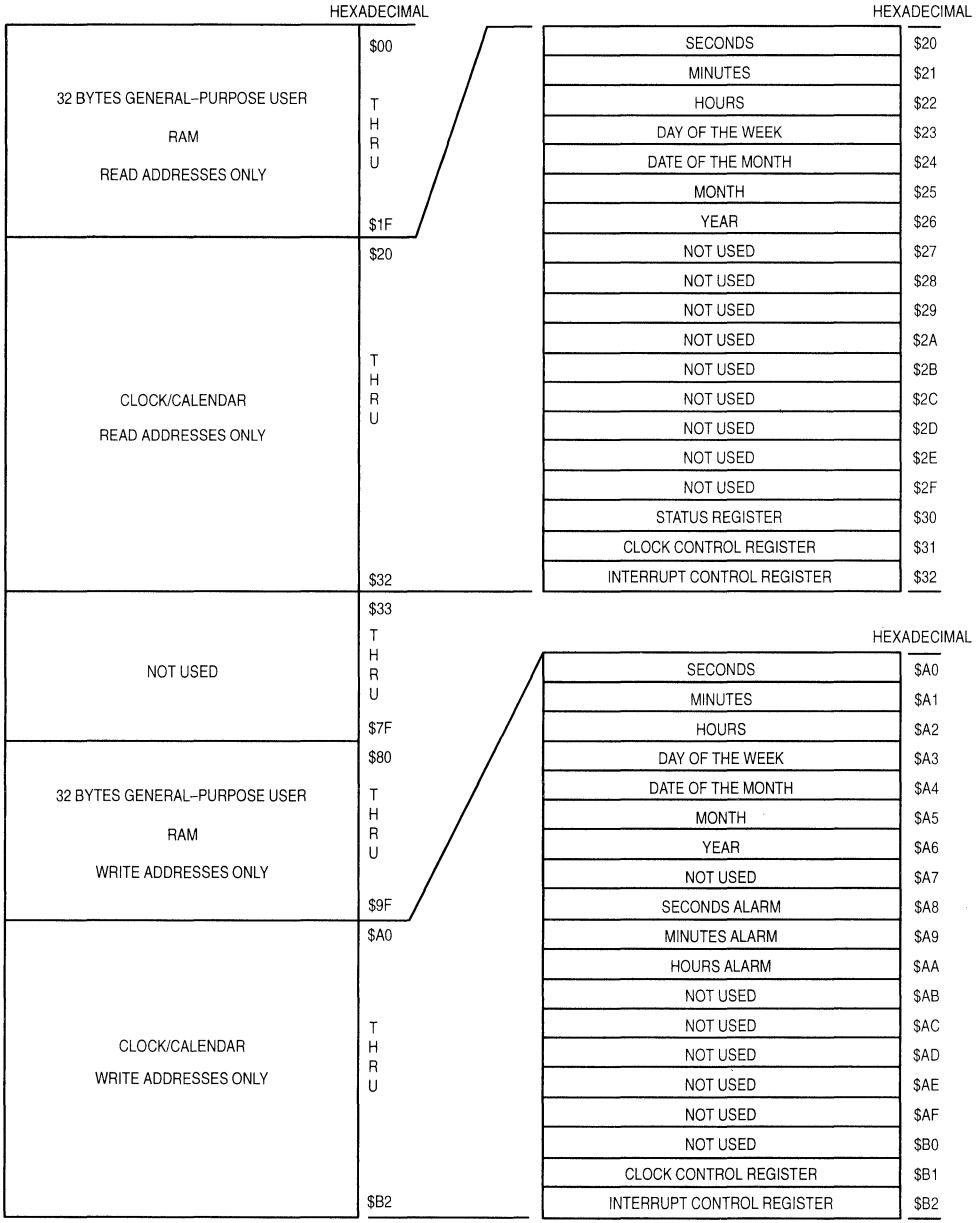
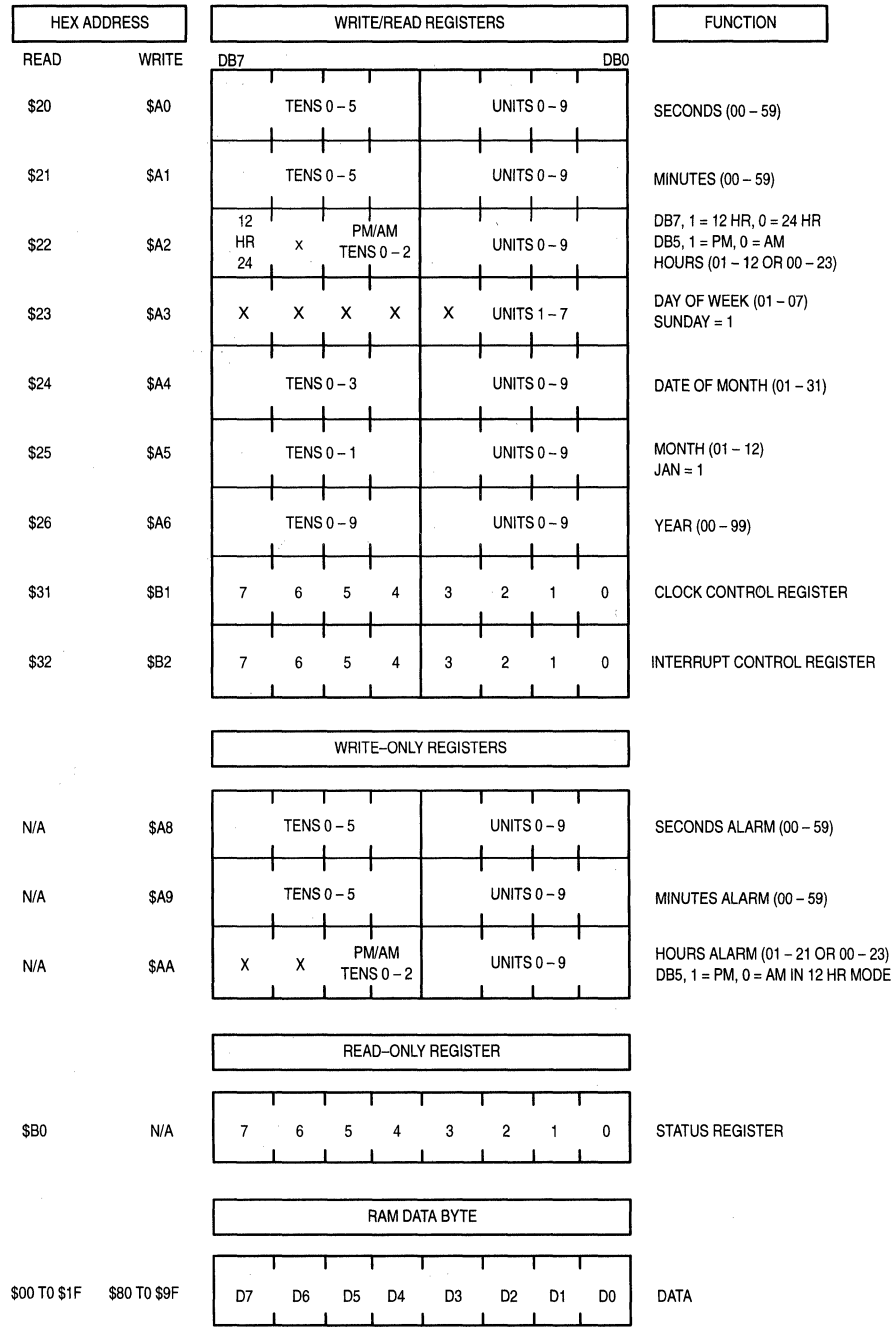


Figure 5. Address Map



NOTE:
X = Don't Care for Write
X = 0 for Read
N/A = Not Applicable

Figure 6. Clock/RAM Registers

Table 1. Clock/Calendar and Alarm Data Modes

Address Location		Function	Decimal Range	BCD Data Range	BCD Date* Example
Read	Write				
$20	$A0	Seconds	0 – 59	00 – 59	21
$21	$A1	Minutes	0 – 59	00 – 59	40
$22	$A2	Hours** (12 Hour Mode)	1 – 12	81 – 92 (AM) A1 – B2 (PM)	90
		Hours (24 Hour Mode)	0 – 23	00 – 23	10
$23	$A3	Day of Week (Sunday = 1)	1 – 7	01 – 07	03
$24	$A4	Date of Month	1 – 31	01 – 31	16
$25	$A5	Month (Jan = 1)	1 – 12	01 – 12	06
$26	$A6	Year	0 – 99	00 – 99	87
N/A	$A8	Seconds Alarm	0 – 59	00 – 59	21
N/A	$A9	Minutes Alarm	0 – 59	00 – 59	40
N/A	$AA	Hours Alarm*** (12 Hour Mode)	1 – 12	01 – 12 (AM) 21 – 32 (PM)	10
		Hours Alarm (24 Hour Mode)	0 – 23	00 – 23	10

N/A = Not Applicable

* Example: 10:40:21 AM, Tuesday, June 16, 1987.

** Most significant data bit, D7, is "0" for 24–hour mode and "1" for 12–hour mode. Data bit D5 is "1" for PM and "0" for AM in 12–hour mode.

*** Data bit D5 is "1" for PM and "0" for AM in 12–hour mode. Data bits D7 and D6 are Don't Cares.

Table 2. Watchdog Service and Reset Times

	50 Hz		60 Hz		XTAL	
	Min	Max	Min	Max	Min	Max
Service Time	—	10 ms	—	8.3 ms	—	7.8 ms
Reset Time	20 ms	40 ms	16.7 ms	33.3 ms	15.6 ms	31.3 ms

NOTE: Reset does not occur immediately after slave select is toggled. Approximately two clock cycles later, reset initiates.

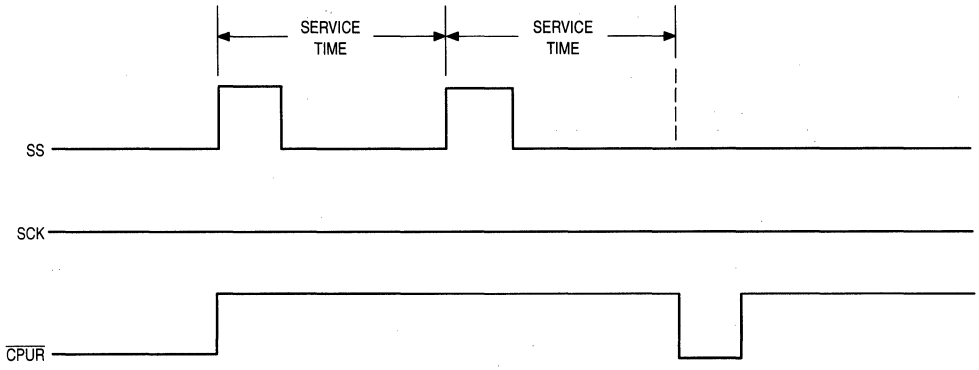
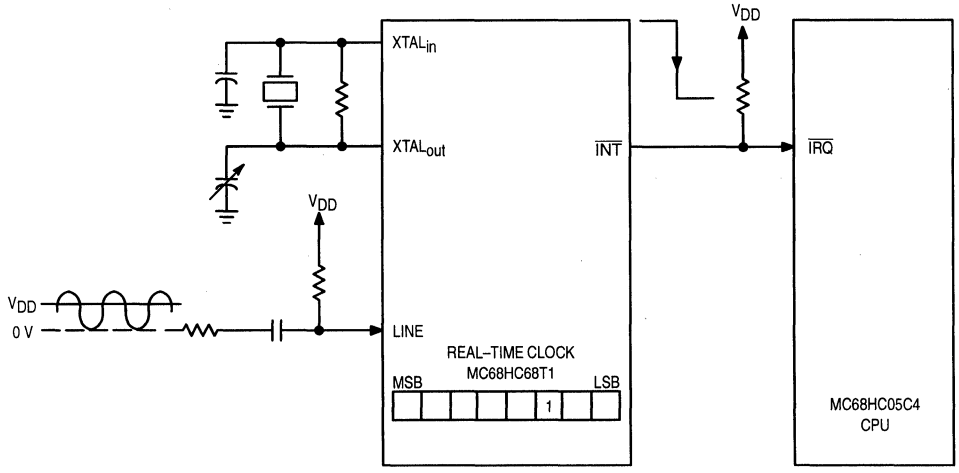


Figure 7. Watchdog Operation Waveforms



NOTE: A 60 Hz, 10 V p–p sine–wave voltage is an acceptable signal to present at the LINE input pin.

Figure 8. Power Sensing Functional Diagram

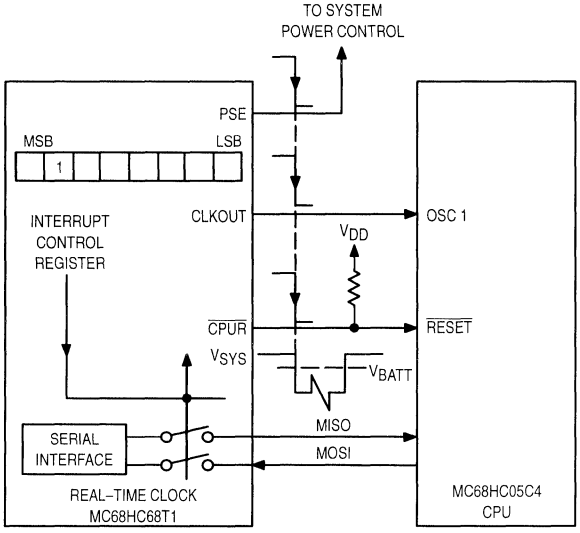
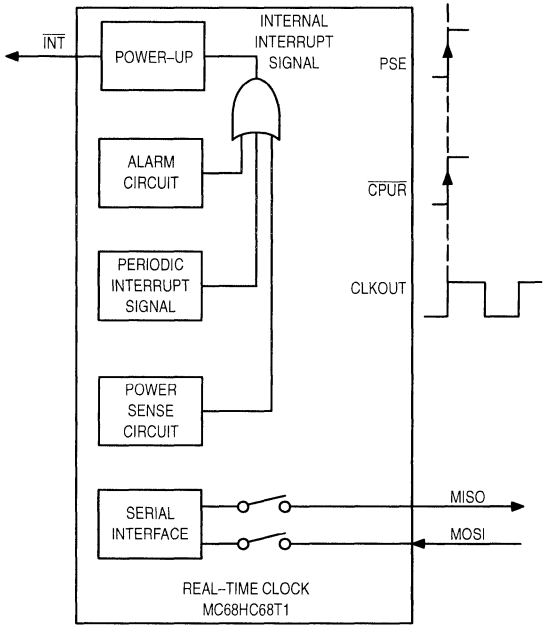


Figure 9. Power–Down Functional Diagram



NOTE: The V_{SYS} pin must be powered up.

Figure 10. Power–Up Functional Diagram
(Initiated by Internal Interrupt Signal Generation)

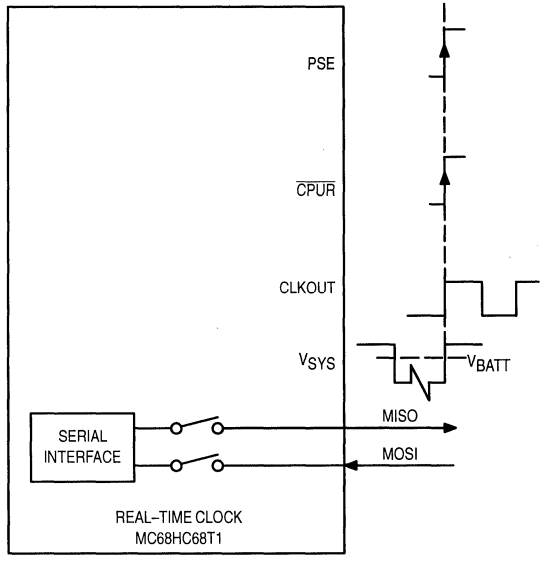


Figure 11. Power–Up Functional Diagram (Initiated by a Rise in Voltage on the V_{SYS} Pin)

PIN DESCRIPTIONS

CLKOUT
Clock Output (Pin 1)

This signal is the buffered clock output which can provide one of the seven selectable frequencies (or this output can be reset low). The contents of the three least significant bit positions in the clock control register determine the output frequency (50% duty cycle, except 2 Hz in the 50 Hz time–base mode). During power–down operation (Power–Down bit in the interrupt control register set high), the CLKOUT pin is reset low.

$\overline{\text{CPUR}}$
CPU Reset (Pin 2)

This pin provides an N channel, open–drain output and requires an external pullup resistor. This active low output can be used to drive the reset pin of a microprocessor to permit orderly power–up/power–down. The $\overline{\text{CPUR}}$ output is low from 15 to 40 ms when the watchdog function detects a CPU failure (see Table 2). The low level time is determined by the input frequency source selected as the time standard. $\overline{\text{CPUR}}$ is reset low when power–down is initiated.

$\overline{\text{INT}}$
Interrupt (Pin 3)

This active–low output is driven from a single N channel transistor and must be tied to an external pullup resistor. Interrupt is activated to a low level when any one of the following takes place:

1. Power sense operation is selected (Power Sense Bit in the interrupt control register is set high) and a power failure occurs.
2. A previously set alarm time occurs. The alarm bit in the status register and the interrupt signal are delayed 30.5 ms when 32 kHz or 1 MHz operation is selected, 15.3 ms for 2 MHz operation, and 7.6 ms for 4 MHz operation.
3. A previously selected periodic interrupt signal activates.

The status register must be read to reset the interrupt output after the selected periodic interval occurs. This is also true when conditions 1 and 2 activate the interrupt. If power–down has been previously selected, the interrupt also sets the power–up function only if power is supplied to the V_{SYS} pin to the proper threshold level above V_{BATT}.

SCK
Serial Clock (Pin 4)

This serial clock input is used to shift data into and out of the on–chip interface logic. SCK retains its previous state if the line driving it goes into a high–impedance state. In other words, if the source driving SCK goes to the high–impedance state, the previous low or high level is retained by on–chip control circuitry.

MOSI
Master Out Slave In (Pin 5)

The serial data present at this port is latched into the interface logic by SCK if the logic is enabled. Data is shifted in, either on the rising or falling edges of SCK, with the most significant bit (MSB) first.

In Motorola's microcomputers with SPI, the state of the CPOL bit determines which is the active edge of SCK. If SCK is high when SS goes high, the state of the CPOL bit is high. Likewise, if a rising edge of SS occurs while SCK is low (see Figure 13), then the CPOL bit in the microcomputer is low.

MOSI retains its previous state if the line driving it goes into high–impedance state. In other words, if the source

driving MOSI goes to the high–impedance state, the previous low or high level is retained by on–chip control circuitry.

MISO
Master In Slave Out (Pin 6)

The serial data present at this port is shifted out of the interface logic by SCK if the logic is enabled. Data is shifted out, either on the rising or falling edge of SCK, with the most significant bit (MSB) first. The state of the CPOL bit in the microcomputer determines which is the active edge of SCK (see Figure 13).

SS
Slave Select (Pin 7)

When high, the slave select input activates the interface logic; otherwise the logic is in a reset state and the MISO pin is in the high–impedance state. The watchdog circuit is toggled at this pin. SS has an internal pulldown device. Therefore, if SS is in a low state before going to high impedance, SS can be left in a high–impedance state. That is, if the source driving SS goes to the high–impedance state, the previous low level is retained by on–chip control circuitry.

V_{SS}
Negative Power Supply (Pin 8)

This negative power supply reference pin is connected to ground.

PSE
Power Supply Enable (Pin 9)

The power supply enable output is used to control system power and is enabled high under any one of the following conditions:

1. V_{SYS} rises above the V_{BATT} voltage after V_{SYS} is reset low by a system failure.
2. An interrupt occurs (if the V_{SYS} pin is powered up 0.7 V above V_{BATT}).
3. A power–on reset occurs (if the V_{SYS} pin is powered up 0.7 V above V_{BATT}).

PSE is reset low by writing a high into the power–down bit of the interrupt control register.

$\overline{POR}$
Power–On Reset (Pin 10)

This active–low Schmitt–trigger input generates an internal power–on reset signal using an external RC network (see Figures 18 through 21). Both control registers and frequency dividers for the oscillator and line inputs are reset. The status register is reset except for the first time–up bit (bit 4), which is set high. At the end of the power–on reset, single–supply or battery–backup mode is selected at this time, determined by the state of V_{SYS}.

LINE
Line Sense (Pin 11)

The LINE sense input can be used to drive one of two functions. The first function utilizes the input signal as the frequency source for the timekeeping counters. This function is selected by setting the line/$\overline{XTAL}$ bit high in the clock control register. The second function enables the LINE input to detect a power failure. Threshold detectors operating above and below V_{DD} sense an ac voltage loss. The Power Sense bit in the interrupt control register must be set high, and crystal or external clock source operation is required. The line/$\overline{XTAL}$ bit in the clock control register must be low to select crystal operation. When Power Sense is enabled, this pin, left unconnected, floats to V_{DD}.

This output has no ESD protection diode tied to V_{DD} which allows this pin's voltage to rise above V_{DD}. Care must be taken in the handling of this device.

V_{SYS}
System Voltage (Pin 12)

This input is connected to system voltage. The level on this pin initiates power–up if it rises 0.7 V above the level at the V_{BATT} input pin after previously falling below 0.7 V below V_{BATT}. When power–up is initiated, the PSE pin returns high and the CLKOUT pin is enabled. The $\overline{CPUR}$ output pin is also set high. Conversely, if the level of the V_{SYS} pin falls below V_{BATT} + 0.7 V, the PSE, CLKOUT, and $\overline{CPUR}$ pins are placed low. The voltage level present at this pin at the end of $\overline{POR}$ determines the device's operating mode.

V_{BATT}
Battery Voltage (Pin 13)

This pin is the *only* oscillator power source and should be connected to the positive terminal of the battery. The V_{BATT} pin **always** supplies power to the MC68HC68T1, even when the device is not in the battery–backup mode. To maintain timekeeping, the V_{BATT} pin must be at least 2.2 V. When the level on the V_{SYS} pin falls below V_{BATT} + 0.7 V, **V_{BATT} is internally connected to the V_{DD} pin.**

When the LINE input is used as the frequency source, the unused V_{BATT} and XTAL pins may be tied to V_{SS}. Alternatively, if V_{BATT} is connected to V_{DD}, $XTAL_{in}$ can be tied to either V_{SS} or V_{DD}.

This output has no ESD protection diode tied to V_{DD} which allows this pin's voltage to rise above V_{DD}. Care must be taken in the handling of this device.

$XTAL_{in}$, $XTAL_{out}$
Crystal Input/Output (Pins 14, 15)

For crystal operation, these two pins are connected to a 32.768 kHz, 1.048576 MHz, 2.097152 MHz, or 4.194304 MHz crystal. If crystal operation is not desired and Line Sense is used as frequency source, connect $XTAL_{in}$ to V_{DD} or V_{SS} (caution: see V_{BATT} pin description) and leave XTA_{out} open. If an external clock is used, connect the external clock to $XTAL_{in}$ and leave $XTAL_{out}$ open. The external clock must swing from at least 30 to 70% of ($V_{DD} - V_{SS}$). Preferably, this input should swing from V_{SS} to V_{DD}.

V_{DD}
Positive Power Supply (Pin 16)

For full functionality, the positive power supply pin may range from 3.0 to 6.0 V with respect to V_{SS}. To maintain timekeeping, the minimum standby voltage is 2.2 V with respect to V_{SS}. For proper operation in battery–backup mode, a diode **must** be placed in series with V_{DD}.

CAUTION

Data transfer to/from the MC68HC68T1 must not be attempted if the supply voltage falls below 3.0 V.

REGISTERS

CLOCK CONTROL REGISTER (READ/WRITE) — READ ADDRESS $31/WRITE ADDRESS $B1

MSB D7	D6	D5	D4	D3	D2	D1	LSB D0
START	LINE	XTAL SELECT	XTAL SELECT	50 Hz	CLK OUT	CLK OUT	CLK OUT
$\overline{\text{STOP}}$	$\overline{\text{XTAL}}$	1	0	$\overline{\text{60 Hz}}$	2	1	0

All bits are reset low by a power–on reset.

Start–$\overline{\text{Stop}}$

A high written into this bit enables the counter stages of clock circuitry. A low holds all bits reset in the divider chain from 32 Hz to 1 Hz. The clock out signal selected by bits D0, D1, and D2 is not affected by the stop function except the 1 and 2 Hz outputs.

Line/ $\overline{\text{XTAL}}$

When this bit is high, clock operation uses the 50 or 60 cycle input present at the LINE input pin. When the bit is low, the $XTAL_{in}$ pin is the source of the time update.

XTAL Select

Accommodation of one of four possible crystals are selected by the value in bits D4 and D5.

0 = 4.194304 MHz 2 = 1.048576 MHz

1 = 2.097152 MHz 3 = 32.768 kHz

The MC68HC68T1 has an on–chip 150 kΩ resistor that is switched in series with the internal inverter when 32 kHz is selected via the clock control register. At power–up, the device sets up for a 4 MHz oscillator and the series resistor is not part of the oscillator circuit. Until this resistor is switched in, oscillations may be unstable with the 32 kHz crystal. (See Figure 12.)

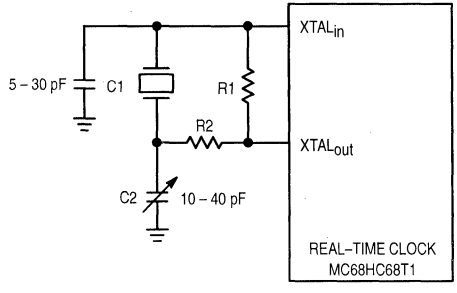


Figure 12. Recommended Oscillator Circuit (C1, C2 Values Depend Upon the Crystal Frequency)

Resistor R1 is recommended to be 10 MΩ for 32 kHz operation. Consult crystal manufacturer for R1 value for other frequencies. Resistor R2 must be used in 32 kHz operation only. Use a 200 to 300 kΩ range. This stabilizes the oscillator until the control register is set properly.

50 Hz – $\overline{\text{60 Hz}}$

50 Hz may be used as the input frequency at the LINE input when this bit is set high; a low accommodates 60 Hz. The power sense bit in the interrupt control register must be reset low for line frequency operation.

Clock Out

Three bits specify one of the seven frequencies to be used as the square–wave clock output (CLKOUT).

0 = XTAL 4 = Disable (low output)

1 = XTAL/2 5 = 1 Hz

2 = XTAL/4 6 = 2 Hz

3 = XTAL/8 7 = 50/60 Hz for LINE operation

7 = 64 Hz for XTAL operation

All bits in the clock control register are reset by a power–on reset. Therefore, XTAL is selected as the clock output at this time.

INTERRUPT CONTROL REGISTER (READ/WRITE) — READ ADDRESS $32/WRITE ADDRESS $B2

MSB D7	D6	D5	D4	D3	D2	D1	LSB D0
WATCH–DOG	POWER–DOWN	POWER SENSE	ALARM	PERIODIC SELECT			

All bits are reset low by power–on reset.

Watchdog

When this bit is set high, the watchdog operation is enabled. This function requires the CPU to toggle the SS pin periodically without a serial transfer requirement. In the event this does not occur, a CPU reset is issued at the $\overline{\text{CPUR}}$ pin. The status register must be read before re–enabling the watchdog function.

Power–Down

A high in this location initiates a power–down. A CPU reset occurs via the $\overline{\text{CPUR}}$ output, the CLKOUT and PSE output pins are reset low, and the serial interface is disabled.

Power Sense

When set high, this bit is used to enable the LINE input pin to sense a power failure. When power sense is selected, the input to the 50/60 Hz prescaler is disconnected; therefore, crystal operation is required. An interrupt is generated when a power failure is sensed and the power sense and interrupt true bit in the status register are set. When power sense is activated, a logic low must be written to this location followed by a high to re–enable power sense.

Alarm

The output of the alarm comparator is enabled when this bit is set high. When an equal comparison occurs between the seconds, minutes, and hours time counters and alarm latches, the interrupt output is activated. When loading the time counters, this bit should be reset low to avoid a false interrupt. This is not required when loading the alarm latches. See $\overline{\text{INT}}$ pin description for explanation of alarm delay.

Periodic Select

The value in these four bits (D0, D1, D2, and D3) selects the frequency of the periodic output (see Table 3).

Table 3. Periodic Interrupt Output Frequencies (at $\overline{INT}$ Pin)

D3 – D0 Value (Hex)	Periodic Interrupt Output Frequency	Frequency Timebase	
		XTAL	Line
0	Disable		
1	2048 Hz	X	
2	1024 Hz	X	
3	512 Hz	X	
4	256 Hz	X	
5	128 Hz	X	
6	64 Hz	X	
	50 or 60 Hz		X
7	32 Hz	X	
8	16 Hz	X	
9	8 Hz	X	
A	4 Hz	X	
B	2 Hz	X	X
C	1 Hz	X	X
D	1 Cycle per Minute	X	X
E	1 Cycle per Hour	X	X
F	1 Cycle per Day	X	X

STATUS REGISTER (READ ONLY) — ADDRESS $30

MSB D7	D6	D5	D4	D3	D2	D1	LSB D0
0	WATCH-DOG	0	FIRST TIME-UP	INTER-RUPT TRUE	POWER SENSE INT	ALARM INT	CLOCK INT

NOTE

All bits are reset low by a power–on reset except the first time–up bit which is set high. All bits except the power sense bit are reset after a read of the status register.

Watchdog

If this bit is set high, the watchdog circuit has detected a CPU failure.

First Time–Up

Power–on reset sets this bit high. This signifies the data in the RAM and Clock is not valid and should be initialized. After the status register is read, the first time–up bit is set low if the $\overline{POR}$ pin is high. Conversely, if the $\overline{POR}$ pin is held low, the first time–up bit remains set high.

Interrupt True

A high in this bit signifies that one of the three interrupts (power sense, alarm, or clock) is valid.

Power–Sense Interrupt

This bit set high signifies that the power–sense circuit has generated an interrupt. This bit is not reset after a read of this register.

Alarm Interrupt

When the contents of the seconds, minutes, and hours time counters and alarm latches are equal, this bit is set high. The status register must be read before loading the interrupt control register for valid alarm indication after the alarm activates.

Clock Interrupt

A periodic interrupt sets this bit high (see Table 3).

SERIAL PERIPHERAL INTERFACE (SPI)

The serial peripheral interface (SPI) utilized by the MC68HC68T1 is a serial synchronous bus for address and data transfers. The shift clock (SCK), which is generated by the microcomputer, is active only during address and data transfer. In systems using the MC68HC05C4 or MC68HC11A8, the inactive clock polarity is determined by the clock polarity (CPOL) bit in the microcomputer's control register.

A unique feature of the MC68HC68T1 is that the level of the inactive clock is determined by sampling SCK when SS becomes active. Therefore, either SCK polarity is accommodated. Input data (MOSI) is latched internally on the internal strobe edge and output data (MISO) is shifted out on the shift edge (see Table 4 and Figure 13). There is one clock for each bit transferred. Address as well as data bits are transferred in groups of eight.

Table 4. Function Table

Mode	Signal			
	SS	SCK	MOSI	MISO
Disabled Reset	L	Input Disabled	Input Disabled	High–Z
Write	H	CPOL = 1 ⌐¬ CPOL = 0 ¬⌐	Data Bit Latch	High–Z
Read	H	CPOL = 1 ¬⌐ CPOL = 0 ⌐¬	X	Next Data Bit Shifted Out*

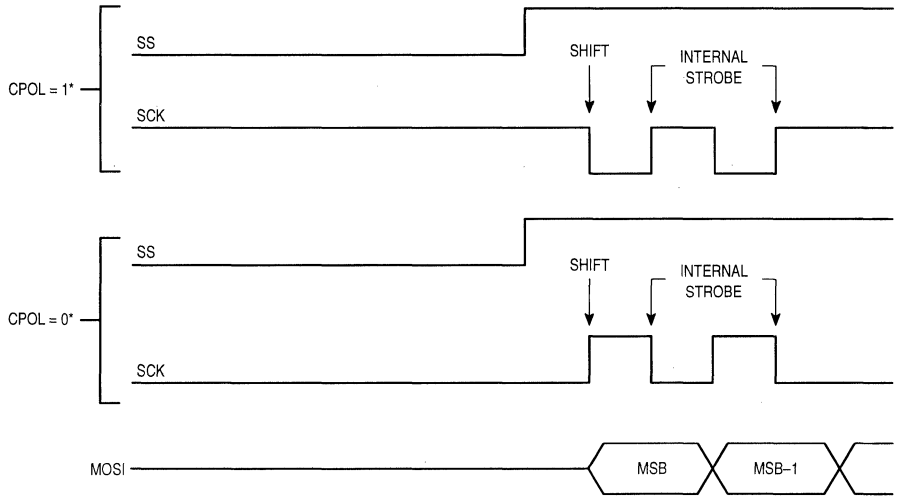
* MISO remains at a High–Z until eight bits of data are ready to be shifted out during a read. MISO remains at a High–Z during the entire write cycle.

ADDRESS AND DATA FORMAT

There are three types of serial transfers:

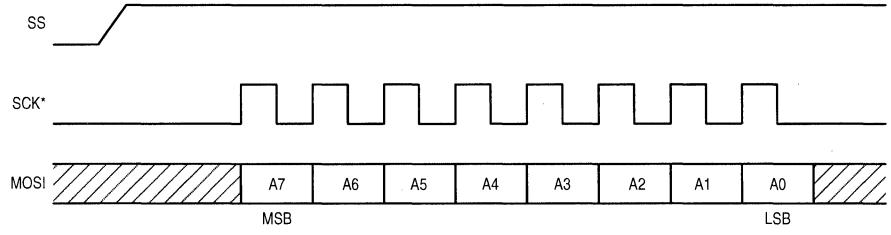
1. Read or write address
2. Read or write data
3. Watchdog reset (actually a non–transfer)

The address and data bytes are shifted MSB first, into the serial data input (MOSI) and out of the serial data output (MISO). Any transfer of data requires the address of the byte to specify a write or read Clock or RAM location, followed by one or more bytes of data. Data is transferred out of MISO for a read operation and into MOSI for a write operation (see Figures 14 and 15).



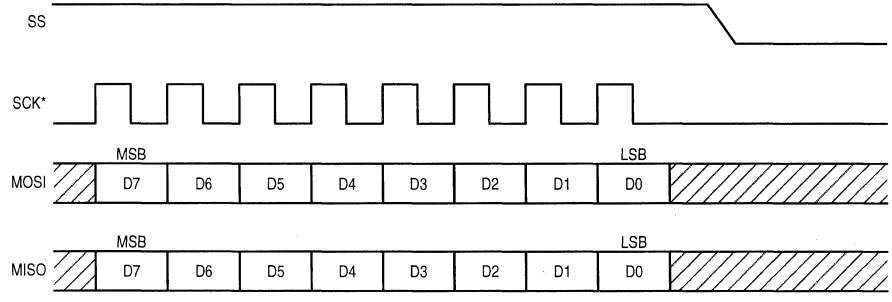
* CPOL is a bit that is set in the microcomputer's Control Register.

Figure 13. Serial Clock (SCK) as a Function of MCU Clock Polarity (CPOL)



* SCK can be either polarity.

Figure 14. Address Byte Transfer Waveforms

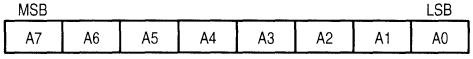


* SCK can be either polarity.

Figure 15. Read/Write Data Transfer Waveforms

Address Byte

The address byte is always the first byte entered after SS goes true. To transmit a new address, SS must first be brought low and then taken high again.



A7 — High initiates one or more write cycles.
Low initiates one or more read cycles.

A6 — Must be low (zero) for normal operation.

A5 — High signifies a clock/calendar location.
Low signifies a RAM location.

A0 – A4 — Remaining address bits (see Figure 5).

Address and Data

Data transfers can occur one byte at a time or in multi–byte burst mode (see Figures 16 and 17). After the MC68HC68T1 is enabled (SS = high), an address byte selects either a read or a write of the Clock/Calendar or RAM. For a single–byte read or write, one byte is transferred to or from the Clock/Calendar register or RAM location specified by an address. Additional reading or writing requires re–enabling the device and providing a new address byte. If the MC68HC68T1 is not disabled, additional bytes can be read or written in a burst mode. Each read or write cycle causes the Clock/Calendar register or RAM address to automatically increment. Incrementing continues after each byte transfer until the device is disabled. After incrementing to $1F or $9F, the address wraps to $00 and continues if the RAM is selected. When the Clock/Calendar is selected, the address wraps to $20 after incrementing to $32 to $B2.

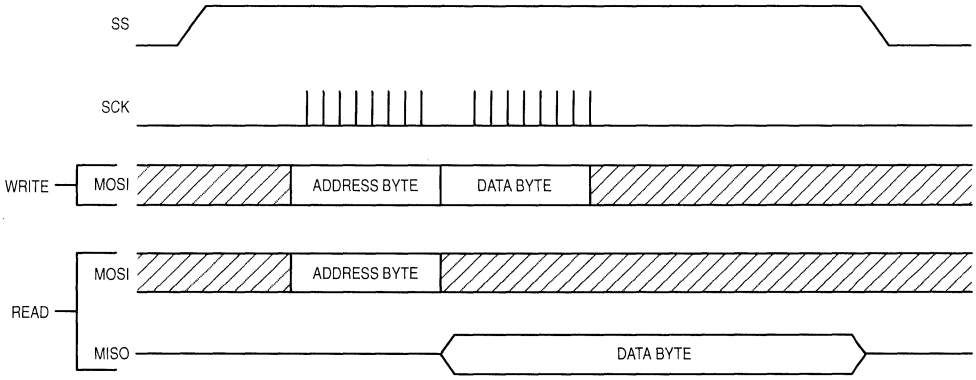


Figure 16. Single–Byte Transfer Waveforms

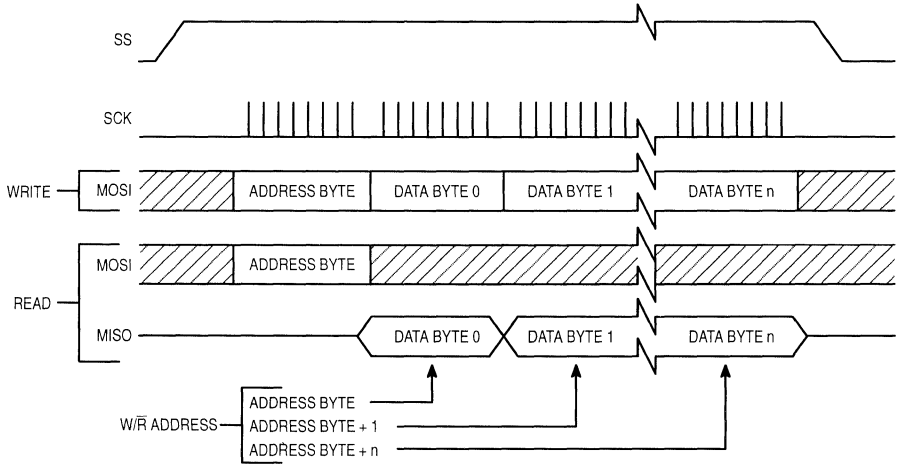
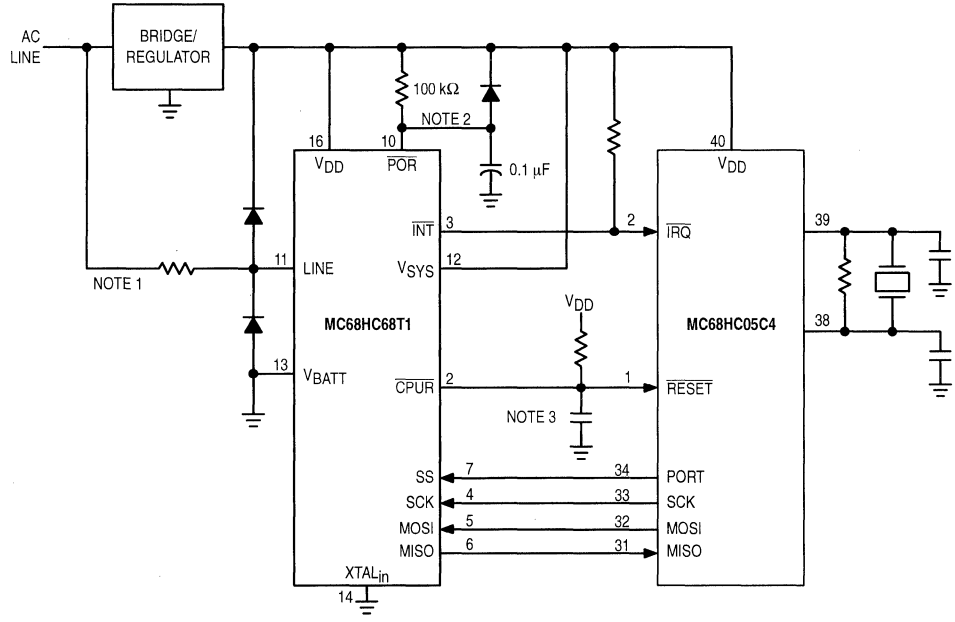


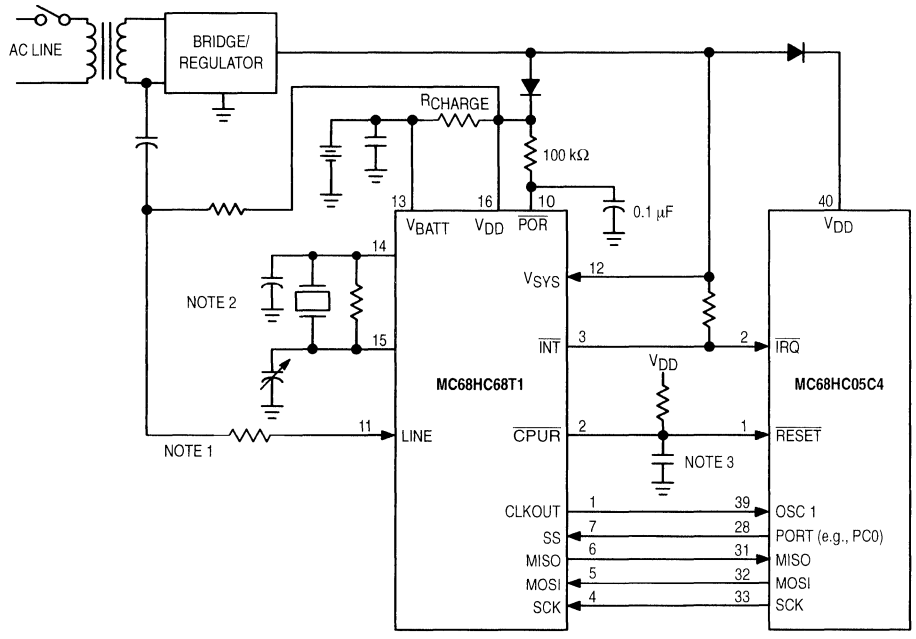
Figure 17. Multiple–Byte Transfer Waveforms

APPLICATION CIRCUITS



NOTES:
1. Clock circuit driven by line input frequency.
2. Power–on reset circuit included to detect power failure.
3. If an MC68HC11 MCU is used, delete the capacitor at the $\overline{\text{RESET}}$ pin.

Figure 18. Power–Always–On System



NOTES:

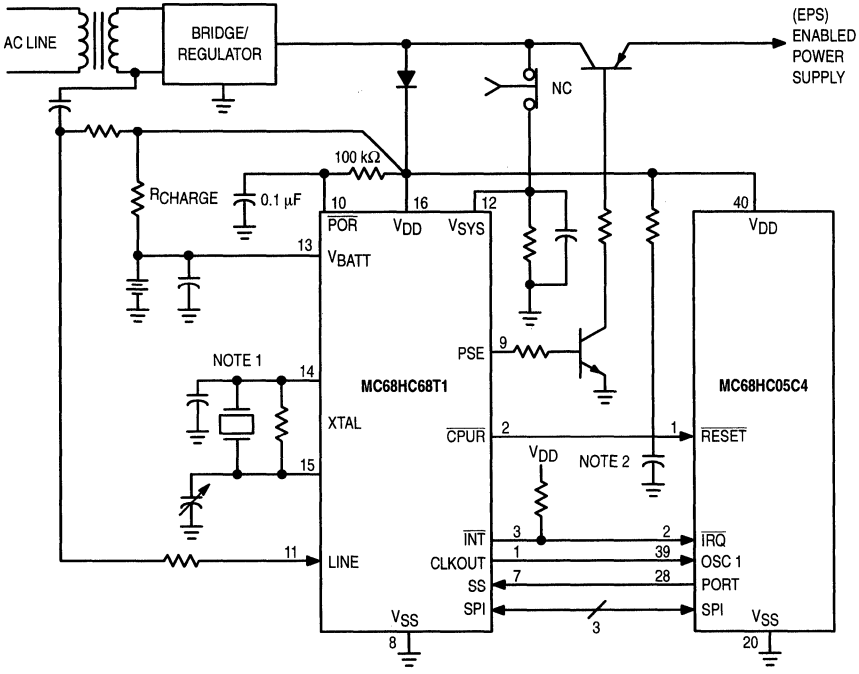
1. The LINE input pin can sense when the switch opens by use of the power sense interrupt. The MC68HC68T1 crystal drives the clock input to the CPU using the CLKOUT pin. On power–down when $V_{SYS} < V_{BATT} + 0.7$ V, V_{BATT} powers the clock. A threshold detect activates an on–chip P channel switch, connecting V_{BATT} to V_{DD}. V_{BATT} always supplies power to the oscillator, keeping voltage frequency variation to a minimum.
2. For 32.768 kHz oscillator, see Figure 12. This configuration, when the MC68HC68T1 supplies the MCU clock, usually requires a 1 to 4 MHz clock.
3. If an MC68HC11 MCU is used, delete the capacitor at the $\overline{\text{RESET}}$ pin.

Figure 19. Externally–Controlled Power System

POWER–DOWN PROCEDURE

A procedure for power–down operation consists of the following:

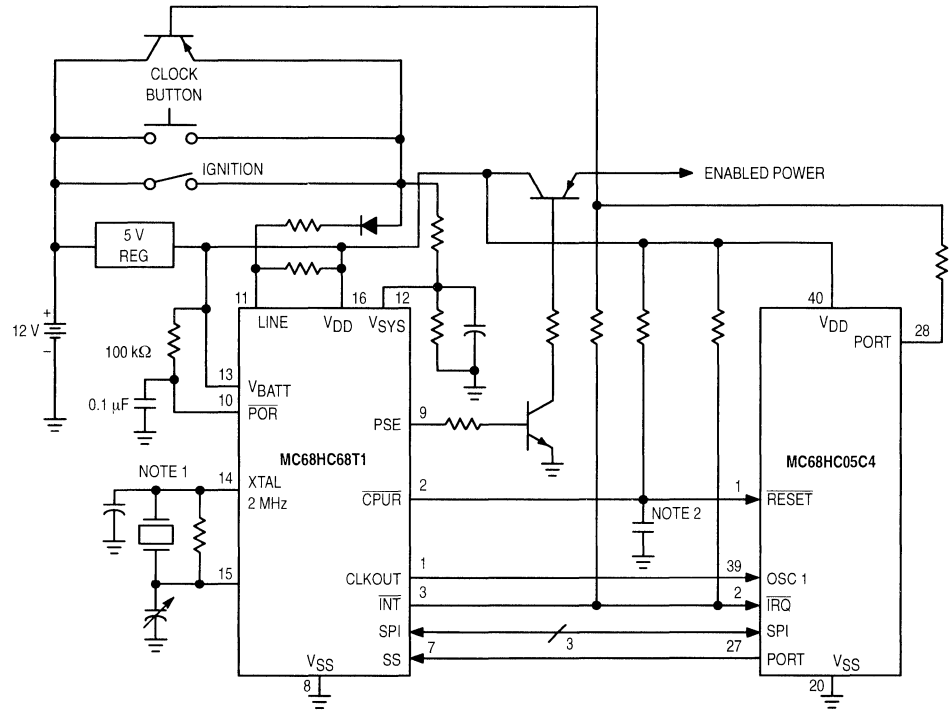
1. Set power sense operation by writing bit 5 high in the interrupt control register.
2. When an interrupt occurs, the CPU reads the status register to determine the interrupt source.
3. Sensing a power failure, the CPU does the necessary housekeeping to prepare for shutdown.
4. The CPU reads the status register again after several milliseconds to determine validity of power failure.
5. The CPU sets power–down (bit 6) and disables all interrupts in the interrupt control register when power–down is verified. This causes the CPU reset and Clock Out pins to be held low and disconnects the serial interface.
6. When power returns and V_{SYS} rises above V_{BATT} + 0.7 V, power–up is initiated. The CPU reset is released and serial communication is established.



NOTES:

1. See Figure 12 for 32.768 kHz operation. This configuration, where the MC68HC68T1 supplies the MCU clock, usually requires a 1 to 4 MHz crystal.
2. If an MC68HC11 MCU is used, delete the capacitor at the $\overline{\text{RESET}}$ pin.

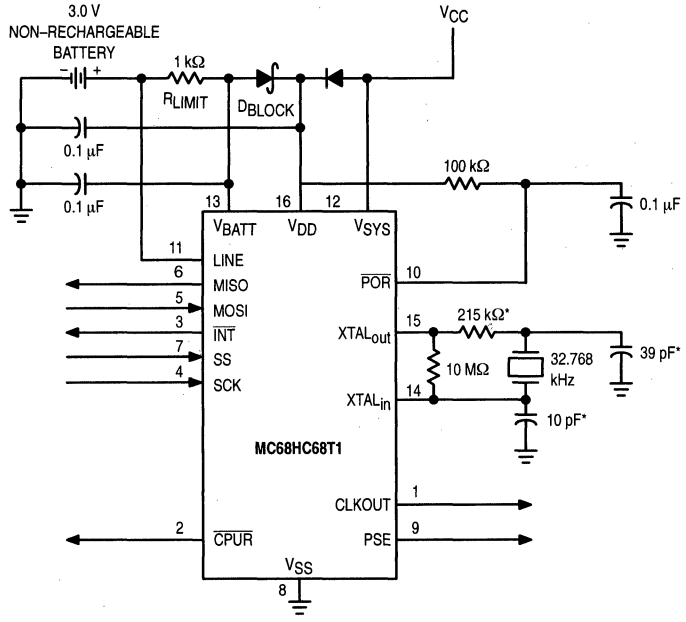
Figure 20. Rechargeable Battery–Backup System



NOTES:

1. The V_{SYS} and Line inputs can be used to sense the ignition turning on and off. An external switch is included to activate the system without turning on the ignition. Also, the CMOS CPU is not powered down with the system V_{DD}, but is held in a low power reset mode during power–down. When restoring power, the MC68HC68T1 enables the CLKOUT pin and sets the PSE and $\overline{CPUR}$ pins high.
2. If an MC68HC11 MCU is used, delete the capacitor at the $\overline{RESET}$ pin.

Figure 21. Automotive System

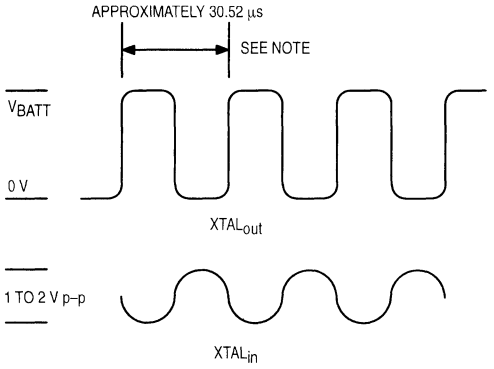


* Actual values may vary, depending on recommendations of crystal manufacturer.

Figure 22. Non–Rechargeable Battery–Backup System

TROUBLESHOOTING

1. *The circuit works, but the standby current is well above the spec. How can the standby current be reduced?*
   a. If using a 32.768 kHz crystal, include a series resistor in the circuit per Figure 12 of the data sheet. A good value to start with is 200 kΩ. The signals at $XTAL_{out}$ and $XTAL_{in}$ pins should look similar to Figure 23 when the correct value is selected. The sharp, clean edges on the $XTAL_{out}$ pin reduces current on the totem pole drivers internal to the device.



NOTE: Refer to item 8.

Figure 23. XTAL Waveforms

   b. Connect the LINE pin to something other than V_{DD} (e.g., V_{BATT}, V_{SS}, V_{SYS})
   c. Ensure that the Power–On–Reset (POR) has a time constant of at least 100 ms.
   d. Ensure that there is a diode from V_{DD} to + 5 V of the system, in battery–backup applications. See **Application Circuits**.
2. *When power is applied, the clock does not start up nor does it hold data in the control registers.*
   Make sure the POR circuit is connected and working.
3. *The clock loses time, but the oscillator is tuned.*
   Do not make constant accesses to the clock. When a read or write cycle is started, the clock stops incrementing time.
4. *When the part is power cycled, the clock loses all time and data.*
   Check the battery installation and ensure that a diode is in the circuit from V_{DD} to + 5 V.
5. *Can a non–rechargeable lithium battery be used?*
   Yes, but the battery must have a large capacity. Careful attention MUST be given if the end unit needs to be UL approved. The circuit of Figure 22 is a good start.
6. *Able to read/write data to the RAM but not to the clock registers, or vice versa.*
   There is a software problem. There is no internal difference from reading/writing to the RAM or clock locations.
7. *How is the oscillator tuned?*
   The best way to tune the oscillator is to set the clock out bits of the Clock Control Register (bits 0, 1, and 2) to output the primary XTAL frequency (000). The frequency can then be more accurately measured from the CLKOUT pin. This prevents the measuring device from loading the oscillator circuit, which may shift the frequency.
8. *What is the accuracy of the oscillator?*
   The oscillator accuracy is dependent on the quality of the crystal used. For every 1 ppm variance in crystal frequency, the clock gains or loses 2.6 seconds per month. 25 ppm is a typical spec for a crystal, which translates to ± 65 seconds per month.
9. *Can the Line pin sense a dc failure?*
   Yes, the Line input is threshold triggered in a window from one diode drop above and below V_{DD}. If supply is removed in the low cycle of a sine wave, the internal network pulls the line pin to within the threshold in a few milliseconds. In the absence of a dc voltage outside the V_{DD} ± 0.7 V window, the internal network pulls the signal to within the window and triggers the interrupt.
10. *Can the V_{SYS} line be more than 0.5 V above V_{DD}?*
    No. There is an ESD protection network that causes a supply problem with this application.
11. *The CLKOUT, $\overline{CPUR}$, and PSE pins do not go inactive when V_{DD} and V_{SYS} are removed. The CLKOUT, $\overline{CPUR}$, and PSE are not active immediately when V_{DD} and V_{SYS} is applied.*
    The problem is related to the power up procedure (battery–backup mode or single–supply mode). See these sections in the data sheet for more information.

TCA3385

Advance Information

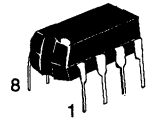
Telephone Ring Signal Converter

2

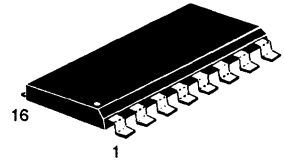
The TCA3385 is a high efficiency telephone ring signal converter designed for use with the TCA3386 (it can also be used stand-alone). These devices, together with a microprocessor, form the basis for a high-performance feature telephone set.

The circuit includes a switching regulator which converts the ring signal from the telephone line into a DC supply signal suitable for powering the other devices in the telephone, e.g. TCA3386 and the MPU, during the ringing phase.

- High efficiency step-down DC/DC converter with linear input impedance
- Power derived from rectified AC ring signal or DC voltage
- Drive output for external PNP transistor
- System supply voltage determined by external transistor, coils and diodes
- Two modes of operation: fixed internal or programmable ring detect threshold (7 to 35V)
- Programmable input impedance between 3K and 15Kohms
- Ring detect output for microprocessor
- Lightning and mains protection
- Applications: telephone set, answering machine, home appliance, etc...



DP SUFFIX
PLASTIC PACKAGE
CASE 626

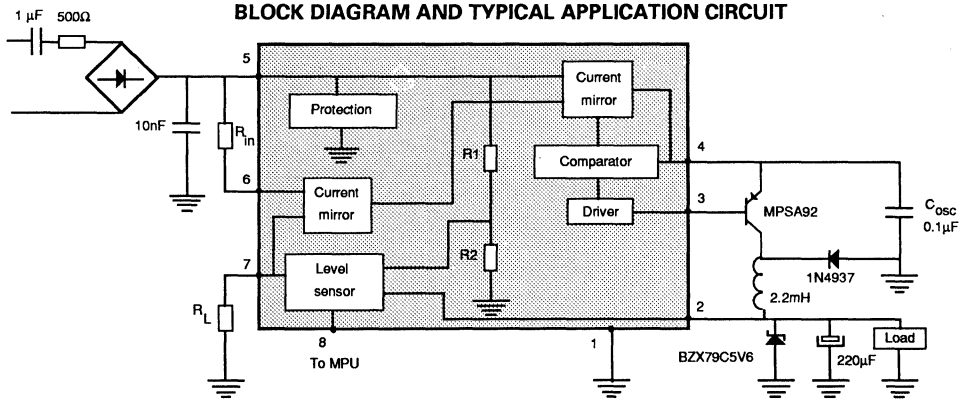


FP SUFFIX
PLASTIC PACKAGE
CASE 751G

ORDERING INFORMATION

TCA3385-DP Plastic DIP
TCA3385-FP SO package

BLOCK DIAGRAM AND TYPICAL APPLICATION CIRCUIT



TCA3385 PIN DESCRIPTIONS

Pin 1 GND, GROUND
This is the reference ground for the overall system.

Pin 2 V_{cc}, POWER SUPPLY
The output is a current which will establish a voltage defined by the load circuit and the voltage regulator (typically 5-6 volts for telephone application).

Pin 3 DRV, DRIVE OUTPUT
This output directly drives the base of the PNP transistor of the switchmode power supply system.

Pin 4 CO, CURRENT OUTPUT
This pin provides constant current output for charging the external capacitor C_{osc}.

Pin 5 LI, LINE INPUT
This pin can be driven either by a DC voltage or a non filtered rectified AC voltage. In a typical telephone application, it is connected to the positive side of a diode bridge before the twisted pair cable.

Pin 6 R_{in}
An external resistor R_{in} connected between this pin and LI sets the input impedance of the circuit.

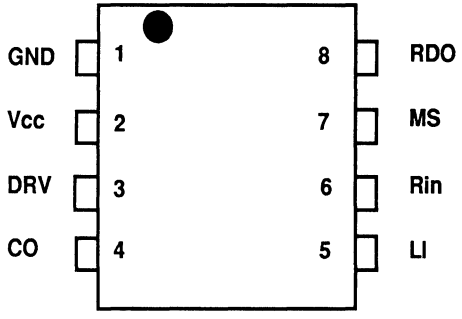
Pin 7 MS, MODE SELECT
An external resistor R_L connected between this pin and ground sets the value of the ring detect threshold.

If $R_L = 0$, Mode 1 is selected and a fixed 12 volt level is automatically chosen by the internal level sensor circuitry.

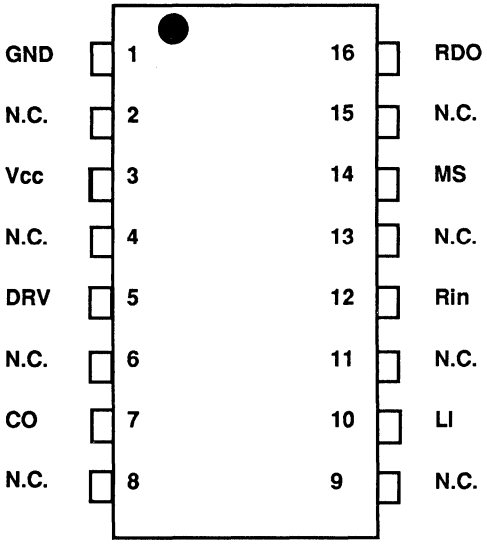
Otherwise Mode 2 is selected and R_L determines the value of the ring detect threshold. In Mode 2 R_L also affects the input impedance of the circuit.

Pin 8 RDO, RING DETECT OUTPUT
This is a digital output for a microprocessor which indicates that a ring signal has been detected. This pin will shift from low to high each time the input voltage passes the preset threshold voltage.

Depending on its load (resistive or capacitive), the signal at this pin can either remain high during the ring time, or be a square wave at twice the ringing signal frequency.



DIL 8 pins



SOIC wide 16 pins

ABSOLUTE MAXIMUM RATINGS

Parameter	Value	Unit
Line Voltage	120	V rms
Input Impedance	3K to 15K	Ohms
Maximum Peak Current (crowbar on)	500	mA
Storage Temperature Range	-65 to +150	°C
Operating Junction Temperature	150	°C

Devices should not be operated at or outside these values. Actual device operation should be restricted to within the "Recommended Operating Limits".

RECOMMENDED OPERATING LIMITS

Parameter	Symbol	Min	Typ	Max	Unit
Operating Ambient Temperature Range	T_a	0		70	°C
Line Voltage	V_{in}			90	V rms
Line Source Impedance	Z_s	500			Ohms

THERMAL DATA

Parameter	Value	Unit
Thermal Resistance Junction-Ambient Plastic Package Case 626 SO Package Case 751G	 90 110	°C/W

ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit
Ring Detect Output Voltage High	V_{oh}	V_{cc} -0.93	V_{cc} -0.7	V_{cc} -0.57	V
Ring detect Output Voltage Low	V_{ol}		11	20	mV
Turn-on Threshold Input Voltage (Mode 1, R_L=0, I_{Load}=0)	V_{d1}	11.2	12	13.0	V
Threshold Temperature Drift (Mode 1, R_L=0)	DV_{d1}		-5		mV/°C
On/Off Threshold Hysteresis (Mode 1, R_L=0, I_{Load}=0)	Hys1	1.2	1.8	2.4	V
Turn-on Threshold Input Voltage (Mode 2, limit fixed by ext res R_L)	V_{d2}	8		35	V
Threshold Temperature Drift (Mode 2)	D_{Vd2}		-20		mV/°C
On/Off Threshold Hysteresis (Mode 2)	Hys2	0.5		7	V
Ring Detect Output Pull-up Current (V_{in} = 15V)	$I_{d\ up}$	0.5	1.5	2.5	mA
Ring Detect Output Pull-down Current Low State ($V_{RDO} < V_{cc}$ /2) High State ($V_{RDO} > V_{cc}$ /2)	$I_{d\ down}$	 60 10	 100 20	 140 26	µA
V_{cc} Level (Ring Detector Enabled) @ V_{cc} max = 5.5V	$V_{cc\ on}$	2.75	3.1	3.45	V
Vcc Level (Ring Detector Disabled) @ V_{cc} max = 5.5V	$V_{cc\ off}$	1.40	1.8	2.3	V
Ring Detect Output Rise Time (no capacitor)	t_r		1		µs
Ring Detect Output Fall Time (no capacitor)	t_f		4		µs
Ring Detect Output Ripple (Crd = 0.47µF, f = 50Hz, no load)	$V_{d\ rip}$		0.25	0.5	V pp

SWITCHMODE POWER SUPPLY

Parameter	Symbol	Min	Typ	Max	Unit
V_{cc} Output Voltage (I_{load} = 36mA)	V_{cc}	Fixed by Zener diode			
Output Power (V_{in} = 90V rms, f = 50Hz)	P_{out}			600	mW
Power Supply Efficiency	Eff	50	55		%
Switching Frequency (V_{in} = 40v, R_{in} = 500KΩ)	Fs	25	35	45	KHz
Output Voltage Ripple (I_{load} = 36mA, C_{load} = 220µF, V_{in} = 90V rms)	$V_{cc\ rip}$		0.5	0.7	V pp
C_{osc} Charge Current (V_{in} = 20V, R_{in} = 500KΩ, R_L = 0)	I_{charge}	3.1	3.5	4.1	mA
C_{osc} Discharge Current (V_{in} = 20V, R_{in} = 500KΩ, R_L = 0)	$I_{disch.}$	11	18	25	mA

LINE INPUT AND PROTECTION

Parameter	Symbol	Min	Typ	Max	Unit
Input Impedance	Z_{in}				Kohm
Off-state (V_{in} = 4.5V, R_{in} = 500KΩ, R_L = 0)		25	50		
On-state (V_{in} > 25V, Mode 1, R_L = 0)		3	$\frac{R_{in}}{100}$	15	
Fixed by external resistance R_{in}					
On-state (V_{in} > 25V, Mode 2)		3	$\frac{R_{in}+2R_L}{100}$	15	
Fixed by external resistance R_{in} and R_L					
Non-linearity @ 35 <V_{in} < 75 V	NL				%
Mode 1			3	8	
Mode 2			3	8	
Overvoltage Protection Threshold (Crowbar on)	V_{ov}	120	135	147	V
Crowbar-on Input Voltage (Crowbar On, I_{limit} = 40mA)	V_{on}	4.3	6.5	8.7	V
Crowbar-on Power Dissipation (Limited by Internal 100 ohms + external res.)	Pd			1.3	W
Crowbar Turn-on Delay (CRD = 0.1µF)	T_{on}		130		µs

INTRODUCTION

The TCA3385 is primarily intended for converting the ring signal delivered by a central office or PABX into a DC voltage which is suitable for powering the other components in an electronic telephone. It will supply the power to enable the use of the features of a sophisticated telephone, such as MPU control, generation and amplification of ringing melodies at a speaker, display short messages of information, etc... while the telephone is on-hook.

The circuit combines a high efficiency DC/DC converter and a level sensor device which acts as a programmable ring detector and indicator for a MPU, thus initiating the operation of the telephone.

Overvoltage protection is also achieved using a "crowbar" technique.

LINE INPUT AND PROTECTION

The DC/DC converter has linear input impedance, which means that the circuit input impedance is ohmic and constant whenever the input voltage varies above the turn-on threshold voltage inside the tolerated limits. Any value between 3K and 15Kohms can be set using one or two resistors, depending on the mode of operation (see paragraph "RING DETECTOR" below). In Mode 1 the circuit input impedance Z_{in} is a ratio of the resistor R_{in} between pin 5 and pin 6: $Z_{in} = R_{in}/100$. In Mode 2, Z_{in} is a function of R_{in} and the resistor R_L between pin 7 and ground: $Z_{in} = (R_{in} + 2R_L)/100$.

On the other hand, the turn-on input circuitry guarantees that the input impedance is high at low voltages to avoid perturbing the line.

The overvoltage protection device consists of two thyristors in series which are turned-on at a voltage between 120V and 150V. The input current is limited by a 100 ohms internal resistor, but an external resistor is mandatory to prevent excessive currents. A 500 ohms series resistor is recommended as minimum.

RING DETECTOR

The TCA3385 includes a ring detector (also called level sensor) whose function is to provide a digital output for a MPU. It only operates when the circuit is sufficiently powered, i.e. when the DC/DC converter output (V_{cc}) has reached a level greater than 3V. It also has hysteresis which powers the level sensor off at 2V.

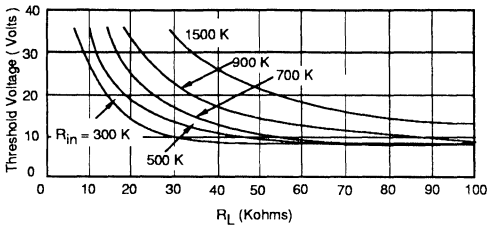


Figure 1. Ring Detection Threshold (Mode 2) vs R_{in} and R_L

The digital output shifts from low to high according to the line input voltage, a preset level for detection and its load at pin 8.

The level for ring detection may be set using one or two modes of operation as previously noted. In Mode 1, where pin 7 is connected to ground, an internally fixed level is set as the ring detect threshold, which is typically 12 Volts. In Mode 2 operation, where an external resistor R_L is connected between pin 7 and ground, the ring detect threshold is programmable. Its value is a function of R_L (see Figure 1).

It should be noted that due to the IC design structure, Mode 1 is not a particular case of Mode 2. In fact, in Mode 2, R_L must be chosen high enough so that the ring detector works efficiently (the minimum limit is fixed by the upper limit of 35V for the ring detect threshold; see Figure 1).

In a telephone application, where the input signal is a rectified AC ringing signal, we can choose between two output modes at pin 8, pulsed or continuous: without a capacitor at pin 8, the ouput voltage will change state each time the input crosses the ring detect turn-on and turn-off thresholds, thus providing information on the frequency of the ring signal; on the other hand, if the load at pin 8 is a capacitor, the output voltage will shift from low to high only the first time the input crosses the turn-on threshold, and remain high until the end of the ringing pulse. This is permitted by the internal input circuitry at pin 8, which has an emitter-follower transistor for pull-up and a non-linear current generator for pull-down (20µA for slow discharge, 100µA for fast discharge; see Figure 2).

SWITCHMODE POWER SUPPLY

The TCA3385 is basically a DC/DC converter which works with external components: a PNP transistor, a coil, a zener diode, a capacitor and a holding diode.

The circuit drives the external PNP for switching the current into the coil. This PNP should be a fast switching transistor, with a switching time of less than 2% of the total pulse time $T_0 = 1/f_0$ (where f_0 is the switching frequency). For example, in a 50KHz application (T_0 = 20µs), rise time and fall time should be less than 400ns; this is mandatory to keep the efficiency of the switchmode greater than 50%. Also, the PNP must withstand voltages as high as 150V. In the suggested application, a MPSA92 (or a BDC06) is used.

The holding diode should also have a low forward voltage drop and fast switching characteristics so that high power output is achieved. It must withstand voltages as high as 150V. The coil as well should have its losses (both magnetic and resistive) minimized.

The DC/DC converter consists of 3 main blocks:

- a current mirror which produces a constant current for charging the external capacitor. This current is dependent on V_{in}.
- a comparator to set the switching frequency of the power supply. The switching frequency is mainly dependent on the input voltage V_{in} and the input impedance Z_{in}.
- a drive stage for the PNP transistor.

EXTERNAL PROTECTION RESISTOR

This device has been designed to accept overvoltage input signals, by switching ON two serial input thyristors, from levels exceeding 120V between pin 5 and pin 1. In this case the current is limited by an internal 100 ohms series resistor with an external resistor Rv (nominally 500 ohms).

a) Fast input signals

If the slew rate of the overvoltage pulse is much greater than 500V/ms (which is valid for a 1µF series capacitor with a current limit of 500mA), then the peak current is equal to the applied peak voltage divided by the external resistance R_v.

Under these conditions, the absolute maximum peak current is equal to 500mA, no matter how short the pulse .

For example : for 400V maximum limit, R_v = 400V/0.5A = 800 ohms.

b) Slow input signals

For slow signals (eg: ringing signals 25, 50, 100 Hz...) the maximum current must be limited to 250mA. So, for the French standard ringing voltage , R_v is equal to $120V_{max}/0.25A$ = 500 ohms.

If the overvoltage is higher, R_v must be calculated for the new maximum input voltage.

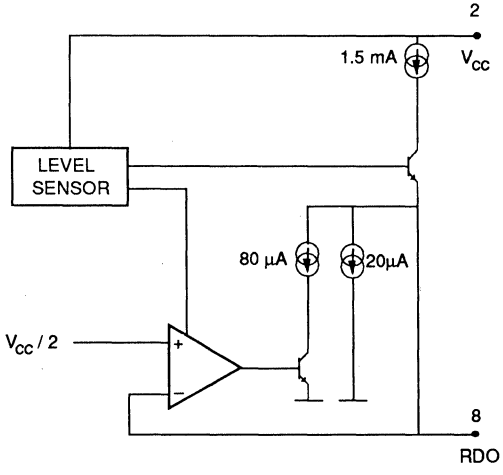


Figure 2. Ring Detect Output Stage

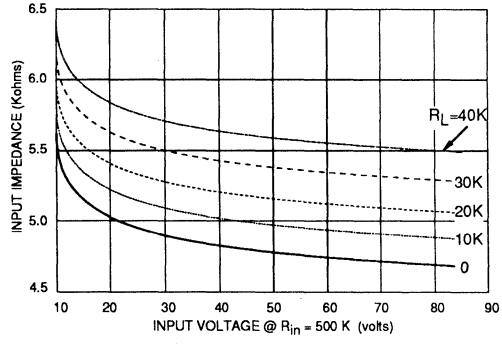


Figure 3. Input Impedance vs V_{in} @ R_{in} = 500K

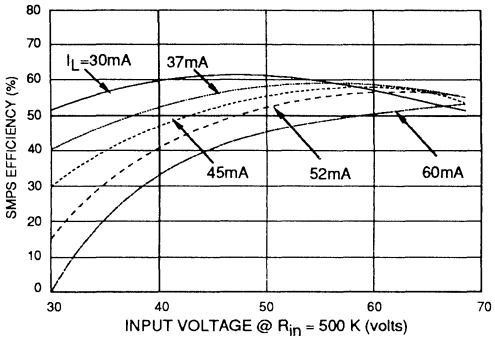


Figure 4. SMPS Efficiency vs V_{in} @ R_{in} = 500K

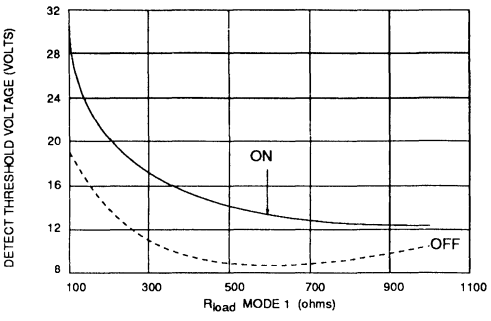


Figure 5. Detect Threshold vs R_{load} (Mode 1)

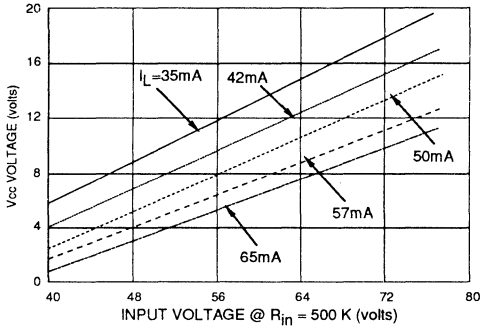


Figure 6. V_{cc} vs V_{in} @ R_{in} = 500K (without Zener)

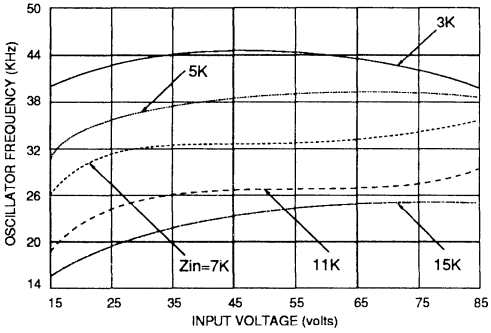


Figure 7. Oscillator frequency vs V_{in}

TCA3388

Advance Information

Telephone Line Interface

TELEPHONE LINE INTERFACE

SEMICONDUCTOR TECHNICAL DATA

The TCA3388 is a telephone line interface circuit which performs the basic functions of a telephone set in combination with a microcontroller and a ringer. It includes dc and ac line termination, the hybrid function with 2 adjustable sidetone networks, handset connections and an efficient supply point.

2

FEATURES

Line Driver and Supply

- DC and AC Termination of the Telephone Line
- Selectable DC Mask: France, U.K., Low Voltage
- Current Protection
- Adjustable Set Impedance for Resistive and Complex Termination
- Efficient Supply Point for Peripherals
- Hook Status Detection

Handset Operation

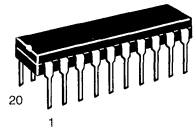
- Transmit and Receive Amplifiers
- Double Anti–Sidetone Network
- Line Length AGC
- Microphone and Earpiece Mute
- Transmit Amplifier Soft Clipping

Dialing and Ringing

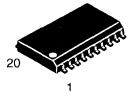
- Interrupter Driver for Pulse–Dialing
- Reduced Current Consumption During Pulse–Dialing
- DTMF Interfacing
- Ringing via External Ringer

Application Areas

- Corded Telephony
- Cordless Telephony Base Station
- Answering Machines
- Fax
- Intercom
- Modem

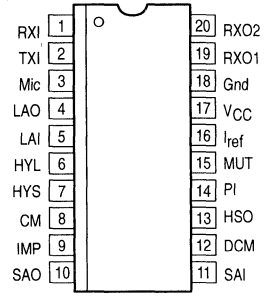


DP SUFFIX
PLASTIC PACKAGE
CASE 738



FP SUFFIX
PLASTIC PACKAGE
CASE 751D

PIN CONNECTIONS



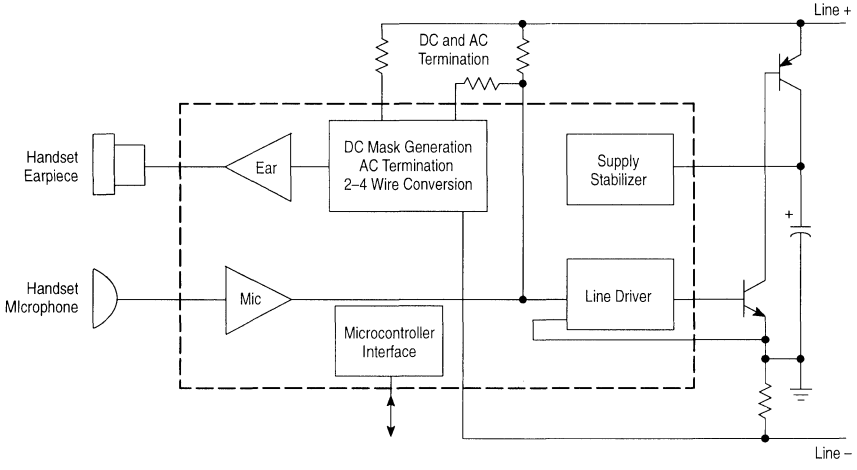
(Top View)

ORDERING INFORMATION

Device	Tested Operating Temperature Range	Package
TCA3388DP	T_A = 0° to +70°C	DIP
TCA3388FP		SOIC

This document contains information on a new product. Specifications and information herein are subject to change without notice.

Simplified Block Diagram



This device contains 1,911 active transistors.

MAXIMUM RATINGS

Rating	Symbol	Min	Max	Unit
Maximum Junction Temperature	T_J	–	+150	°C
Storage Temperature Range	T_{stg}	– 65	+150	°C

NOTE: Devices should not be operated at or outside these values. The "Recommended Operating Limits" provide for actual device operation.

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Min	Typ	Max	Unit
Operating Temperature Range	T_A	0	–	+70	°C

DC ELECTRICAL CHARACTERISTICS (T_A = 25°C)

Characteristic	Symbol	Min	Typ	Max	Unit
VOLTAGE REGULATOR					
Regulated Supply at Pin 17	V_{CC}				Vdc
I_{CC} = 7.0 mA		3.4	3.7	4.0	
I_{CC} = 20 mA		3.45	3.75	4.05	
I_{CC} = 80 mA		3.5	3.8	4.1	
Current Consumption at Pin 17, Pin PI = High	I_{CC}	–	–	600	µA
DRIVER DC CHARACTERISTICS					
Available Current at LAO	I4				µA
Source Current		45	70	100	
Sink Current		–100	–70	– 45	
Amplifier A8 Driver Slope	S8	0.7	1.0	1.2	µA/mV
LAO Voltage (PI = High, I4 = 100 µA)	V_{LAO}	–	–	270	mV
Internal Offset (Pins 5 to 10)	VO1–VO2	30	80	140	mV
SPEECH AMPLIFIERS					
IMP Voltage (Pin 9, Closed Loop)	V_{IMP}	–	1.6	–	Vdc
Earpiece Amplifier DC Bias (R_{ext} = 100 kΩ)					Vdc
RXI, Pin 1	V_{RXI}	–	1.6	–	
RXO1 Pin 19	V_{RXO1}	–	1.7	–	
RXO2, Pin 20	V_{RXO2}	–	1.45	–	

DC ELECTRICAL CHARACTERISTICS (continued) (T_A = 25°C)

Characteristic	Symbol	Min	Typ	Max	Unit
SPEECH AMPLIFIERS					
Offset ($V_{RXO1} - V_{RXO2}$)	V_{Offset}	–	0.25	0.70	
HYL and HYS DC Bias Voltage					Vdc
Normal Mode	V_{HY1}	–	2.4	–	
PI = High	V_{HY2}	–	1.4	–	
Microphone Amplifier DC Bias at TXI	V_{TXI}	–	1.45	–	Vdc
Saturation Voltage at Mic @ 1.0 mA	V_{Mic}	–	250	300	mV
Leakage Current into Mic @ 3.7 V	I_{Leak}	–	–	2.0	µA
HOOK STATUS OUTPUT (Pin 13)					
High Level Voltage @ – 5.0 µA Load Current, Off–Hook, V_{SAI} = Max	V_{HSOH}	2.7	2.9	–	Vdc
Maximum Load Current					µA
Normal Mode	I_{HSOL}	–	–	5.0	
PABX Mode	I_{HSOH}	20	–	–	
Low Level Voltage @ + 5.0 µA Load Current, V_{SAI} = – 5.0 mV					Vdc
Normal On–Hook	V_{HSOL}	–	–	0.60	
PI = High	V_{HSOLPI}	2.7	2.9	–	
Time Delay from On–Hook or Off–Hook	T_{Del}	–	3.5	–	ms
PULSE INPUT (Pin 14)					
Input Impedance	Z_{PI}	–	160	–	kΩ
DC Bias Voltage	V_{PIL}	–	1.4	–	Vdc
Input Current					µA
Make Phase	I_{PIL}	–1.0	–	1.0	
Break Phase	I_{PIH}	–10	–	10	
MUTE INPUT (Pin 15)					
Input Impedance	Z_{MI}	–	160	–	kΩ
DC Bias Voltage	V_{MI}	–	1.4	–	Vdc
Input Current					µA
Speech Mode	I_{MIL}	–1.0	–	1.0	
Mute Mode	I_{MIH}	–10	–	10	
DC MASK CHARACTERISTICS					
French					
Internal Slope	RI	120	160	200	mV/µA
Voltage on SAI (I2C = 3.6 µA)	V_C	0.40	0.47	–	Vdc
Voltage on SAI (I2D = 4.0 µA)	V_D	–	0.49	0.57	Vdc
Delta Offset Voltage on SAI (I2E = 30 µA)	V_E–V_D	–	–	30	mV
U.K.					
Internal Slope	RI	210	260	310	mV/µA
Voltage on SAI (I2C = 3.5 µA)	V_C	0.59	0.70	–	Vdc
Voltage on SAI (I2D = 3.9 µA)	V_D	–	0.72	0.83	Vdc
Delta Offset Voltage on SAI (I2E = 30 µA)	V_E–V_D	–	20	50	mV
Low Voltage Mode					
Internal Slope	RI	100	125	150	mV/µA
Voltage on SAI (I2C = 13 µA)	V_C	1.0	1.2	–	Vdc
Voltage on SAI (I2D = 15 µA)	V_D	–	1.3	1.55	Vdc
Delta Offset Voltage on SAI (I2E = 20 µA)	V_E–V_D	–	–	100	mV
Overvoltage Protection Threshold ($V_{LAI} - V_{SAO}$)	V_{Clamp1}				mV
French and U.K. DC Masks		530	580	650	
Low Voltage DC Mask		280	–	385	
Protection Voltage Level ($V_{LAI} - V_{SAO}$)	V_{Clamp2}				mV
French and U.K. DC Masks		350	–	440	
Low Voltage DC Mask		280	–	440	

AC ELECTRICAL CHARACTERISTICS (T_A = 25°C)

Characteristic	Symbol	Min	Typ	Max	Unit
TRANSMIT MODE					
French and U.K.					dB
Maximum Transmit Gain (I2 = 3.0 μA)	Kμ0	11.25	12.5	13.75	
Line Length Regulation (I2 = 30 μA)	ΔKμ	5.5	6.5	7.5	
Gain in Protection Mode (I2 = 30 μA)	Kμp	10.5	12.5	14.5	
Low Voltage Mode					dB
Maximum Transmit Gain (I2 = 3.0 μA)	Kμ0	11.25	12.5	13.75	
Line Length Regulation (I2 = 8.2 μA)	ΔKμ	4.5	6.0	7.5	
Gain in Protection Mode (I2 = 8.2 μA)	Kμp	10.5	12.5	14.5	
Gain Reduction when Microphone is Muted	ΔKμm	60	–	–	dB
RECEIVE MODE					
French					
Maximum Internal Transconductance (I2 = 3.0 μA)	G_{e0}	150	180	210	μA/V
Line Length Regulation (I2 = 18 μA)	ΔG_e	2.95	3.7	4.45	dB
Hybrid Weighting Factor (I2 = 18 μA)	m_r	0.4	0.5	0.6	
Line Length Regulation (HYS @ V_{CC}, I2 = 9.0 μA)	ΔG_e	1.5	2.1	2.5	dB
Protection Mode (I2 = 18 μA)	G_{ep}	145	185	230	μA/V
U.K.					
Maximum Internal Transconductance (I2 = 3.0 μA)	G_{e0}	150	180	210	μA/V
Line Length Regulation (I2 = 18 μA)	ΔG_e	2.8	3.5	4.3	dB
Hybrid Weighting Factor (I2 = 13 μA)	m_r	0.4	0.5	0.6	
Line Length Regulation (HYS @ V_{CC}, I2 = 9.0 μA)	ΔG_e	1.4	1.9	2.4	dB
Protection Mode (I2 = 18 μA)	G_{ep}	145	185	230	μA/V
Low Voltage Mode					
Maximum Internal Transconductance (I2 = 3.0 μA)	G_{e0}	150	185	210	μA/V
Line Length Regulation (I2 = 8.0 μA)	ΔG_e	4.2	5.7	7.2	dB
Hybrid Weighting Factor (I2 = 7.0 μA)	m_r	–	0.5	–	
Line Length Regulation (HYS @ V_{CC}, I2 = 4.0 μA)	ΔG_e	–	3.0	–	dB
Protection Mode (I2 = 8.0 μA)	G_{ep}	145	185	230	μA/V
Earpiece Gain Reduction when Muted	ΔG_{em}	60	–	–	dB
TRANSMIT PABX MODE					
French and U.K.					dB
Transmit Gain (I2 = 3.0 μA)	K_{PABX}	9.25	10.5	11.75	
Variation with Line Length (I2 = 30 μA)	ΔK_{PABX}	– 0.5	–	0.5	
Low Voltage Mode					dB
Transmit Gain (I2 = 3.0 μA)	K_{PABX}	9.25	10.5	11.75	
Variation with Line Length (I2 = 30 μA)	ΔK_{PABX}	– 0.5	–	0.5	
RECEIVE PABX MODE					
French					
Internal Transconductance (I2 = 5.0 μA)	G_{PABX}	120	145	170	μA/V
Hybrid Weighting Factor (I2 = 5.0 μA)	m_r	0.8	0.9	1.0	
Variation with Line Length (I2 = 30 μA)	ΔG_{PABX}	– 0.5	–	0.5	dB
U.K.					
Internal Transconductance (I2 = 5.0 μA)	G_{PABX}	120	145	170	μA/V
Hybrid Weighting Factor (I2 = 5.0 μA)	m_r	0.65	0.75	0.85	
Variation with Line Length (I2 = 30 μA)	ΔG_{PABX}	– 0.5	–	0.5	dB
Low Voltage Mode					
Internal Transconductance (I2 = 3.0 μA)	G_{PABX}	120	145	170	μA/V
Hybrid Weighting Factor (I2 = 3.0 μA)	m_r	–	0.9	–	
Variation with Line Length (I2 = 30 μA)	ΔG_{PABX}	– 0.5	–	0.5	dB
DISTORTION					
French					%
Transmit (I2 = 10 μA)	THDT	–	–	3.0	
Receive (I2 = 6.0 μA) V_E = 700 mV	THDR	–	–	3.0	
V_E = 1250 mV		–	–	5.0	

NOTE: V_E is the differential earpiece voltage across Pins 19 and 20.

AC ELECTRICAL CHARACTERISTICS (continued) (T_A = 25°C)

Characteristic		Symbol	Min	Typ	Max	Unit
DISTORTION						
Low Voltage						%
Transmit (I2 = 10 μA)		THDT	–	–	3.0	
Receive (I2 = 6.0 μA)	V_E = 700 mV	THDR	–	–	3.0	
	V_E = 1250 mV		–	–	5.0	

NOTE: V_E is the differential earpiece voltage across Pins 19 and 20.

TYPICAL TEMPERATURE PERFORMANCE

Characteristic		Typical Value @ 25°C	Typical Change – 20 to + 60°C
V_{CC} Regulated Supply @ Pin 17		3.7	– 0.8 mV/°C
Current Consumption at Pin 17, Pin PI = High		400 μA	– 0.55 μA/°C
Amplifier A8 Driver Slope		1.0 μA/mV	– 0.0035 μA/mV/°C
Voltage on SAI	V_C	French = 0.47 Vdc U.K. = 0.70 Vdc	0.35 mV/°C
	V_D	French = 0.49 Vdc U.K. = 0.72 Vdc	
Internal Slope for Low Voltage Mode		125 mV/μA	0.07 mV/μA/°C
Transmit Gain Kμ0		12.5 dB	0.01 dB/°C
Line Length Regulation ΔKμ	French U.K. L.V.	6.5 dB 6.5 dB 6.0 dB	< 0.3 dB Variation < 0.3 dB Variation – 0.05 dB/°C
Internal Transconductance G_{e0}		180 μA/V	< 1.0 dB Variation
Line Length Regulation ΔG_e	French U.K. L.V.	3.7 dB 3.5 dB 5.7 dB	< 0.5 dB Variation < 0.5 dB Variation – 0.04 dB/°C

NOTE: Temperature data is typical performance only, based on sample characterization, and does not provide guaranteed limits over temperature.

PIN FUNCTION DESCRIPTION

Pin	Symbol	Description
1	RXI	Earphone Amplifier Input
2	TXI	Microphone Amplifier Input
3	Mic	Microphone Bias Current Sink
4	LAO	Line Driver Amplifier Output
5	LAI	Line Driver Amplifier Input
6	HYL	Hybrid Network Input for Long Lines
7	HYS	Hybrid Network Input for Short Lines
8	CM	DC Mask Signal Filtering
9	IMP	Reference Voltage
10	SAO	Line Current Sense Amplifier Output
11	SAI	Line Current Sense Amplifier Input
12	DCM	DC Mask Select
13	HSO	Hook Status Output, PABX Mode Select
14	PI	Pulse Input
15	MUT	Mute Input
16	I_{ref}	Reference Current
17	V_{CC}	Supply Voltage
18	Gnd	Ground
19	RXO1	Earphone Amplifier Output
20	RXO2	Earphone Amplifier Inverted Output

DESCRIPTION OF THE CIRCUIT

Concept

With a TCA3388, a microcontroller and a ringer, a basic telephone set can be built according to the concept depicted in Figure 1.

In off–hook position, the application is in speech mode. The line current flows through transistor T2 and supplies the externals (microcontroller) at the supply point V_{CC} which is stabilized by the TCA3388. The V_{line}, I_{line} characteristic is adjusted by the external components Z0, Z1, Z21 and R1 which are in a regulator loop, acting on transistor T2. The ac impedance is generated in a similar way. The handset can be connected directly to the TCA3388. Via a logic level interface, the microcontroller drives the TCA3388 to perform the DTMF/pulse–dialing. The user keyboard has to be connected to the microcontroller. In on–hook position, a ringing melody can be generated with a ringer application.

The block diagram of the TCA3388, in Figure 2, shows the basic blocks of the device plus the essential external components.

Figure 1. Telephone Concept with TCA3388

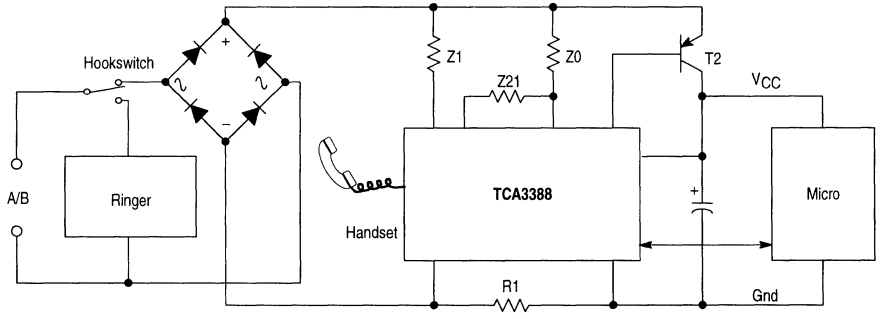
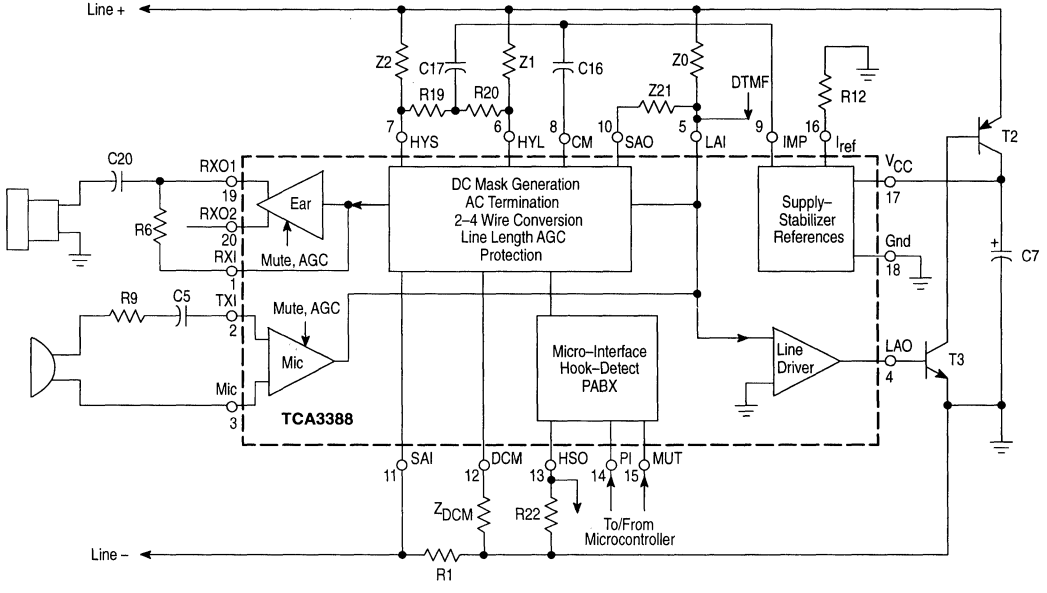


Figure 2. Block Diagram of the TCA3388 with Essential Components

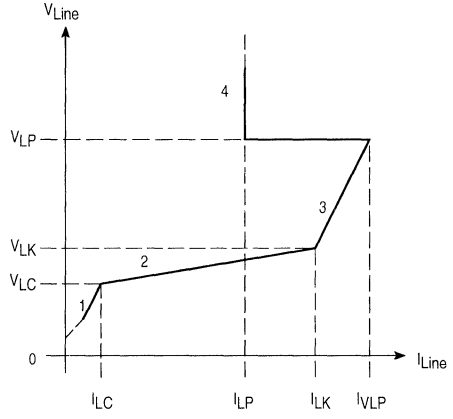


The dc mask has the general form as depicted in Figure 3.

The TCA3388 offers the possibility to adjust the dc characteristics of all 4 regions via mask selection and hardware adjustments.

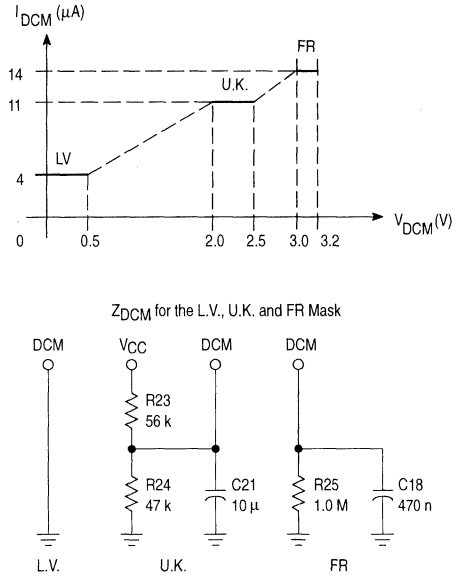
The selection of the 3 masks, France, United Kingdom and Low Voltage, can be done via the Z_{DCM} network at Pin DCM as shown in Figure 4. For French and U.K. masks, the region 3 with the high slope is within the normal dc feeding conditions. For Low Voltage mask the region 3 will be outside this and the dc mask is mainly determined by regions 1 and 2.

Figure 3. General Form of the DC Mask of the TCA3388



Region 1: Startup, Low Line Current, High Slope
Region 2: Mid–Range Line Current, Low Slope
Region 3: High Line Current, High Slope
Region 4: Overload Protection

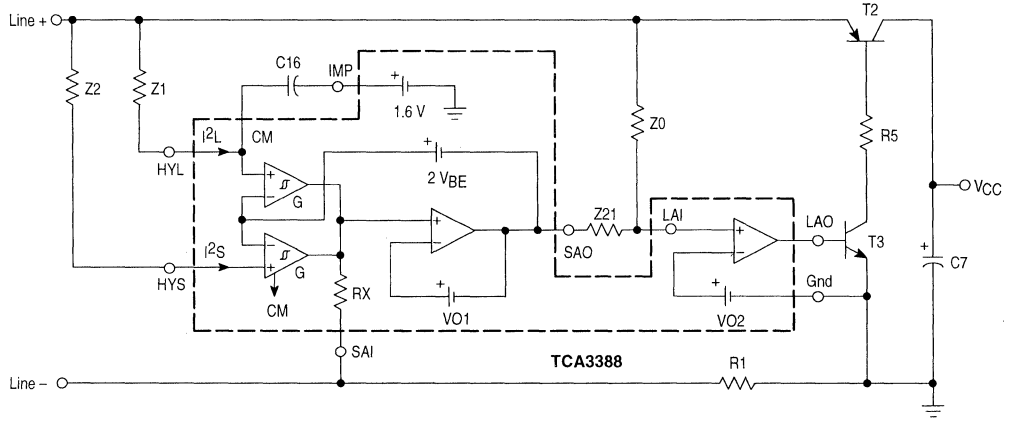
Figure 4. Selection of the Country Mask via Pin DCM



The capacitor in the U.K. network is to ensure a stable selection of the mask during all working modes and transitions. The capacitor in the French network is used to create a startup in Low Voltage Mask.

The adjustment possibilities will be discussed below with the aid of the block diagram of Figure 5.

Figure 5. DC Part of the Block Diagram of the TCA3388



The TCA3388 offers the possibility to connect 2 sidetone networks Z1 and Z2. For correct dc operation, the dc impedance of these networks must be equal. When only 1 sidetone network is used, Pin HYS has to be connected to HYL. All formulas below are based on a single sidetone network, so only Z1 appears. When 2 sidetone networks are used, Z1 has to be replaced by Z1//Z2.

In region 1, the transfer of the amplifier G at the HYL/HYS inputs equals zero. The voltage difference between SAO and SAI will equal VO1. The slope R_{E1} of the V_{Line}, I_{Line} characteristic will equal:

$$R_{E1} = R1 \times \left(1 + \frac{Z0}{Z21}\right)$$

In region 2, the output current of the amplifier G will be proportional to the input current. As a result the voltage between SAO and SAI will increase with the line voltage. Speech signals on the line are of no influence on this because they are filtered out via capacitor C16. The slope R_{E2} of the V_{Line}, I_{Line} characteristic will equal:

$$R_{E2} = R1 \times \left[1 + \frac{1}{\frac{RI}{Z1} + \frac{Z21}{Z0}}\right]$$

In region 3, the output current of the amplifier G is kept constant. As a result the slope in region 3 will equal the slope of region 1.

The transfer from region 2 to 3 occurs at the point V_{LK}, I_{LK} defined by:

$$V_{LK} = Z1 \times I2CD + 2\,V_{BE} + V_{CD} + VO2$$

$$I_{LK} = \frac{\frac{Z21}{Z0} \times \left(Z1 \times I2CD + 2\,V_{BE}\right) + V_{CD}}{R1}$$

With: $I2CD = \frac{I2C + I2D}{2}$, and $V_{CD} = \frac{V_C + V_D}{2}$,

and $2\,V_{BE} \approx 1.4$ V, $V02 \approx 1.1$ V

When the French or U.K. mask is selected, this transfer takes places for line currents of 30 mA to 40 mA depending on the components settings. With the Startup and Low Voltage mask, the transfer lies outside the normal operating range with line currents of 90 mA or more. In most applications the transfer from region 1 to 2 takes place for line currents below 10 mA.

With proper settings, region 4 is entered only during an overload condition. In this mode, the power consumption in the telephone set is limited. In order to detect an overload condition, the voltage between the Pins LAI and SAO is monitored. When the voltage difference is larger than the threshold V_{Clamp1}, the protection is made active. The relation for the line voltage V_{LP} at this point is given as:

$$V_{LP} = \frac{Z0}{Z21} \times V_{Clamp1} + V_{CD} + VO2$$

When the protection mode is entered, the line current is reduced to a lower value I_{LP} of:

$$I_{LP} = \frac{V_{Clamp2} + (VO1 - VO2)}{R1}$$

When the line voltage becomes lower than V_{LP}, the overload condition is removed and the TCA3388 will leave region 4.

The current drawn from the line by the dc part is used to supply the TCA3388 and peripheral circuits. The excess loop current is absorbed by the voltage regulator at Pin V_{CC}, where a filter capacitor is connected. The reference for the circuit is Pin Gnd.

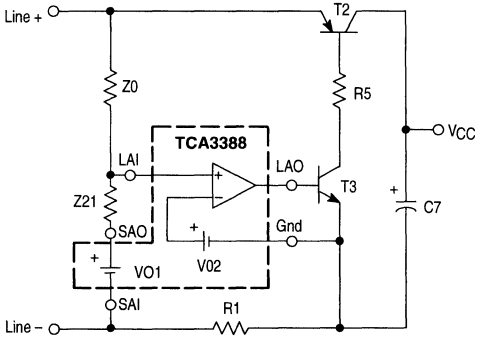
Startup of the application is ensured by an internal startup circuit. When the line current flows, the hook status output pin HSO goes high. This informs the microcontroller that the set is off–hook. When the line current is no longer present the pin will go low again. Because the line current is monitored, and not the line voltage, also an interrupt of the exchange can be recognized.

AC CHARACTERISTICS

Impedance

In Figure 6, the block diagram of the TCA3388 performing the ac impedance is depicted. As can be seen it is partly common with the dc mask block diagram. The part generating the dc mask is replaced by a dc voltage source because for ac, this part has no influence.

Figure 6. AC Stage of the TCA3388



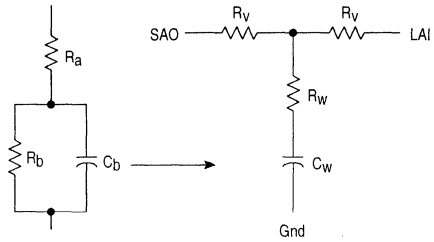
When calculating the ac loop, it can be derived that the set impedance Z_{in} equals

$$Z_{in} = \frac{V_{Line}}{I_{Line}} = R1\left(1 + \frac{Z0}{Z21}\right) \approx R1 \times \frac{Z0}{Z21}$$

As can be noticed, the formula for the ac impedance Z_{in} equals the formula for the dc slope in regions 1 and 3. However, because for the dc slope the resistive part of Z0 and Z21 are used, the actual values for Z_{in} and the dc slopes do not have to be equal.

A complex impedance can be made by making either Z0 or Z21 complex. When Z0 is made complex to fit the set impedance the transmit characteristics will be complex as well. The complex impedance is therefore preferably made via the Z21 network. Because Z21 is in the denominator of the Z_{in} formula, Z21 will not be a direct copy of the required impedance but a derivative of it. Figure 7 gives this derived network to be used for Z21.

Figure 7. Derived Network for Z21 in Case of Complex Set Impedance



$$R_v = \frac{R1 \times Z0}{2(R_a + R_b - R1)}$$

$$R_w = \frac{R1 \times Z0\,(R_a - R1)}{4\,R_b(R_a + R_b - R1)}$$

$$C_w = \frac{4\,R_b^2 \times C_b}{R1 \times Z0}$$

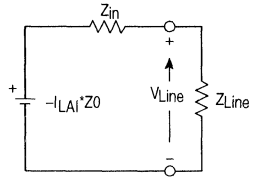
TRANSMIT

When a current is injected on Pin LAI, via the loop depicted in Figure 6, a signal is created on the line. In this way the microphone signals and DTMF signals (from an external source) are transmitted. It can be derived that the signal voltage on the line (V_{Line}) depends on the signal current injected in LAI (I_{LAI}) according to:

$$V_{Line} = -I_{LAI} \times \frac{Z0 \times Z_{Line}}{Z_{in} + Z_{Line}}$$

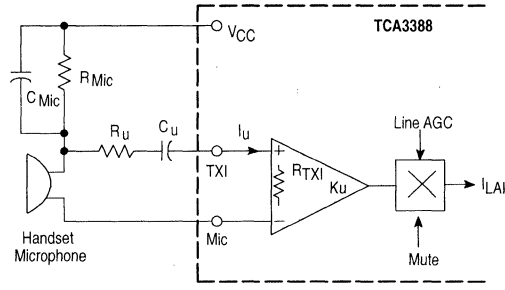
With this relation, a simplified replacement circuit can be made for the transmit amplifier (see Figure 8). Here the product of I_{LAI} and Z0 is replaced by one voltage source.

Figure 8. Replacement Diagram for the Transmit Amplifier



The microphone signal current is derived from the microphone signal according to the schematic in Figure 9.

Figure 9. Microphone Amplifier Input Stage



The input stage of Figure 9 consists of a current amplifier with transfer K_u, an input impedance of 1.0 k (R_{TXI}), plus an attenuator which reduces the signal current at high line currents (AGC). This attenuator can be switched on/off via the microcontroller. The input current I_u within the telephony speech band is derived from the microphone signal according

$$I_u = \frac{V_u}{R_{Mic} + R_u + R_{TXI}} \approx \frac{V_u}{R_u}$$

With: V_u = signal of the microphone only loaded with R_{Mic}

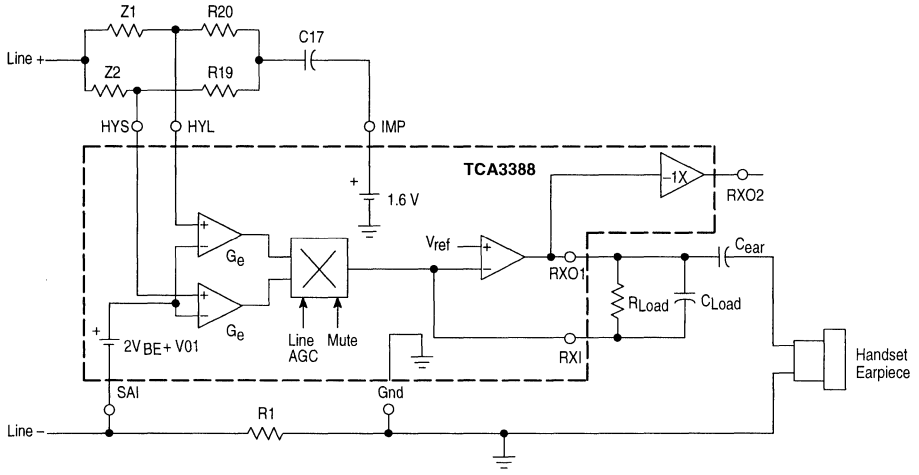
The overall gain from microphone to line (A_{TX}) now follows as

$$A_{TX} = \frac{V_{Line}}{V_u} = \frac{Ku}{R_u} \times \frac{Z0 \times Z_{Line}}{Z_{in} + Z_{Line}}$$

Practically, the gain can be varied only with Z0, R_u and R_{Mic}.

The TCA3388 offers the possibility to mute the microphone, also called privacy mode, by making the MUT Pin high. During pulse–dialing, the microphone bias is switched off. Pin Mic will be made high impedance, shutting off the microphone dc current. This reduces the current consumption of the circuit during pulse–dialing.

Figure 10. Receive Part of the TCA3388



RECEIVE

The receive part of the TCA3388 is shown in Figure 10.

The receive signal is picked up by the amplifiers at the HYL/HYS inputs. These are the same amplifiers present in the dc loop of Figure 5. The signal is first converted to current by the transconductance amplifier with transfer G_e. The multiplier placed after performs the line length AGC. It switches over between the 2 signals at HYS and HYL according to the line current via a modulation factor m. Afterwards, the current is converted back to voltage via the external feedback network Z_{Load}. The resulting voltage is available at output RXO1, and inverted at RXO2.

From the diagram of Figure 10 the receive gain (A_{RX}) can be derived as:

$$A_{RX} = \frac{V_{RXO}}{V_{Line}} = Ge \times R1 \times Z_{Load} \times \left(\frac{1}{Z_H} + \frac{1}{Z_{in}}\right)$$

With: $\frac{1}{Z_H} = \frac{R20}{R1 \times Z1}$ in case of 1 sidetone network and HYS connected to HYL, or

$$\frac{1}{Z_H} = m \times \frac{R20}{R1 \times Z1} + (m-1)\frac{R19}{R1 \times Z2}$$ in case of 2 sidetone networks

More information on Z_H and the modulation factor m can be found under the sidetone characteristics.

The earpiece can either be connected as a single ended or as a differential load. The above calculated gain is valid for the single ended case. When connecting as a differential load, the gain is increased by 6.0 dB. The TCA3388 offers the possibility to mute the signal coming from the line to the earpiece. This can be useful during pulse– and DTMF–dialing.

SIDETONE

When a transmit signal is transmitted to the line, a part of the signal is returned to the receive channel due to the architecture of the 2 to 4 wire conversion of the hybrid. During transmit, the signal on the line will be $-I_{Line} \times Z_{Line}$. During receive, the signal on the line will be $I_{Line} \times Z_{in}$. When replacing Z_{in} in the formula for the receive gain, it follows that the signal on the earpiece output due to a sending signal on the line will be:

$$\frac{V_{ear}}{V_{Line\ (transmit)}} = G_e \times R1 \times Z_{Load} \times \left(\frac{1}{Z_H} - \frac{1}{Z_{Line}}\right)$$

In applications with 1 sidetone network where HYS is connected to HYL, it follows:

$$\frac{1}{Z_H} = \frac{R20}{R1 \times Z1} = \frac{1}{Z_{HL}}$$

Z_H has to be chosen according the average line impedance, and the average linelength of the countries involved in the application. A complex sidetone network can be made via a complex Z1 which is preferred above making R20 complex. The coupling capacitor C17 in series with R20 is meant only to block dc.

For applications with 2 sidetone networks it follows:

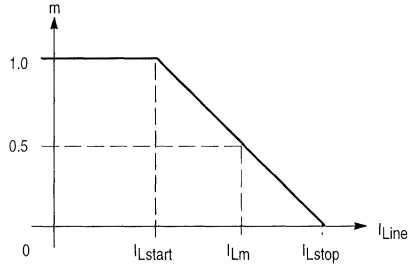
$$\frac{1}{Z_H} = m\frac{R20}{R1 \times Z1} + (m-1)\frac{R19}{R1 \times Z2} =$$

$$m\frac{1}{Z_{HL}} + (m-1)\frac{1}{Z_{HS}}$$

The Z_H thus exists as Z_{HL} for long lines with low line currents and as Z_{HS} for short lines with high line currents. This can be useful in applications such as DECT and handsfree where the sidetone has to be minimized to reduce the effect of delayed echoing and howling respectively. The TCA3388 will automatically switch over between the 2 hybrid networks as a function of line current. This is expressed in the factor m.

The relation between the line current and the factor m is depicted in Figure 11.

Figure 11. Modulation Factor m as a Function of Line Current



For low line currents below I_{Lstart}, thus long lines, the factor m equals 1. This means the hybrid network Z_{HL} is fully used. For high line currents above I_{Lstop}, thus short lines, the factor m equals 0. This means the hybrid network Z_{HS} is fully used. Both networks are used 50% for the intermediate line current Ilm.

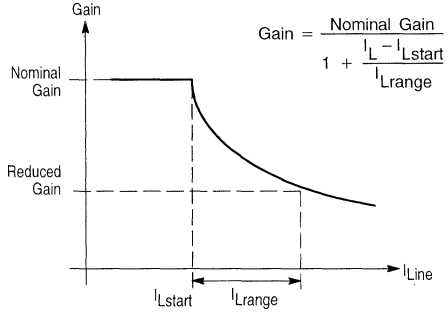
The switch over between the 2 networks takes place in region 3 for the French and U.K. mask and in region 2 for the Low Voltage mask.

LINE LENGTH AGC

The TCA3388 offers the possibility to vary the transmit and receive gain over line length in order to compensate for the loss in gain at longer line lengths. In the block diagrams of the transmit and receive channels (Figures 9, 10) the line AGC is drawn. The line AGC can be switched off by connecting a 150 kΩ resistor between HSO and Gnd. In this case, the transmit and receive gain are lowered by 2.0 dB with respect to the value calculated in the formulas above.

The line AGC characteristics for both transmit and receive channel have the general shape depicted in Figure 12.

Figure 12. General Line AGC Characteristics



For low line currents, and thus long lines, the gains are nominal. When the line current has increased above I_{Lstart} with a current I_{Lrange}, the gain is reduced by 6.0 dB. Due to the general characteristics of the line AGC curve, the gain will be decreased further for higher currents.

For France and U.K., the line AGC will be active in region 3 of the dc characteristics. The I_{Lstart} is approximately equal to the I_{LK}. The range is calculated from:

$$I_{Lrange} = \frac{Z1 \times (I2R - I2CD)}{R_{E3}}$$

For Low Voltage mask, the line AGC is active in region 2.

DIALING

Pulse–dialing is performed by making pin PI high. As a result the output LAO goes low and the loop will be disconnected. Internally the current consumption of the circuit is reduced and the current through the microphone is switched off.

DTMF–dialing is performed by supplying a DTMF signal current to Pin LAI. This is the same node where the microphone signal currents are internally applied. Therefore, for the DTMF gain the same formulas apply. Because the microphone preamplifier is bypassed, there is no influence on DTMF signals by the line length AGC.

A DTMF confidence tone can be generated on the earpiece by injecting a signal current at the RXI pin. Because only the earpiece amplifier itself is used, there are no effects from AGC or hybrid switchover.

For correct DTMF–dialing the pin MUT has to be made high. This mutes both the microphone and earphone preamplifier. In this way signals from the microphone will not be amplified to the line and signals from the line are not amplified to the earpiece.

The complete interfacing of the DTMF generator with the TCA3388 is shown in the typical application.

SUPPORT MATERIAL

Device Specification:	Brief description of the TCA3388, block diagram, device data, test diagram, typical application
User manual TCA3388:	Extended description of the circuit and its concept, adjustment procedure, application hints and proposals
Demonstration board:	Shows performance of the TCA3388 in its basic application

TYPICAL APPLICATION

The typical application below is based on the demoboard of the TCA3388. It contains the speech transmission part, diode bridge, hook switch and microcontroller interfacing. The dc mask setting on the bottom left is given for France, U.K. and Low Voltage applications. The component values are given in the table of Figure 13. The line driver is extended with T1, D5 and R3 which increases the signal swing under low line voltage conditions.

Figure 13. Typical Application

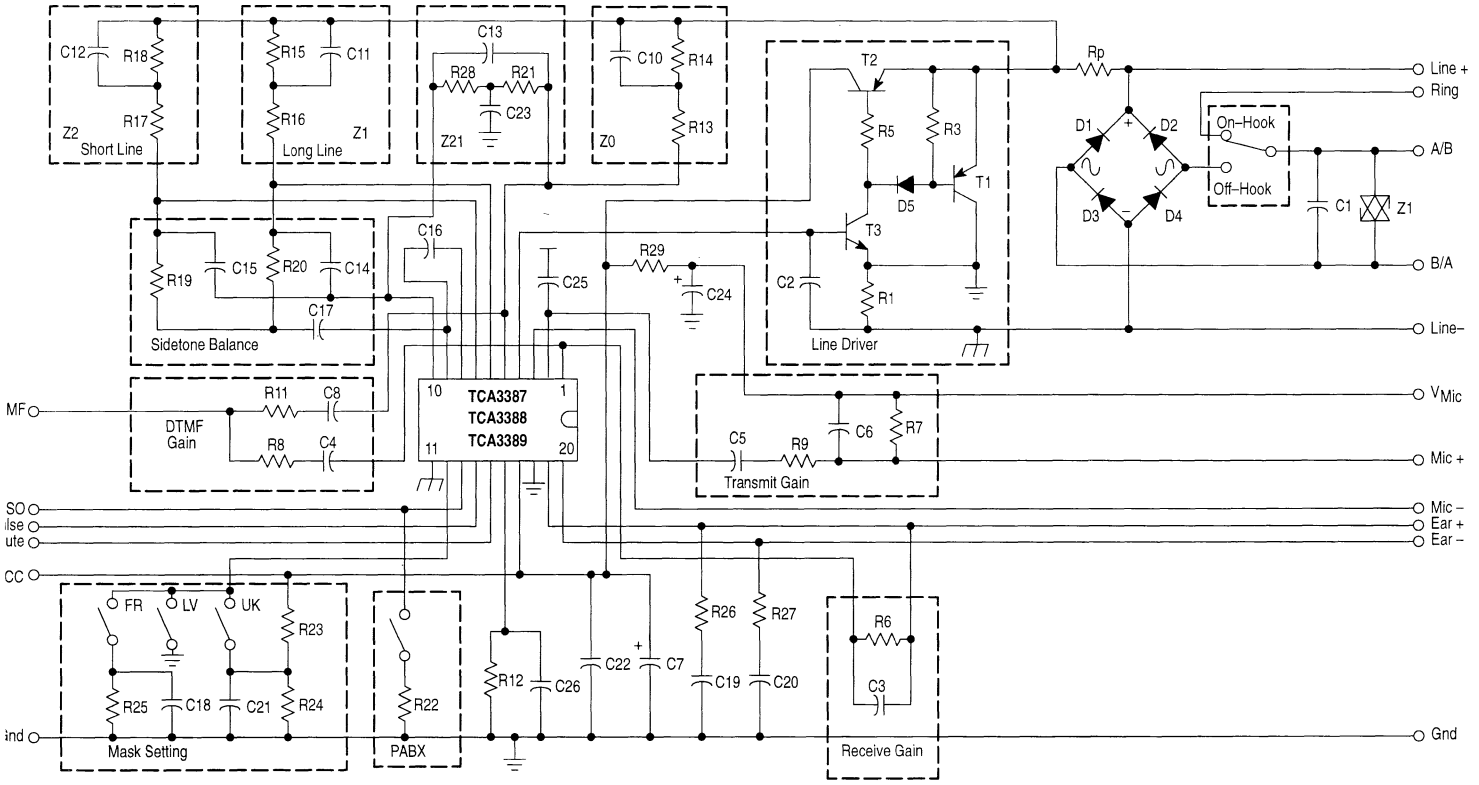


Figure 13. List of Components for Typical Application TCA3388

Item	Location on Board	Application			Remarks
		Basic L.V.	France	U.K.	
R1	Line Driver	16	16	18	
R3	Line Driver	10 k			
R5	Line Driver	1.0 k			
R6	Receive Gain	150 k			
R7	Transmit Gain	2.2 k			
R8	DTMF Gain	470 k			
R9	Transmit Gain	39 k			
R11	DTMF Gain	56 k			
R12	I_{ref}, Pin 16	121 k			1.0%
R13	Z0	580 k	560 k	330 k	
R14	Z0	–	680 k	620 k	
R15	Z1	620 k	1.2 m	1.8 m	
R16	Z1	130 k	300 k	330 k	
R17	Z2	–	620 k	820 k	
R18	Z2	–	820 k	1.5 m	
R19	Sidetone Bal	–	18 k	39 k	
R20	Sidetone Bal	7.5 k	15 k	22 k	
R21	Z21	16 k	16 k	18 k	
R22	PABX	150 k			
R23	Mask Setting	–	–	56 k	
R24	Mask Setting	–	–	47 k	
R25	Mask Setting	–	1.0 m	–	
R26	Pin 19	10			Stability
R27	Pin 20	10			Stability
R28	Z21	0			
R29	Transmit Gain	1.0 k			V_{Mic}
Rp	Line+	0	22	22	
C1	A/B	10 n			EMC
C2	Line Driver	470 p			
C3	Receive Gain	220 p			
C4	DTMF Gain	10 n			
C5	Transmit Gain	10 n			
C6	Transmit Gain	6.8 n			
C7	Pin 17	220 µ			V_{CC}, 10 V
C8	DTMF Gain	10 n			
C10	Z0	–	4.7 n	330 p	
C11	Z1	220 p	120 p	150 p	
C12	Z2	–	82 p	150 p	
C13	Z21	470 p			
C14	Sidetone Bal	470 p			Stability
C15	Sidetone Bal	–	470 p	470 p	Stability
C16	Pin 8	680 n	680 n	2.2 µ	DC Mask
C17	Sidetone Bal	680 n			
C18	Mask Setting	–	470 n	–	
C19	Pin 19	100 n			Stability

Figure 13. List of Components for Typical Application TCA3388

Item	Location on Board	Application			Remarks
		Basic L.V.	France	U.K.	
C20	Pin 20	100 n			Stability
C21	Mask Setting	–	–	10 µ	10 V
C22	Pin 17	100 n			Close to Pin
C23	Z21	–			
C24	Transmit Gain	10 µ			V_{Mic}, 10 V
C25	Pin 2	4.7 n			EMC
C26	Pin 16	1.0 n			EMC
T1	Line Driver	MPSA92			PNP–HV
T2	Line Driver	MJE350			PNP–HV
T3	Line Driver	MPSA42			NPN–HV
D1–D4	Bridge	4 x 1N4004			HV
D5	Line Driver	1N4004			Signal
Z1	A/B	MKP1V270			Sidac

2

Evaluation Kits

3

3

LK45162EVB

Advance Information

Universal Programmable Dual PLL Demo Board

The LK45162EVB is a demo board for the 2.5 to 5.5 V, 60 MHz Universal Dual PLL (MC145162). This demo board implements the front–end receiver of a 1.7/47 MHz base set cordless phone per the United Kingdom standard. It contains three main parts: MCU, FM–IF receiver, and UDPLL. Also, the demo board supports demonstrating reception of additional RF signals encompassing standard cordless phone frequencies of other countries. This is accomplished with proper DIP switch settings and by modifying a capacitor value on the demo board.

LK45162EVB Features

- Front–End Receiver for 1.7/47 MHz Base Set CT–0 per the United Kingdom Standard
- Configurable to One of Seven Different Countries' CT–0 Standard by Proper DIP Switch Setting. The Configurable Country Standards are France, Spain, New Zealand, Australia, United Kingdom, United States, and Korea.
- Eight–Position DIP Switch to Program the On–Board MC145162 for Different Programming Schemes and Different MC145162 Configurations
- Provides MC145162 TEST and NORMAL Mode of Operation
- Two 7–Segment LED Displays Included for Channel Number Indication
- Single 5.0 V Power Supply

MC145162 Features

- Dual Phase Detectors with Programmable Receive, Transmit, Reference, and Auxiliary Reference Dividers
- 2.5 to 5.5 V Operating Voltage Range
- 200 mV p–p Input Sensitivity
- 3 mA @ 2.5 V Operating Current
- Maximum Operation Frequency Up to 60 MHz
- 3– or 4–Pin Serial Interface to External MCU
- Standby Mode

REV 0
8/95

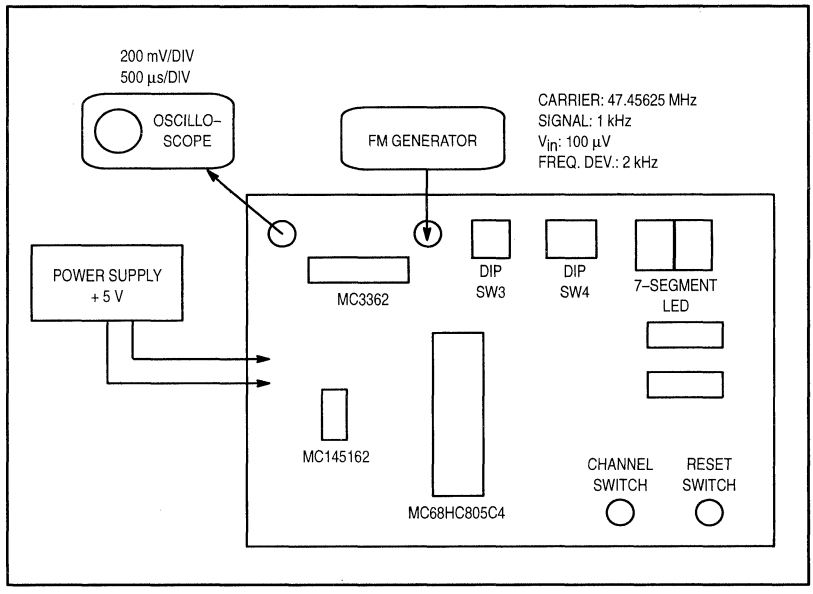


Figure 1. Configuration of LK45162EVB Demo Board

LK45165EVB

Advance Information

Low-Voltage Universal Programmable Dual PLL Demo Board

The LK45165EVB is a demo board for the 1.8 V, 60 MHz Universal Dual PLL (MC145165). This demo board implements the front–end receiver of a 45/48 MHz base set cordless phone per the Chinese standard. It contains four main parts: MCU, adjustable voltage regulator, FM–IF receiver, and UDPLL. Also, the demo board supports demonstrating reception of additional RF signals encompassing standard cordless phone frequencies of other countries. This is accomplished with proper DIP switch settings and by modifying a capacitor value on the demo board.

LK45165EVB Features

- Front–End Receiver for 45/48 MHz Base Set CT–0 per the Chinese Standard
- Controllable Voltage Regulator to Supply 1.8 to 3.6 V to On–Board Low–Voltage UDPLL MC145165 and FM–IF Receiver MC13135
- Configurable to One of Eight Different Countries' CT–0 Standard by Proper DIP Switch Setting. The Configurable Country Standards are France, Spain, New Zealand, Australia, United Kingdom, United States, Korea, and China.
- Eight–Position DIP Switch to Program the On–Board MC145165 for Different Programming Schemes and Different MC145165 Configurations
- Provides MC145165 TEST and NORMAL Mode of Operation
- Two 7–Segment LED Displays Included for Channel Number Indication
- Single 5.0 V Power Supply

MC145165 Features

- Dual Phase Detectors with Programmable Receive, Transmit, Reference, and Auxiliary Reference Dividers
- 1.8 to 3.6 V Operating Voltage Range
- 200 mV p–p Input Sensitivity
- 1.5 mA @ 1.8 V Operating Current
- Maximum Operation Frequency Up to 60 MHz
- 3– or 4–Pin Serial Interface to External MCU
- Standby Mode

REV 0
8/95

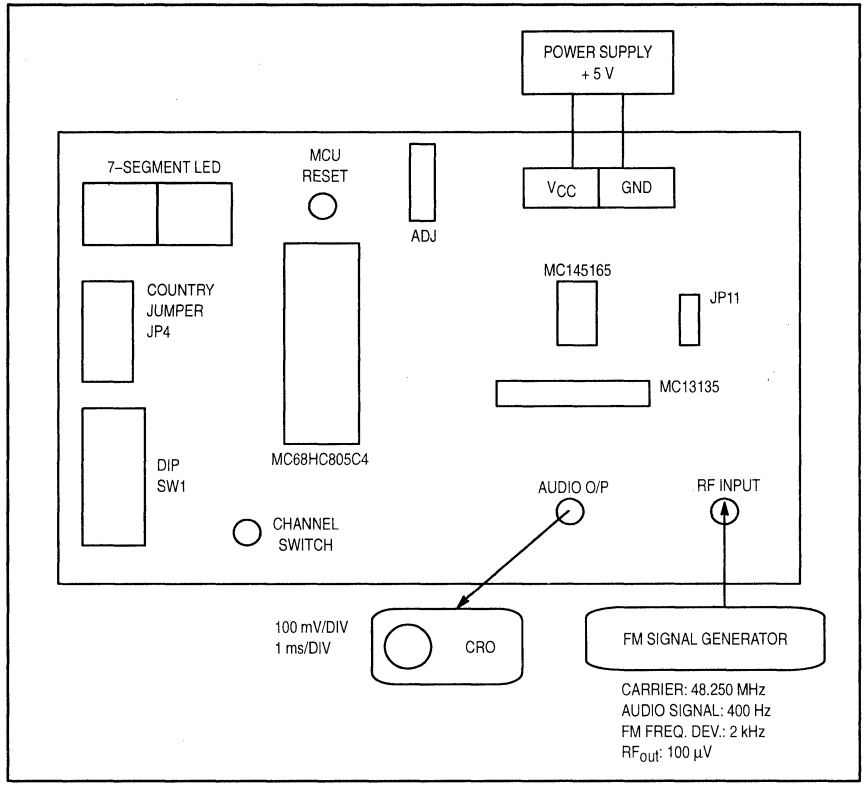


Figure 1. Configuration of LK45165EVB Demo Board

MC145190EVK
MC145191EVK
MC145200EVK
MC145201EVK

Technical Summary

MC145190, MC145191, MC145200 and MC145201 Evaluation Board Manual

INTRODUCTION

The MC145190EVK, '191EVK, '200EVK, and '201EVK are versions of one board with a few component changes. They allow users to exercise features of the four devices and to build PLLs which meet individual performance requirements. The control program works with any board and can be used with other Motorola PLL devices (MC145192, MC145202, MC145220*). (NOTE: The MC145220 is not available with Rev. 3.0 software.) It will select frequency defaults that apply to each. All board functions are controlled through the printer port of an IBM PC. Up to three different EVKs may be controlled at the same time from one printer port. The functional block diagram is given in Figure 1.

This manual is divided into two sections. Section 1 describes the hardware and Section 2 covers the software control program.

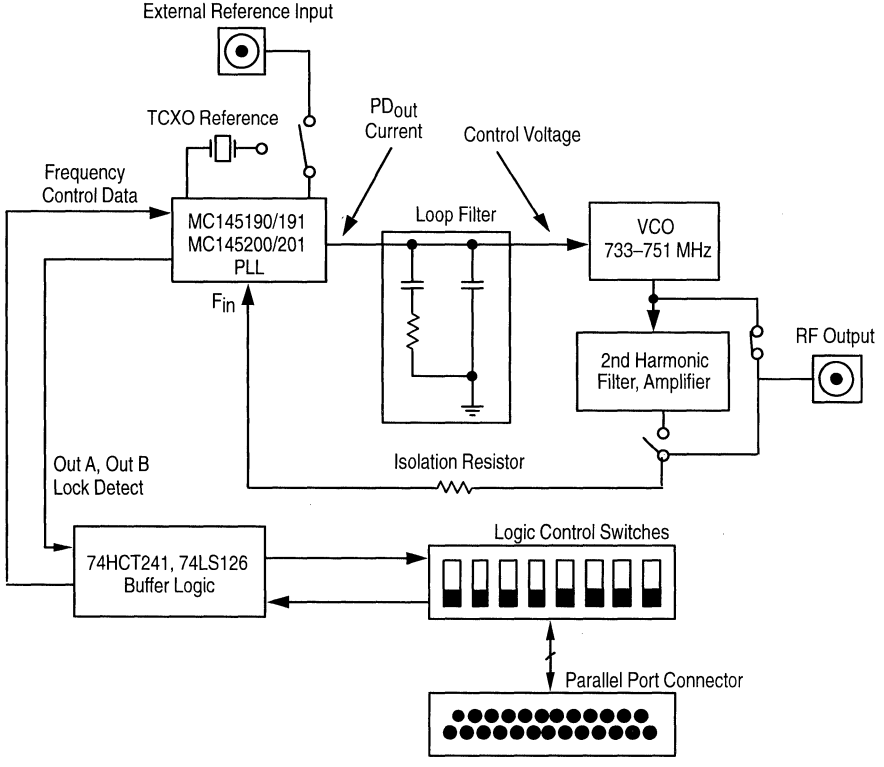


Figure 1. Evaluation Kit Block Diagram

REV 0
9/95

SECTION 1 – HARDWARE

FEATURES

1. The EVK is a complete working synthesizer, including VCO.
2. Control program is written in Turbo Pascal.
3. Board is controlled by an IBM PC–compatible computer through the printer port.
4. Up to three boards can be operated independently through one printer port.
5. A prototype area and mounting holes are provided for VCOs, mixers, and amplifiers.
6. External reference input can be used.
7. Five element loop filter is included.
8. Frequency range of operation, step size and reference frequency can be changed in the control program.
9. Lock Detect, Out A, and Out B on any single board are accessible through the printer port.

CONTENTS OF EVALUATION KIT

1. Assembled evaluation board.
2. Nine–foot flat cable with four DB–25 male connectors.
3. MC145190/191/200/201 EVK manual.
4. 3.5″ PC–compatible disk containing compiled program.
5. PLL device data sheets.

GETTING STARTED

To perform basic functions, do the following:

1. Plug in 12 volts at J6, observing the polarity marked on the board.
2. Short circuit section 1 of the DIP switch (S1) and open circuit all other sections.
3. Connect the supplied flat cable between the computer printer port and the DB–25 connector on the board (J5).
4. Type PLLDEMO at the DOS prompt. Then press enter.
5. Type the number that corresponds with the type of board given in the on–screen menu. Then press Q.

You should now see the main menu displayed. There should be a signal present at J8 on the current output frequency given in the main menu. If the signal is not on the correct frequency, check to see if your printer card address is $278 (hexadecimal 278). If not, then select the P menu item and enter the correct address. After returning to the main menu, select the I menu item to send data to the board. You should now be on frequency.

MODIFICATIONS

The user may modify the hardware, such as utilizing a different VCO, by using the prototyping area of the board. After such modifications are made, the default values in the software may need to be changed. This is facilitated from screen #2 'Select from the available options' screen.

Note that the on–board voltage regulators allow for maximum control voltage to the VCO of approximately 7.8 V for the MC145190EVK and MC145200EVK. The maximum VCO control voltage is approximately 4.3 V for the MC145191EVK and MC145201EVK. The minimum voltage for all four devices is 0.5 V.

TYPICAL PERFORMANCE

Common to all four kits, unless noted.

Supply Voltage (J6)	11.5 – 12.5 V
Supply Current (J6) (Note 1)	120 mA
Available Current (Note 2)	60 mA
Frequency Range ('190)	741 – 751 MHz
Frequency Range ('191)	733 – 743 MHz
Frequency Range ('200)	1482 – 1502 MHz
Frequency Range ('201)	1466 – 1486 MHz
Reference Frequency	14.4 MHz
Temperature Stability (– 30°C to + 85°C)	< ± 2 ppm
TCXO Aging	< ± 1 ppm / year
Step Size ('190, '191)	100 kHz
Step Size ('200, '201)	200 kHz
Power Output	5 – 8 dBm
2nd Harmonic Level ('190, '191)	< – 18 dB
Fundamental Level ('200, '201)	< – 28 dB
3rd Harmonic Level	< – 18 dB
Frequency Accuracy ('190, '191)	± 1.5 kHz
Frequency Accuracy ('200, '201)	± 3.0 kHz
Reference Sidebands	– 70 dB
Phase Noise (100 Hz, '190, '191)	– 69 dBc/Hz
Phase Noise (100 Hz, '200, '201)	– 64 dBc/Hz
Phase Noise (10 kHz, '190, '191) (Note 3)	– 99 dBc/Hz
Phase Noise (10 kHz, '200, '201) (Note 3)	– 92 dBc/Hz
Switching Time (Note 4)	2.6 ms

NOTES:

1. Supply current is current the board requires without user modifications.
2. Available current is the sum of currents available to the user (in the prototype area) from the 5 V and 8.5 V supply. The 12 V supply is not regulated. Current at 12 V is limited by the external power supply. If the on–board VCO and amplifier are disconnected from the power bus, more current can be drawn in the prototype area. The current flowing into U3 (the 8.5 V regulator) should not exceed 180 mA. This will limit temperature rise in U3.
3. 10 kHz phase noise is limited by the PLL device noise. For low noise designs, the loop bandwidth is made more narrow and the VCO is relied upon to provide the 10 kHz phase noise. This can be seen on the EVKs since the VCO has much lower noise.
4. 10 MHz step, within ± 1 kHz of final frequency ('190, '191).
   20 MHz step, within ± 2 kHz of final frequency ('200, '201).

SUPPORT MATERIAL

To provide further information, the following documents are included:

1. Schematic diagram of '190/191/200/201EVK.
2. Separate Bill of Materials for each board.
3. Parts layout diagram.
4. Mechanical drawing of board.
5. MC145190/191 and MC145200/201 data sheets.
6. Printer port diagram.
7. Typical signal plots for each type of EVK.

PRODUCTION TEST

After assembly is complete, the following alignment and test is performed on '190 and '191EVK ('200 and '201EVK):

1. The control program is started in single board '190EVK ('200EVK) mode.
2. L menu item is selected.
3. Power is applied to the board. DIP switch section 1 is closed circuit with all others being open circuit.
4. After attaching computer cable, menu item I is selected.
5. Trim resistor VR1 is adjusted to obtain an output frequency at J8 of 740.999 – 741.001 MHz (1481.998 – 1482.002 MHz).
6. Voltage at the control voltage test point is measured. It must be 2.8 – 3.6 V.
7. When testing more than 1 board, steps 3 – 6 are repeated.

If in step 5 it isn't possible to obtain a signal on frequency, menu item P should be selected and the correct printer port address entered. Menu item I would then be selected to reload the data.

BOARD OPERATION

A computer is connected to the DB–25 connector J5. Data is output from the printer port. The printer card is in slot 0 using the default address in the control program. Data is sent to the PLL device (U1) through the DIP switch (S1), and 74HCT241 buffer (U5). A '190/191/200/201 PLL has three output lines which are routed through a 74LS126 line driver (U2) to the computer.

U5, the 74HCT241, provides isolation, logic translation and a turn–on delay for PLL input lines. Logic translation is needed from the TTL levels on the printer port to the CMOS levels on the '190/191 inputs. Turn–on delay is used to ensure the power–on reset functions properly. The clock line to the PLL must be held low during power up.

A 12 V power supply should be used to power the board at J6 (Augat 2SV–02 connector). The 2SV–02 will accept 18–24 AWG bare copper power leads. No tools are needed for connection. If power is properly connected, LED D2 will be lit.

Power passes from J6 to U3 (78M08 regulator) configured as an 8.5 V regulator. D1 increases output voltage of the regulator by 0.6 V. In the '190 and '200 boards, 8.5 V is routed through J3 to the charge pump supply, VCO, and RF amplifier. The '191 and '201 boards use 8.5 V to power the VCO and RF amplifier. J3 is a cut–trace and jumper. If it is desired to power the 8.5 V circuits directly, the trace under J3 can be cut, J3's shorting plug is removed, and 8.5 V is applied through J7 (2SV03 power connector).

Power for the 5 V logic is provided by U4 (78M05). U4 steps down the 8.5 V from U3. Output voltage from U4 passes through J4, the 5 V cut–trace and jumper. To supply separate power to logic, the trace under J4 is cut, J4 shorting plug is removed, and 5 V is applied to J7. U3 and U4 are cascaded to lower their individual voltage drops. This lowers the power dissipated in the regulators.

The PLL loop is composed of the PLL device (U1), 733 – 751 MHz VCO (M1), passive loop filter (R11, R12, C4, C5, C6) and second harmonic filter amplifier (U6). A passive loop filter was used to keep the design simple, reduce noise, and reduce the quantity of traces susceptible to stray pickup. About 56 dB rejection of fundamental and 23 dB gain is provided by the harmonic filter amplifier. This allows the '200 or '201 to lock at 1466 – 1502 MHz. The harmonic filter amplifier is bypassed on the '190 and '191.

A single VCO model is used for all boards. It is an internal Motorola part which is not sold for other applications. The '190 and '191 have different frequency ranges. This is due to the lower charge pump supply voltage of the '191. A common 10 MHz tune range allows the same loop filter components to be used. For the same reason, the '200 and '201 tune range is 20 MHz with double the step size of the '190 or '191. RF is fed to the PLL chip F_{in} input through a voltage divider. These two resistors terminate the PLL chip RF input with 50 ohms and provide isolation.

All boards use a phase detector current of 2 mA. J1 and J2 are removable jumpers and cut traces. They are used as connection points for a current measurement of V_{PD} or V_{CC}. J11 and J12 are wire jumpers that select 5 V or 8.5 V for V_{PD}. A potentiometer VR1 is used to set M2 (14.4 MHz TCXO) on frequency.

COMPONENTS UNIQUE TO EACH EVK

Components that are not the same on all EVKs are given in the following table:

	'190 EVK	'191 EVK	'200 EVK	'201 EVK
U1	MC145190	MC145191	MC145200	MC145201
R2	47 kΩ	22 kΩ	47 kΩ	22 kΩ
R8	0 Ω	0 Ω	not used	not used
C22	not used	not used	1.0 pF	1.0 pF
J11	connected	not used	connected	not used
J12	not used	connected	not used	connected

EXTERNAL REFERENCE INPUT

As shipped, all boards are configured for a 14.4 MHz TCXO (supplied). To use an external reference, disconnect J13 and connect J9. Use a reference signal at J10 which complies with data sheet requirements. Then modify the reference frequency in the program main menu to reflect the changes made ([F] menu item).

DATA TRANSFER FROM COMPUTER TO EVK

To control the serial input EVK with the parallel printer port, a conversion is done. Printer cards are designed to output 8 bits through eight lines. A bit mask is used to obtain the bit combination for the three required output lines (Data, Clock, Load). As bytes are sent to the printer card in sequence, it appears to be a serial transfer. The printer port was used because data transfer using the serial port would have been much slower. A standard IBM PC can support a parallel port data rate of 4.77 MHz.

IBM PCs and compatibles can accept up to three printer port cards. These ports are called LPT1, LPT2 and LPT3. Each printer card has jumpers or DIP switches on it to set a unique address. Two sets of addresses are in common use. One set applies to IBM PC XT, AT, and clones. The other is for the PS 2 line. To load data into the EVK, the correct address must be selected. The program default is $278, which is LPT1 in a clone. If $278 is not the address in use, it must be modified by entering the O menu item in the main menu. All allowed addresses given in hexadecimal are as follows:

Label	IBM PC and Clones	PS 2
LPT1	278	3BC
LPT2	378	378
LPT3	3BC	278

Up to three EVK boards can operate independently from one printer port. All lines on the printer port are connected to every EVK. Even with three boards operating, only three output lines (Clock, Data and Load) from the printer card are used. If two boards are controlled together, data for the second board is received from the Output A of the first. Output A is a configurable output on 190/191/200/201 devices, which in this case is used to shift data through chip 1 into chip 2. Output A and Data are connected using a printer port input line. This was done to avoid connecting extra wires. Fortunately not all port input lines are needed for computer input. Load and Clock are common to both boards.

A three–board cascade is handled similarly to a two–board cascade. Out A on the first board is fed to Data on the second. Out A on the second connects to Data on the third. Instructing the program on the quantity of boards connected together allows it to modify the number of bits sent.

All boards have a DIP switch S1 which gives each a unique address. The configuration menu is used to tell the program what type of board is connected at a board address. Switch positions for all possible addresses are given in Figure 2.

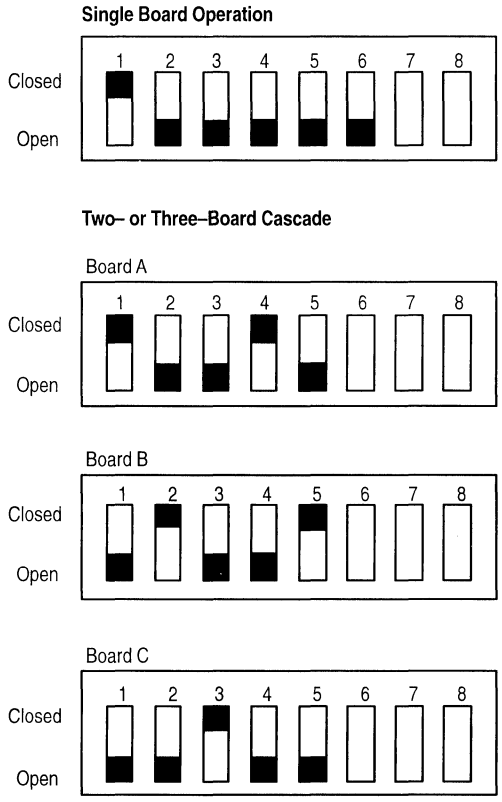


Figure 2. Switch Positions

In Figure 2, DIP switch sections 6, 7, and 8 allow the computer to read Out A, Out B or Lock Detect from the PLL device. Each of the inputs can only be read on one board at a time. But each item could be read on a different board. In a three–board cascade, Out A could be read from the first board, Out B from the second, and Lock Detect from the third. There is no way to determine in software the board address of a particular input. The control program doesn't make use of these inputs. Pin assignment on the printer port connector is:

Label	Pin Number
Out A	12
Out B	13
Lock Detect	15

PRINTER PORT CONFIGURATION

Printer port outputs on an IBM PC or clone use TTL–LS logic levels. Inputs are one TTL–LS load. Signal lines can be used for any purpose. The standard names, direction of data flow, true and inverted data are shown in Figure 3.

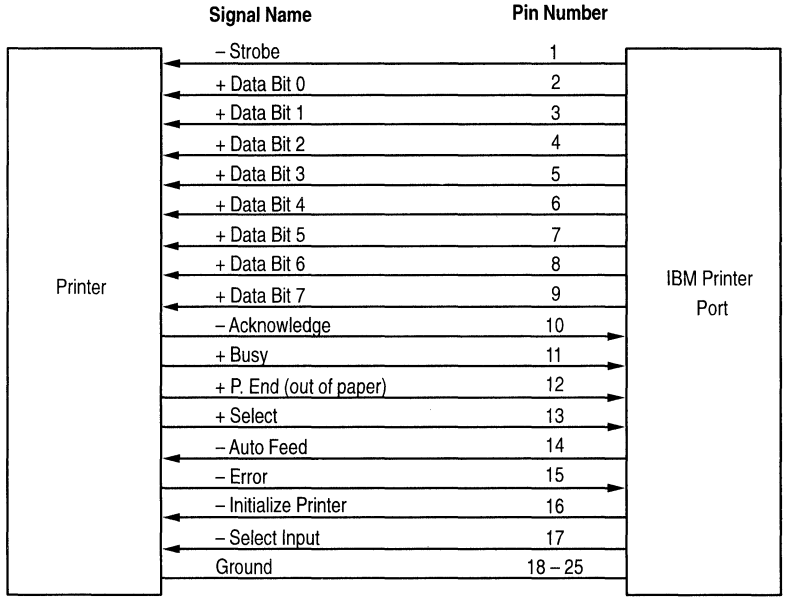


Figure 3. Printer Port Data Lines

Pin numbers for the port connector are shown in Figure 4.

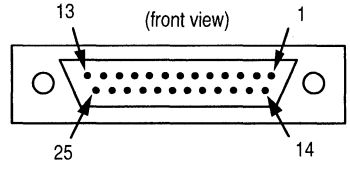


Figure 4. DB–25 Male Connector

SECTION 2 – SOFTWARE SUMMARY

The MC145xxx EVK control program (PLLDEMO) is used to program all PLL evaluation kits. It will simultaneoulsy control up to three different boards independently from one printer port. All features of the PLL device may be accessed. Default frequencies can be modified to allow us of different channel spacings and VCOs.

User input errors are detected and appropriate messages are displayed.

To show the format of PLLDEMO, one of the eighteen program screens is shown below:

Screen #2 'Select from the available options'

```
                Welcome to MC145xxx EVK Demonstration Program, rev 3.0
                          Select from the available options

Available Boards - Current target board is: A, MC145190 EVK
 Brd [A]!: MC145190 EVK    Brd [-]!: N/A              Brd [-]!: N/A
-------------------------------------------------------------------------------
MC145xxx Frequency Commands - Current Output Frequency is 746 MHz
 [L]! Set to low freq      741 MHz       [W] Change default low freq.
 [M]! Set to med. freq     746 MHz       [Y] Change default med. freq.
 [H]! Set to high freq.    751 MHz       [Z] Change default high freq.
 [U]! Step frequency up by step size     [O] Set PLL output frequency
 [D]! Step frequency down by step size   [F] Set REFin freq. & channel spacing
MC145xxx Additional Commands
 [E]  Set function of output A           [N] Change C register and Prescale
 [R]  Set crystal/reference mode - Current mode is Ref. mode, REFout low


-------------------------------------------------------------------------------
Initialization/System Setup Commands:
 [P]  Set output port address - Current address is $278
 [G]  Change board definitions
 [I]  Initialize board(s), Write all registers

              [X]! Terminate demonstration program. [?]! View help screen.
```

MC145192EVK
MC145202EVK

Advance Information

PLL Frequency Synthesizer Evaluation Kits

Evaluation kits are available for the MC145192 (100 MHz – 1.1 GHz) and MC145202 (500 MHz – 2 GHz) PLLs. These are low voltage devices that operate down to 2.7 V.

Features

- PLL is Controlled Through the Printer Port of an IBM PC or Clone. PLLDEMO (the Control Program) Operates Both Boards.
- User Input is Checked for Errors by PLLDEMO and the Specific Problem is Indicated
- Three EVKs Can Be Independently Controlled from One Printer Port
- The Control Program Can Be Used to Modify Any Feature of the PLL Device
- A Prototype Area and Supply Voltages are Provided for an Optional User–Supplied VCO
- All Frequency Defaults are Easy to Modify
- A Common Printed Circuit Board is Used that Allows One Type of EVK to be Converted into the Other with a Few Component Changes
- A Motorola Saber TCXO and Low Noise VCO are Included

* This document contains information on a new product. Specifications and information herein are subject to change without notice.

REV 0
9/95

MC145460EVK

Advance Information

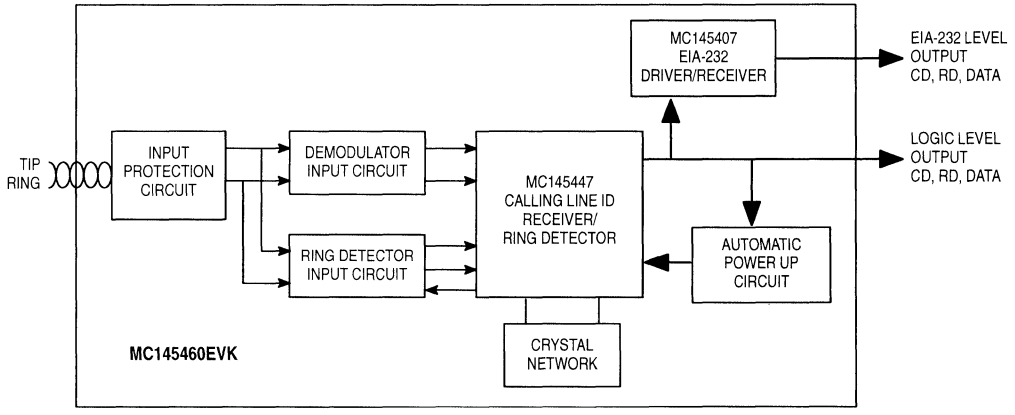
Calling Line I.D. Receiver Evaluation Kit

The MC145460EVK is a low–cost evaluation platform for the MC145447 Calling Line I.D. Receiver with Ring Detector. The MC145460EVK will facilitate development and testing of products that support the Bellcore customer premises equipment (CPE) data interface, which enables services such as Calling Number Delivery (CND). The MC145447 can be easily incorporated into any telephone, FAX, PBX, key system, answering machine, CND adjunct box or other telephone equipment with the help of the MC145460EVK development kit.

MC145460EVK Features

- Easy Clip–On Access to Key MC145447 Signals
- Generous Prototype Area
- Configurable for MC145447 Automatic or External Power–Up Control
- EIA-232 and Logic Level Ports for Connection to Any PC or MCU Development Platform
- Carrier Detect, Ring Detect and Data Status LEDs
- Component Layout for Input Protection Circuit
- Documentation: MC145460EVK User Guide, MC145447 Data Sheet
- Additional MC145447 Sample

MC145460EVK BLOCK DIAGRAM



This document contains information on a new product. Specifications and information herein are subject to change without notice.

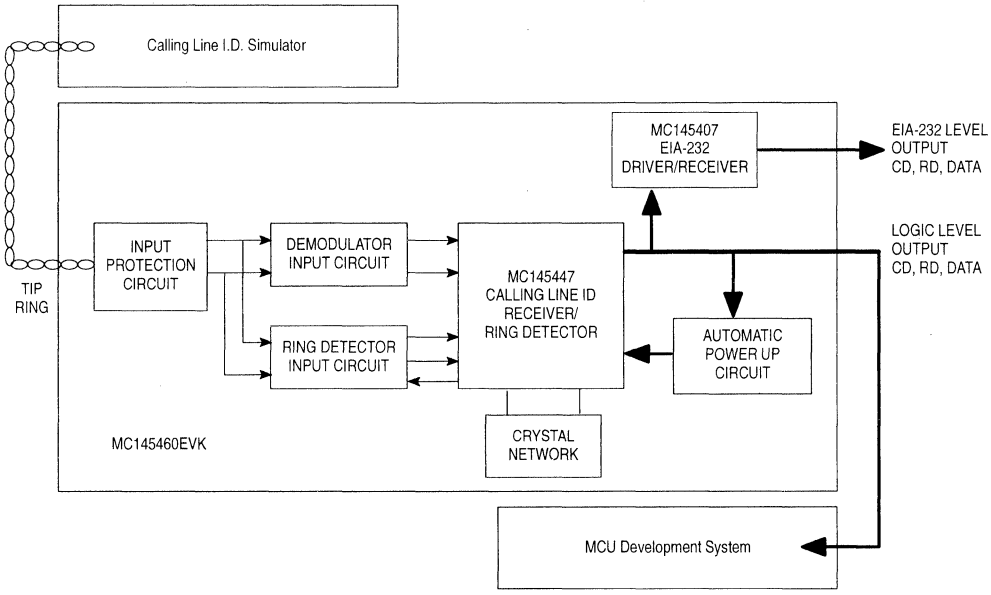


Figure 1. Calling Line I.D. Product Development System

MC145536EVK

Advance Information

Codec-Filter/ADPCM Transcoder Evaluation Kit

The MC145536EVK is the primary tool for evaluation and demonstration of the MC145480 Single + 5 V Supply PCM Codec–Filter and the MC145532 ADPCM Transcoder. The MC145536EVK provides the user with the hardware needed to evaluate the many separate operating modes under which the MC145480 and MC145532 are intended to operate.

General

- Provides Stand Alone Evaluation on Single Board
- + 5 V Only Power Supply
- Easily Interfaced to Test Equipment, Customer System, Second MC145536EVK or MC145537EVK
- Convenient Access to Key Signals
- Generous Prototype Area for Application Development
- The Kit Provides Analog–to–Analog, Analog–to–Digital (64 kbps PCM; 32, 24, or 16 kbps ADPCM) or Digital– (64 kbps PCM; 32, 24, or 16 kbps ADPCM) to–Analog Connections
- Handset Included
- Schematics, Data Sheets, and User's Manual Included

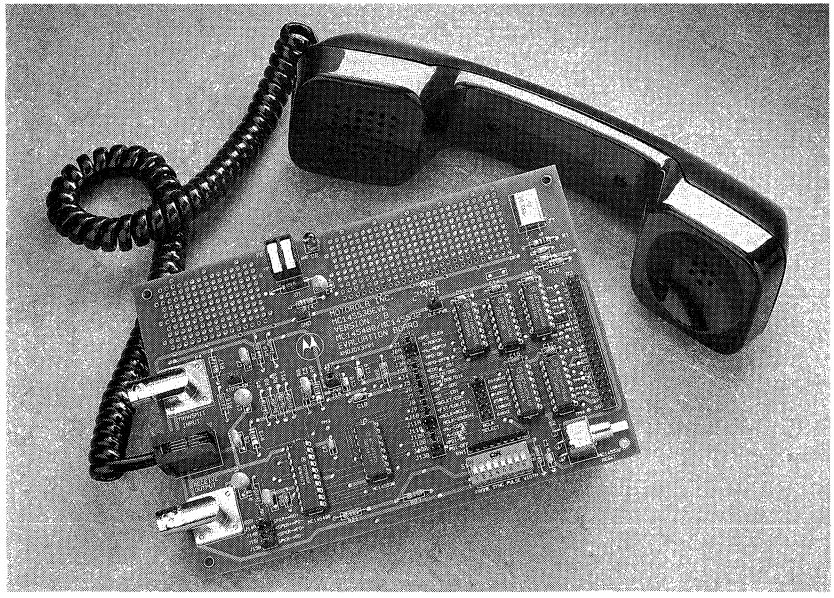
MC145480

- Single + 5 V Power Supply
- Typical Power Dissipation of 25 mW, Power Down of < 1 mW
- Conforms to CCITT and Bell Specifications
- Mu–Law or A–Law Companding
- Differential Analog Circuit Design for Lowest Noise
- 20–Pin Plastic Package
- Production in 1.5 Micron CMOS Process
- UDR Design Layout Rules for Core Cell Applications

MC145532

- Single–Chip Full–Duplex PCM–to–ADPCM Encoder and ADPCM–to–PCM Decoder
- Achieves High Audio Quality at Reduced Bit Rates
- PCM Data Rate of 64 kbps
- ADPCM Data Rates of 32, 24, or 16 kbps
- Conforms to CCITT and ANSI ADPCM Standards
- Custom DSP Engine Optimized for ADPCM Algorithm
- Volume Production in 1.5 Micron CMOS Process
- UDR Design Layout Rules for Core Cell Applications

This document contains information on a new product. Specifications and information herein are subject to change without notice.



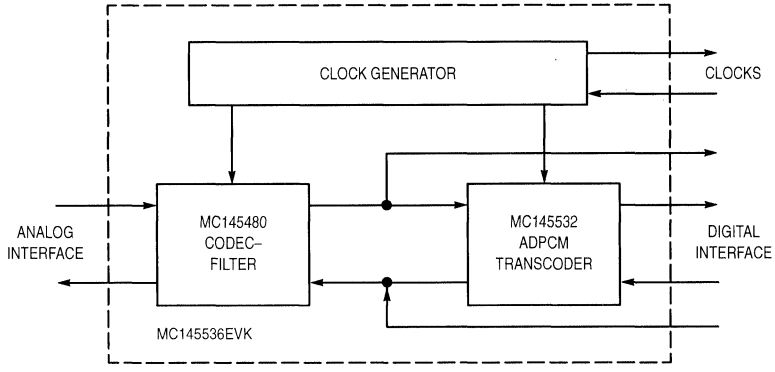


Figure 1. MC145536EVK System–Level Block Diagram

MC145537EVK

Advance Information

MC14LC5540 ADPCM Codec Evaluation Kit

The MC145537EVK is the evaluation platform for the MC14LC5540 ADPCM Codec. This board provides the clock generator circuitry and microcontroller interface to facilitate the evaluation of the MC14LC5540.

MC145537EVK Hardware Features

- Supports MC14LC5540 + 5 V or + 3 V Operation
- Handset Interface/Handset Included
- Easy Access to All Analog and Digital Data, Clock, and Enable Signals
- EIA–232–D/ V.28 Terminal Control
- Analog–to–Digital (64 kbps PCM; 32, 24, or 16 kbps ADPCM) Path
- Digital– (64 kbps PCM; 32, 24, or 16 kbps ADPCM) to–Analog Path
- Supports Hardware Loopbacks
  - Analog–to–Analog
  - Digital–to–Digital
- Ability to Connect Two MC145537EVKs Back–to–Back
- Ability to Connect MC145537EVK and MC145536EVK Back–to–Back for + 5 V Operation Only

MC145537EVK Software Features

- MC68HC705C8 Resident Monitor
- Stand Alone or Terminal Operation
- Device Driver for Serial Control Port Interface
- Ability to Read/Write SCP Registers in MC14LC5540
- Registers Can Be Individually Displayed and Modified
- Help Menu

REV 1
10/95

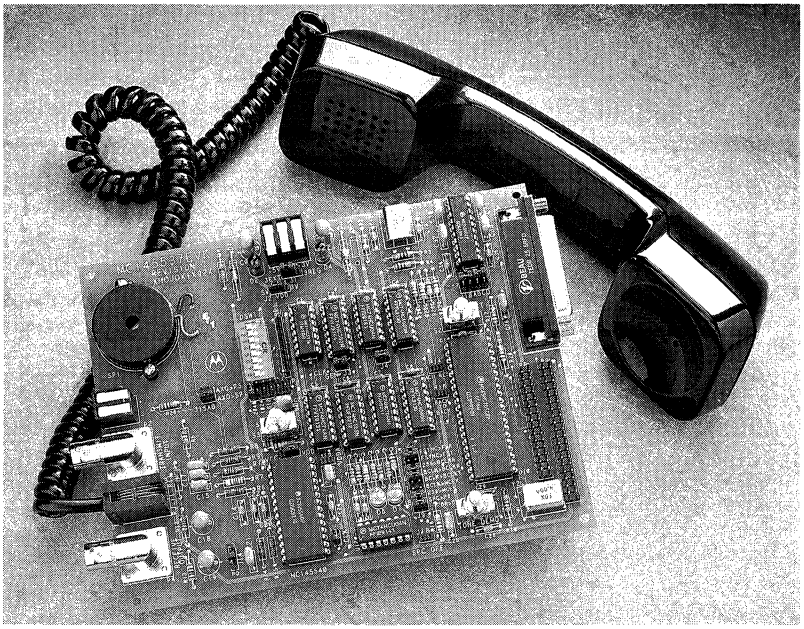
GENERAL OVERVIEW

The MC14LC5540 ADPCM Codec is a single–chip implementation of a PCM Codec–Filter and an ADPCM Encoder/Decoder, and therefore provides an efficient solution for applications requiring the digitization and compression of voiceband signals. This device is designed to operate over a wide voltage range, 2.7 to 5.25 V, and as such is ideal for battery powered as well as ac powered applications. The MC14LC5540 ADPCM Codec also includes a serial control port and internal control and status registers that permit a microcomputer to exercise many built–in features.

The MC14LC5540 ADPCM Codec is designed to meet the 32 kbps ADPCM conformance requirements of CCITT Recommendation G.721 and ANSI T1.301. It also meets ANSI T1.303 and CCITT Recommendation G.723 for 24 kbps ADPCM operation, and the 16 kbps ADPCM standard, CCITT Recommendation G.726. This device also meets the 64 kbps PCM conformance specification of the CCITT G.714 Recommendation.

The MC145537EVK is the evaluation board for the MC14LC5540 ADPCM Codec. This board provides the clock generation that controls both the transfer of PCM and ADPCM data into and out of the MC14LC5540, as well as determining the data compression rate (16 kbps ADPCM, 24 kbps ADPCM, 32 kbps ADPCM, or 64 kbps PCM) for the ADPCM transcoder function. This data compression rate is determined by the duration of the transmit and receive frame synchronization pulses measured in data clock cycles, which are programmed by an 8–position DIP switch. This evaluation board has voltage level shifters that allow the MC14LC5540 to operate at a voltage lower than the + 5 V supply required for the clock generator and microcontroller.

This MC145537EVK has an MC68HC705C8P microcontroller, which is running a monitor routine that interfaces the MC14LC5540 to a 9600 bps EIA–232 port for access by a computer terminal. The microcontroller provides access to the programming registers of the MC14LC5540 for read and write operations. This facilitates exercising both the hardware options for trim gain, sidetone, analog signal routing and charge–pump operation, and the software options of the dual tone generator, noise burst detect and receive gain control. The evaluation board is designed to configure the MC14LC5540 after reset such that the charge–pump is operating and the device is encoding and decoding analog at the rate determined by the clock circuitry. This allows the MC145537EVK to be functional without a computer terminal.



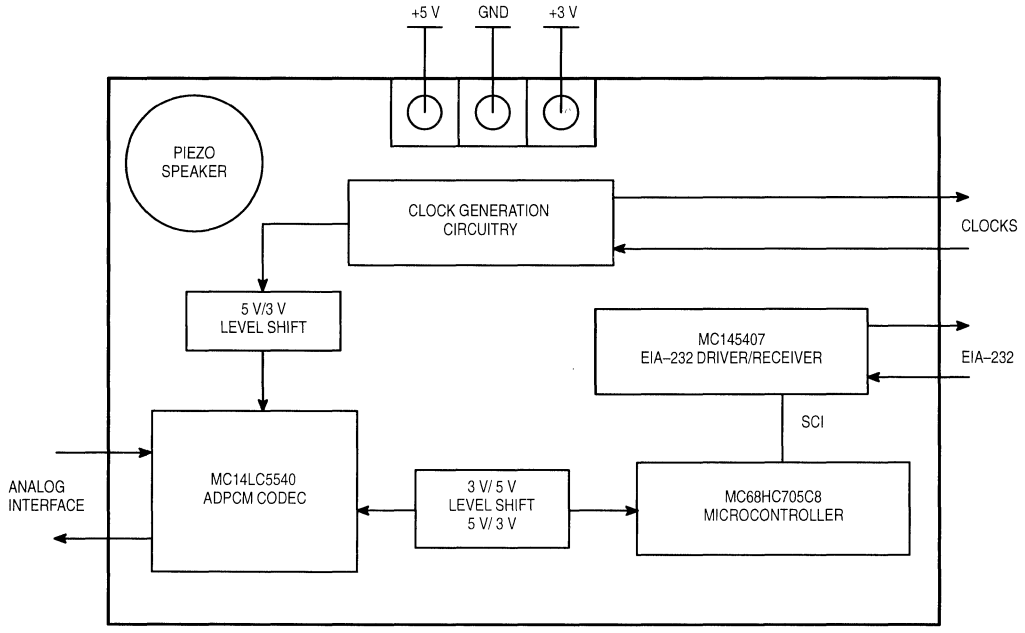


Figure 1. MC145537EVK Block Diagram

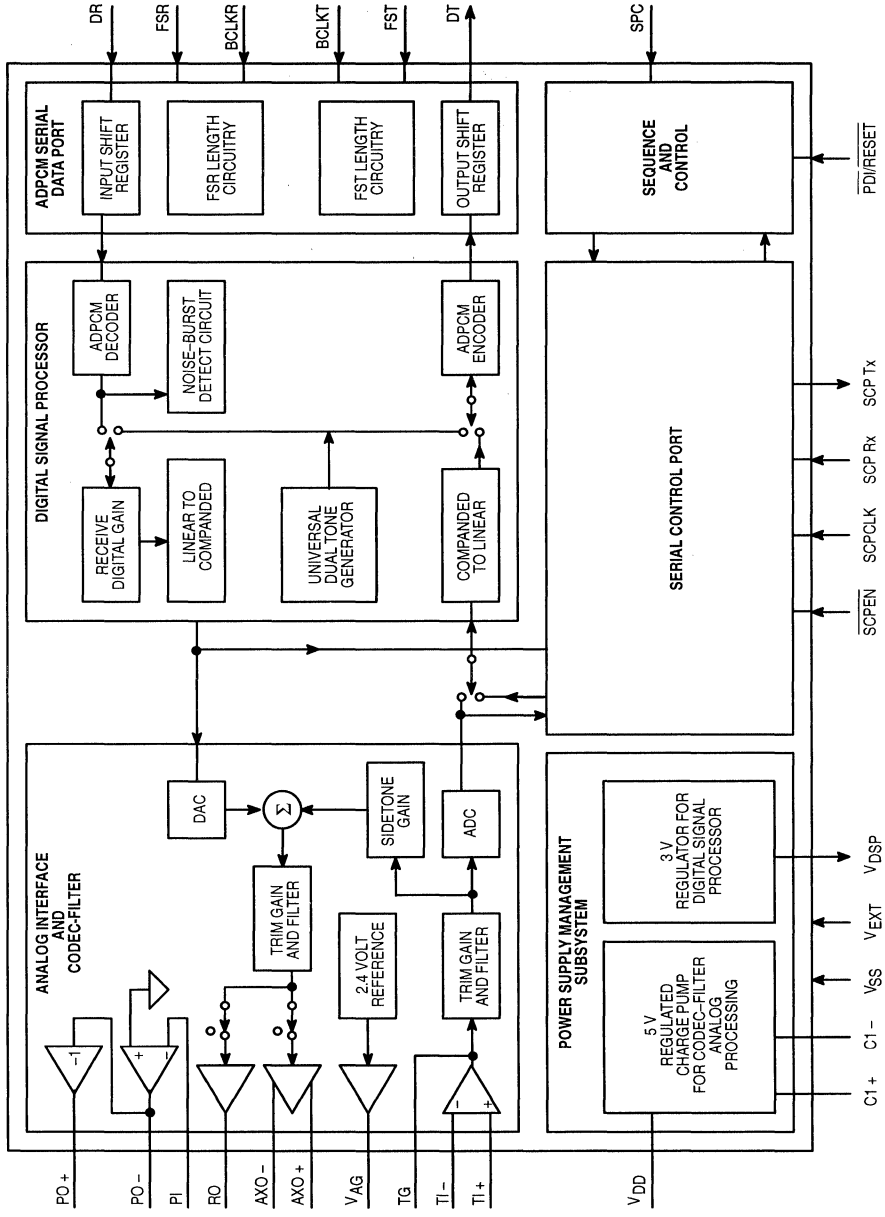


Figure 2. MC14LC5540 ADPCM Codec Block Diagram

MC145572EVK

Technical Summary

ISDN U-Interface Transceiver Evaluation Kit

The MC145572EVK U–Interface Transceiver Evaluation Kit provides Motorola ISDN customers a convenient and efficient vehicle for evaluation of the MC145572 ISDN U–Interface Transceiver. The approach taken to demonstrate the MC145572 U–Interface Transceiver is to provide the user with a fully functional NT1 (Network Termination Type 1) connected to an LT (Line Termination). An NT1 provides transparent 2B+D data transfer between the U– and S/T–Interfaces. In addition, it provides for network initiated maintenance procedures. The MC145572EVK does not terminate any ISDN call control messages. It also does not terminate any maintenance messages received over the S/T–Interface.

The MC145572EVK U–Interface Transceiver Evaluation Kit can be functionally separated into two "halves". The left half of the card is the NT1, while the right half of the card is the LT. Alternately it can be thought of as having both ends of the two–wire U–Interface, extending from the customer premise (NT1) to the switch line card (LT) on a single, stand–alone evaluation board.

The kit provides the ability to interactively manipulate status registers in the MC145572 U–Interface Transceiver as well as in the MC145474 S/T–Interface Transceiver with the aid of an external terminal. A unique combination of hardware and software features allows for standalone or terminal activation of the U–Interface, and as such provides an excellent platform for NT1 and LT hardware/software development. The NT1 function can be disabled by putting DIP switch S3–3 in the NT1 DIS position.

A complete data sheet for the MC145572EVK is available from the MOS Digital–Analog IC Division Service Center.

General

- Provides Standalone NT1 and LT on a Single Board
- Board Can Be Broken Apart Providing Separate NT1 and LT
- On–Board 68HC05 Microcontrollers with Resident Monitor Software
- Convenient Access to Key Signals
- NT1 and LT Software Development Platform

Hardware

- + 5 Volt Only Power Supply
- "Push–Button" Activation of U–Interface from NT1 or LT
- Standalone Operation for Bit Error Rate Testing
- Gated Data Clocks Provided for Bit Error Rate Testing
- Interfaces to ADS302 Evaluation Board
- Can Be Used as a U– or S/T–Interface Terminal Development Tool
- On–Board 5 ppm LT Frequency Reference
- EIA–232 (V.28) Serial Port(s) for Terminal Interface

Software

- Standalone or Terminal Operation
- Resident Firmware Monitor for User Control of Board
- Activation and Deactivation Menus
- Embedded Operations Channel
- Microcontroller Controlled or Automatic Activation/Deactivation
- Access to All Maintenance Channels
- MC68HC05 Assembly Language Source Code Available

REV 0
9/95

BLOCK DIAGRAM

Following is a basic functional block diagram for the MC145572EVK U–Interface Transceiver Evaluation Kit (Figure 1). Note that the dotted line represents the physical and logical separation between the NT1 and the LT sides of the evaluation board. While the board is capable of activating "standalone", the user may decide to use a single ASCII terminal to gain total control of the MC145572EVK's activities. Or, the user may choose to split the board, allowing the NT1 and LT entities to be physically located in separate areas.

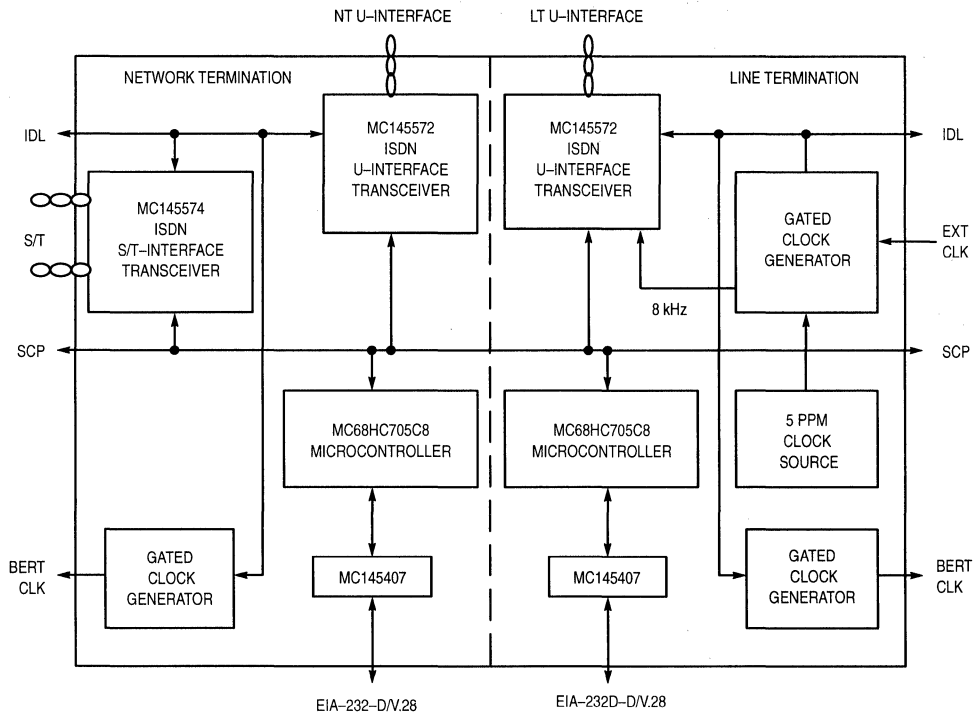


Figure 1. MC145572EVK Functional Block Diagram

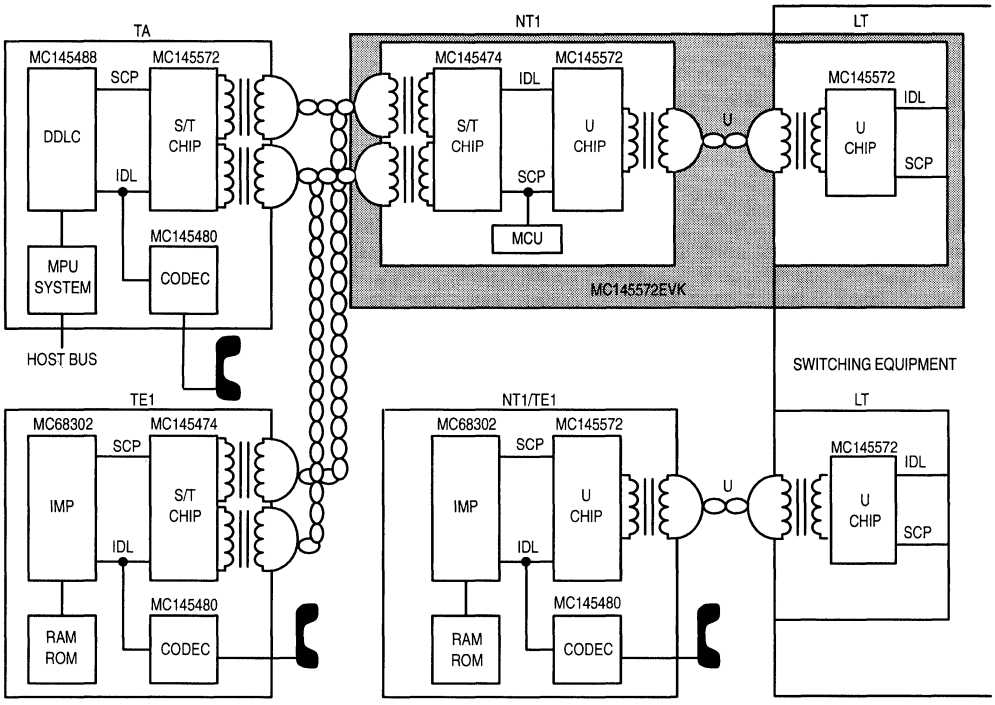


Figure 2. Motorola Silicon Applications and the MC145572EVK

MICROCONTROLLERS

The MC145572EVK is a MC68HC705C8 microcontroller–based system. Two microcontrollers reside on the board, U2 on the NT1 side, and U16 on the LT side. Hardware RESET push–buttons are located above each microcontroller. When the board is operating in the combined NT/LT mode, the NT1 and the LT are controlled via software residing in the NT1 side microcontroller EPROM. The monitor in the LT side microcontroller is used when the boards are physically separated and it becomes necessary to have one microcontroller to coordinate activities for each individual half. Both U2 and U16 must be populated for the display LEDs to operate properly.

The U–Interface may be activated using an ASCII terminal connected to the EIA–232 (V.28) port marked J3 on the NT1 side, when the board is together. When the board is separated, the EIA–232 connectors on both sides are used to monitor and control activities on their respective sides. Finally, the board may be activated as it "stands alone" with the push of a button. The default activation mode for the Activate/Deactivate push–buttons, PB1 and PB4 located near the front of the board, is as an NT1, with INFO1 continually transmitted on the S/T–Interface until it receives INFO2. When DIP switch S3–3 is in the NT1DIS position, the NT1 functionality is disabled. The LT side initiates activation on the U–Interface. Eight status LEDs are continuously updated by the MC68HC705C8s to provide the user a visual update of the U–Interface activation status.

NOTE

The LT side microcontroller (U16) must remain populated to guarantee proper operation of the LT NR1 status LEDs. The firmware version for U2 and U16 must be the same.

When the MC145572EVK is reset, it defaults to NT1 function enabled and automatic handling of M4 maintenance channel on the LT side U–transceiver. The NT1 function can also be disabled by entering the "NOF" command. The LT maintenance can be disabled by entering the "LOF" command.

STATUS LEDs

Fifteen status LEDs are provided on the MC145572EVK to offer the user a quick visual update to critical status parameters.

Two red LEDs, D12 on the NT1 side and D38 on the LT, are located near the power connectors and are illuminated when + 5 V is applied to the board. D12 indicates power is being applied to the NT1 side of the board while D38 indicates power is being applied to the LT side.

One green LED (D34) marked S/T ACT located near the S/T–Interface Transceiver, U10, illuminates to indicate that

the MC145474 when configured as an NT has achieved frame synchronization.

Located on both sides of the board are four LEDs representing Nibble Register 1 (NR1) of each U–Interface Transceiver. The LEDs in each bank are each marked with LINKUP, EI, SFS, and TP/AIP. They map directly to the register contents as shown below:

	b3	b2	b1	b0
NR1	Linkup	Error Indication	Superframe Sync	Transparent/ Activation in Progress
LED Silkscreen	LINKUP	EI	SFS	TP/AIP

NOTE

The received data is not transmitted on the IDL Interface until Linkup is a one, SFS is a one, TP/AIP is a one, and either CustEn (see NR2 in MC145572 U–Interface Transceiver data sheet) or VerifAct is a one (see BR9 in MC145572 U–Interface Transceiver data sheet).

Two red LEDs, D10 and D11 on the NT1 side, are located in the lower left corner of the printed circuit board. They indicate the status of the OUT1 and OUT2 pins of the MC145572 when it is configured for GCI operation.

Two red LEDs, D36 and D37 on the LT side, are located in the lower right corner of the printed circuit board. They indicate the status of the OUT1 and OUT2 pins of the MC145572 when it is configured for GCI operation.

COMMAND SET

A summary of the MC145572EVK software command set:

ACT: Activation/Deactivation Menu

BRL: Read/Write LT U–Interface Transceiver Byte Register

BRN: Read/Write NT U–Interface Transceiver Byte Register

BRS: Read/Write S/T–Interface Transceiver Byte Register

BRT: Read/Write S/T–Interface Transceiver Byte Register, Alternate Form

CLR: Clears febe/nebe, Re–Enters BR4 and BR5 in Both LT and NT Side U–Transceivers

DEA: Activation/Deactivation Menu, Alternate Form

DIS: Display Formatted Registers

EOC: Embedded Operations Channel Menu

HEL: Help Menu

LOF: Disable LT M4 Handler

LON: Enable LT M4 Handler

LPU: U–Interface Transceiver Analog Loopback

MM: Modify Memory

NOF: Disable NT1

NON: Enable NT1

NRL: Read/Write LT U–Interface Transceiver Nibble Register

NRN: Read/Write NT U–Interface Transceiver Nibble Register

NRS: Read/Write S/T–Interface Transceiver Nibble Register

NRT: Read/Write S/T–Interface Transceiver Nibble Register, Alternate Form

ORL: Read/Write LT U–Interface Transceiver Overlay Register

ORN: Read/Write NT U–Interface Transceiver Overlay Register

RES: Reset S/T– and/or U–Interface Transceivers

LOOPBACK OPTIONS

The activate command provides five different points on the MC145572EVK board where loopbacks are permitted when one or both U–Interface Transceivers are activated. At any given time only one loopback point can be enabled. This permits user equipment to be connected to the opposite side of the MC145572EVK. For example, if a loopback is selected on the NT1 half of the board, user equipment can be connected to the IDL Interface on the LT side of the MC145572EVK.

The LT side U–Interface Transceiver can be activated with 2B+D loopback to the U–Interface. This mode enables the received digital data from the U–Interface to be looped back to the LT side U–Interface Transceiver transmitter, and re–transmitted onto the U–Interface. The loopback point occurs in the IDL Interface block internal to the U–Interface Transceiver.

The LT side U–Interface Transceiver can also be activated without any loopbacks initially enabled. A loopback is then implemented simply by shorting JP26–21 to JP26–23.

The NT1 side U–Interface Transceiver can be activated with 2B+D loopback enabled in the S/T–Interface Transceiver IDL Interface. Received data from the NT1 side U–Interface Transceiver is transmitted on the IDL Interface to the S/T–Interface Transceiver where it is looped back to the IDL Interface and re–transmitted by the NT1 U–Interface Transceiver towards the U–Interface.

The NT1 side U–Interface Transceiver can be activated with the S/T–Interface Transceiver disabled. This causes the S/T–Interface Transceiver to three–state its IDL Interface transmitter. This provides the NT1 side U–Interface Transceivers IDL Interface direct access to the NT1 side IDL Interface. This permits the user to connect their own equipment to the NT1 side IDL Interface without any possibility of bus contention with the S/T–Interface Transceiver.

The NT1 side U–Interface Transceiver can also be activated without any loopback. This permits the NT1 side U–Interface Transceiver to communicate with the S/T–Interface Transceiver over the IDL Interface. A loopback is implemented by shorting JP7–21 to JP7–23.

Application Notes and Product Literature

4

In Brief...

Motorola's Applications Literature provides guidance to the effective use of its semiconductor families across a broad range of practical applications. Many different topics are discussed — in a way that is not possible in a device data sheet — from detailed circuit designs complete with PCB layouts, through matters to consider when embarking on a design, to complete overviews of product families and their design philosophies.

Information is presented in the form of Application Notes, Article Reprints, and detailed Engineering Bulletins.

Abstracts of all the applications documents are provided as a guide to their content; each abstract also shows the number of pages in the document, plus the origin of the article in the case of Article Reprints.

4

ORDERING INFORMATION

The application literature listed in this section has been prepared to acquaint the circuits and systems engineer with Motorola communications devices and their applications. To obtain copies of the notes, you may order them by one of the methods given below. Note that not all literature is available through the Literature Distribution Center, but that archived materials will be available via MFAX.

Motorola Literature Distribution
P.O. Box 20912
Phoenix, Arizona 85036
(800) 441–2447 or (602) 303–5454

MFAX:
RMFAX0@email.sps.mot.com
Touchtone (602) 244–6609

INTERNET: http://Design–NET.com

APPLICATION NOTE ABSTRACTS

AN806A ***Operation of the MC14469***

The MC14469 is an addressable asynchronous receiver transmitter that finds applications in control of remote devices, transfer of data to and from remote locations on a shared wire, and as an interface from remote sensors to a central processor. (7 pages)

AN872 ***MC14402 Mono–Circuit Applications Information***

This application note is intended to ease customer evaluation of the Motorola MC14402 PCM mono–circuit, particularly when using the Motorola mono–circuit evaluation board. Schematics and artwork of this board are given, as well as layout guidelines for designing the mono–circuit into a custom PC board. Analog testing considerations are mentioned to help sidestep some of the troublesome aspects of codec/filter evaluations. (5 pages)

AN893 ***Understanding Telephone Key Systems***

This application note is intended to give an understanding of key systems and how they differ. A theoretical architecture based loosely on many of the sixteen station key systems now in existence are presented. Possible variations and the impact on overall design are also discussed. (7 pages)

AN933 ***A Variety of Uses for the MC34012 and MC34017 Tone Ringers***

The MC34012 and MC34017 electronic tone ringers were developed to replace the bulky electromechanical bell assembly of a telephone, while providing the same basic function. When used in conjunction with a piezo ceramic transducer, these circuits will output a warbling sound in response to the applied ringing voltage. With some imagination, however, the circuits can be used in a variety of ways, including non–telephone applications, wherever an alerting sound or indication is required. Applications include appliance buzzers, burglar alarms, safety alerting functions, special sound effects, visual ringing indicators, and others. The circuits in this application note show how a variety of effects can be obtained. (9 pages)

AN937 ***A Telephone Ringer Which Complies with FCC and EIA Impedance Standards***

The MC34012 and MC34017 tone ringers are designed to replace the bulky bell assembly of a telephone, while providing the same function and performance under a variety of conditions. The operational requirements spelled out by the FCC and the EIA, simply stated, are that a ringer circuit MUST function when a ringing signal is provided, and MUST NOT ring when other signals (speech, dialing signals, noise) are on the line. This application note discusses how the ICs operate, the specific operational requirements to be met, and how they are met. Only "on hook" requirements are discussed since off–hook operation is not applicable. (7 pages)

AN940 ***Telephone Dialing Techniques Using the MC6805***

Telephones and associated ancillary equipment providing intelligent features are fast becoming commonplace. Often, it is necessary for the microprocessor providing the intelligence to also dial a telephone number. The MC6805 family microcomputers (MCU), with their proven hardware/software versatility, are ideal candidates for such applications. Illustrated here are two cost–effective methods of telephone dialing. Hardware and software are given for both Dual Tone Multi–Frequency (DTMF) and rotary–pulse type dialing. (18 pages)

AN943 ***UDLT Evaluation Board***

To help meet the demands for a cost effective solution to the ever–growing voice/data world within the digital telephone and PBX realm, Motorola has created the Universal Digital Loop Transceiver (UDLT) voice/data circuit family. The purpose of this application note is to render an understanding of the UDLT voice/data family and show a typical application for these CMOS parts. This is an evaluation of the application and performance of the MC145422/26 UDLT demonstration board, which was designed and built for customer evaluation. (10 pages)

AN946 ***Limited Distance Modem***

The introduction of the Universal Digital Loop Transceiver (UDLT) family of integrated circuits aids the design of a high speed Limited Distance Modem (LDM). With an external clock, the LDM will transmit asynchronous data at rates up to 80 kbps. As shown with an internal clock, the LDM can send as much as 38.4 kbps of asynchronous full–duplex data up to two kilometers on 26 AWG twisted–wire pair. The data transfer is controlled by the following RS–232C handshake signals: request to send (RTS), clear to send (CTS), data set ready (DSR), and carrier detect (CD). If the data link is operating, CTS goes active in response to RTS going active. DSR is active if the LDM is powered up. If synchronization is lost, the CD signal goes inactive. The application note includes a block diagram of the LDM, photostats of the LDM demonstration board (front and back), and a parts list for the slave and master LDM. (10 pages)

AN948 ***Data Multiplexing (Using the Universal Digital Loop Transceiver and the Data Set Interface)***

This application note describes the design of a short–haul multiplexer for asynchronous data at rates up to 9600 baud. The mux combines eight full–duplex data channels along with eight end–to–end RS–232 control signals onto a single pair of telephone wire for distances up to 2 km. Motorola's

UDLTs (MC145422/26) master/slave high–speed synchronous data transceivers and data set interface (MC145428) full–duplex asynchronous to synchronous converter form the heart of this multiplexer. A few MSI CMOS ICs complete the design. (10 pages)

AN949 ***A Voice/Data Modem Using the MC145422/26, MC145428, and MC14403***

This voice/data application allows an analog telephone system to support simultaneous voice and data across a single twisted–wire pair. To use the voice/data modem, the analog telephone line must be intercepted at the telephone system by one modem (the PBX–CPU interface). The analog signals are then converted to digital signals, combined with data, and transmitted down the remaining line as a digital loop. The second modem (the Telset–Terminal interface) terminates the digital loop, reconstructs the analog signals, and sends this information to the telephone that is plugged into the modem. The digital data is removed from the digital loop information and routed to the endpoint terminal. Any signaling information (hookswitch status and ringing) is handled by a second data channel, and it too is combined with the data and digitized voice for transmission on the digital loop. (6 pages)

AN957 ***Interfacing the Speakerphone to the MC34010/11/13 Speech Networks***

Interfacing the MC34018 speakerphone circuit to the MC34010 series of telephone circuits is described in this application note. The series includes the MC340101, MC34011, MC34013, and the newer "A" version of each of those. The interface is applicable to existing designs, as well as to new designs. (12 pages)

AN958 ***Transmit Gain Adjustments for the MC34014 Speech Network***

The MC34014 telephone speech network provides for direct connection to an electret microphone and to tip and ring. In between, the circuit provides gain, drive capability, and determination of the ac impedance for compatibility with the telephone lines. Since different microphones have different sensitivity levels, different gain levels are required from the microphone to the tip and ring lines. This application note discusses how to change the gain level to suit a particular microphone while not affecting the other circuit parameters. (2 pages)

AN959 ***A Speakerphone with Receive Idle Mode***

The MC34018 speakerphone system operates on the principle of comparing the transmit and receive signals to determine which is stronger, and then switching the circuit into that mode. (2 pages)

AN960 ***Equalization of DTMF Signals Using the MC34014***

This application note describes how to obtain equalization (line length compensation) of the DTMF dialing tones by using the MC34014 speech network. (2 pages)

AN968 ***A Digital Voice/Data Telephone Set***

This design provides standard analog telephone functions while simultaneously transmitting 9600 baud asynchronous data. It is based on Motorola's MC145422/26 UDLT family of voice/data ICs which provide 80 kbps full–duplex synchronous communication over distances up to 2 km. The circuit includes a codec/filter, data set interface, and pulse/tone dialer. (7 pages)

AN980 ***VHF Narrowband FM Receiver Design Using the MC3362 and the MC3363 Dual Conversion Receivers***

Motorola has developed a series of low–power narrowband FM dual conversion receivers in monolithic silicon integrated circuits. The MC3362 and the MC3363 are manufactured in Motorola's MOSAIC process technology. This process develops NPN transistors with f_T = 4 + GHz, which allows the MC3362 and the MC3363 to have excellent very high frequency (VHF) operation with low power drain. They are ideal for application in cordless phones, narrowband voice and data receivers, CB and amateur band radios, radio frequency (RF) security devices, and other applications through 200 MHz. (14 pages)

AN1002 ***A Handsfree Featurephone Design Using the MC34114 Speech Network and the MC34018 Speakerphone ICs***

This is a comprehensive application note which develops a full featurephone circuit using the MC34114 speech network, the MC34018 speakerphone IC, and the MC145412 dialer. Functions include 10–number memory pulse/tone dialer, tone ringer, microphone mute, and line length compensation for both handset and speakerphone operation. Options include line–powered circuit, line–powered circuit with booster for long lines, and external supply–powered. Includes glossary of telephone terms. (18 pages)

AN1003 ***A Featurephone Design, with Tone Ringer and Dialer, Using the MC34118 Speakerphone IC***

This application note describes how to add a handset, dialer, and tone ringer to the MC34118 speakerphone circuit. Although any one of several speech networks could be used as an interface between the MC34118 and the phone line, this application note covers the case where simplicity and low cost are paramount. Two circuits are developed in this discussion: line–powered and supply–powered versions. (13 pages)

AN1004 ***A Handsfree Featurephone Design Using the MC34114 Speech Network and the MC34118 Speakerphone ICs***

Complete designs for a featurephone providing 10–number memory, pulse or tone dialing, tone ringer, microphone muting, and line length compensation for both handset and speakerphone operation. Includes line–powered, line–powered plus long–line booster, and supply–powered versions. The MC34114 interfaces with tip and ring and provides 2–to–4 wire conversion. (18 pages)

AN1006 ***Linearize the Volume Control of the MC34118 Speakerphone***

This application note describes how a single resistor added to the volume control potentiometer in an MC34118 speakerphone application will almost perfectly linearize the control law. (1 page)

AN1016 ***Infrared Sensing and Data Transmission Fundamentals***

Many applications need electrical isolation, remote control, or position sensing. Infrared light provides an excellent solution due to its low cost, ease of use, availability of components, and freedom from the licensing and interference concerns of RF techniques. This application note is a brief but informative reference on the design principles for IR systems, including a selection of receiver circuits. (6 pages)

AN1077 ***Adding Digital Volume Control to Speakerphone Circuits***

This application note describes how to control speakerphone volume from UP and DOWN switches in place or the more usual potentiometer. Includes a fully annotated circuit using only three standard CMOS ICs and no critical components. (4 pages)

AN1081 ***Minimize the "Pop" in the MC34119 Low Power Audio Amplifier***

Sometimes a "pop" is heard in the loudspeaker when the MC34119 audio amplifier is re–enabled. There are several possible causes, but this application note offers a simple and low–cost remedy to satisfy the most demanding user. (3 pages)

AN1126 ***Evaluation Systems for Remote Control Devices on an Infrared Link***

The availability at low cost of remote control devices and infrared communication links provides opportunities in many application areas. This application note gives information for constructing the basic building blocks to evaluate both IR links and the most popular remote control devices. Schematics and single–side PCB layouts are presented that should enable the designer to quickly put together a basic control link and evaluate its suitability for a given application in terms of data rate, effective distance, error rate, and cost. Sources for special parts are also given. (10 pages)

AN1510 ***A Mode Indicator for the MC34118 Speakerphone Circuit***

In most applications involving a normal conversation, the operating mode (receive, transmit, idle) of the MC34118 speakerphone IC is obvious to the users of the speakerphone. There are some applications, however, where it is beneficial to have an indication of the operating mode. This indication may have to be visual, or logic levels to a microprocessor or other circuitry. This application note describes how to create a mode indicator for use with the MC34118 speakerphone circuit. (2 pages)

ARTICLE REPRINT ABSTRACTS

ARTICLE 1 ***Telephone Quality CVSD Codecs Using New Bipolar Linear/I^2L IC***

Principles of continuously variable slope delta modulation for communications systems are discussed, including an S plane model for a simple delta modulator with adjustable gain. A new bipolar I^2L circuit for implementing CVSD systems is presented. System performance and design techniques for a basic voice band codec and a telephone quality coded are included. Double integration and active companding ratio control techniques for improving codec performance is discussed. The emphasis is on a practical, mass–producible telephone codec. (6 pages)

ARTICLE 4 ***LSI for Telecommunications (A One–Chip Telephone)***

The MC34010 ETC incorporates 300 bipolar transistors and 520 I^2L gates on a 125 x 146 mil die. The chip is fabricated using a two–layer metal, Linear/I^2L process, and packaged in a 40–pin plastic package. Combining a dialer, speech network, and tone ringer on a single chip represents a major step forward in the modernization and cost reduction of analog telephones. (*Telecommunications Magazine,* April 1984) (4 pages)

ARTICLE 5 ***IC Trio Simplifies Speech Synthesis***

Despite the emergence of special–purpose speech chips, the details of adding voice output to a system are still foreign to most designers. This article shows that highly intelligible speech is possible using a low–cost microprocessor and three readily available integrated circuits. (*Electronic Design,* Vol. 30, No. 11, 1982) (4 pages)

ARTICLE 6 ***Turn I/O Data Port Into Speech Port***

The low–cost, low–power μP peripheral circuit converts an 8–bit I/O data port into a high–quality speech port, using continuously variable slope delta (CVSD) modulation to encode and decode waveforms per μP direction. (*EDN,* May 26, 1982) (1 page)

AR239 ***Implementing Integrated Office Communications***

Motorola's wide variety of integrated circuits offer flexibility to the design engineer. If low–cost voice/data communication is the top priority, the UDLT/DSI system provides a lot of functionality for a minimal cost. If higher data rates are needed, the ISDN UDLT is a solution to consider. And of course, Motorola plans to introduce an S/T transceiver chip and a LAP–D controller chip to provide the extensive features ISDN has to offer. (5 pages)

ENGINEERING BULLETIN ABSTRACTS

EB111 ***The Application of a Duplexer***

The purpose of this document is to explain the application and operation of a duplexer circuit, to show how to balance a duplexer, and to discuss the duplexer's operation analysis when used with two different transformers and with variable components. (2 pages)

EB112 ***The Application of a Telephone Tone Ringer as a Ring Detector***

Telephone ringers are driven by high–voltage, low–frequency ac signals which are superimposed on the 48 V tip–ring feed voltage. An electronic ring detector must sense the presence of an ac signal on the line and produce a dielectrically isolated logic level to the system processor. (2 pages)

PRODUCT LITERATURE

The following data books and selection guides also provide helpful information on other related Motorola communications devices.

DL110/D	Volume 1 and 2, RF Device Data
DL111/D	Bipolar Power Transistor Data
DL118/D	Optoelectronics Device Data
DL122/D	MECL Device Data
DL126/D	Small–Signal Transistors/FETs/Diodes
DL128/D	Volume 1 and 2, Linear and Interface ICs Data
DL150/D	TVS/Zener Device Data
SG73/D	Master Selection Guide
SG96/D	Linear and Interface ICs Selector Guide
SG127/D	Surface Mount Products Selector Guide
SG169/D	MOS Digital–Analog IC Quarterly Update

AN535
Application Note

Phase-Locked Loop Design Fundamentals

Prepared by
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The fundamental design concepts for phase-locked loops implemented with integrated circuits are outlined. The necessary equations required to evaluate the basic loop performance are given in conjunction with a brief design example.

Phase-Locked Loop Design Fundamentals

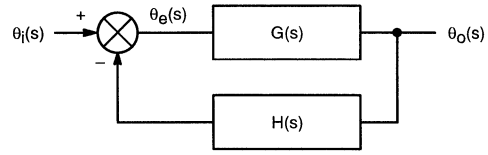
Introduction

The purpose of this application note is to provide the electronic system designer with the necessary tools to design and evaluate Phase-Locked Loops (PLL) configured with integrated circuits. The majority of all PLL design problems can be approached using the Laplace Transform technique. Therefore, a brief review of Laplace is included to establish a common reference with the reader. Since the scope of this article is practical in nature all theoretical derivations have been omitted, hoping to simplify and clarify the content. A bibliography is included for those who desire to pursue the theoretical aspect.

Parameter Definition

The Laplace Transform permits the representation of the time response f(t) of a system in the complex domain F(s). This response is twofold in nature in that it contains both transient and steady state solutions. Thus, all operating conditions are considered and evaluated. The Laplace transform is valid only for positive real time linear parameters; thus, its use must be justified for the PLL which includes both linear and nonlinear functions. This justification is presented in Chapter Three of Phase Lock Techniques by Gardner.[1]

The parameters in Figure 1 are defined and will be used throughout the text.



$\theta_i(s)$ Phase Input
$\theta_e(s)$ Phase Error
$\theta_o(s)$ Output Phase
G(s) Product of the Individual Feed Forward Transfer Functions
H(s) Product of the Individual Feedback Transfer Functions

Figure 1. Feedback System

Using servo theory, the following relationships can be obtained.[2]

$$\theta_e(s) = \frac{1}{1 + G(s)\ H(s)}\ \theta_i(s) \qquad (1)$$

$$\theta_o(s) = \frac{G(s)}{1 + G(s)\ H(s)}\ \theta_i(s) \qquad (2)$$

These parameters relate to the functions of a PLL as shown in Figure 2.

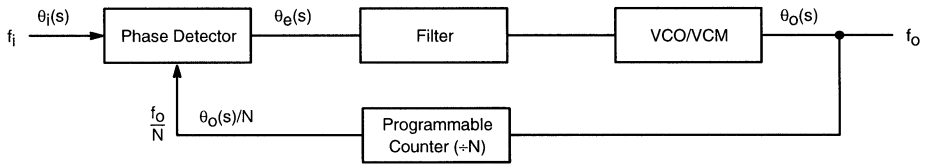


Figure 2. Phase Locked Loop

The phase detector produces a voltage proportional to the phase difference between the signals θ_i and θ_o/N. This voltage upon filtering is used as the control signal for the VCO/VCM (VCM – Voltage Controlled Multivibrator).

Since the VCO/VCM produces a frequency proportional to its input voltage, any time variant signal appearing on the control signal will frequency modulate the VCO/VCM. The output frequency is

$$f_o = N\, fi \qquad (3)$$

during phase lock. The phase detector, filter, and VCO/VCM compose the feed forward path with the feedback path containing the programmable divider. Removal of the programmable counter produces unity gain in the feedback path (N = 1). As a result, the output frequency is then equal to that of the input.

Various types and orders of loops can be constructed depending upon the configuration of the overall loop transfer function. Identification and examples of these loops are contained in the following two sections.

Type — Order

These two terms are used somewhat indiscriminately in published literature, and to date there has not been an established standard. However, the most common usage will be identified and used in this article.

The **type** of a system refers to the number of poles of the loop transfer function G(s) H(s) located at the origin. Example:

$$\text{let} \qquad G(s)\ H(s) = \frac{10}{s(s+10)} \qquad (4)$$

This is a *type one* system since there is only one pole at the origin.

The **order** of a system refers to the highest degree of the polynomial expression

$$1 + G(s)\ H(s) = 0 \triangleq \text{C.E.} \qquad (5)$$

which is termed the **Characteristic Equation** (C.E.). The roots of the characteristic equation become the closed loop poles of the overall transfer function.

Example:

$$G(s)\ H(s) = \frac{10}{s(s+10)} \qquad (6)$$

then

$$1 + G(s)\ H(s) = 1 + \frac{10}{s(s+10)} = 0 \qquad (7)$$

therefore

$$\text{C.E.} = s(s+10) + 10 \qquad (8)$$

$$\text{C.E.} = s^2 + 10s + 10 \qquad (9)$$

which is a *second order* polynomial. Thus, for the given G(s) H(s), we obtain a type 1 second order system.

Error Constants

Various inputs can be applied to a system. Typically, these include step position, velocity, and acceleration. The response of type 1, 2, and 3 systems will be examined with the various inputs.

$\theta_e(s)$ represents the phase error that exists in the phase detector between the incoming reference signal $\theta_i(s)$ and the feedback $\theta_o(s)/N$. In evaluating a system, $\theta_e(s)$ must be examined in order to determine if the steady state and transient characteristics are optimum and/or satisfactory. The transient response is a function of loop stability and is covered in the next section. The steady state evaluation can be simplified with the use of the final value theorem associated with Laplace. This theorem permits finding the steady state system error $\theta_e(s)$ resulting from the input $\theta_i(s)$ without transforming back to the time domain.[3]

Simply stated

$$\lim_{t\ \infty} [\theta(t)] = \lim_{s\ o} [s\theta_e(s)] \qquad (10)$$

Where

$$\theta_e(s) = \frac{1}{1 + G(s)\ H(s)}\ \theta_i(s) \qquad (11)$$

The input signal $\theta_i(s)$ is characterized as follows:

$$\text{Step position: } \theta_i(t) = C_p \quad t \geq 0 \qquad (12)$$

$$\text{Or, in Laplace notation: } \theta_i(s) = \frac{C_p}{s} \qquad (13)$$

where C_p is the magnitude of the phase step in radians. This corresponds to shifting the phase of the incoming reference signal by C_p radians:

$$\text{Step velocity: } \theta_i(t) = C_v t \quad t \geq 0 \qquad (14)$$

$$\text{Or, in Laplace notation: } \theta_i(s) = \frac{C_v}{s^2} \qquad (15)$$

where C_v is the magnitude of the rate of change of phase in radians per second. This corresponds to inputting a frequency that is different than the feedback portion of the VCO frequency. Thus, C_v is the frequency difference in radians per second seen at the phase detector.

$$\text{Step acceleration: } \theta_i(t) = C_a t^2 \quad t \geq 0 \qquad (16)$$

$$\text{Or, in Laplace notation: } \theta_i(s) = \frac{2\ C_a}{s^3} \qquad (17)$$

C_a is the magnitude of the frequency rate of change in radians per second per second. This is characterized by a time variant frequency input.

Typical loop G(s) H(s) transfer functions for types 1, 2, and 3 are:

$$\text{Type 1} \qquad G(s)\ H(s) = \frac{K}{s(s+a)} \qquad (18)$$

4

Type 2 $$G(s)\ H(s) = \frac{K(s + a)}{s^2} \quad (19)$$

Type 3 $$G(s)\ H(s) = \frac{K(s + a)(s + b)}{s^3} \quad (20)$$

The final value of the phase error for a type 1 system with a step phase input is found by using Equations 11 and 13.

$$\theta_e(s) = \left(\frac{1}{1 + \frac{K}{s(s+a)}}\right)\left(\frac{C_p}{s}\right)$$

$$= \frac{(s + a)C_p}{(s^2 + as + K)} \quad (21)$$

$$\theta_e(t = \infty) = \lim_{s \to o}\left[s\left(\frac{s + a}{s^2 + as + K}\right) C_p\right] = 0 \quad (22)$$

Thus, the final value of the phase error is zero when a step position (phase) is applied.

Similarly, applying the three inputs into type 1, 2, and 3 systems and utilizing the final value theorem, the following table can be constructed showing the respective steady state phase errors.

Table 1. Steady State Phase Errors for Various System Types

	Type 1	Type 2	Type 3
Step Position	Zero	Zero	Zero
Step Velocity	Constant	Zero	Zero
Step Acceleration	Continually Increasing	Constant	Zero

A zero phase error identifies phase coherence between the two input signals at the phase detector.

A constant phase error identifies a phase differential between the two input signals at the phase detector. The magnitude of this differential phase error is proportional to the loop gain and the magnitude of the input step.

A continually increasing phase error identifies a time rate change of phase. This is an unlocked condition for the phase loop.

Using Table 1, the system type can be determined for specific inputs. For instance, if it is desired for a PLL to track a reference frequency (step velocity) with zero phase error, a minimum of type 2 is required.

Stability

The root locus technique of determining the position of system poles and zeroes in the s-plane is often used to graphically visualize the system stability. The graph or plot illustrates how the closed loop poles (roots of the characteristic equation) vary with loop gain. For stability, all poles must lie in the left half of the s-plane. The relationship of the system poles and zeroes then determine the degree of stability. The root locus contour can be determined by using the following guidelines.[2]

Rule 1 – The root locus begins at the poles of G(s) H(s) (K = 0) and ends at the zeroes of G(s) H(s) (K = ∞), where K is loop gain.

Rule 2 – The number of root loci branches is equal to the number of poles or number of zeroes, whichever is greater. The number of zeroes at infinity is the difference between the number of finite poles and finite zeroes of G(s) H(s).

Rule 3 – The root locus contour is bounded by asymptotes whose angular position is given by:

$$\frac{(2n + 1)}{\#P - \#Z}\pi;\ n = 0, 1, 2, \ldots \quad (23)$$

Where #P (#Z) is the number of poles (zeroes).

Rule 4 – The intersection of the asymptotes is positioned at the center of gravity C.G.:

$$C.G. = \frac{\Sigma P - \Sigma Z}{\#P - \#Z} \quad (24)$$

Where ΣP (ΣZ) denotes the summation of the poles (zeroes).

Rule 5 – On a given section of the real axis, root loci may be found in the section only if the #P + #Z to the right is odd.

Rule 6 – Breakaway points from negative real axis is given by:

$$\frac{dK}{ds} = 0 \quad (25)$$

Again, where K is the loop gain variable factored from the characteristic equation.

Example:

The root locus for a typical loop transfer function is found as follows:

$$G(s)\ H(s) = \frac{K}{s(s + 4)} \quad (26)$$

The root locus has two branches (Rule 2) which begin at s = 0 and s = –4 and ends at the two zeroes located at infinity (Rule 1). The asymptotes can be found according to Rule 3. Since there are two poles and no zeroes, the equation becomes:

$$\frac{2n + 1}{2}\pi = \begin{cases} \frac{\pi}{2} \text{ for } n = 0 \\ \frac{3\pi}{2} \text{ for } n = 1 \end{cases} \quad (27)$$

The position of the intersection according to the Rule 4 is:

$$s = \frac{\Sigma P - \Sigma Z}{\#P - \#Z} = \frac{(-4 - 0) - (0)}{2 - 0}$$

$$s = -2 \qquad (28)$$

The breakaway point, as defined by Rule 6, can be found by first writing the characteristic equation.

$$C.E. = 1 + G(s)\,H(s) = 0$$

$$= 1 + \frac{K}{s(s+4)} = s^2 + 4s + K = 0 \qquad (29)$$

Now solving for K yields

$$K = -s^2 - 4s \qquad (30)$$

Taking the derivative with respect to s and setting it equal to zero, then determines the breakaway point.

$$\frac{dK}{ds} = \frac{d}{ds}(-s^2 - 4s) \qquad (31)$$

$$\frac{dK}{ds} = -2s - 4 = 0 \qquad (32)$$

or

$$s = -2 \qquad (33)$$

is the point of departure. Using this information, the root locus can be plotted as in Figure 3.

The second order characteristic equation, given by Equation 29, has be normalized to a standard form[2]

$$s^2 + 2\zeta\omega_n s + \omega^2_n \qquad (34)$$

where the damping ratio $\xi = \cos\phi$ ($0° \le \phi \le 90°$) and ω_n is the natural frequency as shown in Figure 3.

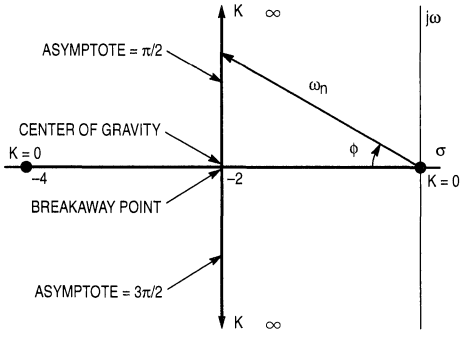


Figure 3. Type 1 Second Order Root Locus Contour

The response of this type 1, second order system to a step input, is shown in Figure 4. These curves represent the phase response to a step position (phase) input for various damping ratios. The output frequency response as a function of time to a step velocity (frequency) input is also characterized by the same set of figures.

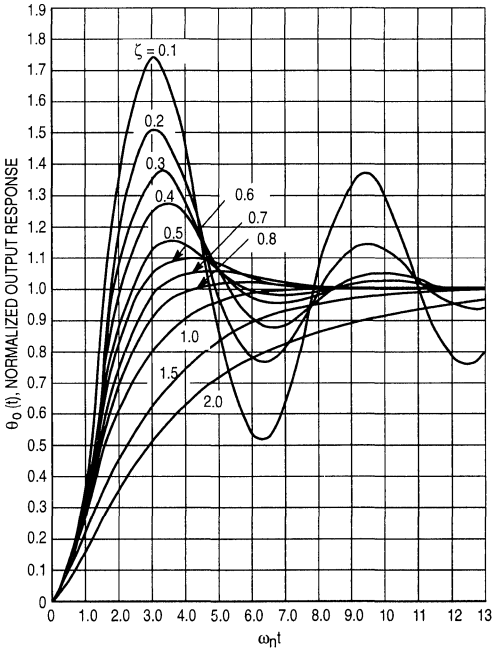


Figure 4. Type 1 Second Order Step Response

The overshoot and stability as a function of the damping ratio ξ is illustrated by the various plots. Each response is plotted as a function of the normalized time $\omega_n t$. For a given ξ and a lock-up time t, the ω_n required to achieve the desired results can be determined. Example:

Assume $\xi = 0.5$
error < 10%
for t > 1ms

From $\xi = 0.5$ curve error is less than 10% of final value for all time greater than $\omega_n t = 4.5$. The required ω_n can then be found by:

$$\omega_n t = 4.5 \qquad (35)$$

or

$$\omega_n = \frac{4.5}{t} = \frac{4.5}{0.001} = 4.5\text{krad/s} \qquad (36)$$

4

ξ is typically selected between 0.5 and 1 to yield optimum overshoot and noise performance.

Example:

Another common loop transfer function takes the form:

$$G(s)\ H(s) = \frac{(s + a)k}{s^2} \qquad (37)$$

This is a type 2 second order system. A zero is added to provide stability. (Without the zero, the poles would move along the jω axis as a function of gain and the system would at all times be oscillatory in nature.) The root locus shown in Figure 5 has two branches beginning at the origin with one asymptote located at 180 degrees. The center of gravity is s = a; however, with only one asymptote, there is no intersection at this point. The root locus lies on a circle centered at s = –a and continues on all portions of the negative real axis to left of the zero. The breakaway point is s = –2a.

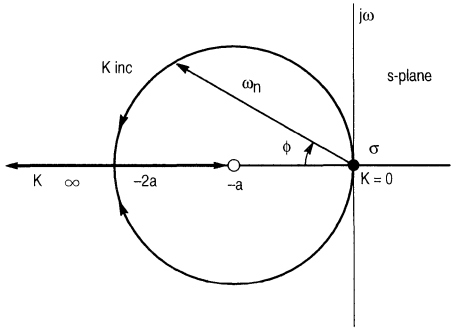


Figure 5. Type 2 Second Order Root Locus Contour

The respective phase or output frequency response of this type 2 second order system to a step position (phase) or velocity (frequency) input is shown in Figure 6. As illustrated in the previous example, the required ω_n can be determined by the use of the graph when ξ and the lock-up time are given.

Bandwidth

The –3dB bandwidth of the PLL is given by:

$$\omega - 3dB = \omega_n\left(1 - 2\zeta^2 + \sqrt{2 - 4\zeta^2 + 4\zeta^4}\right)^{1/2} \qquad (38)$$

for a type 1 second order[4] system, and by:

$$\omega_{-3dB} = \omega_n\left(1 + 2\zeta^2 + \sqrt{2 + 4\zeta^2 + 4\zeta^4}\right)^{1/2} \qquad (39)$$

for a type 2 second order[1] system.

Phase-Locked Loop Design Example

The design of a PLL typically involves determining the type of loop required, selecting the proper bandwidth, and establishing the desired stability. A fundamental approach to these design constraints is now illustrated. It is desired for the system to have the following specifications:

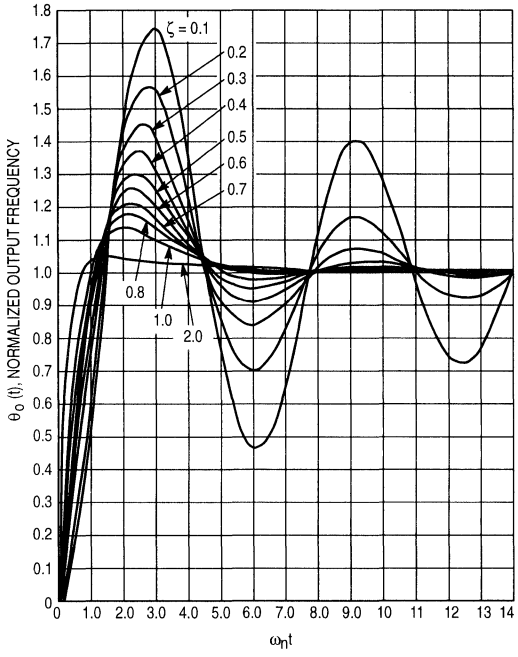


Figure 6. Type 2 Second Order Step Response

Output Frequency	2.0MHz to 3.0MHz
Frequency Steps	100KHz
Phase Coherent Frequency Output	—
Lock-Up Time Between Channels	1ms
Overshoot	<20%

NOTE: These specifications characterize a system function similar to a variable time base generator or a frequency synthesizer

From the given specifications, the circuit parameters shown in Figure 7 can now be determined.

The devices used to configure the PLL are:

Frequency-Phase Detector	MC4044/4344
Voltage Controlled Multivibrator (VCM)	MC4024/4324
Programmable Counter	MC4016/4316

The forward and feedback transfer functions are given by:

$$G(s) = K_p K_f K_o \qquad H(s) = K_n \qquad (40)$$

where $K_n = 1/N$ (41)

The programmable counter divide ratio K_n can be found from Equation 3.

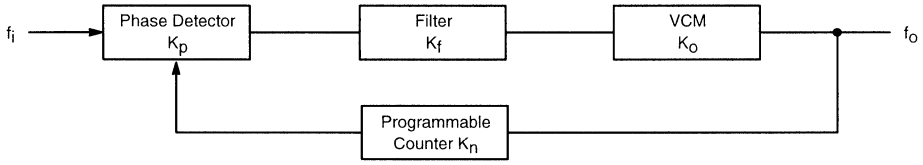


Figure 7. Phase-Locked Loop Circuit Parameters

$$N_{min} = \frac{f_{o\,min}}{f_i} = \frac{f_{o\,min}}{f_{step}} = \frac{2MHz}{100KHz} = 20 \qquad (42)$$

$$N_{max} = \frac{f_{o\,max}}{f_{step}} = \frac{3MHz}{100KHz} = 30 \qquad (43)$$

$$K_n = \frac{1}{20} \text{ to } \frac{1}{30} \qquad (44)$$

A type 2 system is required to produce a phase coherent output relative to the input (See Table 1). The root locus contour is shown in Figure 5 and the system step response is illustrated by Figure 6.

The operating range of the MC4024/4324 VCM must cover 2MHz to 3MHz. Selecting the VCM control capacitor according to the rules contained on the data sheet yields C = 100pF. The desired operating range is then centered within the total range of the device. The input voltage versus output frequency is shown in Figure 8.

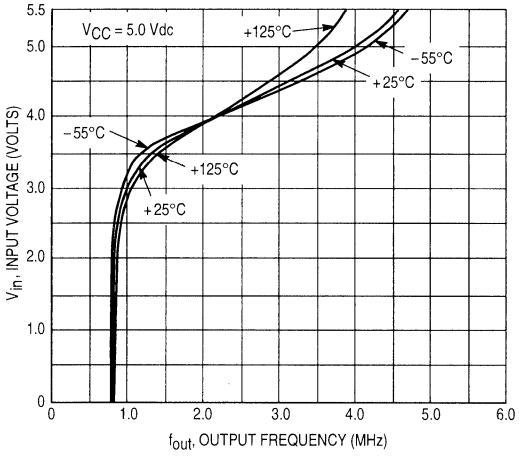


Figure 8. MC4324 Input Voltage versus Output Frequency (100pF Feedback Capacitor)

The transfer function of the VCM is given by:

$$K_o = \frac{K_v}{s} \qquad (45)$$

Where K_v is the sensitivity in radians per second per volt. From the curve in Figure 8, K_v is found by taking the reciprocal of the slope.

$$K_v = \frac{4MHz - 1.5MHz}{5V - 3.6V} 2\pi \text{ rad/s/V}$$

$$K_v = 11.2 \times 10^6 \text{ rad/s/V} \qquad (46)$$

Thus

$$K_o = \frac{11.2 \times 10^6}{s} \text{ rad/s/V} \qquad (47)$$

The s in the denominator converts the frequency characteristics of the VCM to phase, i.e., phase is the integral of frequency.

The gain constant for the MC4044/4344 phase detector is found by[5]

$$K_p = \frac{DFHigh - UFLow}{2(2\pi)} = \frac{2.3V - 0.9V}{4\pi} = 0.111V/rad \qquad (48)$$

Since a type 2 system is required (phase coherent output) the loop transfer function must take the form of Equation 19. The parameters thus far determined include K_p, K_o, K_n leaving only K_f as the variable for design. Writing the loop transfer function and relating it to Equation 19

$$G(s)H(s) = \frac{K_p K_v K_n K_f}{s} = \frac{K(s + a)}{s^2} \qquad (49)$$

Thus, K_f must take the form

$$K_f = \frac{s + a}{s} \qquad (50)$$

in order to provide all of the necessary poles and zeroes for the required G(s) H(s). The circuit shown in Figure 9 yields the desired results.

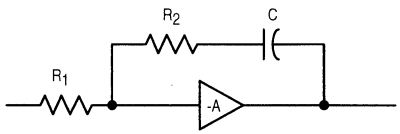


Figure 9. Active Filter Design

K_f is expressed by

$$K_f = \frac{R_2Cs + 1}{R_1Cs} \text{ for large } A \qquad (51)$$

where A is voltage gain of the amplifier.

R_1, R_2, and C are then the variables used to establish the overall loop characteristics.

The MC4044/4344 provides the active circuitry required to configure the filter K_f. An additional low current high β buffering device or FET can be used to boost the input impedance, thus minimizing the leakage current from the capacitor C between sample updates. As a result, longer sample periods are achievable.

Since the gain of the active filter circuitry in the MC4044/4344 is not infinite, a gain correction factor K_c must be applied to K_f in order to properly characterize the function. K_c is found experimentally to be $K_c = 0.5$.

$$K_{fc} = K_f K_c = 0.5\left(\frac{R_2Cs + 1}{R_1Cs}\right) \qquad (52)$$

(For large gain, Equation 51 applies.)

The PLL circuit diagram is shown in Figure 11 and its Laplace representation in Figure 10.

The loop transfer function is

$$G(s)\,H(s) = K_p K_{fc} K_o K_n \qquad (53)$$

$$G(s)H(s) = K_p(0.5)\left(\frac{R_2Cs + 1}{R_1Cs}\right)\left(\frac{K_v}{s}\right)\left(\frac{1}{N}\right) \qquad (54)$$

The characteristic equation takes the form

$$C.E. = 1 + G(s)\,H(s) = 0$$

$$= s^2 + \frac{0.5\,K_p\,K_v\,R_2}{R_1N}s + \frac{0.5\,K_p\,K_v}{R_1CN} \qquad (55)$$

Relating Equation 55 to the standard form given by Equation 34

$$s^2 + \frac{0.5\,K_p\,K_v\,R_2}{R_1N}s + \frac{0.5\,K_p\,K_v}{R_1CN}$$

$$= s^2 + 2\zeta\omega_n s + \omega_n^2 \qquad (56)$$

Equating like coefficients yields

$$\frac{0.5\,K_p\,K_v}{R_1CN} = \omega_n^2 \qquad (57)$$

$$\text{and } \frac{0.5\,K_p\,K_v\,R_2}{R_1N} = 2\zeta\omega_n \qquad (58)$$

With the use of an active filter whose open loop gain (A) is large ($K_c = 1$), Equations 57 and 58 become

$$\frac{K_p\,K_v}{R_1CN} = \omega_n^2 \qquad (59)$$

$$\frac{K_p\,K_v\,R_2}{R_1N} = 2\zeta\omega_n \qquad (60)$$

The percent overshoot and settling time are now used to determine ω_n. From Figure 6, it is seen that a damping ratio $\zeta = 0.8$ will produce a peak overshoot less than 20% and will settle within 5% at $\omega_n t = 4.5$. The required lock-up time is 1ms.

$$\omega_n = \frac{4.5}{t} = \frac{4.5}{0.001} = 4.5\text{krad/s} \qquad (61)$$

Rewriting Equation 57

$$R_1C = \frac{0.5\,K_p\,K_v}{\omega_n^2 N} \qquad (62)$$

$$= \frac{(0.5)\,(0.111)\,(11.2 \times 10^6)}{(4500)^2\,(30)}$$

$$R_1C = 0.00102$$

(Maximum overshoot occurs at N_{max} which is minimum loop gain)

Let $C = 0.5\mu F$

Then $R_1 = \frac{0.00102}{0.5 \times 10^{-6}} = 2.04k\Omega$

Use $R_1 = 2k\Omega$

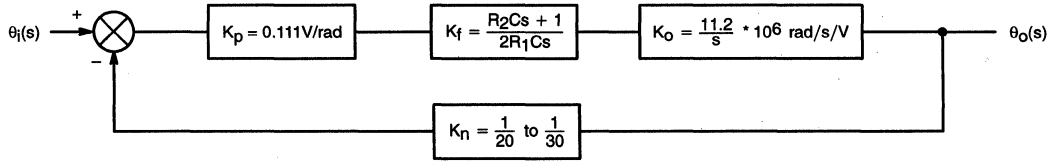


Figure 10. Laplace Representation of Diagram in Figure 11

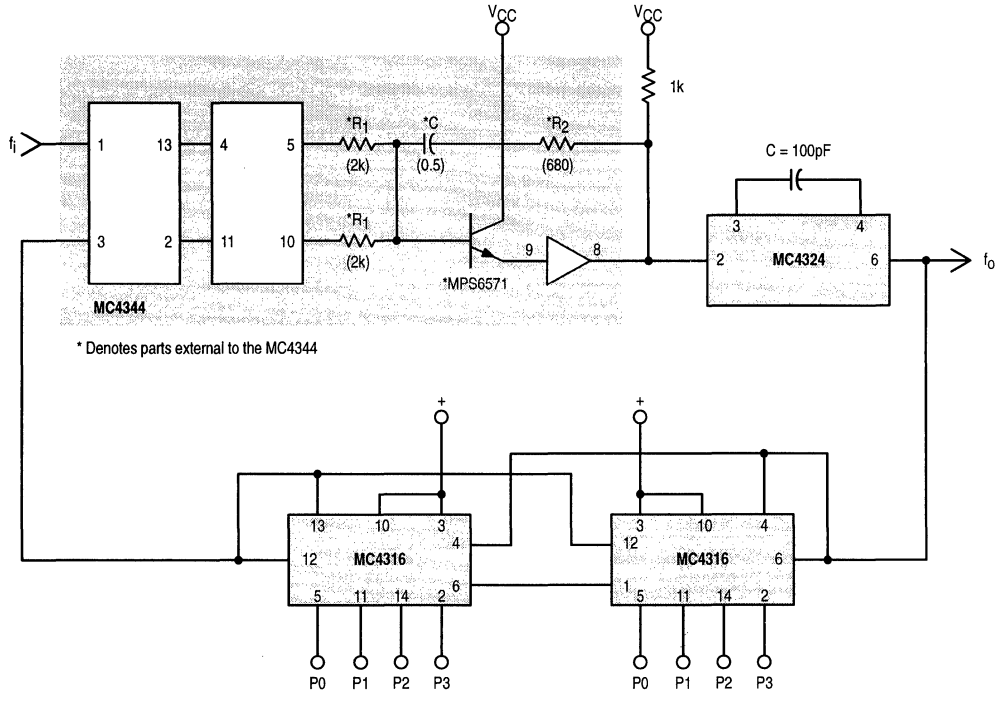


Figure 11. Circuit Diagram of Type 2 Phase-Locked Loop

R_1 is typically selected greater than 1kΩ.

Solving for R_2 in Equation 58

$$R_2 = \frac{2\zeta\ \omega_n\ R_1 N}{K_p\ K_v\ (0.5)} = \frac{2\zeta}{C\ \omega_n} \qquad (63)$$

$$= \frac{2(0.8)}{(0.5 \times 10^{-6})(4.5k)}$$

$$= 711\Omega$$

Use $R_2 = 680\Omega$

All circuit parameters have now been determined and the PLL can be properly configured.

Since the loop gain is a function of the divide ratio K_n, the closed loop poles will vary its position as K_n varies. The root locus shown in Figure 12 illustrates the closed loop pole variation.

The loop was designed for the programmable counter N = 30. The system response for N = 20 exhibits a wider bandwidth and larger damping factor, thus reducing both lock-up time and percent overshoot (see Figure 14).

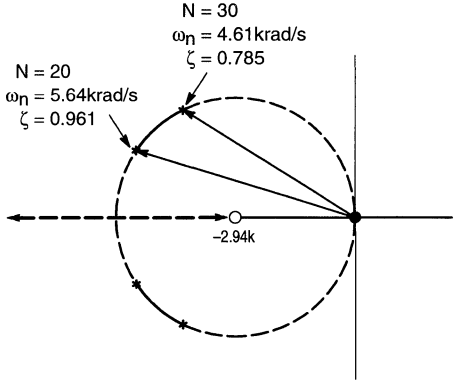


Figure 12. Root Locus Variation

NOTE: The type 2 second order loop was illustrated as a design sample because it provides excellent performance for both type 1 and 2 applications. Even in systems that do not require phase coherency, a type 2 loop still offers an optimum design.

Experimental Results

Figure 13 shows the theoretical transient frequency response of the previously designed system. The curve N = 30 illustrates the frequency response when the programmable counter is stepped from 29 to 30, thus producing a change in the output frequency from 2.9MHz to 3.0MHz. An overshoot of 18% is obtained and the output frequency is within 5kHz of the final value one millisecond after the applied step. The curve N = 20 illustrates the output frequency change as the programmable counter is stepped from 21 to 20.

Since the frequency is proportional to the VCM control voltage, the PLL frequency response can be observed with an oscilloscope by monitoring pin 2 of the VCM. The average frequency response as calculated by the Laplace method is found experimentally by smoothing this voltage at pin 2 with a simple RC filter whose time constant is long compared to the phase detector sampling rate, but short compared to the PLL response time. With the programmable counter set at 29 the quiescent control voltage at pin 2 is approximately 4.37 volts. Upon changing the counter divide ratio to 30, the control voltage increases to 4.43 volts as shown in Figure 14. A similar transient occurs when stepping the programmable counter from 21 to 20. Figure 14 illustrated that the experimental results obtained from the configured system follows the predicted results shown in Figure 13. Linearity is maintained for phase errors less than 2π, i.e. there is no cycle slippage at the phase detector.

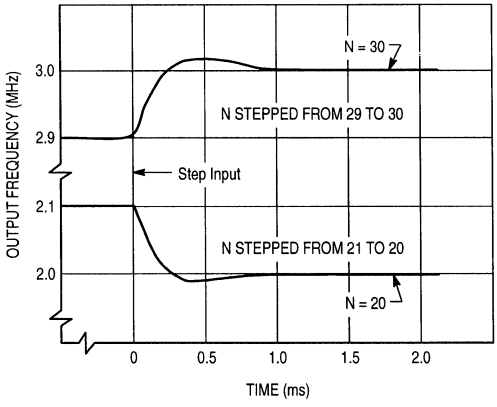


Figure 13. Frequency-Time Response

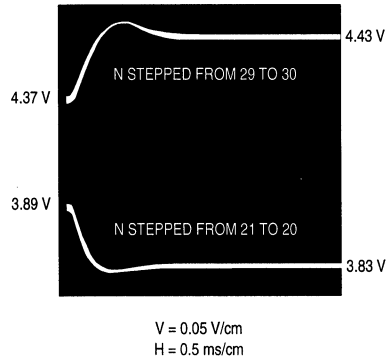


Figure 14. VCM Control Voltage (Frequency) **Transient**

Figure 15 is a theoretical plot of the VCM control voltage transient as calculated by a computer program. The computer program is written with the parameters of Equations 58 and 59 (type 2) as the input variables and is valid for all damping ratios of $\zeta \leq 1.0$. The program prints or plots control voltage transient versus time for desired settings of the programmable counter. The lock-up time can then be readily determined as the various parameters are varied. (If stepping from a higher divide ratio to a lower one, the transient will be negative.) Figures 14 and 15 also exhibit a close correlation between experimental and analytical results.

Summary

This application note describes the basic control system techniques required for phase-locked loop design. Criteria for the selection of the optimum type of loop and methods for establishing the desired performance characteristics are presented. A design example is illustrated in a step-by-step approach along with the comparison of the experimental and analytical results.

*THE PARAMETERS LISTED BELOW APPLY TO THE FOLLOWING PLOT

PHASE DETECTOR GAIN CONSTANT	P1 = 0.111 VOLTS PER RADIAN
VCM GAIN CONSTANT	V1 =1.12 E+7 RAD PER VOLT
FILTER INPUT RESISTOR	R1 = 3900 OHMS ($R1_C$ = 2k)
FILTER FEEDBACK RESISTOR	R2 = 680 OHMS
FILTER CAPACITOR	C1 = 0.5 MICROFARADS
DIVIDER VALUE	N1-N2 = 29 – 30
REFERENCE FREQUENCY	F1 = 100000 CPS
OUTPUT FREQUENCY CHANGE	F5 = 100000 CPS

P2 = 0.111	C2 = 0.5
V2 = 1.12 E+7	N3-N4 = 21 – 20
R3 = 3900 ($R1_C$ = 2k)	F2 (F6) = 100000 (100000)
R4 = 680	

PLOT OF FUNCTIONS

(NOTE: Y(T) IS '+', Z(T) IS '*', AND '0' IS COMMON)

FOR T: TOP = 0 BOTTOM = 0.0015 INCREMENT = 0.0005
FOR FCTS: LEFT = 0 RIGHT = 0.12 INCREMENT = 0.002

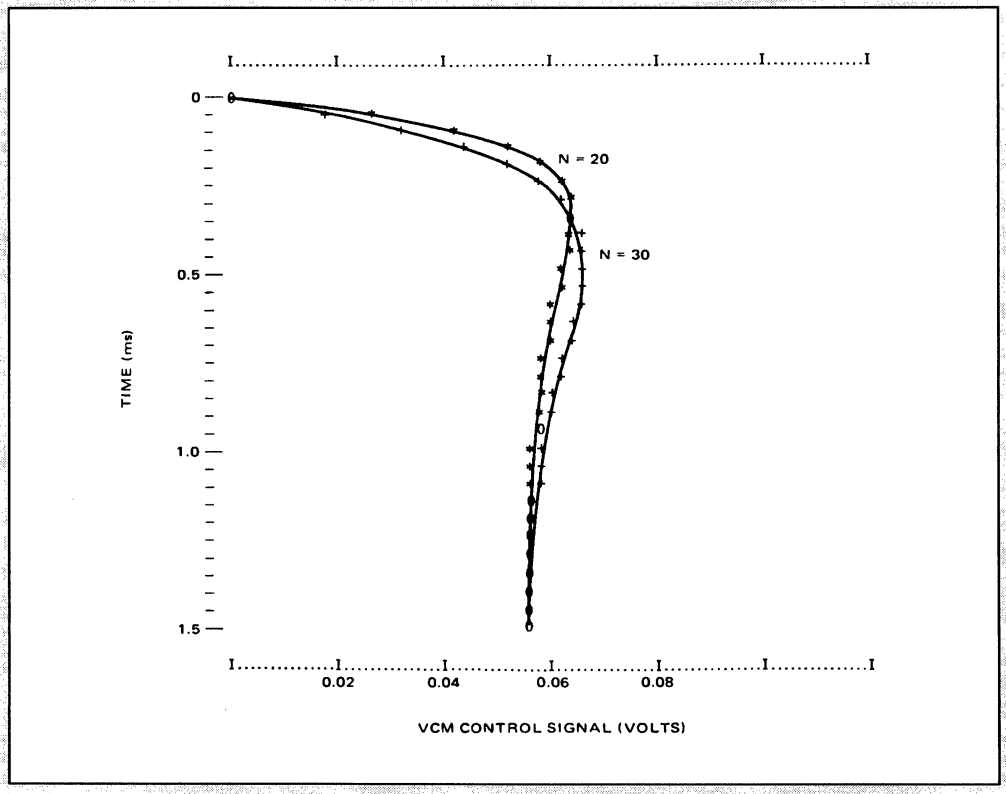


Figure 15. VCM Control Signal Transient

4

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AN827

The Technique of Direct Programming by Using a Two-Modulus Prescaler

Prepared by: PLL Applications

The theory in this application note is still applicable, but some of the products referenced may be discontinued.

INTRODUCTION

The MC12009, MC12011, or MC12013 can be used as part of a variable modulus (divisor) prescaling subsystem used in certain Digital Phase–Locked Loops (PLL).

More often than not, the feedback loop of any PLL contains a counter–divider. Many methods are available for building a divider, but not all are simple, economical, or convenient in a particular application.

The technique and system described here offer a new approach to the construction of a phase–locked loop divider. In addition to using either the MC12009, MC12011, or the MC12013 variable modulus prescaler, this system requires an MC12014 Counter Control Logic Function, together with suitable programmable counters (e.g., MC4016s or SN74LS716s). Data sheets for these additional devices should be consulted for their particular functional descriptions.

DESIGN CONSIDERATIONS

The disadvantage of using a fixed modulus (÷ P) for frequency division in high–frequency phase–locked loops (PLL) is that it requires dividing the desired reference frequency by P also (desired reference frequency equals channel spacing).

The MC12009/11/13 are especially designed for use with a technique called "variable modulus prescaling". This technique allows a simple MECL two–modulus prescaler to be controlled by a relatively slow MTTL programmer counter. The use of this technique permits direct high–frequency prescaling without any sacrifice in resolution since it is no longer necessary to divide the reference frequency by the modulus of the high–frequency prescaler.

The theory of "variable modulus prescaling" may be explained by considering the system shown in Figure 1. For the loop shown:

$$f_{out} = N \bullet P \bullet f_{ref} \quad (1)$$

where P is fixed and N is variable. For a change of 1 in N, the output frequency changes by $P \bullet f_{ref}$. If f_{ref} equals the desired channel spacing, then only every P channel may be programmed using this method. A problem remains: how to program intermediate channels.

One solution to this problem is shown in Figure 2. A ÷ P is placed in series with the desired channel spacing (frequency) to give a new reference frequency: channel spacing/P.

Another solution is found by considering the defining Equation 1 for f_{out} of Figure 1. From the equation it may be seen that only every P channel can be programmed simply, because N is always an integer. To obtain intermediate channels, P must be multiplied by an integer plus a fraction. This fraction would be of the form: A/P. If N is defined to be an integer number, N_P, plus a fraction, A/P, N may be expressed as:

$$N = N_P + A/P.$$

Substituting this expression for N in Equation 1 gives:

$$f_{out} = (N_P + A/P) \bullet P \bullet f_{ref} \quad (2)$$

or

$$f_{out} = (N_P P + A) \bullet f_{ref} \quad (3)$$

$$f_{out} = N_P \bullet P \bullet f_{ref} + A \bullet f_{ref}. \quad (4)$$

Equation 4 shows that all channels can be obtained directly if N can take on fractional values. Since it is difficult to multiply by a fractional number, Equation 4 must be synthesized by some other means.

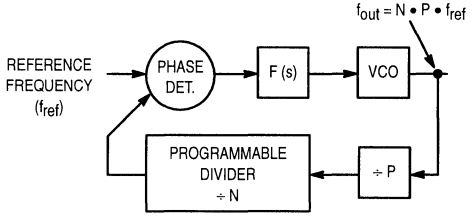

Figure 1. Frequency Synthesis by Prescaling

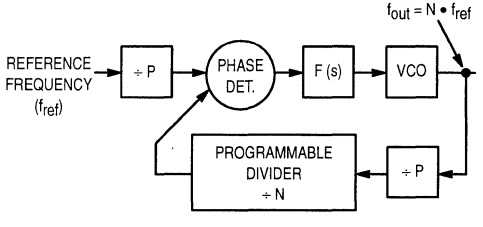

Figure 2. Frequency Synthesis by Prescaling

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Taking Equation 3 and adding ± AP to the coefficient of the f_{ref}, the equation becomes:

$$f_{out} = (N_P \bullet P + A + A \bullet P - A \bullet P) f_{ref}. \quad (5)$$

Collecting terms and factoring gives:

$$f_{out} = [(N_P - A) P + A (P + 1)] f_{ref} \quad (6)$$

From Equation 6 it becomes apparent that the fractional part of N can be synthesized by using a two–modulus counter (P and P + 1) and dividing by the upper modulus, A times, and the lower modulus (N_P – A) times.

Equation 6 suggests the circuit configuration in Figure 3. The A counter shown must be the type that counts from the programmed state (A) to the enable state, and remains in this state until divide by N_P is completed in the programmable counter.

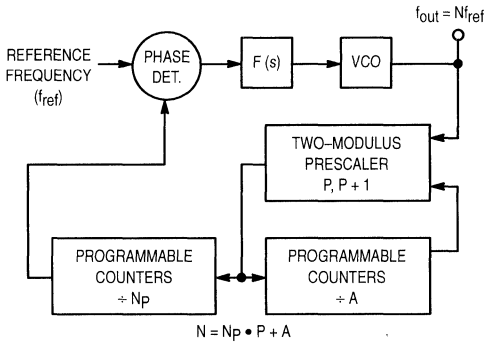

Figure 3. Frequency Synthesis by Two–Modulus Prescaling

In operation, the prescaler divides by P + 1, A times. For every P + 1 pulse into the prescaler, both the A counter and N_P counter are decremented by 1. The prescaler divides by P + 1 until the A counter reaches the zero state. At the end of (P + 1) • A pulses, the state of the N_P counter equals (N_P – A). The modulus of the prescaler then changes to P. The variable modulus counter divides by P until the remaining count, (N_P – A) in the N_P counter, is decremented to zero. Finally, when this is completed, the A and N_P counters are reset and the cycle repeats.

To further understand this prescaling technique, consider the case with P = 10. Equation 6 becomes:

$$f_{out} = (A + 10 N_P) \bullet f_{ref} \quad (7)$$

If N_P consists of 2 decades of counters then:

$$N_P = 10 N_{P1} + N_{P0}$$

(N_{P1} is the most significant digit),

and Equation 7 becomes:

$$f_{out} = (100 N_{P1} + 10 N_{P0} + A) f_{ref}.$$

To do variable modulus prescaling using the variable modulus prescalers (MC12009/11/13) and programmable divide by N counters (MC4016, MC4018) one additional part is required: the MC12014 (Counter Control Logic).

In variable modulus prescaling the MC12014 serves a dual purpose: it detects the terminal (zero) count of the A counter, to switch the modulus of the MC12013; and it extends the maximum operating frequency of the programmable counters to above 25 MHz. (See the MC12014 data sheet for a detailed description of the Counter Control Logic).

Figure 4 shows the method of interconnecting the MC12013, MC12014, and MC4016 (or MC4018) for variable modulus prescaling. To understand the operation of the circuit shown in Figure 4, consider division by 43. Division by 43 is done by programming N_{P1} = 0, N_{P0} = 4, and A = 3.

Waveforms for various points in the circuit are shown in Figure 5 for this division. From the waveforms it may be seen that the two–modulus prescaler starts in the divide by 11 mode, and the first input pulse causes point A to go high. This positive transition decrements the N_P counter to 3, and counter A to 2.

After 11 pulses, point (A) again goes high; the N_P counter decrements to 2 and the A counter to 1. The "2" contained in the N_P counter enables the inputs to the frequency extender portion of the MC12014. After 11 more pulses point (A) goes high again.

With this position transition at (A), the output (f_{out}) of the MC12014 goes low, the N_P counter goes to 1, and the A counter goes to 0. The zero state of the A counter is detected by the MC12014, causing point (B) to go to 1 and changing the modulus of the MC12013 to 10 at the start of the cycle.

When f_{out} goes low, the programmable counters are reset to the programmed number. After 11 pulses (the enable went high after the start of the cycle and therefore doesn't change the modulus until the next cycle), point (A) makes another positive transition. This positive transition causes f_{out} to return high, release the preset on the counter, and generates a pulse to clear the latch (return point (B) to 0).

After 10 pulses the cycle begins again (point (B) was high prior to point (A) going high). The number of input pulses that have occurred during this entire operation is: 11 + 11 + 11 + 10 = 43. Figures 6 and 7 show the waveforms for divide by 42 and divide by 44 respectively.

The variable modulus prescaling technique may be used in any application as long as the number in the N_P counter is greater than or equal to the number in the A counter. Failure to observe this rule will result in erroneous results. (For example, for the system shown in Figure 4, if the number 45 is programmed, the circuit actually will divide by 44. This is not a serious restriction since N_P is greater than A in most applications.)

It is important to note that the A counter has been composed of only one counter for discussion only; where required, the A counter may be made as large as needed by cascading several programmable counters. Figure 8 shows the method of interconnecting counters. Operation is previously described. The number of stages in the A Counter should not exceed the number of stages for the N_P counters. As many counters as desired may be cascaded, as long as fan–in and fan–out rules for each part are observed.

The theory of "variable modulus prescaling" developed above, examined a case in which the upper modulus of the two–modulus prescaler was 1 greater than the lower modulus. However, the technique described is by no means limited to this one special case. There are applications in which it is desirable to use moduli other than P/(P + 1).

It can be shown that for a general case in which the moduli of the two–modulus prescaler are P and P + M, Equation 6 becomes:

$$f_{out} = [(N_P - A)\,P + A\,(P + M)] \bullet f_{ref}$$

or

$$f_{out} = [N_P \bullet P + M \bullet A] \bullet f_{ref}. \quad (8)$$

From Equation 8 it may be seen that the upper modulus of the two–modulus prescaler has no effect on the N_P counter, and that the number programmed in the A counter is simply multiplied by M.

There is no one procedure which will always yield the best counter configuration for all possible applications. Each designer will develop his own special design for the counter portion of his PLL system.

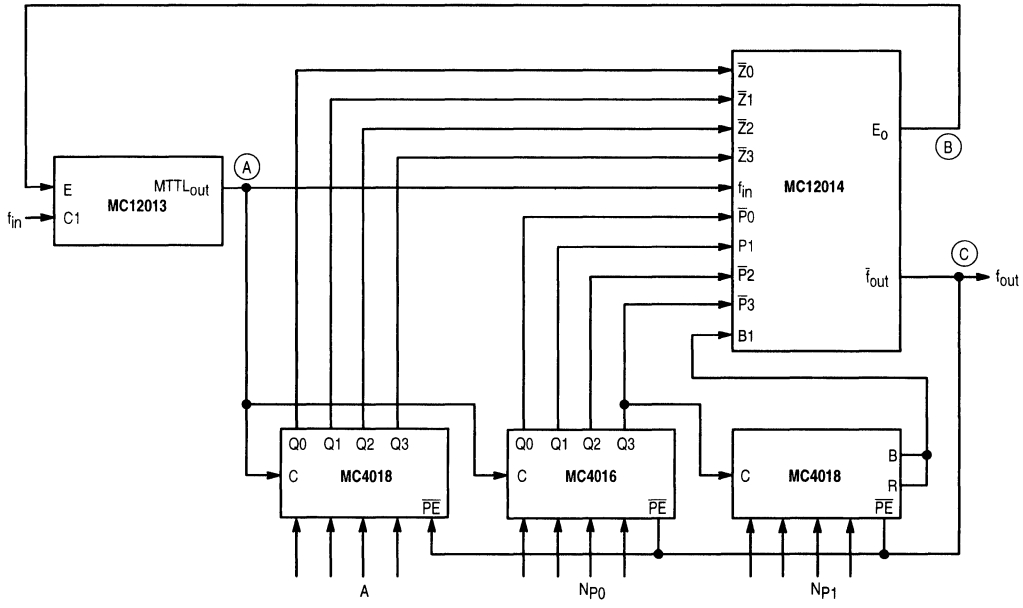

Figure 4. Direct Programming Utilizing Two–Modulus Prescaler

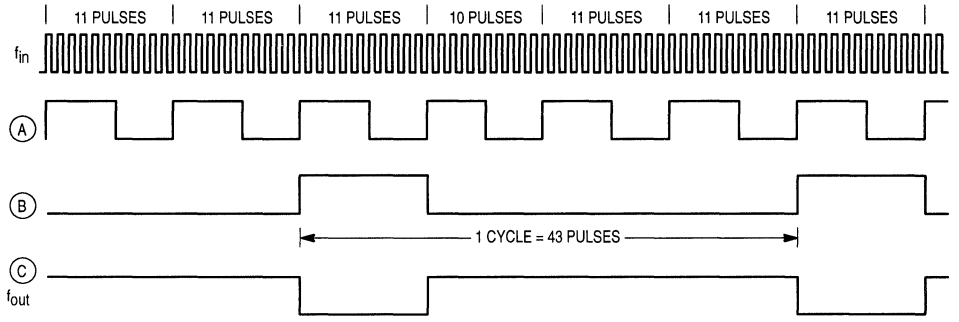

Figure 5. Waveforms for Divide by 43

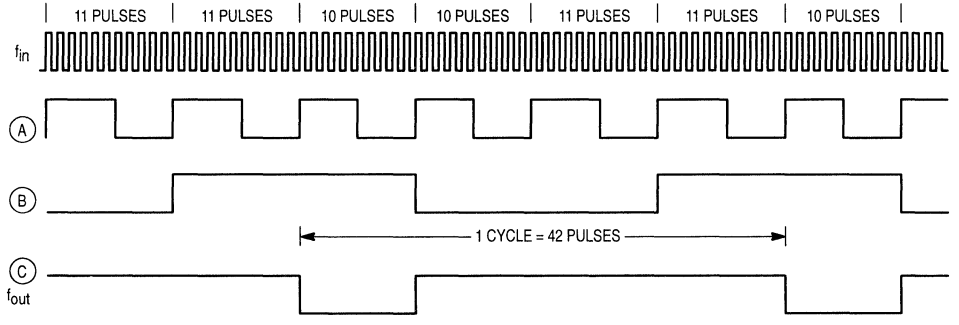

Figure 6. Waveforms for Divide by 42

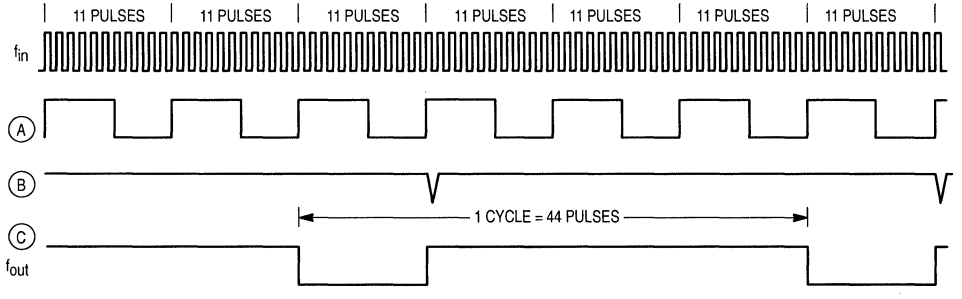

Figure 7. Waveforms for Divide by 44

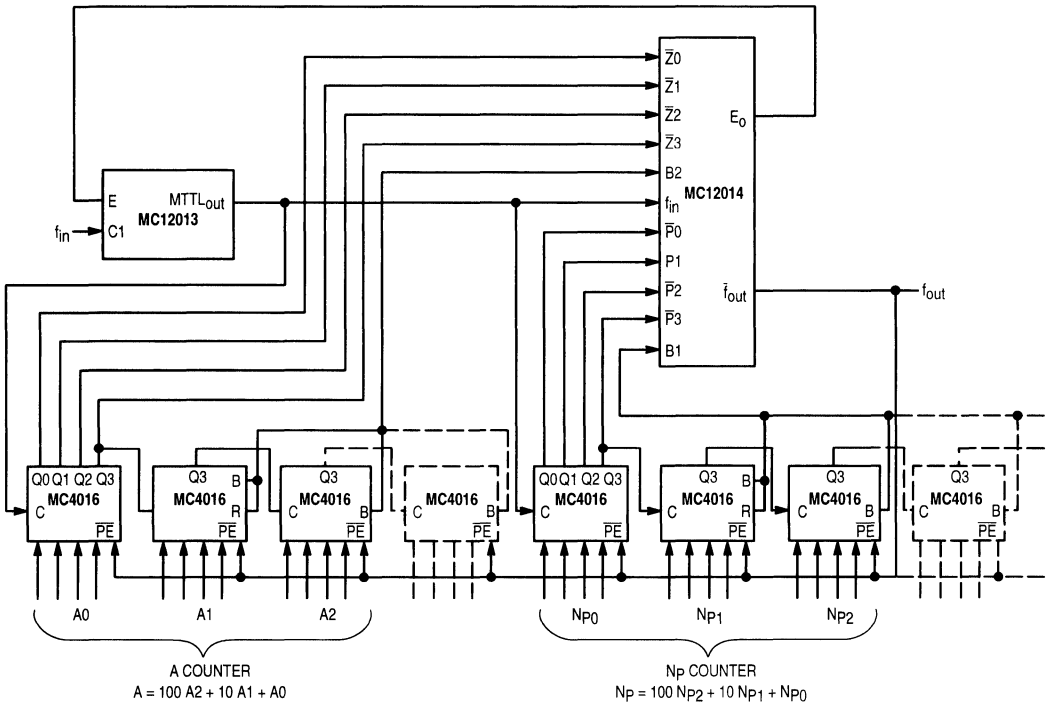

Figure 8. Method of Interconnecting Counters

AN1207

The MC145170 in Basic HF and VHF Oscillators

Prepared by: David Babin and Mark Clark

Phase–locked loop (PLL) frequency synthesizers are commonly found in communication gear today. The carrier oscillator in a transmitter and local oscillator (LO) in a receiver are where PLL frequency synthesizers are utilized. In some cellular phones, a synthesizer can also be used to generate 90 MHz for an offset loop. In addition, synthesizers can be used in computers and other digital systems to create different clocks which are synchronized to a master clock.

The MC145170 is available to address some of these applications. The frequency capability of the MC145170 is very broad — from a few hertz to 160 MHz.

ADVANTAGES

Frequency synthesizers, such as the MC145170, use digital dividers which can be placed under MCU control. Usually, all that is required to change frequencies is to change the divide ratio of the N Counter. Tuning in less than a millisecond is achievable.

The MC145170 can generate many frequencies based on the accuracy of a single reference source. For example, the reference can be a low–cost basic crystal oscillator or a temperature–compensated crystal oscillator (TCXO). Therefore, high tuning accuracies can be achieved. Boosting of the reference frequency by 100x or more is achievable.

ELEMENTS IN THE LOOP

The components used in the PLL frequency synthesizer of Figure 1 are the MC145170 PLL chip, low–pass filter, and voltage–controlled oscillator (VCO). Sometimes a voltage–controlled multivibrator (VCM) is used in place of the VCO. The output of a VCM is a square wave and is usually integrated before being fed to other sections of the radio. The VCM output can be directly used in computers and other digital equipment. The output of a VCO or VCM is typically buffered, as shown.

As shown in Figure 2, the MC145170 contains a reference oscillator, reference counter (R Counter), VCO/VCM counter (N Counter), and phase detector. A more detailed block diagram is shown in the data sheet.

HF SYNTHESIZER

The basic information required for designing a stable high–frequency PLL frequency synthesizer is the frequencies required, tuning resolution, lock time, and overshoot. For the example design of Figure 3, the frequencies needed are 9.20 MHz to 12.19 MHz. The resolution (usually the same as the frequency steps or channel spacing) is 230 kHz. The lock time is 8 ms and a maximum overshoot of approximately 15% is targeted. For purposes of this example, lock is considered to be when the frequency is within about 1% of the final value.

HF SYNTHESIZER LOW–PASS FILTER

In this design, assume a square wave output is acceptable. To generate a square wave, a MC1658 VCM chip is chosen. Per the transfer characteristic given in the data sheet, the MC1658 transfer function, K_{VCM}, is approximately 1×10^8 radians/second/volt. The loading presented by the MC1658 control input is large; the maximum input current is 350 μA. Therefore, an active low–pass filter is used so that loading does not affect the filter's response. See Figure 3. In the filter, a 2N7002 FET is chosen because it has very high transconductance (80 mmhos) and low input leakage (100 nA).

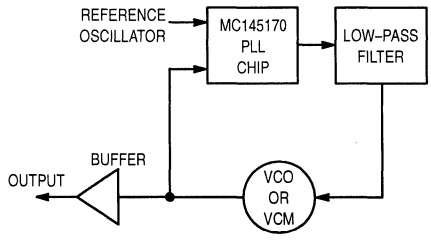

Figure 1. PLL Frequency Synthesizer

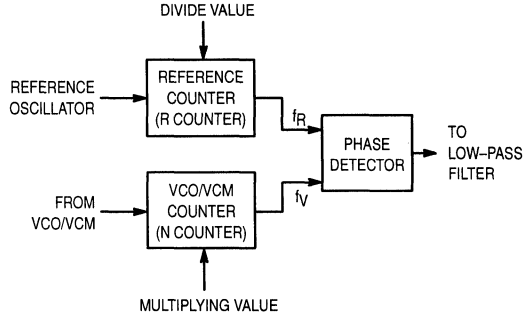

Figure 2. Detail of the MC145170

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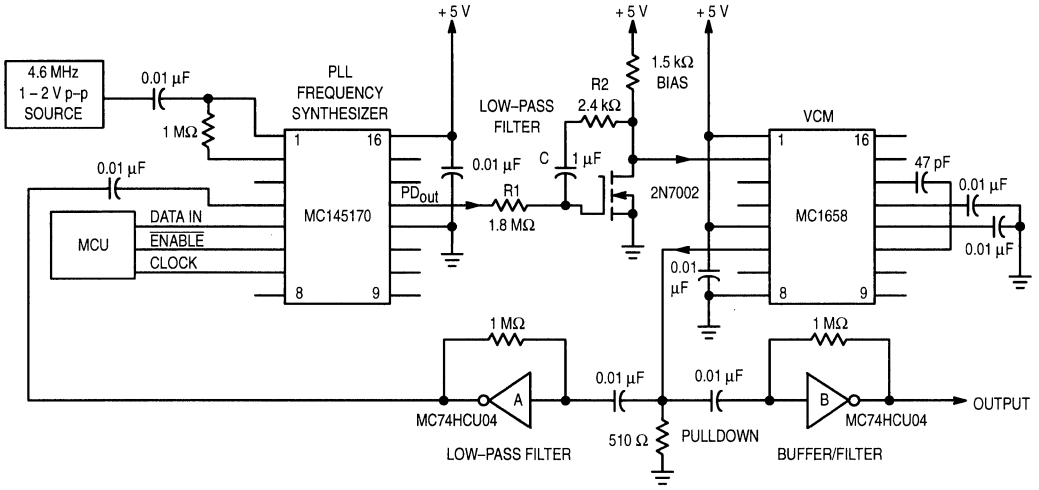

Figure 3. HF Synthesizer

In order to calculate the average divide value for the N Counter, follow this procedure. First, determine the average frequency; this is (12.19 + 9.2)/2 = 10.695 MHz or approximately 10.7 MHz. Next, divide this frequency by the resolution: 10.7 MHz/230 kHz = about 47.

Next, reference application note AN535 (see book DL136/D Rev 3 or 4). The active filter chosen takes the form shown in Figure 9 of the application note. This filter is used with the single–ended phase detector output of the MC145170, PD_{out}. The phase detector associated with PD_{out} has a gain $K_\phi = V_{DD}/4\pi$. For a supply of 5 V, this is $5/4\pi$ = 0.398 V/rad. The system's step response is shown in Figure 4. To achieve about 15% overshoot, a damping factor of 0.8 is used. This causes frequency to settle to within 1% at $\omega_n t = 5.5$.

The information up to this point is as follows.

f_{ref} = 230 kHz

f_{VCM} = 9.2 to 12.19 MHz; the average is 10.7 MHz, average N = 47

power supply = 5 V for the phase detector

$K_{VCM} = 1 \times 10^8$ rad/s/V

overshoot = approximately 15%, yields a damping factor = 0.8

lock time t = 8 ms settling to within 1%, $\omega_n t = 5.5$

$K\phi$ or K_p = 0.398 V/rad.

From the application note, equation 61, $\omega_n = 5.5/t = 5.5/0.008 = 687.5$ rad/s.

Equation 59 is $R1C = (K_p K_V)/\omega_n^2 N$

$= (0.398 \times 1 \times 10^8)/687.5^2 \times 47$

$= 1.79$

Equation 59 is used because of the high–gain FET.

Next, the capacitor C is picked to be 1 µF. Therefore, R1 = 1.79/C which is 1.79 MΩ. The standard value of 1.8 MΩ is used for R1.

Equation 63 is $R2 = (2\zeta)/C\,\omega_n$

$= (2 \times 0.8)/(1 \times 10^{-6} \times 687.5)$

$= 2.33$ kΩ.

A standard value for R2 of 2.4 kΩ is utilized.

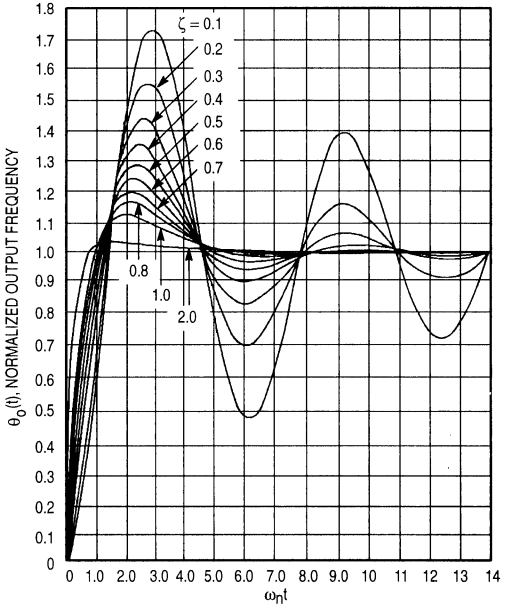

Figure 4. Type 2 Second Order Step Response

HF SYNTHESIZER PROGRAMMING

Programming the MC145170 is straightforward. The three registers may be programmed in a byte–oriented fashion. The registers retain their values as long as power is applied. Thus, usually both the C and R Registers are programmed just once, right after power up.

The C Register, which configures the device, is programmed with $C0 (1 byte). This sets the phase detector to the proper polarity and activates PD_{out}. This also turns off the unused outputs. The phase detector polarity is determined by the filter and the VCM. For this example, the MC1658 data sheet shows that a higher voltage level is needed if speed is to be increased. However, the low–pass filter inverts the signal from the phase detector (due to the active element configuration). Therefore, the programming of the polarity for the phase detector means that the POL bit must be a "1."

The R Register is programmed for a divide value that results in the proper frequency at the phase detector reference input. In this case, 230 kHz is needed. Therefore, with the 4.6 MHz source shown in Figure 3, the R Register needs a value of $000014 (3 bytes, 20 in decimal).

The N Register determines the frequency tuned. Tuning 9.2 MHz requires the proper value for N to multiply up the reference of 230 kHz to 9.2 MHz. This is 40 decimal. For 12.19 MHz, the value is 53 decimal. To tune over the range, change the value in the N Register within the range of 40 to 53 with a 2–byte transfer. Table 1 shows the possible frequencies.

Table 1. The HF Oscillator Frequencies

N Value	Frequency, MHz
40	9.20
41	9.43
42	9.66
43	9.89
44	10.12
45	10.35
46	10.58
47	10.81
48	11.04
49	11.27
50	11.50
51	11.73
52	11.96
53	12.19

4

EXTRA FILTERING FOR THE HF LOOP

When the HF oscillator was built, the proper frequencies could not be tuned. The output of the MC1658 was examined with an oscilloscope and the switching edges were discovered to be "ragged." That is, the output did not appear to be a square wave with clean transitions.

The f_{in} input of the MC145170 is sensitive to 500 mV p–p signals, and the ragged edges were being amplified and counted down by the N Counter. Therefore, the edges needed cleaning up. One method would have been to add a low–pass filter between the MC1658 and MC145170. However, because an additional buffer was needed elsewhere in the circuit, an MC74HCU04 inverter was used in place of the filter. This inverter's frequency response is low enough to clean up the ragged edges. That is, filtering of the ragged edges occurred, and the output had smoother transitions. As mentioned previously, one of the elements in the inverter package was used to buffer the output of the VCM before feeding it to the outside world. See Figure 3.

VHF SYNTHESIZER

The MC145170 may be used in VHF designs, also. The range for this next example is 140 to 160 MHz in 100 kHz increments.

VHF SYNTHESIZER LOW–PASS FILTER

To illustrate design with the doubled–ended phase detector, the ϕ_R and ϕ_V outputs are used. This requires an operational amplifier, as shown in Figure 5. From the design guidelines shown in the MC145170 data sheet, the following equations are used:

$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{N\,C\,R_1}} \qquad (1)$$

$$\text{damping factor} \quad \zeta = \frac{\omega_n R_2 C}{2} \qquad (2)$$

where, from the data sheet, the equation for the ϕ_R and ϕ_V phase detector,

$$K_\phi = \frac{V_{DD}}{2\pi} = \frac{5}{2\pi} = 0.796 \text{ V/rad} \qquad (3)$$

$$\zeta = 0.707,$$

$$\omega_n = \frac{2\pi f_R}{50} = \frac{2\pi \times 100 \text{ kHz}}{50} = 12{,}566 \text{ rad/s} \qquad (4)$$

and

$$K_{VCO} = \frac{2\pi\,\Delta\, f_{VCO}}{\Delta\, V_{VCO}} = \frac{2\pi \times (160 - 140 \text{ MHz})}{10 - 2}$$

$$= 1.57 \times 10^7 \text{ rad/s/V} \qquad (5)$$

The control voltage range on the input to the VCO is picked to be 2 to 10 V.

The average frequency = (140 + 160)/2 = 150 MHz. Therefore, the average N = 1500.

The above choices for ζ and ω_n are rules of thumb that are a good design starting point. A larger ω_n value results in faster loop lock times and higher reference frequency VCO sidebands for similar sideband filtering. (See Advanced Considerations.)

Choosing C_1 to be 4700 pF, R_1 is calculated from the rearranged expression for ω_n as:

$$R_1 = \frac{K_\phi K_{VCO}}{C_1 \omega_n^2 N} = \frac{(0.796 \text{ V/rad})(1.57 \times 10^7 \text{ rad/s/V})}{(4700 \text{ pF})(12{,}566 \text{ rad/s})^2\,(1500)}$$

$$= 11.23 \text{ k}\Omega \qquad (6)$$

Therefore, chose an 11 kΩ standard value resistor.
R_2 is determined from:

$$R_2 = \frac{2\zeta}{\omega_n C_1} = \frac{(2)(0.707)}{(12{,}566)(4700 \text{ pF})}$$

$$= 23.94 \text{ k}\Omega \text{ or}$$
$$24 \text{ k}\Omega \text{ (standard value)} \qquad (7)$$

VHF SYNTHESIZER EXTRA FILTERING

For more demanding applications, extra filtering is sometimes added. This reduces the VCO sidebands caused by a small amount of the reference frequency feeding through the filter. One form of this filtering consists of spitting R1 into two resistors; each resistor is one–half the value of R1, as indicated by R1/2 in Figure 5. Capacitors C_C are added from the

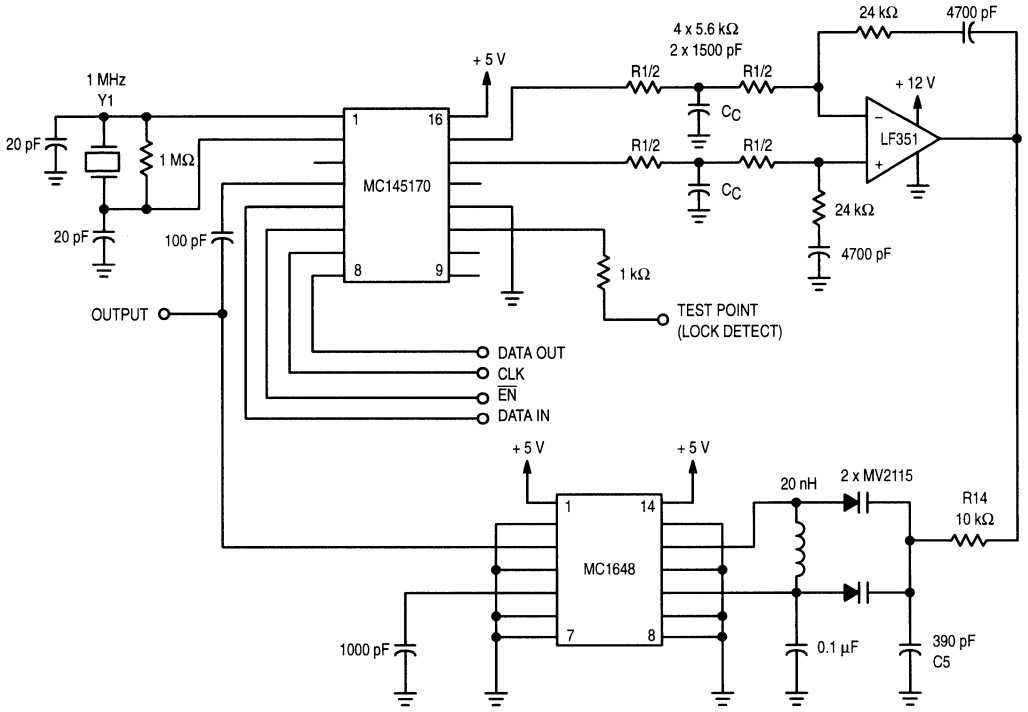

Figure 5. VHF Synthesizer

midpoints to ground to further filter the reference sidebands. The value of C_C is chosen so that the corner frequency of this added network does not significantly affect the original loop bandwidth ω_B.

The rule of thumb for an initial value is $C_C = 4 / (R1\ \omega_{RC})$, where ω_{RC} is the filter cutoff frequency. A good value is to choose ω_{RC} to be 10 x ω_B, so as to not significantly impact the original filter.

$$\omega_B = \omega_n \sqrt{1 + 2\zeta^2 + \sqrt{2 + 4\zeta^2 + 4\zeta^4}} \qquad (8)$$

$$= 12{,}566\sqrt{1+(2)(0.707)^2+ \sqrt{2+(4)(0.707)^2+ (4)(0.707)^4}}$$

$$= 25{,}760 \text{ rad/s}$$

$$\omega_{RC} = 10\ \omega_B = (10)(25{,}760) = 257{,}600 \text{ rad/s} \qquad (9)$$

$$C_C = \frac{4}{R1\omega_{RC}} = \frac{4}{(11.23\ k\Omega)(257{,}600 \text{ rad/s})} \qquad (10)$$

$$= 1383 \text{ pF} \approx 1500 \text{ pF}$$

There is also a filter formed at the input to the VCO. Again, this should be selected to ensure that it does not significantly affect the loop bandwidth. For this example, the filter is dominated by R14 with C5. The capacitance of the varactors (in series with the rest of the circuit) is much smaller than C5 and can therefore be neglected for this calculation.

As above, let $\omega_{RC} = 257{,}600$ rad/s be the cutoff of this filter. R1 was previously chosen to be 10 kΩ. Therefore,

$$C_5 = \frac{1}{\omega_{RC} R_{14}} = \frac{1}{(257{,}600)(10\ k\Omega)} \qquad (11)$$

$$= 388 \text{ pF} \approx 390 \text{ pF}$$

THE VARACTOR

The MV2115 was selected for its tuning ratio of 2.6 to 1. The capacitance can be changed from 49.1 pF to 127.7 pF over a reverse bias swing of 2 to 30 volts. Contact your Motorola representative for information regarding the MV2115 varactor diode.

For example, three parameters are considered.

C_T = Nominal capacitance
CR = Capacitance ratio
fR = Frequency ratio

$$CR = \frac{C_V min}{C_V max} = \left(\frac{V_{max}}{V_{min}}\right)^{\rho} \qquad (12)$$

where ρ = the capacitance exponent

Therefore,

$$CR = 2.6 = \left(\frac{30}{2}\right)^{\rho} \quad (13)$$

$$\log(2.6) = \rho\log(15) \quad (14)$$

$$\rho = \log(2.6)/\log(15) = 0.3528 \quad (15)$$

Using the nominal capacitance of 100 pF at 4 volts:

$$\frac{100\text{ pF}}{C_V\text{max}} = \left(\frac{10}{4\text{ V}}\right)^{0.3528} \quad (16)$$

$$\frac{100\text{ pF}}{C_V\text{max}} = 1.382$$

Solving for $C_V$max:

$$\frac{100\text{ pF}}{1.382} = 72.4\text{ pF}$$

Solving for $C_V$min:

$$2.6 = \frac{C_V\text{min}}{49.1\text{ pF}} \quad (17)$$

$$C_V\text{min} = (2.6)(49.1\text{ pF})$$

$$C_V\text{min} = 127.7\text{ pF}$$

4

THE VCO

For convenience, the MC1648 VCO is selected. The tuning range of the VCO may be calculated as

$$\frac{f_{max}}{f_{min}} = \frac{(C_d\text{max} + C_S)^{0.5}}{(C_d\text{min} + C_S)^{0.5}} \quad (18)$$

where

$$f_{min} = \frac{1}{2\pi[L(C_d\text{max} + C_S)]^{0.5}} \quad (19)$$

As shown in Figure 8 of the data sheet, the VCO tank circuit is comprised of two varactors and an inductor. Typically, a single varactor might be used in either a series or parallel configuration. However, the second varactor has a two–fold purpose. First, if the 10 kΩ isolating impedance is left in place, the varactors add in series for a smaller capacitance. Second, the added varactor acts to eliminate distortion due to the tank voltage changing.

Therefore, with the two varactors in series, $C_d$max′ = $C_d$max/2. The shunt capacitance (input plus external capacitance) is symbolized by C_S.
Therefore, solving for the inductance:

$$L = \frac{1}{(2\pi f_{min})^2(C_d\text{max}' + C_S)} = 19.9\text{ nH} \approx 20\text{ nH} \quad (20)$$

The Q of the inductor should be more than 100 for best performance.

$$f_{min} = \frac{1}{2\pi[(19.9\text{ nH})(69.85\text{ pF})]^{0.5}} = 135\text{ MHz} \quad (21)$$

$$f_{max} = \frac{1}{2\pi[(19.9\text{ nH})(42.2\text{ pF})]^{0.5}} = 173\text{ MHz} \quad (22)$$

The frequency ratio is 1.5 to 1 and is impacted by the tuning range of the MV2115 varactor diode used in the tank circuit. Therefore, the required range of 140 to 160 MHz is not limited by this VCO design.

A pc board should be used to obtain favorable results with this VHF circuit. The lead lengths in the tank circuit should be kept short to minimize parasitic inductance. The length of the trace from the VCO output to the PLL input should be kept as short as possible. In addition, use of surface–mount components is recommended to help minimize strays.

VHF SYNTHESIZER PROGRAMMING

Again, programming the three registers of the MC145170 is straightforward. Also, usually both the C and the R Registers are programmed only once, after power up.

The C Register configures the device and is programmed with $80 (1 byte). This sets the phase detector to the correct polarity and activates the ϕ_R and ϕ_V outputs while turning off the other outputs. Like the HF oscillator, the phase detector polarity is determined by how the filter is hooked up and the VCO.

The R Register is programmed for a divide value that delivers the proper frequency at the phase detector reference input. In this case, 100 kHz is needed. Therefore, with the 1 MHz crystal shown, the R Register needs a value of $00000A (3 bytes, 10 in decimal).

The N Register determines the frequency tuned. To tune 140 MHz, the value required for N to multiply up the reference of 100 kHz to 140 MHz is 1400 decimal. For 160 MHz, the value is 1600 decimal. To tune over the range, simply change the value in the N Register with a 2–byte transfer.

ADVANCED CONSIDERATIONS

The circuit of Figure 5 may not function at very–high temperature. The reason is that the MC145170 is guaranteed to a maximum frequency of 160 MHz at 85°C. Therefore, there is no margin for overshoot (reference Figure 4) at high temperature. There are two possible solutions: (1) use the MC145170–1 which is rated to 185 MHz, or (2) limit the tuning to less than 160 MHz.

Operational amplifiers are usually too noisy for critical applications. Therefore, if an active element is required in the integrator, one or more discrete transistors are utilized. These may be FETs or bipolar devices. However, active filter elements are not needed if the VCO loading is not severe, such as is encountered with most discrete VCO designs. Because active elements add noise, some performance parameters are improved if they are not used. On the other hand, an active filter can be used to scale up the VCO control voltage. For example, to tune a wide range, the control voltage may have to range up to 10 V. For a 5 V PLL output, this would be scaled by 2x via use of active elements.

Some applications have requirements that must be met in the areas of phase noise and reference suppression. These parameters are in conflict with fast lock times. That is, as lock times are reduced, reference suppression becomes more difficult. Both reference suppression and phase noise are advanced areas that are covered in several publications. As an example, consider that the VCO input voltage range for the above VHF loop was merely picked to be 8 V. Advanced

techniques demand a trade off between this voltage range and the spectral purity of the VCO output. This is because the lower the control voltage range, the more sensitive the VCO is to noise coming into its control input.

A VCO IC may not offer enough performance for some applications. Therefore, the VCO may have to be designed from discrete components.

Figure 6 shows the performance of the VHF Oscillator prototype on a spectrum analyzer. Note that the reference sidebands appear at 100 kHz as expected, and are 50 dB down.

REFERENCES

CMOS Application–Specific Standard ICs, book DL130/D, Motorola, 1990, MC145170 data sheet and AN535 application note.

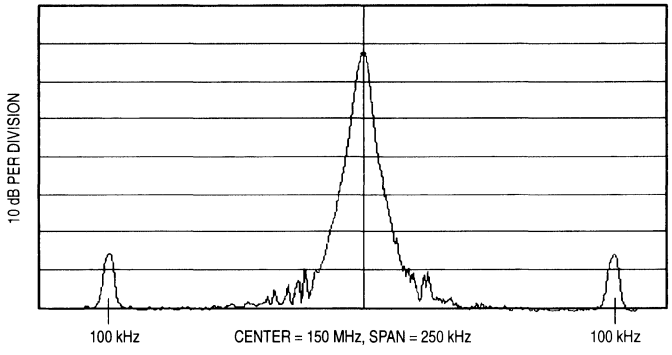

Figure 6. VHF Oscillator Performance

AN1253

An Improved PLL Design Method Without ω_n and ζ

Prepared by: Morris Smith

INTRODUCTION

This paper is a design guide for PLL synthesizers used in wireless products. It focuses on compact, low current and low cost synthesizers. Natural frequency and damping are not used in the calculations. The topics covered are:

a) PLL–related limitations on receiver and transmitter performance.
b) A simple measurement of charge pump spurious current at the reference frequency has been developed. It will be included on future datasheets. Formulas have been developed relating the spurious current at one reference frequency to other frequencies.
c) Optimal loop filter component values and PLL performance where design criteria include reference modulation bandwidth, VCO modulation bandwidth, switching time, overshoot after switching time period, reference sideband level, and noise within loop bandwidth.
d) Circuit and charge pump design compromises. Also design tolerance to changes in loop gain can be determined.

Topics are divided into three sections: system limitations and spurious current measurement; formulas and related tradeoffs; and a worked out and tested example.

4

SYSTEM LIMITATIONS AND SPURIOUS CURRENT MEASUREMENT

THIRD ORDER INTERMODULATION

This is mixing in a receiver front end which causes two adjacent strong undesired signals to mix onto a weak desired signal. Intermod dynamic range is defined as the difference between noise floor and undesired signal level that causes third order products to be mixed at the noise floor level. Third order products are shown below:

Example: f = desired signal, f_1, f_2 = undesired signal
$f_1 = f+\Delta$
$f_2 = f+2\Delta$
Δ = channel spacing

3rd order product falling on f:

$= 2f_1-f_2$
$= 2(f+\Delta) - (f+2\Delta)$
$= 2f+2\Delta - f - 2\Delta$
$= f$

PHASE NOISE

VCO phase noise can mix with strong adjacent channel signals to cover up a weak desired signal. The level of translated noise would depend on IF filter bandwidth and VCO noise density at a one channel offset from center frequency. Phase noise dynamic range is defined as the difference between noise floor and input signal level that causes phase noise to be mixed at the noise floor level. The formula is:

DRØ = |Ø| – 10 log B
DRØ – Phase noise dynamic range (in dB)
Ø – Phase noise power density at adjacent channel offset (in dBc/Hz)
B – IF Bandwidth (in Hz)

REFERENCE SIDEBANDS

Sidebands cause the same effects as phase noise. They are however represented as a power level rather than power density. Also the product on the desired channel can be demodulated. Reference sideband dynamic range is the dB ratio between VCO carrier level and first sideband level.

OPTIMAL DESIGN

Optimal receiver design requires that 3rd order intermod dynamic range be equal to both the phase noise dynamic range and reference sideband dynamic range. Two undesired signals can simultaneously cause intermod, mix with VCO phase noise, and mix with reference sidebands.

SIGNAL TO NOISE RATIO

Signal to noise ratio in an FM or AM system can be estimated from the phase noise at the lowest offset frequency that contains information and the IF filter bandwidth.

SNR = |Ø| – 10 log B, where |Ø| = phase noise at lowest offset frequency

Actual signal to noise is better due to the noise decrease as offset frequency is increased. In an FM system, preemphasis and deemphasis provide additional SNR improvement. A good telephone line has a SNR of 40 dB and a cassette tape is 60 dB. Digital communications need better phase noise closer in.

WHY USE A CURRENT SOURCE CHARGE PUMP?

The current source charge pump has advantages over both the switching (pull up/pull down) and sample and hold types. Switching types have nonlinear gain over their output voltage range, which also depends on the direction the VCO is being pulled. The output FETs have a fixed on resistance. As a supply rail is approached, current the FET supplies when turned on decreases. This effect could mean a 10:1 variation of loop gain. The current source has a constant output current over its operating range. Sample and hold types have a transient output pulse present when state changes from sample to hold. This moves the VCO off frequency.

CHARGE PUMP LINEARITY

Pull up and pull down current must be equal for loop linearity. Current must be constant over the operating voltage

range and from unit to unit over temperature. Loop gain changes proportionate to changes in charge pump current.

As an example of what can happen, a 25 ms switching loop was analyzed with a reduction in loop gain of 40%. Switching time increased to 41 ms, an increase of 64%. Transmitters which modulate the VCO or reference rely on constant current to maintain desired modulation roll–off frequencies. To reduce current consumption and noise, the filter of Figure 1 has been widely adopted.

SPURIOUS CURRENT MEASUREMENT

The spurious current measured is the RMS current component at the reference frequency passing through a two–element filter. The PLL must be phase locked. Current source charge pumps produce current components at least up to the 30th harmonic of reference frequency. Levels do not decline rapidly from harmonic to harmonic.

Through a current probe with 50 ohm output, and possibly a low noise amplifier, the spectrum analyzer can make a direct measurement. Many modern analyzers can convert the units of measure and add a correction factor. Try to use the current transformer with one turn through the core and increase the signal with the LNA. This will reduce the inductance in series with the loop filter. Inductance has not been a problem as long as the hole in the core isn't filled with wire. The test setup is shown in Figure 2.

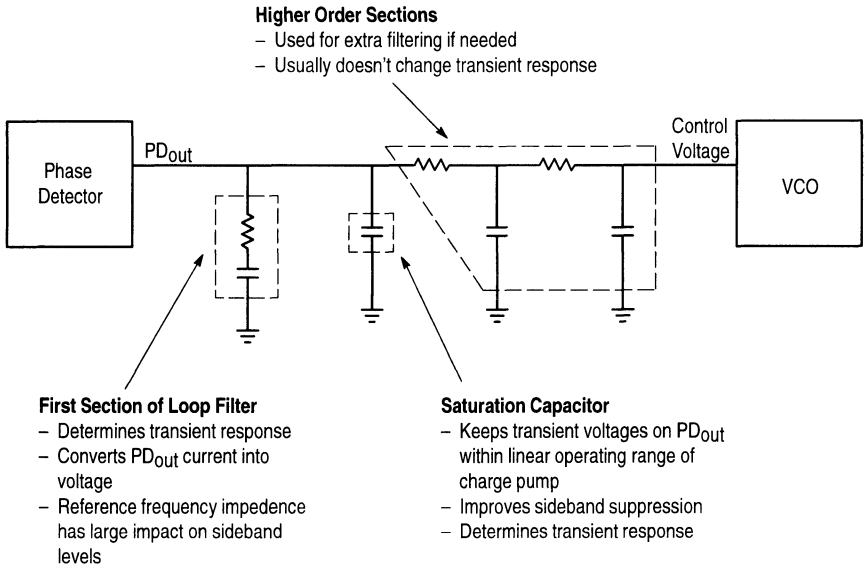

Figure 1. Standard Loop Filter

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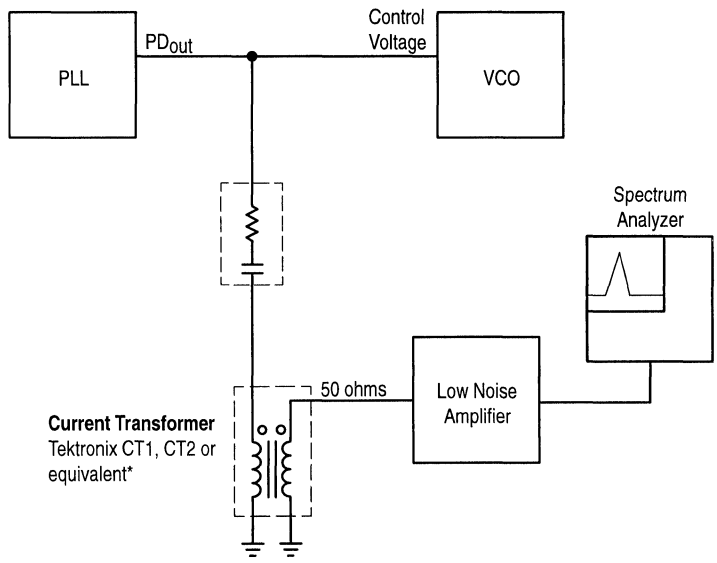

* Motorola cannot recommend one supplier over another and in no way suggests that this is a complete listing of transformer manufacturers.

Figure 2. Spurious Current Measurement

Table 1. Sample Measurements for the Motorola MC145190 PLL

Reference Frequency (kHz)	Current (nA)
10	1.95
20	4.5
25	11.0
50	28.4
100	141

FORMULA SUMMARY FOR SECOND ORDER PLL

DEFINITION OF VARIABLES

Where r and c are referred to, they are the first section resistor and capacitor of the loop filter. The loop analyzed has a second order response. Also described is a way to add additional higher order sections. All variables use base units. Bandwidth relations assume the use of optimal component values for maximum reference suppression. Log[x] is natural Log of x. Log[10,x] is base 10 Log of x. '190 and '191 are the Motorola MC145190 and MC145191 devices.

```
kv =  VCO Gain (Radians/Second)/Volt
kp =  Phase Detector gain (Amps/Radian)
a  =  kp*kv
n  =  Feedback divide ratio from VCO
t  =  time variable or switching time
      depending on formula (Seconds)
w  =  frequency variable or 3dB cutoff
      frequency depending on formula
      (Radians/Second)
r  =  resistor value (Ohms)
c  =  capacitor value (Farads)
```

$$b = \mathrm{Log}\left[\frac{\text{deviation}}{\text{tune\_range}}\right]$$

```
deviation  = Allowed frequency deviation
             (absolute value) from final
             frequency after switching time
             has elapsed (Hz)
tune_range = Output Frequency Range of VCO
             (Hz)
```

Closed loop gain in S plane is:

$$CG = \frac{VCO\_Phase}{Reference\_Phase} = \frac{\frac{a}{a\,r\,s + \frac{a}{c}}}{\frac{a}{n\,c} + \frac{a\,r\,s}{n} + s^2}$$

To satisfy switching time, overshoot requirements, provide best reference suppression and lowest thermal noise, resistance r and capacitance c are:

$$r = -\left(\frac{2\,n\,b}{a\,t}\right)$$

$$c = \frac{2\,a\,t}{n\,(b^2 + Pi^2)}$$

Normalized phase or frequency step response as a function of time (t) is:

$$nsr = 1 - \frac{Cos\left[\frac{a^{1/2}\,(4\,n - a\,c\,r^2)^{2\,1/2}\,t}{2\,c\,n^{1/2}}\right]}{E^{(a\,r\,t)/(2\,n)}} + \frac{a^{1/2}\,c^{1/2}\,r\,Sin\left[\frac{a^{1/2}\,(4\,n - a\,c\,r^2)^{2\,1/2}\,t}{2\,c\,n^{1/2}}\right]}{E^{(a\,r\,t)/(2\,n)}\,(4\,n - a\,c\,r^2)^{2\,1/2}}$$

The step response gives a final value of 1 and can be scaled for any frequency step.

Impedance of the optimal loop filter as a function of radian frequency (w) is:

$$z = \frac{n\,\left(b^4 + 2\,b^2\,Pi^2 + Pi^4 + 4\,b^2\,t^2\,w^2\right)^{1/2}}{t^4\,w^4\,a}$$

VCO MODULATION VOLTAGE

```
l    = RMS leakage current component at
       reference frequency
lx   = RMS leakage current component at
       highest frequency
f    = Reference Frequency
fx   = Highest reference frequency
Vrms = RMS modulation voltage
```

Over at least a 10 kHz to 100 kHz reference frequency range, leakage current can be predicted from a measurement at the highest frequency. Accuracy is better than 3 dB in sideband level.

Charge pump leakage current (lx) is measured using a Tektronix* CT–1 or CT–2 probe and spectrum analyzer. The probe is placed in the ground leg of loop filter. The spectrum analyzer measures RMS voltage into 50 ohms at the reference frequency. Using the probe calibration factor, current is computed. It is important that during measurement, the ground lead of loop filter be connected at the point where it ordinarily would be attached. Currents are in the nano–amp range and can be affected by digital circuit ground currents in other parts of the board. Leakage current is:

$$l = \left(\frac{f}{fx}\right)^2 lx$$

VCO modulation voltage is: Vrms = 1 z

SIDEBAND SUPPRESSION IN dBs

where Vrms = RMS volts modulating voltage on VCO tune line
Psb = Reference sideband suppression in dB (stated as positive number)
kv = VCO tuning sensitivity in (radians/second)/volt
f = Modulation (reference) frequency in Hz

$$Psb = 3.01 + 20\ Log[10, f] - 20\ Log[10, \frac{kv}{2\ Pi}] - 20\ Log[10, Vrms]$$

To increase sideband suppression, without changing other performance traits, an extra resistor–capacitor section can be added. The corner frequency should be at 10x the closed loop gain (– 3 dB) frequency and the resistor value should be 10x the loop filter resistor. A high resistor value helps isolate the two filter sections. On a functioning PLL it may be possible to lower both the corner frequency and resistor value of the added section. An extra section will add 20 dB/decade reference suppression above its corner frequency.

CLOSED LOOP GAIN

Closed loop gain as a function of radian frequency (w) is:

$$\text{Closed loop gain (cgw)} = \frac{\text{VCO frequency deviation}}{\text{Reference frequency deviation}}$$

$$cgw = \left(\frac{n^2\ (b_4^4 + 2\ b_2^2\ Pi^2 + Pi^4 + 4\ b_2^2\ t^2\ w^2)}{b_4^4 + 2\ b_2^2\ Pi^2 + Pi^4 + 2\ b_2^2\ t^2\ w^2 - 2\ Pi^2\ t^2\ w^2 + t^4\ w^4}\right)^{1/2}$$

DC gain is n. At infinite frequency it is 0. For cgw in Hz make the substitution for w (w = 2 Pi f). When stated in dBs, closed loop gain is the phase detector noise multiplication factor. In dBs:

cgwdB = 20*Log[10,cgw]

The following three formulas relate switching time, overshoot and the – 3 dB frequency of closed loop gain using an optimal filter.

The – 3 dB (relative to dc) frequency is:

$$w = \frac{(3\ b_2^2 + Pi^2 + 2\ (5\ b_4^4 + 4\ b_2^2\ Pi^2 + Pi^4)^{1/2})^{1/2}}{t}$$

Overshoot is:

$$b = -(-Pi^2 - 3\ t^2\ w^2 + 2\ t\ w\ (2\ Pi^2 + 5\ t^2\ w^2)^{1/2})$$

Switching time is:

$$t = \frac{(3\ b_2^2 + Pi^2 + 2\ (5\ b_4^4 + 4\ b_2^2\ Pi^2 + Pi^4)^{1/2})^{1/2}}{w}$$

MODULATION RESPONSE

Modulation response as function of radian frequency (w) is:

(If modulation response is needed in Hz, use `Kv/(2 Pi)` to replace Kv and (`w = 2 Pi f`) to replace w.)

```
                              VCO frequency Change
Modulation Response (mr) = ----------------------
                             Control voltage change

                                      2  2
                                   kv t  w
mr = ------------------------------------------------------------
       4       2   2     4       2  2  2        2  2  2    4  4 1/2
     (b  + 2 b  Pi  + Pi  + 2 b  t  w  - 2 Pi  t  w  + t  w )
```

In dBs: mrdB = 20*Log[10,mr]
At infinite frequency mr = kv and at dc mr = 0.

The following three formulas relate switching time, overshoot, and the – 3 dB frequency of VCO modulation response using an optimal filter.

The – 3 dB frequency is:

```
      2     2    1/2   4     4 1/2 1/2
    (b  - Pi  + 2    (b  + Pi )   )
w = ----------------------------------
                    t
```

Overshoot is:

```
         2    2  2    1/2          2    2  2 1/2 1/2
b = -(-Pi  - t  w  + 2    t w (2 Pi  + t  w )   )
```

Switching time is:

```
      2     2    1/2   4     4 1/2 1/2
    (b  - Pi  + 2    (b  + Pi )   )
t = ----------------------------------
                    w
```

CHARGE PUMP DYNAMIC RANGE

The charge pump output voltage range must cover VCO tune range, twice the overshoot, and twice the voltage spikes caused by correction pulses. When switching from low to high channel or high to low channel, there will be a point where correction pulses ride on top of peak overshoot. The voltage spike magnitude is given by ohms law where (i) is charge pump current and (r) is loop filter resistor. For a maximum value of r in a given circuit there is a minimum switching time.

CHARGE PUMP CURRENT

Increasing charge pump current will reduce thermal noise from the loop filter resistor, but it won't change the minimum switching time. It will also increase the capacitor value proportionately.

REDUCE SWITCHING TIME BY INCREASING VCO SENSITIVITY

The 25 ms loop given as an example was the minimum switching time for the tuning range and VCO used with the '190 and a 8.5 volt charge pump supply. Increasing VCO sensitivity reduces switching time somewhat more than proportionately. Sideband levels would remain the same for the same switching time. This is because increasing Kv decreases loop filter resistor to exactly compensate. Noise within loop bandwidth will stay the same but thermal noise from the loop filter resistor gets worse. Thermal noise modulation voltage is proportional to square root of r. For a 10x increase in Kv, r drops by a factor of 10 and thermal noise level increases by 10 dB. It is possible to have spurious pickup problems outside loop bandwidth with high Kv. Also maintaining Q in the VCO while increasing coupling between varicap diodes and tuned circuit, and obtaining high value high tolerance loop filter capacitors can be difficult. Thermal noise will probably not be a problem in common high volume applications of PLLs.

SOURCE/SINK CURRENT MATCH CHANGES SWITCHING TIME

Lack of source/sink match makes it difficult to achieve design values of switching time. For some value of mismatch and switching in one direction, the design value should be in between the source and sink, and closer to the one which is on for the most time. The position of the design value relative to source and sink should be inversely proportionate to the relative on times during the switching period. In the example circuit, for a low to high channel jump, the design value was 2 mA, optimal source current was 1.97 mA, and sink was 2.14 mA. Measured switching time was 27.4 ms. Switching in the opposite direction took 34.3 ms. The 8.5% source sink mismatch caused worst case switching time to be 37% slower than the design value.

EFFECTS OF USING STEP SIZE WHICH IS SUB–MULTIPLE OF CHANNEL SPACING

The same sideband suppression can be obtained with the same switching time at any sub–multiple step size of the channel spacing. This assumes the loop is linear. Since r is proportionate to the feedback divider ratio, the loop will only be linear for longer switching times. Thermal noise gets worse proportionate to square root of r. Noise in loop bandwidth gets a little worse over a wide range of step sizes. The '190 phase detector at 10 Hz offset with 10 kHz step size had noise of –156 dB/Hz and at 100 kHz step size, it was –141 dBc/Hz. Because of noise multiplication, there would be a 5 dB benefit to using the 100 kHz step size.

VCO SENSITIVITY CHANGE AS MODULATION FREQUENCY VARIES

Above the – 3 dB frequency of modulation response, the output frequency will deviate the same amount for the same modulation voltage regardless of modulation frequency. However, the sidebands created will be greatest in magnitude at the lowest frequency. Sidebands will decline in value at a 20 dB/decade rate as modulation frequency increases. Due to the sideband slope, thermal noise, if it is a problem, will appear as a bump at the – 3 dB frequency of modulation response.

HIGHER CHARGE PUMP SUPPLY VOLTAGES REDUCE SWITCHING TIME AND NOISE

Using a higher supply voltage on the charge pump allows correction pulses to be larger with the loop remaining linear. The loop filter resistor can increase in value. Minimum switching time can decrease. Also VCO gain (kv) could be reduced. Lower VCO gain results in less thermal noise, less tendency to pick up noise outside loop bandwidth, higher oscillator Q and smaller value tighter tolerance capacitors in loop filter.

PRODUCTION SENSITIVITY

$$r = -\left(\frac{2\,n\,b}{a\,t}\right)$$

$$c = \frac{a^2\,t^2}{n\,(b^2 + Pi^2)}$$

There are two extrema of performance variation with component change. Only one need be calculated. One is:
n = n_max; a = a_min; r = r_min; c = c_max;

n in most applications varies by up to ± 10%. It isn't a problem if charge pump current can be ramped up and down (in software) to compensate (although the '190 and '191 devices presently do it in 10% steps). (a/n) ratio must be kept constant for all output frequencies. (a=kp*kv) is the major production problem. kv for a Motorola 'V17 VCO varies ± 5%. kp of the 14519X PLLs varies ± 40%. Total variation of (a) could be ± 47% using the above. A second order loop designed with a 40% tolerance of (a) had a 64% tolerance of switching time.

r can have up to 1% tolerance, with 5% being standard. c can be 1% tolerance, up to 5,000 pF (COG dielectric) with 5% standard. Above 5,000 pF, dielectric changes to X7R which has 5% or 10% tolerance. X7R dielectric is available up to about 0.5 µF in 5% tolerance. Above 0.5 µF tantalum, polystyrene or polypropylene can be used. Polypropylene and polystyrene are too large for compact wireless circuits. The only choice left, tantalum, is available only in 10% tolerance. Charge pump current should be set to keep capacitor in high tolerance range.

Conclusion: To build an optimal loop, high tolerance of kv and kp is needed.

CAN (a) BE REDUCED TO LOWER SIDEBAND LEVELS AFTER LOOP LOCK?

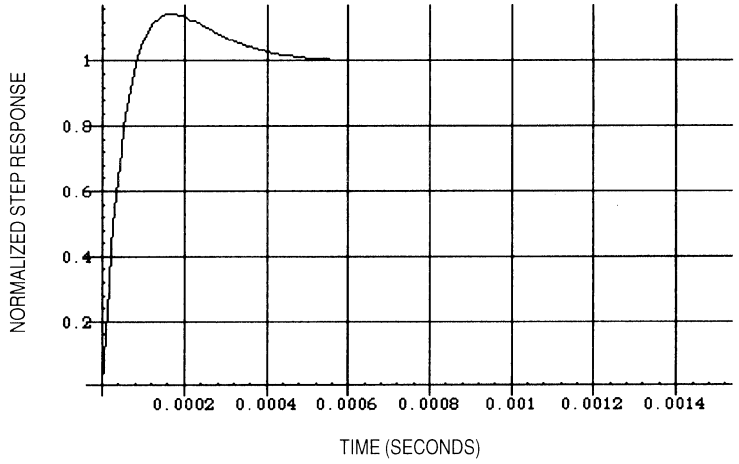

Figure 3. Step Response for a GSM Loop Designed for a = 6300

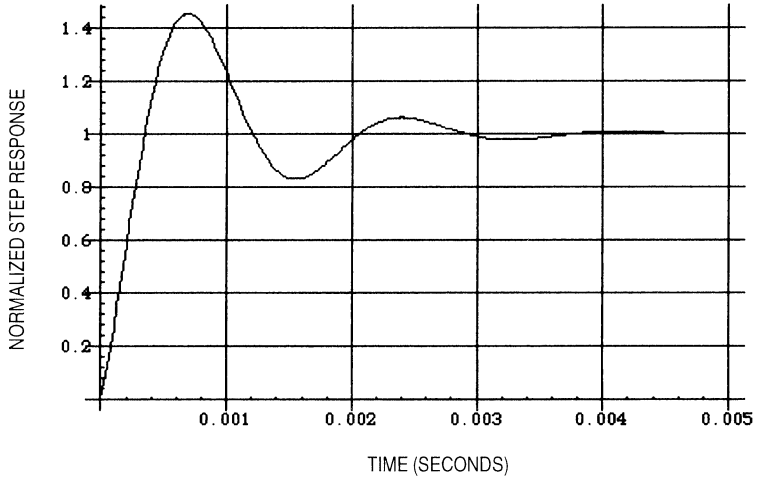

Figure 4. Step Response With All Parameters the Same Except a = 630

Note that time scales for the two graphs are different!

In most instances reducing (a) upsets loop dynamics too much. Even when locked, the VCO experiences disturbances; i.e. vibration. Overshoot can pull the PLL off frequency. Natural frequency is also much lower, so response is slow.

SATURATION CAPACITOR AND EXTRA FILTER SECTIONS

The calculated values for r and c have appeared experimentally to be optimum, with or without the saturation capacitor. To design the loop filter, r and c should first be selected. It is all right for the resistor to cause loop nonlinearity if the saturation capacitor has not been added. The saturation capacitor is added and adjusted for minimum switching time. A good initial value is 5 – 25% of c. Loop linearity is checked by making both small and large frequency jumps. If the loop isn't linear then the filter must be designed for a longer switching time. Extra filter sections are added to roll–off sidebands and PLL device noise, but should not modify transient response.

EXAMPLE: PLL THAT SWITCHES IN 25 ms

The PLL uses a MC145190 with 2 mA of charge pump current. Thus:

$$kp = \frac{0.002}{2\ Pi};$$

The Motorola custom VCO used (a V17) has a sensitivity of 3.0 – 3.3 MHz/volt. So converting to (radians / second) / volt:

$$kv = 2\ Pi\ 3.15\ 10^{6};$$

The design constant a is: a = kp kv = 6300

The VCO operates 739.3 – 749.3 MHz. Channel spacing is 100 kHz. The median feedback divide ratio (n) is:

$$n = \frac{744.3}{0.1} = 7443.$$

Switching time t given by system specification is 25 ms. Thus:

$$t = \frac{25}{10^{3}};$$

Frequency deviation tolerance is set at 1 kHz. Tune range is 10 MHz. b is:

$$b = \mathrm{Log}\left[\frac{0.001}{10}\right] = -9.21034$$

Resistor and capacitor values are:

$$r = -\left(\frac{2\ n\ b}{a\ t}\right) = 870.509$$

$$c = \frac{a\ t^{2}}{n\ (b^{2} + Pi^{2})} = 5.58628\ 10^{-6}$$

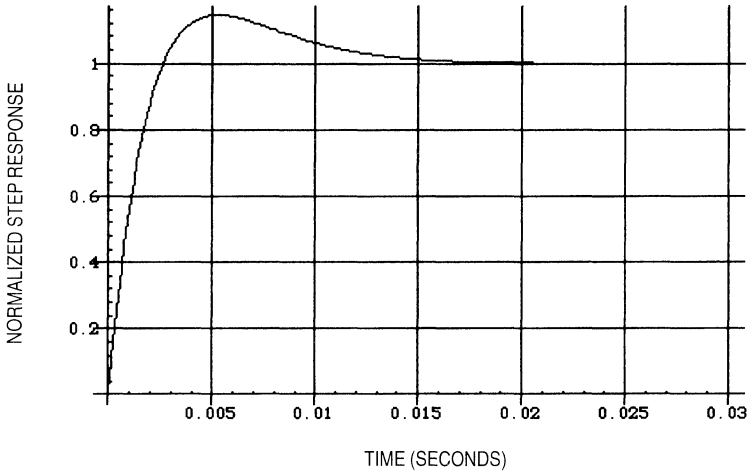

Figure 5. Normalized Step Response

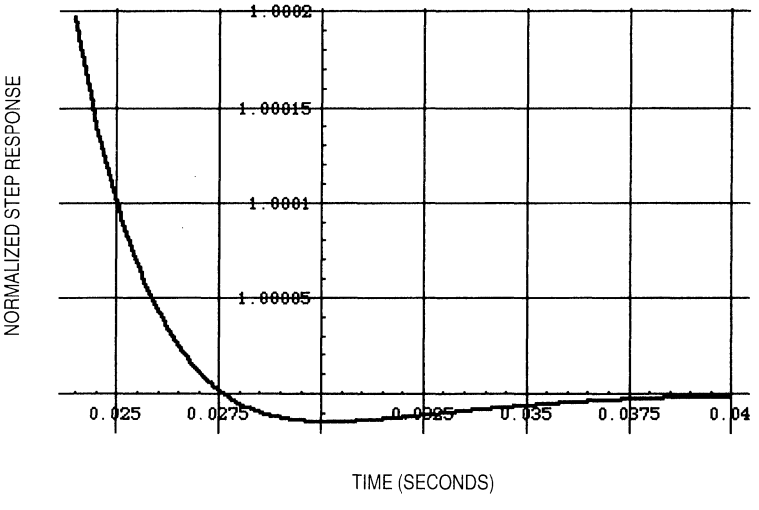

Figure 5a. Normalized Step Response — Expanded View

Loop filter impedance at 100 kHz is:

$$w = 2\,Pi\,1\,10\,;\; t = \frac{5}{10}\,\frac{25}{3};$$

$$z = \frac{n\left(\frac{b^4 + 2\,b^2\,Pi^2 + Pi^4 + 4\,b^2\,t^2\,w^2}{t^4\,w^2}\right)^{1/2}}{a} = 870.509$$

VCO MODULATION VOLTAGE

```
l    = RMS leakage current component at reference frequency
lx   = RMS leakage current component at highest frequency
f    = Reference Frequency
fx   = Highest reference frequency
Vrms = RMS modulation voltage
```

Over at least a 10 kHz to 100 kHz reference frequency range, leakage current can be predicted from a measurement at the highest frequency. Accuracy is better than 3 dB in sideband level.

$$f = 100\,10^{3}\,;\; fx = 200\,10^{3}\,;\; lx = \frac{564}{10^{9}};$$

$$l = \left(\frac{f}{fx}\right)^2 lx$$

$$= 1.41\,10^{-7}$$

VCO modulation voltage is: Vrms = l z = 0.000122742

SIDEBAND SUPPRESSION IN dBs

```
where  Vrms =  RMS volts modulating voltage on VCO tune line
       Psb  =  Reference sideband suppression in dB (stated as positive number)
       Kv   =  VCO tuning sensitivity in (Radians/Second)/volt
       f    =  Modulating frequency in Hz
```

$$Psb = 3.01 + 20\,Log[10, f] - 20\,Log\left[10, \frac{kv}{2\,Pi}\right] - 20\,Log[10, Vrms];$$

$$= 51.2639\ dB$$

CLOSED LOOP GAIN AS A FUNCTION OF FREQUENCY

This also gives phase detector noise multiplication when stated in dBs. For cgw in Hz, make the substitution for w (w = 2 Pi f).

$$\text{Closed loop gain} = \frac{\text{VCO frequency deviation}}{\text{Reference frequency deviation}}$$

$$cgw = \left(\frac{n^2 (b^4 + 2 b^2 Pi^2 + Pi^4 + 4 b^2 t^2 w^2)}{b^4 + 2 b^2 Pi^2 + Pi^4 + 2 b^2 t^2 w^2 - 2 Pi^2 t^2 w^2 + t^4 w^4}\right)^{1/2}$$

```
cgwdB = 20*Log[10,cgw];
```

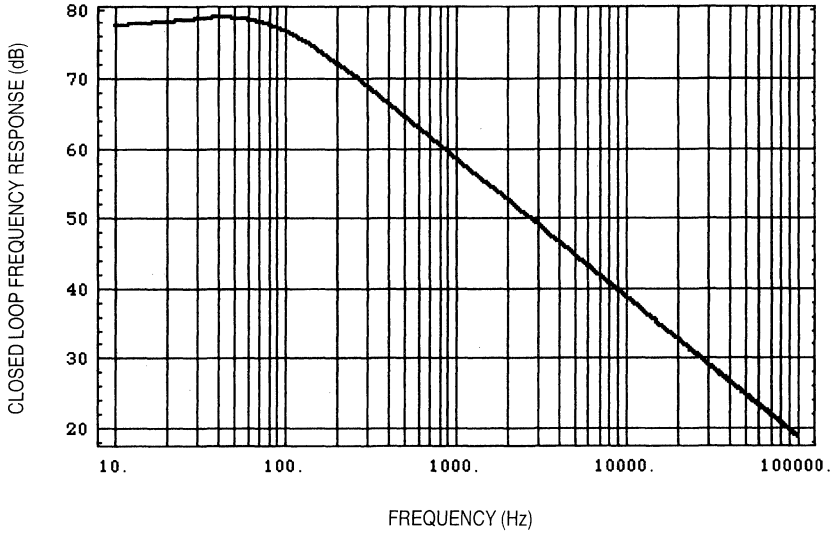

Figure 6. Closed Loop Gain

The – 3 dB frequency of closed loop gain is:

$$w = \frac{\left(3 b^2 + Pi^2 + 2 \left(5 b^4 + 4 b^2 Pi^2 + Pi^4\right)^{1/2}\right)^{1/2}}{t} = 933.956$$

$$f = \frac{w}{2 Pi} = 148.644 \text{ Hz}$$

VCO MODULATION RESPONSE

If modulation response is needed in Hz use `Kv/(2 Pi)` to replace Kv and (`w = 2 Pi f`) to replace w.

$$kv = kv/(2*Pi) = 3.15\ 10^{6}$$

$$mr = \frac{kv\ t^2\ w^2}{(b^4 + 2\ b^2\ Pi^2 + Pi^4 + 2\ b^2\ t^2\ w^2 - 2\ Pi^2\ t^2\ w^2 + t^4\ w^4)^{1/2}}$$

```
mrdB = 20*Log[10,mr];
```

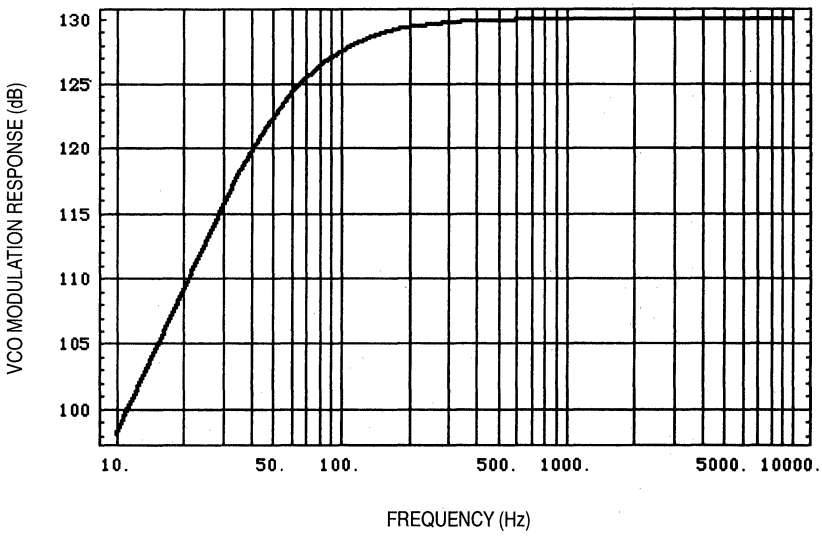

Figure 7. Modulation Response

The – 3 dB frequency of modulation response is:

$$w = \frac{(b^2 - Pi^2 + 2\ (b^4 + Pi^4)^{1/2})^{1/2}}{t}; \text{ where } f = \frac{w}{2\ Pi};$$

$$f = 89.0672\ Hz$$

PRODUCTION SENSITIVITY — A TOLERANCE ONLY

a=kp*kv is decreased by 40% to account for charge pump current tolerance in the '190 or '191 PLL. Thus a = 0.6*a = 3780.

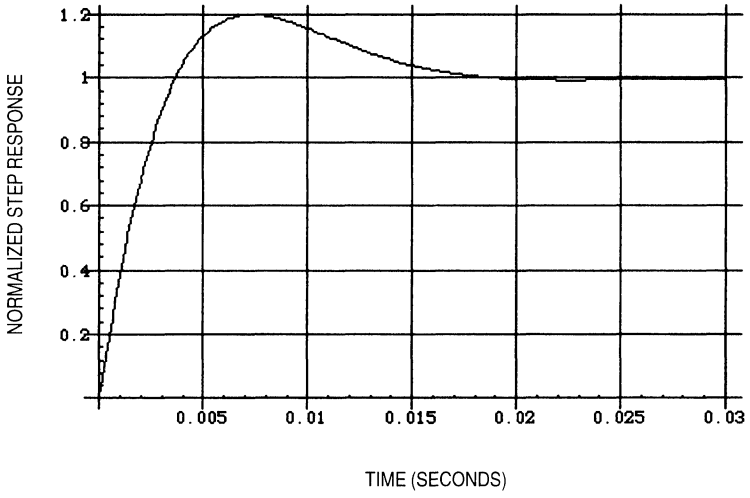

Figure 8. Normalized Step Response (a = 3780)

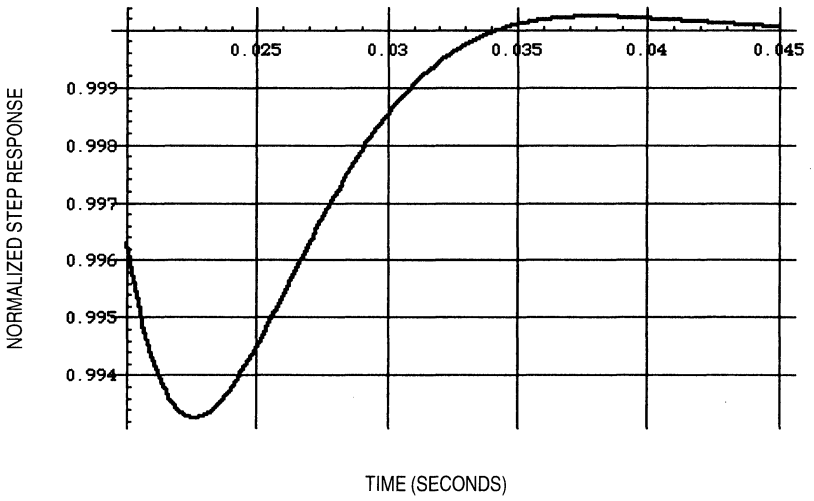

Figure 8a. Normalized Step Response — Expanded View (a = 3780)

The reduction in (a) of 40% has caused switching time to change from 25 ms to 41 ms. This is an increase of 64%.

PRODUCTION SENSITIVITY — CUMULATIVE TOLERANCE

a was decreased previously by 40% to account for tolerance. r and c 5% tolerances are assumed. Therefore:

```
                                -6
c = 1.05*c = 5.86559 10    ,  r = 0.95*r = 826.983
```

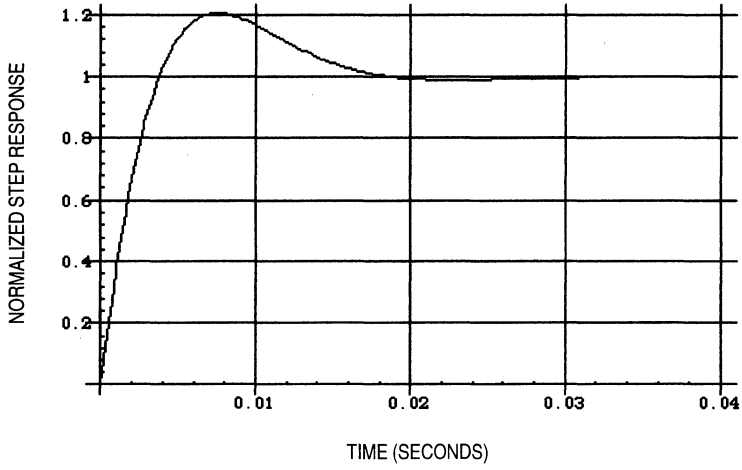

Figure 9. Normalized Step Response

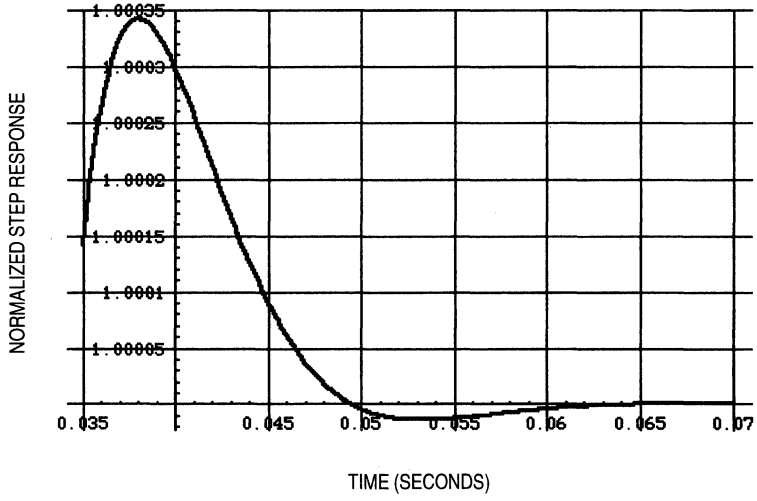

Figure 9a. Normalized Step Response — Expanded View

Switching time is 45 ms with resistor capacitor and charge pump variation. Original design value was 25 ms. Switching time is 80% worse.

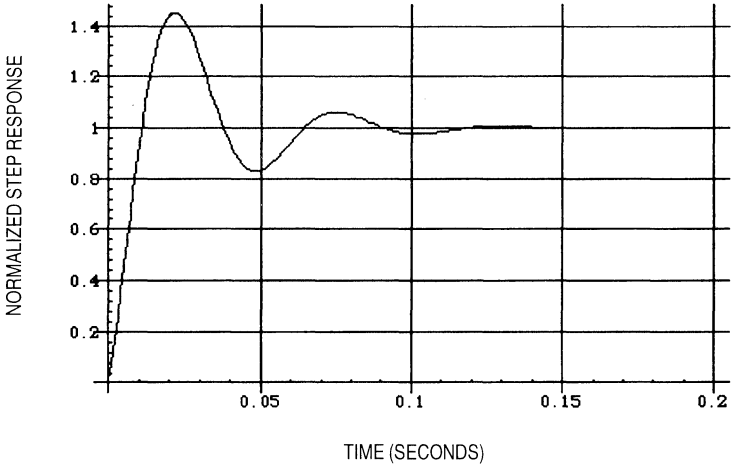

Figure 10. Normalized Step Response When a is Reduced by Factor of 10

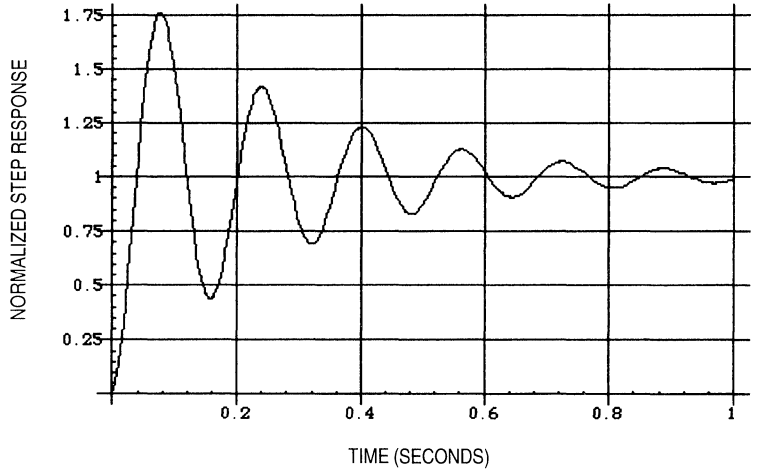

Figure 11. Normalized Step Response When a is Reduced by Factor of 100

REFERENCES

1. Mathematica Enhanced version 2.2, Wolfram Research, Champaign IL, 1993.

2. Discussions with Jim Irwin of Motorola, Semiconductor Products Sector.

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Article Reprint

Phase-Locked Loop Design Articles

- "Analyze, Don't Estimate, Phase–Locked Loop Performance"
- "Optimize Phase–Lock Loops to Meet Your Needs — Or Determine Why You Can't"
- "Suppress Phase–Lock–Loop Sidebands Without Introducing Instability"
- "Programmable Calculator Computes PLL Noise, Stability"

4

Analyze, don't estimate, phase–lock–loop

performance of type–2, third–order systems. You can do the job with a programmable–calculator in 48 steps, or less.

Phase–lock loops certainly have many uses, especially in frequency synthesizers, but exact mathematical calculation of their transfer functions is difficult. This is particularly true for type–2, third–order systems (Figure 1), which don't produce steady–state phase errors for step–position or velocity signal inputs. However, a small programmable calculator, the HP–25, easily — and exactly — determines the complete loop transfer function in 48 steps. In addition, the program data reveals the noise reduction you can expect for the loop's voltage– controlled oscillator (VCO), as well as the loop's stability.

Most other design approaches must resort to second–order loop approximations to simplify calculations; a more exact method manually would take too long.

Unlike a type–1 loop, a type–2 loop has two *true* integrators within the loop — a VCO and an integrator/filter after the phase detector. Replacing the integrator/filter with a passive–RC, low–pass filter results in the more common type–1 response, which doesn't have the phase coherence for step and velocity inputs between the two signal inputs to the phase comparator that the type–2 has.

Moreover, a third–order loop — the order is usually determined by the transfer function of the integrator/filter (F_S) — can reduce VCO noise substantially, without increasing reference–frequency sidebands in the output signal. These sidebands hamper simpler loop–circuit performance.

The transfer function of a generalized phase–lock loop can be represented as follows (Figure 2):

$$\frac{\theta_o\ (s)}{\theta_i\ (s)} = \frac{G_{(s)}}{1 + G_{(s)}H_{(s)}} \qquad (1)$$

where, from Figure

$$G(s) = (K_p)\ (F_{(s)})\ (K_V/s) \qquad (2)$$

and

$$H_{(s)} = 1/N \qquad (3)$$

The phase comparator transfer function is K_p and N is a digital counter/divider factor.

A typical integrator/filter built around an op amp (Figure 3) has a transfer function determined by the amplifier–circuit's closed–
loop gain,

$$A_{CL} = -\frac{Z_f}{Z_I},$$

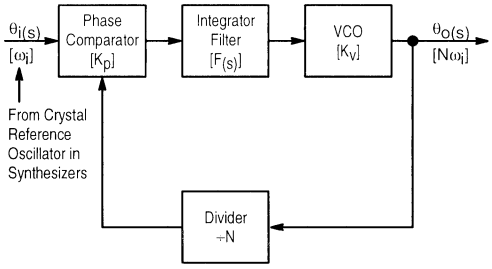

Figure 1. A type–2 phase–lock loop has two true integrators — the integrator/filter ($F_{(s)}$) and the VCO (K_V). Replacing the integrator/filter with a passive–RC network converts the circuit to a type–1 system.

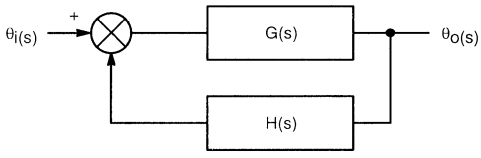

Figure 2. The phase–lock loop's generalized open–loop transfer function, G(s) H(s), has a third–order denominator — from which the circuit's name is derived.

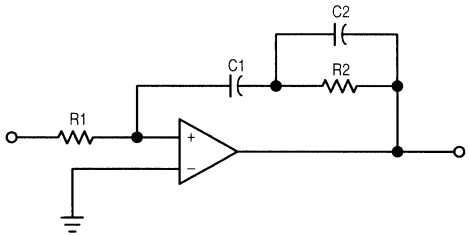

Figure 3. An integrator/filter circuit can be built with a wideband op amp and RC feedback network.

Andrzej B. Przedpelski, Vice President of Development, A.R.F. Products Inc., 2559 75th St., Boulder, CO 80301.

Table 1. Third order type–2 PLL

Display Line	Display Code	Key Entry	Remarks	Registers
00				R_0
01	1573	(g)π		
02	61	x		
03	02	2		R_1 T_1
04	61	x		
05	2307	STO7		
06	2403	RCL3		R_2 T_2
07	61	x		
08	01	1		
09	1509	(g) P		R_3 T_3
10	2304	STO4		
11	22	R↓		
12	2402	RCL2		R_4
13	2407	RCL7		
14	61	x		
15	32	CHS		R_5 $\frac{K_pK_v}{N}$
16	01	1		
17	32	CHS		
18	1509	(g) P		R_6
19	2404	RCL4		
20	71	÷		
21	2405	RCL5		R_7
22	61	x		
23	2401	RCL1		
24	71	÷		
25	2407	RCL7		
26	1502	(g) x^2		
27	71	÷		
28	2304	STO4		
29	1408	(f) log		
30	02	2		
31	00	0		
32	61	x	$\lvert G_{j\omega}H_{j\omega}\rvert$	
33	74	R/S		
34	22	R↓		
35	21	x≷y		
36	41	—	∠θ	
37	74	R/S		
38	2404	RCL4		
39	1409	(f) R		
40	01	1		
41	51	+		
42	1509	(g) P		
43	1522	(g) 1/x		
44	1408	(f) log		
45	02	2		
46	00	0	e/en	
47	61	x		
48	1300	GTO 00		
49				

where $Z_1 = R_1$ (4)

Z_f = impedance of feedback network

The transform of the feedback network is

$$Z_{f(s)} = \frac{s(C_1 + C_2) + \frac{1}{R_2}}{sC_1(sC_2 + \frac{1}{R_2})}, \quad (5)$$

and the integrator/filter transfer function is then

$$F(s) = -\frac{s(C_1 + C_2) + \frac{1}{R_2}}{C_1R_1(sC_2 + \frac{1}{R_2})}, \quad (6)$$

Multiply Equation 6 by R_2/R_2, then

$$F(s) = -\frac{s(C_1R_2 + C_2R_2) + 1}{sC_1R_1(sC_2R_2 + 1)}, \quad (7)$$

or

$$F(s) = -\frac{sT_2 + 1}{sT_1(sT_3 + 1)}, \quad (8)$$

where $T_1 = R_1C_1$

$T_2 = R_2(C_1 + C_2)$

$T_3 = R_2C_2$

The open–loop transfer function of Figure 2 is G(s) H(s); therefore, from Equations 2, 3 and 8

$$G_{(s)}H_{(s)} = \frac{s(T_2)(K_VK_P) + K_VK_P}{s^3NT_1T_3 + s^2NT_1} \quad (9)$$

Note the third–order denominator, from which the circuits name — third–order–loop — is derived. Note also the deletion of the minus sign: the circuit configuration (a phase inverter) provides the negative feedback. Both K_p and K_v are positive.

If you substitute jω for s in Equation 9, you can get the equation for plotting the magnitude and phase of the circuit's open–loop gain as a function of frequency:

$$G_{(j\omega)}H_{(j\omega)} = \frac{j\omega(T_2)(K_VK_P) + K_VK_P}{j\omega^3NT_1T_3 + \omega^2NT_1} \quad (10)$$

Step	Instructions		Input Data/ Units	Keys			Output Data/ Units
1	Enter program						
2	Store	T_1	R_1	ENTER			
			C_1	X	STO	1	
		T_2	C_1	ENTER			
			C_2	+			
			R_2	X	STO	2	
		T_3	R_2	ENTER			
			C_2	X	STO	3	
		$(K_pK_v)/N$	K_p	ENTER			
			K_v	X			
			N	=	STO	5	
3	Calculate		F	(f)	PRGM	R/S	$G_{J\omega}H_{J\omega}$
				R/S			∠θ
				R/S			(e/en)
4	Repeat step 3 for other values of frequency, F						

Table 2. Third order type–2 PLL

Frequency (Hz)	Open–Loop Response		Loop Response to VCO Noise (dB)
	dB	∠θ	
100	116.01	–179.94	–116.01
1000	76.01	–179.44	–76.01
10,000	36.06	–174.44	–35.92
94,650	0*	–139.85	3.27
100,000	–0.71	–138.58	3.30**
1,000,000	–26.25	–139.59	0.32
10,000,000	–63.21	–174.68	0.01

* Unity–gain point ** Maximum overshoot

A servo–loop damping factor that appears in lower–order loops is not defined in third–order loops. Instead you determine stability by the phase margin between –180° and the phase at a frequency where the gain is unity in the open–loop gain function, $G_{j\omega}H_{j\omega}$. The larger the phase margin, the more stable the system. A phase margin of about 45° produces an adequately damped loop. More than 45° means greater stability and, of course, the system may oscillate when the margin approaches zero.

Feedback also reduces noise

Not only does feedback determine the system's stability, but it also delineates its noise–output characteristics. When running free, the VCO is considerably more "noisy" than is the circuit's reference crystal oscillator. But the circuit's feedback loop substantially reduces the VCO's output–noise spectrum, especially, at low frequencies. This particular reduction is fortunate, because the VCO's noise output has 1/f characteristics: high–frequency noise tends to fall off without outside help, but the low frequency needs help.

An approximate expression for the loop's output phase noise is

$$\sqrt{[\,(|\,e/e_n|\,)(e_v)\,]^2 + [\,(N)(e_x)\,]^2}, \qquad (11)$$

where e_x = crystal oscillator noise
e_v = VCO noise
(e/e_n) = loop's response to VCO noise.

And the loop's response to the VCO noise is

$$(e/e_n) = \frac{1}{1 + G_{(s)}H_{(s)}}. \qquad (12)$$

Although $G_{(s)}H_{(s)}$ determined from Equation 9 is complex, only the magnitude of (e/e_n) from Equation 12 is used in Equation 11. Note: The greater the open–loop transfer function, $G_{(s)}H_{(s)}$, the smaller the (e/e_n), and the lower the loop's output noise. However, note also that the reference crystal oscillator's noise contribution is multiplied by the divider constant, N, though, hopefully, the crystal–oscillator noise is low.

In addition, you can get a check on the system's stability by plotting the loop's response to the VCO noise (e/e_n), obtained from Equation 12, versus frequency. You'll find that the curve has a high–pass response with a 12dB/octave slope. For best stability, any overshoot at the cutoff frequency should be less than 6dB. Of course, lower overshoot represents higher stability.

Clearly, the loop's mathematical analysis depends mainly upon calculation of $G_{(j\omega)}H_{(j\omega)}$ in Equation 10.

Now comes the program

To make the calculator program simpler, rewrite Equation 10 as follows:

$$G_{(j\omega)}H_{(j\omega)} = \frac{K_vK_p}{NT_1\omega^2}\left[\frac{-j\omega T_2 - 1}{j\omega T_3 + 1}\right] \qquad (13)$$

1 contains the program that solves Equation 13. It provides both the magnitude and phase angle, ∠θ, of the open–loop response, $G_{(j\omega)}H_{(j\omega)}$, given $T_1, T_2, T_3, K_pK_v/N$ and frequency, $f(\omega=2\pi f)$. The open–loop response magnitude is given in dB and its phase in degrees. Also, the magnitude of the loop's VCO noise response (Equation 12) is given in dB. If answers in dB aren't required, however, seven steps can be eliminated.

To see how the program works, consider a 960 MHz transmitter recently proposed for a Navy application. It calls for a phase–lock loop with the following characteristics to generate the 960 MHz:

$N = 64$
$R_1 = 10{,}000\Omega$
$C_1 = 4700 \times 10^{-12}F$
$R_2 = 330\Omega$
$C_2 = 470 \times 10^{-12}F$
$K_p = 0.25V/rad$
$K_v = 3 \times 10^9$ (rad/s)/V

The stable crystal–oscillator reference frequency used is 15MHz. The frequency divider and phase comparator are built with ECL logic. From the circuit component values and transfer constants we obtain:

$T_1 = 4.7 \times 10^{-5}s$
$T_2 = 1.706 \times 10^{-6}s$
$T_3 = 1.551 \times 10^{-7}s$
$(K_vK_p)/N = 11.72 \times 10^6/s$

The calculator program provided the results in 2. Note that the phase margin at unity gain corresponding to 94,650Hz is 40.15°; thus, the loop is fairly stable. Further, the loop's response to VCO noise shows a maximum overshoot of 3.30dB at 100,000Hz, which confirms the loop's stability (less than 6dB overshoot). If the phase margin is too small or you want overdamped loop operation, the program allows you to check the effects of parameter changes and get the performance you want, quickly. However, keep all additional circuit poles above the area of interest, since they reduce phase margin and stability. In addition, don't ignore the effects of stray capacitances. And use a high–gain op amp with a wide frequency response and a VCO with a wide modulation bandwidth. ■■

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4

Optimize phase–lock loops to meet your needs — or determine why you can't

The time constants of a PLL's integrator/filter are the keys to controlling a loop's performance. In the integrator/filter, you can trade off circuit parameters most easily to meet your needs. The other loop components (Figure 1) have simple, real–valued transfer functions (K_V, K_p, N) that can't be changed as easily. But the integrator/filter's transfer function (F_S), detailed in Figure 1c is the source of the high–order complex function in the following equation for open–loop gain:

$$G(j\omega)H(j\omega) = \frac{K_V K_p}{NT_1\omega^2}\left[\frac{-j\omega T_2 - 1}{j\omega T_3 + 1}\right] \quad (1)$$

where

T_1, T_2, T_3 = time constants defined in Figure 1c, seconds

K_p = phase–detector gain constant, volts/radian

K_V = voltage–controlled–oscillator (VCO) sensitivity, radians/second/volt

N = frequency divisor

ω = $(2\pi f)$ frequency, radians

Usually, K_p, K_V and N are given, but you can choose T_1, T_2 and T_3 to give you the loop performance you want. Generally, of course, you want the loop to be stable, to attenuate the reference frequency and to reduce VCO noise. But stability, being an absolute necessity, gets priority. The other two requirements, unfortunately, are inversely dependent and must be traded off against each other.

A damping factor to control stability as in simpler second–order loops can't be readily defined in the third–order loop of Figure 1. Instead, the phase margin — the difference between 180° and the phase of the open–loop transfer function, where the gain is one — becomes the criterion for stability. Figure 2 is a typical open–loop response curve showing both amplitude and phase response, and the phase margin.

In ED No. 10, May 10, 1978, p. 120, A. B. Przedpelski advised: "Analyze, don't estimate, phase–lock–loop performance." He showed how to calculate the performance of a given type–2, third–order PLL system with a 48–step program for an HP–25 programmable calculator. This article will show you how to optimize such a PLL to your requirements. But you will discover that you may not be able to get all requirements simultaneously. Compromises may be necessary.

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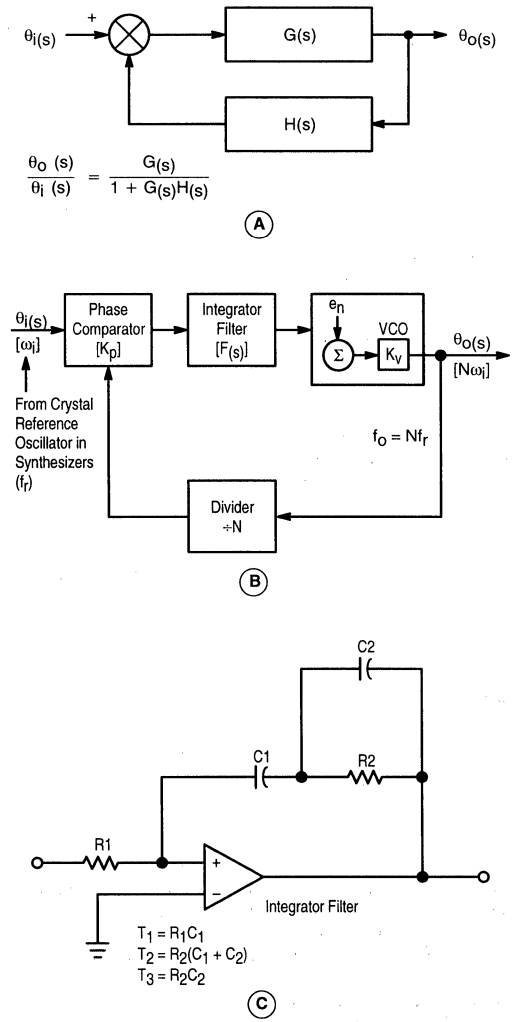

Figure 1. A phase–lock loop (a) with two integrators (b) is classified type 2. And the order — third, in this case — is established by the characteristics of the integrator/filter (c). Time constants T_1, T_2, and T_3 determine the integrator/ filter's detailed performance.

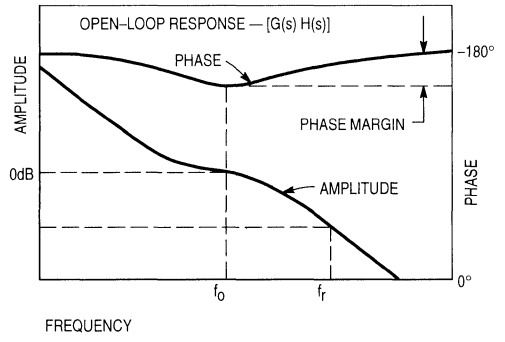

Figure 2. This open–loop gain/phase plot shows a typical phase displacement from –180°. When the frequency, f_o, which corresponds to 0dB gain, is made to align with the maximum phase displacement, calculating T_1, T_2 and T_3 is simplified.

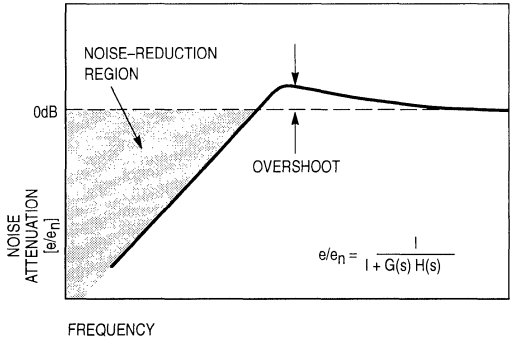

Figure 3. Increase f_o and you increase the noise–reduction region — the shaded area bounded by the 0dB line and the noise–attenuation curve.

The asymptotic slope of the amplitude curve is fixed at 40dB per octave by the loop's integrator/filter and VCO. The phase delay would be constant at –180°, except for the phase lead introduced at the middle frequencies by the transfer function F(s). This phase lead provides the phase margin that ensures loop stability.

45° — a good compromise

The phase margin should be between 30° and 70° for most applications. The larger the phase margin, the more stable the loop. But a large phase margin not only slows the response, it also increases output sidebands and reduces the loop's VCO–noise suppression capability. Thus, a phase margin of about 45° is a good compromise between desired stability and the other generally undesired effects.

Ideally, a phase comparator provides an error signal that is proportional to the phase difference between its two inputs, and nothing else. But in practice, some of the reference frequency, f_r, always leak through the comparator, which frequency modulates the output signal to produce undesirable sideband frequencies. Shifting the open–loop gain–amplitude curve of $G(j\omega)\,H(j\omega)$ Figure 2 to the left would attenuate f_r and the sidebands. But such a shift also would weaken the circuit's VCO–noise suppression capability.

A typical VCO noise–reduction plot is shown in Figure 3. Noise attenuates in the region that lies to the left of the curve and below the 0dB line (shown cross–hatched). The unity–gain frequency, f_o, defines the noise reduction: It's directly proportional to f_o. Clearly, then, shifting the $G(j\omega)\,H(j\omega)$ curve to the right by increasing f_o will also increase the VCO noise–reduction region — which is opposite the requirement for reducing the sidebands. Thus, as so often happens, you must compromise. Locate the point of minimum phase shift (inflection point of the phase response, Figure 2) exactly at f_o, the unity–gain value.

The inflection point is strategic

Locating f_o at the phase inflection point is strategically valuable, because it will help solve for the value of T_1. But first you must determine T_3. Accordingly, from Equation 1 the phase margin, ϕ, is

$$\phi = \tan^{-1}\omega T_2 - \tan^{-1}\omega T_3 + 180°. \qquad (2)$$

Differentiate ϕ with respect to ω and set the result equal to zero to locate ω_o, and the result is

$$\frac{d\phi}{d\omega} = \frac{T_2}{1 + (\omega T_2)^2} - \frac{T_3}{1 + (\omega T_3)^2} = 0 \qquad (3)$$

Solving Equation 3 then gives you

$$\omega_o = \frac{1}{\sqrt{T_2\,T_3}}. \qquad (4)$$

And substituting Equation 4 into Equation 2 gives you

$$\tan\phi = \frac{T_2 - T_3}{2\sqrt{T_2\,T_3}}. \qquad (5)$$

Finally, plug Equation 4 into Equation 5 and re–arrange to get

$$T_3 = \frac{\sec\phi - \tan\phi}{\omega_o}. \qquad (6)$$

Then re–arrange Equation 5 to get

$$T_2 = \frac{1}{\omega_o^2 T_3} \qquad (7)$$

Since you want the gain to be one at the phase–inflection point, solve for T_1 in Equation 1 with $G(j\omega)\,H(j\omega) = 1$; as a result,

$$T_1 = \frac{K_P K_V}{N\omega^2}\left[\frac{-j\omega T_2 - 1}{j\omega T_3 + 1}\right] \qquad (8)$$

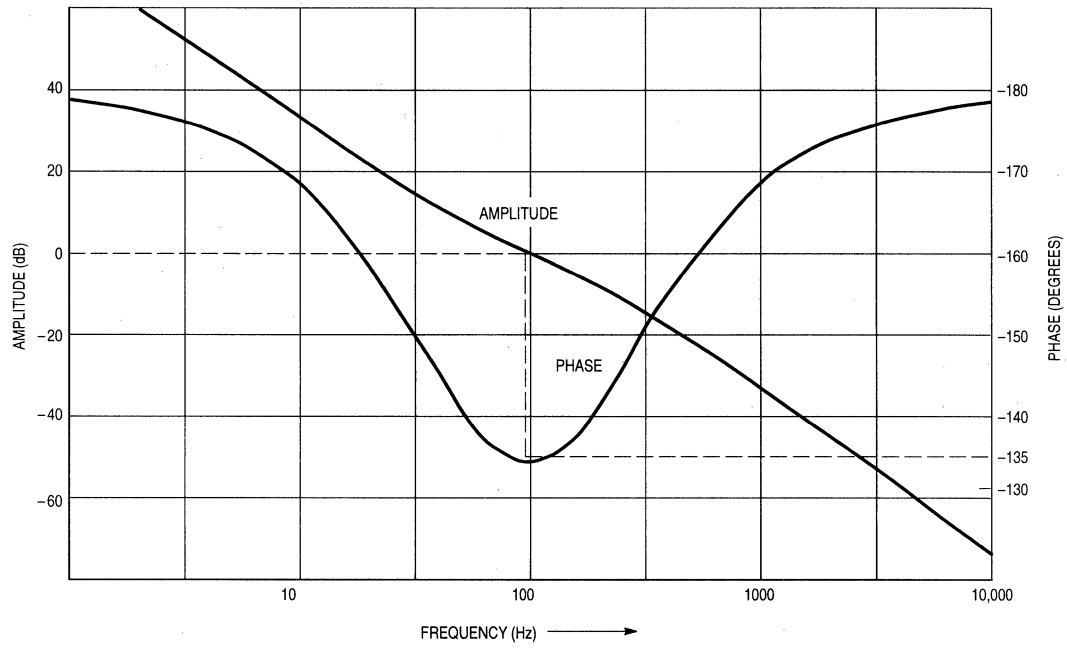

Figure 4. This plot of a PLL's open–loop transfer function confirms the design–parameter choices — a 45° phase margin at an f_O of 100Hz and unity gain. The loop is stable, but some adjustments may be desirable.

4

The 41 steps

The program in the table solves Equations 6, 7 and 8 in 41 steps with an HP–25 programmable calculator. Of course, the program can be adapted to other programmable calculators.

To illustrate the program's procedure, consider a PLL that must produce an output of 16.95MHz from a 5kHz reference, f_r. The phase comparator, VCO and divider transfer fuctions are as follows:

$$K_p = 0.19V/rad$$
$$K_v = 10.6 \times 10^6 \text{ rad/s/V}$$
$$N = 3390$$

For stability, start with a phase margin of 45° and an f_O of about 1/50 of f_r. Thus, with

$$\phi = 45°$$

and

$$f_O = 5000/50$$
$$= 100Hz,$$

calculate T_1, T_2 and T_3 with the program: You get

$$T_1 = 3.63 \times 10^{-3}s$$
$$T_2 = 3.84 \times 10^{-3}s$$
$$T_3 = 6.59 \times 10^{-4}s$$

But with those time constants you would need components with nonstandard values. However, if you select standard capacitors and resistors as follows:

$C_1 = 0.33\mu F$, $R_1 = 12k\Omega$
$C_2 = 0.068\mu F$, $R_2 = 10k\Omega$

you get the following time constants:

$$T_1 = 3.96 \times 10^{-3}s$$
$$T_2 = 3.98 \times 10^{-3}s$$
$$T_3 = 6.8 \times 10^{-4}s$$

which are close enough for a first try.

Verfying the results

To verify the results, the open–loop transfer function, $G_{(j\omega)}$ $H_{(j\omega)}$, and noise response, e/e_n, were calculated with the program provided in the previous article and plotted in Figure 4 and Figure 5. The curves confirm that the design is stable with a maximum phase margin of 45° at a frequency

Display		Key Entry	Remarks	Registers
Line	Code			
00				R_0
01	2407	RCL7		
02	1406	(f) tan		
03	32	CHS		R_1
04	2407	RCL7		
05	1405	(f) cos		
06	1522	(g) 1/x		R_2
07	51	+		
08	2406	RCL6		
09	1573	(g) π		R_3
10	61	x		
11	02	2		
12	61	x		R_4
13	2304	STO4		
14	71	÷		
15	2303	STO3	3	R_5 $\frac{K_pK_v}{N}$
16	74	R/S		
17	2404	RCL4		
18	1502	(g) x^2		R_6 f_o
19	61	x		
20	1522	(g) 1/x		
21	2302	STO2	T_2	R_7 ϕ
22	74	R/S		
23	2404	RCL4		
24	61	x		
25	01	1		
26	1509	(g) P		
27	2403	RCL3		
28	2404	RCL4		
29	61	x		
30	01	1		
31	1509	(g) P		
32	21	x≷y		
33	22	R↓		
34	71	÷		
35	2404	RCL4		
36	1502	(g) x^2		
37	71	÷		
38	2405	RCL5		
39	61	x		
40	2301	STO1	T_1	
41	1300	GTO 00		

Step	Instructions	Input Data/ Units	Keys			Output Data/ Units
1	Enter program					
2	Store	f_o	STO	6		
		ϕ	STO	7		
		K_p	ENTER			
		K_v	X			
		N	:	STO	5	
3	Calculate		(f)	PRGM	R/S	T_3
			R/S			T_2
			R/S			T_1
3	Recall		RCL	1		T_1
	(if desired)		RCL	2		T_2
			RCL	3		T_3
			RCL	4		o

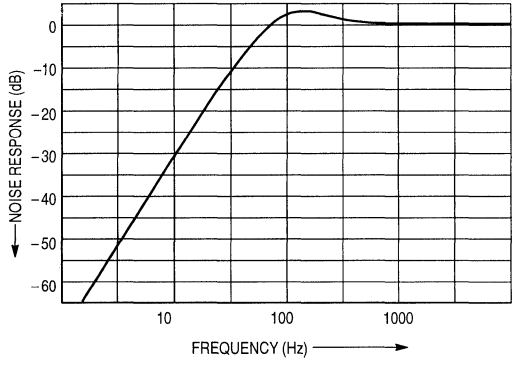

Figure 5. The noise response calculation corresponding to Figure 4 shows that VCO noise is attenuated below about 70Hz.

where the open–loop gain is about unity. And the VCO noise–reduction curve shows a moderate 3.2dB overshoot with noise frequencies below about 70Hz in the attenuation region.

Still, adjustments may be desired. For instance, if you want more reference–frequency (f_r) attenuation, the $G_{(j\omega)}$ $H_{(j\omega)}$ curve can be shifted to the left. Move f_o one decade (to about 10Hz) and you'll increase the f_r attenuation by 40dB. Or, if noise frequencies above 70Hz are bothersome, you can shift the $G_{(j\omega)}$ $H_{(j\omega)}$ curve to the right by increasing f_o.

If you still aren't satisfied, you can change the phase margin. Reduce the margin and you improve both f_r and VCO–noise attenuation — but then you loose some stability. ■■

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Suppress phase–lock–loop sidebands without introducing instability

Phase–lock–loops: Part Three

The first two parts of this series showed how to analyze and then optimize type–2, third–order PLL systems and provided simple calculator programs for an HP–25 to do the otherwise tedious computations.[1,2] This article takes you a step further and shows how to suppress sidebands, especially undesired when the PLL is used in frequency–synthesis systems.

Frequency synthesis, a major application of the phase–lock loop (PLL), always involves PLL–performance compromise: keeping loop bandwidth as wide as possible to reduce acquisition time and voltage–controlled oscillator noise, and at the same time suppressing reference–frequency sidebands that can pass through wide bandwidths (Figure 1).

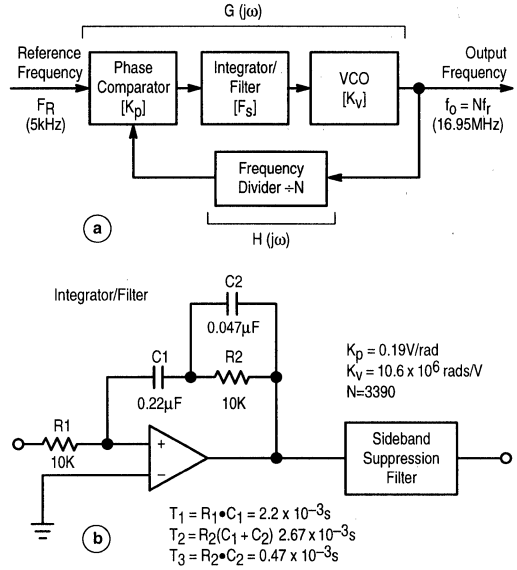
Fortunately, reference frequency is considerably above the required loop bandwidth in most cases, which alleviates the sideband problem to some extent. But for heavy suppression of undesired sidebands, extra filtering is necessary. However, it must be done carefully so as not to introduce loop instability. Three filtering circuits, none of which reduce bandwidth or VCO–noise attenuation can help solve the problem. In fact, an active LP–filtering technique, the most versatile and efficient of the three, is programmed on an HP–25 to speed the design.

All methods assume the the PLL, a type–2 third–order loop,[1] meets all requirements[2] except adequate reference–frequency sideband suppression. The three approaches include RC, active–notch and active–LP filtering. The PLL's phase margin serves as a measure of loop stability, since the damping–factor concept isn't applicable to third–order loops:[2] phase margins between 30° and 45° are minimum criteria for stable operation. And the filter's action in reducing the feedforward gain, $G_{(j\omega)}$, at the sideband frequencies is the criterion for the suppression effectiveness.

Since $H_{(j\omega)}$ is equal to 1/N, a constant, then the open–loop gain, $G_{(j\omega)}\,H_{(j\omega)}$ in Equation 1, can be used as a measure of this sideband–suppression effectiveness:

$$G_{(j\omega)}H_{(j\omega)} = \frac{K_V K_P}{NT_1\omega^2}\left[\frac{-j\omega T_2 - 1}{j\omega T_3 + 1}\right], \quad (1)$$

K_P = gain constant of the phase detector,
K_V = VCO sensitivity,
N = counter divide ratio,
T_1, T_2, T_3 = integrator/filter time constants.



NOTE: Similar to example in Phase–lock Loops: Part Two (ED 19, Sept. 13, 1978, p/ 134) only time constants T_1, T_2 and T_3 have been changed, to improve margin and over–all performance.

Figure 1. A phase–lock loop frequency synthesizer (a) generates 16.95MHz from a crystal–oscillator reference frequency of 5kHz. To help suppress sidebands, a sideband–suppression filter is added in tandem with the output of the loop's original integrator/filter circuit (b).

Table 1. Filter suppression/phase margin tradeoffs

Circuit	Phase Margin	Phase Margin Deterio–ration	First Sideband Reduction	Second Sideband Reduction
Original	44°	—	—	—
RC low–pass RC = 3 x 10^{-4}	32	12°	20dB	26dB
Notch filter				
Q = 10	44	0	∞*	0
Q = 1	43	1	∞*	1.5
Q = 0.1	31	13	∞*	16.5
Second–order active				
d = 0.707	34	10	28	40
d = 0.1	42	2	28	40

*Theoretical — actual value about 40dB

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Table 2. Third order type–2 PLL with two–pole low–pass filter

Display Line	Display Code	Key Entry	Remarks	Registers
00				R_0 ω_0
01	2400	RCL0		
02	1502	(g) X^2		
03	2407	RCL7		R_1 T_1
04	1502	(g) x^2		
05	41	—		
06	2304	STO4		R_2 T_2
07	2403	RCL3		
08	61	x		
09	2406	RCL6		R_3 T_3
10	2400	RCL0		
11	61	x		
12	51	+		R_4
13	2407	RCL7		
14	61	x		
15	2404	RCL4		R_5 $\frac{K_pK_v}{N}$
16	2406	RCL6		
17	2403	RCL3		
18	61	x		R_6 2d
19	2400	RCL0		
20	61	x		
21	2407	RCL7		R_7 ω
22	1502	(g) x^2		
23	61	x		
24	41	—		
25	32	CHS		
26	1509	(g) P		
27	21	x⇆y		
28	2407	RCL7		
29	2402	RCL2		
30	61	x		
31	32	CHS		
32	01	1		
33	32	CHS		
34	1500	(g) P		
35	22	R↓		
36	51	+	∠° Phase–margin	
37	74	R/S		
38	22	R↓		
39	71	÷		
40	2405	RCL5		
41	61	x		
42	2401	RCL1		
43	71	÷		
44	2407	RCL7		
45	1502	(g) x^2		
46	71	÷		
47	2400	RCL0		
48	1502	(g) x^2		
49	61	x	$\lvert G_sH_s \rvert$	

Step	Instructions	Input Data/ Units	Keys			Output Data/ Units
1	Enter program					
2	Store	ω_o	STO	0		
		T_1	STO	1		
		T_2	STO	2		
		T_3	STO	3		
		K_v	ENTER			
		K_p	×			
		N	÷	STO	5	
		d	ENTER	2	×	
			STO	6		
3	Enter		STO	7		
4	Calculate		(f)	PRGM	R/S	∠°Phase
			R/S			margin
5	Repeat step 3					|G(s) H(s)|
	for other values					
	of frequency, F					

Simple but limited

The simplest approach adds in series with the Integrator/ Filter an RC low–pass section (Figure 2a), whose cutoff frquency is larger than the upper end of the loop's bandwidth. For illustration, let the value of RC be 3 x 10^{-4}s for the frequency–synthesizer example outlined in Figure 1. (A larger value would reduce the sidebands more, but would also decrease the phase margin too much.) With a value of 3 x 10^{-4}s, the phase margin remains within a "safe" 30°–to–45°.

The open–loop transfer function then becomes:

$$G(j\omega)H(j\omega) = \frac{K_vK_p}{NT_1\omega^2}\left[\frac{-j\omega T_2 - 1}{j\omega(T_3 + T_4) + 1 + \omega^2T_3T_4}\right], \quad (2)$$

where T_4 is the additional RC time constant.

Solving Equation 1 at frequencies of 5 and 10kHz shows that the first sideband (at 5kHz) is reduced a respectable 20dB and the second sideband (at 10kHz) even more to 26dB. But the phase margin is also reduced to a marginal 32° (1).

However, an active RC notch filter[3] (Figure 2) gives much more attenuation at the first sideband (5kHz) and is more flexible in some applications. Its gain is

$$A(j\omega) = \frac{1}{j\omega\left[\frac{w_\omega}{Q(\omega^2 - \omega_o^2)}\right] + 1}, \quad (3)$$

where ω_o = the notch frequency ($2\pi f_o$),
Q = the circuit Q.

The open–loop transfer function, the product of Equations 1 and 3, is

$$G(j\omega)H(j\omega) = \frac{K_vK_p}{NT_1\omega^2} \times \left[\frac{-j\omega T_2 - 1}{j\omega\left(T_3 - \frac{\omega_o}{Q(\omega^2 - \omega_o^2)}\right) + \omega^2T_3\left(\frac{\omega_o}{Q(\omega^2 - \omega_o^2)}\right) + 1}\right], \quad (4)$$

Although the notch frequency ω_o must be fixed at the reference frequency, the value of Q can vary. Theoretically, the reference frequency receives infinite attenuation. Actually, only about 40dB can be realized, even under ideal

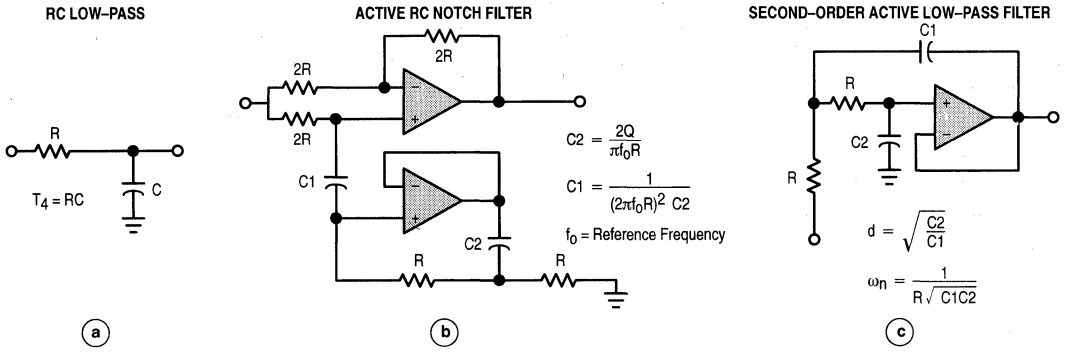

Figure 2. Many filter configurations can be used to supress sidebands. The simplest is a low–pass RC circuit (a). Somewhat more flexible is an active RC notch filter (b). But of all filters, a second–order active low–pass filter (c) is most versatile, since two of its parameters are independently adjustable.

conditions. Evaluation of Equation 4 for Q's of 10, 1 and 0.1 shows that high Q values produce negligible phase–margin deterioration, but attenuation of the second harmonic of the reference frequency is small or zero (1). At a Q of 0.1, however, the second harmonic is reduced 16.5dB, but then the phase margin suffers.

Most versatile, however, is a second–order, active, low–pass filter with variable damping (Figure 2c). Its gain (with "s" functions of its more familiar form replaced by jω) is:[3]

$$A(j\omega) = \frac{\omega_n^2}{-\omega^2 + 2dj\omega\omega_n + \omega_n^2}, \qquad (5)$$

where ω_n = the filter's natural pole frequency,
d = the filter's damping factor.

This time, multiplying Equations 1 and 5, the overall open–loop transfer function bcomes

$$G(j\omega)H(j\omega) = \frac{K_V K_P}{NT_1\omega^2} \times \left[\frac{-j\omega T_2 - 1}{j\omega[2d\omega_n + T_3(\omega_n^2 - \omega)] + [\omega_n^2 - \omega^2 - 2dT_3\omega_n\omega^2]}\right], \qquad (6)$$

If ω_n is chosen to be 6283 ($2\pi \times 1000$) at damping factors of 0.707 (Butterworth response) and 0.1 (16dB peak Chebyshev), Equation 6 gives the same sideband attenuation for both damping factors, but the high–ripple Chebyshev deteriorates the phase margin least (1 and Figure 3).

Since both the pole frequency and the damping factor can be varied in Equation 5, the circuit it represents is most versatile. Therefore, Equation 6 is programmed for easy solution on an HP–25 (2) in 49 steps. However, for easier stability evaluation, the program solves directly for the phase margin — the difference between 180° and the open–loop transfer–function angle — rather than the phase angle itself.

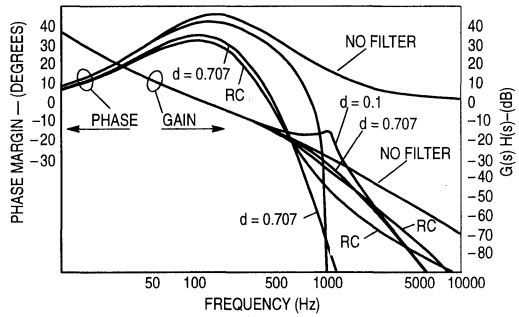

Figure 3. A plot of open–loop gain and phase response of the system in Figure 1 compares sideband suppression at 5 and 10kHz without and extra filter with that of a simple RC and an active, second–order filter.

Clearly, the simple RC circuit is least effecient. It gives the least sideband attenuation andthe largest phase–margin deterioration. The notch filter, although theoretically capable of very high attenuation of the sidebands only with very small phase–margin deterioration, generally requires component tolerances too critcal for other than some special applications. The more complex, active, second–order low–pass filter, however, can be tailored to most applications — illustrating an often observed design phenomenon: the more complex the circuit the better the performance. Of course, then, more complex filter circuits than those used in the examples may offer even better solutions to sideband reduction. ■ ■

References

1 Przedpelski, A. B., "Analyze, Don't Estimate, Phase–lock–loop Performance of Type–2, Third–order Systems," *Electronic Design*, May 10, 1978, p. 120.

2 Przedpelski, A. B., "Optimize Phase–lock Loops to Meet Your Needs," *Electronic Design*, Sept. 13, 1978, p. 134.

3 Stout, D. F., and Kaufman, M., *Operational Amplifier Circuit Design*, McGraw–Hill, NY, 1976.

Calculate the noise spectral density and short–term frequency stability in a PLL with a programmable calculator, and vary the parameters to trade off the noise/functional performance requirements.

Programmable calculator computes PLL noise, stability

This article is the fourth by the author on phase locked loops, starting with "Analyze, Don't Estimate, Phase–Lock–Loop Performance" (May 10, 1978, p. 120); then "Optimize Phase–Lock–Loops to Meet Your Needs" (Sept. 13, 1978, p. 134); followed by "Suppress Phase–Lock–Loop Sidebands without Introducing Instability" (Sept. 13, 1979, p. 142).

The circuit constants of a phase–lock loop can be optimized not only for performance requirements (acquisition time, sideband levels, step response, and stability, among others), but also for noise output and the resulting short–term (or "instantaneous") frequency stability. Because most other frequency generation methods lack this versatile performance and noise and stability control, phase–lock loops (PLLs) are preferable for frequency synthesis. Moreover, a programmable HP–19C (or 21C) calculator with the proper program makes the design tradeoffs between noise effects and functional performance requirements relatively easy to determine.

A properly designed frequency synthesizer derived from a PLL (Figure 1, top) will offer a high degree of flexibility and long–term frequency stability. In a PLL, the frequency of the stable reference oscillator (say, a quartz–crystal circuit) can be multiplied by a precisely controlled factor over a very wide range. Although the PLL may seem more complicated than the conventional so–called frequency–multiplier circuit (Figure 1, bottom), in practice, the PLL is more efficient, more compact, and considerably wider in bandwidth. All the advantages increase as the multiplication factor increases.

In most PLL frequency synthesizers, the primary concern is the functional performance–a problem that has been treated extensively.[1] Even the theoretical aspects of phase noise in low–noise signal sources have been extensively covered.[2,3,4] However, specific methods for calculating the noise and short term frequency stability and details of the tradeoffs are generally not available, except for some recent work by the National Bureau of Standards on low noise signal sources.[5,6,7]

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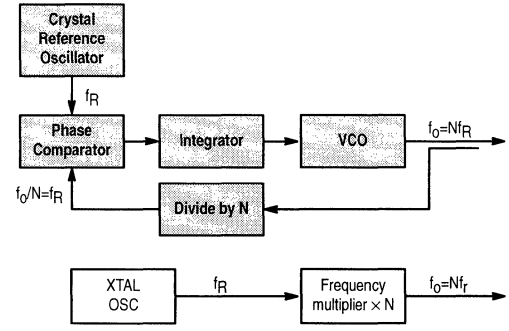

PLL and conventional frequency multiplier

Figure 1. Although the PLL frequency multiplier (top) looks more complex than the conventional multiplier (bottom), it is in fact more compact and more flexible, and can handle a much wider frequency range.

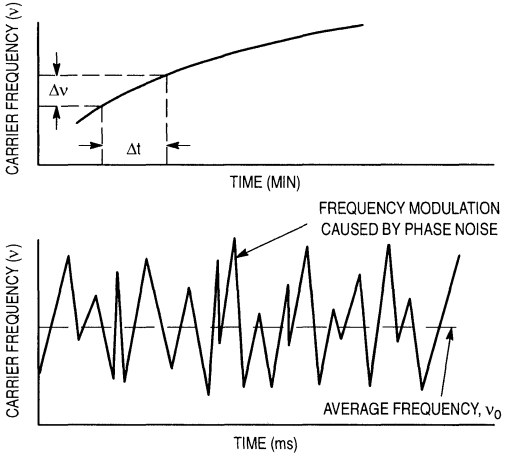

Figure 2. Short–term frequency stability can be far worse (bottom) than the long–term average of a PLL system (top).

Short–term (or "instantaneously" sampled) frequency stability, in the millisecond range, is particularly important for accuracy in position–finding applications, as in LORAN navigation and various radar and sonar Doppler systems. Even though frequency drift over a short time generally is less than the average long–term frequency drift, instantaneously measured samples show much wider variations in the frequency swings caused by phase noise in the signal source (Figure 2).

The overall phase–noise, or spectral–density output, $S_{\phi(\omega)0}$, of a PLL[8] is found by

$$S_{\phi(\omega)0} = S_{\phi(\omega)VCO}\left|\frac{1}{1 + G(\omega)H(\omega)}\right|^2 + S_{\phi(\omega)REF}\left|\frac{G(\omega)}{1 + G(\omega)H(\omega)}\right|^2,$$

where $S_{\phi(\omega)VCO}$ is the open–loop spectral density of phase fluctuations in the PLL's voltage–controlled oscillator (VCO) and $S_{\phi(\omega)REF}$ is the equivalent spectral density of fluctuations in the reference oscillator. These phase fluctuations are measured in rad^2/Hz, but generally plotted in dBc, which is $10\log_{10} S_{\phi(\omega)}$. More commonly, however, vendor–supplied phase–noise data, designated $\mathcal{L}(\omega)$, and also measured in dBc, are for single–sideband noise. (The dBc designation is defined as $10\log_{10}$ of the ratio between the output from a spectrum analyzer with a 1–Hz bandwidth and the signal's carrier level.)

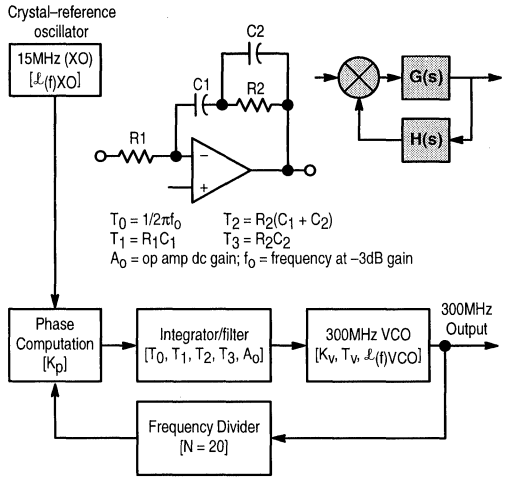

Figure 3. For a fifth–order PLL, four of the time constants are determined by the integrator/filter circuit, and the fifth is determined by the VCO.

Accordingly,

$$\mathcal{L}(\omega) = 10\log_{10}(1/2)S_{\phi(\omega)} \text{ (per rad}^2\text{)},$$

assuming that

$$\mathcal{L}(-\omega) = \mathcal{L}(\omega).$$

Therefore, to convert $\mathcal{L}(\omega)$ data to "straight" $S_{\phi(\omega)}$, data, add 3dB to the $\mathcal{L}(\omega)$ data and take the antilog.

An HP–19C program (see "Noise in a 5th–order PLL") calculates this single–sideband noise, where $G(\omega)H(\omega)$ is the open–loop gain of the PLL[1]. The feedback path, $H(\omega)$, is simply 1/N; and $G(\omega)$ equals

$$\frac{(K_pK_V/\omega T_1)\,(jwT_2 + 1)}{j\left[\omega^2(\omega^2\frac{T_0}{A_0}T_VT_3 - T_3 - T_V) + \frac{1}{A_0T_1}\right] + \omega(\omega^2T_VT_3 - 1)}$$

Optimized for functional performance, the following circuit constants are used for a typical PLL (Figure 3):

$A_0 = 320{,}000$
$T_0 = 7.96 \times 10^{-4}$s
$T_V = 1.59 \times 10^{-7}$s
$T_1 = 2.408 \times 10^{-5}$s
$T_2 = 2.491 \times 10^{-6}$s
$T_3 = 4.700 \times 10^{-7}$s
$K_p = 314 \times 10^6$ V/rad
$K_V = 0.16$ rad/V
$N = 20$

The single–sideband phase noise, when calculated by the program for a range of so–called Fourier frequencies (offsets from a carrier, $f = \omega/2\pi$), can be plotted as in Figure 4 (dotted line). Although this output phase noise can be reduced by varying circuit constants to increase the loop's bandwidth, proceed with caution, because other desirable operating characteristics (such as circuit stability or speed of response) could be compromised. The program, however, offers an easy way to determine how systematic changes in the parameters affect noise.

Oscillator noise should be low

In addition to the calculated PLL noise, Figure 4 shows a plot of the SSB–noise characteristics of the circuit's VCO and crystal–reference oscillator. The oscillators are the main source of phase noise in a PLL. The information for plotting their noise can be obtained from the manufacturers of the oscillators, or from measurements made by the user.

Where noise reduction is of prime importance select oscillators that generate minimum noise and have noise spectral densities that complement each other (as in Figure 5). The point at which the two curves cross is called the crossover frequency (f_C) This frequency is an important parameter for optimizing a PLL's noise characteristics.

In Figure 5, the VCO noise–distribution plot is divided into three characteristic regions. High–quality oscillators generally exhibit this spectral–density relationship. In region I, $S_{\phi(f)}$ is typically proportional to $1/f^3$, so–called flicker–frequency noise; in region II, $S_{\phi(f)}$ is proportional to $1/f^2$, so–called white–frequency noise; and in region III, $S_{\phi(c)}$ is constant, so–called white–phase noise. Beyond region III, the bandwidth limitation of the circuit attenuates the noise to negligible levels.

Noise in 5th order PLL

Step	Instructions	Input Data/Units	Keys	Output Data/Units
1	Enter program			
2	Store	T_0	STO 0	
		T_1	STO 1	
		T_2	STO 2	
		T_3	STO 3	
		T_v	STO 4	
		K_p	STO 5	
		K_{vo}	STO 6	
		N	STO 7	
		A_o	STO 8	
		180	STO 9	
		10	STO .5	
3	Calculate	f	GSB 0	
		$S\phi_{ref}$	R/S	
		$S\phi_{vto}$	R/S	
4	Repeat step 3 for other Fourier frequencies			$S\phi o$

NOTE: Enter $S\phi_{ref}$ and $S\phi_{vto}$ in dB. $S\phi o$ answer is in dB.

Step	Key Entry	Key Code	Step	Key Entry	Key Code
001	(g) LBL 0	25 14 00	050	RCL 9	55 09
002	PRx	65	051	—	31
003	(g) DEG	25 24	052	STO .1	45 .1
004	(g) π	25 63	053	R↓	12
005	×	51	054	÷	61
006	2	02	055	RCL 5	55 05
007	×	51	056	×	51
008	STO .0	45 .0	057	RCL 6	55 06
009	(g) x^2	25 53	058	×	51
010	RCL 0	55 00	059	RCL 7	55 07
011	×	51	060	÷	61
012	RCL 8	55 08	061	RCL 1	55 01
013	÷	61	062	÷	61
014	RCL 4	55 04	063	RCL .0	55 .0
015	×	51	064	÷	61
016	RCL 3	55 03	065	STO .2	45 .2
017	×	51	066	RCL .1	55 .1
018	RCL 3	55 03	067	x ⇆ y	11
019	—	31	068	(f) R	16 34
020	RCL 4	55 04	069	1	01
021	—	31	070	÷	41
022	RCL .0	55 .0	071	(g) P	25 34
023	(g) x^2	25 53	072	(g) 1/x	25 64
024	×	51	073	STO .3	45 .3
025	RCL 8	55 08	074	RCL .2	55 .2
026	RCL 1	55 01	075	RCL 7	55 07
027	×	51	076	×	51
028	(g) 1/x	25 64	077	×	51
029	÷	41	078	STO .4	45 .4
030	RCL .0	55 .0	079	(g) x^2	25 53
031	(g) x^2	25 53	080	R/S	64
032	RCL 3	55 03	081	RCL .5	55 .5
033	×	51	082	÷	61
034	RCL 4	55 04	083	(g) 10^x	25 33
035	×	51	084	×	51
036	1	01	085	RCL .3	55 .3
037	—	31	086	(g) x^2	25 53
038	RCL .0	55 .0	087	R/S	64
039	×	51	088	RCL .5	55 .5
040	CHS	22	089	÷	61
041	(g) P	25 34	090	(g) 10^x	25 33
042	x ⇆ y	11	091	×	51
043	RCL 2	55 02	092	÷	41
044	RCL .0	55 .0	093	(f) log	16 33
045	×	51	094	RCL .5	55 .5
046	1	01	095	x	51
047	(g) P	25 34	096	PRx	65
048	R↓	12	097	(g) SPC	25 65
049	÷	41	098	(g) RTN	25 13

REGISTERS

0 T_0	1 T_1	2 T_2	3 T_3	4 T_v	5 K_p	6 K_{vo}	7 N	8 A_o	9 180
S0	S1	S2	S3	S4	.5 10	S6	S7	S8	S9

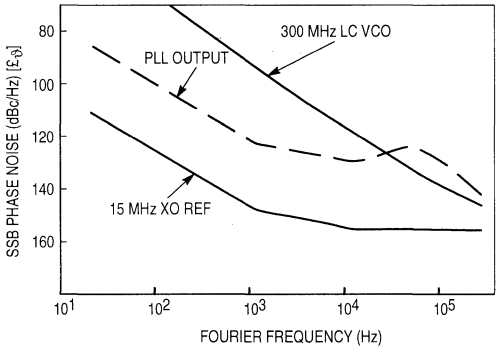

Figure 4. A PLL is optimized for performance characteristics, such as stability, response time, and sideband levels; but the noise characteristics generally fall where they may, as exemplified in this plot of a fifth–order PLL.

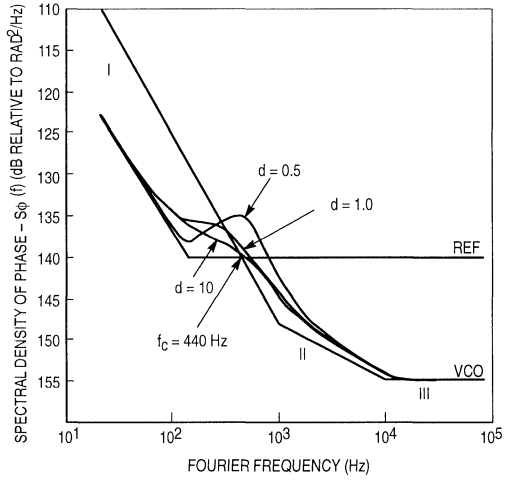

Figure 5. The "optimum" PLL output–noise characteristic is the one that coincides with the PLL's intersecting reference crystal oscillator and VCO–oscillator noise characteristics (heavy lines). A high damping–factor value (such as d=10) makes the best correspondence with this criterion.

Region I noise stems from fluctuations in oscillator–circuit frequency–control components; region II, from thermal noise in the oscillator's gain element; and region III, from additive thermal noise from other elements of the circuit (including the gain element).

A plot of the optimum phase–noise characteristic of a PLL would coincide with the lower parts of the two oscillator curves (heavy lines in Figure 5).

The type–2, second–order PLL circuit in Figure 6 helps to illustrate how closely this condition can be approached. This circuit can be generalized by relating the integrator's time constants (T_1 and T_2) and the VCO's and phase comparator's transfer coefficients (K_V and K_p) with a damping factor (d), and with the reference and VCO crossover frequency ($f_c = \omega_c/2\pi$), as follows:

$$d = (T/2)\sqrt{K_pK_V/T_1};\ d \gg 1$$
$$T_2 = 4d^2/\omega_c$$
$$T_1 = T_2K_pK_V/\omega_c.$$

When these circuit parameters are considered together with the circuit's open–loop gain (note: $H(\omega) = 1$),

$$G(j\omega)H(j\omega) = \frac{K_VK_p}{T_1\omega^2}\ (-j\omega T_2 - 1),$$

and substituted in the phase–noise equation for $S_\phi(\omega)0$ the PLL's spectral density becomes

$$S_\phi(\omega)0 = S_\phi(\omega)VCO\left[\frac{1}{\left(1-\frac{\omega_c^2}{4d^2\omega^2}\right)+\left(\frac{\omega_c^2}{\omega}\right)}\right] +$$

$$S_\phi(\omega)REF\left[\frac{\left(\frac{1}{2d}\right)^2\left(\frac{\omega_c}{\omega}\right)^2+\left(\frac{\omega_c}{\omega}\right)^2}{\left(1-\frac{\omega_c^2}{4d^2\omega^2}\right)+\left(\frac{\omega_c}{\omega}\right)^2}\right]$$

The "Optimizing PLL Phase Noise" program, with its subroutine 0, solves this equation for any Fourier frequency ($f = \omega/2\pi$). In Figure 5, solutions are shown for damping–factor values (d) of 0.5, 1.0, and 10.

The largest damping factor (d = 10) causes the noise curve to approach the "optimum" noise characteristic most closely–when it lies completely between the VCO/reference– oscillator lines and as closely as possible to the lower lines. To satisfy this criterion, the curve generally passes through the frequency crossover point previously mentioned. Larger damping values than 10 will provide little further improvement. In fact, a larger damping value would slow response more than it would lower the noise output. Special cases may require low damping factors — a value of 1 or even 0.5 — to get a faster response or the special noise–distribution shapes that these lower damping factors produce.

After the phase–noise characteristics (based on the fc of the oscillators and a selected damping factor) have been calculated, a second part of the optimizing program (subroutine 1) can then be used to calculate the time constants T_1 and T_2 for the given K_p and K_V of a type–2 second–order PLL.

Determining a PLL's short–term frequency stability requires integration of the spectral density of the phase fluctuations to obtain the so–called Allan variance (a dimensionless measure of stability, where σ_y^2 is f,f in a short sample period). Thus

$$\sigma_y^2(\tau, f_h) = \frac{2}{(\tau\upsilon\pi)^2}\int_0^{f_n} S_\phi(f)\sin^4(\pi f\tau)df,$$

Optimizing PLL phase noise

Step	Instructions	Input Data/Units	Keys	Output Data/Units
1	Enter program			
2	Store	fc	STO 2	
		d	STO 3	
		K_p	STO 7	
		K_v	STO 8	
3	Calculate phase noise	f	GSB 0	
		$S\phi_{vco}$	R/S	
		$S\phi_{ref}$	R/S	$S\phi_o$
4	Repeat step 3 for other values of Fourier frequency			
5	Calculate time constants		GSB 1	T1
				T2

NOTE: $S\phi_{vco}$, $S\phi_{ref}$ and $S\phi_o$ in dB. Subroutine 0 must be performed before the time constants can be calculated with subroutine 1

Step	Key Entry	Key Code	Step	Key Entry	Key Code
001	(g) LBL 0	25 14 00	038	(g) x^2	25 53
002	PRx	65	039	RCL 4	55 04
003	(g) π	25 63	040	÷	41
004	×	51	041	RCL 5	55 05
005	2	02	042	÷	61
006	×	51	043	R/S	64
007	(g) 1/x	25 64	044	1	01
008	RCL 2	55 02	045	0	00
009	(g) π	25 63	046	÷	61
010	×	51	047	(g) 10^x	25 33
011	2	02	048	×	51
012	×	51	049	÷	41
013	STO 1	45 01	050	(f) log	16 33
014	×	51	051	1	01
015	(g) x^2	25 53	052	0	00
016	STO 4	45 04	053	×	51
017	RCL 3	55 03	054	PRx	65
018	(g) x^2	25 53	055	(g) SPC	25 65
019	÷	61	056	(g) RTN	25 13
020	4	04	057	(g) LBL 1	25 14 01
021	÷	61	058	RCL 3	55 03
022	STO 6	45 06	059	(g) x^2	25 53
023	CHS	22	060	4	04
024	1	01	061	×	51
025	÷	41	062	RCL 1	55 01
026	(g) x^2	25 53	063	÷	61
027	RCL 4	55 04	064	PRx	65
028	÷	41	065	RCL 7	55 07
029	STO 5	45 05	066	×	51
030	(g) 1/x	25 64	067	RCL 8	55 08
031	R/S	64	068	×	51
032	1	01	069	RCL 1	55 01
033	0	00	070	÷	61
034	÷	61	071	PRx	65
035	(g) 10^x	25 33	072	(g) SPC	25 65
036	×	51	073	(g) RTN	25 13
037	RCL 6	55 06			

REGISTERS

0	1	2 f_c	3 d	4	5	6	7 K_p	8 K_v	9

where τ is the sampling time (in seconds), υ is the long–term average frequency (in Hz), and f_h is the bandwidth, or maximum excursion of the offset from the carrier (the maximum Fourier frequency).

Figure 7 (top) shows the relationship between frequency or phase and the frequency spectral–noise densities, along with the resultant short–term frequency stabilities, for several distinct types of phase or frequency noise. A typical complex signal source such as a PLL) could have a combined short–term frequency stability as in Figure 7 (bottom). But such noise types generally do not obey simple integer–power curves and, therefore, pose a problem: The Allan equation does not have a closed–form solution for fractional powers, so it cannot be used directly. Nevertheless, very accurate answers can be obtained with Simpson's Rule and a programmable calculator.

Although the Allan equation requires integration over the Fourier frequency range of 0 to f_h, the low–frequency limit of 0Hz cannot be used in a log–log Simpson's Rule integration. Fortunately, frequencies below $(2\pi\tau_h)^{-1}$, where τ_h is the longest sampling time, do not contribute appreciably to the value of the Allan variance. The longest sampling time for short–term effects is generally 1s; therefore, for a measuring–system bandwidth of 1000Hz, just the Fourier frequencies between about 0.16 and an f_h of 1000Hz need be considered. (Since the manufacturer did not supply data below 2Hz for the reference oscillator and VCO used in Figure 5; a new oscillator with data to 0.1Hz was substituted in Figure 8, top.)

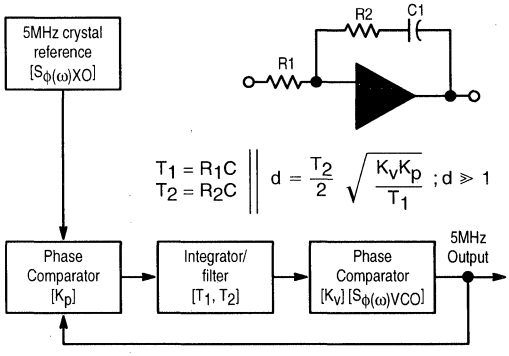

Figure 6. The phase–output noise in this type–2 second– order PLL can be optimized by adjusting the damping factor (d) in relation to the oscillator–noise crossover frequency (f_c).

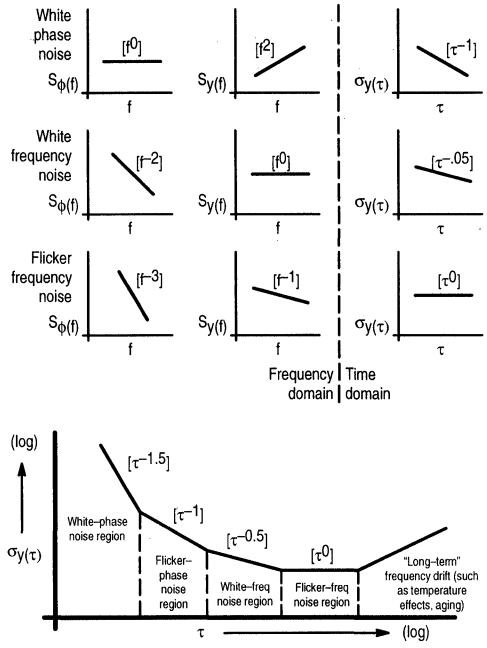

Figure 7. The distribution of the different types of frequency and phase noise can be expressed as line segments that represent powers of frequency or time (top), and the overall distribution of a system can be shown by combining appropriate segments (bottom).

As shown in Figure 7 (bottom) and Figure 8, (top), the phase–noise curves can be approximated with straight–line segments. The segments are plotted on semilog paper with $S_\phi(f)$ measured in dBc on the vertical axis. Therefore, the segments,

$$y = ax^b,$$

can be established from the end points on their phasenoise curves — where $S_\phi(f_1)$ and $S_\phi(f_2)$ correspond to the low–frequency (f_1) and the high–frequency (f_2) end points, as follows:

$$b = \frac{S_\phi(f_1) - S_\phi(f_2)}{10(\log f_1 - \log f_2)}$$

and

$$\left(\frac{S_\phi(f_1) - 10\ b\ \log\ f_1}{10}\right)$$

$$a = 10$$

Allan variance calculations

Step	Instructions	Input Data/Units	Keys	Output Data/Units
1	Key in the program			
2	Store	b	STO 7	
		α	STO .1	
		ν	STO .0	
		τ	STO 8	
3	Enter and start program	f_1	ENT↑	
		f_2	ENT↑	
		n	GSB .3	$\sigma^2 y$

Step	Key Entry	Key Code	Step	Key Entry	Key Code
001	(g) LBL 7	25 14 07	044	RCL 4	55 04
002	RCL 4	55 04	045	STO ÷ 5	45 41 05
003	×	51	046	RCL 5	55 05
004	x ⇆ y	11	047	GSB 0	13 00
005	÷	61	048	GSB 6	13 06
006	GTO 2	14 02	049	(g) RTN	25 13
007	(g) LBL 6	25 14 06	050	(g) LBL 5	25 14 05
008	ENT↑	21	051	3	03
009	+	41	052	RCL 0	55 00
010	STO ÷ 0	45 41 00	053	GTO 7	14 07
011	(g) RTN	25 13	054	(g) LBL 0	25 14 00
012	(g) LBL 3	25 14 03	055	(g) RAD	25 23
013	STO 3	45 03	056	STO 6	45 06
014	R↓	12	057	(g) π	25 63
015	STO 2	45 02	058	×	51
016	R↓	12	059	RCL 8	55 08
017	STO 1	45 01	060	×	51
018	GSB 0	13 00	061	(f) sin	16 42
019	STO 0	45 00	062	(g) x^2	25 53
020	RCL 2	55 02	063	(g) x^2	25 53
021	GSB 0	13 00	064	RCL 6	55 06
022	STO ÷ 0	45 41 00	065	RCL 7	55 07
023	RCL 2	55 02	066	(f) y^x	16 54
024	RCL 1	55 01	067	×	51
025	STO 5	45 05	068	(g) DEG	25 24
026	—	31	069	(g) RTN	25 13
027	RCL 3	55 03	070	(g) LBL 2	25 14 02
028	+	61	071	(g) π	25 63
029	STO 4	45 04	072	RCL 8	55 08
030	0	00	073	×	51
031	STO 9	45 09	074	RCL .0	55 .0
032	(g) LBL 8	25 14 08	075	×	51
033	GSB 4	13 04	076	(g) x^2	25 53
034	STO ÷ 0	45 41 00	077	(g) 1/x	25 64
035	2	02	078	×	51
036	STO ÷ 9	45 41 09	079	2	02
037	RCL 3	55 03	080	×	51
038	RCL 9	55 09	081	RCL .1	55 .1
039	(f) x = y	16 61	082	×	51
040	GTO 5	14 05	083	PRx	65
041	GSB 4	13 04	084	(g) SPC	25 65
042	GTO 8	14 08	085	(g) RTN	25 13
043	(g) LBL 4	25 14 04			

REGISTERS

0	1	2	3	4	5	6	7 **b**	8 τ	9
.0 ν	.1 α	.2	.3	.4	.5	S6	S7	S8	S9

4

With coefficients a and b established for each line segment the contributions of each segment to the overall Allan variance σ_y^2 can be calculated with the approximate Allan equation,

$$\sigma_y^2(\tau, f) = \frac{2a}{(\tau\upsilon\pi)^2} \int_{f_1}^{f_2} f^b \sin^4(\pi f \tau)\, df,$$

by a modified Simpson's Rule program supplied by Hewlett–Packard (HP–19C/29C *Applications' Book*, 1977). The Simpson's Rule is incorporated into the complete program for an HP–19C calculator — "Allan Variance Calculations." With a, b, υ, and τ established, the only decision

Calculated short–term stability

Device	Segment I				
Reference oscillator	f_1 = 0.1Hz, f_2 = 10Hz a = 1.26×10^{-12}, b = –1.40				
	T/n	0.001/10	0.01/10	0.1/20	1/100
	σy^2	1.10×10^{-27}	1.05×10^{-25}	4.80×10^{-25}	1.76×10^{-26}
Voltage–controlled oscillator	f_1 = 0.1Hz, f_2 = 10Hz a = 5.01×10^{-10}, b = –3.90				
	T/n	0.001/10	0.01/10	0.1/20	1/100
	σy^2	4.49×10^{-27}	4.39×10^{-25}	1.34×10^{-23}	8.10×10^{-23}
PLL output	f_1 = 0.1Hz, f_2 = 100Hz a = 4.64×10^{-12}, b = –1.83				
	T/n	0.001/10	0.01/20	0.1/100	1/1000
	σy^2	2.43×10^{-24}	1.46×10^{-23}	1.19×10^{-24}	8.21×10^{-26}
Device	**Segment II**				
Reference oscillator	f_1 = 10Hz, f_2 = 100Hz a = 1.26×10^{-13}, b = –0.40				
	T/n	0.001/10	0.01/20	0.1/100	1/1000
	σy^2	3.27×10^{-23}	8.22×10^{-23}	7.56×10^{-25}	7.56×10^{-27}
Voltage–controlled oscillator	f_1 = 10Hz, f_2 = 100Hz a = 6.31×10^{-12}, b = –2.00				
	T/n	0.001/10	0.01/20	0.1/100	1/1000
	σy^2	1.59×10^{-24}	1.06×10^{-23}	1.63×10^{-25}	1.27×10^{-27}
PLL output	f_1 = 100Hz, f_2 = 1000Hz a = 2.51×10^{-14}, b = –0.70				
	T/n	0.001/20	0.01/100	0.1/1000	1/10,000
	σy^2	1.04×10^{-21}	1.00×10^{-23}	1.01×10^{-25}	1.01×10^{-27}
Device	**Segment III**				
Reference oscillator	f_1 = 100Hz, f_2 = 1000Hz a = 2.00×10^{-14}, b = –0.00				
	T/n	0.001/20	0.01/100	0.1/1000	1/10,000
	σy^2	6.08×10^{-20}	5.47×10^{-22}	5.47×10^{-24}	5.47×10^{-26}
Voltage–controlled oscillator	f_1 = 100Hz, f_2 = 1000Hz a = 6.31×10^{-15}, b = –0.50				
	T/n	0.001/20	0.01/100	0.1/1000	1/10,000
	σy^2	8.88×10^{-27}	8.27×10^{-24}	8.28×10^{-26}	—

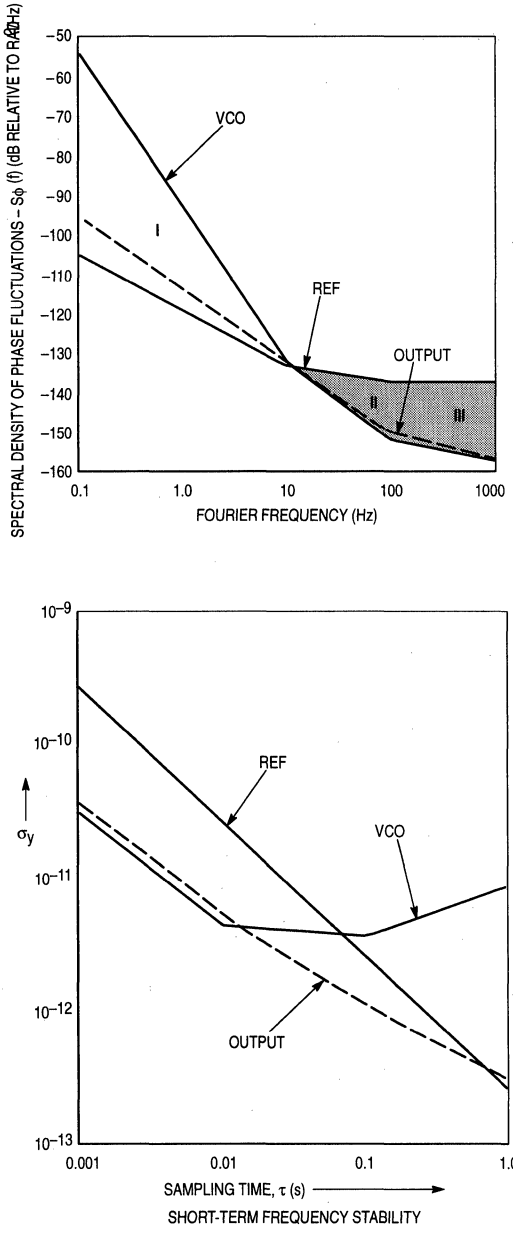

Figure 8. The phase–noise characteristics of the reference oscillator and the VCO can be expressed with three straight–line segments (I, II, and III); and the PLL output by two (top). The short–term stability in the terms of the Allan variance can then be calculated by keying the required coefficients as determined from the coordinates of these line–segement ends into the calculator (see Table) and plotting the results (bottom).

remaining, is the number of intervals, n, into which the segments must be divided. The more intervals chosen, the more accurate the calculation, but the longer the calculation takes. A good choice for a minimum n value (which must be an even number) is

$$n \geq 10\ [\tau(f_2 - f_1)].$$

The calculation time, then, is 0.056n + 0.15min.

To illustrate an application of the Allan variance calculations, the (a and b) program coefficients for the straight–line segments making up the VCO, reference oscillator, and overall output noise were determined from Figure 8 (top). The coefficients are listed in the "Calculated Short–term Stability" table. Sample times of 1, 10, 100, and 1000ms and end frequencies of 0.1, 10, and 1000Hz were employed.

With these inputs, σ_y^2 was determined with the Allan variance program. The frequency stability

$$\sigma_y(\tau) = \sqrt{\Sigma\sigma_y^2\ (\tau, f_h)}\ ,$$

was calculated, after summing the individual σ_y^2 contributions of each segment. A plot of σ_y vs sampling time for the VCO, reference, and output is shown in Figure 8 (bottom). ■ ■

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Glossary

5

Glossary of Terms and Abbreviations

The list contains terms found in this and other Motorola publications concerned with Motorola Semiconductor products for Communications.

A-Law — A European companding/encoding law commonly used in PCM systems.

A/B Signaling — A special case of 8th-bit (LSB) signaling in a μ-law system that allows four logic states to be multiplexed with voice on PCM channels.

A/D (analog-to-digital) converter (ADC) — A converter that uniquely represents all analog input values within a specified total input range by a limited number of digital output codes, each of them exclusively representing a fractional part of the total analog input range.

Aliasing Noise — A distortion component that is created when frequencies present in a sampled signal are greater than one-half the sample rate.

Answer Back — A signal sent by receiving data-processing device in response to a request from a transmitting device, indicating that the receiver is ready to accept or has received data.

Anti-aliasing Filter — A filter (normally low pass) that band limits an input signal *before* sampling to prevent aliasing noise.

Asynchronous — A mode of data transmission in which the time occurrence of the bits within each character or block of characters relates to a fixed time frame, but the start of each character or block of characters is not related to this fixed time frame.

Attenuation — A decrease in magnitude of a communication signal.

Bandwidth — The information-carrying frequencies between the limiting frequencies of a communication line or channel.

Baseband — The frequency band occupied by information-bearing signals before combining with a carrier in the modulation process.

Baud — A unit of signaling speed equal to the number of discrete signal conditions or events per second. This refers to the physical symbols/second used within a transmission channel.

Bit Rate — The speed at which data bits are transmitted over a communication path, usually expressed in bits per second. A 9600 bps terminal is a 2400 baud system with 4 bits/baud.

Blocking — A condition in a switching system in which no paths or circuits are available to establish a connection to the called party even though it is not busy, resulting in a busy tone to the calling party.

BORS(C)HT — Battery, Overvoltage, Ringing, Supervision, (Codec), Hybrid, Test; the functions performed by a subscriber line card in a telephone exchange.

Broadband — A transmission facility whose bandwidth is greater than that available on voice-grade facilities. (Also called wide band.)

C Message — A frequency weighting that evaluates the effects of noise based on its annoyance to the "typical" subscriber of standard telephone service or the effects of noise (background and impulse) on voice-grade data service.

Carrier — An analog signal of fixed amplitude and frequency that combines with an information-bearing signal by modulation to produce an output signal suitable for transmission.

CCITT — Consultative Committee for International Telephone and Telegraph; an international standards group of European International Telecommunications Union.

CCSN — Common Channel Signaling Network.

Central Office (CO) — A main telephone office, usually within a few miles of a subscriber, that houses switching gear; commonly capable of handling about 10,000 subscribers.

Channel Bank — Communication equipment commonly used for multiplexing voice-grade channels into a digital transmission signal (typically 24 channels in the U.S. and 30 channels in Europe).

CIDCW — Calling Identity Delivery on Call Waiting; a subscriber feature which allows for the display of the time, date, number, and possible other information about the caller to the called party while the called party is off-hook.

CLASS — Custom Local Area Signaling Service; a set of services, enhancements, provided to TELCO customers which may include CND, CNAM, Message Waiting, and other features.

CLID — Calling Line IDentification; a subscriber feature which allows for the display of the time, date, number, and possible other information about the caller to the called party.

CNAM — Calling Name Delivery; a subscriber feature which allows for the display of the time, date, number, and name of the caller to the called party.

CND — Calling Number Delivery; a subscriber feature which allows for the display of the time, date, number, and possible other information about the caller to the called party.

CODEC — COder-DECoder; the A/D and D/A function on a subscriber line card in a telephone exchange.

COFIDEC — COder-Filter-DECoder; the combination of a codec, the associated filtering, and voltage references required to code and decode voice in a subscriber line card.

Common Mode Rejection — The ability of a device having a balanced input to reject a voltage applied simultaneously to both differential-input terminals.

Companding — The process in which dynamic range compression of a signal is followed by expansion in accordance

with a given transfer characteristic (companding law) which is usually logarithmic.

Compander — A combination of a compressor at one point in a communication path for reducing the amplitude range of signals, followed by an expander at another point for restoring the original amplitude range, usually to improve the signal-to-noise ratio.

Conference Call — A call between three or more stations, in which each station can carry on a conversation simultaneously.

CPE — Customer Premise Equipment; this could be a POTS phone, answering machine, fax machine, or any number of other devices connected to the PSTN.

Crosspoint — The operating contacts or other low-impedance-path connection over which conversations can be routed.

Crosstalk — The undesired transfer of energy from one signal path to another.

CSN — Circuit Switched Network.

CTS — Clear to send; a control signal between a modem and a controller used to initiate data transmission over a communication line.

CVSD — Continuous Variable Slope Delta (modulation); a simple technique to converting an analog signal (like voice) into a serial bit stream.

D3 — D3 channel bank; a specific generation of AT&T 24-channel PCM terminal that multiplexes 24 voice channels into a 1.544 MHz digital bit stream. The specifications associated with D3 channel banks are the basis for all PCM device specifications.

D/A (digital-to-analog) converter (DAC) — A converter that represents a limited number of different digital input codes by a corresponding number of discrete analog output values.

Data Compression — A technique that provides for the transmission of fewer data bits than originally required without information loss. The receiving location expands the received data bits into the original bit sequence.

dB (decibel) — A power or voltage measurement unit, referred to another power or voltage. It is generally computed as:

10 x log (P1/P2) for power measurements, and

20 x log (V1/V2) for voltage measurements.

dBm — An indication of signal power. 1.0 mW across 600 Ω, or 0.775 volts rms, is defined as 0 dBm. Any other voltage level is converted to dBm by:

dBm = 20 x log (Vrms/0.775), or

dBm = [20 x log (Vrms)] + 2.22.

dBmO — Signal power measured at a point in a standard test tone level at the same point.

i.e., dBmO = dBm = dBr

where dBr is the relative transmission level, or level relative to the point in the system defined as the zero transmission level point.

dBmOp — Relative power expressed in dBmp. (See dBmO and dBmp.)

dBmp — Indicates dBm measurement made with a psophometric weighting filter.

dBrn — Relative signal level expressed in decibels above reference noise, where reference noise is 1 pW. Hence, 0 dBrn = 1 pW = – 90 dBm.

dBrnC — Indicates dBrn measurement made with a C-message weighting filter. (These units are most commonly used in the U.S., where psophometric weighting is rarely used.)

dBrnc0 — Noise measured in dBrnc referenced to zero transmission level.

Decoding — A process in which one of a set of reconstructed analog samples is generated from the digital character signal representing a sample.

Delay Distortion — Distortion that occurs on communication lines due to the different propagation speeds of signals at different frequencies, measured in microseconds of delay relative to the delay at 1700 Hz. (This type of distortion does not affect voice communication, but can seriously impair data transmission.)

Delta Modulation — A simple digital coding technique that produces a serial bit stream corresponding to changes in analog input levels; usually utilized in devices employing continuously variable-slope delta (CVSD) modulation.

Demodulator — A functional section of a modem that converts received analog line signals to digital form.

DN — Directory Number.

Digital Telephone — A telephone terminal that digitizes a voice signal for transmission and decodes a received digital signal back to a voice signal. (It will usually multiplex 64 kbps voice and separate data inputs at multiples of 8 kbps.)

Distortion — The failure to reproduce an original signal's amplitude, phase, delay, etc. characteristics accurately.

DPSK — Differential Phase Shift Keying; a modulation technique for transmission where the frequency remains constant but phase changes will occur from 90°, 180°, and 290° to define the digital information.

DTMF — Dual Tone Multi-Frequency. It is the "tone dialing" system based on outputting two non-harmonic related frequencies simultaneously to identify the number dialed. Eight frequencies have been assigned to the four rows and four columns of a typical keypad.

Duplex — A mode of operation permitting the simultaneously two-way independent transmission of telegraph or data signals.

Echo — A signal that has been reflected or returned as a result of impedance mismatches, hybrid unbalance, or time delay. Depending upon the location of impedance irregularities and the propagation characteristics of a facility, echo may interfere with the speaker/listener or both.

Echo Suppressor — A device used to minimize the effect of echo by blocking the echo return currents; typically a voice-operated gate that allows communication one way at a time.

Encoder (PCM) — A device that performs repeated sampling, compression, and A/D conversion to change an analog signal to a serial stream of PCM samples representing the analog signal.

Equalizer — An electrical network in which phase delay or gain varies with frequency to compensate for an undesired amplitude or phase characteristic in a frequency-dependent transmission line.

ET — Exchange Termination (C.O. Switch).

FDM — Frequency-Division Multiplex; a process that permits the transmission of two or more signals over a common path by using a different frequency band for each signal.

Four Wire Circuit — The portion of a telephone, or central office, that operates on two pairs of wires. One pair is for the transmit path (generally from the microphone), and one pair is for the receive path (generally from the receiver).

Frame — A set of consecutive digit time slots in which the position of each digit slot can be identified by reference to a frame alignment. The frame alignment signal does not necessarily occur, in whole or in part, in each frame.

Full Duplex — A mode of operation permitting simultaneous transmission of information between two locations in both directions.

Gain — The change in signal amplitude (increase or decrease) after passing through an amplifier, or other circuit stage. Usually expressed in dB, an increase is a positive number, and a decrease is a negative number.

Gain Tracking Error — The variation of gain from a constant level (determined at 0 dBm input level) when measuring the dependence of gain on signal level by comparing the output signal to the input signal over a range of input signals.

HDLC — High-Level Data Link Control; a CCITT standard data communication line protocol.

Half Duplex — A transmission system that permits communication in one direction at a time. CB ratios, with "push-to-talk" switches, and voice-activated speakerphones, are half duplex.

Handset — A rigid assembly providing both telephone transmitter and receiver in a form convenient for holding simultaneously to mouth and ear.

Hookswitch — A switch that connects the telephone circuit to the subscriber loop. The name derives from old telephones where the switch was activated by lifting the receiver off and onto a hook on the side of the phone.

Idle Channel Noise (ICN) — The total signal energy measured at the output of a device or channel under test when the input of the device or channel is grounded (often a wideband noise measurement using a C-message weighting filter to band-limit the output noise).

Intermodulation — The modulation of the components of a complex wave by each other (in a nonlinear system).

Intermodulation Distortion — An analog line impairment when two frequencies interact to create an erroneous frequency, in turn distorting the data signal representation.

IRED — Infrared. Used as a wireless link for remote control or to transfer data.

ISDN — Integrated Services Digital Network; a communication network intended to carry digitized voice and data multiplexed onto the public network.

Jitter — A type of analog communication line distortion caused by abrupt, spurious signal variation from a reference timing position, and capable of causing data transmission errors, particularly at high speeds. (The variation can be in amplitude, time, frequency, or phase.)

Key System — A miniature PABX that accepts 4 to 10 lines and can direct them to as many as 30 telsets.

μ-law — A companding law accepted as the North American standard for PCM based systems.

LAN — Local Area Network; a data-only communication network between data terminals using a standard interface to the network.

Line — The portion of a circuit external to an apparatus that consists of the conductors connecting the apparatus to the exchange or connecting two exchanges.

Line Length Compensation — Also referred to as loop length compensation, it involves changing the gain of the transmit and receive paths, within a telephone, to compensate for different signal levels at the end of different line lengths. A short line (close to the CO) will attenuate signals less, and therefore less gain is needed. Compensation circuits generally use the loop current as an indication of the line length.

Longitudinal Balance — The common-mode rejection of a telephone circuit.

Loop — The loop formed by the two subscriber wires (Tip and Ring) connected to the telephone at one end, and the central office (or PBX) at the other end. Generally it is a floating system, not referred to ground, or ac power.

Loopback — Directing signals back toward the source at some point along a communication path.

Loop Current — The dc current that flows through the subscriber loop. It is typically provided by the central office or PBX, and ranges from 20 to 120 mA.

LT — Line Termination (Line Card).

MCU — MicroComputer Unit (also MicroController Unit).

MPU — MicroProcessor Unit.

Mu-Law — A companding/encoding law commonly used in U.S. (same as μ-law).

MUX — Multiplex or multiplexer.

Modem — MOdulator-DEModulator; a unit that modulates and demodulates digital information from a terminal or com-

puter port to an analog carrier signal for passage over an analog line.

Multiplex — To simultaneously transmit two or more messages on a single channel.

NT1 — Network Termination 1 (OSI Layer 1 Only).

NT2 — Network Termination 2 (OSI Layers 2 and 3).

Off-hook — The condition when the telephone is connected to the phone system, permitting loop current to flow. The central office detects the dc current as an indication that the phone is busy.

On-hook — The condition when the telephone's dc path is open, and no dc loop current flows. The central office regards an on-hook phone as available for ringing.

PABX — Private Automatic Branch Exchange; a customer-owned, switchable telephone system providing internal and/or external station-to-station dialing.

Pair — The two associated conductors that form part of a communication channel.

Pass-band Filter — A filter used in communication systems that allows only the frequencies within a communication channel to pass, and rejects all frequencies outside the channel.

PBX — Private Branch Exchange; a class of service in standard Bell System terminology that typically provides the same service as PABX.

PCM — Pulse Code Modulation; a method of transmitting data in which signals are sampled and converted to digital words that are then transmitted serially, typically as 8-bit words.

Phase Jitter — Abrupt, spurious variations in an analog line, generally caused by power and communication equipment along the line that shifts the signal phase relationship back and forth.

PLL — Phase-Locked Loop.

PLL Frequency Synthesizer — Phase-locked loop frequency synthesizer. A frequency synthesizer utilizing a closed loop, as opposed to DDS (direct digital synthesis) which is not a closed loop.

POTS — Plain Old Telephone Service.

Propagation Delay — The time interval between specified reference points on the input and output voltage waveforms.

Psophometric Weighting — A frequency weighting similar to C-Message weighting that is used as the standard for European telephone system testing.

PSN — Packet Switched Network.

PSTN — Public Switched Telephone Network.

Pulse Dialer — A device that generates pulse trains corresponding to digits or characters used in impulse or loop-disconnect dialing.

Quantizing Noise — Signal-correlated noise generally associated with the quantizing error introduced by A/D and D/A conversions in digital transmission systems.

REN — Ringer Equivalence Number; an indication of the impedance, or loading factor, of a telephone bell or ringer circuit. An REN of 1.0 equals about 8 kΩ. The Bell system typically permits a maximum of 5.0 REN (1.6 kΩ) on an individual subscriber line. A minimum REN of 0.2 (40 kΩ) is required by the Bell system.

Repeater — An amplifier and associated equipment used in a telephone circuit to process a signal and retransmit it.

Repertory Dialer — A dialer that stores a repertory of telephone numbers and dials any one of them automatically on request.

Ring — One of the two wires connecting the central office to a telephone. The name derives from the ring portion of the plugs used by operators (in older equipment) to make the connection. Ring is traditionally negative with respect to Tip.

RTS — Request To Send; an EIA-232 control signal between a modem and user's digital equipment that initiates the data transmission sequence on a communication line.

Sampling Rate — The frequency at which the amplitude of an analog signal is gated into a coder circuit. The Nyquist sampling theorem states that if a band-limited signal is sampled at regular intervals and at a rate equal to or greater than twice the highest frequency of interest, the sample contains all the information of the original signal. The frequency band of interest in telephony ranges from 300 to 3400 Hz, so a sampling rate of 8 kHz provides dc to 4000 Hz reproduction.

SCU — Subscriber Channel Unit; the circuitry at a telephone exchange associated with an individual subscriber line or channel.

Sidetone — The sound fed back to the receiver as a result of speaking into the microphone. It is a natural consequence of the 2-to-4 wire conversion system. Sidetone was recognized by Alexander Graham Bell as necessary for a person to be able to speak properly while using a handset.

Signaling — The transmission of control or status information between switching systems in the form of dedicated bits or channels of information inserted on trunks with voice data.

Signal-to-Distortion Ratio (S/D) — The ratio of the input signal level to the level of all components that are present when the input signal (usually a 1.020 kHz sinusoid) is eliminated from the output signal (e.g., by filtering).

SLIC — Subscriber Line Interface Circuit; a circuit that performs the 2-to-4 wire conversion, battery feed, line supervision, and common mode rejection at the central office (or PBX) end of the telephone line.

SOG package — Small-Outline Gull-wing package; formerly SOIC with gull-wing leads. This package has leads which fold out from the body.

SOJ package — Small-Outline J-lead package; formerly SOIC with J leads. This package has leads which are tucked under the body.

Speech Network — A circuit that provides 2-to-4 wire conversion, i.e., connects the microphone and receiver (or the trans-

mit and receive paths) to the Tip and Ring phone lines. Additionally it provides sidetone control, and in many cases, the dc loop current interface.

Subscriber Line — The system consisting of the user's telephone, the interconnecting wires, and the central office equipment dedicated to that subscriber (also referred to as a loop).

Switchhook — A synonym for hookswitch.

Syn (Sync) — (1) A bit character used to synchronize a time frame in a time-division multiplexer. (2) A sequence used by a synchronous modem to perform bit synchronization or by a line controller for character synchronization.

Synchronous Modem — A modem that uses a derived clocking signal to perform bit synchronization with incoming data.

T1 Carrier — A PCM system operating at 1.544 MHz and carrying 24 individual voice-frequency channels.

TA — Terminal Adatper.

Talkdown — Missed signals in the presence of speech. Commonly used to describe the performance of a DTMF receiver when it fails to recognize a valid DTMF tone due to cancellation of that tone by speech.

Talkoff — False detections caused by speech. Commonly used to describe the performance of a DTMF receiver when speech, emulating DTMF, causes the receiver to believe it has detected a valid DTMF tone.

Tandem Trunk — See trunk.

Telephone Exchange — A switching center for interconnecting the lines that service a specific area.

TE1 — Terminal Equipment 1 (ISDN Terminal).

TE2 — Terminal Equipment 2 (Non-ISDN Terminal).

TELETEX — A text communication service between entirely electronic work stations that will gradually replace TELEX with the introduction of the digital network. (Not to be confused with teletext.)

TELETEXT — The name usually used for broadcast text (and graphics) for domestic television reception. (Not to be confused with teletex.)

Time-Division Multiplex — A process that permits the transmission of two or more signals over a common path by using a different time interval for each signal.

Tin Cans and String — A *crude* analog communications system commonly used to introduce voice communications to children.

Tip — One of the two wires connecting the central office to a telephone. The name derives from the tip of the plugs used by operators (in older equipment) to make the connection. Tip is traditionally positive with respect to ring.

Tone Ringer — The modern solid state equivalent of the old electromechanical bell. It provides the sound when the central office alerts the subscriber that someone is calling. Ringing voltage is typically 80–90 volts rms, 20 Hz.

Trunk — A telephone circuit or channel between two central offices or switching entities.

TSAC — Time Slot Assigner Circuit; a circuit that determines when a CODEC will put its 8 bits of data on a PCM bit stream.

TSIC — Time Slot Interchange Circuit; a device that switches digital highways in PCM based switching systems; a "digital" crosspoint switch.

Twist — The amplitude ratio of a pair of DTMF tones. (Because of transmission and equipment variations, a pair of tones that originated equal in amplitude may arrive with a considerable difference in amplitude.)

Two Wire Circuit — Refers to the two wires connecting the central office to the subscriber's telephone. Commonly referred to as Tip and Ring, the two wires carry both transmit and receive signals in a differential manner.

UDLT — Universal Digital Loop Transceiver; a Motorola originated name for a voice/data transceiver circuit.

VCO — Voltage-controlled oscillator. Input is a voltage; output is a sinusoidal waveform.

VCM — Voltage-controlled multivibrator. Input is a voltage; output is a square wave.

Voice Frequency — A frequency within that part of the audio range that is used for the transmission of speech of commercial quality (i.e., 300–3400 Hz).

Weighting Network — A network whose loss varies with frequency in a predetermined manner.

ANSI **American National Standards Institute**
11 West 42nd Street
New York, NY 10036
USA

Bellcore **Bell Communications Research**
Customer Service
60 New England Avenue
Piscataway, NJ 08854-4196
USA
Phone: (201) 699-5800

CCITT **Consultive Committee of the International Telephone and Telegraph**
International Telecommunications Union
Place Des Nations
CH-1211 Geneva
Switzerland
Phone: (011) 4122 730 5851

EIA **Electronic Industries Association**
1722 Eye Street, NW
Suite 440
Washington, DC 20006
USA
Phone (Headquarters): (202) 457-4936
Phone (Standards): (202) 457-4966

ETSI **European Telecommunications Standards Institute**
06921 Sophia Antipolis Cedex
FRANCE
Phone: 33 92 94 42 00
Fax: 33 93 65 47 16

IEEE **Institute of Electrical and Electronics Engineers**
Headquarters:
345 East 47th Street
New York, NY 10017
USA
Phone (212) 705-7900

Standards Office:
IEEE Service Center
PO Box 1331
Piscataway, NJ 00855
USA
Phone: (201) 981-0060

TIA **Telecommunications Industry Association**
2001 Pennsylvania Avenue, NW
Suite 800
Washington, DC 2006-1813
USA
Phone: (202) 457-5430
Fax: (202 457-4939

Handling and Design Guidelines

6

6

Handling and Design Guidelines

HANDLING PRECAUTIONS

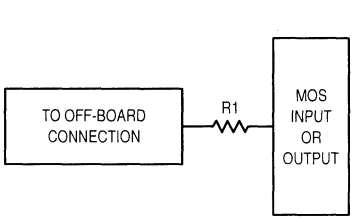
All CMOS devices have an insulated gate that is subject to voltage breakdown. The high-impedance gates on the devices are protected by on-chip networks. However, these on-chip networks do not make the IC immune to electrostatic damage (ESD). Laboratory tests show that devices may fail after one very high voltage discharge. They may also fail due to the cumulative effect of several discharges of lower potential.

Static-damaged devices behave in various ways, depending on the severity of the damage. The most severely damaged are the easiest to detect because the input or output has been completely destroyed and is either shorted to V_{DD}, shorted to V_{SS}, or open-circuited. The effect is that the device is no longer functional. Less severe cases are more difficult to detect because they appear as intermittent failures or degraded performance. Static damage can often increase leakage currents.

CMOS devices are not immune to large static voltage discharges that can be generated while handling. For example, static voltages generated by a person walking across a waxed floor have been measured in the 4–15 kV range (depending on humidity, surface conditions, etc.). Therefore, the following precautions should be observed.

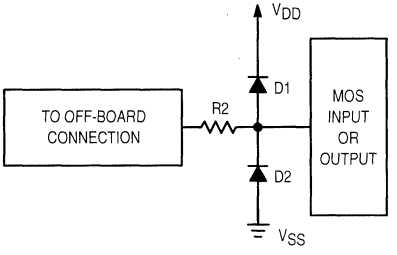
1. Do not exceed the Maximum Ratings specified by the data sheet.
2. All unused device inputs should be connected to V_{DD} or V_{SS}.
3. All low-impedance equipment (pulse generators, etc.) should be connected to CMOS inputs only after the device is powered up. Similarly, this type of equipment should be disconnected before power is turned off.
4. A circuit board containing CMOS or devices is merely an extension of the device and the same handling precautions apply. Contacting connectors wired directly to devices can cause damage. Plastic wrapping should be avoided. When external connections to a PC board address pins of CMOS integrated circuits, a resistor should be used in series with the inputs or outputs. The limiting factor for the series resistor is the added delay caused by the time constant formed by the series resistor and input capacitance. This resistor will help limit accidental damage if the PC board is removed and brought into contact with static generating materials. For convenience, equations for added propagation delay and rise time effects due to series resistance size are given in Figure 1.
5. All CMOS devices should be stored or transported in materials that are antistatic. Devices must not be inserted into conventional plastic "snow", styrofoam or plastic trays, but should be left in their original container until ready for use.

Figure 1. Networks for Minimizing ESD and Reducing CMOS Latch Up Susceptibility



Advantage: Requires minimal board area.

Disadvantage: R1 > R2 for the same level of protection, therefore rise and fall times, propagation delays, and output drives are severely affected.



Advantage: R2 < R1 for the same level of protection. Impact on ac and dc characteristics is minimized.

Disadvantage: More board area, higher initial cost.

NOTE: These networks are useful for protecting the following:

A. digital inputs and outputs
B. analog inputs and outputs
C. 3-state outputs
D. bidirectional (I/O) ports

EQUATION 1 – PROPAGATION DELAY VS SERIES RESISTANCE

$$R \approx \frac{t}{C \bullet k}$$

where:
R = the maximum allowable series resistance in ohms
t = the maximum tolerable propagation delay in seconds
C = the board capacitance plus the driven device's input capacitance in farads
k = 0.33 for devices with TTL input levels (switch point ≈ 1.3 V)
k = 0.7 for devices with CMOS input levels (switch point ≈ 50% V_{DD}).

EQUATION 2 – RISE TIME VS SERIES RESISTANCE

$$R \approx \frac{t}{C \bullet k}$$

where:
R = the maximum allowable series resistance in ohms
t = the maximum tolerable propagation delay in seconds
C = the board capacitance plus the driven device's input capacitance in farads
k = 0.7 for devices with TTL input levels (switch point ≈ 1.3 V)
k = 2.3 for devices with CMOS input levels (switch point ≈ 50% V_{DD}).

6

6. All CMOS devices should be placed on a grounded bench surface and operators should ground themselves prior to handling devices, since a worker can be statically charged with respect to the bench surface. Wrist straps in contact with skin are strongly recommended. See Figure 2.
7. Nylon or other static generating materials should not come in contact with CMOS circuits.
8. If automatic handling is being used, high levels of static electricity may be generated by the movement of devices, belts, or boards. Reduce static build-up by using ionized air blowers or room humidifiers. All parts of machines which come into contact with the top, bottom, and sides of IC packages must be grounded metal or other conductive material.
9. Cold chambers using CO_2 for cooling should be equipped with baffles, and devices must be contained on or in conductive material.
10. When lead-straightening or hand-soldering is necessary, provide ground straps for the apparatus used and be sure that soldering ties are grounded.
11. The following steps should be observed during wave solder operations.
    a. The solder pot and conductive conveyor system of the wave soldering machine must be grounded to an earth ground.
    b. The loading and unloading work benches should have conductive tops which are grounded to an earth ground.
    c. Operators must comply with precautions previously explained.
    d. Completed assemblies should be placed in antistatic containers prior to being moved to subsequent stations.
12. The following steps should be observed during board cleaning operation.
    a. Vapor degreasers and baskets must be grounded to an earth ground. Operators must likewise be grounded.
    b. Brush or spray cleaning should not be used.
    c. Assemblies should be placed into the vapor degreaser immediately upon removal from the antistatic container.
    d. Cleaned assemblies should be placed in antistatic containers immediately after removal from the cleaning basket.
    e. High velocity air movement or application of solvents and coatings should be employed only when module circuits are grounded and a static eliminator is directed at the module.
13. The use of static detection meters for line surveillance is highly recommended.
14. Equipment specifications should alert users to the presence of CMOS devices and require familiarization with this specification prior to performing any kind of maintenance or replacement of devices or modules.
15. Do not insert or remove CMOS devices from test sockets with power applied. Check all power supplies to be used for testing devices to be certain there are no voltage transients present.
16. Double check the equipment setup for proper polarity of voltage before conducting parametric or functional testing.

RECOMMENDED READING

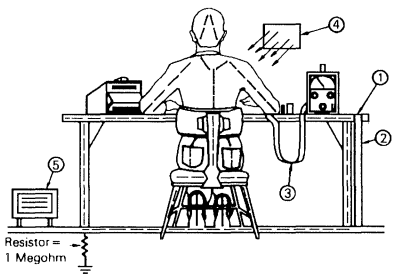
"Total Control of the Static in Your Business"
Available by writing to:

3M
Static Control Systems
Building A145-3N-01
P.O. Box 2963
Austin, TX 78769-2963

Or calling:

1-800-328-1368

Figure 2. Typical Manufacturing Work Station



NOTES:
1. 1/16 inch conductive sheet stock covering bench top work area.
2. Ground strap.
3. Wrist strap in contact with skin.
4. Static neutralizer. (Ionized air blower directed at work.) Primarily for use in areas where direct grounding is impractical.
5. Room humidifier. Primarily for use in areas where the relative humidity is less than 45%. Caution: building heating and cooling systems usually dry the air causing the relative humidity inside of buildings to be less than outside humidity.

CMOS LATCH UP

Latch up will not be a problem for most designs, but the designer should be aware of it, what causes it, and how to prevent it.

Figure 3 shows the layout of a typical CMOS inverter and Figure 4 shows the parasitic bipolar devices that are formed. The circuit formed by the parasitic transistors and resistors is the basic configuration of a silicon controlled rectifier, or SCR. In the latch-up condition, transistors Q1 and Q2 are turned on, each providing the base current necessary for the other to remain in saturation, thereby latching the devices on. Unlike a conventional SCR, where the device is turned on by applying a voltage to the base of the NPN transistor, the parasitic SCR is turned on by applying a voltage to the emitter of either transistor. The two emitters that trigger the SCR are the same point, the CMOS output. Therefore, to latch up the CMOS device, the output voltage must be greater than V_{DD} + 0.5 Vdc or less than – 0.5 Vdc and have sufficient current to trigger the SCR. The latch-up mechanism is similar for the inputs.

Once a CMOS device is latched up, if the supply current is not limited, the device will be destroyed. Ways to prevent such occurrences are listed below.

1. Ensure that inputs and outputs are limited to the maximum rated values, as follows:
   $-0.5 \le V_{in} \le V_{DD} + 0.5$ Vdc referenced to V_{SS}
   $-0.5 \le V_{out} \le V_{DD} + 0.5$ Vdc referenced to V_{SS}
   $|I_{in}| \le 10$ mA
   $|I_{out}| \le 10$ mA when transients or dc levels exceed the supply voltages.
2. If voltage transients of sufficient energy to latch up the device are expected on the outputs, external protection diodes can be used to clamp the voltage. Another method of protection is to use a series resistor to limit the expected worst case current to the Maximum Ratings values (see Figure 1).
3. If voltage transients are expected on the inputs, protection diodes may be used to clamp the voltage or a series resistor may be used to limit the current to a level less than the maximum rating of I_{in} = 10 mA (see Figure 1).
4. Sequence power supplies so that the inputs or outputs of CMOS devices are not powered up first (e.g., recessed edge connectors may be used in plug-in board applications and/or series resistors).
5. Power supply lines should be free of excessive noise. Care in board layout and filtering should be used.
6. Limit the available power supply current to the devices that are subject to latch-up conditions. This can be accomplished with the power supply filtering network or with a current-limiting regulator.

Figure 3. CMOS Wafer Cross Section

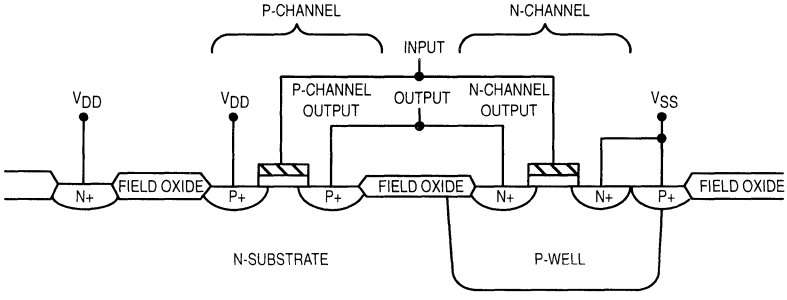
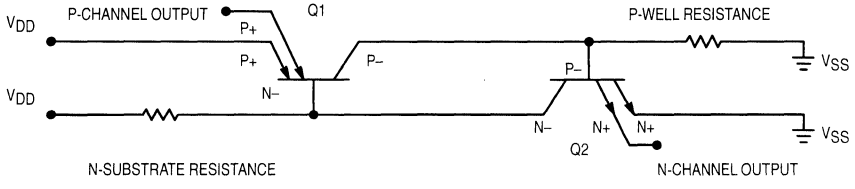


Figure 4. Latch Up Circuit Schematic



6

Quality and Reliability

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7

Quality In Manufacturing

QUALITY IN DESIGN

Motorola's quality activity starts at the product design stage. It is Motorola's philosophy to "design in" reliability. At all development points of any new design reliability oriented guidelines are continuously used to ensure that a thoroughly reliable part is ultimately produced. This is demonstrated by the excellent in-house reliability testing results obtained for all Motorola's semiconductor products and, more importantly, by our numerous customers.

MATERIAL INCOMING CONTROLS

Each vendor is supplied with a copy of the Motorola Procurement Specification which must be agreed in detail between both parties before any purchasing agreement is made. This is followed by a vendor appraisal report whereby each vendor's manufacturing facility is visited by Motorola Quality Engineers responsible for ensuring that the vendor has a well organized and adequately controlled manufacturing process capable of supplying the high quality material required to meet the Motorola Incoming Inspection Specification. Large investments have and are continuously being made and Quality Improvement programs developed with our main suppliers concerning:

Masks — Silicon — Piece-parts — Chemical products — Industrial gas, etc.

Each batch of material delivered to Motorola is quarantined at Goods-in until the Incoming Quality Organization has subjected adequate samples to the incoming detailed inspection specification. In the case of masks, this will include mask inspection for:

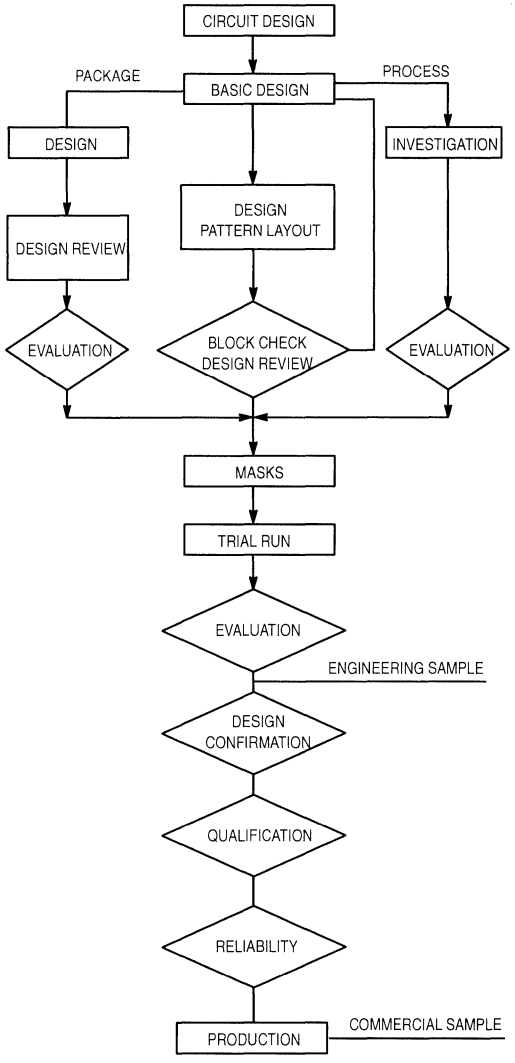
1. Defect Density
2. Intermask Alignment
3. Mask Revision
4. Device to Device Alignment
5. Mask Type

Silicon will undergo the following inspections:

1. Type "N" or "P"
2. Resistivity
3. Resistivity Gradient
4. Defects
5. Physical Dimensions
6. Dislocation Density

Incoming chemicals are also controlled to very rigorous standards. Many are submitted to in-house chemical analysis where the supplier's conformance to specification is meticulously checked. In many cases, line tests are performed before final acceptance. A major issue and responsibility for the Incoming Quality Department is to ensure that the most disciplined safety factors have been employed with regard to chemicals. Chemicals can and are often rejected because safety standards have not been deemed acceptable.

NEW PRODUCT TYPICAL DESIGN FLOW



THIS BASIC DESIGN FLOW-CHART OMITS SOME FEEDBACK LOOPS FOR SIMPLICITY

7

The Six Sigma Challenge

Motorola's expressed objective is the achievement of "error free performance" in products and services. The high quality level of the product-line outputs, followed by stringent outgoing quality control, readily assures this objective. But error-free output from the product lines themselves is a matter that continues to demand full attention at all levels of production, design and administration. This far more stringent requirement has a two-fold goal:

1. To further improve ultimate product reliability — experience has proved that products **designed** for 100% conformance to specifications are far less subject to field failure than products **selected** to a given level of performance.
2. To reduce waste — thereby making the end-product more cost competitive.

Whether or not one-hundred percent perfection is consistently achievable remains subject to conjecture. Motorola's already low reject rates, however, warrant a high level of confidence that the goal can be met, and milestones toward this objective have been firmly established.

Six Sigma Capability — not yet zero defects, but 99.9999998% perfection in both product and in customer services.

Why Six Sigma?

Each process attempts to reproduce its characteristics identically from unit to unit. Inherent in each process, however, there are variations in conditions and in materials that are uncontrollable and unalterable. In all cases, therefore, the unit-to-unit output characteristics vary somewhat from the ideal (design target).

The performance of a product is determined by how much margin exists between the design specifications and the actual value of that specification. For some processes, such as those using real-time feedback to control the output, the variations can be quite small; for others they may be quite large. Many of the parametric data of a given specification tend to follow the normal distribution curve shown in Figure 1.

Variation of the process is measured in Standard Deviations (Sigma) from the Mean. The normal deviation, defined as process width, is ± 3 Sigma about the mean, representing a yield of 99.73%. But is ± 3 Sigma good enough as an overall specification? Statistically, with a ± 3 sigma deviation, approximately 2700 parts per million still fall outside acceptable performance limits. Clearly, for a product to be built virtually defect free it must be designed with a component yield that is significantly better than ± 3 Sigma.

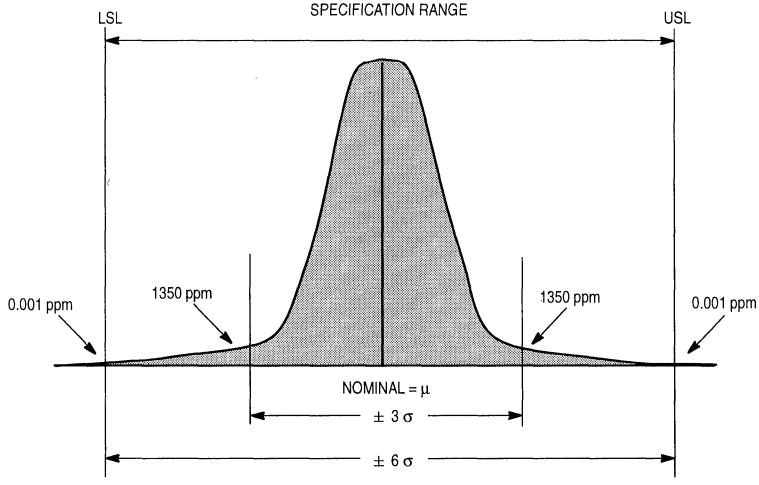


Figure 1. Standard distribution curve illustrates the Three Sigma and Six Sigma Parametric Conformance.

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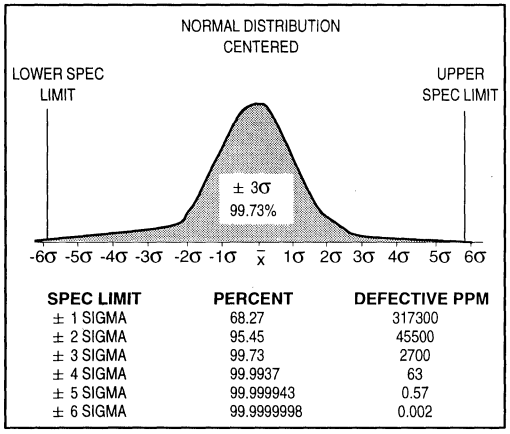
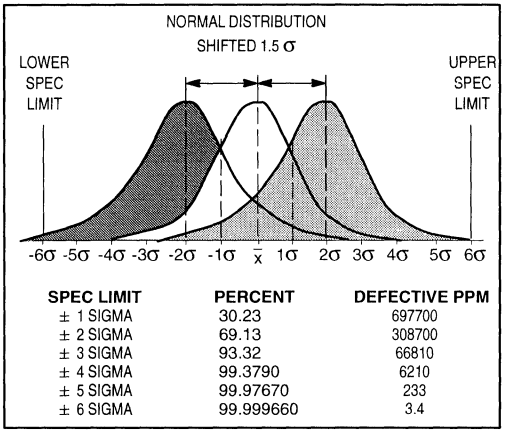


SPEC LIMIT	PERCENT	DEFECTIVE PPM
± 1 SIGMA	68.27	317300
± 2 SIGMA	95.45	45500
± 3 SIGMA	99.73	2700
± 4 SIGMA	99.9937	63
± 5 SIGMA	99.999943	0.57
± 6 SIGMA	99.9999998	0.002

Figure 2. With a Centered Distribution Between Six-Sigma Limits Only Two Devices Per Billion Fail to Meet the Specification Target.



SPEC LIMIT	PERCENT	DEFECTIVE PPM
± 1 SIGMA	30.23	697700
± 2 SIGMA	69.13	308700
± 3 SIGMA	93.32	66810
± 4 SIGMA	99.3790	6210
± 5 SIGMA	99.97670	233
± 6 SIGMA	99.999660	3.4

Figure 3. Effects of a 1.5 Sigma Shift Where Only 3.4 ppm Fail to Meet Specification.

The Six Sigma Latitude

Product yield is a factor of two variables: Process width and design width. If a process is adequately controlled so that its output is ± 3 Sigma, and if the product is so well designed that ± 3 Sigma deviations still place the products well within the specified design limits, then the overall yield is increased.

The table in Figure NO TAG shows that a design which can accept twice the normal ± 3 Sigma variation of the process (design width = ± 6 Sigma) will have a product yield of 99.9999998%, corresponding to 2.0 defective parts per billion. Even if the process mean were to shift by as much as ± 1.5 Sigma from the center of the distribution, the process would be expected to have no more than 3.4 parts per million defective.

The Motorola SPC Program

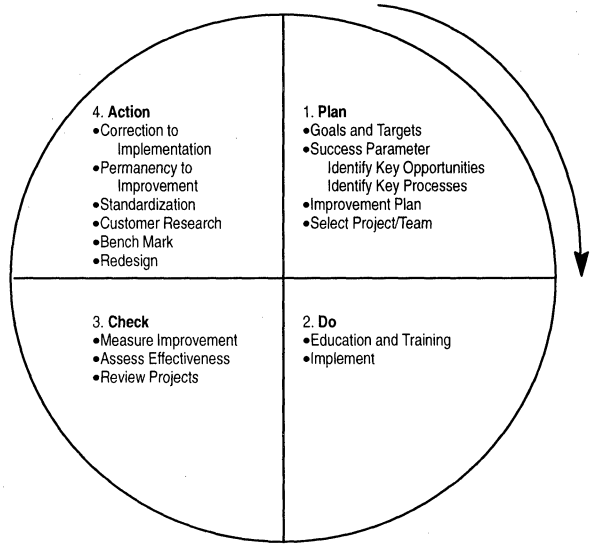
*** Purpose * Objective * Scope**

The Purpose of this program is to establish a standard approach toward continued process improvement through statistical process control.

Its Objective is to maintain all critical processes under tight statistical control in order to enhance quality and reduce scrap through identification of process variation, and through the reduction of these variations by means of real time corrective action. It is expected to establish the cultural environment and the organizational support required to achieve the Six-Sigma goal.

Its Scope encompasses a total quality improvement effort, involving design, manufacturing and management of all Motorola product groups and their suppliers as well as their support departments and vendors. It provides for the establishment of SPC teams and ensures adequate training. It serves as a liaison between teams in order to standardize and unify the approach to continuous quality improvement.

Continuous Improvement



Key Factors for Success

- Management Leadership
  - Top Down
  - Committed
  - Active
- Clear and Agreed-On Goals
- Breakthrough Thinking
- Project/Teamwork
- Training
- Reinforcing Successes

7

Verification of Statistical Process Control

Statistical process control programs have two specific functions:

1. as a monitor, to verify that a specific process is under control, or to indicate that a process is not in control based on interpretation of control-chart abnormalities or other indications;

2. as a quality improvement tool, for the purpose of improving process capability.

In either case, documentation must be available that permits the utilization, verification and interpretation of process control data, or if necessary, to implement new programs for process improvement.

Evidence of Process Capability

Capability indices must be established for each critical process and there must be evidence that the upper and lower specification limits are realistic and not arbitrary. The present goal is $C_p \geq 2.0$ and $C_{pk} \geq 1.5$.

Evidence of a process capability study must be on file. Depending on the level of sophistication, the study may include a factorial experiment, a nested variance study, summation of the results and recommendation for further action. The selection of critical process points must be justified.

Measurement System Capability

Results of measurement system capability study must be on file. Precision-to-Tolerance (P/T) ratio should be less than 0.10.

Process Control Specifications

Process specifications must include procedures to be followed in the event of a process requiring corrective action.

Operator Training

The operators are normally the first to see the control charts. Incorrect interpretation will cause unnecessary and time consuming investigations or delay needed studies. Consequently, operator training is a vital function and documented operator certification must be on file.

Control Chart Accuracy and Visibility

Control charts must be current and readily available. They shall be maintained by the production operators and upper and lower control limits must be calculated according to historical data.

Control Chart Tracking

Control charts must be tracked continuously. All out-of-control points must be highlighted and the appropriate corrective action described either on the chart or in a companion log. The objective is to view the trend, not simply to obtain a snapshot-in-time.

Supplier/Customer Relationships

Customers have no desire to control a supplier's process. Nor are they interested in the confidential details of a supplier's processes. They only want assurance (data) that a supplier has an ongoing program that supports an overall statistical process control plan. Primarily, Motorola's customers are interested in a supplier's statistical control of the critical processes, and his early warning system which keeps a process from becoming marginal. Most importantly, they are interested in what is being done for continuous improvement.

What We Offer Our Customers

It has been adequately demonstrated that a well monitored and controlled manufacturing process with minimum variations will produce a better, more useful and more reliable product at a reduced cost. In many instances, customer satisfaction now hinges not so much on a product's ability to meet specifications as on a manufacturer's ability to control his processes as evidenced by reduced variability. This is used as an indicator of both product quality and projected costs. Motorola provides detailed data and inferential statistics that allow customers to make decisions about the product they buy. In many instances, we provide a customer access to our computer data banks in order to improve communications and reduce turnaround time for product approval.

What We Expect From Our Suppliers

Improved quality of incoming material is crucial to success in achieving our Six Sigma goals. In order to accomplish this goal, we feel it necessary to reduce the number of suppliers and to work closely with those remaining as partners to resolve quality issues.

It is the responsibility of Motorola Supplier Quality Control to ensure that all suppliers maintain an adequate system of process and material controls which provides for prevention (as opposed to detection) of defects in their manufacturing processes. This includes, but is not limited to, the following:

- General plan for continuous improvement
- Detailed product flow
- Process control plan
- Equipment and process capability studies
- Measurement system capability studies
- Specific action plan for out-of-control conditions
- Evidence of statistical process control

Motorola's Reliability and Quality Monitor Philosophy

In order to guarantee that the high standards of reliability and quality required by the Motorola continue throughout the entire production lifetime of each product family, an ongoing Reliability Monitor/Audit Program is established.

Individual product and package family monitors are developed by identifying the appropriate device(s) for each process family (in most cases the same device used to qualify a process/product/package family). Once identified, the appropriate stress test programs are put in place to monitor the ongoing process average of the specific family. This process average measurement is made by understanding the reliability and quality results of individual samples. The stresses and sampling used vary according to the product technologies used and the unique requirements of the customer base. In all cases the monitors have been defined so as to quantify the progress being made toward sector goals of six sigma quality and significant reduction in infant mortality, and long term failure rates.

Monitor testing is completed on an ongoing cycle with test results made available quarterly. These reports detail all test results received for the previous quarter, outlining the reliability data associated with all process/package family types.

With all of these data, an effective ongoing monitor is established which is capable of identifying reliability trends associated with all process/product/package families.

For a complete description, order document BR518/D.

Reliability Stress Tests

The following summary gives brief descriptions of the various reliability tests included in a reliability monitor program. Not all of the tests listed are performed by each product group and other tests can be performed when appropriate. In addition some form of preconditioning may be used in conjunction with the following tests.

HIGH TEMPERATURE OPERATING LIFE

High temperature operating life (HTOL or HTRB) testing is performed to accelerate failure mechanisms which are thermally activated through the application of extreme temperatures and the use of biased operating conditions. The temperature and voltage conditions used in the stress will vary with the product being stressed. However, the typical stress ambient is 125°C, with the bias applied equal to or greater than the data sheet nominal value. All devices used in the HTOL test are sampled directly after final electrical test with no prior burn-in or other prescreening unless called out in the normal production flow. Testing can either be performed with dynamic signals applied to the device or in static bias configuration for a typical test duration of 1008 hours.

TEMPERATURE CYCLE

Temperature cycle accelerates the effects of thermal expansion mismatch among the different components within a specific die and packaging system. This test is typically performed per MIL-STD-883 or MIL-STD-750 with the minimum and maximum temperatures being – 65°C and + 150°C. During temperature cycle testing, devices are inserted into a cycling system and held at the cold dwell temperature for at least ten minutes. Following this cold dwell, the devices are heated to the hot dwell where they remain for another ten minute time period. The system employs a circulating air environment to assure rapid stabilization at the specified temperature. The dwell at each extreme, plus the two transition times of five minutes each (one up to the hot dwell temperature, another down to the cold dwell temperature), constitute one cycle. Test duration for this test will vary with device and packaging system employed. Typical test duration is for 1000 cycles with some tests extended to look for longer term effects.

THERMAL SHOCK

The objective of thermal shock testing is the same as that for temperature cycle testing — to emphasize the differences in expansion coefficients of the packaging system. However, thermal shock provides additional stress in that the device is exposed to a sudden change in temperature due to the transfer time of ten seconds maximum as well as the increased thermal conductivity of a liquid ambient. This test is typically performed per MIL-STD-883 or MIL-STD-750 with minimum and maximum temperatures being – 65°C to + 150°C. Devices are placed in a fluorocarbon bath and cooled to minimum specified temperature. After being held in the cold chamber for five minutes minimum, the devices are transferred to an adjacent chamber filled with fluorocarbon at the maximum specified temperature for an equivalent time. Two five-minute dwells plus two ten-second transitions constitute one cycle. Test duration is for normally 1000 cycles with some tests being extended to look for longer term effects.

TEMPERATURE HUMIDITY BIAS

Temperature humidity bias (THB or H3TRB) is an environmental test performed at a temperature of 85°C and a relative humidity of 85%. The test is designed to measure the moisture resistance of plastic encapsulated circuits. A nominal static bias is applied to the device to create the electrolytic cells necessary to accelerate corrosion of the metalization. Most groups are tested to 1008 hours, with some groups extended beyond to look for longer term effects.

AUTOCLAVE

Autoclave is an environmental test that measures device resistance to moisture penetration and the resultant effects of galvanic corrosion. Conditions employed during the test include 121°C, 100% relative humidity, and 15 psig. Corrosion of the die is the expected failure mechanism. Autoclave is a highly accelerated and destructive test. Typical test durations are 48 and 96 hours. This test may be followed by HTOL or HTRB for 24 to 48 hours to further accelerate the corrosion failure mechanism.

HAST/PTHB (PRESSURE-TEMPERATURE-HUMIDITY-BIAS)

This test is performed to accelerate the effects of moisture penetration with the dominant effect being corrosion. This test detects similar failure mechanisms as THB, but at a greatly accelerated rate. Conditions usually employed during this test are a temperature of 121°C or greater, pressure of 15 psig or greater, humidity of 100% (PTHB) or humidity of

85% (HAST), and a bias level that is the nominal rating of the device.

CYCLED TEMPERATURE HUMIDITY BIAS

This test is used to examine devices ability to withstand the combined effects of temperature cycling, high humidity, and voltage (test can be run without bias). This test differs from a typical humidity test in its use of temperature cycling. A typical test condition used is as follows: humidity = 90 to 98%, temperature cycle of 25°C to 65°C, and bias applied = nominal device rating. This test is usually run for 1008 hours.

POWER TEMPERATURE CYCLING

This test is performed on semiconductor devices to determine the effects of alternate exposures to extremes of high and low temperature with operating voltages periodically applied and removed. A typical test condition used is as follows: temperature cycle range = – 40°C to 125°C, bias applied = nominal device rating, and power cycling rate = 5.0 minutes (ON)/5 minutes (OFF). This test is usually run for 1000 cycles.

POWER CYCLING

This test is performed at a constant ambient temperature with operating voltage(s) periodically applied and removed, producing a ΔTJA, typically between 50°C and 150°C. Ambient temperatures range between 25°C and 150°C. A typical test condition used is as follows: ambient temperature 25°C, ΔTJA = 125°C with nominal bias, power "ON" 5.0 minutes and "OFF" 5.0 minutes. This test is usually run for at least 504 hours.

LOW TEMPERATURE OPERATING LIFE

This test is performed primarily to accelerate HCI (hot carrier injection) effects in semiconductor devices by exposing them to room ambient or colder temperatures with the use of biased operating conditions. Threshold shifts or parametric changes are typically the basis for failure. The length of this test will vary with temperature and bias conditions employed.

WRITE/ERASE CYCLING OF EEPROMs

This test is employed to evaluate the effects of repeated programming and erasing excursions on EEPROM devices without corruption of data. This write/erase cycling will usually be performed at an elevated operating temperature for greater than 10,000 cycles.

HIGH TEMPERATURE STORAGE/DATA RETENTION

High temperature storage is performed to measure the stability of semiconductor devices, including the data retention characteristics of EPROM and EEPROM devices, during storage at elevated temperatures with no electrical stress applied. The devices are typically exposed to an ambient of 150°C. An acceleration of charge loss from the storage cell or threshold changes are the expected results. All groups are typically tested to 1008 hours.

SYSTEM SOFT ERROR

System soft error is designed to detect errors caused by impact ionization of silicon by high energy particles. This stress is performed on a system level basis. The system is operated for millions of device hours to obtain an accurate measure of actual system soft error performance. This test is performed on memory devices only.

MECHANICAL SHOCK

This test is typically performed per MIL-STD-883 or MIL-STD-750 and is used to examine the ability of the device to withstand a sudden change in mechanical stress typically due to abrupt changes in motion as seen in handling, transportation, or actual use. A typical test condition would be as follows: acceleration = 1500 g, orientation = Y1 plane, t = 0.5 ms, and number of pulse = 5.

VARIABLE FREQUENCY VIBRATION

This test is typically performed per MIL-STD-883 or MIL-STD-750 and is used to examine the ability of the device to withstand deterioration due to mechanical resonance. A typical test condition is: peak acceleration = 20 g, frequency range = 20 Hz to 20 kHz, and t = 48 minutes.

CONSTANT ACCELERATION

This test is typically performed per MIL-STD-883 or MIL-STD-750 and is used to indicate structural or mechanical weaknesses in a device/packaging system by applying a severe mechanical stress. A typical test condition used is as follows: stress level = 30 kg, orientation = Y1 plane, and t = 1 minute.

SOLDER HEAT

This test is used to examine the device's ability to withstand the temperatures seen in soldering over a more extended period as compared to the typical exposure levels seen in a production process. Electrical testing is the endpoint criterion for this stress.

LEAD INTEGRITY

This test is typically performed per MIL-STD-883 or MIL-STD-750 and is used to examine the mechanical properties of a device's leads, welds, and seals. Various conditions can be employed and provide for: tensile loading, bending stresses, torque or twist, and peel stress. The failure is determined visually under 3X to 10X magnification.

SALT ATMOSPHERE

This test is performed per MIL-STD-883 or MIL-STD-750 and is used to evaluate the corrosive effects of a seacoast type atmosphere on device and package elements. A failure is determined visually under 10X to 20X magnification.

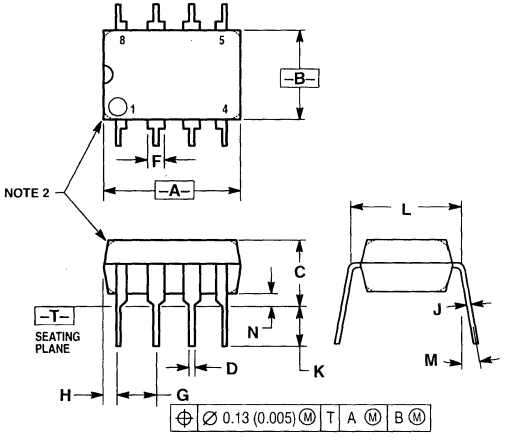
Mechanical Data

8

Package availability for each device is indicated on the front page of the individual data sheets. Dimensions for the packages are given in this chapter.

8–PIN PACKAGES

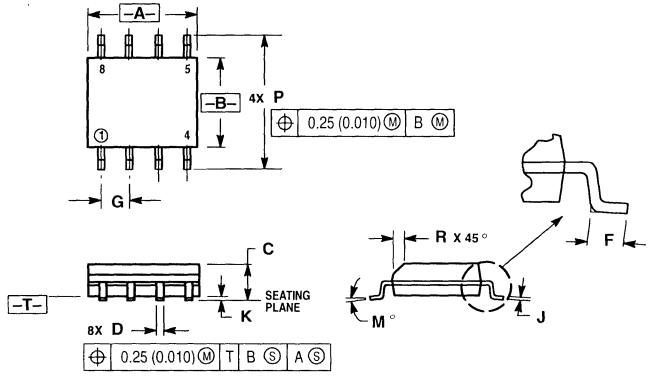
P SUFFIX
PLASTIC DIP (DUAL IN–LINE PACKAGE)
CASE 626–05



NOTES:
1. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
2. PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS).
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.40	10.16	0.370	0.400
B	6.10	6.60	0.240	0.260
C	3.94	4.45	0.155	0.175
D	0.38	0.51	0.015	0.020
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	0.76	1.27	0.030	0.050
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	—	10°	—	10°
N	0.76	1.01	0.030	0.040

D SUFFIX
SOG (SMALL OUTLINE GULL–WING) PACKAGE
CASE 751–05

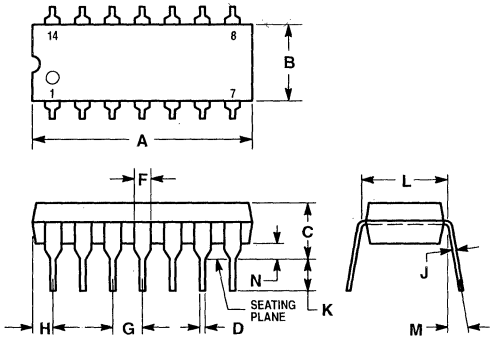


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.196
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.18	0.25	0.007	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

8

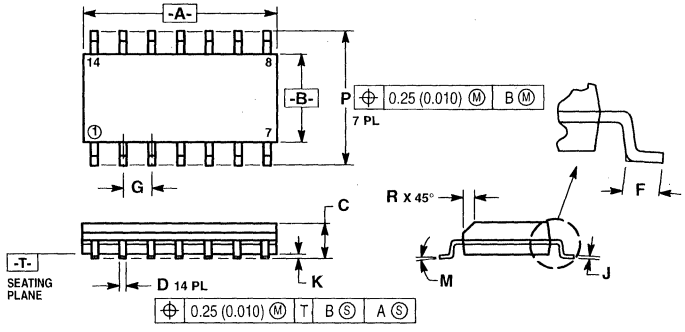
P SUFFIX
PLASTIC DIP (DUAL IN–LINE PACKAGE)
CASE 646–06



NOTES:
1. LEADS WITHIN 0.13 (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
4. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.715	0.770	18.16	19.56
B	0.240	0.260	6.10	6.60
C	0.145	0.185	3.69	4.69
D	0.015	0.021	0.38	0.53
F	0.040	0.070	1.02	1.78
G	0.100 BSC		2.54 BSC	
H	0.052	0.095	1.32	2.41
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.300 BSC		7.62 BSC	
M	0°	10°	0°	10°
N	0.015	0.039	0.39	1.01

D SUFFIX
SOG (SMALL OUTLINE GULL–WING) PACKAGE
CASE 751A–03

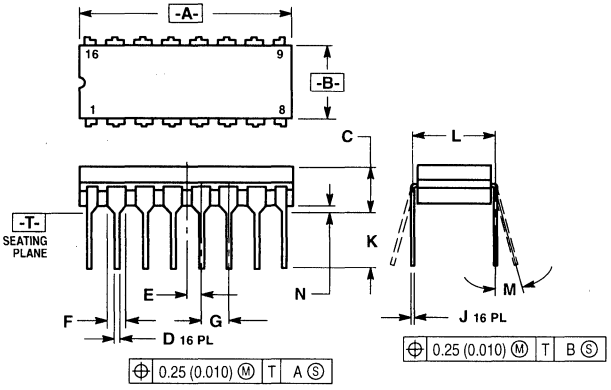


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.299	0.244
R	0.25	0.50	0.010	0.019

8

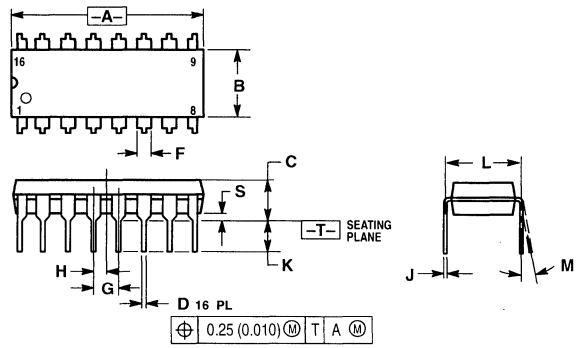
L SUFFIX
CERAMIC PACKAGE
CASE 620–10



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.750	0.770	19.05	19.55
B	0.240	0.290	6.10	7.36
C	—	0.165	—	4.19
D	0.015	0.021	0.39	0.53
E	0.050 BSC		1.27 BSC	
F	0.055	0.070	1.40	1.77
G	0.100 BSC		2.54 BSC	
J	0.009	0.011	0.23	0.27
K	—	0.200	—	5.08
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.015	0.035	0.39	0.88

P SUFFIX
PLASTIC DIP (DUAL IN–LINE PACKAGE)
CASE 648–08

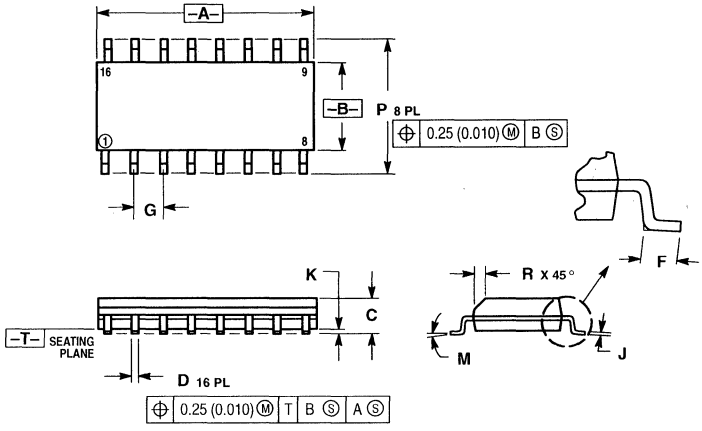


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

8

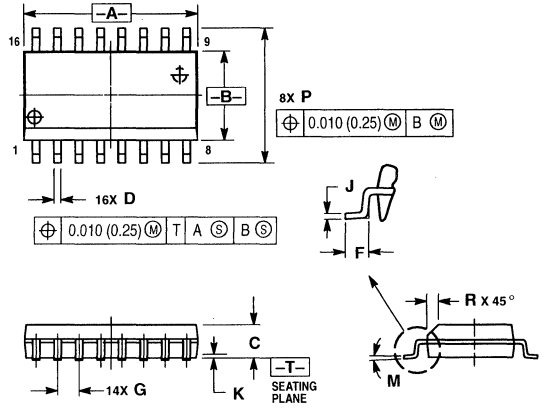
D SUFFIX
SOG (SMALL OUTLINE GULL–WING) PACKAGE
CASE 751B–05



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

DW SUFFIX
SOG (SMALL OUTLINE GULL–WING) PACKAGE
CASE 751G–02

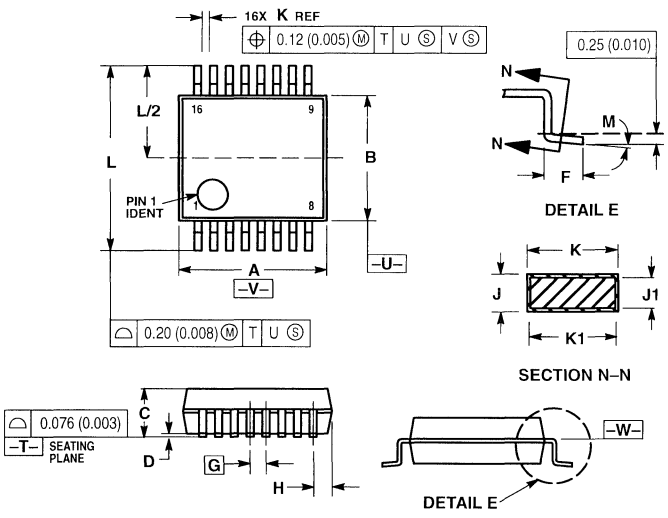


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	10.15	10.45	0.400	0.411
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

8

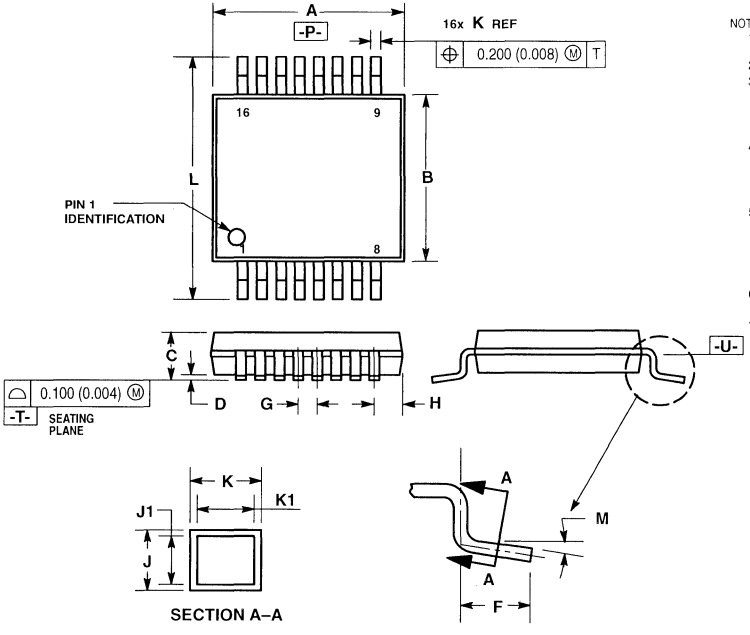
SD SUFFIX
SSOP (SMALL SHRINK OUTLINE PACKAGE)
CASE 940B–02



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF K DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR INTRUSION SHALL NOT REDUCE DIMENSION K BY MORE THAN 0.07 (0.002) AT LEAST MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	6.07	6.33	0.238	0.249
B	5.20	5.38	0.205	0.212
C	1.73	1.99	0.068	0.078
D	0.05	0.21	0.002	0.008
F	0.63	0.95	0.024	0.037
G	0.65 BSC		0.026 BSC	
H	0.73	0.90	0.028	0.035
J	0.09	0.20	0.003	0.008
J1	0.09	0.16	0.003	0.006
K	0.25	0.38	0.010	0.015
K1	0.25	0.33	0.010	0.013
L	7.65	7.90	0.301	0.311
M	0 °	8 °	0 °	8 °

DT SUFFIX
TSSOP (THIN SHRINK SMALL OUTLINE PACKAGE)
CASE 948C–03

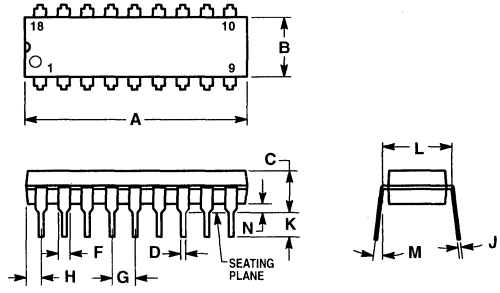


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSIONS A AND B ARE TO BE DETERMINED AT DATUM PLANE –U–.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	—	5.10	—	0.200
B	4.30	4.50	0.169	0.177
C	—	1.20	—	0047
D	0.05	0.25	0.002	0.010
F	0.45	0.55	0.018	0.022
G	0.65 BSC		0.026 BSC	
H	0.22	0.23	0.009	0.010
J	0.09	0.24	0.004	0.009
J1	0.09	0.18	0.004	0.007
K	0.16	0.32	0.006	0.013
K1	0.16	0.26	0.006	0.010
L	6.30	6.50	0.248	0.256
M	0°	10°	0 °	10°

8

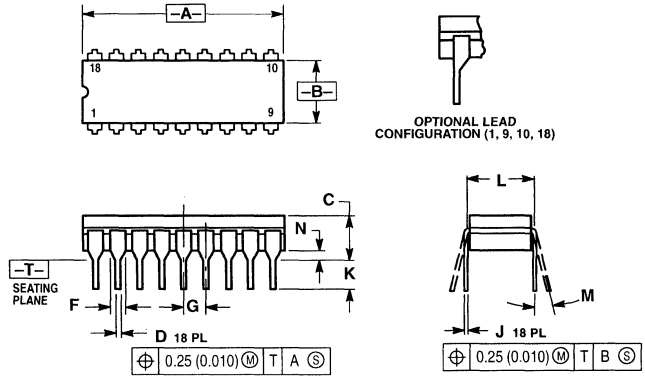
P SUFFIX
PLASTIC DIP (DUAL IN–LINE PACKAGE)
CASE 707–02



NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	22.22	23.24	0.875	0.915
B	6.10	6.60	0.240	0.260
C	3.56	4.57	0.140	0.180
D	0.36	0.56	0.014	0.022
F	1.27	1.78	0.050	0.070
G	2.54 BSC		0.100 BSC	
H	1.02	1.52	0.040	0.060
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

L SUFFIX
CERAMIC PACKAGE
CASE 726–04

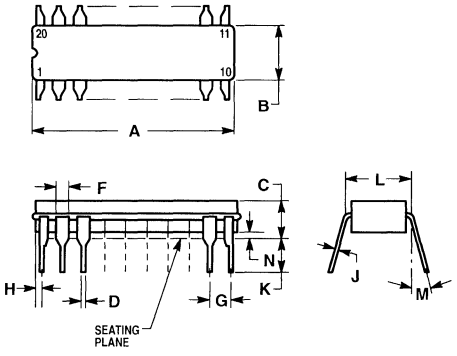


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION F FOR FULL LEADS. HALF LEADS OPTIONAL AT LEAD POSITIONS 1, 9, 10, AND 18.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.880	0.910	22.35	23.11
B	0.240	0.295	6.10	7.49
C	—	0.200	—	5.08
D	0.015	0.021	0.38	0.53
F	0.055	0.070	1.40	1.78
G	0.100 BSC		2.54 BSC	
J	0.008	0.012	0.20	0.30
K	0.125	0.170	3.18	4.32
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.02

8

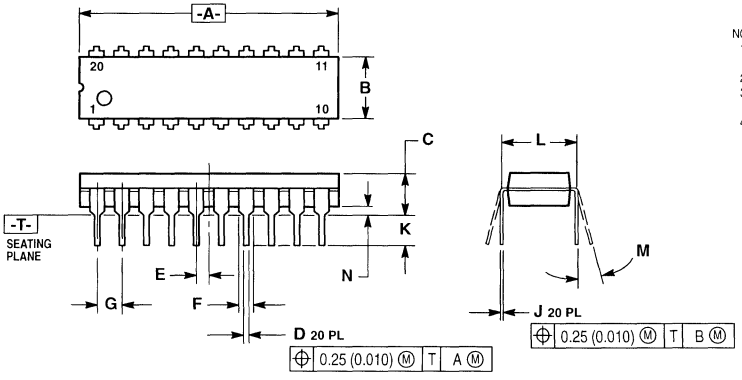
L SUFFIX
CERAMIC PACKAGE
CASE 732–03



NOTES:
1. LEADS WITHIN 0.25 (0.010) DIAMETER, TRUE POSITION AT SEATING PLANE, AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSIONS A AND B INCLUDE MENISCUS.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	23.88	25.15	0.940	0.990
B	6.60	7.49	0.260	0.295
C	3.81	5.08	0.150	0.200
D	0.38	0.56	0.015	0.022
F	1.40	1.65	0.055	0.065
G	2.54 BSC		0.100 BSC	
H	0.51	1.27	0.020	0.050
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.25	1.02	0.010	0.040

P SUFFIX
PLASTIC DIP (DUAL IN–LINE PACKAGE)
CASE 738–03

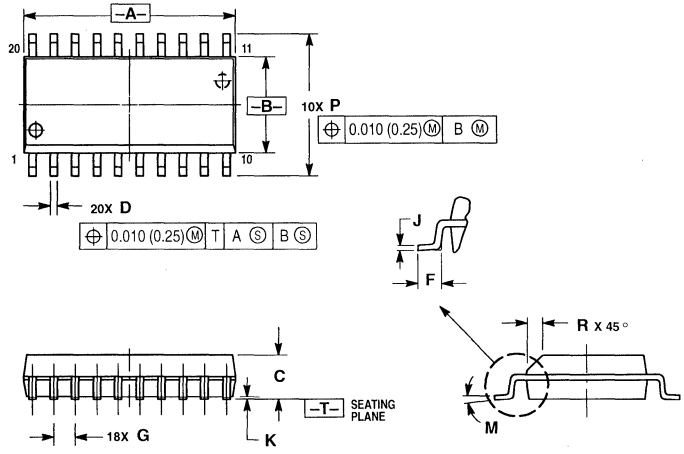


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.010	1.070	25.66	27.17
B	0.240	0.260	6.10	6.60
C	0.150	0.180	3.81	4.57
D	0.015	0.022	0.39	0.55
E	0.050 BSC		1.27 BSC	
F	0.050	0.070	1.27	1.77
G	0.100 BSC		2.54 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.140	2.80	3.55
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

8

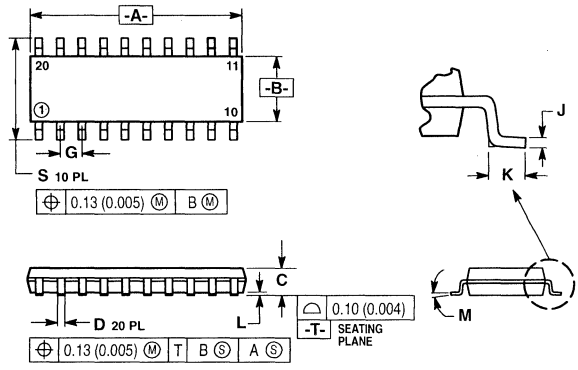
DW SUFFIX
SOG (SMALL OUTLINE GULL–WING) PACKAGE
CASE 751D–04



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.150 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	12.65	12.95	0.499	0.510
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

F SUFFIX
SOG (SMALL OUTLINE GULL–WING) PACKAGE
CASE 751J–02

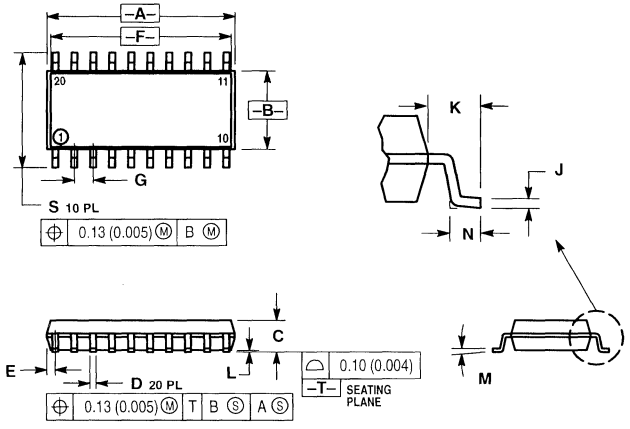


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	12.55	12.80	0.494	0.504
B	5.10	5.40	0.201	0.213
C	—	2.00	—	0.079
D	0.35	0.45	0.014	0.018
G	1.27 BSC		0.050 BSC	
J	0.18	0.23	0.007	0.009
K	0.55	0.85	0.022	0.033
L	0.05	0.20	0.002	0.008
M	0°	7°	0°	7°
S	7.40	8.20	0.291	0.323

8

F SUFFIX
SOG (SMALL OUTLINE GULL–WING) PACKAGE
CASE 803C–01

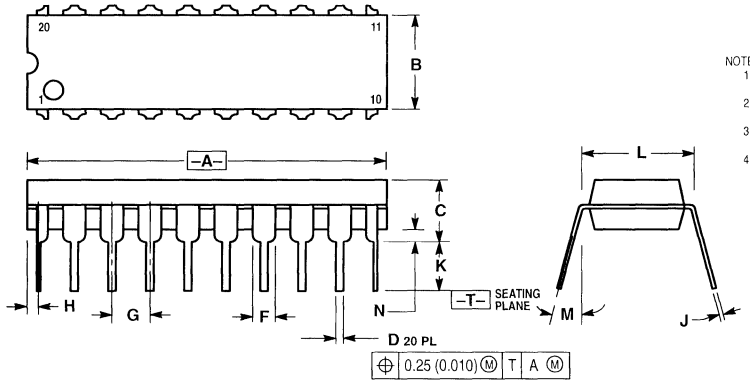


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.008) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.006) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	12.35	12.80	0.486	0.504
B	5.10	5.45	0.201	0.215
C	1.95	2.05	0.077	0.081
D	0.35	0.50	0.014	0.020
E	—	0.81	—	0.032
F	12.40*		0.488*	
G	1.15	1.39	0.045	0.055
H	0.59	0.81	0.023	0.032
J	0.18	0.27	0.007	0.011
K	1.10	1.50	0.043	0.059
L	0.05	0.20	0.001	0.008
M	0°	10°	0°	10°
N	0.50	0.85	0.020	0.033
S	7.40	8.20	0.291	0.323

*APPROXIMATE

H SUFFIX
PLASTIC DIP (DUAL IN–LINE PACKAGE)
CASE 804–01

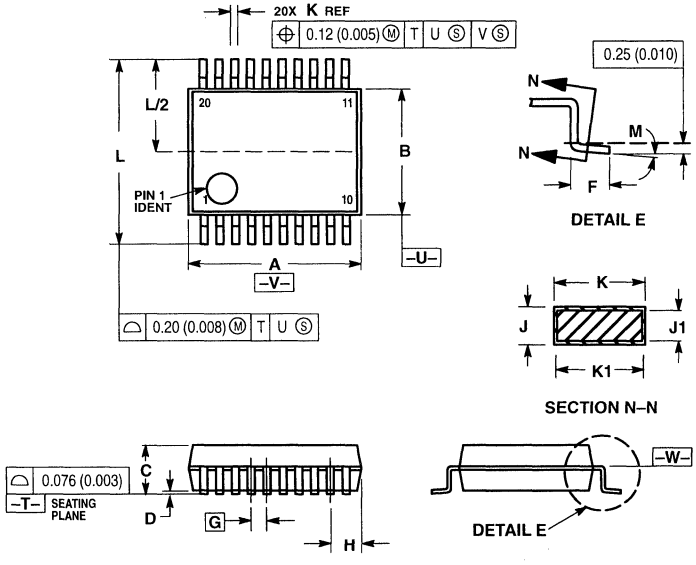


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.930	0.970	23.63	24.63
B	0.240	0.260	6.10	6.60
C	0.150	0.170	3.81	4.31
D	0.015	0.022	0.38	0.56
F	0.050	0.070	1.27	1.78
G	0.100 BSC		2.54 BSC	
H	0.030 NOM		0.76 NOM	
J	0.009	0.013	0.23	0.33
K	0.115	0.140	2.93	3.55
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.02

8

VF SUFFIX
SSOP (SMALL SHRINK OUTLINE PACKAGE)
CASE 940C–03

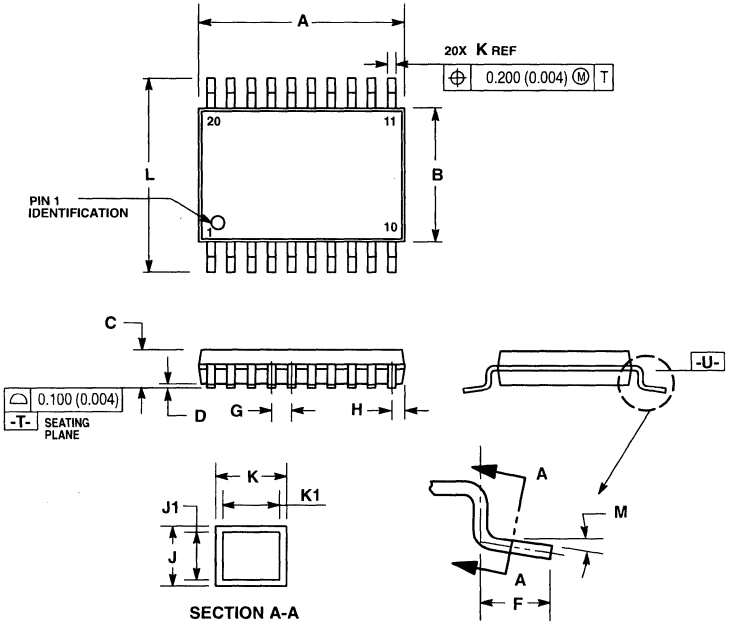


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF K DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR INTRUSION SHALL NOT REDUCE DIMENSION K BY MORE THAN 0.07 (0.002) AT LEAST MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	7.07	7.33	0.278	0.288
B	5.20	5.38	0.205	0.212
C	1.73	1.99	0.068	0.078
D	0.05	0.21	0.002	0.008
F	0.63	0.95	0.024	0.037
G	0.65 BSC		0.026 BSC	
H	0.59	0.75	0.023	0.030
J	0.09	0.20	0.003	0.008
J1	0.09	0.16	0.003	0.006
K	0.25	0.38	0.010	0.015
K1	0.25	0.33	0.010	0.013
L	7.65	7.90	0.301	0.311
M	0°	8°	0°	8°

8

DT SUFFIX
TSSOP (THIN SMALL SHRINK OUTLINE PACKAGE)
CASE 948D–03

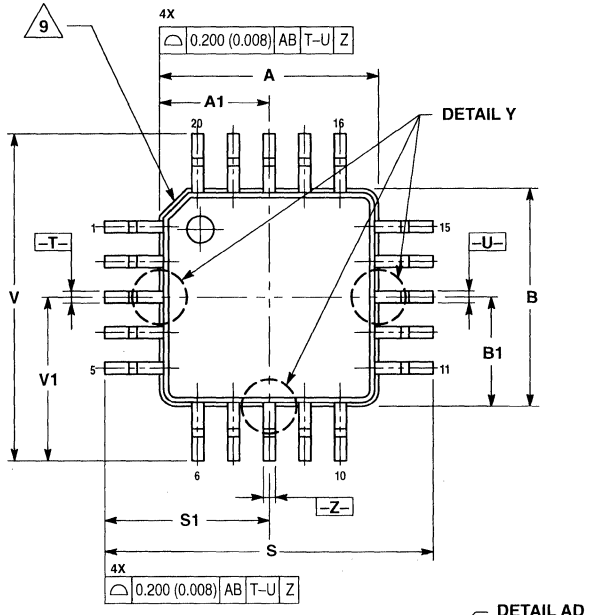


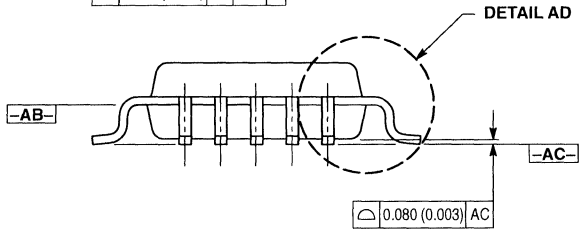
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSIONS A AND B ARE TO BE DETERMINED AT DATUM PLANE -U-.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	—	6.60	—	0.260
B	4.30	4.50	0.169	0.177
C	—	1.20	—	0.047
D	0.05	0.25	0.002	0.010
F	0.45	0.55	0.018	0.022
G	0.65 BSC		0.026 BSC	
H	0.275	0.375	0.011	0.015
J	0.09	0.24	0.004	0.009
J1	0.09	0.18	0.004	0.007
K	0.16	0.32	0.006	0.013
K1	0.16	0.26	0.006	0.010
L	6.30	6.50	0.248	0.256
M	0°	10°	0°	10°

8

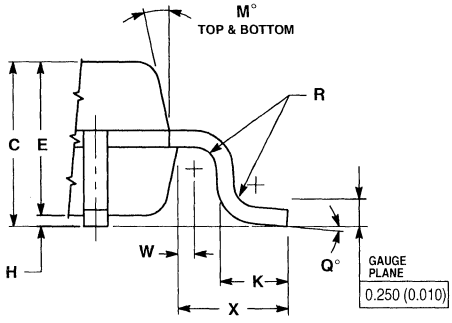
FTB SUFFIX
TQFP (THIN QUAD FLAT PACKAGE)
CASE 976–01



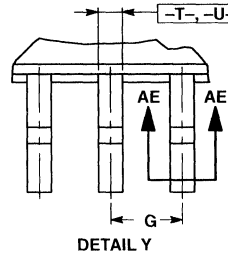


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE –AB– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS –T–, –U–, AND –Z– TO BE DETERMINED AT DATUM PLANE –AB–.
5. DIMENSIONS S AND V TO BE DETERMINED AT DATUM PLANE –AC–.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –AB–.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.350 (0.014).
8. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076 (0.0003).
9. EXACT SHAPE OF EACH CORNER IS OPTIONAL.

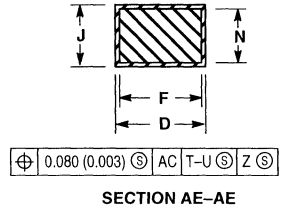
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.000 BSC		0.157 BSC	
A1	2.000 BSC		0.079 BSC	
B	4.000 BSC		0.157 BSC	
B1	2.000 BSC		0.079 BSC	
C	1.400	1.600	0.055	0.063
D	0.170	0.270	0.007	0.011
E	1.350	1.450	0.053	0.057
F	0.170	0.230	0.007	0.009
G	0.650 BSC		0.026 BSC	
H	0.050	0.150	0.002	0.006
J	0.090	0.200	0.004	0.008
K	0.500	0.700	0.020	0.028
M	12°REF		12°REF	
N	0.090	0.160	0.004	0.006
P	0.250 BSC		0.010 BSC	
Q	1°	5°	1°	5°
R	0.150	0.250	0.006	0.010
S	6.000 BSC		0.236 BSC	
S1	3.000 BSC		0.118 BSC	
V	6.000 BSC		0.236 BSC	
V1	3.000 BSC		0.118 BSC	
W	0.200 REF		0.008 REF	
X	1.000 REF		0.039 REF	



DETAIL AD



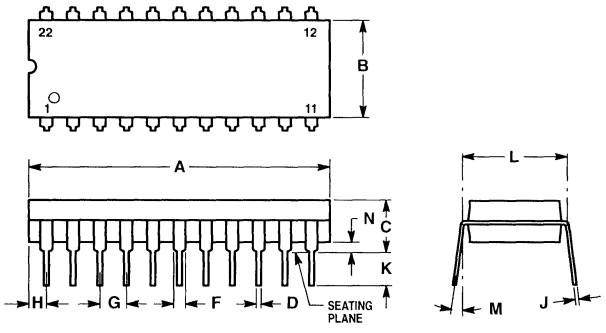
DETAIL Y



SECTION AE–AE

8

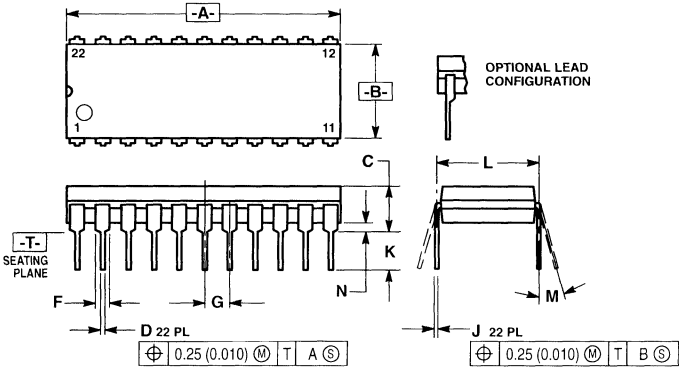
P SUFFIX
PLASTIC DIP (DUAL IN–LINE PACKAGE)
CASE 708–04



NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	27.56	28.32	1.085	1.115
B	8.64	9.14	0.340	0.360
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.27	1.78	0.050	0.070
G	2.54 BSC		0.100 BSC	
H	1.02	1.52	0.040	0.060
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	10.16 BSC		0.400 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

L SUFFIX
CERAMIC PACKAGE
CASE 736–05

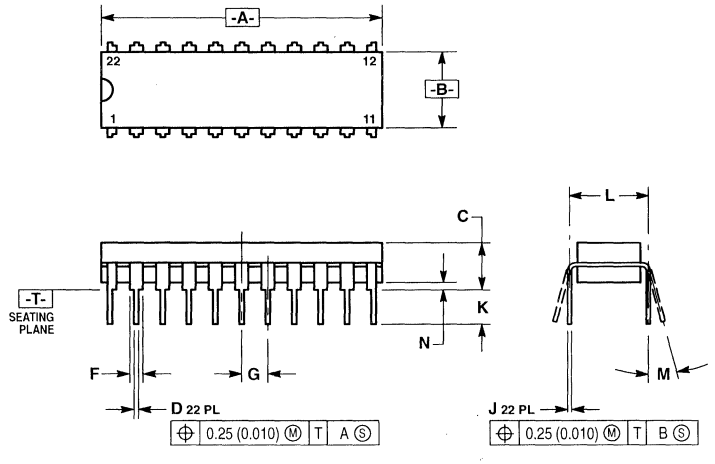


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION F FOR FULL LEADS. HALF LEADS OPTIONAL AT LEAD POSITIONS 1, 11, 12, AND 22.
5. DIMENSION F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.060	1.095	26.93	27.81
B	0.360	0.390	9.15	9.90
C	0.150	0.215	3.81	5.46
D	0.015	0.021	0.39	0.53
F	0.050	0.065	1.27	1.65
G	0.100 BSC		2.54 BSC	
J	0.008	0.015	0.20	0.39
K	0.125	0.170	3.18	4.31
L	0.400 BSC		10.16 BSC	
M	0°	15°	0°	15°
N	0.020	0.050	0.51	1.27

8

P SUFFIX
PLASTIC DIP (DUAL IN–LINE PACKAGE)
CASE 736B–01

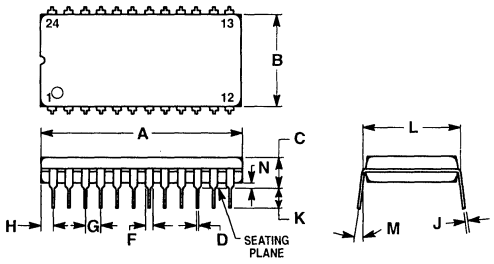


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSIONS A AND B DOES NOT INCLUDE MOLD FLASH. MAXIMUM MOLD FLASH 0.25 (0.010).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.060	1.070	26.92	27.17
B	0.280	0.300	7.12	7.62
C	0.150	0.180	3.81	4.57
D	0.015	0.021	0.39	0.53
F	0.045	0.055	1.15	1.39
G	0.100 BSC		2.54 BSC	
J	0.008	0.012	0.21	0.30
K	0.125	0.135	3.18	3.42
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

8

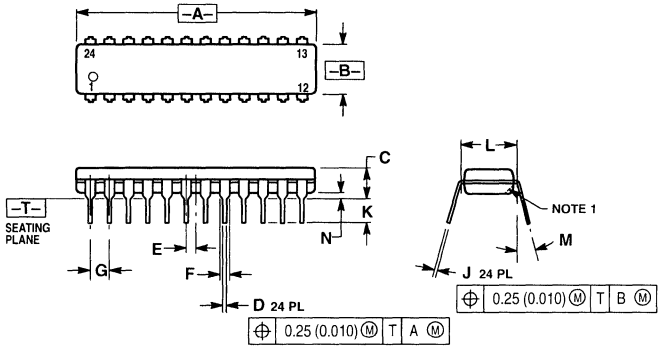
P SUFFIX
PLASTIC DIP (DUAL IN–LINE PACKAGE)
CASE 709–02



NOTES.
1 POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3 DIMENSION B DOES NOT INCLUDE MOLD FLASH.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	31.37	32.13	1.235	1.265
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.03	0.065	0.080
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

P SUFFIX
PLASTIC DIP (DUAL IN–LINE PACKAGE)
CASE 724–03

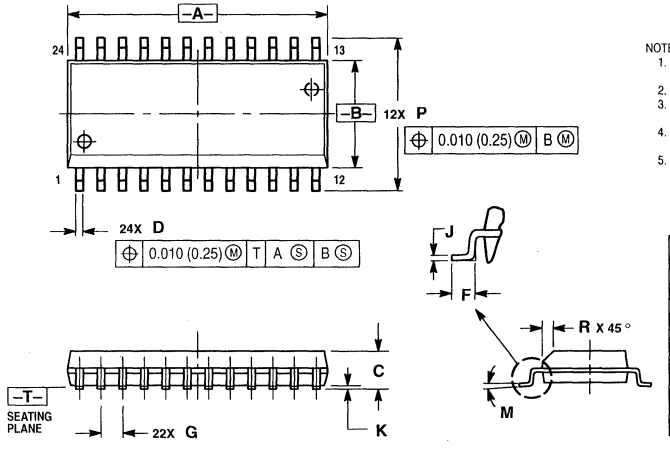


NOTES.
1. CHAMFERED CONTOUR OPTIONAL.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
4. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.230	1.265	31.25	32.13
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.020	0.38	0.51
E	0.050 BSC		1.27 BSC	
F	0.040	0.060	1.02	1.52
G	0.100 BSC		2.54 BSC	
J	0.007	0.012	0.18	0.30
K	0.110	0.140	2.80	3.55
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

8

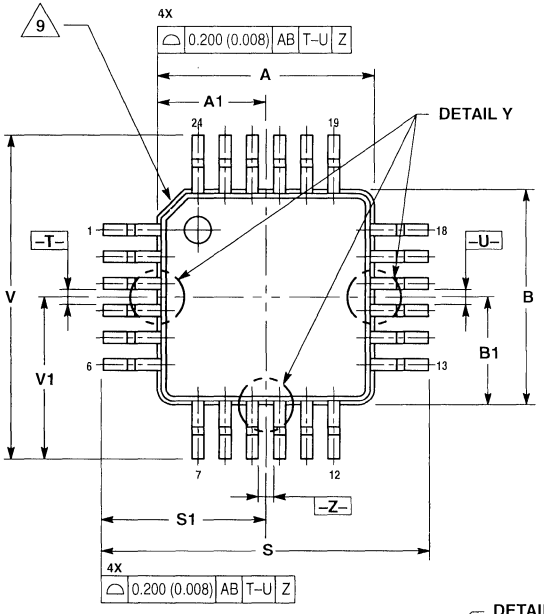
DW SUFFIX
SOG (SMALL OUTLINE GULL–WING) PACKAGE
CASE 751E–04

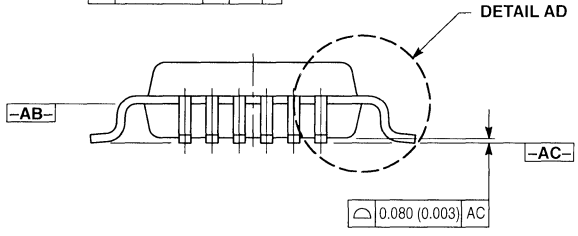


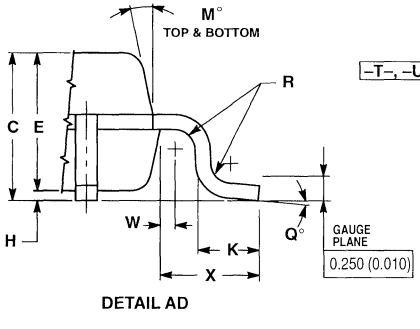
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	15.25	15.54	0.601	0.612
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.41	0.90	0.016	0.035
G	1.27 BSC		0.050 BSC	
J	0.23	0.32	0.009	0.013
K	0.13	0.29	0.005	0.011
M	0°	8°	0°	8°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

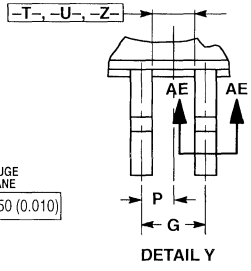
FTA SUFFIX
TQFP (THIN QUAD FLAT PACKAGE)
CASE 977–01



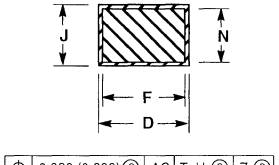




DETAIL AD



DETAIL Y



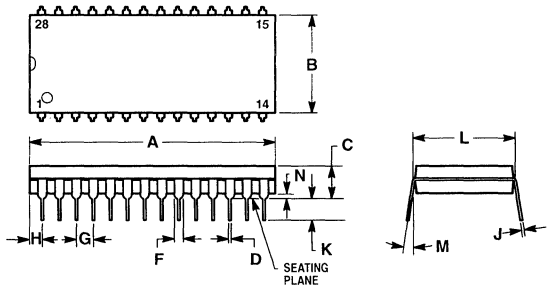
SECTION AE–AE

NOTES.
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE –AB– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS –T–, –U–, AND –Z– TO BE DETERMINED AT DATUM PLANE –AB–.
5. DIMENSIONS S AND V TO BE DETERMINED AT DATUM PLANE –AC–.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 (0.010) PER SIDE DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –AB–.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0 .350 (0.014).
8. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076 (0.0003).
9. EXACT SHAPE OF EACH CORNER IS OPTIONAL.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.000 BSC		0.157 BSC	
A1	2.000 BSC		0.079 BSC	
B	4.000 BSC		0.157 BSC	
B1	2.000 BSC		0.079 BSC	
C	1.400	1.600	0.055	0.063
D	0.170	0.270	0.007	0.011
E	1.350	1.450	0.053	0.057
F	0.170	0.230	0.007	0.009
G	0.500 BSC		0.020 BSC	
H	0.050	0.150	0.002	0.006
J	0.090	0.200	0.004	0.008
K	0.500	0.700	0.020	0.028
M	12° REF		12° REF	
N	0.090	0.160	0.004	0.006
P	0.250 BSC		0.010 BSC	
Q	1°	5°	1°	5°
R	0.150	0.250	0.006	0.010
S	6.000 BSC		0.236 BSC	
S1	3.000 BSC		0.118 BSC	
V	6.000 BSC		0.236 BSC	
V1	3.000 BSC		0.118 BSC	
W	0.200 REF		0.008 REF	
X	1.000 REF		0.039 REF	

8

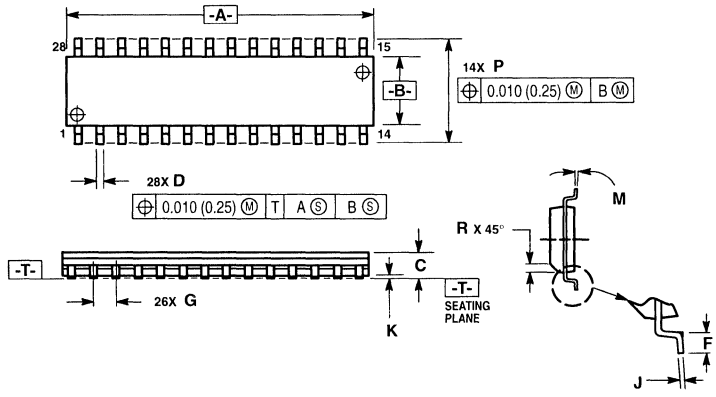
P SUFFIX
PLASTIC DIP (DUAL IN–LINE PACKAGE)
CASE 710–02



NOTES.
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25mm (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	36.45	37.21	1.435	1.465
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

DW SUFFIX
SOG (SMALL OUTLINE GULL–WING) PACKAGE
CASE 751F–04

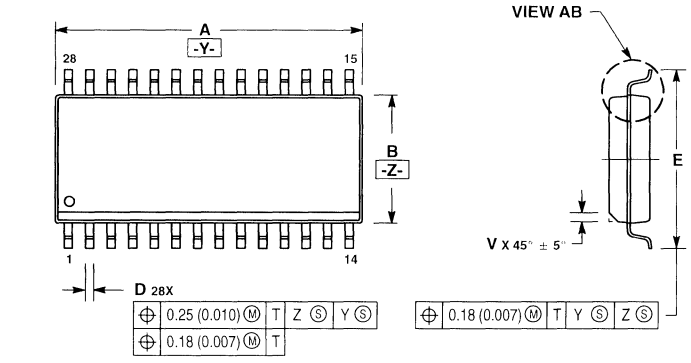


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	17.80	18.05	0.701	0.711
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.41	0.90	0.016	0.035
G	1.27 BSC		0.050 BSC	
J	0.23	0.32	0.009	0.013
K	0.13	0.29	0.005	0.011
M	0°	8°	0°	8°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

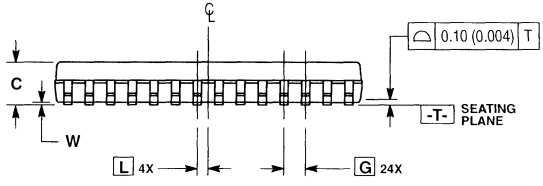
8

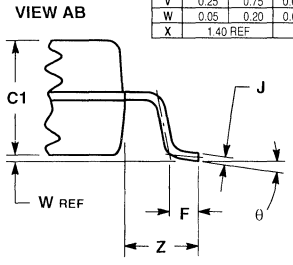
FW SUFFIX
SOG (SMALL OUTLINE GULL–WING) PACKAGE
CASE 751M–01



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. MAXIMUM MOLD PROTRUSION SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.65 (0.026).

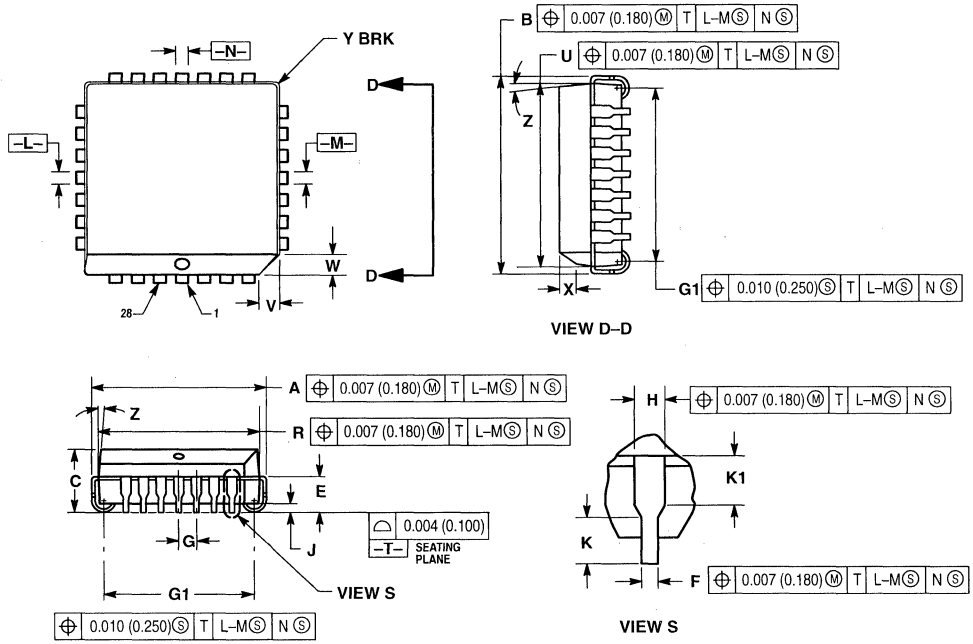
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	17.80	18.03	0.701	0.710
B	7.40	7.62	0.291	0.300
C	—	2.65	—	0.104
C1	2.25	2.45	0.090	0.096
D	0.35	0.51	0.014	0.020
E	10.00	10.60	0.394	0.414
F	0.40	0.70	0.016	0.028
G	1.27 BSC		0.050 BSC	
J	0.10	0.25	0.004	0.010
L	0.635 BSC		0.025 BSC	
θ	—	8°	—	8°
V	0.25	0.75	0.010	0.030
W	0.05	0.20	0.002	0.008
X	1.40 REF		0.110 REF	





8

FN SUFFIX
PLCC (PLASTIC LEADED CHIP CARRIER) PACKAGE
CASE 776–02

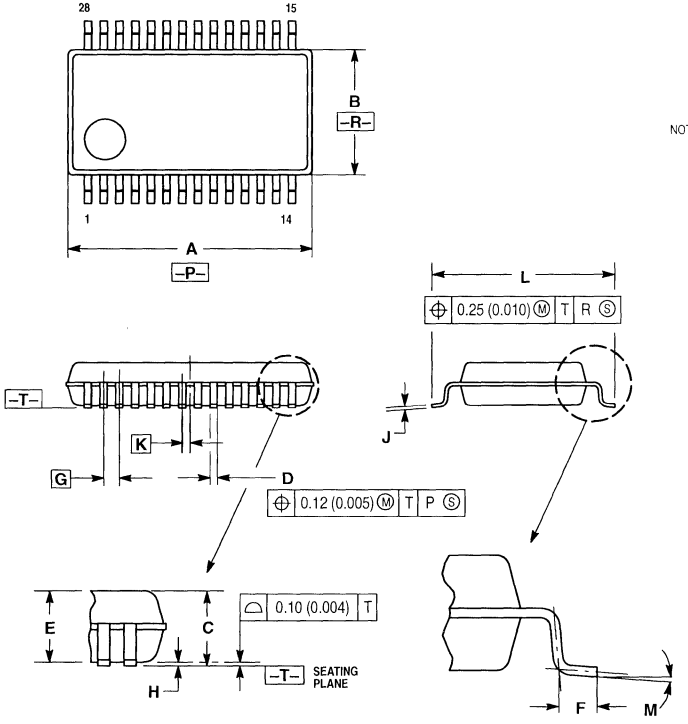


NOTES:
1. DATUMS –L–, –M–, AND –N– DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
2. DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM –T–, SEATING PLANE.
3. DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.
6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
7. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.485	0.495	12.32	12.57
B	0.485	0.495	12.32	12.57
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	—	0.51	—
K	0.025	—	0.64	—
R	0.450	0.456	11.43	11.58
U	0.450	0.456	11.43	11.58
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	—	0.020	—	0.50
Z	2°	10°	2°	10°
G1	0.410	0.430	10.42	10.92
K1	0.040	—	1.02	—

8

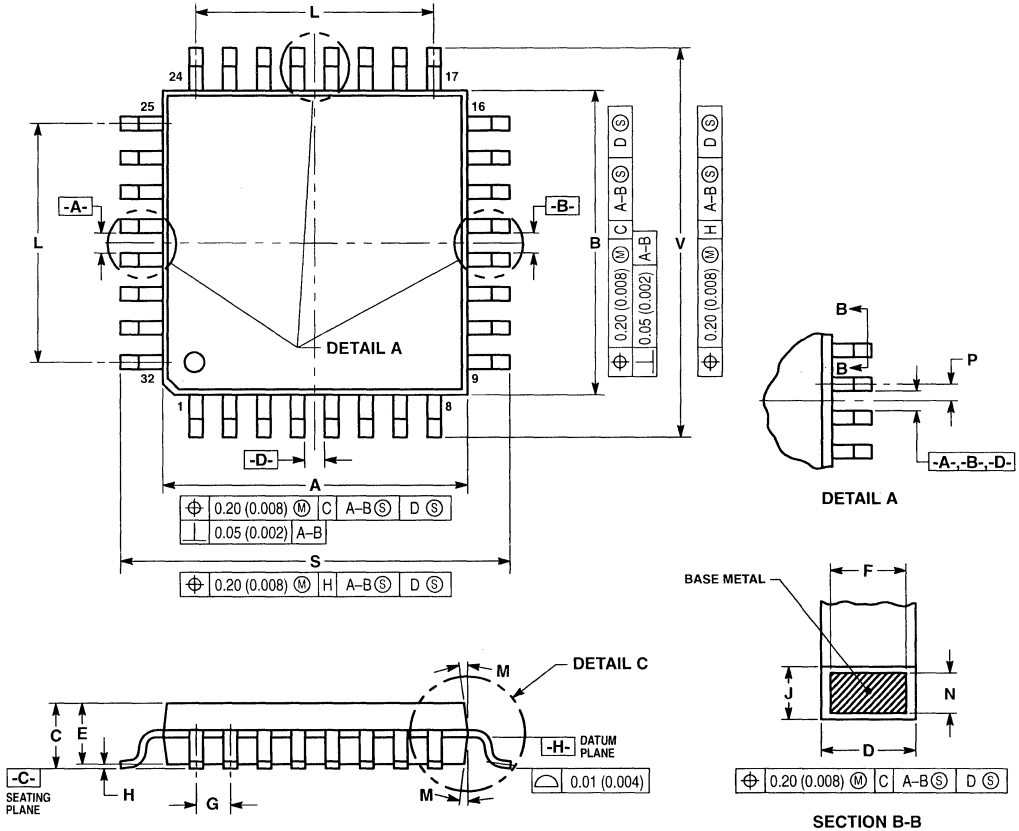
VF SUFFIX
SSOP (SMALL SHRINK OUTLINE PACKAGE)
CASE 940J–01

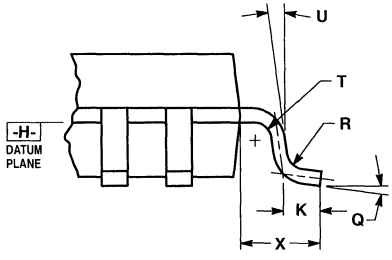


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROSTRUSION. MOLD PROTRUSION IS 0.15 (0.006) MAX PER SIDE.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	10.10	10.20	0.398	0.402
B	5.20	5.30	0.205	0.209
C	—	2.00	—	0.079
D	0.20	0.40	0.008	0.016
E	1.75	1.85	0.069	0.073
F	0.45	0.75	0.018	0.030
G	0.65 BSC		0.0256 BSC	
H	0.00	0.15	0.000	0.006
J	0.10	0.20	0.004	0.008
K	0.325 BSC		0.0128 BSC	
L	7.50	7.90	0.295	0.311
M	1°	7°	1°	7°

FTB SUFFIX
TQFP (THIN QUAD FLAT PACKAGE)
CASE 873–01





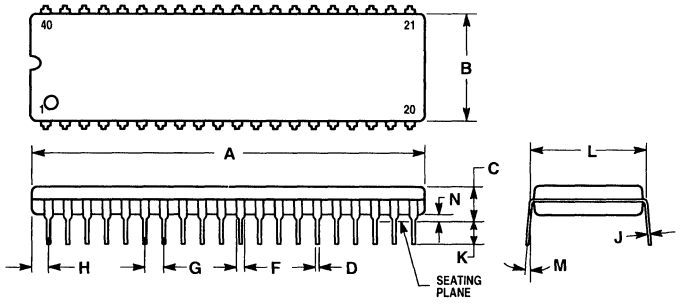
DETAIL C

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE -H- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS -A-, -B- AND -D- TO BE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE -C-.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	6.95	7.10	0.274	0.280
B	6.95	7.10	0.274	0.280
C	1.40	1.60	0.055	0.063
D	0.273	0.373	0.010	0.015
E	1.30	1.50	0.051	0.059
F	0.273	—	0.010	—
G	0.80 BSC		0.031 BSC	
H	—	0.20	—	0.008
J	0.119	0.197	0.005	0.008
K	0.33	0.57	0.013	0.022
L	5.6 REF		0.220 REF	
M	6°	8°	6°	8°
N	0.119	0.135	0.005	0.005
P	0.40 BSC		0.016 BSC	
Q	5°	10°	5°	10°
R	0.15	0.25	0.006	0.010
S	8.85	9.15	0.348	0.360
T	0.15	0.25	0.006	0.010
U	5°	11°	5°	11°
V	8.85	9.15	0.348	0.360
X	1.0 REF		0.039 REF	

8

P SUFFIX
PLASTIC DIP (DUAL IN–LINE PACKAGE)
CASE 711–03

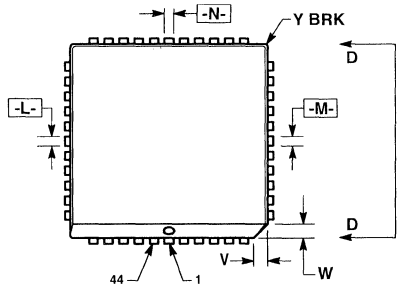


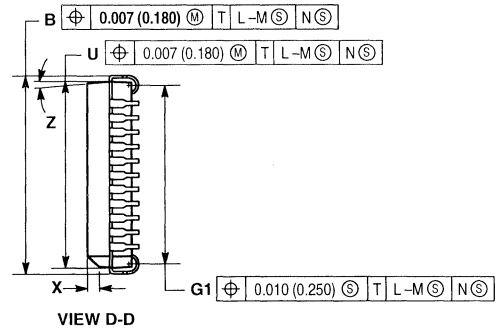
NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	51.69	52.45	2.035	2.065
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

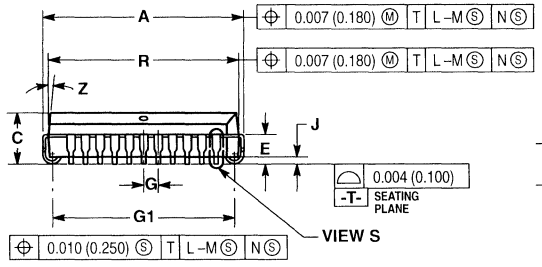
8

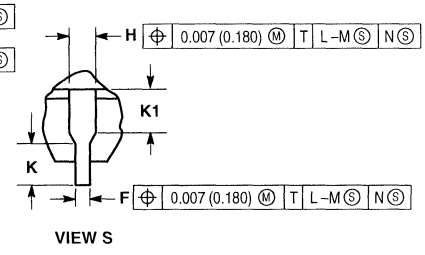
FN SUFFIX
PLCC (PLASTIC LEADED CHIP CARRIER) PACKAGE
CASE 777–02





VIEW D-D





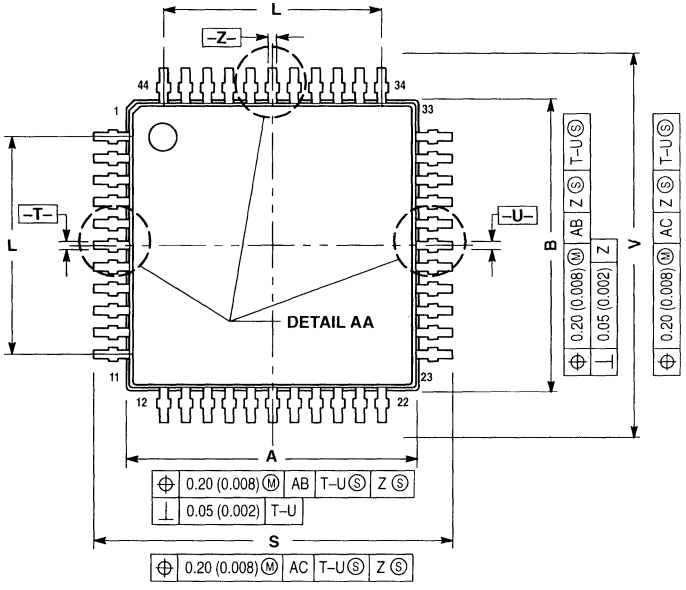
VIEW S

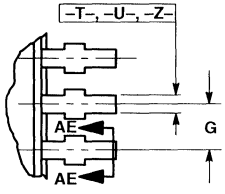
NOTES:
1. DATUMS -L-, -M-, AND -N- DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
2. DIM G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
3. DIM R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS (0.010) 0.25 PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.
6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
7. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.685	0.695	17.40	17.65
B	0.685	0.695	17.40	17.65
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	—	0.51	—
K	0.025	—	0.64	—
R	0.650	0.656	16.51	16.66
U	0.650	0.656	16.51	16.66
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	—	0.020	—	0.50
Z	2°	10°	2°	10°
G1	0.610	0.630	15.50	16.00
K1	0.040	—	1.02	—

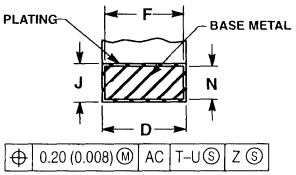
8

PB SUFFIX
TQFP (THIN QUAD FLAT PACKAGE)
CASE 824D–01

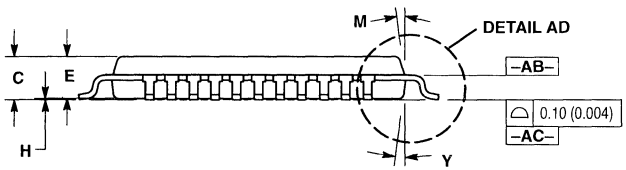


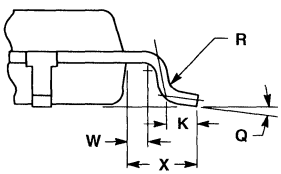


DETAIL AA



SECTION AE–AE





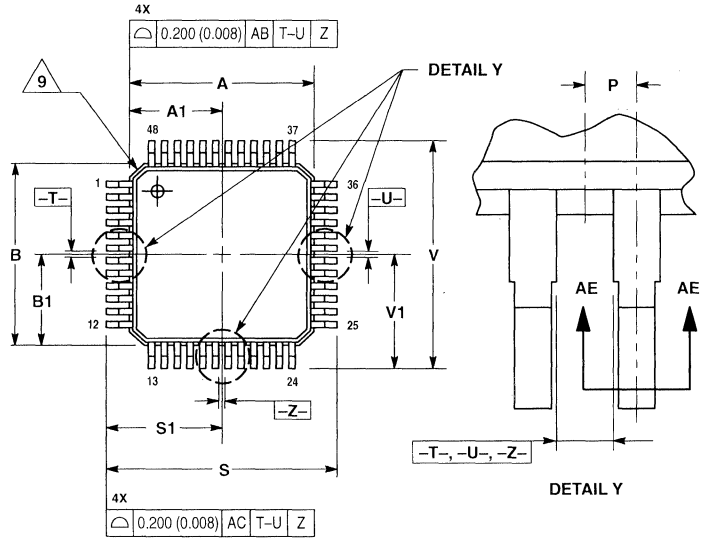
VIEW AD

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE –AB– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS –T–, –U– AND –Z– TO BE DETERMINED AT DATUM PLANE –AB–.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE –AC–.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –AB–.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.530 (0.021).

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.950	10.050	0.392	0.396
B	9.950	10.050	0.392	0.396
C	1.400	1.600	0.055	0.063
D	0.300	0.450	0.012	0.018
E	1.350	1.450	0.053	0.057
F	0.300	0.400	0.012	0.016
G	0.800 BSC		0.031 BSC	
H	0.050	0.150	0.002	0.006
J	0.090	0.200	0.004	0.008
K	0.450	0.550	0.018	0.022
L	8.000 BSC		0.315 BSC	
M	12° REF		12° REF	
N	0.090	0.160	0.004	0.006
Q	1°	5°	1°	5°
R	0.100	0.200	0.004	0.008
S	11.900	12.100	0.469	0.476
V	11.900	12.100	0.469	0.476
W	0.200 REF		0.008 REF	
X	1.000 REF		0.039 REF	
Y	12° REF		12° REF	

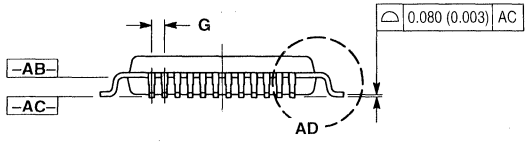
8

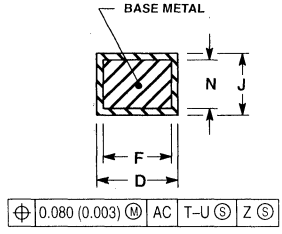
VFU SUFFIX
VQFP
CASE 932–02

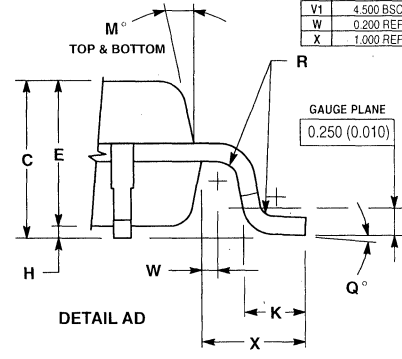


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE -AB- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS -T-, -U-, AND -Z- TO BE DETERMINED AT DATUM PLANE -AB-.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE -AC-.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -AB-.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.350 (0.014).
8. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076 (0.0003).
9. EXACT SHAPE OF EACH CORNER IS OPTIONAL.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	7.000 BSC		0.276 BSC	
A1	3.500 BSC		0.138 BSC	
B	7.000 BSC		0.276 BSC	
B1	3.500 BSC		0.138 BSC	
C	1.400	1.600	0.055	0.063
D	0.170	0.270	0.007	0.011
E	1.350	1.450	0.053	0.057
F	0.170	0.230	0.007	0.009
G	0.500 BASIC		0.020 BASIC	
H	0.050	0.150	0.002	0.006
J	0.090	0.200	0.004	0.008
K	0.500	0.700	0.020	0.028
M	12°REF		12°REF	
N	0.090	0.160	0.004	0.006
P	0.250 BASIC		0.010 BASIC	
Q	1°	5°	1°	5°
R	0.150	0.250	0.006	0.010
S	9.000 BSC		0.354 BSC	
S1	4.500 BSC		0.177 BSC	
V	9.000 BSC		0.354 BSC	
V1	4.500 BSC		0.177 BSC	
W	0.200 REF		0.008 REF	
X	1.000 REF		0.039 REF	

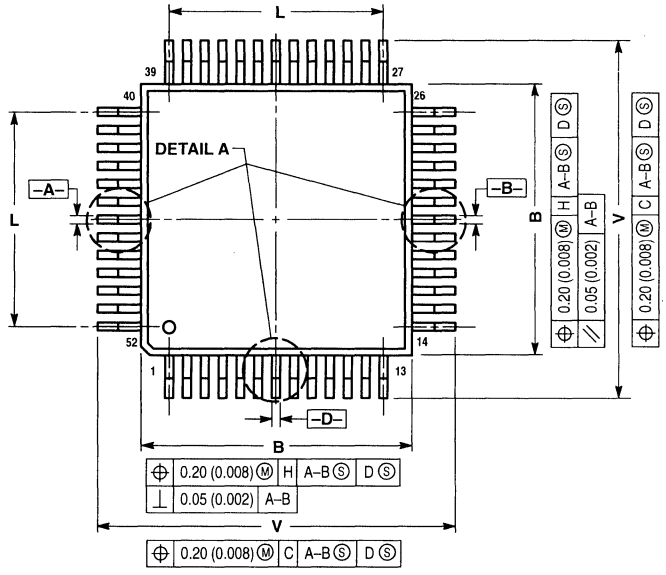


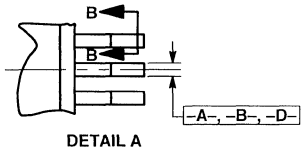




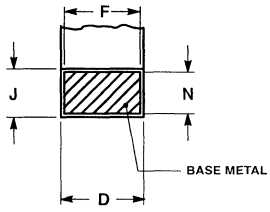
8

FB SUFFIX
PQFP (PLASTIC QUAD FLAT PACKAGE)
CASE 848B–04

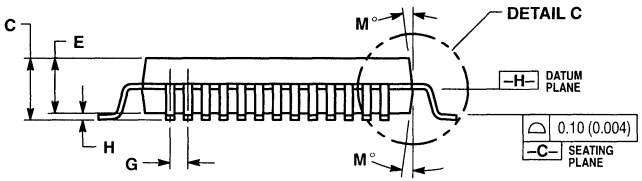


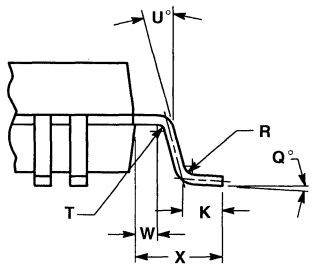


DETAIL A



SECTION B–B





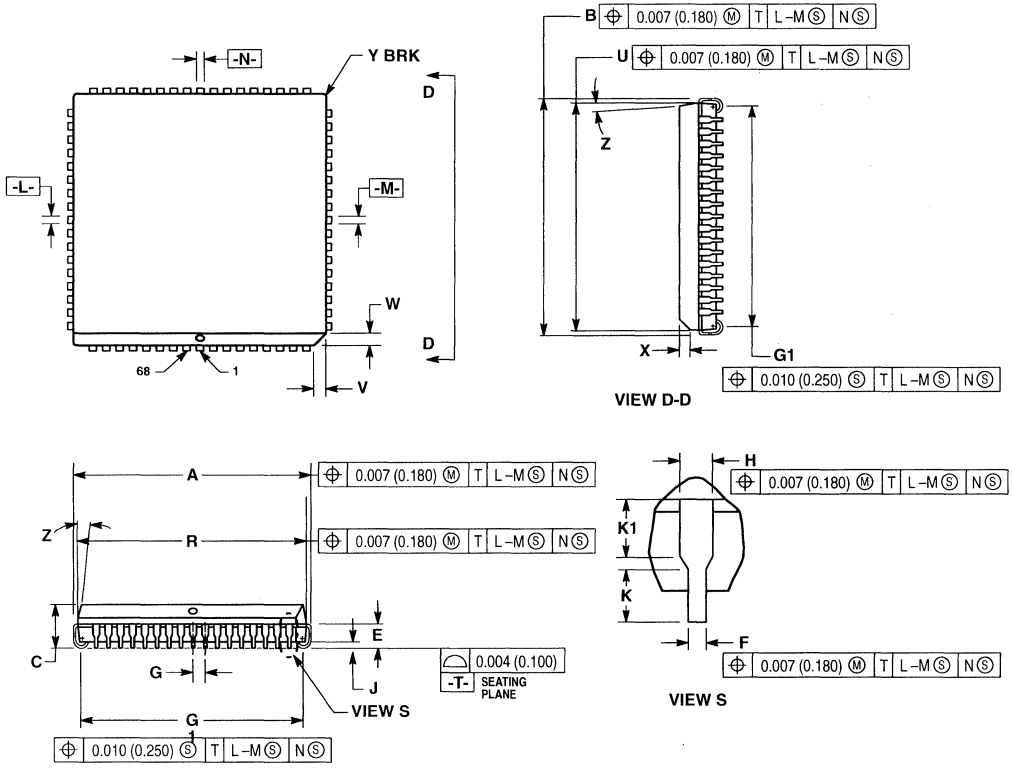
DETAIL C

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE –H– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS –A–, –B– AND –D– TO BE DETERMINED AT DATUM PLANE –H–.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE –C–.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –H–.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.90	10.10	0.390	0.398
B	9.90	10.10	0.390	0.398
C	2.10	2.45	0.083	0.096
D	0.22	0.38	0.009	0.015
E	2.00	2.10	0.079	0.083
F	0.22	0.33	0.009	0.013
G	0.65 BSC		0.026 BSC	
H	—	0.25	—	0.010
J	0.13	0.23	0.005	0.009
K	0.65	0.95	0.026	0.037
L	7.80 REF		0.307 REF	
M	5°	10°	5°	10°
N	0.13	0.17	0.005	0.007
Q	0°	7°	0°	7°
R	0.13	0.30	0.005	0.012
S	12.95	13.45	0.510	0.530
T	0.13	—	0.005	—
U	0°	—	0°	—
V	12.95	13.45	0.510	0.530
W	0.35	0.45	0.014	0.018
X	1.6 REF		0.063 REF	

8

FN SUFFIX
PLCC (PLASTIC LEADED CHIP CARRIER) PACKAGE
CASE 779–01

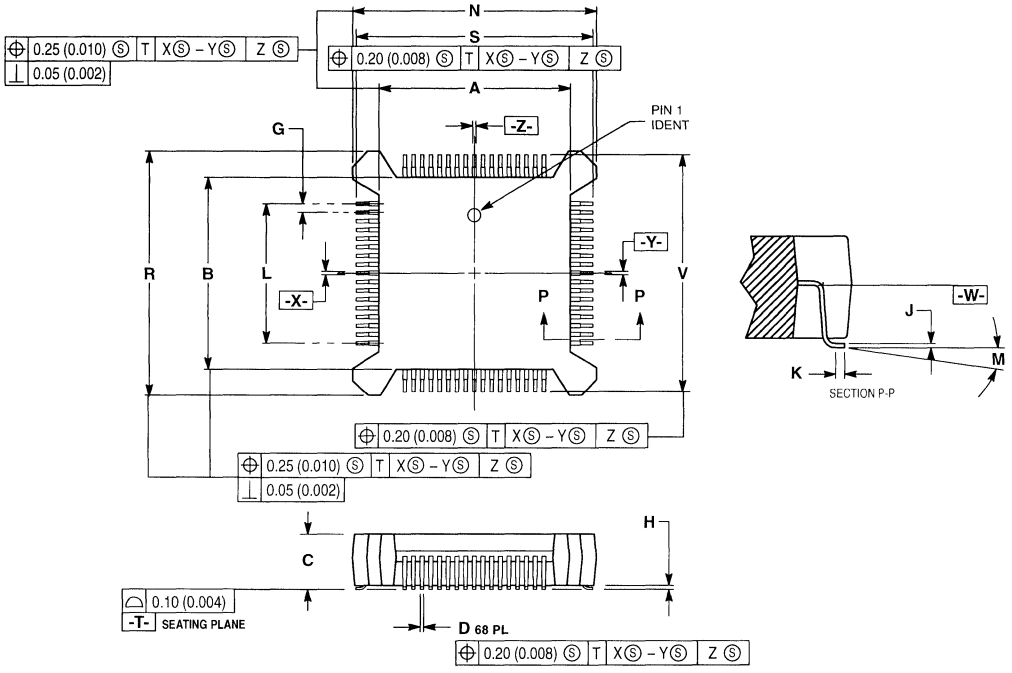


NOTES:
1. DATUMS -L-, -M-, AND -N- DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
2. DIM G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
3. DIM R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.
6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
7. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.985	0.995	25.02	25.27
B	0.985	0.995	25.02	25.27
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	—	0.51	—
K	0.025	—	0.64	—
R	0.950	0.956	24.13	24.28
U	0.950	0.956	24.13	24.28
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	—	0.020	—	0.50
Z	2°	10°	2°	10°
G1	0.910	0.930	23.12	23.62
K1	0.040	—	1.02	—

8

FU SUFFIX
PQFP (PLASTIC QUAD FLAT PACKAGE)
CASE 847–01

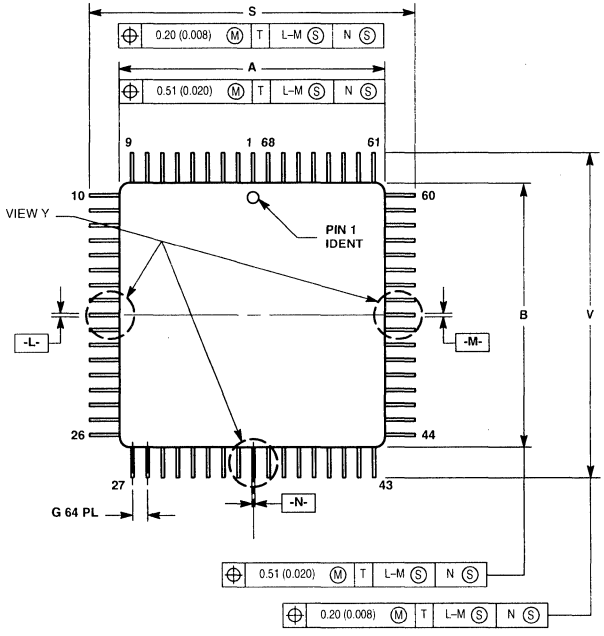


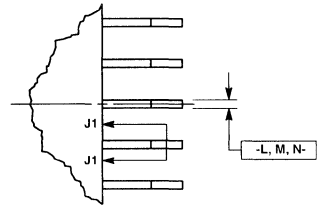
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS A, B, N, AND R DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION FOR DIMENSIONS A AND B IS 0.25 (0.010), FOR DIMENSIONS N AND R IS 0.18 (0.007).
4. DATUM PLANE -W- IS LOCATED AT THE UNDERSIDE OF LEADS WHERE LEADS EXIT PACKAGE BODY.
5. DATUMS X-Y AND -Z- TO BE DETERMINED WHERE CENTER LEADS EXIT PACKAGE BODY AT DATUM -W-.
6. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE, DATUM -T-.
7. DIMENSIONS A, B, N, AND R TO BE DETERMINED AT DATUM PLANE -W-.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.547	0.553	13.90	14.04
B	0.547	0.553	13.90	14.04
C	0.084	0.120	2.14	3.04
D	0.008	0.012	0.21	0.30
G	0.025 BSC		0.64 BSC	
H	0.004	0.019	0.11	0.40
J	0.006	0.008	0.16	0.20
K	0.020	0.030	0.51	0.76
L	0.400 REF		10.16 REF	
M	0°	8°	0°	8°
N	0.697	0.703	17.71	17.85
R	0.697	0.703	17.71	17.85
S	0.675	0.685	17.15	17.39
V	0.675	0.685	17.15	17.39

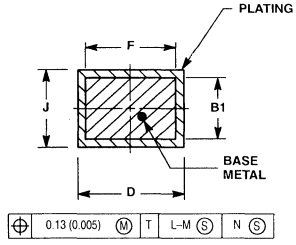
8

FE SUFFIX
CQFP (CERAMIC QUAD FLAT PACKAGE)
CASE 847B–01

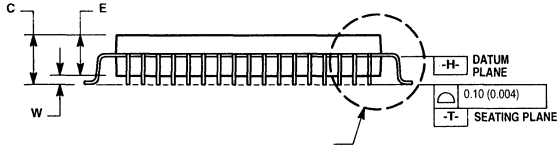


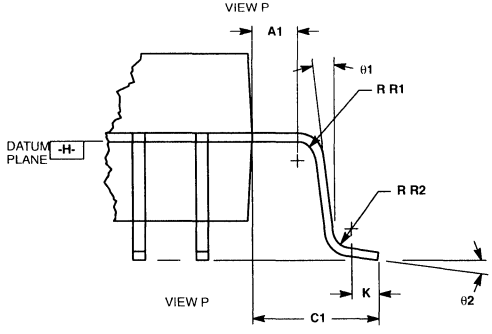


VIEW Y
3 PL



SECTION J1-J1
68 PL





NOTES.
1. ALL DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE -H- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE CERAMIC BODY.
4. DATUMS L-M AND -N- TO BE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE -T-.
6. DIMENSIONS A AND B DEFINE MAXIMUM CERAMIC BODY DIMENSIONS INCLUDING GLASS PROTRUSION AND MISMATCH OF CERAMIC BODY TOP AND BOTTOM

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	21.85	22.86	0.860	0.900
B	21.85	22.86	0.860	0.900
C	3.94	4.31	0.155	0.170
D	0.204	0.292	0.0080	0.011
E	2.95	3.71	0.116	5
F	0.20	0.28	0.008	0.146
G	1.27 BSC		0.050 BSC	
J	0.13	0.20	0.005	0.008
K	0.51	0.76	0.020	0.030
S	27.31	27.55	1.075	1.085
V	27.31	27.55	1.075	1.085
W	0.64	0.88	0.025	0.035
A1	0.64	0.88	0.025	0.035
B1	0.10	0.15	0.004	0.006
C1	2.54 REF		0.100 REF	
R1	0.20 REF		0.008 REF	
R2	0.20 REF		0.008 REF	
θ1	0°	8°	0°	8°
θ2	0°	8°	0°	8°

8

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