Single Chip Data Acquisition System Simplifies Analog-to-Digital Conversion

National Semiconductor
Application Note 193
July 1977

Until recently, building an analog data acquisition system required a hardy cross-breed of both analog design and digital design. Now National Semiconductor has simplified the design problem of a data acquisition system with the introduction of the ADC0816 (MM74C948). This CMOS device incorporates many of the standard features of a data acquisition system onto a single chip. Included on-chip is an 8-bit analog-to-digital converter with bus oriented outputs, a 16-channel expandable multiplexer, provisions for external signal conditioning, and logic control for systems interface. This chip marks the advent of a new generation in A/D converters, bringing versatility, performance, and economy using a technology ideally suited to data acquisition systems.

Figure 1 shows a block diagram of the functions provided within a single package. The chip duplicates the classical structure of a data acquisition system while relieving the user from multichip interface and compatibility problems. A wide range of functional options allows extremely versatile operation of the device in a wide range of applications.

The ADC0816 uses National's low voltage, metal gate technology. The device operates from a single +5V supply and features a 16-channel multiplexer with address input latches, latched TRI-STATE® outputs and a true eight-bit-accurate analog-to-digital converter. It consumes only 20 mW of power. Total conversion time of an analog signal is 100 μs. By using a patented A/D conversion technique the converter is guaranteed to have no missing codes and to be monotonic. The internal chopper stabilized comparator is the key element in minimizing both long term drift and temperature coefficients of other error terms.

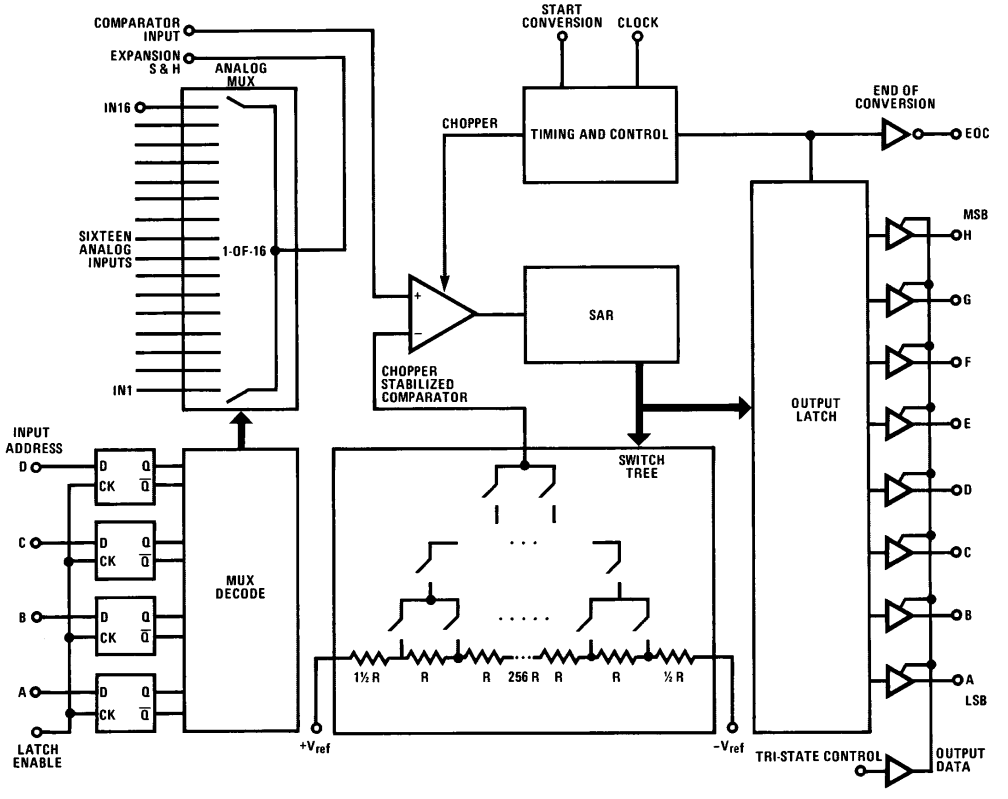

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FIGURE 1. ADC0816/MM74C948 Block Diagram

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Figure 2 shows a typical application employing the ADC0816 for use in a microprocessor-based environmental control system. In this system the microprocessor can select a channel, monitor a particular sensor reading, convert that signal to a digital word, and make a system decision based upon that input. Many other areas of process control, machine control, or multi-input analog system can utilize this basic configuration.

THE CONVERTER

The heart of this single-chip data acquisition system is its 8-bit analog-to-digital converter. The converter is designed to give fast, accurate, and repeatable conversions over a wide range of temperatures. The converter is partitioned into three major sections: the 256R ladder network, the successive approximation register, and the comparator.

The 256R ladder network approach was chosen over the conventional R/2R ladder because of its inherent monotonicity. Monotonicity is particularly important in closed-loop feedback control systems. A non-monotonic relationship can cause oscillations that could be catastrophic. Additionally, the 256R network does not cause load variations on the reference voltage.

Figure 3 shows a comparison of the output characteristic for the two approaches with a variation in the ladder resistance. In the 256R approach with unequal or shorted resistors the slope of the output transfer function cannot be different from the slope of the analog input. For the R/2R ladder network, mismatches in the resistor values can cause the slope of the output digital code to be different from the analog input signal.

The bottom resistor and the top resistor of the ladder network in *Figure 4* are not the same value as the remainder of the network. The difference in these resistors causes the output characteristic to be symmetrical with the zero and full-scale points of the transfer curve. The first output transition occurs when the analog signal has reached +1/2 LSB and succeeding output transitions occur every 1 LSB later up to full-scale.

The successive approximation register (SAR) performs eight iterations to approximate the input voltage. For any SAR-type converter, n iterations are required for an n-bit converter. *Figure 4* shows a typical example of a 3-bit converter with an input voltage of 1/4 full-scale. Since the initial approximation at 7/16 of full-scale is too high, a zero is posted for the most significant bit (MSB). The second approximation is too low, therefore a one is posted for the second bit. The final approximation is determined to be too high, so a zero is posted for the least significant bit (LSB). In the ADC0816/MM74C948 the approximation technique is extended to eight bits using the 256R network.

The most important section of the A/D converter is the comparator. It is this section which is responsible for the ultimate accuracy of the entire converter. It is also the comparator drift which has the greatest influence on the respectability of the device. A chopper stabilized comparator provides the most effective method of satisfying all the converter requirements.

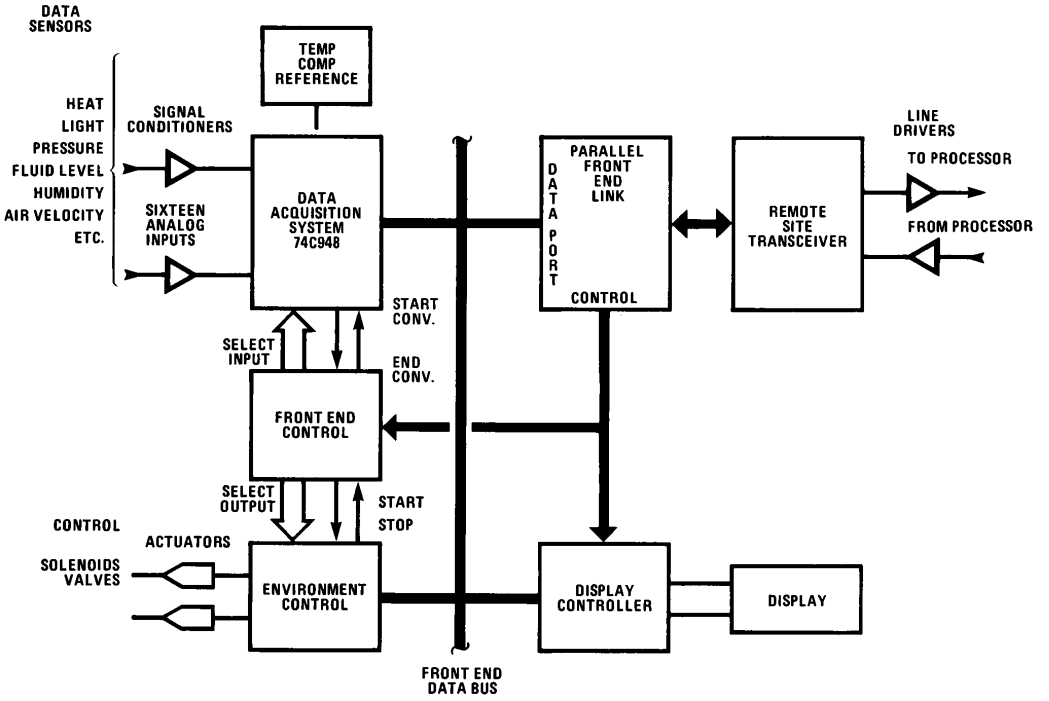

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FIGURE 2. Remote Environmental Control System

The chopper stabilized comparator converts the DC input signal into an AC signal. This signal is then fed through a high gain AC amplifier and has the DC level restored. This technique limits the drift component of the amplifier since the drift is a DC component which is not passed by the AC amplifier. This makes the entire A/D converter extremely insensitive to temperature, long-term drift, and input offset errors.

The design of this A/D converter has been optimized by incorporating the most desirable aspects of several conversion techniques. The ADC0816 offers high speed, high accuracy, low temperature dependence, excellent long-term accuracy and repeatability, and consumes minimal power. These features make this device ideally suited to applications such as process control, industrial control, and machine control.

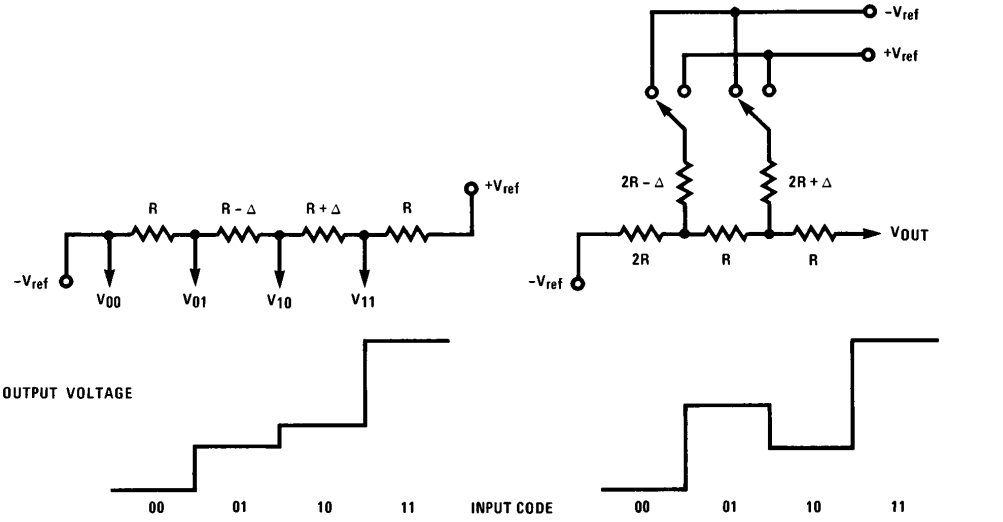

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FIGURE 3. 2^nR and R2R Ladder Transfer Curves. In a 2^nR ladder the most unequal resistors can do is cause a nonuniform voltage step. Since a single voltage is across the ladder it must be monotonic. In a R2R ladder unequal resistors may cause a sign change in the transfer curve, causing it to be nonmonotonic.

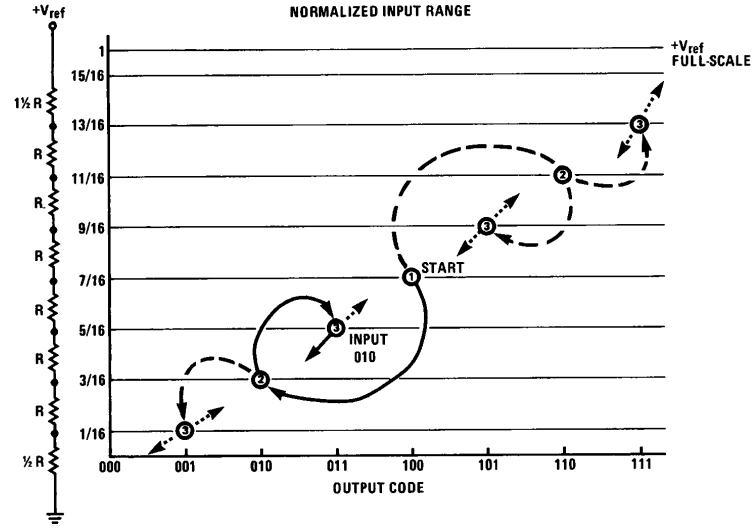

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FIGURE 4. Offset-Adjusted 8R Ladder gives ±½ LSB quantizing error of 3 bits with three comparisons. The output code is derived by posting a one when upward arrows are followed and a zero when downward arrows are followed to the input voltage.

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