Building an ISDN Terminal/ Terminal Adapter

National Semiconductor
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Chris Stacey
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INTRODUCTION

As ISDN starts to gather momentum, an ever-increasing variety of equipment will need to be designed, both by traditional Telecom switching and transmission vendors and by the data communications industry. ISDN chip sets which have not been defined with this perspective in mind are likely to be cumbersome and not cost-effective to use. A chip set for ISDN Basic Access which provides a high level of integration while retaining architectural flexibility is described here, beginning at the 'Layer 1' boundary, the 'S/T' interface.

The 'S/T' Interface

CCITT specification I.430 defines the physical layer of this interface for ISDN Basic Access. The 'S' interface is a full-duplex interface which passes the 2 'B' channels and the 'D' channel between the Network Termination (NT-1 or NT-2) and the customer's terminals, together with some additional bits used for synchronization, contention control in the 'D' channel, and other housekeeping functions. A transceiver is required for transmission at the 192 kb/s bit rate, over separate transmit and receive twisted pairs (2 pairs already exist in both office and residential telephone wiring within the premises in many countries). Alternate Mark Inversion coding, with the binary data inverted, is used.

2 additional twisted pairs are specified as an option, 1 for power and 1 for spare, making this an 8 wire interface if fully equipped. A plug and jack have been standardized so that the 'S' interface can be a ''universal portability point'' for ISDN terminals from any manufacturer in the world, see *Figure 1.*

An interesting feature of the 'S' interface is that it includes one of the elements of Local Area Networking: multiple access with contention resolution to enable up to 8 terminals to use the interface, even though there are only 2 'B' channels and 1 'D' channel. Collisions are allowed and resolved only in the 'D' channel, however, and a TE cannot use a B channel until it has first requested and been allocated one, using Layer 3 call control procedures via the D channel.

AN ADVANCED ISDN CHIP SET

In developing the architecture of this ISDN chip set, a major objective has been to create a flexible set of building blocks which provide elegant and cost-effective solutions for a wide range of applications. With just these few highly integrated devices a broad spectrum of ISDN equipment can be designed, ranging from Centrol Office and PBX line cards to X.25 and ISDN Terminals and telephones, PC and Terminals Adapters, packet-mode statistical multiplexers, NT-1's, and other ISDN equipment.

A key factor here is that device functions in the chip set are specifically aligned with the first 3 layers of the OSI 7 layer Protocol Reference Model. Thus this chip set has a distinct partitioning of functions into several transceivers which provide the bit-level transport for Layer 1, the Physical Layer, while the functions of Layer 2, the Data Link Layer, and Layer 3, the Network Layer, are supported entirely by a single microprocessor. All devices in the chip set, together with other standard components such as PCM Codec/filter Combos, can be interconnected via a common serial interface without the need for any ''glue'' components. The re-

'S' INTERFACE: THE UNIVERSAL ''PORTABILITY'' POINT

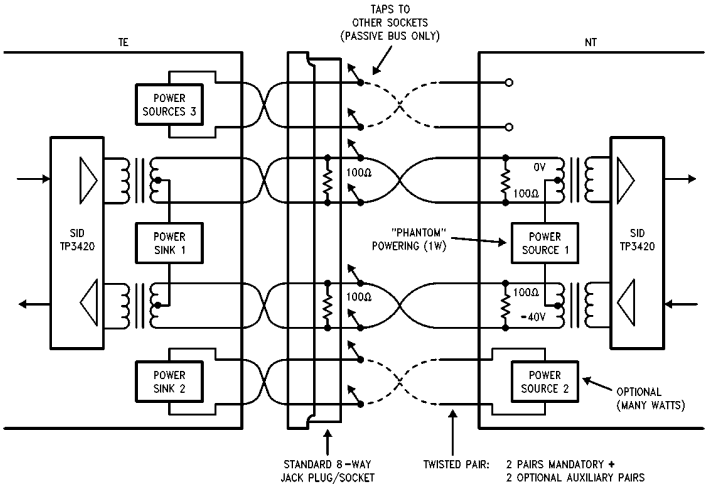

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FIGURE 1. The S Interface

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sult is a very elegant architecture offering many advantages including the following:

1. a high degree of modularity with minimal component count;
2. the same transceiver can be used at either end of a loop;
3. simplified software for packet management;
4. minimization of CPU interrupts;
5. tight coupling between Layers 2 and 3;
6. simplified exchange of primitives between Layers.

The Chip Set: Layer 1

For Layer 1, 2 CMOS transceivers have been developed to cover a wide variety of twisted-pair applications for Basic Access. Each transceiver is capable of transmitting and receiving 2 ''B'' channels plus 1 ''D'' channel, and has mode selections to enable it to work at either end of the loop. As shown in *Figure 2*, these devices are:

1. The TP3420 'S' Interface Device (SID), a 4-wire transceiver which includes all the Layer 1 functions specified in CCITT Recommendation I.430. This specifications covers the interface between the Terminal Equipment (TE) and the Network Termination (NT) on the customer's premises. In addition the TP3420 includes adaptive equalization and filtering, as well as a high resolution digital phase-locked loop in the receive side to provide transmission performance far superior to the minimum requirements of I.430. All Activation and 'D' channel access algorithms are handled automatically without the need to invoke any action from a microprocessor.
2. The second transceiver is the TP3401 Digital Adapter for Subscriber Loops (DASL), which is a low-cost burst-mode transceiver for 2-wire PBX and private network loops up to 6 kft in range. Scrambled Alternate Mark Inversion coding is used, together with adaptive equalization and timing-recovery, to ensure low bit error rates on a wide variety of cable types. All activation and loop timing control circuitry is also included. While this transmission scheme has not been standardized, it offers a practical solution for wiring installations where only a single pair is available, at lower cost than the 'S' Interface.

Note: Another transceiver has now been developed, the TP3410 2B1Q Echo-canceller for the U Interface. A TE/TA for direct connection to the U Interface maybe designed using this device, see the TP3410 datasheet.

TP3420 S INTERFACE TRANSCEIVER

This CMOS device, shown in *Figure 3,* has been designed to meet the latest version of the U.S. Draft Standard for the S/T interface, including the late addition of the 800 b/s bidirectional multiframing channel for Layer 1 maintenance messages. It also includes the Activation state machines to enable the same device to be used at either the NT or TE end of the loop, simply by mode selection during device initialization. For applications in which the TE is powered remotely from the NT or line card , requiring a low power deactivated state, the device can be totally powered down, with the exception of a line signal detect circuit, so that power-up and Activation can be initiated by either end of the loop.

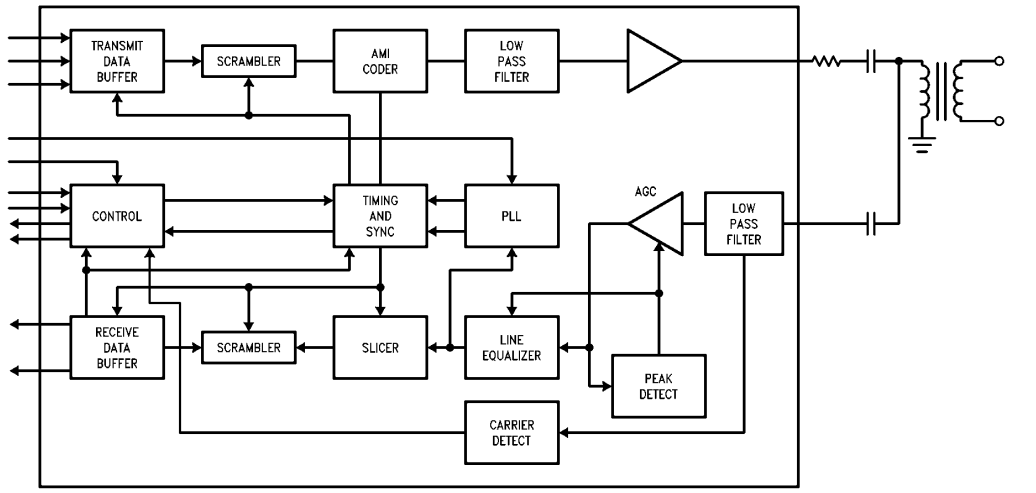

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FIGURE 2. TP3401 Transceiver

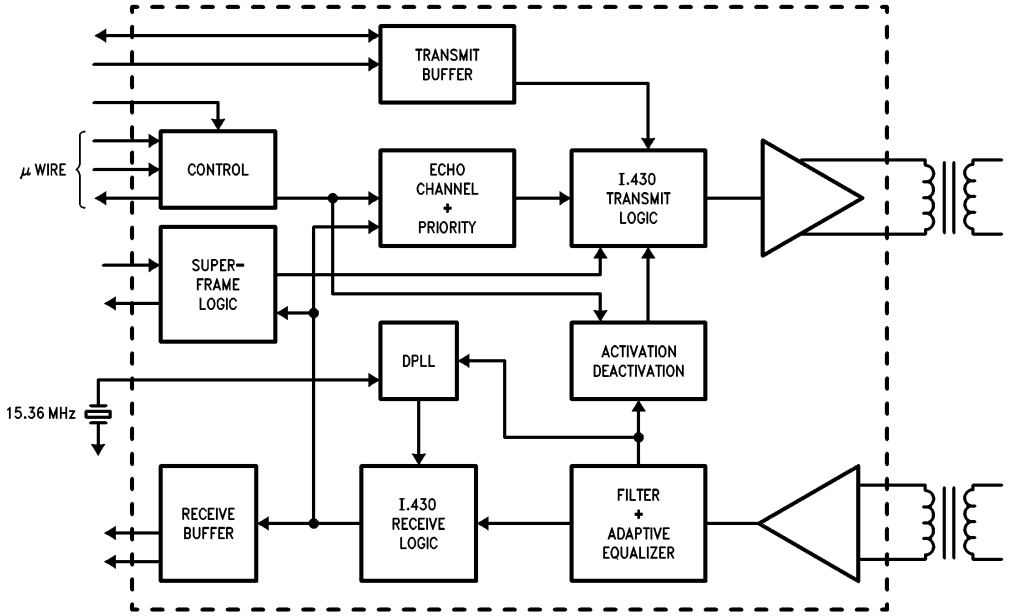


FIGURE 3. TP3420 SID

Various twisted pair wiring schemes are outlined in I.430, although in practice it is highly desirable that the transceiver should be able to work well on any existing premises wiring without special 'grooming'. Unfortunately, the transmission performance tests called up in I.430 are not as stressful on the transceiver design as are those in the recently completed 'U' Interface specification. The problem is exacerbated by the fast rise and fall times specified for the rectangular transmitted pulses, the spectrum of which includes high energy levels at frequencies in excess of 500 kHz. Bearing in mind that the cable is usually low-cost unshielded twisted pair, there is a distinct possibility that, in the presence of noise, crosstalk and jitter on the S interface, the customer will find that the better than 1 in 10E−7 BER provided on the U interface is not preserved through to the TE.

To prevent this it is important that the receiver section of the S transceiver should be designed with some additional noise margin. Certainly the TP3420, by virtue of its receiver filtering and equalization, can function with very low BER over many wiring schemes which exceed those specified, even when the received 'eye' is virtually closed by noise and jitter. Furthermore, since jitter at the digital interface in an NT can be considerably worse than that specified, for example when the U interface has been derived from a carrier system which passes its own jitter on, resynchronizers are used in the data buffers on the TP3420 to accommodate a high degree of jitter and low-frequency wander without 'slip'.

NT-2 Synchronization with the TP3420

Another feature of the device is particularly useful when designing an NT-2. The NT-2, typically a PBX, has a number of S Interfaces on the customers' side and, if it uses Basic Access to the network, each trunk is a T Interface to an NT-1 (in the classical reference model). Linking the two is the time-slot interchanging switch matrix. *Figure 4* shows the arrangement.

Functionally the S and T interfaces are identical, i.e. both conform to I.430. Thus, the TP3420 can operate on the S Interface side of the switch, with NT Mode selected (either fixed or adaptive receive sampling as appropriate for the wiring), while on the T Interface side the TP3420 operates like a terminal, in TE Mode. However, the complete NT-2 must have all its clocking and data interfaces synchronized to the network. This requires a system clock at, typically, 2.048 MHz, to be phase-locked to one of the T interfaces.

Normally, therefore, the construction of a discrete PLL to generate this frequency-locked clock is necessary; however the TP3420 includes this PLL, with a CLK output, when it is programmed to be in the TE Mode but the Slave of the digital system interface. Thus, any one of the TP3420's can be chosen as the source of this clock, and all will take their BCLK and FS timing from the same one, i.e. they are slaved to the network clock and synchronized to each other. In this way, the complete NT-2 is synchronized to any one of the activated T interfaces, and the clocking is synchronized all the way from the terminal to the network.

THE CHIP SET: LAYER 2 AND LAYER 3

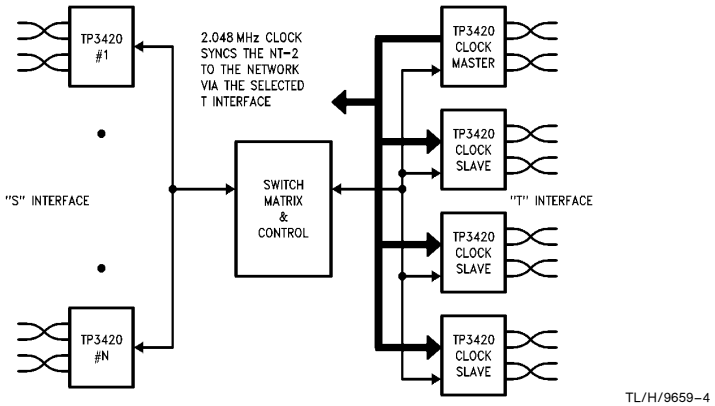
Complementing the Layer 1 transceivers, a highly integrated communications controller has been developed for implementing both Layer 2 (Data Link Layer) and Layer 3 (Network Layer) of various protocols, including X.25 LAPB and LAPD (Q.921 and Q.931), together with the capability of several Terminal Adapation schemes. A single device can run all the processing for these functions: the HPC16400. One of National's growing family of 16-bit single chip CMOS microcontrollers, the HPC16400 is based on a high-speed (20 MHz) 16-bit CPU 'core', which achieves instruction cycle times as low as 200 ns. To this core has been added 2 full HDLC formatters supported by DMA to external memory, and a UART, see *Figure 5.*

The set of features included on the HPC16400 makes it an ideal processor for running all the Layer 2 and 3 functions of an ISDN Terminal Adapter, TE or telephone, or the communications port of an X.25 or multi-protocol terminal. Because of the large ROM and RAM requirements for Layer 3 and the Control Field elements of procedure of Layer 2 in LAPB and LAPD protocols, the HPC16400 is configured as a ROMless processor. 256 bytes of RAM are provided on the core for storage of user variables; packet storage RAM and all user ROM is off-chip, this being by far the most cost-effective and flexible combination. A multiplexed bus to external memory provides direct addressing for up to 64 kbytes of memory, with additional control outputs available for expanded addressing for up to 544 kbytes of memory. Interrupts are managed by a vectored interrupt handler, which includes arbitration logic to process up to 8 pending interrupts, from both internal and external sources.

The HDLC controllers on the HPC16400 allow continuous HDLC data rates up to 4.6 Mb/s to be used, making it ideal for Primary Access and proprietary higher speed networks as well as Basic Access channels. Minor differences in the framing between these HDLC-based protocols, such as the need for different interframe-fill characters for Basic and Primary rate, and options on the CRC algorithm, can be selected during initialization. In addition to handling all Layer 2 framing, the HDLC circuitry includes automatic multiple address recognition on incoming Layer 2 frames, to support, for example, multiple TEI's in LAPD.

As an aid in implementing multiple protocols within the one design, a 'Bypass' mode is included for each HDLC channel, whereby the HDLC framing circuits are bypassed. Thus a straightforward USRT interface is then established, enabling non-HDLC protocols to be run in software. This mode may be selected and deselected at will, so that data transfer sessions between different types of terminal can be handled on a per-call basis. To enable the speed capabilities of the HDLC channels to be fully exploited, they interface to external data buffer RAM via a Direct Memory Access controller on the device. A bus request is issued by the DMA controller to the CPU when one or more of the individual HDLC channels request service. Upon receiving a bus acknowledge from the CPU, the DMA completes all requests pending,

NT-2 Synchronization



TP3420 Can Be Clock Master or Slave

FIGURE 4. NT-2

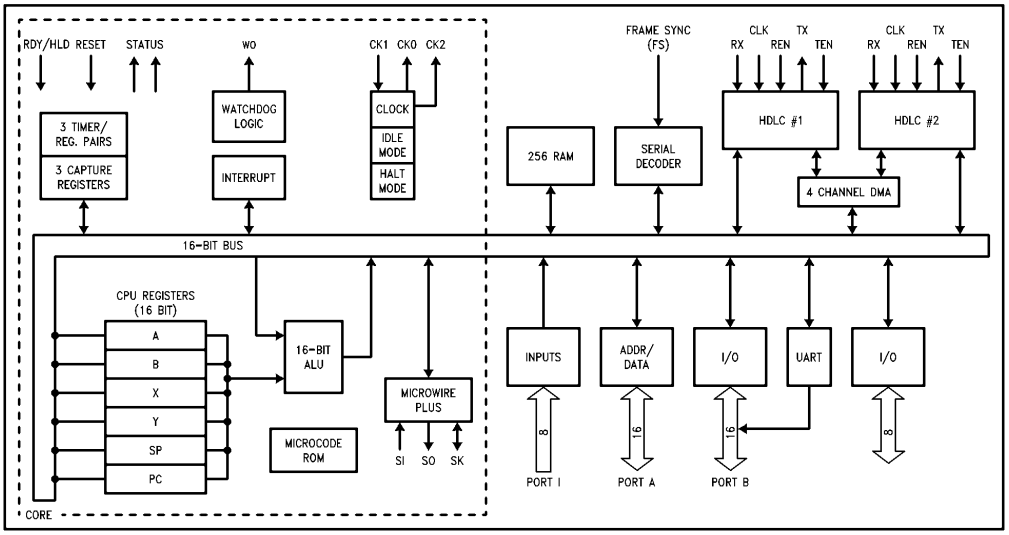


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FIGURE 5. HPC 16400 Block Diagram

and any that may occur during this operation, before relinquishing the bus back to the CPU. All this takes place merely by stealing bus cycles away from the CPU, there is no need for ''pushing'' and ''popping'' the stack as is the case where the Layer 1 transceiver includes FIFOs for data buffering, which demand service by means of interrupts.

Furthermore, several register sets are included to simplify packet RAM management, again with minimal CPU intervention. These registers facilitate ''chaining'' of successive packets, in which the memory pointers for the following packet can be set up during transfer of the current packet so that there is no latency period between packets during high-speed transmission. Additionally, if required, the header and Information fields of Layer 2 frames can be segmented into different areas of memory to help structure the packet RAM economically. This integrated design achieves a high throughput of packet data without the need for costly FIFO's and external interrupts, thereby minimizing the impact of packet handling on CPU time.

TYPICAL TE/TA APPLICATIONS

Figure 6 shows a typical application of the chip set in a Basic Access TE which offers one voice channel and an RS232 interface to support an external terminal. Other combinations, such as 2 voice channels or 2 data channels are easily implemented by adding a second Combo or an external HDLC controller, and a few gates are all that is necessary to multiplex between them. The TP3420 'S' Interface Device ensures that the system is compatible with any 'S' or 'T' standard jack socket and provides the multiplexing signals for the other devices operating in the 'B' and 'D' channels; all timing for the TE is derived by the TP3420 from the received line signal.

In the application shown, LAPD signalling in the 'D' channel is provided via HDLC #1 on the HPC16400. The UART would serve as an RS232 interface and, by using a 15.36 MHz crystal, which can be shared between the HPC and the SID, all the standard asynchronous baud rates up to 19,200 (and beyond) can be generated. Terminal adapation of the data and the terminal handshaking signals is performed by the HPC16400 via the UART and HDLC controller #2, which can be assigned to either of the 'B' channels.

For voice calls, the TP3054/7 Codec/filter Combos are quite suitable, since the analog ports are readily interfaced to an electret microphone and a moving-coil earpiece, with a sidetone leak path added. B and D channel data passes between the devices multiplexed together, clocked by the BCLK output from the SID, and synchronized by the 8 kHz frame sync, FS, from SID. A serial interface decoder allows either or both HDLC controllers to be directly interfaced and synchronized to either of the Layer 1 transceivers or to a variety of backplanes, line-card controllers and other devices using time-division multiplexed serial interfaces. Both the SID and the HPC16400 include several selectable formats for this multiplexing, to simplify the interface to other vendors' Codecs. Format 1 on the SID is the correct one for the TP3054 Combo, while on the HPC Serial Decoder, Format 4 is the correct choice for this combination of devices. Although the simplified interface timing on the TP3054/7 means that it will always need to use the B1 channel to and from the SID, the SID has a control function which allows it to to exchange data between the B1 and B2 channels as it passes through it. Thus, if the network assigns channel B2 to a voice call, SID does the exchange from the Combo in

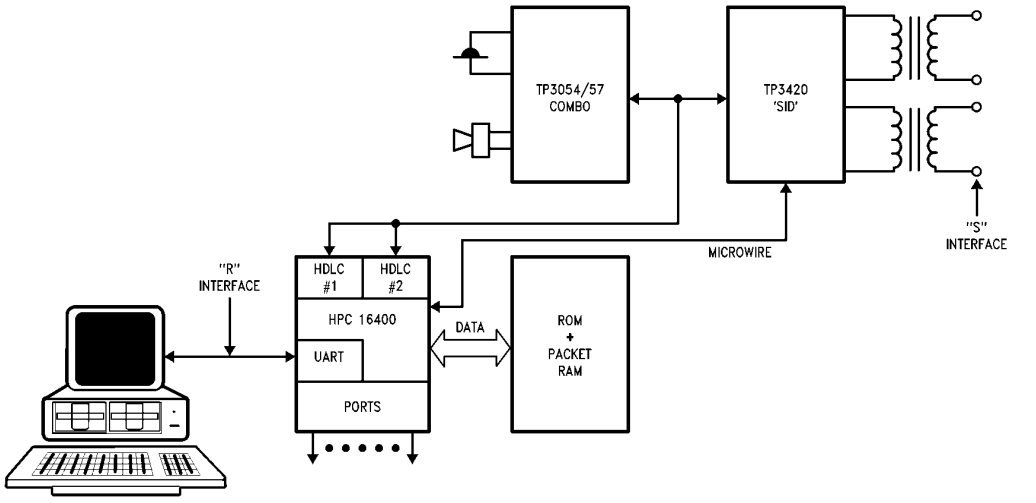

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FIGURE 6. Typical Terminal Application

the B1 channel on the Digital System Interface to the B2 channel on the S Interface. Because of the way the Serial Decoder on the HPC is designed, its HDLC channel #1 will normally be selected for the D channel, while either HDLC controller can be used for data in either B channel.

In applications where the TE must go into a low-power mode when there are no calls in progress, the HPC is put into the HALT mode, with all other devices powered-down. The correct way to restart the HPC to initiate a call is to pull the Non-maskable Interrupt high. Since this may be invoked by an off-hook signal in the TE, or by the SID's Line Signal Detector detecting a wake-up signal (INFO 2 on the S interface) and pulling low, these 2 signals are simply NOR'd together to pull NMI high. The LSD output has been designed to prevent multiple pulses from repeatedly causing interrupts; mechanical hookswitches, however, may bounce, requiring a simple R-C debouncing filter to be inserted.

In many applications a number of other peripheral functions must also be provided, such as sensing switches or scanning a small keyboard, interfacing to a display controller etc. A number of extra I/O pins and a MICROWIRE/PLUS™ serial data expansion interface are available on the HPC 16400 to service these functions. In addition, 4 user configurable 16 bit timer-counters simplify the many time-outs required to manage such a system, including the default timers specified in the various protocol specifications. A ''Watchdog'' timer can also be enabled, to provide a means for recovery from erroneous software states.

D-Channel Flow Control

D-Channel Flow Control refers to the way the HPC transfers a Layer 2 frame (or packet) to the SID transmit buffer, and from there onto the S Interface in a Terminal. When the Layer 2 entity wants to transmit a packet, it does not know if another TE is already occupying the D Channel, since all the D Channel monitoring and contention resolution is done at Layer 1 by the SID. To transmit its packet, therefore, the HPC primes its HDLC #1 transmit buffer, ready to send byte 1, then sends a DREQ (D-channel Request) over MICROWIRE™ to the SID. DREQ messages must also indicate if the pending packet is high priority, for signalling, or low priority, for all other types of data. The TP3420 SID then uses a special clock control output to fetch data from the HPC, multiplexed on the digital system interface. Concurrently, it tests to see if the D Channel towards the NT is in use by another TE, by checking the number of consecutive 1s counted in the D-echo channel from the NT. When the access algorithm allows, SID starts transmitting D-channel bits from its buffer, beginning with the opening flag, and clocks further D channel bits from the HPC's HDLC #1 to the SID, always 2 bits per 8 kHz frame. As the HPC empties its transmit buffer, a DMA cycle is prompted to replenish it. Thus, D-channel data now flows from the HPC through SID and onto the S interface without interrupts until either:

i) the TP3420 SID detects that it has lost a collision with another TE, so it stops fetching data from the HPC, transmits 1s in the following D-bit positions on the S interface, and INTerrupts the HPC with a CONtention message;

or:

ii) the SID detects the closing flag passing through onto the S interface, forces 1's into the D-channel after the closing flag, stops fetching data, and sends an EOM (End of Message) INTerrupt to the HPC.

Note that the HPC cannot follow immediately with another packet because the successful TE must now decrement its priority and check that no other TE starts using the D-channel. Thus TEs waiting to send signalling packets all succeed in order first, and data packets are only sent when no TE has a signalling packet pending.

TERMINAL ADAPTION

One of the hurdles facing the widespread deployment of ISDN is the confusion over terminal adaption techniques. While the X.31 standard has been adopted for connection of X.25 terminals to Packet switches via the ISDN, the situation for the majority of terminals which will require circuit-switched access is far less certain. Currently, there is only one standard, V.110, which is CCITT approved for these applications, although certain recent additions for the support of asynchronous terminals have yet to be ratified. There are, however, several other contenders, most notably a recent spec, colorfully known a V.tad, which is a simpler technique than V.110, and offers the major advantage that

data is rate adapted into HDLC frames using Q.921 procedures. V.tad, proposed by the U.S., is currently under the scrutiny of CCITT. Then there are several proprietary schemes in existence, notably AT&T's DMI mode 2 and Northern Telecom's T-Link, which are already deployed in the network, yet will not be standardized at the national or international level. Thus there is considerable interest in terminal adapters which can support multiple protocols, a task for which the HPC16400 is ideally suited.

To build a terminal adapter around the HPC, an area of external RAM is first set up as the data buffers for the 2 directions. Different software modules are then called up to assemble and disassemble the frames to and from the network, using the appropriate method of rate adapting the data. HDLC channel #2 provides access to either of the B channels in the SID Layer 1 transceiver. For a data call using V.110 or other non-HDLC based protocols, the bypass mode is selected for the HDLC framing circuits, while for a V.tad call the HDLC circuits are switched in, this being selectable on a call-by-call basis if desired. On the terminal side, for a V.24/RS232C async terminal interface, the onboard UART provides the start/stop bit manipulation and terminal clocking functions between the terminal and the data buffers. For a TA plug-in card for a PC, an INS8250 or 16450 UART can be added to interface to the backplane if it is required to maintain compatibility with existing DOS I/O drivers. Either way, it takes the power of an HPC16400, with its high speed processing, efficient compiling of high-level languages and expandable address space, to implement these multiple, complex, real-time tasks.

Note: V.tad is now numbered as V.120 in the CCITT Blue Book.

PBX 2-Wire Terminals

Thus far, the terminal designs discussed have been based on compatibility with the S Interface Layer 1 specification. *Figure 7* shows how simple it is to convert an 'S' Interface terminal, which of course requires 2 twisted pairs, to a terminal using only a single pair by replacing the TP3420 SID by a TP3401 DASL. The clean partitioning of device functions makes this possible with practically no other changes to the design.

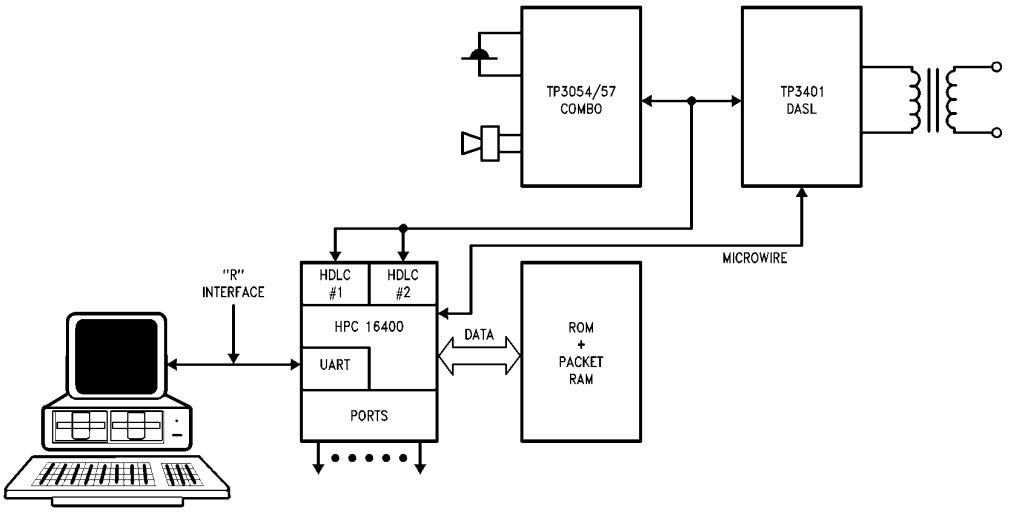

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FIGURE 7. 2-Wire Terminal Application

Basic Access Line Cards

For operation on a line card in a PABX or NT-2, such as that shown in *Figure 7,* both of the transceiver devices can be set to operate as the timing master for the loop, being synchronized to the system clock and controlling all loop frame timing. If programmable time-slot assignment is required, the TP3155 TSAC provides 8 individually programmable frame sync pulse outputs locked to a common frame marker. 'B' channels can be interfaced to standard backplane interfaces, while 'D' channels can be either multiplexed on and off the card for processing or can undergo Layer 2 processing on the card itself.

Building an NT-1

An NT-1 Network Termination is defined as a Layer 1 device only, which converts the 2-wire public network 'U' interface to the limited distance 4-wire 'S' interface on the customer's premises. It has no capability for intercepting higher layers of the 'D' channel protocol. As such, it is built simply by connecting a TP3420 SID, configured in NT mode, to a U Interface transceiver operating in Slave mode. Layer 1 maintenance protocols across both the 'U' and 'S/T' interfaces, which are as yet still in a state of flux for most administrations, may be handled by a low-cost COPs Microcontroller via its serial MICROWIRE interface. *Figure 8* shows the arrangement.

SUMMARY

Designing ISDN equipment is not going to be a cakewalk for this first generation. There are numerous new standard specifications to become familiar with, and many protocol and real-time processing problems to be overcome. The chip set described here provides designers with the confidence of knowing that the hardware is fully compliant with the latest standards, and that the necessary processing power is available in the HPC to satisfy a wide range of designs without the need to re-learn a different set of components for every new product.

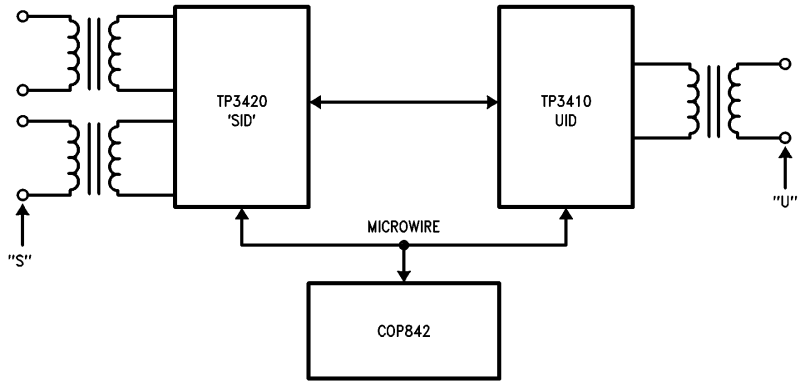

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FIGURE 8. NT-1 Application

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National Semiconductor Corporation
1111 West Bardin Road
Arlington, TX 76017
Tel: 1(800) 272-9959
Fax: 1(800) 737-7018

National Semiconductor Europe
Fax: (+49) 0-180-530 85 86
Email: cnjwge@tevm2.nsc.com
Deutsch Tel: (+49) 0-180-530 85 85
English Tel: (+49) 0-180-532 78 32
Français Tel: (+49) 0-180-532 93 58
Italiano Tel: (+49) 0-180-534 16 80

National Semiconductor Hong Kong Ltd.
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: (852) 2737-1600
Fax: (852) 2736-9960

National Semiconductor Japan Ltd.
Tel: 81-043-299-2309
Fax: 81-043-299-2408