400030

National Semiconductor

Interface Databook

Transmission Line Drivers and Receivers
Bus Transceivers
Peripheral Power Drivers
Display Drivers
Memory Support
Microprocessor Support
Level Translators and Buffers
Frequency Synthesis
Hi-Rel Interface

A Corporate Dedication to Quality and Reliability

National Semiconductor is an industry leader in the manufacture of high quality, high reliability integrated circuits. We have been the leading proponent of driving down IC defects and extending product lifetimes. From raw material through product design, manufacturing and shipping, our quality and reliability is second to none.

We are proud of our success . . . it sets a standard for others to achieve. Yet, our quest for perfection is ongoing so that you, our customer, can continue to rely on National Semiconductor Corporation to produce high quality products for your design systems.

Charles E. Sporck
President, Chief Executive Officer
National Semiconductor Corporation

Wir fühlen uns zu Qualität und Zuverlässigkeit verpflichtet

National Semiconductor Corporation ist führend bei der Herstellung von integrierten Schaltungen hoher Qualität und hoher Zuverlässigkeit. National Semiconductor war schon immer Vorreiter, wenn es galt, die Zahl von IC Ausfällen zu verringern und die Lebensdauern von Produkten zu verbessern. Vom Rohmaterial über Entwurf und Herstellung bis zur Auslieferung, die Qualität und die Zuverlässigkeit der Produkte von National Semiconductor sind unübertroffen.

Wir sind stolz auf unseren Erfolg, der Standards setzt, die für andere erstrebenswert sind. Auch ihre Ansprüche steigen ständig. Sie als unser Kunde können sich auch weiterhin auf National Semiconductor verlassen.

La Qualité et La Fiabilité:

Une Vocation Commune Chez National Semiconductor Corporation

National Semiconductor Corporation est un des leaders industriels qui fabrique des circuits intégrés d'une très grande qualité et d'une fiabilité exceptionelle. National a été le premier à vouloir faire chuter le nombre de circuits intégrés défectueux et a augmenter la durée de vie des produits. Depuis les matières premières, en passant par la conception du produit sa fabrication et son expédition, partout la qualité et la fiabilité chez National sont sans équivalents.

Nous sommes fiers de notre succès et le standard ainsi défini devrait devenir l'objectif à atteindre par les autres sociétés. Et nous continuons à vouloir faire progresser notre recherche de la perfection; il en résulte que vous, qui êtes notre client, pouvez toujours faire confiance à National Semiconductor Corporation, en produisant des systèmes d'une très grande qualité standard.

Un Impegno Societario di Qualità e Affidabilità

National Semiconductor Corporation è un'industria al vertice nella costruzione di circuiti integrati di altà qualità ed affidabilità. National è stata il principale promotore per l'abbattimento della difettosità dei circuiti integrati e per l'allungamento della vita dei prodotti. Dal materiale grezzo attraverso tutte le fasi di progettazione, costruzione e spedizione, la qualità e affidabilità National non è seconda a nessuno.

Noi siamo orgogliosi del nostro successo che fissa per gli altri un traguardo da raggiungere. Il nostro desiderio di perfezione è d'altra parte illimitato e pertanto tu, nostro cliente, puoi continuare ad affidarti a National Semiconductor Corporation per la produzione dei tuoi sistemi con elevati livelli di qualità.

Charles E. Sporck
President, Chief Executive Officer
National Semiconductor Corporation

INTERFACE
DATABOOK

TRADEMARKS

Following is the most current list of National Semiconductor Corporation's trademarks and registered trademarks.

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ANS-R-TRANTM
APPSTM
Auto-Chem DeflasherTM
BI-FETTM
BI-FET IITM
BI-LINETM
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DISCERNTM
DISTILLTM
DNRTM
DPVMTM
ELSTARTM
E-Z-LINKTM
GENIXTM
GNXTM
HEX 3000TM
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Integral ISETM
IntelisplayTM
ISETM
ISE/06TM
ISE/08TM
ISE/16TM
ISE32TM
LMCMOSTM
MacrobusTM
MacrocomponentTM
Meat✓ChekTM
Microbus™ data bus (adjective)
MICRO-DACTM
μtalkerTM
MicrotalkerTM
MICROWIRETM
MICROWIRE/PLUSTM
MOLETM
MSTTM
Naked-8TM
National®
NAX 800TM
Nitride PlusTM
Nitride Plus OxideTM
NMLTM
NOBUSTM
NSC800TM
NSX-16TM
NS-XC-16TM
NURAMTM
OXISSTM
Perfect WatchTM
Pharma✓ChekTM
PLANTM
PolycraftTM
POSitalkerTM
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RTX16TM
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Starlink™
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STARPLEX IITM
SuperChipTM
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NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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Introduction

Since its creation in 1973, National Semiconductor's Interface design and production teams have produced technically advanced products unparalleled in the semiconductor industry.

Growing from a line of early drivers and receivers, which pioneered the introduction of the TRI-STATE® function, National Semiconductor's Interface product line today is the most comprehensive available—with over 200 devices in a variety of product categories.

Based on its advanced design and process capabilities, National's Interface product line includes:

- The industry's most advanced RS-232 drivers and receivers.
- The industry's most advanced RS-422 drivers, receivers, and transceivers
- The industry's most advanced RS-485 transceivers
- The industry's only offering of over 16 devices incorporating power up/down glitch-free protection
- The industry's first Trapezoidal™ bus transceiver
- The industry's first transceivers for the Future Bus standard
- The industry's first fault protected peripheral driver incorporating a major breakthrough in current sensing and shut down circuitry.

In addition to the detailed Interface product datasheets included in this databook, complete product selection guides can be found at the beginning of each section for quick reference.

The Interface Appendix supplies helpful application notes, terms and definitions, cross references, design and process information and package information.

These Interface devices support and complement Nationals advanced VLSI APPS™ product families. These Advanced Peripheral Processing Solutions or APPS products are families of VLSI peripheral circuits designed to serve a variety of applications. The APPS products are especially well suited for microcomputer and microprocessor based systems such as graphic workstations, personal computers, and many others. National Semiconductor's APPS devices are fully described in a series of databooks and handbooks.

Among the APPS books are the following titles:

MASS STORAGE

MEMORY SUPPORT

LOCAL AREA NETWORKS AND DATACOMMUNICATIONS

GRAPHICS

All the APPS products currently provided by National Semiconductor and their appropriate APPS Databook title are listed in the Table of Contents of this Databook.

For more information on National Semiconductor's INTERFACE and APPS products contact your local National authorized sales representative or distributor.

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Section 1

Transmission Line Drivers/Receivers

Section Contents

Section Contents

***Also available processed to various Military screening levels. Refer to Section 9.**

Transmission Line Drivers/Receivers

The common purpose of transmission line drivers and receivers is to transmit data quickly and reliably through a variety of environments over electrically long distances. This task is complicated by the fact that externally introduced noise and ground shifts can severely degrade the data.

The connection between two elements in a system should be considered a transmission line if the transmitted signal takes longer than twice its rise or fall time to travel from the driver to the receiver.

Single-Ended Data Transmission

In data processing systems today there are two basic means of communicating between components. One method is single-ended, which uses only one signal line for data transmission, and the other is differential, which uses two signal lines.

The Electronics Industry Association (EIA) has developed several standards to simplify the interface in data communications systems.

RS-232

The first of these, RS-232, was introduced in 1962 and has been widely used throughout the industry. RS-232 was developed for single-ended data transmission at relatively slow data rates (20 kBaud) over short distances (up to 50 ft.).

RS-423

With the need to transmit data faster and over longer distances, RS-423, a newer standard for single-ended applications, was established. RS-423 extends the maximum data rate to 100 kBaud (up to 30 ft.) and the maximum distance to 4000 feet (up to 1 kBaud). RS-423 also requires high impedance driver outputs with power off so as not to load the transmission line.

Differential Data Transmission

When transmitting at very high data rates, over long distances and through noisy environments, single-ended transmission is often inadequate. In these applications, differential data transmission offers superior performance. Differential transmission nullifies the effects of ground shifts and noise signals which appear as common mode voltages on the transmission line.

RS-422

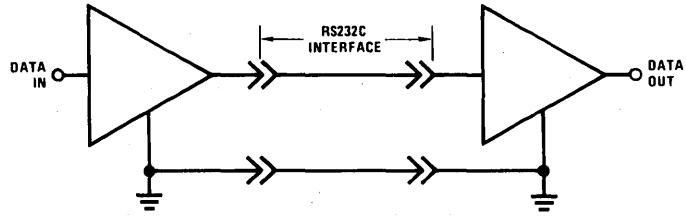
RS-422 was defined by the EIA for this purpose and allows data rates up to 10 MBaud (up to 40 ft.) and line lengths up to 4000 feet (up to 100 kBaud).

Drivers designed to meet this standard are well suited for party-line type applications where only one driver is connected to, and transmits on, a bus and up to 10 receivers can receive the data. While a party-line type of application has many uses, RS-422 devices cannot be used to construct a truly multipoint bus. A multipoint bus consists of multiple drivers and receivers connected to a single bus, and any one of them can transmit or receive data.

RS-485

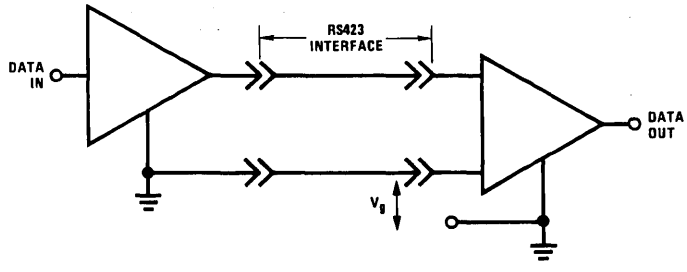
To meet the need for truly multipoint communications, the EIA established RS-485 in 1983. RS-485 meets all the requirements of RS-422, but in addition, this new standard allows up to 32 drivers and 32 receivers to be connected to a single bus—thus allowing a truly multipoint bus to be constructed.

RS-232C Application



CI11-1

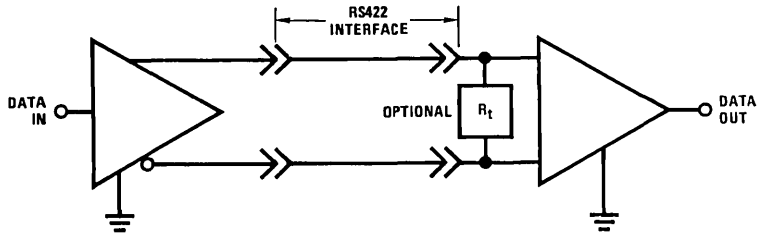
EIA RS-423 Application



CI11-2

Differential Data Transmission (Continued)

EIA RS-422 Application



CI11-3

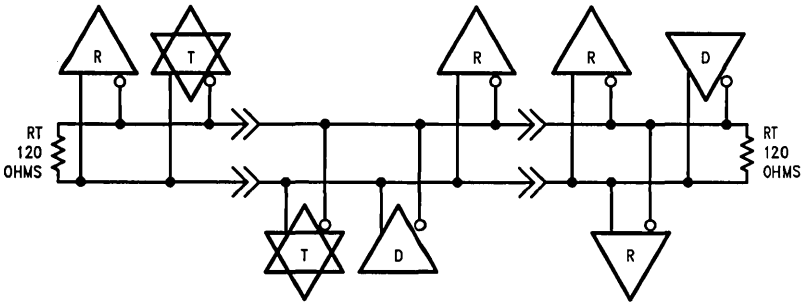
The key features of RS-485:

- Implements a truly multipoint bus consisting of up to 32 drivers and 32 receivers
- An extended common-mode range for both drivers and receivers in TRI-STATE and with power off (−7V to +12V)
- Drivers can withstand bus contention and bus faults

National Semiconductor produces a variety of drivers, receivers, and transceivers for these four very popular transmission standards and numerous other data transmission requirements.

Shown below is a table that highlights key aspects of the EIA Standards. More detailed comparisons can be found in the various application notes in Section 1.

RS-485 Application



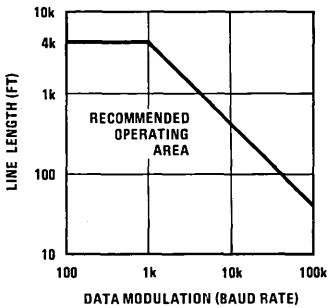
D — Driver
R — Receiver
T — Transceiver

CI11-4

Specification		RS-232C	RS-423	RS-422	RS-485
Mode of Operation		Single-Ended	Single-Ended	Differential	Differential
Number of Drivers and Receivers Allowed on One Line		1 Driver, 1 Receiver	1 Driver, 10 Receivers	1 Driver, 10 Receivers	32 Drivers, 32 Receivers
Maximum Cable Length		50 feet	4000 feet	4000 feet	4000 feet
Maximum Data Rate		20 kb/s	100 kb/s	10 Mb/s	10 Mb/s
Driver Output Maximum Voltage		±25V	±6V	−0.25V to +6V	−7V to +12V
Driver Output Signal Level	Loaded	±5V	±3.6V	±2V	±1.5V
	Unloaded	±15V	±6V	±5V	±5V
Driver Load Impedance		3 kΩ to 7 kΩ	450Ω min	100Ω	54Ω
Maximum Driver Output Current (High Impedance State)	Power On	——	——	——	±100 μA
	Power Off	V_{MAX}/300Ω	±100 μA	±100 μA	±100 μA
Slew Rate		30 V/μs max	Controls Provided	——	——
Receiver Input Voltage Range		±15V	±12V	−7V to +7V	−7V to +12V
Receiver Input Sensitivity		±3V	±200 mV	±200 mV	±200 mV
Receiver Input Resistance		3 kΩ to 7 kΩ	4 kΩ min	4 kΩ min	12 kΩ min

1

Line length is a function of data rate (baud) and slew rate. The recommended safe operating area (line length vs baud rate) is shown below for 24 AWG wire. It assumes that a differential line receiver is used which is referenced at the driver ground. Also, it assumes that the driver slew rate is between 0.1 to 0.3 times the reciprocal of the baud rate (minimum unit interval). Otherwise, line lengths greater than 50 feet are not recommended. The exception to line length is the 360 I/O coaxial interface. The coaxial provides improved grounding and eliminates crosstalk.



C112-1

UNBALANCED DRIVERS

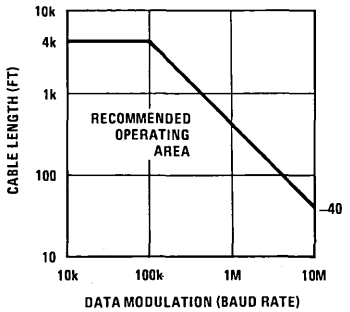
Standard	Device Number		Circuits Per Package	Power Supplies (V)	Open-Collector/ Open Emitter TRI-STATE	Party-Line Application	Slew Rate Control	Output Current (mA)	Output Voltage (V)	Propagation Delay (ns)	Comments	Page No.
	Commercial 0°C to +70°C	Military −55°C to +125°C										
RS-232	DS1488		4	±9 or ±15			IOS/C	±6	±6 or ±9	200		1-11
RS-232	DS14C88			±9 or ±15			Internal	±6	±7 or ±11			1-15
RS-232	DS75150		2	±12			IOS/C	±10	±5	60		1-117
RS-423	DS3691	DS1691A	4	+5 or ±5	TRI-STATE	Yes	CEXT	±20	±2	200		1-68
MIL-188-114	DS3692	DS1692	4	+5 or ±5	TRI-STATE	Yes	CEXT	±20	±2	200	±10V Common-Mode Range	1-74
360 I/O	DS75121	DS55121	2	5	Emitter	Yes		−100	2.4	10	50Ω Coax Driver	1-102
360 I/O	DS75123		2	5	Emitter	Yes		−100	2.4	10	50Ω Coax Driver (IBM)	1-104
	DS75450		2	5	Emitter and Collector	Yes		300	0.7	20		3-41
	DS75451	DS55451	2	5	Collector	Yes		300	0.7	18		3-41
	DS75452	DS55452	2	5	Collector	Yes		300	0.7	26		3-41
	DS75453	DS55453	2	5	Collector	Yes		300	0.7	18		3-41
	DS75454	DS55454	2	5	Collector	Yes		300	0.7	27		3-41

UNBALANCED RECEIVERS

Standard	Device Number		Circuits Per Package	Power Supplies (V)	Strobed or TRI-STATE	Response Control	Hysteresis (mV)	Input Range (V)	Threshold Sensitivity (V)	Propagation Delay (ns)	Comments	Page No.
	Commercial 0°C to +70°C	Military −55°C to +125°C										
RS-232	DS1489		4	5		CEXT	250	±25	3	30		1-21
RS-232	DS1489A		4	5		CEXT	1150	±25	3	30	Preferential in Applications to DS1489	1-21
RS-232	DS14C89A		4	5				±25	3			1-15
RS-232	DS75154		4	5 or 15		CEXT	800	±25	3	22		1-121
RS-423	DS26C32		4	5	TRI-STATE							1-35
RS-423	DS26LS32C	DS26LS32M	4	5	TRI-STATE		100	±7	±0.2	17		1-32
RS-423	DS26LS32AC		4	5	TRI-STATE		100	±7	±0.2	23	Fail-Safe	1-32
RS-423	DS3486		4	5	TRI-STATE		100	±15	±0.2	25		1-38
RS-423	DS34C86		4	5	TRI-STATE							1-42
RS-423	DS88C20	DS78C20	2	5	Strobed	CEXT	50	±25	±0.2	50		1-140
RS-423	DS88C120	DS78C120	2	5	Strobed	CEXT	50	±25	±0.2	50	Fail-Safe	1-155
RS-423	DS88LS120	DS78LS120	2	5 to 15	Strobed	CEXT	50	±25	±0.2	50	Fail-Safe	1-163
360 I/O	DS75124		3	5	Strobed		400	7	0.8 to 2	20	50Ω Coax. Receiver (IBM)	1-106
360 I/O	DS75125		7	5				−2/7	0.7 to 1.7	16	IBM Coax. Receiver	1-109
360 I/O	DS75127		7	5				−2/7	0.7 to 1.7	16	IBM Coax. Receiver	1-109
360 I/O	DS75128		8	5	Strobed			−2/7	0.7 to 1.7	16	IBM Coax. Receiver	1-113
360 I/O	DS75129		8	5	Strobed			−2/7	0.7 to 1.7	16	IBM Coax. Receiver	1-113
	DS26LS33C	DS26LS33M	4	5	TRI-STATE		200	±15	±0.5	17		1-32
	DS26LS33AC		4	5	TRI-STATE		200	±15	±0.5	23	Fail-Safe	1-32

BALANCED DIFFERENTIAL TRANSMISSION LINE DRIVERS AND RECEIVERS

The balanced or differential scheme of data transmission is preferred for applications incorporating high data rates and long transmission lines in the presence of high common-mode noise. Induced signals appear as common-mode levels and are rejected by the differential line receiver.



C112-2

BALANCED DIFFERENTIAL TRANSMISSION LINE DRIVERS AND RECEIVERS (Continued)

BALANCED DRIVERS

Standard	Device Number		Circuits Per Package	Power Supplies (V)	Open Collector	Party-Line Application	TRI-STATE	V_{OH} (V) I_{OH} (mA)	V_{OL} (V) I_{OL} (mA) (V)	Propagation Delay (ns)	Comments	Page No.
	Commercial 0°C to +70°C	Military −55°C to +125°C										
RS-422	DS26C31											1-28
RS-422	DS26LS31C	DS26LS31M	4	5		Yes	Yes	2.5/−20	0.5/40	12		1-25
RS-422	DS3487	DS3587	4	5		Yes	Yes	2.0/−50	0.5/48	15		1-45
RS-422	DS34C87											1-48
RS-422	DS3691	DS1691A	2	+5 or ±5		Yes	Yes	2/−20	−2/20	200		1-68
RS-422	DS8921, 21A		1	5		No	No	2.5/−20	0.5/20	12	Transceiver	1-170
RS-422	DS8922 DS8922A		2	5		Yes	Yes	2.5/−20	0.5/20	12	Dual Transceiver with Driver/Receiver Pair Disable	1-175
RS-422	DS8923 DS8923A		2	5		Yes	Yes	2.5/−20	0.5/20	12	Dual Transceiver with Separate Driver and Receiver Disables	1-175
RS-485	DS3695		1	5		Yes	Yes			15	Transceiver	1-79
RS-485	DS3696		1	5		Yes	Yes			15	Transceiver with Line Fault Reporting	1-79
RS-485	DS3697		1	5		Yes	Yes			15	Repeater	1-79
RS-485	DS3698		1	5		Yes	Yes			15	Repeater with Line Fault Reporting	1-79
RS-485	DS75176A		1	5		Yes	Yes				Transceiver	1-126
	DS8830	DS7830	2	5		No	No	1.8/−40	0.5/40	10		1-144
	DS8831	DS7831	2	5		Yes	Yes	1.8/−40	0.5/40	10		1-148
	DS8832	DS7832	2	5		Yes	Yes	1.8/−40	0.5/40	10	DS8831 without V_{CC} Clamp Diode	1-148
	DS8924		4	5		Yes	Yes	2.0/−48	0.5/48	12		1-181
	DS75113	DS55113	2	5	Optional	Yes	Yes	2.0/−40	0.4/40	13		1-85
	DS75114	DS55114	2	5	Optional			2.0/−40	0.4/40	15		1-92
	MM88C29	MM78C29	2	5 or 15				2.9/−57	0.4/11	100		CMOS
	MM88C30	MM78C30	2	5 or 15				2.9/−57	0.4/11	100		CMOS

BALANCED RECEIVERS

Standard	Device Number		Circuits Per Package	Power Supplies (V)	Strobed or TRI-STATE	Response Control	Hysteresis (mV)	Common-Mode Range (V)	Threshold Sensitivity (V)	Propagation Delay (ns)	Comments	Page No.
	Commercial 0°C to +70°C	Military −55°C to +125°C										
RS-422	DS26C32		4		TRI-STATE							1-35
RS-422	DS26LS32C	DS26LS32M	4	5	TRI-STATE		100	±7	±200	17		1-32
RS-422	DS26LS32AC		4	5	TRI-STATE		100	±7	±200	17	Fail-Safe	1-32
RS-422	DS3486		4	5	TRI-STATE		80	±10	±200	17		1-38
RS-422	DS34C86		4	5	TRI-STATE							1-42
RS-422	DS88C20	DS78C20	2	5 to 15	Strobed	Yes	50	±10	±200	60	Fail-Safe CMOS Compatible	1-140
RS-422	DS88C120	DS78C120	2	5 to 15	Strobed	Yes	50	±10	±200	60		1-155
RS-422	DS88LS120	DS78LS120	2	5	Strobed	Yes	50	±10	±200	50		1-163
RS-422	DS8921		1	5			50	±7	±200			1-170
RS-422	DS8921A		1	5			50	±7	±200		Low Skew	1-170
RS-422	DS8922		2	5	TRI-STATE		50	±7	±200			1-175
RS-422	DS8922A		2	5	TRI-STATE		50	±7	±200		Low Skew	1-175
RS-422	DS8923		2	5	TRI-STATE		50	±7	±200			1-175
RS-422	DS8923A		2	5	TRI-STATE		50	±7	±200		Low Skew	1-175
RS-485	DS3695		1	5	TRI-STATE		70	+12/−7	±200	22	Transceiver	1-79
RS-485	DS3696		1	5	TRI-STATE		70	+12/−7	±200	22	Transceiver with Line Fault Reporting	1-79
RS-485	DS3697		1	5	TRI-STATE		70	+12/−7	±200	22	Repeater	1-79
RS-485	DS3698		1	5	TRI-STATE		70	+12/−7	±200	22	Repeater with Line Fault Reporting	1-79
RS-485	DS75176A		1	5	TRI-STATE		70	+12/−7	±200		Transceiver	1-126
	DS3603	DS1603	2	±5	TRI-STATE			±3	±25	17		1-52
	DS3650	DS1650	4	±5	TRI-STATE			±3	±25	10		1-60
	DS3652	DS1652	4	±5	Strobed			±3	±25	10		1-60
	DS8820	DS7820	2	5	Strobed	Yes		±15	±1000	40		1-131
	DS8820A	DS7820A	2	5	Strobed	Yes		±15	±1000	30		1-135
	DS75107	DS55107	2	±5	Strobed			±3	±25	17		1-52
	DS75108	DS55108	2	±5	Strobed			±3	±25	17		1-52
	DS75115	DS55115	2	5	Strobed	Yes		±15	±500	20		1-97
	DS75208		2	±5	Strobed			±3	±10	17		1-52

National Semiconductor Corporation

DS1488 Quad Line Driver

General Description

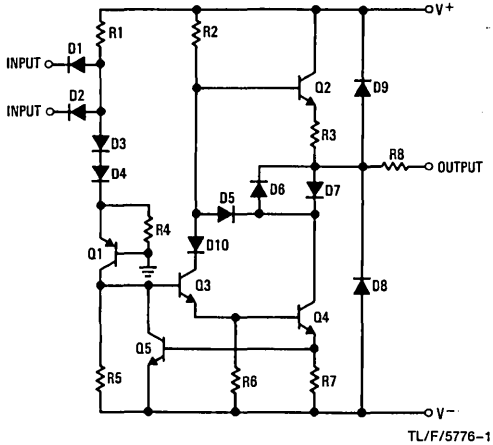
The DS1488 is a quad line driver which converts standard TTL input logic levels through one stage of inversion to output levels which meet EIA Standard No. RS-232C and CCITT Recommendation V.24.

Features

- Current limited output ±10 mA typ
- Power-off source impedance 300Ω min
- Simple slew rate control with external capacitor
- Flexible operating supply range
- Inputs are TTL/LS compatible

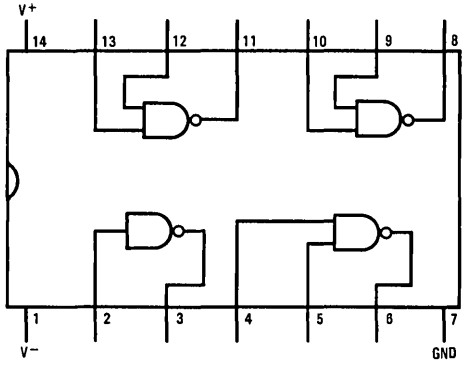
Schematic and Connection Diagrams

1/4 Circuit



TL/F/5776-1

Dual-In-Line Package



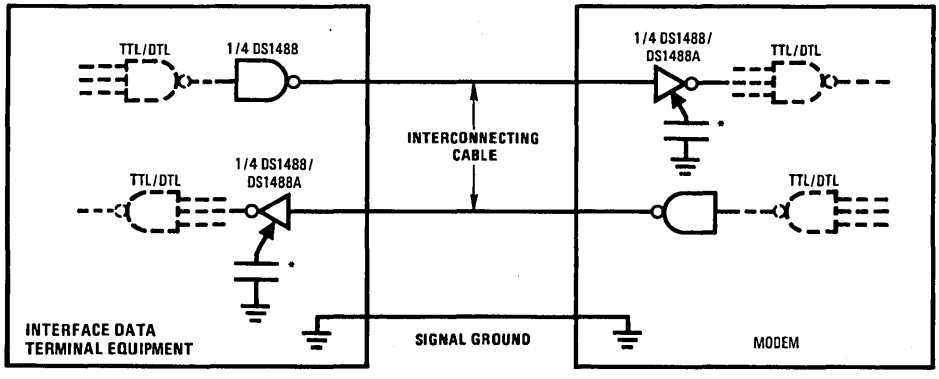
TL/F/5776-2

Top View

Order Number DS1488J, DS1488M or DS1488N
See NS Package Number J14A, M14A or N14A

Typical Applications

RS-232C Data Transmission



TL/F/5776-3

*Optional for noise filtering

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	
V^+	±15V
V^-	−15V
Input Voltage (V_{IN})	$-15V \le V_{IN} \le 7.0V$
Output Voltage	±15V
Operating Temperature Range	0°C to +75°C
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1364 mW
Molded DIP Package	1280 mW
SO Package	974 mW
Lead Temperature (Soldering, 4 sec.)	260°C

*Derate cavity package 9.1 mW/°C above 25°C; derate molded DIP package 10.2 mW/°C above 25°C; derate SO package 7.8 mW/°C above 25°C.

Electrical Characteristics (Notes 2 and 3) $V_{CC}+ = 9V$, $V_{CC}- = -9V$ unless otherwise specified

Symbol	Parameter	Conditions		Min	Typ	Max	Units
I_{IL}	Logical "0" Input Current	$V_{IN} = 0V$			−1.0	−1.3	mA
I_{IH}	Logical "1" Input Current	$V_{IN} = +5.0V$			0.005	10.0	µA
V_{OH}	High Level Output Voltage	$R_{IL} = 3.0\ k\Omega$, $V_{IN} = 0.8V$	$V^+ = 9.0V, V^- = -9.0V$	6.0	7.0		V
			$V^+ = 13.2V, V^- = -13.2V$	9.0	10.5		V
V_{OL}	Low Level Output Voltage	$R_L = 3.0\ k\Omega$, $V_{IN} = 1.9V$	$V^+ = 9.0V, V^- = -9.0V$	−6.0	−6.8		V
			$V^+ = 13.2V, V^- = -13.2V$	−9.0	−10.5		V
$I_{OS}+$	High Level Output Short-Circuit Current	$V_{OUT} = 0V$, $V_{IN} = 0.8V$		−6.0	−10.0	−12.0	mA
$I_{OS}-$	Low Level Output Short-Circuit Current	$V_{OUT} = 0V$, $V_{IN} = 1.9V$		6.0	10.0	12.0	mA
R_{OUT}	Output Resistance	$V^+ = V^- = 0V$, $V_{OUT} = \pm 2V$		300			Ω
$I_{CC}+$	Positive Supply Current (Output Open)	$V_{IN} = 1.9V$	$V^+ = 9.0V, V^- = -9.0V$		15.0	20.0	mA
			$V^+ = 12V, V^- = -12V$		19.0	25.0	mA
			$V^+ = 15V, V^- = -15V$		25.0	34.0	mA
		$V_{IN} = 0.8V$	$V^+ = 9.0V, V^- = -9.0V$		4.5	6.0	mA
			$V^+ = 12V, V^- = -12V$		5.5	7.0	mA
			$V^+ = 15V, V^- = -15V$		8.0	12.0	mA
$I_{CC}-$	Negative Supply Current (Output Open)	$V_{IN} = 1.9V$	$V^+ = 9.0V, V^- = -9.0V$		−13.0	−17.0	mA
			$V^+ = 12V, V^- = -12V$		−18.0	−23.0	mA
			$V^+ = 15V, V^- = -15V$		−25.0	−34.0	mA
		$V_{IN} = 0.8V$	$V^+ = 9.0V, V^- = -9.0V$		−0.001	−0.015	mA
			$V^+ = 12V, V^- = -12V$		−0.001	−0.015	mA
			$V^+ = 15V, V^- = -15V$		−0.01	−2.5	mA
P_d	Power Dissipation	$V^+ = 9.0V, V^- = -9.0V$			252	333	mW
		$V^+ = 12V, V^- = -12V$			444	576	mW

Switching Characteristics ($V_{CC} = 9V$, $V_{EE} = -9V$, $T_A = 25°C$)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd1}	Propagation Delay to a Logical "1"	$R_L = 3.0\ k\Omega$, $C_L = 15\ pF$, $T_A = 25°C$		230	350	ns
t_{pd0}	Propagation Delay to a Logical "0"	$R_L = 3.0\ k\Omega$, $C_L = 15\ pF$, $T_A = 25°C$		70	175	ns
t_r	Rise Time	$R_L = 3.0\ k\Omega$, $C_L = 15\ pF$, $T_A = 25°C$		75	100	ns
t_f	Fall Time	$R_L = 3.0\ k\Omega$, $C_L = 15\ pF$, $T_A = 25°C$		40	75	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +75°C temperature range for the DS1488.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Applications

By connecting a capacitor to each driver output the slew rate can be controlled utilizing the output current limiting characteristics of the DS1488. For a set slew rate the appropriate capacitor value may be calculated using the following relationship

$$C = I_{SC}(\Delta T/\Delta V)$$

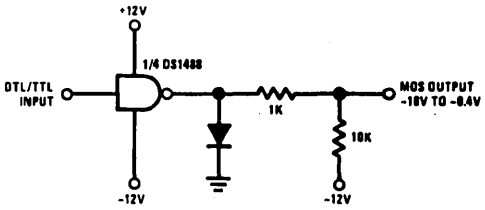
where C is the required capacitor, I_{SC} is the short circuit current value, and $\Delta V/\Delta T$ is the slew rate.

RS-232C specifies that the output slew rate must not exceed 30V per microsecond. Using the worst case output short circuit current of 12 mA in the above equation, calculations result in a required capacitor of 400 pF connected to each output.

See Typical Performance Characteristics.

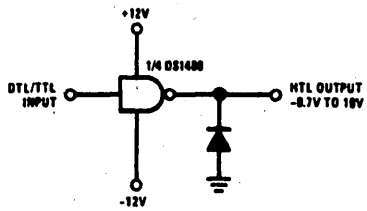
Typical Applications (Continued)

DTL/TTL-to-MOS Translator



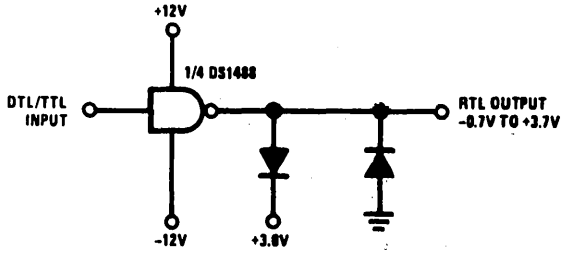
TL/F/5776–4

DTL/TTL-to-HTL Translator



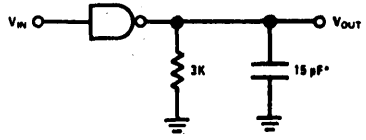
TL/F/5776–5

DTL/TTL-to-RTL Translator



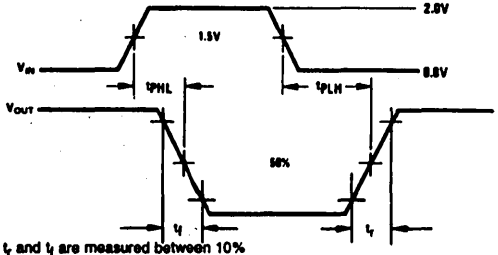
TL/F/5776–6

AC Load Circuit and Switching Time Waveforms



TL/F/5776–7

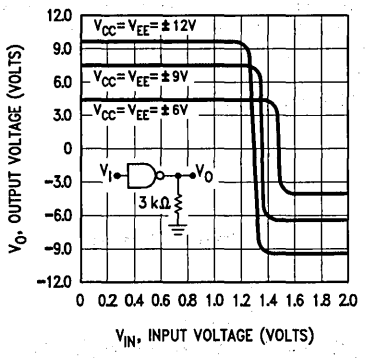
*C_L includes probe and jig capacitance.



t_r and t_f are measured between 10% and 90% of the output waveform.

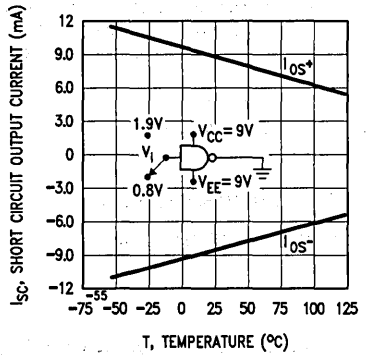
TL/F/5776–8

Typical Performance Characteristics T_A = +25°C unless otherwise noted



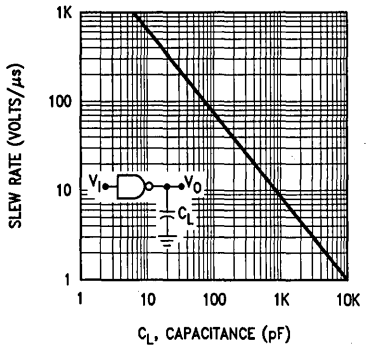
TL/F/5776–9

FIGURE 1. Transfer Characteristics vs Power Supply Voltage



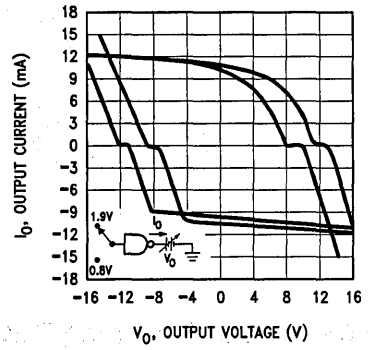
TL/F/5776–10

FIGURE 2. Short-Circuit Output Current vs Temperature



TL/F/5776–11

FIGURE 3. Output Slew Rate vs Load Capacitance



TL/F/5776–12

FIGURE 4. Output Voltage and Current-Limiting Characteristics

National Semiconductor Corporation

PRELIMINARY

DS14C88/DS14C89A Quad CMOS Line Driver/Receiver

General Description

The DS14C88 and DS14C89A, pin-for-pin replacements for the DS1488/MC1488 and the DS1489/MC1489, are line drivers/receivers designed to interface data terminal equipment (DTE) with data communications equipment (DCE). These devices translate standard TTL or CMOS logic levels to/from levels conforming to RS-232-C or CCITT V.24 standards.

Both devices are fabricated in low threshold CMOS metal gate technology. They provide very low power consumption in comparison to their bipolar equivalents; 900 μA versus 26 mA for the receiver and 500 μA versus 25 mA for the driver.

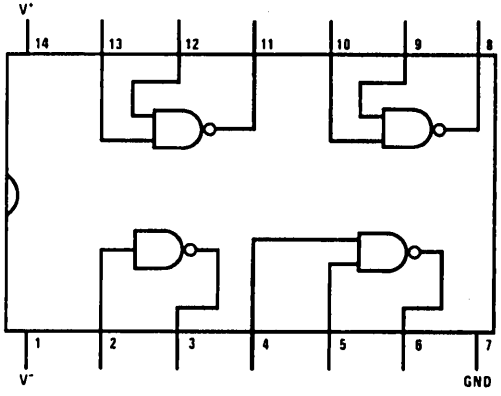
The DS14C88/DS14C89A simplify designs by eliminating the need for external capacitors. For the DS14C88, slew rate control in accordance with RS-232-C is provided on chip, eliminating the output capacitors. For the DS14C89A, noise pulse rejection circuitry eliminates the need for response control filter capacitors. When replacing the DS1489 with DS14C89A, the response control filter pins can be tied high, low or not connected.

Features

- Meets EIA RS-232-C or CCITT V.24 standard
- Low power consumption
- Pin-for-pin equivalent to DS1488/MC1488 and DS1489/MC1489
- Low Delay Slew
- DS14C88 Driver
  - — Power-off source impedance 300Ω min.
  - — Wide operating voltage range: 4.5V–12.6V
  - — TTL/LSTTL compatible
- DS14C89A
  - — Internal noise filter
  - — Inputs withstand ±30V
  - — Fail-safe operating mode
  - — Internal input threshold with hysterisis

Connection Diagrams

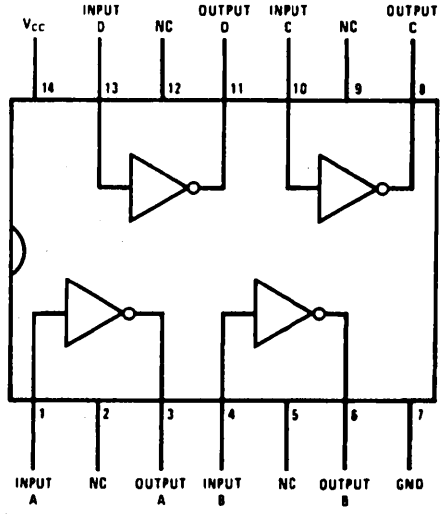
DS14C88 Dual-In-Line Package



TL/F/8508–9

Order Number DS14C88J, DS14C88N and DS14C88M
See NS Package Number J14A, M14A or N14A

DS14C89A Dual-In-Line Package



TL/F/8508–2

Order Number DS14C89AJ, DS14C89AM or DS14C89AN
See NS Package Number J14A, M14A or N14A

DS14C88 Quad CMOS Line Driver

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Voltage at Any Input Pin	$(V^+)+0.3V$ to GND$-0.3V$
Voltage at Any Output Pin	$-25V$ to $+25V$
Storage Temp.	$-65°C$ to $+150°C$
Power Dissipation	(See Note 2)
Junction Temperature	$+150°C$
Lead Temp. (Soldering 10 seconds)	$+260°C$

Operating Conditions

	Min	Max
Supply Voltage V^+ (GND = 0V)	$+4.5V$	$+12.6V$
Supply Voltage V^- (GND = 0V)	$-4.5V$	$-12.6V$
Temperature Range	0°C	$+70°C$

DC Electrical Characteristics

T_A = 0°C to +70°C, V^+ = 4.5V to 12V, GND = 0V, V^- = −4.5V to −12V unless otherwise specified

Symbol	Parameter	Conditions	Min	Max	Units
I_{IL}, I_{IH}	Maximum Input Current	V_{IN} = GND or V^+	−10	10	µA
V_{IH}	High Level Input Voltage		2.0	V_{DD}	V
V_{IL}	Low Level Input Voltage	$V^+ \geq 7V, V^- \leq -7V$	GND	0.8	V
		$V^+ \leq 7V, V^- \geq -7V$	GND	0.6	V
V_{OH}	High Level Output Voltage	$V_{IN} = V_{IL}$ R_L = 3kΩ or 7kΩ			
		$V^+ = +4.5V, V^- = -4.5V$	3.0		V
		$V^+ = +9V, V^- = -9V$	6.5		V
		$V^+ = +12V, V^- = -12V$	9.0		V
V_{OL}	Low Level Output Voltage	$V_{IN} = V_{IH}$ R_L = 3kΩ or 7kΩ			
		$V^+ = +4.5V, V^- = -4.5V$		−3.0	V
		$V^+ = +9V, V^- = -9V$		−6.5	V
		$V^+ = +12V, V^- = -12V$		−9.0	V
$I_{OS}+$	High Level Output Short Circuit Current (Note 3)	$V_{IN} = V_{IL}$ V_{OUT} = GND $V^+ = +12V, V^- = -12V$		+45	mA
$I_{OS}-$	Low Level Output Short Circuit Current (Note 3)	$V_{IN} = V_{IH}$ V_{OUT} = GND $V^+ = +12V, V^- = 12V$		−45	mA
R_{OUT}	Output Resistance	$V^+ = V^- = 0V$ $-2V \leq V_{OUT} \leq 2V$	300		Ω
$I_{CC}+$	Positive Supply Current (per package)	$V_{IN} = V_{IL}, R_L$ = open			
		$V^+ = +4.5V, V^- = -4.5V$		10	µA
		$V^+ = +9V, V^- = -9V$		30	µA
		$V^+ = +12V, V^- = -12V$		60	µA
		$V_{IN} = V_{IH}, R_L$ = open			
		$V^+ = +4.5V, V^- = -4.5V$		30	µA
		$V^+ = +9V, V^- = -9V$		190	µA
		$V^+ = +12V, V^- = -12V$		425	µA
$I_{CC}-$	Negative Supply Current (per package)	$V_{IN} = V_{IL}, R_L$ = open			
		$V^+ = +4.5V, V^- = -4.5V$		−10	µA
		$V^+ = +9V, V^- = -9V$		−10	µA
		$V^+ = +12V, V^- = -12V$		−10	µA
		$V_{IN} = V_{IH}, R_L$ = open			
		$V^+ = +4.5V, V^- = -4.5V$		−30	µA
		$V^+ = +9V, V^- = -9V$		−30	µA
		$V^+ = +12V, V^- = -12V$		−60	µA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Power Dissipation N-Package: 1300 mW at 25°C, J-Package: 1000 mW at 25°C.

Note 3: $I_{OS}+$ and $I_{OS}-$ values are for one output at a time. If more than one output is shorted simultaneously, the device dissipation may be exceeded.

DS14C88 Quad CMOS Line Driver

AC Electrical Characteristics $T_A = 0°C$ to $+70°C$, $V^+ = +4.5V$ to $12V$, GND = 0V, $V^- = -4.5V$ to $-12V$, $R_L = 3\ k\Omega$, $C_L = 50\ pF$ unless otherwise specified (Notes 4 and 5).

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd1}	Propagation Delay to a Logic "1"	$V^+ = +4.5V, V^- = -4.5V$ $V^+ = +9V, V^- = -9V$ $V^+ = +12V, V^- = -12V$			6.0 5.0 4.0	μs μs μs
t_{pd0}	Propagation Delay to a Logic "0"	$V^+ = +4.5V, V^- = -4.5V$ $V^+ = +9V, V^- = -9V$ $V^+ = +12V, V^- = -12V$			6.0 5.0 4.0	μs μs μs
t_r, t_f	Output Rise and Fall Time (Note 6)		0.2			μs
t_{SK}	Typical Propagation Delay Skew	$V^+ = 12V, V^- = -12V$		400		ns
S_R	Output Slew Rate (Note 6)	$R_L = 3\ k\Omega$ to $7\ k\Omega$ $15\ pF \le C_L \le 2.5\ nF$			30	V/μs

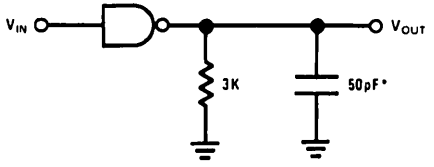
Note 4: AC input waveforms for test purposes:

$t_r = t_f \le 20$ ns, $V_{IH} = 2.0V$, $V_{IL} = 0.8V$ (0.6V at $V^+ = 4.5$, $V^- = -4.5V$)

Note 5: Input rise and fall times must not exceed 5 μs.

Note 6: The output slew rate, rise time, and fall time are measured by measuring the time from +3.0V to −3.0V on the output waveforms.

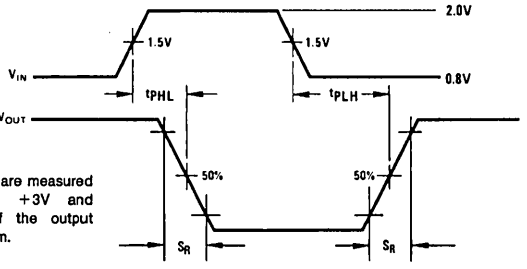
AC Load Circuit



*C_L includes probe and jig capacitance.

TL/F/8508–7

Switching Time Waveforms



t_r and t_f are measured between +3V and −3V of the output waveform.

TL/F/8508–8

DS14C89A Quad CMOS Line Receiver

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Voltage at Any Input Pin	−30V to +30V
Voltage at Any Output Pin	(V_{CC}) +0.3V to GND − 0.3V
Storage Temperature	−65°C to +150°C
Power Dissipation	500 mW at +70°C
Junction Temperature	+150°C
Lead Temp. (Soldering 10 sec)	+260°C

Operating Conditions

	Min	Max
Supply Voltage V_{CC} (GND=0V)	+4.5V	+5.5V
Temperature Range	0°C	+70°C

DC Electrical Characteristics

T_A = 0°C to +70°C, +4.5 ≤ V_{CC} ≤ 5.5V, GND = 0V, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{TH}	Input High Threshold Voltage		1.3		2.5	V
V_{TL}	Input Low Threshold Voltage		0.5		1.7	V
V_H	Typical Input Hysteresis			1.0		V
I_{IN}	Input Current	V_{IN} = +25V V_{IN} = −25V V_{IN} = +3V V_{IN} = −3V	3.6 −3.6 +0.43 −0.43		8.3 −8.3 +1.0 −1.0	mA mA mA mA
V_{OH}	Output High Voltage	V_{IN} = V_{TL} (min) I_{OUT} = −3.2 mA	2.8			V
V_{OL}	Output Low Voltage	V_{IN} = V_{TH}(max) I_{OUT} = +3.2 mA			0.4	V
I_{CC}	Supply Current	R_L = open V_{IN} = V_{TH} (max) or V_{TL} (min)			+900	μA

AC Electrical Characteristics

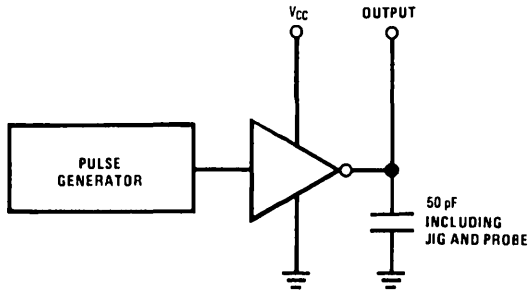
T_A = 0°C to +70°C, +4.5V ≤ V_{CC} ≤ +5.5V, GND = 0V, CL = 50 pF, unless otherwise specified (Note 2)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PLH}	Propagation Delay to a Logic "1"	Input pulse width ≥ 10 μs			6.5	μs
t_{PHL}	Propagation Delay to a Logic "0"	Input pulse width ≥ 10 μs			6.5	μs
t_{SK}	Typical Propagation Delay Skew			400		ns
t_r	Output Rise Time				300	ns
t_f	Output Fall Time				300	ns
t_{nw}	Pulse Width Assumed to be Noise				1.0	μs

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range", they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

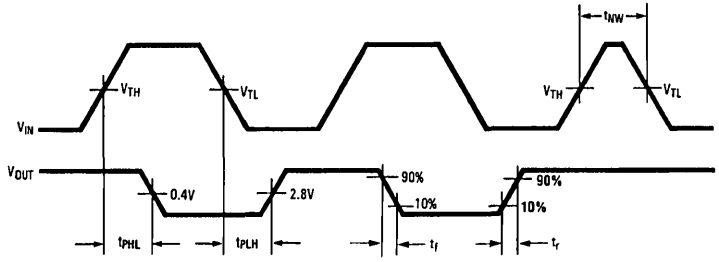
Note 2: AC input waveform for test purposes: t_r = t_f = 200 ns, V_{IH} = +3V, V_{IL} = −3V, f = 20 kHz.

DS14C89A AC Test Circuit



TL/F/8508–4

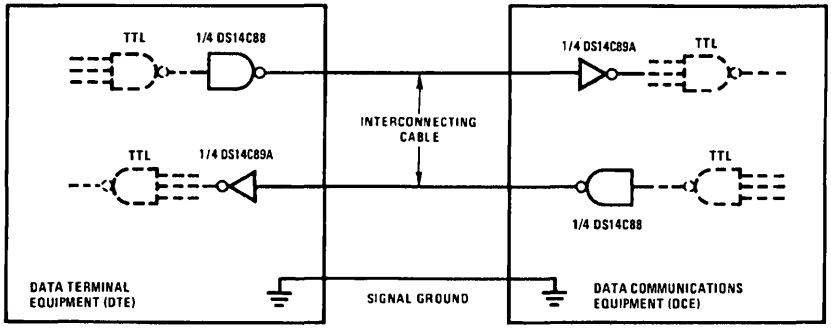
DS14C89A Timing Diagram



TL/F/8508–5

Typical Applications for DS14C88 and DS14C89A

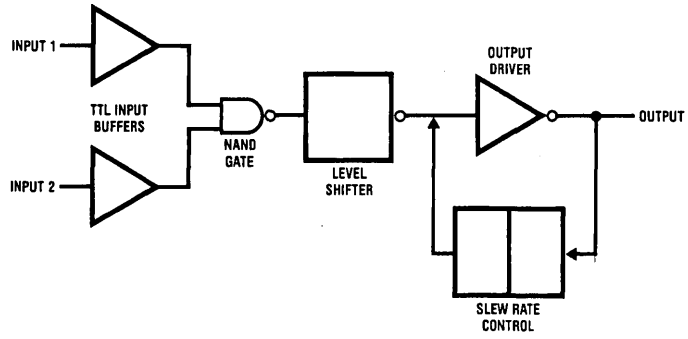
RS232C Data Transmission



TL/F/8508–3

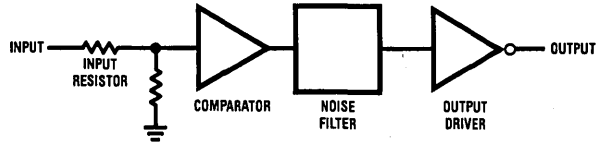
Block Diagrams

DS14C88
(¼ circuit shown)



TL/F/8508–6

DS14C89A
(¼ circuit shown)



TL/F/8508–1

National Semiconductor Corporation

DS1489/DS1489A Quad Line Receiver

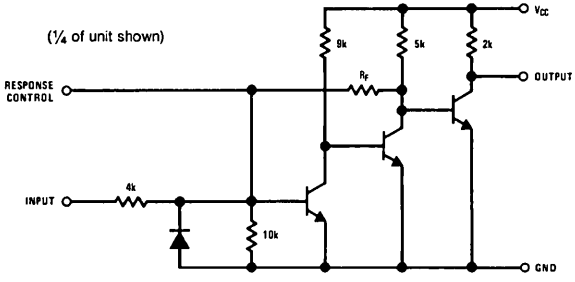
General Description

The DS1489/DS1489A are quad line receivers designed to interface data terminal equipment with data communications equipment. They are constructed on a single monolithic silicon chip. These devices satisfy the specifications of EIA Standard RS-232C. The DS1489/DS1489A meet and exceed the specifications of MC1489/MC1489A and are pin-for-pin replacements.

Features

- Four totally separate receivers per package
- Programmable threshold
- Built-in input threshold hysteresis
- "Fail safe" operating mode
- Inputs withstand ±30V

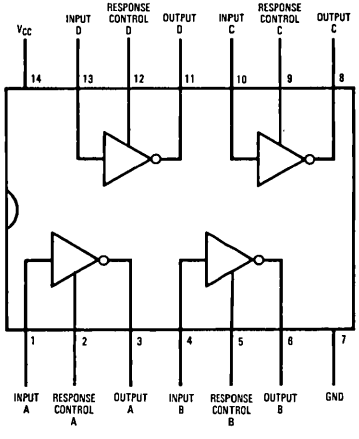
Schematic and Connection Diagrams



DS1489: R_F = 10k
DS1489A: R_F = 2k

TL/F/5777–1

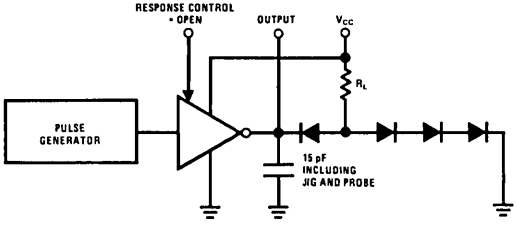
Dual-In-Line Package



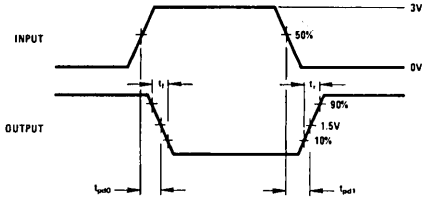
TL/F/5777–2

Top View
Order Number DS1489J, DS1489AJ, DS1489M, DS1489AM, DS1489N or DS1489AN
See NS Package Number J14A, M14A or N14A

AC Test Circuit and Voltage Waveforms



TL/F/5777–3



TL/F/5777–4

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Power Supply Voltage	10V
Input Voltage Range	±30V
Output Load Current	20 mA
Power Dissipation (Note 2)	1W
Operating Temperature Range	0°C to +75°C
Storage Temperature Range	−65°C to +150°C

Maximum Power Dissipation* at 25°C	
Cavity Package	1308 mW
Molded DIP Package	1207 mW
SO Package	1042 mW
Lead Temperature (Soldering, 4 sec.)	260°C

*Derate cavity package 8.7 mW/°C above 25°C; derate molded DIP package 9.7 mW/°C above 25°C; derate SO package 8.33 mW/°C above 25°C.

Electrical Characteristics (Notes 2, 3 and 4)

DS1489/DS1489A: The following apply for V_{CC} = 5.0V ±1%, 0°C ≤ T_A ≤ +75°C unless otherwise specified.

Symbol	Parameter	Conditions			Min	Typ	Max	Units
V_{TH}	Input High Threshold Voltage	V_{OUT} ≤ 0.45V, I_{OUT} = 10 mA	DS1489	T_A = 25°C	1.0	1.25	1.5	V
					0.9		1.6	V
			DS1489A	T_A = 25°C	1.75	2.00	2.25	V
					1.55		2.40	V
V_{TL}	Input Low Threshold Voltage	V_{OUT} ≥ 2.5V, I_{OUT} = −0.5 mA		T_A = 25°C	0.75	1.00	1.25	V
					0.65		1.35	V
I_{IN}	Input Current	V_{IN} = +25V			+3.6	+5.6	+8.3	mA
		V_{IN} = −25V			−3.6	−5.6	−8.3	mA
		V_{IN} = +3V			+0.43	+0.53		mA
		V_{IN} = −3V			−0.43	−0.53		mA
V_{OH}	Output High Voltage	I_{OUT} = −0.5 mA	V_{IN} = 0.75V		2.6	3.8	5.0	V
			Input = Open		2.6	3.8	5.0	V
V_{OL}	Output Low Voltage	V_{IN} = 3.0V, I_{OUT} = 10 mA				0.33	0.45	V
I_{SC}	Output Short Circuit Current	V_{IN} = 0.75V				−3.0		mA
I_{CC}	Supply Current	V_{IN} = 5.0V				14	26	mA
P_d	Power Dissipation	V_{IN} = 5.0V				70	130	mW

Switching Characteristics V_{CC} = 5V, T_A = 25°C

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd1}	Input to Output "High" Propagation Delay	R_L = 3.9k, *(Figure 1)* (AC Test Circuit)		28	85	ns
t_{pd0}	Input to Output "Low" Propagation Delay	R_L = 390Ω, *(Figure 1)* (AC Test Circuit)		20	50	ns
t_r	Output Rise Time	R_L = 3.9k, *(Figure 1)* (AC Test Circuit)		110	175	ns
t_f	Output Fall Time	R_L = 390Ω, *(Figure 1)* (AC Test Circuit)		9	20	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

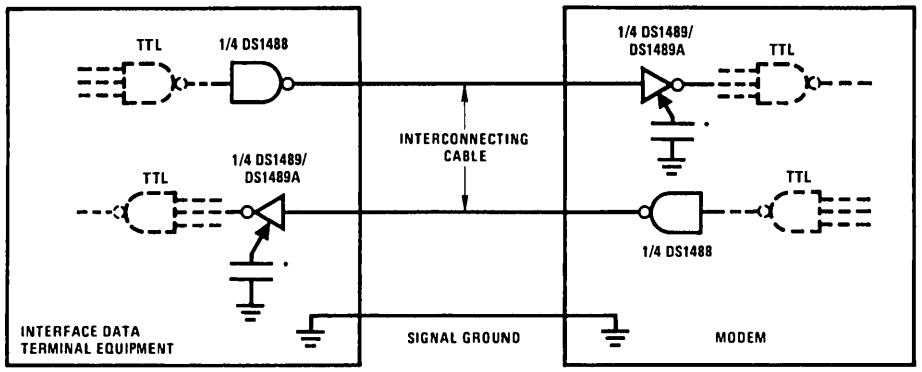
Note 2: Unless otherwise specified min/max limits apply across the 0°C to +75°C temperature range for the DS1489 and DS1489A.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: These specifications apply for response control pin = open.

Typical Applications

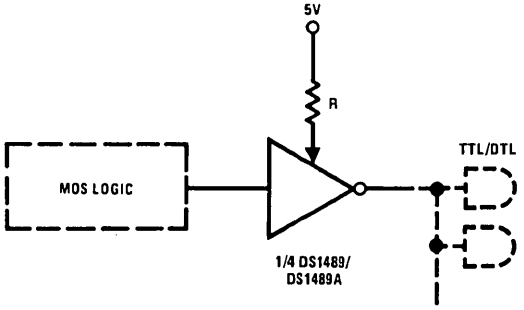
RS-232C Data Transmission



TL/F/5777–5

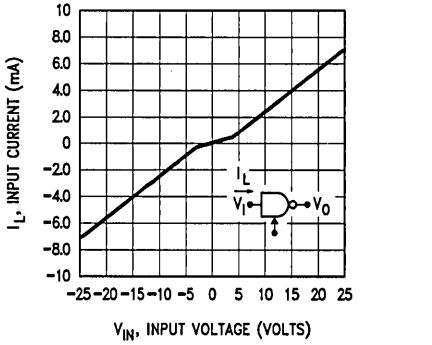
*Optional for noise filtering.

MOS to TTL/LS Translator



TL/F/5777–6

Typical Characteristics V_{CC} = 5.0 V_{DC}, T_A = +25°C unless otherwise noted



TL/F/5777–7

FIGURE 1. Input Current

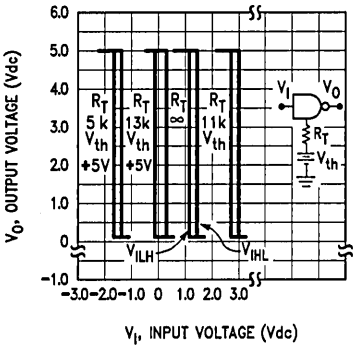


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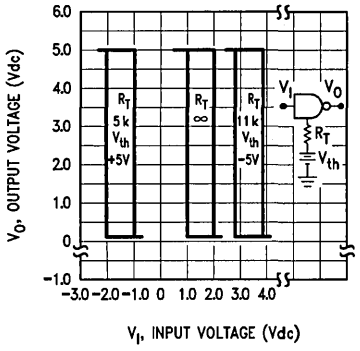
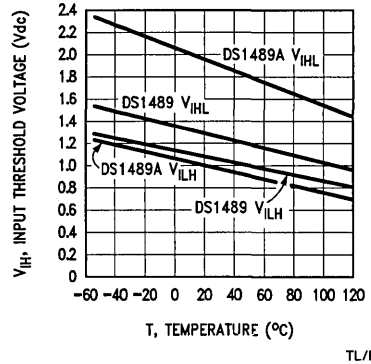
FIGURE 2. DS1489 Input Threshold Voltage Adjustment

Typical Characteristics V_{CC} = 5.0 V_{DC}, T_A = +25°C unless otherwise noted (Continued)



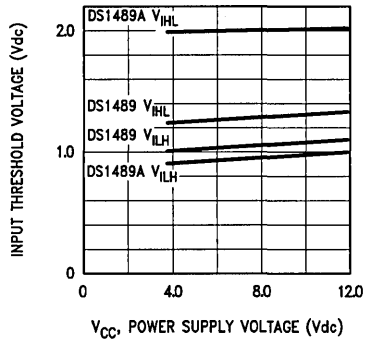
TL/F/5777-9

FIGURE 3. DS1489A Input Threshold Voltage Adjustment



TL/F/5777-10

FIGURE 4. Input Threshold Voltage vs Temperature



TL/F/5777-11

FIGURE 5. Input Threshold vs Power Supply Voltage

National Semiconductor Corporation

DS26LS31C/DS26LS31M Quad High Speed Differential Line Driver

General Description

The DS26LS31 is a quad differential line driver designed for digital data transmission over balanced lines. The DS26LS31 meets all the requirements of EIA Standard RS-422 and Federal Standard 1020. It is designed to provide unipolar differential drive to twisted-pair or parallel-wire transmission lines.

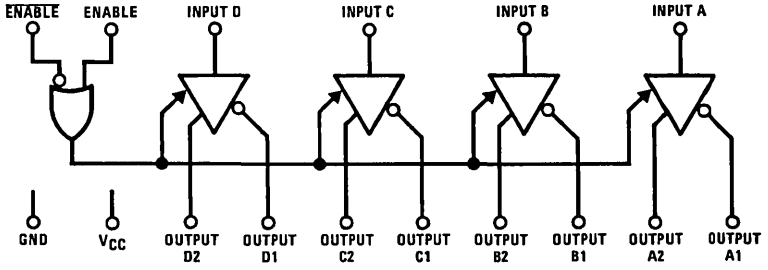
The circuit provides an enable and disable function common to all four drivers. The DS26LS31 features TRI-STATE® outputs and logically ANDed complementary outputs. The inputs are all LS compatible and are all one unit load.

The DS26LS31 features a power up/down protection circuit which keeps the output in a high impedance (TRI-STATE) state the outputs during power up or down preventing erroneous glitches on the transmission lines.

Features

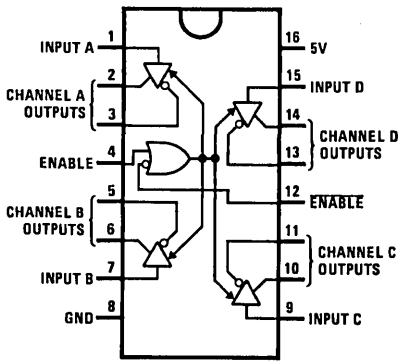
- Output skew—2.0 ns typical
- Input to output delay—10 ns
- Operation from single 5V supply
- 16-pin hermetic and molded DIP package
- Outputs won't load line when $V_{CC} = 0$
- Four line drivers in one package for maximum package density
- Output short-circuit protection
- Complementary outputs
- Meets the requirements of EIA Standard RS-422
- Pin compatible with AM26LS31
- Available in military and commercial temperature range
- Glitch free power up/down

Logic and Connection Diagrams



TL/F/5778–1

Dual-In-Line Package



TL/F/5778–2

Top View
Order Number DS26LS31CJ, DS26LS31CM, DS26LS31CN or DS26LS31MJ
See NS Package Number J16A, M16A or N16A

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	7V
Output Voltage	5V
Output Voltage (Power OFF)	−0.25 to 6V
Maximum Power Dissipation* at 25°C	
Cavity Package	1509 mW
Molded DIP Package	1476 mW
SO Package	1051 mW

*Derate cavity package 10.1 mW/°C above 25°C; derate molded DIP package 11.9 mW/°C above 25°C; derate SO package 8.41 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage, V_{CC}			
DS26LS31M	4.5	5.5	V
DS26LS31	4.75	5.25	V
Temperature, T_A			
DS26LS31M	−55	+125	°C
DS26LS31	0	+70	°C

Electrical Characteristics (Notes 2, 3 and 4)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OH}	Output High Voltage	I_{OH} = −20 mA	2.5			V
V_{OL}	Output Low Voltage	I_{OL} = 20 mA			0.5	V
V_{IH}	Input High Voltage		2.0			V
V_{IL}	Input Low Voltage				0.8	V
I_{IL}	Input Low Current	V_{IN} = 0.4V		−40	−200	μA
I_{IH}	Input High Current	V_{IN} = 2.7V			20	μA
I_I	Input Reverse Current	V_{IN} = 7V			0.1	mA
I_O	TRI-STATE Output Current	V_O = 2.5V			20	μA
		V_O = 0.5V			−20	μA
V_{CL}	Input Clamp Voltage	I_{IN} = −18 mA			−1.5	V
I_{SC}	Output Short-Circuit Current		−30		−150	mA
I_{CC}	Power Supply Current	All Outputs Disabled or Active		35	60	mA

Switching Characteristics V_{CC} = 5V, T_A = 25°C

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PLH}	Input to Output	C_L = 30 pF		10	15	ns
t_{PHL}	Input to Output	C_L = 30 pF		10	15	ns
Skew	Output to Output	C_L = 30 pF		2.0	6.0	ns
t_{LZ}	Enable to Output	C_L = 10 pF, S2 Open		15	35	ns
t_{HZ}	Enable to Output	C_L = 10 pF, S1 Open		15	25	ns
t_{ZL}	Enable to Output	C_L = 30 pF, S2 Open		20	30	ns
t_{ZH}	Enable to Output	C_L = 30 pF, S1 Open		20	30	ns

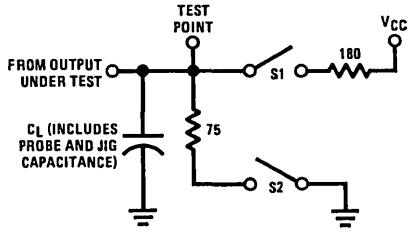
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS726LS31M and across the 0°C to +70°C range for the DS26LS31. All typicals are given for V_{CC} = 5V and T_A = 25°C.

Note 3: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified.

Note 4: Only one output at a time should be shorted.

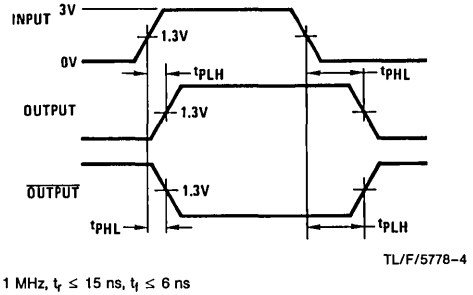
AC Test Circuit and Switching Time Waveforms



TL/F/5778-3

Note: S1 and S2 of load circuit are closed except where shown.

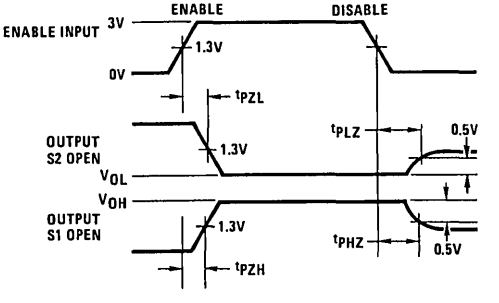
FIGURE 1. AC Test Circuit



TL/F/5778-4

f = 1 MHz, $t_r \leq 15$ ns, $t_f \leq 6$ ns

FIGURE 2. Propagation Delays



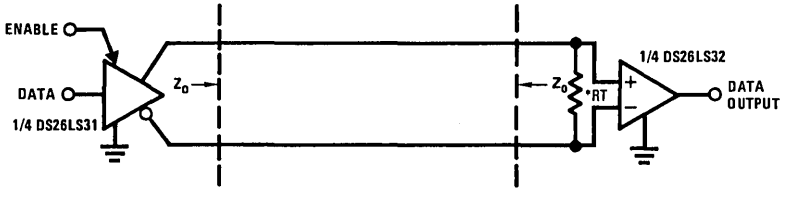
TL/F/5778-5

f = 1 MHz, $t_r \leq 15$ ns, $t_f \leq 6$ ns

FIGURE 3. Enable and Disable Times

Typical Applications

Two-Wire Balanced System, RS-422



TL/F/5778-6

*R_T is optional although highly recommended to reduce reflection.

National Semiconductor Corporation

PRELIMINARY

DS26C31C CMOS Quad TRI-STATE® Differential Line Driver

General Description

The DS26C31 is a quad differential line driver designed for digital data transmission over balanced lines. The DS26C31 meets all the requirements of EIA standard RS-422 while retaining the low power characteristics of CMOS. This enables the construction of serial and terminal interfaces while maintaining minimal power consumption.

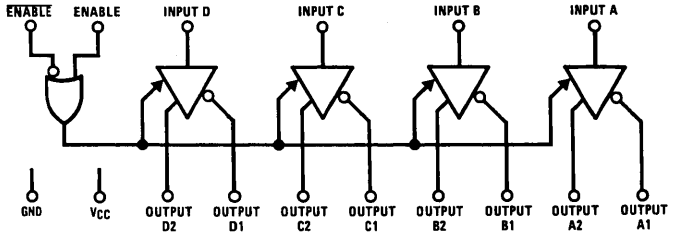
The DS26C31 accepts TTL or CMOS input levels and translates these to RS-422 output levels. This part uses special output circuitry that enables the individual drivers to power down without loading down the bus. The DS26C31 also includes special power up and down circuitry which will TRI-STATE the outputs during power up or down, preventing spurious glitches on its outputs. This device has enable and disable circuitry common to all four drivers. The DS26C31 is pin compatible to the AM26LS31 and the DS26LS31.

All inputs are protected against damage due to electrostatic discharge by diodes to V_{CC} and ground.

Features

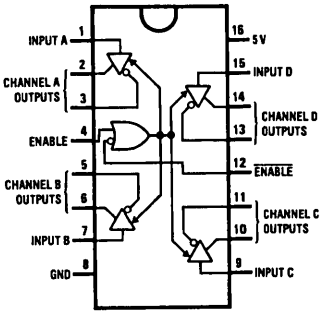
- TTL input compatible
- Typical propagation delays: 10 ns
- Typical output skew: 0.5 ns
- Outputs won't load line when V_{CC} = 0V
- Meets the requirements of EIA standard RS-422
- Operation from single 5V supply
- TRI-STATE outputs for connection to system buses
- Low quiescent current

Logic and Connection Diagrams



TL/F/8574–2

Dual-In-Line Package



TL/F/8574–1

Top View
Order Number DS26C31CJ, DS26C31CM or DS26C31CN
See NS Package Number J16A, M16A or N16A

Truth Table

Active High Enable	Active Low Enable	Input	Non-Inverting Output	Inverting Output
L	H	X	Z	Z
All other combinations of enable inputs		L	L	H
		H	H	L

L = Low logic state
H = High logic state
X = Irrelevant
Z = TRI-STATE (high impedance)

Absolute Maximum Ratings (Notes 1 & 2)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage (V_{CC})	−0.5 to 7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±150 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±150 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering, 4 sec.)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.75	5.25	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temperature Range (T_A)	−40	+85	°C
Input Rise or Fall Times (t_r, t_f)		500	ns

DC Electrical Characteristics V_{CC} = 5V ±5% (unless otherwise specified) (Note 4)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IH}	High Level Input Voltage			2.0			V
V_{IL}	Low Level Input Voltage					0.8	V
V_{OH}	High Level Output Voltage	V_{IN} = V_{IH} or V_{IL}, I_{OUT} = −20 mA		2.5			V
V_{OL}	Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL}, I_{OUT} = 20 mA				0.5	V
V_T	Differential Output Voltage	R_L = 100Ω (Note 5)		2.0			V
$\lvert V_T \rvert - \lvert \overline{V_T} \rvert$	Difference In Differential Output	R_L = 100Ω (Note 5)				0.4	V
V_{OS}	Common Mode Output Voltage	R_L = 100Ω (Note 5)				3.0	V
$\lvert V_{OS} - \overline{V_{OS}} \rvert$	Difference In Common Mode Output	R_L = 100Ω (Note 5)				0.4	V
I_{IN}	Input Current	V_{IN} = V_{CC}, GND, V_{IH}, or V_{IL}				±1.0	µA
I_{CC}	Quiescent Supply Current	I_{OUT} = 0 µA, V_{IN} = V_{CC} or GND V_{IN} = 2.4V or 0.5V (Note 6)			200 0.8		µA mA
I_{OZ}	TRI-STATE Output Leakage Current	V_{OUT} = V_{CC} or GND, ENABLE = V_{IL}, $\overline{\text{ENABLE}}$ = V_{IH}			±0.5	±0.5	µA
I_{SC}	Output Short Circuit Current	V_{IN} = V_{CC} or GND (Note 7)		−30		−150	mA
I_{OFF}	Output Leakage Current Power Off	V_{CC} = 0	V_{OUT} = 6V			100	µA
			V_{OUT} = −0.25V			−100	µA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified, all voltages are referenced to ground. All currents into device pins are positive, all currents out of device pins are negative.

Note 3: Power Dissipation temperature derating-plastic "N" package: −12 mW/°C from 65°C to 85°C.
ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: Unless otherwise specified, min/max limits apply across the −40°C to 85°C temperature range. All typicals are given for V_{CC} = 5V and T_A = 25°C.

Note 5: See EIA Specification RS-422 for exact test conditions.

Note 6: Measured per input. All other inputs at V_{CC} or GND.

Note 7: Only one output at a time should be shorted.

Switching Characteristics V_{CC} = 5V ±5%, $t_r = t_f$ = 6 ns (*Figures 1, 2, 3* and *4*) (Note 4)

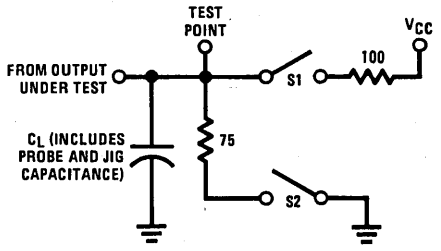
Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PLH}, t_{PHL}	Propagation Delay Input to Output	C_L = 50 pF		8		ns
Skew	(Note 8)	C_L = 50 pF		0.5		ns
t_{TLH}, t_{THL}	Differential Output Rise And Fall Times	C_L = 50 pF		4		ns
t_{PZH}	Output Enable Time	C_L = 50 pF S1 Open		18		ns
t_{PZL}	Output Enable Time	C_L = 50 pF S2 Open		19		ns
t_{PHZ}	Output Disable Time (Note 9)	C_L = 50 pF S1 Open		9		ns
t_{PLZ}	Output Disable Time (Note 9)	C_L = 50 pF S2 Open		9		ns
C_{PD}	Power Dissipation Capacitance (Note 10)			100		pF
C_{IN}	Input Capacitance			10		pF

Note 8: Skew is defined as the difference in propagation delays between complementary outputs at the 50% point.

Note 9: Output disable time is the delay from ENABLE or $\overline{\text{ENABLE}}$ being switched to the output transistors turning off. The actual disable times are less than indicated due to the delay added by the RC time constant of the load. The added delay is typically 1 ns for t_{PLZ} and 0.6 ns for t_{PHZ}.

Note 10: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

AC Test Circuit and Switching Time Waveforms



TL/F/8574–3

Note: S1 and S2 of load circuit are closed except where shown.

FIGURE 1. AC Test Circuit

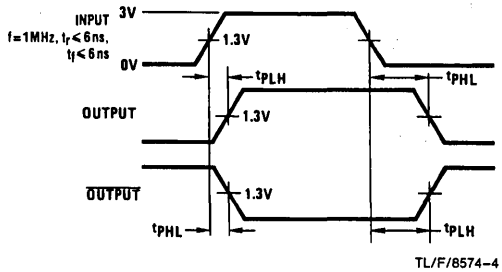


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FIGURE 2. Propagation Delays

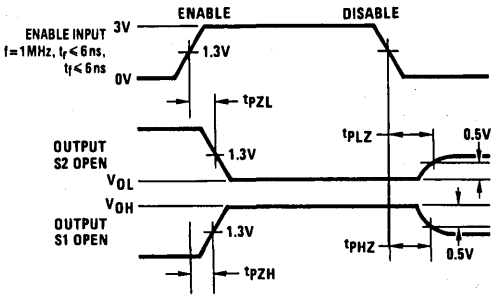

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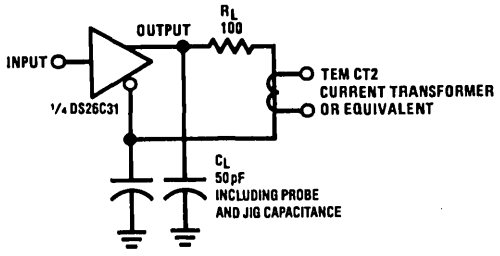
FIGURE 3. Enable and Disable Times

AC Test Circuit and Switching Time Waveforms (Continued)



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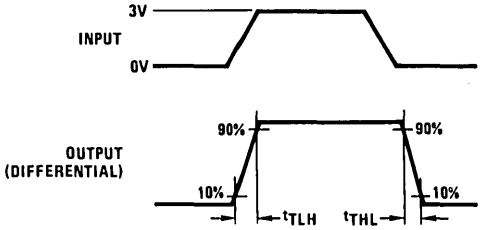

Input pulse; f = 1MHz, 50%; $t_r = t_f \leq 6$ns.

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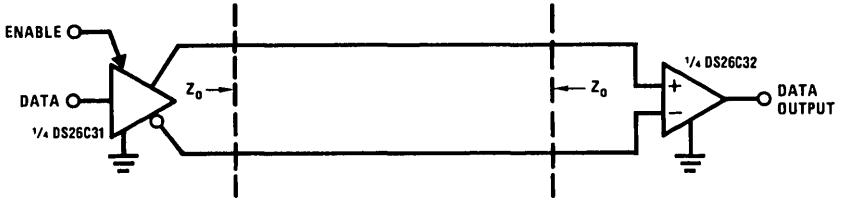
FIGURE 4. Differential Rise and Fall Times

Typical Applications

Two-Wire Balanced System, RS-422



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National Semiconductor Corporation

DS26LS32C/DS26LS32M/DS26LS32AC/DS26LS33C/ DS26LS33M/DS26LS33AC Quad Differential Line Receivers

General Description

The DS26LS32 and DS26LS32A are quad differential line receivers designed to meet the RS-422, RS-423 and Federal Standards 1020 and 1030 for balanced and unbalanced digital data transmission.

The DS26LS32 and DS26LS32A have an input sensitivity of 200 mV over the input voltage range of ±7V and the DS26LS33 and DS26LS33A have an input sensitivity of 500 mV over the input voltage range of ±15%V.

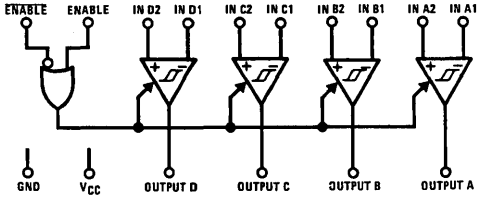
Both the DS26LS32A and DS26LS33A differ in function from the popular DS26LS32 and DS26LS33 in that input fail-safe circuitry is provided for each receiver, which causes the outputs to go to a logic "1" state when the inputs are open.

Each version provides an enable and disable function common to all four receivers and features TRI-STATE® outputs with 8 mA sink capability. Constructed using low power Schottky processing, these devices are available over the full military and commerical operating temperature ranges.

Features

- High differential or common-mode input voltage ranges of ±7V on the DS26LS32 and DS26LS32A and ±15V on the DS26LS33 and DS26LS33A
- ±0.2V sensitivity over the input voltage range on the DS26LS32 and DS26LS32A, ±0.5V sensitivity on the DS26LS33 and DS26LS33A
- Input fail-safe circuitry on the DS26LS32A and DS26LS33A
- DS26LS32 and DS26LS32A meet all requirements of RS-422 and RS-423
- 6k minimum input impedance
- 100 mV input hysteresis on the DS26LS32 and DS26LS32A, 200 mV on the DS26LS33 and DS26LS33A
- Operation from a single 5V supply
- TRI-STATE drive, with choice of complementary output enables for receiving directly onto a data bus
- Pin replacement for Advanced Micro Devices AM26LS32

Logic Diagram



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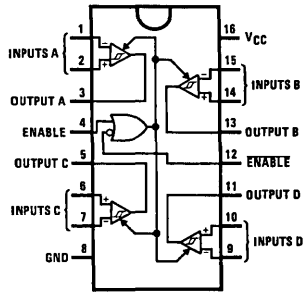
Connection Diagram

Dual-In-Line Package



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Top View

Truth Table

ENABLE	$\overline{\text{ENABLE}}$	Input	Output
1	1	X	Hi-Z
See Note Below		$V_{ID} \geq V_{TH}$ (Max)	1
		$V_{ID} \leq V_{TH}$ (Min)	0
		Open	1*

Hi-Z = TRI-STATE

*DS26LS32A and DS26LS33A only

Note: Input conditions may be any combination not defined for ENABLE and $\overline{\text{ENABLE}}$.

Order Number DS26LS32MJ, DS26LS32CJ, DS26LS32CM, DS26LS32CN, DS26LS32ACJ, DS26LS32ACN, DS26LS32ACM, DS26LS33MJ, DS26LS33CJ, DS26LS33CN, DS26LS33ACJ or DS26LS33ACN
See NS Package Number J16A, M16A or N16A

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Common-Mode Range	±25V
Differential Input Voltage	±25V
Enable Voltage	7V
Output Sink Current	50 mA
Maximum Power Dissipation* at 25°C	
Cavity Package	1433 mW
Molded Dip Package	1362 mW
SO Package DS26LS32	1002 mW
DS26LS232A	1051 mW

*Derate cavity package 9.6 mW/°C above 25°C; derate molded DIP package 10.9 mW/°C above 25°C.

Derate SO Package 8.01 mW/°C for DS26LS32
8.41 mW/°C for DS26LS32A

Storage Temperature Range	−65°C to +165°C
Lead Temperature (Soldering, 4 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage, (V_{CC})			
DS26LS32M, DS26LS33M (MIL)	4.5	5.5	V
DS26LS32C, DS26LS33C DS26LS32AC, DS26LS33AC (COML)	4.75	5.25	V
Temperature, (T_A)			
DS26LS32M, DS26LS33M (MIL)	−55	+125	°C
DS26LS32C, DS26LS33C DS26LS32AC, DS26LS33AC (COML)	0	+70	°C

Electrical Characteristics over the operating temperature range unless otherwise specified (Notes 2, 3 and 4)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{TH}	Differential Input Voltage	$V_{OUT} = V_{OH}$ or V_{OL}	DS26LS32, DS26LS32A, $-7V \le V_{CM} \le +7V$	−0.2	±0.07	0.2	V
			DS26LS33, DS26LS33A, $-15V \le V_{CM} + 15V$	−0.5	±0.14	0.5	V
R_{IN}	Input Resistance	$-15V \le V_{CM} \le +15V$ (One Input AC GND)		6.0	8.5		kΩ
I_{IN}	Input Current (Under Test)	$V_{IN} = 15V$, Other Input $-15V \le V_{IN} \le +15V$				2.3	mA
		$V_{IN} = -15V$, Other Input $-15V \le V_{IN} \le +15V$				−2.8	mA
V_{OH}	Output High Voltage	V_{CC} = MIN, ΔV_{IN} = 1V, $V_{\overline{ENABLE}}$ = 0.8V, $I_{OH} = -440\ \mu A$	Commercial	2.7	4.2		V
			Military	2.5	4.2		V
V_{OL}	Output Low Voltage	V_{CC} = Min, $\Delta V_{IN} = -1V$, $V_{\overline{ENABLE}}$ = 0.8V	I_{OL} = 4 mA			0.4	V
			I_{OL} = 8 mA			0.45	V
V_{IL}	Enable Low Voltage					0.8	V
V_{IH}	Enable High Voltage			2.0			V
V_I	Enable Clamp Voltage	V_{CC} = Min, $I_{IN} = -18$ mA				−1.5	V
I_O	OFF-State (High Impedance) Output Current	V_{CC} = Max	V_O = 2.4V			20	μA
			V_O = 0.4V			−20	μA
I_{IL}	Enable Low Current	V_{IN} = 0.4V				−0.36	mA
I_{IH}	Enable High Current	V_{IN} = 2.7V				20	μA
I_{SC}	Output Short-Circuit Current	V_O = 0V, V_{CC} = Max, ΔV_{IN} = 1V		−15		−85	mA
I_{CC}	Power Supply Current	V_{CC} = Max, All V_{IN} = GND, Outputs Disabled	DS26LS32, DS26LS32A		52	70	mA
			DS26LS33, DS26LS33A		57	80	mA
I_I	Input High Current	V_{IN} = 5.5V				100	μA
V_{HYST}	Input Hysteresis	T_A = 25°C, V_{CC} = 5V, V_{CM} = 0V	DS26LS32, DS26S32A		100		mV
			DS26LS33, DS26LS33A		200		mV

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All currents into device pins are shown as positive, all currents out of device pins are shown as negative, all voltages are referenced to ground, unless otherwise specified. All values shown as max or min are so classified on absolute value basis.

Note 3: All typical values are V_{CC} = 5V, T_A = 25°C.

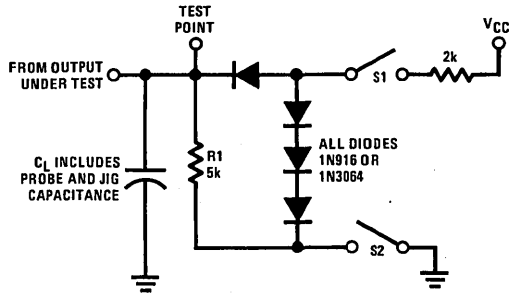
Note 4: Only one output at a time should be shorted.

Switching Characteristics V_{CC} = 5V, T_A = 25°C

Symbol	Parameter	Conditions	DS26LS32/DS26LS33			DS26LS32A/DS26LS33A			Units
			Min	Typ	Max	Min	Typ	Max	
t_{PLH}	Input to Output	C_L = 15 pF		17	25		23	35	ns
t_{PHL}				17	25		23	35	ns
t_{LZ}	ENABLE to Output	C_L = 5 pF		20	30		15	22	ns
t_{HZ}				15	22		20	25	ns
t_{ZL}	ENABLE to Output	C_L = 15 pF		15	22		14	22	ns
t_{ZH}				15	22		15	22	ns

AC Test Circuit and Switching Time Waveforms

Load Test Circuit for TRI-STATE Outputs



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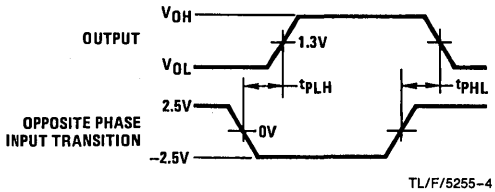
Propagation Delay (Notes 1 and 3)



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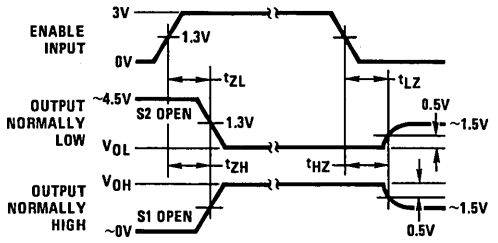
Enable and Disable Times (Notes 2 and 3)



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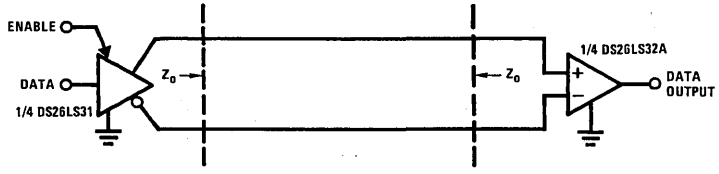
Note 1: Diagram shown for $\overline{\text{ENABLE}}$ low.

Note 2: S1 and S2 of load circuit are closed except where shown.

Note 3: Pulse generator for all pulses: Rate ≤ 1.0 MHz; Z_O = 50Ω; t_r ≤ 15 ns; t_f ≤ 6.0 ns.

Typical Applications

Two-Wire Balanced Systems, RS-422



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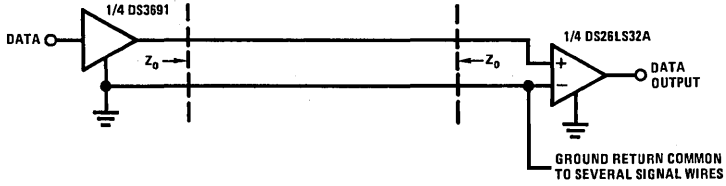
Single Wire with Common Ground Unbalanced Systems, RS-423



TL/F/5255–7

National Semiconductor Corporation

PRELIMINARY

DS26C32C Quad Differential Line Receiver

General Description

The DS26C32 is a quad differential line receiver designed to meet the RS-422, RS-423, and Federal Standards 1020 and 1030 for balanced and unbalanced digital data transmission, while retaining the low power characteristics of CMOS.

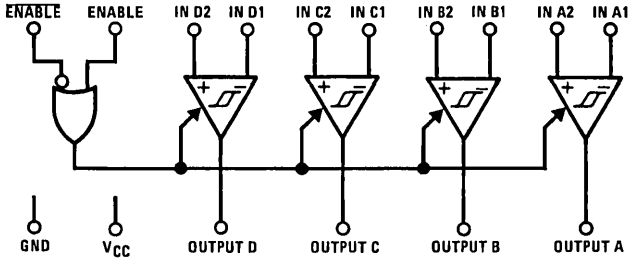
The DS26C32 has an input sensitivity of 200 mV over the common mode input voltage range of ±7V. Each receiver is also equipped with input fail-safe circuitry, which causes the output to go to a logic "1" state when the inputs are open.

The DS26C32 provides an enable and disable function common to all four receivers, and features TRI-STATE® outputs with 6 mA source and sink capability. This product is pin compatible with the DS26LS32A and the AM26LS32.

Features

- Low power CMOS design
- ±0.2V sensitivity over the entire common mode range
- Typical propagation delays: 15 ns
- Typical input hysteresis: 50 mV
- Input fail-safe circuitry
- Inputs won't load line when V_{CC} = 0V
- Meets the requirements of EIA standard RS-422
- TRI-STATE outputs for connection to system buses

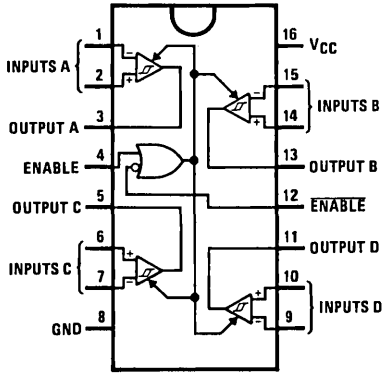
Logic Diagram



TL/F/8674–1

Connection Diagram

Dual-In-Line Package



TL/F/8674–2

Top View

Order Number DS26C32CJ, DS26C32CM, DS26C32CN, DS26C32MJ or DS26C32MN
See NS Package J16A, M16A or N16A

Truth Table

ENABLE	$\overline{\text{ENABLE}}$	Input	Output
0	1	X	Hi-Z
See Note Below		$V_{ID} \geq V_{TH}$ (Max)	1
		$V_{ID} \leq V_{TH}$ (Min)	0
		Open	1

Hi-Z = TRI-STATE

Note: Input conditions may be any combination not defined for ENABLE and $\overline{\text{ENABLE}}$.

Absolute Maximum Ratings (Notes 1 & 2)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage (V_{CC})	7V
Common Mode Range (V_{CM})	±14V
Differential Input Voltage (V_{DIFF})	±14V
Enable Input Voltage (V_{IN})	7V
Storage Temperature Range (T_{STG})	−65°C to +150°C
Lead Temperature (Soldering 4 sec.)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.75	5.25	V
Operating Temperature Range (T_A)	−40	+85	°C
Enable Input Rise or Fall Times		500	ns

DC Electrical Characteristics V_{CC} = 5V ±5% (unless otherwise specified) (Note 3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{TH}	Minimum Differential Input Voltage	$V_{OUT} = V_{OH}$ or V_{OL}	−0.2		+0.2	V
R_{IN}	Input Resistance	−15V < V_{CM} < +15V (One Input AC GND)		10		kΩ
I_{IN}	Input Current (Under Test)	V_{IN} = +10V, Other Input = GND		−1.1		mA
		V_{IN} = −10V, Other Input = GND		+1.6		mA
V_{OH}	Minimum High Level Output Voltage	V_{CC} = Min, V_{DIFF} = +1V, I_{OUT} = −6.0 mA	3.84	4.2		V
V_{OL}	Maximum Low Level Output Voltage	V_{CC} = Max, V_{DIFF} = +1V, I_{OUT} = 6.0 mA		0.2	0.33	V
V_{IH}	Minimum Enable High Input Level Voltage		2.0			V
V_{IL}	Maximum Enable Low Input Level Voltage				0.8	V
I_{OZ}	Maximum TRI-STATE Output Leakage Current	V_{OUT} = V_{CC} or GND, ENABLE = V_{IL}, $\overline{\text{ENABLE}}$ = V_{IH}		±0.5	±5.0	μA
I_I	Maximum Enable Input Current	V_{IN} = V_{CC} or GND			±1.0	μA
I_{SC}	Output Short Circuit Current	V_{CC} = Max, V_{DIFF} = +1V		65		mA
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max, V_{DIFF} = +1V		12		mA
V_{HYST}	Input Hysteresis			50		mV

AC Electrical Characteristics V_{CC} = 5V ±5% (Note 3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PLH}, t_{PHL}	Propagation Delay Input to Output	C_L = 50 pF		15		ns
t_{PLZ}, t_{PHZ}	Propagation Delay ENABLE to Output	C_L = 50 pF, R_L = 1000Ω, V_{DIFF} = 2.5V		12		ns
t_{PZL}, t_{PZH}	Propagation Delay ENABLE to Output	C_L = 50 pF, R_L = 1000Ω, V_{DIFF} = 2.5V		14		ns

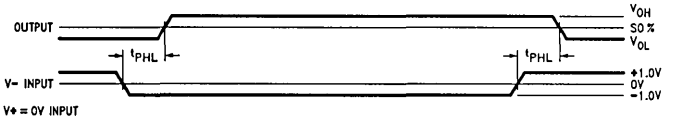
Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified, all voltages are referenced to ground.

Note 3: Unless otherwise specified, Min/Max limits apply across the −40°C to +85°C temperature range. All typicals are given for V_{CC} = 5V and T_A = 25°C.

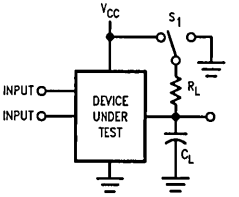
Test and Switching Waveforms

Propagation Delay



TL/F/8674-3

Test Circuit for TRI-STATE Output Tests



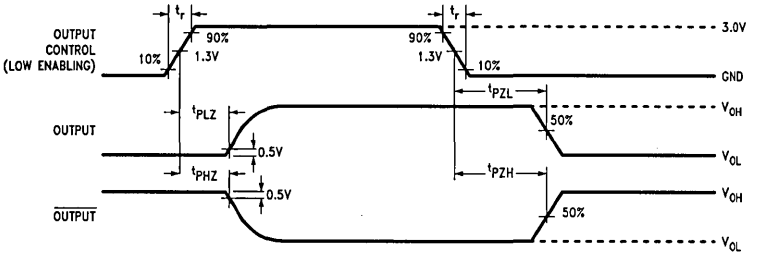
TL/F/8674-4

C_L includes load and test jig capacitance.

S1 = V_{CC} for t_{PZL}, and t_{PLZ} measurements.

S1 = Gnd for t_{PZH} and t_{PHZ} measurements.

TRI-STATE Output Enable and Disable Waveforms



TL/F/8674-5

National Semiconductor Corporation

DS3486 Quad RS-422, RS-423 Line Receiver

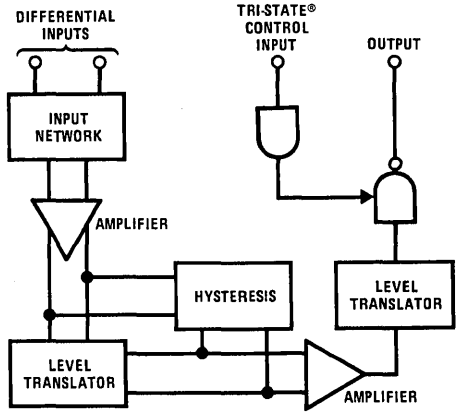
General Description

National's quad RS-422, RS-423 receiver features four independent receiver chains which comply with EIA Standards for the electrical charactersitics of balanced/unbalanced voltage digital interface circuits. Receiver outputs are 74LS compatible, TRI-STATE® structures which are forced to a high impedance state when the appropriate output control pin reaches a logic zero condition. A PNP device buffers each output control pin to assure minimum loading for either logic one or logic zero inputs. In addition, each receiver chain has internal hysteresis circuitry to improve noise margin and discourage output instability for slowly changing input waveforms.

Features

- Four independent receiver chains
- TRI-STATE outputs
- High impedance output control inputs (PIA compatible)
- Internal hysteresis −140 mV (typ)
- Fast propagation times −18 ns (typ)
- TTL compatible
- Single 5V supply voltage
- Pin compatible and interchangeable with MC3486

Block and Connection Diagrams



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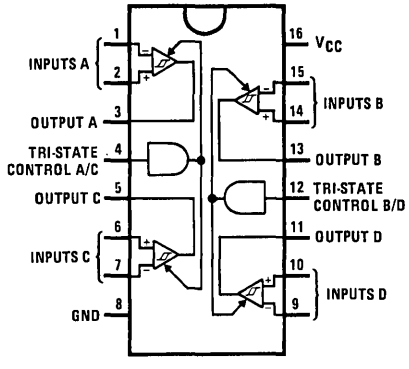
Dual-In-Line Package



TL/F/5779–2

Top View

Order Number DS3486J, DS3486M or DS3486N
See NS Package Number J16A, M16A or N16A

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Power Supply Voltage, V_{CC}	8V
Input Common-Mode Voltage, V_{ICM}	±25V
Input Differential Voltage, V_{ID}	±25V
TRI-STATE Control Input Voltage, V_I	8V
Output Sink Current, I_O	50 mA
Storage Temperature, T_{STG}	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1433mW
Molded Dip Package	1362 mW
SO Package	1002 mW

*Derate cavity package 9.6 mW/°C above 25°C; derate Dip molded package 10.2 mW/°C above 25°C. Derate SO package 8.01 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Power Supply Voltage, V_{CC}	4.75	5.25	V
Operating Temperature, T_A	0	70	°C
Input Common-Mode Voltage Range, V_{ICR}	−7.0	7.0	V

Electrical Characteristics

(Unless otherwise noted, minimum and maximum limits apply over recommended temperature and power supply voltage ranges. Typical values are for T_A = 25°C, V_{CC} = 5V and V_{IC} = 0V. See Note 2.)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	Input Voltage—High Logic State (TRI-STATE Control)		2.0			V
V_{IL}	Input Voltage—Low Logic State (TRI-STATE Control)				0.8	V
$V_{TH(D)}$	Differential Input Threshold Voltage	$-7V \le V_{IC} \le 7V$, V_{IH} TRI-STATE = 2V $I_O = -0.4$ mA, $V_{OH} \ge 2.7V$		0.070	0.2	V
		I_O = 8 mA, $V_{OL} \ge 0.5V$		0.070	−0.2	V
$I_{IB(D)}$	Input Bias Current	V_{CC} = 0V or 5.25V, Other Inputs at 0V				
		$V_I = -10V$			−3.25	mA
		$V_I = -3V$			−1.50	mA
		V_I = 3V			1.50	mA
		V_I = 10V			3.25	mA
	Input Balance	$-7V \le V_{IC} \le 7V$, $V_{IH(3C)}$ = 2V, (Note 4)				
	V_{OH}	$I_O = -0.4$ mA, V_{ID} = 0.4V	2.7			V
	V_{OL}	I_O = 8 mA, $V_{ID} = -0.4V$			0.5	V
I_{OZ}	Output TRI-STATE Leakage Current	$V_{I(D)}$ = 3V, V_{IL} = 0.8V, V_{OL} = 0.5V			−40	μA
		$V_{I(D)} = -3V$, V_{IL} = 0.8V, V_{OH} = 2.7V			40	μA
I_{OS}	Output Short-Circuit Current	$V_{I(D)}$ = 3V, V_{IH} TRI-STATE = 2V, V_O = 0V, (Note 3)	−15		−100	mA
I_{IL}	Input Current—Low Logic State (TRI-STATE Control)	V_{IL} = 0.5V			−100	μA
I_{IH}	Input Current—High Logic State (TRI-STATE Control)	V_{IH} = 2.7V			20	μA
		V_{IL} = 5.25V			100	μA
V_{IC}	Input Clamp Diode Voltage (TRI-STATE Control)	$I_{IN} = -10$ mA			−1.5	V
I_{CC}	Power Supply Current	All Inputs V_{IL} = 0V			85	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All currents into device pins are shown as positive, out of device pins are negative. All voltages referenced to ground unless otherwise noted.

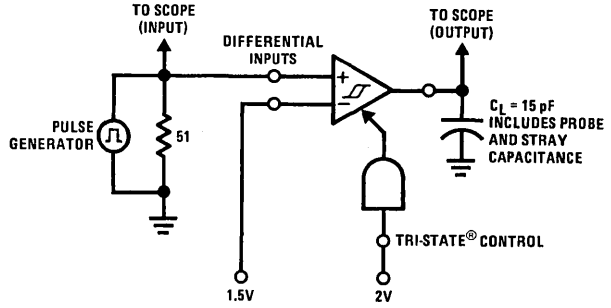
Note 3: Only one output at a time should be shorted.

Note 4: Refer to EIA RS-422/3 for exact conditions.

Switching Characteristics (Unless otherwise noted, V_{CC} = 5V and T_A = 25°C.)

Symbol	Parameter	Min	Typ	Max	Units
$t_{PHL(D)}$	Propagation Delay Time—Differential Inputs to Output Output High to Low		19	35	ns
$t_{PLH(D)}$	Output Low to High		19	30	ns
t_{PLZ}	TRI-STATE Control to Output Output Low to TRI-STATE		23	35	ns
t_{PHZ}	Output High to TRI-STATE		25	35	ns
t_{PZH}	Output TRI-STATE to High		18	30	ns
t_{PZL}	Output TRI-STATE to Low		20	30	ns

AC Test Circuits and Switching Time Waveforms



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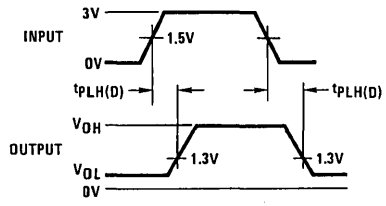

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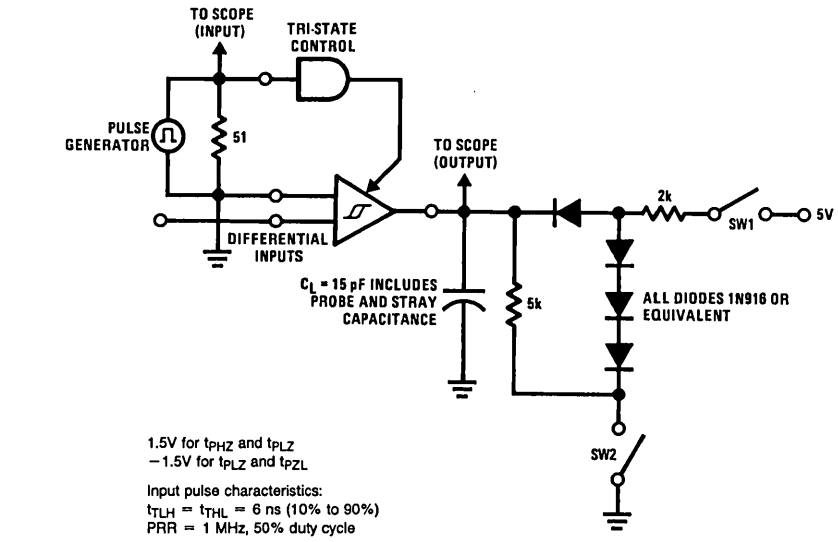
Input pulse characteristics:
$t_{TLH} = t_{THL}$ = 6 ns (10% to 90%)
PRR = 1 MHz, 50% duty cycle

FIGURE 1. Propagation Delay Differential Input to Output

AC Test and Switching Time Waveforms (Continued)



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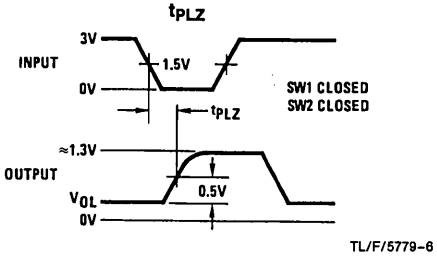

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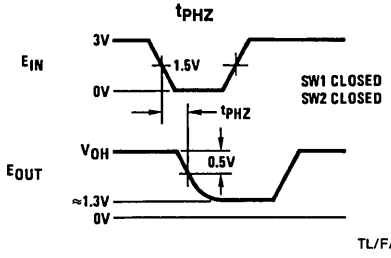

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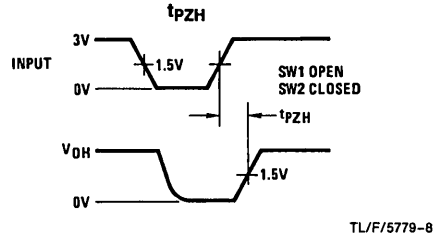

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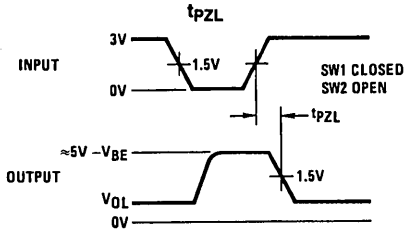


TL/F/5779–9

FIGURE 2. Propagation Delay TRI-STATE Control Input to Output

National Semiconductor Corporation

PRELIMINARY

DS34C86 Quad CMOS Differential Line Receiver

General Description

The DS34C86 is a quad differential line receiver designed to meet the RS-422, RS-423, and Federal Standards 1020 and 1030 for balanced and unbalanced digital data transmission, while retaining the low power characteristics of CMOS.

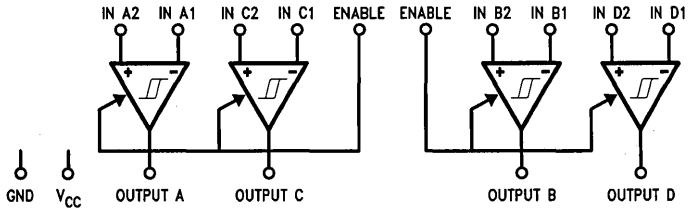
The DS34C86 has an input sensitivity of 200 mV over the common mode input voltage range of ±7V. Hysteresis is provided to improve noise margin and discourage output instability for slowly changing input waveforms.

Separate enable pins allow independent control of receiver pairs. The TRI-STATE® outputs have 6 mA source and sink capability. The DS34C86 is pin compatible with the DS3486.

Features

- Low power CMOS design
- ±0.2V sensitivity over the entire common mode range
- Typical propagation delays: 15 ns
- Typical input hysteresis: 50 mV
- Inputs won't load line when V_{CC} = 0V
- Meets the requirements of EIA standard RS-422
- TRI-STATE outputs for connection to system buses

Logic Diagram



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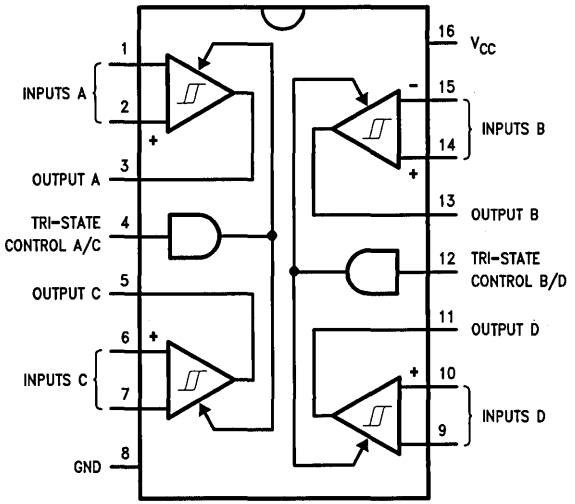
Connection Diagram

Dual-In-Line Package



TL/F/8699–2

Top View

Order Number DS34C86J, DS34C86M, and DS34C86N
See NS Package Number J16A, M16A and N16A

Absolute Maximum Ratings (Notes 1 & 2)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage (V_{CC})	7V
Common Mode Range (V_{CM})	±14V
Differential Input Voltage (V_{DIFF})	±14V
Enable Input Voltage (V_{IN})	7V
Storage Temperature Range (T_{STG})	−65°C to +150°C
Lead Temperature (Soldering 10 sec)	260°C

Operating Conditions

	Min	Max	Unit
Supply Voltage (V_{CC})	4.75	5.25	V
Operating Temperature Range (T_A)	−40	+85	°C
Enable Input Rise or Fall Times		500	ns

DC Electrical Characteristics V_{CC} = 5V ±5% (unless otherwise specified) (Note 3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{TH}	Minimum Differential Input Voltage	$V_{OUT} = V_{OH}$ or V_{OL}	−0.2		+0.2	V
R_{IN}	Input Resistance	−7V < V_{CM} < +7V (One Input AC GND)		10		kΩ
I_{IN}	Input Current (Under Test)	V_{IN} = +10V, Other Input = GND V_{IN} = −10V, Other Input = GND		+1.1 −1.6		mA mA
V_{OH}	Minimum High Level Output Voltage	V_{CC} = Min., $V_{(DIFF)}$ = +1V I_{OUT} = −6.0 mA	3.84	4.2		V
V_{OL}	Maximum Low Level Output Voltage	V_{CC} = Max., $V_{(DIFF)}$ = +1V I_{OUT} = 6.0 mA		0.2	0.33	V
V_{IH}	Minimum Enable High Input Level Voltage		2.0			V
V_{IL}	Maximum Enable Low Input Level Voltage				0.8	V
I_{OZ}	Maximum TRI-STATE Output Leakage Current	$V_{OUT} = V_{CC}$ or GND, TRI-STATE Control = V_{IL}		±0.5	±5.0	μA
I_I	Maximum Enable Input Current	$V_{IN} = V_{CC}$ or GND			±1.0	μA
I_{SC}	Output Short Circuit Current	V_{CC} = Max., $V_{(DIFF)}$ = +1V		65		mA
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max., $V_{(DIFF)}$ = +1V		12		mA
V_{HYST}	Input Hysteresis			50		mV

AC Electrical Characteristics V_{CC} = 5V ±5% (unless otherwise specified) (Note 3)

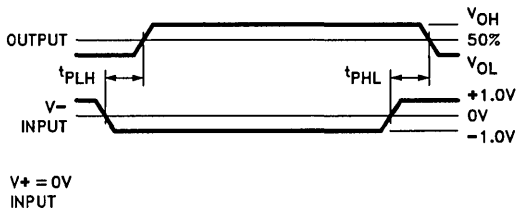
Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PLH}, t_{PHL}	Propagation Delay Input to Output	C_L = 50 pF		15		ns
t_{PLZ}, t_{PHZ}	Propagation Delay TRI-STATE Control to Output	C_L = 50 pF R_L = 1000Ω V_{DIFF} = 2.5V		12		ns
t_{PZL}, t_{PZH}	Propagation Delay TRI-STATE Control to Output	C_L = 50 pF R_L = 1000Ω V_{DIFF} = 2.5V		14		ns

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified, all voltages are referenced to ground.

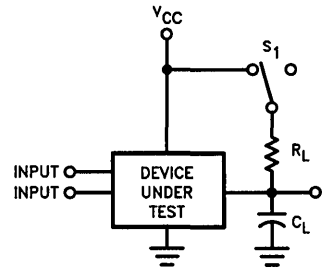
Note 3: Unless otherwise specified, Min/Max limits apply across the −40°C to +85°C temperature range.
All typicals are given for V_{CC} = 5V and T_A = 25°C.

Propagation Delay



TL/F/8699–3

Test Circuit for TRI-STATE Output Tests



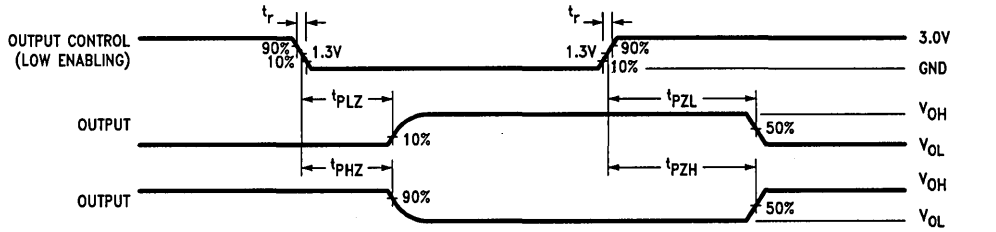
TL/F/8699–4

C_L Includes load and test jig capacitance.

S1 = V_{CC} for t_{PZL}, and t_{PLZ} measurements.

S1 = GND for t_{PZH}, and t_{PHZ} measurements.

TRI-STATE Output Enable and Disable Waveforms



TL/F/8699–5

National Semiconductor Corporation

DS3587/DS3487 Quad TRI-STATE® Line Driver

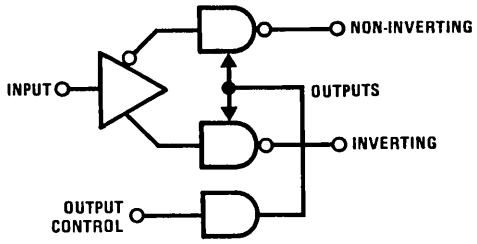
General Description

National's quad RS-422 driver featrues four independent driver chains which comply with EIA Standards for the electrical characteristics of balanced voltage digital interface circuits. The outputs are TRI-STATE structures which are forced to a high impedance state when the appropriate output control pin reaches a logic zero condition. All input pins are PNP buffered to minimize input loading for either logic one or logic zero inputs. In addition, internal circuitry assures a high impedance output state during the transition between power up and power down.

Features

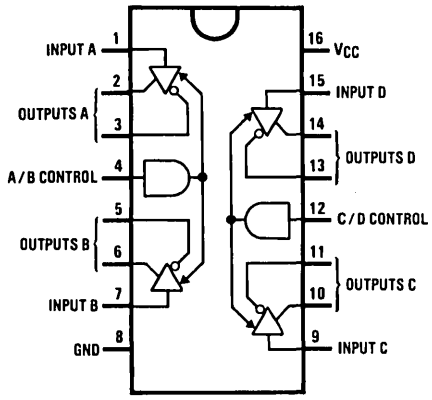
- Four independent driver chains
- TRI-STATE outputs
- PNP high impedance inputs (PIA compatible)
- Power up/down protection
- Fast propagation times (typ 10 ns)
- TTL compatible
- Single 5V supply voltage
- Output rise and fall times less than 20 ns (typ 10 ns)
- Pin compatible with DS8924 and MC3487
- Output skew—2 ns typ

Block and Connection Diagrams



TL/F/5780–1

Dual-In-Line Package



TL/F/5780–2

Top View

Order Number DS3587J, DS3487J, DS3487M or DS3487N
See NS Package Number J16A, M16A or N16A

Truth Table

Input	Control Input	Non-Inverter Output	Inverter Output
H	H	H	L
L	H	L	H
X	L	Z	Z

L = Low logic state
H = High logic state
X = Irrelevant
Z = TRI-STATE (high impedance)

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	8V
Input Voltage	5.5V
Storage Temperature	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1509 mW
Molded DIP Package	1476 mW
Lead Temperature (Soldering, 4 seconds)	260°C
SO Package	1051 mW

*Derate cavity package 10.1 mW/°C above 25°C; derate DIP molded package 11.9 mW/°C above 25°C. Derate SO package 8.41 mW/°C above 25°C

Operating Conditions

	Min	Max	Units
Supply Voltage, V_{CC}			
DS3587	4.5	5.5	V
DS3487	4.75	5.25	V
Temperature (T_A)			
DS3587	−55	+125	°C
DS3487	0	+70	°C

Electrical Characteristics (Notes 2, 3, 4 and 5)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IL}	Input Low Voltage					0.8	V
V_{IH}	Input High Voltage			2.0			V
I_{IL}	Input Low Current	V_{IL} = 0.5V				−200	μA
I_{IH}	Input High Current		V_{IH} = 2.7V			50	μA
			V_{IH} = 5.5V			100	μA
V_{CL}	Input Clamp Voltage	I_{CL} = −18 mA				−1.5	V
V_{OL}	Output Low Voltage	I_{OL} = 48 mA				0.5	V
V_{OH}	Output High Voltage	I_{OH} = −20 mA		2.5			V
I_{OS}	Output Short-Circuit Current			−40		−140	mA
I_{OZ}	Output Leakage Current (TRI-STATE)		V_O = 0.5V			−100	μA
			V_O = 5.5V			100	μA
I_{OFF}	Output Leakage Current Power OFF	V_{CC} = 0	V_O = 6V			100	μA
			V_O = −0.25V			−100	μA
$\|V_{OS}-\overline{V}_{OS}\|$	Difference in Output Offset Voltage					0.4	V
V_T	Differential Output Voltage			2.0			V
$\|V_T\|-\|\overline{V}_T\|$	Difference in Differential Output Voltage					0.4	V
I_{CC}	Power Supply Current		Active		50	80	mA
			TRI-STATE		35	60	mA

Switching Characteristics V_{CC} = 5V, T_A = 25°C

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHL}	Input to Output			10	15	ns
t_{PLH}	Input to Output			10	15	ns
t_{THL}	Differential Fall Time			10	15	ns
t_{TLH}	Differential Rise Time			10	15	ns
t_{PHZ}	Enable to Output	R_L = 200Ω, C_L = 50 pF		17	25	ns
t_{PLZ}	Enable to Output	R_L = 200Ω, C_L = 50 pF		15	25	ns
t_{PZH}	Enable to Output	R_L = ∞, C_L = 50 pF, S1 Open		11	25	ns
t_{PZL}	Enable to Output	R_L = 200Ω, C_L = 50 pF, S2 Open		15	25	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

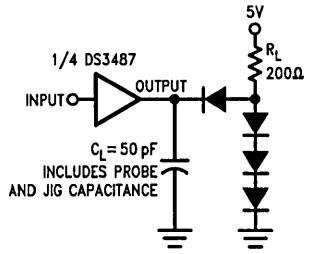
Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C range for the DS3487. All typicals are given for V_{CC} = 5V and T_A = 25°C.

Note 3: All currents into device pins are positive, all currents out of device pins as negative. All voltages are referenced to ground unless otherwise specified.

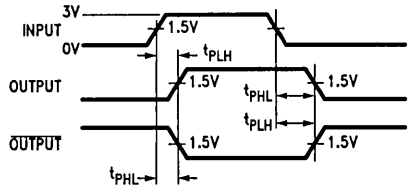
Note 4: Only one output at a time should be shorted.

Note 5: Symbols and definitions correspond to EIA RS-422, where applicable.

AC Test Circuits and Switching Time Waveforms



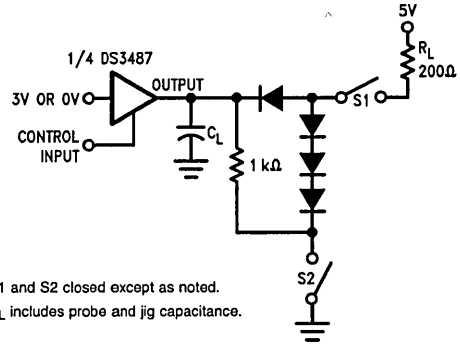
TL/F/5780–3



TL/F/5780–4

Input pulse: f = MHz, 50%; $t_r = t_f \leq 15$ ns.

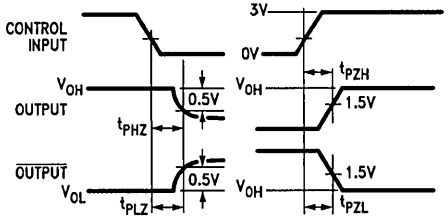
FIGURE 1. Propagation Delays



S1 and S2 closed except as noted.

C_L includes probe and jig capacitance.

TL/F/5780–5



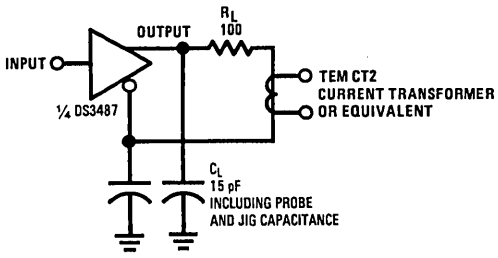
TL/F/5780–6

Input pulse: f = MHz, 50%; $t_r = t_f \leq 15$ ns.

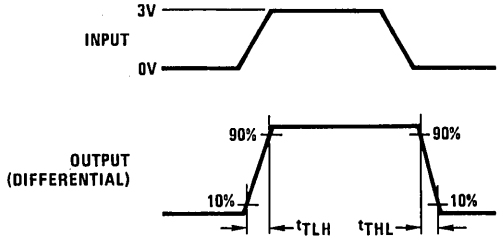
S1 = open for t_{PZH}

S2 = open for t_{PZL}

FIGURE 2. TRI-STATE Enable and Disable Delays



TL/F/5780–7



TL/F/5780–8

Input pulse: f = MHz, 50%; $t_r = t_f \leq 15$ ns.

FIGURE 3. Differential Rise and Fall Times

National Semiconductor Corporation

PRELIMINARY

DS34C87 CMOS Quad TRI-STATE® Differential Line Driver

General Description

The DS34C87 is a quad differential line driver designed for digital data transmission over balanced lines. The DS34C87 meets all the requirements of EIA standard RS-422 while retaining the low power characteristics of CMOS. This enables the construction of serial and terminal interfaces while maintaining minimal power consumption.

The DS34C87 accepts TTL or CMOS input levels and translates these to RS-422 output levels. This part uses special output circuitry that enables the individual drivers to power down without loading down the bus. The DS34C87 also includes special power up and down circuitry which will TRI-STATE the outputs during power up or down, preventing spurious glitches on its outputs. This device has separate enable circuitry for each pair of the four drivers. The DS34C87 is pin compatible to the DS3487.

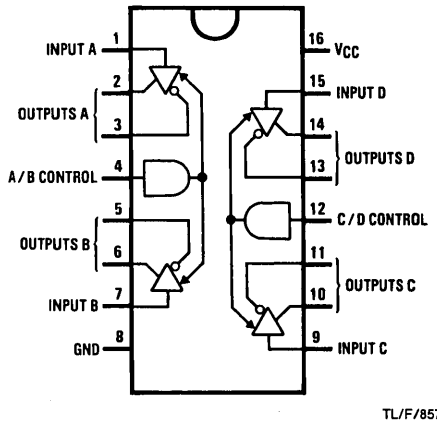
All inputs are protected against damage due to electrostatic discharge by diodes to V_{CC} and ground.

Features

- TTL input compatible
- Typical propagation delays: 10 ns
- Typical output skew: 0.5 ns
- Outputs won't load line when V_{CC} = 0V
- Meets the requirements of EIA standard RS-422
- Operation from single 5V supply
- TRI-STATE outputs for connection to system buses
- Low quiescent current

Connection and Logic Diagrams

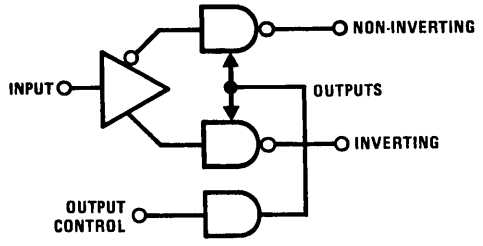
Dual-In-Line Package



TL/F/8576–1

Top View

Order Number DS34C87J, DS34C87N or DS34C87M
See NS Package Number J16A, M16A or N16A



TL/F/8576–2

Truth Table

Input	Control Input	Non-Inverting Output	Inverting Output
H	H	H	L
L	H	L	H
X	L	Z	Z

L = Low logic state X = Irrelevant
H = High logic state Z = TRI-STATE (high impedance)

Absolute Maximum Ratings (Notes 1 & 2)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage (V_{CC})	−0.5 to 7.0V
DC Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±140 mA
DC V_{CC} or GND Current (I_{CC})	±140 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (Note 3) (P_D)	500 mW
Lead Temperature (T_L) (Soldering 4 sec)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltqge (V_{CC})	4.75	5.25	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temperature Range (T_A)	−40	+85	°C
Input Rise or Fall Times (t_r, t_f)		500	ns

DC Electrical Characteristics V_{CC} = 5V ±5% (unless otherwise specified) (Note 4)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IH}	High Level Input Voltage			2.0			V
V_{IL}	Low Level Input Voltage					0.8	V
V_{OH}	High Level Output Voltage	V_{IN} = V_{IH} or V_{IL}, I_{OUT} = −20 mA		2.5			V
V_{OL}	Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL}, I_{OUT} = 48 mA				0.5	V
V_T	Differential Output Voltage	R_L = 100 Ω (Note 5)		2.0			V
$\lvert V_T\rvert-\lvert\overline{V}_T\rvert$	Difference In Differential Output	R_L = 100 Ω (Note 5)				0.4	V
V_{OS}	Common Mode Output Voltage	R_L = 100 Ω (Note 5)				3.0	V
$\lvert V_{OS}-\overline{V}_{OS}\rvert$	Difference In Common Mode Output	R_L = 100 Ω (Note 5)				0.4	V
I_{IN}	Input Current	V_{IN} = V_{CC}, GND, V_{IH}, or V_{IL}				±1.0	μA
I_{CC}	Quiescent Supply Current	I_{OUT} = 0 μA, V_{IN} = V_{CC} or GND V_{IN} = 2.4V or 0.5V (Note 6)			200 0.8		μA mA
I_{OZ}	TRI-STATE Output Leakage Current	V_{OUT} = V_{CC} or GND Control = V_{IL}			±0.5	±5.0	μA
I_{SC}	Output Short Circuit Current	V_{IN} = V_{CC} or GND (Note 7)		−40		−140	mA
I_{OFF}	Output Leakage Current Power Off	V_{CC} = 0	V_{OUT} = 6V V_{OUT} = −0.25V			100 −100	μA μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified, all voltages are referenced to ground. All currents into device pins are positive; all currents out of device pins are negative.

Note 3: Power Dissipation temperature derating—plastic "N" package: −12 mW/°C from 65°C to 85°C.
ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: Unless otherwise specified, min/max limits apply across the −40°C to 85°C temperature range. All typicals are given for V_{CC} = 5V and T_A = 25°C.

Note 5: See EIA Specification RS-422 for exact test conditions.

Note 6: Measured per input. All other inputs at V_{CC} or GND.

Note 7: Only one output at a time should be shorted.

Switching Characteristics V_{CC} = 5V ±5%, $t_r = t_f$ = 6 ns (*Figures 1, 2, 3,* and *4*) (Note 4)

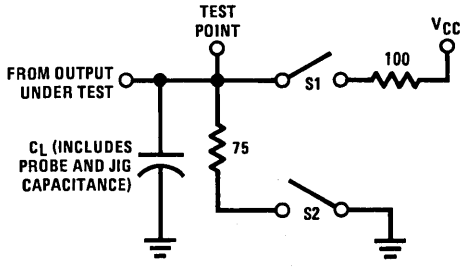
Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PLH}, t_{PHL}	Propagation Delay Input to Output	C_L = 50 pF		8		ns
Skew	(Note 8)	C_L = 50 pF		0.5		ns
t_{TLH}, t_{THL}	Differential Output Rise And Fall Times	C_L = 50 pF		4		ns
t_{PZH}	Output Enable Time	C_L = 50 pF S1 Open		13		ns
t_{PZL}	Output Enable Time	C_L = 50 pF S2 Open		15		ns
t_{PHZ}	Output Disable Time (Note 9)	C_L = 50 pF S1 Open		9		ns
t_{PLZ}	Output Disable Time (Note 9)	C_L = 50 pF S2 Open		10		ns
C_{PD}	Power Dissipation Capacitance (Note 10)			100		pF
C_{IN}	Input Capacitance			10		pF

Note 8: Skew is defined as the difference in propagation delays between complementary outputs at the 50% point.

Note 9: Output disable time is the delay from ENABLE or $\overline{\text{ENABLE}}$ being switched to the output transistors turning off. The actual disable times are less than indicated due to the delay added by the RC time constant of the load. The added delay is typically 1 ns for t_{PLZ} and 0.6 ns for t_{PHZ}.

Note 10: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

AC Test Circuit and Switching Time Waveforms

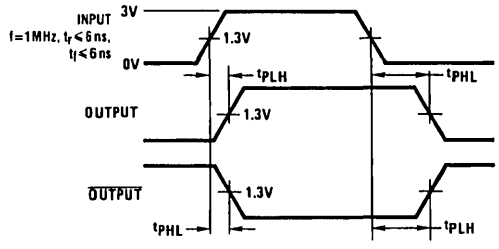


TL/F/8576–3

Note S1 and S2 of load circuit are closed except where shown.

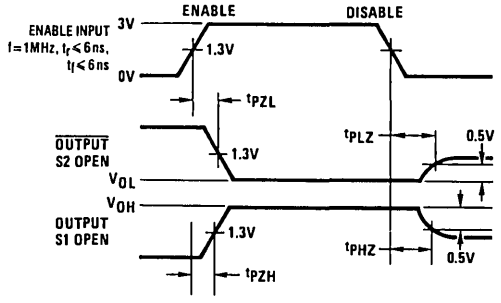
FIGURE 1. AC Test Circuit

AC Test Circuit and Switching Time Waveforms (Continued)



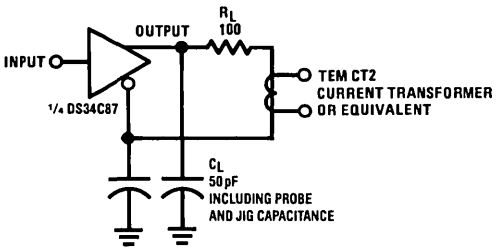
TL/F/8576-4

FIGURE 2. Propagation Delays

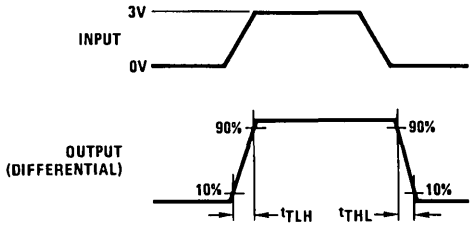


TL/F/8576-5

FIGURE 3. Enable and Disable Times



TL/F/8576-6



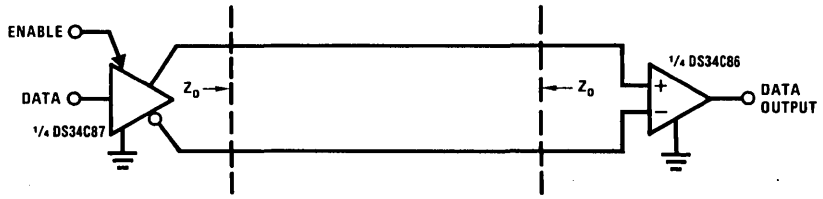
Input pulse; $f = 1$MHz, 50%; $t_r = t_f \leq 6$ns.

TL/F/8576-7

FIGURE 4. Differential Rise and Fall Times

Typical Applications

Two-Wire Balanced System, RS-422



TL/F/8576-8

National Semiconductor Corporation

DS1603/DS3603/DS55107/DS55108/DS75107/DS75108/ DS75208 Dual Line Receivers

General Description

The seven products described herein are TTL compatible dual high speed circuits intended for sensing in a broad range of system applications. While the primary usage will be for line receivers of MOS sensing, any of the products may effectively be used as voltage comparators, level translators, window detectors, transducer preamplifiers, and in other sensing applications. As digital line receivers the products are applicable with the SN55109/SN75109 and SN55110/SN75110 companion drivers, or may be used in other balanced or unbalanced party-line data transmission systems. The improved input sensitivity and delay specifications of the DS75208 make it ideal for sensing high performance MOS memories as well as high sensitivity line receivers and voltage comparators. TRI-STATE® products enhance bused organizations.

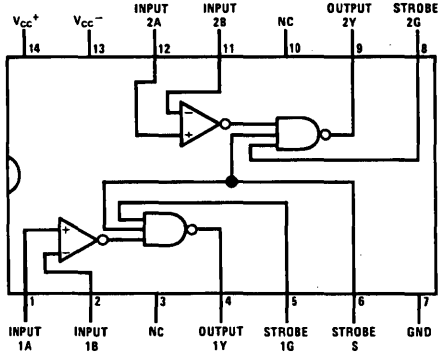
Input protection diodes are incorporated in series with the collectors of the differential input stage. These diodes are useful in certain applications that have multiple $V_{CC}+$ supplies or $V_{CC}+$ supplies that are turned off.

Features

- Diode protected input stage for power "OFF" condition
- 17 ns typ high speed
- TTL compatible
- ±10 mV or ±25 mV input sensitivity
- ±3V input common-mode range
- High input impedance with normal V_{CC}, or V_{CC} = 0V
- Strobes for channel selection
- TRI-STATE outputs for high speed buses
- Dual circuits
- Sensitivity gntd. over full common-mode range
- Logic input clamp diodes—meets both "A" and "B" version specifications
- ±5V standard supply voltages

Connection Diagrams

Dual-In-Line Package

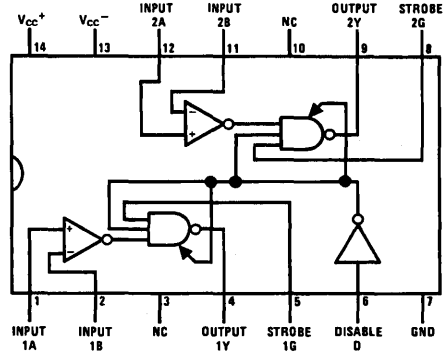


TL/F/5781–1

Top View

Order Number DS55107J, DS75107J, DS55108J, DS75108J, DS75208J, DS75107N, DS75108N or DS75208N
See NS Package Number J14A or N14A

Dual-In-Line Package



TL/F/5781–2

Top View

Order Number DS1603J, DS3603J or DS3603N
See NS Package Number J14A or N14A

Selection Guide

Temperature → / Package →	$-55°C \le T_A \le +125°C$ Cavity Dip	$0°C \le T_A \le +70°C$ Cavity or Molded Dip	
Input Sensitivity → / Output Logic ↓	±25 mV	±25 mV	±10 mV
TTL Active Pull-Up	DS55107	DS75107	
TTL Open Collector	DS55108	DS75108	DS75208
TTL TRI-STATE	DS1603	DS3603	

Absolute Maximum Ratings (Notes 1, 2 and 3)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage, V_{CC}^+	7V
Supply Voltage, V_{CC}^-	−7V
Differential Input Voltage	±6V
Common Mode Input Voltage	±5V
Strobe Input Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1308 mW
Molded Package	1207 mW
Lead Temperature (Soldering, 4 sec)	260°C

*Derate cavity package 8.7 mW/°C above 25°C; derate molded package 9.7 mW/°C above 25°C.

Operating Conditions

	DS55107 DS55108, DS1603			DS75107, DS75108, DS75208 DS3603		
	Min	**Nom**	**Max**	**Min**	**Nom**	**Max**
Supply Voltage V_{CC}^+	4.5V	5V	5.5V	4.75V	5V	5.25V
Supply Voltage V_{CC}^-	−4.5V	−5V	−5.5V	−4.75V	−5V	−5.25V
Operating Temperature Range	−55°C	to	+125°C	0°C	to	+70°C

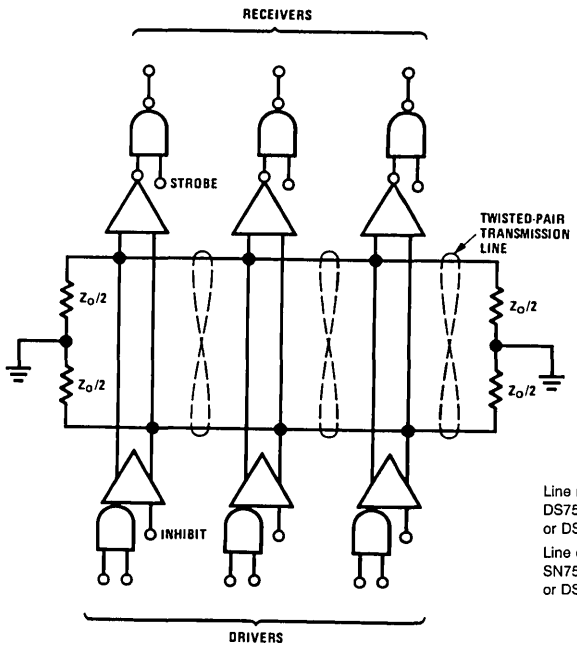
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2. Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS1603, DS55107 and DS55108 and across the 0°C to +70°C range for the DS3603, DS75107, DS75108. All typical values are for T_A = 25°C and V_{CC} = 5V.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Typical Applications

Line Receiver Used in a Party-Line or Data-Bus System



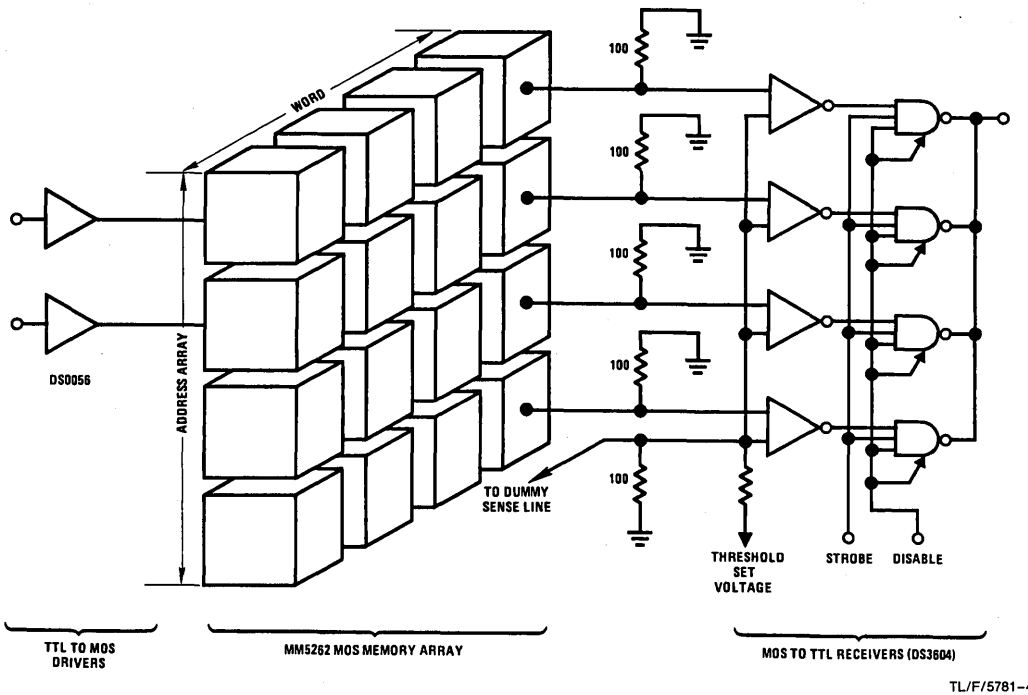
Line receivers are DS75107/DS75108 or DS3603

Line drivers are SN75109/SN75110 or DS8831

TL/F/5781–3

Typical Applications (Continued)

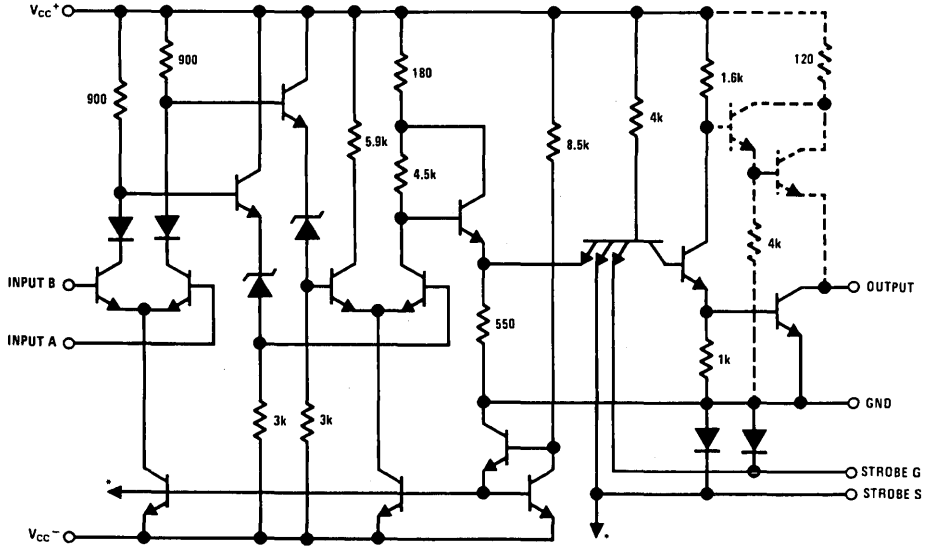
Line Receiver Used in MOS Memory System



TL/F/5781–4

Schematic Diagrams

DS55107/DS75107, DS55108/DS75108, DS75208



TL/F/5781–5

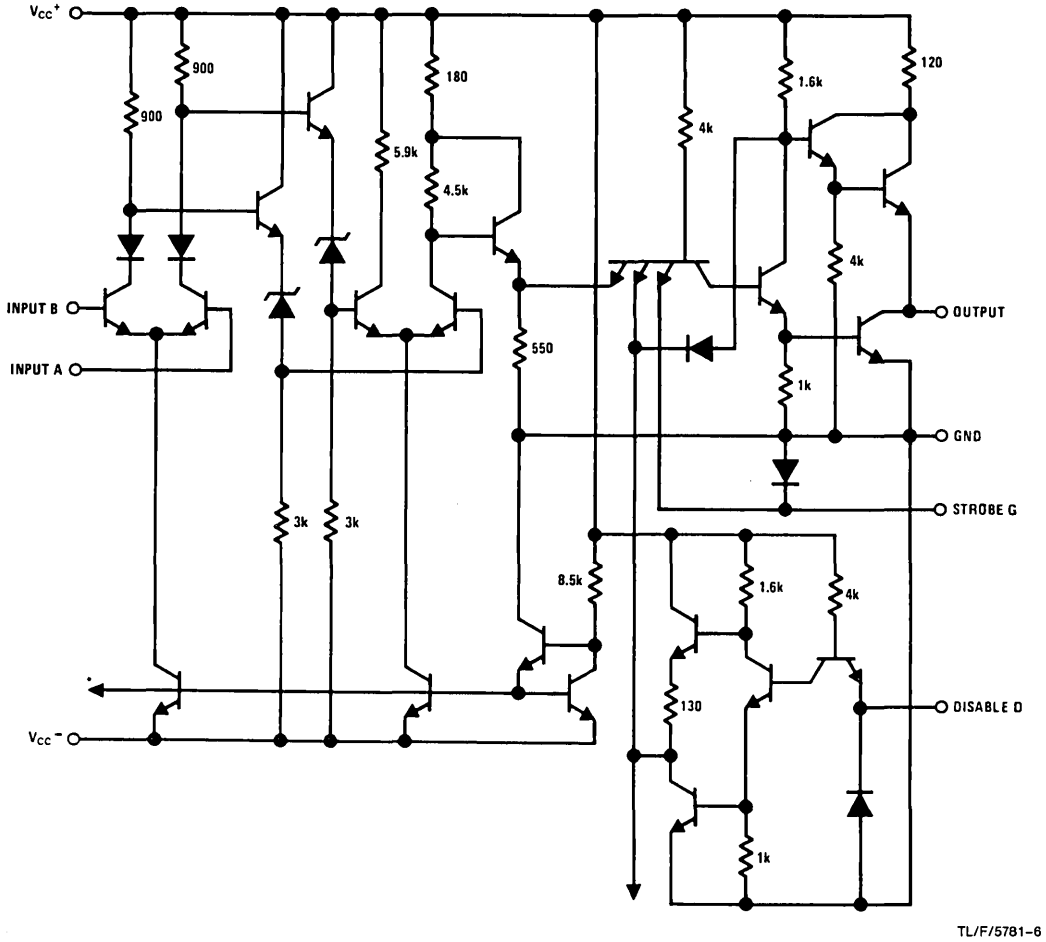
Note 1: ½ of the dual circuit is shown.

Note 2: *Inidcates connections common to second half of dual circuit.

Note 3: Components shown with dash lines are applicable to the DS55107, DS75207 and DS75107 only.

Schematic Diagrams (Continued)

DS1603/DS3603



TL/F/5781–6

Note 1: ½ of the dual circuit is shown.

Note 2: *Indicates connections common to second half of dual circuit.

DS55107/DS75107, DS55108/DS75108

Electrical Characteristics ($T_{MIN} \le T_A \le T_{MAX}$)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
I_{IH}	High Level Input Current Into A1, B1, A2 or B2	V_{CC+} = Max, V_{CC-} = Max, V_{ID} = 0.5V, V_{IC} = −3V to 3V			30	75	μA
I_{IL}	Low Level Input Current Into A1, B1, A2 or B2	V_{CC+} = Max, V_{CC-} = Max, V_{ID} = −2V, V_{IC} = −3V to 3V				−10	μA
I_{IH}	High Level Input Current Into G1 or G2	V_{CC+} = Max, V_{CC-} = Max	$V_{IH(S)}$ = 2.4V			40	mA
			$V_{IH(S)}$ Max V_{CC+}			1	mA
I_{IL}	Low Level Input Current Into G1 or G2	V_{CC+} = Max, V_{CC-} = Max, $V_{IL(S)}$ = 0.4V				−1.6	mA
I_{IH}	High Level Input Current Into S	V_{CC+} = Max, V_{CC-} = Max	$V_{IH(S)}$ = 2.4V			80	μA
			$V_{IH(S)}$ = Max V_{CC+}			2	mA
I_{IL}	Low Level Input Current Into S	V_{CC+} = Max, V_{CC-} = Max, $V_{IL(S)}$ = 0.4V				−3.2	mA
V_{OH}	High Level Output Voltage	V_{CC+} = Min, V_{CC-} = Min, I_{LOAD} = −400 μA, V_{ID} = 25 mV, V_{IC} = −3V to 3V, (Note 3)		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC+} = Min, V_{CC-} = Min, I_{SINK} = 16 mA, V_{ID} = −25 mV, V_{IC} = −3V to 3V				0.4	V
I_{OH}	High Level Output Current	V_{CC+} = Min, V_{CC-} = Min V_{OH} = Max V_{CC+}, (Note 4)				250	μA
I_{OS}	Short Circuit Output Current	V_{CC+} = Max, V_{CC-} = Max, (Notes 2 and 3)		−18		−70	mA
I_{CCH+}	High Logic Level Supply Current From V_{CC}	V_{CC+} = Max, V_{CC-} = Max, V_{ID} = 25 mV, T_A = 25°C			18	30	mA
I_{CCH-}	High Logic Level Supply Current From V_{CC}	V_{CC+} = Max, V_{CC-} = Max, V_{ID} = 25 mV, T_A = 25°C			−8.4	−15	mA
V_I	Input Clamp Voltage on G or S	V_{CC+} = Min, V_{CC-} = Min, I_{IN} = −12 mA, T_A = 25°C			−1	−1.5	V

Switching Characteristics (V_{CC+} = 5V, V_{CC-} = −5V, T_A = 25°C)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
$t_{PLH(D)}$	Propagation Delay Time, Low to High Level, From Differential Inputs A and B to Output	R_L = 390Ω, C_L = 50 pF, (Note 1)	(Note 3)		17	25	ns
			(Note 4)		19	25	ns
$t_{PHL(D)}$	Propagation Delay Time, High to Low Level, From Differential Inputs A and B to Output	R_L = 390Ω, C_L = 50 pF, (Note 1)	(Note 3)		17	25	ns
			(Note 4)		19	25	ns
$t_{PLH(S)}$	Propagation Delay Time, Low to High Level, From Strobe Input G or S to Output	R_L = 390Ω, C_L = 50 pF	(Note 3)		10	15	ns
			(Note 4)		13	20	ns
$t_{PHL(S)}$	Propagation Delay Time, High to Low Level, From Strobe Input G or S to Output	R_L = 390Ω, C_L = 50 pF	(Note 3)		8	15	ns
			(Note 4)		13	20	ns

Note 1: Differential input is +100 mV to −100 mV pulse. Delays read from 0 mV on input to 1.5V on output.

Note 2: Only one output at a time should be shorted.

Note 3: DS55107/DS75107 only.

Note 4: DS55108/DS75108 only.

DS75208

Electrical Characteristics ($0°C \le T_A \le +70°C$)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
I_{IH}	High Level Input Current Into A1, B1, A2 or B2	V_{CC+} = Max, V_{CC-} = Max, V_{ID} = 0.5V, V_{IC} = −3V to 3V			30	75	μA
I_{IL}	Low Level Input Current Into A1, B1, A2 or B2	V_{CC+} = Max, V_{CC-} = Max, V_{ID} = −2V, V_{IC} = −3V to 3V				−10	μA
I_{IH}	High Level Input Current Into G1 or G2	V_{CC+} = Max, V_{CC-} = Max	$V_{IH(S)}$ = 2.4V			40	μA
			$V_{IH(S)}$ = Max V_{CC+}			1	mA
I_{IL}	Low Level Input Current Into G1 or G2	V_{CC+} = Max, V_{CC-} = Max, $V_{IL(S)}$ = 0.4V				−1.6	mA
I_{IH}	High Level Input Current Into S	V_{CC+} = Max, V_{CC-} = Max	$V_{IH(S)}$ = 2.4V			80	μA
			$V_{IH(S)}$ = Max V_{CC+}			2	mA
I_{IL}	Low Level Input Current Into S	V_{CC+} = Max, V_{CC-} = Max, $V_{IL(S)}$ = 0.4V				−3.2	mA
V_{OL}	Low Level Output Voltage	V_{CC+} = Min, V_{CC-} = Min, I_{SINK} = 16 mA, V_{ID} = −10 mV, V_{IC} = −3V to 3V				0.4	V
I_{OH}	High Level Output Current	V_{CC+} = Min, V_{CC-} = Min, V_{OH} = Max V_{CC+}				250	μA
I_{CCH+}	High Logic Level Supply Current From V_{CC+}	V_{CC+} = Max, V_{CC-} = Max, V_{ID} = 10 mV, T_A = 25°C			18	30	mA
I_{CCH-}	High Logic Level Supply Current From V_{CC-}	V_{CC+} = Max, V_{CC-} = Max, V_{ID} = 10 mV, T_A = 25°C			−8.4	−15	mA
V_I	Input Clamp Voltage on G or S	V_{CC+} = Min, V_{CC-} = Min, I_{IN} = −12 mA, T_A = 25°C			−1	−1.5	V

Switching Characteristics (V_{CC+} = 5V, V_{CC-} = −5V, T_A = 25°C)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$t_{PLH(D)}$	Propagation Delay Time, Low-to-High Level, From Differential Inputs A and B to Output	R_L = 470Ω, C_L = 15 pF, (Note 1)			35	ns
$t_{PHL(D)}$	Propagation Delay Time, High-to-Low Level, From Differential Inputs A and B to Output	R_L = 470Ω, C_L = 15 pF, (Note 1)			20	ns
$t_{PLH(S)}$	Propagation Delay Time, Low-to-High Level, From Strobe Input G or S to Output	R_L = 470Ω, C_L = 15 pF			17	ns
$t_{PHL(S)}$	Propagation Delay Time, High-to-Low Level, From Strobe Input G or S to Output	R_L = 470Ω, C_L = 15 pF			17	ns

Note 1: Differential input is +10 mV to −30 mV pulse. Delays read from 0 mV on input to 1.5V on output.

DS1603/DS3603

Electrical Characteristics ($T_{MIN} \le T_A \le T_{MAX}$)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
I_{IH}	High Level Input Current Into A1, B1, A2 or B2	V_{CC+} = Max, V_{CC-} = Max, V_{ID} = 0.5V, V_{IC} = −3V to 3V			30	75	μA
I_{IL}	Low Level Input Current Into A1, B1, A2 or B2	V_{CC+} = Max, V_{CC-} = Max, V_{ID} = −2V, V_{IC} = −3V to 3V				−10	μA
I_{IH}	High Level Input Current Into G1, G2 or D	V_{CC+} = Max, V_{CC-} = Max	$V_{IH(S)}$ = 2.4V			40	μA
			$V_{IH(S)}$ = Max V_{CC+}			1	mA
I_{IL}	Low Level Input Current Into D	V_{CC+} = Max, V_{CC-} = Max, $V_{IL(D)}$ = 0.4V				−1.6	mA
I_{IL}	Low Level Input Current Into G1 or G2	V_{CC+} = Max, V_{CC-} = Max, $V_{IL(G)}$ = 0.4V	$V_{IH(D)}$ = 2V			−40	μA
			$V_{IL(D)}$ = 0.8V			−1.6	mA
V_{OH}	High Level Output Voltage	V_{CC+} = Min, V_{CC-} = Min, I_{LOAD} = −2 mA, V_{ID} = 25 mV, $V_{IL(D)}$ = 0.8V, V_{IC} = −3V to 3V		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC+} = Min, V_{CC-} = Min, I_{SINK} = 16 mA, V_{ID} = −25 mV, $V_{IL(D)}$ = 0.8V, V_{IC} = −3V to 3V				0.4	V
I_{OD}	Output Disable Current	V_{CC+} = Max, V_{CC-} = Max, $V_{IH(D)}$ = 2V	V_{OUT} = 2.4V			40	μA
			V_{OUT} = 0.4V			−40	μA
I_{OS}	Short Circuit Output Current	V_{CC+} = Max, $V_{IL(D)}$ = 0.8V, V_{CC-} = Max, (Note 2)		−18		−70	mA
I_{CCH+}	High Logic Level Supply Current From V_{CC+}	V_{CC+} = Max, V_{CC-} = Max, V_{ID} = 25 mV, T_A = 25°C			28	40	mA
I_{CCH-}	High Logic Level Supply Current From V_{CC-}	V_{CC+} = Max, V_{CC-} = Max, V_{ID} = 25 mV, T_A = 25°C			−8.4	−15	mA
V_I	Input Clamp Voltage on G or D	V_{CC+} = Min, V_{CC-} = Min, I_{IN} = −12 mA, T_A = 25°C			−1	−1.5	V

Switching Characteristics (V_{CC+} = 5V, V_{CC-} = −5V, T_A = 25°C)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$t_{PLH(D)}$	Propagation Delay Time, Low-to-High Level, From Differential Inputs A and B to Output	R_L = 390Ω, C_L = 50 pF, (Note 1)		17	25	ns
$t_{PHL(D)}$	Propagation Delay Time, High-to-Low Level, From Differential Inputs A and B to Output	R_L = 390Ω, C_L = 50 pF, (Note 1)		17	25	ns
$t_{PLH(S)}$	Propagation Delay Time, Low-to-High Level, From Strobe Input G to Output	R_L = 390Ω, C_L = 50 pF		10	15	ns
$t_{PHL(S)}$	Propagation Delay Time, High-to-Low Level, From Strobe Input G to Output	R_L = 390Ω, C_L = 50 pF		8	15	ns

Switching Characteristics (V_{CC+} = 5V, V_{CC-} = −5V, T_A = 25°C) (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{1H}	Disable Low-to-High to Output High to Off	R_L = 390Ω, C_L = 5 pF			20	ns
t_{0H}	Disable Low-to-High to Output Low to Off	R_L = 390Ω, C_L = 5 pF			30	ns
t_{H1}	Disable High-to-Low Output Off to High	R_L = 1k to 0V, C_L = 50 pF			25	ns
t_{H0}	Disable High-to-Low to Output Off to Low	R_L = 390Ω, C_L = 50 PF			25	ns

Note 1: Differential input is +100 mV to −100 mV pulse. Delays read from 0 mV on input to 1.5V on output.

Note 2: Only one output at a time should be shorted.

National Semiconductor Corporation

DS1650/DS1652/DS3650/DS3652 Quad Differential Line Receivers

General Description

The DS1650/DS3650 and DS1652/DS3652 are TTL compatible quad high speed circuits intended primarily for line receiver applications. Switching speeds have been enhanced over conventional line receivers by the use of Schottky technology, and TRI-STATE® strobing is incorporated offering a high impedance output state for bussed organizations.

The DS1650/DS3650 has active pull-up outputs and offers a TRI-STATE strobe, while the DS1652/DS3652 offers open collector outputs providing implied "AND" operation.

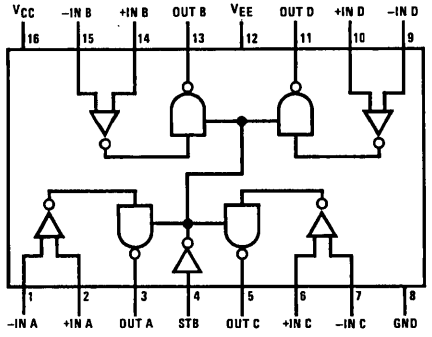
The DS1652/DS3652 can be used for address decoding as illustrated below. All outputs of the DS1652/DS3652 are tied together through a common resistor to 5V. In this configuration, the DS1652/DS3652 provides the "AND" function. All addresses have to be true before the output will go high. This scheme eliminates the need for an "AND" gate and enhances speed throughput for address decoding.

Features

- High speed
- TTL compatible
- Input sensitivity ±25 mV
- TRI-STATE outputs for high speed busses
- Standard supply voltages ±5V
- Pin and function compatible with MC3450 and MC3452

Connection Diagram

Dual-In-Line Package



Top View TL/F/5782-1

Order Number DS1650J, DS1652J, DS3650J, DS3652J, DS3650M, DS3652M, DS3650N or DS3652N
See NS Package Number J16A, M16A, or N16A

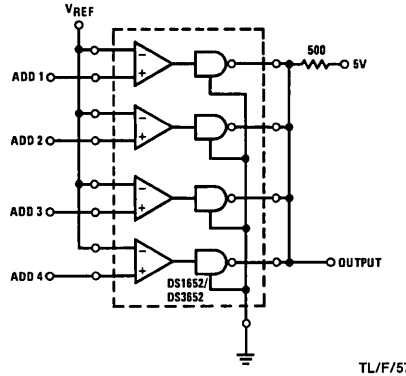
Truth Table

Input	Strobe	Output	
		DS1650/ DS3650	DS1652/ DS3652
$V_D \geq 25$ mV	L	H	Open
	H	Open	Open
-25 mV $\leq V_{ID} \leq 25$ mV	L	X	X
	H	Open	Open
$V_{ID} \leq -25$ mV	L	L	L
	H	Open	Open

L = Low Logic State Open = TRI-STATE
H = High Logic State X = Indeterminate State

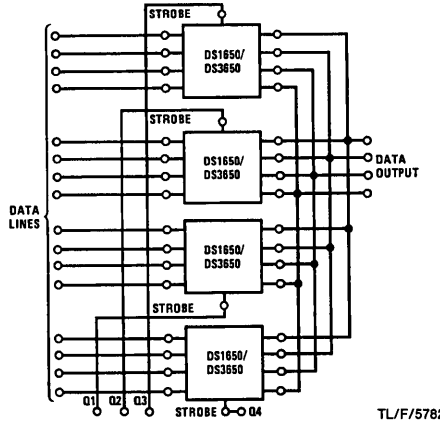
Typical Applications

Implied "AND" Gating



TL/F/5782-2

Wired "OR" Data Selecting Using TRI-STATE Logic



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Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Power Supply Voltages	
V_{CC}	+7.0 V_{DC}
V_{EE}	−7.0 V_{DC}
Differential-Mode Input Signal Voltage Range, V_{IDR}	±6.0 V_{DC}
Common-Mode Input Voltage Range, V_{ICR}	±5.0 V_{DC}
Strobe Input Voltage, $V_{I(S)}$	5.5 V_{DC}
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 4 seconds)	260°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1509 mW
Molded DIP Package	1476 mW
SO Package	1051 mW

*Derate cavity package 10.1 mW/°C above 25°C; derate molded DIP package 11.8 mW/°C above 25°C; derate SO package 8.41 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage, V_{CC}			
DS1650, DS1652	4.5	5.5	V_{DC}
DS3650, DS3652	4.75	5.25	V_{DC}
Supply Voltage, V_{EE}			
DS1650, DS1652	−4.5	−5.5	V_{DC}
DS3650, DS3652	−4.75	−5.25	V_{DC}
Operating Temperature, T_A			
DS1650, DS1652	−55	+125	°C
DS3650, DS3652	0	+70	°C
Output Load Current, I_{OL}		16	mA
Differential-Mode Input Voltage Range, V_{IDR}	−5.0	+5.0	V_{DC}
Common-Mode Input Voltage Range, V_{ICR}	−3.0	+3.0	V_{DC}
Input Voltage Range (Any Input to GND), V_{IR}	−5.0	+3.0	V_{DC}

Electrical Characteristics

(V_{CC} = 5.0 V_{DC}, V_{EE} = −5.0 V_{DC}, Min ≤ T_A ≤ Max, unless otherwise noted) (Notes 2 and 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IS}	Input Sensitivity, (Note 5) (Common-Mode Voltage Range = −3V ≤ V_{IN} ≤ 3V)	Min ≤ V_{CC} ≤ Max Min ≥ V_{EE} ≥ Max				±25.0	mV
$I_{IH(I)}$	High Level Input Current to Receiver Input	*(Figure 5)*				75	µA
$I_{IL(I)}$	Low Level Input Current to Receiver Input	*(Figure 6)*				−10	µA
$I_{IH(S)}$	High Level Input Current to Strobe Input	*(Figure 3)*	$V_{IH(S)}$ = 2.4V, DS1650, DS1652			100	µA
			$V_{IH(S)}$ = 2.4V, DS3650, DS3652			40	µA
			$V_{IH(S)}$ = V_{CC}			1	mA
$I_{IL(S)}$	Low Level Input Current to Strobe Input		$V_{IH(S)}$ = 0.4V			−1.6	mA
V_{OH}	High Level Output Voltage	*(Figure 1)*	DS1650, DS3650	2.4			V
I_{CEX}	High Level Output Leakage Current	*(Figure 1)*	DS1652, DS3652			250	µA
V_{OL}	Low Level Output Voltage	*(Figure 1)*	DS3650, DS3652			0.45	V
			DS1650, DS1652			0.50	
I_{OS}	Short-Circuit Output Current (Note 4)	*(Figure 4)*	DS1650/DS3650	−18		−70	mA
I_{OFF}	Output Disable Leakage Current	*(Figure 7)*	DS1650			100	µA
			DS3650			40	µA

Electrical Characteristics

(V_{CC} = 5.0 V_{DC}, V_{EE} = −5.0 V_{DC}, Min ≤ T_A ≤ Max, unless otherwise noted) (Notes 2 and 3) (Continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
I_{CCH}	High Logic Level Supply Current from V_{CC}	*(Figure 2)*			45	60	mA
I_{EEH}	High Logic Level Supply Current from V_{EE}	*(Figure 2)*			−17	−30	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified, min/max limits apply across the 0°C to +70°C range for the DS3650, DS3652 and the −55°C to +125°C range for the DS1650, DS1652. All typical values are for T_A = 25°C, V_{CC} = 5V and V_{EE} = −5V.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

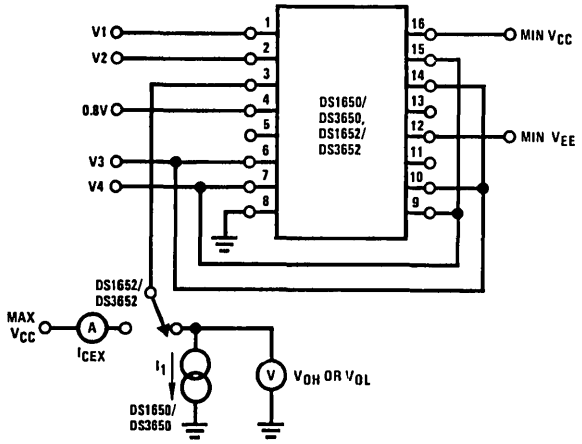
Note 4: Only one output at a time should be shorted.

Note 5: A parameter which is of primary concern when designing with line receivers is, what is the minimum differential input voltage required as the receiver input terminals to guarantee a given output logic state. This parameter is commonly referred to as threshold voltage. It is well known that design considerations of threshold voltage are plagued by input offset currents, bias currents, network source resistances, and voltage gain. As a design convenience, the DS1650, DS1652 and the DS3650, DS3652 are specified to a parameter called input sensitivity (V_{IS}). This parameter takes into consideration input offset currents and bias currents and guarantees a minimum input differential voltage to cause a given output logic state with respect to a maximum source impedance of 200Ω at each input.

Switching Characteristics (V_{CC} = 5 V_{DC}, V_{EE} = −5 V_{DC}, T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
$t_{PHL(D)}$	High-to-Low Logic Level Propagation Delay Time (Differential Inputs)	*(Figure 8)*	DS1650/DS3650		21	25	ns
			DS1652/DS3652		20	25	ns
$t_{PLH(D)}$	Low-to-High Logic Level Propagation Delay Time (Differential Inputs)		DS1650/DS3650		20	25	ns
			DS1652/DS3652		22	25	ns
$t_{POH(S)}$	TRI-STATE to High Logic Level Propagation Delay Time (Strobe)	*(Figure 9)*	DS1650/DS3650		16	21	ns
$t_{PHO(S)}$	High Logic Level to TRI-STATE Propagation Delay Time (Strobe)		DS1650/DS3650		7	18	ns
$t_{POL(S)}$	TRI-STATE to Low Logic Level Propagation Delay Time (Strobe)		DS1650/DS3650		19	27	ns
$t_{PLO(S)}$	Low Logic Level to TRI-STATE Propagation Delay Time (Strobe)		DS1650/DS3650		14	29	ns
$t_{PHL(S)}$	High-to-Low Logic Level Propagation Delay Time (Strobe)	*(Figure 10)*	DS1652/DS3652		16	25	ns
$t_{PLH(S)}$	Low-to-High Logic Level Propagation Delay Time (Strobe)		DS1652/DS3652		13	25	ns

Electrical Characteristic Test Circuits



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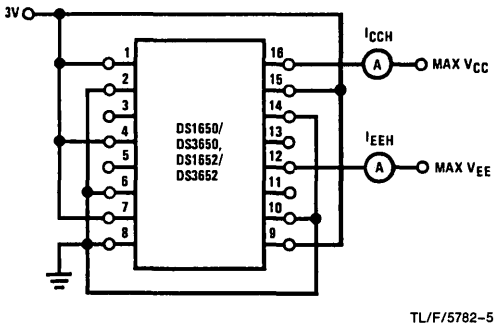
	V1		V2		V3		V4		
	DS1650/ DS3650	DS1652/ DS3652	DS1650/ DS3650	DS1652/ DS1652	DS1650/ DS1650	DS1652/ DS1652	DS1650/ DS1650	DS1652/ DS1652	I_1
V_{OH}	+2.975V −3.0V		+3.0V −2.975V		+3.0V GND		GND −3.0V		−0.4 mA −0.4 mA
I_{CEX}		+2.975V −3.0V		+3.0V −2.975V		+3.0V GND		GND −3.0V	
V_{OL}	+3.0V −2.975V	+3.0V −2.975V	+2.975V −3.0V	+2.975V −3.0V	GND −3.0V	GND −3.0V	+3.0V GND	+3.0V GND	+16 mA +16 mA

Channel A shown under test. Other channels are tested similarly.

FIGURE 1. I_{CEX}, V_{OH} and V_{OL}



TL/F/5782–5

FIGURE 2. I_{CCH} and I_{EEH}

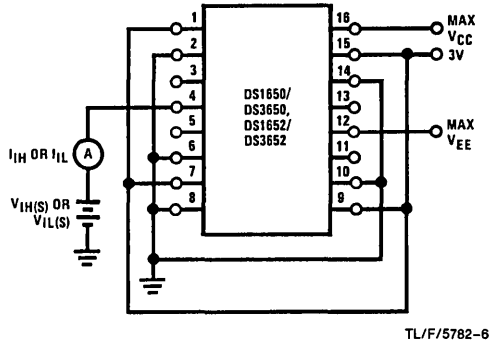


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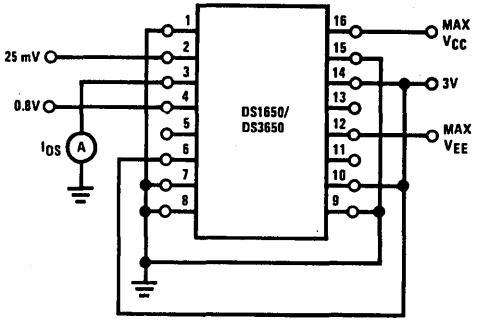
FIGURE 3. $I_{IH(S)}$ and $I_{IL(S)}$

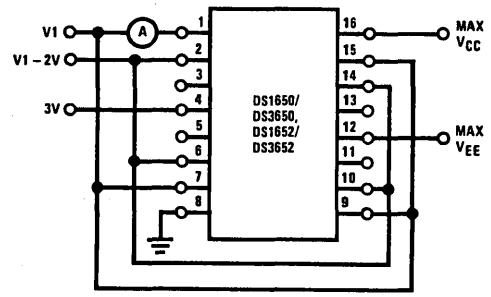
Electrical Characteristic Test Circuits (Continued)



TL/F/5782–7

Note: Channel A shown under test, other channels are tested similiarly. Only one output shorted at a time.

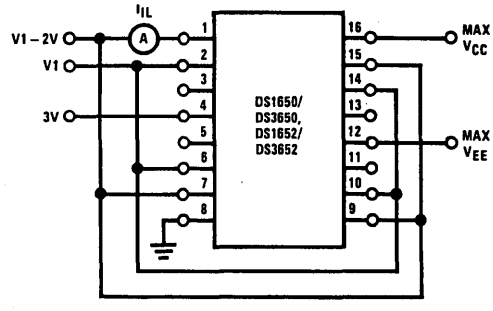
FIGURE 4. I_{OS}



TL/F/5782–8

Note: Channel A(−) shown under test, other channels are tested similarly. Devices are tested with V1 from 3V to −3V.

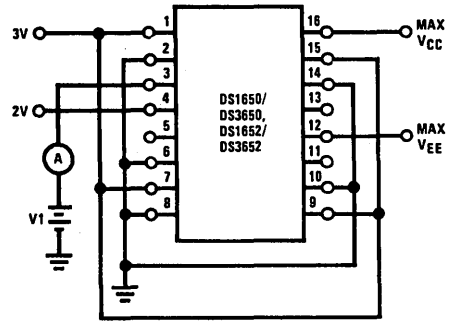
FIGURE 5. I_{IH}



TL/F/5782–9

Note: Channel A(−) shown under test, other channels are tested similarly. Devices are tested with V1 from 3V to −3V.

FIGURE 6. I_{IL}

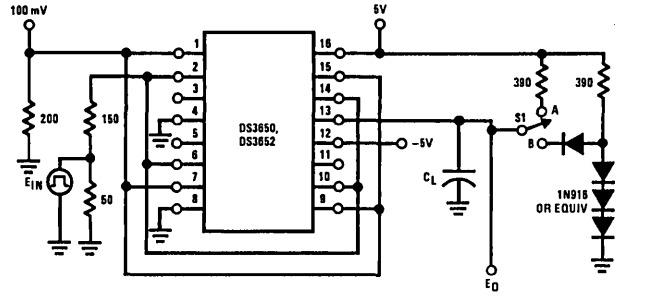


TL/F/5782–10

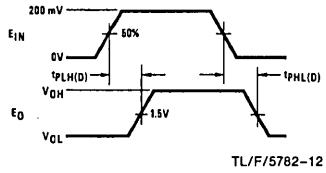
Note: Output of Channel A shown under test, other outputs are tested similarly for V1 = 0.4V and 2.4V.

FIGURE 7. I_{OFF}

AC Test Circuits and Switching Time Waveforms



TL/F/5782–11



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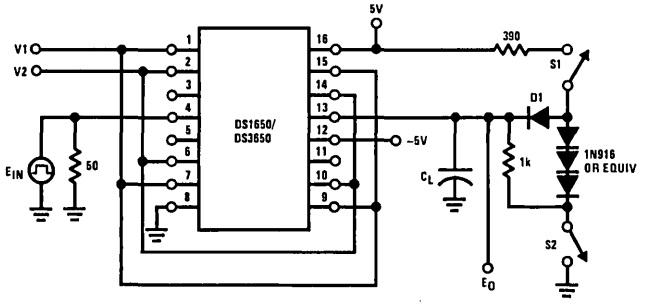
Note: E_{IN} waveform characteristics:
t_{TLH} and $t_{THL} \leq 10$ ns measured
10% to 90%
PRR = 1 MHz
Duty Cycle = 50%

Note: Output of Channel B shown under test, other channels are tested similarly.

S1 at "A" for DS1652/DS3652
S1 at "B" for DS1650/DS3650
C_L = 15 pF total for DS1652/DS3652
C_L = 50 pF total for DS1650/DS3650

FIGURE 8. Receiver Propagation Dealy $t_{PLH(D)}$ and $t_{PHL(D)}$



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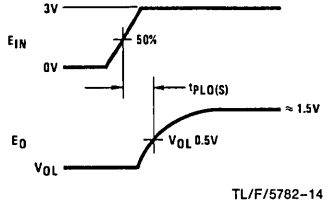

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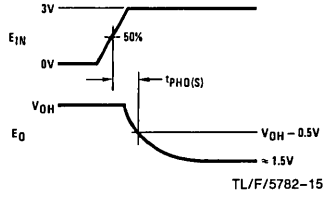
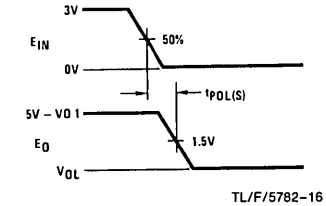


TL/F/5782–15

Note: Output of Channel B shown under test, other channels are tested similiarly.

	V1	V2	S1	S2	C_L
$t_{PLO(S)}$	100 mV	GND	Closed	Closed	15 pF
$t_{POL(S)}$	100 mV	GND	Closed	Open	50 pF
$t_{PHO(S)}$	GND	100 mV	Closed	Closed	15 pF
$t_{POH(S)}$	GND	100 mV	Open	Closed	50 pF

C_L includes jig and probe capacitance.
E_{IN} waveform characteristics: t_{TLH} and $t_{THL} \leq 10$ ns measured 10% to 90%
PRR = 1 MHz
Duty Cycle = 50%



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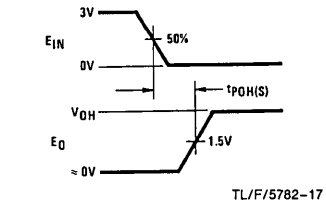
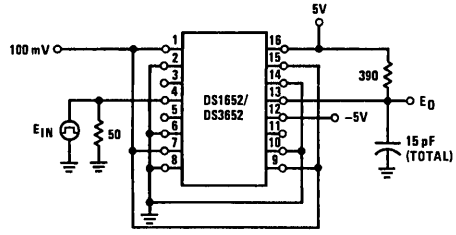


TL/F/5782–17

FIGURE 9. Strobe Propagation Delay $t_{PLO(S)}$, $t_{POL(S)}$, $t_{PHO(S)}$ and $t_{POH(S)}$

AC Test Circuits and Switching Time Waveforms (Continued)



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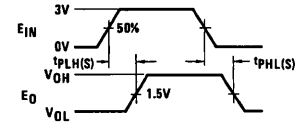


TL/F/5782–19

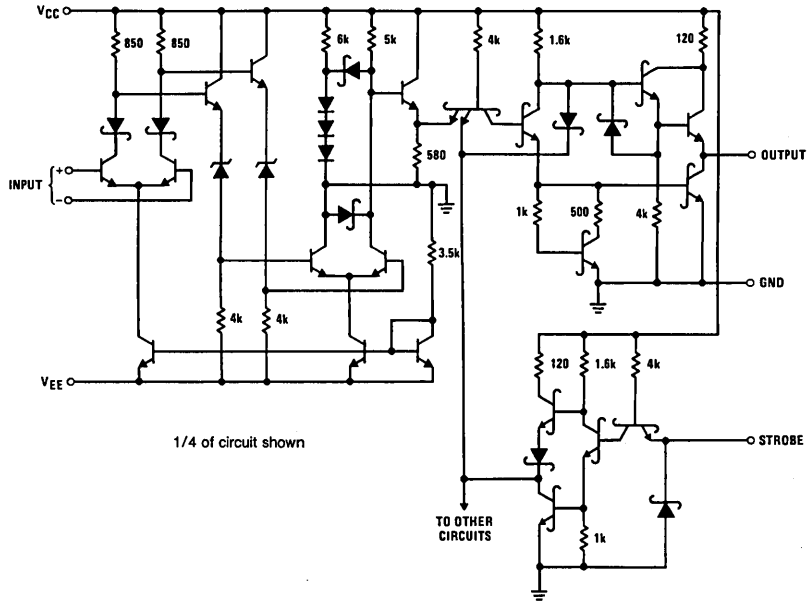
Note: Output of Channel B shown under test, other channels are tested similarly.

Note: E_{IN} waveform characteristics:
t_{TLH} and $t_{THL} \leq 10$ ns measured 10% and 90%
PRR = 1 MHz
Duty Cycle = 500 ns

FIGURE 10. Strobe Propagation Delay $t_{PLH(S)}$ and $t_{PHL(S)}$

Schematic Diagrams

DS1650/DS3650

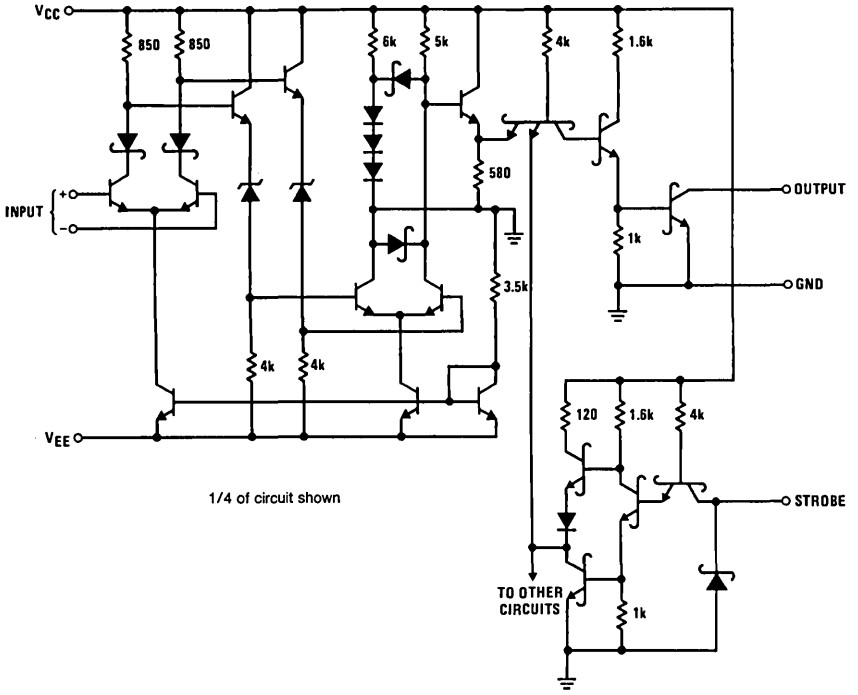


1/4 of circuit shown

TL/F/5782–20

Schematic Diagrams (Continued)

DS1652/DS3652



1/4 of circuit shown

TL/F/5782–21

National Semiconductor Corporation

DS1691A/DS3691 (RS-422/RS-423) Line Drivers with TRI-STATE® Outputs

General Description

The DS1691A/DS3691 are low power Schottky TTL line drivers designed to meet the requirements of EIA standards RS-422 and RS-423. They feature 4 buffered outputs with high source and sink current capability with internal short circuit protection. A mode control input provides a choice of operation either as 4 independent line drivers or 2 differential line drivers. A rise time control pin allows the use of an external capacitor to reduce rise time for suppression of near end crosstalk to other receivers in the cable.

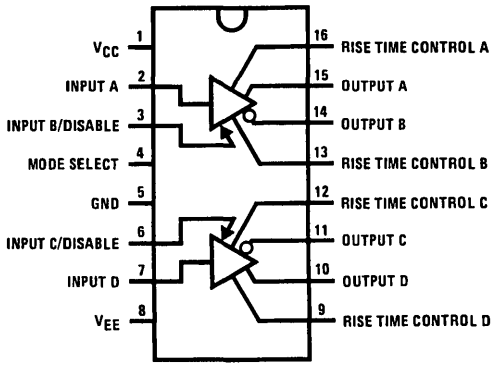
With the mode select pin low, the DS1691A/DS3691 are dual-differential line drivers with TRI-STATE outputs. They feature ±10V output common-mode range in TRI-STATE mode and 0V output unbalance when operated with ±5V supply.

Features

- Dual RS-422 line driver with mode pin low, or quad RS-423 line driver with mode pin high
- TRI-STATE control for individual outputs
- Short circuit protection for both source and sink outputs
- Outputs will not clamp line with power off or in TRI-STATE
- Individual rise mode time control for each output
- 100Ω transmission line drive capability
- Low I_{CC} and I_{EE} power consumption
  - RS-422 35 mW/driver typ
  - RS-423 26 mW/driver typ
- Low current PNP inputs compatible with TTL, MOS and CMOS

Connection Diagram

With Mode Select LOW (RS-422 Connection)



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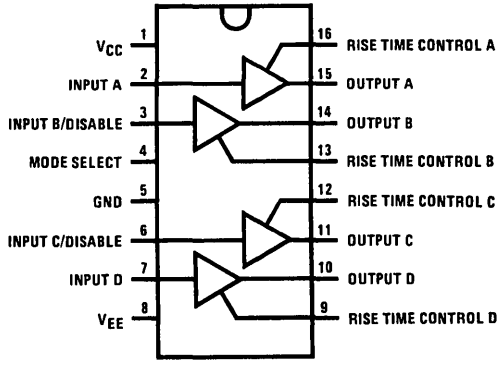
Top View

With Mode Select HIGH (RS-423 Connection)



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Top View

Truth Table

Operation	Inputs			Outputs	
	Mode	A (D)	B (C)	A (D)	B (C)
RS-422	0	0	0	0	1
	0	0	1	TRI-STATE	TRI-STATE
	0	1	0	1	0
	0	1	1	TRI-STATE	TRI-STATE
RS-423	1	0	0	0	0
	1	0	1	0	1
	1	1	0	1	0
	1	1	1	1	1

Order Number DS1691AJ, DS3691J, DS3691M or DS3691N
See NS Package Number J16A, M16A or N16A

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage
- V_{CC} 7V
- V_{EE} −7V

Maximum Power Dissipation* at 25°C
- Cavity Package 1509 mW
- Molded DIP Package 1476 mW
- SO Package 1051 mW

Input Voltage 15V

Output Voltage (Power OFF) ±15V

Storage Temperature −65°C to + 150°C

Lead Temperature (Soldering, 4 seconds) 260°C

*Derate cavity package 10.1 mW/°C above 25°C; derate molded DIP package 11.9 mW/°C above 25°C. Derate SO package 8.41 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage			
DS1691A			
V_{CC}	4.5	5.5	V
V_{EE}	−4.5	−5.5	V
DS3691			
V_{CC}	4.75	5.25	V
V_{EE}	4.75	5.25	V
Temperature (T_A)			
DS1691A	−55	+125	°C
DS3691	0	+70	°C

DC Electrical Characteristics (Notes 2, 3, 4 and 5)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
RS-422 CONNECTION, V_{EE} CONNECTION TO GROUND, MODE SELECT ≤ 0.8V							
V_{IH}	High Level Input Voltage			2			V
V_{IL}	Low Level Input Voltage					0.8	V
I_{IH}	High Level Input Current	V_{IN} = 2.4V			1	40	µA
		V_{IN} ≤ 15V			10	100	µA
I_{IL}	Low Level Input Current	V_{IN} = 0.4V			−30	−200	µA
V_I	Input Clamp Voltage	I_{IN} = −12 mA				−1.5	V
V_O	Differential Output Voltage	R_L = ∞	V_{IN} = 2V		3.6	6.0	V
$\overline{V_O}$	$V_{A,B}$		V_{IN} = 0.8V		−3.6	−6.0	V
V_T	Differential Output Voltage	R_L = 100Ω	V_{IN} = 2V	2	2.4		V
$\overline{V_T}$	$V_{A,B}$	V_{CC} ≥ 4.75V	V_{IN} = 0.8V	−2	−2.4		V
V_{OS}, $\overline{V_{OS}}$	Common-Mode Offset Voltage	R_L = 100Ω			2.5	3	V
$\lvert V_T \rvert - \lvert \overline{V_T} \rvert$	Difference in Differential Output Voltage	R_L = 100Ω			0.05	0.4	V
$\lvert V_{OS} \rvert - \lvert \overline{V_{OS}} \rvert$	Difference in Common-Mode Offset Voltage	R_L = 100Ω			0.05	0.4	V
V_{SS}	$\lvert V_T - \overline{V_T} \rvert$	R_L = 100Ω, V_{CC} ≥ 4.75V		4.0	4.8		V
V_{CMR}	Output Voltage Common-Mode Range	$V_{DISABLE}$ = 2.4V		±10			V
I_{XA}	Output Leakage Current Power OFF	V_{CC} = 0V	V_{CMR} = 10V			100	µA
I_{XB}			V_{CMR} = −10V			−100	µA
I_{OX}	TRI-STATE Output Current	V_{CC} = Max	V_{CMR} ≤ 10V			100	µA
			V_{CMR} ≥ −10V			−100	µA
I_{SA}	Output Short Circuit Current	V_{IN} = 0.4V	V_{OA} = 6V		80	150	mA
			V_{OB} = 0V		−80	−150	mA
I_{SB}	Output Short Circuit Current	V_{IN} = 2.4V	V_{OA} = 0V		−80	−150	mA
			V_{OB} = 6V		80	150	mA
I_{CC}	Supply Current				18	30	mA

AC Electrical Characteristics T_A = 25°C (Note 5)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
RS-422 CONNECTION, V_{CC} = 5V, MODE SELECT = 0.8V						
t_r	Output Rise Time	R_L = 100Ω, C_L = 500 pF *(Figure 1)*		120	200	ns
t_f	Output Fall Time	R_L = 100Ω, C_L = 500 pF *(Figure 1)*		120	200	ns
t_{PDH}	Output Propagation Delay	R_L = 100Ω, C_L = 500 pF *(Figure 1)*		120	200	ns
t_{PDL}	Output Propagation Delay	R_L = 100Ω, C_L = 500 pF *(Figure 1)*		120	200	ns
t_{PZL}	TRI-STATE Delay	R_L = 450Ω, C_L = 500 pF, C_C = 0 pF *(Figure 4)*		250	350	ns
t_{PZH}	TRI-STATE Delay	R_L = 450Ω, C_L = 500 pF, C_C = 0 pF *(Figure 4)*		180	300	ns
t_{PLZ}	TRI-STATE Delay	R_L = 450Ω, C_L = 500 pF, C_C = 0 pF *(Figure 4)*		180	300	ns
t_{PHZ}	TRI-STATE Delay	R_L = 450Ω, C_L = 500 pF, C_C = 0 pF *(Figure 4)*		250	350	ns

DC Electrical Characteristics (Notes 2, 3, 4 and 5)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
RS-423 CONNECTION, $\|V_{CC}\| = \|V_{EE}\|$, MODE SELECT ≥ 2V							
V_{IH}	High Level Input Voltage			2			V
V_{IL}	Low Level Input Voltage					0.8	V
I_{IH}	High Level Input Current	V_{IN} = 2.4V			1	40	μA
		V_{IN} ≤ 15V			10	100	μA
I_{IL}	Low Level Input Current	V_{IN} = 0.4			−30	−200	μA
V_I	Input Clamp Voltage	I_{IN} = −12 mA				−1.5	V
V_O	Output Voltage	R_L = ∞, (Note 6) V_{CC} ≥ 4.75V	V_{IN} = 2V	4.0	4.4	6.0	V
$\overline{V_O}$			V_{IN} = 0.4V	−4.0	−4.4	−6.0	V
V_T	Output Voltage	R_L = 450Ω V_{CC} ≥ 4.75V	V_{IN} = 2.4V	3.6	4.1		V
$\overline{V_T}$			V_{IN} = 0.4V	−3.6	−4.1		V
$\|V_T\| - \|\overline{V_T}\|$	Output Unbalance	$\|V_{CC}\| = \|V_{EE}\|$ = 4.75V, R_L = 450Ω			0.02	0.4	V
I_X^+	Output Leakage Power OFF	$V_{CC} = V_{EE}$ = 0V	V_O = 6V		2	100	μA
I_X^-	Output Leakage Power OFF	$V_{CC} = V_{EE}$ = 0V	V_O = −6V		−2	−100	μA
I_S^+	Output Short Circuit Current	V_O = 0V	V_{IN} = 2.4V		−80	−150	mA
I_S^-	Output Short Circuit Current	V_O = 0V	V_{IN} = 0.4V		80	150	mA
I_{SLEW}	Slew Control Current				±140		μA
I_{CC}	Positive Supply Current	V_{IN} = 0.4V, R_L = ∞			18	30	mA
I_{EE}	Negative Supply Current	V_{IN} = 0.4V, R_L = ∞			−10	−22	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: Unless otherwise specified, min/max limits apply across the −55°C to +125°C temperature range for the DS1691A and across the 0°C to +70°C range for the DS3691. All typicals are given for V_{CC} = 5V and T_A = 25°C. V_{CC} and V_{EE} as listed in operating conditions.

Note 3: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified.

Note 4: Only one output at a time should be shorted.

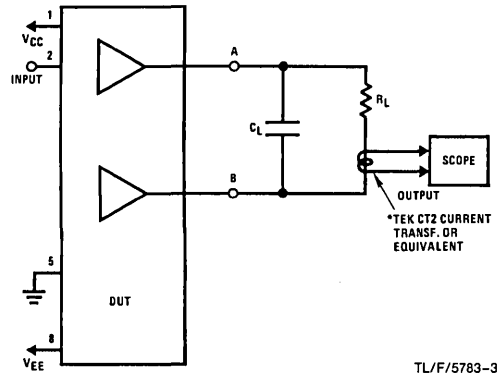
Note 5: Symbols and definitions correspond to EIA RS-422 and/or RS-423 where applicable.

Note 6: At −55°C, the output voltage is +3.9V minimum and −3.9V minimum.

AC Electrical Characteristics T_A = 25°C (Note 5)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
RS-423 CONNECTION, V_{CC} = 5V, V_{EE} −5V, MODE SELECT = 2.4V						
t_r	Rise Time	R_L = 450Ω, C_L = 500 pF, C_C = 0 *(Figure 2)*		120	300	ns
t_f	Fall Time	R_L = 450Ω, C_L = 500 pF, C_C = 0 *(Figure 2)*		120	300	ns
t_r	Rise Time	R_L = 450Ω, C_L = 500 pF C_C = 50 pF *(Figure 3)*		3.0		µs
t_f	Fall Time	R_L = 450Ω, C_L = 500 pF C_C = 50 pF *(Figure 3)*		3.0		µs
t_{rc}	Rise Time Coefficient	R_L = 450Ω, C_L = 500 pF, C_C = 50 pF *(Figure 3)*		0.06		µs/pF
t_{PDH}	Output Propagation Delay	R_L = 450Ω, C_L = 500 pF, C_C = 0 *(Figure 2)*		180	300	ns
t_{PDL}	Output Propagation Delay	R_L = 450Ω, C_L = 500 pF, C_C = 0 *(Figure 2)*		180	300	ns

AC Test Circuits and Switching Time Waveforms



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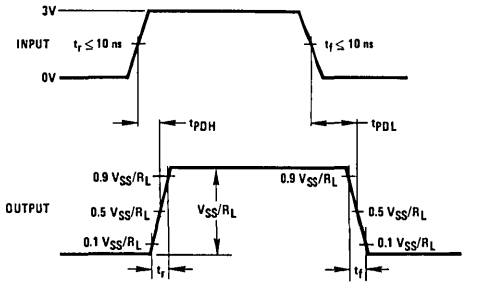
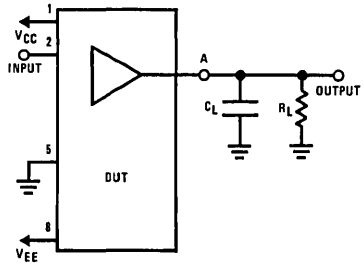
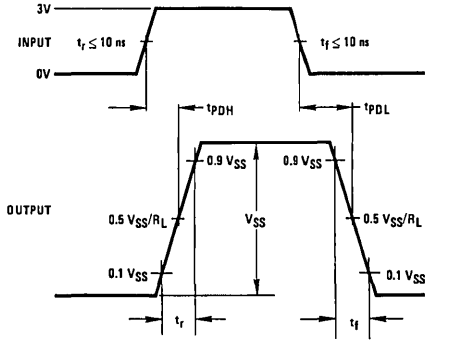


TL/F/5783-4

FIGURE 1. Differential Connection



TL/F/5783-5



TL/F/5783-6

FIGURE 2. RS-423 Connection

AC Test Circuits and Switching Time Waveforms (Continued)

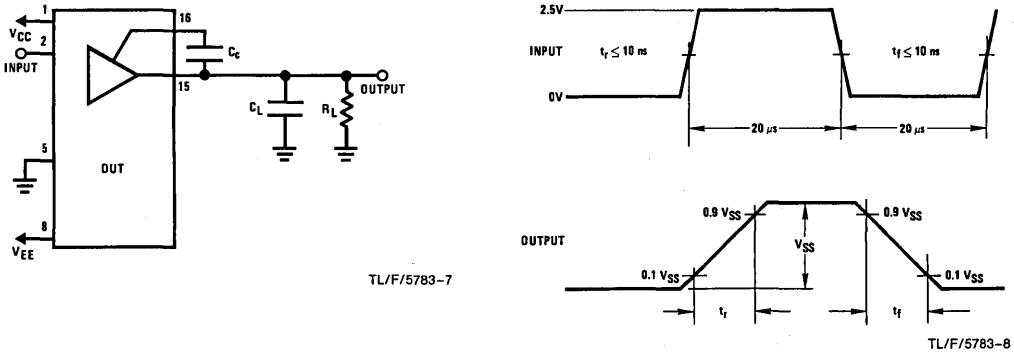


FIGURE 3. Rise Time Control for RS-423

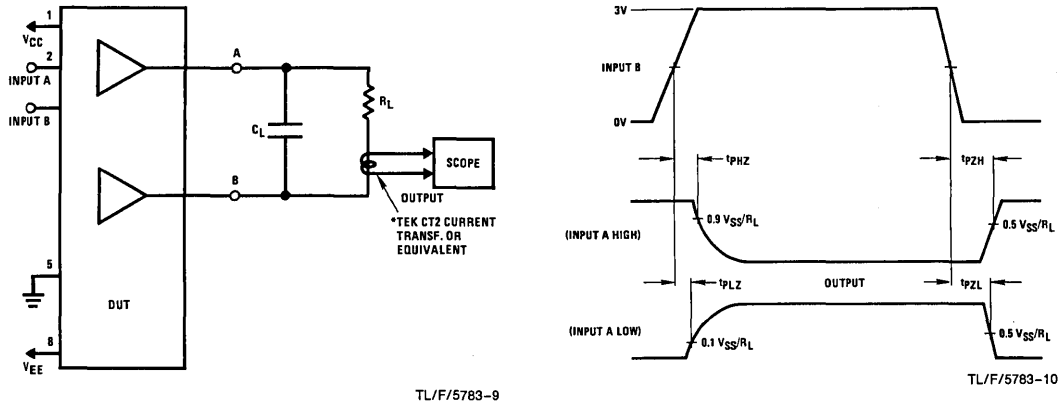
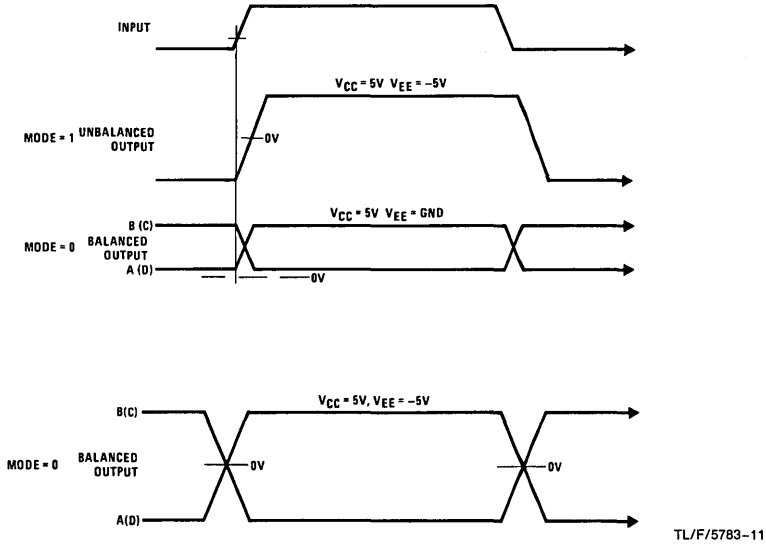


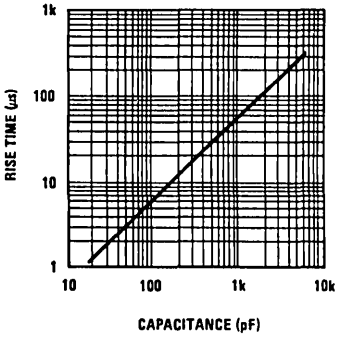
FIGURE 4. TRI-STATE Delays

Switching Waveforms



Typical Rise Time Control Characteristics

Rise Time vs External Capacitor



TL/F/5783–12

National Semiconductor Corporation

DS1692/DS3692 TRI-STATE® Differential Line Drivers

General Description

The DS1692/DS3692 are low power Schottky TTL line drivers electrically similar to the DS1691A/DS3691 but tested to meet the requirements of MIL-STD-188-114. They feature 4 buffered outputs with high source and sink current capability with internal short circuit protection. A mode control input provides a choice of operation either as 4 independent line drivers or 2 differential line drivers. A rise time control pin allows the use of an external capacitor to reduce rise time for suppression of near end cross-talk to other receivers in the cable.

With the mode select pin low, the DS1692/DS3692 are dual differential line drivers with TRI-STATE outputs. They feature ±10V output common-mode range in TRI-STATE and 0V output unbalance when operated with ±5V supply.

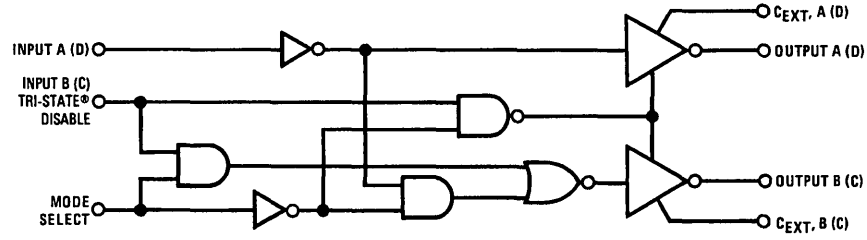
Features

- Dual differential line driver or quad single-ended line driver
- TRI-STATE differential drivers meet MIL-STD-188-114
- Short circuit protection for both source and sink outputs
- Individual rise time control for each output
- 100Ω transmission line drive capability
- Low I_{CC} and I_{EE} power consumption

Differential mode	35 mW/driver typ
Single-ended mode	26 mW/driver typ

- Low current PNP inputs compatible with TTL, MOS and CMOS

Logic Diagram (½ Circuit Shown)



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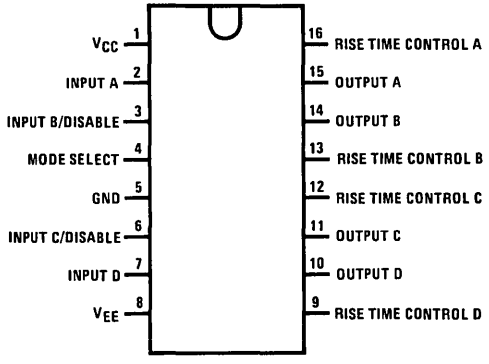
Connection Diagram



TL/F/5784–2

Top View

Order Number DS1692J, DS3692J or DS3692N
See NS Package Number J16A or N16A

Truth Table

Inputs			Outputs	
Mode	A (D)	B (C)	A (D)	B (C)
0	0	0	0	1
0	0	1	TRI-STATE	TRI-STATE
0	1	0	1	0
0	1	1	TRI-STATE	TRI-STATE
1	0	0	0	0
1	0	1	0	1
1	1	0	1	0
1	1	1	1	1

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	
V_{CC}	7V
V_{EE}	−7V
Maximum Power Dissipation* at 25°C	
Cavity Package	1509 mW
Molded Package	1476 mW
Input Voltage	15V
Output Voltage (Power OFF)	±15V
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 4 sec.)	260°C

*Derate cavity package 10.1 mW/°C; derate molded package 11.9 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage			
DS1692			
V_{CC}	4.5	5.5	V
V_{EE}	−4.5	−5.5	V
DS3692			
V_{CC}	4.75	5.25	V
V_{EE}	−4.75	−5.25	V
Temperature (T_A)			
DS1692	−55	+125	°C
DS3692	0	+70	°C

Electrical Characteristics DS1692/DS3692 (Notes 2, 3 and 4)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
DS1692, V_{CC} = 5V ±10%, DS3692, V_{CC} = 5V ±5%, V_{EE} CONNECTION TO GROUND, MODE SELECT ≤ 0.8V							
V_O / $\overline{V_O}$	Differential Output Voltage $V_{A,B}$	R_L = ∞	V_{IN} = 2V	2.5	3.6		V
			V_{IN} = 0.8V	−2.5	−3.6		V
V_T / $\overline{V_T}$	Differential Output Voltage $V_{A,B}$	R_L = 100Ω, V_{CC} ≥ 4.75V	V_{IN} = 2V	2	2.6		V
			V_{IN} = 0.8V	−2	−2.6		V
V_{OS}, $\overline{V_{OS}}$	Common-Mode Offset Voltage	R_L = 100Ω			2.5	3	V
$\lvert V_T \rvert - \lvert \overline{V_T} \rvert$	Difference in Differential Output Voltage	R_L = 100Ω			0.05	0.4	V
$\lvert V_{OS} \rvert - \lvert \overline{V_{OS}} \rvert$	Difference in Common-Mode Offset Voltage	R_L = 100Ω			0.05	0.4	V
V_{SS}	$\lvert V_T - \overline{V_T} \rvert$	R_L = 100Ω, V_{CC} ≥ 4.75V		4.0	4.8		V
I_{OX}	TRI-STATE Output Current	V_O ≤ −10V			−0.002	−0.15	mA
		V_O ≥ 15V			0.002	0.15	mA
I_{SA}	Output Short Circuit Current	V_{IN} = 0.4V	V_{OA} = 6V		80	150	mA
			V_{OB} = 0V		−80	−150	mA
I_{SB}	Output Short Circuit Current	V_{IN} = 2.4V	V_{OA} = 0V		−80	−150	mA
			V_{OB} = 6V		80	150	mA
I_{CC}	Supply Current				18	30	mA
DS1692, V_{CC} = 5V ±10%, V_{EE} = −5V ±10%, DS3692, V_{CC} = 5V ±5%, V_{EE} = −5 ±5%, MODE SELECT ≤ 0.8V							
V_O / $\overline{V_O}$	Differential Output Voltage $V_{A,B}$	R_L = ∞	V_{IN} = 2.4V	7	8.5		V
			V_{IN} = 0.4V	−7	−8.5		V
V_T / $\overline{V_T}$	Differential Output Voltage $V_{A,B}$	R_L = 200Ω	V_{IN} = 2.4V	6	7.3		V
			V_{IN} = 0.4V	−6	−7.3		V
$\lvert V_T \rvert - \lvert \overline{V_T} \rvert$	Output Unbalance	$\lvert V_{CC} \rvert = \lvert V_{EE} \rvert$, R_L = 200Ω			0.02	0.4	V
I_{OX}	TRI-STATE Output Current		V_O = 10V		0.002	0.15	mA
			V_O = −10V		−0.002	−0.15	mA
I_S^+ / I_S^-	Output Short Circuit Current	V_O = 0V	V_{IN} = 2.4V		−80	−150	mA
			V_{IN} = 0.4V		80	150	mA
I_{SLEW}	Slew Control Current				±140		µA
I_{CC}	Positive Supply Current	V_{IN} = 0.4V, R_L = ∞			18	30	mA
I_{EE}	Negative Supply Current	V_{IN} = 0.4V, R_L = ∞			−10	−22	mA

Electrical Characteristics (Notes 2 and 3) $V_{EE} \leq 0V$

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IH}	High Level Input Voltage			2			V
V_{IL}	Low Level Input Voltage					0.8	V
I_{IH}	High Level Input Current	$V_{IN} = 2.4V$			1	40	μA
		$V_{IN} \leq 15V$			10	100	μA
I_{IL}	Low Level Input Current	$V_{IN} = 0.4V$			−30	−200	μA
V_I	Input Clamp Voltage	$I_{IN} = -12$ mA				−1.5	V
I_{XA}	Output Leakage Current	$V_{CC} = V_{EE} = 0$	$V_O = 15V$		0.01	0.15	mA
I_{XB}	Power OFF		$V_O = -15V$		−0.01	−0.15	mA

Switching Characteristics $T_A = 25°C$

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{CC} = 5V, MODE SELECT = 0.8V						
t_r	Differential Output Rise Time	$R_L = 100\Omega$, $C_L = 500$ pF *(Figure 1)*		120	200	ns
t_f	Differential Output Fall Time	$R_L = 100\Omega$, $C_L = 500$ pF *(Figure 1)*		120	200	ns
t_{PDH}	Output Propagation Delay	$R_L = 100\Omega$, $C_L = 500$ pF *(Figure 1)*		120	200	ns
t_{PDL}	Output Propagation Delay	$R_L = 100\Omega$, $C_L = 500$ pF *(Figure 1)*		120	200	ns
t_{PZL}	TRI-STATE Delay	$R_L = 100\Omega$, $C_L = 500$ pF *(Figure 2)*		180	250	ns
t_{PZH}	TRI-STATE Delay	$R_L = 100\Omega$, $C_L = 500$ pF *(Figure 2)*		180	250	ns
t_{PLZ}	TRI-STATE Delay	$R_L = 100\Omega$, $C_L = 500$ pF *(Figure 2)*		80	150	ns
t_{PHZ}	TRI-STATE Delay	$R_L = 100\Omega$, $C_L = 500$ pF *(Figure 2)*		80	150	ns
V_{CC} = 5V, V_{EE} = −5V, MODE SELECT = 0.8V						
t_r	Differential Output Rise Time	$R_L = 200\Omega$, $C_L = 500$ pF *(Figure 1)*		190	300	ns
t_f	Differential Output Fall Time	$R_L = 200\Omega$, $C_L = 500$ pF *(Figure 1)*		190	300	ns
t_{PDL}	Output Propagation Delay	$R_L = 200\Omega$, $C_L = 500$ pF *(Figure 1)*		190	300	ns
t_{PDH}	Output Propagation Delay	$R_L = 200\Omega$, $C_L = 500$ pF *(Figure 1)*		190	300	ns
t_{PZL}	TRI-STATE Delay	$R_L = 200\Omega$, $C_L = 500$ pF *(Figure 2)*		180	250	ns
t_{PZH}	TRI-STATE Delay	$R_L = 200\Omega$, $C_L = 500$ pF *(Figure 2)*		180	250	ns
t_{PLZ}	TRI-STATE Delay	$R_L = 200\Omega$, $C_L = 500$ pF *(Figure 2)*		80	150	ns
t_{PHZ}	TRI-STATE Delay	$R_L = 200\Omega$, $C_L = 500$ pF *(Figure 2)*		80	150	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: Unless otherwise specified, min/max limits apply across the −55°C to +125°C temperature range for the DS1692 and across the 0°C to +70°C range for the DS3692. All typicals are given for V_{CC} = 5V and T_A = 25°C. V_{CC} and V_{EE} as listed in operating conditions.

Note 3: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified.

Note 4: Only one output at a time should be shorted.

AC Test Circuits and Switching Time Waveforms

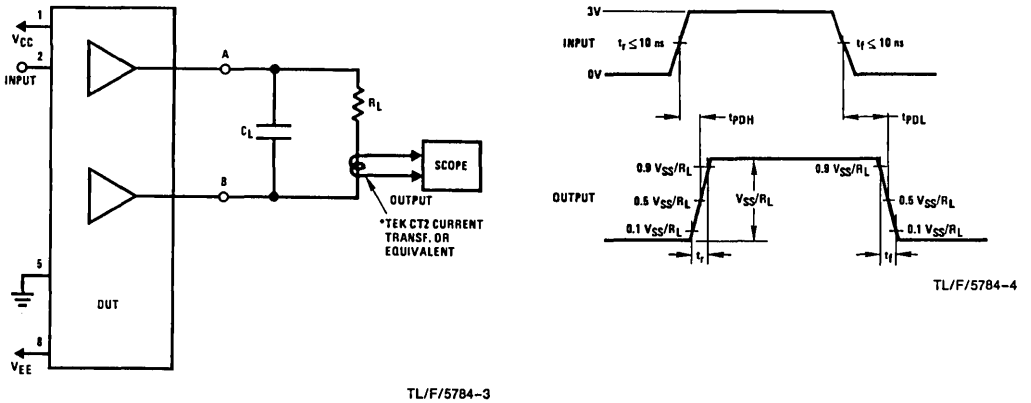


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FIGURE 1. Differential Connection

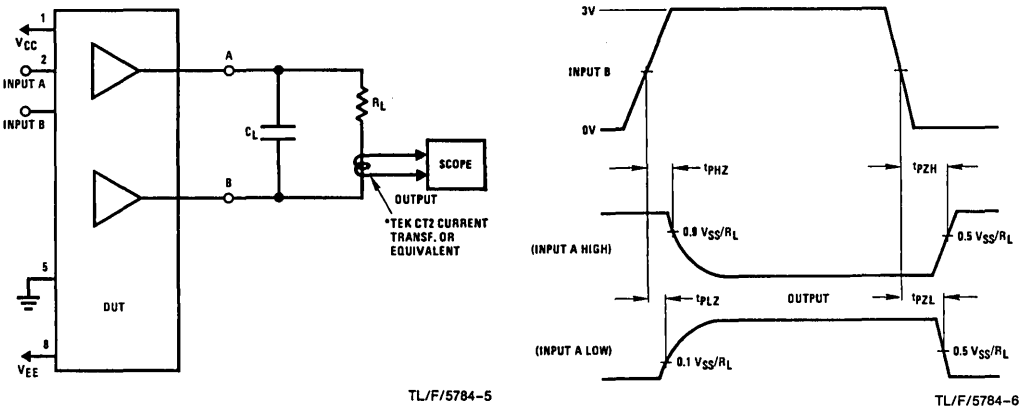

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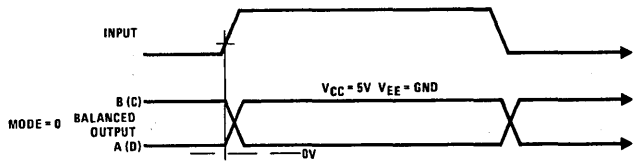
FIGURE 2. TRI-STATE Delays for DS1692/DS3692

Switching Waveforms



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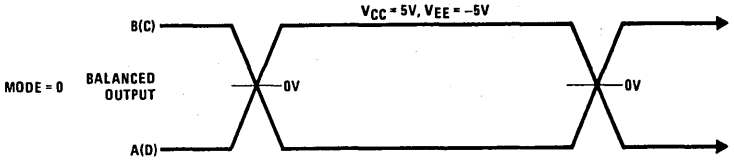

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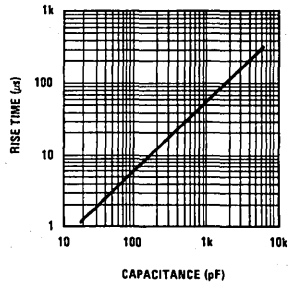
Typical Rise Time Control Characteristics



TL/F/5784–9

National Semiconductor Corporation

DS3695/DS3695T/DS3696/DS3696T/DS3697/DS3698 Multipoint RS485/RS422 Transceivers/Repeaters

General Description

The DS3695, DS3696, DS3697 and DS3698 are high speed differential TRI-STATE® bus/line transceivers/repeaters designed to meet the requirements of EIA standard RS485 with extended common mode range (+12V to −7V), for multipoint data transmission. In addition they meet the requirements of RS422.

The driver and receiver outputs feature TRI-STATE capability, for the driver outputs over the entire common mode range of +12V to −7V. Bus contention or fault situations that cause excessive power dissipation within the device are handled by a thermal shutdown circuit, which forces the driver outputs into the high impedance state. The DS3696 and DS3698 provide an output pin which reports the occurrence of a line fault causing thermal shutdown of the device. This is an "open collector" pin with an internal 10 kΩ pull-up resistor. This allows the line fault outputs of several devices to be wire OR-ed.

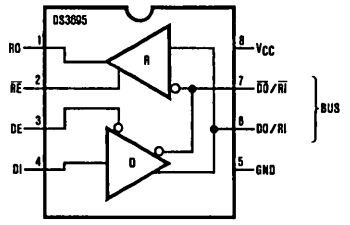
The receiver incorporates a fail safe feature which guarantees a high output state when the inputs are left open.

Both AC and DC specifications are guaranteed over the 0 to 70°C temperature and 4.75V to 5.25V supply voltage range.

Features

- Meets EIA standard RS485 for multipoint bus transmission and RS422.
- 15 ns driver propagation delays with 2 ns skew (typical).
- Single channel per package isolates faulty channels (from shutting down good channels).
- Single +5V supply.
- −7V to +12V bus common mode range permits ±7V ground difference between devices on the bus.
- Thermal shutdown protection.
- Power-up down glitch-free driver outputs permit live insertion or removal of transceivers.
- High impedance to bus with driver in TRI-STATE or with power off, over the entire common mode range allows the unused devices on the bus to be powered down.
- Line fault reporting capability on DS3696 and DS3698 allows automated fault location and re-routing under processor control.
- Combined impedance of a driver output and receiver input is less than one RS485 unit load, allowing up to 32 transceivers on the bus.
- 70 mV typical receiver hysteresis.

Connection and Logic Diagrams



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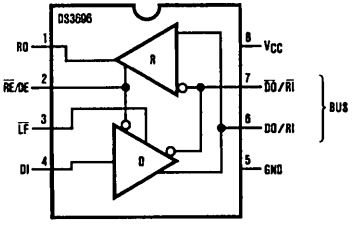
Top View



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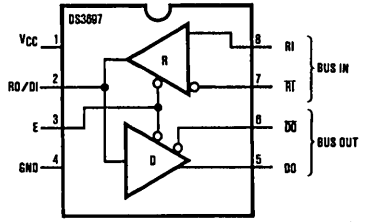
Top View



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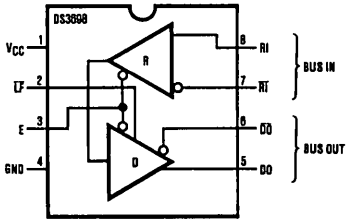
Top View



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Top View

Molded Dual-In-Line Package (N)
Order Number DS3695J, DS3696J, DS3697J, DS3698J, DS3695M, DS3696M, DS3695N, DS3696N, DS3697N, DS3698N, DS3695TN, DS3696TN, DS3695TJ or DS3696TJ
See NS Package Number M08A or N08E

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage, V_{CC}	7V
Control Input Voltages	7V
Driver Input Voltage	7V
Driver Output Voltages	+15V/−10V
Receiver Input Voltages (DS3695, DS3696)	+15V/−10V
Receiver Common Mode Voltage (DS3697, DS3698)	±25V
Receiver Output Voltage	5.5V
Continuous Power Dissipation @ 25°C	
N Package	900 mW (Note 4)
M Package	675 mW (Note 5)
Storage Temp. Range	−65°C to +150°C
Lead Temp. (Soldering 4 seconds)	260°C

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage, V_{CC}	4.75	5.25	V
Bus Voltage	−7	+12	V
Operating Free Air Temp. T_A	−40	+85	°C

Electrical Characteristics $0°C \le T_A \le 70°C$, $4.75V < V_{CC} < 5.25V$ unless otherwise specified (Notes 2 & 3)

Symbol	Parameter		Conditions		Min	Typ	Max	Units
V_{OD1}	Differential Driver Output Voltage (Unloaded)		$I_O = 0$				5	V
V_{OD2}	Differential Driver Output Voltage (with Load)		*(Figure 1)*	R = 50Ω; (RS-422) (Note 6)	2			V
				R = 27Ω; (RS-485)	1.5			V
ΔV_{OD}	Change in Magnitude of Driver Differential Output Voltage For Complementary Output States		*(Figure 1)*	R = 27Ω			0.2	V
V_{OC}	Driver Common Mode Output Voltage						3.0	V
$\Delta\lvert V_{OC}\rvert$	Change in Magnitude of Driver Common Mode Output Voltage For Complementary Output States						0.2	V
V_{IH}	Input High Voltage	DI, DE, $\overline{RE}$, E			2			V
V_{IL}	Input Low Voltage						0.8	V
V_{CL}	Input Clamp Voltage			$I_{IN} = -18$ mA			−1.5	V
I_{IL}	Input Low Current			$V_{IL} = 0.4V$			−200	µA
I_{IH}	Input High Current			$V_{IH} = 2.4V$			20	µA
I_{IN}	Input Current	DO/RI, $\overline{DO}/\overline{RI}$ RI, $\overline{RI}$	$V_{CC} = 0V$ or 5.25V DE/E = 0V	$V_{IN} = 12V$			+1.0	mA
				$V_{IN} = -7V$			−0.8	mA
I_{OZD}	TRI-STATE Current DS3697 & DS3698	DO, $\overline{DO}$	$V_{CC} = 0V$ or 5.25V, E = 0V $-7V < V_O < +12V$				±100	µA
V_{TH}	Differential Input Threshold Voltage for Receiver		$-7V \le V_{CM} \le +12V$		−0.2		+0.2	V
ΔV_{TH}	Receiver Input Hysteresis		$V_{CM} = 0V$			70		mV
V_{OH}	Receiver Output High Voltage		$I_{OH} = -400$ µA		2.4			V
V_{OL}	Output Low Voltage	RO	$I_{OL} = 16$ mA (Note 6)				0.5	V
		$\overline{LF}$	$I_{OL} = 8$ mA				0.45	V
I_{OZR}	OFF-State (High Impedance) Output Current at Receiver		V_{CC} = Max $0.4V \le V_O \le 2.4V$				±20	µA
R_{IN}	Receiver Input Resistance		$-7V \le V_{CM} \le +12V$		12			kΩ
I_{CC}	Supply Current		No Load (Note 6)	Driver Outputs Enabled		42	60	mA
				Driver Outputs Disabled		27	40	mA

Electrical Characteristics

$0°C \le T_A \le 70°C$, $4.75V < V_{CC} < 5.25V$ unless otherwise specified (Notes 2 & 3) (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{OSD}	Driver Short-Circuit Output Current	$V_O = -7V$ (Note 6)			−250	mA
		$V_O = +12V$ (Note 6)			+250	mA
I_{OSR}	Receiver Short-Circuit Output Current	$V_O = 0V$,	−15		−85	mA

Note 1. "Absolute maximum ratings" are those beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

Note 2. All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to device ground unless otherwise specified.

Note 3. All typicals are given for $V_{CC} = 5V$ and $T_A = 25°C$.

Note 4. Derate linearly at 5.56 mW/°C to 650 mW at 70°C.

Note 5. Derate linearly at 6.11 mW/°C to 400 mW at 70°C.

Note 6. All worst case parameters for which Note 6 is applied, must be increased by 10% for DS3695T and DS3696T. Other parameters remain the same for these extended temperature range devices for $-40°C < T_A < +85°C$.

Switching Characteristics $4.75V \le V_{CC} \le 5.25V$; $0°C < T_A < 70°C$ (Note 7)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PLH}	Driver Input to Output	$R_{LDIFF} = 60\Omega$, $C_{L1} = C_{L2} = 100$ pF (*Figures 3* and *5*)	9	15	22	ns
t_{PHL}	Driver Input to Output		9	15	22	ns
t_{SKEW}	Driver Output to Output		0	2	8	ns
t_r, t_f	Driver Rise or Fall Time		6	10	18	ns
t_{ZH}	Driver Enable to Output High	$C_L = 100$ pF (*Figures 4* and *6*) S1 open	30	35	50	ns
t_{ZL}	Driver Enable to Output Low	$C_L = 100$ pF (*Figures 4* and *6*) S2 open	30	35	50	ns
t_{LZ}	Driver Disable Time from Low	$C_L = 15$ pF (*Figures 4* and *6*) S2 Open	7	15	30	ns
t_{HZ}	Driver Disable Time from High	$C_L = 15$ pF (*Figures 4* and *6*) S1 Open	7	15	30	ns
t_{PLH}	Receiver Input to Output	$C_L = 15$ pF (*Figures 2* and *7*) S1 and S2 Closed	15	25	37	ns
t_{PHL}	Receiver Input to Output		15	25	37	ns
t_{ZL}	Receiver Enable to Output Low	$C_L = 15$ pF (*Figures 2* and *8*) S2 Open	7	15	20	ns
t_{ZH}	Receiver Enable to Output High	$C_L = 15$ pF (*Figures 2* and *8*) S1 Open	7	15	20	ns
t_{LZ}	Receiver Disable from Low	$C_L = 15$ pF (*Figures 2* and *8*) S2 Open	5	12	16	ns
t_{HZ}	Receiver Disable from High	$C_L = 15$ pF (*Figures 2* and *8*) S1 Open	5	12	16	ns

Note 7. Derate worst case ac parameters by 10% for DS3695T and DS3696T.

AC Test Circuits

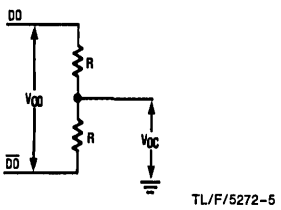

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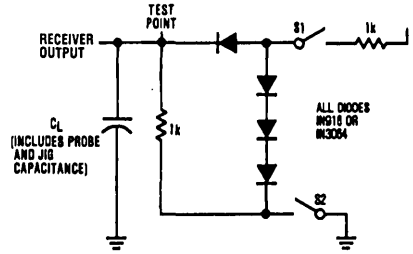
FIGURE 1



Note: S1 and S2 of load circuit are closed except as otherwise mentioned.

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FIGURE 2

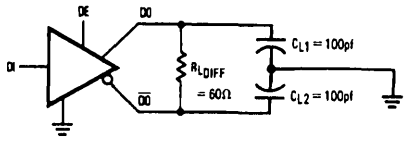

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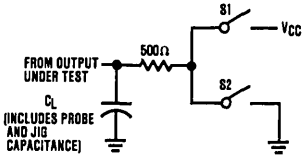
FIGURE 3



Note: Unless otherwise specified the switches are closed.

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FIGURE 4

Switching Time Waveforms

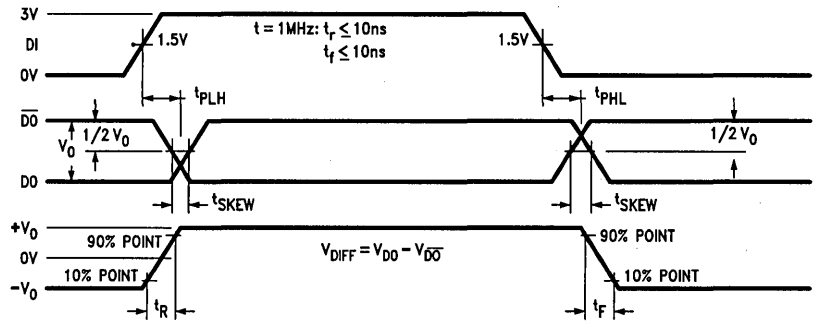

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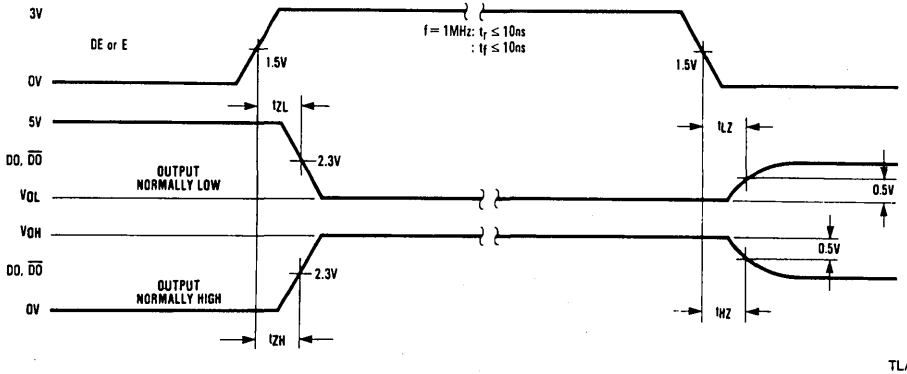
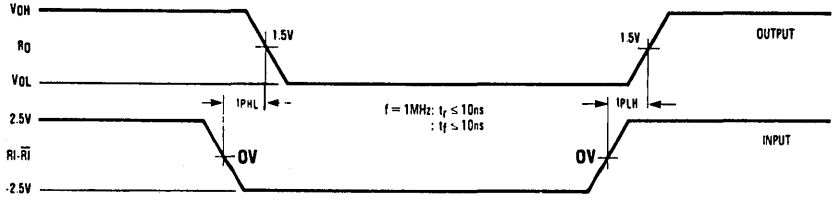
FIGURE 5. Driver Propagation Delays



TL/F/5272-10

FIGURE 6. Driver Enable and Disable Times

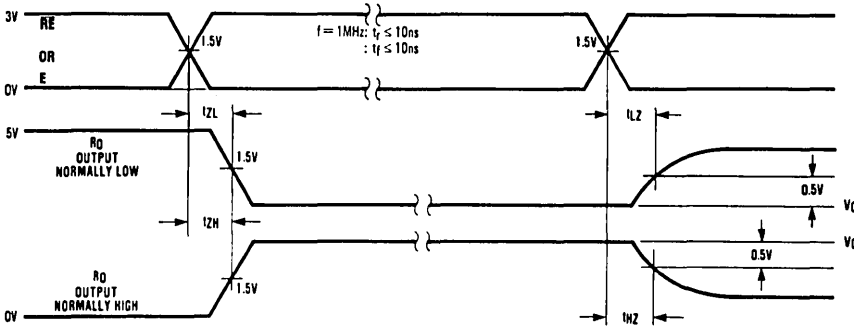


TL/F/5272-11

Note: Differential input voltage may be realized by grounding $\overline{RI}$ and pulsing RI between +2.5V and −2.5V

FIGURE 7. Receiver Propagation Delays

Switching Time Waveforms (Continued)



TL/F/5272–12

FIGURE 8. Receiver Enable and Disable Times

Function Tables

DS3695/DS3696 Transmitting

Inputs			Line Condition	Outputs		
$\overline{RE}$	DE	DI		$\overline{DO}$	DO	$\overline{LF}$* (DS3696 Only)
X	1	1	No Fault	0	1	H
X	1	0	No Fault	1	0	H
X	0	X	X	Z	Z	H
X	1	X	Fault	Z	Z	L

DS3695/DS3696 Receiving

Inputs			Outputs	
$\overline{RE}$	DE	RI–$\overline{RI}$	RO	$\overline{LF}$* (DS3696 Only)
0	0	≥ +0.2V	1	H
0	0	≤ −0.2V	0	H
0	0	Inputs Open**	1	H
1	0	X	Z	H

DS3697/DS3698

Inputs		Line Condition	Outputs			
E	RI–$\overline{RI}$		$\overline{DO}$	DO	RO/DI (DS3697 Only)	$\overline{LF}$* (DS3698 Only)
1	≥ +0.2V	No Fault	0	1	1	H
1	≤ −0.2V	No Fault	1	0	0	H
1	Open**	No Fault	0	1	1	H
0	X	X	Z	Z	Z	H
1	≥ +0.2V	Fault	Z	Z	1	L
1	≤ −0.2V	Fault	Z	Z	0	L

X — Don't care condition

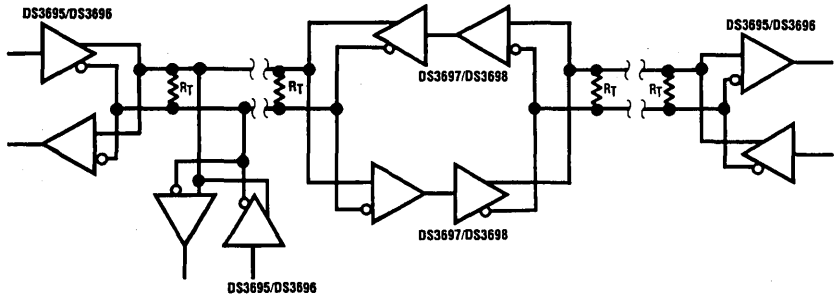
Z — High impedance state

Fault — Improper line conditions causing excessive power dissipation in the driver, such as shorts or bus contention situations

*$\overline{LF}$ is an "open collector" output with an on-chip 10 kΩ pull-up resistor

**** This is a fail safe condition**

Typical Application



TL/F/5272–13

National Semiconductor Corporation

DS55113/DS75113 Dual TRI-STATE® Differential Line Driver

General Description

The DS55113/DS75113 dual differential line drivers with TRI-STATE outputs are designed to provide all the features of the DS55114/DS75114 line drivers with the added feature of driver output controls. There are individual controls for each output pair, as well as a common control for both output pairs. When an output control is low, the associated output is in a high-impedance state and the output can neither drive nor load the bus. This permits many devices to be connected together on the same transmission line for party-line applications.

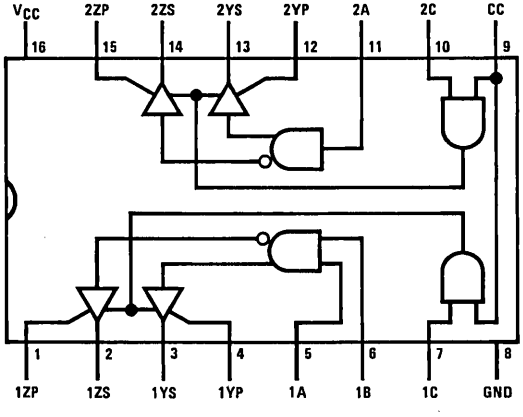
The output stages are similar to TTL totem-pole outputs, but with the sink outputs, YS and ZS, and the corresponding active pull-up terminals, YP and ZP, available on adjacent package pins.

Features

- Each circuit offers choice of open-collector or active pull-up (totem-pole) outputs
- Single 5V supply
- Differential line operation
- Dual channels
- TTL/LS compatibility
- High-impedance output state for party-line applications
- Short-circuit protection
- High current outputs
- Single-ended or differential AND/NAND outputs
- Common and individual output controls
- Clamp diodes at inputs
- Easily adaptable to DS55114/DS75114 applications

Connection Diagram

Dual-In-Line Package



Positive logic: $Y = \overline{AB}$, $Z = \overline{AB}$

Output is OFF when C or CC is low

TL/F/5785–1

Top View
Order Number DS55113J, DS75113J, DS75113M or DS75113N
See NS Package Number J16A, M16A or N16A

Truth Table

Inputs				Outputs	
Output Control		Data		AND	NAND
C	CC	A	B*	Y	Z
L	X	X	X	Z	Z
X	L	X	X	Z	Z
H	H	L	X	L	H*
H	H	X	L	L	H
H	H	H	H	H	L

H = high level
L = low level
X = irrelevant
Z = high impedance (OFF)
*B input and 4th line of truth table applicable only to driver number 1

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage (V_{CC}) (Note 1)	7V
Input Voltage	5.5V
OFF-State Voltage Applied to Open-Collector Outputs	12V
Maximum Power Dissipation* at 25°C	
Cavity Package	1433 mW
Molded DIP Package	1362 mW
SO Package	1002 mW
Operating Free-Air Temperature Range	
DS55113	−55°C to +125°C
DS75113	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (1/16" from case for 60 seconds): J Package	300 °C
Lead Temperature (1/16" from case for 4 seconds): N Package	260°C

*Derate cavity package 9.6 mW/°C above 25°C; derate molded DIP package 10.9 mW/°C above 25°C; derate SO package 8.01 mW/°C above 25°C (Note 2).

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
DS55113	4.5	5.5	V
DS75113	4.75	5.25	V
High Level Output Current (I_{OH})		−40	mA
Low Level Output Current (I_{OL})		40	mA
Operating Free-Air Temperature (T_A)			
DS55113	−55	125	°C
DS75113	0	70	°C

Electrical Characteristics Over recommended operating free-air temperature range (unless otherwise noted)

Symbol	Parameter		Conditions (Note 3)			DS55113 Min	DS55113 Typ (Note 4)	DS55113 Max	DS75113 Min	DS75113 Typ (Note 4)	DS75113 Max	Units
V_{IH}	High Level Input Voltage					2			2			V
V_{IL}	Low Level Input Voltage							0.8			0.8	V
V_{IK}	Input Clamp Voltage		V_{CC} = Min, I_I = −12 mA				−0.9	−1.5		−0.9	−1.5	V
V_{OH}	High Level Output Voltage		V_{CC} = Min, V_{IH} = 2V, V_{IL} = 0.8V		I_{OH} = −10 mA	2.4	3.4		2.4	3.4		V
					I_{OH} = −40 mA	2	3.0		2	3.0		
V_{OL}	Low Level Output Voltage		V_{CC} = Min, V_{IH} = 2V, V_{IL} = 0.8V, I_{OL} = 40 mA				0.23	0.4		0.23	0.4	V
V_{OK}	Output Clamp Voltage		V_{CC} = Max, I_O = −40 mA				−1.1	−1.5		−1.1	−1.5	V
$I_{O(off)}$	Off-State Open-Collector Output Current		V_{CC} = Max	V_{OH} = 12V	T_A = 25°C		1	10				µA
					T_A = 125°C			200				
				V_{OH} = 5.25V	T_A = 25°C					1	10	
					T_A = 70°C						20	
I_{OZ}	Off-State (High-Impedance-State) Output Current		V_{CC} = Max, Output Controls at 0.8V	T_A = 25°C, V_O = 0 to V_{CC}				±10			±10	µA
				T_A = Max	V_O = 0V			−150			−20	
					V_O = 0.4V			±80			±20	
					V_O = 2.4V			±80			±20	
					V_O = V_{CC}			80			20	
I_I	Input Current at Maximum Input Voltage	A, B, C	V_{CC} = Max, V_I = 5.5V					1			1	mA
		CC						2			2	
I_{IH}	High Level Input Current	A, B, C	V_{CC} = Max, V_I = 2.4V					40			40	µA
		CC						80			80	
I_{IL}	Low Level Input Current	A, B, C	V_{CC} = Max, V_I = 0.4V					−1.6			−1.6	mA
		CC						−3.2			−3.2	

Electrical Characteristics

Over recommended operating free-air temperature range (unless otherwise noted) (Continued)

Symbol	Parameter	Conditions (Note 3)		DS55113			DS75113			Units
				Min	Typ (Note 4)	Max	Min	Typ (Note 4)	Max	
I_{OS}	Short-Circuit Output Current (Note 5)	V_{CC} = Max, V_O = 0V		−40	−90	−120	−40	−90	−120	mA
I_{CC}	Supply Current (Both Drivers)	All Inputs at 0V, No Load T_A = 25°C	V_{CC} = Max		47	65		47	65	mA
			V_{CC} = 7V		65	85		65	85	

Note 1: All voltage values are with respect to network ground terminal.

Note 2: For operation above 25°C free-air temperature, refer to Dissipation Derating Curves in the Thermal information section.

Note 3: All parameters with the exception of OFF-state open-collector output current are measured with the active pull-up connected to the sink output.

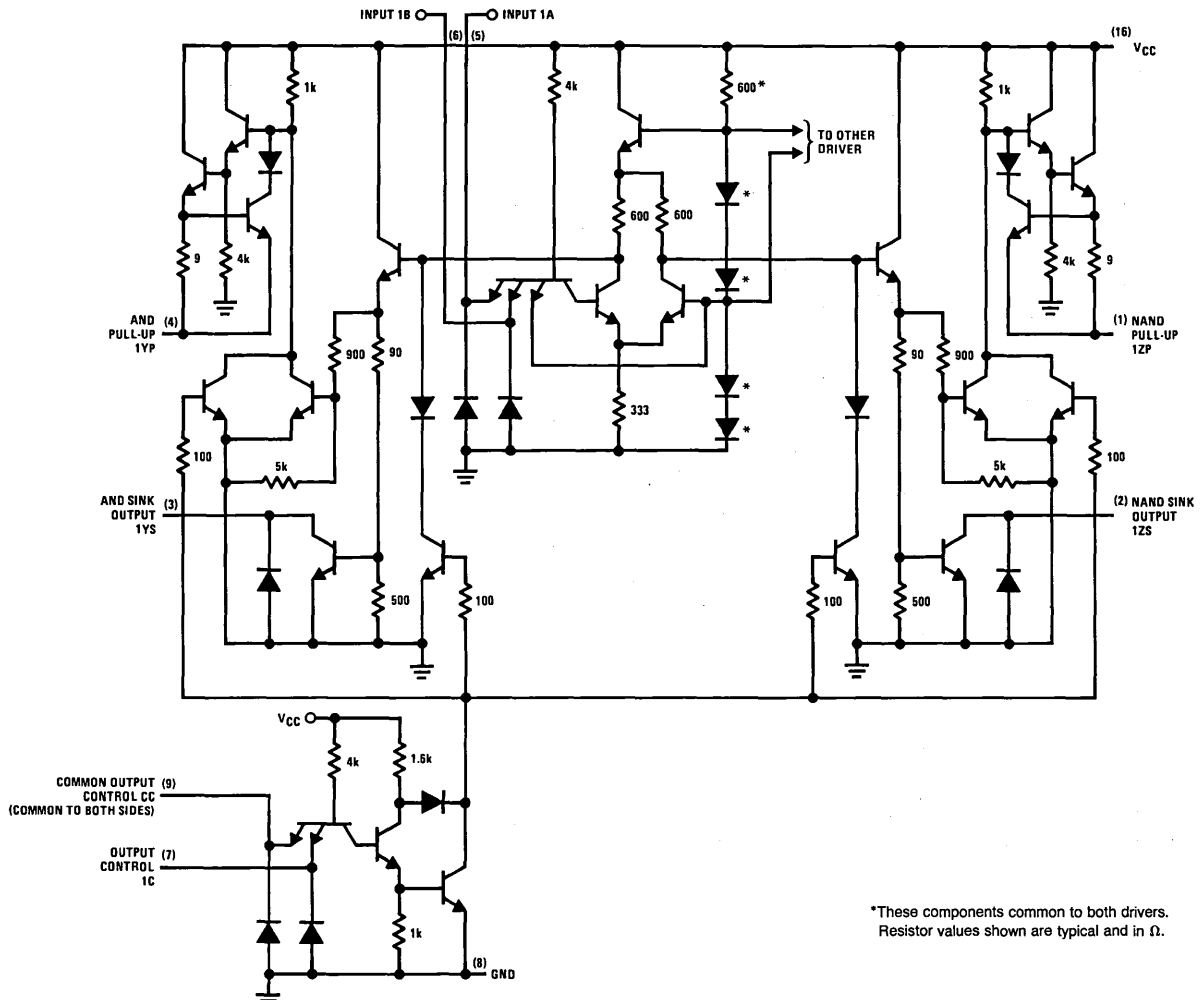
Note 4: All typical values are at T_A = 25°C and V_{CC} = 5V, with the exception of I_{CC} at 7V.

Note 5: Only one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

Switching Characteristics V_{CC} = 5V, C_L = 30 pF, T_A = 25°C

Symbol	Parameter	Conditions	DS55113			DS75113			Unit
			Min	Typ	Max	Min	Typ	Max	
t_{PLH}	Propagation Delay Time, Low-to High-Level Output	*(Figure 1)*		13	20		13	30	ns
t_{PHL}	Propagation Delay Time, High-to Low-Level Output			12	20		12	30	ns
t_{PZH}	Output Enable Time to High Level	R_L = 180Ω, *(Figure 2)*		7	15		7	20	ns
t_{PZL}	Output Enable Time to Low Level	R_L = 250Ω, *(Figure 3)*		14	30		14	40	ns
t_{PHZ}	Output Disable Time from High Level	R_L = 180Ω, *(Figure 2)*		10	20		10	30	ns
t_{PLZ}	Output Disable Time from Low Level	R_L = 250Ω, *(Figure 3)*		17	35		17	35	ns

Schematic Diagram (One side shown only)



*These components common to both drivers.
Resistor values shown are typical and in Ω.

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AC Test Circuits and Switching Time Waveforms

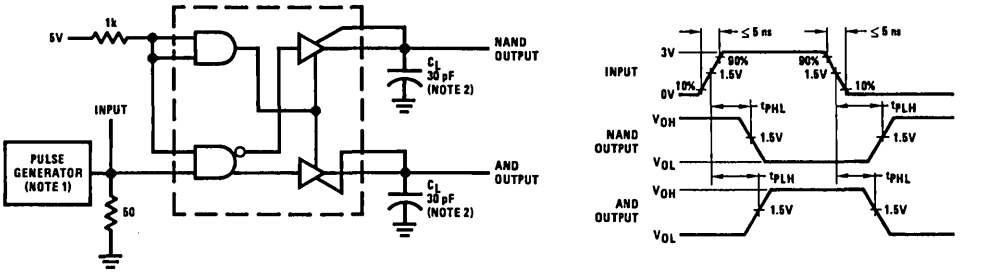

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FIGURE 1. t_{PLH} and t_{PHL}

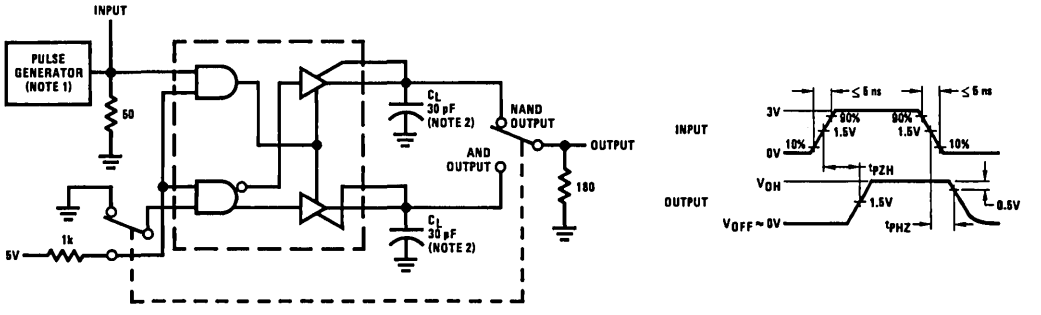

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FIGURE 2. t_{PZH} and t_{PHZ}

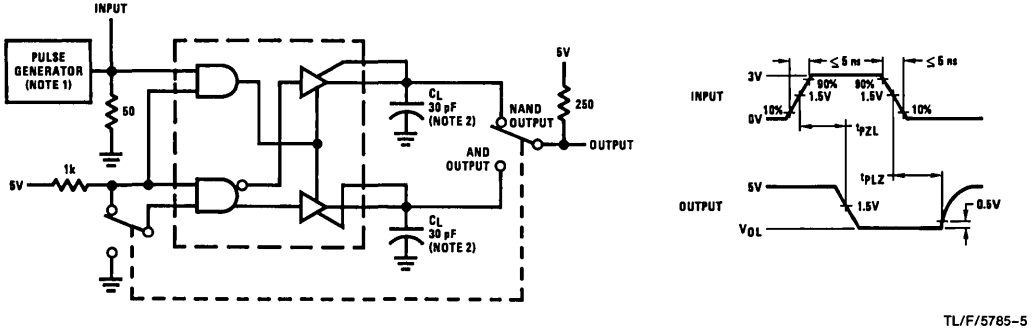

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FIGURE 3. t_{PZL} and t_{PLZ}

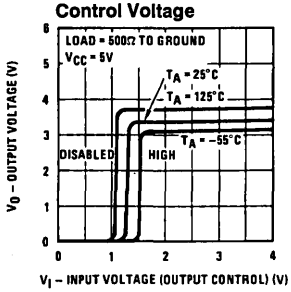
Note 1: The pulse generator has the following characteristics: $Z_{OUT} = 50\Omega$, PRR = 500 kHz, t_W = 100 ns.

Note 2: C_L includes probe and jig capacitance.

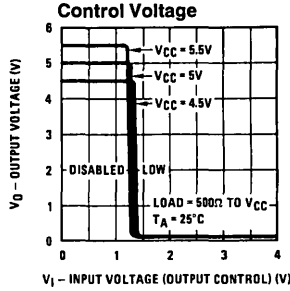
1

Typical Performance Characteristics*

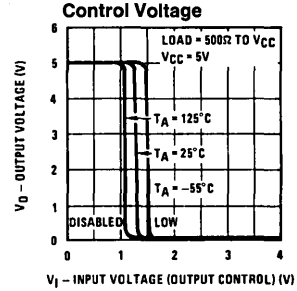
Output Voltage vs Output Control Voltage



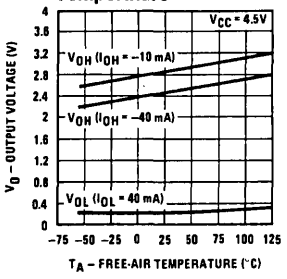
Output Voltage vs Output Control Voltage



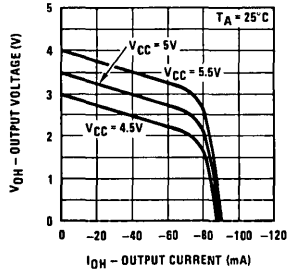
Output Voltage vs Output Control Voltage



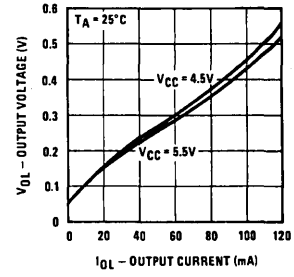
Output Voltage vs Free-Air Temperature



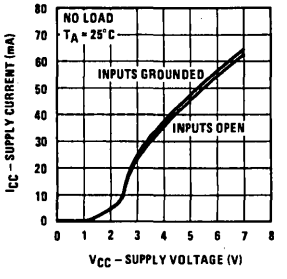
High Level Output Voltage vs Output Current



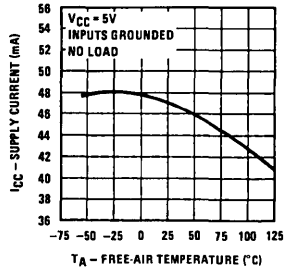
Low Level Output Voltage vs Output Current



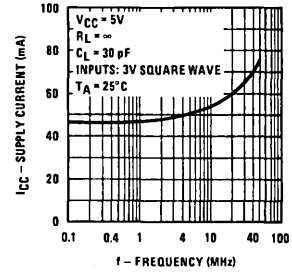
Supply Current (Both Drivers) vs Supply Voltage



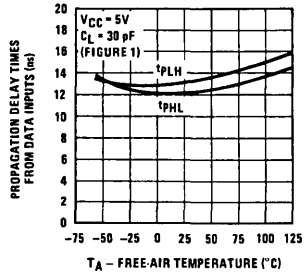
Supply Current (Both Drivers) vs Free-Air Temperature



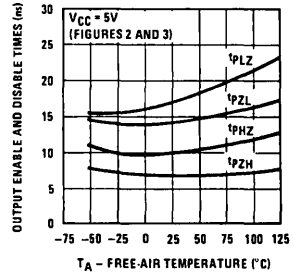
Supply Current (Both Drivers) vs Frequency



Propagation Delay Times from Data Inputs vs Free-Air Temperature



Output Enable and Disable Times vs Free-Air Temperature



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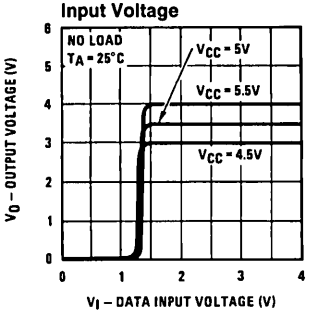
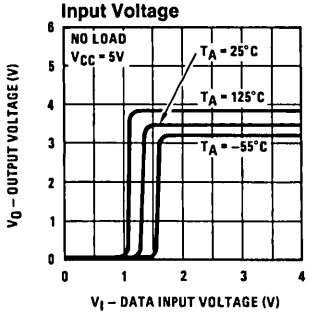
*Data for temperatures below 0°C and above 70°C and for supply voltages below 4.75V and above 5.25V are applicable to DS55113 circuits only. These parameters were measured with the active pull-up connected to the sink output.

Typical Performance Characteristics* (Continued)

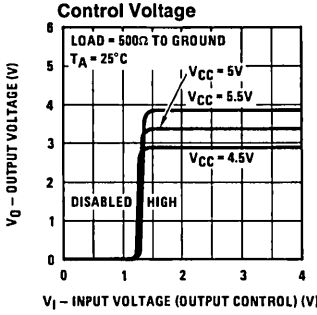
Output Voltage vs Data Input Voltage



Output Voltage vs Data Input Voltage



Output Voltage vs Output Control Voltage



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*Data for temperatures below 0°C and above 70°C and for supply voltages below 4.75V and above 5.25V are applicable to DS55113 circuits only. These parameters were measured with the active pull-up connected to the sink output.

National Semiconductor Corporation

DS55114/DS75114 Dual Differential Line Drivers

General Description

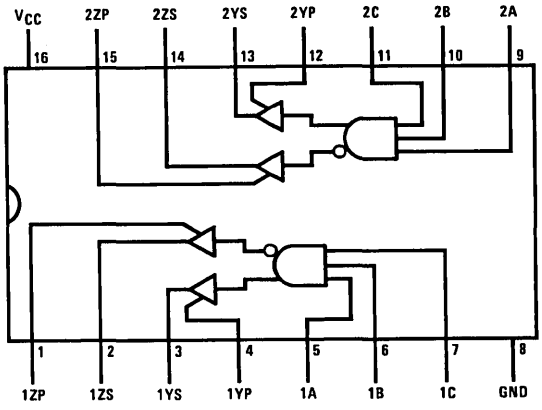
The DS55114/DS75114 dual differential line drivers are designed to provide differential output signals with high current capability for driving balanced lines, such as twisted pair at normal line impedances, without high power dissipation. The output stages are similar to TTL totem-pole outputs, but with the sink outputs, YS and ZS, and the corresponding active pull-up terminals, YP and ZP, available on adjacent package pins. Since the output stages provide TTL compatible output levels, these devices may also be used as TTL expanders or phase splitters.

Features

- Each circuit offers choice of open-collector or active pull-up (totem-pole) outputs
- Single 5V supply
- Differential line operation
- Dual channels
- TTL/LS compatibility
- Design to be interchangeable with Fairchild 9614 line drivers
- Short-circuit protection of outputs
- High current outputs
- Clamp diodes at inputs and outputs to terminate line transients
- Single-ended or differential AND/NAND outputs
- Triple inputs

Connection Diagram

Dual-In-Line Package



TL/F/5786–1

Top View

Positive logic: Y = ABC

Z = $\overline{ABC}$

Order Number DS55114J, DS75114J, or DS75114N
See NS Package Number J16A or N16A

Truth Table

Inputs			Outputs	
A	B	C	Y	Z
H	H	H	H	L
All Other Input Combinations			L	H

H = high level

L = low level

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage (V_{CC})	7V
Input Voltage	5.5V
OFF-State Voltage Applied to Open-Collector Outputs	12V
Maximum Power Dissipation* at 25°C	
Cavity Package	1433 mW
Molded Package	1362 mW
Operating Free-Air Temperature Range	
DS55114	−55°C to +125°C
DS75114	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature ($1/16$" from case for 60 seconds): J Package	300°C
Lead Temperature ($1/16$" from case for 4 seconds): N Package	260°C

*Derate cavity package 9.6 mW/°C above 25°C; derate molded package 10.9 mW/°C above 25°C (Note 2).

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
DS55114	4.5	5.5	V
DS75114	4.75	5.25	V
High Level Output Current (I_{OH})		−40	mA
Low Level Output Current (I_{OL})		40	mA
Operating Free-Air Temperature (T_A)			
DS55114	−55	125	°C
DS75114	0	70	°C

Electrical Characteristics Over recommended operating free-air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions (Note 3)			DS55114 Min	DS55114 Typ (Note 4)	DS55114 Max	DS75114 Min	DS75114 Typ (Note 4)	DS75114 Max	Units
V_{IH}	High Level Input Voltage				2			2			V
V_{IL}	Low Level Input Voltage						0.8			0.8	V
V_{IK}	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−0.9	−1.5		−0.9	−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IH} = 2V		I_{OH} = −10 mA	2.4	3.4		2.4	3.4		V
		V_{IL} = 0.8V		I_{OH} = −40 mA	2	3.0		2	3.0		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = 0.8V, I_{OL} = 40 mA				0.2	0.4		0.2	0.45	V
V_{OK}	Output Clamp Voltage	V_{CC} = 5V, I_O = 40 mA, T_A = 25°C				6.1	6.5		6.1	6.5	V
		V_{CC} = Max, I_O = −40 mA, T_A = 25°C				−1.1	−1.5		−1.1	−1.5	V
$I_{O(off)}$	OFF-State Open-Collector Output Current	V_{CC} = Max	V_{OH} = 12V	T_A = 25°		1	100				μA
				T_A = 125°C			200				μA
			V_{OH} = 5.25V	T_A = 25°C					1	100	μA
				T_A = 70°C						200	μA
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5V					1			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V					40			40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.1	−1.6		−1.1	−1.6	mA
I_{OS}	Short-Circuit Output Current (Note 5)	V_{CC} = Max, V_O = 0V			−40	−90	120	−40	−90	−120	mA
I_{CC}	Supply Current (Both Drivers)	Inputs Grounded, No Load, T_A = 25°C		V_{CC} = Max		37	50		37	50	mA
				V_{CC} = 7V		47	65		47	70	mA

Note 1: All voltage values are with respect to network ground terminal.

Note 2: For operation above 25°C free-air temperature, refer to Dissipation Derating Curves in the Thermal information section.

Note 3: All parameters, with the exception of OFF-state open-collector output current, are measured with the active pull-up connected to the sink output.

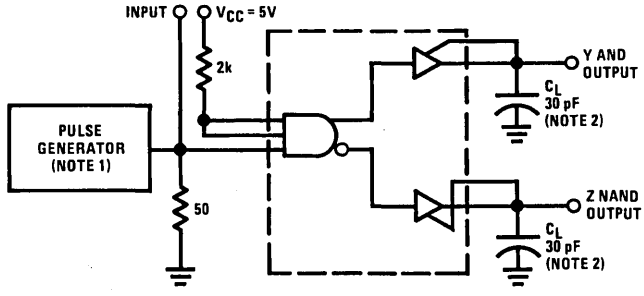
Note 4: All typical values are at T_A = 25°C and V_{CC} = 5V, with the exception of I_{CC} at 7V.

Note 5: Only one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

Switching Characteristics V_{CC} = 5V, T_A = 25°C

Symbol	Parameter	Conditions	DS55114			DS75114			Units
			Min	Typ	Max	Min	Typ	Max	
t_{PLH}	Propagation Delay Time, Low-to-High-Level Output	C_L = 30 pF, *(Figure 1)*		15	20		15	30	ns
t_{PHL}	Propagation Delay Time High-to-Low-Level Output			11	20		11	30	ns

AC Test Circuit and Switching Time Waveforms



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Note 1: The pulse generator has the following characteristics: Z_{OUT} = 50Ω, t_w = 100 ns, PRR = 500 kHz.

Note 2: C_L includes probe and jig-capacitance.

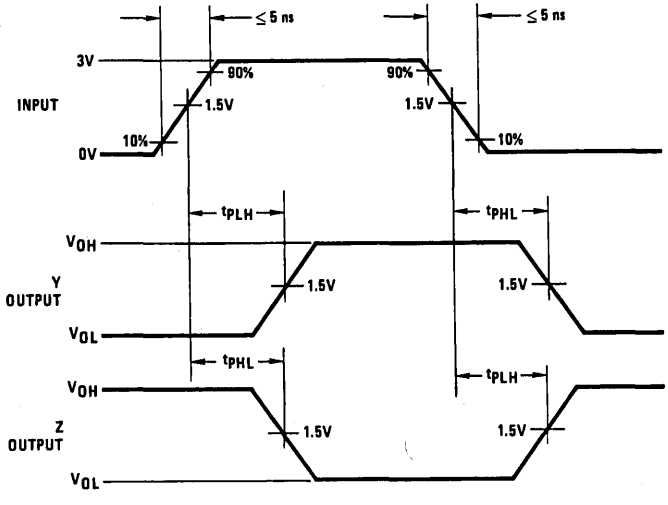

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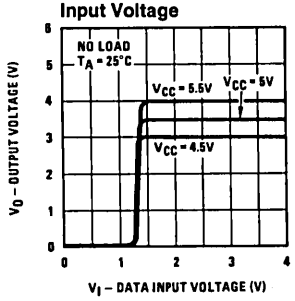
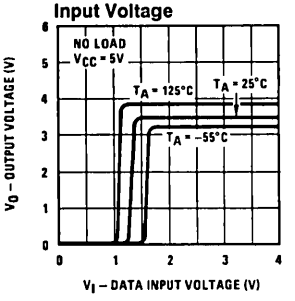
FIGURE 1

Typical Performance Characteristics*

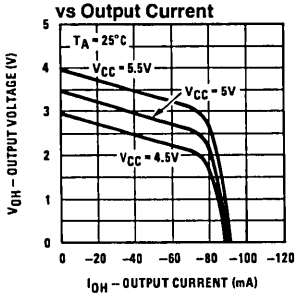
Output Voltage vs Data Input Voltage



Output Voltage vs Data Input Voltage



High Level Output Voltage vs Output Current



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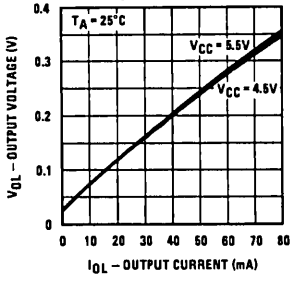
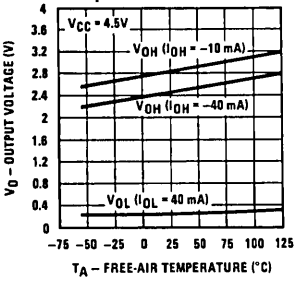
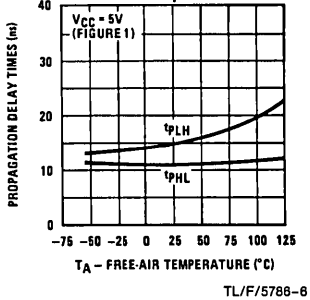
Low Level Output Voltage vs Output Current



Output Voltage vs Free-Air Temperature



Propagation Delay Times vs Free-Air Temperature



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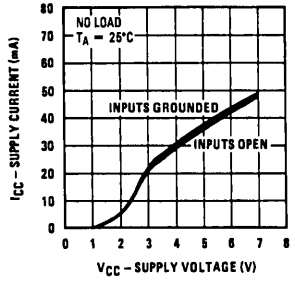
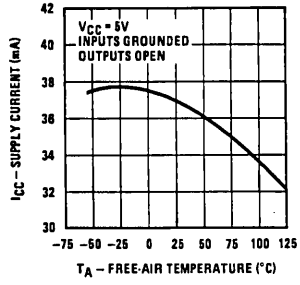
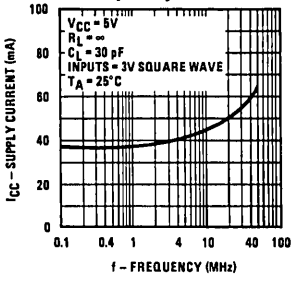
Supply Current (Both Drivers) vs Supply Voltage



Supply Current (Both Drivers) vs Free-Air Temperature



Supply Current (Both Drivers) vs Frequency



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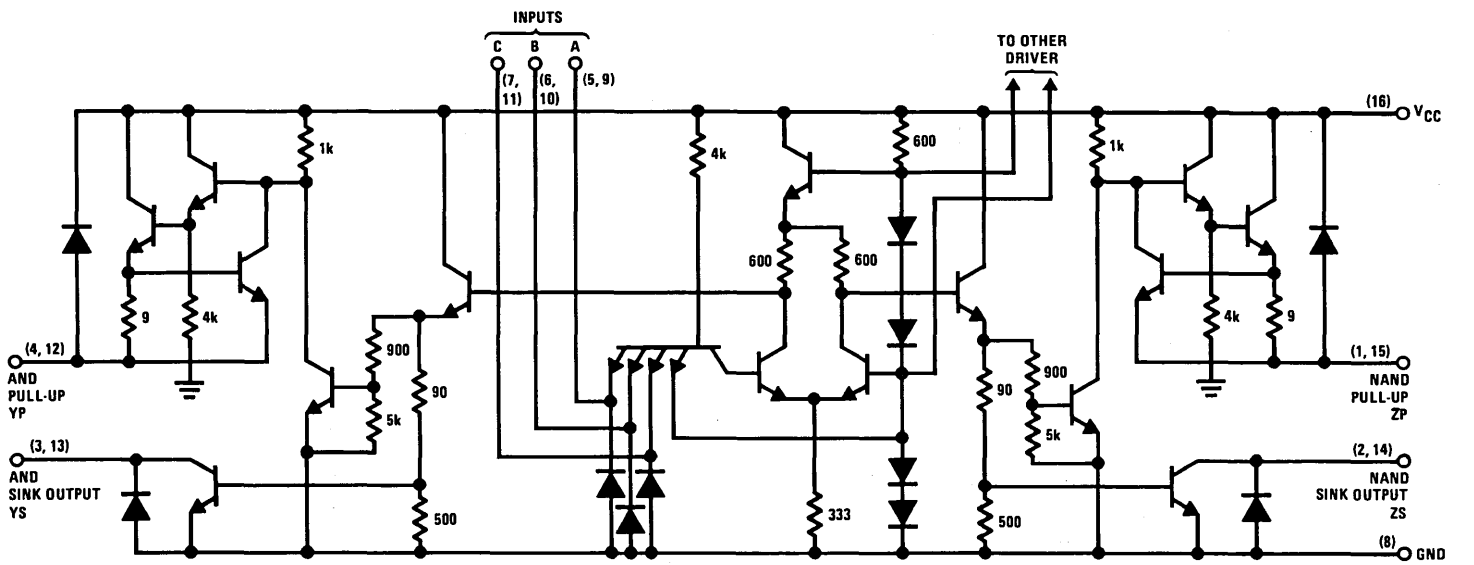
*Data for temperatures below 0°C and above 70°C and for supply voltages below 4.75V and above 5.25V are applicable to DS55114 circuits only. These parameters were measured with the active pull-up connected to the sink output.

1

Schematic Diagram (Each Driver)



Resistor values shown are typical and in ohms.

TL/F/5786–2

National Semiconductor Corporation

DS55115/DS75115 Dual Differential Line Receiver

General Description

The DS55115/DS75115 is a dual differential line receiver designed to sense differential signals from data transmission lines. Designed for operation over military and commercial temperature ranges, the DS55115/DS75115 can typically receive ±500 mV differential data with ±15V common-mode noise. Outputs are open-collector and give TTL compatible signals which are a function of the polarity of the differential input signal. Active output pull-ups are also available, offering the option of an active TTL pull-up through an external connection.

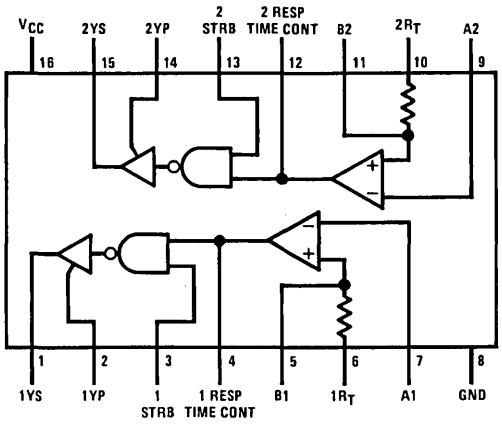
Response time may be controlled with the use of an external capacitor. Each channel may be independently controlled and optional input termination resistors are also available.

Features

- Single 5V supply
- High common-mode voltage range
- Each channel individually strobed
- Independent response time control
- Uncommitted collector or active pull-up option
- TTL compatible output
- Optional 130Ω termination resistors
- Direct replacement for 9615

Connection Diagram

Dual-In-Line Package



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Top View

Order Number DS55115J, DS75115J or DS75115N
See NS Package Number J16A or N16A

Function Table

Strobe	Diff. Input	Output
L	X	H
H	L	H
H	H	L

H = $V_I \geq V_{IH}$ min or V_{ID} more positive than V_{TH} max
L = $V_I \leq V_{IL}$ max or V_{ID} more negative than V_{TL} max
X = irrelevant

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage, V_{CC} (Note 1) 7V

Input Voltage at A, B and R_T Inputs ±25V

Input Voltage at Strobe Input 5.5V

Off-State Voltage Applied to Open-Collector Outputs 14V

Maximum Power Dissipation* at 25°C

Cavity Package 1433 mW

Molded Package 1362 mW

Operating Free-Air Temperature Range

DS55115 −55°C to +125°C

DS57115 0°C to +70°C

Storage Temperature Range −65°C to +150°C

Lead Temperature

($1/16$ inch from case for 4 seconds) 260°C

*Derate cavity package 9.6 mW/°C above 25°C; derate molded package 10.9 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage, (V_{CC})			
DS55115	4.5	5.5	V
DS75115	4.75	5.25	V
High Level Output Current (I_{OH})		−5	mA
Low Level Output Current (I_{OL})		15	mA
Operating Temperature (T_A)			
DS55115	−55	125	°C
DS75115	0	70	°C

Electrical Characteristics (Notes 2, 3 and 5)

Symbol	Parameter	Conditions		DS55115			DS75115			Units
				Min	Typ	Max	Min	Typ	Max	
V_{TH}	Differential Input High-Threshold Voltage	V_O = 0.4V, I_{OL} = 15 mA, V_{IC} = 0			200	500		200	500	mV
V_{TL}	Differential Input Low-Threshold Voltage	V_O = 2.4V, I_{OH} = −5 mA, V_{IC} = 0			−200	−500		−200	−500	mV
V_{ICR}	Common-Mode Input Voltage Range	V_{ID} = ±1V		15 to −15	24 to −19		15 to −15	24 to −19		V
$V_{IH(STROBE)}$	High-Level Strobe Input Voltage			2.4			2.4			V
$V_{IL(STROBE)}$	Low-Level Strobe Input Voltage					0.4			0.4	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{ID} = −0.5V, I_{OH} = −5 mA	T_A = Min	2.2			2.4			V
			T_A = 25°C	2.4	3.4		2.4	3.4		
			T_A = Max	2.4			2.4			
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{ID} = 0.5V, I_{OL} = 15 mA			0.22	0.4		0.22	0.45	V
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V, Other Input at 5.5V	T_A = Min			−0.9			−0.9	mA
			T_A = 25°C		−0.5	−0.7		−0.5	−0.7	
			T_A = Max			−0.7			−0.7	
I_{SH}	High Level Strobe Current	V_{CC} = Min, V_{ID} = −0.5V, V_{STROBE} = 4.5V	T_A = 25°C		0.5	2		0.5	5	µA
			T_A = Max			5			10	
I_{SL}	Low Level Strobe Current	V_{CC} = Max, V_{ID} = 0.5V, V_{STROBE} = 0.4V	T_A = 25°C		−1.15	−2.4		−1.15	−2.4	mA
I_4, I_{12}	Response Time Control Current (Pin 4 or Pin 12)	V_{CC} = Max. V_{ID} = 0.5V, V_{RC} = 0	T_A = 25°C	−1.2	−3.4		−1.2	−3.4		mA
$I_{O(OFF)}$	Off-State Open-Collector Output Current	V_{CC} = Min, V_{OH} = 12V, V_{ID} = −4.5V	T_A = 25°C			100				µA
			T_A = Max			200				
		V_{CC} = Min, V_{OH} = 5.25V, V_{ID} = −4.75V	T_A = 25°C						100	
			T_A = Max						200	

Electrical Characteristics (Notes 2, 3 and 5) (Continued)

Symbol	Parameter	Conditions		DS55115			DS75115			Units
				Min	Typ	Max	Min	Typ	Max	
R_T	Line Terminating Resistance	V_{CC} = 5V	T_A = 25°C	77	130	167	74	130	179	Ω
I_{OS}	Short-Circuit Output Current	V_{CC} = Max, V_O = 0V, V_{ID} = −0.5V, (Note 4)	T_A = 25°C	−15	−40	−80	−14	−40	−100	mA
I_{CC}	Supply Current (Both Receivers	V_{CC} = Max, V_{ID} = 0.5V, V_{IC} = 0V	T_A = 25°C		32	50		32	50	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for the actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS55115 and across the 0°C to +70°C range for the DS75115. All typical values are for T_A = 25°C, V_{CC} = 5V and V_{CM} = 0V.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

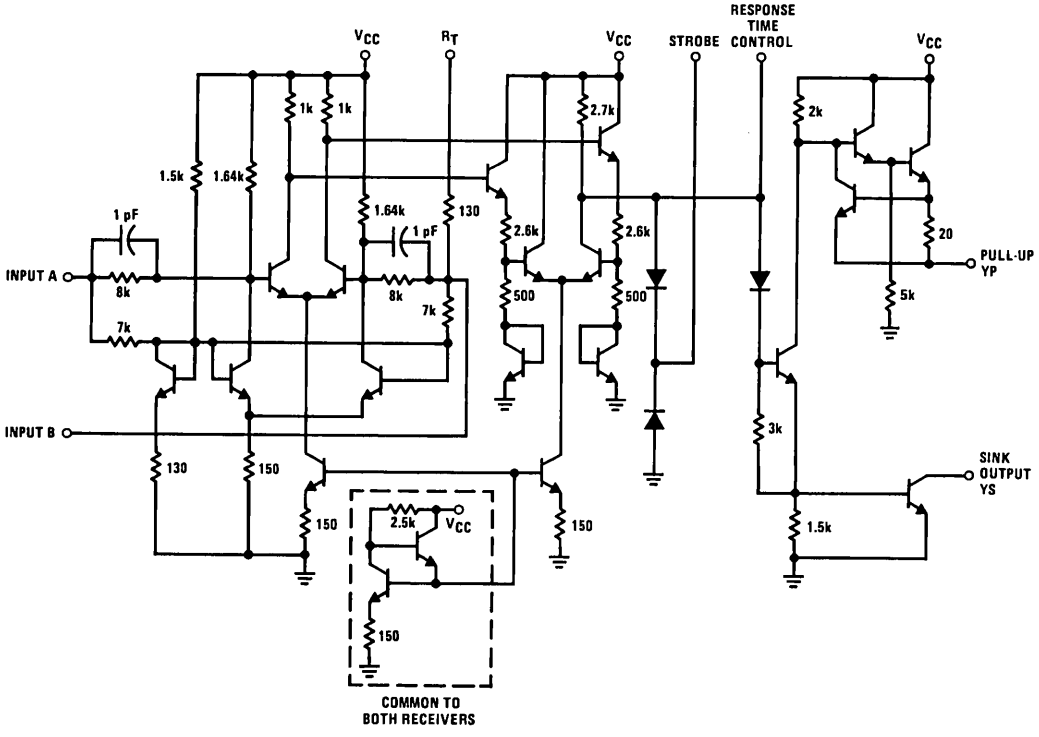
Note 4: Only one output at a time should be shorted.

Note 5: Unless otherwise noted, V_{STROBE} = 2.4V. All parameters with the exception of off-state open-collector output current are measured with the active pull-up connected to the sink output.

Switching Characteristics V_{CC} = 5V, C_L = 30 pF, T_A = 25°C

Symbol	Parameter	Conditions	DS55115			DS75115			Units
			Min	Typ	Max	Min	Typ	Max	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	R_L = 3.9 kΩ, *(Figure 1)*		18	50		18	75	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	R_L = 390Ω, *(Figure 1)*		20	50		20	75	ns

Schematic Diagram



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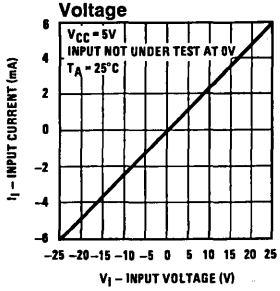
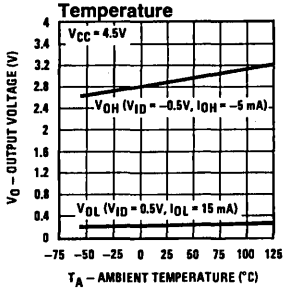
Typical Performance Characteristics (Note 3)

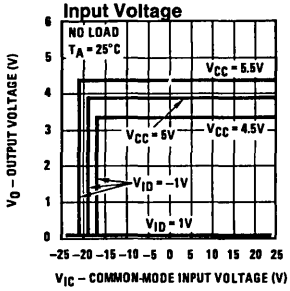
Input Current vs Input Voltage



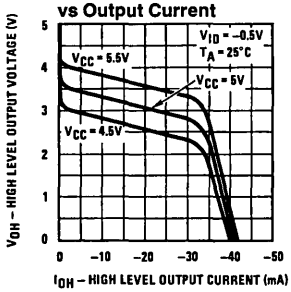
Output Voltage vs Temperature



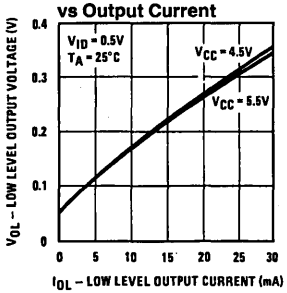
Output Voltage vs Common-Mode Input Voltage



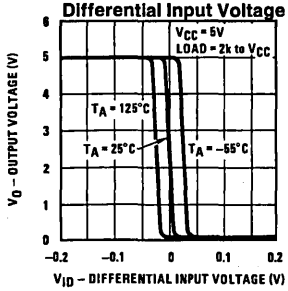
High Level Output Voltage vs Output Current



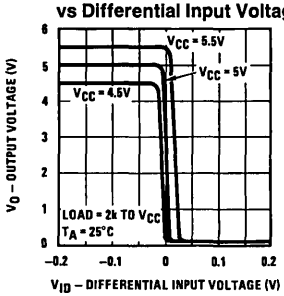
Low Level Output Voltage vs Output Current



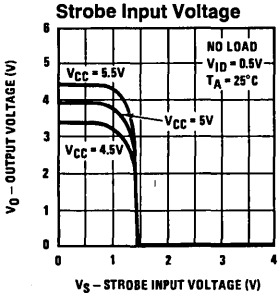
Output Voltage vs Differential Input Voltage



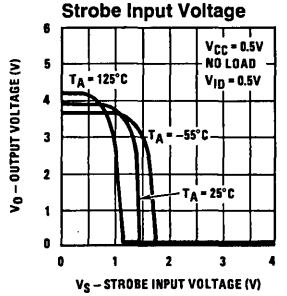
Output Voltage vs Differential Input Voltage



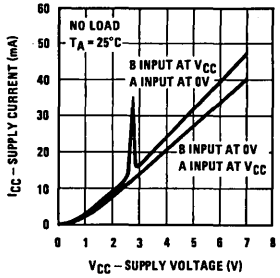
Output Voltage vs Strobe Input Voltage



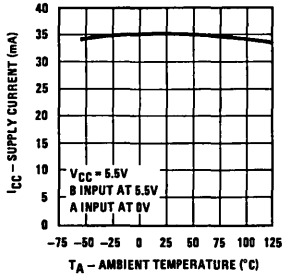
Output Voltage vs Strobe Input Voltage



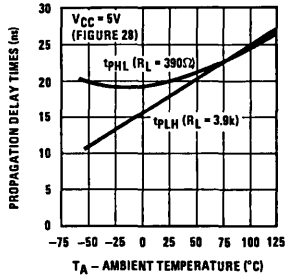
Supply Current (Both Receivers) vs Supply Voltage



Supply Current (Both Receivers) vs Temperature



Propagation Delay Times vs Temperature



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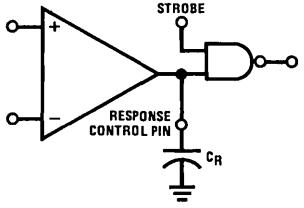
Frequency Response Control



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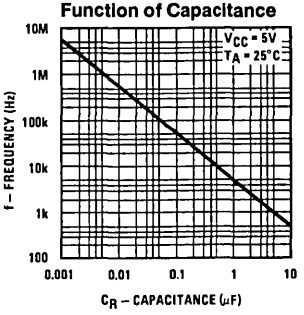
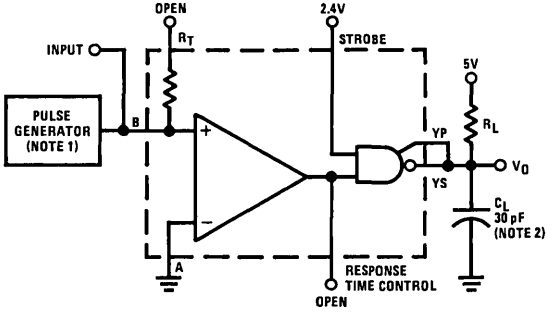
Note: C_R (response control) > 0.01 μF may cause slowing of rise and fall times of the output.

Frequency Response as a Function of Capacitance



TL/F/5787–6

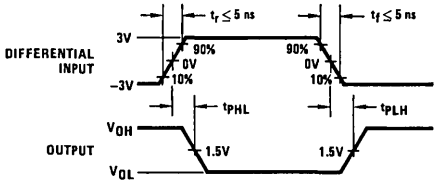
AC Test Circuit and Switching Time Waveforms



TL/F/5787–7

Note 1: The pulse generator has the following characteristics: Z_{OUT} = 50Ω, PRR = 500 kHz/t_W = 100 ns

Note 2: C_L includes probe and test fixture capacitance

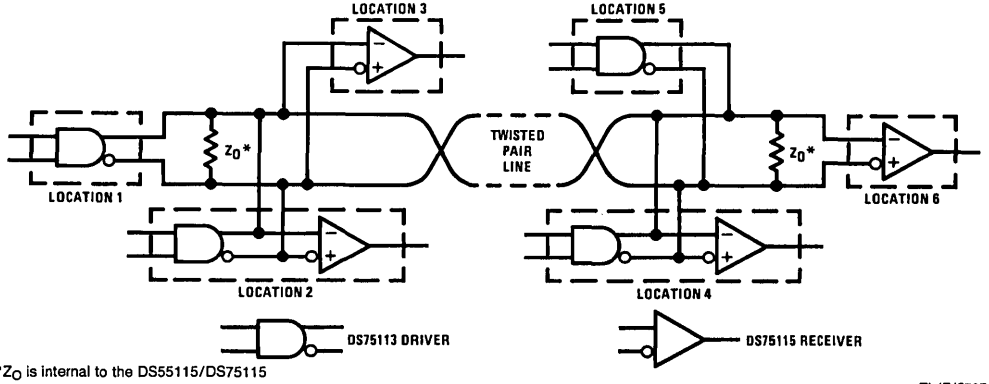


TL/F/5787–8

FIGURE 1. Propagation Delay Time

Typical Application

Basic Party-Line or Data-Bus Differential Data Transmission



*Z_O is internal to the DS55115/DS75115

A capacitor may be connected in series with Z_O to reduce power dissipation.

TL/F/5787–3

National Semiconductor Corporation

DS55121/DS75121 Dual Line Drivers

General Description

The DS55121/DS75121 are monolithic dual line drivers designed to drive long lengths of coaxial cable, strip line, or twisted pair transmission lines having impedances from 50Ω to 500Ω. Both are compatible with standard TTL logic and supply voltage levels.

The DS55121/DS75121 will drive terminated low impedance lines due to the low-impedance emitter-follower outputs. In addition the outputs are uncommitted allowing two or more drivers to drive the same line.

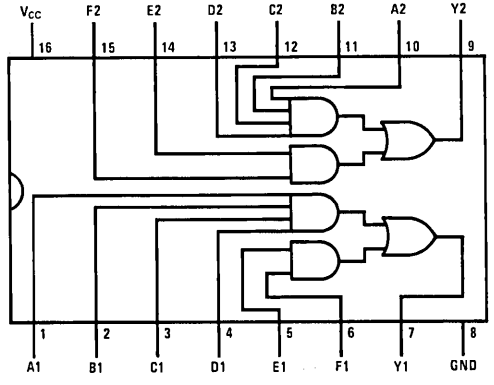
Output short-circuit protection is incorporated to turn off the output when the output voltage drops below approximately 1.5V.

Features

- Designed for digital data transmission over 50Ω to 500Ω coaxial cable, strip line, or twisted pair transmission lines
- TTL compatible
- Open emitter-follower output structure for party-line operation
- Short-circuit protection
- AND-OR logic configuration
- High speed (max propagation delay time 20 ns)
- Plug-in replacement for the SN55121/SN75121 and the 8T13

Connection Diagram

Dual-In-Line Package

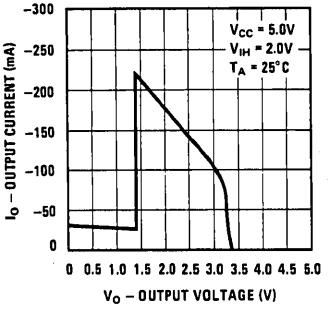


TL/F/5788-1

Top View
Order Number DS55121J, DS75121J or DS75121N
See NS Package Number J16A or N16A

Typical Performance Characteristics

Output Current vs Output Voltage



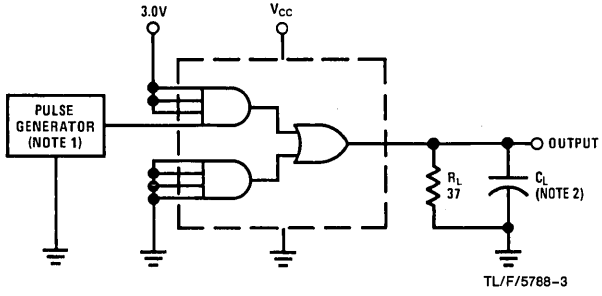
TL/F/5788-2

Truth Table

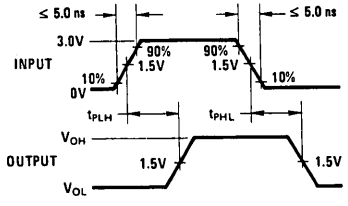
Inputs						Output
A	B	C	D	E	F	Y
H	H	H	H	X	X	H
X	X	X	X	H	H	H
All Other Input Combinations						L

H = High Level, L = Low Level, X = Irrelevant

AC Test Circuit and Switching Time Waveforms



TL/F/5788-3



TL/F/5788-4

Note 1: The pulse generators have the following characteristics:
$Z_{OUT} \approx 50\Omega$, t_W = 200 ns, duty cycle = 50%, t_r = t_f = 5.0 ns.

Note 2: C_L includes probe and jig capacitance.

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage, V_{CC}	6.0V
Input Voltage	6.0V
Output Voltage	6.0V
Output Current	−75 mA
Maximum Power Dissipation* at 25°C	
Cavity Package	1371 mW
Molded Package	1280 mW
Lead Temperature (Soldering, 4 seconds)	260°C

*Derate cavity package 9.1 mW/°C above 25°C; derate molded package 10.2 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage, V_{CC}	4.75	5.25	V
Temperature, T_A			
DS55121	−55	+125	°C
DS75121	0	+75	°C

Electrical Characteristics V_{CC} = 4.75V to 5.25V (unless otherwise noted) (Notes 2 and 3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	High Level Input Voltage		2.0			V
V_{IL}	Low Level Input Voltage				0.8	V
V_I	Input Clamp Voltage	V_{CC} = 5.0V, I_I = −12 mA			−1.5	V
I_I	Input Current at Max Input Voltage	V_{CC} = 5.25V, V_{IN} = 5.5V			1	mA
V_{OH}	High Level Output Voltage	V_{IH} = 2.0V, I_{OH} = −75 mA (Note 4)	2.4			V
I_{OH}	High Level Output Current	V_{CC} = 5.0V, V_{IH} = 4.75V, V_{OH} = 2.0V, T_A = 25°C (Note 4)	−100		−250	mA
I_{OL}	Low Level Output Current	V_{IL} = 0.8V, V_{OL} = 0.4V (Note 4)			−800	μA
$I_{O(OFF)}$	Off State Output Current	V_{CC} = 0V, V_O = 3.0V			500	μA
I_{IH}	High Level Input Current	V_I = 4.5V			40	μA
I_{IL}	Low Level Input Current	V_I = 0.4V	−0.1		−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = 5.0V, T_A = 25°C			−30	mA
I_{CCH}	Supply Current, Outputs High	V_{CC} = 5.25V, All Inputs at 2.0V, Outputs Open			28	mA
I_{CCL}	Supply Current, Outputs Low	V_{CC} = 5.25V, All Inputs at 0.8V, Outputs Open			60	mA

Switching Characteristics V_{CC} = 5.0V, T_A = 25°C

Symbol	Parameter	Conditions		Min	Typ	Max	Units
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	R_L = 37Ω, (See AC Test Circuit and Switching Time Waveforms)	C_L = 15 pF		11	20	ns
			C_L = 1000 pF		22	50	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	R_L = 37Ω, (See AC Test Circuit and Switching Time Waveforms)	C_L = 15 pF		8.0	20	ns
			C_L = 1000 pF		20	50	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS55121 and across the 0°C to +70°C range for the DS75121. All typical values are for T_A = 25°C and V_{CC} = 5V.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: The output voltage and current limits are guaranteed for any appropriate combination of high and low inputs specified by the truth table for the desired output.

National Semiconductor Corporation

DS75123 Dual Line Driver

General Description

The DS75123 is a monolithic dual line driver designed specifically to meet the I/O interface specifications for IBM System 360. It is compatible with standard TTL logic and supply voltage levels.

The low-impedance emitter-follower outputs of the DS75123 enable driving terminated low impedance lines. In addition the outputs are uncommitted allowing two or more drivers to drive the same line.

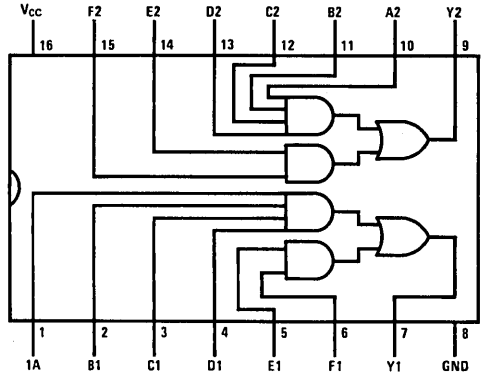
Output short-circuit protection is incorporated to turn off the output when the output voltage drops below approximately 1.5V.

Features

- Meet IBM System 360 I/O interface specifications for digital data transmission over 50Ω to 500Ω coaxial cable, strip line, or terminated pair transmission lines
- TTL compatible with single 5.0V supply
- 3.11V output at $I_{OH} = -59.3$ mA
- Open emitter-follower output structure for party-line operation
- Short circuit protection
- AND-OR logic configuration
- Plug-in replacement for the SN75123 and the 8T23

Connection Diagram

Dual-In-Line Package



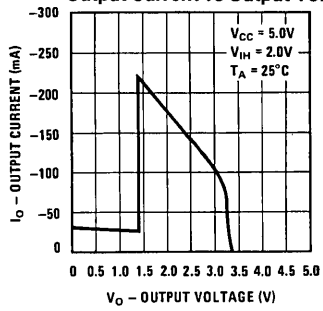
TL/F/5790-1

Top View

Order Number DS75123J or DS75123N
See NS Package Number J16A or N16A

Typical Performance Characteristics

Output Current vs Output Voltage



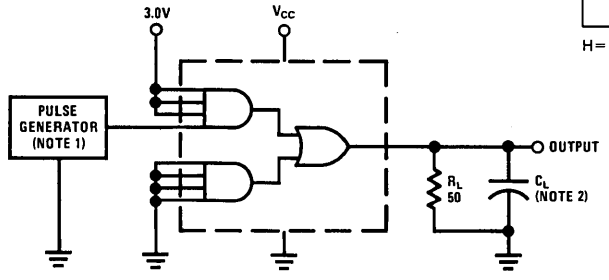
TL/F/5790-3

Truth Table

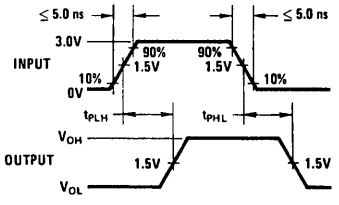
INPUTS						OUTPUT
A	B	C	D	E	F	Y
H	H	H	H	X	X	H
X	X	X	X	H	H	H
All Other Input Combinations						L

H = High level, L = Low level, X = Irrelevant

AC Test Circuit and Switching Time Waveforms



TL/F/5790-2



TL/F/5790-4

Note 1: The pulse generators have the following characteristics: $Z_{OUT} \approx 50\Omega$, $t_W = 200$ ns, duty cycle = 50%.

Note 2: C_L includes probe and jig capacitance.

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage, V_{CC}	7.0V
Input Voltage	5.5V
Output Voltage	7.0V
Maximum Power Dissipation* at 25°C	
Cavity Package	1371 mW
Molded Package	1280 mW
Operating Free-Air Temperature Range	0°C to +75°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 4 seconds)	260°C

*Derate cavity package 9.1 mW/°C above 25°C; derate molded package 10.2 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage, V_{CC}	4.75	5.25	V
High Level Output Current, I_{OH}		−100	mA
Temperature, T_A	0	+75	°C

Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IH}	High Level Input Voltage			2.0			V
V_{IL}	Low Level Input Voltage					0.8	V
V_I	Input Clamp Voltage	V_{CC} = 5.0V, I_I = −12 mA				−1.5	V
I_I	Input Current at Max Input Voltage	V_{CC} = 5.25V, V_{IN} = 5.5V				1	mA
V_{OH}	High Level Output Voltage	V_{CC} = 5.0V, V_{IH} = 2.0V, I_{OH} = −59.3 mA, (Note 4)	T_A = 25°C	3.11			V
			T_A = 0°C to +75°C	2.9			V
I_{OH}	High Level Output Current	V_{CC} = 5.0V, V_{IH} = 4.5V, T_A = 25°C, V_{OH} = 2.0V, (Note 4)		−100		−250	mA
V_{OL}	Low Level Output Voltage	V_{IL} = 0.8V, I_{OL} = −240 μA, (Note 4)				0.15	V
$I_{O(OFF)}$	Off State Output Current	V_{CC} = 0, V_O = 3.0V				40	μA
I_{IH}	High Level Input Current	V_I = 4.5V				40	μA
I_{IL}	Low Level Input Current	V_I = 0.4V		−0.1		−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = 5.0V, T_A = 25°C				−30	mA
I_{CCH}	Supply Current, Outputs High	V_{CC} = 5.25V, All Inputs at 2.0V, Outputs Open				28	mA
I_{CCL}	Supply Current, Outputs Low	V_{CC} = 5.25V, All Inputs at 0.8V, Outputs Open				60	mA

Switching Characteristics V_{CC} = 5.0V, T_A = 25°C

Symbol	Parameter	Conditions		Min	Typ	Max	Units
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	R_L = 50Ω, (See AC Test Circuit and Switching Time Waveforms	C_L = 15 pF		12	20	ns
			C_L = 100 pF		20	35	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	R_L = 50Ω, (See AC Test Circuit and Switching Time Waveforms	C_L = 15 pF		12	20	ns
			C_L = 100 pF		15	25	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All currents into device pins are shown as positive, currents out of device pins shown as negative, all voltage values are referenced with respect to network ground terminal, unless otherwise noted. All values shown as max or min on absolute value basis.

Note 3: Min/max limits apply across the guaranteed operating temperature range of 0°C to +75°C for DS75123, unless otherwise specified. Typicals are for V_{CC} = 5.0V, T_A = 25°C. Positive current is defined as current into the referenced pin.

Note 4: The output voltage and current limits are guaranteed for any appropriate combination of high and low inputs specified by the truth table for the desired output.

National Semiconductor Corporation

DS75124 Triple Line Receiver

General Description

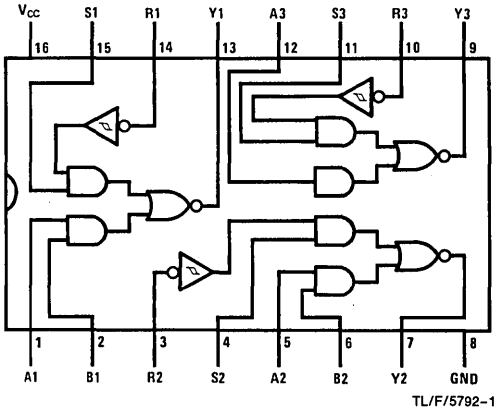
The DS75124 is designed to meet the input/output interface specifications for IBM System 360. It has built-in hysteresis on one input on each of the three receivers to provide large noise margin. The other inputs on each receiver are in a standard TTL configuration. The DS75124 is compatible with standard TTL logic and supply voltage levels.

Features

- Built-in input threshold hysteresis
- High speed . . . type propagation delay time 20 ns
- Independent channel strobes
- Input gating increases application flexibility
- Single 5.0V supply operation
- Plug-in replacement for the SN75124 and the 8T24

Connection Diagram and Truth Table

Dual-In-Line Package



TL/F/5792–1

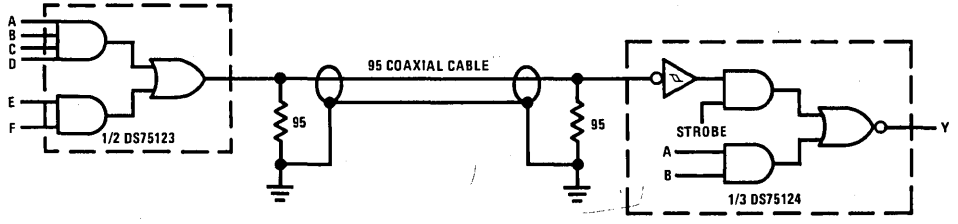
Top View

Order Number DS75124J or DS75124N
See NS Package Number J16A or N16A

Inputs				Output
A	B†	R	S	Y
H	H	X	X	L
X	X	L	H	L
L	X	H	X	H
L	X	X	L	H
X	L	H	X	H
X	L	X	L	H

H = high level, L = low level, X = irrelevant
†B input and last two lines of the truth table are applicable to receivers 1 and 2 only

Typical Application



TL/F/5792–2

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage, V_{CC}	7.0V
Input Voltage	
R Input with V_{CC} Applied	7.0V
R Input with V_{CC} not Applied	6.0V
A, B, or S Input	5.5V
Output Voltage	7.0V
Output Current	±100 mA
Maximum Power Dissipation* at 25°C	
Cavity Package	1433 mW
Molded Package	1362 mW
Operating Temperature Range	0°C to +75°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 4 seconds)	260°C

*Derate cavity package 9.6 mW/°C above 25°C; derate molded package 10.9 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage, V_{CC}	4.75	5.25	V
High Level Output Current, I_{OH}		−800	μA
Low Level Output Current, I_{OL}		16	mA
Operating Temperature, T_A	0	+75	°C

Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IH}	High Level Input Voltage	A, B, or S		2.0			V
		R		1.7			V
V_{IL}	Low Level Input Voltage	A, B, or S				0.8	V
		R				0.8	V
$V_{T+} - V_{T-}$	Hysteresis	V_{CC} = 5.0V, T_A = 25°C, R, (Note 6)		0.2	0.4		V
V_I	Input Clamp Voltage	V_{CC} = 5.0V, I_I = −12 mA, A, B, or S				−1.5	V
I_I	Input Current at Maximum Input Voltage	V_{CC} = 5.25V, V_{IN} = 5.5V, A, B, or S				1	mA
		R	V_I = 7.0V			5.0	mA
			V_I = 6.0V, V_{CC} = 0			5.0	mA
V_{OH}	High Level Output Voltage	$V_{IH} = V_{IHMIN}$, $V_{IL} = V_{ILMAX}$, I_{OH} = −800 μA, (Note 4)		2.6			V
V_{OL}	Low Level Output Voltage	$V_{IH} = V_{INMIN}$, $V_{IL} = V_{ILMAX}$, I_{OL} = 16 mA, (Note 4)				0.4	V
I_{IH}	High Level Input Current	V_I = 4.5V, A, B, or S				40	μA
		V_I = 3.11V, R				170	μA
I_{IL}	Low Level Input Current	V_I = 0.4V, A, B, or S		−0.1		−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = 5.0V, T_A = 25°C, (Note 5)		−50		−100	mA
I_{CC}	Supply Current	V_{CC} = 5.25V				72	mA

Switching Characteristics T_A = 25°C, nominal power supplies unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PLH}	Propagation Delay Time, Low-to-High Level Output from R Input	(See AC Test Circuit and Switching Time Waveforms)		20	30	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output from R Input	(See AC Test Circuit and Switching Time Waveforms)		20	30	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All currents into device pins are shown as positive, currents out of device pins shown as negative, all voltage values are referenced with respect to network ground terminal, unless otherwise noted. All values shown as max or min on absolute value basis.

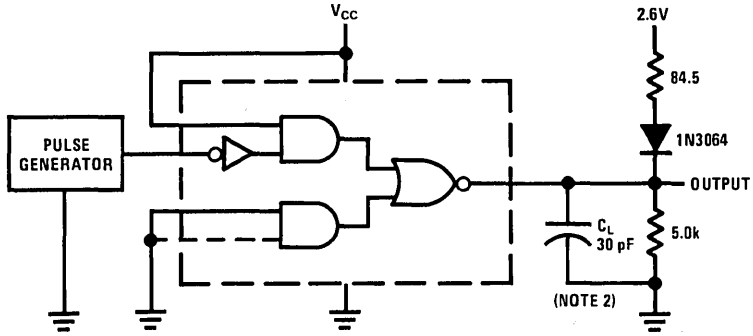
Note 3: Min/max limits apply across the guaranteed operating temperature range of 0°C to +75°C for DS75124, unless otherwise specified. Typicals are for V_{CC} = 5.0V, T_A = 25°C. Positive current is defined as current into the referenced pin.

Note 4: The output voltage and current limits are guaranteed for any appropriate combination of high and low inputs specified by the truth table for the desired output.

Note 5: Not more than one output should be shorted at a time.

Note 6: Hysteresis is the difference between the positive going input threshold voltage, V_{T+}, and the negative going input threshold voltage, V_{T-}.

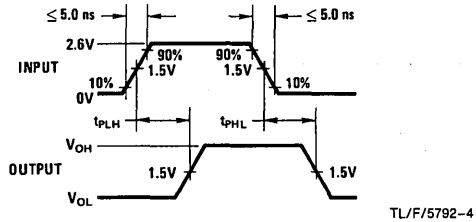
AC Test Circuit and Switching Time Waveforms



TL/F/5792-3

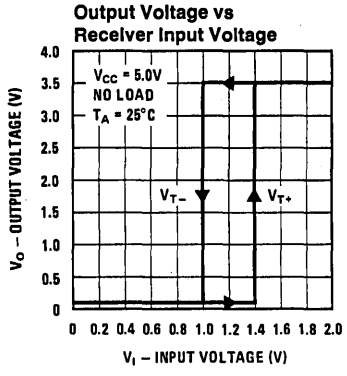
Note 1: The pulse generator has the following characteristics: $Z_{OUT} \approx 50\Omega$, $t_W = 200$ ns, duty cycle = 50%

Note 2: C_L includes probe and jig capacitance.



TL/F/5792-4

Typical Performance Characteristics



TL/F/5792-5

National Semiconductor Corporation

DS75125/DS75127 Seven-Channel Line Receivers

General Description

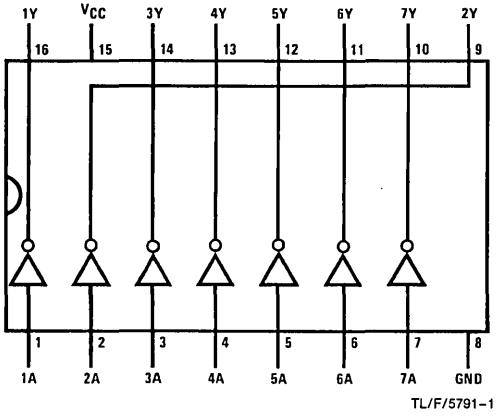
The DS75125 and DS75127 are monolithic seven-channel line receivers designed to satisfy the requirements of the IBM System 360/370 input/output interface specifications. Special low-power design and Schottky clamped transistors allow for low supply current requirements while maintaining fast switching speeds and high current TTL outputs. The DS75125 and DS75127 are characterized for operation from 0°C to 70°C.

Features

- Meets IBM 360/370 I/O specification
- Input resistance—7 kΩ to 20 kΩ
- Output compatible with TTL
- Schottky-clamped transistors
- Operates from single 5V supply
- High speed—low propagation delay
- Ratio specification for propagation delay time, low-to-high/high-to-low
- Seven channels in one 16-pin package
- Standard V_{CC} and ground positioning on DS75127

Connection Diagrams

DS75125
Dual-In-Line Package



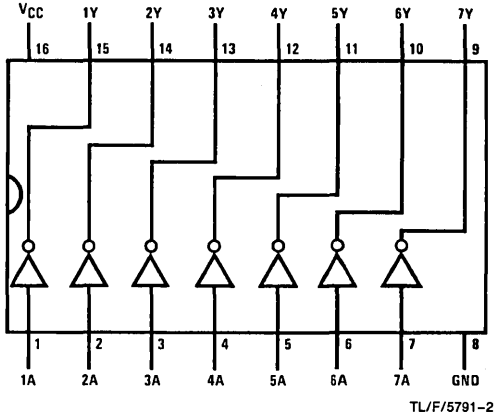
TL/F/5791–1

Top View

logic: Y = A

Order Number DS75125J or DS75125N
See NS Package Number J16A or N16A

DS75127
Dual-In-Line Package



TL/F/5791–2

Top View

logic: Y = A

Order Number DS75127J or DS75127N
See NS Package Number J16A or N16A

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage, V_{CC} (Note 1)	7V
Input Voltage Range	
DS75125	−0.15V to 7V
DS75127	−2V to 7V
Operating Free-Air Temperature Range	0°C to 70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 4 seconds)	260°C

Maximum Power Dissipation* at 25°C (Note 2)	
Cavity Package	1509 mW
Molded Package	1476 mW

*Derate cavity package 10.1 mW/°C above 25°C; derate molded package 11.9 mW/°C above 25°C.

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage, V_{CC}	4.5	5	5.5	V
High-Level Output Current, I_{OH}			−0.4	mA
Low-Level Output Current, I_{OL}			16	mA
Operating Free-Air Temperature, T_A	0		70	°C

Electrical Characteristics over recommended operating free-air temperature range (Note 3)

Symbol	Parameter	Conditions	Min	Typ (Note 5)	Max	Units
V_{IH}	High-Level Input Voltage		1.7			V
V_{IL}	Low-Level Input Voltage				0.7	V
V_{OH}	High-Level Output Voltage	V_{CC} = 4.5V, V_{IL} = 0.7V, I_{OH} = −0.4 mA	2.4	3.1		V
V_{OL}	Low-Level Output Voltage	V_{CC} = 4.5V, V_{IH} = 1.7V, I_{OL} = 16 mA		0.4	0.5	V
I_{IH}	High-Level Input Current	V_{CC} = 5.5V, V_I = 3.11V		0.3	0.42	mA
I_{IL}	Low-Level Input Current	V_{CC} = 5.5V, V_I = 0.15V			−0.24	mA
I_{OS}	Short-Circuit Output Current (Note 4)	V_{CC} = 5.5V, V_O = 0	−18		−60	mA
r_I	Input Resistance	V_{CC} = 4.5V, 0V, or Open, ΔV_I = 0.15V to 4.15V	7		20	kΩ
I_{CC}	Supply Current	V_{CC} = 5.5V, I_{OH} = −0.4 mA, All Inputs at 0.7V		15	25	mA
		V_{CC} = 5.5V, I_{OL} = 16 mA, All Inputs at 4V		28	47	mA

Switching Characteristics V_{CC} = 5V, T_A = 25°C

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PLH}	Propagation Delay Time, Low-to-High-Level Output	R_L = 400Ω, C_L = 50 pF, (See *Figure 1*)	7	14	25	ns
t_{PHL}	Propagation Delay Time, High-to-Low-Level Output		10	18	30	ns
$\frac{t_{PLH}}{t_{PHL}}$	Ratio of Propagation Delay Times		0.5	0.8	1.3	ns
t_{TLH}	Transition Time, Low-to-High-Level Output		1	7	12	ns
t_{THL}	Transition Time, High-to-Low-Level Output		1	3	12	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

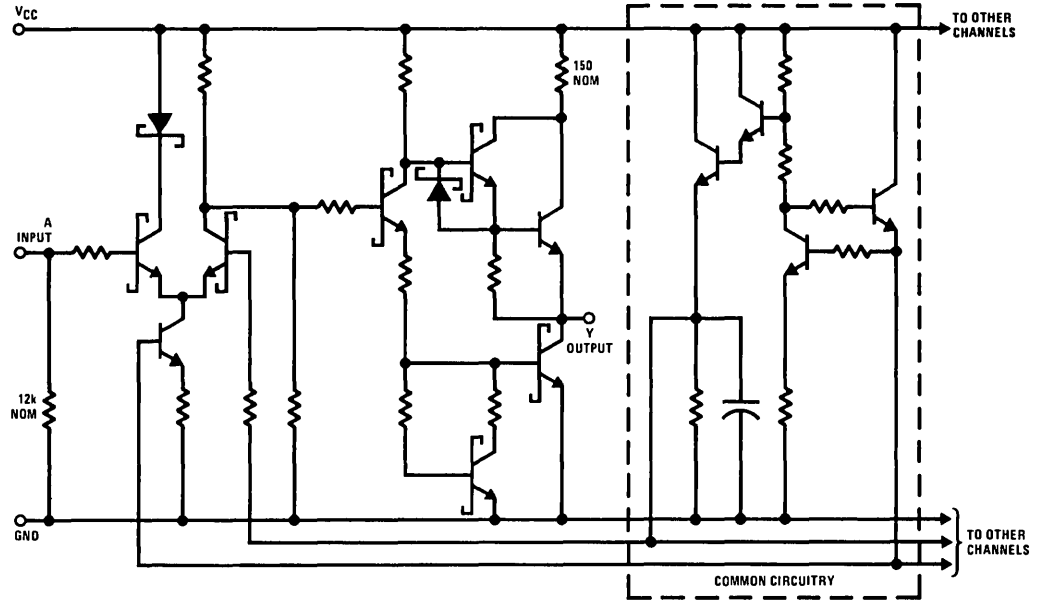
Note 2: For operation above 25°C free-air temperature, refer to Thermal Ratings for ICs, in App Note AN-336.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Only one output should be shorted at a time.

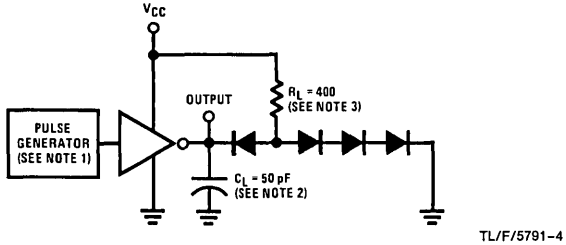
Note 5: All typical values are at V_{CC} = 5V, T_A = 25°C.

Schematic (each receiver)

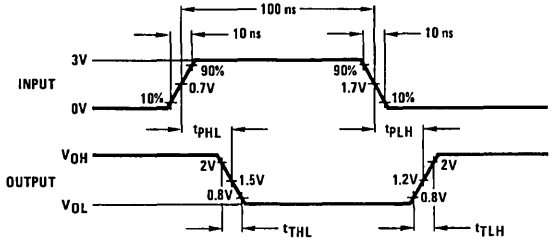


TL/F/5791–3

AC Test Circuit and Switching Time Waveforms



TL/F/5791–4



TL/F/5791–5

Note 1: The pulse generator has the following characteristics: Z_{OUT} = 50Ω, PRR = 5 MHz.

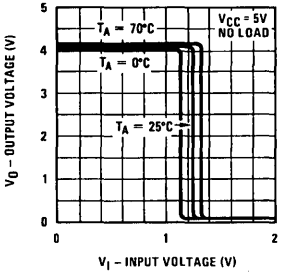
Note 2: C_L includes probe and jig capacitance.

Note 3: All diodes are 1N3064 or equivalent.

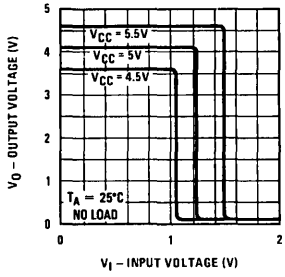
FIGURE 1

Typical Performance Characteristics

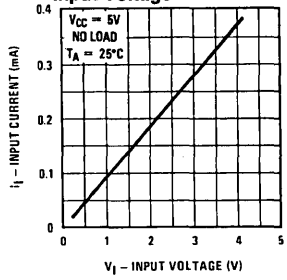
Voltage Transfer Characteristics



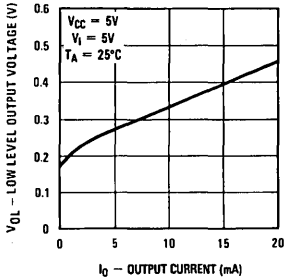
Voltage Transfer Characteristics



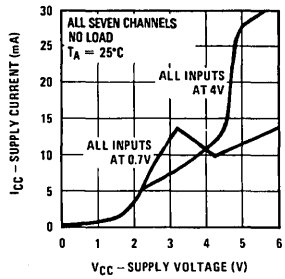
Input Current vs Input Voltage



Low-Level Output Voltage vs Output Current



Supply Current vs Supply Voltage



TL/F/5791–6

National Semiconductor Corporation

DS75128/DS75129 Eight-Channel Line Receivers

General Description

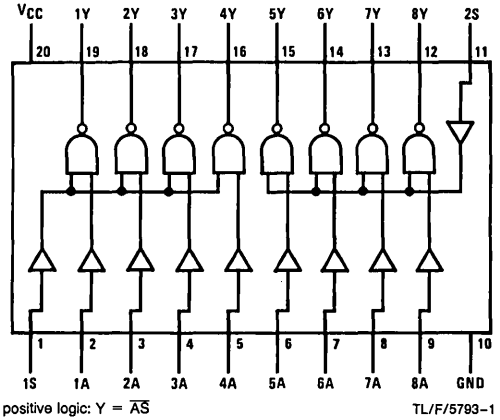
The DS75128 and DS75129 are eight-channel line receivers designed to satisfy the requirements of the input-output interface specification for IBM 360/370. Both devices feature common strobes for each group of four receivers. The DS75128 has an active-high strobe; the DS75129 has an active-low strobe. Special low-power design and Schottky-diode-clamped transistors allow low supply-current requirements while maintaining fast switching speeds and high-current TTL outputs. The DS75128 and DS75129 are characterized for operation from 0°C to 70°C.

Features

- Meets IBM 360/370 I/O specification
- Input resistance—7 kΩ to 20 kΩ
- Output compatible with TTL
- Schottky-clamped transistors
- Operates from a single 5V supply
- High speed—low propagation delay
- Ratio specification—t_{PLH}/t_{PLH}
- Common strobe for each group of four receivers
- DS75128 strobe—active-high
  DS75129 strobe—active-low

Connection Diagrams

DS75128
Dual-In-Line Package

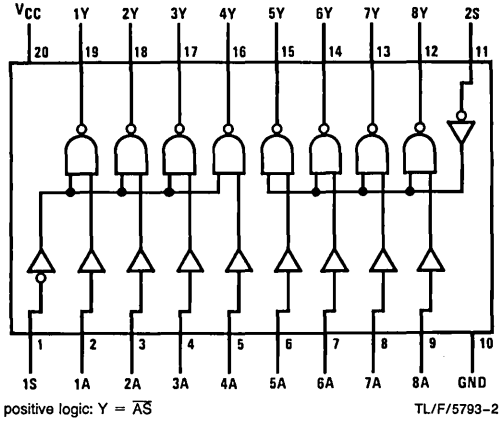


positive logic: $Y = \overline{AS}$ TL/F/5793–1

Top View

Order Number DS75128J or DS75128N
See NS Package Number J20A or N20A

DS75129
Dual-In-Line Package



positive logic: $Y = \overline{AS}$ TL/F/5793–2

Top View

Order Number DS75129J or DS75129N
See NS Package Number J20A or N20A

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage, V_{CC}	7V
Input Voltage Range	−0.15V to 7V
Strobe Input Voltage	7V
Maximum Power Dissipation* at 25°C (Note 2)	
Cavity Package	1564 mW
Molded Package	1687 mW
Operating Free-Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature	300°C
1/16 Inch from Case for 60 Seconds: J Package	
Lead Temperature	260°C
1/16 Inch from Case for 4 Seconds: N Package	

*Derate cavity package 10.4 mW/°C above 25°C; derate molded package 13.5 mW/°C above 25°C.

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage, V_{CC}	4.5	5.0	5.5	V
High-Level Output Current, I_{OH}			−0.4	mA
Low-Level Output Current, I_{OL}			16	mA
Operating Free-Air Temperature, T_A	0		70	°C

Electrical Characteristics over recommended operating free-air temperature range (Note 3)

Symbol	Parameter		Conditions	Min	Typ (Note 5)	Max	Units
V_{IH}	High-Level Input Voltage	A		1.7			V
		S		2			
V_{IL}	Low-Level Input Voltage	A				0.7	V
		S				0.7	
V_{OH}	High-Level Output Voltage		V_{CC} = 4.5V, V_{IL} = 0.7V, I_{OH} = 0.4 mA	2.4	3.1		V
V_{OL}	Low-Level Output Voltage		V_{CC} = 4.5V, V_{IH} = 1.7V, I_{OL} = 16 mA		0.4	0.5	V
V_I	Input Clamp Voltage	S	V_{CC} = 4.5V, I_I = −18 mA			−1.5	V
I_{IH}	High-Level Input Current	A	V_{CC} = 5.5V, V_I = 3.11V		0.3	0.42	mA
		S	V_{CC} = 5.5V, V_I = 2.7V			20	μA
I_{IL}	Low-Level Input Current	A	V_{CC} = 5.5V, V_I = 0.15V			−0.24	mA
		S	V_{CC} = 5.5V, V_I = 0.4V			−0.4	
I_{OS}	Short-Circuit Output Current (Note 4)		V_{CC} = 5.5V, V_O = 0V	−18		−60	mA
r_I	Input Resistance		V_{CC} = 4.5V, 0V, or Open, ΔV, = 0.15V to 4.15V	7		20	kΩ
I_{CC}	Supply Current	DS75128	V_{CC} = 5.5V, Strobe at 2.4V, All A Inputs at 0.7V		19	31	mA
		DS75129	V_{CC} = 5.5V, Strobe at 0.4V, All A Inputs at 0.7V		19	31	
		DS75128	V_{CC} = 5.5V, Strobe at 2.4V, All A Inputs at 4V		32	53	
		DS75129	V_{CC} = 5.5V, Strobe at 0.4V, All A Inputs at 4V		32	53	

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: For operation above 25°C free-air temperature, refer to Thermal Ratings for ICs, in App Note AN-336.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

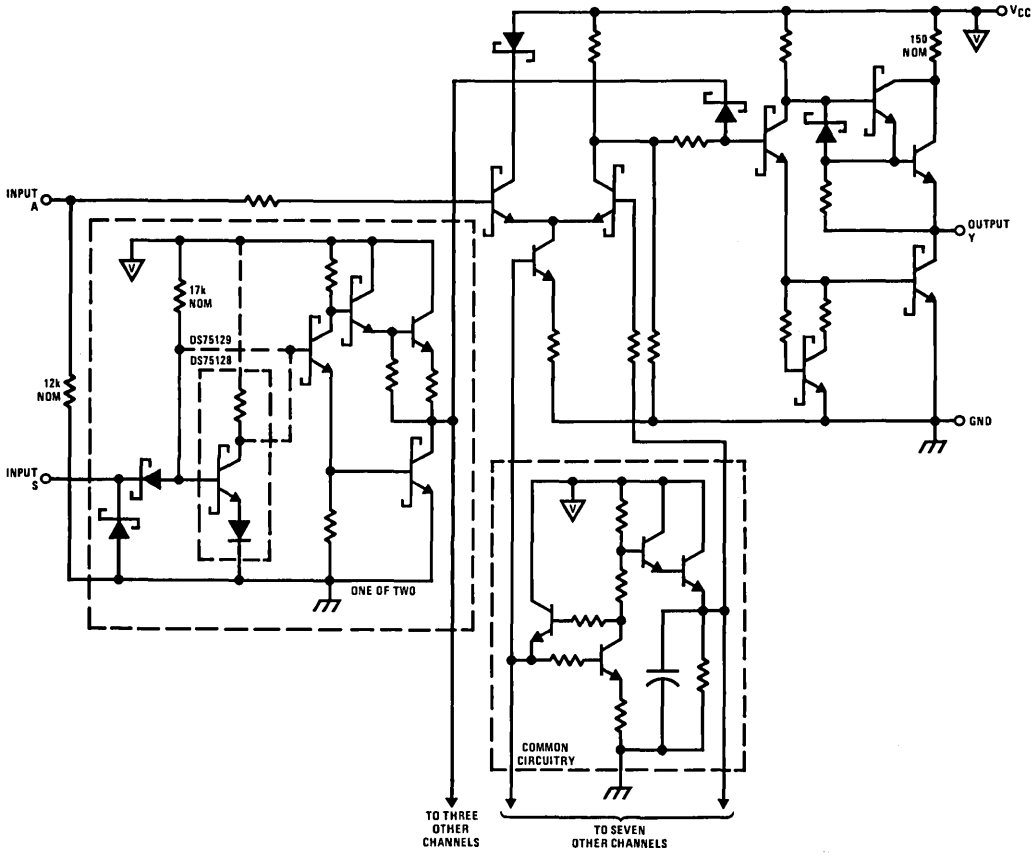
Note 4: Only one output should be shorted at a time.

Note 5: All typical values are at V_{CC} = 5V, T_A = 25°C.

Switching Characteristics V_{CC} = 5V, T_A = 25°C

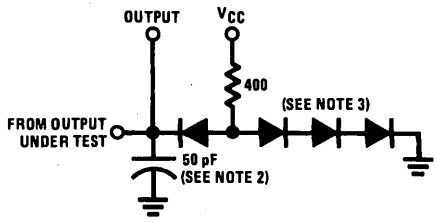
Symbol	Parameter		Conditions	DS75128			DS75129			Units
				Min	Typ	Max	Min	Typ	Max	
t_{PLH}	Propagation Delay Time, Low-to-High-Level Output	A	R_L = 400Ω, C_L = 50 pF, See *Figure 1*	7	14	25	7	14	25	ns
t_{PHL}	Propagation Delay Time, High-to-Low-Level Output	A		10	18	30	10	18	30	ns
t_{PLH}	Propagation Delay Time, Low-to-High-Level Output	S			26	40		20	35	ns
t_{PHL}	Propagation Delay Time, High-to-Low-Level Output	S			22	35		16	30	ns
t_{PLH} / t_{PHL}	Ratio of Propagation Delay Times	A		0.5	0.8	1.3	0.5	0.8	1.3	
t_{TLH}	Transition Time, Low-to-High-Level Output			1	7	12	1	7	12	ns
t_{THL}	Transition Time, High-to-Low-Level Output			1	3	12	1	3	12	ns

Schematic Diagram (each receiver)

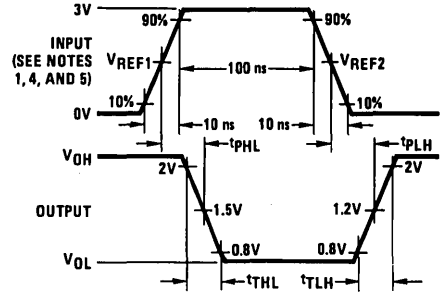


TL/F/5793–3

AC Test Circuit and Switching Time Waveforms



TL/F/5793–4



TL/F/5793–5

Note 1: Input pulses are supplied by a generator having the following characteristics: $Z_O = 50\Omega$, PRR = 5 MHz.

Note 2: Includes probe and jig capacitance.

Note 3: All diodes are 1N3064 or equivalent.

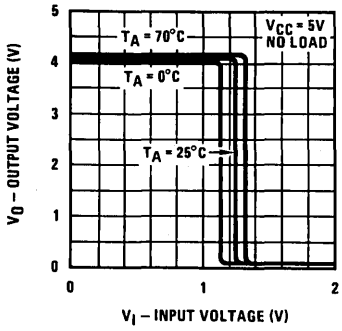
Note 4: The strobe inputs of DS75129 are in-phase with the output.

Note 5: $V_{REF1} = 0.7V$ and $V_{REF2} = 1.7V$ for testing data (A) inputs, $V_{REF1} = V_{REF2} = 1.3V$ for strobe inputs.

FIGURE 1

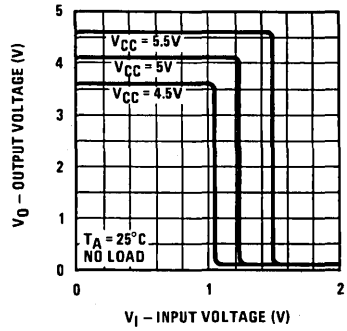
Typical Characteristics

Voltage Transfer Characteristics From A Inputs



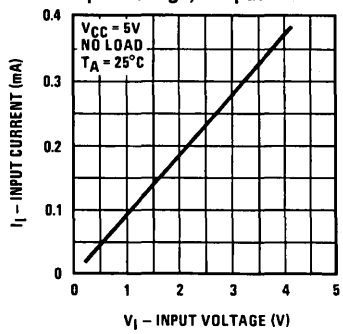
TL/F/5793–6

Voltage Transfer Characteristics From A Inputs



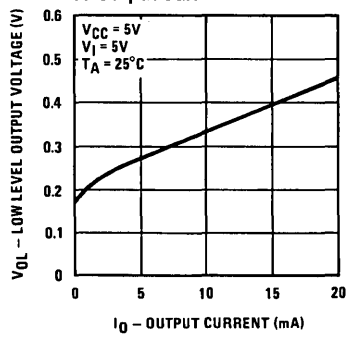
TL/F/5793–7

Input Current vs Input Voltage, A Inputs



TL/F/5793–8

Low-Level Output Voltage vs Output Current



TL/F/5793–9

National Semiconductor Corporation

DS75150 Dual Line Driver

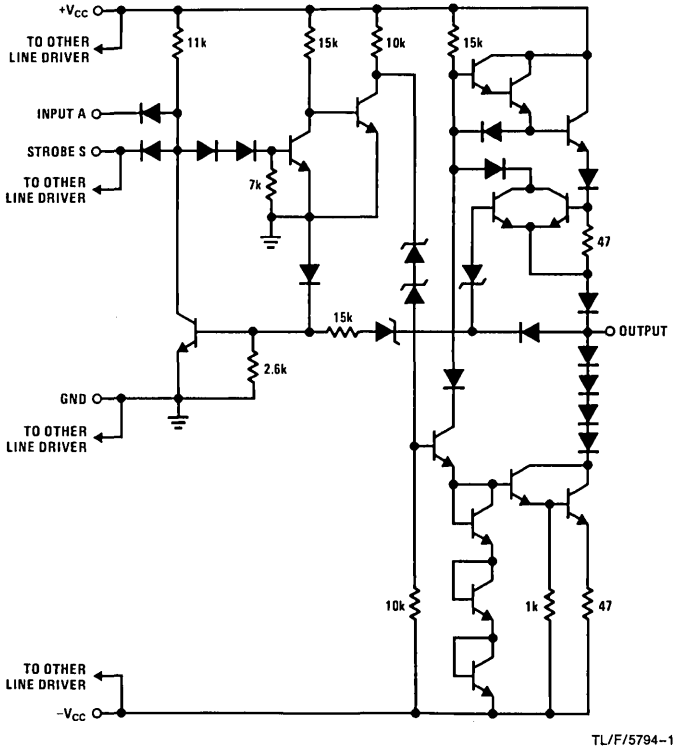
General Description

The DS75150 is a dual monolithic line driver designed to satisfy the requirements of the standard interface between data terminal equipment and data communication equipment as defined by EIA Standard RS-232-C. A rate of 20,000 bits per second can be transmitted with a full 2500 pF load. Other applications are in data-transmission systems using relatively short single lines, in level translators, and for driving MOS devices. The logic input is compatible with most TTL and LS families. Operation is from −12V and +12V power supplies.

Features

- Withstands sustained output short-circuit to any low impedance voltage between −25V and +25V
- 2 μs max transition time through the −3V to +3V transition region under full 2500 pF load
- Inputs compatible with most TTL and LS families
- Common strobe input
- Inverting output
- Slew rate can be controlled with an external capacitor at the output
- Standard supply voltages ±12V

Schematic and Connection Diagrams



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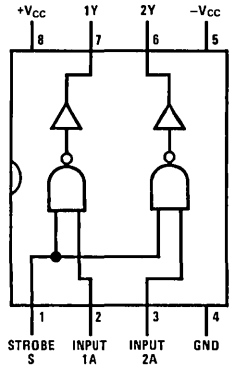
Component values shown are nominal.
1/2 of circuit shown

Dual-In-Line Package



TL/F/5794–2

Top View

Positive Logic C = $\overline{AS}$

Order Number DS75150J-8, DS75150M or DS75150N
See NS Package Number J08A, M08A or N08E

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage $+V_{CC}$	15V
Supply Voltage $-V_{CC}$	15V
Input Voltage	15V
Applied Output Voltage	+25V
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1133 mW
Molded DIP Package	1022 mW
SO Package	655 mW
Lead Temperature (Soldering, 4 sec.)	260°C

*Derate cavity package 7.6 mW/°C above 25°C; derate molded DIP package 8.2 mW/°C above 25°C. Derate SO package 8.01 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage ($+V_{CC}$)	10.8	13.2	V
Supply Voltage ($-V_{CC}$)	−10.8	−13.2	V
Input Voltage (V_I)	0	+5.5	V
Output Voltage (V_O)		±15	V
Operating Ambient Temperature Range (T_A)	0	+70	°C

DC Electrical Characteristics (Notes 2, 3, 4 and 5)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IH}	High-Level Input Voltage	*(Figure 1)*		2			V
V_{IL}	Low-Level Input Voltage	*(Figure 2)*				0.8	V
V_{OH}	High-Level Output Voltage	$+V_{CC}$ = 10.8V, $-V_{CC}$ = −13.2V, V_{IL} = 0.8V, R_L = 3 kΩ to 7 kΩ *(Figure 2)*		5	8		V
V_{OL}	Low-Level Output Voltage	$+V_{CC}$ = 10.8V, $-V_{CC}$ = −10.8V, V_{IH} = 2V, R_L = 3 kΩ to 7 kΩ *(Figure 1)*			−8	−5	V
I_{IH}	High-Level Input Current	$+V_{CC}$ = 13.2V, $-V_{CC}$ = −13.2V, V_I = 2.4V, *(Figure 3)*	Data Input		1	10	μA
		$+V_{CC}$ = 13.2V, $-V_{CC}$ = −13.2V, V_I = 2.4V, *(Figure 3)*	Strobe Input		2	20	μA
I_{IL}	Low-Level Input Current	$+V_{CC}$ = 13.2V, $-V_{CC}$ = −13.2V, V_I = 0.4V, *(Figure 3)*	Data Input		−1	−1.6	mA
		$+V_{CC}$ = 13.2V, $-V_{CC}$ = −13.2V, V_I = 0.4V, *(Figure 3)*	Strobe Input		−2	−3.2	mA
I_{OS}	Short-Circuit Output Current	$+V_{CC}$ = 13.2V, $-V_{CC}$ = −13.2V, *(Figure 4)*, (Note 4)	V_O = 25V		2	5	mA
			V_O = −25V		−3	−6	mA
			V_O = 0V, V_I = 3V		15	30	mA
			V_O = 0V, V_I = 0V		−15	−30	mA
$+I_{CCH}$	Supply Current From $+V_{CC}$, High-Level Output	$+V_{CC}$ = 13.2V, $-V_{CC}$ = −13.2V, V_I = 0V, R_L = 3 kΩ, T_A = 25°C, *(Figure 5)*			10	22	mA
$-I_{CCH}$	Supply Current From $-V_{CC}$, High-Level Output	$+V_{CC}$ = 13.2V, $-V_{CC}$ = −13.2V, V_I = 0V, R_L = 3 kΩ, T_A = 25°C, *(Figure 5)*			−1	−10	mA
$+I_{CCL}$	Supply Current From $+V_{CC}$, Low-Level Output	$+V_{CC}$ = 13.2V, $-V_{CC}$ = −13.2V, V_I = 3V, R_L = 3 kΩ, T_A = 25°C, *(Figure 5)*			8	17	mA
$-I_{CCL}$	Supply Current From $-V_{CC}$, Low-Level Output	$+V_{CC}$ = 13.2V, $-V_{CC}$ = −13.2V, V_I = 3V, R_L = 3 kΩ, T_A = 25°C, *(Figure 5)*			−9	−20	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C range for the DS75150. All typical values are T_A = 25°C and $+V_{CC}$ = 12V, $-V_{CC}$ = −12V.

Note 3: All current into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

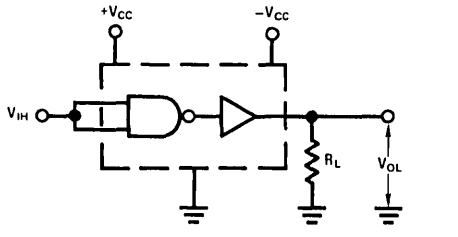
Note 4: Only one output at a time should be shorted.

Note 5: The algebraic convention where the most-positive (least-negative) limit is designated as maximum is used in this data sheet for logic levels only, e.g., when −5V is the maximum, the typical value is more-negative voltage.

AC Electrical Characteristics ($+V_{CC}$ = 12V, $-V_{CC}$ = −12V, T_A = 25°C)

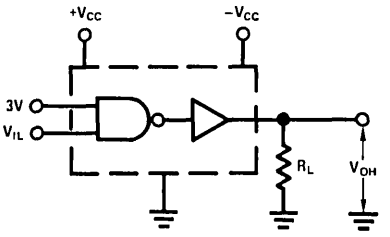
Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{TLH}	Transition Time, Low-to-High Level Output	C_L = 2500 pF, R_L = 3 kΩ to 7 kΩ, *(Figure 6)*	0.2	1.4	2	μs
t_{THL}	Transition Time, High-to-Low Level Output	C_L = 2500 pF, R_L = 3 kΩ to 7 kΩ, *(Figure 6)*	0.2	1.5	2	μs
t_{TLH}	Transition Time, Low-to-High Level Output	C_L = 15 pF, R_L = 7 kΩ, *(Figure 6)*		40		ns
t_{THL}	Transition Time, High-to-Low Level Output	C_L = 15 pF, R_L = 7 kΩ, *(Figure 6)*		20		ns
t_{PLH}	Propagation Delay Time Low-to-High Level Output	C_L = 15 pF, R_L = 7 kΩ, *(Figure 6)*		60		ns
t_{PHL}	Propagation Delay Time High-to-Low Level Output	C_L = 15 pF, R_L = 7 kΩ, *(Figure 6)*		45		ns

DC Test Circuits



TL/F/5794–3

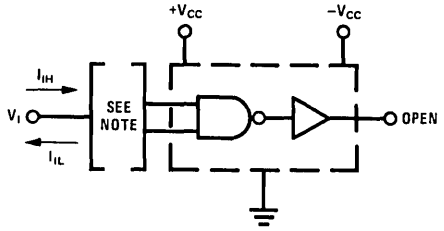
FIGURE 1. V_{IH}, V_{OL}



TL/F/5794–4

Each input is tested separately.

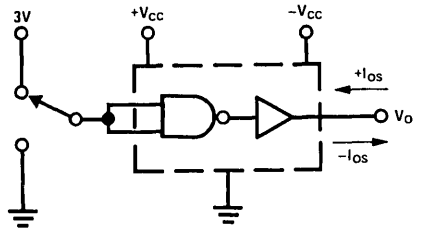
FIGURE 2. V_{IL}, V_{OH}



TL/F/5794–5

Note: When testing I_{IH}, the other input is at 3V; when testing I_{IL}, the other input is open.

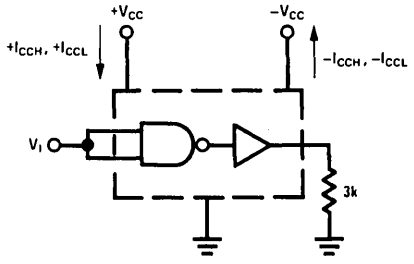
FIGURE 3. I_{IH}, I_{IL}



TL/F/5794–6

I_{OS} is tested for both input conditions at each of the specified output conditions.

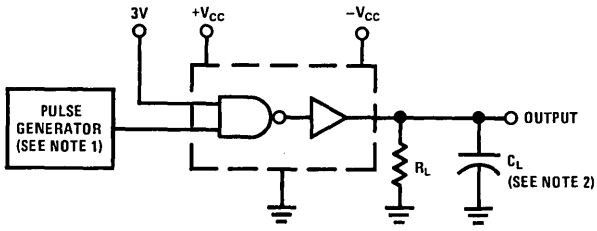
FIGURE 4. I_{OS}



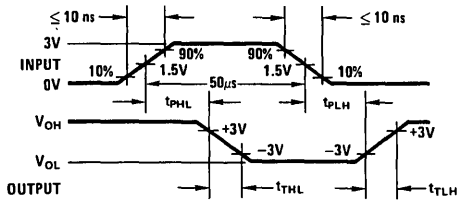
TL/F/5794–7

FIGURE 5. $I_{CCH}+$, $I_{CCH}-$, $I_{CCL}+$, $I_{CCL}-$

AC Test Circuit and Switching Waveforms



TL/F/5794–8



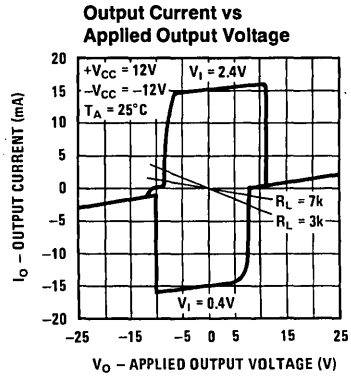
TL/F/5794–9

Note 1: The pulse generator has the following characterstics:
duty cycle ≤ 50%, $Z_{OUT} \cong 50\Omega$.

Note 2: C_L includes probe and jig capacitance.

FIGURE 6

Typical Performance Characteristics



TL/F/5794–10

FIGURE 7

National Semiconductor Corporation

DS75154 Quad Line Receiver

General Description

The DS75154 is a quad monolithic line receiver designed to satisfy the requirements of the standard interface between data terminal equipment and data communication equipment as defined by EIA Standard RS-232C. Other applications are in relatively short, single-line, point-to-point data transmission systems and for level translators. Operation is normally from a single 5V supply; however, a built-in option allows operation from a 12V supply without the use of additional components. The output is compatible with most TTL and LS circuits when either supply voltage is used.

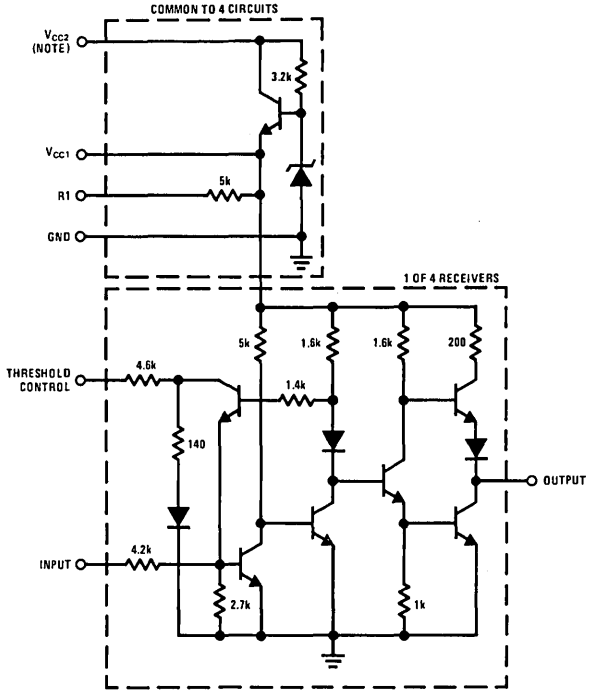
In normal operation, the threshold-control terminals are connected to the V_{CC1} terminal, pin 15, even if power is being supplied via the alternate V_{CC2} terminal, pin 16. This provides a wide hysteresis loop which is the difference between the positive-going and negative-going threshold voltages. In this mode, if the input voltage goes to zero, the output voltage will remain at the low or high level as determined by the previous input.

For fail-safe operation, the threshold-control terminals are open. This reduces the hysteresis loop by causing the negative-going threshold voltage to be above zero. The positive-going threshold voltage remains above zero as it is unaffected by the disposition of the threshold terminals. In the fail-safe mode, if the input voltage goes to zero or an open-circuit condition, the output will go to the high level regardless of the previous input condition.

Features

- Input resistance, 3 kΩ to 7 kΩ over full RS-232C voltage range
- Input threshold adjustable to meet "fail-safe" requirements without using external components
- Inverting output compatible with TTL or LS
- Built-in hysteresis for increased noise immunity
- Output with active pull-up for symmetrical switching speeds
- Standard supply voltage—5V or 12V

Schematic Diagram



TL/F/5795–1

Note: When using V_{CC1} (pin 15), V_{CC2} (pin 16) may be left open or shorted to V_{CC1}. When using V_{CC2}, V_{CC1} must be left open or connected to the threshold control pins.

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Normal Supply Voltage (Pin 15), (V_{CC1})	7V
Alternate Supply Voltage (Pin 16), (V_{CC2})	14V
Input Voltage	±25V
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1433 mW
Molded DIP Package	1362 mW
Lead Temperature (Soldering, 4 seconds)	260°C

*Derate cavity package 9.6 mW/°C above 25°C; derate molded DIP package 10.9 mW/°C above 25°C; derate SO package 8.01 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage (Pin 15), (V_{CC1})	4.5	5.5	V
Alternate Supply Voltage (Pin 16), (V_{CC2})	10.8	13.2	V
Input Voltage		±15	V
Temperature, (T_A)	0	+70	°C

Electrical Characteristics (Notes 2, 3 and 4)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IH}	High-Level Input Voltage	*(Figure 1)*		3			V
V_{IL}	Low-Level Input Voltage	*(Figure 1)*				−3	V
V_{T+}	Positive-Going Threshold Voltage	*(Figure 1)*	Normal Operation	0.8	2.2	3	V
			Fail-Safe Operation	0.8	2.2	3	V
V_{T-}	Negative-Going Threshold Voltage	*(Figure 1)*	Normal Operation	−3	−1.1	0	V
			Fail-Safe Operation	0.8	1.4	3	V
$V_{T+}-V_{T-}$	Hysteresis	*(Figure 1)*	Normal Operation	0.8	3.3	6	V
			Fail-Safe Operation	0	0.8	2.2	V
V_{OH}	High-Level Output Voltage	$I_{OH}=-400\ \mu A$, *(Figure 1)*		2.4	3.5		V
V_{OL}	Low-Level Output Voltage	$I_{OL}=16$ mA, *(Figure 1)*			0.23	0.4	V
r_I	Input Resistance	*(Figure 2)*	$\Delta V_I=-25V$ to $-14V$	3	5	7	kΩ
			$\Delta V_I=-14V$ to $-3V$	3	5	7	kΩ
			$\Delta V_I=-3V$ to $+3V$	3	6		kΩ
			$\Delta V_I=3V$ to $14V$	3	5	7	kΩ
			$\Delta V_I=14V$ to $25V$	3	5	7	kΩ
$V_{I(OPEN)}$	Open-Circuit Input Voltage	$I_I=0$, *(Figure 3)*		0	0.2	2	V
I_{OS}	Short-Circuit Output Current (Note 5)	$V_{CC1}=5.5V$, $V_I=-5V$, *(Figure 4)*		−10	−20	−40	mA
I_{CC1}	Supply Current From V_{CC1}	$V_{CC1}=5.5V$, $T_A=25°C$, *(Figure 5)*			20	35	mA
I_{CC2}	Supply Current From V_{CC2}	$V_{CC2}=13.2V$, $T_A=25°C$, *(Figure 5)*			23	40	mA

Switching Characteristics ($V_{CC1}=5V$, $T_A=25°C$)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	$C_L=50$ pF, $R_L=390\Omega$, *(Figure 6)*		22		ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	$C_L=50$ pF, $R_L=390\Omega$, *(Figure 6)*		20		ns
t_{TLH}	Transition Time, Low-to-High Level Output	$C_L=50$ pF, $R_L=390\Omega$, *(Figure 6)*		9		ns
t_{THL}	Transition Time, High-to-Low Level Output	$C_L=50$ pF, $R_L=390\Omega$, *(Figure 6)*		6		ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C range for the DS75154. All typical values are for $T_A=25°C$ and $V_{CC1}=5V$.

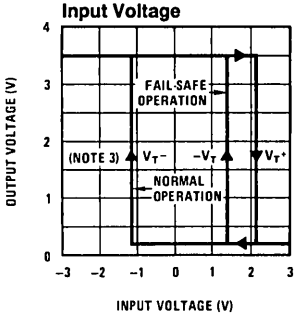
Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: The algebraic convention where the most-positive (least-negative) limit is designated as maximum is used in this data sheet for logic and threshold levels only, e.g., when −3V is the maximum, the minimum limit is a more-negative voltage.

Note 5: Only one output at a time should be shorted.

Typical Performance Characteristics

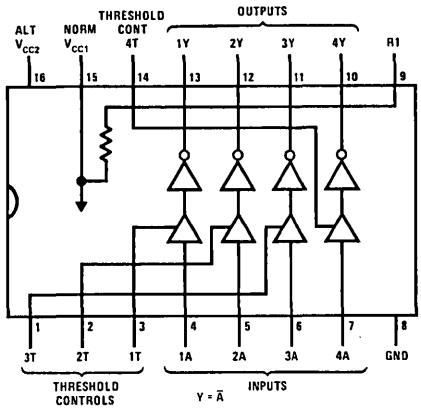
Output Voltage vs Input Voltage



TL/F/5795–10

Connection Diagram

Dual-In-Line Package

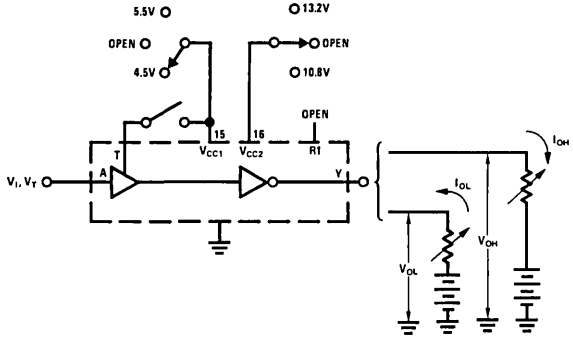


TL/F/5795–2

Top View

Order Number DS75154J, DS75154M or DS75154N
See NS Package Number J16A, M16A or N16A

DC Test Circuits and Truth Tables



TL/F/5795–3

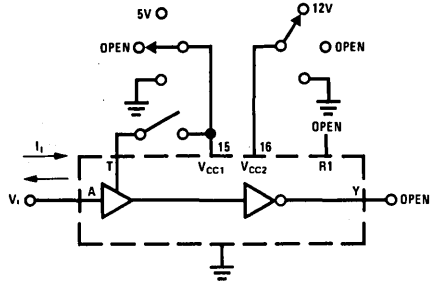
Test	Measure	A	T	Y	V_{CC1} (Pin 15)	V_{CC2} (Pin 16)
Open-Circuit Input (Fail-Safe)	V_{OH} V_{OH}	Open Open	Open Open	I_{OH} I_{OH}	4.5V Open	Open 10.8V
V_{T+} min, V_{T-} (Fail-Safe)	V_{OH} V_{OH}	0.8V 0.8V	Open Open	I_{OH} I_{OH}	5.5V Open	Open 13.2V
V_{T+} min (Normal)	V_{OH} V_{OH}	(Note 1) (Note 1)	Pin 15 Pin 15	I_{OH} I_{OH}	5.5V and T T	Open 13.2V
V_{IL} max, V_{T-} min (Normal)	V_{OH} V_{OH}	−3V −3V	Pin 15 Pin 15	I_{OH} I_{OH}	5.5V and T T	Open 13.2V
V_{IH} min, V_{T+} max, V_{T-} max (Fail-Safe)	V_{OL} V_{OL}	3V 3V	Open Open	I_{OL} I_{OL}	4.5V Open	Open 10.8V
V_{IH} min, V_{T+} max, (Normal)	V_{OL} V_{OL}	3V 3V	Pin 15 Pin 15	I_{OL} I_{OL}	4.5V and T T	Open 10.8V
V_{T-} max (Normal)	V_{OL} V_{OL}	(Note 2) (Note 2)	Pin 15 Pin 15	I_{OL} I_{OL}	5.5V and T T	Open 13.2V

Note 1: Momentarily apply −5V, then 0.8V.

Note 2: Momentarily apply 5V, then ground.

FIGURE 1. V_{IH}, V_{IL}, V_{T+}, V_{T-}, V_{OH}, V_{OL}

DC Test Circuits and Truth Tables (Continued)

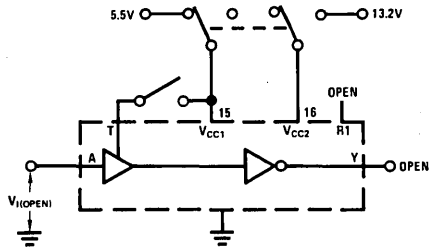


$r_I = \frac{\Delta V_I}{\Delta I_I}$

TL/F/5795–4

T	V_{CC1} (Pin 15)	V_{CC2} (Pin 16)
Open	5V	Open
Open	Gnd	Open
Open	Open	Open
Pin 15	T and 5V	Open
Gnd	Gnd	Open
Open	Open	12V
Open	Open	Gnd
Pin 15	T	12V
Pin 15	T	Gnd
Pin 15	T	Open

FIGURE 2. r_I



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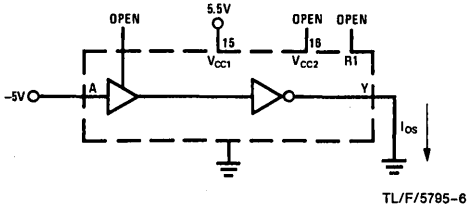
T	V_{CC1} (Pin 15)	V_{CC2} (Pin 16)
Open	5.5V	Open
Pin 15	5.5V	Open
Open	Open	13.2V
Pin 15	T	13.2V

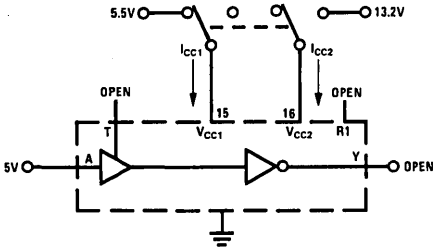
FIGURE 3. $V_{I(OPEN)}$



TL/F/5795–6

Each output is tested separately.

FIGURE 4. I_{OS}

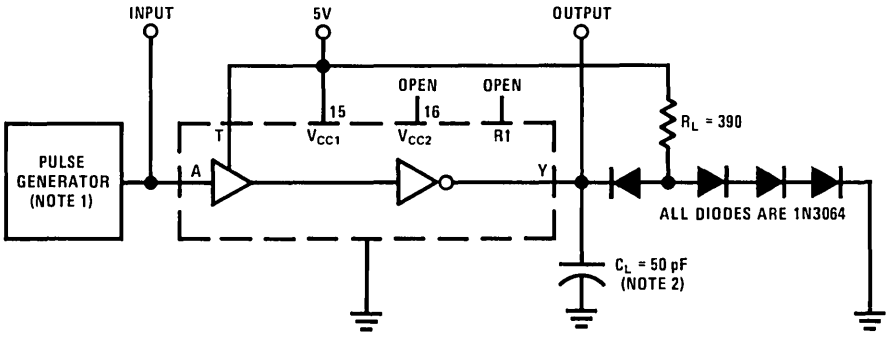


TL/F/5795–7

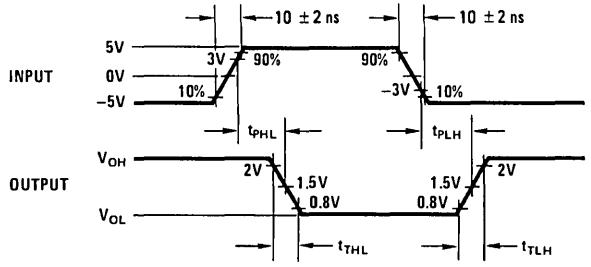
All four line receivers are tested simultaneously.

FIGURE 5. I_{CC}

AC Test Circuit and Switching Time Waveforms



TL/F/5795–8



TL/F/5795–9

Note 1: The pulse generator has the following characteristics: $Z_{OUT} = 50\Omega$, $t_W = 200$ ns, duty cycle ≤ 20%.

Note 2: C_L includes probe and jig capacitance.

FIGURE 6

National Semiconductor Corporation

PRELIMINARY

DS75176A/DS75176AT Multipoint RS-485/RS-422 Transceivers

General Description

The DS75176A is a high speed differential TRI-STATE® bus/line transceiver designed to meet the requirements of EIA standard RS485 with extended common mode range (+12V to −7V), for multipoint data transmission. In addition it meets the requirements of RS422.

The driver and receiver outputs feature TRI-STATE capability, for the driver outputs over the entire common mode range of +12V to −7V. Bus contention or fault situations that cause excessive power dissipation within the device are handled by a thermal shutdown circuit, which forces the driver outputs into the high impedance state.

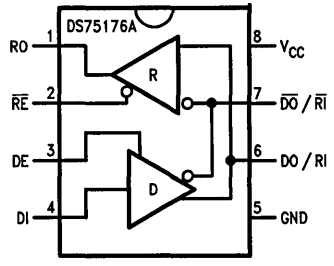
The receiver incorporates a fail safe feature which guarantees a high output state when the inputs are left open.

Both AC and DC specifications are guaranteed over the 0 to 70°C temperature and 4.75V to 5.25V supply voltage range.

Features

- Meets EIA standard RS485 for multipoint bus transmission and RS422.
- Small Outline (SO) Package option available for minimum board space.
- 22 ns driver propagation delays with 8 ns skew (typical).
- Single channel per package isolates faulty channels (from shutting down good channels).
- Single +5V supply.
- −7V to +12V bus common mode range permits ±7V ground difference between devices on the bus.
- Thermal shutdown protection.
- Power-up down glitch-free driver outputs permit live insertion or removal of transceivers.
- High impedance to bus with driver in TRI-STATE or with power off, over the entire common mode range allows the unused devices on the bus to be powered down.
- Pin out capatible with DS3695 and SN75176A.
- Combined impedance of a driver output and receiver input is less than one RS485 unit load, allowing up to 32 transceivers on the bus.
- 70 mV typical receiver hysteresis.

Connection and Logic Diagram



TL/F/8759–1

Top View

Order Number DS75176AN, DS75176AM, DS75176AJ-8, DS75176ATN
See NS Package Number N08E, M08A or J08A

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage, V_{CC}	7V
Control Input Voltages	7V
Driver Input Voltage	7V
Driver Output Voltages	+15V/ −10V
Receiver Input Voltages (DS75176A)	+15V/ −10V
Receiver Output Voltage	5.5V
Continuous Power Dissipation @25°C for M Package	675 mW (Note 5)
Continuous Power Dissipation @25°C (for N Package)	900 mW (Note 4)
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 4 seconds)	260°C

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage, V_{CC}	4.75	5.25	V
Voltage at Any Bus Terminal (Separate or Common Mode)	−7	+12	V
Operating Free Air Temperature T_A	−40	+85	°C
Differential Input Voltage, VID (Note 6)			+12V

Electrical Characteristics (Notes 2 and 3)

0°C ≤ T_A ≤ 70°C, 4.75V < V_{CC} < 5.25V unless otherwise specified

Symbol	Parameter		Conditions		Min	Typ	Max	Units
V_{OD1}	Differential Driver Output Voltage (Unloaded)		I_O = 0				5	V
V_{OD2}	Differential Driver Output Voltage (with Load)		*(Figure 1)*	R = 50Ω; (RS-422) (Note 4)	2			V
				R = 27Ω; (RS-485)	1.5			V
ΔV_{OD}	Change in Magnitude of Driver Differential Output Voltage For Complementary Output States		*(Figure 1)*	R = 27Ω			0.2	V
V_{OC}	Driver Common Mode Output Voltage						3.0	V
$\Delta\lvert V_{OC}\rvert$	Change in Magnitude of Driver Common Mode Output Voltage For Complementary Output States						0.2	V
V_{IH}	Input High Voltage	DI, DE, $\overline{RE}$, E			2			V
V_{IL}	Input Low Voltage						0.8	
V_{CL}	Input Clamp Voltage			I_{IN} = −18 mA			−1.5	
I_{IL}	Input Low Current			V_{IL} = 0.4V			−200	μA
I_{IH}	Input High Current			V_{IH} = 2.4V			20	μA
I_{IN}	Input Current	DO/RI, $\overline{DO}/\overline{RI}$	V_{CC} = 0V or 5.25V DE = 0V	V_{IN} = 12V			+1.0	mA
				V_{IN} = −7V			−0.8	mA
V_{TH}	Differential Input Threshold Voltage for Receiver		−7V ≤ V_{CM} ≤ + 12V		−0.2		+0.2	V
ΔV_{TH}	Receiver Input Hysteresis		V_{CM} = 0V			70		mV
V_{OH}	Receiver Output High Voltage		I_{OH} = −400 μA		2.4			V
V_{OL}	Output Low Voltage	RO	I_{OL} = 16 mA (Note 7)				0.5	V
		$\overline{LF}$	I_{OL} = 8 mA				0.45	V
I_{OZR}	OFF-State (High Impedance) Output Current at Receiver		V_{CC} = Max 0.4V ≤ V_O ≤ 2.4V				±20	μA
R_{IN}	Receiver Input Resistance		−7V ≤ V_{CM} ≤ +12V		12			kΩ
I_{CC}	Supply Current		No Load (Note 7)	Driver Outputs Enabled		35	50	mA
				Driver Outputs Disabled		27	40	mA

1

Electrical Characteristics (Notes 2 and 3)

$0°C \le T_A \le 70°C$, $4.75V < V_{CC} < 5.25V$ unless otherwise specified (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{OSD}	Driver Short-Circuit Output Current	$V_O = -7V$ (Note 7)			−250	mA
		$V_O = +12V$ (Note 7)			+250	mA
I_{OSR}	Receiver Short-Circuit Output Current	$V_O = 0V$	−15		−85	mA

Note 1: "Absolute Maximum Ratings" are those beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to device ground unless otherwise specified.

Note 3: All typicals are given for $V_{CC} = 5V$ and $T_A = 25°C$.

Note 4: Derate linearly at 5.56 mW/°C to 650 mW at 70°C.

Note 5: Derate linearly @ 6.11 mW/°C to 400 mW at 70°C.

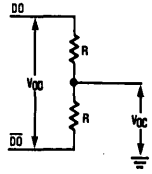
Note 6: Differential - Input/Output bus voltage is measured at the noninverting terminal A with respect to the inverting terminal B.

Note 7: All worst case parameters for which note 7 is applied, must be increased by 10% for DS75176AT. The other parameters remain valid for $-40°C < T_A < +85°C$.

Switching Characteristics $4.75V \le V_{CC} \le 5.25V$; $0°C < T_A < 70°C$

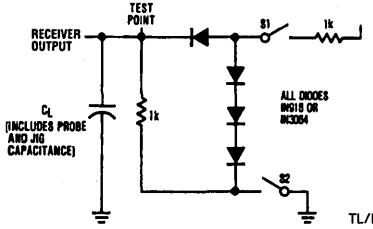
Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PLH}	Driver Input to Output	$R_{L_{DIFF}} = 60\Omega$, $C_{L1} = C_{L2} = 100$ pF *(Figures 3 and 5)*		22		ns
t_{PHL}	Driver Input to Output			22		ns
t_{SKEW}	Driver Output to Output			8		ns
t_r	Driver Rise Time	$R_{L_{DIFF}} = 60\Omega$, $C_{L1} = C_{L2} = 100$ pF *(Figures 3 and 5)*		10		ns
t_f	Driver Fall Time			10		ns
t_{ZH}	Driver Enable to Output High	$C_L = 100$ pF *(Figures 4 and 6)* S1 Open		35		ns
t_{ZL}	Driver Enable to Output Low	$C_L = 100$ pF *(Figures 4 and 6)* S2 Open		35		ns
t_{LZ}	Driver Disable Time from Low	$C_L = 15$ pF *(Figures 4 and 6)* S2 Open		15		ns
t_{HZ}	Driver Disable Time from High	$C_L = 15$ pF *(Figures 4 and 6)* S1 Open		15		ns
t_{PLH}	Receiver Input to Output	$C_L = 15$ pF *(Figures 2 and 7)* S1 and S2 Closed		25		ns
t_{PHL}	Receiver Input to Output			25		ns
t_{ZL}	Receiver Enable to Output Low	$C_L = 15$ pF *(Figures 2 and 8)* S2 Open		15		ns
t_{ZH}	Receiver Enable to Output High	$C_L = 15$ pF *(Figures 2 and 8)* S1 Open		15		ns
t_{LZ}	Receiver Disable from Low	$C_L = 15$ pF *(Figures 2 and 8)* S2 Open		12		ns
t_{HZ}	Receiver Disable from High	$C_L = 15$ pF *(Figures 2 and 8)* S1 Open		12		ns

AC Test Circuits



TL/F/8759–2

FIGURE 1



TL/F/8759–3

Note: S1 and S2 of load circuit are closed except as otherwise mentioned.

FIGURE 2

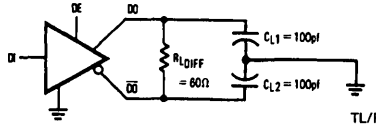


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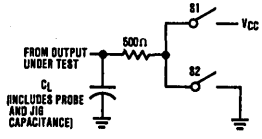
FIGURE 3



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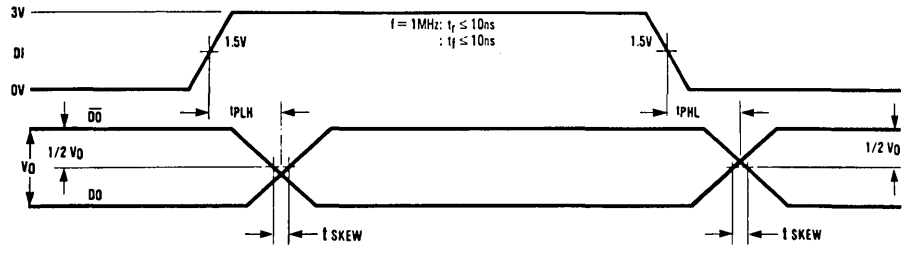
Note: Unless otherwise specified the switches are closed.

FIGURE 4

Switching Time Waveforms



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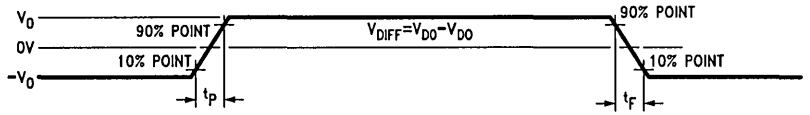

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FIGURE 5. Driver Propagation Delays

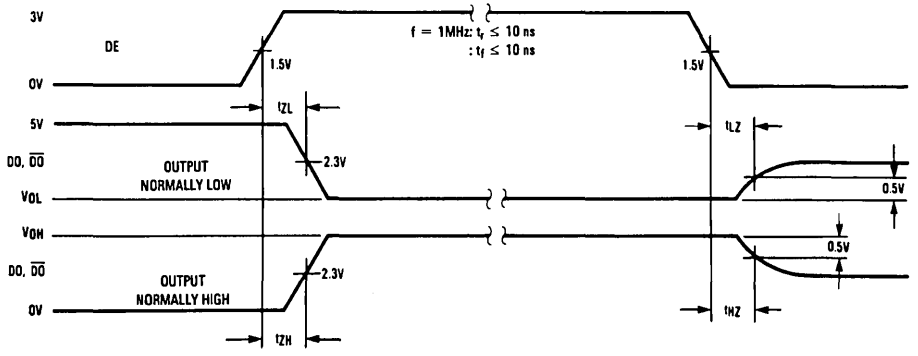

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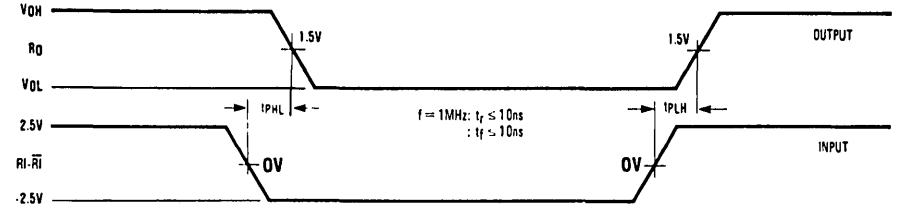
FIGURE 6. Driver Enable and Disable Times



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Note: Differential input voltage may may be realized by grounding $\overline{RI}$ and pulsing RI between +2.5V and −2.5V

FIGURE 7. Receiver Propagation Delays

Switching Time Waveforms (Continued)

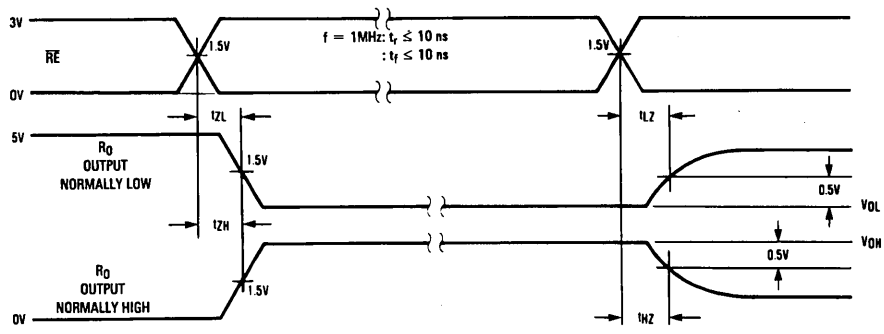

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FIGURE 8. Receiver Enable and Disable Times

Function Tables

DS75176A Transmitting

Inputs			Line Condition	Outputs	
$\overline{RE}$	DE	DI		$\overline{DO}$	DO
X	1	1	No Fault	0	1
X	1	0	No Fault	1	0
X	0	X	X	Z	Z
X	1	X	Fault	Z	Z

DS75176A Receiving

Inputs			Outputs
$\overline{RE}$	DE	RI-$\overline{RI}$	RO
0	0	≥ +0.2V	1
0	0	≤ −0.2V	0
0	0	Inputs Open**	1
1	0	X	Z

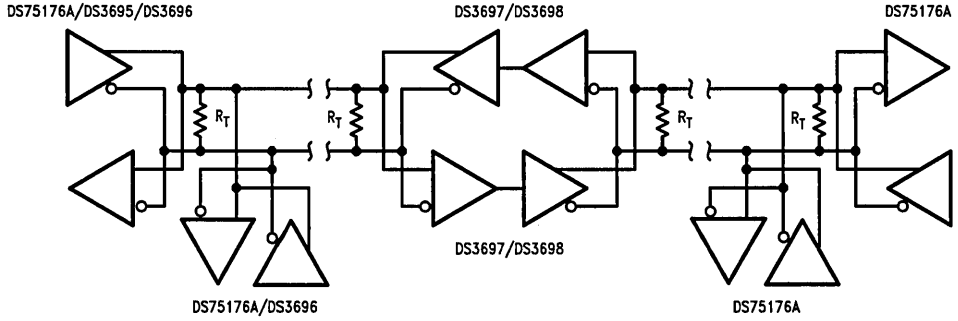
X — Don't care condition

Z — High impedance state

Fault — Improper line conditons causing excessive power dissipation in the driver, such as shorts or bus contention situations

**This is a fail safe condition

Typical Application



TL/F/8759–11

National Semiconductor Corporation

DS7820/DS8820 Dual Line Receiver

General Description

The DS7820, specified from −55°C to +125°C, and the DS8820, specified from 0°C to +70°C, are digital line receivers with two completely independent units fabricated on a single silicon chip. Intended for use with digital systems connected by twisted pair lines, they have a differential input designed to reject large common mode signals while responding to small differential signals. The output is directly compatible with TTL or LS integrated circuits.

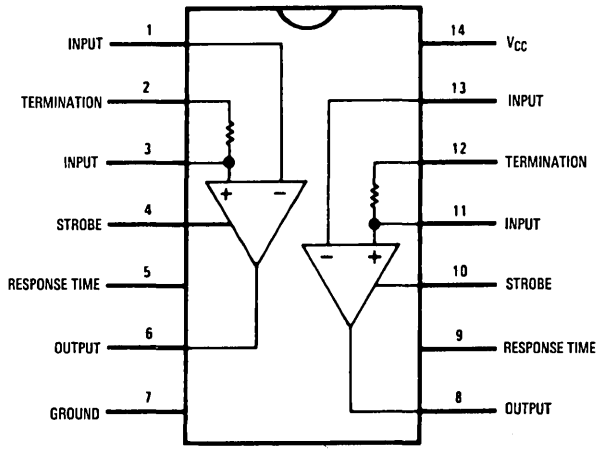
The response time can be controlled with an external capacitor to eliminate noise spikes, and the output state is determined for open inputs. Termination resistors for the twisted pair line are also included in the circuit. Both the DS7820 and the DS8820 are specified, worst case, over their full operating temperature range, for ±10-percent supply voltage variations and over the entire input voltage range.

Features

- Operation from a single +5V logic supply
- Input voltage range of ±15V
- Each channel can be strobed independently
- High input resistance
- Fan out of two with TTL integrated circuits
- Strobe low forces output to "1" state

Connection Diagram

Dual-In-Line Package



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Top View

Order Number DS7820J, DS8820J or DS8820N
See NS Package Number J14A or N14A

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	8.0V
Input Voltage	±20V
Differential Input Voltage	±20V
Strobe Voltage	8.0V
Output Sink Current	25 mA
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 4 sec.)	260°C

Maximum Power Dissipation* at 25°C

Cavity Package	1308 mW
Molded Package	1207 mW

*Derate cavity package 8.7 mW/°C above 25°C; derate molded package 9.7 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
DS7820	4.5	5.5	V
DS8820	4.75	5.25	V
Temperature (T_A)			
DS7820	−55	+125	°C
DS8820	0	+70	°C

Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{TH}	Input Threshold Voltage	$V_{CM} = 0$	−0.5	0	0.5	V
		$-15V \le V_{CM} \le 15V$	−1.0	0	1.0	V
V_{OH}	High Output Level	$I_{OUT} \le 0.2$ mA	2.5		5.5	V
V_{OL}	Low Output Level	$I_{SINK} \le 3.5$ mA	0		0.4	V
R_I-	Inverting Input Resistance		3.6	5.0		kΩ
R_I+	Non-Inverting Input Resistance		1.8	2.5		kΩ
R_T	Line Termination Resistance	$T_A = 25°C$	120	170	250	Ω
t_r	Response Time	$C_{DELAY} = 0$		40		ns
		$C_{DELAY} = 100$ pF		150		ns
I_{ST}	Strobe Current	$V_{STROBE} = 0.4V$		−1.0	−1.4	mA
		$V_{STROBE} = 5.5V$			5.0	μA
I_{CC}	Power Supply Current	$V_{IN} = 15V$		3.2	6.0	mA
		$V_{IN} = 0$		5.8	10.2	mA
		$V_{IN} = -15V$		8.3	15.0	mA
$I_{IN}+$	Non-Inverting Input Current	$V_{IN} = 15V$		5.0	7.0	mA
		$V_{IN} = 0$	−1.6	−1.0		mA
		$V_{IN} = -15V$	−9.8	−7.0		mA
$I_{IN}-$	Inverting Input Current	$V_{IN} = 15V$		3.0	4.2	mA
		$V_{IN} = 0$		0	−0.5	mA
		$V_{IN} = -15V$	−4.2	−3.0		mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

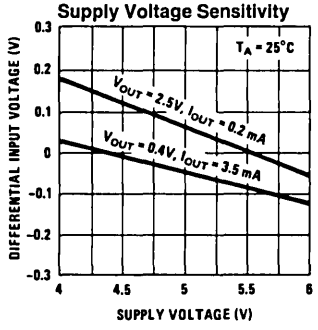
Note 2: These specifications apply for $4.5V \le V_{CC} \le 5.5V$, $-15V \le V_{CM} \le 15V$ and $-55°C \le T_A \le +125°C$ for the DS7820 or $0°C \le T_A \le +70°C$ for the DS8820 unless otherwise specified; typical values given are for $V_{CC} = 5.0V$, $T_A = 25°C$ and $V_{CM} = 0$ unless stated differently.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

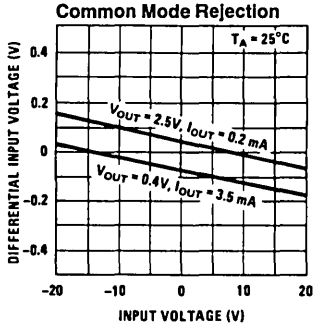
Note 4: The specifications and curves given are for one side only. Therefore, the total package dissipation and supply currents will be double the values given when both receivers are operated under identical conditions.

Typical Performance Characteristics (Note 3)

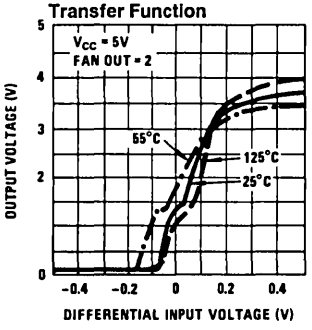
Supply Voltage Sensitivity



Common Mode Rejection



Transfer Function



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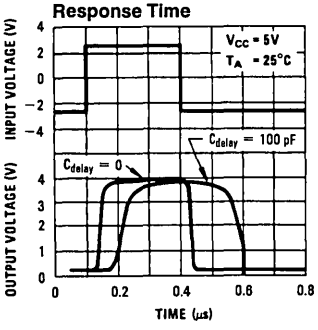
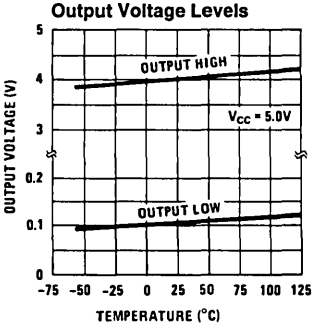
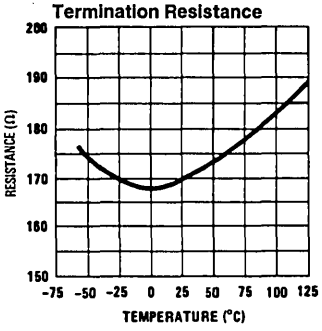
Response Time



Output Voltage Levels



Termination Resistance



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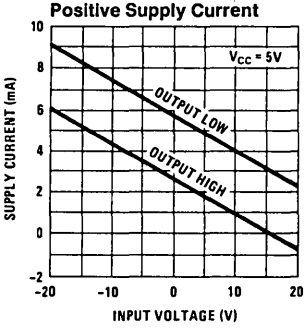
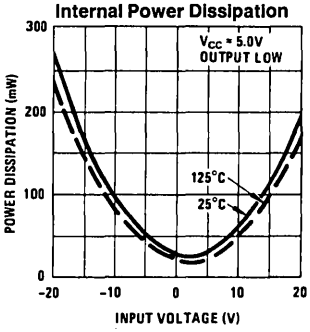
Positive Supply Current



Internal Power Dissipation



TL/F/5796–6

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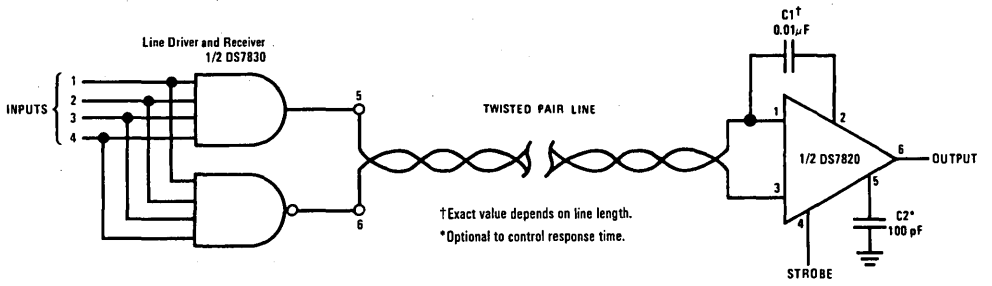
Typical Application



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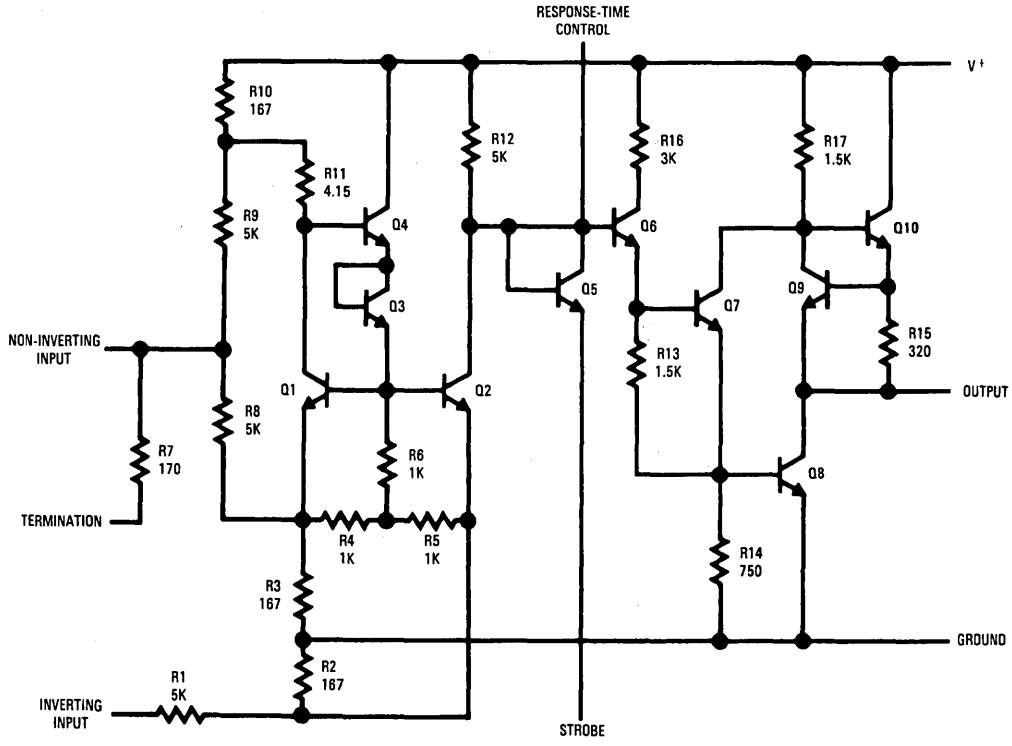
Schematic Diagram



TL/F/5796-1

National Semiconductor Corporation

DS7820A/DS8820A Dual Line Receiver

General Description

The DS7820A and the DS8820A are improved performance digital line receivers with two completely independent units fabricated on a single silicon chip. Intended for use with digital systems connected by twisted pair lines, they have a differential input designed to reject large common mode signals while responding to small differential signals. The output is directly compatible with TTL or LS integrated circuits.

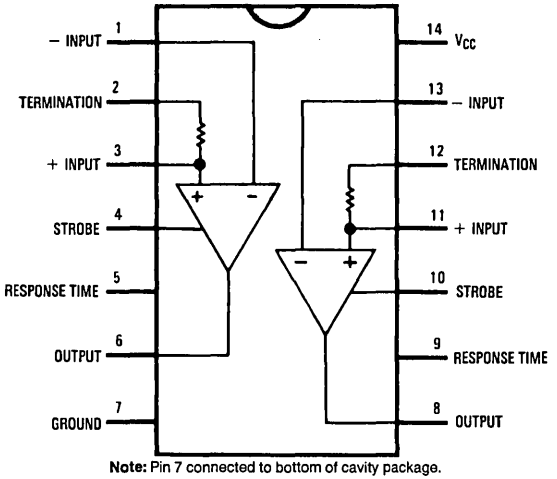
The response time can be controlled with an external capacitor to reject input noise spikes. The output state is a logic "1" for both inputs open. Termination resistors for the twisted pair line are also included in the circuit. Both the DS7820A and the DS8820A are specified, worst case, over their full operating temperature range (−55°C to +125°C and 0°C to 70°C respectively), over the entire input voltage range, for ±10% supply voltage variations.

Features

- Operation from a single +5V logic supply
- Input voltage range of ±15V
- Strobe low forces output to "1" state
- High input resistance
- Fanout of ten with TTL integrated circuits
- Outputs can be wire OR'ed
- Series 54/74 compatible

Connection Diagram

Dual-In-Line Package



Note: Pin 7 connected to bottom of cavity package. TL/F/5797–2

Top View

Order Number DS7820AJ, DS8820AJ or DS8820AN
See NS Package Number J14A or N14A

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	8.0V
Common-Mode Voltage	±20V
Differential Input Voltage	±20V
Strobe Voltage	8.0V
Output Sink Current	50 mA
Storage Temperature Range	−65°C to 150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1308 mW
Molded Package	1207 mW
Lead Temperature (Soldering, 4 sec.)	260°C

*Derate cavity package 8.7 mW/°C above 25°C; derate molded package 9.7 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
DS7820A	4.5	5.5	V
DS8820A	4.75	5.25	V
Temperature (T_A)			
DS7820A	−55	+125	°C
DS8820A	0	+70	°C

Electrical Characteristics (Notes 2, 3, and 4)

Symbol	Parameter	Conditions			Min	Typ	Max	Units
V_{TH}	Differential Threshold Voltage	I_{OUT} = −400 μA, $V_{OUT} \geq$ 2.5V	−3V ≤ V_{CM} ≤ +3V			0.06	0.5	V
			−15V ≤ V_{CM} ≤ +15V			0.06	1.0	V
		I_{OUT} = +16 mA, $V_{OUT} \leq$ 0.4V	−3V ≤ V_{CM} ≤ +3V			−0.08	−0.5	V
			−15V ≤ V_{CM} ≤ +15V			−0.08	−1.0	V
R_I^-	Inverting Input Resistance	−15V ≤ V_{CM} ≤ +15V			3.6	5		kΩ
R_I^+	Non-Inverting Input Resistance	−15V ≤ V_{CM} ≤ +15V			1.8	2.5		kΩ
R_T	Line Termination Resistance	T_A = 25°C			120	170	250	Ω
I_I^-	Inverting Input Current	V_{CM} = 15V				3.0	4.2	mA
		V_{CM} = 0V				0	−0.5	mA
		V_{CM} = −15V				−3.0	−4.2	mA
I_I^+	Non-Inverting Input Current	V_{CM} = 15V				5.0	7.0	mA
		V_{CM} = 0V				−1.0	−1.6	mA
		V_{CM} = −15V				−7.0	−9.8	mA
I_{CC}	Power Supply Current One Side Only	I_{OUT} = Logical "0"	V_{DIFF} = −1V	V_{CM} = 15V		3.9	6.0	mA
				V_{CM} = −15V		9.2	14.0	mA
			V_{DIFF} = −0.5V, V_{CM} = 0V			6.5	10.2	mA
V_{OH}	Logical "1" Output Voltage	I_{OUT} = −400 μA, V_{DIFF} = 1V			2.5	4.0	5.5	V
V_{OL}	Logical "0" Output Voltage	I_{OUT} = +16 mA, V_{DIFF} = −1V			0	0.22	0.4	V
V_{SH}	Logical "1" Strobe Input Voltage	I_{OUT} = +16 mA, $V_{OUT} \leq$ 0.4V, V_{DIFF} = −3V			2.1			V
V_{SL}	Logical "0" Strobe Input Voltage	I_{OUT} = −400 μA, $V_{OUT} \geq$ 2.5V, V_{DIFF} = −3V					0.9	V
I_{SH}	Logical "1" Strobe Input Current	V_{STROBE} = 5.5V, V_{DIFF} = 3V				0.01	5.0	μA
I_{SL}	Logical "0" Strobe Input Current	V_{STROBE} = 0.4V, V_{DIFF} = −3V				−1.0	−1.4	mA
I_{SC}	Output Short Circuit Current	V_O = 0V, V_{CC} = 5.5V, V_{STROBE} = 0V			−2.8	−4.5	−6.7	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: These specifications apply for 4.5V ≤ V_{CC} ≤ 5.5V, −15V ≤ V_{CM} ≤ 15V and −55°C ≤ T_A ≤ +125°C for the DS7820A or 4.75V ≤ V_{CC} ≤ 5.25V, 0°C ≤ T_A ≤ +70°C for the DS8820A unless otherwise specified. Typical values given are for V_{CC} = 5.0V, T_A = 25°C and V_{CM} = 0V unless stated differently.

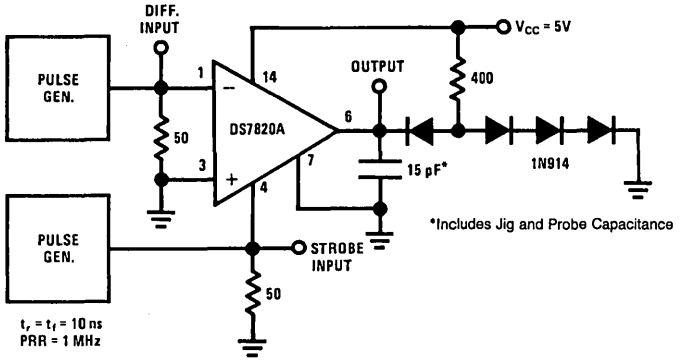
Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Only one output at a time should be shorted.

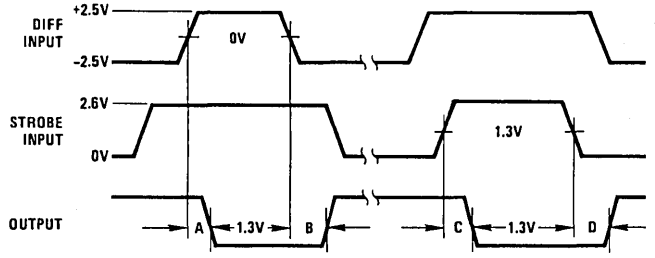
Switching Characteristics $T_A = 25°C$, $V_{CC} = 5V$, unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd0}	Propagation Delay, Differential Input to "0" Output	$R_L = 400\ \Omega$, $C_L = 15$ pF, see *Figure 1*		30	45	ns
t_{pd1}	Propagation Delay, Differential Input to "1" Output			27	40	ns
t_{pd0}	Propagation Delay, Strobe Input to "0" Output			16	25	ns
t_{pd1}	Propagation Delay, Strobe Input to "1" Output			18	30	ns

AC Test Circuit and Waveforms



TL/F/5797–7



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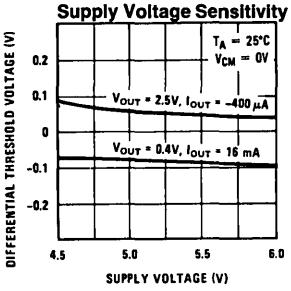
A = Differential Input to "0" Output
B = Differential Input to "1" Output
C = Strobe Input to "0" Output
D = Strobe Input to "1" Output

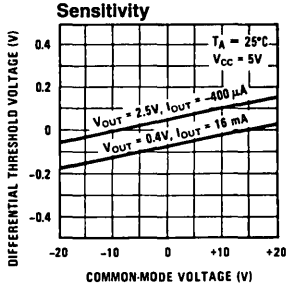
FIGURE 1

Typical Performance Characteristics (Note 3)

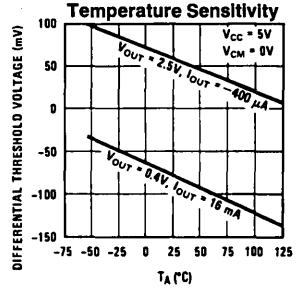
Supply Voltage Sensitivity



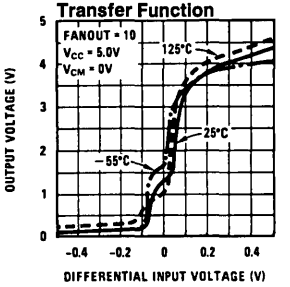
Common-Mode Voltage Sensitivity



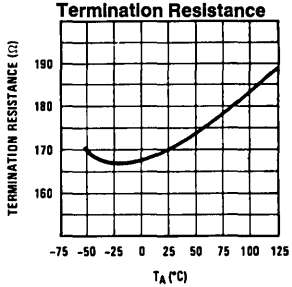
Temperature Sensitivity



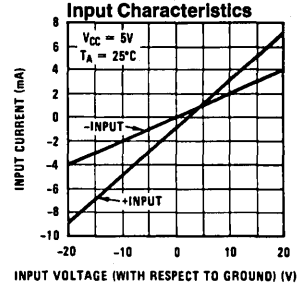
Transfer Function



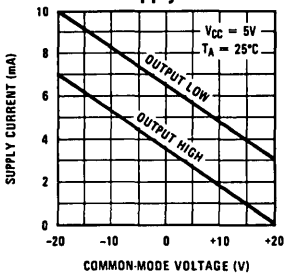
Termination Resistance



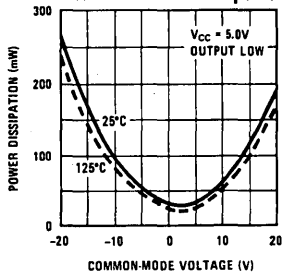
Input Characteristics



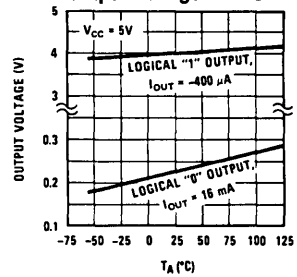
Power Supply Current



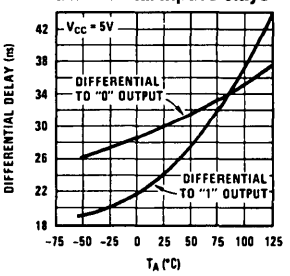
Internal Power Dissipation



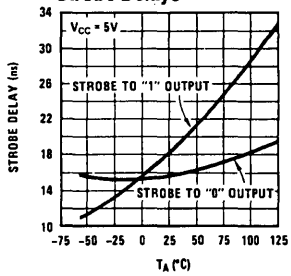
Output Voltage Levels



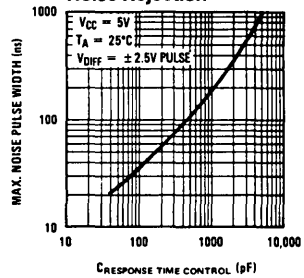
Differential Input Delays



Strobe Delays



Noise Rejection



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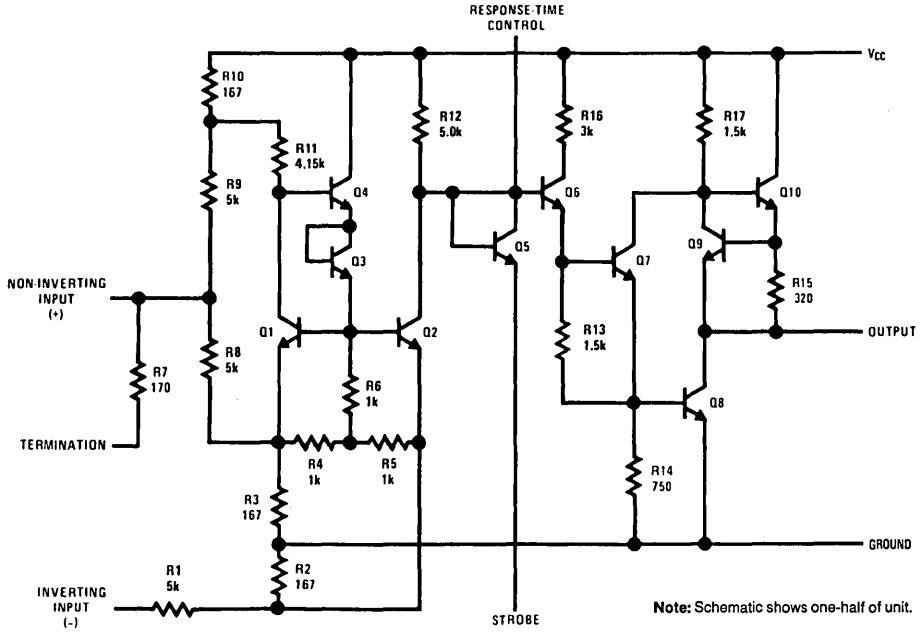
Schematic Diagram

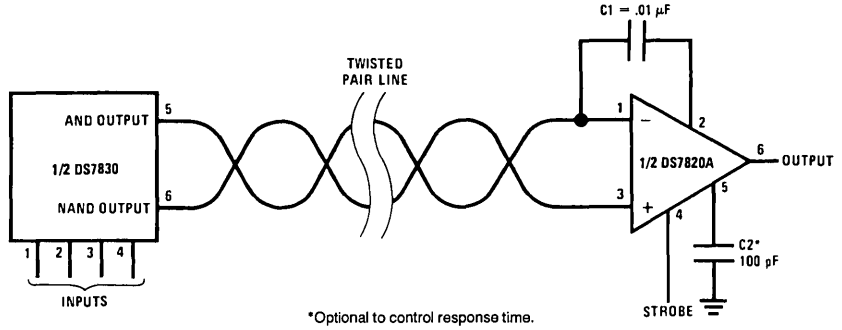


Note: Schematic shows one-half of unit.

TL/F/5797–1

Typical Applications

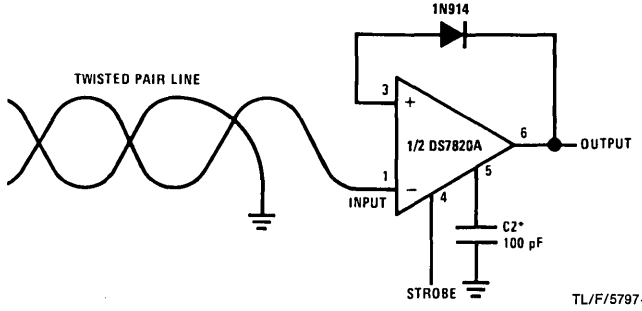
Differential Line Driver and Receiver



*Optional to control response time.

TL/F/5797–3

Single Ended (EIA-RS232C) Receiver with Hysteresis



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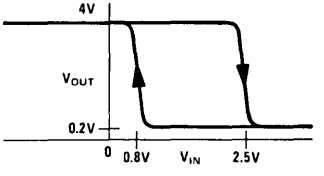


TL/F/5797–5

(Output = "1" for Open Input)

National Semiconductor Corporation

DS78C20/DS88C20 Dual CMOS Compatible Differential Line Receiver

General Description

The DS78C20 and DS88C20 are high performance, dual differential, CMOS compatible line receivers for both balanced and unbalanced digital data transmission. The inputs are compatible with EIA and Federal Standards.

Input specifications meet or exceed those of the popular DS7820/DS8820 line receiver, and the pinout is identical.

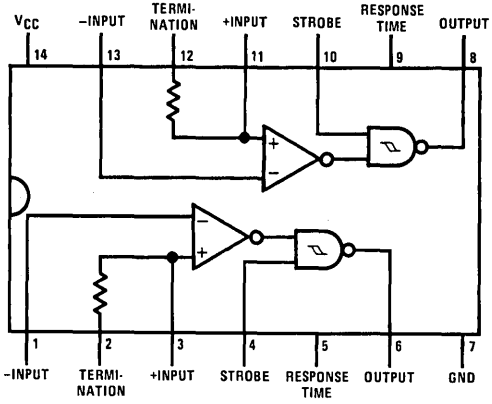
A response pin is provided for controlling sensitivity to input noise spikes with an external capacitor. Each receiver includes a 180Ω terminating resistor, which may be used optionally on twisted pair lines. The DS78C20 is specified over a −55°C to +125°C operating temperature range, and the DS88C20 over a 0°C to +70°C range.

Features

- Meets requirements of EIA Standards RS-232-C RS-422 and RS-423, and Federal Standards 1020 and 1030
- Input voltage range of ±15V (differential or common-mode)
- Separate strobe input for each receiver
- ½ V_{CC} strobe threshold for CMOS compatibility
- 5k typical input impedance
- 50 mV input hysteresis
- 200 mV input threshold
- Operation voltage range = 4.5V to 15V
- DS7830/DS8830 or MM78C30/MM88C30 recommended driver

Connection Diagram

Dual-In-Line Package



TL/F/5798–1

Top View

Order Number DS78C20J, DS88C20J or DS88C20N
See NS Package Number J14A or N14A

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	18V
Common-Mode Voltage	±25V
Differential Input Voltage	±25V
Strobe Voltage	18V
Output Sink Current	50 mA
Maximum Power Dissipation* at 25°C	
Cavity Package	1364 mW
Molded Package	1280 mW
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 4 seconds)	260°C

*Derate cavity package 9.1 mW/°C; derate molded package 10.2 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	15	V
Temperature (T_A)			
DS78C20	−55	+125	°C
DS88C20	0	+70	°C
Common-Mode Voltage (V_{CM})	−15	+15	V

Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{TH}	Differential Threshold Voltage	I_{OUT} = −200 μA, $V_{OUT} \geq V_{CC}$ −1.2V	−10V ≤ V_{CM} ≤ 10V		0.06	0.2	V
			−15V ≤ V_{CM} ≤ 15V		0.06	0.3	V
		I_{OUT} = 1.6 mA, $V_{OUT} \leq$ 0.5V	−10V ≤ V_{CM} ≤ 10V		−0.08	−0.2	V
			−15V ≤ V_{CM} ≤ 15V		−0.08	−0.3	V
R_{IN}	Input Resistance	−15V ≤ V_{CM} ≤ 15V			5		kΩ
R_T	Line Termination Resistance	T_A = 25°C		100	180	300	Ω
I_{IND}	Data Input Current (Unterminated)	V_{CM} = 10V			2	3.1	mA
		V_{CM} = 0V			0	−0.5	mA
		V_{CM} = −10V			−2	−3.1	mA
V_{THB}	Input Balance	I_{OUT} = 200 μA, $V_{OUT} \geq$ V_{CC} −1.2V, R_S = 500Ω, (Note 5)	−7V ≤ V_{CM} ≤ 7V		0.1	0.4	V
		I_{OUT} = 1.6 mA, $V_{OUT} \leq$ 0.5V, R_S = 500Ω, (Note 5)	−7V ≤ V_{CM} ≤ 7V		−0.1	−0.4	V
V_{OH}	Logical "1" Output Voltage	I_{OUT} = −200 μA, V_{DIFF} = 1V		V_{CC} − 1.2	V_{CC} − 0.75		V
V_{OL}	Logical "0" Output Voltage	I_{OUT} = 1.6 mA, V_{DIFF} = −1V			0.25	0.5	V
I_{CC}	Power Supply Current	15V ≤ V_{CM} ≤ −15V, V_{DIFF} = −0.5V (Both Receivers)	V_{CC} = 5.5V		8	15	mA
			V_{CC} = 15V		15	30	mA
$I_{IN(1)}$	Logical "1" Strobe Input Current	V_{STROBE} = 15V, V_{DIFF} = 3V	V_{CC} = 15V		15	100	μA
$I_{IN(0)}$	Logical "0" Strobe Input Current	V_{STROBE} = 0V, V_{DIFF} = −3V	V_{CC} = 15V		−0.5	−100	μA
V_{IH}	Logical "1" Strobe Input Voltage	I_{OUT} = 1.6 mA, $V_{OL} \leq$ 0.5V	V_{CC} = 5V	3.5	2.5		V
			V_{CC} = 10V	8.0	5.0		V
			V_C = 15V	12.5	7.5		V
V_{IL}	Logical "0" Strobe Input Voltage	I_{OUT} = −200 μA, V_{OH} = V_{CC} −1.2V	V_{CC} = 5V		2.5	1.5	V
			V_{CC} = 10V		5.0	2.0	V
			V_{CC} = 15V		7.5	2.5	V
I_{OS}	Output Short-Circuit Current	V_{OUT} = 0V, V_{CC} = 15V, V_{STROBE} = 0V, (Note 4)		−5	−20	−40	mA

1

Switching Characteristics V_{CC} = 5V, T_A = 25°C

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$t_{pd0(D)}$	Differential Input to "0" Output	C_L = 50 pF		60	100	ns
$t_{pd1(D)}$	Differential Input to "1" Output	C_L = 50 pF		100	150	ns
$t_{pd0(S)}$	Strobe Input to "0" Output	C_L = 50 pF		30	70	ns
$t_{pd1(S)}$	Strobe Input to "1" Output	C_L = 50 pF		100	150	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS78C20 and across the 0°C to +70°C range for the DS88C20. All typical values are for T_A = 25°C, V_{CC} = 5V and V_{CM} = 0V.

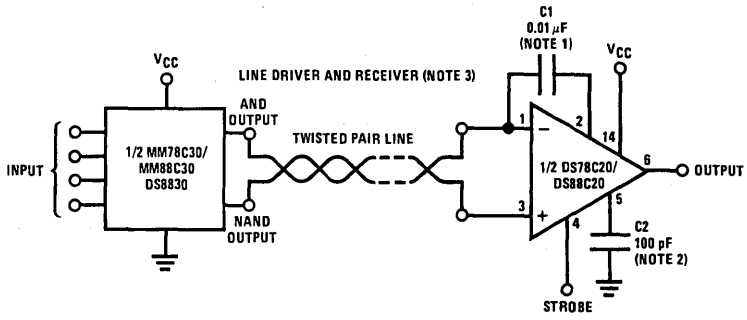
Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Only one output at a time should be shorted.

Note 5: Refer to EIA-RS-422 for exact conditions.

Typical Applications

RS-422/RS-423 Application



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Note 1: (Optional internal termination resistor.)

a) Capacitor in series with internal line termination resistor, terminates the line and saves termination power. Exact value depends on line length.

b) Pin 1 connected to pin 2; terminates the line.

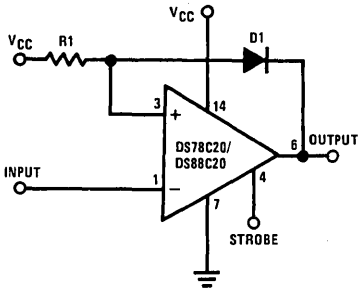
c) Pin 2 open; no internal line termination.

d) Transmission line may be terminated elsewhere or not at all.

Note 2: Optional to control response time.

Note 3: V_{CC} 4.5V to 15V for the DS78C20. For further information on line drivers and line receivers, refer to applicaton notes AN-22, AN-83 and AN-108.

RS-232-C Application with Hysteresis



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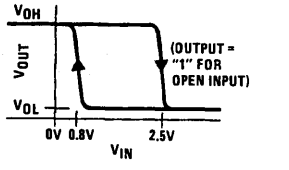
For signals which require fail-safe or have slow rise and fall times, use R1 and D1 as shown above. Otherwise, the positive input (pin 3 or 11) may be connected to ground.

V_{CC}	R1 ±5%
5V	4,3 kΩ
10V	15 kΩ
15V	24 kΩ



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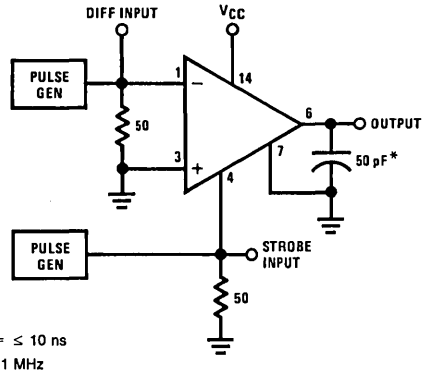
AC Test Circuit



$t_r = t_f = \leq 10$ ns
PRR = 1 MHz

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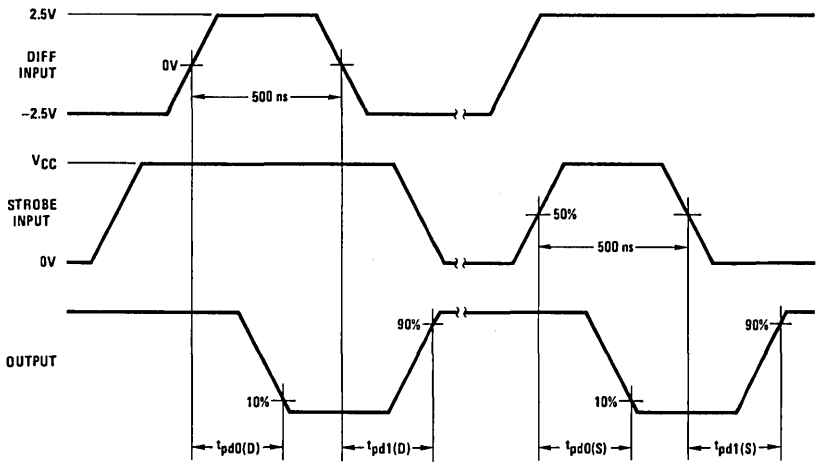
*Includes probe and jig capacitance

Switching Time Waveforms



TL/F/5798–6

National Semiconductor Corporation

DS7830/DS8830 Dual Differential Line Driver

General Description

The DS7830/DS8830 is a dual differential line driver that also performs the dual four-input NAND or dual four-input AND function.

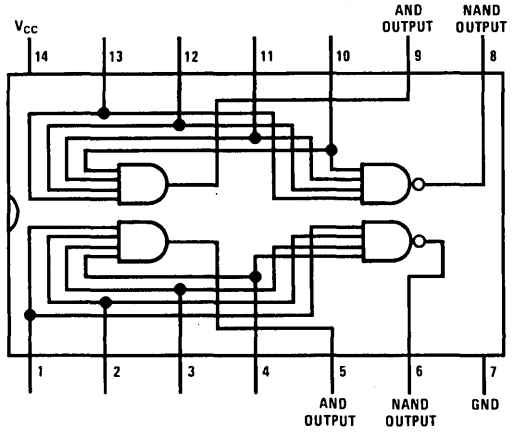
TTL (Transistor-Transistor-Logic) multiple emitter inputs allow this line driver to interface with standard TTL systems. The differential outputs are balanced and are designed to drive long lengths of coaxial cable, strip line, or twisted pair transmission lines with characteristic impedances of 50Ω to 500Ω. The differential feature of the output eliminates troublesome ground-loop errors normally associated with single-wire transmissions.

Features

- Single 5V power supply
- Diode protected outputs for termination of positive and negative voltage transients
- Diode protected inputs to prevent line ringing
- High speed
- Short circuit protection

Connection Diagram

Dual-In-Line and Flat Package



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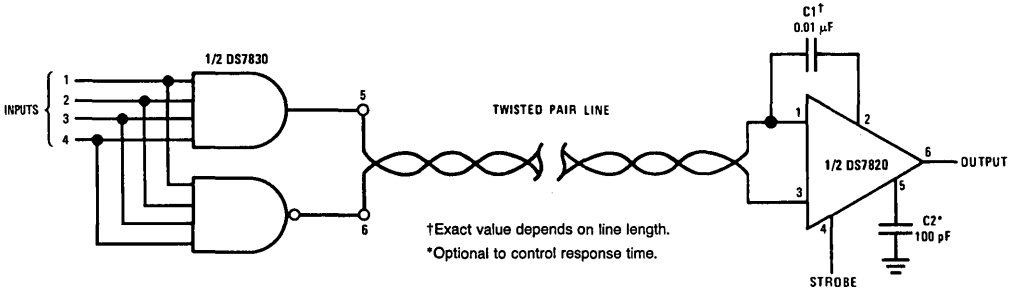
Top View

Order Number DS7830J, DS8830J or DS8830N
See NS Package Number J14A or N14A

Typical Application

Digital Data Transmission



†Exact value depends on line length.
*Optional to control response time.

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Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

V_{CC}	7.0V
Input Voltage	5.5V
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 4 sec.)	260°C
Output Short Circuit Duration (125°C)	1 second
Maximum Power Dissipation* at 25°C	
Cavity Package	1308 mW
Molded Package	1207 mW

*Derate cavity package 8.7 mW/°C above 25°C; derate molded package 9.7 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
DS8730	4.5	5.5	V
DS8830	4.75	5.25	V
Temperature (T_A)			
DS7830	−55	+125	°C
DS8830	0	+70	°C

Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IH}	Logical "1" Input Voltage			2.0			V
V_{IL}	Logical "0" Input Voltage					0.8	V
V_{OH}	Logical "1" Output Voltage	V_{IN} = 0.8V	I_{OUT} = −0.8 mA	2.4			V
			I_{OUT} = 40 mA	1.8	3.3		V
V_{OL}	Logical "0" Output Voltage	V_{IN} = 2.0V	I_{OUT} = 32 mA		0.2	0.4	V
			I_{OUT} = 40 mA		0.22	0.5	V
I_{IH}	Logical "1" Input Current	V_{IN} = 2.4V				120	μA
		V_{IN} = 5.5V				2	mA
I_{IL}	Logical "0" Input Current	V_{IN} = 0.4V				−4.8	mA
I_{SC}	Output Short Circuit Current	V_{CC} = 5.0V, T_A = 125°C, (Note 4)		−40	−100	−120	mA
I_{CC}	Supply Current	V_{IN} = 5.0V, (Each Driver)			11	18	mA
V_I	Input Clamp	V_{CC} = Min, I_{IN} = − 12 mA			−1.0	−1.5	V

Switching Characteristics T_A = 25°C, V_{CC} = 5V, unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd1}	Propagation Delay AND Gate	R_L = 400Ω, C_L = 15 pF *(Figure 1)*		8	12	ns
t_{pd0}				11	18	ns
t_{pd1}	Propagation Delay NAND Gate	R_L = 400Ω, C_L = 15 pF *(Figure 1)*		8	12	ns
t_{pd0}				5	8	ns
t_1	Differential Delay	Load, 100Ω and 5000 pF, *(Figure 2)*		12	16	ns
t_2	Differential Delay	Load, 100Ω and 5000 pF, *(Figure 2)*		12	16	ns

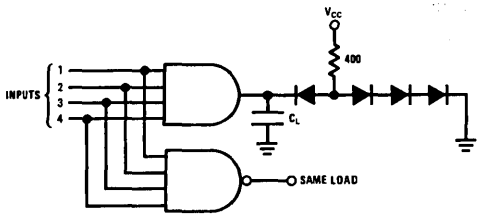
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS7830 and across the 0°C to +70°C range for the DS8830. Typical values for T_A = 25°C and V_{CC} = 5.0V.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Only one output at a time should be shorted.

AC Test Circuit and Switching Time Waveforms



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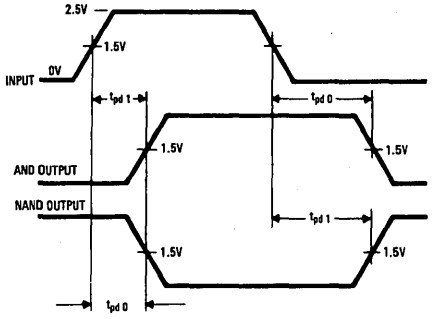

f = 1 MHz
$t_r = t_f \leq 10$ ns (10% to 90%)
Duty cycle = 50%

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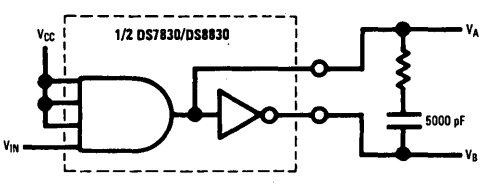
FIGURE 1



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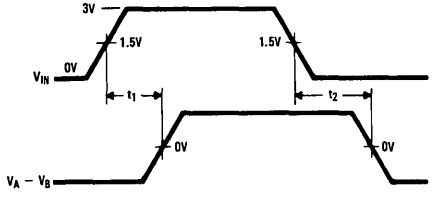

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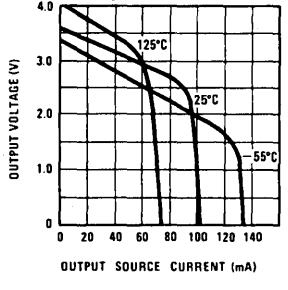
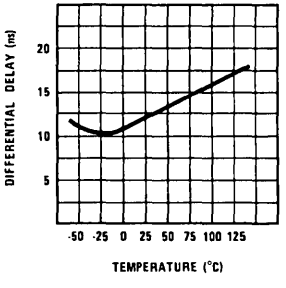
FIGURE 2

Typical Performance Characteristics

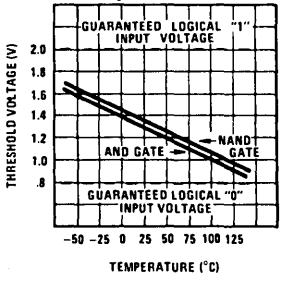
Output High Voltage (Logical "1") vs Ouput Current



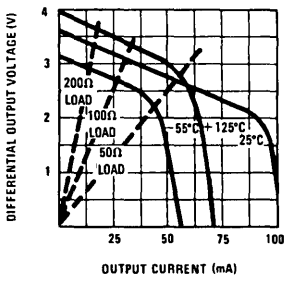
Differential Delay vs Temperature



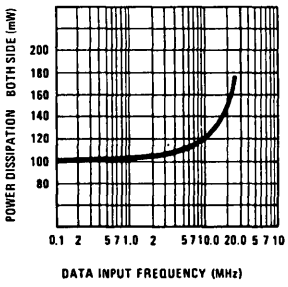
Threshold Voltage vs Temperature



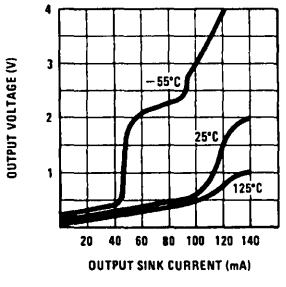
Differential Output Voltage ($|V_{AND} - V_{NAND}|$) vs Differential Output Current



Power Dissipation (No Load) vs Data Input Frequency



Output Low Voltage (Logical "0") vs Output Current



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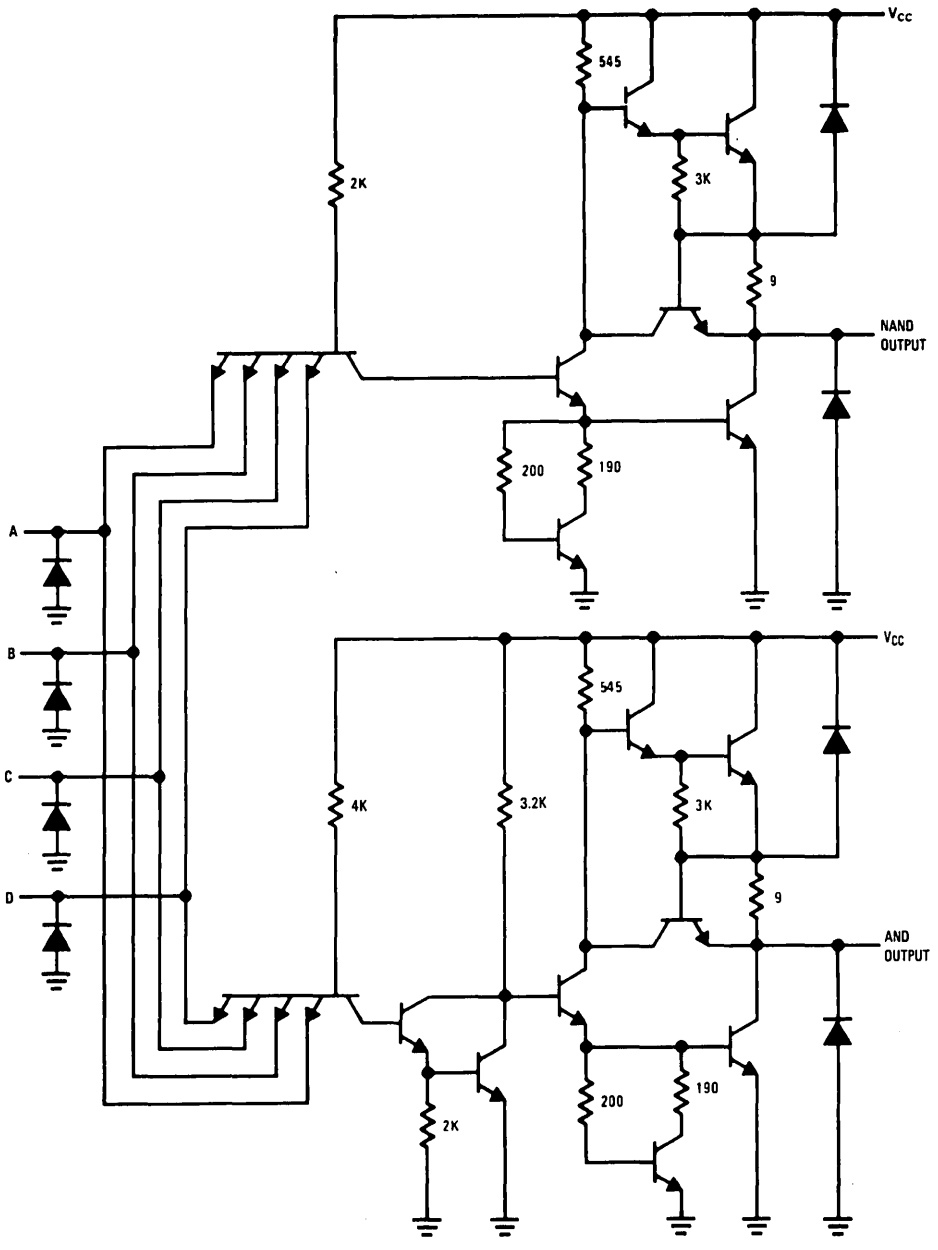
Schematic Diagram



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*2 Per Package

National Semiconductor Corporation

DS7831/DS8831/DS7832/DS8832 Dual TRI-STATE® Line Driver

General Description

Through simple logic control, the DS7831/DS8831, DS7832/DS8832 can be used as either a quad single-ended line driver or a dual differential line driver. They are specifically designed for party line (bus-organized) systems. The DS7832/DS8832 does not have the V_{CC} clamp diodes found on the DS7831/DS8831.

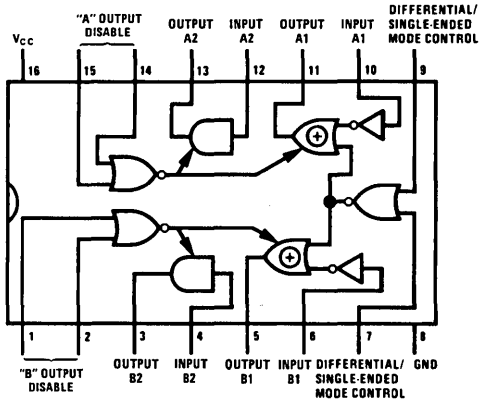
The DS7831 and DS7832 are specified for operation over the −55°C to +125°C military temperature range. The DS8831 and DS8832 are specified for operation over the 0°C to +70°C temperature range.

Features

- Series 54/74 compatible
- 17 ns propagation delay
- Very low output impedance—high drive capability
- 40 mA sink and source currents
- Gating control to allow either single-ended or differential operation
- High impedance output state which allows many outputs to be connected to a common bus line

Connection and Logic Diagram

Dual-In-Line Package



TL/F/5800–1

Top View

Order Number DS7831J, DS8831J, DS7832J, DS8832J, DS8831N or DS8832N
See NS Package Number J16A or N16A

Truth Table (Shown for A Channels Only)

"A" Output Disable		Differential/ Single-Ended Mode Control		Input A1	Output A1	Input A2	Output A2
0	0	0	0	Logical "1" or Logical "0"	Same as Input A1	Logical "1" or Logical "0"	Same as Input A2
0	0	X 1	1 X	Logical "1" or Logical "0"	Opposite of Input A1	Logical "1" or Logical "0"	Same as Input A2
1 X	X 1	X	X	X	High Impedance State	X	High Impedance State

X = Don't Care

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5.5V
Output Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 4 sec.)	260°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1433 mW
Molded Package	1362 mW

*Derate cavity package 9.6 mW/°C above 25°C; derate molded package 10.9 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
DS7831/DS7832	4.5	5.5	V
DS8831/DS8832	4.75	5.25	V
Temperature (T_A)			
DS7831/DS7832	−55	+125	°C
DS8831/DS8832	0	+70	°C

Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions			Min	Typ	Max	Units
V_{IH}	Logical "1" Input Voltage	V_{CC} = Min			2.0			V
V_{IL}	Logical "0" Input Voltage	V_{CC} = Min					0.8	V
V_{OH}	Logical "1" Output Voltage	DS7831/DS7832	V_{CC} = Min	I_O = −40 mA	1.8	2.3		V
				I_O = −2 mA	2.4	2.7		V
		DS8831/DS8832		I_O = −40 mA	1.8	2.5		V
				I_O = −5.2 mA	2.4	2.9		V
V_{OL}	Logical "0" Output Voltage	DS7831/DS7832	V_{CC} = Min	I_O = 40 mA		0.29	0.50	V
				I_O = 32 mA			0.40	V
		DS8831/DS8832		I_O = 40 mA		0.29	0.50	V
				I_O = 32 mA			0.40	V
I_{IH}	Logical "1" Input Current	V_{CC} = Max	DS7831/DS7832, V_{IN} = 55.5V				1	mA
			DS8831/DS8832, V_{IN} = 2.4V				40	μA
I_{IL}	Logical "0" Input Current	V_{CC} = Max, V_{IN} = 0.4V				−1.0	−1.6	mA
I_{OD}	Output Disable Current	V_{CC} = Max, V_O = 2.4V or 0.4V			−40		40	μA
I_{SC}	Output Short Circuit Current	V_{CC} = Max, (Note 4)			−40	−100	−120	mA
I_{CC}	Supply Current	V_{CC} = Max in TRI-STATE				65	90	mA
V_{CLI}	Input Diode Clamp Voltage	V_{CC} = 5.0V, T_A = 25°C, I_{IN} = −12 mA					−1.5	V
V_{CLO}	Output Diode Clamp Voltage	V_{CC} = 5.0V, T_A = 25°C	I_{OUT} = −12 mA	DS7831/DS8831 DS7832/DS8832			−1.5	V
			I_{OUT} = 12 mA	DS7831/DS8831			V_{CC} + 1.5	V

1

Switching Characteristics $T_A = 25°C$, $V_{CC} = 5V$, unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd0}	Propagation Delay to a Logical "0" from Inputs A1, A2, B1, B2 Differential Single-ended Mode Control to Outputs	(See *Figures 4* and *5*)		13	25	ns
t_{pd1}	Propagation Delay to a Logical "1" from Inputs A1, A2, B1, B2 Differential Single-ended Mode Control to Outputs			13	25	ns
t_{1H}	Delay from Disable Inputs to High Impedance State (from Logical "1" Level)			6	12	ns
t_{0H}	Delay from Disable Inputs to High Impedance State (from Logical "0" Level)			14	22	ns
t_{H1}	Propagation Delay from Disable Inputs to Logical "1" Level (from High Impedance State)			14	22	ns
t_{H0}	Propagation Delay from Disable Inputs to Logical "0" Level (from High Impedance State)			18	27	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS7831 and DS7832 and across the 0°C to +70°C range for the DS8831 and DS8832. All typical values are for $T_A = 25°C$ and $V_{CC} = 5V$.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltage referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Applies for $T_A = 125°C$ only. Only one output should be shorted at a time.

Mode of Operation

To operate as a quad single-ended line driver apply logical "0"'s to to the output disable pins (to keep the outputs in the normal low impedance mode) and apply logical "0"s to both Differential/Single-ended Mode Control inputs. All four channels will then operate independently and no signal inversion will occur between inputs and outputs.

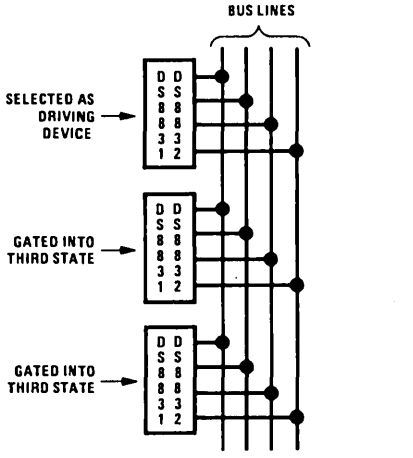
To operate as a dual differential line driver apply logical "0"s to the Output Disable pins and apply at least one logical "1" to the Differential/Single-ended Mode Control inputs.

The inputs to the A channels should be connected together and the inputs to the B channels should be connected together.

In this mode the signals applied to the resulting inputs will pass non-inverted on the A_2 and B_2 outputs and inverted on the A_1 and B_1 outputs.

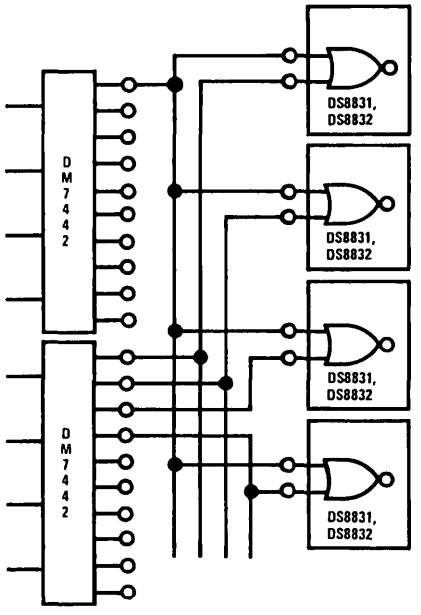
When operating in a bus-organized system with outputs tied directly to outputs of other DS7831/DS8831's, DS7832/DS8832's *(Figure 1),* all devices except one must be placed in the "high impedance" state. This is accomplished by ensuring that a logical "1" is applied to at least one of the Output Disable pins of each device which is to be in the "high impedance" state. A NOR gate was purposely chosen for this function since it is possible with only two DM5442/DM7442, BCD-to-decimal decoders, to decode as many as 100 DS7831/DS8831's, DS7832/DS8832's *(Figure 2).*

The unique device whose Disable inputs receive two logical "0" levels assumes the normal low impedance output state, providing good capacitive drive capability and waveform integrity especially during the transition from the logical "0" to logical "1" state. The other outputs—in the high impedance state—take only a small amount of leakage current from the low impedance outputs. Since the logical "1" output current from the selected device is 100 times that of a conventional Series 54/74 device (40 mA vs. 400 μA), the output is easily able to supply that leakage current for several hundred other DS7831/DS8831's, DS7832/DS8832's and still have available drive for the bus line *(Figure 3).*



TL/F/5800–2

FIGURE 1



TL/F/5800–3

FIGURE 2

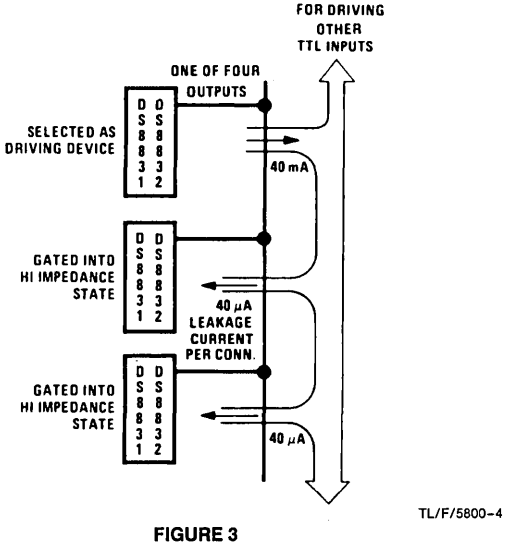


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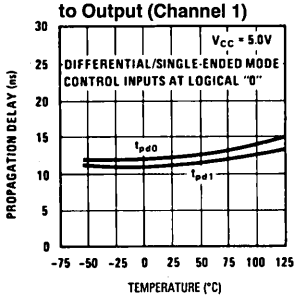
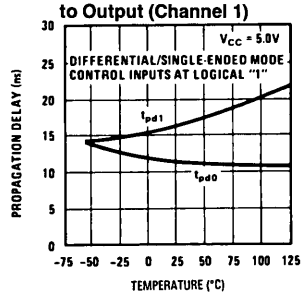
FIGURE 3

Typical Performance Characteristics

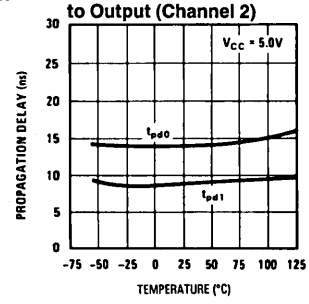
Propagation Delay from Input to Output (Channel 1)



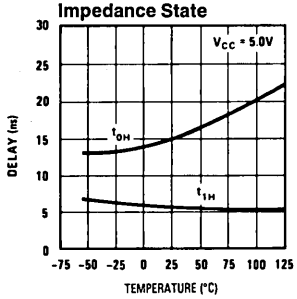
Propagation Delay from Input to Output (Channel 1)



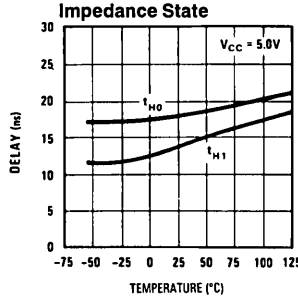
Propagation Delay from Input to Output (Channel 2)



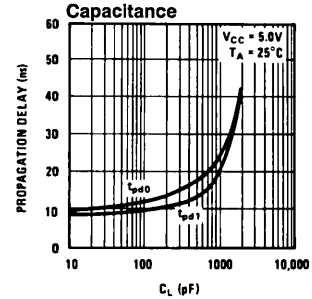
Delay from Disable to High Impedance State



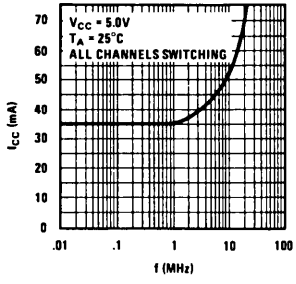
Delay from Disable to Low Impedance State



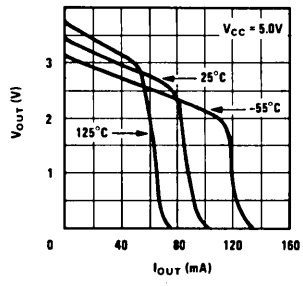
Propagation Delay vs Load Capacitance



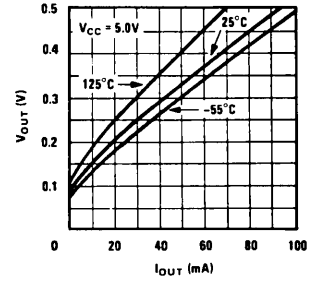
Total Supply Current vs Frequency



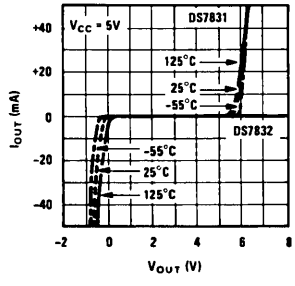
Logical "1" Output Voltage vs Source Current



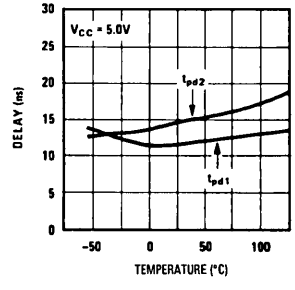
Logical "0" Output Voltage vs Sink Current



I_{OUT} vs V_{OUT} High Impedance Output State



Propagation Delay in Differential Mode



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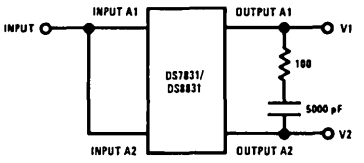
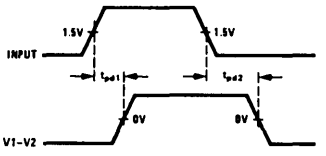
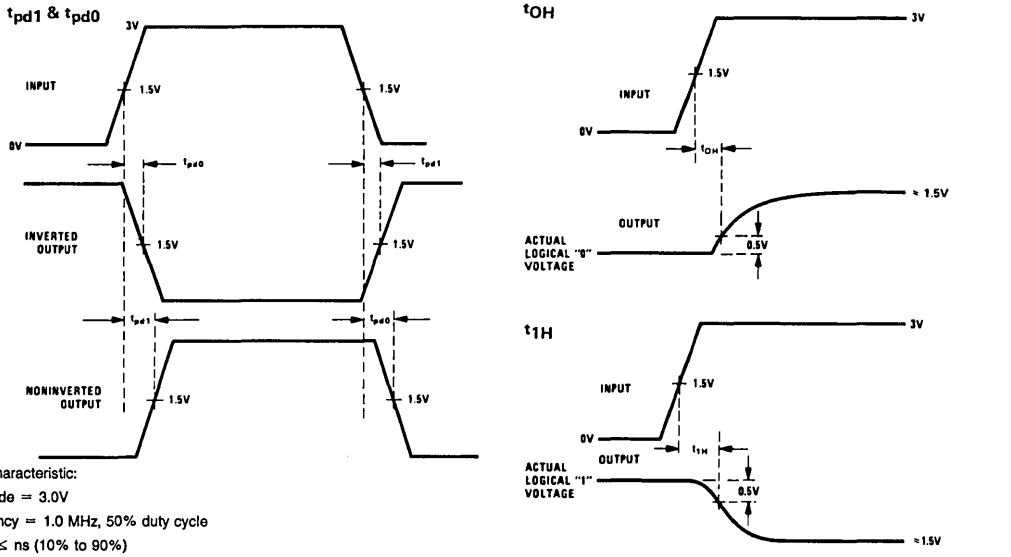
Typical Performance Characteristics (Continued)





TL/F/5800-6

Switching Time Waveforms



Input characteristic:
Amplitude = 3.0V
Frequency = 1.0 MHz, 50% duty cycle
$t_r = t_f \leq$ ns (10% to 90%)

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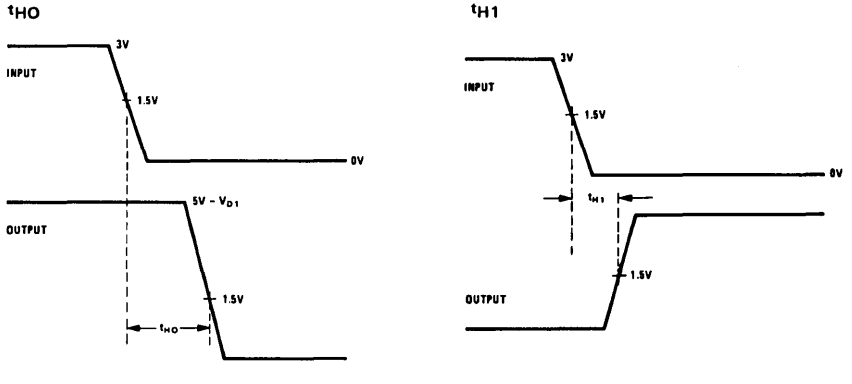

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FIGURE 4

AC Load Circuit

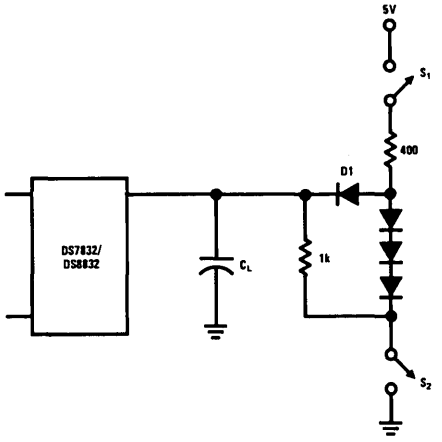

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FIGURE 5

Symbol	Switch S1	Switch S2	C_L
t_{pd1}	closed	closed	50 pF
t_{pd0}	closed	closed	50 pF
t_{0H}	closed	closed	*5 pF
t_{1H}	closed	closed	*5 pF
t_{H0}	closed	open	50 pF
t_{H1}	open	closed	50 pF

*Jig capacitance

National Semiconductor Corporation

DS78C120/DS88C120 Dual CMOS Compatible Differential Line Receiver

General Description

The DS78C120 and DS88C120 are high performance, dual differential, CMOS compatible line receivers for both balanced and unbalanced digital data transmission. The inputs are compatible with EIA, Federal and MIL standards.

Input specifications meet or exceed those of the popular DS7820/DS8820 line receiver.

The line receiver will discriminate a ±200 mV input signal over a common-mode range of ±10V and a ±300 mV signal over a range of ±15V.

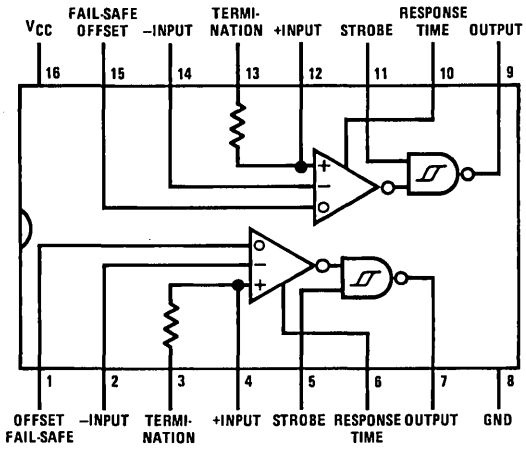
Circuit features include hysteresis and response control for applications where controlled rise and fall times and/or high frequency noise rejection are desirable. Threshold offset control is provided for fail-safe detection, should the input be open or short. Each receiver includes a 180Ω terminating resistor and the output gate contains a logic strobe for time discrimination. The DS78C120 is specified over a −55°C to +125°C temperature range and the DS88C120 from 0°C to +70°C.

Features

- Full compatibility with EIA Standards RS232-C, RS422 and RS423, Federal Standards 1020, 1030 and MIL-188-114
- Input voltage range of ±15V (differential or common-mode)
- Separate strobe input for each receiver
- 1/2 V_{CC} strobe threshold for CMOS compatibility
- 5k typical input impedance
- 50 mV input hysteresis
- 200 mV input threshold
- Operation voltage range = 45.V to 15V
- Separate fail-safe mode

Connection Diagram

Dual-In-Line Package



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Top View

Order Number DS78C120J, DS88C120J or DS88C120N
See NS Package Number J16A or N16A

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	18V
Input Voltage	±25V
Strobe Voltage	18V
Output Sink Current	50 mA
Maximum Power Dissipation* at 25°C	
Cavity Package	1433 mW
Molded Package	1362 mW

*Derate cavity package 9.6 mW/°C above 25°C; derate molded package 10.9 mW/°C above 25°C.

Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 4 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	15	V
Temperature (T_A)			
DS78C120	−55	+125	°C
DS88C120	0	+70	°C
Common-Mode Voltage (V_{CM})	−15	+15	V

Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{TH}	Differential Threshold Voltage	$I_{OUT} = -200\ \mu A$, $V_{OUT} \geq V_{CC} - 1.2V$	$-7V \leq V_{CM} \leq 7V$		0.06	0.2	V
			$-15V \leq V_{CM} \leq 15V$		0.06	0.3	V
V_{TL}	Differential Threshold Voltage	$I_{OUT} = 1.6\ mA, V_{OUT} \leq 0.5V$	$-7V \leq V_{CM} \leq 7V$		−0.08	−0.2	V
			$-15V \leq V_{CM} \leq 15V$		−0.08	−0.3	V
V_{TH}	Differential Threshold Voltage Fail-Safe	$I_{OUT} = -200\ \mu A$, $V_{OUT} \geq V_{CC} - 1.2V$	$-7V \leq V_{CM} \leq 7V$		0.47	0.7	V
V_{TL}	Offset = 5V	$I_{OUT} = 1.6\ mA, V_{OUT} \leq 0.5V$	$-7V \leq V_{CM} \leq 7V$	0.2	0.42		V
R_{IN}	Input Resistance	$-15V \leq V_{CM} \leq 15V, 0V \leq V_{CC} \leq 15V$		4	5		kΩ
R_T	Line Termination Resistance	$T_A = 25°C$		100	180	300	Ω
R_O	Offset Control Resistance	$T_A = 25°C$			56		kΩ
I_{IND}	Data Input Current (Unterminated)	$0V \leq V_{CC} \leq 15V$	$V_{CM} = 10V$		2	3.1	mA
			$V_{CM} = 0V$		0	−0.5	mA
			$V_{CM} = -10V$		−2	−3.1	mA
V_{THB}	Input Balance (Note 5)	$I_{OUT} = 200\ \mu A, V_{OUT} \geq V_{CC} - 1.2V, R_S = 500\Omega$	$-7V \leq V_{CM} \leq 7V$		0.1	0.4	V
		$I_{OUT} = 1.6\ mA, V_{OUT} \leq 0.5V$ $R_S = 500\Omega$	$-7V \leq V_{CM} \leq 7V$		−0.1	−0.4	V
V_{OH}	Logical "1" Output Voltage	$I_{OUT} = -200\ \mu A, V_{DIFF} = 1V$		$V_{CC} - 1.2$	$V_{CC} - 0.75$		V
V_{OL}	Logical "0" Output Voltage	$I_{OUT} = 1.6\ mA, V_{DIFF} = -1V$			0.25	0.5	V
I_{CC}	Power Supply Current	$15V \leq V_{CM} \leq -15V$, $V_{DIFF} = -0.5V$ (Both Receivers)	$V_{CC} = 5.5V$		8	15	mA
			$V_{CC} = 15V$		15	30	mA
$I_{IN(1)}$	Logical "1" Strobe Input Current	$V_{STROBE} = 15V, V_{DIFF} = 3V$			15	100	μA
$I_{IN(0)}$	Logical "0" Strobe Input Current	$V_{STROBE} = 0V, V_{DIFF} = -3V$			−0.5	−100	μA
V_{IH}	Logical "1" Strobe Input Voltage	$V_{OL} \leq 0.5V, I_{OUT} = 1.6\ mA$	$V_{CC} = 5V$	3.5	2.5		V
			$V_{CC} = 10V$	8.0	5.0		V
			$V_{CC} = 15V$	12.5	7.5		V

Electrical Characteristics (Notes 2 and 3) (Continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IL}	Logical "0" Strobe Input Voltage	V_{OH} V_{CC} − 1.2V, I_{OUT} = −200 μA	V_{CC} = 5V		2.5	1.5	V
			V_{CC} = 10V		5.0	2.0	V
			V_{CC} = 15V		7.5	2.5	V
I_{OS}	Output Short-Circuit Current	V_{OUT} = 0V, V_{CC} = 15V, V_{STROBE} = 0V, (Note 4)		−5	−20	−40	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS78C120 and across the 0°C to +70°C range for the DS88C120. All typical values for T_A = 25°C, V_{CC} = 5V and V_{CM} = 0V.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Only one output at a time should be shorted.

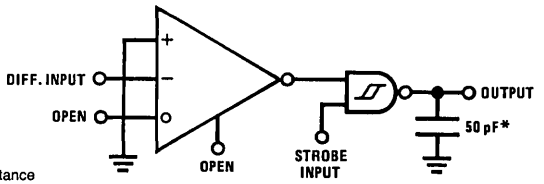
Note 5: Refer to EIA-RS422 for exact conditions.

Switching Characteristics V_{CC} = 5V, T_A = 25°C

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$t_{pd0(D)}$	Differential Input to "0" Output	C_L = 50 pF		60	100	ns
$t_{pd1(D)}$	Differential Input to "1" Output	C_L = 50 pF		100	150	ns
$t_{pd0(S)}$	Strobe Input to "0" Output	C_L = 50 pF		30	70	ns
$t_{pd1(S)}$	Strobe Input to "1" Output	C_L = 50 pF		100	150	ns

AC Test Circuit and Switching Time Waveforms

Differential and Strobe Input Signal



*Includes probe and test fixture capacitance

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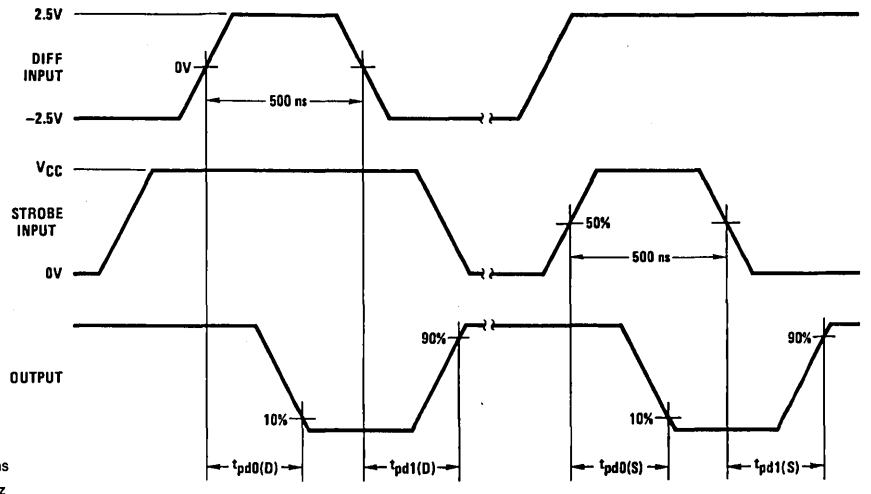

$t_r = t_f \leq 10$ ns

PRR = 1 MHz

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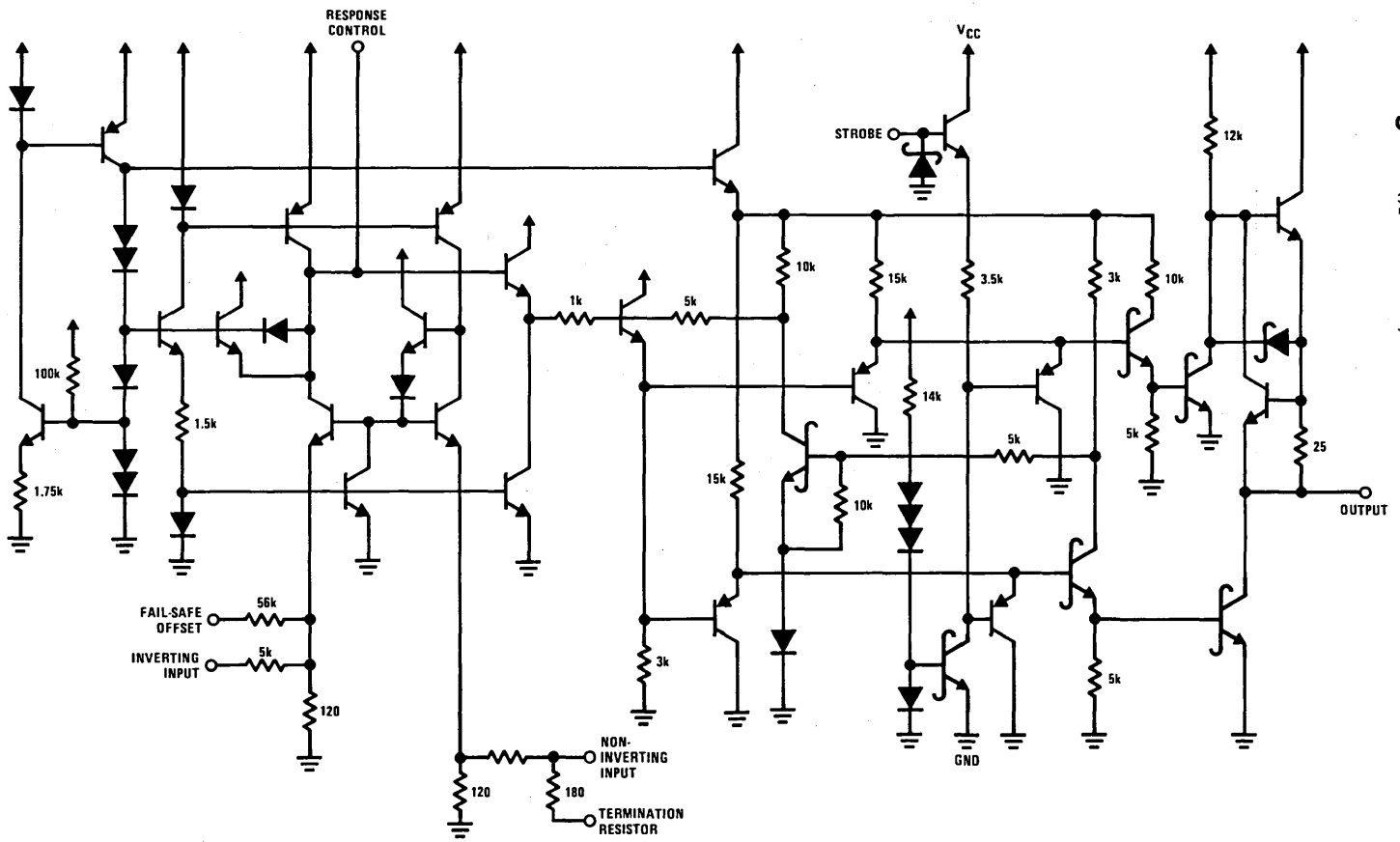
Note: Optimum switching response is obtained by minimizing stray capacitance on Response Control pin (no external connection).

Schematic Diagram (½ Circuit Shown)



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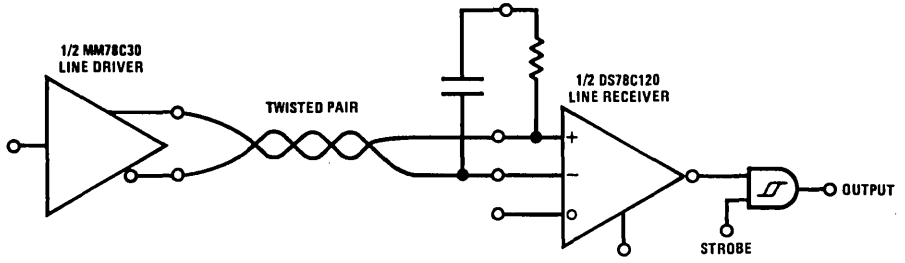
Application Hints

Balanced Data Transmission



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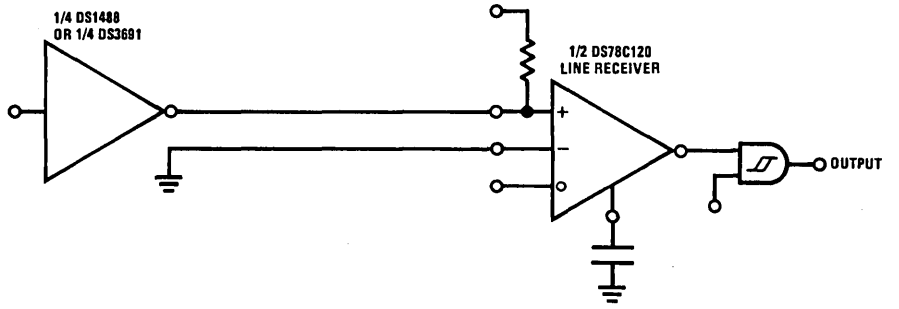
Unbalanced Data Transmission



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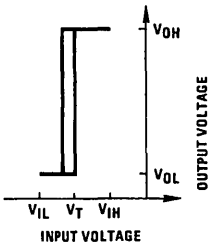
Logic Level Translator



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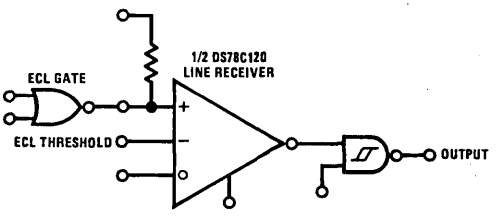

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The DS78C120/DS88C120 may be used as a level transistor to interface between ±12V MOS, ECL, TTL and CMOS. To configure, bias either input to a voltage equal to ½ the voltage of the input signal, and the other input to the driving gate.

Application Hints (Continued)

LINE DRIVERS

Line drivers which will interface with the DS78C120/DS88C120 are listed below.

Balanced Drivers

DS26LS31	Quad RS-422 Line Driver
DS7830, DS8830	Dual TTL
DS7831, DS8831	Dual TRI-STATE® TTL
DS7832, DS8832	Dual TRI-STATE TTL
DS1691A, DS3691	Quad RS-423/Dual RS-422 TTL
DS1692, DS3692	Quad RS-423/Dual TRI-STATE RS-422 TTL
DS3587, DS3487	Quad TRI-STATE RS-422

Unbalanced Drivers

DS1488	Quad RS-232
DS14C88	Quad RS-232
DS75150	Dual RS-232

RESPONSE CONTROL AND HYSTERESIS

In unbalanced (RS-232/RS-423) applications it is recommended that the rise time and fall time of the line driver be controlled to reduce cross-talk. Elimination of switching noise is accomplished in the DS78C120/DS88C120 by the 50 mV of hysteresis incorporated in the output gate. This eliminates the oscillations which may appear in a line receiver due to the input signal slowly varying about the threshold level for extended periods of time.

High frequency noise which is superimposed on the input signal which may exceed 50 mV can be reduced in amplitude by filtering the device input. On the DS78C120/DS88C120, a high impedance response control pin in the input amplifier is available to filter the input signal without affecting the termination impedance of the transmission line. Noise pulse width rejection vs the value of the response control capacitor is shown in *Figures 1* and *2*. This combination of filters followed by hysteresis will optimize performance in a worse case noise environment.

TRANSMISSION LINE TERMINATION

On a transmission line which is electrically long, it is advisable to terminate the line in its characteristic impedance to prevent signal reflection and its associated noise/cross-talk. A 180Ω termination resistor is provided in the DS78C120/DS88C120 line receiver. To use the termination resistor, connect pins 2 and 3 together and pins 13 and 14 together. The 180Ω resistor provides a good compromise between line reflections, power dissipation in the driver, and IR drop in the transmission line. If power dissipation and IR drop are still a concern, a capacitor may be connected in series with the resistor to minimize power loss.

The value of the capacitor is recommended to be the line length (time) divided by 3 times the resistor value. Example: if the transmission line is 1,000 feet long, (approximately 1000 ns) the capacitor value should be 1852 pF. For additional application details, refer to application notes AN-22 and AN-108.

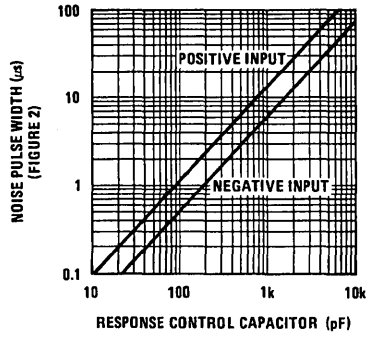

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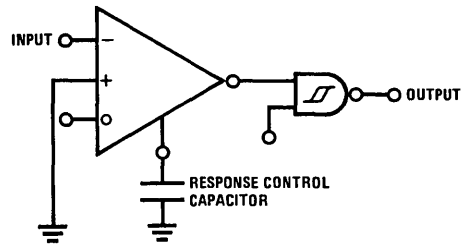
FIGURE 1. Noise Pulse Width vs Response Control Capacitor



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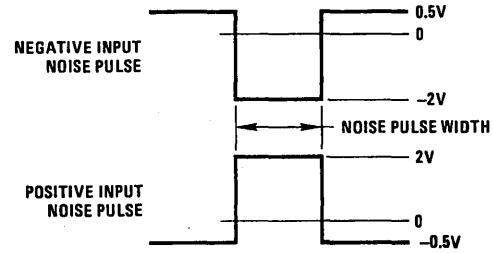

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FIGURE 2

Application Hints (Continued)

FAIL-SAFE OPERATION

Communication systems require elements of a system to detect the presence of signals in the transmission lines, and it is desirable to have the system shut-down in a fail-safe mode if the transmission line is open or short. To facilitate the detection of input opens or shorts, the DS78C120/DS88C120 incorporates an input threshold voltage offset. This feature will force the line receiver to a specific logic state if presence of either fault is a condition.

Given that the receiver input threshold is ±200 mV, an input signal greater than ±200 mV insures the receiver will be in a specific logic state. When the offset control input (pins 1 and 15) is connected to V_{CC} = 5V, the input thresholds are offset from 200 mV to 700 mV, referred to the non-inverting input, or −200 mV to −700 mV, referred to the inverting input. Therefore, if the input is open or short, the input will be greater than the input threshold and the receiver will remain in a specified logic state.

The input circuit of the receiver consists of a 5k resistor terminated to ground through 120Ω on both inputs. This network acts as an attenuator, and permits operation with common-mode input voltages greater than ±15V. The offset control input is actually another input to the attenuator, but its resistor value is 56k. The offset control input is connected to the inverting input side of the attenuator, and the input voltage to the amplifier is the sum of the inverting input plus 0.09 times the voltage on the offset control input. When the offset control input is connected to 5V the input amplifier will see $V_{IN(INVERTING)}$ + 0.45V or $V_{IN(INVERTING)}$ + 0.9V when the control input is connected to 10V. The offset control input will not significantly affect the differential performance of the receiver over its common-mode operating range, and will not change the input impedance balance of the receiver.

It is recommended that the receiver be terminated (500Ω or less) to insure it will detect an open circuit in the presence of noise.

The offset control can be used to insure fail-safe operation for unbalanced interface (RS-423) or for balanced interface (RS-422) operation.

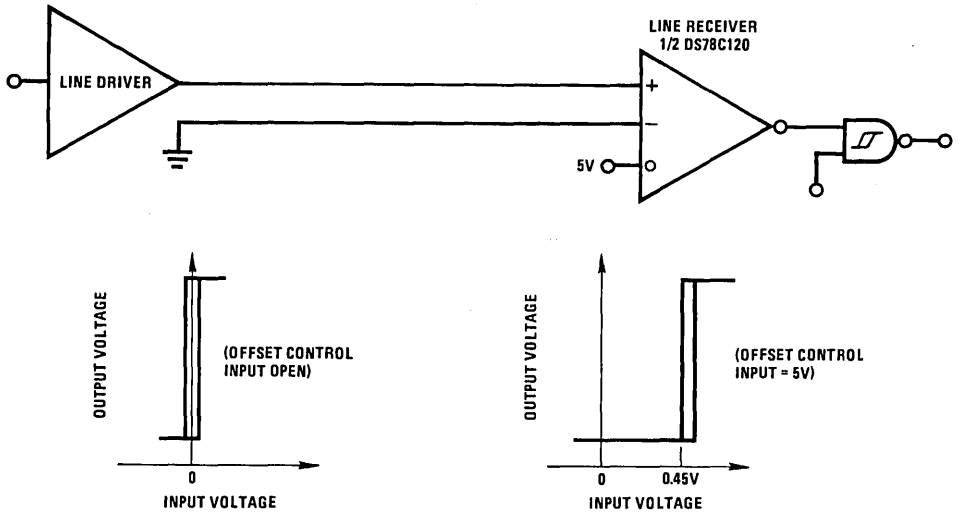
For unbalanced operation, the receiver would be in an indeterminate logic state if the offset control input was open. Connecting the offset to 5V offsets the receiver threshold 0.45V. The output is forced to a logic zero state if the input is open or short.

For balanced operation with inputs short or open, receiver C will be in an indeterminate logic state. Receivers A and will be in a logic zero state allowing the NOR gate to detect the short or open condition. The strobe will disable receivers A and B and may therefore be used to sample the fail-safe detector. Another method of fail-safe detection consists of filtering the output of the NOR gate D so it would not indicate a fault condition when receiver inputs pass through the threshold region, generating an output transient.

In a communications system, only the control signals are required to detect input fault condition. Advantages of a balanced data transmission system over an unbalanced transmission system are:

1. High noise immunity
2. High data ratio
3. Long line lengths

Unbalanced RS-423 and RS-232 Fail-Safe



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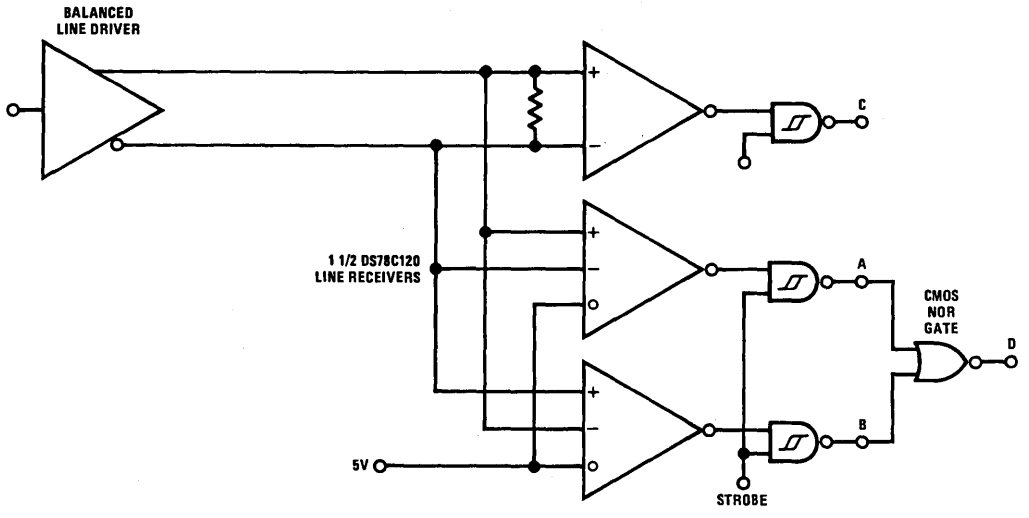
Application Hints (Continued)

Balanced RS-422 Fail-Safe



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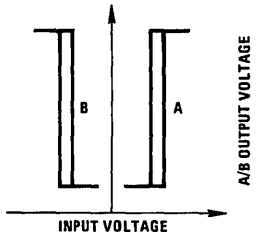

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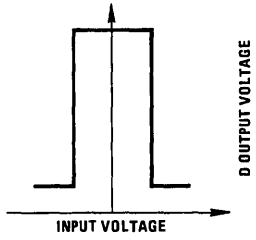

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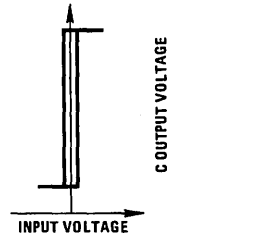

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Truth Table (For Balanced Fail-Safe)

Input	Strobe	A-OUT	B-OUT	C-OUT	D-OUT
0	1	0	1	0	0
1	1	1	0	1	0
X	1	0	0	X	1
0	0	1	1	0	0
1	0	1	1	0	0
X	0	1	1	0	0

National Semiconductor Corporation

DS78LS120/DS88LS120 Dual Differential Line Receiver (Noise Filtering and Fail-Safe)

General Description

The DS78LS120 and DS88LS120 are high performance, dual differential, TTL compatible line receivers for both balanced and unbalanced digital data transmission. The inputs are compatible with EIA, Federal and MIL standards.

The line receiver will discriminate a ±200 mV input signal over a common-mode range of ±10V and a ±300 mV signal over a range of ±15V.

Circuit features include hysteresis and response control for applications where controlled rise and fall times and/or high frequency noise rejection are desirable. Threshold offset control is provided for fail-safe detection, should the input be open or short. Each receiver includes an optional 180Ω terminating resistor and the output gate contains a logic strobe for time discrimination. The DS78LS120 is specified over a −55°C to +125°C temperature range and the DS88LS120 from 0°C to +70°C.

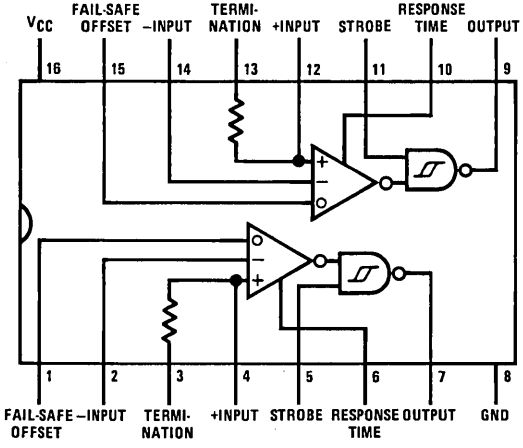
Input specifications meet or exceed those of the popular DS7820/DS8820 line receiver.

Features

- Meets EIA standards RS232-C, RS422 and RS423, Federal Standards 1020, 1030 and MIL-188-114
- Input voltage range of ±15V (differential or common-mode)
- Separate strobe input for each receiver
- 5k typical input impedance
- Optional 180Ω termination resistor
- 50 mV input hysteresis
- 200 mV input threshold
- Separate fail-safe mode

Connection Diagram

Dual-In-Line Package



TL/F/7499–1

Top View

Order Number DS78LS120J, DS88LS120J or DS88LS120N
See NS Package Number J16A or N16A

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	±25V
Strobe Voltage	7V
Output Sink Current	50 mA
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1433 mV
Molded Package	1362 mW
Lead Temperature (Soldering, 4 sec)	260°C

*Derate cavity package 9.6 mW/°C above 25°C; derate molded package 10.9 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	5.5	V
Temperature (T_A)			
DS78LS120	−55	+125	°C
DS88LS120	0	+70	°C
Common-Mode Voltage (V_{CM})	−15	+15	V

Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{TH}	Differential Threshold Voltage	I_{OUT} = −400 μA, V_{OUT} ≥ 2.5V	−7V ≤ V_{CM} ≤ 7V		0.06	0.2	V
			−15 ≤ V_{CM} ≤15V		0.06	0.3	V
V_{TL}	Differential Threshold Voltage	I_{OUT} = 4 mA, V_{OUT} ≤ 0.5V	−7V ≤ V_{CM} ≤7V		−0.08	−0.2	V
			−15V ≤ V_{CM} ≤ 15V		−0.08	−0.3	V
V_{TH}	Differential Threshold Voltage with Fail-Safe Offset = 5V	I_{OUT} = −400 μA, V_{OUT} ≥ 2.5V	−7V ≤ V_{CM} ≤ 7V		0.47	0.7	V
V_{TL}		I_{OUT} = 4 mA, V_{OUT} ≤ 0.5	−7V ≤ V_{CM} ≤ 7V	−0.2	−0.42		V
R_{IN}	Input Resistance	−15V ≤ V_{CM} ≤ 15V, 0V ≤ V_{CC} ≤ 7V		4	5		kΩ
R_T	Line Termination Resistance	T_A = 25°C		100	180	300	Ω
R_O	Offset Control Resistance	T_A = 25°C		42	56	70	kΩ
I_{IND}	Data Input Current (Unterminated)	V_{CM} = 10V	0V ≤ V_{CC} ≤ 7V		2	3.1	mA
		V_{CM} = 0V			0	−0.5	mA
		V_{CM} = −10V			−2	−3.1	mA
V_{THB}	Input Balance (Note 5)	I_{OUT} = −400 μA, V_{OUT} ≥ 2.5V, R_S = 500Ω	−7V ≤ V_{CM} 7V		0.1	0.4	V
		I_{OUT} = 4 mA, V_{OUT} ≤ 0.5V, R_S = 500Ω	−7V ≤ V_{CM} ≤ 7V		−0.1	−0.4	V
V_{OH}	Logical "1" Output Voltage	I_{OUT} = −400 μA, V_{DIFF} = 1V, V_{CC} = 4.5V		2.5	3		V
V_{OL}	Logical "0" Output Voltage	I_{OUT} = 4 mA, V_{DIFF} = −1V, V_{CC} = 4.5V			0.35	0.5	V
I_{CC}	Power Supply Current	V_{CC} = 5.5V, V_{DIFF} = −0.5V, (Both Receivers)	V_{CM} = 15V		10	16	mA
			V_{CM} = −15V		10	16	mA
$I_{IN(1)}$	Logical "1" Strobe Input Current	V_{STROBE} = 5.5V, V_{DIFF} = 3V			1	100	μA
$I_{IN(0)}$	Logical "0" Strobe Input Current	V_{STROBE} = 0V, V_{DIFF} = −3			−290	−400	μA
V_{IH}	Logical "1" Strobe Input Voltage	V_{OL} ≤ 0.5, I_{OUT} = 4mA		2.0	1.12		V
V_{IL}	Logical "0" Strobe Input Voltage	V_{OH} ≥ 2.5V, I_{OUT}, = −400 μA			1.12	0.8	V
I_{OS}	Output Short-Circuit Current	V_{OUT} = 0V, V_{CC} = 5.5V, V_{STROBE} = 0V, (Note 4)		−30	−100	−170	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS78LS120 and across the 0°C to +70°C for the DS88LS120. All typical values are for T_A = 25°C, V_{CC} = 5V and V_{CM} = 0V.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Only one output at a time should be shorted.

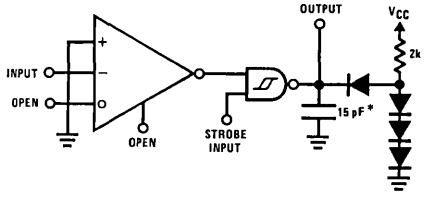
Note 5: Refer to EIA-RS422 for exact conditions.

Switching Characteristics V_{CC} = 5V, T_A = 25°C

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$t_{pd0(D)}$	Differential Input to "0" Output	Response Pin Open, C_L = 15 pF, R_L = 2 kΩ		38	60	ns
$t_{pd1(D)}$	Differential Input to "1" Output			38	60	ns
$t_{pd0(S)}$	Strobe Input to "0" Output			16	25	ns
$t_{pd1(S)}$	Strobe Input to "1" Output			12	25	ns

AC Test Circuit and Switching Time Waveforms

Differential and Strobe Input Signal



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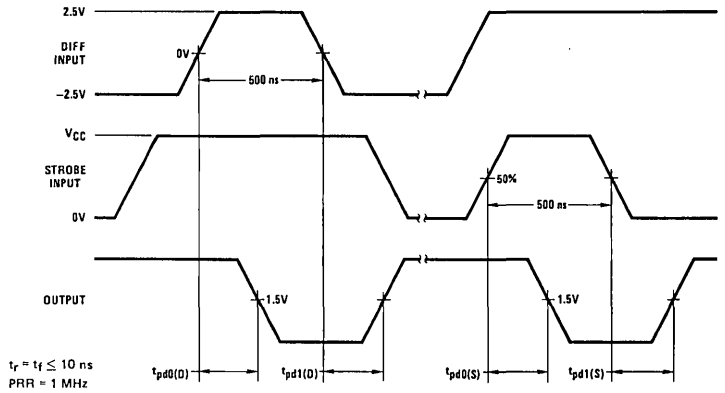
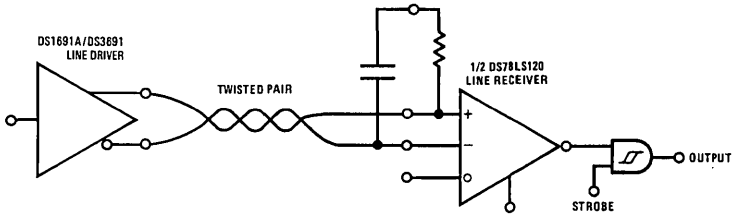
*Includes probe and test fixture capacitance



Note: Optimum switching response is obtained by minimizing stray capacitance on Response Control pin (no external connection). TL/F/7499-4

Application Hints

Balanced Data Transmission



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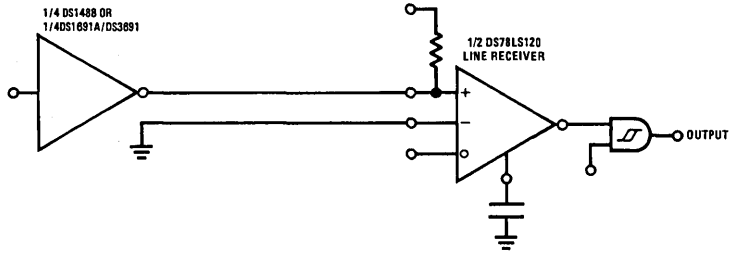
Application Hints (Continued)

Unbalanced Data Transmission



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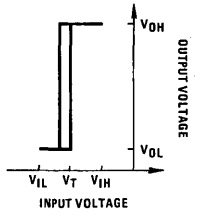

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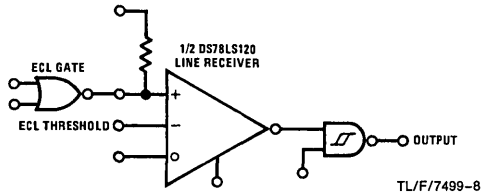
Logic Level Translator



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The DS78LS120/DS88LS120 may be used as a level translator to interface between ±12V MOS, ECL, TTL and CMOS. To configure, bias either input to a voltage equal to ½ the voltage of the input signal, and the other input to the driving gate.

LINE DRIVERS

Line drivers which will interface with the DS78LS120/DS88LS120 are listed below.

Balanced Drivers

DS26LS31	Quad RS-422 Line Driver Dual CMOS
DS7830, DS8830	Dual TTL
DS7831, DS8831	Dual TRI-STATE TTL
DS7832, DS8832	Dual TRI-STATE TTL
DS1691A, DS3691	Quad RS-423/Dual RS-422 TTL
DS1692, DS3692	Quad RS-423/Dual TRI-STATE RS-422 TTL
DS3487	Quad TRI-STATE RS-422

Unbalanced Drivers

DS1488	Quad RS-232
DS75150	Dual RS-232

RESPONSE CONTROL AND HYSTERESIS

In unbalanced (RS-232/RS-423) applications it is recommended that the rise time and fall time of the line driver be controlled to reduce cross-talk. Elimination of switching noise is accomplished in the DS78LS120/DS88LS120 by the 50 mV of hysteresis incorporated in the output gate. This eliminates the oscillations which may appear in a line receiver due to the input signal slowly varying about the threshold level for extended periods of time.

High frequency noise which is superimposed on the input signal which may exceed 50 mV can be reduced in amplitude by filtering the device input. On the DS78LS120/DS88LS120, a high impedance response control pin in the input amplifier is available to filter the input signal without affecting the termination impedance of the transmission line. Noise pulse width rejection vs the value of the response control capacitor is shown in *Figures 1* and *2*. This combination of filters followed by hysteresis will optimize performance in a worse case noise environment.

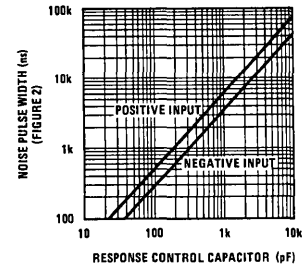

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FIGURE 1. Noise Pulse Width vs Response Control Capacitor

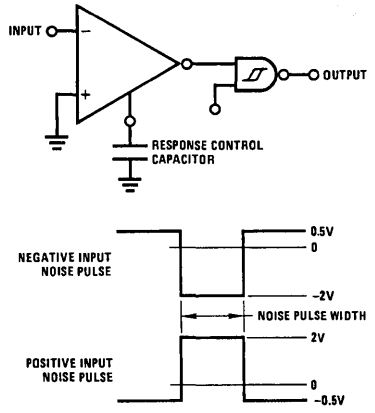

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FIGURE 2

Application Hints (Continued)

TRANSMISSION LINE TERMINATION

On a Transmission line which is electrically long, it is advisable to terminate the line in its characteristic impedance to prevent signal reflection and its associated noise/crosstalk. A 180Ω termination resistor is provided in the DS78LS120/DS88LS120 line receiver. To use the termination resistor, connect pins 2 and 3 together and pins 13 and 14 together. The 180Ω resistor provides a good compromise between line reflections, power dissipation in the driver, and IR drop in the transmission line. If power dissipation and IR drop are still a concern, a capacitor may be connected in series with the resistor to minimize power loss.

The value of the capacitor is recommended to be the line length (time) divided by 3 times the resistor value. Example: if the transmission line is 1,000 feet long, (approximately 1000 ns), and the termination resistor value is 180Ω, the capacitor value should be 1852 pF. For additional application details, refer to application notes AN-22 and AN-108.

FAIL-SAFE OPERATION

Communication systems require elements of a system to detect the presence of signals in the transmission lines, and it is desirable to have the system shut-down in a fail-safe mode if the transmission line is open or short. To facilitate the detection of input opens or shorts, the DS78LS120/DS88LS120 incorporates an input threshold voltage offset. This feature will force the line receiver to a specific logic state if presence of either fault is a condition.

Given that the receiver input threshold is ±200 mV, an input signal greater than ±200 mV insures the receiver will be in a specific logic state. When the offset control input (pins 1 and 15) is connected to V_{CC} = 5V, the input thresholds are offset from 200 mV to 700 mV, referred to the non-inverting input, or −200 mV to −700 mV, referred to the inverting input. Therefore, if the input is open or short, the input will be greater than the input threshold and the receiver will remain in a specified logic state.

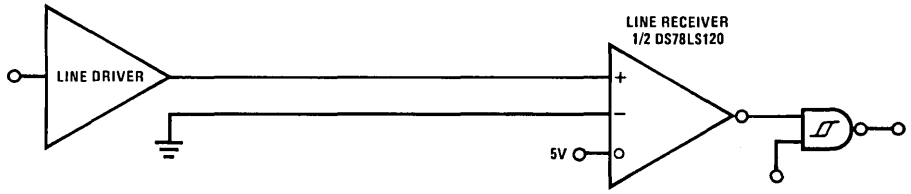
The input circuit of the receiver consists of a 5k resistor terminated to ground through 120Ω on both inputs. This network acts as an attenuator, and permits operation with common-mode input voltages greater than ±15V. The offset control input is actually another input to the attenuator, but its resistor value is 56k. The offset control input is connected to the inverting input side of the attenuator, and the input voltage to the amplifier is the sum of the inverting input plus 0.09 times the voltage on the offset control input. When the offset control input is connected to 5V the input amplifier will see $V_{IN(INVERTING)}$ +0.45V or $V_{IN(INVERTING)}$ +0.9V when the control input is connected to 10V. The offset control input will not significantly affect the differential performance of the receiver over its common-mode operating range, and will not change the input impedance balance of the receiver.

It is recommended that the receiver be terminated (500Ω or less) to insure it will detect an open circuit in the presence of noise.

The offset control can be used to insure fail-safe operation for unbalanced interface (RS-423) or for balanced interface (RS-422) operation.

For unbalanced operation, the receiver would be in an indeterminate logic state if the offset control input was open. Connecting the offset to 5V offsets the receiver threshold 0.45V. The output is forced to a logic zero state if the input is open or short.

Unbalanced RS-423 and RS-232 Fail-Safe



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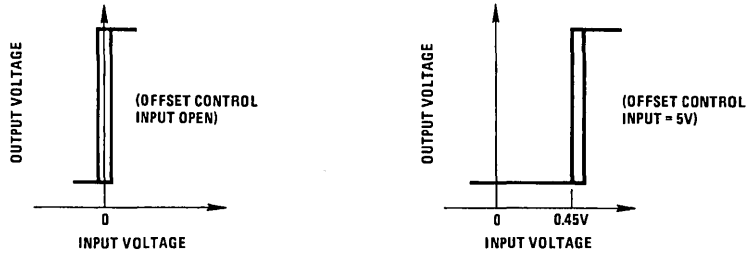

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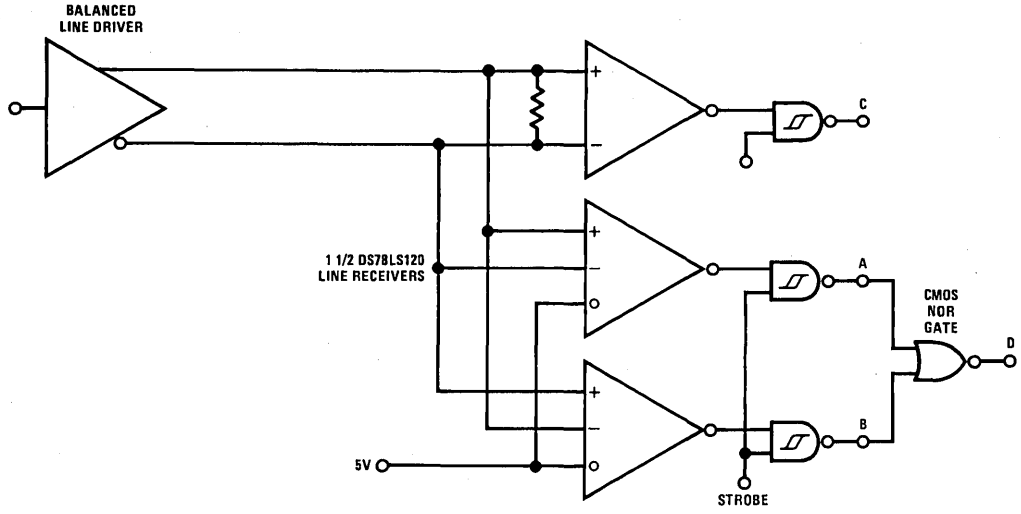
Application Hints (Continued)

Balanced RS-422 Fail-Safe



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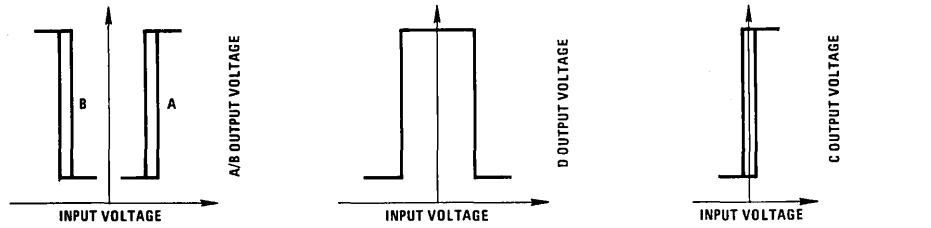

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For balanced operation with inputs short or open, receiver C will be in an indeterminate logic state. Receivers A and B will be in a logic zero state allowing the NOR gate to detect the short or open condition. The strobe will disable receivers A and B and may therefore be used to sample the fail-safe detector. Another method of fail-safe detection consists of filtering the output of NOR gate D so it would not indicate a fault condition when receiver inputs pass through the threshold region, generating an output transient.

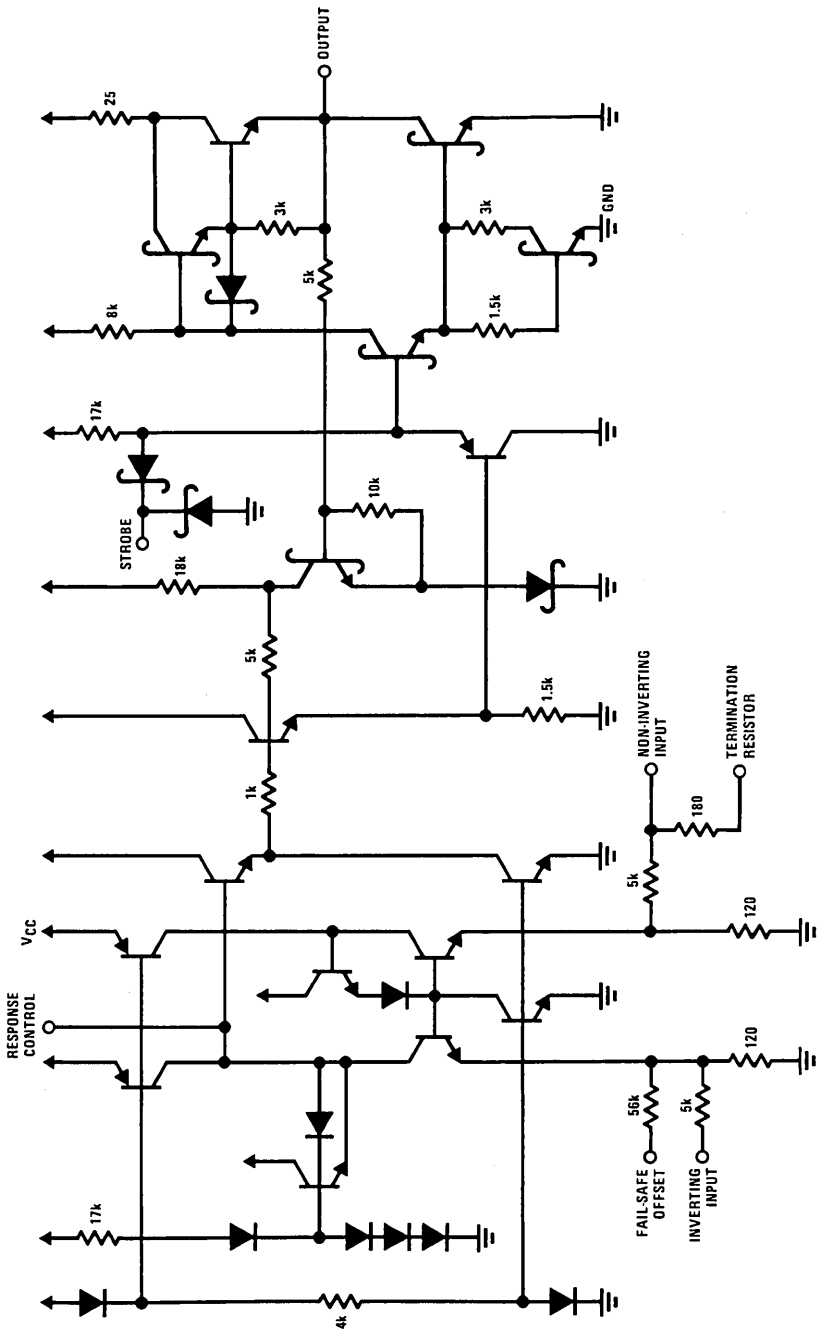
In a communications system, only the control signals are required to detect input fault conditions. Advantages of a balanced data transmission system over an unbalanced transmission system are:

1. High noise immunity
2. High data ratio
3. Long line lengths

Truth Table (For Balanced Fail-Safe)

Input	Strobe	A-Out	B-Out	C-Out	D-Out
0	1	0	1	0	0
1	1	1	0	1	0
X	1	0	0	X	1
0	0	1	1	0	0
1	0	1	1	0	0
X	0	1	1	0	0

Schematic Diagram



National Semiconductor Corporation

PRELIMINARY

DS8921/DS8921A Differential Line Driver and Receiver Pair

General Description

The DS8921, DS8921A are Differential Line Driver and Receiver pairs designed specifically for applications meeting the ST506, ST412 and ESDI Disk Drive Standards. In addition, these devices meet the requirements of the EIA Standard RS-422.

The DS8921A receiver offers an input sensitivity of 200 mV over a ±7V common mode operating range. Hysteresis is incorporated (typically 70 mV) to improve noise margin for slowly changing input waveforms. An input fail-safe circuit is provided such that if the receiver inputs are open the output assumes the logical one state.

The DS8921A driver is designed to provide unipolar differential drive to twisted pair or parallel wire transmission lines. Complementary outputs are logically ANDed and provide an output skew of 0.5 ns (typ.) with propagation delays of 12 ns.

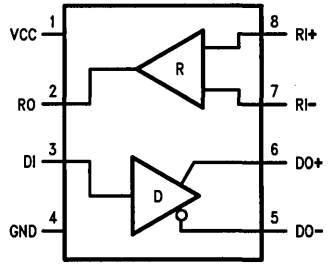
Power up/down circuitry is featured which TRI-STATE® the outputs and prevents erroneous glitches on the transmission lines during system power up or power down operation.

The DS8921A is designed to be compatible with TTL and CMOS.

Features

- 12 ns typical propagation delay
- Output skew - 0.5 ns typical
- Meet the requirements of EIA Standard RS-422
- Complementary Driver Outputs
- High differential or common-mode input voltage ranges of ±7V
- ±0.2V receiver sensitivity over the input voltage range
- Receiver input fail-safe circuitry
- Receiver input hysteresis-70 mV typical
- Glitch free power up/down

Connection Diagram



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Order Number DS8921M, DS8921N, DS8921AM, DS8921AN, DS8921J or DS8921AJ
See NS Package Number J08A, M08A or N08E

Truth Table

Receiver		Driver		
Input	V_{OUT}	Input	V_{OUT}	$\overline{V_{OUT}}$
$V_{ID} \geq V_{TH}$ (MAX)	1	1	1	0
$V_{ID} \leq V_{TH}$ (MIN)	0	0	0	1

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Driver Input Voltage	−0.5V to +7V
Output Voltage	5.5V
Receiver Output Sink Current	50 mA
Receiver Input Voltage	±10V
Differential Input Voltage	±12V
Storage Temperature Range	−65°C to +165°C
Lead Temperature (Soldering, 4 sec.)	260°C

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage	4.5	5.5	V
Temperature (T_A)	0	70	°C

DS8921/DS8921A Electrical Characteristics (Notes 2, 3 and 4)

Symbol	Conditions	Min	Typ	Max	Units
RECEIVER					
V_{TH}	$-7V \le V_{CM} \le +7V$	−200	±35	+200	mV
V_{HYST}	$-7V \le V_{CM} \le +7V$	15	70		mV
R_{IN}	$-7V \le V_{CM} \le +7V$	4.0	6.0		kΩ
I_{IN}	$V_{IN} = 10V$			3.25	mA
	$V_{IN} = -10V$			−3.25	mA
V_{OH}	$I_{OH} = -400\ \mu A$	2.5			V
V_{OL}	$I_{OL} = 8$ mA			0.5	V
I_{SC}	V_{CC} = MAX V_{OUT} = 0V	−15		−100	mA
DRIVER					
V_{IH}		2.0			V
V_{IL}				0.8	V
I_{IL}	V_{CC} = MAX V_{IN} = 0.4V		−40	−200	μA
I_{IH}	V_{CC} = MAX V_{IN} = 2.7V			20	μA
I_I	V_{CC} = MAX V_{IN} = 7.0V			100	μA
V_{CL}	V_{CC} = MIN I_{IN} = −18 mA			−1.5	V
V_{OH}	V_{CC} = MIN I_{OH} = −20 mA	2.5			V
V_{OL}	V_{CC} = MIN I_{OL} = +20 mA			0.5	V
I_{OFF}	V_{CC} = 0V, V_{OUT} = 5.5V			100	μA
$\lvert V_T \rvert - \lvert \overline{VT} \rvert$				0.4	V
V_T		2.0			V
$\lvert V_{OS} - \overline{V_{OS}} \rvert$				0.4	V
I_{SC}	V_{CC} = MAX V_{OUT} = 0V	−30		−150	mA
DRIVER and RECEIVER					
I_{CC}	V_{CC} = MAX V_{OUT} = Logic 0			35	mA

Receiver Switching Characteristics (*Figures 1* and *2*)

Symbol	Conditions	Min	Typ	Max		Units
				8921	8921A	
T_{pLH}	C_L = 30 pF		14	22.5	20	ns
T_{pHL}	C_L = 30 pF		14	22.5	20	ns
$\lvert T_{pLH} - T_{pHL} \rvert$	C_L = 30 pF		0.5	5	3.5	ns

Driver Switching Characteristics (*Figures 3* and *4*)

SINGLE ENDED CHARACTERISTICS

Symbol	Conditions	Min	Typ	Max		Units
				8921	8921A	
T_{pLH}	C_L = 30 pF		10	15		ns
T_{pHL}	C_L = 30 pF		10	15		ns
T_{TLH}	C_L = 30 pF		5	8		ns
T_{THL}	C_L = 30 pF		5	8		ns
Skew	CL = 30 pF (Note 5)		1	5	3.5	ns

Driver Switching Characteristics (*Figures 3* and *5*)

DIFFERENTIAL CHARACTERISTICS (Note 6)

Symbol	Conditions	Min	Typ	Max		Units
				8921	8921A	
T_{pLH}	C_L = 30 pF		10	15		ns
T_{pHL}	C_L = 30 pF		10	15		ns
$\lvert T_{pLH} - T_{pHL} \rvert$	C_L = 30 pF		0.5	6	2.75	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The Table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All currents into device pins are shown as positive values; all currents out of the device are shown as negative; all voltages are referenced to ground unless otherwise specified. All values shown as max or min are classified on absolute value basis.

Note 3: All typical values are V_{CC} = 5V, T_A = 25°C.

Note 4: Only one output at a time should be shorted.

Note 5: Difference between complementary outputs at the 50% point.

Note 6: Differential Delays are defined as calculated results from single ended rise and fall time measurements. This approach in establishing AC performance specifications has been taken due to limitations of available Automatic Test Equipment (ATE).

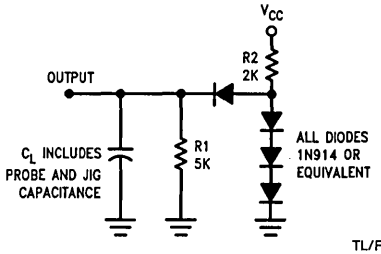
The calculated ATE results assume a linear transition between measurement points and are a result of the following equations:

$$T_{cr} = \frac{(T_{fb} \times T_{rb}) - (T_{ra} \times T_{fa})}{T_{rb} - T_{ra} - T_{fa} + T_{fb}}$$

Where: T_{cr} = Crossing Point

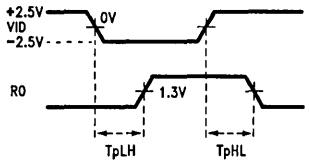
T_{ra}, T_{rb}, T_{fa} and T_{fb} are time measurements with respect to the input. See *Figure 6.*

AC Test Circuits and Switching Diagrams



TL/F/8512-3

FIGURE 1



TL/F/8512-4

FIGURE 2

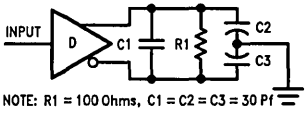


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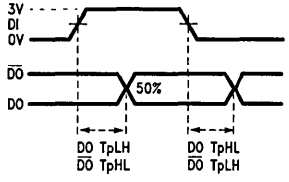
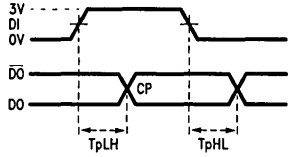
FIGURE 3



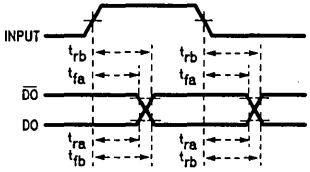
TL/F/8512-6

FIGURE 4



TL/F/8512-7

FIGURE 5

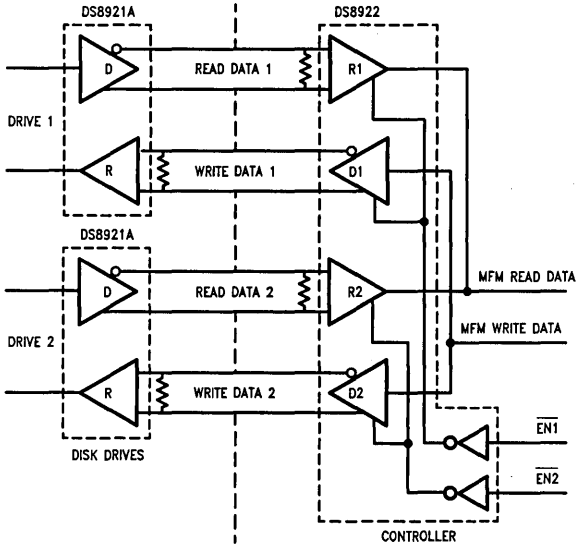


TL/F/8512-2

FIGURE 6

Typical Applications

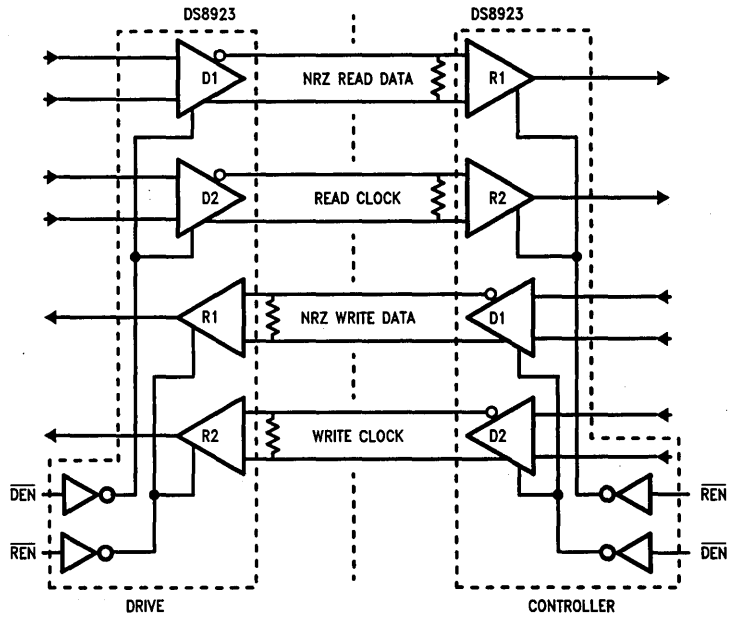
ST506 and ST412 Application



TL/F/8512-8

Typical Applications (Continued)

ESDI Application



TL/F/8512–9

National Semiconductor Corporation

PRELIMINARY

DS8922/22A/DS8923/23A TRI-STATE® RS-422 Dual Differential Line Driver and Receiver Pairs

General Description

The DS8922/22A and DS8923/23A are Dual Differential Line Driver and Receiver pairs. These devices are designed specifically for applications meeting the ST506, ST412 and ESDI Disk Drive Standards. In addition, the devices meet the requirements of the EIA Standard RS-422.

These devices offer an input sensitivity of 200 mV over a ±7V common mode operating range. Hysteresis is incorporated (typically 70 mV) to improve noise margin for slowly changing input waveforms. An input fail-safe circuit is provided such that if the receiver inputs are open the output assumes the logical one state.

The DS8922A and DS8923A drivers are designed to provide unipolar differential drive to twisted pair or parallel wire transmission lines. Complementary outputs are logically ANDed and provide an output skew of 0.5 ns (typ.) with propagation delays of 12 ns.

Both devices feature TRI-STATE outputs. The DS8922/22A have independent control functions common to a driver and receiver pair. The DS8923/23A have separate driver and receiver control functions.

Power up/down circuitry is featured which will TRI-STATE the outputs and prevents erroneous glitches on the transmission lines during system power up or power down operation.

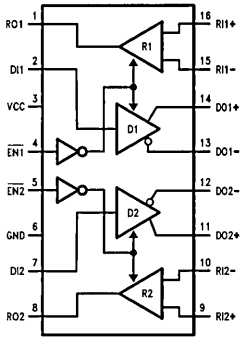
The DS8922/22A and DS8923/23A are designed to be compatible with TTL and CMOS.

Features

- 12 ns typical propagation delay
- Output skew—±0.5 ns typical
- Meets the requirements of EIA Standard RS-422
- Complementary Driver Outputs
- High differential or common-mode input voltage ranges of ±7V
- ±0.2V receiver sensitivity over the input voltage range
- Receiver input fail-safe circuitry
- Receiver input hysteresis—±70 mV typical
- Glitch free power up/down
- TRI-STATE outputs

Connection Diagrams

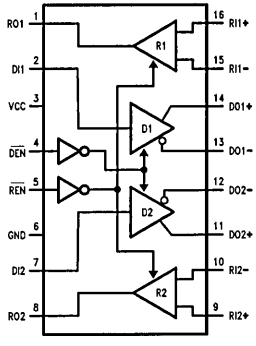
DS8922A Dual-In-Line



TL/F/8511–1

Order Number DS8922N, J, M, DS8922AN, AJ, AM
See NS Package Number N16A, J16A or M16A

DS8923A Dual-In-Line



TL/F/8511–2

Order Number DS8923N, J, M DS8923AN, AJ, AM
See NS Package Number N16A, J16A or M16A

Truth Tables

DS8922/22A

$\overline{EN1}$	$\overline{EN2}$	RO1	RO2	DO1	DO2
0	0	ACTIVE	ACTIVE	ACTIVE	ACTIVE
1	0	HI-Z	ACTIVE	HI-Z	ACTIVE
0	1	ACTIVE	HI-Z	ACTIVE	HI-Z
1	1	HI-Z	HI-Z	HI-Z	HI-Z

DS8923/23A

$\overline{DEN}$	$\overline{REN}$	RO1	RO2	DO1	DO2
0	0	ACTIVE	ACTIVE	ACTIVE	ACTIVE
1	0	ACTIVE	ACTIVE	HI-Z	HI-Z
0	1	HI-Z	HI-Z	ACTIVE	ACTIVE
1	1	HI-Z	HI-Z	HI-Z	HI-Z

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Drive Input Voltage	−0.5V to +7V
Output Voltage	5.5V
Receiver Output Sink Current	50 mA
Receiver Input Voltage	±10V
Differential Input Voltage	±12V
Storage Temperature Range	−65°C to +165°C
Lead Temp. (Soldering, 4 seconds)	260°C

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage	4.5	5.5	V
Temperature (T_A)	0	70	°C

DS8922/22A and DS8923/23A Electrical Characteristics (Notes 2, 3, and 4)

Symbol	Conditions		Min	Typ	Max	Units
RECEIVER						
V_{TH}	$-7V \le V_{CM} \le +7V$		−200	±35	+200	mV
V_{HYST}	$-7V \le V_{CM} \le +7V$		15	50		mV
R_{IN}	$-7V \le V_{CM} \le +7V$		4.0	6.0		kΩ
I_{IN}	$V_{IN} = 10V$				3.25	mA
	$V_{IN} = -10V$				−3.25	mA
V_{OH}	V_{CC} = MIN $I_{OH} = -400\ \mu A$		2.5			V
V_{OL}	V_{CC} = MAX I_{OL} = 8 mA				0.5	V
I_{SC}	V_{CC} = MAX V_{OUT} = 0V		−15		−100	mA
DRIVER						
V_{OH}	V_{CC} = MIN $I_{OH} = -20$ mA		2.5			V
V_{OL}	V_{CC} = MIN $I_{OL} = +20$ mA				0.5	V
I_{OFF}	V_{CC} = 0V V_{OUT} = 5.5V				100	μA
$\lvert VT\rvert - \lvert\overline{VT}\rvert$					0.4	V
VT			2.0			V
$\lvert V_{OS} - \overline{V_{OS}}\rvert$					0.4	V
I_{SC}	V_{CC} = MAX V_{OUT} = 0V		−30		−150	mA
DRIVER and RECEIVER						
I_{OZ} TRI-STATE Leakage	V_{CC} = MAX	V_{OUT} = 2.5V			50	μA
		V_{OUT} = 0.4V			−50	μA
I_{CC}	V_{CC} = MAX	ACTIVE			76	mA
		TRI-STATE			78	mA
DRIVER and ENABLE INPUTS						
V_{IH}			2.0			V
V_{IL}					0.8	V
I_{IL}	V_{CC} = MAX V_{IN} = 0.4V			−40	−200	μA
I_{IH}	V_{CC} = MAX V_{IN} = 2.7V				20	μA
I_I	V_{CC} = MAX V_{IN} = 7.0V				100	μA
V_{CL}	V_{CC} = MIN $I_{IN} = -18$ mA				−1.5	V

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The Table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All currents into device pins are shown as positive values; all currents out of the device are shown as negative; all voltages are referenced to ground unless otherwise specified. All values shown as max or min are classified on absolute value basis.

Note 3: All typical values are $V_{CC} = 5V$, $T_A = 25°C$.

Note 4: Only one output at a time should be shorted.

Receiver Switching Characteristics (*Figures 1, 2* and *3*)

Parameter	Conditions	Min	Typ	Max		Units
				8922/23	8922A/23A	
T_{pLH}	CL = 30 pF		12	22.5	20	ns
T_{pHL}	CL = 30 pF		12	22.5	20	ns
$\lvert T_{pLH}-T_{pHL}\rvert$	CL = 30 pF		0.5	5	3.5	ns
Skew (Channel to Channel)	CL = 30 pF		0.5	3.0	2.0	ns
T_{pLZ}	CL = 15 pF S2 Open		15			ns
T_{pHZ}	CL = 15 pF S1 Open		15			ns
T_{pZL}	CL = 30 pF S2 Open		20			ns
T_{pZH}	CL = 30 pF S1 Open		20			ns

Driver Switching Characteristics (*Figures 4, 5* and *6*)

Parameter	Conditions	Min	Typ	Max		Units
				8922/23	8922A/23A	
SINGLE ENDED CHARACTERISTICS						
T_{pLH}	CL = 30 pF		12			ns
T_{pHL}	CL = 30 pF		12			ns
T_{TLH}	CL = 30 pF		5			ns
T_{THL}	CL = 30 pF		5			ns
$\lvert T_{pLH}-T_{pHL}\rvert$	CL = 30 pF		0.5			ns
Skew	CL = 30 pF (Note 5)		0.5	5	3.5	ns
Skew (Channel to Channel)			0.5	3.0	2.0	ns
T_{pLZ}	CL = 30 pF		15			ns
T_{pHZ}	CL = 30 pF		15			ns
T_{pZL}	CL = 30 pF		20			ns
T_{pZH}	CL = 30 pF		20			ns

Differential Switching Characteristics (Note 6, *Figure 7*)

Parameter	Conditions	Min	Typ	Max		Units
				8922/23	8922A/23A	
T_{pLH}	CL = 30 pF		12	15		ns
T_{pHL}	CL = 30 pF		12	15		ns
$\lvert T_{pLH}-T_{pHL}\rvert$	CL = 30 pF		0.5	6.0	2.75	ns

Note 5: Difference between complementary outputs at the 50% point.

Note 6: Differential Delays are defined as calculated results from single ended rise and fall time measurements. This approach in establishing AC performance specifications has been taken due to limitations of available Automatic Test Equipment (ATE).

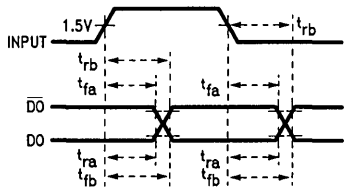
The calculated ATE results assume a linear transition between measurement points and are a result of the following equations:

$$Tcr = \frac{(Tfb \times Trb) - (Tra \times Tfa)}{Trb - Tra - Tfa + Tfb}$$

Where: Tcr = Crossing Point

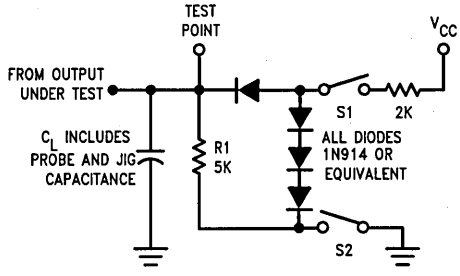
Tra, Trb, Tfa and Tfb are time measurements with respect to the input.

Switching Time Waveforms



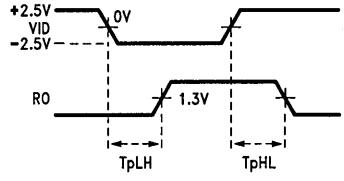
TL/F/8511–3

AC Test Circuits and Switching Waveforms



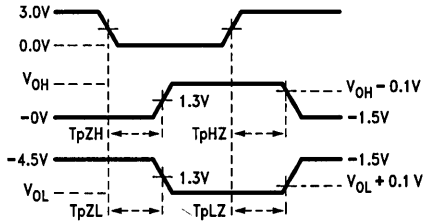
TL/F/8511–4

FIGURE 1



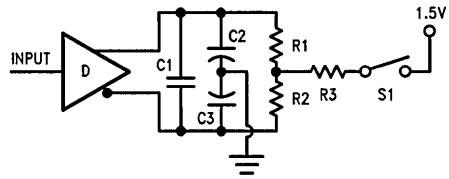
TL/F/8511–5

FIGURE 2



TL/F/8511–6

FIGURE 3



NOTE: C1=C2=C3=30 pF, R1=R2=50 Ω, R3=500 Ω

TL/F/8511–7

FIGURE 4

AC Test Circuit and Switching Waveforms (Continued)

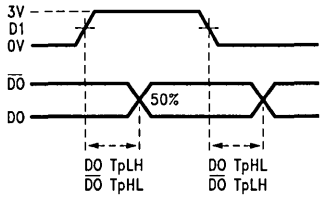


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FIGURE 5

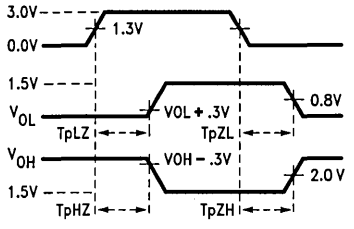

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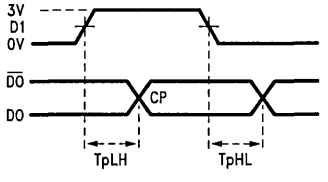
FIGURE 6

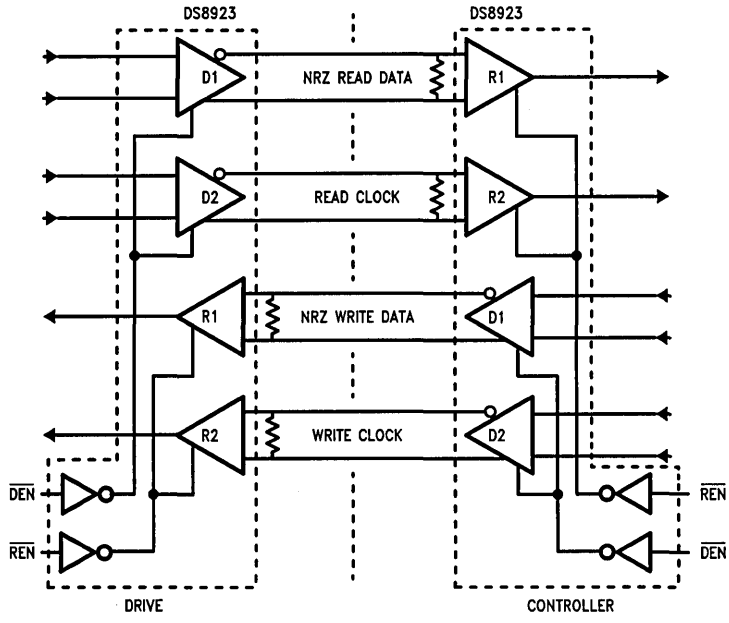


TL/F/8511–10

FIGURE 7

Typical Applications

ESDI Application



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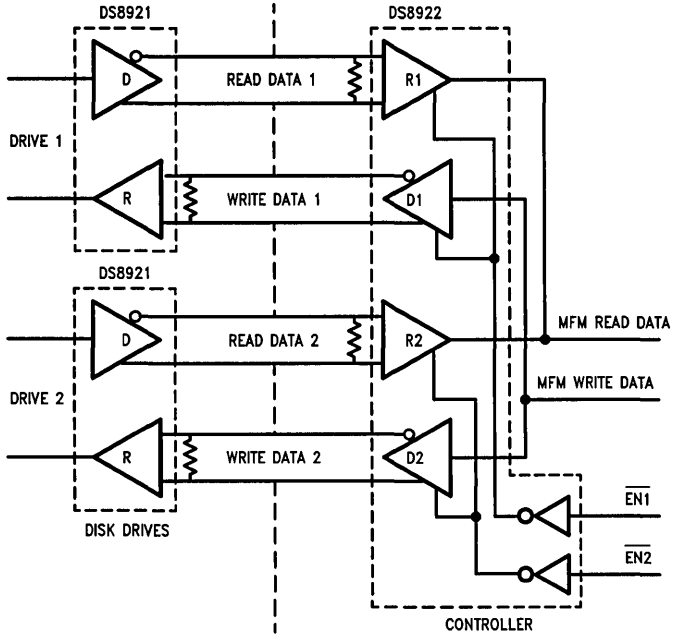
ST504 and ST412 Applications



TL/F/8511–12

National Semiconductor Corporation

DS8924 Quad TRI-STATE® Differential Line Driver

General Description

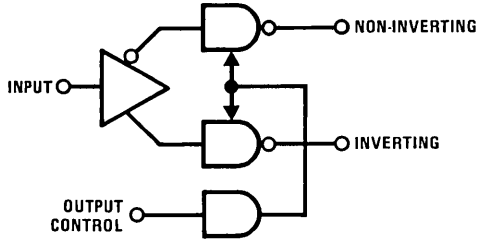
The DS8924 is a quad differential line driver designed for digital data transmission over balanced lines. The outputs are TRI-STATE® structures which are forced to a high impedance state when the appropriate output control pin reaches a logic zero condition. All input pins are PNP buffered to minimize input loading for either logic one or logic zero inputs. In addition, internal circuitry assures a high impedance output state during the transition between power up and power down.

The DS8924 is pin and functionally compatible with DS3487. It features improved performance over 3487-type circuit as outputs can source and sink 48 mA. In addition, outputs are not significantly affected by negative line reflections that can occur when the transmission line is unterminated at the receiver end.

Features

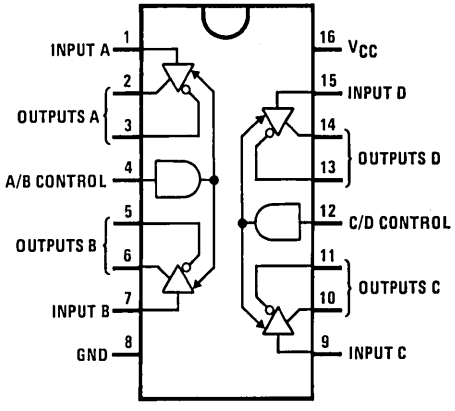
- Four independent driver chains
- TRI-STATE outputs
- PNP high impedance inputs
- Power up/down protection
- Fast propagation times (typ 12 ns)
- TTL compatible
- Single 5V supply voltage
- Output rise and fall times less than 20 ns (typ 10 ns)
- Pin compatible with DS3487 and MC3487
- Output skew—2 ns typ

Block and Connection Diagrams



TL/F/8507–1

Dual-In-Line Package



TL/F/8507–2

Top View

Order Number DS8924J or N
See NS Package J16A or N16A

Truth Table

Input	Control Input	Non-Inverter Output	Inverter Output
H	H	H	L
L	H	L	H
X	L	Z	Z

L = Low logic state
H = High logic state
X = Irrelevant
Z = TRI-STATE (high impedance)

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 4 sec.)	260°C

Maximum Power Dissipation* at 25°C

Cavity Package	1550 mW
Molded Package	1560 mW

*Derate cavity package 10.3 mW/°C above 25°C; derate molded package 12.5 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
DS8924	4.75	5.25	V
Temperature (T_A)			
DS8924	0	70	°C

Electrical Characteristics (Notes 2, 3, 4 and 5)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IL}	Input Low Voltage					0.8	V
V_{IH}	Input High Voltage			2.0			V
I_{IL}	Input Low Current	V_{IL} = 0.5V				−200	μA
I_{IH}	Input High Current		V_{IH} = 2.7V			50	μA
			V_{IH} = 5.5V			100	μA
V_{CL}	Input Clamp Voltage	I_{CL} = −18 mA				−1.5	V
V_{OL}	Output Low Voltage	I_{OL} = 48 mA				0.5	V
V_{OH}	Output High Voltage	I_{OH} = −20 mA		2.5			V
V_{OH}	Output High Voltage	I_{OH} = −48 mA		2.0			V
I_{OS}	Output Short-Circuit Current			−80		−260	mA
I_{OZ}	Output Leakage Current (TRI-STATE)		V_O = 0.5V			−100	μA
			V_O = 5.5V			100	μA
I_{OFF}	Output Leakage Current Power OFF	V_{CC} = 0	V_O = 6V			100	μA
			V_O = −0.25V			−100	μA
$\lvert V_{OS} - \overline{V}_{OS} \rvert$	Difference in Output Offset Voltage					0.4	V
V_T	Differential Output Voltage			2.0			V
$\lvert V_T \rvert - \lvert \overline{V}_T \rvert$	Difference in Differential Output Voltage					0.4	V
I_{CC}	Power Supply Current		Active		50	80	mA
			TRI-STATE		35	60	mA

Switching Characteristics V_{CC} = 5V, T_A = 25°C

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHL}	Input to Output			12	20	ns
t_{PLH}	Input to Output			12	20	ns
Skew	Output to Output	C_L = 50 pF		2.0	5.0	ns
t_{THL}	Differential Fall Time			10	20	ns
t_{TLH}	Differential Rise Time			10	20	ns
t_{PHZ}	Enable to Output	R_L = 200Ω, C_L = 50 pF		17	25	ns
t_{PLZ}	Enable to Output	R_L = 200Ω, C_L = 50 pF		20	30	ns
t_{PZH}	Enable to Output	R_L = ∞, C_L = 50 pF, S1 Open		13	25	ns
t_{PZL}	Enable to Output	R_L = 200Ω, C_L = 50 pF, S2 Open		17	30	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: Unless otherwise specified, min/max limits apply across the 0°C to +70°C range for the DS8924. All typicals are given for V_{CC} = 5V and T_A = 25°C.

Note 3: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified.

Note 4: Only one output at a time should be shorted.

Note 5: Symbols and definitions correspond to EIA RS-422, where applicable.

AC Test Circuits and Switching Time Waveforms

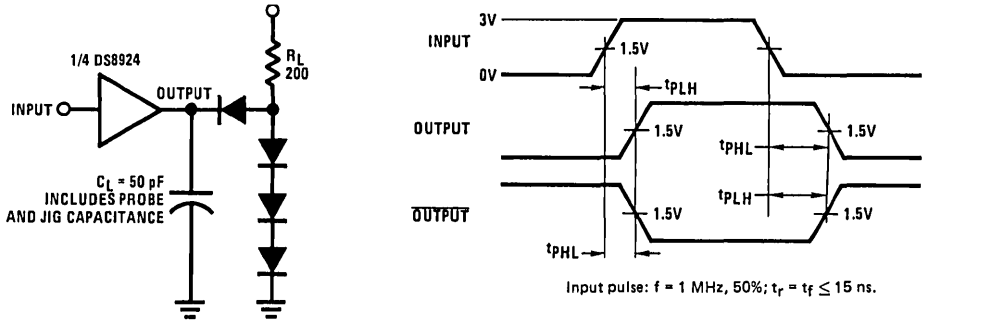


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FIGURE 1. Propagation Delays

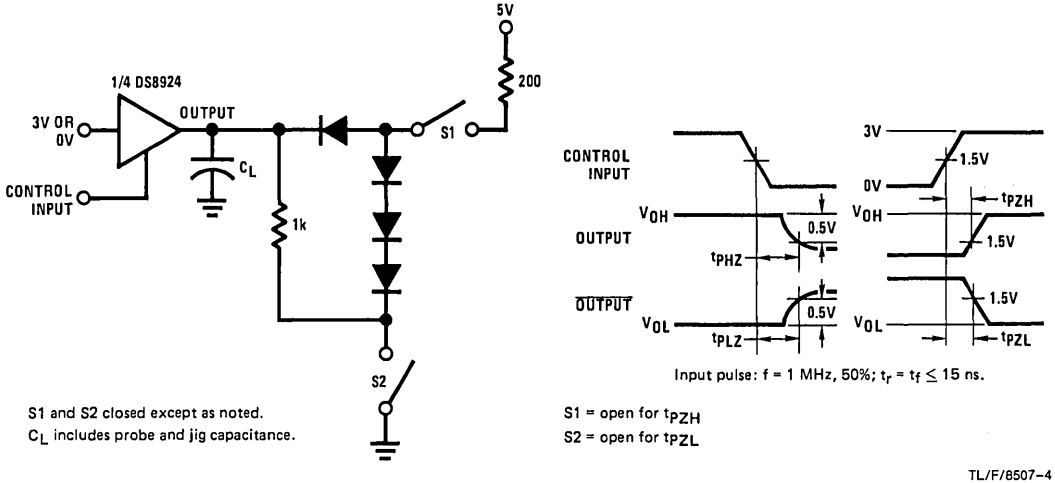

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FIGURE 2. TRI-STATE Enable and Disable Delays

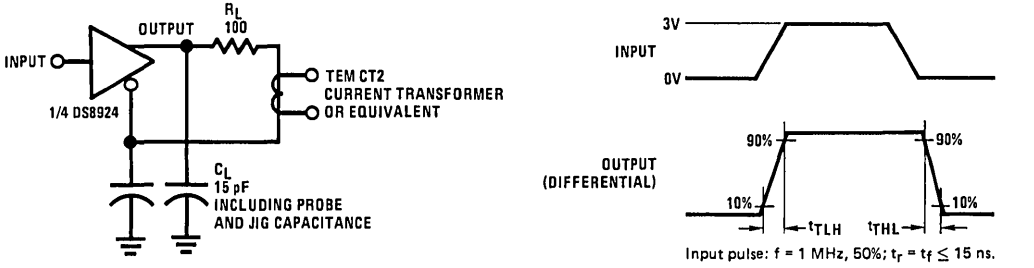

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FIGURE 3. Differential Rise and Fall Times

Integrated Circuits for Digital Data Transmission

National Semiconductor Corp.
Application Note 22

INTRODUCTION

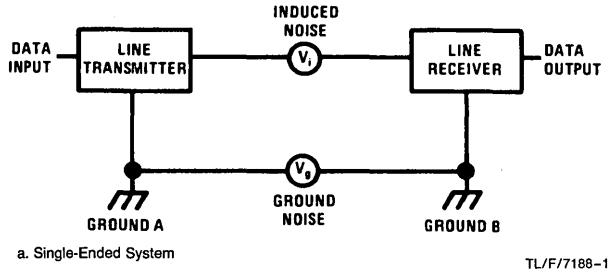
It is frequently necessary to transmit digital data in a high-noise environment where ordinary integrated logic circuits cannot be used because they do not have sufficient noise immunity. One solution to this problem, of course, is to use high-noise-immunity logic. In many cases, this approach would require worst case logic swings of 30V, requiring high power-supply voltages. Further, considerable power would be needed to transmit these voltage levels at high speed. This is especially true if the lines must be terminated to eliminate reflections, since practical transmission lines have a low characteristic impedance.

A much better solution is to convert the ground referred digital data at the transmission end into a differential signal and transmit this down a balanced, twisted-pair line. At the receiving end, any induced noise, or voltage due to ground-loop currents, appears equally on both ends of the twisted-pair line. Hence, a receiver which responds only to the differential signal from the line will reject the undesired signals even with moderate voltage swings from the transmitter.

Figure 1 illustrates this situation more clearly. When ground is used as a signal return as in *Figure 1a*, the voltage seen at the receiving end will be the output voltage of the transmitter plus any noise voltage induced in the signal line. Hence, the noise immunity of the transmitter-receiver combination must be equal to the maximum expected noise from both sources.

The differential transmission scheme diagrammed in *Figure 1b* solves this problem. Any ground noise or voltage induced on the transmission lines will appear equally on both inputs of the receiver. The receiver responds only to the differential signal coming out of the twisted-pair line and delivers a single-ended output signal referred to the ground at the receiving end. Therefore, extremely high noise immunities are not needed; and the transmitter and receiver can be operated from the same supplies as standard integrated logic circuits.

This article describes the operation and use of a line driver and line receiver for transmission systems using twisted-pair lines. The transmitter provides a buffered differential output from a DTL or TTL input signal. A four-input gate is included on the input so that the circuit can also perform logic. The receiver detects a zero crossing in the differential input voltage and can directly drive DTL or TTL integrated circuits at the receiving end. It also has strobe capability to blank out unwanted input signals. Both the transmitter and the receiver incorporate two independent units on a single silicon chip.



a. Single-Ended System

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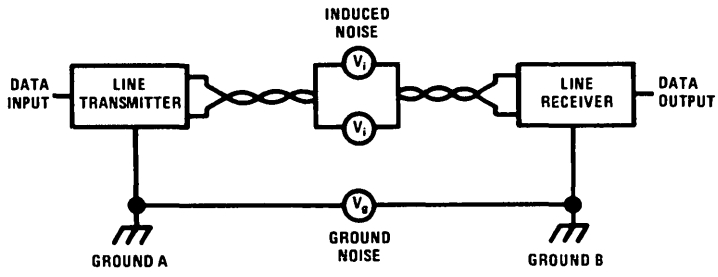

b. Difference System

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FIGURE 1. Comparing Differential and Single-Ended Data Transmission

LINE DRIVER

Figure 2 shows a schematic diagram of the line transmitter. The circuit has a marked resemblance to a standard TTL buffer. In fact, it is possible to use a standard dual buffer as a transmitter. However, the DS7830 incorporates additional features. For one, the output is current limited to protect the driver from accidental shorts in the transmission lines. Secondly, diodes on the output clamp sever voltage transients that may be induced into the transmission lines. Finally, the circuit has internal inversion to produce a differential output signal, reducing the skew between the outputs and making the output state independent of loading.

As can be seen from the upper half of *Figure 2*, a quadruple-emitter input transistor, Q9, provides four logic inputs to the transmitter. This transistor drives the inverter stage formed by Q10 and Q11 to give a NAND output. A low state logic input on any of the emitters of Q9 will cause the base drive to be removed from Q10, since Q9 will be saturated by current from R8, holding the base of Q10 near ground. Hence, Q10 and Q11 will be turned off; and the output will be in a high state. When all the emitters of Q9 are at a one logic level, Q10 receives base drive from R8 through the forward biased collector-base junction of Q9. This saturates Q10 and also Q11, giving a low output state. The input voltage at which the transition occurs is equal to the sum of the emitter-base turn on voltages of Q10 and Q11 minus the saturation voltage of Q9. This is about 1.4V at 25°C.

A standard "totem-pole" arrangement is used on the output stage. When the output is switched to the high state, with Q10 and Q11 cut off, current is supplied to the load by Q13 and Q14 which are connected in a modified Darlington configuration. Because of the high compound current gain of these transistors, the output resistance is quite low and a large load current can be supplied. R10 is included across the emitter-base junction of Q13 both to drain off any collector-base leakage current in Q13 and to discharge the collector-base capacitance of Q13 when the output is switched to

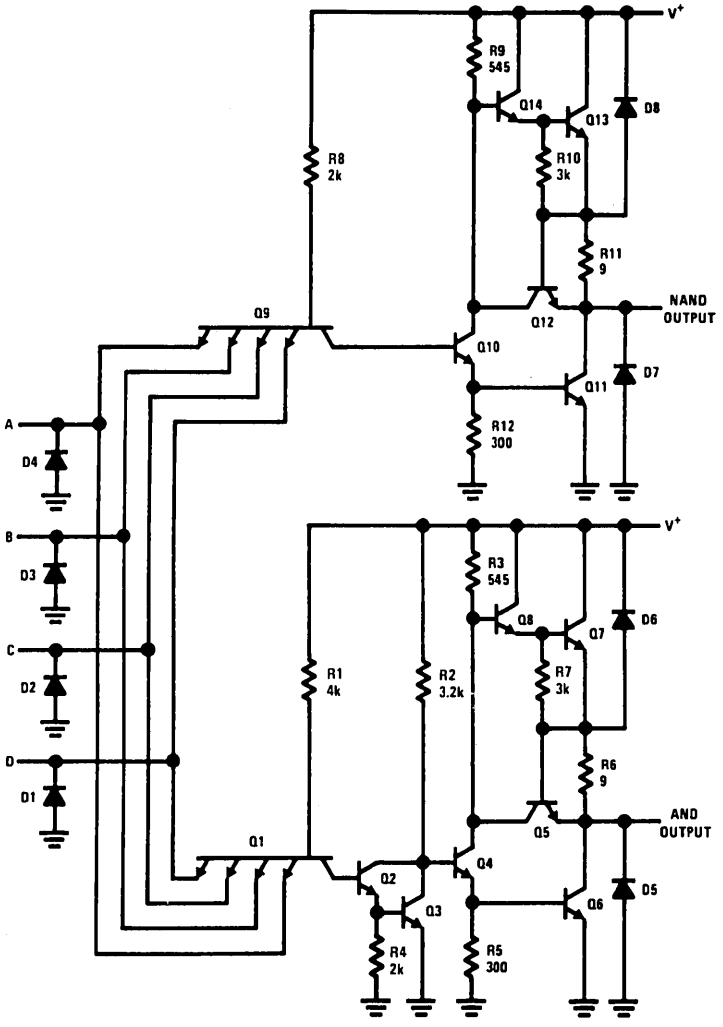

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FIGURE 2. Schematic Diagram of the DS7830 Line Driver

the low state. In the high state, the output level is approximately two diode drops below the positive supply, or roughly 3.6V at 25°C with a 5.0V supply.

With the output switched into the low state, Q10 saturates, holding the base of Q14 about one diode drop above ground. This cuts off Q13. Further, both the base current and the collector current of Q10 are driven into the base of Q11 saturating it and giving a low-state output of about 0.1V. The circuit is designed so that the base of Q11 is supplied 6 mA, so the collector can drive considerable load current before it is pulled out of saturation.

The primary purpose of R12 is to provide current to remove the stored charge in Q11 and charge its collector-base capacitance when the circuit is switched to the high state. Its value is also made less than R9 to prevent supply current transients which might otherwise occur* when the power supply is coming up to voltage.

The lower half of the transmitter in *Figure 2* is identical to the upper, except that an inverter stage has been added. This is needed so that an input signal which drives the output of the upper half positive will drive the lower half negative, and vice versa, producing a differential output signal. Transistors Q2 and Q3 produce the inversion. Even though the current gain is not necessarily needed, the modified Darlington connection is used to produce the proper logic transition voltage on the input of the transmitter. Because of the low load capacitance that the inverter sees when it is completely within the integrated circuit, it is extremely fast, with a typical delay of 3 ns. This minimizes the skew between the outputs.

One of the schemes used when dual buffers are employed as a differential line driver is to obtain the NAND output in the normal fashion and provide the AND output by connecting the input of the second buffer to the NAND output. Using an internal inverter has some distinct advantages over this: for one, capacitive loads which slow down the response of the NAND output will not introduce a time skew between the two outputs; secondly, line transients on the NAND output will not cause an unwanted change of state on the AND output.

Clamp diodes, D1 through D4, are added on all inputs to clamp undershoot. This undershoot and ringing can occur in TTL systems because the rise and fall times are extremely short.

Output-current limiting is provided by adding a resistor and transistor to each of the complementary outputs. Referring again to *Figure 2*, when the current on the NAND output increases to a value where the voltage drop across R11 is sufficient to turn on Q12, the short circuit protection comes into effect. This happens because further increases in output current flow into the base of Q12 causing it to remove base drive from Q14 and, therefore, Q13. Any substantial increase in output current will then cause the output voltage to collapse to zero. Since the magnitude of the short circuit depends on the emitter base turn-on voltage of Q12, this current has a negative temperature coefficient. As the chip temperature increases from power dissipation, the available short circuit current is reduced. The current limiting also serves to control the current transient that occurs when the output is going through a transition with both Q11 and Q13 turned on.

*J. Kalb, "Design Considerations for a TTL Gate", *National Semiconductor* TP-6, May, 1968.

The AND output is similarly protected by R6 and Q5, which limits the maximum output current to about 100 mA, preventing damage to the circuit from shorts between the outputs and ground.

The current limiting transistors also serve to increase the low state output current capability under severe transient conditions. For example, when the current into the NAND output becomes so high as to pull Q11 out of saturation, the output voltage will rise to two diode drops above ground. At this voltage, the collector-base junction of Q12 becomes forward biased and supplies additional base drive to Q11 through Q10 which is saturated. This minimizes any further increase in output voltage.

When either of the outputs are in the high state, they can drive a large current towards ground without a significant change in output voltage. However, noise induced on the transmission line which tries to drive the output positive will cut it off since it cannot sink current in this state. For this reason, D6 and D8 are included to clamp the output and keep it from being driven much above the supply voltage, as this could damage the circuit.

When the output is in a low state, it can sink a lot of current to clamp positive-going induced voltages on the transmission line. However, it cannot source enough current to eliminate negative-going transients so D5 and D7 are included to clamp those voltages to ground.

It is interesting to note that the voltage swing produced on one of the outputs when the clamp diodes go into conduction actually increases the differential noise immunity. For example with no induced common mode current, the low-state output will be a saturation voltage above ground while the high output will be two diode drops below the positive supply voltage. With positive-going common mode noise on the line, the low output remains in saturation; and the high output is clamped at a diode drop above the positive supply. Hence, in this case, the common mode noise increases the differential swing by three diode drops.

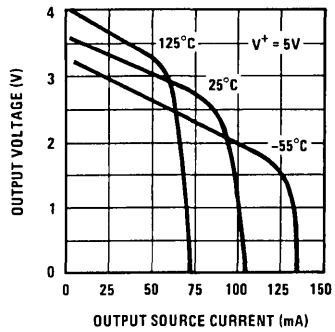

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FIGURE 3. High State Output Voltage as a Function of Output Current

Having explained the operation of the line driver, it is appropriate to look at the performance in more detail. *Figure 3* shows the high-state output characteristics under load. Over the normal range of output currents, the output resistance is about 10Ω. With higher output currents, the short circuit protection is activated, causing the output voltage to drop to zero. As can be seen from the figure, the short-circuit current decreases at higher temperatures to minimize the possibility of over-heating the integrated circuit.

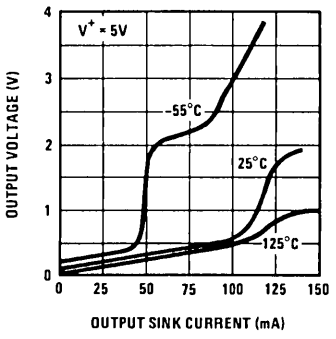

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FIGURE 4. Low-State Output Current as a Function of Output Current

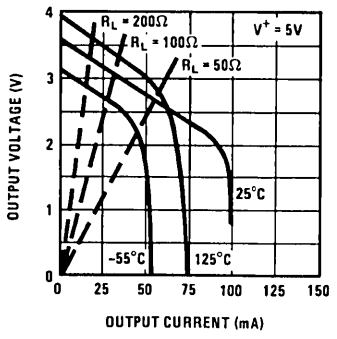

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FIGURE 5. Differential Output Voltage as a Function of Differential Output Current

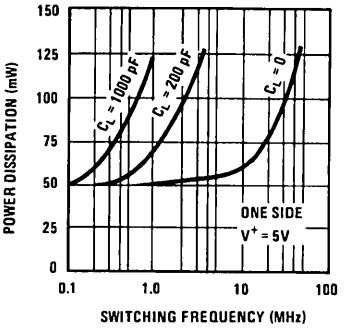

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FIGURE 6. Power Dissipation as a Function of Switching Frequency

Figure 4 is a similar graph of the low-state output characteristics. Here, the output resistance is about 5Ω with normal values of output current. With larger currents, the output transistor is pulled out of saturation; and the output voltage increases. This is more pronounced at −55°C where the transistor current gain is the lowest. However, when the output voltage rises about two diode drops above ground, the collector-base junction of the current-limit transistor becomes forward biased, providing additional base drive for the output transistor. This roughly doubles the current available for clamping positive common-mode transients on the twisted-pair line. It is interesting to note that even though the output level increases to about 2V under this condition, the differential noise immunity does not suffer because the high-state output also increases by about 3V with positive going common-mode transients.

It is clear from the figure that the low state output current is not effectively limited. Therefore, the device can be damaged by shorts between the output and the 5V supply. However, protection against shorts between outputs or from the outputs to ground is provided by limiting the high-state current.

The curves in *Figures 3* and *4* demonstrate the performance of the line driver with large, capacitively-coupled common-mode transients, or under gross overload conditions. *Figure 5* shows the ability of the circuit to drive a differential load: that is, the transmission line. It can be seen that for output currents less than 35 mA, the output resistance is approximately 15Ω. At both temperature extremes, the output falls off at high currents. At high temperatures, this is caused by current limiting of the high output state. At low temperatures, the fall off of current gain in the low-state output transistor produces this result.

Load lines have been included on the figure to show the differential output with various load resistances. The output swing can be read off from the intersection of the output characteristic with the load line. The figure shows that the driver can easily handle load resistances greater than 100Ω.

This is more than adequate for practical, twisted-pair lines.

Figure 6 shows the no load power dissipation, for one-half of the dual line driver, as a function of frequency. This information is important for two reasons. First, the increase in power dissipation at high frequencies must be added to the excess power dissipation caused by the load to determine the total package dissipation. Second, and more important, it is a measure of the "glitch" current which flows from the positive supply to ground through the output transistors when the circuit is going through a transition. If the output stage is not properly designed, the current spikes in the power supplies can become quite large; and the power dissipation can increase by as much as a factor of five between 100 kHz and 10 MHz. The figure shows that, with no capacitive loading, the power increases with frequencies as high as 10 MHz is almost negligible. However, with large capacitive loads, more power is required.

The line receiver is designed to detect a zero crossing in the differential output of the line driver. Therefore, the propagation time of the driver is measured as the time difference between the application of a step input and the point where the differential output voltage crosses zero. A plot of the propagation time over temperature is shown in *Figure 7*. This delay is added directly to the propagation time of the transmission line and the delay of the line receiver to determine the total data-propagation time. However, in most cases, the delay of the driver is small, even by comparison to the uncertainties in the other delays.

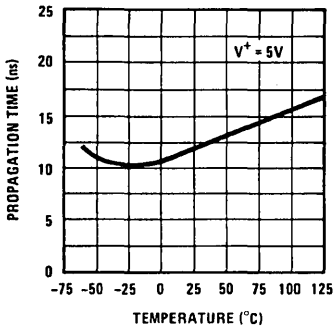

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FIGURE 7. Propagation Time as a Function of Temperature

To summarize the characteristics of the DS7830 line driver, the input interfaces directly with standard TTL circuits. It presents a load which is equivalent to a fan out of 3 to the circuit driving it, and it operates from the 5.0V, ±10% logic supplies. The output can drive low impedance lines down to 50Ω and capacitive loads up to 5000 pF. The time skew between the outputs is minimized to reduce radiation from the twisted-pair lines, and the circuit is designed to clamp common mode transients coupled into the line. Short circuit protection is also provided. The integrated circuit consists of two independent drivers fabricated on a 41 x 53 mil-square die using the standard TTL process. A photomicrograph of the chip is shown in *Figure 8*.

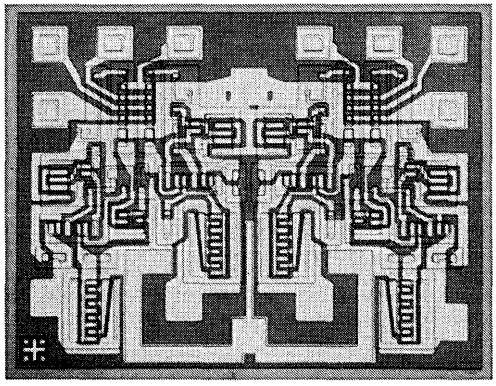

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FIGURE 8. Photomicrograph of the DS7830 Dual Line Driver

LINE RECEIVER

As mentioned previously, the function of the line receiver is to convert the differential output signal of the line driver into a single ended, ground-referred signal to drive standard digital circuits on the receiving end. At the same time it must reject the common mode and induced noise on the transmission line.

Normally this would not be too difficult a task because of the large signal swings involved. However, it was considered important that the receiver operate from the +5V logic supply without requiring additional supply voltages, as do most other line receiver designs. This complicates the situation because the receive must operate with ±15V input signals which are considerably greater than the operating supply voltage.

The large common mode range over which the circuit must work can be reduced with an attenuator on the input of the receiver. In this design, the input signal is attenuated by a factor of 30. Hence, the ±15V common mode voltage is reduced to ±0.5V, which can be handed easily by circuitry operating from a 5V supply. However, the differential input signal, which can go down as low as ±2.4V in the worst case, is also reduced to ±80 mV. Hence, it is necessary to employ a fairly accurate zero crossing detector in the receiver.

System requirements dictated that the threshold inaccuracy introduced by the zero crossing detector be less than 17 mV. In principle, this accuracy requirement should not pose insurmountable problems because it is a simple matter to make well matched parts in an integrated circuit.

Figure 9 shows a simplified schematic diagram of the circuit configuration used for the line receiver. The input signal is attenuated by the resistive dividers R1-R2 and R8-R3. This attenuated signal is fed into a balanced DC amplifier, operating in the common base configuration. This input amplifier, consisting of Q1 and Q2, removes the common mode component of the input signal. Further, it delivers an output signal at the collector of Q2, which is nearly equal in amplitude to the original differential input signal. this output signal is buffered by Q6 and drives an output amplifier, Q8. The output stage drives the logic load directly.

An understanding of the circuit can be obtained by first considering the input stage. Assuming high current gains and neglecting the voltage drop across R3, the collector current of Q1 will be:

$$I_{C1} = \frac{V^+ - V_{BE1} - V_{BE3} - V_{BE4}}{R11} \quad (1)$$

With equal emitter-base voltages for all transistors, this becomes:

$$I_{C1} = \frac{V^+ - 3V_{BE}}{R11} \quad (2)$$

The output voltage at the collector of Q2 will be:

$$V_{C2} = V^+ - I_{C2}R12 \quad (3)$$

When the differential input voltage to the receiver is zero, the voltages presented to the emitters of Q1 and Q2 will be equal. If Q1 and Q2 are matched devices, which is easy to arrange when they are fabricated close together on a single silicon chip, their collector currents will be equal with zero input voltage. Hence, the output voltage from Q2 can be determined by substituting (2) into (3):

$$V_{C2} = V^+ - \frac{R12}{R11}(V^+ - 3V_{BE}) \quad (4)$$

For R11 = R12, this becomes:

$$V_{C2} = 3V_{BE}$$

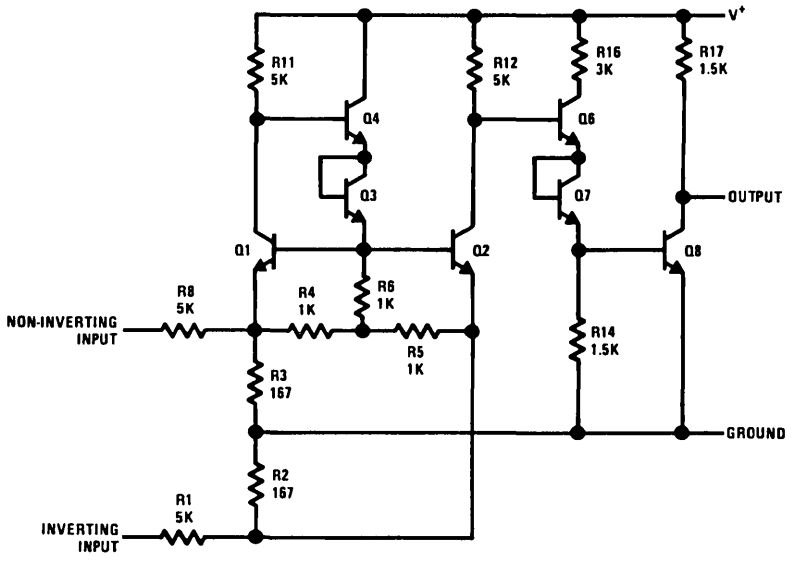

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FIGURE 9. Simplified Schematic of the Line Receiver

The voltage on the base of Q6 will likewise be $3V_{BE}$ when the output is on the verge of switching from a zero to a one state. A differential input signal which causes Q2 to conduct more heavily will then make the output go high, while an input signal in the opposite direction will cause the output to saturate.

It should be noted that the balance of this circuit is not affected by absolute values of components—only by how well they match. Nor is it affected by variations in the positive supply voltage, so it will perform well with standard logic supply voltages between 4.5V and 5.5V. In addition, component values are chosen so that the collector currents of Q4 and Q6 are equal. As a result, the base currents of Q4 and Q6 do not upset the balance of the input stage. This means that circuit performance is not greatly affected by production or temperature variations in transistor current gain.

A complete schematic of the line receiver, shown in *Figure 10*, shows several refinements of the basic circuit which are needed to secure proper operation under all conditions. For one, the explanation of the simplified circuit ignores the fact that the collector current of Q1 will be affected by common mode voltage developed across R3. This can give a 0.5V threshold error at the extremes of the ±15V common mode range. To compensate for this, a separate divider, R9 and R10, is used to maintain a constant collector current in Q1 with varying common mode signals. With an increasing common mode voltage on the non-inverting input, the voltage on the emitter of Q1 will increase. Normally, this would cause the voltage across R11 to decrease, reducing the collector current of Q1. However, the increasing common mode signal also drives the top end of R11 through R9 and R10 so as to hold the voltage drop across R11 constant.

In addition to improving the common mode rejection, R9 also forces the output of the receiver into the high state when nothing is connected to the input lines. This means that the output will be in a pre-determined state when the transmission cables are disconnected.

A diode connected transistor, Q5, is also added in the complete circuit to provide strobe capability. With a logic zero on the strobe terminal, the output will be high no matter what the input signal is. With the strobe, the receiver can be made immune to any noise signals during intervals where no digital information is expected. The output state with the strobe on is also the same as the output state with the input terminals open.

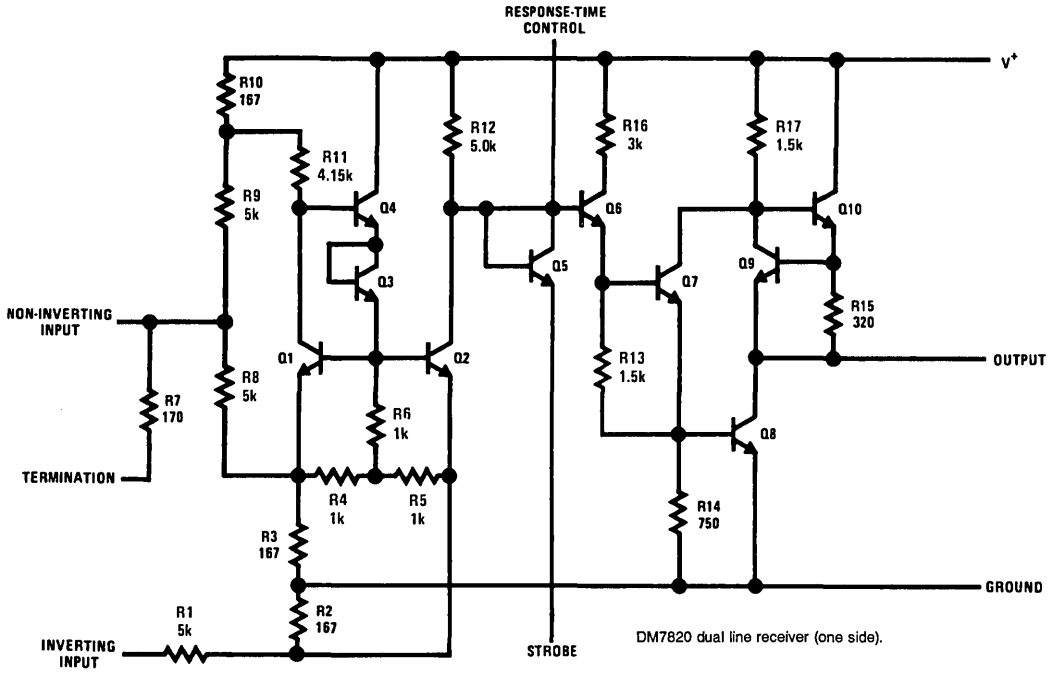

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FIGURE 10. Complete Schematic of One Half of the DS7820 Line Receiver

The collector of Q2 is brought out so that an external capacitor can be used to slow down the receiver to where it will not respond to fast noise spikes. This capacitor, which is connected between the response-time-control terminal and ground, does not give exactly-symmetrical delays. The delay for input signals which produce a positive-going output will be less than for input signals of opposite polarity. This happens because the impedance on the collector of Q2 drops as Q6 goes into saturation, reducing the effectiveness of the capacitor.

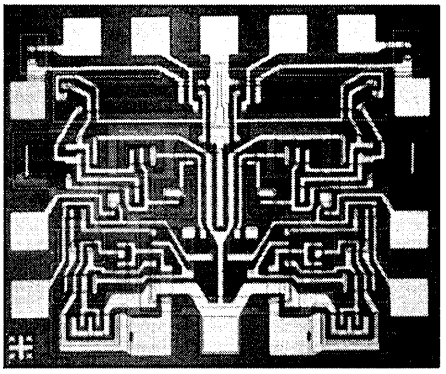
Another difference in the complete circuit is that the output stage is improved both to provide more gain and to reduce the output resistance in the high output state. This was accomplished by adding Q9 and Q10. When the output stage is operating in the linear region, that is, on the verge of switching to either the high or the low state, Q9 and Q10 form sort of an active collector load for Q8. The current through R15 is constant at approximately 2 mA as the output voltage changes through the active region. Hence, the percentage change in the collector current of Q8 due to the voltage change across R17 is made smaller by this pre-bias current; and the effective stage gain is increased.

With the output in the high state (Q8 cut off), the output resistance is equal to R15, as long as the load current is less than 2 mA. When the load current goes above this value, Q9 turns on; and the output resistance increases to 1.5k, the value of R17.

This particular output configuration gives a higher gain than either a standard DTL or TTL output stage. It can also drive enough current in the high state to make it compatible with TTL, yet outputs can be wire OR'ed as with DTL.

Remaining details of the circuit are that Q7 is connected as an emitter follower to make the circuit even less sensitive to transistor current gains. R16 limits the base drive to Q7 with the output saturated, while R17 limits the base drive to the output transistor, Q8. A resistor, R7, which can be used to terminate the twisted-pair line is also included on the chip. It is not connected directly across the inputs. Instead, one end is left open so that a capacitor can be inserted in series with the resistor. The capacitor significantly reduces the power dissipation in both the line transmitter and receiver, especially in low-duty-cycle applications, by terminating the line at high frequencies but blocking steady-state current flow in the terminating resistor.

Since line receivers are generally used repetitively in a system, the DS7820 has been designed with two independent receivers on a single silicon chip. The device is fabricated on a 41 x 49 mil-square die using the standard six mask planar-epitaxial process. The processing employed is identical to that used on TTL circuits, and the design does not impose any unusual demands on the processing. It is only required that various parts within the circuit match well, but this is easily accomplished in a monolithic integrated circuit without any special effort in manufacturing. A photomicrograph of the integrated circuit chip is shown in *Figure 11*.



TL/F/7188–12

FIGURE 11. Photomicrograph of the DS7820 Dual Line Receiver

The only components in the circuit which see voltages higher than standard logic circuits are the resistors used to attenuate the input signal. These resistors, R1, R7, R8 and R9, are diffused into a separate, floating, N-type isolation tub, so that the higher voltage is not seen by any of the transistors. For a ±15V input voltage range, the breakdown voltages required for the collector-isolation and collector-base diodes are only 15V and 19V, respectively. These breakdown voltages can be achieved readily with standard digital processing.

The purpose of the foregoing was to provide some insight into circuit operation. A more exact mathematical analysis of the device is developed in Appendix A.

RECEIVER PERFORMANCE

The characteristics of the line receiver are described graphically in *Figures 12* through *18*. *Figure 12* illustrates the effect of supply voltage variations on the threshold accuracy. The upper curve gives the differential input voltage required to hold the output at 2.5V while it is supplying 200 μA to the digital load. The lower curve shows the differential input needed to hold the output at 0.4V while it sinks 3.5 mA from the digital load. This load corresponds to a worst case fanout of 2 with either DTL or TTL integrated circuits. The data shows that the threshold accuracy is only affected by ±60 mV for a ±10% change in supply voltage. Proper operation can be secured over a wider range of supply voltages, although the error becomes excessive at voltages below 4V.

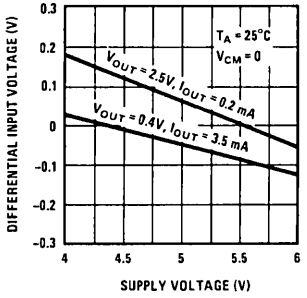


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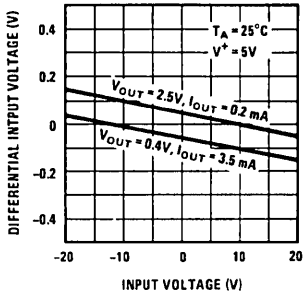
FIGURE 12. Differential Input Voltage Required for High or Low Output as a Function of Supply Voltage

Figure 13 is a similar plot for varying common mode input voltage. Again the differential input voltages are given for high and low states on the output with a worst case fanout of 2. With precisely matched components within the integrated circuit, the threshold voltage will not change with common mode voltage. The mismatches typically encountered give a threshold voltage change of ±100 mV over a ±20V common mode range. This change can have either a positive slope or a negative slope.



TL/F/7188–14

FIGURE 13. Differential Input Voltage Required for High or Low Output as a Function of Common Mode Voltage

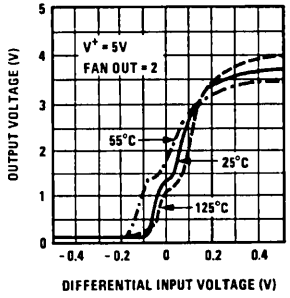


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FIGURE 14. Voltage Transfer Function

The transfer function of the circuit is given in *Figure 14*. The loading is for a worst case fanout of 2. The digital load is not linear, and this is reflected as a non-linearity in the transfer function which occurs with the output around 1.5V. These transfer characteristics show that the only significant effect of temperature is a reduction in the positive swing at −55°C. However, the voltage available remains well above the 2.5V required by digital logic.

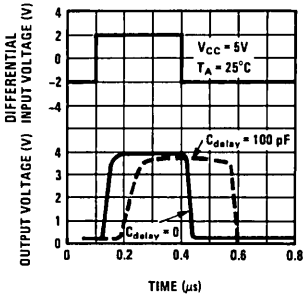

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FIGURE 15. Response Time with and without an External Delay Capacitor

Figure 15 gives the response time, or propagation delay, of the receiver. Normally, the delay through the circuit is about 40 ns. As shown, the delay can be increased, by the addition of a capacitor between the response-time terminal and ground, to make the device immune to fast noise spikes on the input. The delay will generally be longer for negative going outputs than for positive going outputs.

Under normal conditions, the power dissipated in the receiver is relatively low. However, with large common mode input voltages, dissipation increases markedly, as shown in *Figure 16*. This is of little consequence with common mode transients, but the increased dissipation must be taken into account when there is a DC difference between the grounds of the transmitter and the receiver. It is important to note that *Figure 16* gives the dissipation for one half the dual receiver. The total package dissipation will be twice the values given when both sides are operated under identical conditions.

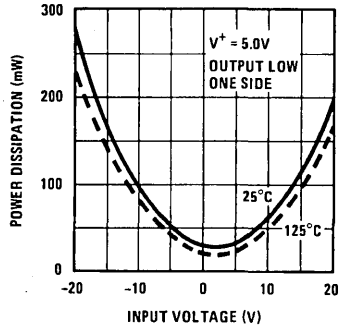

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FIGURE 16. Internal Power Dissipation as a Function of Common Mode Input Voltage

Figure 17 shows that the power supply current also changes with common mode input voltage due to the current drawn out of or fed into the supply through R9. The supply current reaches a maximum with negative input voltages and can actually reverse with large positive input voltages. The figure also shows that the supply current with the output switched into the low state is about 3 mA higher than with a high output.

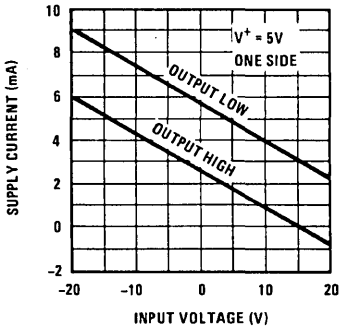

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FIGURE 17. Power Supply Current as a Function of Common Mode Input Voltage

The variation of the internal termination resistance with temperature is illustrated in *Figure 18*. Taking into account the initial tolerance as well as the change with temperature, the termination resistance is by no means precise. Fortunately, in most cases, the termination resistance can vary appreciably without greatly affecting the characteristics of the transmission line. If the resistor tolerance is a problem, however, an external resistor can be used in place of the one provided within the integrated circuit.

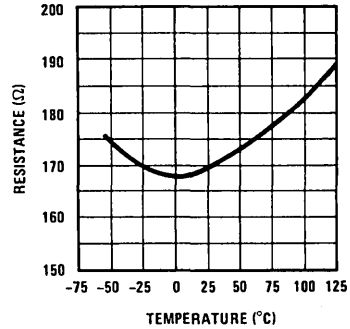

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FIGURE 18. Variation of Termination Resistance with Temperature

DATA TRANSMISSION

The interconnection of the DS7830 line driver with the DS7820 line receiver is shown in *Figure 19*. With the exception of the transmission line, the design is rather straightforward. Connections on the input of the driver and the output or strobe of the receiver follow standard design rules for DTL or TTL integrated logic circuits. The load presented by the driver inputs is equal to 3 standard digital loads, while the receiver can drive a worst-case fanout of 2. The load presented by the receiver strobe is equal to one standard load.

The purpose of C1 on the receiver is to provide DC isolation of the termination resistor for the transmission line. This capacitor can both increase the differential noise immunity, by reducing attenuation on the line, and reduce power dissipation in both the transmitter and receiver. In some applications, C1 can be replaced with a short between Pins 1 and 2, which connects the internal termination resistor of the DS7820 directly across the line. C2 may be included, if necessary, to control the response time of the receiver, making it immune to noise spikes that may be coupled differentially into the transmission lines.

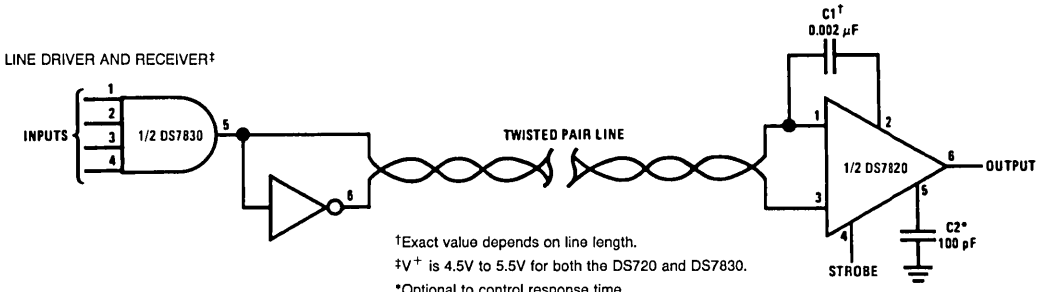

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FIGURE 19. Interconnection of the Line Driver and Line Receiver

The effect of termination mismatches on the transmission line is shown in *Figure 20.* The line was constructed of a twisted pair of No. 22 copper conductors with a characteristic impedance of approximately 170Ω. The line length was about 150 ns and it was driven directly from a DS7830 line driver. The data shows that termination resistances which are a factor of two off the nominal value do not cause significant reflections on the line. The lower termination resistors do, however, increase the attenuation.

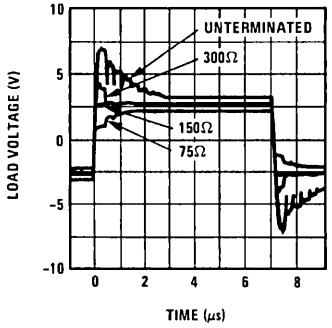

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FIGURE 20. Transmission Line Response with Various Termination Resistances

Figure 21 gives the line-transmission characteristics with various termination resistances when a DC isolation capacitor is used. The line is identical to that used in the previous example. It can be seen that the transient reponse is nearly the same as a DC terminated line. The attenuation, on the other hand, is considerably lower, being the same as an unterminated line. An added advantage of using the isolation capacitor is that the DC signal current is blocked from the termination resistor which reduces the average power drain of the driver and the power dissipation in both the driver and receiver.

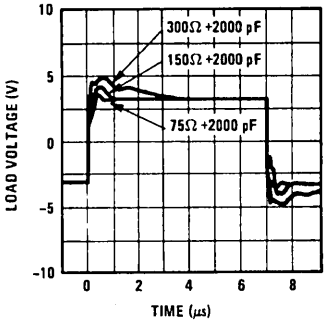

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FIGURE 21. Line Response for Various Termination Resistances with a DC Isolation Capacitor

The effect of different values of DC isolation capacitors is illustrated in *Figure 22.* This shows that the RC time constant of the termination resistor/isolation capacitor combination should be 2 to 3 times the line delay. As before, this data was taken for a 150 ns long line.

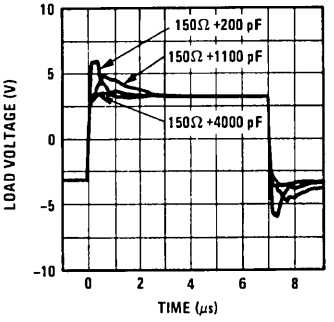

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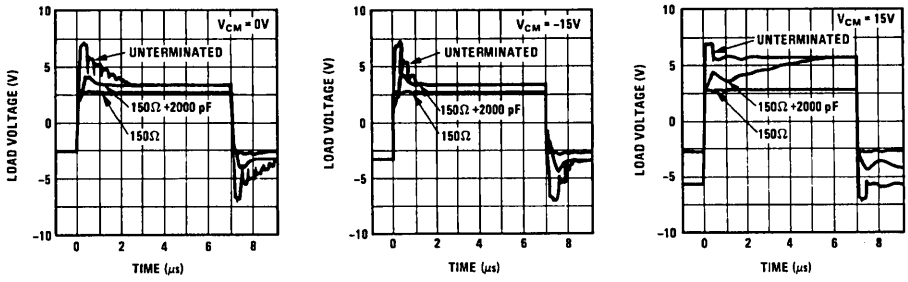
FIGURE 22. Response of Terminated Line with Different DC Isolation Capacitors



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a. V_{CM} = 0V b. V_{CM} = −15V c. V_{CM} = 15V

FIGURE 23. Line Response With Different Terminations and Common Mode Input Voltages

In *Figure 23*, the influence of a varying ground voltage between the transmitter and the receiver is shown. The difference in the characteristics arises because the source resistance of the driver is not constant under all conditions. The high output of the transmitter looks like an open circuit to voltages reflected from the receiving end of the transmission line which try to drive it higher than its normal DC state. This condition exists until the voltage at the transmitting end becomes high enough to forward bias the clamp diode on the 5V supply. Much of the phenomena which does not follow simple transmission-line theory is caused by this. For example, with an unterminated line, the overshoot comes from the reflected signal charging the line capacitance to where the clamp diodes are forward biased. The overshoot then decays at a rate determined by the total line capacitance and the input resistance of the receiver.

When the ground on the receiver is 15V more negative than the ground at the transmitting end, the decay with an unterminated line is faster, as shown in *Figure 23b*. This occurs because there is more current from the input resistor of the receiver to discharge the line capacitance. With a terminated line, however, the transmission characteristics are the same as for equal ground voltages because the terminating resistor keeps the line from getting charged.

Figure 23c gives the transmission characteristics when the receiver ground is 15V more positive than the transmitter ground. When the line is not terminated, the differential voltage swing is increased because the high output of the driver will be pulled against the clamp diodes by the common mode input current of the receiver. With a DC isolation capacitor, the differential swing will reach this same value with a time constant determined by the isolation capacitor and the input resistance of the receiver. With a DC coupled termination, the characteristics are unchanged because the differential load current is large by comparison to the common mode current so that the output transistors of the driver are always conducting.

The low output of the driver can also be pulled below ground to where the lower clamp diode conducts, giving effects which are similar to those described for the high output. However, a current of about 9 mA is required to do this, so it does not happen under normal operating conditions.

To summarize, the best termination is an RC combination with a time constant approximately equal to 3 times the transmission-line delay. Even though its value is not precisely determined, the internal termination resistor of the integrated circuit can be used because the line characteristics are not greatly affected by the termination resistor.

The only place that an RC termination can cause problems is when the data transmission rate approaches the line delay and the attenuation down the line (terminated) is greater than 3 dB. This would correspond to more than 1000 ft. of twisted-pair cable with No. 22 copper conductors. Under these conditions, the noise margin can disappear with low-duty-cycle signals. If this is the case, it is best to operate the twisted-pair line without a termination to minimize transmission losses. Reflections should not be a problem as they will be absorbed by the line losses.

CONCLUSION

A method of transmitting digital information in high-noise environments has been described. The technique is a much more attractive solution than high-noise-immunity logic as it has lower power consumption, provides more noise rejection, operates from standard 5V supplies, and is fully compatible with almost all integrated logic circuits. An additional advantage is that the circuits can be fabricated with integrated circuit processes used for standard logic circuits.

APPENDIX A

LINE RECEIVER

Design Analysis

The purpose of this appendix is to derive mathematical expressions describing the operation of the line receiver. It will be shown that the performance of the circuit is not greatly affected by the absolute value of the components within the integrated circuit or by the supply voltage. Instead, it depends mostly on how well the various parts match.

The analysis will assume that all the resistors are well matched in ratio and that the transistors are likewise matched, since this is easily accomplished over a broad temperature range with monolithic construction. However, the effects of component mismatching will be discussed where important. Further, large transistor current gains will be assumed, but it will be pointed out later that this is valid for current gains greater than about 10.

A schematic diagram of the DS7820 line receiver is shown in *Figure A-1*. Referring to this circuit, the collector current of the input transistor is given by

$$I_{C1} = \frac{V^+ - V_{BE1} - V_{BE3} - V_{BE4}}{R9//R10 + R11 + R3//R8} - \frac{\frac{R3}{R4 + 2R6 + R3} V_{BE1} - \frac{R3//R11}{R8 + R3//R1} V_{IN}}{R9//R10 + R11 + R3//R8} + \frac{(V_{IN} - V^+)\frac{R10//R11}{R9 + R10//R11}}{R9//R10 + R11 + R3//R8} \quad (A.1)$$

where V_{IN} is the common mode input voltage and $R_a//R_b$ denotes the parallel connection of the two resistors. In Equation (A.1), R8 = R9, R3 = R10, R10 ≪ R11, R9 ≫ R10, R3 ≪ R11, R8 ≫ R3 and

$$\frac{R3}{R4 + 2R6 + R3} \ll 3$$

so it can be reduced to

$$I_{C1} = \frac{V^+ - 3V_{BE} - \frac{R10}{R9} V^+}{R10 + R11 + R3} \quad (A.2)$$

which shows that the collector current of Q1 is not affected by the common mode voltage.

The output voltage on the collector of Q2 is

$$V_{C2} = V^+ - I_{C2}R12 \quad (A.3)$$

For zero differential input voltage, the collector currents of Q1 and Q2 will be equal so Equation (A.3) becomes

$$V_{C2} = V^+ - \frac{R12\left(V^+ - 3V_{BE} - \frac{R10}{R9} V^+\right)}{R10 + R11 + R3} \quad (A.4)$$

It is desired that this voltage be $3V_{BE}$ so that the output stage is just on the verge of switching with zero input. Forcing this condition and solving for R12 yields

$$R12 = (R10 + R11 + R3)\frac{V^+ - 3V_{BE}}{V^+ - 3V_{BE} - \frac{R10}{R9} V^+} \quad (A.5)$$

This shows that the optimum value of R12 is dependent on supply voltage. For a 5V supply it has a value of 4.7 kΩ. Substituting this and the other component values into (A.4),

$$V_{C2} = 2.83V_{BE} + 0.081V^+, \quad (A.6)$$

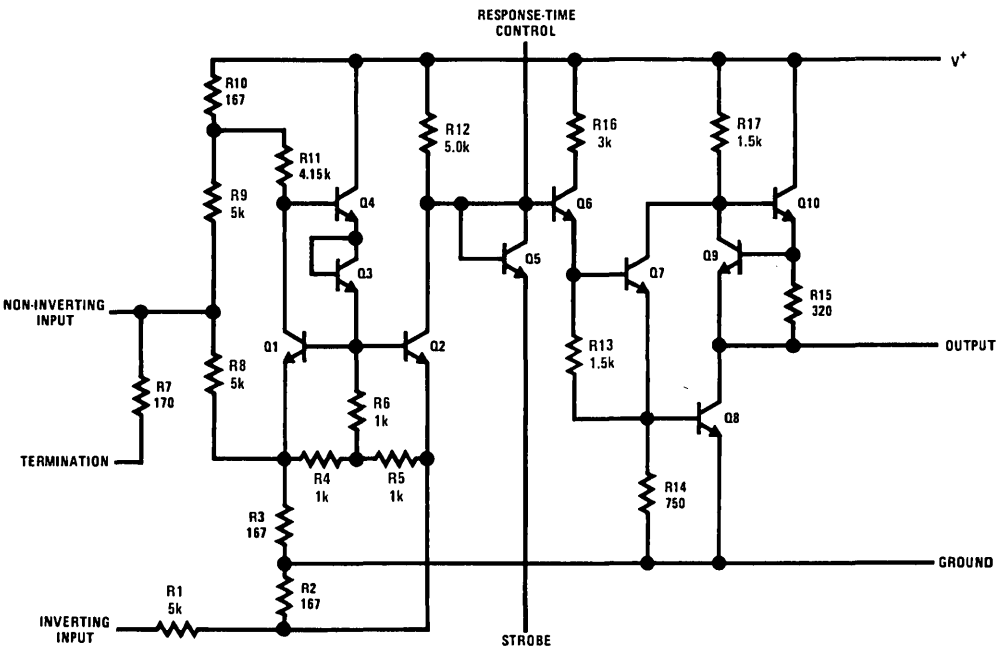

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FIGURE A-1. Schematic Diagram of One Half of the DS7820 Line Receiver

which shows that the voltage on the collector of Q2 will vary by about 80 mV for a 1V change in supply voltage.

The next step in the analysis is to obtain an expression for the voltage gain of the input stage.

An equivalent circuit of the input stage is given in *Figure A-2.* Noting that R6 = R7 = R8 and R2 ≅ 0.1 (R6 + R7//R8), the change in the emitter current of Q1 for a change in input voltage is

$$\Delta I_{E2} = \frac{0.9\,R2}{R1\,(0.9\,R2 + R_{E2})}\,\Delta V_{IN} \qquad (A.7)$$

Hence, the change in output voltage will be

$$\Delta V_{OUT} = \alpha I_{E2} R12$$

$$= \frac{0.9\,\alpha\,R2\,R12}{R1\,(0.9\,R2 + R_{E2}}\,\Delta V_{IN} \qquad (A.8)$$

Since $\alpha \cong 1$, the voltage gain is

$$A_{V1} = \frac{0.9\,R2\,R12}{R1\,(0.9\,R2 + R_{E2})} \qquad (A.9)$$

The emitter resistance of Q2 is given by

$$R_{E2} = \frac{kT}{qI_{C2}} \qquad (A.10)$$

where

$$I_{C2} = \frac{V^+ - 3V_{BE}}{R12} \qquad (A.11)$$

so

$$R_{E2} = \frac{kT\,R12}{q\,(V^+ - 3V_{BE})} \qquad (A.12)$$

Therefore, at 25°C where V_{VE} = 670 mV and kT/q = 26 mV, the computed value for gain is 0.745. The gain is not greatly affected by temperature as the gain at −55°C where V_{BE} = 810 mV and kT/q = 18 mV is 0.774, and the gain at 125°C where V_{BE} = 480 mV and kT/q = 34 mV is 0.730.

With a voltage gain of 0.75, the results of Equation (A.6) show that the input referred threshold voltage will change by 0.11V for a 1V change in supply voltage. With the standard ±10-percent supplies used for logic circuits, this means that the threshold voltage will change by less than ±60 mV.

Finally, the threshold error due to finite gain in the output stage can be considered. The collector current of Q7 from the bleeder resistor R14, is large by comparison to the base current of Q8, if Q8 has a reasonable current gain. Hence, the collector current of Q7 does not change appreciably when the output switches from a logic one to a logic zero. This is even more true for Q6, an emitter follower which drives Q7. Therefore, it is safe to presume that Q6 does not load the output of the first-stage amplifier, because of the compounded current gain of the three transistors, and that Q8 is driven from a low resistance source.

It follows that the gain of the output stage can be determined from the change in the emitter-base voltage of Q8 required to swing the output from a logic one state to a logic zero state. The expression

$$\Delta V_{BE} = \frac{kT}{q} \log_e \frac{I_{C1}}{I_{C2}} \qquad (A.13)$$

describes the change in emitter-base voltage required to vary the collector current from one value, I_{C1}, to a second, I_{C2}. With the output of the receiver in the low state, the collector current of Q8 is

$$I_{OL} = \frac{V^+ - V_{OL} - V_{BE9} - V_{BE10}}{R17} + \frac{V_{BE9}}{R15} - \frac{V_{BE8}}{R14} + \frac{V_{BE7}}{R13} + I_{SINK}, \qquad (A.14)$$

where V_{OL} is the low state output voltage and I_{SINK} is the current load from the logic that the receiver is driving. Noting that R13 = 2R14 and figuring that all the emitter-base voltages are the same, this becomes

$$I_{OL} = \frac{V^+ - V_{OL} - 2V_{BE}}{R17} + \frac{V_{BE}}{R15} - \frac{V_{BE}}{2R14} + I_{SINK} \qquad (A.15)$$

Similarly, with the output in the high state, the collector current of Q8 is

$$I_{OH} = \frac{V^+ - V_{OH} - V_{BE9} - V_{BE10}}{R17} + \frac{V_{BE9}}{R15} - \frac{V_{BE8}}{R14} + \frac{V_{BE7}}{R13} - I_{SOURCE}, \qquad (A.16)$$

where V_{OH} is the high-level output voltage and I_{SOURCE} is the current needed to supply the input leakage of the digital circuits loading the comparator.

With the same conditions used in arriving at (A.15), this becomes

$$I_{OH} = \frac{V^+ - V_{OH} - 2V_{BE}}{R17} + \frac{V_{BE}}{R15} - \frac{V_{BE}}{2R14} - I_{SOURCE} \qquad (A.17)$$

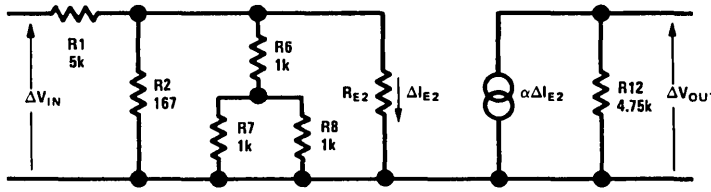

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FIGURE A-2. Equivalent Circuit Used to Calculate Input Stage Gain

From (A.13) the change in the emitter-base voltage of Q8 in going from the high output level to the low output level is

$$\Delta V_{BE} = \frac{kT}{q} \log_e \frac{I_{OL}}{I_{OH}} \qquad (A.18)$$

providing that Q8 is not quite in saturation, although it may be on the verge of saturation.

The change of input threshold voltage is then

$$\Delta V_{TH} = \frac{kT}{qA_{v1}} \log_e \frac{I_{OL}}{I_{OH}} \qquad (A.19)$$

where A_{v1} is the input stage gain. With a worst case fanout of 2, where $V_{OH} = 2.5V$, $V_{OL} = 0.4V$, $I_{SOURCE} = 40\ \mu A$ and $I_{SINK} = 3.2$ mA, the calculated change in threshold is 37 mV at 25°C, 24 mV at −55°C and 52 mV at 125°C.

The measured values of overall gain differ by about a factor of two from the calculated gain. This is not too surprising because a number of assumptions were made which introduce small errors, and all these errors lower the gain. It is also not too important because the gain is high enough where another factor of two reduction would not cause the circuit to stop working.

The main contributors to this discrepancy are the non-ideal behavior of the emitter-base voltage of Q8 due to current crowding under the emitter and the variation in the emitter base voltage of Q7 and Q8 with changes in collector-emitter voltage (h_{RE}).

Although these parameters can vary considerably with different manufacturing methods, they are relatively fixed for a given process. The ΔV_{BE} errors introduced by these quantities, if known, can be added directly into Equation (A.18) to give a more accurate gain expression.

The most stringent matching requirement in the receiver is the matching of the input stage divider resistors: R1 with R8 and R2 with R3. As little as 1% mismatch in one of these pairs can cause a threshold shift of 150 mV at the extremes of the ±15V common mode range. Because of this, it is necessary to make the resistors absolutely identical and locate them close together. In addition, since R1 and R8 do dissipate a reasonable amount of power, they have to be located to minimize the thermal gradient between them. To do this, R9 was located between R1 and R8 so that it would heat both of these resistors equally. There are not serious heating problems with R2 and R3; however, because of their low resistance value, it was necessary even to match the lengths of the aluminum interconnects, as the resistance of the aluminum is high enough to cause intolerable mismatches. Of secondary importance is the matching of Q1 and Q2 and the matching of ratios between R11 and R12. A 1 mV difference in the emitter-base voltages of Q1 and Q2 causes a 30 mV input offset voltage as does a 1% mismatch in the ratio of R11 to R12.

The circuit is indeed insensitive to transistor current gains as long as they are above 10. The collector currents of Q4 and Q6 are made equal so that their base currents load the collectors of Q1 and Q2 equally. Hence, the input threshold voltage is affected only by how well the current gains match. Low current gain in the output transistor, Q8, can cause a reduction in gain. But even with a current gain of 10, the error produced in the input threshold voltage is less than 50 mV.

Transmission Line Characteristics

National Semiconductor Corp.
Application Note 108
Bill Fowler

INTRODUCTION

Digital systems generally require the transmission of digital signals to and from other elements of the system. The component wavelengths of the digital signals will usually be shorter than the electrical length of the cable used to connect the subsystems together and, therefore, the cables should be treated as a transmissions line. In addition, the digital signal is usually exposed to hostile electrical noise source which will require more noise immunity then required in the individual subsystems environment.

The requirements for transmission line techniques and noise immunity are recognized by the designers of subsystems and systems, but the solutions used vary considerably. Two widely used example methods of the solution are shown in *Figure 1.* The two methods illustrated use unbalanced and balanced circuit techniques. This application note will delineate the characteristics of digital signals in transmission lines and characteristics of the line that effect the quality, and will compare the unbalanced and balanced circuits performance in digital systems.

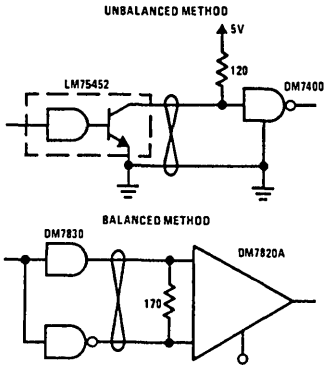

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FIGURE 1

NOISE

The cables used to transmit digital signals external to a subsystem and in route between the subsystem, are exposed to external electromagnetic noise caused by switching transients from actuating devices of neighboring control systems. Also external to a specific subsystem, another subsystem may have a ground problem which will induce noise on the system, as indicated in *Figure 2.*

The signals in adjacent wires inside a cable may induce electromagnetic noise on other wires in the cable. The induced electromagnetic noise is worse when a line terminated at one end of the cable is near to a driver at the same end, as shown in *Figure 3.* Some noise may be induced from relay circuits which have very large transient voltage swings compared to the digital signals in the same cable. Another source of induced noise is current in the common ground wire or wires in the cable.

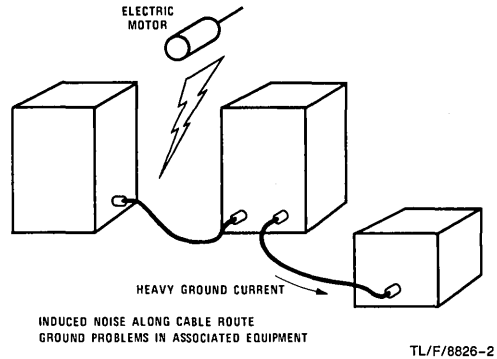

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FIGURE 2. External Noise Sources

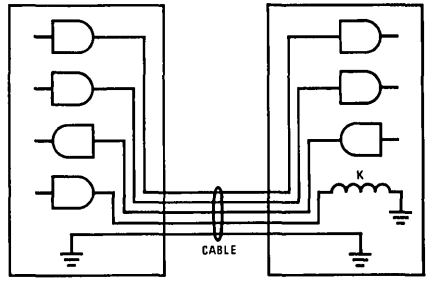

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FIGURE 3. Internal Noise Sources

DISTORTION

The objective is the transmission and recovery of digital intelligence between subsystems, and to this end, the characteristics of the data recovered must resemble the data transmitted. In *Figure 4* there is a difference in the pulse width of the data and the timing signal transmitted, and the corresponding signal received. In addition there is a further difference in the signal when the data is "AND"ed with the timing signal. The distortion of the signal occurred in the transmission line and in the line driver and receiver.

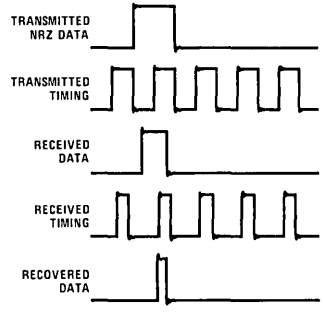

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FIGURE 4. Effect of Distortion

A primary cause of distortion is the effect the transmission line has on the rise time of the transmitted data. *Figure 5* shows what happens to a voltage step from the driver as it travels down the line. The rise time of the signal increases as the signal travels down the line. This effect will tend to affect the timing of the recovered signal.

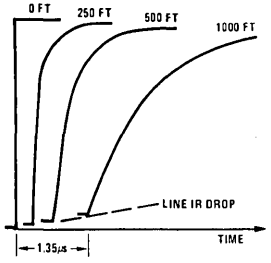

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FIGURE 5. Signal Response at Receiver

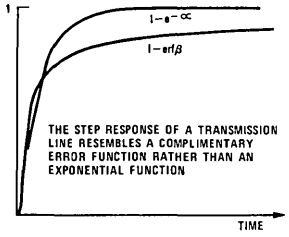

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FIGURE 6. Signal Rise Time

The rise time in a transmission line is not an exponential function but a complementary error function. The high frequency components of the step input are attenuated and delayed more than the low frequency components. This attenuation is inversely proportional to the frequency. Notice in *Figure 6* particularly that the signal takes much longer to reach its final DC value. This effect is more significant for fast risetimes.

The Duty Cycle of the transmitted signal also causes distortion. The effect is related to the signal rise time as shown in *Figure 7*. The signal doesn't reach one logic level before the signal changes to another level. If the signal has a ½ (50%) Duty Cycle and the threshold of the receiver is halfway between the logic levels, the distortion is small. But if the Duty Cycle is ⅛ as shown in the second case the signal is considerably distorted. In some cases, the signal may not reach the receiver threshold at all.

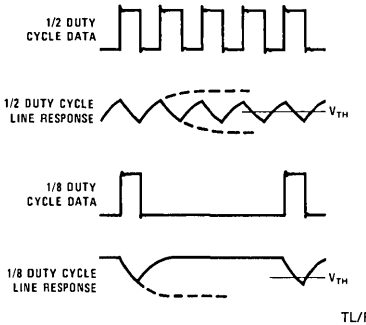

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FIGURE 7. Signal Distortion Due to Duty Cycle

In the previous example, it was assumed that the threshold of the receiver was halfway between the ONE and ZERO logic levels. If the receiver threshold isn't halfway the receiver will contribute to the distortion of the recovered signal. As shown in *Figure 8,* the pulse time is lengthened or shortened, depending on the polarity of the signal at the receiver. This is due to the offset of the receiver threshold.

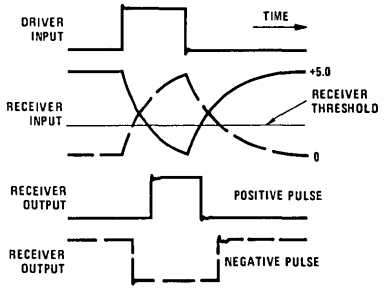

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FIGURE 8. Slicing Level Distortion

UNBALANCED METHOD

Another source of distortion is caused by the IR losses in the wire. *Figure 9* shows the IR losses that occur in a thousand feet of no. 22 AWG wire. Notice in this example that the losses reduce the signal below the threshold of the receiver in the unbalanced method. Also that part of the IR drop in the ground wire is common to other circuits—this ground signal will appear as a source of noise to the other unbalanced line receivers in the system.

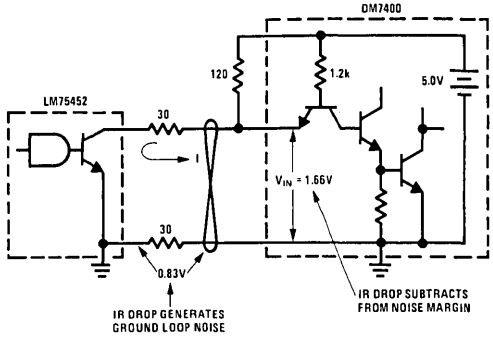

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FIGURE 9. Unbalanced Method

Transmission lines don't necessarily have to be perfectly terminated at both ends, (as will be shown later) but the termination used in the unbalanced method will cause additional distortion. *Figure 10* shows the signal on the transmission line at the driver and at the receiver. In this case the receiver was terminated in 120Ω, but the characteristic impedance of the line is much less. Notice that the wave forms have significant steps due to the incorrect termination of the line. The signal is subject to misinterpretation by the line receiver during the period of this signal transient because of the distortion caused by Duty Cycle and attenuation. In addition, the noise margin of the signal is reduced.

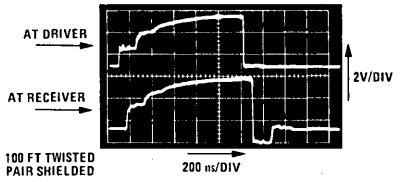

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FIGURE 10. LM75451, DM7400 Line Voltage Waveforms

The signal waveforms on the transmission line can be estimated before hand by a reflection diagram. *Figure 11* shows the reflection diagram of the rise time wave forms. The voltage versus current plot on left is used to predict the transient rise time of the signal shown on the right. The initial condition on the transmission line is an IR drop across the line termination. The first transient on the line traverses from this initial point to zero current. The path it follows corresponds to the characteristic impedance of the line. The second transient on the diagram is at the line termination. As shown, the signal reflects back and forth until it reaches its final DC value.

Figure 12 shows the reflection diagram of the fall time. Again the signal reflects back and forth between the line termination until it reaches its final DC value. In both the rise and fall time diagrams, there are transient voltage and current signals that subtract from the particular signal and add to the system noise.

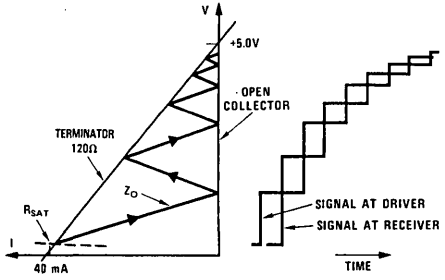

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FIGURE 11. Line Reflection Diagram of Rise Timer

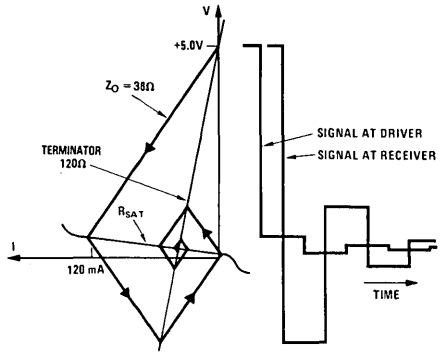

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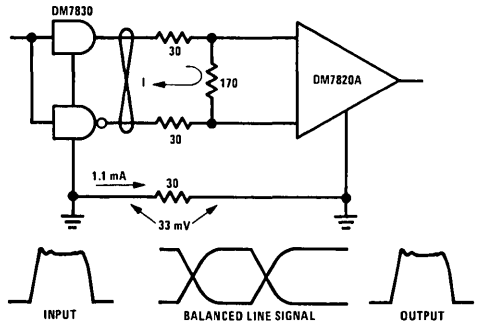
FIGURE 12. Line Reflection Diagram of Fall Time

BALANCED METHOD

In the balanced method shown in *Figure 13*, the transient voltages and currents on the line are equal and opposite and cancel each others noise. Also unlike the unbalanced method, they generate very little ground noise. As a result, the balanced circuit doesn't contribute to the noise pollution of its environment.



THE GROUND LOOP CURRENT IS MUCH LESS THAN SIGNAL CURRENT

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FIGURE 13. Cross Talk of Signals

The circuit used for a line receiver in the balanced method is a differential amplifier. *Figure 14* shows a noise transient induced equally on lines A and line B from line C. Because the signals on line A and B are equal, the signals are ignored by the differential line receiver.

Likewise for the same reason, the differential signals on lines A and B from the driver will not induce transients on line C. Thus, the balanced method doesn't generate noise and also isn't susceptible to noise. On the other hand the unbalanced method is more sensitive to noise and also generates more noise.

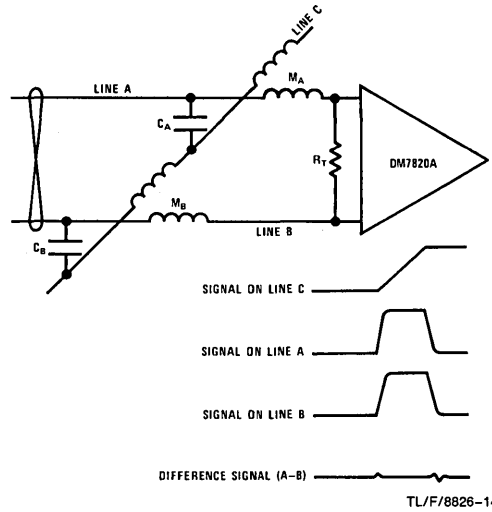

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FIGURE 14. Cross Talk of Signals

The characteristic impedance of the unbalanced transmission line is less than the impedance of the balanced transmission line. In the unbalanced method there is more capacitance and less inductance than in the balanced method. In the balanced method the Reactance to adjacent wires is almost cancelled (see *Figure 15*). As a result a transmission line may have a 60Ω unbalanced impedance and a 90Ω balanced impedance. This means that the unbalanced

method, which is more susceptible to IR drop, must use a smaller value termination, which will further increase the IR drop in the line.

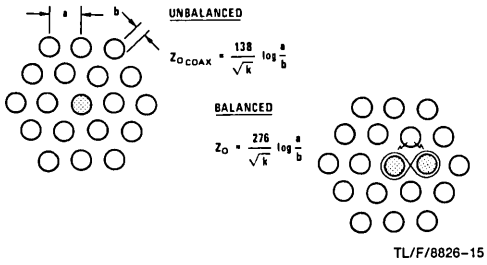

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FIGURE 15. Z_O Unbalanced < Z_O Balanced

The impedance measurement of an unbalance and balance line must be made differently. The balanced impedance must be measured with a balanced signal. If there is any unbalance in the signal on the balanced line, there will be an unbalance reflection at the terminator. Therefore, the lines should also be terminated for unbalanced signals. *Figure 16* shows the perfect termination configuration of a balanced transmission line. This termination method is primarily required for accurate impedance measurements.

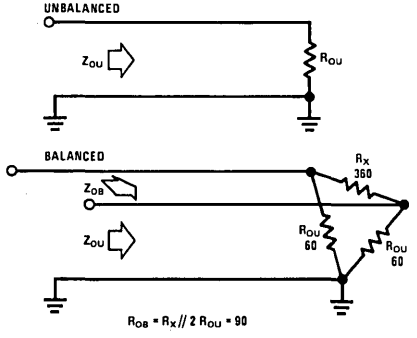

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FIGURE 16. Impedance Measurement

MEASURED PERFORMANCE

The unbalanced method circuit used in this application note up to this point is the unbalanced circuit shown in *Figure 1*. The termination of its transmission line was greater than the characteristic impedance of the unbalanced line and the circuit had considerable threshold offset. The measured performance of the unbalanced circuit wasn't comparable to the balanced method. Therefore, for the following comparison of unbalanced and balanced circuits, an improved termination shown in *Figure 17* will be used. This circuit terminates the line in 60Ω and minimized the receiver threshold offset.

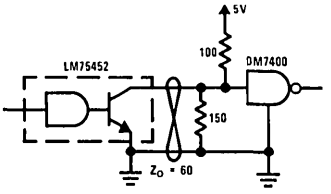

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FIGURE 17. Improved Unbalanced Method

A plot of the Absolute Maximum Data Rate versus cable type is shown in *Figure 18*. The graph shows the different performances of the DM7820A line receiver and the DM7830 line driver circuits with a worse case 1/8 Duty Cycle in no. 22 AWG stranded wire cables. In a single twisted pair cable there is less reactance than in a cable having nine twisted pairs and in turn this cable has less reactance than shielded pairs. The line length is reduced in proportion to the increased line attenuation which is proportional to the line reactance. The plot shows that the reactance and attenuation has a significant effect on the cable length. Absolute Maximum Data Rate is defined as the Data Rate at which the output of the line receiver is starting to be degraded. The roll off of the performance above 20 mega baud is due to the circuit switching response limitation.

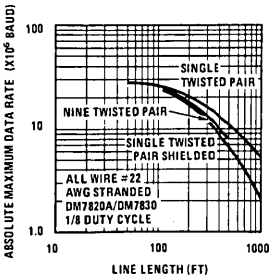

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FIGURE 18. Data Rate vs Cable Type

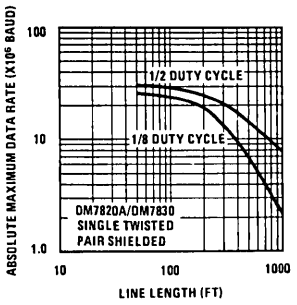

FIGURE 19. Data Rate vs Duty Cycle

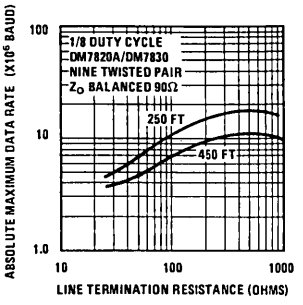

FIGURE 20. Data Rate vs Line Termination

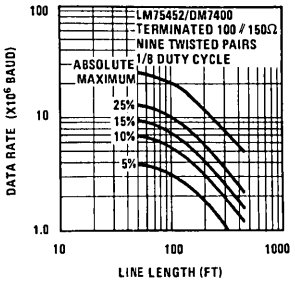

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FIGURE 21. Data Rate vs Distortion of LM75452, DM7400

Figure 19 shows the reduction in Data Rate caused by Duty Cycle. It can be observed that the Absolute Maximum Duty Rate of 1/8 Duty Cycle is less than 1/2 Duty Cycle. The following performance curves will use 1/8 Duty Cycle since it is the worst case.

Absolute Maximum Duty Rate versus the Line Termination Resistance for two different lengths of cable is shown in *Figure 20*. It can be seen from the figure that the termination doesn't have to be perfect in the case of balanced circuits. It is better to have a termination resistor to minimize the extra transient signal reflecting between the ends of the line. The reason the Data Rate increases with increased Termination Resistance is that there is less IR drop in the cable.

The graphs in *Figure 21* show the Data Rate versus the Line Length for various percentages of timing distortion using the unbalanced LM75452 and DM7400 circuits shown in *Figure 17*. The definition of Timing Distortion is the percentage difference in the pulse width of the data sent versus the data received.

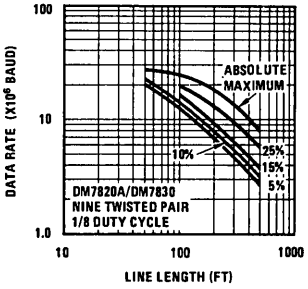

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FIGURE 22. Data Rate vs Distortion of DM7820A, DM7830

Data Rate versus the Line Length for various percentage of timing distortion using the balanced DM7820A and DM7830 circuit is shown in *Figure 22*. The distortion of this method is improved over the unbalanced method, as was previously theorized.

The Absolute Maximum Data Rate versus Line Lengths shown in the previous two figures didn't include any induced signal noise. *Figure 23* shows the test configuration of the unbalanced circuits which was used to measure near end cross talk noise. In this configuration there are eight line drivers and one receiver at one end of the cable. The performance of the receiver measured in the presence of the driver noise is shown in *Figure 24*.

Figure 24 shows the Absolute Maximum Duty Rate of the unbalanced method versus line length and versus the number of line drivers corresponding to the test configuration delineated in *Figure 23*. In the noise measurement set-up there was a ground return for each signal wire. If there is only one ground return in the cable the performance is worse. The graph shows that the effective line length is drastically reduced as additional Near End Drivers are added. When this performance is compounded by timing distortion the performance is further reduced.

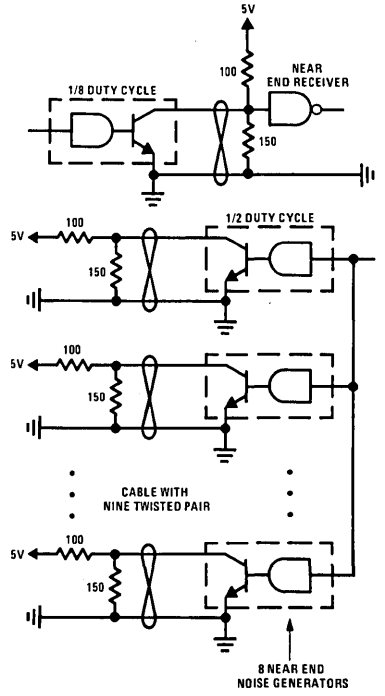

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FIGURE 23. Signal Cross Talk Experiment Using DM75452, DM7400

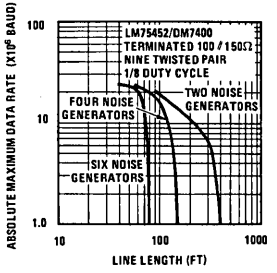

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FIGURE 24. Data Rate vs Signal Cross Talk of LM75452, DM7400

Figure 25 shows the test configuration of the balanced circuit used to generate worst case Near End cross talk noise similar to the unbalance performance shown in the previous figure. Unlike the unbalanced case, there was no measurable degradation of the circuits Data Rate or distortion.

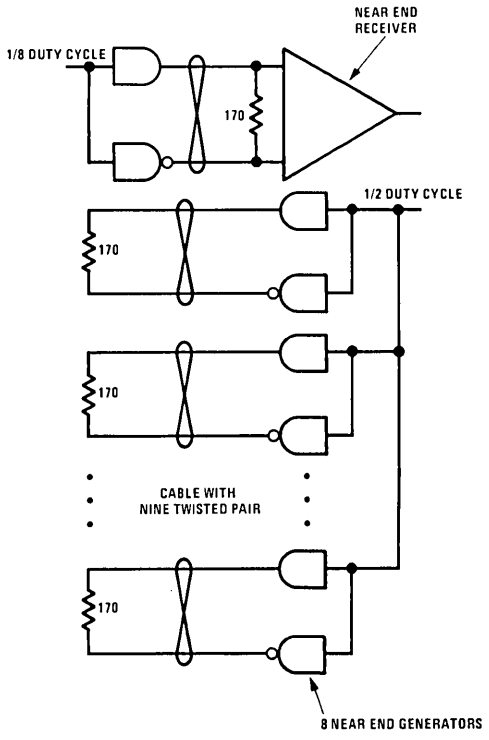

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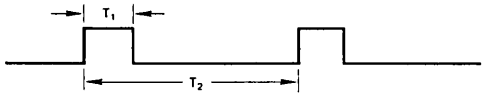
FIGURE 25. Signal Cross Talk Experiment Using DS7830, DS7820A

CONCLUSION

National has a full line of both Balanced and Unbalanced Line Drivers and Receivers. Both circuit types work well when used within their limitation. This application note shows that the balanced method is preferable for long lines in noisy electrical environments. On the other hand the unbalanced circuit works perfectly well with shorter lines and reduced data rates.

DEFINITION OF BAUD RATE



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$$\text{BIT RATE} = \frac{1}{\text{INTERVAL PER BIT}} = \frac{1}{T_2}$$

$$\text{BAUD RATE} = \frac{1}{\text{MINIMUM UNIT INTERVAL}} = \frac{1}{T_1}$$

The data in this note was plotted versus Baud Rate. The minimum unit interval reflected the worse case conditions and also normalized the diagrams so that the diagrams were independent of duty cycle. If the duty cycle is 50% then the Baud Rate is twice the Bit Rate.

REFERENCES

IC's for Digital Data Transmission, Widlar and Kubinec, *National Semiconductor Application Note AN-22.*

RADC TR73-309, Experimental Analysis of the Transmission of Digital Signals over Twisted Pair Cable, Hendrickson and Evanowski, *Digital Communication Section Communications and Navigation Division,* Rome Air Development Center, Griffis Air Force Base, New York.

Fast Pulse Techniques, Thad Dreher, E-H Research Laboratories, Inc., *The Electronic Engineer,* Aug. 1969.

Transient Analysis of Coaxial Cables, Considering Skin Effects, Wigingtom and Nahmaj, *Proceedings of the IRE,* Feb. 1957.

Relection and Crosstalk in Logic, Circuit Interconnection, John De Falco, Honeywell, Inc., *IEEE Spectrum,* July 1970.

Transmission Line Drivers and Receivers for EIA Standards RS-422 and RS-423

National Semiconductor Corp.
Application Note 214
John Abbott

With the advent of the microprocessor, logic designs have become both sophisticated and modular in concept. Frequently the modules making up the system are very closely coupled on a single printed circuit board or cardfile. In a majority of these cases a standard bus transceiver will be adequate. However because of the distributed intelligence ability of the microprocessor, it is becoming common practice for the peripheral circuits to be physically separated from the host processor with data communications being handled over cables (e.g. plant environmental control or security system). And often these cables are measured in hundreds or thousands of feet as opposed to inches on a backplane. At this point the component wavelengths of the digital signals may become shorter than the electrical length of the cable and consequently must be treated as transmission lines. Further, these signals are exposed to electrical noise sources which may require greater noise immunity than the single chassis system.

It is the object of this application note to underscore the more important design requirements for balanced and unbalanced transmission lines, and to show that National's DS1691 driver and DS78LS120 receiver meet or exceed all of those requirements.

THE REQUIREMENTS

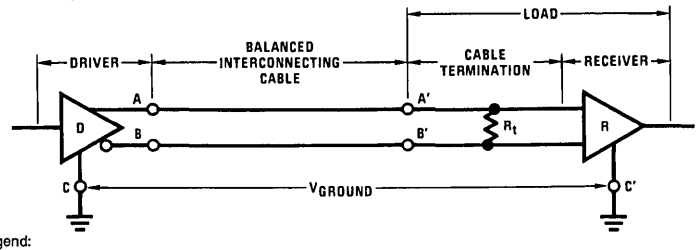
The requirements for transmission lines and noise immunity have been adequately recognized by National Semiconductor's application note AN-108 and EIA standards RS-422 (balanced) and RS-423 (unbalanced). A summary review of these notes will show that the controlling factors in a voltage digital interface are:

1) The cable length
2) The modulation rate
3) The characteristic of the interconnection cable
4) The rise time of the signal

RS-422 and RS-423 contain several useful guidelines relative to the choice of balanced circuits versus unbalanced circuits. *Figures 1a* and *1b* are the digital interface for balanced *(1a)* and unbalanced *(1b)* circuits.

Even though the unbalanced interface circuit is intended for use at lower modulation rates than the balanced circuit, its use is not recommended where the following conditions exist:

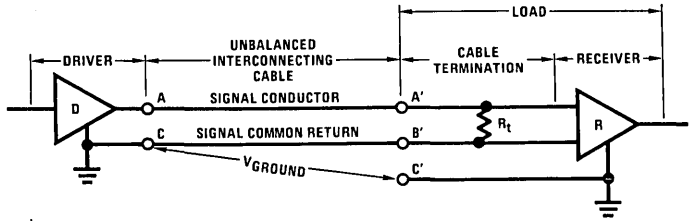
1) The interconnecting cable is exposed to noise sources which may cause a voltage sufficient to indicate a change of binary state at the load.
2) It is necessary to minimize interference with other signals, such as data versus clock.
3) The interconnecting cable is too long electrically for unbalanced operation *(Figure 2)*.



TL/F/5854–1

Legend:
R_t = Optional cable termination resistance/receiver input impedance.
V_{GROUND} = Ground potential difference
A, B = Driver interface
A', B' = Load interface
C = Driver circuit ground
C' = Load circuit ground

FIGURE 1a. RS-422 Balanced Digital Interface Circuit



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Legend:
R_t = Transmission line termination and/or receiver input impedance
V_{GROUND} = Ground potential difference
A, C = Driver interface
A', B' = Load interface
C = Driver circuit ground
C' = Load circuit ground

FIGURE 1b. RS-423 Unbalanced Digital Interface Circuit

CABLE LENGTH

While there is no maximum cable length specified, guidelines are given with respect to conservative operating distances as a function of modulation rate. *Figure 2* is a composite of the guidelines provided by RS-422 and RS-423 for data modulation versus cable length. The data is for 24 AWG twisted pair cable terminated for worst case (due to IR drop) in a 100Ω load, with rise and fall times equal to or less than one half unit interval at the applied modulation rate.

The maximum cable length between driver and load is a function of the baud rate. But it is influenced by:

1) A maximum common noise range of ±7 volts

   A) The amount of common-mode noise

      Difference of driver and receiver ground potential plus driver offset voltage and coupled peak random noise.

   B) Ground potential differences between driver and load.

   C) Cable balance

      Differential noise caused by imbalance between the signal conductor and the common return (ground)

2) Cable termination

   At rates above 200 kilobaud or where the rise time is 4 times the one way propagation delay time of the cable (RS-422 Sec 7.1.2)

3) Tolerable signal distortion

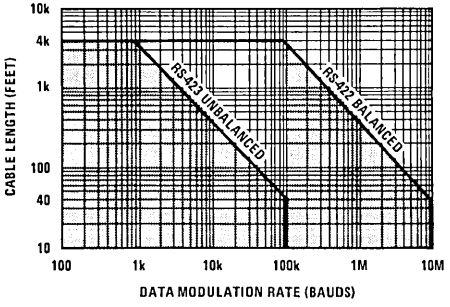

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FIGURE 2. Data Modulation Rate vs Cable Length

MODULATION RATE

Section 3 of RS-422 and RS-423 states that the unbalanced voltage interface will normally be utilized on data, timing or control circuits where the modulation rate on these circuits is below 100 kilobauds, and balanced voltage digital interface on circuits up to 10 megabauds. The voltage digital interface devices meeting the electrical characteristics of this standard need not meet the entire modulation range specified. They may be designed to operate over narrower ranges to more economically satisfy specific applications, particularly at the lower modulation rates.

As pointed out in AN-108, the duty cycle of the transmitted signal contributes to the distortion. The effect is the result of rise time. Due to delay and attenuation caused by the cable, it is possible due to AC averaging of the signal, to be unable to reach one binary level before it is changed to another. If the duty cycle is ½ (50%) and the receiver threshold is midway between logic levels, the distortion is small. However if the duty cycle were ⅛ (12.5%) the signal would be considerably distorted.

CHARACTERISTICS

Driver Unbalanced (RS-423)

The unbalanced driver characteristics as specified by RS-423 Sec 4.1 are as follows:

1) A driver circuit should be a low impedance (50Ω or less) unbalanced voltage source that will produce a voltage applied to the interconnecting cable in the range of 4V to 6V.

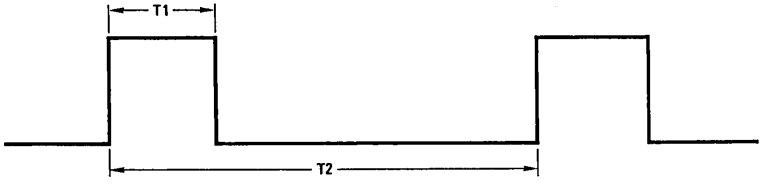
2) With a test load of 450Ω connected between the driver output terminal and the driver circuit ground, the magnitude of the voltage (VT) measured between the driver output and the driver circuit ground shall not be less than 90% of the magnitude for either binary state.

3) During transitions of the driver output between alternating binary states, the signal measured across a 450Ω test load connected between the driver output and circuit ground should be such that the voltage monotonically changes between 0.1 and 0.9 of V_{SS}. Thereafter, the signal shall not vary more than 10% of V_{SS} from the steady state value, until the next binary transition occurs, and at no time shall the instantaneous magnitude of VT and $\overline{VT}$ exceed 6V, nor be less than 4V. V_{SS} is defined as the voltage difference between the 2 steady state values of the driver output.

Driver Balanced (RS-422)

The balanced driver characteristics as specified by RS-422 Sec 4.1 are as follows:

1) A driver circuit should result in a low impedance (100Ω or less) balanced voltage source that will produce a differential voltage applied to the interconnecting cable in the range of 2V to 6V.



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$$\text{Bit Rate} = \frac{1}{\text{Interval Per Bit}} = \frac{1}{T2}$$

$$\text{Baud Rate} = \frac{1}{\text{Minimum Unit Interval}} = \frac{1}{T1}$$

FIGURE 3a. Definition of Baud Rate

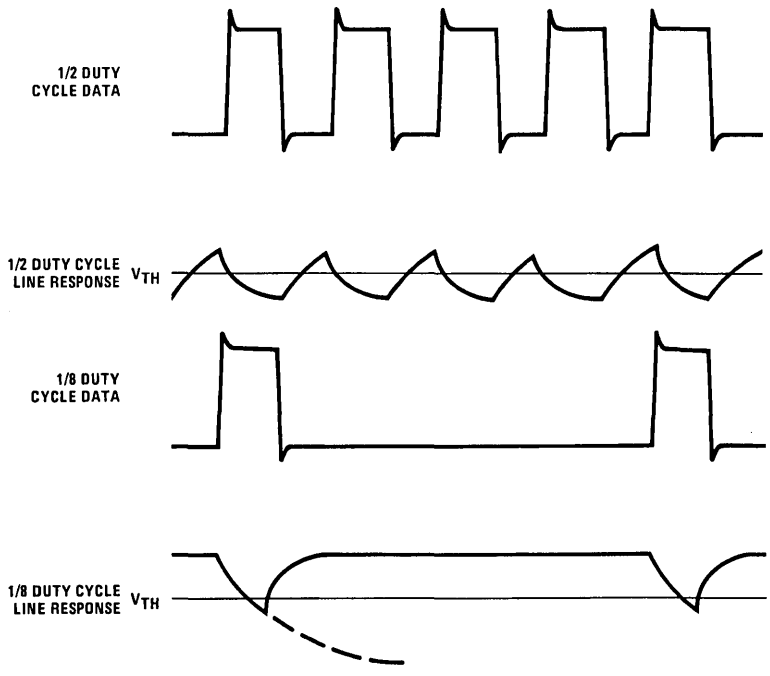


FIGURE 3b. Signal Distortion Due to Duty Cycle

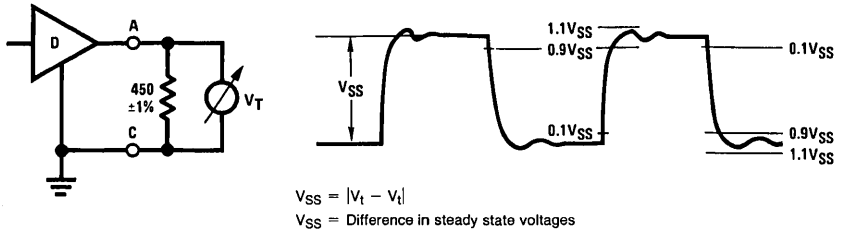


FIGURE 4. Unbalanced Driver Output Signal Waveform

2) With a test load of 2 resistors, 50Ω each, connected in series between the driver output terminals, the magnitude of the differential voltage (VT) measured between the 2 output terminals shall not be less than either 2.0V or 50% of the magnitude of V_O, whichever is greater. For the opposite binary state the polarity of VT shall be reversed ($\overline{VT}$). The magnitude of the difference in the magnitude of VT and $\overline{VT}$ shall be less than 0.4V. The magnitude of the driver offset voltage (V_{OS}) measured between the center point of the test load and driver circuit ground shall not be greater than 3.0V. The magnitude of the difference in the magnitude of V_{OS} for one binary state and $\overline{V_{OS}}$ for the opposing binary state shall be less than 0.4V.

3) During transitions of the driver output between alternating binary states, the differential signal measured across a 100Ω test load connected between the driver output terminals shall be such that the voltage monotonically changes between 0.1 and 0.9 of V_{SS} within 0.1 of the unit interval or 20 ns, whichever is greater. Thereafter the signal voltage shall not vary more than 10% of V_{SS} from the steady state value, until the next binary transition occurs, and at no time shall the instantaneous magnitude of VT or $\overline{VT}$ exceed 6V, nor less than 2V.

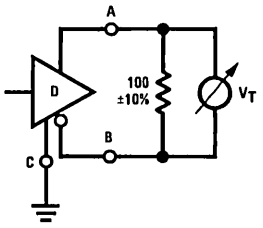
Interconnecting Cable

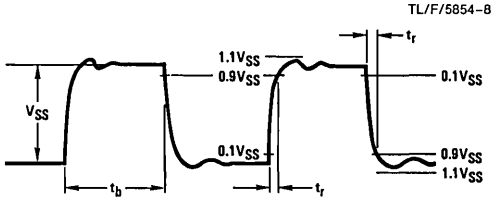
The characteristics of the interconnecting cable should result in a transmission line with a characteristic impedance in the general range of 100Ω to frequencies greater than 100 kHz, and a DC series loop resistance not exceeding 240Ω. The cable may be composed of twisted or untwisted pair (flat cable) possessing the characteristics specified in RS-422 Sec 4.3 as follows:

1) Conductor size of the 2 wires shall be 24 AWG or larger with wire resistance not to exceed 30Ω per 1000 feet per conductor.

2) Mutual pair capacitance between 1 wire in the pair to the other shall not exceed 20 pF per foot.

3) Stray capacitance between 1 wire in the pair with all other wires connected to ground, shall not exceed 40 pF per foot.





t_b = Time duration of the unit interval at the applicable modulation rate.

$t_r \leq 0.1\ t_b$ when $t_b \geq 200$ ns

$t_r \leq 20$ ns when $t_b < 200$ ns

V_{SS} = Difference in steady state voltages

$V_{SS} = |V_t - \overline{V_t}|$

FIGURE 5. Balanced Driver Output Signal Waveform

Receiver

The load characteristics are identical for both balanced (RS-422) and unbalanced (RS-423) circuits. Each consists of a receiver and optional termination resistance as shown in *Figure 1*. The electrical characteristics single receiver without termination or optional fail-safe provisions are specified in RS-422/423 Sec 4.2 as follows:

1) Over an entire common-mode voltage range of −7V to +7V, the receiver shall not require a differential input voltage of more than 200 mV to correctly assume the intended binary state. The common-mode voltage (V_{CM}) is defined as the algebraic mean of the 2 voltages appearing at the receiver input terminals with respect to the receiver circuit ground. Reversing the polarity of VT shall cause the receiver to assume the opposite binary state. This allows for operations where there are ground differences caused by IR drop and noise of up to ±7V.
2) To maintain correct operation for differential input signal voltages ranging between 200 mV and 6V in magnitude.
3) The maximum voltage present between either receiver input terminal and receiver circuit ground shall not exceed 10V (3V signal plus 7V common-mode) in magnitude nor cause the receiver to operationally fail. Additionally, the receiver shall tolerate a maximum differential signal of 12V applied across its input terminals without being damaged.
4) The total load including up to 10 receivers shall not have a resistance greater than 90Ω for balanced, and 400Ω for unbalanced at its input points and shall not require a differential input voltage of greater than 200 mV for all receivers to assume the correct binary state.
5) Fail-safe operation per RS-423 Sec 4.2.5 states that other standards and specifications using the electrical characteristics of the unbalanced interface circuit may require that specific interchange leads be made fail-safe to certain fault conditions. Where fail-safe operation is required by such referencing standards and specifications, a provisions shall be incorporated in the load to provide a steady binary condition (either "1" or "0") to protect against certain fault conditions (open or shorted cable).

The designer should be aware that in circuits employing pull-up resistors, the resistors used become part of the termination.

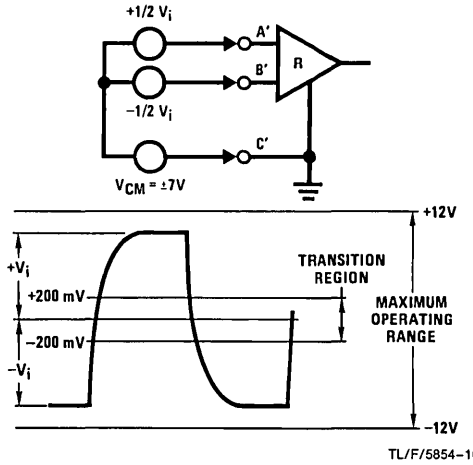


FIGURE 6. Receiver Input Sensitivity Measurement

Note: Designers of terminating hardware should be aware that slow signal transitions with superimposed noise present may give rise to instability or oscillations in the receiving device, and therefore appropriate techniques should be implemented to prevent such behavior. For example, adequate hysteresis and response control may be incorporated into the receiver to prevent such conditions.

SIGNAL RISE TIME

The signal rise time is a high frequency component which causes interference (near end cross-talk) to be coupled to adjacent channels in the interconnecting cable. The near-end crosstalk is a function of both rise time and cable length, and in considering wave shaping, both should be considered. Since in the balanced voltage digital interface the output is complementary, there is practically no cross-talk coupled and therefore wave shaping is limited to unbalanced circuits.

Per RS-423 Sec 4.1.6, the rise time of the signal should be controlled so that the signal has reached 90% of V_{SS} between 10% and 30% of the unit interval at the maximum modulation rate. Below 1 kilobaud the time to reach 90% V_{SS} shall be between 100 μs and 300 μs. If a driver is to operate over a range of modulation rates and employ a fixed amount of wave shaping which meets the specification for the maximum modulation rate of the operating range, the wave shaping is considered adequate for all lesser modulation rates.

However a major cause of distortion is the effect the transmission line has on the rise time of the transmitted signal. *Figure 7* shows the effect of line attenuation and delay to a voltage step as it progresses down the cable. The increase of the rise time with distance will have a considerable effect on the distortion at the receiver. Therefore in fixing the amount of wave shaping employed, caution should be taken not to use more than the minimum required.

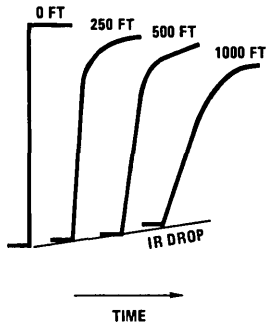


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FIGURE 7. Signal Rise Time on Transmission Line vs Line Length

DS1691A, DS78LS120

The Driver

The DS1691A/DS3691 are low power Schottky TTL line drivers designed to meet the above listed requirements of EIA standard RS-422 and RS-423. They feature 4 buffered outputs with high source and sink current capability with internal short circuit protection. The DS1691/DS3691 employ a mode selection pin which allows the circuit to become either a pair of balanced drivers *(Figure 8)* or 4 independent unbalanced drivers *(Figure 9)*. When configured for unbalanced operation *(Figure 10)* a rise time control pin allows the use of an external capacitor to control rise time for suppression of near end cross-talk to adjacent channels in the interconnect cable. *Figure 11* is the typical rise time vs external capacitor used for wave shaping.

The DS3691 configured for RS-422 is connected V_{CC} = 5V V_{EE} = 0V, and configured for RS-423 connected V_{CC} = 5V V_{EE} = −5V. For applications outside RS-422 conditions and for greater cable lengths the DS1691/DS3691 may be connected with a V_{CC} of 5 volts and V_{EE} of −5 volts. This will create an output which is symmetrical about ground, similar to Mil Standard 188-114.

When configured as balanced drivers *(Figure 8)*, each of the drivers is equipped with an independent TRI-STATE® control pin. By use of this pin it is possible to force the driver into its high impedance mode for applications using party line techniques.

If the common-mode voltage, between driver 1 and all other drivers in the circuit, is small then several line drivers (and receivers) may be incorporated into the system. However, if the common-mode voltage exceeds the TRI-STATE common-mode range of any driver, then the signal will become attenuated by that driver to the extent the common-mode voltage exceeds its common-mode range (see *Figure 12*, top waveform).

It is important then to select a driver with a common-mode range equal to or larger than the common-mode voltage requirement of the system. In the case of RS-422 and RS-423 the minimum common-mode range would be ±7V. The DS1692/DS3692 driver is tested to a common-mode range of ±10V and will operate within the requirements of such a system (see *Figure 12*, bottom waveform).

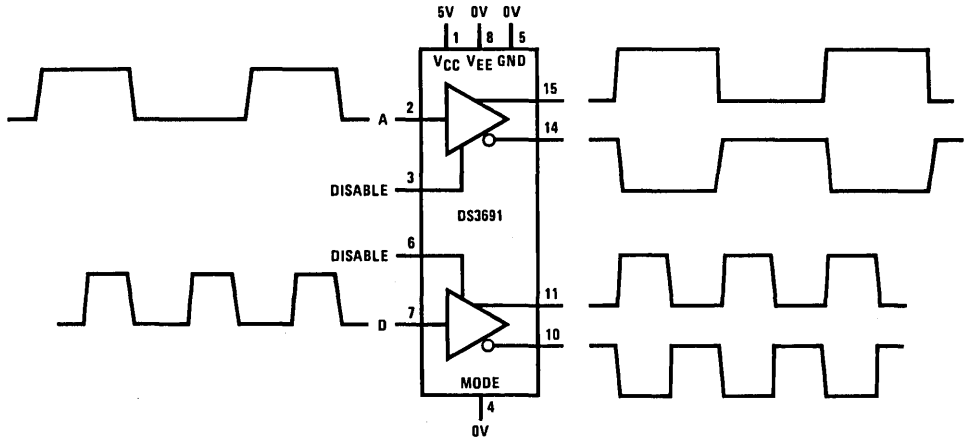

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FIGURE 8. DS3691 Connected for Balanced Mode Operation

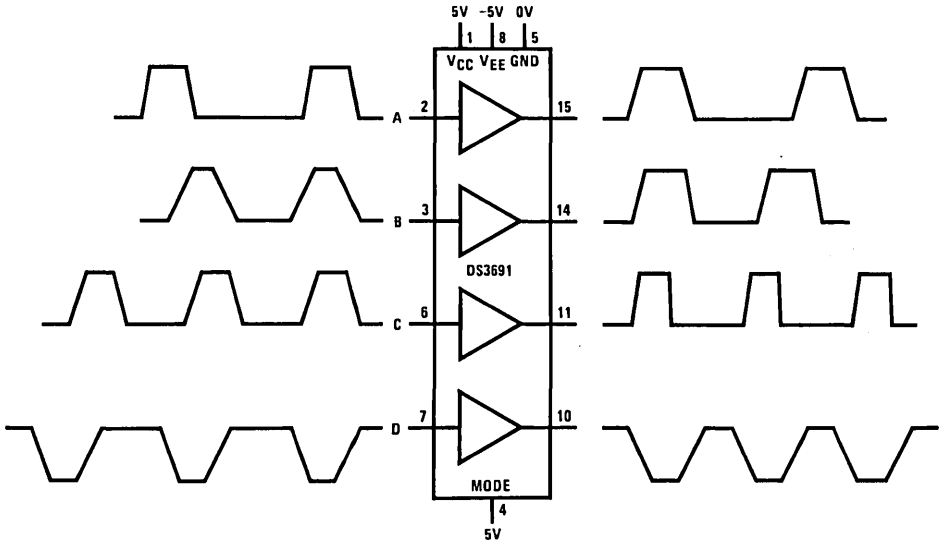

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FIGURE 9. DS3691 Connected for Unbalanced Mode Operation

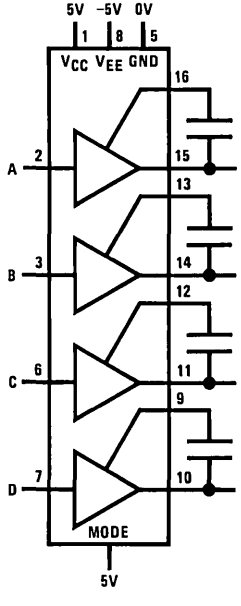

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FIGURE 10. Using an External Capacitor to Control Rise Time of DS3691

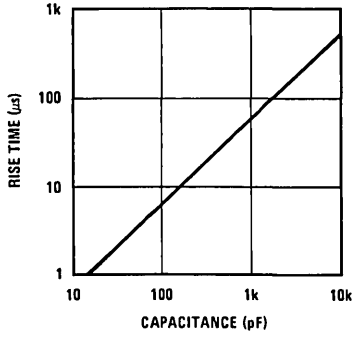

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FIGURE 11. DS3691 Rise Time vs External Capacitor

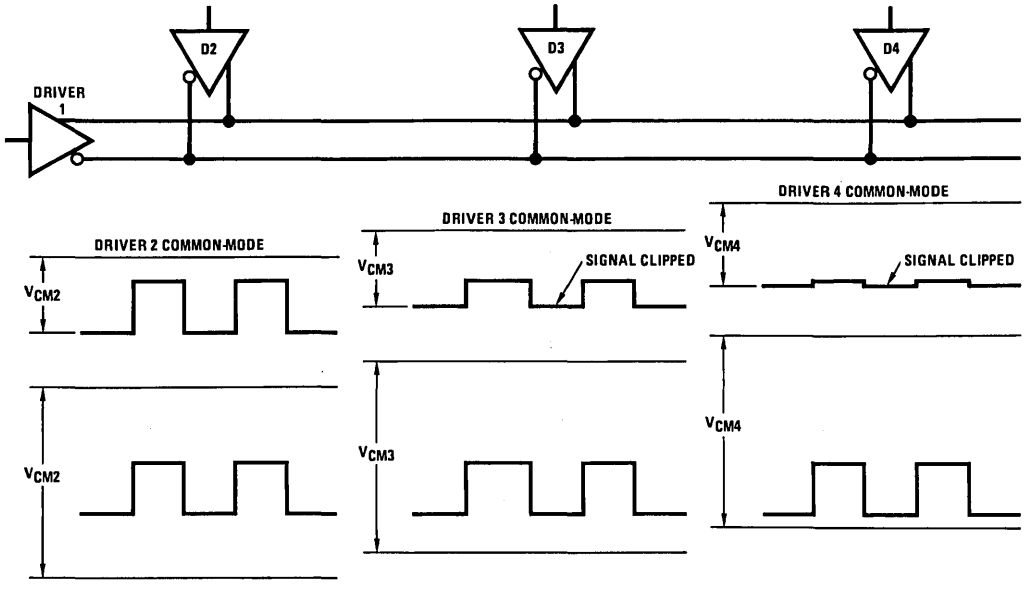

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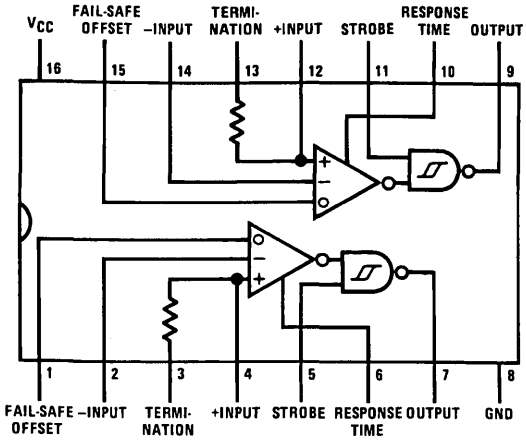
FIGURE 12. Comparison of Drivers without TRI-STATE Common-Mode Output Range (top waveforms) to DS3691 (bottom waveforms)



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Top View

FIGURE 13. DS78LS120/DS88LS120 Dual Differential Line Receiver

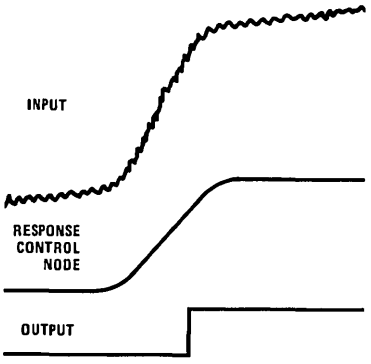
DS78LS120/DS88LS120

The Receiver

The DS78LS120/DS88LS120 are high peformance, dual differential TTL compatible line receivers which meet or exceed the above listed requirements for both balanced and unbalanced voltage digital interface.

The line receiver will discriminate a ±200 millivolt input signal over a full common-mode range of ±10 volts and a ±300 millivolt signal over a full common-mode range of ±15 volts.

The DS78LS120/DS88LS120 include response control for applications where controlled rise and fall times and/or high frequency noise rejection are desirable. Switching noise which may occur on the input signal can be eliminated by the 50 mV (referred to input) of hysteresis built into the output gate *(Figure 14)*. The DS78LS120/DS88LS120 makes use of a response control pin for the addition of an external capacitor, which will not affect the line termination impedance of the interconnect cable. Noise pulse width rejection versus the value of the response control capacitor is shown in *Figure 15*. The combination of the filter followed by hysteresis will optimize performance in a worst case noise environment. The DS78C120/DS88C120 is identical in performance to the DS78LS120/DS88LS120, except it's compatible with CMOS logic gates.



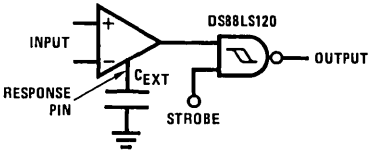


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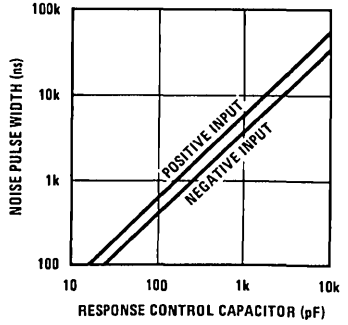
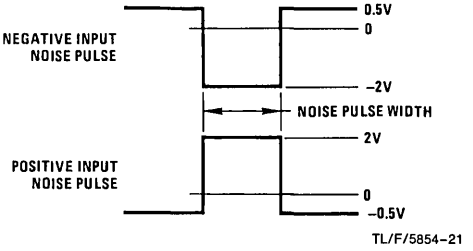
FIGURE 14. Application of DS88LS120 Receiver Response Control and Hysteresis





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TL/F/5854–20

FIGURE 15. Noise Pulse Width vs Response Control Capacitor

FAIL-SAFE OPERATION

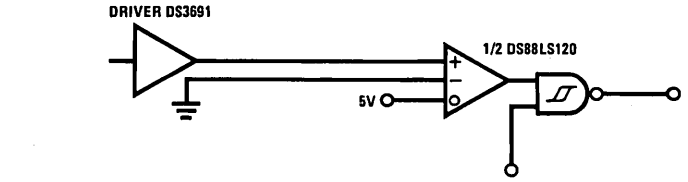
Communication systems require elements of a system to detect the loss of signals in the transmission lines. And it is desirable to have the system shut-down in a fail-safe mode if the transmission line is open or short. To facilitate the detection of input opens or shorts, the DS78LS120/ DS88LS120 incorporates an input threshold voltage offset. This feature will force the line receiver to a specific logic state if presence of either fault condition exists.

The receiver input threshold is ±200 mV and an input signal greater than ±200 mV insures the receiver will be in a specific logic state. When the offset control input is connected to a V_{CC} = 5V, the input thresholds are offset from 200 mV to 700 mV, referred to the non-inverting input, or −200 mV to −700 mV, referred to the inverting input. Therefore, if the input is open or short, the input will remain in a specific state (see *Figure 16*).

It is recommended that the receiver be terminated in 500Ω or less to insure it will detect an open circuit in the presence of noise.

For unbalanced operation, the receiver would be in an indeterminate logic state if the offset control input was open. Connecting the offset to +5V, offsets the receiver threshold 0.45V. The output is forced to a logic zero state if the input is open or short.

For balanced operation with inputs short or open, receiver C will be in an indeterminate logic state. Receivers A and B will be in a logic zero state allowing the NOR gate to detect the short or open fault condition. The "strobe" input will disable the A and B receivers and therefore may be used to "sample" the fail-safe detector (see *Figure 17*).



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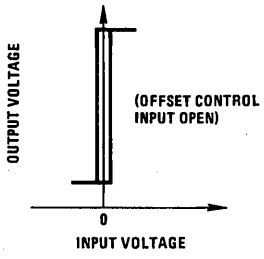

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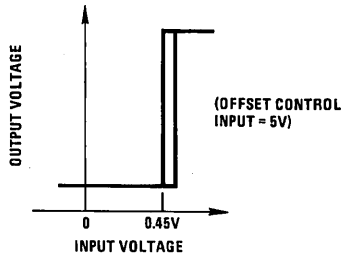

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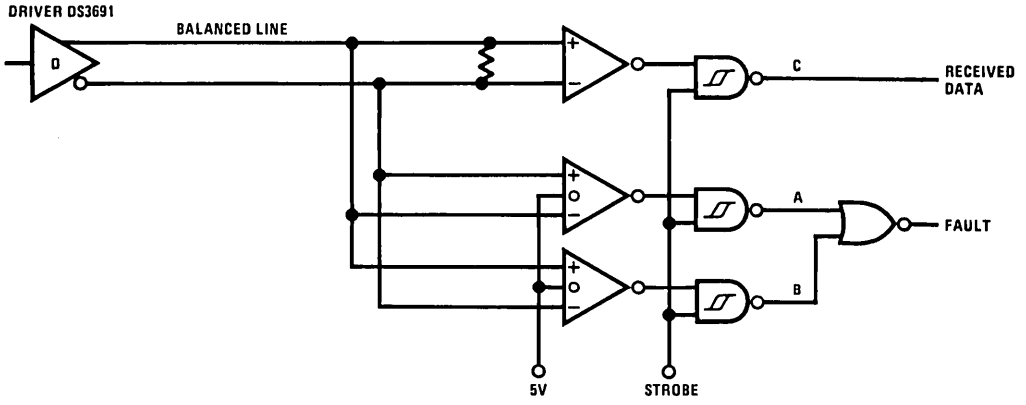
FIGURE 16. Fail-Safe Using the DS88LS120 Threshold Offset for Unbalanced Lines



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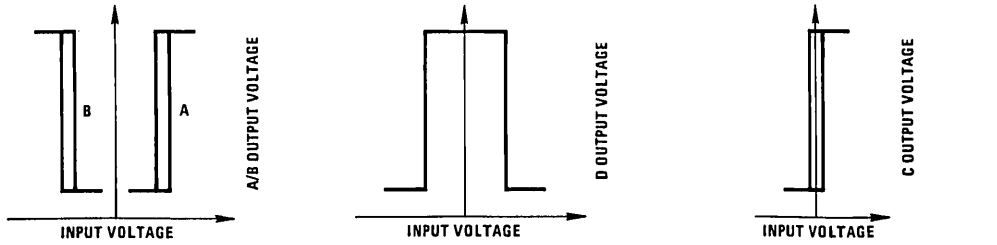

TL/F/5854-26 TL/F/5854-27 TL/F/5854-28

FIGURE 17. Fail-Safe Using the DS88LS120 Threshold Offset for Balanced Lines

Summary of Electrical Characteristics of Some Well Known Digital Interface Standards

National Semiconductor Corp.
Application Note 216
Don Tarver

FOREWORD

Not the least of the problems associated with the design or use of data processing equipment is the problem of providing for or, actually interconnecting the differing types and models of equipment to form specific processing systems.

The magnitude of the problem becomes apparent when one realizes that every aspect of the electrical, mechanical and architectural format must be specified. The most common of the basic decisions confronting the engineer include:

- Type of logic (negative or positive)
- Threshold levels
- Noise immunity
- Form of transmission
  - Balanced/unbalanced, terminated/unterminated
  - Unidirectional/bidirectional, simplex/multiplexed
- Type of transmission line
- Connector type and pin out
- Bit or byte oriented
- Baud rate

If each make and/or model of equipment presented a unique interface at its I/O ports, "interface" engineering would become a major expenditure associated with the use of data processing equipment.

Fortunately, this is not the case as various interested or cognizant groups have analyzed specific recurring interface areas and recommended "official" standards around which common I/O ports could be structured. Also, the I/O specifications of some equipment with widespread popularity such as the IBM 360/370 computer and DEC minicomputer have become "defacto" standards because of the desire to provide/use equipment which interconnect to them.

Compliance with either the "official" or "defacto" standards on the part of equipment manufacturers is voluntary. However, it is obvious that much can be gained and little lost by providing equipment that offers either the "official" or "defacto" standard I/O ports.

As can be imagined, the entire subject of interface in data processing systems is complicated and confusing, particularly to those not intimately involved in the day-to-day aspects of interface engineering or management. However, at the component level the questions simplify to knowing what standards apply and what circuits or components are available to meet the standards.

This application note summarizes the important electrical characteristics of the most commonly accepted interface standards and offers recommendations on how to use National Semiconductor integrated circuits to meet those standards.

1.0 INTRODUCTION

The interface standards covered in this application note are listed in Table I. The body of the text expands upon the scope and application of each listed standard and summarizes important electrical parameters.

Table II summarizes the National Semiconductor IC's applicable to each standard.

TABLE I. Common Line Driver/Receiver Interface Standards Summary

Interface Area	Application	Standard	Origin	Comments
Data Communications Equipment (DCE*) to Data Terminal Equipment (DTE)	U.S.A. Industrial	RS-232C	EIA	Unbalanced, Short Lines
		RS-422	EIA	Balanced, Long Lines
		RS-423	EIA	Unbalanced, RS-232 Up-Grade
		RS-449	EIA	System Standard Covering Use of RS-422, RS-423
		RS-485	EIA	Balanced, Long Line Multipoint
	International	CCITT Vol. VIII V. 24	International Telephone and Telegraph Consultative Committee	Similar to RS-232
		CCITT No. 97 X. 26		Similar to RS-423
		CCITT No. 97 X. 27		Similar to RS-422
	U.S.A. Military	MIL-STD-188C	D.O.D.	Unbalanced, Short Lines
		MIL-STD-188-114	D.O.D.	Similar to RS-422, RS-423
		MIL-STD-1397 (NTDS–Slow)	Navy	42k bits/sec.
		MIL-STD-1397 (NTDS–Fast)	Navy	250k bits/sec
	U.S. Government, Non-Military	FED-STD-1020	GSA	Identical to RS-423
		FED-STD-1030	GSA	Identical to RS-422

TABLE I. Common Line Driver/Receiver Interface Standards Summary (Continued)

Interface Area	Application	Standard	Origin	Comments
Computer to Peripheral	IBM 360/370	System 360/370 Channel I/O	IBM	Unbalanced Bus
	DEC Mini-Computer	DEC Unibus®	DEC	Unbalanced Bus
Instrument to Computer	Nuclear Instrumentation	CAMAC (IEEE Std. 583-1975)	NIM (AEC)	DTL/TTL Logic Levels
	Laboratory Instrumentation	488	IEEE	Unbalanced Bus
Microprocessor to Interface Devices	Microprocessor Circuits	Microbus™	National Semiconductor	Short Line; 8-Bit Parallel, Digital Transmission
Facsimile Equipment to DTE	Facsimile Transmission	RS-357	EIA	Incorporates RS-232
Automatic Calling Equipment to DTE	Impulse Dialing and Multi-Tone Keying	RS-366	EIA	Incorporates RS-232
Numerically Controlled Equipment to DTE	Numerically Controlled Equipment	RS-408	EIA	Short Lines (<4 Ft.)

* Changed to "Data Circuit-Terminating Equipment"

TABLE II. Line Driver/Receiver Integrated Circuit Selection Guide for Digital Interface Standards

Standard Designation	Part Number			
	Line Driver		Line Receiver	
	0°C to +70°C	−55°C to +125°C	0° to +70°C	−55°C to +125°C
U.S. INDUSTRIAL STANDARDS				
RS-232C	DS1488 DS75150	Not Applicable Not Applicable	DS1489 (A) DS75154	Not Applicable Not Applicable
RS-357	See RS-232C			
RS-366	See RS-232C			
RS-408	DS75453 DS75454	DS55454 DS55454	DS7820A DS75115	DS7820A DS55115
RS-422	DS3691 DS26LS31C DS3487	DS1691A DS26LS31M DS3587	DS88LS120 DS26LS32C DS3486 DS26LS33C DS88C20 DS88C120	DS78LS120 DS26LS32M DS26LS33M DS78C20 DS78C120
RS-423	DS3691 DS3692	DS1691A DS1692	DS88LS120 DS88C20 DS88C120	DS78LS120 DS78C20 DS78C120
RS-449	See RS-422, RS-423			
RS-485 Transceivers	DS3695 DS3696 DS3697 DS3698 DS75176A		DS3695 DS3696 DS3697 DS3698 DS75176A	
IEEE 488	DS3666 DS75160A DS75161A DS75162A		DS3666 DS75160A DS75161A DS75162A	
CAMAC	See RS-232C, RS-422, RS-423 or IEEE 488			
IBM 360/370 I/O Port	DS75123	Not Applicable	DS75124	Not Applicable

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TABLE II. Line Driver/Receiver Integrated Circuit Selection Guide for Digital Interface Standards (Continued)

Standard Designation	Part Number			
	Line Driver		Line Receiver	
	0°C to +70°C	−55°C to +125°C	0° to +70°C	−55°C to +125°C
DEC Unibus®	DS36147 DS8641 Transceiver	DS16147 DS7641 Transceiver	DS8640 DS8641 Transceiver	DS7640 DS7641 Transceiver
Microbus™	DS3628 DP8228 DP8216 DP8212 DP8340B Transceiver	DS1628 DP8228M DP8216M DP8212M	DP8304B Transceiver	
GOVERNMENT STANDARDS				
MIL-STD-188C	DS3692	DS1692	DS88LS120	DS78LS120
MIL-STD-188-114	DS3692	DS1692	DS88LS120	DS78LS120
FED-STD-1020	See RS-423			
FED-STD-1030	See RS-422			
MIL-STD-1397 (NTDS-Slow)	Use Discrete Components and/or Comparators			
MIL-STD-1397 (NTDS-Fast)	Use Discrete Components and/or Comparators			
INTERNATIONAL STANDARDS (CCITT)				
1969 White Book Vol. VIII, V. 24	See RS-232C			
Circular No. 97, X. 26	See RS-422			
Circular No. 97, X. 27	See RS-423			

2.0 (DTE) (DCE)

Data terminal equipment (DTE) to data communications equipment (DCE) interface standards

2.1 Application

The DTE/DCE standards cover the electrical, mechanical and functional interface between or among terminals (i.e., teletypewriters, CRT's etc.) and communications equipment (i.e., modems, cryptographics sets, etc.).

2.2 U.S. Industrial DTE/DCE Standards

2.2.1 EIA RS-232

RS-232C is the oldest and most widely known DTE/DCE interface standard. Viewed by many as a complete standard, it provides for one-way/non-reversible, single ended (unbalanced) non terminated line, serial digital data transmission. *Figure 1* shown below illustrates a typical application. See Table III for Specification Summary.

Important features are:

* Positive logic (±5V min to ±15V max)
* Fault protection
* Slew-rate control
* 50 feet recommended cable length
* 20k bits per second data rate

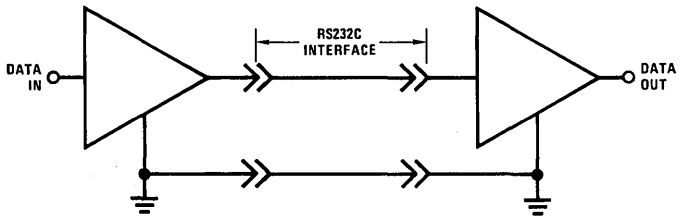

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FIGURE 1. EIA RS-232C Application

2.2.2 EIA RS-422, RS-423 and RS-485

In a move to upgrade system capabilities by using state-of-the-art devices and technology the EIA in 1975, introduced two new specifications covering RS-422 balanced and RS-423 unbalanced data transmission. Both of these standards offered major advantages over the popular RS-232C interface. Understanding the advantages of the balanced interface RS-422, the EIA introduced in 1983 the RS-485 Multipoint Systems standard that eliminates several limitations of RS-422.

2.2.2.1 RS-423

RS-423 closely resembles RS-232C in that it, too specifies a one-way/non-reversible, data transmission. Several key advantages of the standard include a 100k Baud data rate at 30 feet and a balanced receiver offering an input voltage common mode (VCM) of ±7V. As shown in *Figure 2* the receiver input is referenced to the driver ground permitting ground differences between the driver and receiver. See Table IV for Specification Summary.

Important features are:

* Positive logic (±4V min to ±6V max)
* Fault protected driver outputs
* Controlled Slew-rate reduces crosstalk and reflections
* 30 feet maximum cable length at 100k Baud
* Differential receiver with ±7V VCM and ±200 mV sensitivity

2.2.2.2 RS-422

RS-422 provides for balanced data tranmission with unidirectional/non-reversible, terminated or non-terminated transmission lines. Several key advantages offered by this standard include the differential receiver defined in RS-423, a differential driver and data rates as high as 10M Baud at 40 feet. *Figure 3* shows a typical interconnect application. See Table V for Specification Summary.

2.2.2.3 RS-485

RS-485 standards accommodates the requirements on a balanced transmission line used in party-line circuit configurations. This standard is similar to RS-422 and is considered to be an extension permitting multipoint applications where multiple drivers and receivers share the same line in data transmission.

Several key characteristics of the standard that differentiate it from RS-422 are; the expanded common mode range of both the driver and receiver, (VCM range +12 to −7V), and characteristics that permit 32 drivers and receivers on the line. *Figure 4* shows a typical party-line application. Note that the transmission line which is intended to be 120Ω twisted pair is terminated at both ends. See Table VI for Specifications Summary.

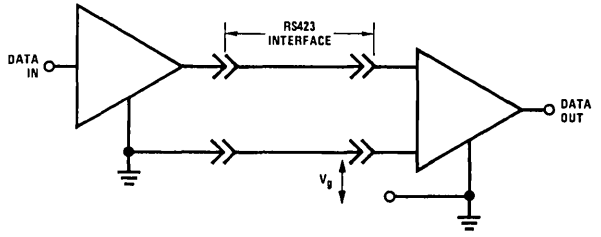

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FIGURE 2. EIA RS-423 Application

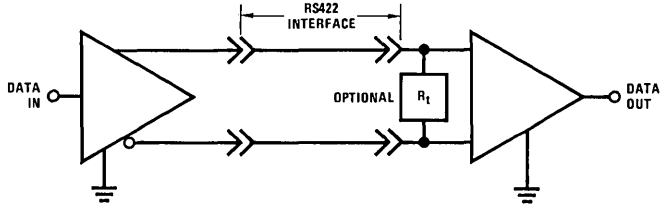

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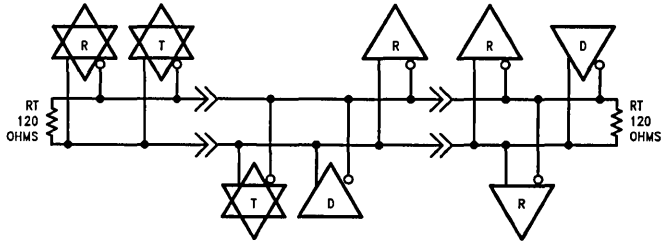
FIGURE 3. EIA RS-222 Application

Note: The termination resistor is defined as optional by RS-422. However this termination resistor is highly recommended to reduce the possibility of line reflections caused by mis-matched impedance between the cable and the driver.



D—Driver
R—Receiver
T—Transceiver

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FIGURE 4. A Typical RS-485 Party-Line Configuration

TABLE III. EIA RS-232C Specification Summary

Symbol	Parameter	Conditions	EIA RS-232C			Units
			Min	Typ	Max	
V_{OH}	Driver Output Voltage Open				25	V
V_{OL}	Circuit		−25			V
V_{OH}	Driver Output Voltage Loaded	3 kΩ ≤ R_L ≤ 7 kΩ	5		15	V
V_{OL}	Output		−15		−5	V
R_O	Driver Output Resistance Power Off	−2V ≤ V_O ≤ 2V			300	Ω
I_{OS}	Driver Output Short-Circuit Current		−500		500	mA
	Driver Output Slew Rate					
	All Interchange Circuits				30	V/μs
	Control Circuits		6			V/ms
	Rate and Timing Circuits		6			V/ms
		% of Unit Interval	4			%
R_{IN}	Receiver Input Resistance	3V ≤ V_{IN} ≤ 25V	3000		7000	Ω
	Receiver Open Circuit Input Bias Voltage		−2		2	V
	Receiver Input Threshold					
	Output = MARK		−3			V
	Output = SPACE				3	V

TABLE IV. EIA RS-423 Specification Summary

Symbol	Parameter	Conditions	EIA RS-423			Units
			Min	Typ	Max	
V_O	Driver Unloaded Output Voltage		4		6	V
$\overline{V_O}$			−4		−6	V
V_T	Driver Loaded Output Voltage	R_L = 450Ω	3.6			V
$\overline{V_T}$			−3.6			V
R_S	Driver Output Resistance				50	Ω
I_{OS}	Driver Output Short-Circuit Current	V_O = 0V			±150	mA
	Driver-Output Rise and Fall Time	Baud Rate ≤ 1k Baud			300	μs
		Baud Rate ≥ 1k Baud			30	% Unit Interval
I_{OX}	Driver Power OFF Current	V_O = ±6V			±100	μA
V_{TH}	Receiver Sensitivity	V_{CM} ≤ ±7V			±200	mV
V_{CM}	Receiver Common-Mode Range				±10	V
R_{IN}	Receiver Input Resistance		4000			Ω
	Receiver Common-Mode Input Offset				±3	V

TABLE V. EIA RS-422 Specification Summary

Symbol	Parameter	Conditions	EIA RS-422			Units
			Min	Typ	Max	
V_O	Driver Unloaded Output Voltage				6	V
$\overline{V_O}$					−6	V
V_T	Driver Loaded Output Voltage	R_T = 100Ω	2			V
$\overline{V_T}$			−2			V
R_S	Driver Output Resistance	Per Output			50	Ω
I_{OS}	Driver Output Short-Circuit Current	V_O = 0V			150	mA
	Driver Output Rise Time				10	% Unit Interval
I_{OX}	Driver Power OFF Current	−0.25V ≤ V_O ≤ 6V			±100	μA
V_{TH}	Receiver Sensitivity	V_{CM} = ±7V			200	mV
V_{CM}	Receiver Common-Mode Voltage		−12		12	V
	Receiver Input Offset		±3			V
R_{IN}	Receiver Input Resistance		4000			Ω

TABLE VI. EIA RS-485 Specification Summary

Symbol	Parameter	Conditions	EIA RS-485			Units
			Min	Typ	Max	
V_O $\overline{V_O}$	Driver Unloaded Output Voltage					V
V_T $\overline{V_T}$	Driver Loaded Output Voltage	$R_T = 100\Omega$ RS-422	2 −2			V V
		$R_T = 54\Omega$, CL = 50 ps RS-485	1.5 −1.5			V V
I_{OS}	Driver Output Short-Circuit Current	$V_O = \pm 12V$ $V_O = -7V$			250 −250	mA mA
V_{OS}	Driver Common Mode Output Voltage				3	V
$V_{OS}-V_{\overline{OS}}$	Difference in Common Mode Offset				0.2	V
V_{TH}	Receiver Sensitivity	$-7V \le V_{CM} \le +12V$			200	mV
V_{CM}	Receiver Common Mode Voltage		−7		+12	V
R_{IN}	Receiver Input Resistance		12k			Ω

2.3 International Standards

2.3.1 CCITT 1969 White Book Vol. VIII, V.24. This standard is identical to RS-232C.

2.3.2 CCITT circular No. 97 Com SPA/13, X. 26. This standard is similar to RS-422 with the exception that the receiver sensitivity at the specified maximum common-mode voltage (±7V) shall be ±300 mV vs ±200 mV for RS-422.

2.3.3 CCITT circular No. 97 Com SPA/13, X. 27. This standard is similar to RS-423 with 2 exceptions:

a) The receiver sensitivity is as specified in paragraph X.26, and

b) The driver output voltage is specified at a load resistance of 3.9 kΩ.

2.4 U.S. Military Standards

2.4.1 MIL-STD-188C (Low Level)

The military equivalent to RS-232C is MIL-STD-188C. Devices intended for RS-232C can be applied to MIL-STD-188C by use of external wave shaping components on the driver end and input resistance and threshold tailoring on the receiver end.

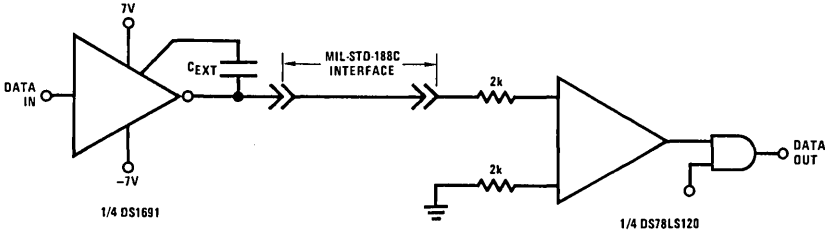

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FIGURE 5. MIL-STD-188C Application

TABLE VII. MIL-STD-188C Specification Summary

Symbol	Parameter	Conditions	MIL-STD-188C Low Level Limits			Units
			Min	Typ	Max	
V_{OL}	Driver Output Voltage Open Circuit	(Note 1)	5		7	V
V_{OL}			−7		−5	V
R_O	Driver Output Resistance Power ON	$I_{OUT} \le 10$ mA			100	Ω
I_{OS}	Driver Output Short-Circuit Current		−100		100	mA
	Driver Output Slew Rate					
	All Interchange Circuits Control Circuits Rate and Timing Circuits	(Note 2)	5		15	% IU
R_{IN}	Receiver Input Resistance	Mode Rate ≤ 200k Baud	6			Ω
	Receiver Input Threshold					
	Output = MARK	(Note 3)			100	μA
	Output = SPACE		−100			μA

Note 1: Ripple <0.5%, V_{OH}, V_{OL} matched to within 10% of each other.

Note 2: Waveshaping required on driver output such that the signal rise or fall time is 5% to 15% of the unit interval at the applicable modulation rate.

Note 3: Balance between marking and spacing (threshold) currents actually required shall be within 10% of each other.

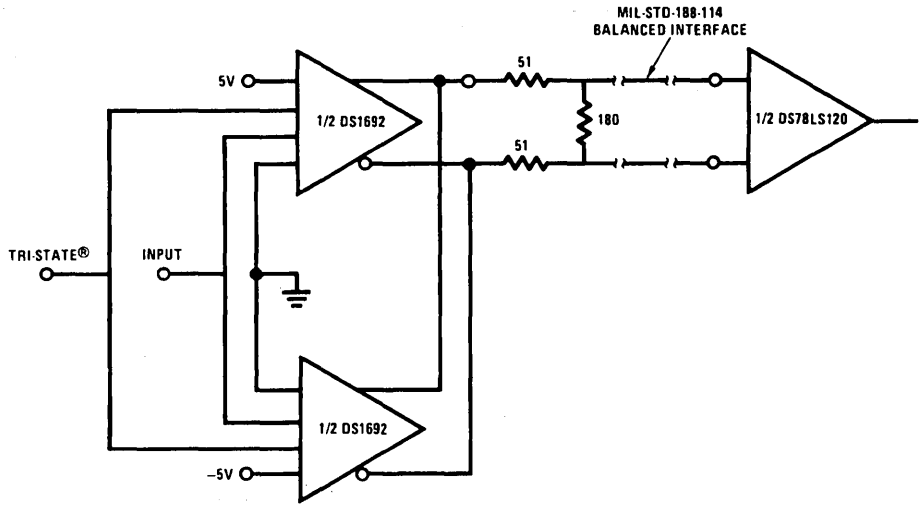

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FIGURE 6. MIL-STD-188-114 (Balanced Applications)

2.4.2 MIL-STD-188-114 Balanced

This standard is similar to RS-422 with the exception that the driver offset voltage level is limited to ±0.4V vs ±3V allowed in RS-422.

2.4.3 MIL-STD-188-114 Unbalanced.

This standard is similar to RS-423 with the exception that loaded circuit driver output voltage at R_L = 450Ω must be 90% of the open circuit output voltage vs ±2V at R_S = 100Ω for RS-422.

2.4.4 MIL-STD-1397 (Slow and Fast)

2.5 FED-STD-1020/1030

U.S. Government (non-military) standards FED-STD-1020 and 1030 are identical without exception to EIA RS-423 and RS-422, respectively.

3.0 COMPUTER TO PERIPHERAL INTERFACE STANDARDS

To date, the only standards dealing with the interface between processors and other equipment are the "defacto" standards in the form of specifications issued by IBM and DEC covering the models 360/370 I/O ports and the Unibus, respectively.

3.1 GA-22-6974-0

IBM specification GA-22-6974-0 covers the electrical characteristics, the format of information and the control sequences of the data transmitted between 360/370's and up to 10 I/O ports.

The interface is an unbalanced bus using 95Ω, terminated, coax cables. Devices connected to the bus should feature short-circuit protection, hysteresis in the receivers, and open-emitter drivers. Careful attention should be paid to line lengths and quality in order to limit cable noise to less than 400 mV.

TABLE VIII. MIL-STD-1397 Specification Summary

Symbol	Parameter	Conditions	Comparison Limits (MIL-STD)		Units
			1397 (Slow)	1397 (Fast)	
	Data Transmission Rate		42	250	k Bits/Sec
V_{OH} V_{OL}	Driver Output Voltage		±1.5 −10 to −15.5	0 −3	V V
I_{OH} I_{OL}	Driver Output Current		≥ −4 1		mA mA
R_S	Driver Power OFF Impedance		≥100		kΩ
V_{IH} V_{IL}	Receiver Input Voltage	Fail-Safe Open Circuit	≤4.5 ≥ −7.5	≤ −1.1 ≥ −1.9	V V

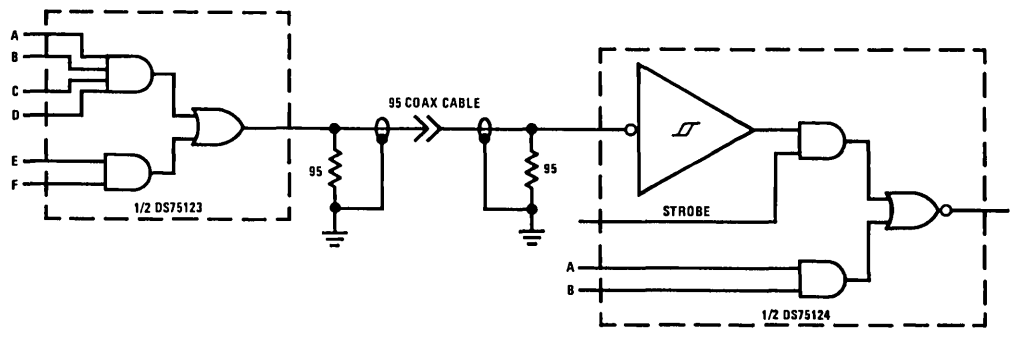

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FIGURE 7. IBM 360/370 I/O Application

TABLE IX. IBM 360/370 Specification Summary

Symbol	Parameter	Conditions	IBM 360/370			Units
			Min	Typ	Max	
V_{OH}	Driver Output Voltage	I_{OH} = 123 mA			7	V
V_{OH}		I_{OH} = 30 μA			5.85	V
V_{OH}		I_{OH} = 59.3 mA	3.11			V
V_{OL}		I_{OL} = −240 μA			0.15	V
V_{IH}	Receiver Input Threshold				1.7	V
V_{IL}	Voltage		0.7			V
I_{IH}	Receiver Input Current	V_{IN} = 3.11V			−0.42	mA
I_{IL}		V_{IN} = 0.15V	0.24			mA
	Receiver Input Voltage Range					
V_{IN}	Power ON		−0.15		7	V
V_{IN}	Power OFF		−0.15		6	V
V_{IN}	Power ON		−0.15		7	V
V_{IN}	Power OFF		−0.15		6	V
R_{IN}	Receiver Input Impedance	0.15V ≤ V_{IN} ≤ 3.9V	7400			Ω
I_{IN}	Receiver Input Current	V_{IN} = 0.15V			240	μA
Z_O	CABLE Impedance		83		101	Ω
R_O	CABLE Termination	P_D ≥ 390 mW	90		100	Ω
	Line Length (Specified as Noise on Signal and Ground Lines)				400	mV

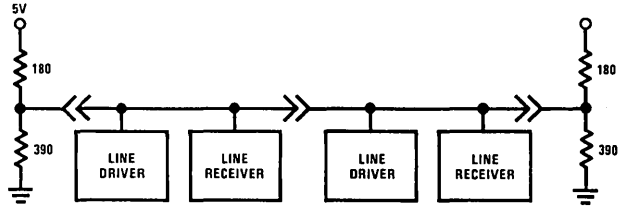

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FIGURE 8. DEC Unibus Application

TABLE X. DEC Unibus Specification Summary

Symbol	Parameter	Conditions	DEC Unibus			Units
			Min	Typ	Max	
V_{OL} V_O	Driver Output Voltage	I_{OL} = 50 mA Absolute Maximum			0.7 7	V V
V_{IH} V_{IL}	Receiver Input Voltage		1.7		 1.3	V V
I_{IH} I_{IL}	Receiver Input Current	V_{IN} = 4V V_{IN} = 4V Power OFF			100 100	μA μA

3.2 DEC UNIBUS

Another example of an unofficial industry standard is the interface to a number of DEC minicomputers. This interface, configured as a 120Ω double-terminated data bus is given the name Unibus. Devices connected to the bus should feature hysteresis in the receivers and open-collector driver outputs. Cable noise should be held to less than 600 mV.

4.0 INSTRUMENTATION TO COMPUTER INTERFACE STANDARDS

4.1 INTRODUCTION

The problem of linking instrumentation to processors to handle real-time test and measurement problems was largely a custom interface problem. Each combination of instruments demanded unique interfaces, thus inhibiting the wide spread usage of small processors to day-to-day test, measurement and control applications.

Two groups addressed the problem for specific environments. The results are:

a) IEEE 488 bus standard based upon proposals made by HP, and

b) The CAMAC system pioneered by the nuclear physics community.

4.2 IEEE 488

IEEE 488 covers the functional, mechanical and electrical interface between laboratory instrumentation (i.e., signal generators, DPM's, counters, etc.) and processors such as programmable calculators and minicomputers. Equipment with IEEE 488 I/O ports can be readily daisy chained in any combination of up to 15 equipments (including processor) spanning distances of up to 60 feet. 16 lines (3 handshake, 5 control and 8 data lines) are required.

4.3 CAMAC

The CAMAC system is the result of efforts by those in the nuclear physics community to standardize the interface between laboratory instruments and computers before the introduction of IEEE 488.

It allows either serial or parallel interconnection of instruments via a "crate" controller.

The electrical requirements of the interfaces are compatible with DTL and TTL logic levels.

5.0 MICROPROCESSOR SYSTEMS INTERFACE STANDARDS

5.1 Microprocessor Systems

Microprocessor systems are bus organized systems with two types of bus requirements:

a) Minimal system: for data transfer over short distances (usually on 1 PC board), and,

b) Expanded system: for data transfer to extend the memory or computational capabilities of the system.

5.2 Minimal Systems and Microbus

Microbus considers the interface between MOS/LSI microprocessors and interfacing devices in close physical proximity which communicate over 8-bit parallel unified bus systems. It specifies both the functional and electrical characteristics of the interface and is modeled after the 8060, 8080 and 8090 families of microprocessors as shown in *Figures 10, 11* and *12*.

The electrical characteristics of Microbus are shown in Table XII.

TABLE XI. IEEE 488 Specification Summary

Symbol	Parameter	Conditions	IEEE 488			Units
			Min	Typ	Max	
V_{OH} V_{OL}	Driver Output Voltage	I_{OH} = −5.2 mA I_{OL} = 48 mA	2.4		 0.4	V V
 I_{OZ} I_{OH}	Driver Output Current TRI-STATE® Open Collector	 V_O = 2.4V V_O = 5.25V			 ±40 250	 μA μA
V_{IH} V_{IL}	Receiver Input Voltage	0.4V Hysteresis Recommended	2.0		 0.8	V V
I_{IH} I_{IL}	Receiver Input Current	V_{IN} = 2.4V V_{IN} = 0.4V			40 −1.6	μA mA
	Receiver Clamp Current	V_{IN} = −1.5V			12	mA
R_{L1} R_{L2}	Termination Resistor	V_{CC} = 5V (±5%) V = Gnd	2850 5890		3150 6510	

TABLE XII. Microbus Electrical Specification Summary

Symbol	Parameter	Driver	Receiver		Units
			Standard	Hysteresis (Recommended)	
V_{OL}	Output Voltage (At 1.6 mA)	≤0.4V			
V_{OH}	(At −100 μA)	≥2.4V			
V_{IL}	Input Voltage		0.8	0.6	V
V_{IH}			2.0	2.0	V
	Internal Capacitive Load at 25°C	15	10	10	pF
t_r	Rise Time (Maximum)	100			ns
t_f	Fall Time (Maximum)	100			ns

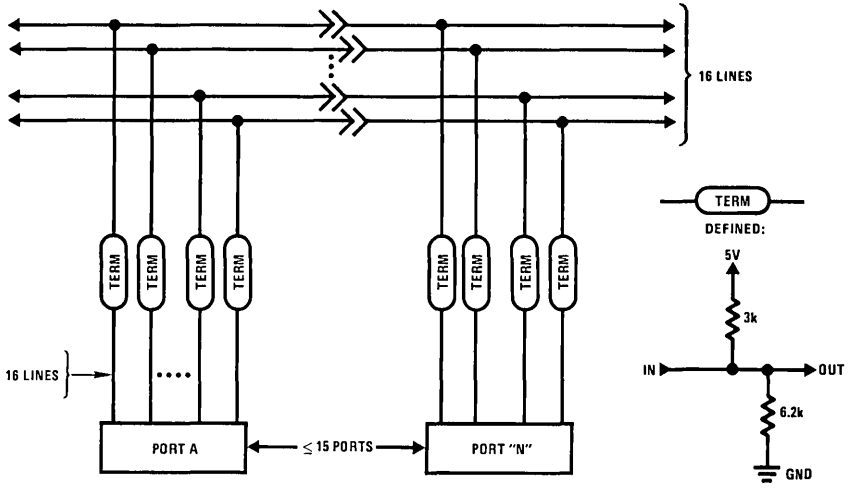

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FIGURE 9. IEEE 488 Application

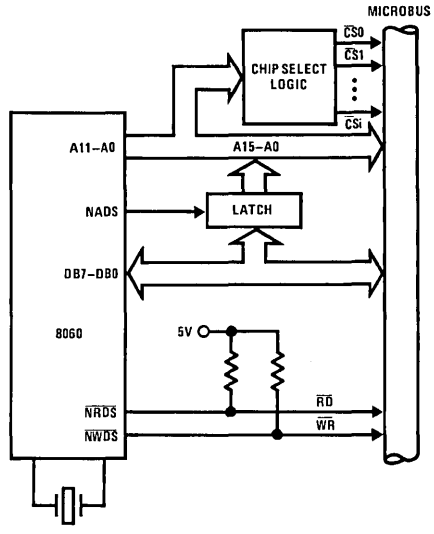

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FIGURE 10. 8060 SC/MP II System Moldel

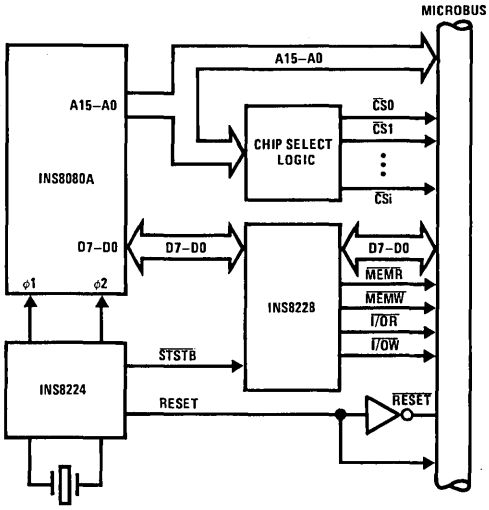

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FIGURE 11. 8080 System Model for the Basic Microbus Interface

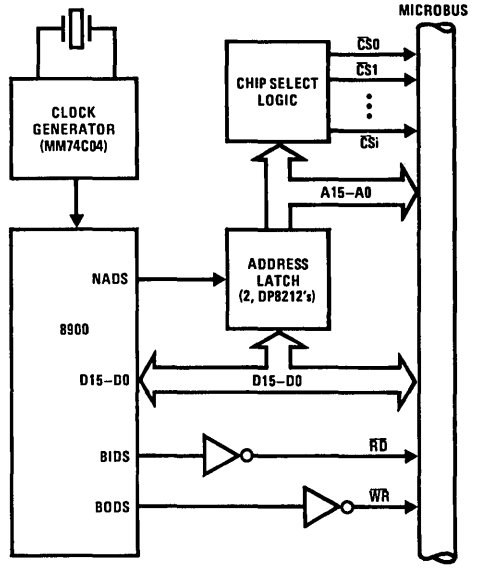

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FIGURE 12. 8900 System Model

5.3 Expanded Microprocessor System Interfaces

Since the outputs of most microprocessor devices are limited to a loading of one relative to a TTL load, expanded system will require buffers on both their address and data lines.

To date, no formal standards exist which govern this interface. However, "defacto" standards are emerging in the form of the specifications for "recommended devices" which are mentioned in the data sheets and application notes for the widely sourced microprocessor devices. Here, the answer to the question of how to provide a "standard" interface is simplified to that of proper usage of recommended devices.

Table XIII summarizes the important electrical characteristics of recommended bus drivers for expanded microprocessor systems.

6.0 OTHER INTERFACE STANDARDS

Some other commonly occurring interfaces which have become standardized are:

a) Interface between facsimile terminals and voice frequency communication terminals,

b) Interface between terminals and automatic calling equipment used for data communications, and

c) Interface between numerically controlled equipment and data terminals.

TABLE XIII. Recommended Specification of Bus Drivers for Expanded Microprocessor Systems

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}			2			V
V_{IL}					0.8	V
V_{OH}	Driver Output Voltage	$I_{OH} = -10$ mA	2.4			V
V_{OL}		$I_{OL} = 48$ mA			0.5	V
I_{OS}	Short-Circuit Current	$V_{CC} = 5.25V$			−150	mA
C_L	Bus Drive Capability		300			pF

6.1 EIA RS-357

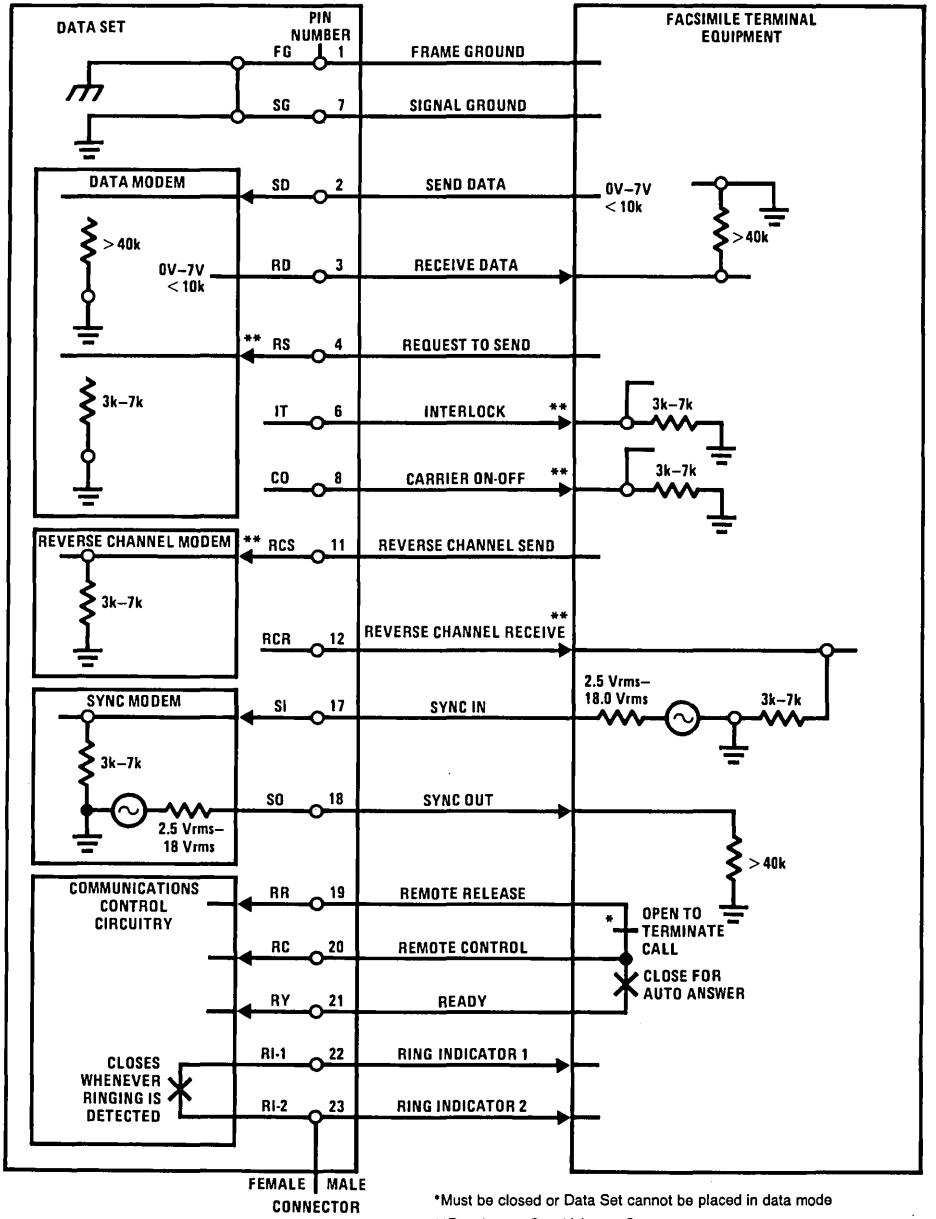
RS-357 defines the electrical, functional and mechanical characteristics of the interface between analog facsimile equipment to be used for telephone data transmission and the data sets used for controlling/transmitting the data.

Figure 13 summarizes the functional and electrical characteristics of RS-357.

6.2 EIA RS-366

RS-366 defines the electrical, functional and mechanical characteristics of the interface between automatic calling equipment for data communications and data terminal equipment.

The electrical characteristics are encompassed by RS-232C.



*Must be closed or Data Set cannot be placed in data mode

**Receive	Sensitivity	Source
ON	3V–25V	5V–25V
OFF	3V–25V	5V–25V

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FIGURE 13. Functional and Electrical Characteristics RS-357

6.3 EIA RS-408

RS-408 recommends the standardization of the 2 interfaces shown in *Figure 14.*

The electrical characteristics of NCE to DTE interface are, in summary, those of conventional TTL drivers (series 7400) with:

$V_{OL} \leq 0.4V$ at $I_{OL} = 48$ mA

$V_{OH} \geq 2.4V$ at $I_{OH} \leq -1.2$ mA, and

$C_L \leq 2000$ pF.

Short circuit protection should be provided.

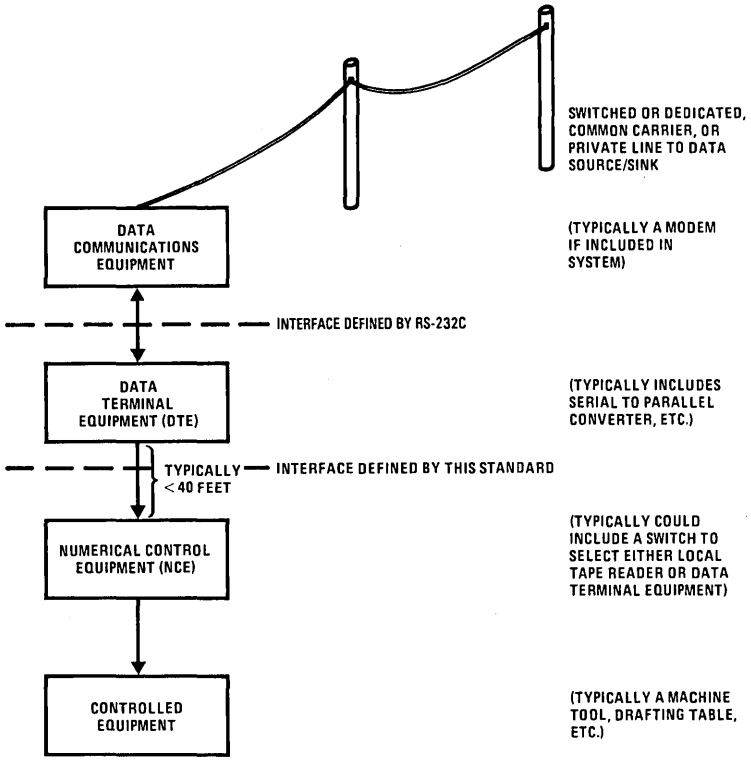

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FIGURE 14. EIA RS-408 Interface Applications

Transceivers and Repeaters Meeting the EIA RS-485 Interface Standard

National Semiconductor Corp.
Application Note 409
Sivakumar Sivasothy

INTRODUCTION

The Electronics Industries Association (EIA), in 1983, approved a new balanced transmission standard called RS-485. The EIA RS-485 standard addresses the problem of data transmission, where a balanced transmission line is used in a party-line configuration. It is similar in many respects to the popular EIA RS-422 standard; in fact RS-485 may be considered the outcome of expanding the scope of RS-422 to allow multipoint—multiple drivers and receivers sharing the same line—data transmission. The RS-485 standard, like the RS-422 standard, specifies only the electrical characteristics of the driver and the receiver to be used at the line interface; it does not specify or recommend any protocol. The protocol is left to the user.

The EIA RS-485 standard has found widespread acceptance and usage since its ratification. Users are now able to configure inexpensive local area networks and multi-drop communication links using twisted pair wire and the protocol of their choice. They also have the flexibility to match cable quality, signalling rate and distance to the specific application and thus obtain the best tradeoff between cost and performance. The acceptance of the RS-485 standard is also reflected by the fact that other standards refer to it when specifying multipoint data links. The ANSI (American National Standards Institute) standards IPI (Intelligent Peripheral Interface) and SCSI (Small Computer Systems Interface) have used the RS-485 standard as the basis for their voltage mode differential interface class. The IPI standard specifies the interface between disc drive controllers and host adapters and requires a data rate of 2.5 megabaud over a 50 meters NRZ data link. The SCSI standard specifies the interface between personal computers, disc drives and printers at data rates up to a maximum of 4 megabaud over 25 meters.

It is not possible to use standard gate structures and meet the requirements of RS-485. The modifications necessary to comply with the DC requirements of the standard, tend to exact a heavy toll on speed and other AC characteristics like skew. However, it is possible to vastly improve the ac performance by employing special design techniques. The DS3695 family of chips made by National Semiconductor meets all the requirements of EIA RS-485, and still provides ac performance comparable with most existing RS-422 devices. The chip set consists of four devices; they are the DS3695/DS3696 transceivers and the DS3697/DS3698 repeaters. National's RS-485 devices incorporate several features in addition to those specified by the RS-485 standard. These features provide greater versatility, easier use and much superior performance. This article discusses the requirements of a multi-point system, and the way in which RS-485 addresses these requirements. It also explains the characteristics necessary and desirable in the multi-point drivers and receivers, so that these may provide high performance and comply with generally accepted precepts of data transmission practice.

WHY RS-485?

Until the introduction of the RS-485 standard, the RS-422 standard was the most widely accepted interface standard for balanced data transmission. The RS-422 drivers and re-

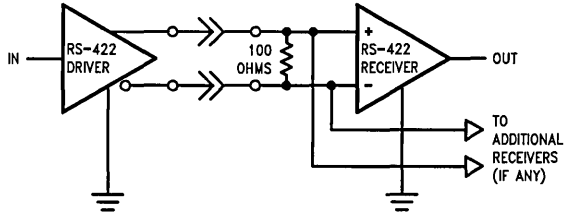

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FIGURE 1a. An RS-422 Configuration

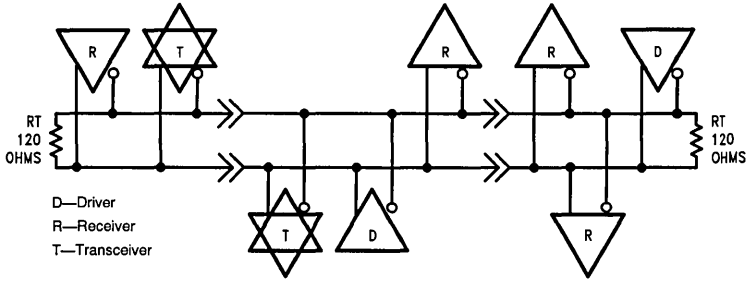

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FIGURE 1b. A Typical RS-485 Party-Line Configuration

ceivers were intended for use in the configuration shown in *Figure 1a*. The driver is at one end of the line; the termination resistor (equal to 100Ω) and up to 10 receivers reside at the other end of the line. This approach works well in simplex (unidirectional) data transmission applications, but creates problems when data has to be transmitted back and forth between several pieces of equipment. If several Data Terminal Equipments (DTEs) have to communicate with one another over long distances using RS-422 links, two such balanced lines have to be established between each pair of DTEs. The hardware cost associated with such a solution would normally be unacceptable.

A party line is the most economical solution to the above problem. RS-422 hardware could conceivably be used to implement a party line if the driver is provided with TRI-STATE® capability, but such an implementation would be subjected to severe restrictions because of inadequacies in the electrical characteristics of the driver. The biggest problem is caused by ground voltage differences. The common mode voltage on a balanced line is established by the enabled driver. The common mode voltage at the receiver is the sum of the driver offset voltage and the ground voltage difference between the driver and the receiver. In simplex systems only the receiver need have a wide common mode range. Receiver designs that provide a wide common mode range are fairly straightforward. In a party-line network several hundred feet long, in which each piece of equipment is earthed at a local ac outlet, the ground voltage difference between two DTEs could be as much as a few volts. In such a case both the receiver and the driver must have a wide common mode range. Most RS-422 drivers are not designed to remain in the high impedance state over a wide enough common mode range, to make them immune to even small ground drops.

Classical line drivers are vulnerable to ground drops because of their output stage designs. A typical output stage is shown in *Figure 2a*. Two such stages driven by complementary input signals, may be used to provide the complementary outputs of a differential line driver. Transistors Q1 and Q4 form a Darlington pull up for the totem pole output stage; Q2 is the pull down transistor. The phase splitter Q3 switches current between the upper and lower transistors to obtain the desired output state. DSUB is the diode formed by the collector of Q2 and the grounded substrate of the integrated circuit. The output in *Figure 2a* can be put into the high impedance state by pulling down the bases of transistors Q3 and Q4. Unfortunately, the high impedance state cannot be maintained if the output is pulled above the power supply voltage or below ground voltage. In party-line applications, where ground voltage differences of a few volts will be common, it is essential that the drivers be able to hold the high impedance state while their outputs are taken above V_{CC} and below ground.

The output in *Figure 2a* can be taken high until the emitter-base junction of Q1 breaks down. Thereafter, the output will be clamped to a zener voltage plus a base-collector diode voltage above V_{CC}; V_{CC} could be zero if the device is powered off. If the output is taken below ground, it will cause the substrate diode, DSUB, associated with Q2 to turn on and clamp the output voltage at a diode drop below ground. If a disabled driver turns on and clamps the line, the signal put out by the active driver will get clipped and distorted. It is also possible for ground drops to cause dangerously large substrate currents to flow and damage the devices as illustrated in *Figure 2b*. *Figure 2b* depicts two drivers A and B; it shows the pull down transistors (Q2A and Q2B) and their associated substrate diodes (DSUB-A and DSUB-B) for the two drivers A and B. Here driver A is ON in the low output state; driver B is disabled, and therefore, should neither source nor sink current. The ground of driver A is 3 volts lower than that of driver B. Consequently, the substrate diode DSUB-B sees a forward bias voltage of about 2.7V (the collector-emitter voltage of Q2A will be about 0.3V), which causes hundreds of milliamperes of current to flow out of it.

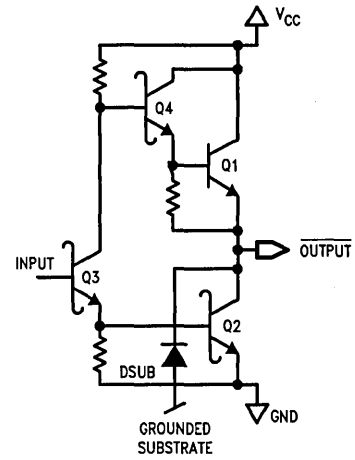

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FIGURE 2a. Driver Output Stage (not RS-485)

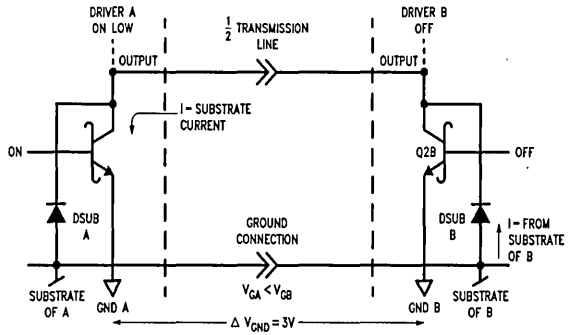

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FIGURE 2b. Two DCEs Separated by a Ground Drop

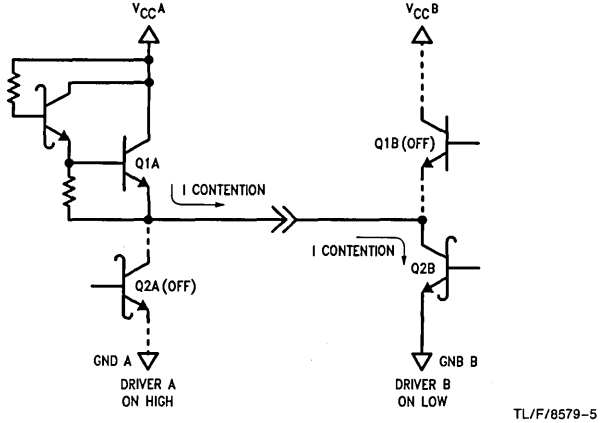

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FIGURE 2c. Bus Contention

Another problem is line contention, i.e. two drivers being 'ON' simultaneously. Even if the protocol does not allow two drivers to be on at the same time, such a contingency could arise as a result of a fault condition. A line contention situation, where two drivers are on at the same time, is illustrated in *Figure 2c*. Here, drivers A and B are 'ON' simultaneously; driver A is trying to force a high level on the line whereas driver B is trying to force a low level. Transistors Q1A and Q2B are 'ON' while transistors Q2A and Q1B are 'OFF'. As a result, a large current is sourced by Q1A and sunk by Q2B; the magnitude of this current is limited only by the parasitic resistances of the two devices and the line. The problem is compounded by any ground drop that may exist between the two contending drivers. This large contention current can cause damage to one or both of the contending drivers. Most RS-422 drivers are not designed to handle line contention.

A multi-point driver should also be capable of providing more drive than a RS-422 driver. The RS-422 driver is only required to drive one 100Ω termination resistor, and ten receivers each with an input impedance no smaller than 4 kΩ. A party-line, however, would have to be terminated at both ends; it should also be able to drive more devices to be useful and economical.

Because of the above limitations, it is quite impractical to use RS-22 hardware to interconnect systems on a party-line. Clearly, a new standard had to be generated to meet the more stringent hardware requirements of muti-point data links.

THE RS-485 STANDARD

The RS-485 standard specifies the electrical characteristics of drivers and receivers that could be used to implement a balanced milti-point transmission line (party-line). A data exchange network using these devices will operate properly in the presence of reasonable ground drops, withstand line contention situations and carry 32 or more drivers and receivers on the line. The intended transmission medium is a 120Ω twisted pair line terminated at both ends in its characteristic impedance. The drivers and receivers can be distributed between the termination resistors as shown in *Figure 1b*.

The effects of ground voltage differences are mitigated by expanding the common mode voltage (V_{CM}) range of the driver and the receiver to $-7V < V_{CM} < +12V$. A driver forced into the high impedance state, should be able to have its output taken to any voltage in the common mode range and still remain in the high impedance state, whether powered on or powered off. The receiver should respond properly to a 200 mV differential signal super-imposed on any common mode voltage in this range. With a 5V power supply, the common mode voltage range specified by RS-485 has a 7V spread from either supply terminal. The system will therefore perform properly in the presence of ground drops and longitudinally coupled extraneous noise, provided that the sum of these is less than 7 volts.

The output drive capability of the driver and the input impedance of the receiver are increased to accommodate two termination resistors and several devices (drivers, receivers and transceivers) on the line. The RS-485 standard defines a 'unit load' so that the load presented to the line by each device can be expressed in terms of unit loads (a 12 kΩ resistor, with one end tied to any voltage between ground and $V_{CC}/2$, will satisfy the requirements of a unit load). It was anticipated that most manufacturers would design their drivers and receivers such that the combined load of one receiver and one disabled driver would be less than one unit load. This would require the RS-485 receiver to have three times the input resistance of a RS-422 receiver. The required receiver sensitivity is ±200 mV—the same as for RS-422. The driver is required to provide at least 1.5V across its outputs when tied to a terminated line populated with 32 transceivers. Although this output voltage is smaller than the 2.0V specified for RS-422, a careful design of the driver, with special regard to ac performance, can allow the user to operate a multi-point network at data rates and distances comparable to RS-422.

RS-485 has additional specifications to guarantee device safety in the event of line contention or short circuits. An enabled driver whose output is directly shorted to any voltage in the common mode range, is required to limit its current output to ±250 mA. Even with such a current limit, it is possible for a device to dissipate as much as 3 Watts (if the device draws 250 mA while shorted to 12 volts). Power dissipation of such a magnitude will damage most ICs; therefore, the standard requires that manufacturers include some additional safeguard(s) to protect the devices in such situations.

The ±250 mA current limit also serves another purpose. If a contending driver is abruptly turned off, a voltage transient, of magnitude $I_C Z/2$, is reflected along the line as the line discharges its stored energy (I_C is the contention current and Z is the characteristic impedance of the line). This voltage transient must be small enough to avoid breaking down the output transistors of the drivers on the line. If the contention current is limited to 250 mA, the magnitude of this voltage transient, on a 120Ω line, is limited to 15V, a value that is a good compromise between transistor breakdown voltage and speed.

AC PERFORMANCE

To achieve reliable transmission at high data rates over long distances, the driver should have optimum ac characteristics. The response should be fast and the output transients sharp and symmetrical.

(1) **Propagation Delay:** The propagation delay through the driver should be small compared to the bit interval so that the data stream does not encounter a bottle-neck at the driver. If the propagation delay is comparable to the bit interval, the driver will not have time to reach the full voltage swing it is capable of. In lines a few hundred feet long, the line delay would impose greater limits on data throughput than the driver propagation delay. However, a fast driver would be desirable for short haul networks such as those in automobile vehicles or disc drives; in the latter case high data throughput would be essential. Driver propagation delays less than 20 ns would be very good for a wide range of applications.

(2) **Transition Time:** For distortion free data transmission, the signal at the farthest receiver must have rise and fall times much smaller than the bit interval. Signal distortion results from driver imbalance, receiver threshold offset and skew. RS-485 limits the DC imbalance in the driver output to ±0.2V i.e., 13% of worst-case signal amplitude. Usually, the greatest distortion is caused by offset in the receiver threshold. In a long line in which a 1.5V driver output signal amplitude is attenuated by the loop resistance to about 0.4V, a 200 mV offset in the receiver threshold can cause severe pulse width distortion if the rise time is comparable to the bit interval. For lines longer than about five hundred feet, the rise time would be dominated by the line and not the driver. In short-haul networks, the transient response of the driver can significantly affect signal distortion; a faster transient creates less distortion and hence permits a smaller bit interval and a higher baud rate. A rise time less than 20 ns will be a good target spec., for it will permit a baud rate of 10 Meg over 50' of standard twisted pair wire with less than 5% distortion.

The driver should provide the above risetime and propagation delay numbers while driving a reasonable capacitance, say 100 pF from each output, in addition to the maximum resistive load of 54Ω. A properly terminated transmission line appears purely resistive to the driver. Most manufacturers take this into account and specify their driver delays with 15 pF loads. However, if any disabled transceivers are situated close to the driver (such that the round trip delay is less than the rise time), the input capacitances of these transceivers will appear as lumped circuit loads to the driver. The driver output rise time will then be affected by all other devices in such close proximity. In the case of high speed short-haul networks, where rise time and propagation delay are critical, several devices could be clustered in a short span. In such an instance, specifying propagation delays with 15 pF loads is quite meaningless. A 100 pF capacitive load is more reasonable; even if we allocate a generous 20 pF per transceiver, it allows up to six transceivers to be clustered together in an eight foot span (the eight foot span is the approximate round trip distance travelled by the wavefront in one rise time of 20 ns).

(3) **Skew:** The ideal differential driver will have the following waveform characteristics: the propagation delay times from the input to the high and low output states will be equal; the rise and fall times of the complementary outputs will be equal and the output waveforms will be perfectly symmetrical.

If the propagation delay to the low output state is different from the propagation delay to the high output state, there is said to be 'propagation skew' between output states. If a square wave input is fed into a driver with such skew, the output will be distorted in that it will no longer have a 50% duty cycle.

If the mid-points of the waveforms from the two complementary driver outputs are not identical, there is said to be SKEW between the complementary outputs. This type of skew is undesirable because it impairs the noise immunity of the system and increases the amount of electromagnetic emission.

Figure 3a shows the differential signal from a driver that has no skew. *Figure 3b* shows the case when there is 80 ns of skew. The first signal makes its transition uniformly and passes rapidly through 0V. The second waveform flattens out for tens of nanoseconds near 0V. Unfortunately, this flat region occurs near the receiver threshold. A common mode noise spike hitting the inputs of a slightly unbalanced receiver would create a small differential noise pulse at the receiver inputs. If this noise

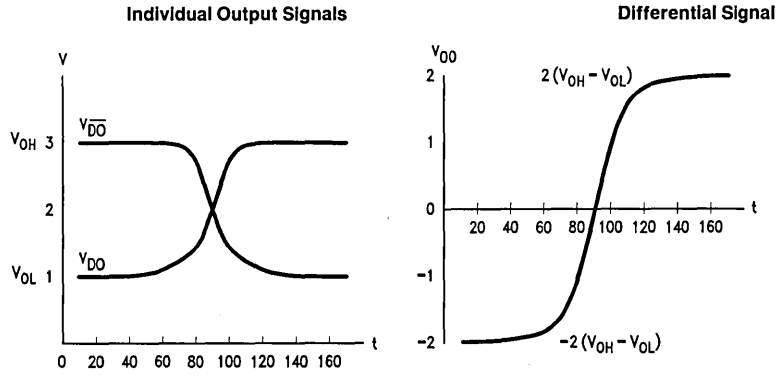

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FIGURE 3a. Transients with no Skew

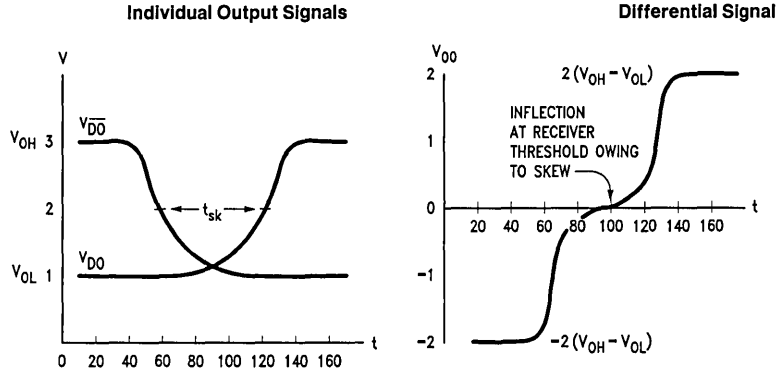

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FIGURE 3b. Skewed Transients

pulse occurs when the driver transition is flat near 0V, there will be a glitch at the receiver output. A glitch could also occur if a line reflection reaches the receiver input when the driver transition is temporarily flat. Skew is insidious in that it can cause erroneous outputs to occur at random. It can also increase the amount of electromagnetic interference (EMI) generated by the transmission system. If the complementary outputs are perfectly symmetrical, and the twisted pair medium is perfectly balanced, the radiation from one wire is cancelled exactly by the radiation from the other wire. If there is skew between the outputs, there will be net radiation proportional to the skew.

(4) **Balance:** The impedance seen looking into each of the complementary inputs of the transceiver should be identical. If there is any imbalance at these nodes, the common mode rejection will be degraded. Any DC imbalance, due to a mismatch in the receiver input resistances, will manifest itself as an offset in the receiver threshold, and can be easily detected during testing. AC imbalance is more difficult to detect, but it can hurt noise immunity at high frequencies. A sharp common mode noise spike striking an unbalanced receiver will cause a spurious differential signal. If the receiver is fast enough (as it is bound to be in most cases), it will respond to this noise signal. It is best to keep the imbalance below 4 pF. This number is reasonable to achieve; in addition, the combined imbalance of 32 transceivers will still provide sufficient immunity from h.f. interference.

DESIGN CONSIDERATIONS

The driver poses the greatest design challenge. Its speed, drive and common mode voltage requirements are best met using a bipolar process. National Semiconductor uses an established Schottky process with a 5μ deep epitaxial layer. NPN transistors are fabricated with LVCEO values greater than 15V to satisfy the breakdown requirements. It will be seen that lateral PNP transistors are crucial to the driver. The 5μ EPI process provides adequate lateral PNP transistors, and NPN transistors of sufficient speed.

Figure 4 shows the driver output circuit used by National. It is a standard totem pole output circuit modified to provide a common mode range that exceeds the supply limits. If the driver output is to be taken to −7V while the driver is in TRI-STATE, precautions must be taken to prevent the substrate diodes from turning on. This is achieved in the lower output transistor Q1 by including Schottky diode S1 in series. The only way to isolate the upper half of the totem pole from the substrate is by using a lateral PNP transistor. Lateral PNP transistors are, however, notoriously slow; the trick therefore is not to use the PNP transistor in the switching path. In the circuit shown, the PNP transistor is a current source which feeds NPN transistor Q2 and therefore, does not participate in the switching function. This allows National's driver to have 15 ns propagation delays and 10 ns rise timers. A Darlington stage cannot be used instead of Q2 because it would reduce the voltage swing below the 1.5V specification. Consequently, the rise time is bound to be significantly larger than the fall time, resulting in a large skew. National's driver uses a patented circuit with a plurality of discharge paths, to slow down the falltime so that it matches the rise time, and to keep the two transition times on track over temperature. This keeps the skew small (2 ns typical at 25°C) over the entire operating temperature range. The symmetry of the complementary outputs of National's DS3695 driver can be seen from the photographs in *Figure 5*. The lateral PNP transistor which has been kept out of the switching path has nevertheless got to be turned on or off when the driver is respectively enabled or disabled. Another patented circuit is used to hasten turn-on and turn-off of the lateral PNP transistors so that these switch in 25 ns instead of in 100 ns. Consequently, the driver can be enabled or disabled in 35 ns.

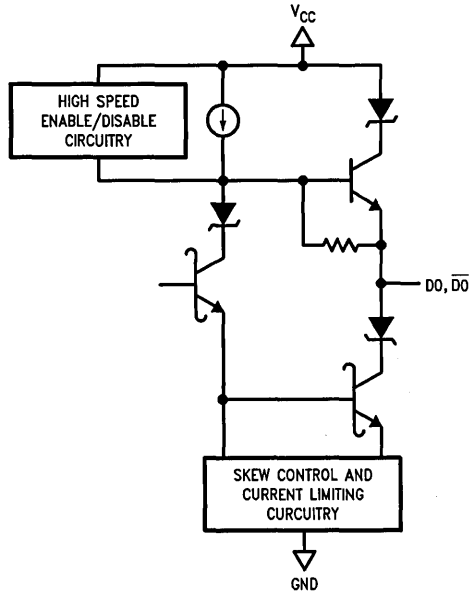

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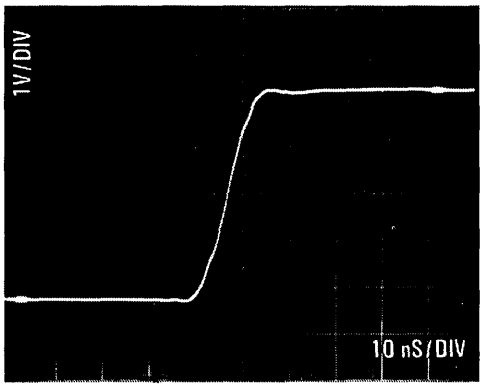
FIGURE 4

Complementary Outputs of National's RS-485 Driver



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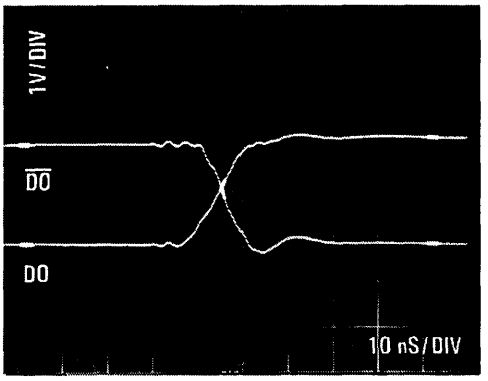
Differential Output of National's RS-485 Driver



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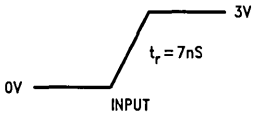

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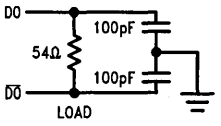

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FIGURE 5

The devices must be protected in fault conditions and contention situations. One way of doing this is by sensing current and voltage to determine power, and then if necessary, turning the device off or limiting its output current to prevent damage. This method has the advantage of fast detection of a fault and rapid recovery from one. However, too many contingencies have to be accounted for; the corresponding circuitry will increase the die size and the cost beyond what would be acceptable in many low cost applications. National preferred the simpler and inherently more reliable thermal shutdown protection scheme. Here, the device is disabled when the die temperature exceeds a certain value. This method is somewhat slower (order of milliseconds), but fast enough to protect the part. A fault would usually result from a breakdown in network protocol or from a hardware failure. In either case it is immaterial how long the device takes to shut down or recover as long as it stays undamaged. It would be useful to be notified of the occurrence of a fault in any particular channel, so that remedial action may be taken. Two of National's devices, the DS3696 receiver and the DS3698 repeater, provide a fault reporting pin which can flag the processor or drive an alarm LED in the event of a fault. National also decided to make its devices as single transceivers housed in 8 pin mini DIP packages. If thermal shutdown protection is employed, it is pointless to have dual or quad versions because a faulty channel will shut down a good one. Since most RS-485 applications will employ single channel serial data, the 8 pin package will give optimum flexibility, size and economy.

The receiver has 70 mV (typical) hysteresis for improved noise immunity. Hysteresis can contribute some distortion, especially in short lines, if the rise and fall times are different. However, this is more than adequately compensted for by the noise immunity it provides with long lines where rise times are slow. The matched rise and fall times with National's drivers assure low pulse width distortion even at short distances and high data rates.

Low Power RS-232C Driver and Receiver in CMOS

National Semiconductor Corp.
Application Note 438
Gordon W. Campbell

This article sets out to describe the new innovative low power CMOS RS-232C driver and receiver IC's introduced by National Semiconductor with particular reference to the EIA RS-232C standard. Comparison will also be made with existing bipolar driver and receiver circuits.

The DS14C88 and DS14C89A are monolithic MOS circuits utilizing a standard CMOS process. Important features are a wide operating voltage range (4.5V–12.6V), together with ESD and latch up protection and proven reliability.

The Electronics Industries Association released Data Terminal Equipment (DTE) to Data Communications Equipment (DCE) interface standards to cover the electrical, mechanical and functional interface between/among terminals (i.e. teletypewriters, CRT's etc.) and communications equipment (i.e. modems, cryptographic sets etc.).

The EIA RS-232C is the oldest and most widely known DTE/DCE standard. Its European version is CCITT V.24 specification. It provides for one-way/non-reversible, single ended (unbalanced) non-terminated line, serial digital data transmission.

The DS14C88 quad CMOS driver and its companion circuit, the DS14C89A quad CMOS receiver, combine to provide an efficient low power system for RS-232C or CCITT V.24 applications.

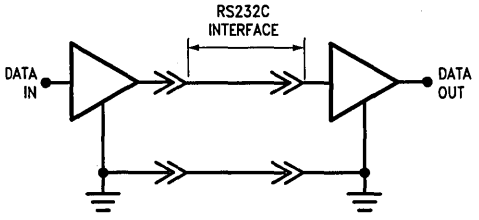


FIGURE 1. EIA RS-232C Application

THE DRIVER

The DS14C88 quad CMOS line driver is a pin replacement of the existing bipolar circuit DS1488/MC1488.

The DS14C88 is fabricated in CMOS technology and therefore has an inherent advantage over the bipolar DS1488/MC1488 line driver in terms of current consumption. Under worst case static conditions, the DS14C88 is a miser when it comes to current consumption. In comparison with the DS1488/MC1488 line driver, a current consumption reduction of 425 μA max versus 25 mA can be achieved.

The RS-232C specification states that the required driver output voltage is defined as being between +5V and +15V and is positive for a logic "0" (+5V to +15V) and negative for a logic "1" (−5V to −15V). These voltage levels are defined when driver is loaded ($3000\Omega < R_L < 7000\Omega$). The DS14C88 meets this voltage requirement by converting HC or TTL/LSTTL levels into RS-232C levels through one stage of inversion.

In applications where strict compliance to RS-232C voltage levels is not essential, a ±5V power supply to the driver may be used. The output voltage of the DS14C88 will be high enough to be recognized by either the 1489 or 14C89A receiver as valid data.

The RS-232C specification further states that, during transitions, the driver output slew rate must not exceed 30V/μs. The inherent slew rate of the equivalent bipolar circuit DS14C88/MC1488 is much too fast and requires the connection of one external capacitor (330–400 pF) to each driver output in order to limit the slew rate to the specified value. However, the DS14C88 does not require any external components. The DS14C88 has a novel feature in that unique internal slew rate control circuitry has been incorporated which eliminates the need for external capacitors; to be precise, a saving of four capacitors per package. The 14C88 minimizes RFI and transition noise spikes by typically setting the slew rate at 5V–6V/μs. This will enable optimum noise performance, but will restrict data rates to below 40k baud.

The DS14C88 can also withstand an accidental short circuit from a conductor in the interconnecting cable to any one of four outputs in a package without sustaining damage to itself or its associated equipment.

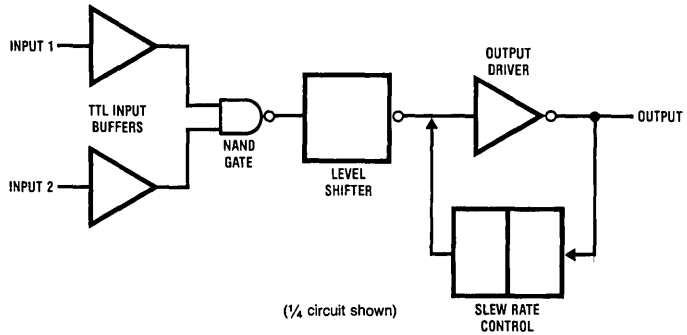


FIGURE 2. DS14C88 Line Driver Block Diagram

THE RECEIVER

The DS14C89A quad CMOS line receiver is a pin replacement of the existing bipolar circuit DS1489/MC1489/DS1489A/MC1489A.

The DS14C89A is fabricated in CMOS technology giving it an inherent advantage over the bipolar DS1489/MC1489/DS1489A/MC1489A circuits in terms of power consumption. Under worst case static conditions a power consumption reduction of 97% (600 μA against 26 mA) is achieved.

The RS-232C specification states that the required receiver input impedance as being between 3000Ω and 7000Ω for input signals between 3.0V and 25.0V. Furthermore, the receiver open circuit bias voltage must not be greater than +2V.

The DS14C89A meets these requirements and is able to level shift voltages in the range of −30V to +30V to HC or TTL/LSTTL logic levels through one stage of inversion. A voltage of between −3.0V and −25.0V is detected as a logic "1" and a voltage of between +3.0V and +25.0V is detected as logic "0".

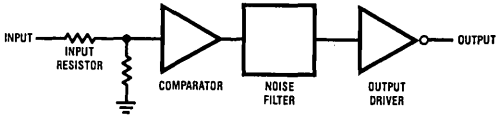
The RS-232C specification states that the receiver should interpret an open circuit or power off condition (source impedance of driver must be 300Ω or more to ground) as an OFF condition. In order to meet this requirement the input threshold of the DS14C89A is positive with respect to ground resulting in an open circuit or "power off" condition being interpreted as a logic "1" at the input.

Although the DS14C89A is pin replacement for the bipolar circuits DS1489/MC1489/DS1489A/MC1489A, its performance characteristics are modeled on the DS1489A/MC1489A.

The response control input on each of the bipolar circuits facilitates the rejection of noise signals by means of an external capacitor between each response control pin and ground.

When communicating between components of a data processing system in a hostile environment, spurious data such as ground shifts and noise signals may be introduced and it can become difficult to distinguish between a valid data signal and those signals introduced by the environment.

The DS14C89A eliminates the need for external response control capacitors and overcomes the effects of spurious data by means of unique internal noise filtering circuitry. *Figure 4* shows typical turn on threshold versus response control capacitance for existing bipolar devices. Note the curve for the DS14C89A CMOS device. The DS14C89A will not recognize any input signal whose pulse width is less than 1 μs, regardless of the voltage level of that input signal. Noise rejection in the bipolar parts depends on the voltage level of the noise transients. Therefore, in hostile environments the CMOS parts offer improved noise rejection properties. The DS14C89A has an internal comparator which provides input hysteresis for noise rejection. The DS14C89A has a typical turn-on voltage of 2.0V and a typical turn-off voltage of 1.0V resulting in 1.0V of hysteresis.



(¼ circuit shown) TL/F/8681–3

FIGURE 3. DS14C89A Line Receiver Block Diagram

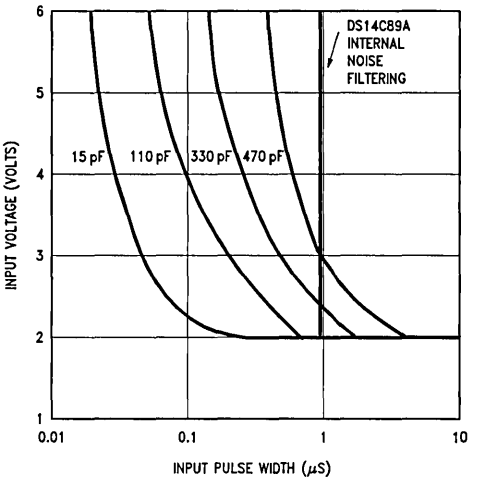


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FIGURE 4

TYPICAL APPLICATIONS

Obviously the major advantage of these CMOS devices is that with the large reduction of operating current, it is now possible to implement the "FULL" RS-232 interface in remote or portable equipment. Imagine that previously a designer, using a CMOS μP, RAM, ROM, and peripherals, could implement a complete system that consumes between 200 and 300 mW, but just adding the RS-232 interface (one driver, and one receiver) would add another 450 to 700 mW to the total system power consumption. This would severely shorten the battery life. The CMOS driver and receiver would only add about 40–50 mW.

In addition, the CMOS devices provide better noise rejection in harsh EMI environments, thus better data integrity. At the same time the internal slew rate limiting of the driver reduces the output transition time along the cable interface, hence reducing RFI emission, and easing the ability for portable (or non-portable) systems to meet FCC noise emission regulations. Also, since space is a premium in remote and portable systems, by integrating the function of the external capacitors on-chip (eliminating 8 capacitors), and designing these into S.O. packages, significant reduction in board space can be achieved.

For example, *Figure 5* shows a small CMOS system utilizing a CMOS NSC800 microprocessor, NSC858 CMOS UART, CMOS RAM/ROM, and a clock timer. This system runs off a 9V battery so a DC–DC converter is used to generate −9V for the RS-232 interface. In this design a standard DC–DC convert IC is used to generate a −9V supply from the single +9V battery.

As a second example, a "cheater" RS-232 interface is sometimes implemented. This interface is compatible with the current RS-232 driver/receiver products, but rather than using a ±(9–15)V supply, a ±5V supply is used. The drivers will not meet the RS-232 output voltage level specifications, but will correctly drive either the CMOS or bipolar receivers. The DC–DC converter circuit in *Figure 5* may be used to implement this. While for non-portable applications this can be done with the old bipolar 1488/89s, the DC–DC

converter is somewhat simpler with the CMOS parts due to the much reduced current consumption.

The RS-232 driver/receivers are also useful in non-power sensitive multi-user computers. Imagine a 16 terminal cluster controller for a multi-user computer system, *Figure 6.* This controller would require 16 drivers and 16 receivers with a total power of 8 watts when using the bipolar devices. The CMOS devices need only 400 mW.

Also proper noise rejection for receivers and slew rate limiting for the driver would require 128 capacitors for the bipolar parts, but they are unnecessary in the CMOS implementation.

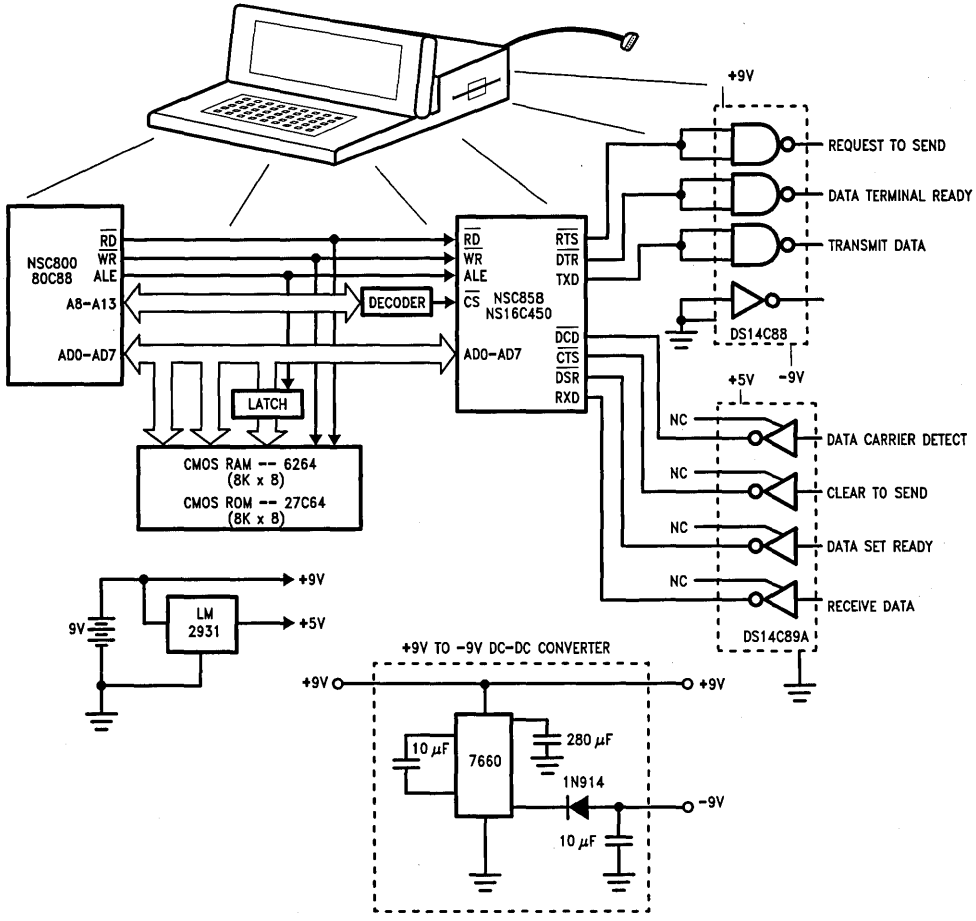

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FIGURE 5. Typical portable system application using CMOS μP, ROM, RAM, and UART. RS-232 interface is shown using 7660 supply inverter and CMOS Receiver/Driver.

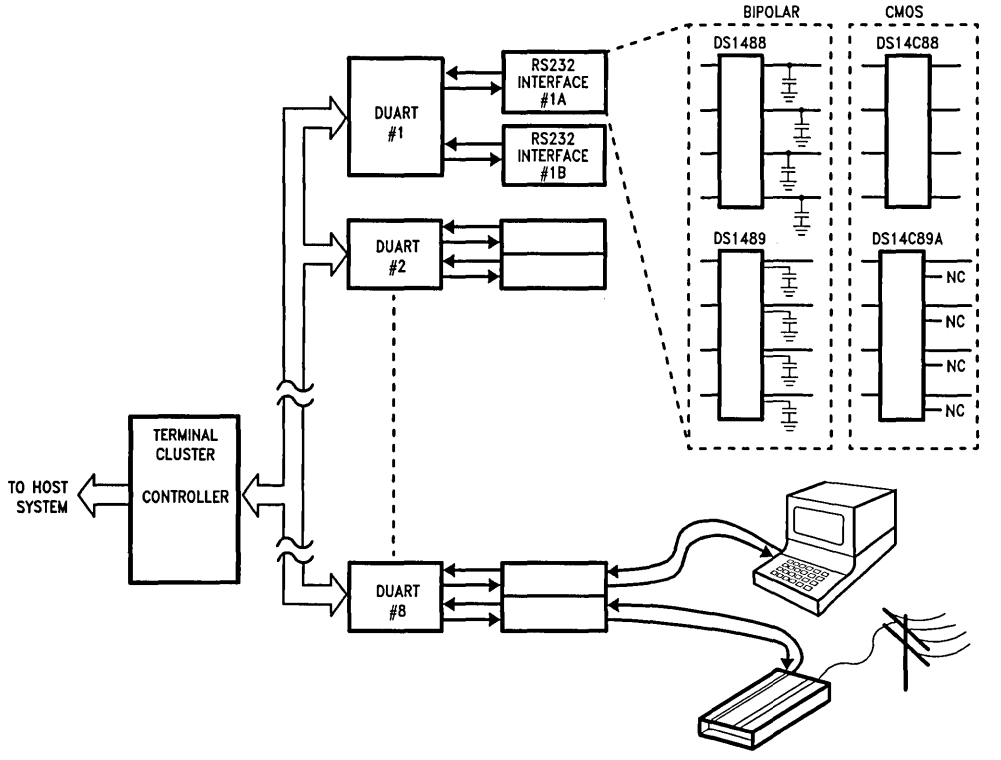

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FIGURE 6. A multi-terminal application showing a comparison of Bipolar vs CMOS solutions.

Lit # 100438

High Speed, Low Skew RS-422 Drivers and Receivers Solve Critical System Timing Problems

National Semiconductor Corp.
Application Note 457
Toan Tran
Larry Kendall

In system design, due to the distributed intelligence ability of the microprocessor, it is a common practice to have the peripheral circuits physically separated from the host processor with data communications being handled over cables. Usually, these cables are measured in hundreds or thousands of feet long. Signals which are transmitted on these transmission lines (or cables) are exposed to electrical noise sources which may require large noise immunity. The requirements for transmission lines and noise immunity are covered in E.I.A. standard RS-422.

The object of this application note is to describe the design requirement of RS-422 standard and to show that the National's DS8921, DS8922 and DS8923 Differential Driver and Receiver pair meet all of those requirements. Special circuit design techniques are used to achieve small skew on complementary signals of the driver outputs. In fact, these devices are designed specifically for applications which must meet stringent timing constraints including the ESDI Disk Drive standard. Also, the DS8921 series meet the requirement of ST506 and ST412HP standards.

BALANCED VOLTAGE DIGITAL INTERFACE CIRCUITS (RS-422) REQUIREMENT

Balanced circuits are normally used in data, timing, or control applications where the data signaling rate approaches fast speeds of 10 Mbit/s. In addition balanced data transmission techniques should be used when ever the following conditions exist:

1. The interconnecting cable is too long for effective unbalanced operation.
2. The interconnecting cable is exposed to a noise source which may cause a voltage sufficient to indicate a change of binary state at the load.
3. It is necessary to minimize interference with other signals.

Figure 1 below is a balanced circuit connection.

There are three major controlling factors in balanced voltage digital interface:

1. The cable length
2. The modulation rate
3. The characteristics of the Driver and Receiver

CABLE LENGTH

There is no maximum cable length specified in the RS-422 standard. Guidelines are given with respect to conservative operating distances as a function of modulation rate. *Figure 2* below is the guideline provided by RS-422 for data modulation rate versus cable length.

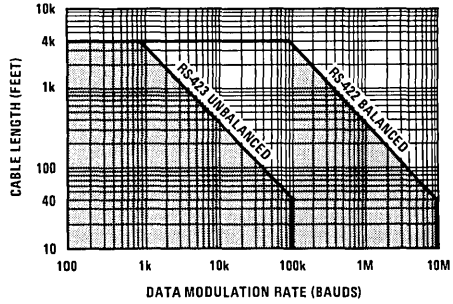

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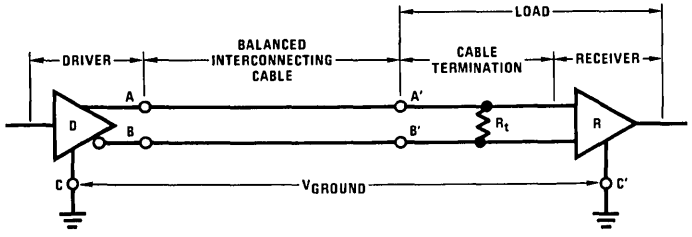
FIGURE 2. Data Modulation Rate vs Cable Length

The curve is based on empirical data using a 24 AWG, copper conductor, twisted pair cable terminated for worst case in a 100Ω load, with rise and fall time, equal or less than one half unit interval at the applied modulation rate.

Even though the maximum cable length between driver and load is a function of data signaling rate, it is also influenced by the tolerable signal distortion the amount of longitudinally coupled noise and ground potential difference introduced between the generator and load circuit grounds.



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Legend:

R_t = Optional cable transmission resistance/receiver input impedance.

V_{GROUND} = Ground potential difference

A, B = Driver interface

A', B' = Load Interface

C = Driver circuit ground

C' = Load circuit ground

FIGURE 1. RS-422 Balanced Digital Interface Circuit

MODULATION RATE

The balanced (or differential) voltage mode interface will normally be utilized on data, timing or control circuits operating at up to 10 Mbauds. The voltage digital interface devices meeting the electrical characteristics of this standard need not meet the entire modulation range specified. They may be designed to operate over narrower ranges to more economically satisfy specific applications, particularly at the lower modulation rates. The DS8921 family of devices meets or exceeds all of the recommended RS-422 performance specifications.

RS-422 CHARACTERISTICS

A. The Driver

The balanced driver characteristics are specified in RS-422 as follows:

1. A driver circuit should result in a low impedance (100Ω or less) balanced voltage source that will produce a differential voltage to the interconnecting cable in the range of 2V to 6V.
2. With a test load of 2 resistors, 50Ω each, connected in series between the driver output terminals, the magnitude of the differential voltage (VT) measured between the two output terminals shall be equal to or greater than 2V or 50% of the magnitude of V_O, whichever is greater. For the opposite binary state the polarity of VT is reversed ($\overline{VT}$).
3. During transitions of the driver output between alternating binary states the differential voltage measured across 100Ω load shall monotonically change between 0.1 and 0.9 of V_{SS} within 0.1 of the unit interval or 20 ns, whichever is greater. Thereafter, the signal voltage shall not change more than 10% of V_{SS} from the steady state value until the binary state occurs.

B. The Receiver

The electrical characteristics of the receiver are specified in RS-422 as follows:

1. The receiver shall not require a differential input voltage more than 200 mV to correctly assume the intended binary state, over an entire common-mode voltage range of −7 to +7V. The common-mode voltage (V_{CM}) is defined as the algebraic mean of the 2 voltages appearing at the receiver input terminals with respect to the receiver circuit ground. This allows for operations where there are ground differences caused by IR drop and noise of up to ±7V.
2. The receiver shall maintain correct operation for a differential input signal ranging between 200 mV and 6V in magnitude.
3. The maximum voltage between either receiver input terminal and receiver circuit ground shall not exceed 10V (3V signal + 7V common-mode) in magnitude. Also, the receiver shall tolerate a maximum differential signal of 12V applied across its input terminals without being damaged.
4. The total load (up to 10 receivers) shall not have a resistance more than 90Ω at its input points.

DS8921, DS8922 AND DS8923

The DS8921 is a single differential line driver and receiver pair. Whereas, the DS8922 and DS8923 are dual differential line driver and receiver pairs. The difference between the DS8922 and DS8923 is in the TRI-STATE® control.

These devices are designed to meet the full specifications of RS-422. The driver features high source and sink current capability *(Figure 3)*.

The receiver will discriminate a ±200 mV input signal over a full common-mode range of ±7V. Switching noise which may occur on input signal can be eliminated by the built-in hysteresis (50 mV typical, and 15 mV min.). An input fail-safe circuit is provided so that if the receiver inputs are open, the output will assume the logical one state.

These devices have power up/down circuitry will TRI-STATE the outputs and prevents erroneous glitches on the transmission lines during system power up or down operation.

The most attractive feature of these devices is the small skew beween the complementary outputs of the driver, typically about 0.5 ns. This small skew specification is often necessary to meet tight system timing requirements.

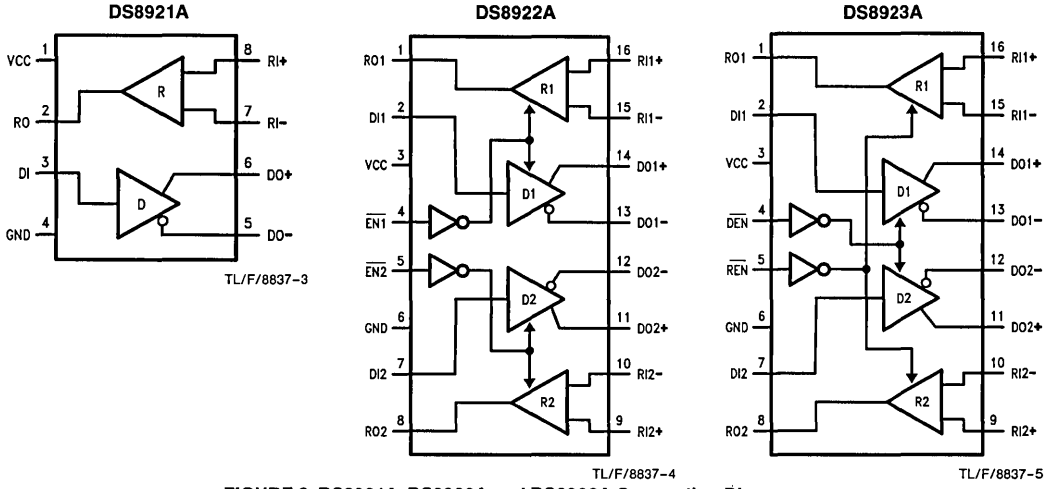
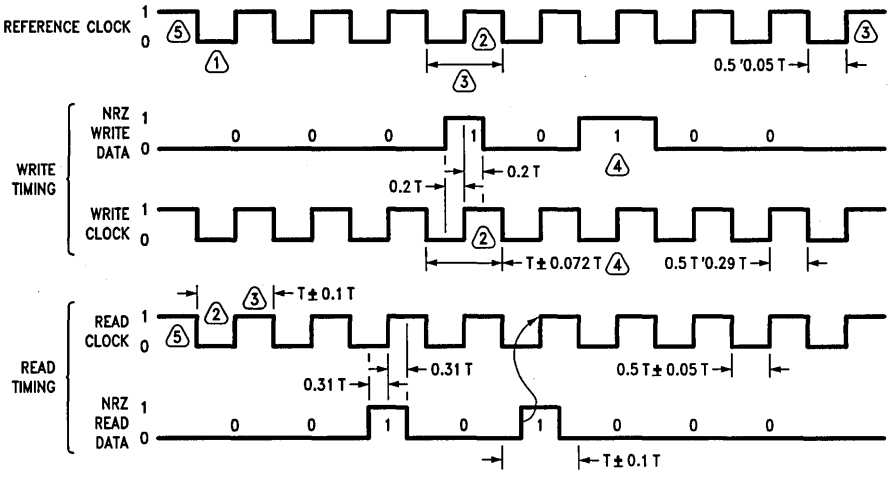


FIGURE 3. DS8921A, DS8922A and DS8923A Connection Diagrams



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Note 1. All times in ns measured at I/O connector of the drive. T is the period of the clock signals and is the inverse of the reference or read clock frequency.

Note 2. Similar period symmetry shall be in ±4 ns between any two adjacent cycles during reading and writing.

Note 3. Except during a head change or PLO synchronization the clock variances for spindle speed and circuit tolerances shall not vary more than −5.5% to +5.0%. Phase relationship between reference clock and NRZ write data or write clock is not defined.

Note 4. The write clock must be the same frequency as the drive supplied reference clock (i.e., the write clock is the controller received and retransmitted drive reference clock).

Note 5. Reference clock is valid when read gate is inactive. Read clock is valid when read gate is active and PLO synchronization has been established.

Note 6. See *Figure 3* for definition of 0 and 1 on these differential signal lines.

FIGURE 4. ESDI Timing Diagrams

DM74AS74 Switching Characteristics

over recommended operating free air temperature range (Note 1). All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Parameter	From	To	Conditions	DM74AS74			Units
				Min	Typ	Max	
F_{MAX}			V_{CC} = 4.5V to 5.5V R_L = 500Ω C_L = 50 pF	105			MHz
T_{PLH}	Preset or clear	Q or Q		3.3		7.5	ns
T_{PHL}				3.5		10.5	ns
T_{PLH}	Clock	Q or Q		3.5		8	ns
T_{PHL}				4.5		9	ns

Note 1: See Section 1 for test waveforms and output load.

FIGURE 5. 1 ns Clock Skew

ESDI ENHANCED SMALL DEVICE INTERFACE

The ESDI specification necessitates the use of National's DS8921A/22A/23A series of transceivers. A look at the specification *Figure 1* will show this. The read and Reference Clock must meet the symmetry specification shown. All specifications are in % T, where $T = \frac{1}{F}$, the ESDI specification is assumed to be a 10 Mbits/second standard, T = 100 ns.

Given this, the negative pulse width measured at the drive connector must equal 0.5T (50 ns) ±0.05T (±5 ns). The best available RS-422 driver, except for the DS8921A Family, is specified at ±4 ns differential skew. If the clock is from a high speed 74AS74 device, shown in *Figure 2*, it will have a typical skew of 1 ns.

This combination of 4 ns +1 ns uses all of the ESDI specified 5 ns and leaves no margin for noise. Use of the DS8921A, 22A, or 23A, specified at ±2.75 ns max. differential skew would allow up to ±2.25 ns for clock skew and noise. This is as close a guarantee to meeting the ±5 ns spec. of ESDI, as is possible with todays advanced testing systems.

One other consideration is the relationship between Read Clock and Read Data. *Figure 1* shows that the positive edge of Read Clock must be 0.31T (31 ns) after the leading edge of Read Data, and 0.31T (31 ns) before the trailing edge of Read Data.

The Read Clock positive edges will be used to strobe Read Data into the controller after both signals go through their respective cable lines and receivers. Use of the DS8922A/23A assures minimum skew between these two signals. Because both drivers, or both receivers, are on the same piece of silicon an optimum match is achieved.

The above is applicable to an ESDI controller as well as the Drive itself. The controller receives the Reference Clock and uses both positive and negative edges to generate WRITE CLOCK. The negative edge of WRITE CLOCK is used to strobe out WRITE DATA and the positive edge will strobe WRITE DATA into the Drive.

The WRITE CLOCK positive edge has to be centered within WRITE DATA after it is received by the drive. The transmitted WRITE CLOCK and WRITE DATA must be as closely matched as possible.

National's DS8921A, 22A, and DS8923A devices offer the combination of tightly spec'd parameters and drivers and receivers on one chip to meet various system timing constraints.

Section 2

Bus Transceivers

Section Contents

*Also available processed to various Military screening levels. Refer to Section 9.

Bus Transceivers

A bus is a common communication medium, such as a cable or a printed circuit trace, that is time shared by several elements of a system. Single-ended bus circuits are listed in this section and these may be further categorized into open-collector circuits and TRI-STATE circuits.

When not transmitting, a bus driver should be capable of presenting a high impedance output in order to allow other drivers to freely use the bus. This is achieved by using either an open-collector or TRI-STATE output.

Open-collector drivers may be connected in a wired-or configuration which is very useful for polling and bus arbitration. These devices require pull-up resistors, which can also serve as bus terminators.

TRI-STATE drivers, on the other hand, do not require bus termination for short bus runs on PC boards. In addition, TRI-STATE devices provide improved rise time characteristics with low power dissipation. Hence, they are popular in high-speed microcomputer systems.

A single-ended bus is highly susceptible to noise, including ground noise and crosstalk. For this reason the bus should not be extended beyond the subsystem's enclosure without special care. Line lengths in excess of 10 feet are not recommended without the use of noise reduction techniques, such as slew rate control, high receiver thresholds and noise filtering. Devices such as National Semiconductor's DS3662 and DS3862 Trapezoidal bus transceivers and DS3896 and DS3897 Future Bus transceivers are specifically designed for reducing crosstalk and noise susceptibility on high-speed buses.

FUTUREBUS TRANSCEIVERS

The DS3896 and DS3897 are the first two devices designed for driving high-speed microcomputer backplane buses. Both devices meet the proposed IEEE-P896 Future Bus standard and incorporate low output capacitance (<5 pF) with the ability to drive a bus with a loaded impedance of less than 18Ω. This excellent drive capability is achieved while still maintaining high levels of noise immunity.

POWER UP/DOWN GLITCH FREE PROTECTION

Powering a device up or down, or simply connecting or disconnecting a device from an active bus, has frequently presented the design engineer with the problem of invalid data glitches being transmitted onto the bus. National Semiconductor is the industry leader in offering bus transceivers incorporating glitch-free power up/down protection. For more detailed information on National Semiconductor's line of bus transceivers, refer to the following Selection Guide and application notes within this section.

BUS CIRCUITS

Data bus circuits are not transmission line circuits in the normal interpretation where the transmission line is electrically long (1/4 wavelength) with respect to the baud rate. Like unbalanced transmission lines, the data transmission is susceptible to common-mode noise, such as ground IR noise and induced reactive noise from crosstalk. A bus is a communications method where many elements of a system time share the same signal (address or data) bus. A bus shouldn't extend out of its subsystem's electronic enclosure without special care. Line length in excess of 10 feet is not recommended without slew rate control. Cables should be in the form of twisted pair or flat cable where a signal wire is alternated with a ground wire.

OPEN-COLLECTOR BUS CIRCUITS

Device Number		Circuits/ Package	Driver/ Receiver/ Transceiver	Bus Driver		Bus Receiver				Comments	Page No.
Commercial 0°C to +70°C	Military −55°C to +125°C			Propagation Delay (ns)	V_{OL} (V)/ I_{OL} (mA)	Propagation Delay (ns)	V_{IL} (V)/ I_{IL} (μA)	V_{IH} (V)/ I_{IH} (μA)	Hysteresis (V)		
DM8131	DM7131	1	Receiver			30	0.95/50	2/50	0.65	6-Bit Bus Comparator	LOGIC
DM8136	DM7136	1	Receiver			30	0.95/50	2/50	0.65	6-Bit Bus Comparator	LOGIC
DS26S10	DS26S10M	4	Transceiver	10	0.8/100	10	1.75/−100	2.25/100			2-34
DS26S11	DS26S11M	4	Transceiver	10	0.8/100	10	1.75/−100	2.25/100		Input to Bus is Non-Inverting	2-34
DS3662		4	Transceiver	30	0.9/100	40	1.50/400	1.9/100		Trapezoidal Transceiver	2-39
DS3862		8	Transceiver							Trapezoidal Transceiver	2-70
DS3890		8	Driver	15						Futurebus Driver	2-76
DS3892		8	Receiver			18				Futurebus Receiver	2-76
DS3893		4	Transceiver	7		8				TURBOTRANSCEIVER	2-82
DS3896		8	Transceiver							Futurebus Transceiver	2-87
DS3897		4	Transceiver							Futurebus Transceiver	2-87
DS3898		8	Repeator	30						Futurebus Repeator	2-76
DS75450	DS55450	2	Driver	20	0.7/300					AND Separate Output Transistors	3-41
DS75451	DS55451	2	Driver	18	0.7/300					AND	3-41
DS75452	DS55452	2	Driver	26	0.7/300					NAND	3-41
DS75453	DS55453	2	Driver	18	0.7/300					OR	3-41
DS75454	DS55454	2	Driver	27	0.7/300					NOR	3-41
DS8640	DS7640	4	Receiver			23	1.2/−50	1.8/50		Quad NOR Receiver	2-107
DS8641	DS7641	4	Transceiver	30	0.7/50	30	1.2/−100	1.8/100			2-109
DS8836	DS7836	4	Receiver			20	1.05/−50	2.65/50	1	Quad NOR Receiver	2-120
DS8837	DS7837	6	Receiver			20	1.05/−50	2.65/50	1		2-122
DS8838	DS7838	4	Transceiver	25	0.8/50	30	1.05/−100	2.65/100	1		2-125

TRI-STATE® BUS CIRCUITS

Device Number		Circuits/ Package	Driver/ Receiver/ Transceiver	Bus Driver			Bus Receiver				Comments	Page No.
Commercial 0°C to +70°C	Military −55°C to +125°C			Propagation Delay Typ (ns)	V_{OL} (V)/ I_{OL} (mA)	V_{OH} (V)/ I_{OH} (mA)	Propagation Delay Typ (ns)	V_{IL} (V)/ I_{IL} (μA)	V_{IH} (V)/ I_{IH} (μA)	Hysteresis (mV)		
DM74S240	DM54S240	4 or 8	Transceiver	4.5	0.55/64	2.4/−3	4.5	0.8/−400	2/50	400	Non-Inverting	LOGIC
DM74S241	DM54S241	4 or 8	Transceiver	6	0.55/64	2.4/−3	6	0.8/−400	2/50	400	Inverting	LOGIC
DM74S940	DM54S940	8	Transceiver	4.5	0.55/64	2.4/−3	4.5	0.8/−400	2/50	400	Non-Inverting	LOGIC
DM74S941	DM54S941	8	Transceiver	6	0.55/64	2.4/−3	6	0.8/−400	2/50	400	Inverting	LOGIC
DP8212	DP8212M	8	Driver	20	0.45/15	3.6/−1					8080 MPU Data Latch and Service Request f/f	6-5
DP8216	DP8216M	4	Transceiver	20	0.6/55	3.6/−1	15	0.95/−250	2/10		8080 MPU Non-Inverting	6-13
DP8226	DP8226M	4	Transceiver	16	0.6/50	3.6/−1	15	0.95/−250	2/10		8080 MPU Inverting	6-13
DP8228	DP8228M	8	Transceiver	30	0.45/10	2.4/−1	20	0.8/−250	2/20		8080 MPU System Bus Controller and Bus Driver	6-24
DP8238	DP8238M	8	Transceiver	30	0.45/10	2.4/−1	20	0.8/−250	2/20		8080 MPU System Bus Controller and Bus Driver	6-24
DP8303A		8	Transceiver	10	0.5/50	3.6/−5	10	0.8/−250	2/80		Bidirectional Inverting	2-6
DP8304B	DP7304B	8	Transceiver	10	0.5/50	3.6/−5	15	0.8/−250	2/80		Bidirectional Non-Inverting IEEE 488	2-11
DP83BC04		8	Transceiver									2-16
DP8307A		8	Transceiver	10	0.5/50	3.6/−5	10	0.8/−250	2/80		Bidirectional Inverting	2-21
DP8308	DP7308	8	Transceiver	11	0.5/50	3.6/−5	15	0.8/−250	2/80		Bidirectional Non-Inverting	2-25
DP83BC08		8	Transceiver									2-29
DS3647		4	Transceiver	8	0.5/50	2.4/−5	7	0.8/−500	2/100		Quad Bidirectional I/O Register	5-32
DS3666		8	Transceiver	20	0.5/48	2.5/−5.2	20	0.8/−100	2/20	400	IEEE 488 GPIB	2-57
DS3667		8	Transceiver	20	0.5/48	2.5/−5.2	20	0.8/−100	2/20	400		2-65
DS75160A		8	Transceiver	20	0.5/48	2.5/−5.2	20	0.8/−100	2/20	400	IEEE 488 GPIB	2-99
DS75161A		8	Transceiver	20	0.5/48	2.5/−5.2	20	0.8/−100	2/20	400	IEEE 488 GPIB	2-99
DS75162A		8	Transceiver	20	0.5/48	2.5/−5.2	20	0.8/−100	2/20	400	IEEE 488 GPIB	2-99
DS8T26A	DS8T26AM	4	Transceiver	14	0.5/48	2.4/−10	14	0.85/−200	2/20		Inverting	2-128
DS8T28	DS8T28M	4	Transceiver	17	0.5/48	2.4/−10	17	0.85/−200	2/20		Non-Inverting	2-128
DS8833	DS7833	4	Transceiver	14	0.5/50	2.4/−10	20	0.8/−40	2/80	400	Non-Inverting TRI-STATE Receiver	2-112
DS8834	DS7834	4	Transceiver	14	0.5/50	2.4/−10	20	0.8/−40	2/80	400	Inverting	2-116
DS8835	DS7835	4	Transceiver	14	0.5/50	2.4/−10	20	0.8/−40	2/80	400	Inverting TRI-STATE Receiver	2-112
DS8839	DS7839	4	Transceiver	14	0.5/50	2.4/−10	20	0.8/−40	2/80	400	Non-Inverting	2-116
DS8940		9	Transceiver		0.5/48	2.5/−15		0.8/−500	2/50		9-Bit Latchable	2-132
DS8941		9	Transceiver		0.5/48	2.5/−15		0.8/−500	2/50		9-Bit Latchable	2-132

Note: Unless otherwise specified, bus circuits listed above are TTL compatible and use 5V supplies.

National Semiconductor Corporation

DP8303A 8-Bit TRI-STATE® Bidirectional Transceiver (Inverting)

General Description

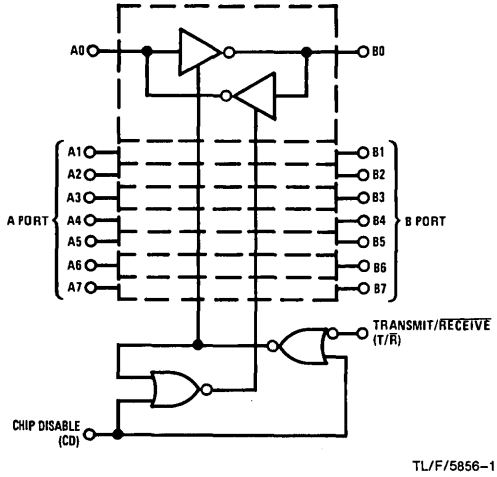
This family of high speed Schottky 8-bit TRI-STATE bidirectional transceivers are designed to provide bidirectional drive for bus oriented microprocessor and digital communications systems. They are all capable of sinking 16 mA on the A ports and 48 mA on the B ports (bus ports). PNP inputs for low input current and an increased output high (V_{OH}) level allow compatibility with MOS, CMOS, and other technologies that have a higher threshold and less drive capabilities. In addition, they all feature glitch-free power up/down on the B port preventing erroneous glitches on the system bus in power up or down.

DP8303A and DP7304B/DP8304B are featured with Transmit/$\overline{\text{Receive}}$ (T/$\overline{\text{R}}$) and Chip Disable (CD) inputs to simplify control logic. For greater design flexibility, DP8307A and DP7308/DP8308 are featured with $\overline{\text{Transmit}}$ ($\overline{\text{T}}$) and $\overline{\text{Receive}}$ ($\overline{\text{R}}$) control inputs.

Features

- 8-bit directional data flow reduces system package count
- Bidirectional TRI-STATE inputs/outputs interface with bus oriented systems
- PNP inputs reduce input loading
- Output high voltage interfaces with TTL, MOS, and CMOS
- 48 mA/300 pF bus drive capability
- Pinouts simplify system interconnections
- Transmit/$\overline{\text{Receive}}$ and chip disable simplify control logic
- Compact 20-pin dual-in-line package
- Bus port glitch free power up/down

Logic and Connection Diagrams



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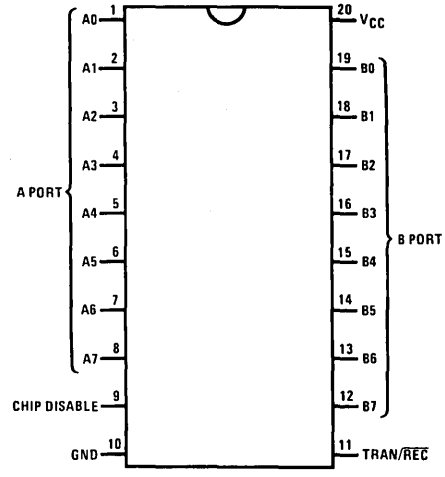
Dual-In-Line Package



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Top View
Order Number DP8303AJ or DP8303AN
See NS Package Number J20A, N20A

Logic Table

Inputs		Resulting Conditions	
Chip Disable	Transmit/$\overline{\text{Receive}}$	A Port	B Port
0	0	OUT	IN
0	1	IN	OUT
1	X	TRI-STATE	TRI-STATE

X = Don't care

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5.5V
Output Voltage	5.5V
Maximum Power Dissipation* at 25°C	
Cavity Package	1667 mW
Molded Package	1832 mW

*Derate cavity package 11.1 mW/°C above 25°C; derate molded package 14.7 mW/°C.

Storage Temperature	−65°C to +150°C
Lead Temperature (soldering, 4 seconds)	260°C

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
DP8303A	4.75	5.25	V
Temperature (T_A)			
DP8303A	0	70	°C

DC Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
A PORT (A0–A7)							
V_{IH}	Logical "1" Input Voltage	CD = V_{IL}, T/$\overline{R}$ = 2.0V		2.0			V
V_{IL}	Logical "0" Input Voltage	CD = V_{IL}, T/$\overline{R}$ = 2.0V				0.7	V
V_{OH}	Logical "1" Output Voltage	CD = T/$\overline{R}$ = V_{IL}, V_{IL} = 0.5V	I_{OH} = −0.4 mA	V_{CC} − 1.15	V_{CC} − 0.7		V
			I_{OH} = −3 mA	2.7	3.95		V
V_{OL}	Logical "0" Output Voltage	CD = T/$\overline{R}$ = V_{IL}, V_{IL} = 0.5V	I_{OL} = 16 mA		0.35	0.5	V
			I_{OL} = 8 mA		0.3	0.4	V
I_{OS}	Output Short Circuit Current	CD = V_{IL}, T/$\overline{R}$ = V_{IL}, V_O = 0V, V_{CC} = Max, (Note 4)		−10	−38	−75	mA
I_{IH}	Logical "1" Input Current	CD = V_{IL}, T/$\overline{R}$ = 2.0V, V_{IH} = 2.7V			0.1	80	μA
I_I	Input Current at Maximum Input Voltage	CD = 2.0V, V_{CC} = Max, V_{IH} = 5.25V				1	mA
I_{IL}	Logical "0" Input Current	CD = V_{IL}, T/$\overline{R}$ = 2.0V, V_{IN} = 0.4V			−70	−200	μA
V_{CLAMP}	Input Clamp Voltage	CD = 2.0V, I_{IN} = −12 mA			−0.7	−1.5	V
I_{OD}	Output/Input TRI-STATE Current	CD = 2.0V	V_{IN} = 0.4V			−200	μA
			V_{IN} = 4.0V			80	μA
B PORT (B0–B7)							
V_{IH}	Logical "1" Input Voltage	CD = V_{IL}, T/$\overline{R}$ = V_{IL}		2.0			V
V_{IL}	Logical "0" Input Voltage	CD = V_{IL}, T/$\overline{R}$ = V_{IL}				0.7	V
V_{OH}	Logical "1" Output Voltage	CD = V_{IL}, T/$\overline{R}$ = 2.0V, V_{IL} = 0.5V	I_{OH} = −0.4 mA	V_{CC} − 1.15	V_{CC} −0.8		V
			I_{OH} = −5 mA	2.7	3.9		V
			I_{OH} = −10 mA	2.4	3.6		V
V_{OL}	Logical "0" Output Voltage	CD = V_{IL}, T/$\overline{R}$ = 2.0V	I_{OL} = 20 mA		0.3	0.4	V
			I_{OL} = 48 mA		0.4	0.5	V
I_{OS}	Output Short Circuit Current	CD = V_{IL}, T/$\overline{R}$ = 2.0V, V_O = 0V, V_{CC} = Max, (Note 4)		−25	−50	−150	mA
I_{IH}	Logical "1" Input Current	CD = V_{IL}, T/$\overline{R}$ = V_{IL}, V_{IH} = 2.7V			0.1	80	μA
I_I	Input Current at Maximum Input Voltage	CD = 2.0V, V_{CC} = Max, V_{IH} = 5.25V				1	mA
I_{IL}	Logical "0" Input Current	CD = V_{IL}, T/$\overline{R}$ = V_{IL}, V_{IN} = 0.4V			−70	−200	μA
V_{CLAMP}	Input Clamp Voltage	CD = 2.0V, I_{IN} = −12 mA			−0.7	−1.5	V
I_{OD}	Output/Input TRI-STATE Current	CD = 2.0V	V_{IN} = 0.4V			−200	μA
			V_{IN} = 0.4V			+200	μA

DC Electrical Charcateristics (Notes 2 and 3) (Continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
CONTROL INPUTS CD, T/$\overline{R}$							
V_{IH}	Logical "1" Input Voltage			2.0			V
V_{IL}	Logical "0" Input Voltage					0.7	V
I_{IH}	Logical "1" Input Current	V_{IH} = 2.7V			0.5	20	μA
I_I	Maximum Input Current	V_{CC} = Max, V_{IH} = 5.25V				1.0	mA
I_{IL}	Logical "0" Input Current	V_{IL} = 0.4V	T/$\overline{R}$		−0.1	−0.25	mA
			CD		−0.25	−0.5	mA
V_{CLAMP}	Input Clamp Voltage	I_{IN} = −12 mA			−0.8	−1.5	V
POWER SUPPLY CURRENT							
I_{CC}	Power Supply Current	CD = 2.0V, V_{IN}, V_{CC} = Max			70	100	mA
		CD = 0.4V, V_{INA} = T/$\overline{R}$ = 2V, V_{CC} = Max			100	150	mA

AC Electrical Characteristics V_{CC} = 5V, T_A = 25°C

Symbol	Parameter	Conditions	Min	Typ	Max	Units
A PORT DATA/MODE SPECIFICATIONS						
t_{PDHLA}	Propagation Delay to a Logical "0" from B Port to A Port	CD = 0.4V, T/$\overline{R}$ = 0.4V *(Figure A)* R1 = 1k, R2 = 5k, C1 = 30 pF		8	12	ns
t_{PDLHA}	Propagation Delay to a Logical "1" from B Port to A Port	CD = 0.4V, T/$\overline{R}$ = 0.4V *(Figure A)* R1 = 1k, R2 = 5k, C1 = 30 pF		11	16	ns
t_{PLZA}	Propagation Delay from a Logical "0" to TRI-STATE from CD to A Port	B0 to B7 = 2.4V, T/$\overline{R}$ = 0.4V *(Figure C)* S3 = 1, R5 = 1k, C4 = 15 pF		10	15	ns
t_{PHZA}	Propagation Delay from a Logical "1" to TRI-STATE from CD to A Port	B0 to B7 = 0.4V, T/$\overline{R}$ = 0.4V *(Figure C)* S3 = 0, R5 = 1k, C4 = 15 pF		8	15	ns
t_{PZLA}	Propagation Delay from TRI-STATE to a Logical "0" from CD to A Port	B0 to B7 = 2.4V, T/$\overline{R}$ = 0.4V *(Figure C)* S3 = 1, R5 = 1k, C4 = 30 pF		20	30	ns
t_{PZHA}	Propagation Delay from TRI-STATE to a Logical "1" from CD to A Port	B0 to B7 = 0.4V, T/$\overline{R}$ = 0.4V *(Figure C)* S3 = 0, R5 = 5k, C4 = 30 pF		19	30	ns
B PORT DATA/MODE SPECIFICATIONS						
t_{PDHLB}	Propagation Delay to a Logical "0" from A Port to B Port	CD = 0.4V, T/$\overline{R}$ = 2.4V *(Figure A)* R1 = 100Ω, R2 = 1k, C1 = 300 pF R1 = 667Ω, R2 = 5k, C1 = 45 pF		12 7	18 12	ns ns
t_{PDLHB}	Propagation Delay to a Logical "1" from A Port to B Port	CD = 0.4V, T/$\overline{R}$ = 2.4V *(Figure A)* R1 = 100Ω, R2 = 1k, C1 = 300 pF R1 = 667Ω, R2 = 5k, C1 = 45 pF		15 9	20 14	ns ns
t_{PLZB}	Propagation Delay from a Logical "0" to TRI-STATE from CD to B Port	A0 to A7 = 2.4V, T/$\overline{R}$ = 2.4V *(Figure C)* S3 = 1, R5 = 1k, C4 = 15 pF		13	18	ns
t_{PHZB}	Propagation Delay from a Logical "1" to TRI-STATE from CD to B Port	A0 to A7 = 0.4V, T/$\overline{R}$ = 2.4V *(Figure C)* S3 = 0, R5 = 1k, C4 = 15 pF		8	15	ns
t_{PLZB}	Propagation Delay from TRI-STATE to a Logical "0" from CD to B Port	A0 to A7 = 2.4V, T/$\overline{R}$ = 2.4V *(Figure C)* S3 = 1, R5 = 100Ω, C4 = 300 pF S3 = 1, R5 = 667Ω, C4 = 45 pF		25 16	35 25	ns ns
t_{PZHB}	Propagation Delay from TRI-STATE to a Logical "1" from CD to B Port	A0 to A7 = 0.4V, T/$\overline{R}$ = 2.4V *(Figure C)* S3 = 0, R5 = 1k, C4 = 300 pF S3 = 0, R5 = 5kΩ, C4 = 45 pF		22 14	35 25	ns ns

AC Electrical Characteristics V_{CC} = 5V, T_A = 25°C (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
TRANSMIT/RECEIVE MODE SPECIFICATIONS						
t_{TRL}	Propagation Delay from Transmit Mode to Receive a Logical "0", T/$\overline{R}$ to A Port	CD = 0.4V *(Figure B)* S1 = 1, R4 = 100Ω, C3 = 5 pF S2 = 1, R3 = 1k, C2 = 30 pF		23	35	ns
t_{TRH}	Propagation Delay from Transmit Mode to Receive a Logical "1", T/$\overline{R}$ to A Port	CD = 0.4V *(Figure B)* S1 = 0, R4 = 100Ω, C3 = 5 pF S2 = 0, R3 = 5k, C2 = 30 pF		23	35	ns
t_{RTL}	Propagation Delay from Receive Mode to Transmit a Logical "0", T/$\overline{R}$ to B Port	CD = 0.4V *(Figure B)* S1 = 1, R4 = 100Ω, C3 = 300 pF S2 = 1, R3 = 300Ω, C2 = 5 pF		23	35	ns
t_{RTH}	Propagation Delay from Receive Mode to Transmit a Logical "1", T/$\overline{R}$ to B Port	CD = 0.4V (*Figure B*) S1 = 0, R4 = 1k, C3 = 300 pF S2 = 0, R3 = 300Ω, C2 = 5 pF		27	35	ns

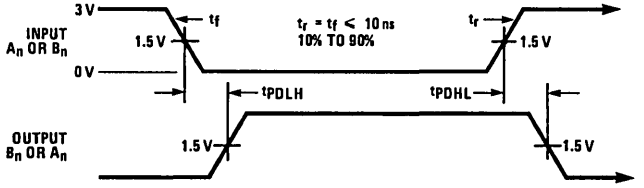
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: Unless otherwise specified, min/max limits apply across the supply and temperature range listed in the table of Recommended Operating Conditions. All typical values given are for V_{CC} = 5V and T_A = 25°C.

Note 3: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified.

Note 4: Only one output at a time should be shorted.

Switching Time Waveforms and AC Test Circuits



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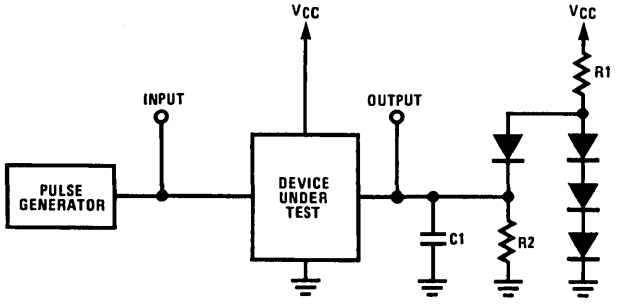

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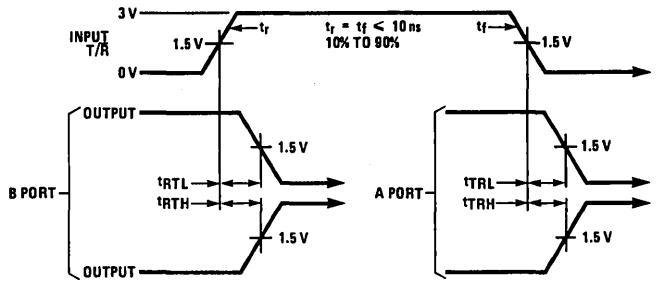
Note: C1 includes test fixture capacitance.

FIGURE A. Propagation Delay from A Port to B Port or from B Port to A Port

Switching Time Waveforms and AC Test Circuits (Continued)



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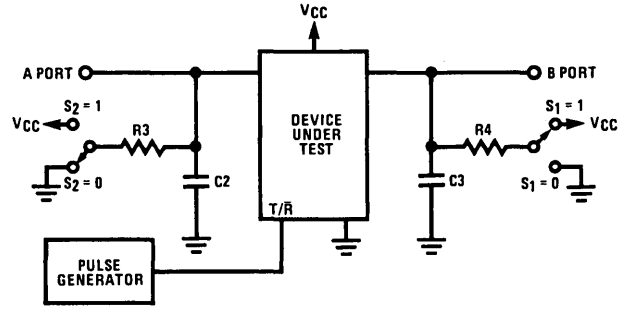

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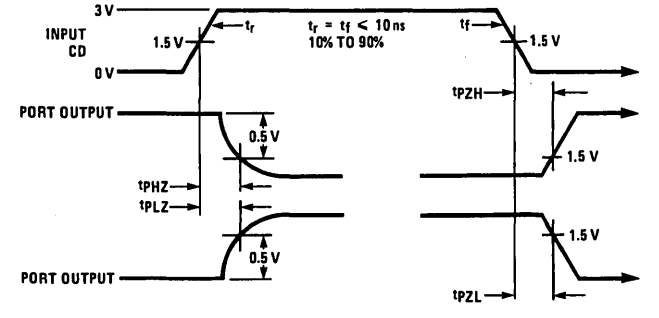
Note: C2 ad C3 include test fixture capacitance.

FIGURE B. Propagation Delay from T/$\overline{R}$ to A Port or B Port



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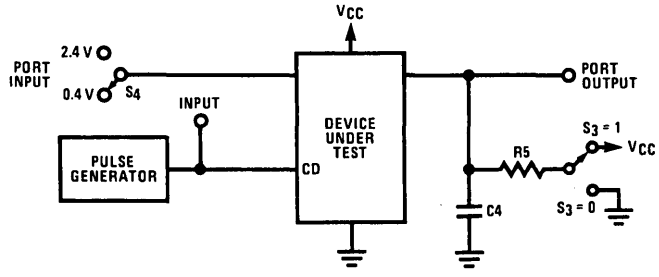


TL/F/5856–8

Note: C4 includes test fixture capacitance. Port input is in a fixed logical condition. See AC table.

FIGURE C. Propagation Delay to/from TRI-STATE from CD to A Port or B Port

National Semiconductor Corporation

DP7304B/DP8304B 8-Bit TRI-STATE® Bidirectional Transceiver (Non-Inverting)

General Description

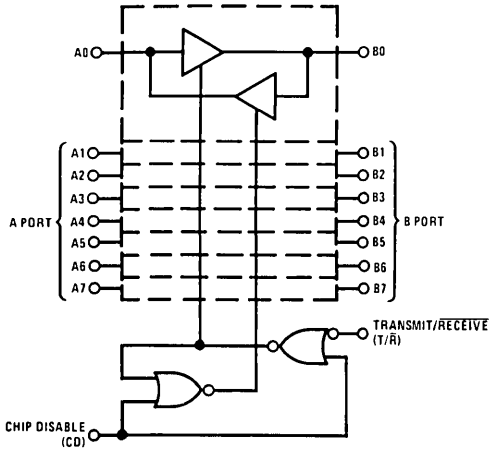
The DP73048B/DP8304B are high speed Schottky 8-bit TRI-STATE bidirectional transceivers designed to provide bidirectional drive for bus oriented microprocessor and digital communications systems. They are all capable of sinking 16 mA on the A ports and 48 mA on the B ports (bus ports). PNP inputs for low input current and an increased output high (V_{OH}) level allow compatibility with MOS, CMOS, and other technologies that have a higher threshold and less drive capabilities. In addition, they all feature glitch-free power up/down on the B port preventing erroneous glitches on the system bus in power up or down.

DP7304B/DP8304B are featured with Transmit/$\overline{\text{Receive}}$ (T/$\overline{\text{R}}$) and Chip Disable (CD) inputs to simplify control logic.

Features

- 8-bit bidirectional data flow reduces system package count
- Bidirectional TRI-STATE inputs/outputs interface with bus oriented systems
- PNP inputs reduce input loading
- Output high voltage interfaces with TTL, MOS, and CMOS
- 48 mA/300 pF bus drive capability
- Pinouts simplify system interconnections
- Transmit/$\overline{\text{Receive}}$ and chip disable simplify control logic
- Compact 20-pin dual-in-line package
- Bus port glitch free power up/down

Logic and Connection Diagrams



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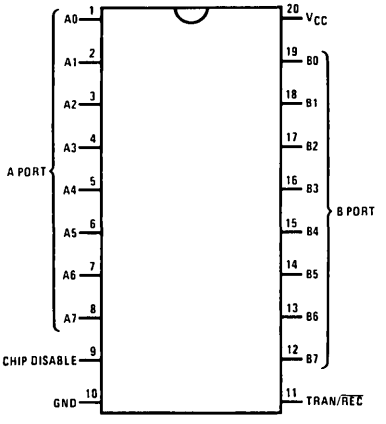
Dual-In-Line Package



TL/F/8793–2

Top View

Order Number DP7304BJ, DP8304BJ, DP8304BN or DP8304BWM

See NS Package Number J20A, N20A or M20B

Logic Table

Inputs		Resulting Conditions	
Chip Disable	Transmit/$\overline{\text{Receive}}$	A Port	B Port
0	0	OUT	IN
0	1	IN	OUT
1	X	TRI-STATE	TRI-STATE

X = Don't Care

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5.5V
Output Voltage	5.5V
Storage Temperature	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1667 mW
Molded Package	1832 mW
Lead Temperature (soldering, 4 sec.)	260°C

*Derate cavity package 11.1 mW/°C above 25°C; derate molded package 14.7 mW/°C above 25°C.

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
DP7304B	4.5	5.5	V
DP8304B	4.75	5.25	V
Temperature (T_A)			
DP7304B	−55	125	°C
DP8304B	0	70	°C

DC Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
A PORT (A0–A7)							
V_{IH}	Logical "1" Input Voltage	CD = V_{IL}, T/$\overline{R}$ = 2.0V		2.0			V
V_{IL}	Logical "0" Input Voltage	CD = V_{IL}, T/$\overline{R}$ = 2.0V	DP8304B			0.8	V
			DP7304B			0.7	V
V_{OH}	Logical "1" Output Voltage	CD = V_{IL}, T/$\overline{R}$ = V_{IL}	I_{OH} = −0.4 mA	V_{CC}−1.15	V_{CC}−0.7		V
			I_{OH} = −3 mA	2.7	3.95		V
V_{OL}	Logical "0" Output Voltage	CD = T/$\overline{R}$ = V_{IL}	I_{OL} = 16 mA (8304B)		0.35	0.5	V
			I_{OL} = 8 mA (both)		0.3	0.4	V
I_{OS}	Output Short Circuit Current	CD = V_{IL}, T/$\overline{R}$ = V_{IL}, V_O = 0V, V_{CC} = max (Note 4)		−10	−38	−75	mA
I_{IH}	Logical "1" Input Current	CD = V_{IL}, T/$\overline{R}$ = 2.0V, V_{IH} = 2.7V			0.1	80	μA
I_I	Input Current at Maximum Input Voltage	CD = 2.0V, V_{CC} = max, V_{IH} = 5.25V				1	mA
I_{IL}	Logical "0" Input Current	CD = V_{IL}, T/$\overline{R}$ = 2.0V, V_{IN} = 0.4V			−70	−200	μA
V_{CLAMP}	Input Clamp Voltage	CD = 2.0V, I_{IN} = −12 mA			−0.7	−1.5	V
I_{OD}	Output/Input TRI-STATE Current	CD = 2.0V	V_{IN} = 0.4V			−200	μA
			V_{IN} = 4.0V			80	μA
B PORT (B0–B7)							
V_{IH}	Logical "1" Input Voltage	CD = V_{IL}, T/$\overline{R}$ = V_{IL}		2.0			V
V_{IL}	Logical "0" Input Voltage	CD = V_{IL}, T/$\overline{R}$ = V_{IL}	DP8304B			0.8	V
			DP7304B			0.7	V
V_{OH}	Logical "1" Output Voltage	CD = V_{IL}, T/$\overline{R}$ = 2.0V	I_{OH} = −0.4 mA	V_{CC}−1.15	V_{CC}−0.8		V
			I_{OH} = −5 mA	2.7	3.9		V
			I_{OH} = −10 mA	2.4	3.6		V
V_{OL}	Logical "0" Output Voltage	CD = V_{IL}, T/$\overline{R}$ = 2.0V	I_{OL} = 20 mA		0.3	0.4	V
			I_{OL} = 48 mA		0.4	0.5	V
I_{OS}	Output Short Circuit Current	CD = V_{IL}, T/$\overline{R}$ = 2.0V, V_O = 0V, V_{CC} = max (Note 4)		−25	−50	−150	mA

DC Electrical Characteristics (Notes 2 and 3) (Continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
B PORT (B0–B7) (Continued)							
I_{IH}	Logical "1" Input Current	CD = V_{IL}, T/$\overline{R}$ = V_{IL}, V_{IH} = 2.7V			0.1	80	μA
I_I	Input Current at Maximum Input Voltage	CD = 2.0V, V_{CC} = max, V_{IH} = 5.25V				1	mA
I_{IL}	Logical "0" Input Current	CD = V_{IL}, T/$\overline{R}$ = V_{IL}, V_{IN} = 0.4V			−70	−200	μA
V_{CLAMP}	Input Clamp Voltage	CD = 2.0V, I_{IN} = −12 mA			−0.7	−1.5	V
I_{OD}	Output/Input TRI-STATE Current	CD = 2.0V	V_{IN} = 0.4V			−200	μA
			V_{IN} = 4.0V			+200	μA
CONTROL INPUTS CD, T/$\overline{R}$							
V_{IH}	Logical "1" Input Voltage			2.0			V
V_{IL}	Logical "0" Input Voltage		DP8304B			0.8	V
			DP7304B			0.7	V
I_{IH}	Logical "1" Input Current	V_{IH} = 2.7V			0.5	20	μA
I_I	Maximum Input Current	V_{CC} = max, V_{IH} = 5.25V				1.0	mA
I_{IL}	Logical "0" Input Current	V_{IL} = 0.4V	T/$\overline{R}$		−0.1	−0.25	mA
			CD		−0.25	−0.5	mA
V_{CLAMP}	Input Clamp Voltage	I_{IN} = −12 mA			−0.8	−1.5	V
POWER SUPPLY CURRENT							
I_{CC}	Power Supply Current	CD = 2.0V, V_{IN} = 0.4V, V_{CC} = max			70	100	mA
		CD = V_{INA} = 0.4V, T/$\overline{R}$ = 2V, V_{CC} = max			90	140	mA

AC Electrical Characteristics V_{CC} = 5V, T_A = 25°C

Symbol	Parameter	Conditions	Min	Typ	Max	Units
A PORT DATA/MODE SPECIFICATIONS						
t_{PDHLA}	Propagation Delay to a Logical "0" from B Port to A Port	CD = 0.4V, T/$\overline{R}$ = 0.4V *(Figure A)* R1 = 1k, R2 = 5k, C1 = 30 pF		14	18	ns
t_{PDLHA}	Propagation Delay to a Logical "1" from B Port to A Port	CD = 0.4V, T/$\overline{R}$ = 0.4V *(Figure A)* R1 = 1k, R2 = 5k, C1 = 30 pF		13	18	ns
t_{PLZA}	Propagation Delay from a Logical "0" to TRI-STATE from CD to A Port	B0 to B7 = 0.4V, T/$\overline{R}$ = 0.4V *(Figure C)* S3 = 1, R5 = 1k, C4 = 15 pF		11	15	ns
t_{PHZA}	Propagation Delay from a Logical "1" to TRI-STATE from CD to A Port	B0 to B7 = 2.4V, T/$\overline{R}$ = 0.4V *(Figure C)* S3 = 0, R5 = 1k, CR = 15 pF		8	15	ns
t_{PZLA}	Propagation Delay from TRI-STATE to a Logical "0" from CD to A Port	B0 to B7 = 0.4V, T/$\overline{R}$ = 0.4V *(Figure C)* S3 = 1, R5 = 1k, C4 = 30 pF		27	35	ns
t_{PZHA}	Propagation Delay from TRI-STATE to a Logical "1" from CD to A Port	B0 to B7 = 2.4V, T/$\overline{R}$ = 0.4V *(Figure C)* S3 = 0, R5 = 5k, C4 = 30 pF		19	25	ns
B PORT DATA/MODE SPECIFICATIONS						
t_{PDHLB}	Propagation Delay to a Logical "0" from A Port to B Port	CD = 0.4V, T/$\overline{R}$ = 2.4V *(Figure A)* R1 = 100Ω, R2 = 1k, C1 = 300 pF R1 = 667Ω, R2 = 5k, C1 = 45 pF		18 11	23 18	ns ns
t_{PDLHB}	Propagation Delay to a Logical "1" from A Port to B Port	CD = 0.4V, T/$\overline{R}$ = 2.4V *(Figure A)* R1 = 100Ω, R2 = 1k, C1 = 300 pF R1 = 667Ω, R2 = 5k, C1 = 45 pF		16 11	23 18	ns ns

AC Electrical Characteristics V_{CC} = 5V, T_A = 25°C (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
B PORT DATA/MODE SPECIFICATIONS (Continued)						
t_{PLZB}	Propagation Delay from a Logical "0" to TRI-STATE from CD to B Port	A0 to A7 = 0.4V, T/$\overline{R}$ = 2.4V *(Figure C)* S3 = 1, R5 = 1k, C4 = 15 pF		13	18	ns
t_{PHZB}	Propagation Delay from a Logical "1" to TRI-STATE from CD to B Port	A0 to A7 = 2.4V, T/$\overline{R}$ = 2.4V *(Figure C)* S3 = 0, R5 = 1k, C4 = 15 pF		8	15	ns
t_{PZLB}	Propagation Delay from TRI-STATE to a Logical "0" from CD to B Port	A0 to A7 = 0.4V, T/$\overline{R}$ = 2.4V *(Figure C)* S3 = 1, R5 = 100Ω, C4 = 300 pF S3 = 1, R5 = 667Ω, C4 = 45 pF		32 16	40 22	ns ns
t_{PZHB}	Propagation Delay from TRI-STATE to a Logical "1" from CD to B Port	A0 to A7 = 2.4V, T/$\overline{R}$ = 2.4V *(Figure C)* S3 = 0, R5 = 1k, C4 = 300 pF S3 = 0, R5 = 5k, C4 = 45 pF		26 14	35 22	ns ns
TRANSMIT/$\overline{\text{RECEIVE}}$ MODE SPECIFICATIONS						
t_{TRL}	Propagation Delay from Transmit Mode to $\overline{\text{Receive}}$ a Logical "0", T/$\overline{R}$ to A Port	CD = 0.4V *(Figure B)* S1 = 0, R4 = 100Ω, C3 = 5 pF S2 = 1, R3 = 1k, C2 = 30 pF		30	40	ns
t_{TRH}	Propagation Delay from Transmit Mode to $\overline{\text{Receive}}$ a Logical "1", T/$\overline{R}$ to A Port	CD = 0.4V, *(Figure B)* S1 = 1, R4 = 100Ω, C3 = 5 pF S2 = 0, R3 = 5k, C2 = 30 pF		28	40	ns
t_{RTH}	Propagation Delay from $\overline{\text{Receive}}$ Mode to Transmit a Logical "1", T/$\overline{R}$ to B Port	CD = 0.4V *(Figure B)* S1 = 0, R4 = 1k, C3 = 300 pF S2 = 1, R3 = 300Ω, C2 = 5 pF		28	40	ns

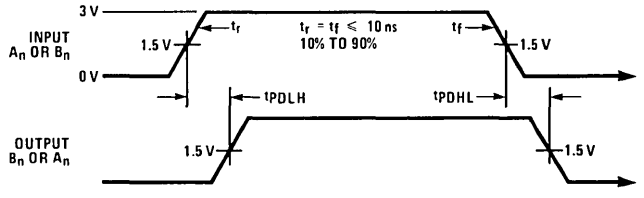
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: Unless otherwise specified, min/max limits apply across the supply and temperature range listed in the table of Recommended Operating Conditions. All typical values given are for V_{CC} = 5V and T_A = 25°C.

Note 3: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified.

Note 4: Only one output at a time should be shorted.

Switching Time Waveforms and AC Test Circuits



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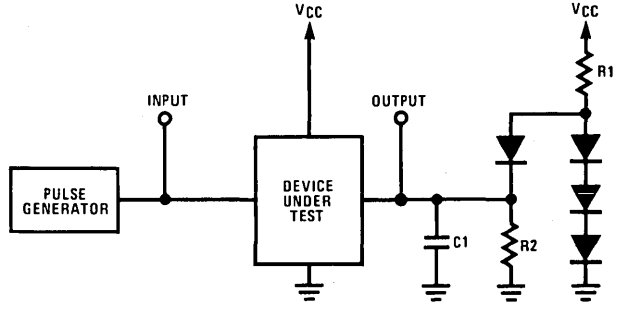
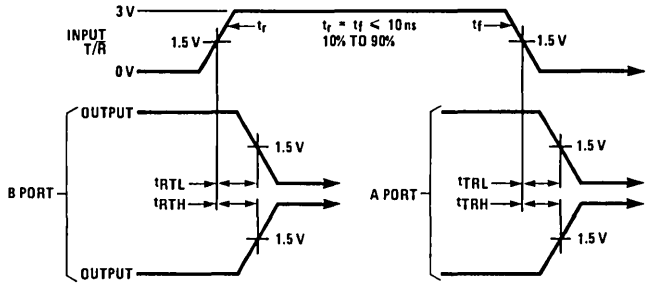


TL/F/8793-4

Note: C1 includes test fixture capacitance.

FIGURE A. Propagation Delay from A Port to B Port or from B Port to A Port

Switching Time Waveforms and AC Test Circuits (Continued)



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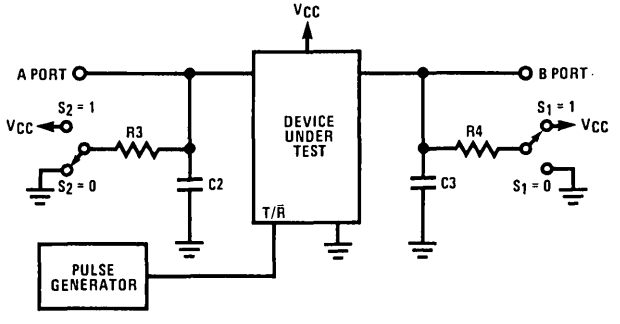
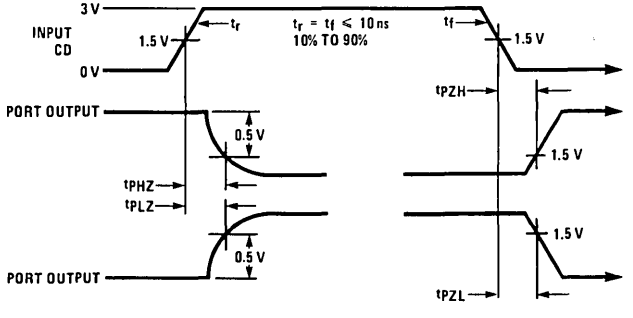


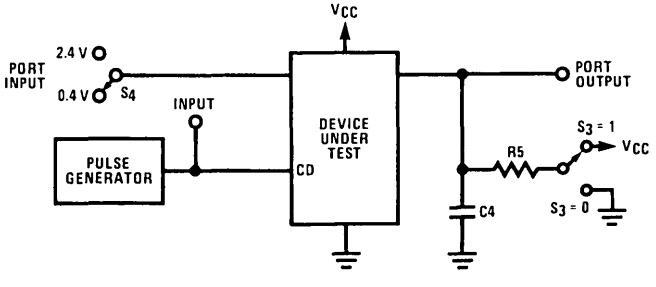
TL/F/8793–6

Note: C2 and C3 include test fixture capacitance.

FIGURE B. Propagation Delay from T/$\overline{R}$ to A Port or B Port



TL/F/8793–7



TL/F/8793–8

Note: C4 includes test fixture capacitance.

Port input is in a fixed logical condition. See AC table.

FIGURE C. Propagation Delay to/from TRI-STATE from CD to A Port or B Port

National Semiconductor Corporation

PRELIMINARY

DP83BC04 8-Bit TRI-STATE® Bidirectional Transceiver (Non-Inverting)

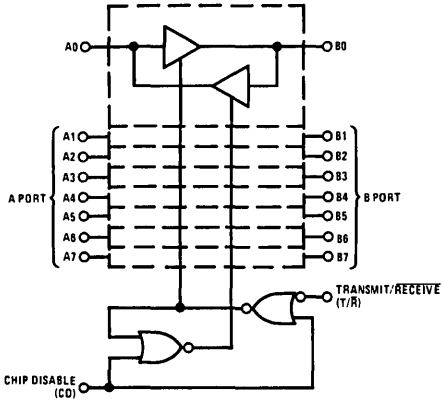
General Description

The DP83BC04 is a Bipolar-CMOS 8-bit TRI-STATE bidirectional transceiver (non-inverting), designed to provide bidirectional drive for bus oriented microprocessor and digital communication systems. It is capable of sinking 16 mA on the A ports and 48 mA on the B ports (bus ports). PNP transistors are used for low input currents and an increased output high (V_{OH}) level allows compatibility with MOS, CMOS, and other technologies that have a higher threshold and less drive capability. In addition it features glitch free power up/down on the B port, preventing erroneous glitches on the system bus.

Features

- 8-bit bidirectional data flow reduces system package count
- Bidirectional TRI-STATE inputs/outputs interface with bus oriented systems
- 5 mA maximum ICC in TRI-STATE mode
- 40 mA maximum ICC in active mode
- PNP inputs reduce input loading
- Output high voltage interfaces with TTL, MOS, and CMOS
- 48 mA/300 pF bus drive capability
- Pinouts simplify system interconnections
- Transmit/$\overline{\text{Receive}}$ and chip disable simplify control logic
- Compact 20-pin dual-in-line package
- Bus port glitch free power up/down

Logic and Connection Diagrams



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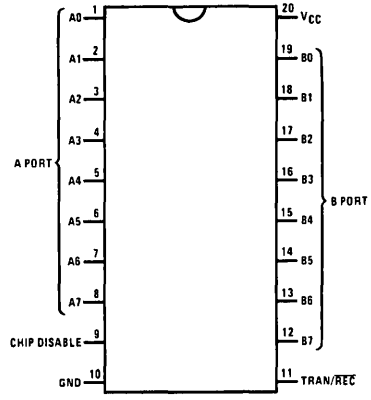
Dual-In-Line Package



Top View

TL/F/8626–2

Order Number DP83BC04BJ
or DP83BC04BN
See NS Package Number J20A or N20A

Logic Table

Inputs		Resulting Conditions	
Chip Disable	Transmit/$\overline{\text{Receive}}$	A Port	B Port
0	0	OUT	IN
0	1	IN	OUT
1	X	TRI-STATE	TRI-STATE

X = Don't care

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5.5V
Output Voltage	5.5V
Storage Temperature	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1667 mW
Molded Package	1832 mW
Lead Temperature (soldering, 4 seconds)	260°C

*Derate cavity package 11.1 mW/°C above 25°C; derate molded package 14.7 mW/°C above 25°C.

Recommended Operating Conditions

	Min	Max
Supply Voltage (V_{CC})		
DP83BC04	4.75	5.25
Temperature (T_A)		
DP83BC04	0	70

DC Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
A PORT (A0–A7)							
V_{IH}	Logical "1" Input Voltage	CD = V_{IL}, T/$\overline{R}$ = 2.0V		2.0			V
V_{IL}	Logical "0" Input Voltage	CD = V_{IL}, T/$\overline{R}$ = 2.0V	DP83BC04			0.8	V
V_{OH}	Logical "1" Output Voltage	CD = V_{IL}, T/$\overline{R}$ = V_{IL}	I_{OH} = −0.4 mA	V_{CC}−1.15	V_{CC}−0.7		V
			I_{OH} = −3 mA	2.7	3.95		V
V_{OL}	Logical "0" Output Voltage	CD = T/$\overline{R}$ = V_{IL}	I_{OL} = 16 mA		0.35	0.5	V
			I_{OL} = 8 mA		0.3	0.4	V
I_{OS}	Output Short Circuit Current	CD = V_{IL}, T/$\overline{R}$ = V_{IL}, V_O = 0V, V_{CC} = Max. (Note 4)		−10	−38	−75	mA
I_{IH}	Logical "1" Input Current	CD = V_{IL}, T/$\overline{R}$ = 2.0V, V_{IH} = 2.7V			0.1	80	μA
I_I	Input Current at Maximum Input Voltage	CD = 2.0V, V_{CC} = Max, V_{IH} = 5.25V				1	mA
I_{IL}	Logical "0" Input Current	CD = V_{IL}, T/$\overline{R}$ = 2.0V, V_{IN} = 0.4V			−70	−200	μA
V_{CLAMP}	Input Clamp Voltage	CD = 2.0V, I_{IN} = −12 mA			−0.7	−1.5	V
I_{OD}	Output/Input TRI-STATE Current	CD = 2.0V	V_{IN} = 0.4V			−200	μA
			V_{IN} = 4.0V			80	μA
B PORT (B0–B7)							
V_{IH}	Logical "1" Input Voltage	CD = V_{IL}, T/$\overline{R}$ = V_{IL}		2.0			V
V_{IL}	Logical "0" Input Voltage	CD = V_{IL}, T/$\overline{R}$ = V_{IL}	DP83BC04			0.8	V
V_{OH}	Logical "1" Output Voltage	CD = V_{IL}, T/$\overline{R}$ = 2.0V	I_{OH} = −0.4 mA	V_{CC}−1.15	V_{CC}−0.8		V
			I_{OH} = −5 mA	2.7	3.9		V
			I_{OH} = −10 mA	2.4	3.6		V
V_{OL}	Logical "0" Output Voltage	CD = V_{IL}, T/$\overline{R}$ = 2.0V	I_{OL} = 20 mA		0.3	0.4	V
			I_{OL} = 48 mA		0.4	0.5	V
I_{OS}	Output Short Circuit Current	CD = V_{IL}, T/$\overline{R}$ = 2.0V, V_O = 0V, V_{CC} = Max, (Note 4)		−25	−50	−150	mA
I_{IH}	Logical "1" Input Current	CD = V_{IL}, T/$\overline{R}$ = V_{IL}, V_{IH} = 2.7V			0.1	80	μA
I_I	Input Current at Maximum Input Voltage	CD = 2.0V, V_{CC} = Max, V_{IH} = 5.25V				1	mA
I_{IL}	Logical "0" Input Current	CD = V_{IL}, T/$\overline{R}$ = V_{IL}, V_{IN} = 0.4V			−70	−200	μA
V_{CLAMP}	Input Clamp Voltage	CD = 2.0V, I_{IN} = −12 mA			−0.7	−1.5	V
I_{OD}	Output/Input TRI-STATE Current	CD = 2.0V	V_{IN} = 0.4V			−200	μA
			V_{IN} = 4.0V			+200	μA

DC Electrical Characteristics (Notes 2 and 3) (Continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
CONTROL INPUTS CD, T/$\overline{R}$							
V_{IH}	Logical "1" Input Voltage			2.0			V
V_{IL}	Logical "0" Input Voltage		DP83BC04			0.8	V
I_{IH}	Logical "1" Input Current	V_{IH} = 2.7V			0.5	20	μA
I_I	Maximum Input Current	V_{CC} = Max, V_{IH} = 5.25V				1.0	mA
I_{IL}	Logical "0" Input Current	V_{IL} = 0.4V	T/$\overline{R}$		−0.1	−0.25	mA
			CD		−0.25	−0.5	mA
V_{CLAMP}	Input Clamp Voltage	I_{IN} = −12 mA			−0.8	−1.5	V
POWER SUPPLY CURRENT							
I_{CC}	Power Supply Current	CD = 2.0V, V_{IN} = 0.4V, V_{CC} = Max			5		mA
		CD = V_{INA} = 0.4V, T/$\overline{R}$ = 2V, V_{CC} = Max			40		mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DP83BC04B and across the 0°C to +70°C range for the DP73BC04B. All typical values are for T_A = 25°C and V_{CC} = 5V.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min or absolute value basis.

AC Electrical Characteristics V_{CC} = 5V, T_A = 25°C

Symbol	Parameter	Conditions	Min	Typ	Max	Units
A Port Data/Mode Specification (*Figure A*)						
t_{PDHLA}	Propagation Delay to a Logical "0" from B Port to A Port	CD = 0.4V, T/$\overline{R}$ = 0.4V, R1 = 1k, C1 = 50 pF S1 = 0, S2 = X, S3 = 0, S4 = 0, S5 = 2		8.5		ns
t_{PDLHA}	Propagation Delay to a Logical "1" from B Port to A Port	CD = 0.4V, T/$\overline{R}$ = 0.4V, R1 = 1k, C1 = 50 pF S1 = 0, S2 = X, S3 = 0, S4 = 0, S5 = 2		10		ns
t_{PCDLZA}	Propagation Delay from "0" to TRI-STATE from CD to A Port	B0–B7 = 0.4V, T/$\overline{R}$ = 0.4V, R1 = 1k, C1 = 50 pF S1 = 1, S2 = 1, S3 = 1, S4 = 0, S5 = 0		15.5		ns
t_{PCDHZA}	Propagation Delay from "1" to TRI-STATE from CD to A Port	B0–B7 = 2.4V, T/$\overline{R}$ = 0.4V, R1 = 1k, C1 = 50 pF S1 = 1, S2 = 0, S3 = 1, S4 = 0, S5 = 1		14		ns
t_{PCDZLA}	Propagation Delay from TRI-STATE to "0" from CD to A Port	B0–B7 = 0.4V, T/$\overline{R}$ = 0.4V, R1 = 1k, C1 = 50 pF S1 = 1, S2 = 1, S3 = 1, S4 = 0, S5 = 0		26		ns
t_{PCDZHA}	Propagation Delay from TRI-STATE to "1" from CD to A Port	B0–B7 = 2.4V, T/$\overline{R}$ = 0.4V, R1 = 1k, C1 = 50 pF S1 = 1, S2 = 0, S3 = 1, S4 = 0, S5 = 1		32		ns
t_{PTRLZA}	Propagation Delay from "0" to TRI-STATE from T/$\overline{R}$ to A Port	B0–B7 = 0.4V, CD = 0.4V, R1 = 1k, C1 = 50 pF S1 = 1, S2 = 1, S3 = 0, S4 = 1, S5 = 0		16.5		ns
t_{PTRHZA}	Propagation Delay from "1" to TRI-STATE from T/$\overline{R}$ to A Port	B0–B7 = 2.4V, CD = 0.4V, R1 = 1k, C1 = 50 pF S1 = 1, S2 = 0, S3 = 0, S4 = 1, S5 = 1		15		ns
t_{PTRZLA}	Propagation Delay from TRI-STATE to "0" from T/$\overline{R}$ to A Port	B0–B7 = 0.4V, CD = 0.4V, R1 = 1k, C1 = 50 pF S1 = 1, S2 = 1, S3 = 0, S4 = 1, S5 = 0		27		ns
t_{TPRZHA}	Propagation Delay from TRI-STATE to "1" from T/$\overline{R}$ to A Port	B0–B7 = 2.4V, CD = 0.4V, R1 = 1k, C1 = 50 pF S1 = 1, S2 = 0, S3 = 0, S4 = 1, S5 = 1		33		ns

AC Electrical Characteristics V_{CC} = 5V, T_A = 25°C (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
B PORT DATA/MODE SPECIFICATION (*FIGURE B*)						
t_{PDHLB}	Propagation Delay to a Logical "0" from A Port to B Port	CD = 0.4V T/$\overline{R}$ = 2.4V, R2 = 150Ω, R3 = 100Ω, C2 = 300 pF, S6 = 0, S7 = 1, S8 = 0, S9 = 2		11		ns
t_{PDLHB}	Propagation Delay to a Logical "1" from A Port to B Port	CD = 0.4, T/$\overline{R}$ = 2.4V, R2 = 150Ω, R3 = 100Ω, C2 = 300 pF, S6 = 0, S7 = 1, S8 = 0, S9 = 2		18.5		ns
t_{PCDLZB}	Propagation Delay from "0" to TRI-STATE from CD to B Port	A0–A7 = 0.4V, T/$\overline{R}$ = 2.5V, R2 = 150Ω, R3 = 100Ω, C2 = 300 pF, S6 = 1, S7 = 1, S8 = 1, S9 = 0		15.5		ns
t_{PCDHZB}	Propagation Delay from "1" to TRI-STATE from CD to B Port	A0–A7 = 2.4V, T/$\overline{R}$ = 2.5V, R2 = 150Ω, R3 = 100Ω, C2 = 300 pF, S6 = 0, S7 = 1, S8 = 1, S9 = 1		13.5		ns
t_{PCDZLB}	Propagation Delay from TRI-STATE "0" from CD to B Port	A0–A7 = 0.4V, T/$\overline{R}$ = 2.5V, R2 = 150Ω, R3 = 100Ω, C2 = 300 pF, S6 = 1, S7 = 1, S8 = 1, S9 = 0		25		ns
t_{PCDZHB}	Propagation Delay from TRI-STATE to "1" from CD to B Port	A0–A7 = 2.5V, T/$\overline{R}$ = 2.5V, R2 = 150Ω, R3 = 100Ω, C2 = 300 pF, S6 = 0, S7 = 1, S8 = 1, S9 = 1		36		ns
t_{PTRLZB}	Propagation Delay from "0" to TRI-STATE from T/$\overline{R}$ to B Port	A0–A7 = 0.4V, CD = 0.4V, R2 = 150Ω, R3 = 100Ω, C2 = 300 pF, S6 = 1, S7 = 0, S8 = 0, S9 = 0		22		ns
t_{PTRHZB}	Propagation Delay from "1" to TRI-STATE from T/$\overline{R}$ to B Port	A0–A7 = 2.5V, CD = 0.4V, R2 = 150Ω, R3 = 100Ω, C2 = 300 pF, S6 = 0, S7 = 0, S8 = 0, S9 = 1		23		ns
t_{PTRZLB}	Propagation Delay from TRI-STATE to "0" from T/$\overline{R}$ to B Port	A0–A7 = 0.4V, CD = 0.4V, R2 = 150Ω, R3 = 100Ω, C2 = 300 pF, S6 = 1, S7 = 0, S8 = 0, S9 = 0		48		ns
t_{PTRZHB}	Propagation Delay from TRI-STATE to "1" from T/$\overline{R}$ to B Port	A0–A7 = 2.5V, CD = 0.4V, R2 = 150Ω, R3 = 100Ω, C2 = 300 pF, S6 = 0, S7 = 0, S8 = 0, S9 = 1		53		ns

Test Circuit

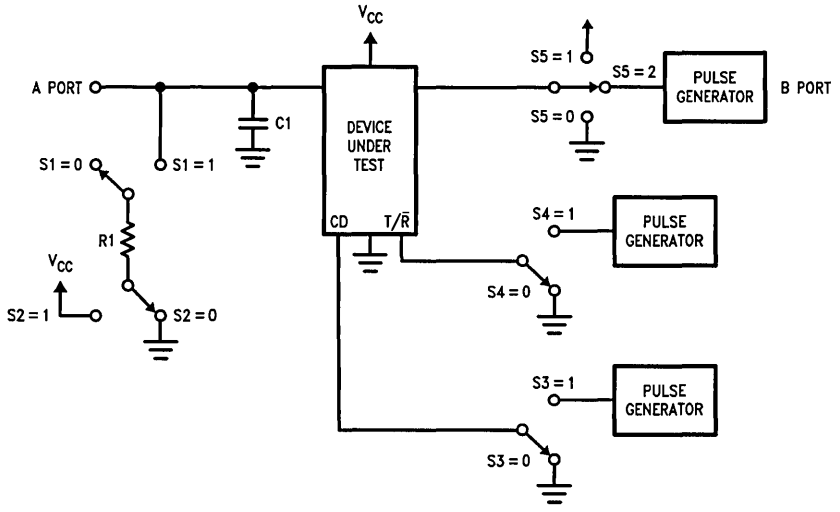


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FIGURE A. A Port Test Load

Test Circuit (Continued)

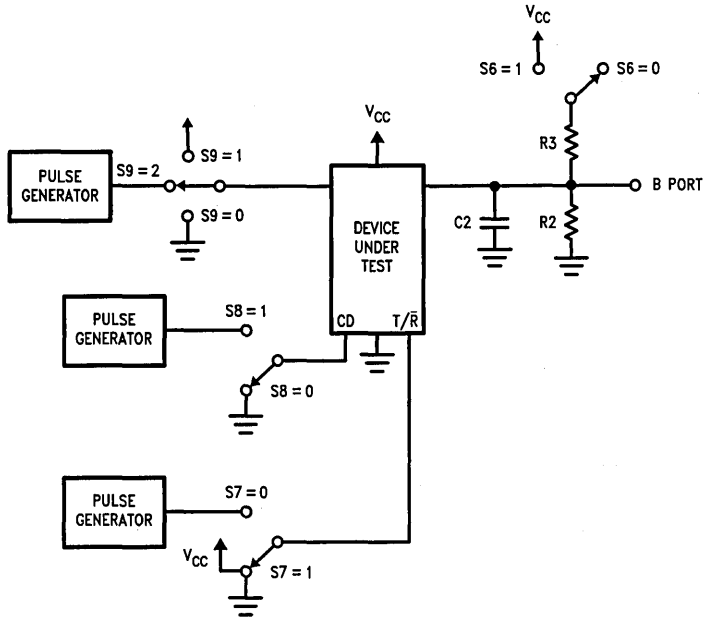

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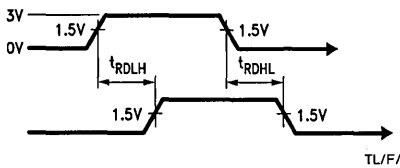
FIGURE B. B Port Test Load

Timing Waveforms

Data Path Delays:



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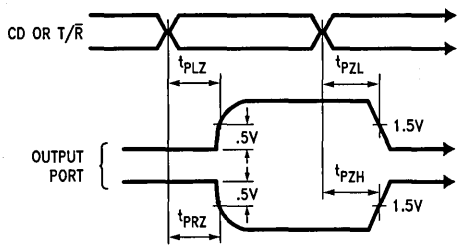

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FIGURE C

National Semiconductor Corporation

DP8307A 8-Bit TRI-STATE® Bidirectional Transceiver (Inverting)

General Description

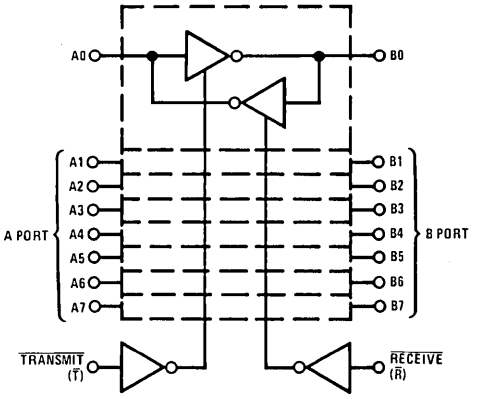
The DP8307A is a high speed Schottky 8-bit TRI-STATE bidirectional transceiver designed to provide bidirectional drive for bus oriented microprocessor and digital communications systems. It is capable of sinking 16 mA on the A ports and 48 mA on the B ports (bus ports). PNP inputs for low input current and an increased output high (V_{OH}) level allow compatibility with MOS, CMOS, and other technologies that have a higher threshold and less drive capabilities. In addition, it features glitch-free power up/down on the B port preventing erroneous glitches on the system bus in power up or down.

DP8303A and DP7304B/DP8304B are featured with Transmit/$\overline{\text{Receive}}$ (T/$\overline{\text{R}}$) and Chip Disable (CD) inputs to simplify control logic. For greater design flexibility, DP8307A and DP7308/DP8308 is featured with $\overline{\text{Transmit}}$ ($\overline{\text{T}}$) and $\overline{\text{Receive}}$ ($\overline{\text{R}}$) control inputs.

Features

- 8-bit bidirectional data flow reduces system package count
- Bidirectional TRI-STATE inputs/outputs interface with bus oriented systems
- PNP inputs reduce input loading
- Output high votlage interfaces with TTL, MOS, and CMOS
- 48 mA/300 pF bus drive capability
- Pinouts simplify system interconnections
- Independent $\overline{\text{T}}$ and $\overline{\text{R}}$ controls for versatility
- Compact 20-pin dual-in-line package
- Bus port glitch free power up/down

Logic and Connection Diagrams



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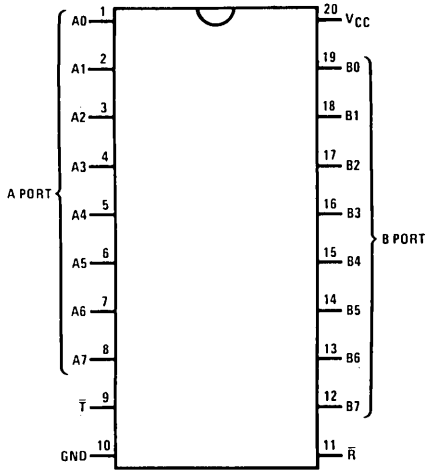
Dual-In-Line Package



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Top View

Order Number DP8307AJ or DP8307AN
See NS Package Number J20A or N20A

Logic Table

Control Inputs		Resulting Conditions	
$\overline{\text{Transmit}}$	$\overline{\text{Receive}}$	A Port	B Port
1	0	OUT	IN
0	1	IN	OUT
1	1	TRI-STATE	TRI-STATE
0	0	Both Active*	

*This is not an intended logic condition and may cause oscillations.

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5.5V
Output Voltage	5.5V
Maximum Power Dissipation* at 25°C	
Cavity Package	1667 mW
Molded Package	1832 mW

*Derate cavity package 11.1 mW/°C above 25°C; derate molded package 14.7 mW/°C above 25°C.

Lead Temperature (soldering, 4 sec.)	260°C
Storage Temperature	−65°C to +150°C

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.75	5.25	V
Temperature (T_A)	0	70	°C

DC Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
A PORT (A0–A7)							
V_{IH}	Logical "1" Input Voltage	$\overline{T} = V_{IL}, \overline{R} = 2.0V$		2.0			V
V_{IL}	Logical "0" Input Voltage	$\overline{T} = V_{IL}, \overline{R} = 2.0V$				0.7	V
V_{OH}	Logical "1" Output Voltage	$\overline{T} = 2.0V, \overline{R} = V_{IL}$, $V_{IL} = 0.5V$	$I_{OH} = -0.4$ mA	$V_{CC} - 1.15$	$V_{CC} - 0.7$		V
			$I_{OH} = -3$ mA	2.7	3.95		V
V_{OL}	Logical "0" Output Voltage	$\overline{T} = 2.0V$, $\overline{R} = V_{IL}$	$I_{OL} = 16$ mA		0.35	0.5	V
			$I_{OL} = 8$ mA		0.3	0.4	V
I_{OS}	Output Short Circuit Current	$\overline{T} = 2.0V, \overline{R} = V_{IL}, V_O = 0V$, V_{CC} = max, (Note 4)		−10	−38	−75	mA
I_{IH}	Logical "1" Input Current	$\overline{T} = V_{IL}, \overline{R} = 2.0V, V_{IH} = 2.7V$			0.1	80	μA
I_I	Input Current at Maximum Input Voltage	$\overline{R} = \overline{T} = 2.0V, V_{CC}$ = max, $V_{IH} = 5.25V$				1	mA
I_{IL}	Logical "0" Input Current	$\overline{T} = V_{IL}, \overline{R} = 2.0V, V_{IN} = 0.4V$			−70	−200	μA
V_{CLAMP}	Input Clamp Voltage	$\overline{T} = \overline{R} = 2.0V, I_{IN} = -12$ mA			−0.7	−1.5	V
I_{OD}	Output/Input TRI-STATE Current	$\overline{T} = \overline{R} = 2.0V$	$V_{IN} = 0.4V$			−200	μA
			$V_{IN} = 4.0V$			80	μA
B PORT (B0–B7)							
V_{IH}	Logical "1" Input Voltage	$\overline{T} = 2.0V, \overline{R} = V_{IL}$		2.0			V
V_{IL}	Logical "0" Input Voltage	$\overline{T} = 2.0V, \overline{R} = V_{IL}$				0.7	V
V_{OH}	Logical "1" Output Voltage	$\overline{T} = V_{IL}, \overline{R} = 2.0V$, $V_{IL} = 0.5V$	$I_{OH} = -0.4$ mA	$V_{CC} - 1.15$	$V_{CC} - 0.8$		V
			$I_{OH} = -5$ mA	2.7	3.9		V
			$I_{OH} = -10$ mA	2.4	3.6		V
V_{OL}	Logical "0" Output Voltage	$\overline{T} = V_{IL}, \overline{R} = 2.0V$	$I_{OL} = 20$ mA		0.3	0.4	V
			$I_{OL} = 48$ mA		0.4	0.5	V
I_{OS}	Output Short Circuit Current	$\overline{T} = V_{IL}, \overline{R} = 2.0V, V_O = 0V$, V_{CC} = max, (Note 4)		−25	−50	−150	mA
I_{IH}	Logical "1" Input Current	$\overline{T} = 2.0V, \overline{R} = V_{IL}, V_{IH} = 2.7V$			0.1	80	μA
I_I	Input Current at Maximum Input Voltage	$\overline{T} = \overline{R} = 2.0V, V_{CC}$ = max, $V_{IH} = 5.25V$				1	mA
I_{IL}	Logical "0" Input Current	$\overline{T} = 2.0V, \overline{R} = V_{IL}, V_{IN} = 0.4V$			−70	−200	μA
V_{CLAMP}	Input Clamp Voltage	$\overline{T} = \overline{R} = 2.0V, I_{IN} = -12$ mA			−0.7	−1.5	V
I_{OD}	Output/Input TRI-STATE Current	$\overline{T} = \overline{R} = 2.0V$	$V_{IN} = 0.4V$			−200	μA
			$V_{IN} = 4.0V$			+200	μA

DC Electrical Characteristics (Notes 2 and 3) (Continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
CONTROL INPUTS $\overline{T}$, $\overline{R}$							
V_{IH}	Logical "1" Input Voltage			2.0			V
V_{IL}	Logical "0" Input Voltage					0.7	V
I_{IH}	Logical "1" Input Current	V_{IH} = 2.7V			0.5	20	μA
I_I	Maximum Input Current	V_{CC} = max, V_{IH} = 5.25V				1.0	mA
I_{IL}	Logical "0" Input Current	V_{IL} = 0.4V	$\overline{R}$		−0.1	−0.25	mA
			$\overline{T}$		−0.25	−0.5	mA
V_{CLAMP}	Input Clamp Voltage	I_{IN} = −12 mA			−0.8	−1.5	V
POWER SUPPLY CURRENT							
I_{CC}	Power Supply Current	$\overline{T}$ = $\overline{R}$ = 2.0V, V_{IN} = 2.0V, V_{CC} = max			70	100	mA
		$\overline{T}$ = 0.4V, V_{INA} = $\overline{R}$ = 2V, V_{CC} = max			100	150	mA

AC Electrical Characteristics V_{CC} = 5V, T_A = 25°C

Symbol	Parameter	Conditions	Min	Typ	Max	Units
A PORT DATA/MODE SPECIFICATIONS						
t_{PDHLA}	Propagation Delay to a Logical "0" from B Port to A Port	$\overline{T}$ = 2.4V, $\overline{R}$ = 0.4V *(Figure A)* R1 = 1k, R2 = 5k, C1 = 30 pF		8	12	ns
t_{PDLHA}	Propagation Delay to a Logical "1" from B Port to A Port	$\overline{T}$ = 2.4V, $\overline{R}$ = 0.4V *(Figure A)* R1 = 1k, R2 = 5k, C1 = 30 pF		11	16	ns
t_{PLZA}	Propagation Delay from a Logical "0" to TRI-STATE from $\overline{R}$ to A Port	B0 to B7 = 2.4V, $\overline{T}$ = 2.4V *(Figure B)* S3 = 1, R5 = 1k, C4 = 15 pF		10	15	ns
t_{PHZA}	Propagation Delay from a Logical "1" to TRI-STATE from $\overline{R}$ to A Port	B0 to B7 = 0.4V, $\overline{T}$ = 2.4V *(Figure B)* S3 = 0, R5 = 1k, C4 = 15 pF		8	15	ns
t_{PZLA}	Propagation Delay from TRI-STATE to a Logical "0" from $\overline{R}$ to A Port	B0 to B7 = 2.4V, $\overline{T}$ = 2.4V *(Figure B)* S3 = 1, R5 = 1k, C4 = 30 pF		25	35	ns
t_{PZHA}	Propagation Delay from TRI-STATE to a Logical "1" from $\overline{R}$ to A Port	B0 to B7 = 0.4V, $\overline{T}$ = 2.4V *(Figure B)* S3 = 0, R5 = 5k, C4 = 30 pF		24	35	ns
B PORT DATA/MODE SPECIFICATIONS						
t_{PDHLB}	Propagation Delay to a Logical "0" from A Port to B Port	$\overline{T}$ = 0.4V, $\overline{R}$ = 2.4V *(Figure A)* R1 = 100Ω, R2 = 1k, C1 = 300 pF R1 = 667Ω, R2 = 5k, C1 = 45 pF		 12 8	 18 12	 ns ns
t_{PDLHB}	Propagation Delay to a Logical "1" from A Port to B Port	$\overline{T}$ = 0.4V, $\overline{R}$ = 2.4V *(Figure A)* R1 = 100Ω, R2 = 1k, C1 = 300 pF R1 = 667Ω, R2 = 5k, C1 = 45 pF		 15 9	 23 14	 ns ns
t_{PLZB}	Propagation Delay from a Logical "0" to TRI-STATE from $\overline{T}$ to B Port	A0 to A7 = 2.4V, $\overline{R}$ = 2.4V *(Figure B)* S3 = 1, R5 = 1k, C4 = 15 pF		13	18	ns
t_{PHZB}	Propagation Delay from a Logical "1" to TRI-STATE from $\overline{T}$ to B Port	A0 to A7 = 0.4V, $\overline{R}$ = 2.4V *(Figure B)* S3 = 0, R5 = 1k, C4 = 15 pF		8	15	ns
t_{PZLB}	Propagation Delay from TRI-STATE to a Logical "0" from $\overline{T}$ to B Port	A0 to A7 = 2.4V, $\overline{R}$ = 2.4V *(Figure B)* S3 = 1, R5 = 100Ω, C4 = 300 pF S3 = 1, R5 = 667Ω, C4 = 45 pF		 32 18	 40 25	 ns ns
t_{PZHB}	Propagation Delay from TRI-STATE to a Logical "1" from $\overline{T}$ to B Port	A0 to A7 = 0.4V, $\overline{R}$ = 2.4V *(Figure B)* S3 = 0, R5 = 1k, C4 = 300 pF S3 = 0, R5 = 5k, C4 = 45 pF		 25 16	 35 25	 ns ns

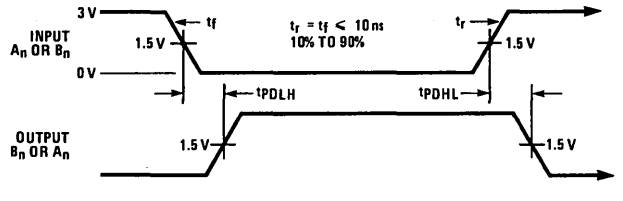
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: Unless otherwise specified, min/max limits apply across the supply and temperature range listed in the table of Recommended Operating Conditions. All typical values given are for V_{CC} = 5V and T_A = 25°C.

Note 3: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified.

Note 4: Only one output at a time should be shorted.

Switching Time Waveforms and AC Test Circuits



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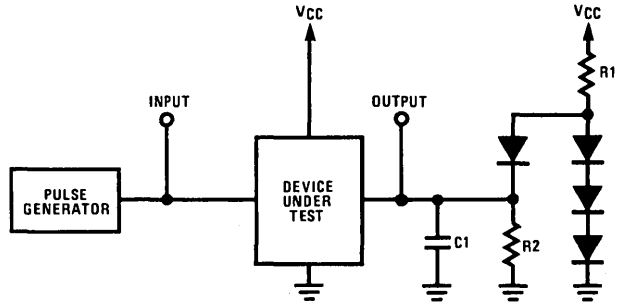

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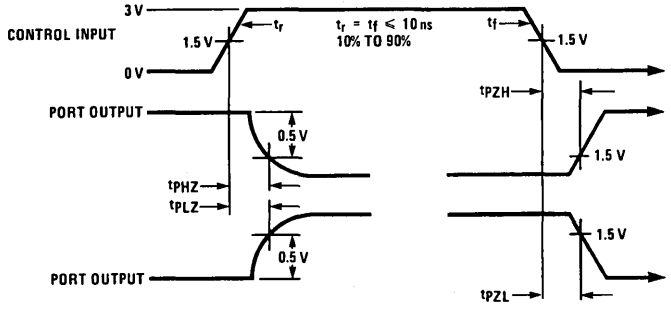
Note: C1 includes test fixture capacitance.

FIGURE A. Propagation Delay from A Port to B Port or from B Port to A Port



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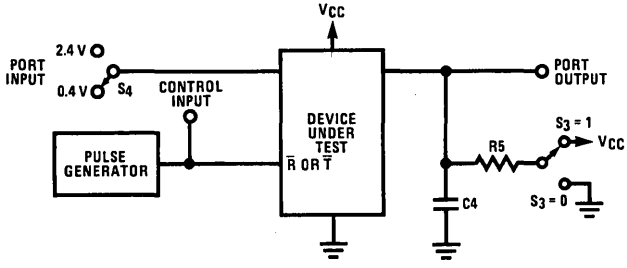

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Note: C4 includes test fixture capacitance. Port input is in a fixed logical condition. See AC Table.

FIGURE B. Propagation Delay to/from TRI-STATE from $\overline{R}$ to A Port and $\overline{T}$ to B Port

National Semiconductor Corporation

DP7308/DP8308 8-Bit TRI-STATE® Bidirectional Transceiver (Non-Inverting)

General Description

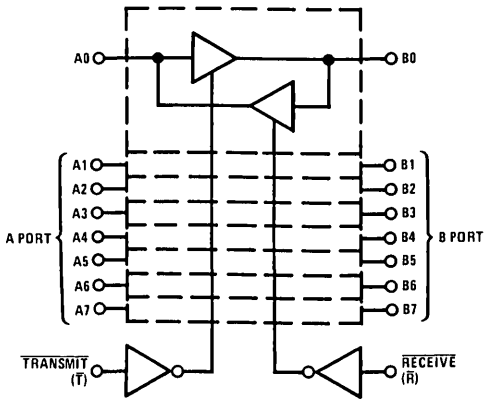
The DP7308/DP8308 are high speed Schottky 8-bit TRI-STATE bidirectional transceivers designed to provide bidirectional drive for bus oriented microprocessor and digital communications systems. They are all capable of sinking 16 mA on the A ports and 48 mA on the B ports (bus ports). PNP inputs for low input current and an increased output high (V_{OH}) level allow compatibility with MOS, CMOS, and other technologies that have a higher threshold and less drive capabilities. In addition, they all feature glitch-free power up/down on the B port preventing erroneous glitches on the system bus in power up or down.

DP7308/DP8308 are featured with $\overline{\text{Transmit}}$ ($\overline{T}$) and $\overline{\text{Receive}}$ ($\overline{R}$) control inputs.

Features

- 8-bit bidirectional data flow reduces system package count
- Bidirectional TRI-STATE inputs/outputs interface with bus oriented systems
- PNP inputs reduce input loading
- Output high voltage interfaces with TTL, MOS, and CMOS
- 48 mA/300 pF bus drive capability
- Pinouts simplify system interconnections
- Independent $\overline{T}$ and $\overline{R}$ controls for versatility
- Compact 20-pin dual-in-line package
- Bus port glitch free power up/down

Logic and Connection Diagrams



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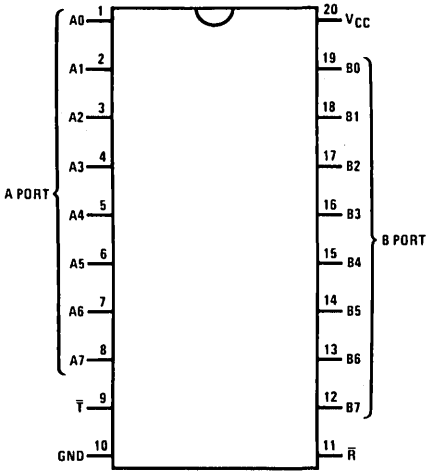
Dual-In-Line Package



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Top View

Order Number DP7308J, DP8308J or DP8308N

See NS Package Number J20A or N20A

Logic Table

Control Inputs		Resulting Conditions	
$\overline{\text{Transmit}}$	$\overline{\text{Receive}}$	A Port	B Port
1	0	OUT	IN
0	1	IN	OUT
1	1	TRI-STATE	TRI-STATE
0	0	Both Active*	

*This is not an intended logic condition and may cause oscillations.

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5.5V
Output Voltage	5.5V
Storage Temperature	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1667 mW
Molded Package	1832 mW
Lead Temperature (soldering, 4 sec.)	260°C

*Derate cavity package 11.1 mW/°C above 25°C; derate molded package 14.7 mW/°C above 25°C.

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
DP7308	4.5	5.5	V
DP8308	4.75	5.25	V
Temperature (T_A)			
DP7308	−55	+125	°C
DP8308	0	+70	°C

DC Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
A PORT (A0–A7)							
V_{IH}	Logical "1" Input Voltage	$\overline{T} = V_{IL}, \overline{R} = 2.0V$		2.0			V
V_{IL}	Logical "0" Input Voltage	$\overline{T} = V_{IL}, \overline{R} = 2.0V$	DP8308			0.8	V
			DP7308			0.7	V
V_{OH}	Logical "1" Output Voltage	$\overline{T} = 2.0V, \overline{R} = V_{IL}$	$I_{OH} = -0.4$ mA	$V_{CC}-1.15$	$V_{CC}-0.7$		V
			$I_{OH} = -3$ mA	2.7	3.95		V
V_{OL}	Logical "0" Output Voltage	$\overline{T} = 2.0V$, $\overline{R} = V_{IL}$	$I_{OL} = 16$ mA (8308)		0.35	0.5	V
			$I_{OL} = 8$ mA (both)		0.3	0.4	V
I_{OS}	Output Short Circuit Current	$\overline{T} = 2.0V, \overline{R} = V_{IL}, V_O = 0V$, V_{CC} = max (Note 4)		−10	−38	−75	mA
I_{IH}	Logical "1" Input Current	$\overline{T} = V_{IL}, \overline{R} = 2.0V, V_{IH} = 2.7V$			0.1	80	μA
I_I	Input Current at Maximum Input Voltage	$\overline{R} = \overline{T} = 2.0V, V_{CC}$ = max, $V_{IH} = 5.25V$				1	mA
I_{IL}	Logical "0" Input Current	$\overline{T} = V_{IL}, \overline{R} = 2.0V, V_{IN} = 0.4V$			−70	−200	μA
V_{CLAMP}	Input Clamp Voltage	$\overline{T} = \overline{R} = 2.0V, I_{IN} = -12$ mA			−0.7	−1.5	V
I_{OD}	Output/Input TRI-STATE Current	$\overline{T} = \overline{R} = 2.0V$	$V_{IN} = 0.4V$			−200	μA
			$V_{IN} = 4.0V$			80	μA
B PORT (B0–B7)							
V_{IH}	Logical "1" Input Voltage	$\overline{T} = 2.0V, \overline{R} = V_{IL}$		2.0			V
V_{IL}	Logical "0" Input Voltage	$\overline{T} = 2.0V, \overline{R} = V_{IL}$	DP8308			0.8	V
			DP7308			0.7	V
V_{OH}	Logical "1" Output Voltage	$\overline{T} = V_{IL}, \overline{R} = 2.0V$	$I_{OH} = -0.4$ mA	$V_{CC}-1.15$	$V_{CC}-0.8$		V
			$I_{OH} = -5$ mA	2.7	3.9		V
			$I_{OH} = -10$ mA	2.4	3.6		V
V_{OL}	Logical "0" Output Voltage	$\overline{T} = V_{IL}, \overline{R} = 2.0V$	$I_{OL} = 20$ mA		0.3	0.4	V
			$I_{OL} = 48$ mA		0.4	0.5	V
I_{OS}	Output Short Circuit Current	$\overline{T} = V_{IL}, \overline{R} = 2.0V, V_O = 0V$, V_{CC} = max (Note 4)		−25	−50	−150	mA
I_{IH}	Logical "1" Input Current	$\overline{T} = 2.0V, \overline{R} = V_{IL}, V_{IH} = 2.7V$			0.1	80	μA
I_I	Input Current at Maximum Input Voltage	$\overline{T} = \overline{R} = 2.0V, V_{CC}$ = max, $V_{IH} = 5.25V$				1	mA
I_{IL}	Logical "0" Input Current	$\overline{T} = 2.0V, \overline{R} = V_{IL}, V_{IN} = 0.4V$			−70	−200	μA
V_{CLAMP}	Input Clamp Voltage	$\overline{T} = \overline{R} = 2.0V, I_{IN} = -12$ mA			−0.7	−1.5	V
I_{OD}	Output/Input TRI-STATE Current	$\overline{T} = \overline{R} = 2.0V$	$V_{IN} = 0.4V$			−200	μA
			$V_{IN} = 4.0V$			+200	μA

DC Electrical Characteristics (Notes 2 and 3) (Continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
CONTROL INPUTS $\overline{T}$, $\overline{R}$							
V_{IH}	Logical "1" Input Voltage			2.0			V
V_{IL}	Logical "0" Input Voltage		DP8308			0.8	V
			DP7308			0.7	V
I_{IH}	Logical "1" Input Current	V_{IH} = 2.7V			0.5	20	μA
I_I	Maximum Input Current	V_{CC} = max, V_{IH} = 5.25V				1.0	mA
I_{IL}	Logical "0" Input Current	V_{IL} = 0.4V	$\overline{R}$		−0.1	−0.25	mA
			$\overline{T}$		−0.25	−0.5	mA
V_{CLAMP}	Input Clamp Voltage	I_{IN} = −12 mA			−0.8	−1.5	V
POWER SUPPLY CURRENT							
I_{CC}	Power Supply Current	$\overline{T}$ = $\overline{R}$ = 2.0V, V_{IN} = 0.4V, V_{CC} = max			70	100	mA
		$\overline{T}$ = V_{INA} = 0.4V, $\overline{R}$ = 2V, V_{CC} = max			90	140	mA

AC Electrical Characteristics V_{CC} = 5V, T_A = 25°C

Symbol	Parameter	Conditions	Min	Typ	Max	Units
A PORT DATA/MODE SPECIFICATIONS						
t_{PDHLA}	Propagation Delay to a Logical "0" from B Port to A Port	$\overline{T}$ = 2.4V, $\overline{R}$ = 0.4V *(Figure A)* R1 = 1k, R2 = 5k, C1 = 30 pF		14	18	ns
t_{PDLHA}	Propagation Delay to a Logical "1" from B Port to A Port	$\overline{T}$ = 2.4V, $\overline{R}$ = 0.4V *(Figure A)* R1 = 1k, R2 = 5k, C1 = 30 pF		13	18	ns
t_{PLZA}	Propagation Delay from a Logical "0" to TRI-STATE from $\overline{R}$ to A Port	B0 to B7 = 0.4V, $\overline{T}$ = 2.4V *(Figure B)* S3 = 1, R5 = 1k, C4 = 15 pF		11	15	ns
t_{PHZA}	Propagation Delay from a Logical "1" to TRI-STATE from $\overline{R}$ to A Port	B0 to B7 = 2.4V, $\overline{T}$ = 2.4V *(Figure B)* S3 = 0, R5 = 1k, C4 = 15 pF		8	15	ns
t_{PZLA}	Propagation Delay from TRI-STATE to a Logical "0" from $\overline{R}$ to A Port	B0 to B7 = 0.4V, $\overline{T}$ = 2.4V *(Figure B)* S3 = 1, R5 = 1k, C4 = 30 pF		24	35	ns
t_{PZHA}	Propagation Delay from TRI-STATE to a Logical "1" from $\overline{R}$ to A Port	B0 to B7 = 2.4V, $\overline{T}$ = 2.4V *(Figure B)* S3 = 0, R5 = 5k, C4 = 30 pF		21	30	ns
B PORT DATA/MODE SPECIFICATIONS						
t_{PDHLB}	Propagation Delay to a Logical "0" from A Port to B Port	$\overline{T}$ = 0.4V, $\overline{R}$ = 2.4V *(Figure A)* R1 = 100Ω, R2 = 1k, C1 = 300 pF R1 = 667Ω, R2 = 5k, C1 = 45 pF		18 11	23 18	ns ns
t_{PDLHB}	Propagation Delay to a Logical "1" from A Port to B Port	$\overline{T}$ = 0.4V, $\overline{R}$ = 2.4V *(Figure A)* R1 = 100Ω, R2 = 1k, C1 = 300 pF R1 = 667Ω, R2 = 5k, C1 = 45 pF		16 11	23 18	ns ns
t_{PLZB}	Propagation Delay from a Logical "0" to TRI-STATE from $\overline{T}$ to B Port	A0 to A7 = 0.4V, $\overline{R}$ = 2.4V *(Figure B)* S3 = 1, R5 = 1k, C4 = 15 pF		13	18	ns
t_{PHZB}	Propagation Delay from a Logical "1" to TRI-STATE from $\overline{T}$ to B Port	A0 to A7 = 2.4V, $\overline{R}$ = 2.4V *(Figure B)* S3 = 0, R5 = 1k, C4 = 15 pF		8	15	ns
t_{PZLB}	Propagation Delay from TRI-STATE to a Logical "0" from $\overline{T}$ to B Port	A0 to A7 = 0.4V, $\overline{R}$ = 2.4V *(Figure B)* S3 = 1, R5 = 100Ω, C4 = 300 pF S3 = 1, R5 = 667Ω, C4 = 45 pF		25 17	35 25	ns ns
t_{PZHB}	Propagation Delay from TRI-STATE to a Logical "1" from $\overline{T}$ to B Port	A0 to A7 = 2.4V, $\overline{R}$ = 2.4V *(Figure B)* S3 = 0, R5 = 1k, C4 = 300 pF S3 = 0, R5 = 5k, C4 = 45 pF		24 17	35 25	ns ns

AC Electrical Characteristics (Continued)

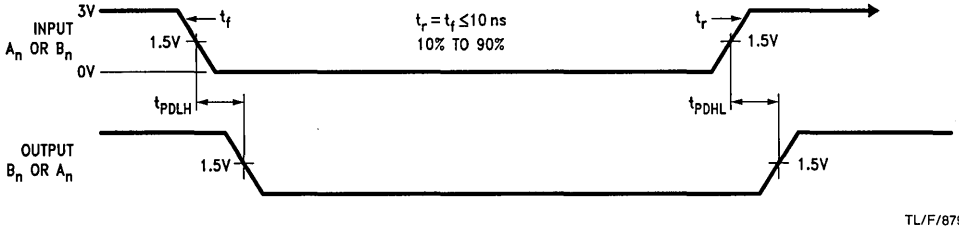
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified, min/max limits apply across the supply and temperature range listed in the table of Recommended Operating Conditions. All typical values given are for V_{CC} = 5V and T_A = 25°C.

Note 3: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified.

Note 4: Only one output at a time should be shorted.

Switching Time Waveforms and AC Test Circuits



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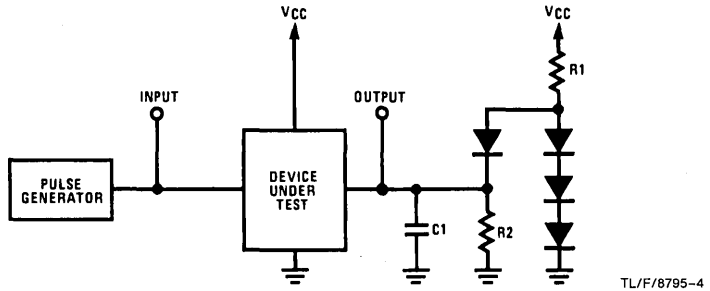

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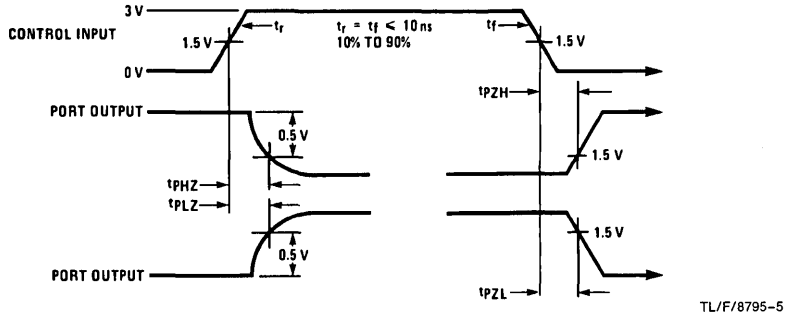
Note: C1 includes test fixture capacitance.

FIGURE A. Propagation Delay from A Port to B Port or from B Port to A Port



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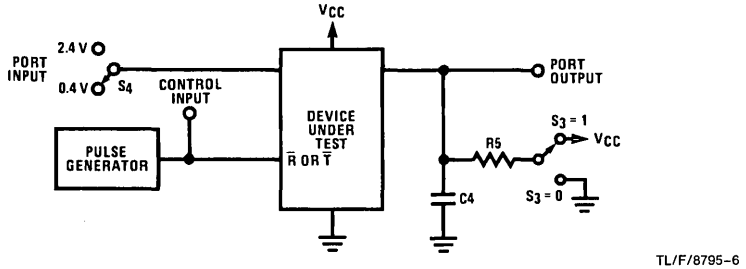

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Note: C4 includes test fixture capacitance. Port input is in a fixed logical condition. See AC Table.

FIGURE B. Propagation Delay to/from TRI-STATE from $\overline{R}$ to A Port and $\overline{T}$ to B Port

National Semiconductor Corporation

PRELIMINARY

DP83BC08 8-Bit TRI-STATE® Bidirectional Transceiver (Non-Inverting)

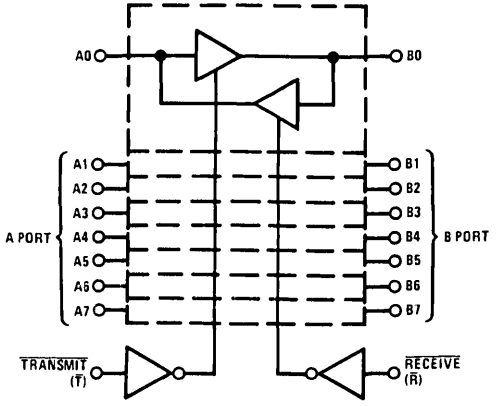
General Description

The DP83BC08 is a Bipolar/CMOS 8-bit TRI-STATE bidirectional transceiver (non-inverting), designed to provide bidirectional drive for bus oriented microprocessor and digital communication systems. It is capable of sinking 16 mA on the A ports and 48 mA on the B ports (bus ports). PNP transistors are used for low input currents and an increased output high (V_{OH}) level allows compatibility with MOS, CMOS, and other technologies that have a higher threshold and less drive capability. In addition it features glitch free power up/down on the B port, preventing erroneous glitches on the system bus.

Features

- 8-bit bidirectional data flow reduces system package count
- Bidirectional TRI-STATE inputs/outputs interface with bus oriented systems
- 5 mA maximum I_{CC} in TRI-STATE mode
- 40 mA maximum I_{CC} in ACTIVE mode
- PNP inputs reduce input loading
- Output high voltage interfaces with TTL, MOS, and CMOS
- 48 mA/300 pF bus drive capability
- Pinouts simplify system interconnections
- Independent $\overline{T}$ and $\overline{R}$ controls for versatility
- Compact 20-pin dual-in-line package
- Bus port glitch free power up/down

Logic and Connection Diagrams



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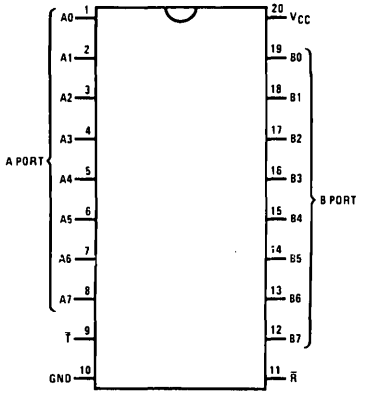
Dual-In-Line Package



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Top View
Order Number DP83BC08J
or DP83BC08N
See NS Package Number J20A or N20A

Logic Table

Control Inputs		Resulting Conditions	
$\overline{\text{Transmit}}$	$\overline{\text{Receive}}$	A Port	B Port
1	0	OUT	IN
0	1	IN	OUT
1	1	TRI-STATE	TRI-STATE
0	0	Both Active*	

* This is not an intended logic condition and may cause oscillations.

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5.5V
Output Voltage	5.5V
Storage Temperature	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1667 mW
Molded Package	1832 mW
Lead Temp. (Soldering, 4 seconds)	260°C

*Derate cavity package 11.1 mW/°C above 25°C; derate molded package 14.7 mW/°C above 25°C.

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
DP83BC08	4.75	5.25	V
Temperature (T_A)			
DP83BC08	0	70	°C

DC Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
A PORT (A0–A7)							
V_{IH}	Logical "1" Input Voltage	$\overline{T} = V_{IL}$, $\overline{R}$ = 2.0V		2.0			V
V_{IL}	Logical "0" Input Voltage	$\overline{T} = V_{IL}$ $\overline{R}$ = 2.0V	DP83BC08			0.8	V
V_{OH}	Logical "1" Output Voltage	$\overline{T}$ = 2.0V, $\overline{R} = V_{IL}$	I_{OH} = −0.4 mA	V_{CC} − 1.15	V_{CC} − 0.7		V
			I_{OH} = −3 mA	2.7	3.95		V
V_{OL}	Logical "0" Output Voltage	$\overline{T}$ = 2.0V, $\overline{R} = V_{IL}$	I_{OL} = 16 mA		0.35	0.5	V
			I_{OL} = 8 mA		0.3	0.4	V
I_{OS}	Output Short Circuit Current	$\overline{T}$ = 2.0V, $\overline{R} = V_{IL}$, V_O = 0V, V_{CC} = max, Note 4		−10	−38	−75	mA
I_{IH}	Logical "1" Input Current	$\overline{T} = V_{IL}$, $\overline{R}$ = 2.0V, V_{IH} = 2.7V			0.1	80	μA
I_I	Input Current at Maximum Input Voltage	$\overline{R} = \overline{T}$ = 2.0V, V_{CC} = max, V_{IH} = 5.25V				1	mA
I_{IL}	Logical "0" Input Current	$\overline{T} = V_{IL}$, $\overline{R}$ = 2.0V, V_{IN} = 0.4V			−70	−200	μA
V_{CLAMP}	Input Clamp Voltage	$\overline{T} = \overline{R}$ = 2.0V, I_{IN} = −12 mA			−0.7	−1.5	V
I_{OD}	Output/Input TRI-STATE Current	$\overline{T} = \overline{R}$ = 2.0V	V_{IN} 0.4V			−200	μA
			V_{IN} = 4.0V			80	μA
B PORT (B0–B7)							
V_{IH}	Logical "1" Input Voltage	$\overline{T}$ = 2.0V, $\overline{R} = V_{IL}$		2.0			V
V_{IL}	Logical "0" Input Voltage	$\overline{T}$ = 2.0V, $\overline{R} = V_{IL}$	DP83BC08			0.8	V
V_{OH}	Logical "1" Output Voltage	$\overline{T} = V_{IL}$, $\overline{R}$ = 2.0V	I_{OH} = −0.4 mA	V_{CC} − 1.15	V_{CC} − 0.8		V
			I_{OH} = −5 mA	2.7	3.9		V
			I_{OH} = −10 mA	2.4	3.6		V
V_{OL}	Logical "0" Output Voltage	$\overline{T} = V_{IL}$, $\overline{R}$ = 2.0V	I_{OL} = 20 mA		0.3	0.4	V
			I_{OL} = 48 mA		0.4	0.5	V
I_{OS}	Output Short Circuit Current	$\overline{T} = V_{IL}$, $\overline{R}$ = 2.0V, V_O = 0V, V_{CC} = max, Note 4		−25	−50	−150	mA
I_{IH}	Logical "1" Input Current	$\overline{T}$ = 2.0V, $\overline{R} = V_{IL}$, V_{IH} = 2.7V			0.1	80	μA
I_I	Input Current at Maximum Input Voltage	$\overline{T} = \overline{R}$ = 2.0V, V_{CC} = max, V_{IH} = 5.25V				1	mA
I_{IL}	Logical "0" Input Current	$\overline{T}$ = 2.0V, $\overline{R} = V_{IL}$, V_{IN} = 0.4V			−70	−200	μA
V_{CLAMP}	Input Clamp Voltage	$\overline{T} = \overline{R}$ = 2.0V, I_{IN} = − 12 mA			−0.7	−1.5	V
I_{OD}	Output/Input TRI-STATE Current	$\overline{T} = \overline{R}$ = 2.0V	V_{IN} = 0.4V			−200	μA
			V_{IN} = 4.0V			+200	μA

DC Electrical Characteristics (Notes 2 and 3) (Continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
CONTROL INPUTS $\overline{T}$, $\overline{R}$							
V_{IH}	Logical "1" Input Voltage			2.0			V
V_{IL}	Logical "0" Input Voltage		DP8308			0.8	V
			DP7308			0.7	V
I_{IH}	Logical "1" Input Current	V_{IH} = 2.7V			0.5	20	μA
I_I	Maximum Input Current	V_{CC} = max, V_{IH} = 5.25V				1.0	mA
I_{IL}	Logical "0" Input Current	V_{IL} = 0.4V	$\overline{R}$		−0.1	−0.25	mA
			$\overline{T}$		−0.25	−0.5	mA
V_{CLAMP}	Input Clamp Voltage	I_{IN} = −12 mA			−0.8	−1.5	V
POWER SUPPLY CURRENT							
I_{CC}	Power Supply Current	$\overline{T}$ = $\overline{R}$ = 2.0V, V_{IN} = 0.4V, V_{CC} = max			5.0		mA
		$\overline{T}$ = V_{INA} = 0.4V, $\overline{R}$ = 2V, V_{CC} = max			40.0		mA

AC Electrical Characteristics V_{CC} = 5V, T_A = 25°C

Symbol	Parameter	Conditions	Min	Typ	Max	Units
A PORT DATA/MODE SPECIFICATION *(Figure A)*						
t_{PDHLA}	Propagation Delay to a Logical "0" from B Port to A Port	$\overline{T}$ = 2.5V, $\overline{R}$ = 0.4V, R1 = 1k, C1 = 50 pF S1 = 0, S2 = X, S3 = 0, S4 = 2		11		ns
t_{PDLHA}	Propagation Delay to a Logical "1" from B Port to A Port	$\overline{T}$ = 2.5V, $\overline{R}$ = 0.4V, R1 = 1k, C1 = 50 pF S1 = 0, S2 = X, S3 = 0, S4 = 2		11		ns
t_{PTLZA}	Propagation Delay from "0" to TRI-STATE from $\overline{R}$ to A Port	B0–B7 = 0.4V, $\overline{T}$ = 2.5V, R1 = 1k, C1 = 50 pF 81 = 1, S2 = 1, S3 = 1, S4 = 0		17		ns
t_{PTHZA}	Propagation Delay from "1" to TRI-STATE from $\overline{R}$ to A Port	B4–B7 = 2.4V, $\overline{T}$ = 2.5V, R1 = 1k, C1 = 50 pF S1 = 1, S2 = 0, S3 = 1, S4 = 1		16		ns
t_{PTZLA}	Propagation Delay from TRI-STATE to "0" from $\overline{R}$ to A Port	B0–B7 = 0.4V, $\overline{T}$ = 2.5V, R1 = 1k, C1 = 50 pF S1 = 1, S2 = 1, S3 = 1, S4 = 0		26		ns
t_{PTZHA}	Propagation Delay from TRI-STATE to "1" from $\overline{R}$ to A Port	B0–B7 = 2.4V, $\overline{T}$ = 2.5V, R1 = 1k, C1 = 50 pF S1 = 1, S2 = 0, S3 = 1, S4 = 1		30		ns

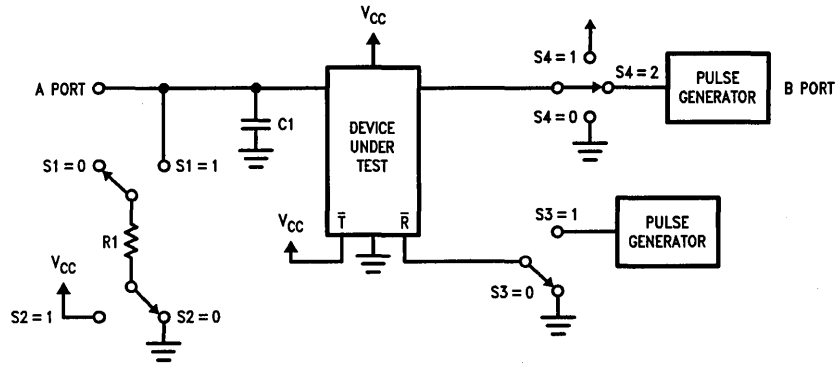
Symbol	Parameter	Conditions	Min	Typ	Max	Units
B PORT DATA/MODE SPECIFICATION *(Figure B)*						
t_{PDHLB}	Propagation Delay to a Logical "0" from A Port to B Port	$\overline{T}$ = 0.4V, $\overline{R}$ = 2.4V, R2 = 150Ω, R3 = 100Ω, C2 = 300 pF, S6 = 0, S7 = 0, S8 = 2		14		ns
t_{PDLHB}	Propagation Delay to a Logical "1" from A Port to B Port	$\overline{T}$ = 0.4V, $\overline{R}$ = 2.4V, R2 = 150Ω, R3 = 100Ω, C2 = 300 pF, S6 = 0, S7 = 0, S8 = 2		22		ns
t_{PALZB}	Propagation Delay from "0" to TRI-STATE from $\overline{R}$ to B Port	A0–A7 = 0, $\overline{R}$ = 2.4V, R2 = 150Ω, R3 = 100Ω, C2 = 300 pF, S6 = 1, S7 = 1, S8 = 0		17		ns
t_{PRHZB}	Propagation Delay from "1" to TRI-STATE from $\overline{R}$ to B Port	A0–A7 = 2.4V, $\overline{R}$ = 2.4V, R2 = 150Ω, R3 = 100Ω, C2 = 300 pF, S6 = 0, S7 = 1, S8 = 1		15		ns
t_{PRZLB}	Propagation Delay from TRI-STATE to "0" from $\overline{R}$ to B Port	A0–A7 = 0.4V, $\overline{R}$ = 2.4V, R2 = 150Ω, R3 = 100Ω, C2 = 300 pF, S6 = 1, S7 = 1, S8 = 0		24		ns
t_{PRZHB}	Propagation Delay from TRI-STATE to "1" from $\overline{R}$ to B Port	A0–A7 = 2.4V, $\overline{R}$ = 2.4V, R2 = 150Ω, R3 = 100Ω, C2 = 300 pF, S6 = 0, S7 = 1, S8 = 1		38		ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: Unless otherwise specified, min/max limits apply across the supply and temperature range listed in the table of Recommended Operating Conditions. All typical values given are for V_{CC} = 5V and T_A = 25°C.

Note 3: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified.

Test Circuits



TL/F/8627–3

FIGURE A. A Port Test Load

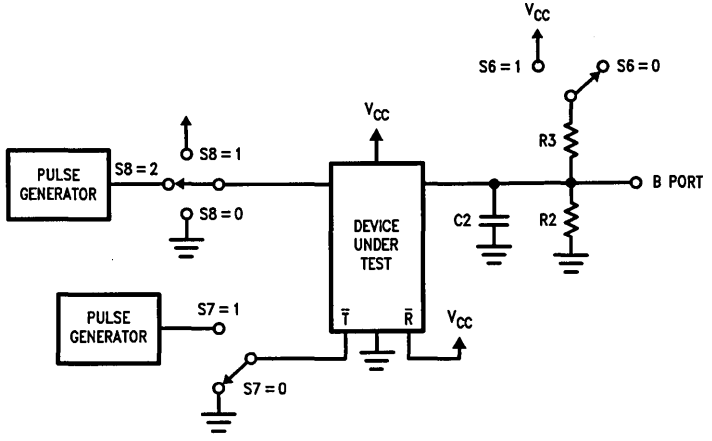


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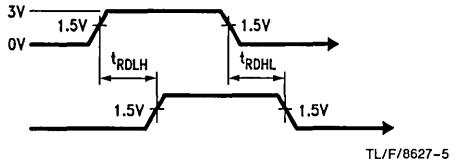
FIGURE B. B Port Test Load

Timing Waveforms



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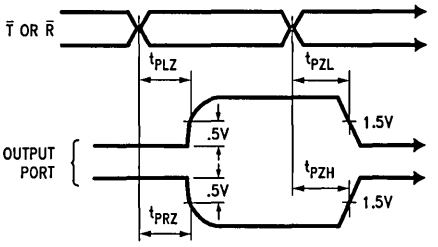


TL/F/8627–6

FIGURE C

National Semiconductor Corporation

DS26S10C/DS26S10M/DS26S11C/DS26S11M Quad Bus Transceivers

General Description

The DS26S10 and DS26S11 are quad Bus Transceivers consisting of 4 high speed bus drivers with open-collector outputs capable of sinking 100 mA at 0.8V and 4 high speed bus receivers. Each driver output is connected internally to the high speed bus receiver in addition to being connected to the package pin. The receiver has a Schottky TTL output capable of driving 10 Schottky TTL unit loads.

An active low enable gate controls the 4 drivers so that outputs of different device drivers can be connected together for party-line operation.

The bus output high-drive capability in the low state allows party-line operation with a line impedance as low as 100Ω. The line can be terminated at both ends, and still give considerable noise margin at the receiver. The receiver typical switching point is 2V.

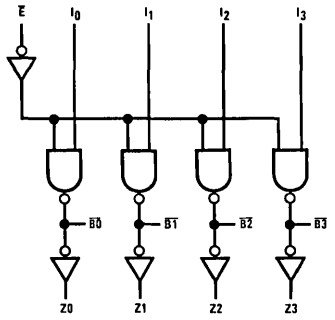
The DS26S10 and DS26S11 feature advanced Schottky processing to minimize propagation delay. The device package also has 2 ground pins to improve ground current handling and allow close decoupling between V_{CC} and ground at the package. Both GND 1 and GND 2 should be tied to the ground bus external to the device package.

Features

- Input to bus is inverting on DS26S10
- Input to bus is non-inverting on DS26S11
- Quad high speed open-collector bus transceivers
- Driver outputs can sink 100 mA at 0.8V maximum
- Advanced Schottky processing
- PNP inputs to reduce input loading

Logic and Connection Diagrams

DS26S10



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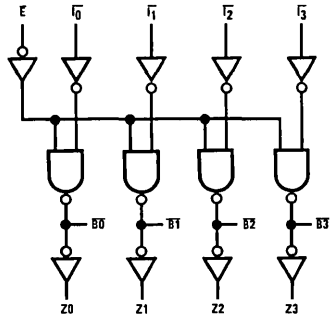
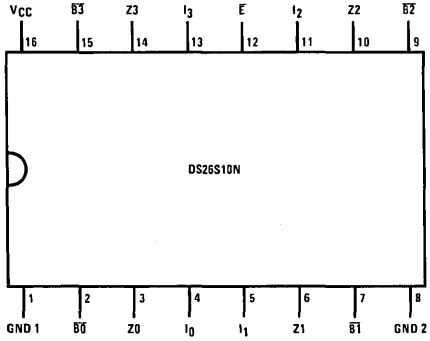
DS26S11



TL/F/5802–2

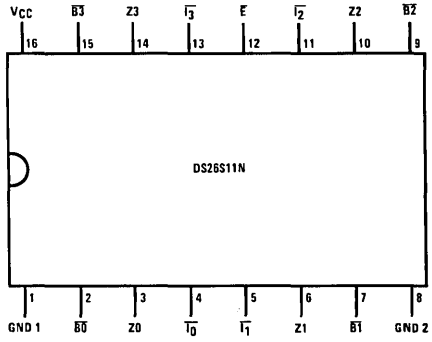
Dual-In-Line Package



TL/F/5802–3

Top View
Order Number DS26S10CJ, DS26S10MJ or DS26S10CN
See NS Package Number J16A or N16A

Dual-In-Line Package



TL/F/5802–4

Top View
Order Number DS26S11CJ, DS26S11MJ or DS26S11CN
See NS Package Number J16A or N16A

Absolute Maximum Ratings

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	−0.5V to +7V
DC Voltage Applied to Outputs for High Output State	−0.5V to +V_{CC} Max
DC Input Voltage	−0.5V to +5.5V
Output Current, Into Bus	200 mA
Output Current, Into Outputs (Except Bus)	30 mA
DC Input Current	−30 mA to +5 mA

Maximum Power Dissipation* at 25°C

Cavity Package	1433 mW
Molded Package	1362 mW

*Derate cavity package 9.6 mW/°C above 25°C; derate molded package 10.9 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
DS26S10C, DS26S11C	4.75	5.25	V
DS26S10M, DS26S11M	4.5	5.5	V
Temperature (T_A)			
DS26S10C, DS26S11C	0	+70	°C
DS26S10M, DS26S11M	−55	+125	°C

Electrical Characteristics (Unless otherwise noted)

Symbol	Parameter	Conditions (Note 1)		Min	Typ (Note 2)	Max	Units
V_{OH}	Output High Voltage (Receiver Outputs)	V_{CC} = Min, I_{OH} = −1 mA, V_{IN} = V_{IL} or V_{IH}	Military	2.5	3.4		V
			Commercial	2.7	3.4		V
V_{OL}	Output Low Voltage (Receiver Outputs)	V_{CC} = Min, I_{OL} = 20 mA, V_{IN} = V_{IL} or V_{IH}				0.5	V
V_{IH}	Input High Level (Except Bus)	Guaranteed Input Logical High for All Inputs		2.0			V
V_{IL}	Input Low Level (Except Bus)	Guaranteed Input Logical Low for All Inputs				0.8	V
V_I	Input Clamp Voltage (Except Bus)	V_{CC} = Min, I_{IN} = −18 mA				−1.2	V
I_{IL}	Input Low Current (Except Bus)	V_{CC} = Max, V_{IN} = 0.4V	Enable			−0.36	mA
			Data			−0.54	mA
I_{IH}	Input High Current (Except Bus)	V_{CC} = Max, V_{IN} = 2.7V	Enable			20	μA
			Data			30	μA
I_I	Input High Current (Except Bus)	V_{CC} = Max, V_{IN} = 5.5V				100	μA
I_{SC}	Output Short-Circuit Current (Except Bus)	V_{CC} = Max, (Note 3)	Military	−20		−55	mA
			Commercial	−18		−60	mA
I_{CCL}	Power Supply Current (All Bus Outputs Low)	V_{CC} = Max, Enable = GND	DS26S10		45	70	mA
			DS26S11			80	mA

Bus Input/Output Characteristics

Symbol	Parameter	Conditions (Note 1)			Min	Typ (Note 2)	Max	Units
V_{OL}	Output Low Voltage	V_{CC} = Min	Military	I_{OL} = 40 mA		0.33	0.5	V
				I_{OL} = 70 mA		0.42	0.7	
				I_{OL} = 100 mA		0.51	0.8	
			Commercial	I_{OL} = 40 mA		0.33	0.5	
				I_{OL} = 70 mA		0.42	0.7	
				I_{OL} = 100 mA		0.51	0.8	
I_O	Bus Leakage Current	V_{CC} = Max		V_O = 0.8V			−50	μA
			Military	V_O = 4.5V			200	
			Commercial	V_O = 4.5V			100	
I_{OFF}	Bus Leakage Current (Power OFF)	V_O = 4.5V					100	μA
V_{TH}	Receiver Input High Threshold	Bus Enable = 2.4V, V_{CC} = Max		Military	2.4	2.0		V
				Commercial	2.25	2.0		
V_{TL}	Receiver Input Low Threshold	Bus Enable = 2.4V, V_{CC} = Min		Military		2.0	1.6	V
				Commercial		2.0	1.75	

Note 1: For conditions shown as min or max, use the appropriate value specified under Electrical Characteristics for the applicable device type.

Note 2: Typical limits are at V_{CC} = 5V, 25°C ambient and maximum loading.

Note 3: Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

Switching Characteristics (T_A = 25°C, V_{CC} = 5V)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
t_{PLH}	Data Input to Bus	R_B = 50Ω, C_B = 50 pF (Note 1)	DS26S10		10	15	ns
t_{PHL}	Data Input to Bus				10	15	ns
t_{PLH}	Data Input to Bus		DS26S11		12	19	ns
t_{PHL}	Data Input to Bus				12	19	ns
t_{PLH}	Enable Input to Bus		DS26S10		14	18	ns
t_{PHL}	Enable Input to Bus				13	18	ns
t_{PLH}	Enable Input to Bus		DS26S11		15	20	ns
t_{PHL}	Enable Input to Bus				14	20	ns
t_{PLH}	Bus to Receiver Out	R_B = 50Ω, R_L = 280Ω, C_B = 50 pF (Note 1), C_L = 15 pF			10	15	ns
t_{PHL}	Bus to Receiver Out				10	15	ns
t_r	Bus	R_B = 50Ω, C_B = 50 pF (Note 1)		4.0	10		ns
t_f	Bus			2.0	4.0		ns

Note 1: Includes probe and jig capacitance.

Truth Tables

DS26S10

Inputs		Outputs	
$\overline{E}$	I	$\overline{B}$	Z
L	L	H	L
L	H	L	H
H	X	Y	$\overline{Y}$

DS26S11

Inputs		Outputs	
$\overline{E}$	$\overline{I}$	$\overline{B}$	Z
L	L	L	H
L	H	H	L
H	X	Y	$\overline{Y}$

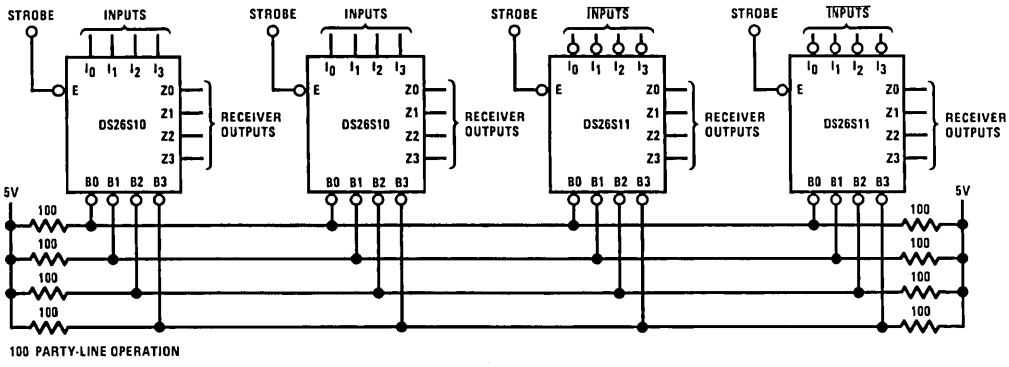
H = High voltage level

L = Low voltage level

X = Don't care

Y = Voltage level of bus (assumes control by another bus transceiver)

Typical Application



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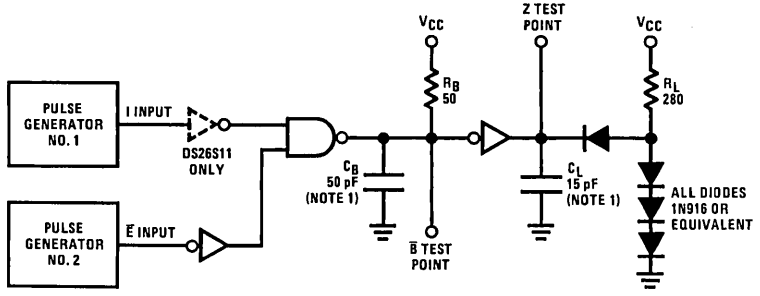
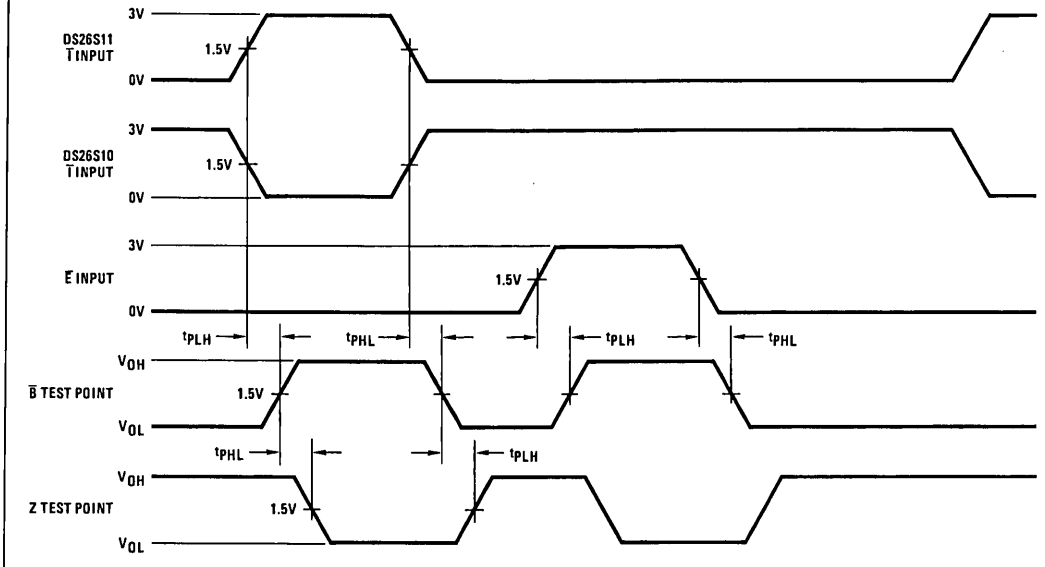
AC Test Circuit and Switching Time Waveforms



TL/F/5802-6

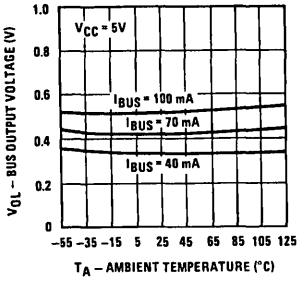
Note 1: Includes probe and jig capacitance.



TL/F/5802-7

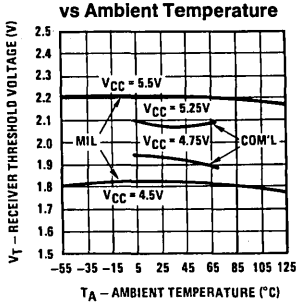
Typical Performance Characteristics

Typical Bus Output Low Voltage vs Ambient Temperature



TL/F/5802–8

Receiver Threshold Variation vs Ambient Temperature



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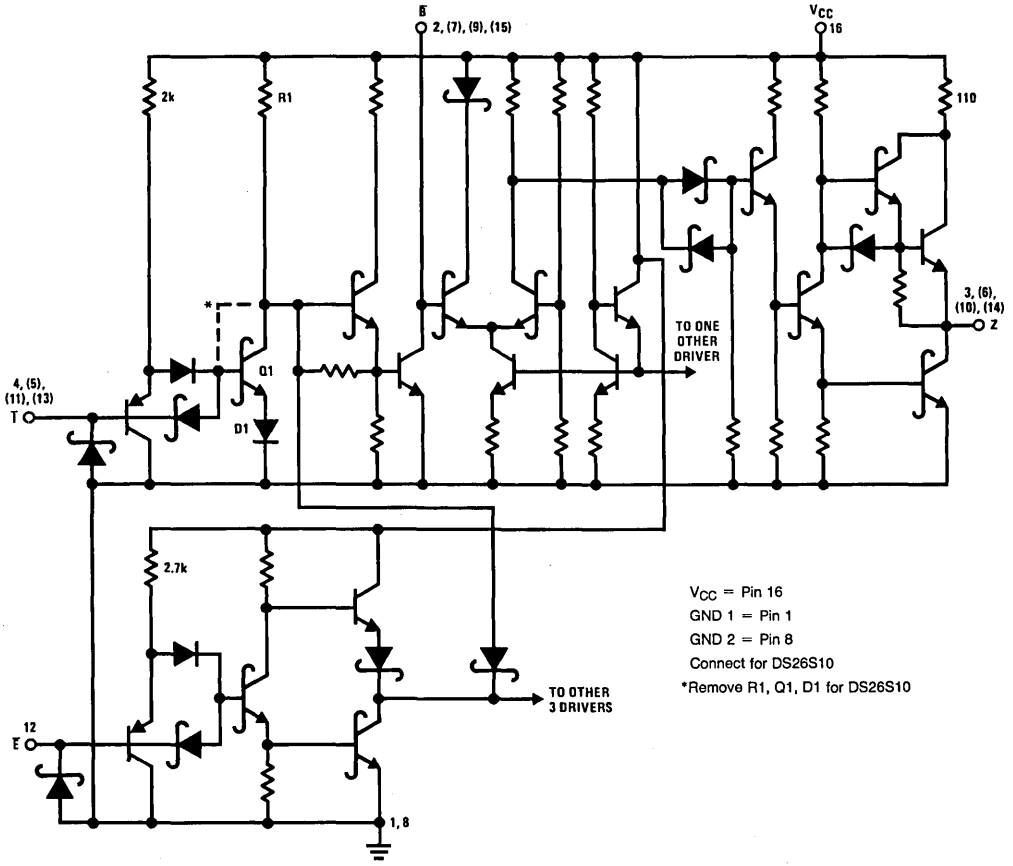
Schematic Diagram



TL/F/5802–10

National Semiconductor Corporation

DS3662 Quad High Speed Trapezoidal™ Bus Transceiver

General Description

The DS3662 is a quad high speed Schottky bus transceiver intended for use with terminated 120Ω impedance lines. It is specifically designed to reduce noise in unbalanced transmission systems. The open collector drivers generate precise trapezoidal waveforms with rise and fall times of 15 ns (typical), which are relatively independent of capacitive loading conditions on the outputs. This reduces noise coupling to the adjacent lines without any appreciable impact on the maximum data rate obtainable with high speed bus transceivers. In addition, the receivers use a low pass filter in conjunction with a high speed comparator, to further enhance the noise immunity. Tightly controlled threshold levels on the receiver provide equal rejection to both negative and positive going noise pulses on the bus.

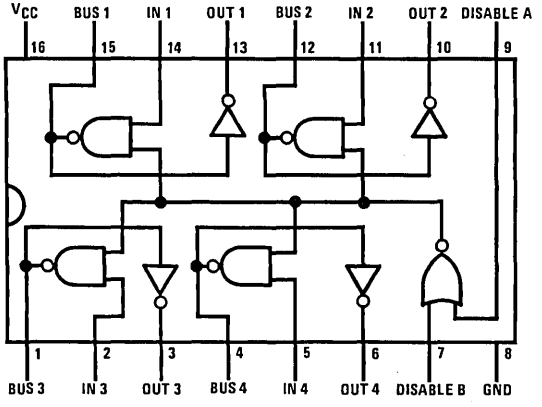
The external termination is intended to be a 180Ω resistor from the bus to 5V logic supply, together with a 390Ω resistor from the bus to ground. The bus can be terminated at one or both ends. A two input NOR gate is provided to disable all drivers in a package simultaneously.

Features

- Pin to pin functional replacement for DS8641
- Guaranteed AC specifications on noise immunity and propagation delay over the specified temperature and supply voltage range
- Temperature insensitive receiver thresholds track bus logic level
- Trapezoidal bus waveforms reduce noise coupling to adjacent lines
- Precision receiver thresholds provide maximum noise immunity and symmetrical response to positive and negative going pulses
- Open collector driver output allows wire-OR connection
- High speed Schottky technology
- 15 μA typical bus termination current with normal V_{CC} or with V_{CC} = 0V
- Glitch free power up/down protection on the driver output
- TTL compatible driver and disable inputs, and receiver outputs

Block and Connection Diagram

Dual-In-Line Package



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Top View

Order Number DS3662J or DS3662N
See NS Package Number J16A or N16A

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input and Output Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1509 mW
Molded Package	1476 mW
Lead Temperature (Soldering, 4 sec.)	260°C

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.75	5.25	V
Temperature Range (T_A)	0	70	°C

*Derate cavity package 10.1 mW/°C above 25°C; derate molded package 11.8 mW/°C above 25°C.

Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRIVER AND DISABLE INPUTS						
V_{IH}	Logical "1" Input Voltage		2.0			V
V_{IL}	Logical "0" Input Voltage				0.8	V
I_I	Logical "1" Input Current	V_{IN} = 5.5V			1	mA
I_{IH}	Logical "1" Input Current	V_{IN} = 2.4V			40	μA
I_{IL}	Logical "0" Input Current	V_{IN} = 0.4V		−1	−1.6	mA
V_{CL}	Input Diode Clamp Voltage	I_{CLAMP} = −12 mA		−0.8	−1.5	V
DRIVER OUTPUT/RECEIVER INPUT						
V_{OLB}	Low Level Bus Voltage	V_{DIS} = 0.8V, V_{IN} = 2V, I_{BUS} = 100 mA		0.6	0.9	V
I_{IHB}	Maximum Bus Current	V_{IN} = 0.8V, V_{BUS} = 4V, V_{CC} = 5.25V		10	100	μA
I_{ILB}	Maximum Bus Current	V_{IN} = 0.8V, V_{BUS} = 4V, V_{CC} = 0V			100	μA
V_{IH}	High Level Receiver Threshold	V_{IN} = 0.8V, V_{OL} = 16 mA	1.90	1.70		V
V_{IL}	Low Level Receiver Threshold	V_{IN} = 0.8V, I_{OH} = −400 μA		1.70	1.50	V
RECEIVER OUTPUT						
V_{OH}	Logical "1" Output Voltage	V_{IN} = 0.8V, V_{BUS} = 0.5V, I_{OH} = −400 μA	2.4	3.2		V
V_{OL}	Logical "0" Output Voltage	V_{IN} = 0.8V, V_{BUS} = 4V, I_{OL} = 16 mA		0.35	0.5	V
I_{OS}	Output Short Circuit Current	V_{DIS} = 0.8V, V_{IN} = 0.8V, V_{BUS} = 0.5V, V_{OS} = 0V, V_{CC} = 5.25V, (Note 4)	−40	−70	−100	mA
I_{CC}	Supply Current	V_{DIS} = 0V, V_{IN} = 2V		50	90	mA

Switching Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
PROPAGATION DELAYS						
t_{PLHD}	Disable to Bus "1"	*Figure 1*		25	35	ns
t_{PHLD}	Disable to Bus "0"			25	35	ns
t_{PLHB}	Driver Input to Bus "1"	*Figure 2*		20	30	ns
t_{PHLB}	Driver Input to Bus "0"			20	30	ns
t_{PLHR}	Bus to Logical "1" Receiver Output	*Figure 3*		25	40	ns
t_{PHLR}	Bus to Logical "0" Receiver Output			25	40	ns
NOISE IMMUNITY						
t_{rB}, t_{fB}	Rise and Fall Times (10%–90%) of the Driver Output	*Figure 2*	10	15	20	ns
t_{nR}	Receiver Noise Rejection Pulse Width	No Response at Receiver Output as per *Figure 4*		20	10	ns

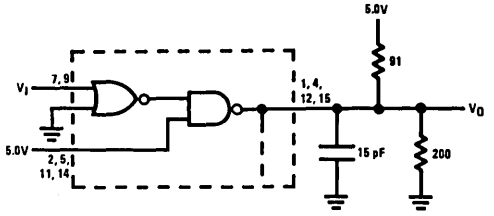
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" and "Recommended Operating Conditions" provide conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the supply and temperature range listed in the table of "Recommended Operating Conditions". All typical values are for T_A = 25°C and V_{CC} = 5V.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Only one output at a time should be shorted.

AC Test Circuits and Switching Waveforms



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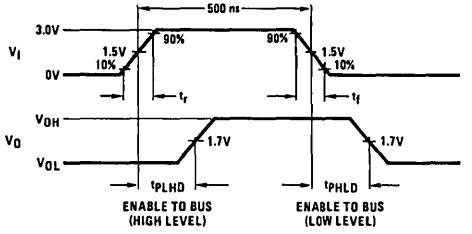
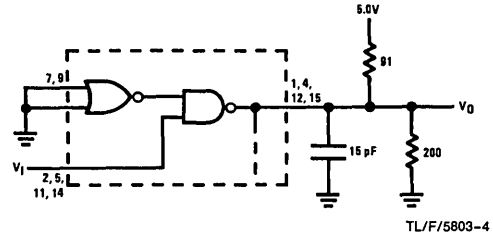


TL/F/5803-3

Note: $t_r = t_f = 2.5$ ns. Pulse width = 500 ns measured between 1.5V levels. f = 1 MHz.

FIGURE 1. Disable Delays



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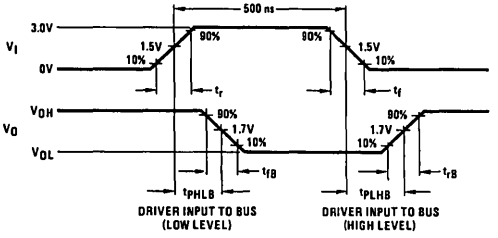
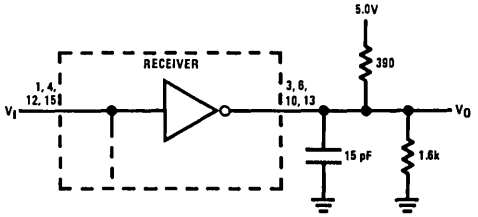


TL/F/5803-5

Note: $t_r = t_f = 2.5$ ns. Pulse width = 500 ns measured between 1.5V levels. f = 1 MHz.

FIGURE 2. Driver Propagation Delays



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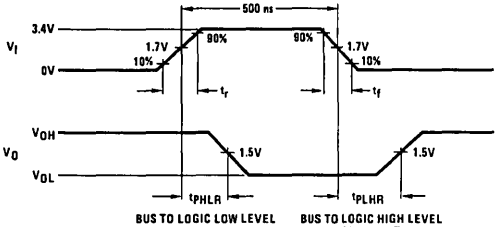
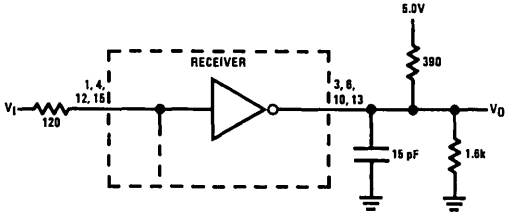


TL/F/5803-7

Note: $t_r = t_f = 15$ ns. Pulse width = 500 ns measured between 1.7V levels. f = 1 MHz.

FIGURE 3. Receiver Propagation Delays



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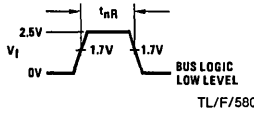

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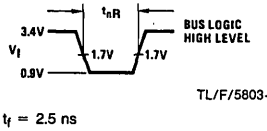
$t_r = t_f = 2.5$ ns

(a) Receiver Output (V_O) to Remain Greater than 2.2V



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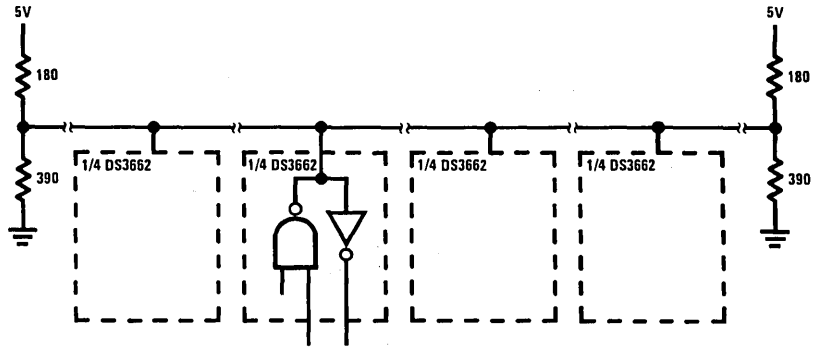
$t_r = t_f = 2.5$ ns

(b) Receiver Output (V_O) to Remain Less than 0.7V

FIGURE 4. Receiver Noise Immunity: "No Response at Output" Input Waveforms

Typical Application

120Ω Unified Data Bus



TL/F/5803–11

DS3662—The Bus Optimizer

National Semiconductor Corp.
Application Note 259
R. V. Balakrishnan

I. INTRODUCTION

A single ended Bus is an unbalanced Data Transmission medium, which is timeshared by several system elements. Like any unbalanced system, it is highly susceptible to common-mode noise, such as ground noise and crosstalk. In general, the latter determines the maximum physical length of the Bus that can be incorporated with acceptable reliability. Crosstalk is a major problem in high speed computer Buses which employ Schottky Transceivers for increased data rate capability. It is therefore highly desirable to minimize crosstalk noise in Bus circuits to allow for longer Buses and to provide higher system reliability.

This article describes the operation of the DS3662 Quad High Speed Trapezoidal Bus Transceiver, which has been specially designed to minimize crosstalk problems. The Driver generates precise Trapezoidal waveforms that reduce noise coupling to adjacent Bus channels. The Receiver uses a low pass filter, whose time constant is matched to the Driver slew rate to provide maximum noise rejection with acceptable signal delay characteristics. Precision high speed circuitry optimizes noise immunity without sacrificing the high data rate capability of Schottky Transceivers.

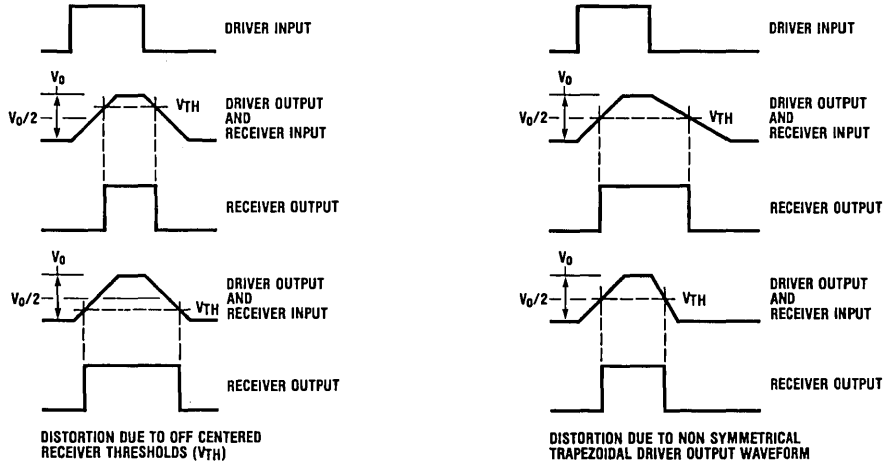
II. THE PROBLEM

Conventional Bus Drivers are designed to provide high output currents for charging and discharging relatively large Bus capacitances quickly. These high speed transitions are characterized by peak slew rates of up to 5V/ns around the mid-region of the transition. This can cause considerable noise coupling to adjacent lines, commonly referred to as crosstalk. Crosstalk also includes noise induced by sources external to the Bus. Additional noise may be generated due to reflections at imperfect terminations.

Bus Receviers are designed to respond to high speed transitions and to provide low propagation delays. Unfortunately, their fast response results in high noise sensitivity. The combined effect of the noise on the Bus and the sensitivity of the Receiver to the noise severely limits the Bus performance.

III. THE SOLUTION

The above situation can be considerably improved by employing noise reduction techniques in both the Driver and the Receiver circuits. Slew rate control can be used in the Driver to reduce crosstalk, and Receiver noise sensitivity can be reduced by using a low pass filter at its input. These techniques are commonly used in line transmission circuits where the associated data rates in general are considerably lower. However, these techniques do present some difficulties in high speed Bus circuits. Increased rise and fall times, resulting from slew rate control, can affect data rates unless care is taken to limit the maximum rise and fall times to minimum pulse width requirements. With any appreciable slew rate control, the rise and fall times of the resulting Driver output waveform will be comparable to the pulse widths at maximum data rates. This condition dictates high fidelity of the transmitted waveform and precise Receiver thresholds at the middle of the Bus voltage swing in order to minimize pulse width distortion. *Figure 1* illustrates the different sources of pulse width distortion due to the trapezoidal nature of the signal.



TL/F/5857–1 TL/F/5857–2

FIGURE 1. Pulse Width Distortion

The low pass filter in the Receiver should provide optimum noise rejection without introducing excessive delay in passing the signal waveform. In addition, the Receiver should have a symmetrical response to positive and negative going transitions in order to maintain a low level of pulse width distortion, as well as equal noise rejection to positive and negative going noise pulses. The response of an ideal low pass filter to signal and noise pulses is shown in *Figure 2.*

The DS3662 overcomes these and other problems by using high speed linear circuitry with on-chip capacitors for controlling slew rate and low pass filtering. The Driver is of open collector type intended for use with terminated 120Ω Buses. The external termination consists of a 180Ω resistor from the Bus to +5V logic supply with a 390Ω resistor from the Bus to ground. Such a termination results in a Bus logic high level of 3.4V with V_{CC} at 5V (See *Figure 2*). The Bus can be terminated at one or both ends as shown in *Figure 3.*

IV. THE DRIVER

Using a Miller integrator circuit, the Driver generates a linearly rising and falling waveform with a constant slew rate of 0.2V/ns (typical) during the entire period of transition. This corresponds to typical rise and fall times of 15 ns. *Figure 4* compares the output waveform of a typical Schottky Driver and the DS3662 under different capacitive loads. It should be noted that even under heavy loading, the regular Drivers have peak slew rates that are considerably higher than the average. In contrast, the trapezoidal waveform provides considerably lower slew rate with slightly higher rise and fall times. Such an increase in rise and fall time has very little effect on data rates. In fact, the high fidelity of the transmitted waveform allows pulse widths as low as 20 ns to be transmitted on the Bus, as shown in *Figure 5.*

The block diagram of the Driver is shown in *Figure 6* and *7.* When a high to low transition is applied to the input, switch 'S' opens and node 'A' is pulled low by the current source 'I'. This switches the amplifier output to a high state. The slew rate of the output transition is limited by the charging current through the capacitor, a constant value equal to I/C volts/sec.

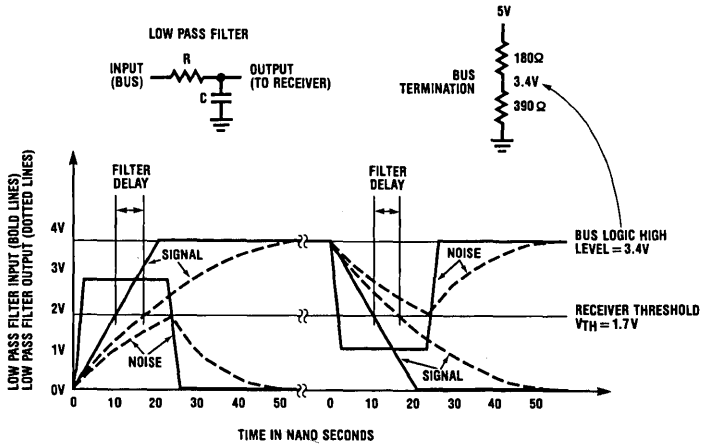


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FIGURE 2. Ideal Receiver Low Pass Filter Response

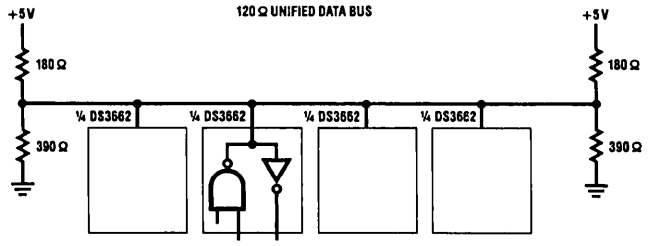

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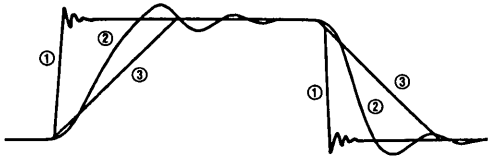
FIGURE 3. Bus Termination



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①—Typical High Speed Driver Output Unloaded

②—Typical High Speed Driver Output Loaded

③—Typical Output of Controlled Slew Rate Driver Which is Load Independent

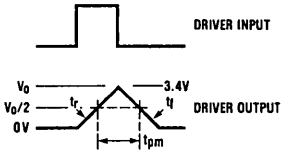
① $t_r = t_f \sim 3$ ns

② $t_r = t_f \sim 10$ ns

③ $t_r = t_f \sim 15$ ns

Note: The word "loading" here refers to capacitive loading only.

FIGURE 4. Waveform Comparison



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$t_{pm} \approx 20$ ns $\quad t_r \approx t_f \approx 15$ ns (10% to 90%)

FIGURE 5. Minimum Pulse Width Driver Output

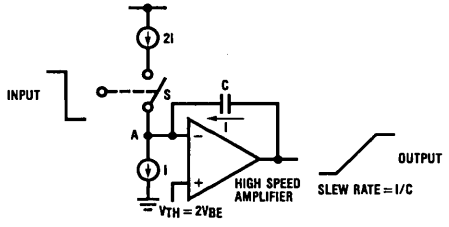

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FIGURE 6. Driver

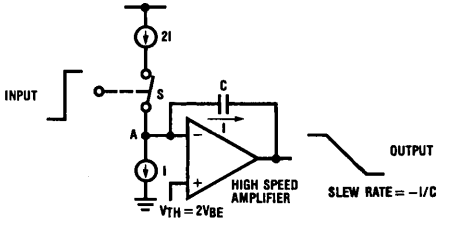

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FIGURE 7. Driver

Likewise, when a low to high transition is applied to the input, switch 'S' closes and node 'A' is pulled up by the '21' current source, switching the amplifier output to a low state. The capacitor now has an equal but opposite charging current which once again limits the slew rate to $-I/C$ volts/sec. The inherent tracking ability of I.C. current sources provide equal rise and fall times resulting in a symmetrical output waveform.

The on-chip capacitors are fabricated using back to back junction diodes. The use of junction capacitors reduces die area and the back to back connection allows operation with either polarity. The capacitor terminal, connected to the amplifier input, remains at $V_{th} \cong 1.6V$ during the output transition. This voltage, being close to the middle of the output swing, reduces the effect of the capacitor voltage sensitivity on the output waveshape.

V. THE RECEIVER

The Receiver consists of a low pass filter followed by a high speed comparator with a typical threshold of 1.7V (see *Figure 8*). This threshold value corresponds to the mid-point voltage of the 0 to 3.4V Bus swing. It is derived from a potential divider allowing the Bus logic levels to track with V_{CC} variations. If the low pass filter capacitor is voltage insensitive, this circuit will provide equal propagation delay for positive and negative going signal transitions on the Bus. In addition, it will also provide equal noise rejection to a positive and negative going pulse (see *Figure 2*). However, the junction capacitors, being voltage sensitive, will exhibit non-symmetrical response in the above circuit. This problem is overcome in the DS3662 Receiver by using a back to back junction capacitor with the ground end biased at 1.7V (see *Figure 9*). Although the capacitor still varies with the voltage at node 'A', the variation is symmetrical about 1.7V (the middle of the Bus swing) and therefore will provide an identical response to transitions of either polarity.

VI. TRANSCEIVER PERFORMANCE

The characteristics of the trapezoidal Transceiver are fully detailed in the device data sheet. Some of the more important specifications are discussed below. Both AC and DC specifications are guaranteed over a 0–70°C temperature range and a supply range of 4.75–5.25V.

The Driver typically has a propagation delay of 15 ns with a maximum of 30 ns. The Receiver propagation delays are specified at 25 ns typical and 40 ns maximum. The Driver output rise and fall times are guaranteed to be within 10 to 20 ns with a typical of 15 ns. The noise immunity of the Receiver is specified in terms of the width of a 2.5V pulse that is guaranteed to be rejected by the Receiver (see *Figure 10*). The Receiver typically rejects a 20 ns pulse going positive from ground level or going negative from a 3.4V logic 1 level. Worst case rejection is specified at 10 ns.

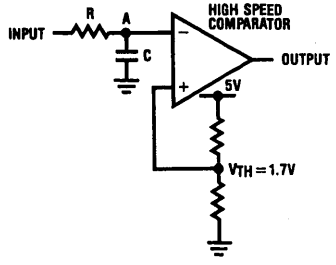

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FIGURE 8. Receiver

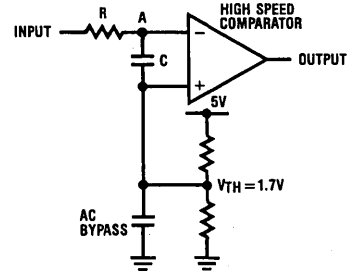

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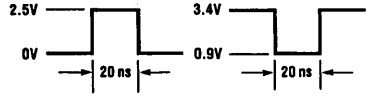
FIGURE 9. Receiver



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Rejects positive or negative going noise pulses of pulse widths up to 20 ns typical.
Detects and propagates trapezoidal signal pulses in 20 ns typical.

FIGURE 10. Receiver Noise Immunity

The AC response of the DS3662 Driver and Receiver are depicted in *Figures 11* and *12* respectively. *Figure 11* shows the typical Driver output waveform as compared to a standard high speed Transceiver output. Oscillograms in *Figure 12* demonstrate the ability of the Receiver to distinguish the trapezoidal signal from the noise. Here the Receiver rejects a noise pulse of 19 ns width, while accepting a narrower signal pulse (= 16 ns) of the same amplitude (The signal is triangular since the pulse width is smaller than the rise and fall time of the Trapezoidal Driver output).

The performance of the Transceiver under actual operating condition is demonstrated in *Figures 13* through *15*. Oscillograms in *Figure 13* clearly show the capability of the DS3662 in real life situations. Here it is compared with the DS8834 under identical conditions. The Transceivers drive a minicomputer Bus (flat ribbon cable) 100 feet long, terminated at the far end with taps at various lengths for connecting to the Receiver input. The cable is randomly folded to generate crosstalk between the various parts. In addition a noise pulse is induced on the signal line by driving an adjacent line with a pulse generator. This corresponds to the second dominant pulse in the Bus waveforms at approximately 600 ns from the main signal pulse. As can be seen, the DS8834 with fast rise and fall times on the Driver output generates more crosstalk and its Receiver easily responds to this crosstalk and to the externally induced noise (even though it has hysteresis!), limiting the useful Bus length to less than 10 feet. In contrast, the DS3662's Driver generates much less crosstalk and its Receiver is immune to the induced noise even when the noise amplitude exceeds the signal amplitude as seen in the oscillogram at 50 feet. When the same experiment was repeated with the DS8641, it responded to the noise even at 10 feet as shown in *Figure 14*.

Figure 15 shows the plots of maximum data rate versus line length for the three Transceivers discussed above under two different conditions. The graph in *Figure 15a* is obtained with no consideration to the pulse width distortion whereas the one in *Figure 15b* is obtained for a maximum allowable pulse width distortion of ±10%. A square waveform is used so that the pulse width distortion criteria will apply to both positive and negative going pulses. These graphs clearly show that the DS3662 can be used at considerably higher data rates with lower distortion for longer distances than the other two Transceivers *(Figure 15b)* although the others have a slightly higher data rate capability at short distances with high timing distortion *(Figure 15a)*.

VII. CONCLUSION

The DS3662, with its combination of a trapezoidal Driver and a noise rejecting Receiver utilizing on chip capacitors, represents a significant improvement in high speed Bus circuits and a solution to Bus noise problems commonly encountered in Mini and Microcomputer systems.

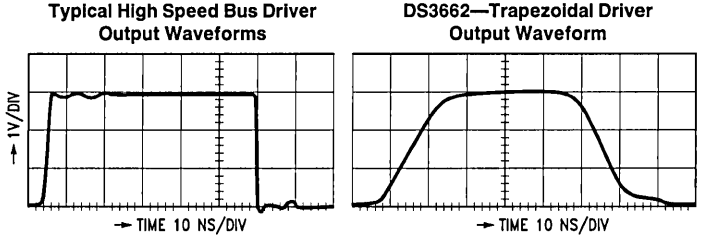

FIGURE 11

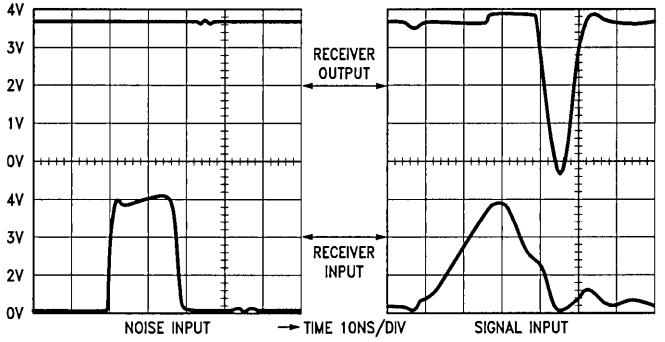

FIGURE 12. DS3662 Receiver Response

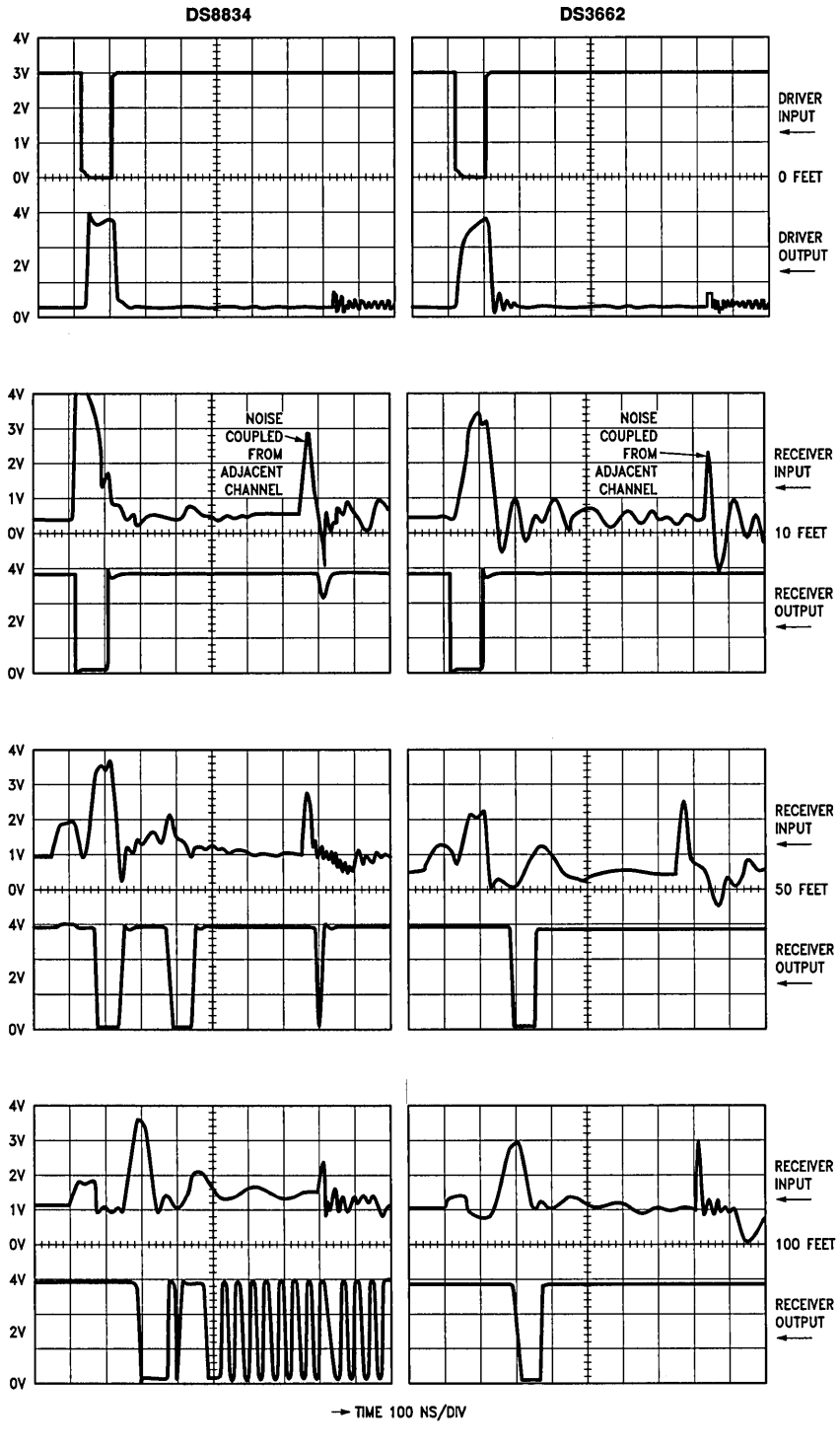
DS8834
DS3662
4V
3V
2V
1V
0V
DRIVER INPUT
0 FEET
DRIVER OUTPUT
TL/F/5857–14
NOISE COUPLED FROM ADJACENT CHANNEL
RECEIVER INPUT
10 FEET
RECEIVER OUTPUT
TL/F/5857–15
50 FEET
TL/F/5857–16
100 FEET
TIME 100 NS/DIV
TL/F/5857–17

FIGURE 13

DS8641

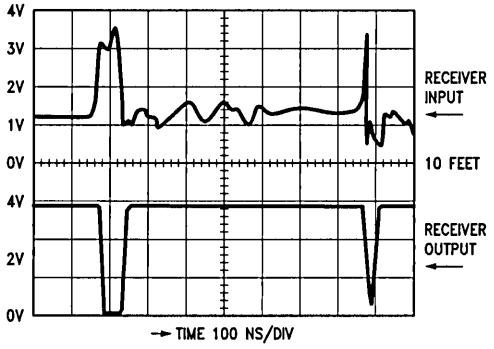

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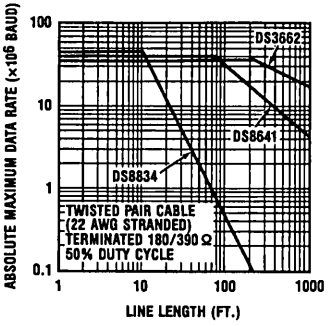
FIGURE 14



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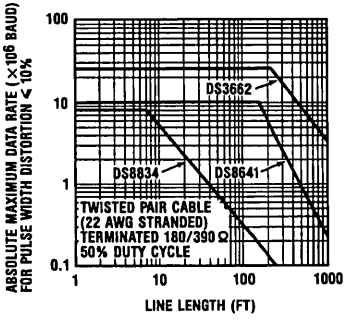

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FIGURE 15. Data Rate vs. Line Length

Reducing Noise on Microcomputer Buses

National Semiconductor Corp.
Application Note 337
R. V. Balakrishnan

Abstract: *This paper focuses on the noise components that have a significant impact on the performance of a high speed microcomputer bus. An overview of their nature is followed by ways to minimize their contribution by suitable design of the PC board backplane, the termination network and the bus transceiver. The DS3662 trapezoidal bus transceiver, which is specifically designed to minimize such noise on high speed buses, is presented along with its performance data. And to conclude, some possible new transceiver designs for further improvement of the bus performance are explored.*

INTRODUCTION

As the microcomputer bus bandwidth is extended to handle ever increasing clock rates, the noise susceptibility of a single-ended bus poses a serious threat to the overall system integrity. Thus, it is mandatory that the various noise contributions be taken into account in the design of the bus transceiver, the PC board backplane and the bus terminations to avoid intermittent or total failure of the system.

Although noise such as crosstalk and reflections are inevitable in any practical bus configuration, their impact on the system can be determined and minimized by careful design of all three components mentioned above. The combined contribution of the noise under worst-case conditions should be within the noise margin for reliable bus operation.

The design of the transceiver plays a significant role in minimizing crosstalk and reflection. The bus can be optimized for minimum noise at a given bandwidth by using a trapezoidal driver having suitable rise and fall times along with a matched low pass filtered receiver which provides a symmetrical noise margin. The DS3662 is one such transceiver, the first member in the family of trapezoidal bus transceviers available from National Semiconductor Corporation. This device represents a significant improvement in high speed bus circuit design and provides a solution to commonly encountered bus noise problems.

THE MICROCOMPUTER BUS

A typical microcomputer bus usually consists of a printed circuit board backplane with signal and ground traces on one side and a ground plane on the other. The length ranges from a few inches to several feet with as many as 32 closely spaced (0.6" typical) card edge connectors. Each signal line interacts with the ground plane to form a transmission line with characteristic impedance 'Z' in the range of 90Ω–120Ω typical. It is desirable to have as large a 'Z' as possible in order to reduce the drive requirement of the bus driver and to reduce the power dissipated at the terminations. But much larger values of 'Z" translate to significantly larger physical dimensions and therefore are not very practical.

The bus appears like a transmission line to any signal having a transition time 't_r' less than the round trip delay '$2T_L$' of the bus. The bus delay 'T_L' is given by:

$$T_L = L\sqrt{L1\,C1} \quad (1)$$

where L = length of the bus
L1 = distributed inductance per unit length
C1 = distributed capacitance per unit length

For a typical unloaded 100Ω microstrip line, C1 ≅ 20 pF/ft and L1 ≅ 0.2 μH/ft. Therefore, T_L = 2.0 ns/ft. This corresponds to approximately half the speed of light. However, the capacitive loading at each connector on the backplane increases the delay time significantly. The loaded delay time 'T_{LL}' is given by:

$$T_{LL} = T_L\sqrt{1 + (C_L/C_1} \quad (2)$$

where C_L = distributed load capacitance/unit length

Given a 10 pF loading at each connector (connector + transceiver capacitance) and a 0.6" spacing between connectors, C_L = 200 pF/ft and T_{LL} = 6.6 ns/ft. So even a 6" long bus has a $2T_{LL}$ = 6.6 ns, which is higher than the transition time (t_r) of many high speed bus drivers. When in doubt, it is always better to use the transmission line approach than the lumped circuit approach as the latter is an approximation of the former. Also, the transmission line analysis gives more pessimistic (worst-case) values of crosstalk and reflection and is, hence, safer.

CROSSTALK REDUCTION

The crosstalk is due to the distributed capacitive coupling C_C and the distributed inductive coupling L_C between two lines. When crosstalk is measured on an undriven sense line next to a driven line (both terminated at their characteristic impedances), the near end crosstalk and the far end crosstalk have quite distinct features, as shown in *Figure 1.* Their respective peak amplitudes are:

$$V_{NE} = K_{NE}(2T_L)(V_I/t_r) \quad \text{for } t_r > 2T_L \quad (3)$$

$$V_{NE} = K_{NE}(V_I) \quad \text{for } t_r < 2T_L \quad (4)$$

$$V_{FE} = K_{FE}(L)(V_I/t_r) \quad (5)$$

where V_I = signal swing on the drive line.

The coupling constants are given by the expressions:

$$K_{NE} = \frac{L(C_C Z + L_C/Z)}{4T_L} \quad (6)$$

$$K_{FE} = \frac{C_C Z - L_C/Z}{2} \text{ ns/ft} \quad (7)$$

The near end component reduces to zero at the far end and vice versa. At any point in between, the crosstalk is a fractional sum of near and far end crosstalk waveforms shown.

It should be noted from expressions 6 and 7 that the far end crosstalk can have either polarity whereas the near end crosstalk always has the same polarity as the signal causing it. In microstrip backplanes the far end crosstalk pulse is usually the opposite polarity of the original signal.

Although the real world bus is far from the ideal situation depicted in *Figure 1,* several useful observations that apply to a general case can be made:

1. The crosstalk always scales with the signal amplitude.
2. Absolute crosstalk amplitude is proportional to slew rate V_I/t_r, not just $1/t_r$.
3. Far end crosstalk width is always t_r.
4. For $t_r < 2T_L$, the near end crosstalk amplitude V_{NE} expressed as a fraction of signal amplitude V_I is a function of physical layout only.
5. The higher the value of 't_r' the lower the percentage of crosstalk (relative to signal amplitude).

The corresponding design implications are:

1. The noise margin expressed as a percentage of the signal swing is what's important, not the absolute noise margin. Therefore, to improve noise immunity, the percentage noise margin has to be maximized. This is achieved by reducing the receiver threshold uncertainty region and by centering the threshold between the high and low levels.
2. Smaller signal amplitude with the same transition time reduces bus drive requirements without reducing noise immunity.
3. Far end crosstalk is eliminated if the receiver is designed to reject pulses having pulse widths less than or equal to t_r.
4. When $t_r < 2T_L$, the near end crosstalk immunity for a given percentage noise margin has to be built into the backplane PC layout. Since $(V_{NE}/V_I) = K_{NE}$ for this case, K_{NE} should be kept lower than the available worst-case noise margin. K_{NE} may be reduced by either increasing the spacing between lines or by introducing a ground line in between. The ground line, in addition to increasing the spacing between the signal lines, forces the electric field lines to converge on it, significantly reducing crosstalk.
5. For minimum crosstalk the rise and fall times of the signal waveform should be as large as possible consistent with the minimum pulse width requirements of the bus. A driver that automatically limits the slew rate of the transition can go a long way in reducing crosstalk.

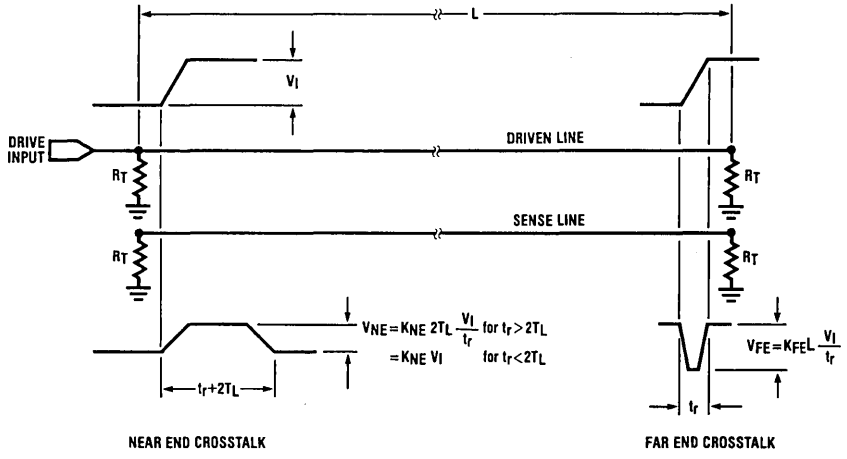

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FIGURE 1. Crosstalk under Ideal Conditions

CROSSTALK MEASUREMENT

When multiple lines on either side of the sense lines switch simultaneously the crosstalk is considerably larger, typically 3.5 times the single line switching case for microstrip backplanes. Also, the location of the drivers on the driven lines and the receiver on the sense line for worst-case crosstalk differs for the near end and far end cases as shown in *Figure 2* and *3* for a uniformly loaded bus. But if the far end crosstalk is not of the opposite polarity, then the combined effect of far end and near end crosstalk could have a larger amplitude and pulse width at a point near the middle of the sense line in *Figure 2*. So in a general case, or in the case of a non-uniformly loaded bus, it is advisable to check the sense line at several locations along the length of the bus to determine the worst-case crosstalk. The measurement should be made for both the positive and the negative transition of the drive signal.

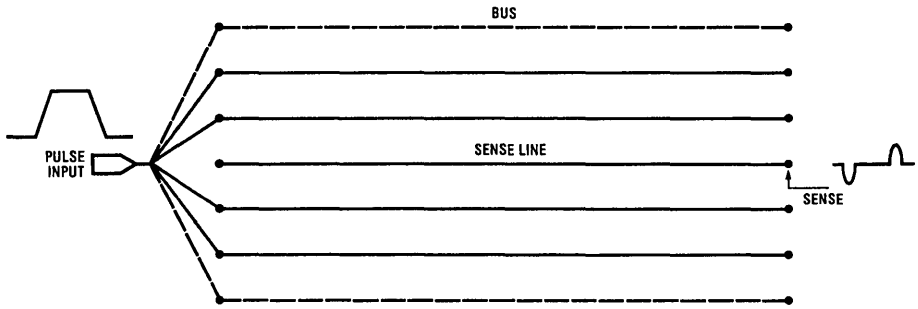
THE TERMINATION

A properly terminated transmission line has no reflections. But a practical microcomputer bus is neither a perfect transmission line nor is it properly terminated under all conditions. The capacitive loading at discrete locations, such as a used card slot, act as sources of reflection. However, in the limiting case when the bus is uniformly populated with a large number of modules, the bus behaves like a lower impedance transmission line. The loaded impedance 'Z_L' of the bus is given by the expression:

$$Z_L = \frac{Z}{\sqrt{1 + C_L/C_1}} \tag{8}$$

where Z = unloaded line impedance

Unfortunately, uniform loading of the bus is not guaranteed at all times and even if it were (by dummy loading of



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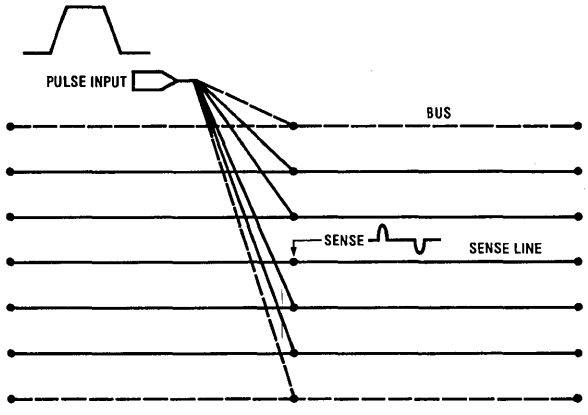
Note: All lines terminated at both ends (not shown)

FIGURE 2. Worst-Case Far End Crosstalk Measurement



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Note: All lines terminated at both ends (not shown)

FIGURE 3. Worst-Case Near End Crosstalk Measurement

the unused slots) Z_L is usually too low for proper termination of the bus. For example, a 10 pF per module loading of the 100Ω microstrip bus at 0.6" spacing results in a Z_L = 30Ω. One such termination at each end will require a 200 mA drive capacity on the bus driver for a nominal 3V swing. Such large drive currents and low value terminations increase the power dissipation of the system significantly in addition to causing other problems such as increased ground drop, inductive drops in traces due to large current being switched, etc. As a compromise the bus is usually terminated at an impedance higher than Z_L but less than or equal to Z. Consequently, there is always some amount of reflection present. For a perfect transmission line the reflection coefficient 'Γ' is given by the well known expression:

$$\Gamma = \frac{Z - R_t}{Z + R_t} \tag{9}$$

where Z = impedance of the bus

R_t = termination resistance

The net effect, in the general case of a nonuniformly loaded bus, is that it may take several round trip bus delays after a bus driver output transition, before the quiescent voltage level is established. However, this delay is avoided by using a bus driver that has sufficient drive to generate a large enough voltage step during the first transition to cross well beyond the receiver threshold region under the worst-case load conditions.

Figure 4 illustrates the driver output waveform under such a condition. Here the fully loaded bus (with Z_L = 30Ω), of the previous example, is driven by the DS3662 bus transceiver at the mid point. The driver is actually driving two transmission lines of Z_L = 30Ω in either direction from the middle and hence the initial step is given by:

$$V1 = \left(\frac{Z_L}{2}\right) 2I_S \tag{10}$$

where I_S = Standing current on the bus due to each termination

For the DS3662, the termination can be designed for $2I_S$ = 100 mA and therefore:

V1 = (30/2)100 = 1.5V

This value of the initial swing is large enough to cross the narrow threshold region of the receiver as shown and therefore no waiting period is required for the reflections to build up the output high level. On the negative transition the problem is less critical due to the much higher sink capability of the DS3662 during pull down.

Reflections can also be caused by resistive loading of the bus by the DC input current of the receiver. The resulting reflectoin coefficient (Γ) is given by the expression:

$$\Gamma = -\tfrac{1}{2}\left(\frac{I_R}{I_S}\right) \tag{11}$$

where I_R = receiver input current

Having a receiver with a high input impedance not only makes this component of reflection insignificant but also reduces the DC load on the driver, allowing the use of lower value termination resistors. This is particularly true when a large number of modules are connected to the bus.

The design implications of the above discussion may be summarized as follows:

1. If the driver has adequate drive to produce the necessary voltage swing under the worst-case loading (Z_L/2), reflections do not restrict the bus performance. This translates to a 100 mA minimum drive requirement for a typical microstrip bus.

2. If the drive is insufficient, time should be allowed for the reflections to build up the voltage level before the data is sampled.

3. For signals such as clock, strobe, etc., wherein the edge is used for triggering events, it is mandatory that the driver meet the above drive requirements if delayed or multiple triggering is to be avoided.

4. An ideal TTL bus transceiver should have at least a 100 mA drive, a high input impedance receiver with a narrow threshold uncertainty region.

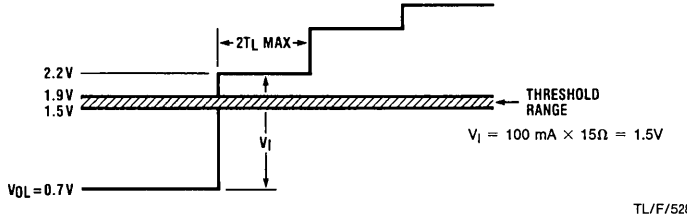

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FIGURE 4. Worst-Case DS3662 Output Transition for Z_L = 15Ω and R_T = 50Ω

THE DS3662 TRANSCEIVER

The DS3662 quad trapezoidal bus transceiver has been designed specifically to minimize the noise problems discussed previously. The driver generates precise trapezoidal waveforms that reduce crosstalk and the receiver uses a low pass filter to reject noise pulses having pulse widths up to the maximum driver output transition times. Precision output circuitry optimizes noise immunity without sacrificing the high data rate capability of Schottky transceivers.

Figure 5 shows the recommended configuration for microcomputer buses. The use of a 3.4V source with a single termination resistor at each end reduces the average power dissipation of the bus. However, a two resistor termination connected between the line and the power rails, having the same Thevenin's equivalent, can be substituted for lower cost.

Using a Miller integrator circuit, the driver generates a linearly rising and falling waveform with a constant slew rate of 0.2 V/ns *(Figure 6)*. This corresponds to a nominal transition time of 15 ns. *Figure 7* compares the output waveform of a typical high speed driver to that of DS3662 under different load conditions. It should be noted that even under heavy loading, the regular drivers have peak slew rates that are much higher than the average. On the other hand, the trapezoidal waveform has a much lower slew rate with only a slight increase in the transition time. Such an increase in the transition time has little or no effect on the data rates. In fact, the high fidelity of the DS3662 driver output waveform allows pulse widths as low as 20 ns to be transmitted on the bus.

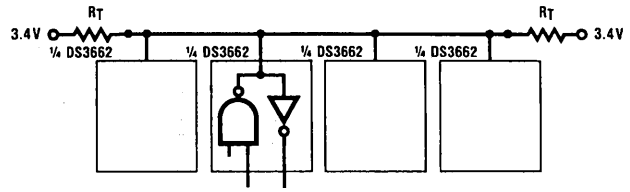


FIGURE 5. Recommended Bus Termination for Heavily Loaded Microstrip Backplanes

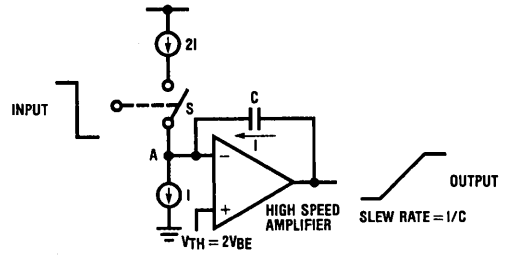
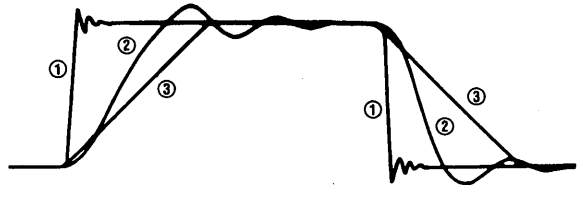


FIGURE 6. DS3662 Driver



Note 1: Typical high speed driver output unloaded; $t_r = t_f \approx 3$ ns

Note 2: Typical high speed driver output loaded; $t_r = t_f \approx 10$ ns

Note 3: Typical outupt of controlled slew rate driver which is load independent; $t_r = t_f \approx 15$ ns

FIGURE 7. Waveform Comparison

The receiver consists of a low pass filter followed by a high speed comparator, with a typical threshold of 1.7V *(Figure 8)*. The noise immunity of the receiver is specified in terms of the width of a 2.5V pulse that is guaranteed to be rejected by the receiver. The receiver typically rejects a 20 ns pulse going positive from the ground level or going negative from the 3.4V logic 1 level. The receiver threshold lies within a specified 400 mV region over the supply and temperature range and is centered between the low and high levels of the bus for a symmetrical noise margin.

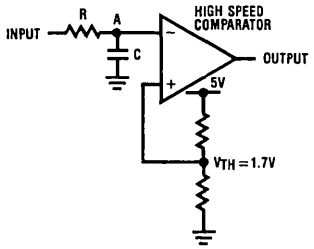


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FIGURE 8. DS3662 Receiver

Other features of the device include a 100 μA maximum DC bus loading specification under power ON or OFF condition and a glitch-free power up/down protection on the bus output.

Waveforms in *Figure 9* demonstrate the ability of the receiver to distinguish the trapezoidal signal from noise. Here the receiver rejects a noise pulse of 19 ns width, while accepting a narrower signal pulse (16 ns) of the same peak amplitude (the signal is triangular because of the pulse width which is smaller than the transition time).

The real-world performance of the DS3662 transceiver shows an order of magnitude improvement in noise immunity over conventional transceivers under actual operating conditions (Reference #3). The controlled rise and fall times on the driver output significantly reduces both near end and the far end crosstalk. As expected, the pulse discrimination at the receiver input virtually eliminates the far end crosstalk, even on extremely long buses (over 100 feet). The near end crosstalk, which is particularly severe on the state of the art backplanes due to the tight spacing between the signal lines, is easily accommodated by the large percentage noise margin (>75%) provided by the receiver.

Field reports indicate that the DS3662 not only solves those mysterious intermittent failure problems in mini and microcomputer systems, but also helps them meet the new FCC emission requirements due to the reduced RF radiation from the bus.

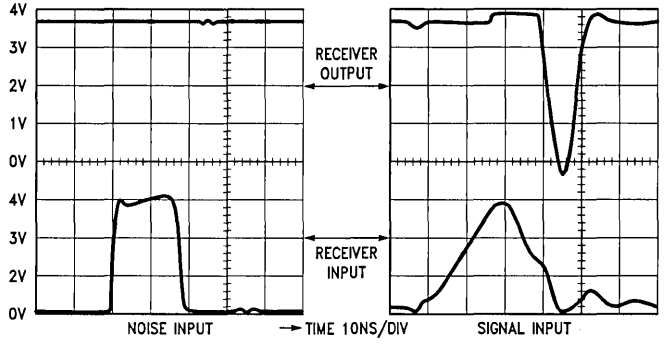

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FIGURE 9. DS3662 Receiver Response

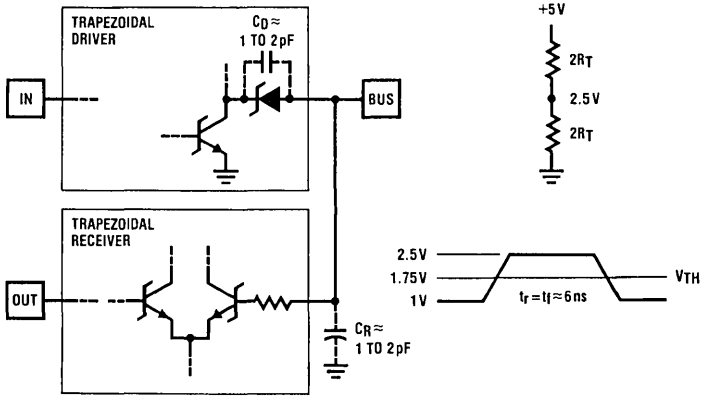

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FIGURE 10. High Speed Bus Transceiver with Low Output Loading for MicroComputer Backplanes

WHAT NEXT?

Since crosstalk scales with the signal amplitude, reducing the signal swing has not effect on the noise immunity as long as the percentage noise margin remains the same. On the other hand, there are several advantages in having lower signal swing. It reduces the drive current requirement of the driver thus reducing its output capacitance. Lower capacitive loading on the bus decreases its impedance reducing the drvie requirement even further. Having a lower current drive not only reduces the power dissipated at the terminations but also allows better matching of the termination due to the increased line impedance. In the ideal limiting case the driver has negligible loading effect on the bus and thus allows perfect termination under all load conditions.

In practice however, there are some obvious limitations. The receiver thresholds have to be maintained within tighter limits at lower signal swings to maintain the same percentage noise margin. Also, the capacitive loading is difficult to reduce beyond a certain point, due to the diminishing return in the way of lower current rating, as the loaded bus impedance approaches the unloaded impedance. However, the capacitance of an open collector driver output can be reduced significantly by using a Schottky diode as shown in *Figure 10.* The diode isolates the driver capacitance when the output is disabled. Using reduced signal swings and precise receiver thresholds, such a transceiver can provide significant improvements in microcomputer bus performance. The transceiver design presented in *Figure 10* is being considered for incorporation into the Futurebus standard by the IEEE.

CONCLUSION

A well designed bus transceiver goes a long way in improving the noise immunity of a single-ended TTL bus. Further improvements in bus performance may come from the use of reduced voltage swings and better transceiver designs for lower bus loading and tighter receiver threshold limits. Although such approaches may not be TTL compatible, the improvement in performance gained may indeed justify a new standard for bus transceivers.

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1) Bill Fowler, *"Transmission Line Characteristics,"* National Semiconductor—Application Note 108, May 1974.

2) A. Feller, H. P. Kaupp, and J. J. Digiacomo, *"Crosstalk And Reflections In High Speed Digital Systems,"* proceedings—Fall Joint Computer Conference, pp. 511–525, 1965

3) R. V. Balakrishnan, *"Bus Optimizer,"* National Semiconductor—Application Note 259, April 1981

4) David Montgomery, *"Borrowing RF Techniques For Digital Design,"* Computer Design, pp. 207–217, May 1982

5) R. V. Balakrishnan, *"Eliminating Crosstalk Over Long Distance Busing,"* Computer Design, pp. 155–162, March 1982

National Semiconductor Corporation

DS3666 IEEE-488 GPIB Transceiver

General Description

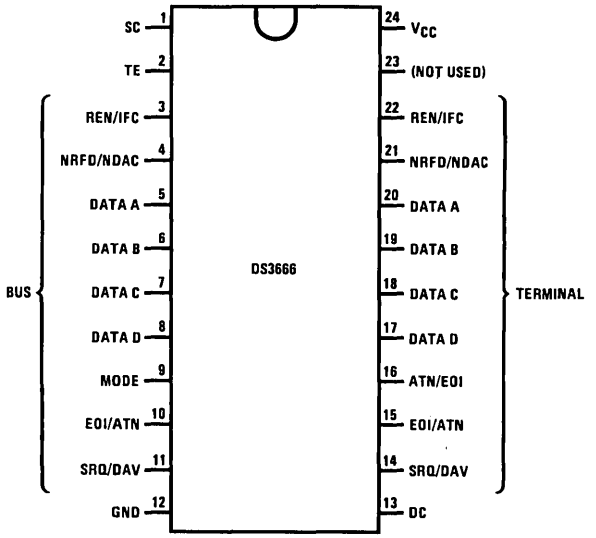
The DS3666 is a high-speed Schottky 8-channel bi-directional transceiver designed to interface TTL/MOS logic to the IEEE Standard 488-1978 General Purpose Interface Bus. PNP inputs are used at all driver inputs for minimum loading, and hysteresis is provided at all receiver inputs for added noise margin. The IEEE-488 required bus termination is provided internally with an active turn-off feature which disconnects the termination from the bus when V_{CC} is removed. A power up/down protection circuit is included at all bus outputs to provide glitch-free operation during V_{CC} power up or down. Implementing the IEEE-488 bus interface is accomplished by connecting two DS3666 devices together using the expansion control inputs provided. Each device is assigned to 4 data channels and 4 management signal channels to achieve the 16-line format.

Features

- 8-channel bi-directional non-inverting transceivers
- Bi-directional control implemented with TRI-STATE® output design
- Meets IEEE Standard 488-1978
- High speed Schottky design
- Low power consumption
- High impedance PNP inputs (drivers)
- 500 mV (typ) input hysteresis (receivers)
- On-chip bus terminators
- No bus loading when V_{CC} is removed
- Power up/down protection (glitch-free)
- Mode control implements 2-device expansion for complete IEEE-488 interface configuration
- Accommodates multi-controller systems

Connection Diagram

Dual-In-Line Package



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Top View

Order Number DS3666N
See NS Package Number N24C

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage, V_{CC}	7.0V
Input Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C Molded Package	2005 mW
Lead Temperature (Soldering, 4 sec.)	260°C

*Derate molded package 16.0 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.75	5.25	V
Ambient Temperature (T_A)	0	70	°C
Output Low Current (I_{OL})			
Bus		48	mA
Terminal		16	mA

Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter		Conditions		Min	Typ	Max	Units
V_{IH}	High-Level Input Voltage				2			V
V_{IL}	Low-Level Input Voltage						0.8	V
V_{IK}	Input Clamp Voltage		I_I = −18 mA			−0.8	−1.5	V
V_{HYS}	Input Hysteresis	Bus			400	500		mV
V_{OH}	High-Level Output Voltage	Terminal	I_{OH} = −800 μA		2.7	3.5		V
		Bus (Note 5)	I_{OH} = −5.2 mA		2.5	3.4		
V_{OL}	Low-Level Output Voltage	Terminal	I_{OL} = 16 mA			0.3	0.5	V
		Bus	I_{OL} = 48 mA			0.4	0.5	
I_{IH}	High-Level Input Current	Terminal and Control Inputs	V_I = 5.5V			0.2	100	μA
			V_I = 2.7V			0.1	20	
I_{IL}	Low-Level Input Current		V_I = 0.5V			−10	−100	μA
V_{BIAS}	Terminator Bias Voltage at Bus Port	Bus	Driver Disabled	$I_{I(bus)}$ = 0 (No Load)	2.5	3.0	3.7	V
I_{LOAD}	Terminator Bus Loading Current		Driver Disabled	$V_{I(bus)}$ = −1.5V to 0.4V	−1.3			mA
				$V_{I(bus)}$ = 0.4V to 2.5V	0		−3.2	
				$V_{I(bus)}$ = 2.5V to 3.7V			2.5 −3.2	
				$V_{I(bus)}$ = 3.7V to 5V	0		2.5	
				$V_{I(bus)}$ = 5V to 5.5V	0.7		2.5	
			V_{CC} = 0, $V_{I(bus)}$ = 0V to 2.5V				40	μA
I_{OS}	Short-Circuit Output Current	Terminal	V_I = 2V, V_O = 0V (Note 4)		−15	−35	−75	mA
		Bus (Note 5)			−35	−75	−150	
I_{CC}	Supply Current		V_I = 0.8V, SC = 2.0V, TE = 2.0V, DC = 2.0V, Mode = 2.0V, ATN/EOI = 2.0V			90	135	mA
C_{IN}	Bus-Port Capacitance	Bus	V_{CC} = 5V or 0V, V_I = 0V to 2V, f = 1 MHz			20	30	pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified, min/max limits apply across the 0°C to +70° temperature range and the 4.75V to 5.25V power supply range. All typical values are for T_A = 25°C and V_{CC} = 5.0V.

Note 3: All currents into device pins are shown as positive; all currents out of device pins are shown as negative; all voltages are referenced to ground, unless otherwise specified. All values shown as max or min are so classified on absolute value basis.

Note 4: Only one output at a time should be shorted.

Note 5: This characteristic does not apply to the NRFD/NDAC bus output since it is open collector.

Switching Characteristics V_{CC} = 5.0V ±5%, T_A = 0°C to 70°C (Note 1)

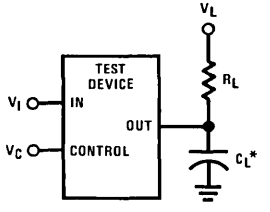
Symbol	Parameter	From	To	Conditions	Min	Typ	Max	Units
t_{PLH}	Propagation Delay Time, Low to High Level Output	Terminal	Bus	V_L = 2.3V, R_L = 38.3Ω, C_L = 30 pF *(Figure 1)*		10	20	ns
t_{PHL}	Propagation Delay Time, High to Low Level Output					14	20	
t_{PLH}	Propagation Delay Time, Low to High Level Output	Bus	Terminal	V_L = 5.0V, R_L = 240Ω, C_L = 30 pF *(Figure 2)*		14	20	ns
t_{PHL}	Propagation Delay Time, High to Low Level Output					10	20	
t_{PZH}	Output Enable Time to High Level	Control Inputs (Note 2) (Note 3)	Bus	V_I = 3.0V, V_L = 0V, R_L = 480Ω, C_L = 15 pF *(Figure 1)*		23	40	ns
t_{PHZ}	Output Disable Time from High Level					15	27	
t_{PZL}	Output Enable Time to Low Level			V_I = 0V, V_L = 2.3V, R_L = 38.3Ω, C_L = 15 pF *(Figure 1)*		28	48	ns
t_{PLZ}	Output Disable Time from Low Level					17	35	
t_{PZH}	Output Enable Time to High Level	Control Inputs (Note 2) (Note 3)	Terminal	V_I = 3.0V, V_L = 0V, R_L = 3 kΩ, C_L = 15 pF *(Figure 1)*		18	45	ns
t_{PHZ}	Output Disable Time from High Level					22	33	
t_{PZL}	Output Enable Time to Low Level			V_I = 0V, V_L = 5V, R_L = 280Ω, C_L = 15 pF *(Figure 1)*		28	56	ns
t_{PLZ}	Output Disable Time from Low Level					20	35	
t_{PZH}	Output Pull-Up Enable Time	ATN/EOI Input (Note 2)	Bus Data Outputs	V_I = 3V, V_L = 0V, R_L = 480Ω, C_L = 15 pF *(Figure 1)*		10	20	ns
t_{PHZ}	Output Pull-Up Disable Time					10	20	

Note 1: Typical values are for V_{CC} = 5.0V and T_A = 25°C and are meant for reference only.

Note 2: Refer to functional truth table for control input definition.

Note 3: Test configuration should be connected to only one transceiver at a time due to the high current stress caused by the V_I voltage source when the output connected to that input becomes active.

Switching Load Configurations



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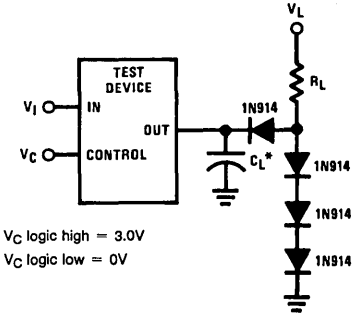
V_C logic high = 3.0V
V_C logic low = 0V
*C_L includes jig and probe capacitance

FIGURE 1



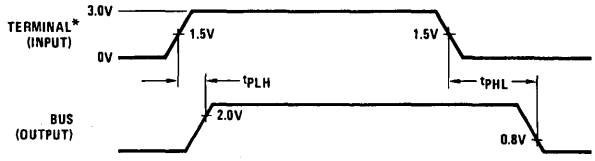
V_C logic high = 3.0V
V_C logic low = 0V
*C_L includes jig and probe capacitance

TL/F/5244–6

FIGURE 2

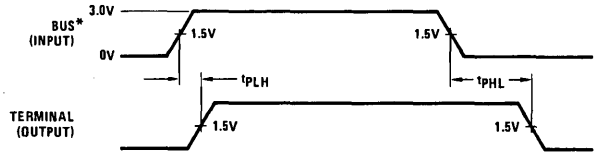
Switching Waveforms

Transmit Propagation Delays



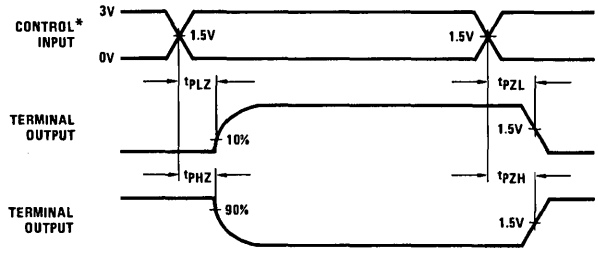
TL/F/5244–7

Receive Propagation Delays



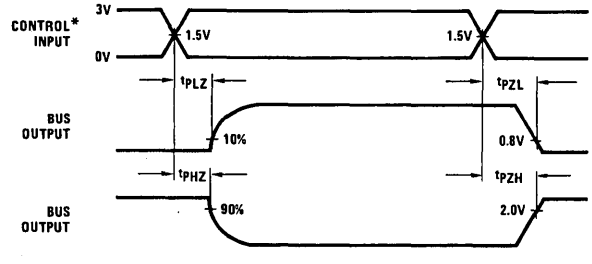
TL/F/5244–8

Terminal Enable/Disable Times



TL/F/5244–9

Bus Enable/Disable Times

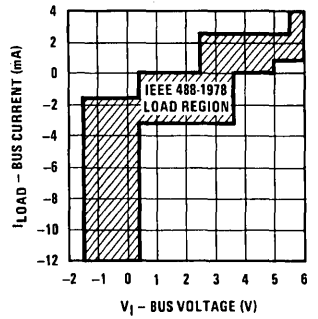


TL/F/5244–10

*Input signal: f = 1.0 MHz, 50% duty cycle, $t_r = t_f \leq 5$ ns

Performance Characteristics

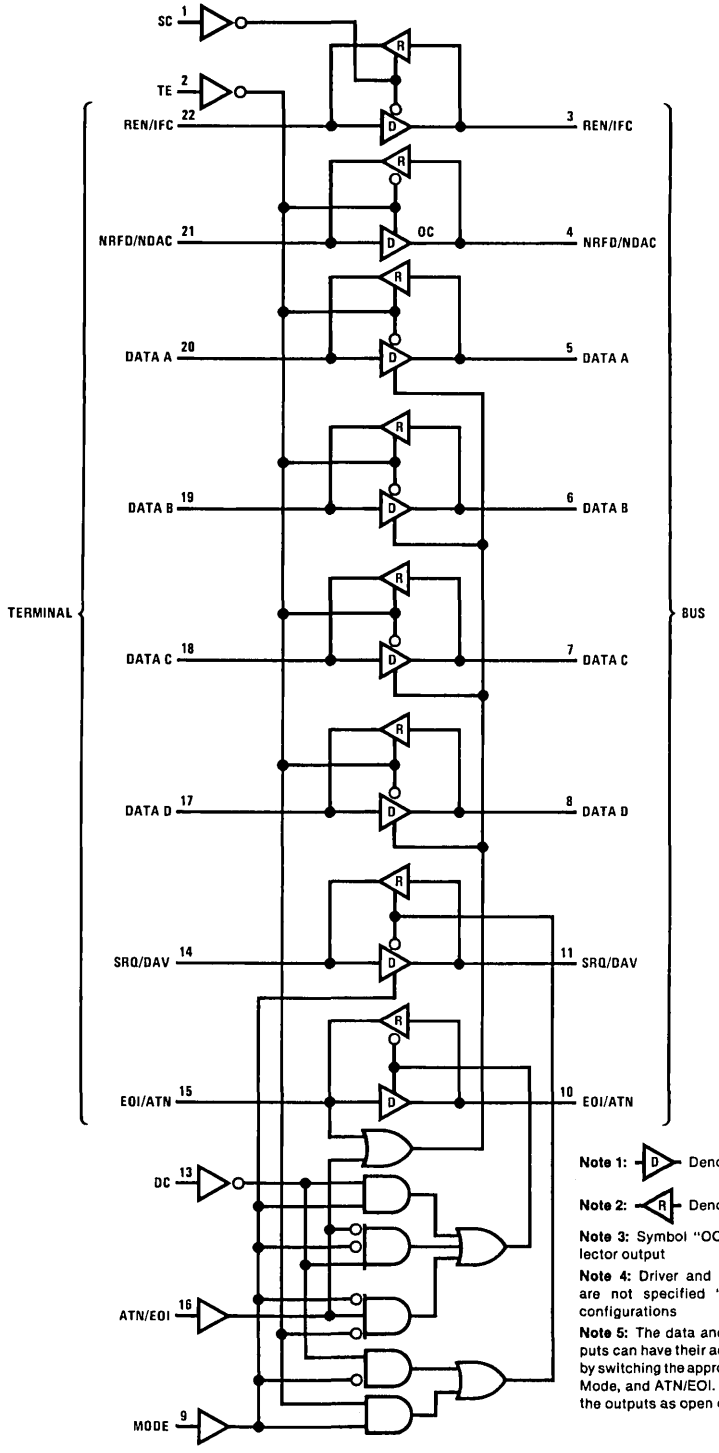
Bus Port Load Characteristic



Refer to Electrical Characteristics Table

TL/F/5244–11

Logic Diagram



Note 1: D Denotes driver

Note 2: R Denotes receiver

Note 3: Symbol "OC" specifies open collector output

Note 4: Driver and receiver outputs that are not specified "OC" are totem-pole configurations

Note 5: The data and SRQ/DAV driver outputs can have their active pull-ups disabled by switching the appropriate inputs EOI/ATN, Mode, and ATN/EOI. This mode configures the outputs as open collector.

TL/F/5244–2

Device Truth Tables

Transceiver Direction

Control Input Level					Transceiver Signal Direction				
Mode	SC	TE	DC	ATN/EOI	REN/IFC	NRFD/NDAC	SRQ/DAV	EOI/ATN	Data
X	H	X	X	X	T				
X	L	X	X	X	R				
X	X	H	X	X		R			T
X	X	L	X	X		T			R
H	X	H	X	X			T		
H	X	L	X	X			R		
H	X	X	H	X				R	
H	X	X	L	X				T	
L	X	X	H	X			T		
L	X	X	L	X			R		
L	X	H	X	H				T	
L	X	L	X	H				R	
L	X	X	H	L				R	
L	X	X	L	L				T	

Output Configuration

Control Input Level			Transceiver Bus Output Configuration	
Mode	ATN/EOI	EOI/ATN*	Data	SRQ/DAV
X	H	H	Totem-Pole	
X	H	L	Totem-Pole	
X	L	H	Totem-Pole	
X	L	L	Open Collector	
H	X	X		Totem-Pole
L	X	X		Open Collector

H = High level input

L = Low level input

X = Don't care

T = Transmit, i.e., signal outputted to bus

R = Receive, i.e., signal outputted to terminal

*The EOI/ATN transceiver signal level is sensed for internal logic control of bus port data output configuration.

Functional Description

The DS3666 is an 8-channel bi-directional transceiver with internal logic specifically configured to implement the IEEE-488 bus interface. Expansion logic is included so that two DS3666 devices may be interconnected to form the complete 16-line interface. This approach is equivalent to pairing the DS75160A and the DS75162A devices to implement the 16-line bus. The port connections to the bus lines have internal terminators, in accordance with the IEEE-488 Standard, that are deactivated when the device is powered down. This feature guarantees no bus loading when V_{CC} = 0V. The bus port data outputs have a control mode that either enables or disables the active upper stage of the totem-pole configuration. When the upper stage is disabled, the data outputs operate as open collector outputs, which are necessary for parallel polling. In compliance with the system organization of the management signal lines, the NRFD/NDAC bus port output is a fixed open collector configuration. Also, the SRQ/DAV bus port output is configured so that the SRQ output is open collector in the expanded implementation of the device. Transceiver direction control is divided into three groups. The NRFD/NDAC and data lines are controlled by the TE input. The REN/IFC line is controlled by the SC input. And the EOI/ATN and SRQ/DAV lines are controlled by the TE or DC input, depending on the expansion mode. A special case is the direction of the designated EOI line, which is a function of both the TE and DC inputs, as well as the logic level present on the ATN line.

Table of Signal Line Abbreviations

Signal Line Classification	Mnemonic	Definition
Control Signals	DC	Direction Control
	TE	Talk Enable
	SC	System Controller
Data I/O Ports	Data A, Data B, Data C, Data D	Bi-Directional Data Transceivers
Management Signals	ATN	Attention
	DAV	Data Valid
	EOI	End or Identify
	IFC	Interface Clear
	NDAC	Not Data Accepted
	NRFD	Not Ready for Data
	REN	Remote Enable
	SRQ	Service Request

IEEE-488 Interface Configuration Truth Tables (see Configuration Diagram)

Management Signals

Control Input Level				Transceiver Signal Direction						
SC	TE	DC	ATN*	EOI	REN	IFC	SRQ	NRFD	NDAC	DAV
H	H	H		R	T	T	T	R	R	T
H	H	L		T	T	T	R	R	R	T
H	L	H		R	T	T	T	T	T	R
H	L	L		T	T	T	R	T	T	R
L	H	H		R	R	R	T	R	R	T
L	H	L		T	R	R	R	R	R	T
L	L	H		R	R	R	T	T	T	R
L	L	L		T	R	R	R	T	T	R
X	H	X	H		T					
X	L	X	H		R					
X	X	H	L		R					
X	X	L	L		T					

Data Signals

Control Input Level			Data Transceivers	
ATN	EOI	TE	Direction	Bus Port Configuration
X	X	L	R	Input
H	H	H	T	Totem-Pole Output
H	L	H	T	Totem-Pole Output
L	H	H	T	Totem-Pole Output
L	L	H	T	Open Collector Output

H = High level input

L = Low level input

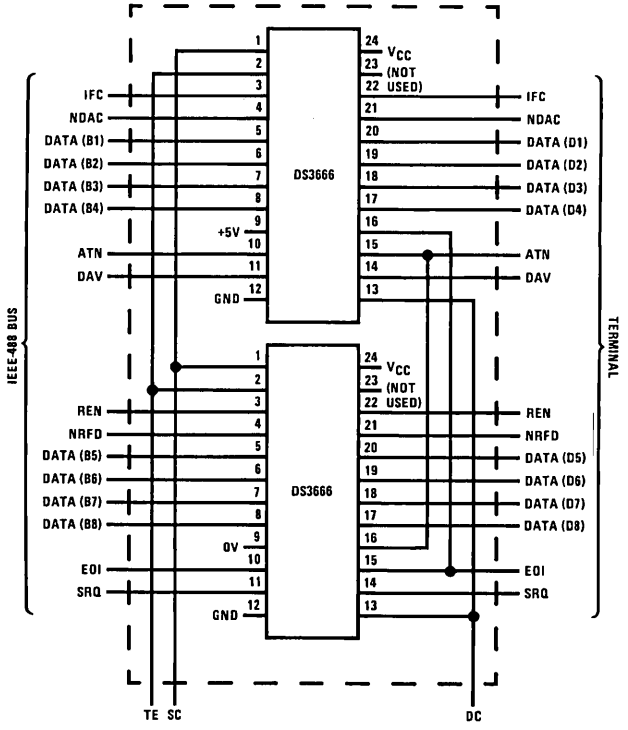
X = Don't care

T = Transmit, i.e., signal outputted to bus

R = Receive, i.e., signal outputted to terminal

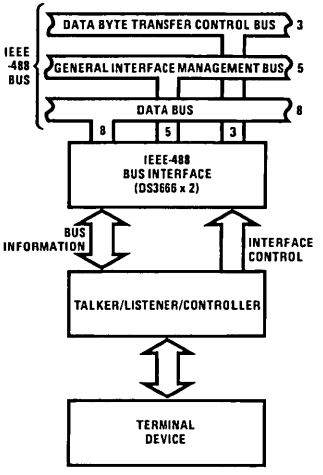
*The ATN signal level is sensed for internal multiplex control of EOI transmission direction logic.

IEEE-488 Interface Configuration Implementation Using the DS3666



TL/F/5244–3

Terminal Interface Block Diagram



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IEEE-488 Specification Summary

Logic Nomenclature. When referring to the IEEE-488 specification publication, the following logic conventions are used:

1) A "true" condition corresponds to a logic low signal level.
2) A "false" condition corresponds to a logic high signal level.

Bus Specification. The IEEE-488 bus is comprised of 16 signal lines intended for digital data exchange at a maximum rate of 1 Mbaud and for a maximum transmission path length of 20 meters.

Terminal Devices. The IEEE-488 bus will support a maximum of 15 interconnected devices. These devices may be configured in four different modes of operation:

1) Talk only (e.g., counter)
2) Listen only (e.g., printer)
3) Listen and talk (e.g., multimeter)
4) Listen, talk, and control (e.g., calculator)

Data Bus. The data bus has 8 signal lines, denoted DIO_1 through DIO_8. These lines carry data and interface messages in a bi-directional asynchronous, bit parallel, byte serial form.

Data Byte Transfer Control Bus. These 3 signal lines are used to control the transfer of data bytes across the data bus lines.

1) NRFD (Not Ready for Data). This signal originates from a listen device and indicates to a talker that a listen device is not ready to accept data.
2) DAV (Data Valid). This signal originates from a talker device and indicates to a listen device that data present on the data bus is valid.
3) NDAC (Not Data Accepted). This signal originates from a listen device and indicates to a talker device that data on the data bus has not been accepted.

General Interface Management Bus. These 5 signal lines provide general management of all bus operations.

1) ATN (Attention). This signal originates from a controller device and indicates to other devices on the bus how the data bus information is to be interpreted.
2) IFC (Interface Clear). This signal originates from a controller device and causes all interface logic to be set to a known state.
3) REN (Remote Enable). This signal originates from a controller device and is used in conjunction with other messages to tell a remote device which of two sources of information is to be used. The source is designated as being remote or local.
4) SRQ (Service Request). This signal is generated by a remote device to indicate to the controller device a need for attention.
5) EOI (End or Identify). This signal is generated by a talker device to indicate the end of a multibyte transfer. This signal may also originate from a controller, in conjunction with ATN to execute a polling sequence.

National Semiconductor Corporation

DS3667 TRI-STATE® Bidirectional Transceiver

General Description

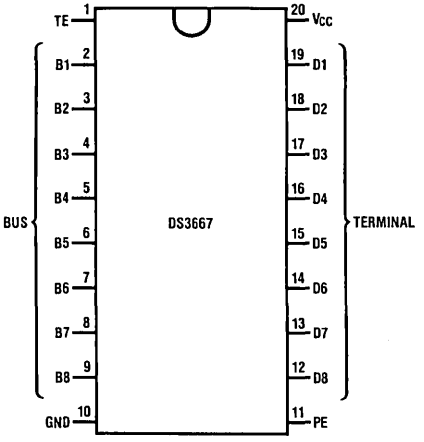
The DS3667 is a high-speed Schottky 8-channel bidirectional transceiver designed for digital information and communication systems. Pin selectable totem-pole/open collector outputs are provided at all driver outputs. This feature, together with the Dumb Mode which puts both driver and receiver outputs in TRI-STATE at the same time, means higher flexibility of system design. PNP inputs are used at all driver inputs for minimum loading, and hysteresis is provided at all receiver inputs for added noise margin. A power up/down protection circuit is included at all outputs to provide glitch-free operation during V_{CC} power up or down.

Features

- 8-channel bidirectional non-inverting transceivers
- Bidirectional control implemented with TRI-STATE output design
- High speed Schottky design
- Low power consumption
- High impedance PNP inputs (drivers)
- Pin selectable totem-pole/open collector outputs (drivers)
- 500 mV (typ) input hysteresis (receivers)
- Power up/down protection (glitch-free)
- Dumb Mode capability

Connection Diagram

Dual-In-Line Package

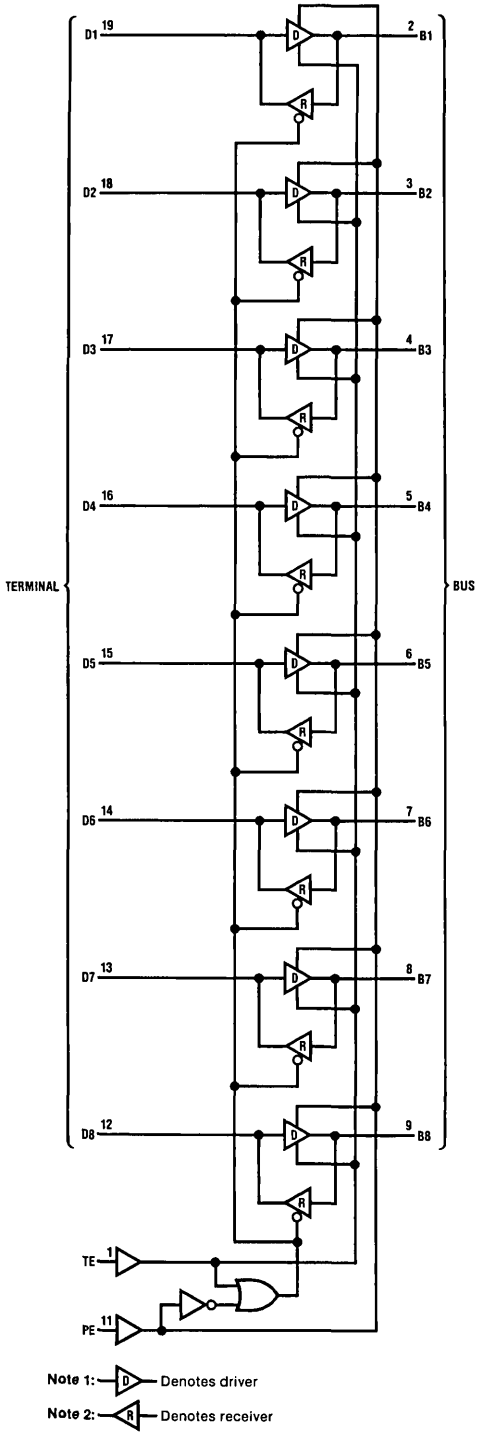


TL/F/5245–1

Top View

Order Number DS3667N
See NS Package Number N20A

Logic Diagram



Note 1: D — Denotes driver

Note 2: R — Denotes receiver

TL/F/5245–2

Functional Truth Table

Control Input Level		Data Transceivers		
TE	**PE**	**Mode**	**Bus Port**	**Terminal Port**
H	H	T	Totem-Pole Output	Input
H	L	T	Open Collector Output	Input
L	H	R	Input	Output
L	L	D	TRI-STATE	TRI-STATE

H: High Level Input
L: Low Level Input
T: Transmitting Mode
R: Receiving Mode
D: Dumb Mode

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage (V_{CC})	7.0V
Input Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C Molded Package	1832 mW
Lead Temperature (Soldering, 4 seconds)	260°C

*Derate molded package 14.7 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
V_{CC}, Supply Voltage	4.75	5.25	V
T_A, Ambient Temperature	0	70	°C
I_{OL}, Output Low Current			
Bus		48	mA
Terminal		16	mA

Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter		Conditions	Min	Typ	Max	Units
V_{IH}	High Level Input Voltage			2			V
V_{IL}	Low Level Input Voltage					0.8	V
V_{IK}	Input Clamp Voltage		$I_I = -18$ mA		−0.8	−1.5	V
V_{HYS}	Input Hysteresis	Bus		400	500		mV
V_{OH}	High Level Output Voltage	Terminal	$I_{OH} = -800\ \mu A$	2.7	3.5		V
		Bus	$I_{OH} = -5.2$ mA	2.5	3.4		
V_{OL}	Low Level Output Voltage	Terminal	$I_{OL} = 16$ mA		0.3	0.5	V
		Bus	$I_{OL} = 48$ mA		0.4	0.5	
I_{IH}	High Level Input Current	TE, PE	$V_I = 5.5V$		0.2	100	μA
			$V_I = 2.7V$		0.1	20	
		Terminal and Bus	$V_I = 4V$			200	
I_{IL}	Low Level Input Current	Terminal and TE, PE	$V_I = 0.5V$		−10	−100	μA
		Bus			−0.4	−1.0	mA
I_{OS}	Short Circuit Output Current	Terminal	$V_I = 2V$, $V_O = 0V$ (Note 4)	−15	−35	−75	mA
		Bus		−50	−120	−200	
I_{CC}	Supply Current		Transmit, TE = 2V, PE = 2V, $V_I = 0.8V$		75	100	mA
			Receive, TE = 0.8V, PE = 2V, $V_I = 0.8V$		65	90	
C_{IN}	Bus-Port Capacitance	Bus	$V_{CC} = 0V$, $V_I = 0V$, f = 10 kHz (Note 5)		20	30	pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operations.

Note 2: Unless otherwise specified, min/max limits apply across the 0°C to +70°C temperature range and the 4.75V to 5.25V power supply range. All typical values are for $T_A = 25°C$ and $V_{CC} = 5.0V$.

Note 3: All currents into device pins are shown as positive; all currents out of device pins are shown as negative; all voltages are referenced to ground, unless otherwise specified. All values shown as max or min are so classified on absolute value basis.

Note 4: Only one output at a time should be shorted.

Note 5: This parameter is guaranteed by design. It is not a tested parameter.

Switching Characteristics V_{CC} = 5.0V ±5%, T_A = 0°C to +70°C (Note 1)

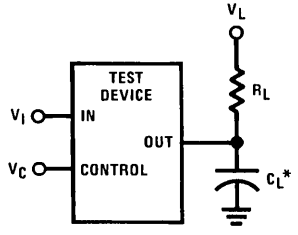
Symbol	Parameter	From	To	Conditions	Min	Typ	Max	Units
t_{PLH}	Propagation Delay Time, Low to High Level Output	Terminal	Bus	V_L = 2.3V, R_L = 38.3Ω, C_L = 30 pF *(Figure 1)*		10	20	ns
t_{PHL}	Propagation Delay Time, High to Low Level Output					14	20	ns
t_{PLH}	Propagation Delay Time, Low to High Level Output	Bus	Terminal	V_L = 5.0V, R_L = 240Ω, C_L = 30 pF *(Figure 2)*		15	20	ns
t_{PHL}	Propagation Delay Time, High to Low Level Output					10	20	ns
t_{PZH}	Output Enable Time to High Level	TE (Notes 2 and 3)	Bus	V_I = 3.0V, V_L = 0V, R_L = 480Ω, C_L = 15 pF *(Figure 1)*		19	30	ns
t_{PHZ}	Output Disable Time to High Level					15	20	ns
t_{PZL}	Output Enable Time to Low Level			V_I = 0V, V_L = 2.3V, R_L = 38.3Ω, C_L = 15 pF *(Figure 1)*		24	40	ns
t_{PLZ}	Output Disable Time to Low Level					17	30	ns
t_{PZH}	Output Enable Time to High Level	TE, PE (Notes 2 and 3)	Terminal	V_I = 3.0V, V_L = 0V, R_L = 3 kΩ, C_L = 15 pF *(Figure 1)*		19	35	ns
t_{PHZ}	Output Disable Time to High Level					17	25	ns
t_{PZL}	Output Enable Time to Low Level			V_I = 0V, V_L = 5V, R_L = 280Ω, C_L = 15 pF *(Figure 1)*		27	40	ns
t_{PLZ}	Output Disable Time to Low Level					17	30	ns
t_{PZH}	Output Pull-Up Enable Time	PE (Notes 2 and 3)	Bus	V_I = 3V, V_L = 0V, R_L = 480Ω, C_L = 15 pF *(Figure 1)*		10	20	ns
t_{PHZ}	Output Pull-Up Disable Time					10	20	ns

Note 1: All typical values are for T_A = 25°C, V_{CC} = 5V.

Note 2: Refer to Functional Truth Table for control input definition.

Note 3: Test configuration should be connected to only one transceiver at a time due to the high current stress caused by the V_I voltage source when the output connected to that input becomes active.

Switching Load Configurations

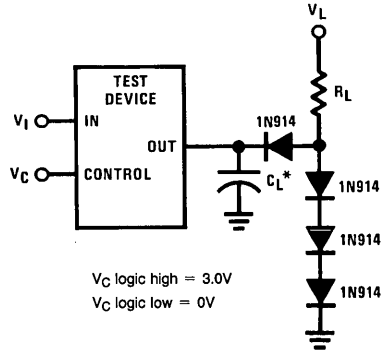


TL/F/5245–3

V_C logic high = 3.0V
V_C logic low = 0V

*C_L includes jig and probe capacitance

FIGURE 1



V_C logic high = 3.0V
V_C logic low = 0V

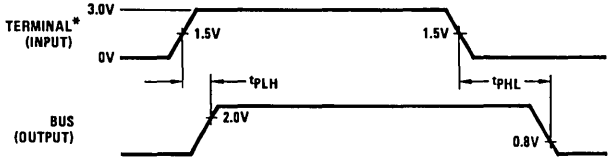
TL/F/5245–4

*C_L includes jig and probe capacitance

FIGURE 2

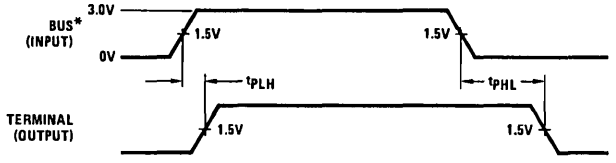
Switching Waveforms

Transmit Propagation Delays



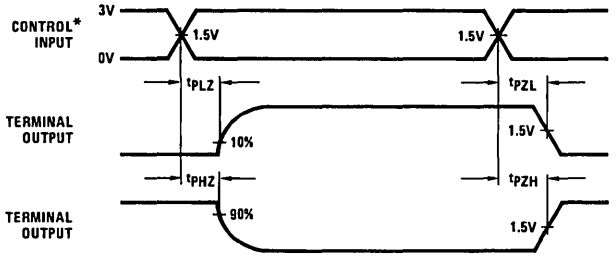
TL/F/5245–5

Receive Propagation Delays



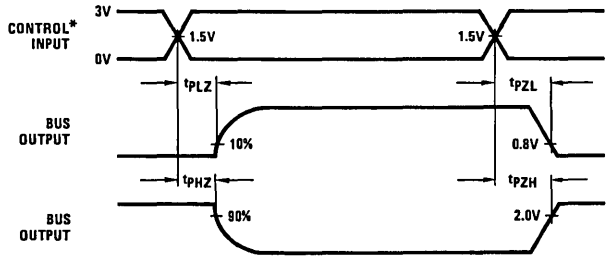
TL/F/5245–6

Terminal Enable/Disable Times



TL/F/5245–7

Bus Enable/Disable Times



TL/F/5245–8

*Input signal: f = 1.0 MHz, 50% duty cycle, $t_r = t_f \leq 5$ ns

National Semiconductor Corporation

PRELIMINARY

DS3862 Octal High Speed Trapezoidal Bus Transceiver

General Description

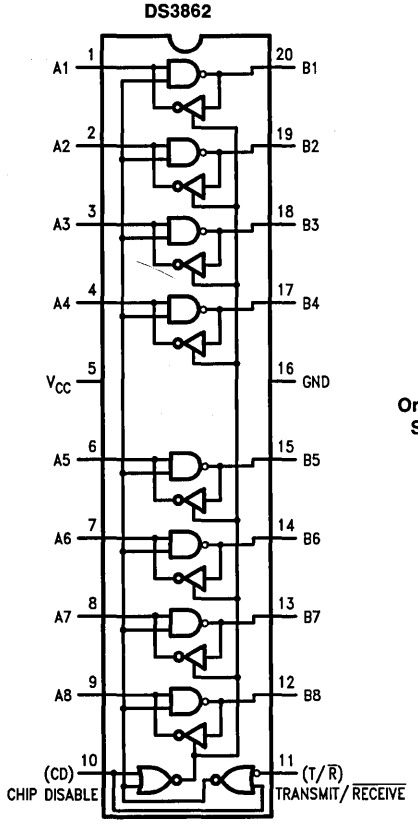
The DS3862 is an octal high speed schottky bus transceiver intended for use with terminated 120Ω impedance lines. It is specifically designed to reduce noise in unbalanced transmission systems. The open collector drivers generate precise trapezoidal waveforms with rise and fall times of 9 ns (typical), which are relatively independent of capacitive loading conditions on the outputs. This reduces noise coupling to the adjacent lines without any appreciable impact on the maximum data rate obtainable with high speed bus transceivers. In addition, the receivers use a low pass filter in conjunction with a high speed comparator, to further enhance the noise immunity. Tightly controlled threshold levels on the receiver provide equal rejection to both negative and positive going noise pulses on the bus.

The external termination is intended to be a 180Ω resistor from the bus to 5V logic supply, together with a 390Ω resistor from the bus to ground. The bus can be terminated at one or both ends.

Features

- Guaranteed A.C. specifications on noise immunity and propagation delay over the specified temperature and supply voltage range
- Temperature insensitive receiver thresholds track bus logic level and respond symmetrically to positive and negative going pulses
- Trapezoidal bus waveforms reduce noise coupling to adjacent lines
- Open collector driver output allows wire-or connection
- Advanced low power schottky technology
- Glitch free power up/down protection on driver and receiver outputs
- TTL compatible driver and control inputs, and receiver outputs
- Control logic is the same as the DS3896

Logic and Connection Diagram



Order Number DS3862J or DS3862N
See NS Package Number J20A or N20A

TL/F/8539–1

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	6V
Control Input Voltage	5.5V
Driver Input and Receiver Output	5.5V
Receiver Input and Driver Output	5.5V
Power Dissipation	1400 mW
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 4 seconds)	260°C

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage, V_{CC}	4.75	5.25	V
Operating Free Air Temperature	0	70	°C

Electrical Characteristics $0°C \le T_A \le 70°C$, $4.75V \le V_{CC} \le 5.25V$ unless otherwise specified (Notes 2 and 3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Driver and Control Inputs:						
V_{IH}	Logical "1" Input Voltage		2.0			V
V_{IL}	Logical "0" Input Voltage				0.8	V
I_I	Logical "1" Input Current	An = V_{CC}			1	mA
I_{IH}	Logical "1" Input Current	An = 2.4V			40	μA
I_{IL}	Logical "0" Input Current	An = 0.4V		−1	−1.6	mA
I_{IL}	CD & T/$\overline{R}$ Logical "0" Input Current	CD = T/$\overline{R}$ = 0.4V		−180	−400	μA
V_{CL}	Input Diode Clamp Voltage	Iclamp = −12 mA		−0.9	−1.5	V
Driver Output/Receiver Input						
V_{OLB}	Low Level Bus Voltage	An = T/$\overline{R}$ = 2V, Ibus = 100 mA		0.6	0.9	V
I_{IHB}	Logical "1" Bus Current	An = 0.8V, Bn = 4V, V_{CC} = 5.25V and 0V		10	100	μA
I_{ILB}	Logical "0" Bus Current	An = 0.8V, Bn = 0V, V_{CC} = 5.25V and 0V			100	μA
V_{TH}	Input Threshold	V_{CC} = 5V	1.5	1.7	1.9	V
Receiver Output						
V_{OH}	Logical "1" Output Voltage	Bn = 0.9V, I_{oh} = −400μA	2.4	3.2		V
V_{OL}	Logical "0" Output Voltage	Bn = 4V, I_{ol} = 16 mA		0.35	0.5	V
I_{OS}	Output Short Circuit Current	Bn = 0.9V	−40	−70	−100	mA
I_{CC}	Supply Current	V_{CC} = 5.25V		90	135	mA

Note 1: "Absolute Maximum Ratings" are those beyond which the safety of the device cannot be guaranteed. They are not meant to imply that device should be operated at these limits. The table of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to device ground unless otherwise specified.

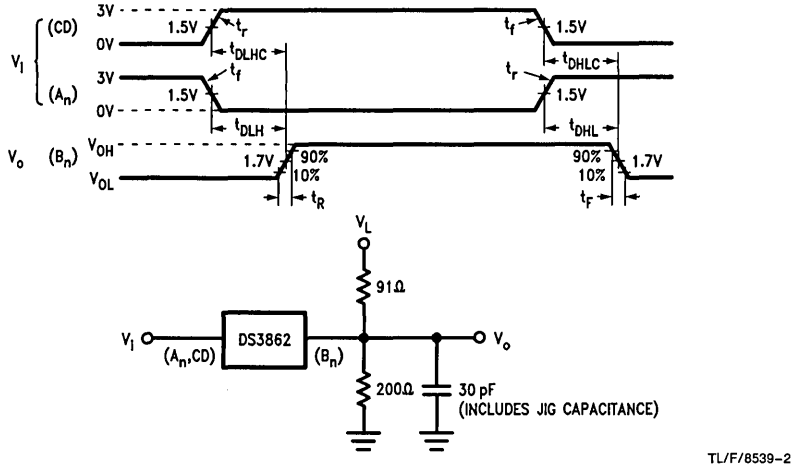
Note 3: All typicals are given for V_{CC} = 5V and T_A = 25°C.

Switching Characteristics $0°C \le T_A \le 70°C$, $4.75V \le V_{CC} \le 5.25V$ unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Driver:						
t_{DLH}	An to Bn	CD = 0.8V, T/$\overline{R}$ = 2.0V, VL = 5V (*Figure 1*)		12	20	ns
t_{DHL}				12	20	ns
t_{DLHC}	CD to Bn	An = T/$\overline{R}$ = 2.0V, VL = 5V, (*Figure 1*)		12	20	ns
t_{DHLC}				15	25	ns
t_{DLHT}	T/$\overline{R}$ to Bn	VCI = An, VC = 5V, (*Figure 2*)		20	30	ns
t_{DHLT}		CD = 0.8V, RC = 390Ω, CL = 30 pF RL1 = 91Ω, RL2 = 200Ω, VL = 5V		25	40	ns
t_R	Driver Output Rise Time	CD = 0.8V, T/$\overline{R}$ = 2V, VL = 5V (*Figure 1*)	4	9	20	ns
t_F	Driver Output Fall Time		4	9	20	ns
Receiver:						
t_{RLH}	Bn to An	CD = 0.8V, T/$\overline{R}$ = 0.8V (*Figure 3*)		15	25	ns
t_{RHL}				15	25	ns
t_{RLZC}	CD to An	Bn = 2.0V, T/$\overline{R}$ = 0.8V, CL = 5 pF RL1 = 390Ω, RL2 = NC, VL = 5V (*Figure 4*)		15	25	ns
t_{RZLC}		Bn = 2.0V, T/$\overline{R}$ = 0.8V, CL = 30 pF RL1 = 390Ω, RL2 = 1.6K, VL = 5V (*Figure 4*)		10	20	ns
t_{RHZC}		Bn = 0.8V, T/$\overline{R}$ = 0.8V, VL = 0V, RL1 = 390Ω, RL2 = NC, CL = 5 pF (*Figure 4*)		5	10	ns
t_{RZHC}		Bn = 0.8V, T/$\overline{R}$ = 0.8V, VL = 0V, RL1 = NC, RL2 = 1.6K, CL = 30 pF (*Figure 4*)		8	15	ns
t_{RLZT}	T/$\overline{R}$ to An	VCI = Bn, VC = 3.4V, RC = 39Ω CD = 0.8V, VL = 5V, RL1 = 390Ω, RL2 = NC, CL = 5 pF (*Figure 2*)		20	30	ns
t_{RZLT}		VCI = Bn, VC = 3.4V, RC = 39Ω, CD = 0.8V, VL = 5V, RL1 = 390Ω, RL2 = 1.6K, CL = 30 pF (*Figure 2*)		30	45	ns
t_{RHZT}		VCI = Bn, VC = 0V, RC = 39Ω CD = 0.8V, VL = 0V, RL1 = 390Ω, RL2 = NC, CL = 5 pF (*Figure 2*)		5	10	ns
t_{RZHT}		VCI = Bn, VC = 0V, RC = 39Ω, CD = 0.8V, VL = 0V, RL1 = NC RL2 = 1.6K, CL = 30 pF (*Figure 2*)		10	20	ns
t_{NR}	Receiver Noise Rejection Pulse Width	(*Figure 5*)	9	12		ns

Note: NC means open

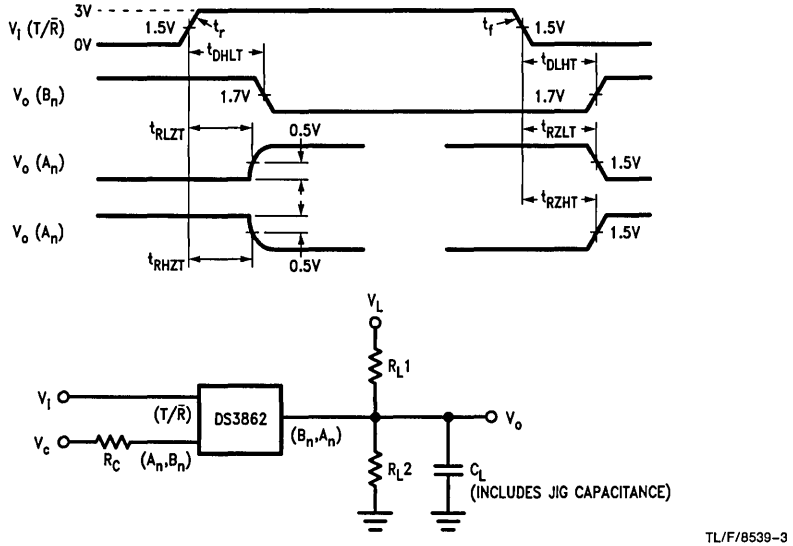
Switching Waveforms



TL/F/8539–2

Note: $t_r = t_f \leq 5$ ns from 10% to 90%

FIGURE 1. Driver Propagation Delays



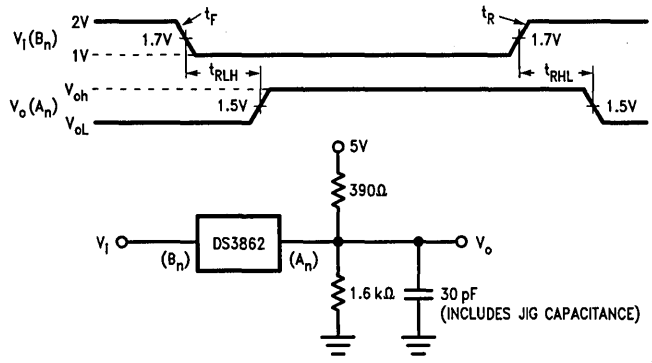
TL/F/8539–3

Note: $t_r = t_f \leq 5$ ns from 10% to 90%

FIGURE 2. Propagation Delay From T/$\overline{R}$ Pin to An or Bn.

2

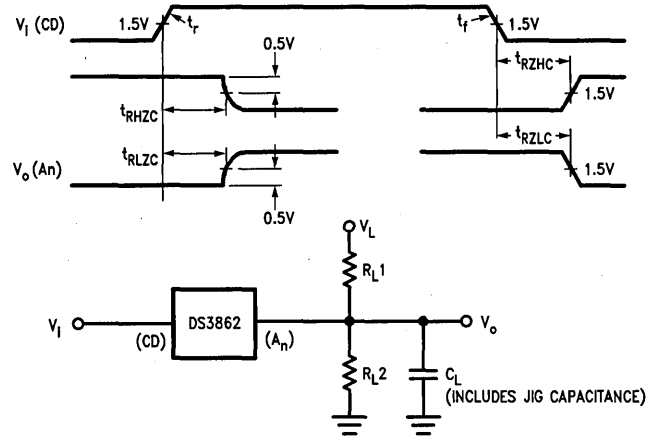
Switching Waveforms (Continued)



TL/F/8539–4

Note: $t_R = t_F \leq 10$ ns from 10% to 90%

FIGURE 3. Receiver Propagation Delays

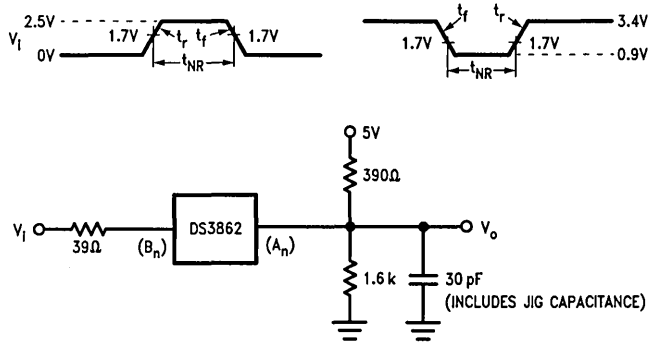


TL/F/8539–5

Note: $t_r = t_f \leq 5$ ns from 10% to 90%

FIGURE 4. Propagation Delay From CD Pin to An

Switching Waveforms (Continued)

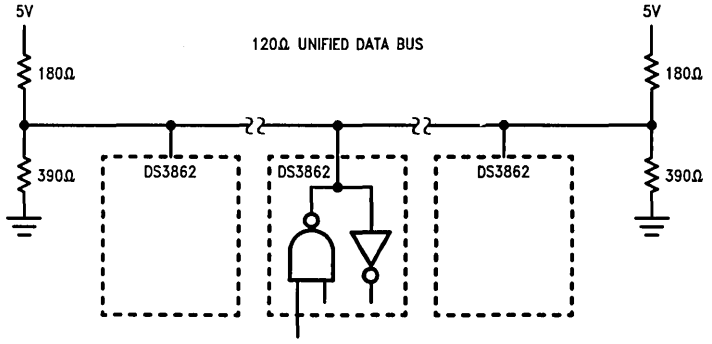


TL/F/8539–6

Note: $t_r = t_f = 2$ ns from 10% to 90%

FIGURE 5. Receiver Noise Immunity: No Response at Output Input Waveform.

Typical Application



TL/F/8539–7

National Semiconductor Corporation

PRELIMINARY

DS3890 BTL™ Octal Trapezoidal Driver
DS3892 BTL Octal TRI-STATE® Receiver
DS3898 BTL Octal Trapezoidal Repeater

General Description

The DS3890, DS3892 and DS3898 are advanced IEEE-896 Future Bus compatible devices designed specifically to overcome problems associated with driving densely populated backplanes. These products provide significant improvement in both speed and data integrity in comparison to conventional bus drivers and receivers. Their low output capacitance, low voltage swing and noise immunity features make them ideal for driving low impedance busses with minimum power dissipation.

The DS3890 and DS3898 feature open collector outputs that generate precise trapezoidal waveforms with typical rise and fall times of 6 ns which are relatively independent of capacitive loading conditions. These controlled output characteristics significantly reduce noise coupling to adjacent lines.

To minimize bus loading, the DS3890 and DS3898 also feature a schottky diode in series with the open collector outputs that isolates the driver output capacitance in the disabled state. With this type of configuration the output low voltage is typically "1V". The output high level is intended to be 2 volts. This is achieved by terminating the bus with a pull up resistor. Both devices can drive an equivalent DC load of 18.5Ω (or greater) in the defined configuration.

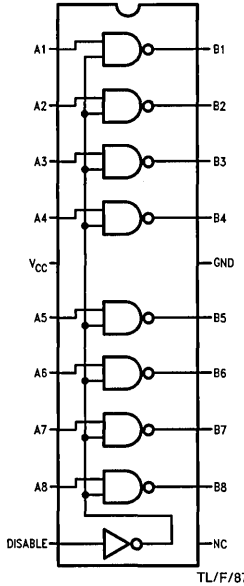
(General Description to be continued)

Features

- Meets IEEE 896 Future Bus Specification
- Driver output capacitance less than 5 pF
- 1 volt bus signal reduces power consumption
- Trapezoidal driver waveforms (t_r, t_f, typically 6 ns) reduces noise coupling to adjacent lines
- Precise receiver threshold track the bus logic high level to maximize noise immunity in both logic high ahd low states
- Open collector driver output allows wire-or connection
- Advanced low power schottky technology
- Glitch free power up/down protection
- TTL compatible driver and control inputs and receiver output

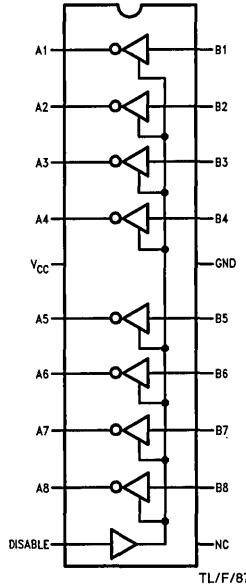
Logic and Connection Diagrams

DS3890 Octal Future Bus Drivers



TL/F/8700–1

DS3892 Octal Future Bus Receivers



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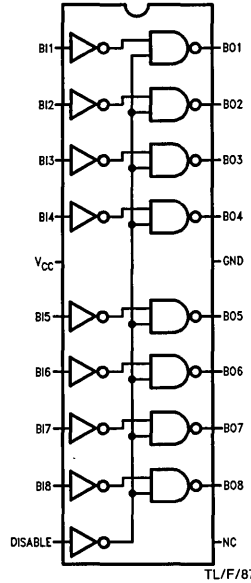
DS3898 Octal Future Bus Repeaters



TL/F/8700–3

Order Numbers DS3890J, N, DS3892J, N or DS3898J, N
See NS Package Number J20A or N20A

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	6V
Control Input Voltage	5.5V
Driver Input and Receiver Output	5.5V
Receiver Input and Driver Output	2.5V
Storage Temperature Range	−65°C to +165°C
Lead Temperature (Soldering, 4 sec.)	260°C

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage	4.75	5.25	V
Temperature (T_A)	0	70	°C

DS3890 Electrical Characteristics (Notes 2 and 3)

DRIVER AND CONTROL INPUTS

Symbol	Conditions	Min	Typ	Max	Units
V_{IH}		2.0			V
V_{IL}				0.8	V
I_{IL} An	V_{CC} = Max V_{IN} = 0.4V		−1	−1.6	mA
I_{IL} Dis	V_{CC} = Max V_{IN} = 0.4		−180	−400	μA
I_{IH}	V_{CC} = Max V_{IN} = 2.4V			40	μA
I_I	V_{CC} = Max V_{IN} = 5.25V			1	mA
V_{CL}	V_{CC} = Min I_{IN} = −12 mA		−0.9	−1.5	V
DRIVER OUTPUT					
V_{OL}	V_{CC} = Min R_L = 18.5Ω	0.75	1.0	1.2	V
I_{OH}	V_{CC} = Max V_{OUT} = 2V	−20	10	100	μA
I_O	V_{CC} = 0V V_{OUT} = 2V			100	μA
I_{IL}	V_{CC} = Max V_{OUT} = 0.75V		−100	−250	μA
I_{CC} Low	V_{CC} = Max		50	80	mA
I_{CC} High				TBD	mA

DS3892 Electrical Characteristics (Notes 2 and 3)

CONTROL INPUTS

Symbol	Conditions	Min	Typ	Max	Units
V_{IH}		2.0			V
V_{IL}				0.8	V
I_{IL}	V_{CC} = Max V_{IN} = 0.4		−180	−400	μA
I_{IH}	V_{CC} = Max V_{IN} = 2.4V			40	μA
I_I	V_{CC} = Max V_{IN} = 5.25V			1	mA
V_{CL}	V_{CC} = Min I_{IN} = −12 mA		−0.9	−1.5	V
RECEIVER					
V_{OL}	V_{CC} = Min I_{OL} = 16 mA		0.35	0.5	V
V_{OH}	V_{CC} = Min I_{OH} = −400 μA	2.4	3.2		V
I_{OS}	V_{CC} = Max V_{OUT} = 0V	−40	−70	−100	mA
V_{TH} Rec	V_{CC} = 5V	1.5	1.55	1.6	V
I_{IH} Rec	V_{CC} = Max V_{IN} = 2V		10	100	μA
I_I Rec	V_{CC} = 0V V_{IN} = 2V			100	μA
I_{IL} Rec	V_{CC} = Max V_{IN} = 0.75V			TBD	μA
I_{CC} Low	V_{CC} = Max			80	mA
I_{CC} High				TBD	mA

DS3898 Electrical Characteristics (Notes 2 and 3)

CONTROL INPUTS

Symbol	Conditions	Min	Typ	Max	Units
V_{IH}		2.0			V
V_{IL}				0.8	V
I_{IL}	V_{CC}=Max V_{IN}=0.4		−180	−400	μA
I_{IH}	V_{CC}=Max V_{IN}=2.4V			40	μA
I_I	V_{CC}=Max V_{IN}=5.25V			1	mA
V_{CL}	V_{CC}=Min I_{IN}=−12 mA		−0.9	−1.5	V
RECEIVER INPUT					
V_{TH} Rec	V_{CC}=5V	1.5	1.55	1.6	V
I_{IH} Rec	V_{CC}=Max V_{IN}=2V		10	100	μA
I_I Rec	V_{CC}=0V V_{IN}=2V			100	μA
I_{IL} Rec	V_{CC}=Max V_{IN}=0.75V			TBD	μA
DRIVER OUTPUT					
V_{OL}	V_{CC}=Min R_L=18.5Ω	0.75	1.0	1.2	V
I_{OH}	V_{CC}=Max V_{OUT}=2V	−20	10	100	μA
I_O	V_{CC}=0V V_{OUT}=2V			100	μA
I_{IL}	V_{CC}=Max V_{OUT}=0.75V		−100	−250	mA
I_{CC} Low	V_{CC}=Max		90	135	mA
I_{CC} High				TBD	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The Table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All currents into device pins are shown as positive values; all currents out of the device are shown as negative; all voltages are referenced to ground unless otherwise specified. All values shown as max or min are classified on absolute value basis and apply to the full operating temperature and V_{CC} range.

Note 3: All typical values are V_{CC}=5V, T_A= 25°C.

DS3890 Switching Characteristics *(Figure 1)*

(0°C≤T_A≤70°C, 4.75V≤V_{CC}≤5.25V unless otherwise specified)

Symbol	Conditions	Min	Typ	Max	Units
T_{dLH}	An to Bn		9	15	ns
T_{dHL}			9	15	ns
T_{dLH}	Dis to Bn		10	18	ns
T_{dHL}			12	20	ns
T_r & T_f	Bn rise and fall time	3	6	10	ns

DS3892 Switching Characteristics *(Figures 2, 3 and 4)*

Symbol	Conditions	Min	Typ	Max	Units
T_{dLH}	Bn to An		12	18	ns
T_{pHL}			10	18	ns
T_{dLZ}	Dis to An		10	18	ns
T_{dZL}			8	15	ns
T_{dHZ}			4	8	ns
T_{dZH}			7	12	ns
TNR	Receiver noise rejection	3	6		ns

DS3898 Switching Characteristics (*Figures 4* and *5*)

Symbol	Conditions	Min	Typ	Max	Units
T_{dLH}	Bi to BOn		20	30	ns
T_{dHL}			20	30	ns
T_{dLH}	Dis to BOn		10	18	ns
T_{dHL}			12	20	ns
T_r & T_f	Bn rise and fall time	3	6	10	ns
TNR	Receiver noise rejection	3	6		ns

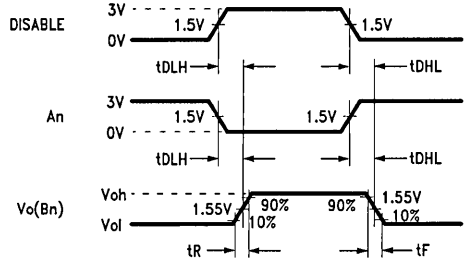
General Descriptions (Continued)

The DS8982 and DS3898 receiver inputs incorporate a low pass filter in conjunction with high speed comparator to further enhance the noise immunity. Both devices provide equal rejection to both positive and negative noise pulses (typically 6 ns) on the bus.

The DS3890 features TTL compatible inputs while both the DS3892 and DS3898 inputs are BTL compatible. The control inputs on all devices are TTL compatible.

BTL "Backplane Transceiver Logic" is a new logic signaling method developed by IEEE P896 Future Bus Standards Committee. This standard was adopted to enhance the performance of Backplane Busses. BTL compatible bus interface circuits feature low capacitance drivers to minimize bus loading, a 1V nominal signal swing for reduced power consumption and receivers with precision thresholds for maximum noise immunity. This new standard overcomes some of the fundamental limitations of TTL bus transceivers in heavily loaded backplane bus applications. Devices designed to this standard provide significant improvements in switching speed and data integrity.

AC Switching Waveforms



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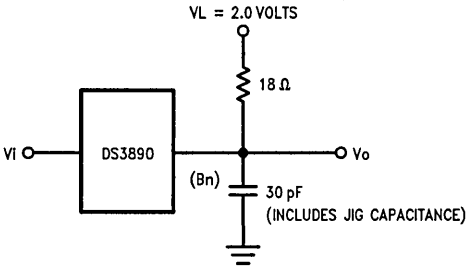


Note: $t_R = t_F < 10$ ns from 10% to 90%

TL/F/8700–5

FIGURE 1
Driver Propagation Delays

2

AC Switching Waveforms (Continued)

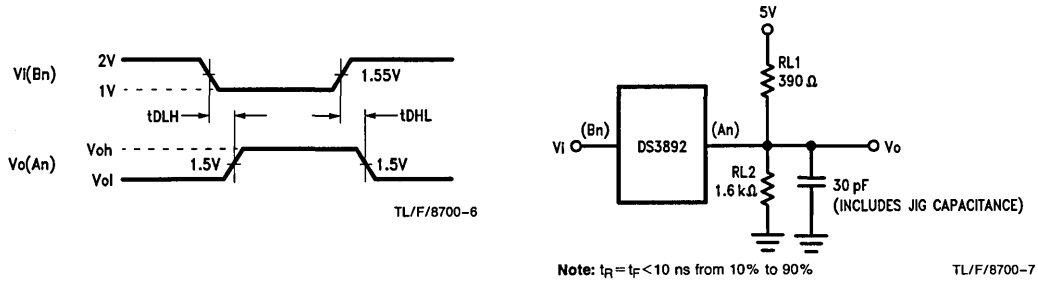
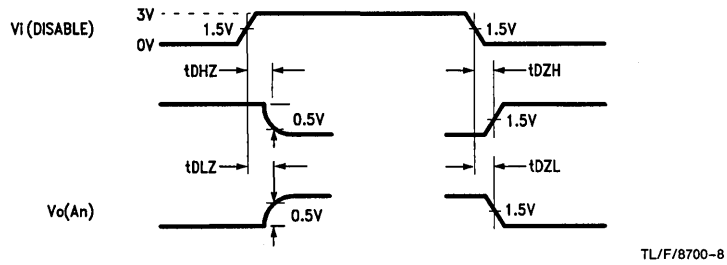


FIGURE 2. Receiver Propagation Delays



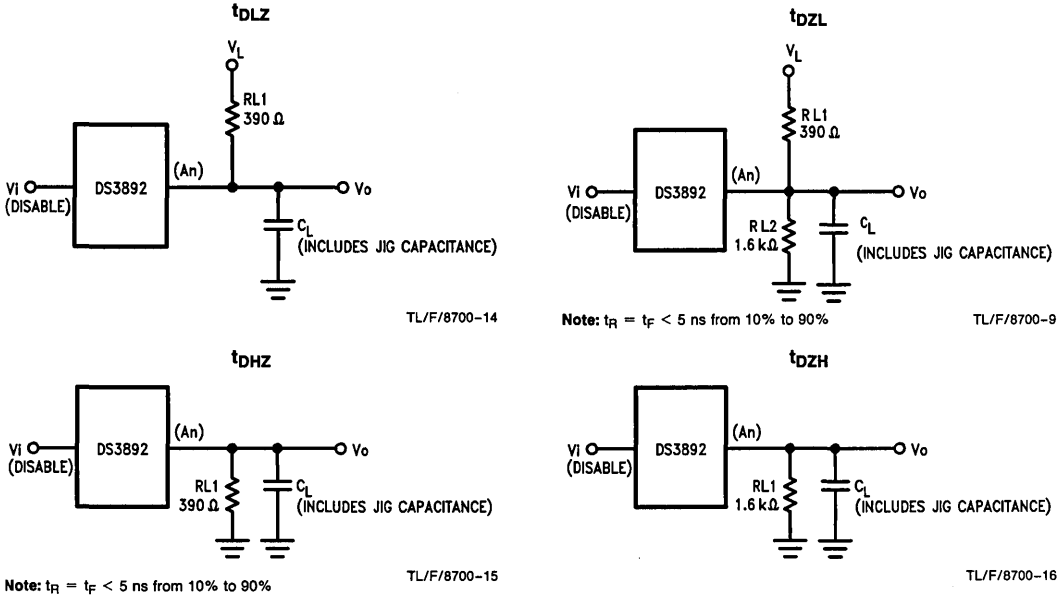
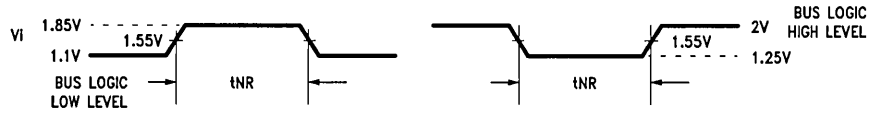
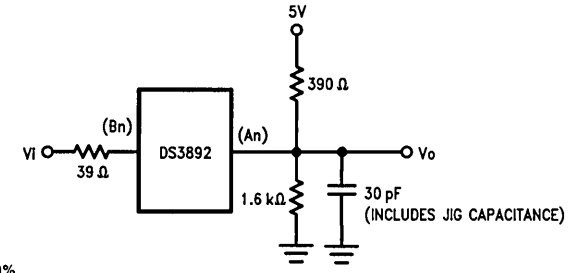


FIGURE 3. Propagation Delay from Disable Pin to An

AC Switching Waveforms (Continued)



TL/F/8700–10



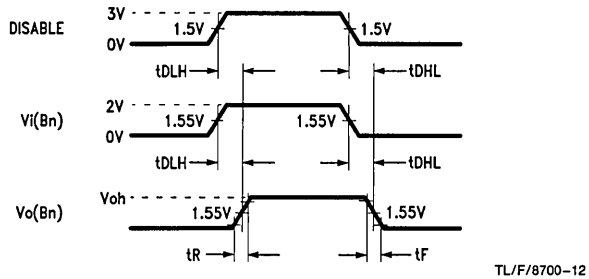
Note: $t_R = t_F < 2$ ns from 10% to 90%

TL/F/8700–11

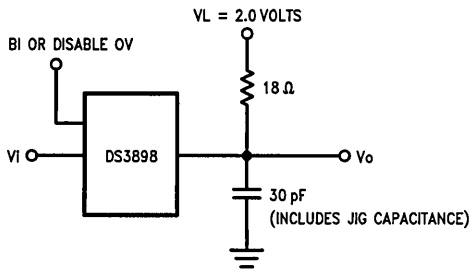
FIGURE 4

Receiver Noise Immunity:
"No Response at Output" Input Waveforms

Typical Application



TL/F/8700–12



Note: $t_R = t_F < 10$ ns from 10% to 90%

TL/F/8700–13

FIGURE 5

Repeater Propagation Delays

2

National Semiconductor Corporation

PRELIMINARY

DS3893 BTL™ TURBOTRANSCEIVER™

General Description

The TURBOTRANSCEIVER is designed for use in very high speed bus systems. The signaling characteristics of the TURBOTRANSCEIVER are referred to as "Backplane Transceiver Logic" (BTL). BTL is a new logic signaling standard that has been developed to enhance the performance of backplane buses. BTL compatible transceivers feature low output capacitance drivers to minimize bus loading, a 1V nominal signal swing for reduced power consumption and receivers with precision thresholds for maximum noise immunity. This new standard eliminates the settling time delays, that severely limit the TTL bus performance, to provide significantly higher bus transfer rates.

The TURBOTRANSCEIVER is compatible with the requirements of the IEEE 896 Futurebus standard. It is similar to the DS3896/97 BTL TRAPEZOIDAL Transceivers (low output capacitance and 1V logic swing) but the trapezoidal feature has been removed to improve the propagation delay. A stripline backplane is therefore required to reduce the crosstalk induced by the faster rise and fall times. This device can drive a 10Ω load with a typical propagation delay of 3.5 ns for the driver and the reciever.

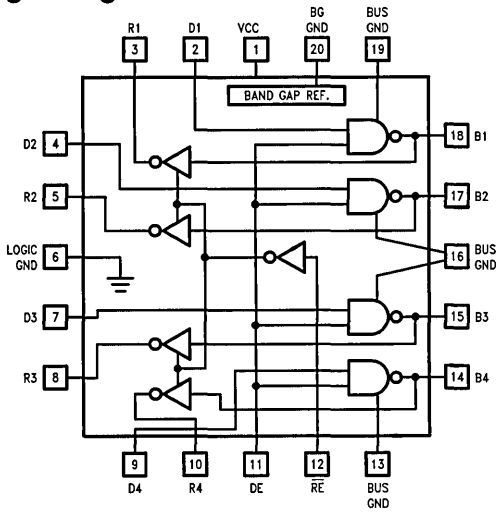
When multiple devices are used to drive a parallel bus, the driver enables can be tied together and used as a common control line to get on and off the bus. The driver enable delay is designed to be the same as the driver propagation delay in order to provide maximum speed in this configuration. The low input current on the enable pin eases the drive required for the common control line.

The bus driver is an open collector NPN with a Schottky diode in series to isolate the transistor output capacitance from the bus when the driver is in the inactive state. The active output low voltage is typically 1V. The bus is intended to be operated with termination resistors (selected to match the bus impedance) to 2V at both ends. Each of the resistors can be as low as 20Ω.

Features

- The fastest single ended transceiver (driver enable and receiver propagation delay are 3.5 ns typical)
- Backplane Transceiver Logic (BTL™) levels (1V logic swing)
- Less than 7 pF bus-port capacitance
- Drives densely loaded backplanes with equivalent load impedances down to 10Ω
- Complies with IEEE 896 Futurebus standard
- 4 transceivers in 20 pin PCC package
- Specially designed for stripline backplanes
- Separate bus ground returns for each driver to minimize ground noise
- High impedance, MOS and TTL compatible inputs
- TRI-STATE® control for receiver outputs
- Built-in bandgap reference provides accurate receiver threshold
- Glitch free power up/down protection on all outputs
- Oxide isolated bipolar technology

Connection and Logic Diagram



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Order Number DS3893V
See NS Package Number V20A

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	6.5V
Control Input Voltage	6V
Driver Input and Receiver Output	6V
Receiver Input and Driver Output	3V
Power Dissipation at 70°C	900 mW
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 4 sec.)	260°C

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage, V_{CC}	4.75	5.25	V
Bus Termination Voltage (V_T)	1.9	2.1	V
Operating Free Air Temperature	0	70	°C

Electrical Characteristics (Notes 2 and 3) T_A = 0 to +70°C, V_{CC} = 5V ±5%

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRIVER AND CONTROL INPUT: (DE, $\overline{RE}$, Dn)						
V_{IH}	Minimum Input High Voltage		2.0			V
V_{IL}	Maximum Input Low Voltage				0.8	V
I_I	Input Leakage Current	DE = $\overline{RE}$ = Dn = V_{CC}			1	mA
I_{IH}	Input High Current	DE = $\overline{RE}$ = Dn = 2.4V			40	μA
I_{IL}	D_n and $\overline{RE}$ Inputs	Dn = $\overline{RE}$ = 0V			−100	μA
I_{ILE}	DE Input	DE = 0V			−400	μA
V_{CL}	Input Diode Clamp Voltage	I_{clamp} = 12 mA			−1.5	V
DRIVER OUTPUT/RECEIVER INPUT: (Bn)						
V_{OLB}	Output Low Bus Voltage	Dn = DE = 2.4V *(Figure 2)* R_T = 10Ω, V_T = 2V			1.2	V
I_{OHB}	Output High Bus Current (Power On)	Dn = DE = 0.8V, V_{CC} = 5.25V Bn = 2V		10	100	μA
I_{OHB}	Output High Bus Current (Power Off)	Dn = DE = 0.8V, V_{CC} = 0V Bn = 2V			100	μA
V_{TH}	Receiver Input Threshold		1.475	1.55	1.625	V
C_{IN}	Bus-Port Capacitance	Bn = V_T = 2V			7	pF
RECEIVER OUTPUT: (Rn)						
V_{OH}	Voltage Output High	Bn = 1.2V, I_{oh} = −1 mA $\overline{RE}$ = 0.8V	2.5V			V
V_{OL}	Voltage Outputs Low	Bn = 2V, I_{ol} = 20 mA $\overline{RE}$ = 0.8V		0.35	0.5	V
I_{OS}	Output Short Circuit Current	Bn = 1.2V $\overline{RE}$ = 0.8V			−200	mA
I_{CC}	Supply Current			70		mA

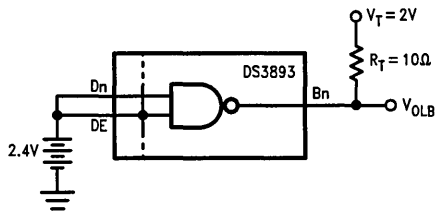
Note 1: "Absolute maximum ratings" are those beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to device ground unless otherwise specified.

Note 3: All typicals are given for V_{CC} = 5V and T_A = 25°C.

Switching Characteristics $T_A = 0$ to $+70°C$, $V_{CC} = 5V \pm 5\%$

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRIVER: (*Figures 3* and *6*)						
t_{DHL}	Prop. Delay	$V_T = 2V$ $R_T = 10\Omega$, $C_L = 30$ pF, DE = 3V	2	3.5	7	ns
t_{DLH}	Prop. Delay	$V_T = 2V$, $R_T = 10\Omega$, $C_L = 30$ pF, DE = 3V	2	3.5	7	ns
t_{DR}	Output Rise time	$V_T = 2V$, $R_T = 10\Omega$, $C_L = 30$ pF, DE = 3V	1		5	ns
t_{DF}	Output Fall Time	$V_T = 2V$, $R_T = 10\Omega$, $C_L = 30$ pF, DE = 3V	1		5	ns
t_{Dskew}	Skew Between Drivers in Same Package				1	ns
DRIVER ENABLE: (*Figures 3* and *6*)						
t_{EHL}	Enable Delay	$V_T = 2V$, $R_T = 10\Omega$, $C_L = 30$ pF, Dn = 3V	2	3.5	7	ns
t_{ELH}	Disable Delay	$V_T = 2V$, $R_T = 10\Omega$, $C_L = 30$ pF, Dn = 3V	2	3.5	7	ns
RECEIVER: (*Figures 4* and *7*)						
t_{RHL}	Prop. Delay	$C_L = 50$ pF, $\overline{RE}$ = DE = 0.3V	2	3.5	8	ns
t_{RLH}	Prop. Delay	$C_L = 50$ pF, $\overline{RE}$ = DE = 0.3V	2	3.5	8	ns
t_{Rskew}	Skew Between Receivers in Same Package				1	ns
RECEIVER ENABLE: (*Figures 5* and *8*)						
t_{RZL}	Receiver Enable to Output Low	$C_L = 5$ pF, $R_L = 500$, DE = 0.3V S2 Open Bn = 2V		10	12	ns
t_{RZH}	Receiver Enable to Output High	$C_L = 5$ pF, $R_L = 500$, DE = 0.3V S1 Open Bn = 1V		9	12	ns
t_{RLZ}	Receiver Disable From Low	$C_L = 5$ pF, $R_L = 500$, DE = 0.3V S2 Open Bn = 2V		4	6	ns
t_{RHZ}	Receiver Disable From High	$C_L = 5$ pF, $R_L = 500$, DE = 0.3V S1 Open Bn = 1V		4	6	ns



Note: n = 1, 2, 3, 4

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FIGURE 2. Driver Output Low Voltage

AC Test Circuits

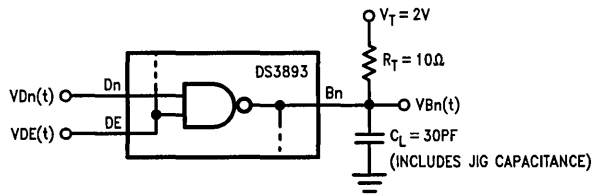

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FIGURE 3

AC Test Circuits (Continued)

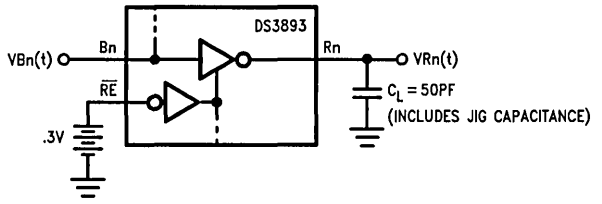

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FIGURE 4

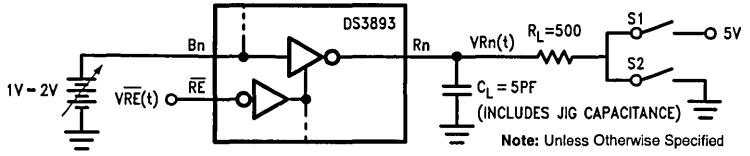

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FIGURE 5

Switching Time Waveforms

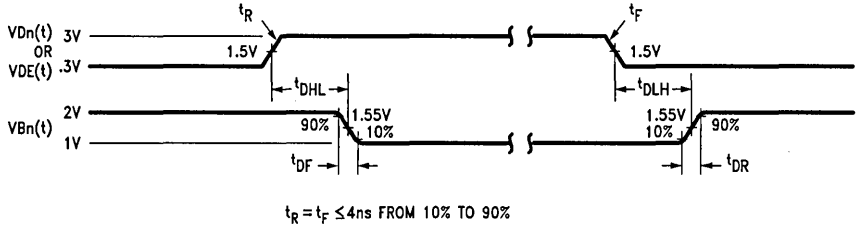

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FIGURE 6. Driver Propagation Delay

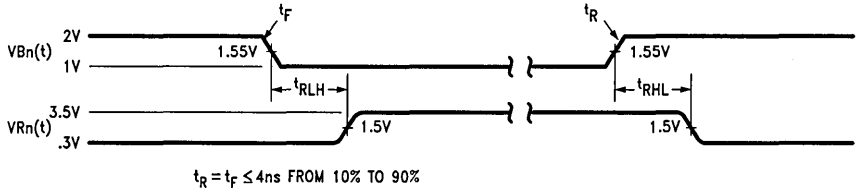

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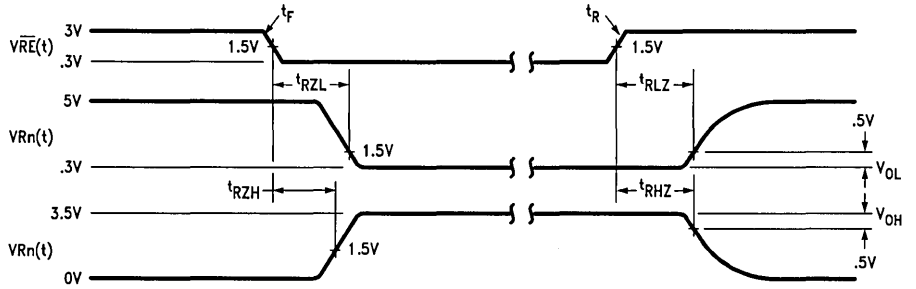
FIGURE 7. Receiver Propagation Delay



Note: $t_R = t_F \leq 4$ ns From 10% to 90%

Note: n = 1, 2, 3, 4

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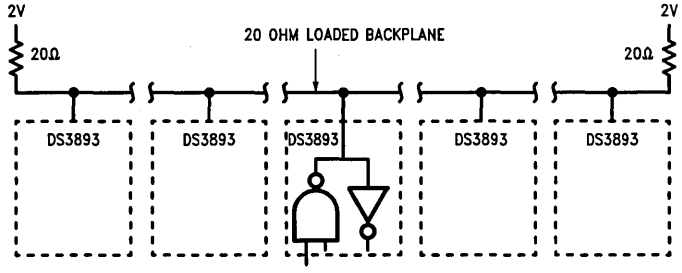
FIGURE 8. Receiver Enable and Disable Times

2

Typical Application



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Application Information

Due to the high current and very high speed capability of the TURBOTRANSCEIVER's driver output stage, circuit board layout and bus grounding are critical factors that affect the system performance.

Each of the TURBOTRANSCEIVER's bus ground pins should be connected to the nearest backplane ground pin with a separate trace. The ground pins on the connector should be distributed evenly through its length.

Although the bandgap reference receiver threshold provides sufficient DC noise margin *(Figure 1)*, ground noise and ringing on the data paths could easily exceed this margin if the series inductance of the traces and connectors are not kept to a minimum. The transceivers should be mounted as close as possible to the connector. It should be noted that even one inch of trace can add a significant amount of ringing to the bus signal.

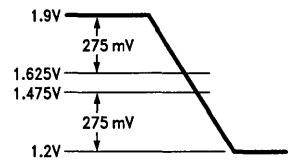

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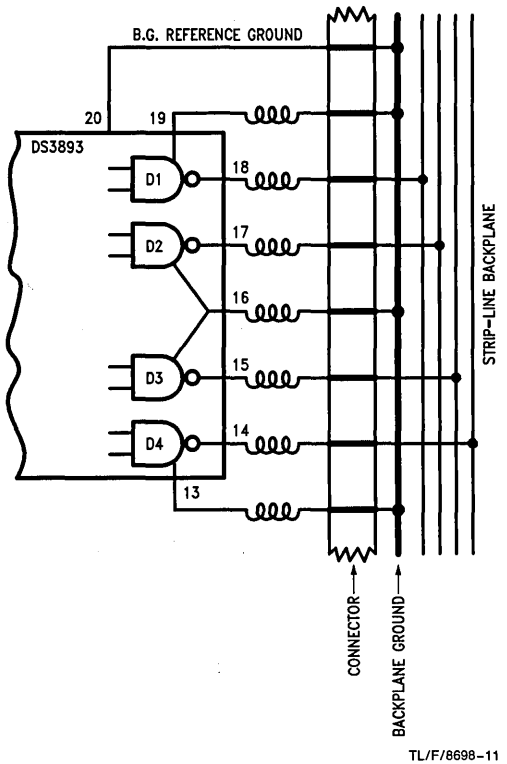
FIGURE 1. Noise Margin



TL/F/8698–11

FIGURE 2

National Semiconductor Corporation

DS3896/DS3897 Futurebus Trapezoidal™ Transceivers

General Description

These advanced IEEE-896 Futurebus compatible transceivers are specifically designed to overcome problems associated with driving a densely populated backplane, and thus provide significant improvement in both speed and data integrity. Their low output capacitance, low output signal swing and noise immunity features make them ideal for driving low impedance buses with minimum power consumption.

The DS3896 is an octal high speed schottky bus transceiver with common control signals, whereas the DS3897 is a quad device with independent driver input and receiver output pins. The DS3897 has a separate driver disable for each driver and is, therefore, suitable for arbitration lines. On the other hand, the DS3896 provides high package density for data/address lines.

The open collector drivers generate precise trapezoidal waveforms, which are relatively independent of capacitive loading conditions on the outputs. This significantly reduces noise coupling to adjacent lines. In addition, the receivers use a low pass filter in conjunction with a high speed comparator, to further enhance the noise immunity and provide equal rejection to both negative and positive going noise pulses on the bus.

To minimize bus loading, these devices also feature a schottky diode in series with the open collector output that isolates the driver output capacitance in the disabled state. The output low voltage is typically "1V" and the output high level is intended to be 2V. This is achieved by terminating the bus with a pull up resistor to 2V at both ends. The device can drive an equivalent DC load of 18.5Ω (or greater) in the above configuration.

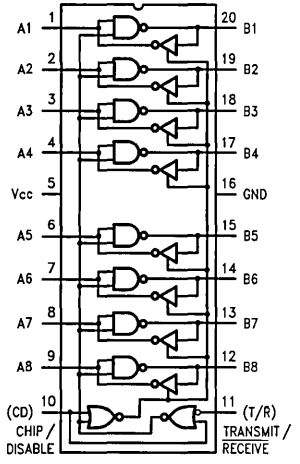
These signalling requirements, including a 1 volt signal swing, low output capacitance and precise receiver thresholds are referred to as Bus Transceiver Logic (BTL™).

Features

- 8 bit DS3896 transceiver provides high package density
- 4 bit DS3897 transceiver provides separate driver input and receiver output pins
- Meets IEEE 896 Futurebus specification
- BTL compatible
- Less than 5 pF output capacitance for minimal bus loading
- 1 Volt bus signal swing reduces power consumption
- Trapezoidal driver waveforms (t_r, $t_f \cong 6$ ns typical) reduce noise coupling to adjacent lines
- Temperature insensitive receiver thresholds track the bus logic high level to maximize noise immunity in both high and low states
- Guaranteed A.C. specifications on noise immunity and propagation delay over the specified temperature and supply voltage range
- Open collector driver output allows wire-or connection
- Advanced low power schottky technology
- Glitch free power up/down protection on driver and receiver outputs
- TTL compatible driver and control inputs and receiver outputs

Logic and Connection Diagrams

DS3896N, J



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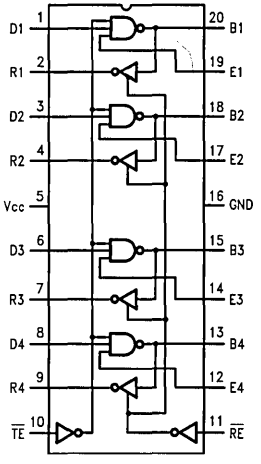
DS3897N, J



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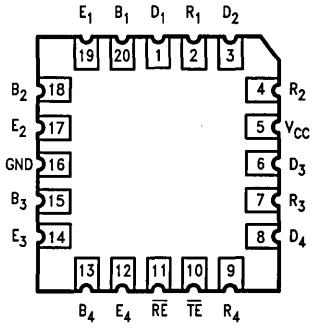
DS3897V



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Order Number DS3896J, N, DS3897J, N or DS3897V
See NS Package Number J20A, N20A or V20A

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	6V
Control Input Voltage	5.5V
Driver Input and Receiver Output	5.5V
Receiver Input and Driver Output	2.5V
Power Dissipation at 70°C N Package	1480 mW
J Package	1250 mW
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 4 sec.)	260°C

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage, V_{CC}	4.75	5.25	V
Bus Termination Voltage	1.90	2.10	V
Operating Free Air Temperature	0	70	°C

Electrical Characteristics: (Note 2 and 3) ($0°C \le T_A \le 70°C$, $4.75V \le V_{CC} \le 5.25V$ unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Driver and Control Inputs: (An, Dn, En, CD, T/$\overline{R}$, $\overline{RE}$, $\overline{TE}$)						
V_{IH}	Logical "1" Input Voltage		2.0			V
V_{IL}	Logical "0" Input Voltage				0.8	V
I_I	Logical "1" Input Current	An = Dn = En = V_{CC}			1	mA
I_{IH}	Logical "1" Input Current	An = Dn = En = 2.4V			40	μA
I_{IL}	Logical "0" Input Current	An = Dn = En = 0.4V		−1	−1.6	mA
I_{ILC}	Logical "0" Input Current	CD = T/$\overline{R}$ = $\overline{RE}$ = $\overline{TE}$ = 0.4V		−180	−400	μA
V_{CL}	Input Diode Clamp Voltage	Iclamp = −12 mA		−0.9	−1.5	V
Driver Output/Receiver Input: (Bn)						
V_{OLB}	Low Level Bus Voltage	An = Dn = En = T/$\overline{R}$ = 2V, VL = 2V RL = 18.5Ω, CD = $\overline{TE}$ = 0.8V (*Figure 1*)	0.75	1.0	1.2	V
I_{IHB}	Maximum Bus Current (Power On)	An = Dn = En = 0.8V, V_{CC} = 5.25V Bn = 2V		10	100	μA
I_{ILB}	Maximum Bus Current (Power Off)	An = Dn = En = 0.8V, V_{CC} = 0V Bn = 2V			100	μA
V_{TH}	Receiver Input Threshold	V_{CC} = 5V	1.5	1.55	1.60	V
Receiver Output: (An, Rn)						
V_{OH}	Logical "1" Output Voltage	Bn = 1.2V, I_{OH} = −400 μA CD = T/$\overline{R}$ = $\overline{RE}$ = 0.8V	2.4	3.2		V
V_{OL}	Logical "0" Output Voltage	Bn = 2V, I_{OL} = 16 mA CD = T/$\overline{R}$ = $\overline{RE}$ = 0.8V		0.35	0.5	V
I_{OS}	Output Short Circuit Current	Bn = 1.2V CD = T/$\overline{R}$ = $\overline{RE}$ = 0.8V	−40	−70	−100	mA
I_{CC}	Supply Current (DS3896)	V_{CC} = 5.25V		90	135	mA
I_{CC}	Supply Current (DS3897)	V_{CC} = 5.25V		50	80	mA

Note 1. "Absolute maximum ratings" are those beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristic" provide conditions for actual device operation.

Note 2. All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to device ground unless otherwise specified.

Note 3. All typicals are given for V_{CC} = 5V and T_a = 25°C.

DS3896 Switching Characteristics

(0°C ≤ T_A ≤ 70°C, 4.75V ≤ V_{CC} ≤ 5.25V unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Driver:						
t_{DLH}	An to Bn	CD = 0.8V, T/$\overline{R}$ = 2.0V, VL = 2V		9	15	ns
t_{DHL}		*(Figure 2)*		9	15	ns
t_{DLHC}	CD to Bn	An = T/$\overline{R}$ = 2.0V, VL = 2V,		10	18	ns
t_{DHLC}		*(Figure 2)*		12	20	ns
t_{DLHT}	T/$\overline{R}$ to Bn	VCI = An, VC = 5V, *(Figure 5)*		15	25	ns
t_{DHLT}		CD = 0.8V, RC = 390Ω, CL = 30 pF RL1 = 18Ω, RL2 = NC, VL = 2V		22	35	ns
t_R	Driver Output Rise Time	CD = 0.8V, T/$\overline{R}$ = 2V, VL = 2V	3	6	10	ns
t_F	Driver Output Fall Time	*(Figure 2)*	3	6	10	ns
Receiver:						
t_{RLH}	Bn to An	CD = 0.8V, T/$\overline{R}$ = 0.8V		12	18	ns
t_{RHL}		*(Figure 3)*		10	18	ns
t_{RLZC}	CD to An	Bn = 2.0V, T/$\overline{R}$ = 0.8V, CL = 5 pF RL1 = 390Ω, RL2 = NC, VL = 5V *(Figure 4)*		10	18	ns
t_{RZLC}		Bn = 2.0V, T/$\overline{R}$ = 0.8V, CL = 30 pF RL1 = 390Ω, RL2 = 1.6k, VL = 5V *(Figure 4)*		8	15	ns
t_{RHZC}		Bn = 0.8V, T/$\overline{R}$ = 0.8V, VL = 0V, RL1 = 390Ω, RL2 = NC, CL = 5 pF *(Figure 4)*		4	8	ns
t_{RZHC}		Bn = 0.8V, T/$\overline{R}$ = 0.8V, VL = 0V, RL1 = NC, RL2 = 1.6k, CL = 30 pF *(Figure 4)*		7	12	ns
t_{RLZT}	T/$\overline{R}$ to An	VCI = Bn, VC = 2V, RC = 18Ω, CD = 0.8V, VL = 5V, RL1 = 390Ω, RL2 = NC, CL = 5 pF *(Figure 5)*		14	20	ns
t_{RZLT}		VCI = Bn, VC = 2V, RC = 18Ω, CD = 0.8V, VL = 5V, RL1 = 390Ω, RL2 = 1.6k, CL = 30 pF *(Figure 5)*		24	40	ns
t_{RHZT}		VCI = Bn, VC = 0V, RC = 18Ω, CD = 0.8V, VL = 0V, RL1 = 390Ω, RL2 = NC, CL = 5 pF *(Figure 5)*		4	8	ns
t_{RZHT}		VCI = Bn, VC = 0V, RC = 18Ω, CD = 0.8V, VL = 0V, RL1 = NC RL2 = 1.6k, CL = 30 pF *(Figure 5)*		8	15	ns
t_{NR}	Receiver Noise Rejection Pulse Width	*(Figure 6)*	3	6		ns

Note: NC means open

DS3897 Switching Characteristics

(0°C ≤ T_A ≤ 70°C, 4.75V ≤ V_{CC} ≤ 5.25V unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Driver:						
t_{DLH}	Dn, En to Bn	$\overline{TE}$ = 0.8V, $\overline{RE}$ = 2.0V, VL = 2V		9	15	ns
t_{DHL}		*(Figure 2)*		9	15	ns
t_{DLHT}	$\overline{TE}$ to Bn	An = $\overline{RE}$ = 2.0V, VL = 2V, *(Figure 2)*		10	18	ns
t_{DHLT}		RL1 = 18Ω, RL2 = NC, VL = 2V *(Figure 5)*		12	20	ns
t_R	Driver Output Rise Time	CD = 0.8V, T/$\overline{R}$ = 2V, VL = 2V	3	6	10	ns
tF	Driver Output Fall Time	*(Figure 2)*	3	6	10	ns

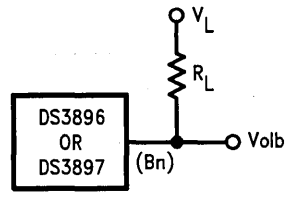
2

DS3897 Switching Characteristics (Continued)

(0°C ≤ T_A ≤ 70°C, 4.75V ≤ V_{CC} ≤ 5.25V unless otherwise specified)

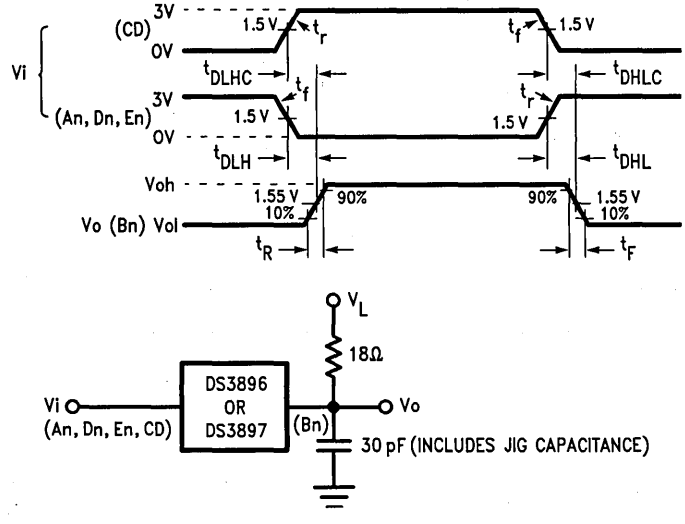
Symbol	Parameter	Conditions	Min	Typ	Max	Units
Receiver:						
t_{RLH}	Bn to Rn	$\overline{TE}$ = 2.0V, $\overline{RE}$ = 0.8V (*Figure 3*)		10	18	ns
t_{RHL}				12	18	ns
t_{RLZR}	$\overline{RE}$ to Rn	Bn = $\overline{TE}$ = 2V, VL = 5V, CL = 5 pF RL1 = 390Ω, RL2 = NC (*Figure 4*)		10	18	ns
t_{RZLR}		Bn = $\overline{TE}$ = 2V, VL = 5V, CL = 30 pF RL1 = 390Ω, RL2 = 1.6k (*Figure 4*)		8	15	ns
t_{RHZR}		Bn = 0.8V, $\overline{TE}$ = 2V, VL = 0V, RL1 = 390Ω, RL2 = NC, CL = 5 pF(*Figure 4*)		4	8	ns
t_{RZHR}		Bn = 0.8V, $\overline{TE}$ = 2V, VL = 0V, RL1 = NC, RL2 = 1.6k, CL = 30 pF(*Figure 4*)		7	12	ns
t_{NR}	Receiver Noise Rejection Pulse Width	(*Figure 6*)	3	6		ns
Driver plus Receiver:						
t_{DRLH}	Dn to Rn	$\overline{TE}$ = $\overline{RE}$ = 0.8V (*Figure 7*)		20	30	ns
t_{DRHL}				20	30	ns

Note: NC means open



TL/F/8510–3

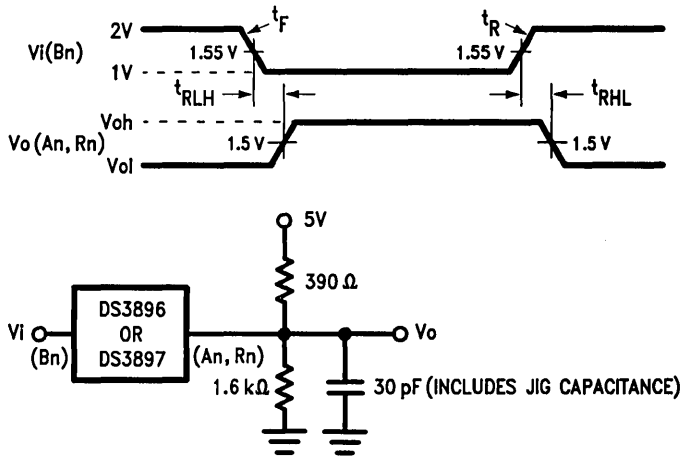
FIGURE 1. Driver Output Low Voltage Test



TL/F/8510–4

Note: $t_r = t_f \leq 5$ ns from 10% to 90%

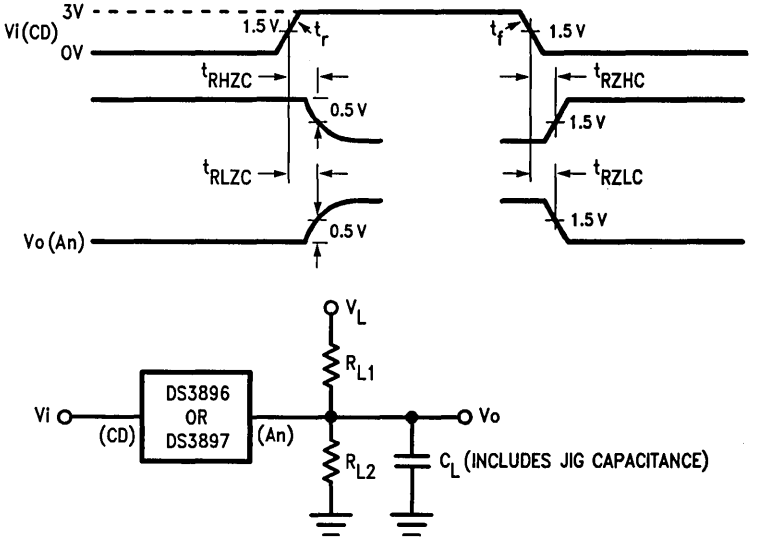
FIGURE 2. Driver Propagation Delays



TL/F/8510–5

Note: $t_R = t_F \leq 10$ ns from 10% to 90%

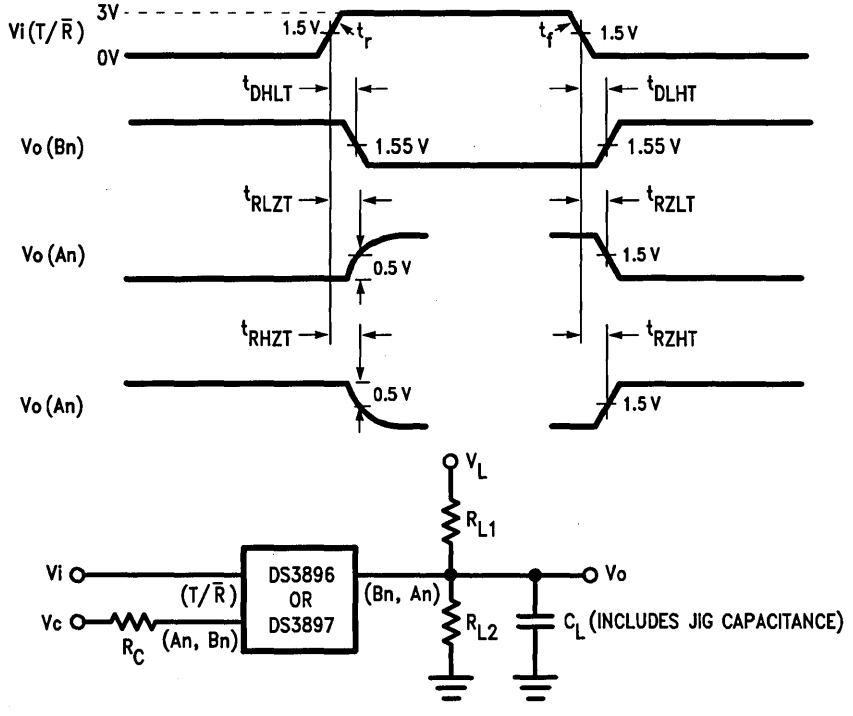
FIGURE 3. Receiver Propagation Delays



TL/F/8510–6

Note: $t_r = t_f \leq 5$ ns from 10% to 90%

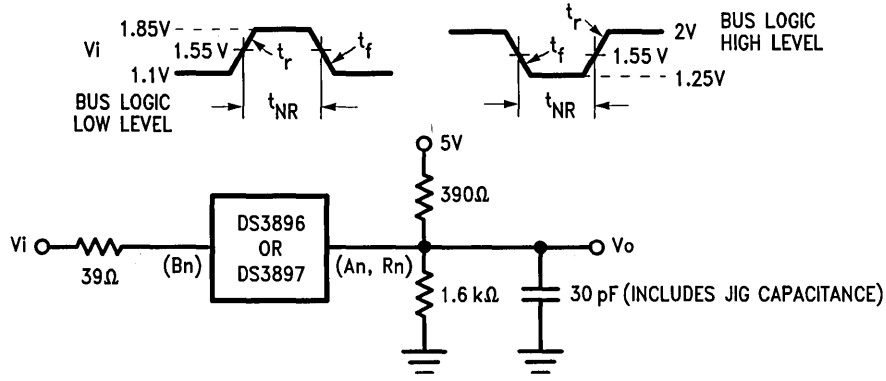
FIGURE 4. Propagation Delay from CD pin to An



TL/F/8510–7

Note: $t_r = t_f \leq 5$ ns from 10% to 90%

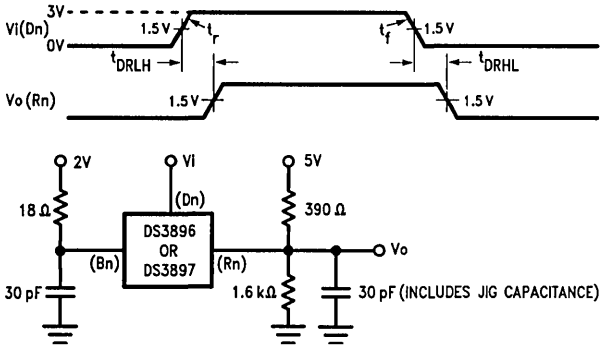
FIGURE 5. Propagation Delay from T/$\overline{R}$ pin to An or Bn



TL/F/8510–8

Note: $t_r = t_f = 2$ ns from 10% to 90%

FIGURE 6. Receiver Noise Immunity: "No Response at Output" Input Waveforms

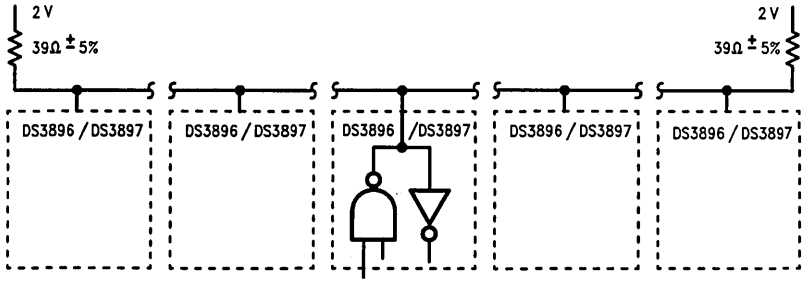


TL/F/8510–9

Note: $t_r = t_f \leq 5\ \mu s$ from 10% to 90%

FIGURE 7. Driver Plus Receiver Delays

Typical Application



TL/F/8510–10

The Proposed IEEE 896 Futurebus—A Solution to the Bus Driving Problem

National Semiconductor Corp.
Application Note 458
R. V. Balakrishnan

The IEEE 896 Futurebus is a proposed general-purpose bus standard for high-performance microcomputer systems. With a strong emphasis on speed and reliability, P896 offers a number of innovative features that are not found in other backplane buses.

A major contribution to its performance comes from its electrical specifications. The Futurebus solves, for the first time, the fundamental problems associated with driving a densely populated backplane—as a result, it provides significant improvements in both speed and data integrity. Two years of effort by the P896 committee have culminated in a deeper understanding of the physics of the backplane bus, leading to an ingenious solution to the bus problem.

Speed is probably the most important feature of any bus standard. This is especially true for the Futurebus, since its totally asynchronous protocol permits continuous speed enhancements through advances in technology. In fact, the maximum data transfer rate between any two plug-in cards is determined simply by the sum of the response times of the two cards and the bus delay. Ultimately, as logic devices get faster, bus delay will be the dominating factor limiting bus speed.

There are two components to the bus delay in a typical system, namely, the settling time and the propagation delay. The settling time is the time needed for reflections and crosstalk to subside before data are sampled; it is usually several times longer than the backplane propagation delay. As will be shown later, the settling time is the price the user pays for not driving the bus properly.

By using a special transceiver, the Futurebus not only eliminates the settling time delay but also reduces the propagation delay of the loaded backplane to provide maximum possible bus throughput.

THE PHYSICS OF THE BACKPLANE BUS

For high-speed signals the bus acts like a transmission line with an associated characteristic impedance and propagation delay whose unloaded values, Z_o and t_{po}, are given by

$$Z_o = \sqrt{L/C}$$

$$t_{po} = \sqrt{L/C}$$

ℓ = length of the bus, L = distributed inductance per unit length, and C = distributed capacitance per unit length.(1)

These values can be calculated for a typical microstrip backplane *(Figure 1)* by means of the following equations:

$$Z_o = (87/\sqrt{\epsilon_r + 1.41}) \cdot \ln [5.98h/(0.8w + t)]\,\Omega$$

$$t_{po} = 1.017\sqrt{0.475\,\epsilon_r + 0.67}\ \text{ns/ft}$$

where ϵ_r = relative dielectric constant of the board material (typically $\epsilon_r = 4.7$ for fiberglass and w,h,t = the dimensions indicated in *Figure 1*. For a typical P896 backplane, t = 1.4 mils, w = 25 mils, h = 1/16 inch, and $\epsilon_r = 4.7$. By substituting these values we get $Z_o = 100\Omega$ and $t_{po} = 1.7$ ns/ft.

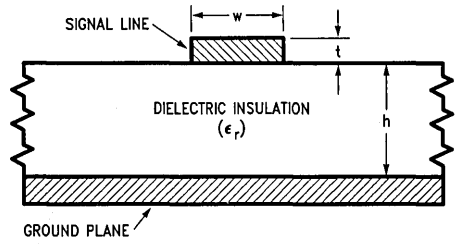
These values correspond to an *unloaded* backplane. When the backplane is uniformly loaded with the capacitance of plug-in cards and connectors at frequent intervals, the loaded values of the impedance, Z_L, and the propagation delay, t_{pL}, are given by

$$Z_L = Z_o/\sqrt{1 + C_L/C)}$$

$$t_{pL} = t_{po}/\sqrt{1 + C_L/C)}$$

where C_L = the distributed load capacitance per unit length.(1)

The distributed capacitance, C of the unloaded backplane can be measured in the lab. For our microstrip, it is 20 pF/ft. This does not include, however, the capacitance of the connectors mounted on the backplane and the associated plated-through holes, which can amount to 5 pF per card slot.



TL/F/8842–1

FIGURE 1. Cross Section of a Microstrip Bus Line

The loading capacitance of the plug-in card, however, is dominated by the loading capacitance of the transceiver, which can be 12–20 pF for TTL devices. Allowing another 3–5 pF for printed-circuit traces and the connector, the total loading per card slot can add up to 30 pF. For a system such as P896, which has 15 slots per foot, C_L = 450 pF/ft. Therefore,

$$Z_L = 100/\sqrt{1 + (450/20)} = 20\Omega$$

$$t_{pL} = 1.7\sqrt{1 + (450/20)} = 8.25\ \text{ns/ft}$$

As can be seen above, the capacitive loading drastically alters both the impedance and the propagation delay of the bus. This reduces the bus throughput in two ways. One obvious impact is the increased propagation delay. But the not so obvious and even more serious problem is the reduced bus impedance, which is much harder to drive.

For example, to drive the loaded bus properly with a TTL driver which has a 3V nominal swing, the required drive current, I_D, must be

$$I_D = 3V/(Z_L/2)$$

The impedance seen by the driver is half of Z_L, since from a given board two transmission lines are being driven, one towards each terminator *(Figure 2)*. Therefore,

$$I_D = 3/(20/2) = 300\ \text{mA}$$

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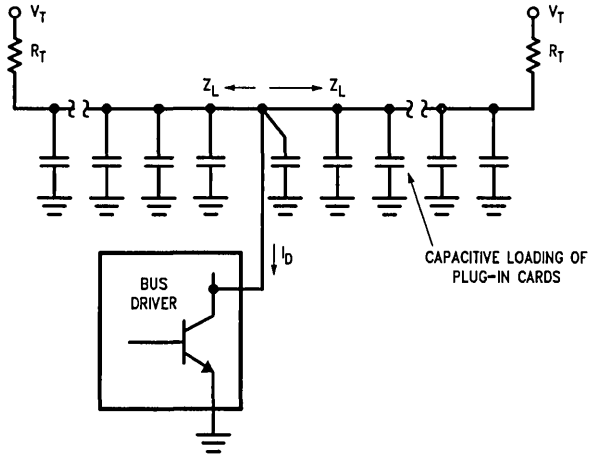

TL/F/8842–2

FIGURE 2. The Loaded Bus—Each Driver Sees Two Loaded Line Impedances in Parallel ($Z_L \| Z_L = Z_{L/2}$).

This is much higher than the standard TTL's drive capability of 50 to 100 mA. *Figure 3* shows the effect of using a 50 mA driver, in this situation, on the bus waveform. The voltage swing on the bus has its first transition at 0.5V, the product of the drive current and $Z_L/2$. This value falls well below the upper threshold limit of the TTL receiver. Therefore, *several round-trip delays to the nearest termination are required for the waveform to cross the receiver threshold region.* In our example, one round-trip delay is $2t_{pL}$ = 16.5 ns/ft. Therefore the settling times can exceed 100 ns even for relatively short buses. This long settling time drastically affects bus throughput at high speeds. Even worse, the voltage steps in the threshold region can cause multiple triggering in the cases of the clock and strobe signals.

One way to solve these problems is to use 100 mA drivers with precision receivers that have a narrow threshold region such that the first transition crosses well over the threshold. This technique is widely used for clock lines to avoid multiple triggering. Its use on data/address lines is limited because of the significantly higher power requirement arising from the large number of lines involved (32 address/data lines).

Even if power is not a limitation, switching to higher current drivers provides only a marginal improvement. The reason for this is quite simple. A higher current driver unfortunately has a higher output capacitance, which reduces the bus impedance further. This in turn requires an even higher current drive for proper operation.

The Futurebus Transceiver

A more elegant solution—one that is now a part of the P896 proposal—directly attacks the root of the problem, namely, the large output capacitance of the transceiver. By simply adding a Schottky diode in series with an open-collector driver output, the capacitance of the drive transistor is isolated by the small reverse-biased capacitance of the diode in the non-transmitting state *(Figure 4)*. The Schottky diode capacitance is typically less than 2 pF and is relatively independent of the drive current. Allowing for a receiver input capacitance of another 2 pF, the total loading of the Futurebus transceiver can be kept under 5 pF. The P896 draft specifies a maximum plug-in card capacitance of 10 pF to accommodate the 5 pF trace and connector capacitances.

In addition to reducing the loading on the bus, the Futurebus transceiver features several other enhancements over a conventional TTL transceiver that drastically reduce power consumption and improve system reliability.

A major portion of the power savings comes from a reduced voltage swing—1V—on the bus. Contrary to popular belief, the lower swing does not reduce crosstalk immunity (provided the receiver threshold is tightly controlled).[2] The induced crosstalk from other lines on the bus scales down with the amplitude of the signal transistion causing it. Consequently, if a line receiver has a precision threshold, the noise margin, expressed as a percentage of signal amplitude, remains the same, as does the crosstalk immunity. However, the absolute noise margin, with reference to a noise source external to the bus, does shrink linearly with amplitude. Fortunately, the low impedance and the relatively short length of the bus make this externally generated noise component insignificant in high-speed backplanes. Nevertheless, it is recommended that the backplane be shielded from strong noise sources external to the bus.

Noise Immunity and EMI

The Futurebus transceiver has a precision receiver threshold centered between the low and high bus levels of 1 and 2V, respectively *(Figure 5)*. Confined to a narrow region of ±3 percent ±50 mV), the threshold voltage tracks the bus high level to provide a maximum-percentage noise margin with respect to the low and high signal levels of the bus. In addition, to reduce crosstalk, which is proportional to di/dt, the driver features a trapezoidal output waveform with a 6 ns transition time. Moreover, the receiver incorporates a noise filter which selectively rejects crosstalk noise pulses of up to 8 ns in pulse width. These techniques, borrowed from the DS3662 trapezoidal bus transceiver from National Semiconductor, virtually eliminate crosstalk, thereby increasing system reliability by several orders of magnitude.

Detailed analyses of crosstalk problems in buses, and discussions of how the trapezoidal tranceiver overcomes the problems, can be found in three articles by Balakrishnan.(2-4)

DRIVE CURRENT

The backplane impedance in the P896 draft is specified as 50Ω minimum and 60Ω maximum with the connectors mounted. In our microstrip example, due to the connector and the plated-through holes, a 50Ω minimum impedance translates into a maximum allowable capacitance of 4 pF per slot. This can be easily attained with some care in printed-circuit board design. A fully loaded Futurebus, therefore, has an impedance whose worst-case value is given by

$$Z_{min} = 50/\sqrt{1 + \frac{15 \bullet 10}{20 + 4 \bullet 15}}\ \Omega$$

$$= 30\Omega$$

The drive current required for a 1V swing is

$$I_D = 1/(30/2)$$

However, with a precision receiver threshold it is possible for the driver to swing past the threshold with a comfortable margin even if the first step climbs to only 75 percent of the final amplitude under worst-case loading (see again *Figure 5*). Therefore, the drive current can be reduced by 25 percent to save power, without affecting performance:

$$I_D = \frac{1}{30/2} 0.75 = 50\ mA$$

At this current level, the power dissipated in the driver is low enough to allow eight to ten transceivers to be built into a single, narrow, dual-in-line plastic package.

National Semiconductor has two Futurebus transceivers, the DS3896 and the DS3897, that are now available in sample quantities. The DS3896 is an octal device with common control signals, whereas the DS3897 is a quad device with independent driver input and receiver output pins. The DS3897 has a separate driver disable for each driver and is, therefore, suitable for arbitration lines. On the other hand, the DS3896 provides high package density for data/address lines.

Fabricated in an oxide-isolated bipolar process, these devices combine very high speed with large drive capability. The propagation delays are 8 ns typical for the driver and 10 ns typical for the receiver.

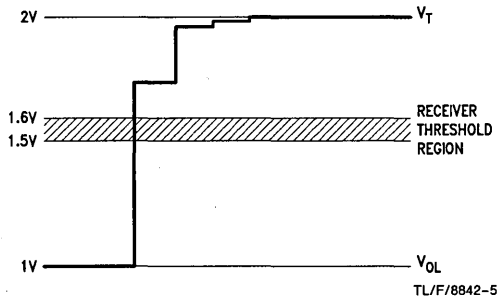

FIGURE 5. P896 Signaling Levels and the Worst-Case Bus Waveform

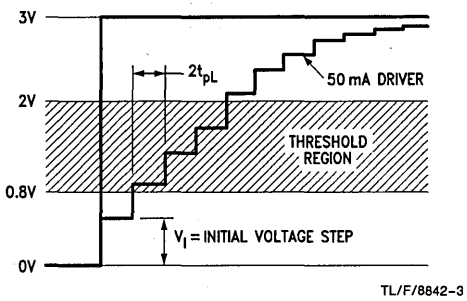

FIGURE 3. TTL Bus Waveforms—50 mA Driver vs 300 mA Driver

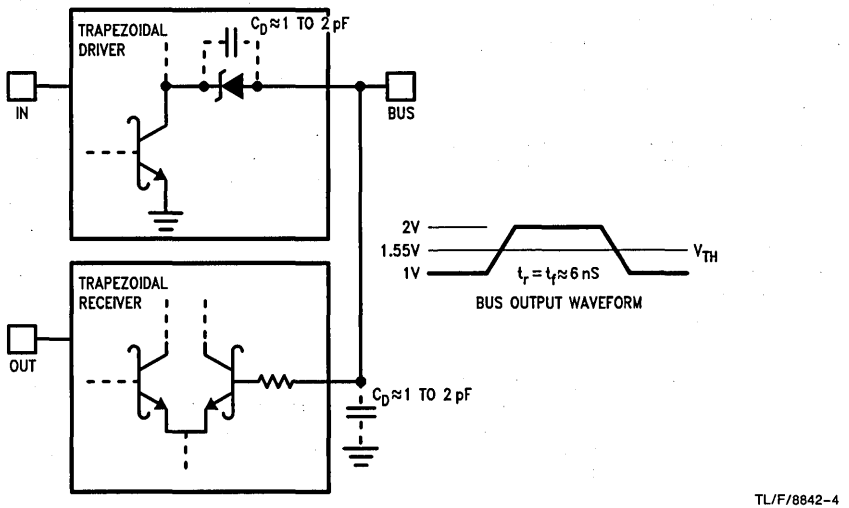

FIGURE 4. The Futurebus Trapezoidal Transceiver

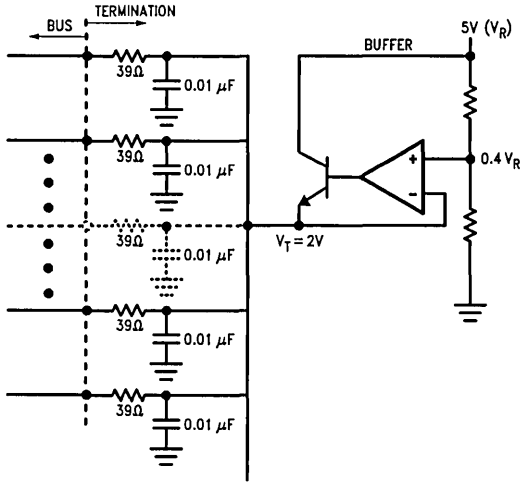

FIGURE 6. The Futurebus Termination Circuit

OTHER HIGHLIGHTS

Bus Propagation Delay

There is an additional benefit resulting from reducing the capacitive loading on the bus. This benefit arises from the reduced propagation delay, which further improves the bus speed.

Recalculating the loaded propagation delay for the Futurebus transceiver yields

$$t_{PL} = t_{po}\sqrt{1 + (C_L/C)}$$
$$= 1.7\sqrt{1 + \frac{(10 + 4)15}{20}}$$
$$= 5.765 \text{ ns/ft}$$

This is a 30-percent improvement over the TTL example. It should be noted that this is the worst-case delay per foot and that the asynchronous nature of the Futurebus protocol will take full advantage of lower propagation delays in a typical system, either due to lower loading levels or due to the closer spacing of two plug-in boards that are in communication.

Termination

The drive current and the signal swing determine the termination resistors. If the drive current is derived properly, the termination will match the bus impedance under the given loading. For P896, the value of each of the two termination resistors, R_T, is

$$R_T = \left(\frac{1V}{50 \text{ mA}}\right) 2 = 40\Omega$$

This value is greater than the loaded impedance of the Futurebus, because the drive current is only 75 percent of that required for a full swing on the first transition. However, in a practical bus the impedance varies with various load conditions, and therefore the above termination value is a good compromise between the worst-case values of the bus impedances of 30 and 50Ω.

The P896 draft requires that the bus be terminated at both ends, with a single resistor of 39Ω connected to an active voltage source of 2V *(Figure 6)*. This arrangement has a significantly lower power dissipation than a "Thévenin-equivalent" two-resistor termination connected to ground and the 5V rail. The 2V source is derived from the 5V supply using a potential divider followed by a buffer; the source can be shared among all the bus lines as long as it is properly bypassed for alternating current close to each resistor. The termination voltage is deliberately made to follow the 5V supply variation in order to keep the receiver threshold at the center of the bus swing with supply variations.

Wire-OR Glitch

One of the advantages of an open-collector bus is a wire-OR capability. This feature is fully exploited in the P896 bus, particularly in its sophisticated arbitration protocol and broadcast mechanism. Unfortunately, due to the fundamental nature of transmission lines, wire-ORing on the bus can cause erroenous glitches having pulse widths of up to the round-trip delay of the bus. The analysis of the wire-OR glitch is covered well by Theus and Gustavson.[5]

To overcome the wire-OR glitch, the broadcast acknowledge lines (AI* and DI*) and the three arbitration control lines are required to have integrators at the output of the receiver capable of rejecting pulses having widths of up to the maximum round-trip delay of the bus.

And More

Geographic addressing and live insertion and withdrawal capability are some of the other highlights of the Futurebus.

The reader is encouraged to read the draft proposal,[6] and the article by Theus and Borrill in this issue, for more details.

The electrical specification of P896 is based on a thorough knowledge of backplane operation. A combination of theoretical analysis and bench measurements has been used to create an electrically clean bus environment. Significant improvements have been made in favor of higher performance—at the expense of only a slight increase in today's cost and complexity—to assure a long design lifetime for the standard. The result is a proposed standard that has the performance, in terms of both speed and reliability, to justify the name, "Futurebus".

ACKNOWLEDGEMENT

I would like to thank Paul Borrill for his help and encouragement in finding this solution to the bus driving problem.

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3. R. V. Balakrishnan, "Cut Bus Reflections, Crosstalk with a Trapezoidal Transceiver", *EDN*, Aug. 4, 1983, pp. 151–156.
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5. John Theus and David B. Gustavson, "Wire-OR Logic on Transmission Lines", *IEEE Micro*, Vol. 3, No. 3, June 1983, pp. 51–55.
6. "Project P896.1—Futurebus Proposed Standard Specification, Draft 6.2", Nov. 1983. (Available from the IEEE Computer Society, PO Box 80452, Worldway Postal Center, Los Angeles, CA 90080. The price to members of the Computer Society is $10 plus $2 for handling and shipping within the United States. The nonmember price is $20 plus $3 handling and shipping within the United States. Shipping to Europe and the rest of the world is an additional $10. You will receive faster service with prepaid orders in US dollars.)

National Semiconductor Corporation

DS75160A/DS75161A/DS75162A IEEE-488 GPIB Transceivers

General Description

This family of high-speed-Schottky 8-channel bi-directional transceivers is designed to interface TTL/MOS logic to the IEEE Standard 488-1978 General Purpose Interface Bus (GPIB). PNP inputs are used at all driver inputs for minimum loading, and hysteresis is provided at all receiver inputs for added noise margin. The IEEE-488 required bus termination is provided internally with an active turn-off feature which disconnects the termination from the bus when V_{CC} is removed. A power up/down protection circuit is included at all bus outputs to provide glitch-free operation during V_{CC} power up or down.

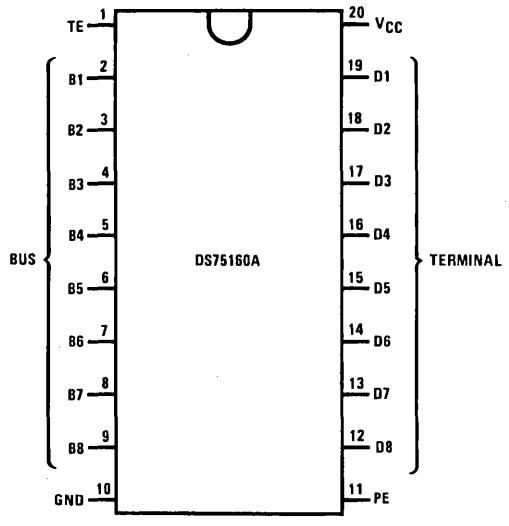
The General Purpose Interface Bus is comprised of 16 signal lines — 8 for data and 8 for interface management. The data lines are always implemented with DS75160A, and the management lines are either implemented with DS75161A in a single-controller system, or with DS75162A in a multi-controller system.

Features

- 8-channel bi-directional non-inverting transceivers
- Bi-directional control implemented with TRI-STATE® output design
- Meets IEEE Standard 488-1978
- High-speed Schottky design
- Low power consumption
- High impedance PNP inputs (drivers)
- 500 mV (typ) input hysteresis (receivers)
- On-chip bus terminators
- No bus loading when V_{CC} is removed
- Power up/down protection (glitch-free)
- Pin selectable open collector mode on DS75160A driver outputs
- Accommodates multi-controller systems

Connection Diagrams

Dual-In-Line Package



TL/F/5804–1

Top View

Order Number DS75160AN
See NS Package Number N20A

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage, V_{CC}	7.0V
Input Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 4 sec.)	260°C
Maximum Power Dissipation* at 25°C	
Molded Package	1897 mW

*Derate molded package 15.2 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
V_{CC}, Supply Voltage	4.75	5.25	V
T_A, Ambient Temperature	0	70	°C
I_{OL}, Output Low Current			
Bus		48	mA
Terminal		16	mA

Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter		Conditions		Min	Typ	Max	Units
V_{IH}	High-Level Input Voltage				2			V
V_{IL}	Low-Level Input Voltage						0.8	V
V_{IK}	Input Clamp Voltage		I_I = −18 mA			−0.8	−1.5	V
V_{HYS}	Input Hysteresis	Bus			400	500		mV
V_{OH}	High-Level Output Voltage	Terminal	I_{OH} = −800 μA		2.7	3.5		V
		Bus (Note 5)	I_{OH} = −5.2 mA		2.5	3.4		
V_{OL}	Low-Level Output Voltage	Terminal	I_{OL} = 16 mA			0.3	0.5	V
		Bus	I_{OH} = 48 mA			0.4	0.5	
I_{IH}	High-Level Input Current	Terminal and TE, PE, DC, SC Inputs	V_I = 5.5V			0.2	100	μA
			V_I = 2.7V			0.1	20	
I_{IL}	Low-Level Input Current		V_I = 0.5V			−10	−100	μA
V_{BIAS}	Terminator Bias Voltage at Bus Port	Bus	Driver Disabled	$I_{I(bus)}$ = 0 (No Load)	2.5	3.0	3.7	V
I_{LOAD}	Terminator Bus Loading Current		Driver Disabled	$V_{I(bus)}$ = −1.5V to 0.4V	−1.3			mA
				$V_{I(bus)}$ = 0.4V to 2.5V	0		−3.2	
				$V_{I(bus)}$ = 2.5V to 3.7V			2.5 −3.2	
				$V_{I(bus)}$ = 3.7V to 5V	0		2.5	
				$V_{I(bus)}$ = 5V to 5.5V	0.7		2.5	
			V_{CC} = 0, $V_{I(bus)}$ = 0V to 2.5V				40	μA
I_{OS}	Short-Circuit Output Current	Terminal	V_I = 2V, V_O = 0V (Note 4)		−15	−35	−75	mA
		Bus (Note 5)			−35	−75	−150	
I_{CC}	Supply Current	DS75160A	Transmit, TE = 2V, PE = 2V, V_I = 0.8V			85	125	mA
			Receive, TE = 0.8V, PE = 2V, V_I = 0.8V			70	100	
		DS75161A	TE = 0.8V, DC = 0.8V, V_I = 0.8V			84	125	
		DS75162A	TE = 0.8V, DC = 0.8V, SC = 2V, V_I = 0.8V			85	125	
C_{IN}	Bus-Port Capacitance	Bus	V_{CC} = 5V or 0V, V_I = 0V to 2V, f = 1 MHz			20	30	pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified, min/max limits apply across the 0°C to +70°C temperature range and the 4.75V to 5.25V power supply range. All typical values are for T_A = 25°C and V_{CC} = 5.0V.

Note 3: All currents into device pins are shown as positive; all currents out of device pins are shown as negative; all voltages are referenced to ground, unless otherwise specified. All values shown as max or min are so classified on absolute value basis.

Note 4: Only one output at a time should be shorted.

Note 5: This characteristic does not apply to outputs on DS75161A and DS75162A that are open collector.

Switching Characteristics V_{CC} = 5.0V ±5%, T_A = 0°C to 70°C (Note 1)

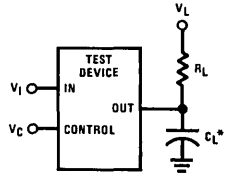
Symbol	Parameter	From	To	Conditions	DS75160A			DS75161A			DS75162A			Units
					Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{PLH}	Propagation Delay Time, Low to High Level Output	Terminal	Bus	V_L = 2.3V R_L = 38.3Ω C_L = 30 pF *Figure 1*		10	20		10	20		10	20	ns
t_{PHL}	Propagation Delay Time, High to Low Level Output					14	20		14	20		14	20	ns
t_{PLH}	Propagation Delay Time, Low to High Level Output	Bus	Terminal	V_L = 5.0V R_L = 240Ω C_L = 30 pF *Figure 2*		14	20		14	20		14	20	ns
t_{PHL}	Propagation Delay Time, High to Low Level Output					10	20		10	20		10	20	ns
t_{PZH}	Output Enable Time to High Level	TE, DC, or SC (Note 2) (Note 3)	Bus	V_I = 3.0V V_L = 0V R_L = 480Ω C_L = 15 pF *Figure 1*		19	32		23	40		23	40	ns
t_{PHZ}	Output Disable Time From High Level					15	22		15	25		15	25	ns
t_{PZL}	Output Enable Time to Low Level			V_I = 0V V_L = 2.3V R_L = 38.3Ω C_L = 15 pF *Figure 1*		24	35		28	48		28	48	ns
t_{PLZ}	Output Disable Time From Low Level					17	25		17	27		17	27	ns
t_{PZH}	Output Enable Time to High Level	TE, DC, or SC (Note 2) (Note 3)	Terminal	V_I = 3.0V V_L = 0V R_L = 3 kΩ C_L = 15 pF *Figure 1*		17	33		18	40		18	40	ns
t_{PHZ}	Output Disable Time From High Level					15	25		22	33		22	33	ns
t_{PZL}	Output Enable Time to Low Level			V_I = 0V V_L = 5V R_L = 280Ω C_L = 15 pF *Figure 1*		25	39		28	52		28	52	ns
t_{PLZ}	Output Disable Time From Low Level					15	27		20	35		20	35	ns
t_{PZH}	Output Pull-Up Enable Time (DS75160A Only)	PE (Note 2)	Bus	V_I = 3V V_L = 0V R_L = 480Ω C_L = 15 pF *Figure 1*		10	17		NA			NA		ns
t_{PHZ}	Output Pull-UP Disable Time (DS75160A Only)					10	15		NA			NA		ns

Note 1: Typical values are for V_{CC} = 5.0V and T_A = 25°C and are meant for reference only.

Note 2: Refer to Functional Truth Tables for control input definition.

Note 3: Test configuration should be connected to only one transceiver at a time due to the high current stress caused by the V_I voltage source when the output connected to that input becomes active.

Switching Load Configurations



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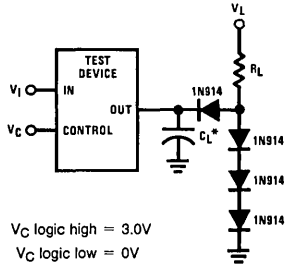
V_C logic high = 3.0V
V_C logic low = 0V

*C_L includes jig and probe capacitance

FIGURE 1



V_C logic high = 3.0V
V_C logic low = 0V

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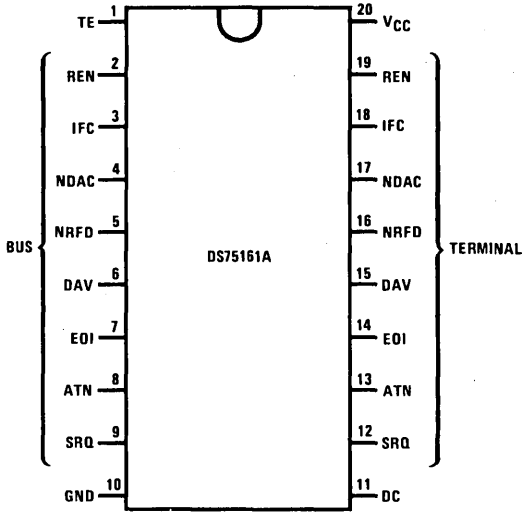
*C_L includes jig and probe capacitance

FIGURE 2

2

Connection Diagrams (Continued)

Dual-In-Line Package



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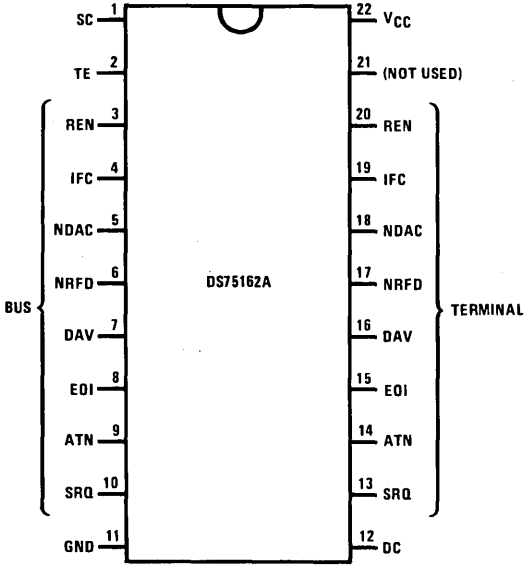
Top View

Dual-In-Line Package



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Top View

Order Number DS75161AN or DS75162AN
See NS Package Number N20A or N22A

Functional Description

DS75160A

This device is an 8-channel bi-directional transceiver with one common direction control input, denoted TE. When used to implement the IEEE-488 bus, this device is connected to the eight data bus lines, designated DIO_1–DIO_8. The port connections to the bus lines have internal terminators, in accordance with the IEEE-488 Standard, that are deactivated when the device is powered down. This feature guarantees no bus loading when V_{CC} = 0V. The bus port outputs also have a control mode that either enables or disables the active upper stage of the totem-pole configuration. When this control input, denoted PE, is in the high state, the bus outputs operate in the high-speed totem-pole mode. When PE is in the low state, the bus outputs operate as open collector outputs which are necessary for parallel polling.

DS75161A

This device is also an 8-channel bi-directional transceiver which is specifically configured to implement the eight management signal lines of the IEEE-488 bus. This device, paired with the DS75160A, forms the complete 16-line interface between the IEEE-488 bus and a single controller instrumentation system. In compliance with the system organization of the management signal lines, the SRQ, NDAC, and NRFD bus port outputs are open collector. In contrast to the DS75160A, these open collector outputs are a fixed configuration. The direction control is divided into three groups. The DAV, NDAC, and NRFD transceiver directions are controlled by the TE input. The ATN, SRQ, REN, and IFC transceiver directions are controlled by the DC input. The EOI transceiver direction is a function of both the TE and DC inputs, as well as the logic level present on the ATN channel. The port connections to the bus lines have internal terminators identical to the DS75160A.

DS75162A

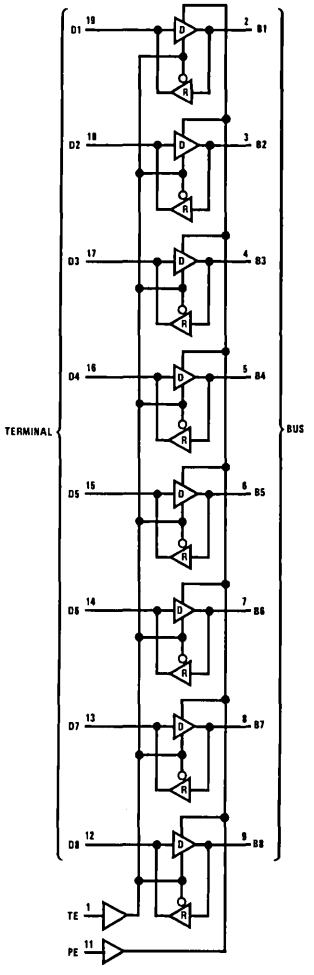
This device is identical to the DS75161A, except that an additional direction control input is provided, denoted SC. The SC input controls the direction of the REN and IFC transceivers that are normally controlled by the DC input on the DS75161A. This additional control function is instrumental in implementing multiple controller systems.

Table of Signal Line Abbreviations

Signal Line Classification	Mnemonic	Definition	Device
Control Signals	DC	Direction Control	DS75161A/ DS75162A
	PE	Pull-Up Enable	DS75160A
	TE	Talk Enable	All
	SC	System Controller	DS75162A
Data I/O Ports	B1–B8	Bus Side of Device	DS75160A
	D1–D8	Terminal Side of Device	
Management Signals	ATN	Attention	DS75161A/ DS75162A
	DAV	Data Valid	
	EOI	End or Identify	
	IFC	Interface Clear	
	NDAC	Not Data Accepted	
	NRFD	Not Ready for Data	
	REN	Remote Enable	
	SRQ	Service Request	

Logic Diagrams

DS75160A



Note 1: D Denotes driver

Note 2: R Denotes receiver

Note 3: Driver and receiver outputs are totem-pole configurations

Note 4: The driver outputs of DS75160A can have their active pull-ups disabled by switching the PE input (pin 11) to the logic low state. This mode configures the outputs as open collector.

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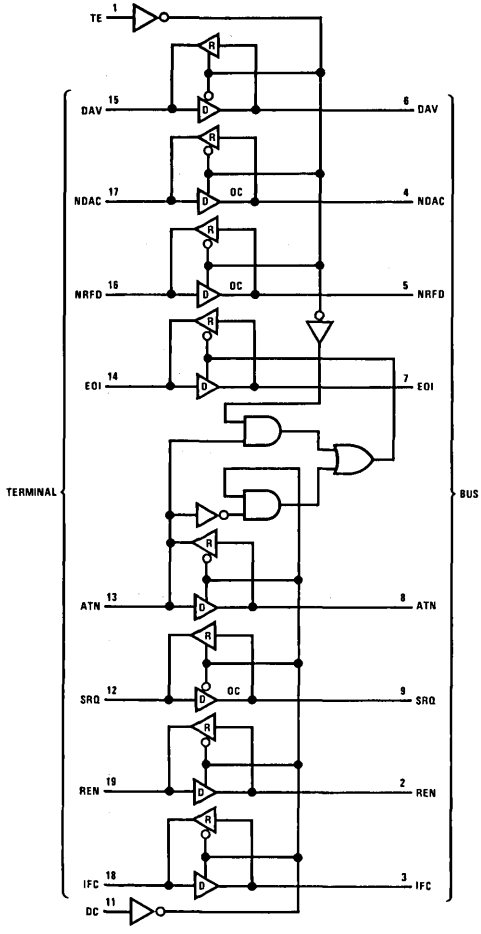
Logic Diagrams (Continued)

DS75161A



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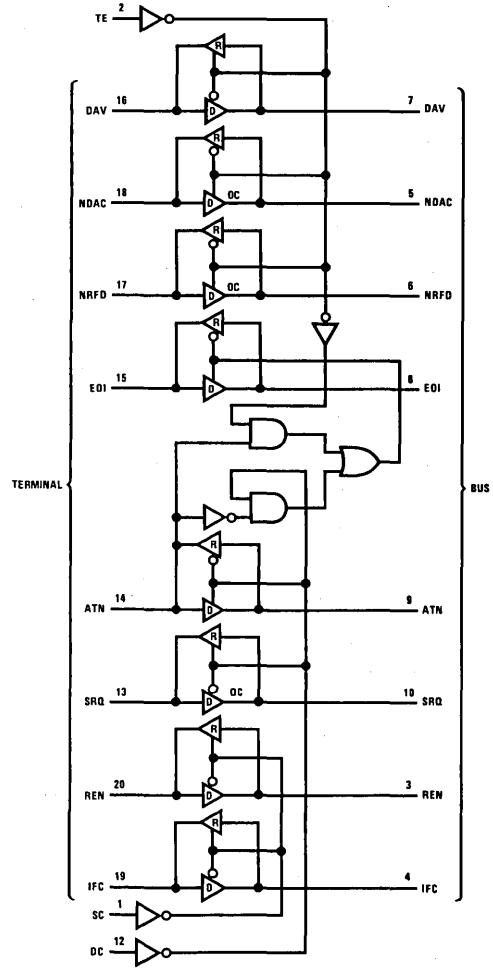
DS75162A



TL/F/5804–6

Note 1: Denotes driver

Note 2: Denotes receiver

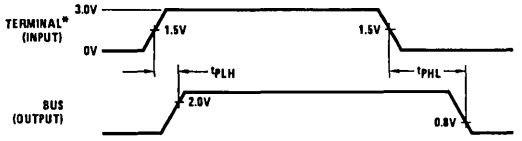
Note 3: Symbol "OC" specifies open collector output

Note 4: Driver and receiver outputs that are not specified "OC" are totem-pole configurations

TL/F/5804–7

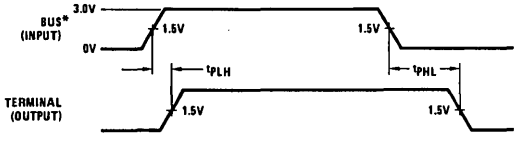
Switching Waveforms

Transmit Propagation Delays



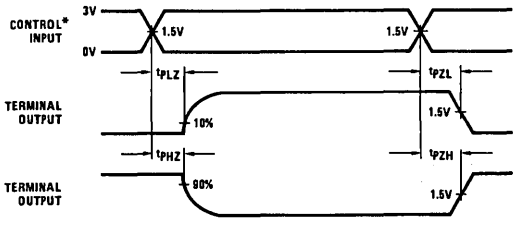
TL/F/5804–10

Receive Propagation Delays



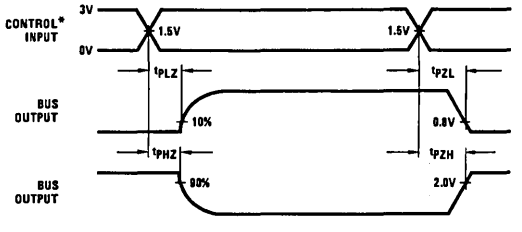
TL/F/5804–11

Terminal Enable/Disable Times



TL/F/5804–12

Bus Enable/Disable Times

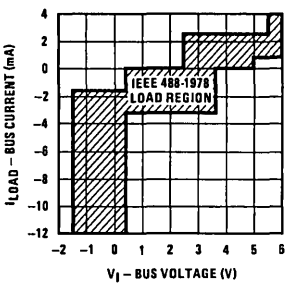


TL/F/5804–13

*Input signal: f = 1.0 MHz, 50% duty cycle, $t_r = t_f \leq 5$ ns

Performance Characteristics

Bus Port Load Characteristics



TL/F/5804–14

Refer to Electrical Characteristics table

Functional Truth Tables

DS75160A

Control Input Level		Data Transceivers	
TE	PE	Direction	Bus Port Configuration
H	H	T	Totem-Pole Output
H	L	T	Open Collector Output
L	X	R	Input

DS75161A

Control Input Level				Transceiver Signal Direction						
TE	DC	ATN*		EOI	REN	IFC	SRQ	NRFD	NDAC	DAV
H	H		R		R	R	T	R	R	T
H	L		T		T	T	R	R	R	T
L	H		R		R	R	T	T	T	R
L	L		T		T	T	R	T	T	R
H	X	H		T						
L	X	H		R						
X	H	L		R						
X	L	L		T						

DS75162A

Control Input Level				Transceiver Signal Direction						
SC	TE	DC	ATN*	EOI	REN	IFC	SRQ	NRFD	NDAC	DAV
H	H	H	R		T	T	T	R	R	T
H	H	L	T		T	T	R	R	R	T
H	L	H	R		T	T	T	T	T	R
H	L	L	T		T	T	R	T	T	R
L	H	H	R		R	R	T	R	R	T
L	H	L	T		R	R	R	R	R	T
L	L	H	R		R	R	T	T	T	R
L	L	L	T		R	R	R	T	T	R
X	H	X	H	T						
X	L	X	H	R						
X	X	H	L	R						
X	X	L	L	T						

H = High level input

L = Low level input

X = Don't care

T = Transmit, i.e., signal outputted to bus

R = Receive, i.e., signal outputted to terminal

*The ATN signal level is sensed for internal multiplex control of EOI transmission direction logic.

National Semiconductor Corporation

DS7640/DS8640 Quad NOR Unified Bus Receiver

General Description

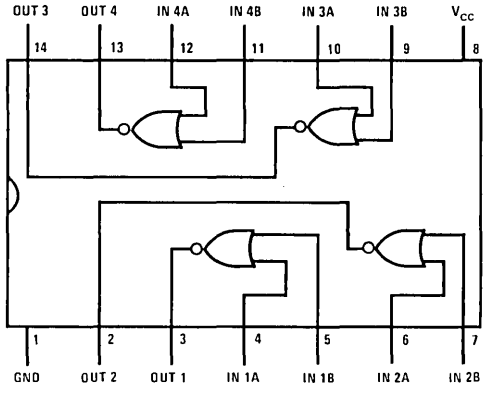
The DS7640 and DS8640 are quad 2-input receivers designed for use in bus organized data transmission systems interconnected by terminated 120Ω impedance lines. The external termination is intended to be 180Ω resistor from the bus to the +5V logic supply together with a 390Ω resistor from the bus to ground. The design employs a built-in input threshold providing substantial noise immunity. Low input current allows up to 27 driver/receiver pairs to utilize a common bus.

Features

- Low input current with normal V_{CC} or V_{CC} = 0V (30 μA typ)
- High noise immunity (1.1V typ)
- Temperature-insensitive input thresholds track bus logic levels
- TTL compatible output
- Matched, optimized noise immunity for "1" and "0" levels
- High speed (19 ns typ)

Connection Diagram

Dual-In-Line Package



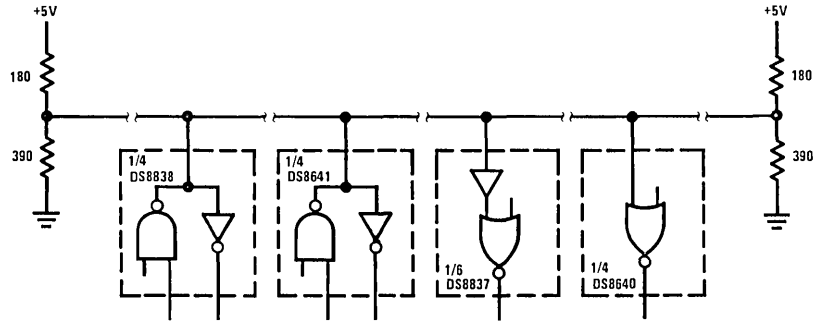
TL/F/5805–1

Top View

Order Number DS7640J, DS8640J or DS8640N
See NS Package Number J14A or N14A

Typical Application

120Ω Unified Data Bus



TL/F/5805–2

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7.0V
Input Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1308 mW
Molded Package	1207 mW
Lead Temperature (Soldering, 4 seconds)	260°C

*Derate cavity package 8.7 mW/°C above 25°C; derate molded package 9.7 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
DS7640	4.5	5.5	V
DS8640	4.75	5.25	V
Temperature (T_A)			
DS7640	−55	+125	°C
DS8640	0	+70	°C

Electrical Characteristics

The following apply for $V_{MIN} \le V_{CC} \le V_{MAX}$, $T_{MIN} \le T_A \le T_{MAX}$, unless otherwise specified (Notes 2 and 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IH}	High Level Input Threshold	$V_{OUT} = V_{OL}$	DS7640	1.80	1.50		V
			DS8640	1.70	1.50		V
V_{IL}	Low Level Input Threshold	$V_{OUT} = V_{OH}$	DS7640		1.50	1.20	V
			DS8640		1.50	1.30	V
I_{IH}	Maximum Input Current	$V_{IN} = 4V$	$V_{CC} = V_{MAX}$		30	80	μA
			$V_{CC} = 0V$		1.0	50	μA
I_{IL}	Maximum Input Current	$V_{IN} = 0.4V$, $V_{CC} = V_{MAX}$			1.0	50	μA
V_{OH}	Output Voltage	$I_{OH} = -400\ \mu A$, $V_{IN} = V_{IL}$		2.4			V
V_{OL}	Output Voltage	$I_{OL} = 16$ mA, $V_{IN} = V_{IH}$			0.25	0.4	V
I_{OS}	Output Short Circuit Current	$V_{IN} = 0.5V$, $V_{OS} = 0V$, $V_{CC} = V_{MAX}$, (Note 4)		−18		−55	mA
I_{CC}	Power Supply Current	$V_{IN} = 4V$, (Per Package)			25	40	mA

Switching Characteristics $T_A = 25°C$, nominal power supplies unless otherwise noted

Symbol	Parameter	Conditions		Min	Typ	Max	Units
t_{pd}	Propagation Delays	(Notes 5 and 6)	Input to Logic "1" Output	10	23	35	ns
			Input to Logic "0" Output	10	15	30	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS7640 and across the 0°C to +70°C range for the DS8640. All typical values are $T_A = 25°C$ and $V_{CC} = 5V$.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Only one output at a time should be shorted.

Note 5: Fan-out of 10 load, $C_{LOAD} = 15$ pF total, measured from $V_{IN} = 1.5V$ to $V_{OUT} = 1.5V$, $V_{IN} = 0V$ to 3V pulse.

Note 6: Apply to $V_{CC} = 5V$, $T_A = 25°C$.

National Semiconductor Corporation

DS7641/DS8641 Quad Unified Bus Transceiver

General Description

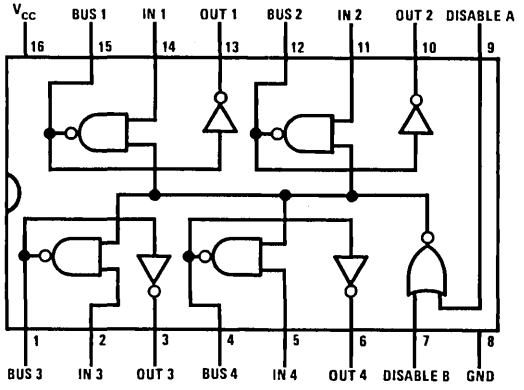
The DS7641 and DS8641 are quad high speed drivers/receivers designed for use in bus organized data transmission systems interconnected by terminated 120Ω impedance lines. The external termination is intended to be a 180Ω resistor from the bus to the +5V logic supply together with a 390Ω resistor from the bus to ground. The bus can be terminated at one or both ends. Low bus pin current allows up to 27 driver/receiver pairs to utilize a common bus. The bus loading is unchanged when V_{CC} = 0V. The receivers incorporate tight thresholds for better bus noise immunity. One two-input NOR gate is included to disable all drivers in a package simultaneously.

Features

- 4 separate driver/receiver pairs per package
- Guaranteed minimum bus noise immunity of 0.6V, 1.1V typ
- Temperature insensitive receiver thresholds track bus logic levels
- 30 μA typical bus terminal current with normal V_{CC} or with V_{CC} = 0V
- Open collector driver output allows wire-OR connection
- High speed
- Series 74 TTL compatible driver and disable inputs and receiver outputs

Connection Diagram

Dual-In-Line Package



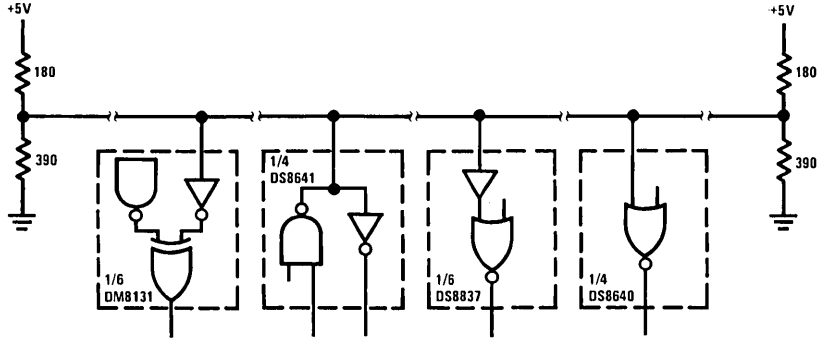
TL/F/5806–1

Top View

Order Number DS7641J, DS8641J or DS8641N
See NS Package Number J16A or N16A

Typical Application

120Ω Unified Data Bus



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Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input and Output Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1433 mW
Molded Package	1362 mW
Lead Temperature (Soldering, 4 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage, (V_{CC})			
DS7641	4.5	5.5	V
DS8641	4.75	5.25	V
Temperature Range, (T_A)			
DS7641	−55	+125	°C
DS8641	0	+70	°C

*Derate cavity package 9.6 mW/°C above 25°C; derate molded package 10.9 mW/°C above 25°C.

Electrical Characteristics

The following apply for $V_{MIN} \le V_{CC} \le V_{MAX}$, $T_{MIN} \le T_A \le T_{MAX}$ unless otherwise specified (Notes 2 and 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
DRIVER AND DISABLE INPUTS							
V_{IH}	Logical "1" Input Voltage			2.0			V
V_{IL}	Logical "0" Input Voltage					0.8	V
I_I	Logical "1" Input Current	$V_{IN} = 5.5V$				1	mA
I_{IH}	Logical "1" Input Current	$V_{IN} = 2.4V$				40	μA
I_{IL}	Logical "0" Input Current	$V_{IN} = 0.4V$				−1.6	mA
V_{CL}	Input Diode Clamp Voltage	$I_{DIS} = -12$ mA, $I_{IN} = -12$ mA, $I_{BUS} = -12$ mA, $T_A = 25°C$			−1	−1.5	V
DRIVER OUTPUT/RECEIVER INPUT							
V_{OLB}	Low Level Bus Voltage	$V_{DIS} = 0.8V$, $V_{IN} = 2V$, $I_{BUS} = 50$ mA			0.4	0.7	V
I_{IHB}	Maximum Bus Current	$V_{IN} = 0.8V$, $V_{BUS} = 4V$, $V_{CC} = V_{MAX}$			30	100	μA
I_{ILB}	Maximum Bus Current	$V_{IN} = 0.8V$, $V_{BUS} = 4V$, $V_{CC} = 0V$			2	100	μA
V_{IH}	High Level Receiver Threshold	$V_{IND} = 0.8V$, $V_{OL} = 16$ mA	DS7641	1.80	1.50		V
			DS8641	1.70	1.50		V
V_{IL}	Low Level Receiver Threshold	$V_{IND} = 0.8V$, $V_{OH} = -400$ μA	DS7641		1.50	1.20	V
			DS8641		1.50	1.30	V
RECEIVER OUTPUT							
V_{OH}	Logical "1" Output Voltage	$V_{IN} = 0.8V$, $V_{BUS} = 0.5V$, $I_{OH} = -400$ μA		2.4			V
V_{OL}	Logical "0" Output Voltage	$V_{IN} = 0.8V$, $V_{BUS} = 4V$, $I_{OL} = 16$ mA			0.25	0.4	V
I_{OS}	Output Short Circuit Current	$V_{DIS} = 0.8V$, $V_{IN} = 0.8V$, $V_{BUS} = 0.5V$, $V_{OS} = 0V$, $V_{CC} = V_{MAX}$, (Note 4)		−18		−55	mA
I_{CC}	Supply Current	$V_{DIS} = 0V$, $V_{IN} = 2V$, (per Package)			50	70	mA

Switching Characteristics $T_A = 25°C$, $V_{CC} = 5V$, unless otherwise indicated

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PD}	Propagation Delays (Note 7)	(Note 5)				
	Disable to Bus "1"			19	30	ns
	Disable to Bus "0"			15	30	ns
	Driver Input to Bus "1"			17	25	ns
	Driver Input to Bus "0"			17	25	ns
	Bus to Logical "1" Receiver Output	(Note 6)		20	30	ns
	Bus to Logical "0" Receiver Output			18	30	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS7641 and across the 0°C to +70°C range for the DS8641. All typical values are for $T_A = 25°C$ and $V_{CC} = 5V$.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Only one output at a time should be shorted.

Note 5: 91Ω from bus pin to V_{CC} and 200Ω from bus pin to ground. $C_{LOAD} = 15$ pF total. Measured from $V_{IN} = 1.5V$ to $V_{BUS} = 1.5V$, $V_{IN} = 0V$ to 3V pulse.

Note 6: Fan-out of 10 load, $C_{LOAD} \approx 15$ pF total. Measured from $V_{IN} = 1.5V$ to $V_{OUT} = 1.5V$, $V_{IN} = 0V$ to 3V pulse.

Note 7: The following apply for $V_{CC} = 5V$, $T_A = 25°C$ unless otherwise specified.

National Semiconductor Corporation

DS7833/DS8833/DS7835/DS8835
Quad TRI-STATE® Bus Transceivers

General Description

This family of TRI-STATE bus transceivers offers extreme versatility in bus organized data transmission systems. The data bus may be unterminated, or terminated DC or AC, at one or both ends. Drivers in the third (high impedance) state load the data bus with a negligible leakage current. The receiver input current is low allowing at least 100 driver/receiver pairs to utilize a single bus. The bus loading is unchanged when V_{CC} = 0V. The receiver incorporates hysteresis to provide greater noise immunity. All devices utilize a high current TRI-STATE output driver. The DS7833/DS8833 and DS7835/DS8835 employ TRI-STATE outputs on the receiver also.

The DS7833/DS8833 are non-inverting quad transceivers with a common inverter driver disable control and common inverter receiver disable control.

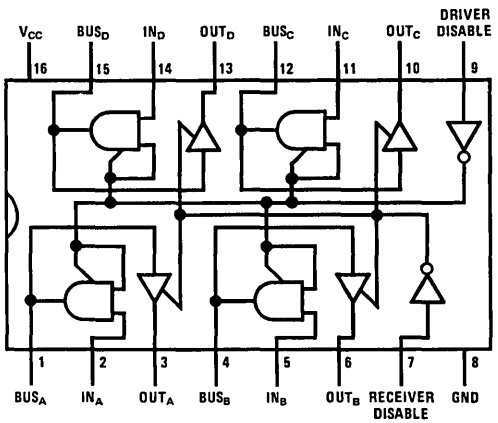
The DS7835/DS8835 are inverting quad transceivers with a common inverter driver disable control and a common inverter receiver disable control.

Features

- Receiver hysteresis — 400 mV typ
- Receiver noise immunity — 1.4V typ
- Bus terminal current for normal V_{CC} or V_{CC} = 0V — 80 μA max
- Receivers
  - Sink — 16 mA at 0.4V max
  - Source — 2.0 mA (Mil) at 2.4V min; 5.2 mA (Com) at 2.4V min
- Drivers
  - Sink — 50 mA at 0.5V max; 32 mA at 0.4V max
  - Source — 10.4 mA (Com) at 2.4V min; 5.2 mA (Mil) at 2.4V min
- Drivers have TRI-STATE outputs
- DS7833/DS8833, DS7835/DS8835 receivers have TRI-STATE outputs
- Capable of driving 100Ω DC—terminated buses
- Compatible with Series 54/74

Connection Diagram

Dual-In-Line Package



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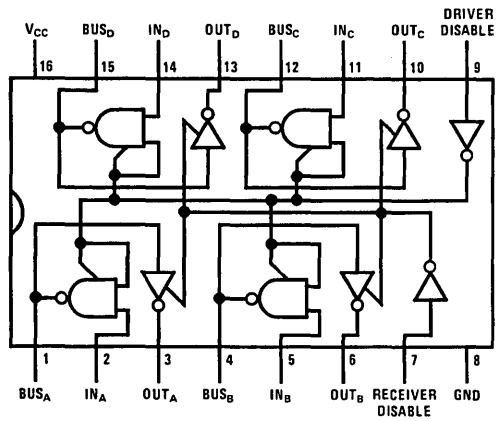
Top View

Order Number DS7833J, DS8833J or DS8833N
See NS Package Number J16A or N16A

Dual-In-Line Package



TL/F/5808–2

Top View

Order Number DS7835J, DS8835J or DS8835N
See NS Package Number J16A or N16A

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7.0V
Input Voltage	5.5V
Output Voltage	5.5V
Storage Temperature	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1509 mW
Molded Package	1476 mW
Lead Temperature (Soldering, 4 sec.)	260°C

*Derate cavity package 10.1 mW/°C above 25°C; derate molded package 11.8 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage, V_{CC}			
DS7833/DS7835	4.5	5.5	V
DS8833/DS8835	4.75	5.25	V
Temperature (T_A)			
DS7833/DS7835	−55	+125	°C
DS8833/DS8835	0	+70	°C

Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions			Min	Typ	Max	Units
DISABLE/DRIVER INPUT								
V_{IH}	High Level Input Voltages	V_{CC} = Min			2.0			V
V_{IL}	Low Level Input Voltage	V_{CC} = Min	DS7833, DS8833, DS8835				0.8	V
			DS7835				0.7	
I_{IH}	High Level Input Current	V_{CC} = Max	V_{IN} = 2.4V				40	μA
			V_{IN} = 5.5V				1.0	mA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_{IN} = 0.4V				−1.0	−1.6	mA
V_{CL}	Input Clamp Diode	V_{CC} = 5.0V, I_{IN} = −12 mA, T_A = 25°C				−0.8	−1.5	V
I_{IT}	Driver Low Level Disabled Input Current	Driver Disable Input = 2.0V, V_{IN} = 0.4V					−40	μA
RECEIVER INPUT/BUS OUTPUT								
V_{TH}	High Level Threshold Voltage			DS7833, DS7835	1.4	1.75	2.1	V
				DS8833, DS8835	1.5	1.75	2.0	V
V_{TL}	Low Level Threshold Voltage			DS7833, DS7835	0.8	1.35	1.6	V
				DS8833, DS8835	0.8	1.35	1.5	V
I_S	Bus Current, Output Disabled or High	V_{BUS} = 4.0V	V_{CC} = Max			25	80	μA
			V_{CC} = 0V			5.0	80	μA
		V_{CC} = Max, V_{BUS} = 0.4V				−2.0	−40	μA
V_{OH}	Logic "1" Output Voltage	V_{CC} = Min	I_{OUT} = −5.2 mA	DS7833, DS7835	2.4	2.75		V
			I_{OUT} = −10.4 mA	DS8833, DS8835	2.4	2.75		V
V_{OL}	Logic "0" Output Voltage	V_{CC} = Min	I_{OUT} = 50 mA			0.28	0.5	V
			I_{OUT} = 32 mA				0.4	V
I_{OS}	Output Short Circuit Current	V_{CC} = Max, (Note 4)			−40	−62	−120	mA
RECEIVER OUTPUT								
V_{OH}	Logic "1" Output Voltage	V_{CC} = Min	I_{OUT} = −2.0 mA	DS7833, DS7835	2.4	3.0		V
			I_{OUT} = −5.2 mA	DS8833, DS8835	2.4	2.9		V
V_{OL}	Logic "0" Output Voltage	V_{CC} = Min, I_{OUT} = 16 mA				0.22	0.4	V
I_{OT}	Output Disabled Current	V_{CC} = Max, Disable	V_{OUT} = 2.4V				40	μA
		Inputs = 2.0V	V_{OUT} = 0.4V				−40	μA

2

Electrical Characteristics (Notes 2 and 3) (Continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
RECEIVER OUTPUT (Continued)							
I_{OS}	Output Short Circuit Current	V_{CC} = Max, (Note 4)	DS7833, DS7835	28	−40	−70	mA
			DS8833, DS8835	−30		−70	mA
I_{CC}	Supply Current	V_{CC} = Max	DS7833, DS8833		84	116	mA
			DS7835, DS8835		75	95	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS7833, DS7835 and across the 0°C to +70°C range for the DS8833, DS8835. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Only one output at a time should be shorted.

Switching Characteristics V_{CC} = 5.0V, T_A = 25°C

Symbol	Parameter	Conditions		Min	Typ	Max	Units
t_{pd0}	Propagation Delay to a Logic "0" from Input to Bus	*(Figure 1)*	DS7833/DS8833		14	30	ns
			DS7835/DS8835		10	20	ns
t_{pd1}	Propagation Delay to a Logic "1" from Input to Bus	*(Figure 1)*	DS7833/DS8833		14	30	ns
			DS7835/DS8835		11	30	ns
t_{pd0}	Propagation Delay to a Logic "0" from Bus to Input	*(Figure 2)*	DS7833/DS8833		24	45	ns
			DS7835/DS8835		16	35	ns
t_{pd1}	Propagation Delay to a Logic "1" from Bus to Input	*(Figure 2)*	DS7833/DS8833		12	30	ns
			DS7835/DS8835		18	30	ns
t_{PHZ}	Delay from Disable Input to High Impedance State (from Logic "1" Level)	C_L = 5.0 pF, (*Figures 1* and *2*)	Driver		8.0	20	ns
			Receiver		6.0	15	ns
t_{PLZ}	Delay from Disable Input to High Impedance State (from Logic "0" Level)	C_L = 5.0 pF, (*Figures 1* and *2*)	Driver		20	35	ns
			Receiver		13	25	ns
t_{PZH}	Delay from Disable Input to Logic "1" Level (from High Impedance State)	C_L = 5.0 pF, (*Figures 1* and *2*)	Driver		24	40	ns
			Receiver		16	35	ns
t_{PZL}	Delay from Disable Input to Logic "0" Level (from High Impedance State)	C_L = 5.0 pF, (*Figures 1* and *2*)	Driver		19	35	ns
			Receiver DS7833/DS8833		15	30	ns
			Receiver DS7835/DS8835		33	50	ns

AC Test Circuits

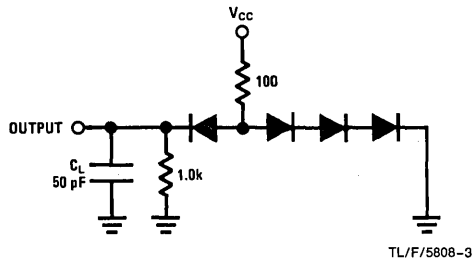


FIGURE 1. Driver Output Load

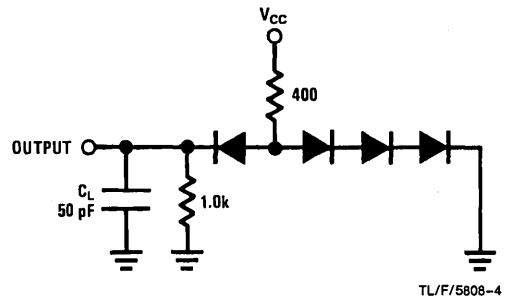
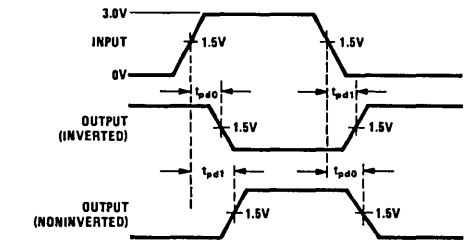


FIGURE 2. Receiver Output Load

Switching Time Waveforms

t_{pd1} & t_{pd0}



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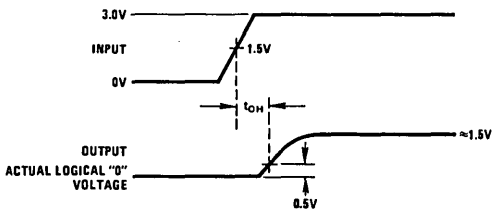
t_{PLZ}



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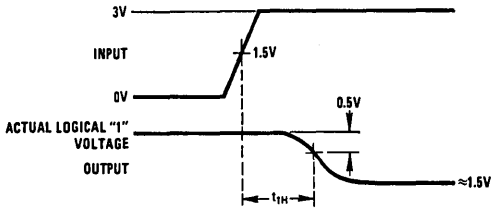
f = 1 MHz
$t_r = t_f \leq 10$ ns (10% to 90%)
DUTY CYCLE = 50%

t_{PHZ}



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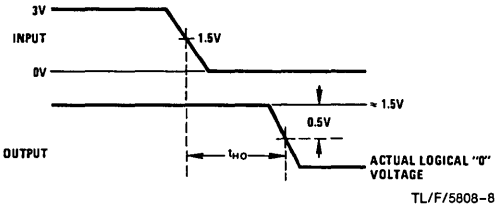
t_{PZL}



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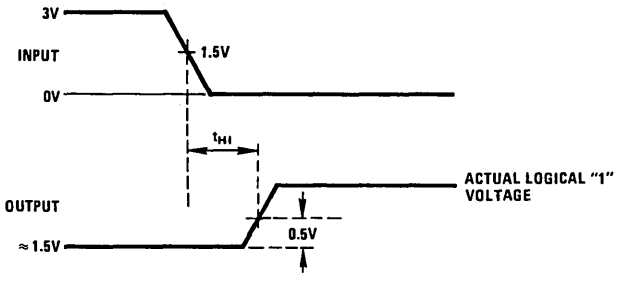
t_{PZH}



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2

National Semiconductor Corporation

DS7834/DS8834/DS7839/DS8839 Quad TRI-STATE® Bus Transceivers

General Description

This family of TRI-STATE bus transceivers offers extreme versatility in bus organized data transmission systems. The data bus may be unterminated, or terminated DC or AC, at one or both ends. Drivers in the third (high impedance) state load the data bus with a negligible leakage current. The receiver input current is low, allowing at least 100 driver/receiver pairs to utilize a single bus. The bus loading is unchanged when V_{CC} = 0V. The receiver incorporates hysteresis to provide greater noise immunity. Both devices utilize a high current TRI-STATE output driver. The DS7834/DS8834 and DS7839/DS8839 employ TTL outputs on the receiver.

The DS7839/DS8839 are non-inverting quad tranceivers with two common inverter driver disable controls.

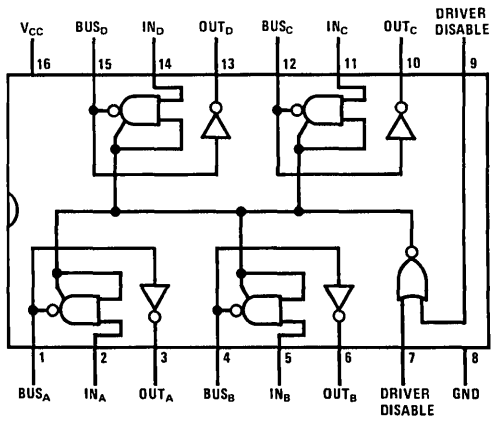
The DS7834/DS8834 are inverting quad transceivers with two common inverter driver disable controls.

Features

- Receiver hysteresis — 400 mV typ
- Receiver noise immunity — 1.4V typ
- Bus terminal current for normal V_{CC} or V_{CC} = 0V — 80 μA max
- Receivers
  - Sink — 16 mA at 0.4V max
  - Source — 2.0 mA (Mil) at 2.4V min; 5.2 mA (Com) at 2.4V min
- Drivers
  - Sink — 50 mA at 0.5V max; 32 mA at 0.4V max
  - Source — 10.4 mA (Com) at 2.4V min; 5.2 mA (Mil) at 2.4V min
- Drivers have TRI-STATE outputs
- Receivers have TRI-STATE outputs
- Capable of driving 100Ω DC-terminated Buses
- Compatible with Series 54/74

Connection Diagrams

Dual-In-Line Package

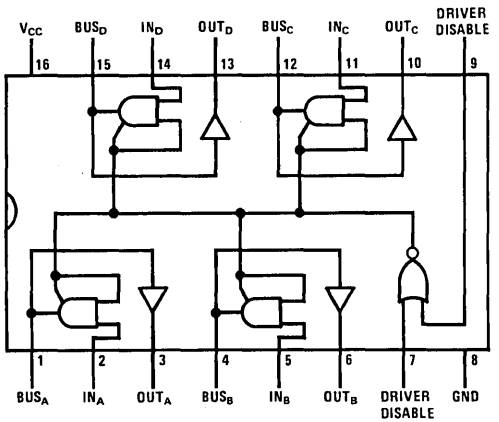


TL/F/5809–1

Top View

Order Number DS7834J, DS8834J or DS8834N
See NS Package Number J16A or N16A

Dual-In-Line Package



TL/F/5809–2

Top View

Order Number DS7839J, DS8839J or DS8839N
See NS Package Number J16A or N16A

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7.0V
Input Voltage	5.5V
Output Voltage	5.5V
Maximum Power Dissipation* at 25°C	
Cavity Package	1509 mW
Molded Package	1476 mW

*Derate cavity package 10.1 mW/°C above 25°C; derate molded package 11.8 mW/°C above 25°C.

Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 4 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
DS7834, DS7839	4.5	5.5	V
DS8834, DS8839	4.75	5.25	V
Temperature (T_A)			
DS7834, DS7839	−55	+125	°C
DS8834, DS8839	0	+70	°C

Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions			Min	Typ	Max	Units
DISABLE/DRIVER INPUT								
V_{IH}	High Level Input Voltage	V_{CC} = Min			2.0			V
V_{IL}	Low Level Input Voltage	V_{CC} = Min					0.8	V
I_{IH}	High Level Input Current	V_{CC} = Max	V_{IN} = 2.4V				40	μA
			V_{IN} = 5.5V				1.0	mA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_{IN} = 0.4V				−1.0	−1.6	mA
I_{IND}	Driver Diasbled Input Low Current	Driver Disable Input = 2.0V, V_{IN} = 0.4V					−40	μA
V_{CL}	Input Clamp Diode	V_{CC} = 5.0V, I_{IN} = −12 mA, T_A = 25°C				−0.8	−1.5	V
RECEIVER INPUT/BUS OUTPUT								
V_{TH}	High Level Threshold Voltage	V_{CC} = Max		DS7834, DS7839	1.4	1.75	2.1	V
				DS8834, DS8839	1.5	1.75	2.0	V
V_{TL}	Low Level Threshold Voltage	V_{CC} = Min		DS7834, DS7839	0.8	1.35	1.6	V
				DS8834, DS8839	0.8	1.35	1.5	V
I_{BH}	Bus Current, Output Disabled or High	V_{BUS} = 4.0V	V_{CC} = Max, Disable Input = 2.0V			25	80	μA
			V_{CC} = 0V			5.0	80	μA
		V_{CC} = Max, V_{SUS} = 0.4V, Disable Input = 2.0V					−40	μA
V_{OH}	Logic "1" Output Voltage	V_{CC} = Min	I_{OUT} = −5.2 mA	DS7834, DS7839	2.4	2.75		V
			I_{OUT} = −10.4 mA	DS8839	2.4	2.75		V
V_{OL}	Logic "0" Output Voltage	V_{CC} = Min	I_{OUT} = 50 mA			0.28	0.5	V
			I_{OUT} = 32 mA				0.4	V
I_{OS}	Output Short Circuit Current	V_{CC} = Max, (Note 4)			−40	−62	−120	mA
RECEIVER OUTPUT								
V_{OH}	Logic "1" Output Voltage	V_{CC} = Min	I_{OUT} = −2.0 mA	DS7834, DS7839	2.4	3.0		V
			I_{OUT} = −5.2 mA	DS8834, DS8839	2.4	2.9		V
V_{OL}	Logic "0" Output Voltage	V_{CC} = Min, I_{OUT} = 16 mA				0.22	0.4	V
I_{OS}	Output Short Circuit Current	V_{CC} = Max, (Note 4)		DS7834, DS7839	−28	−40	−70	mA
				DS8834, DS8839	−30		−70	mA
I_{CC}	Supply Current	V_{CC} = Max				75	95	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified, min/max limits apply across the −55°C to +125°C temperature range for the DS7834, DS7839 and across the 0°C to +70°C range for the DS8834, DS8839. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Only one output at a time should be shorted.

Switching Characteristics V_{CC} = 5.0V, T_A = 25°C

Symbol	Parameter	Conditions		Min	Typ	Max	Units
t_{pd0}	Propagation Delay to a Logic "0" from Input to Bus	*(Figure 1)*	DS7839/DS8839		14	30	ns
			DS7834/DS8834		10	20	ns
t_{pd1}	Propagation Delay to a Logic "1" from Input to Bus	*(Figure 1)*	DS7839/DS8839		14	30	ns
			DS7834/DS8834		11	30	ns
t_{pd0}	Propagation Delay to a Logic "0" from Bus to Output	*(Figure 2)*	DS7839/DS8839		24	45	ns
			DS7834/DS8834		16	35	ns
t_{pd1}	Propagation Delay to a Logic "1" from Bus to Output	*(Figure 2)*	DS7839/DS8839		12	30	ns
			DS7834/DS8834		18	30	ns
t_{PHZ}	Delay from Disable Input to High Impedance State (from Logic "1" Level)	C_L = 5.0 pF, *(Figures 1* and *2)* Driver Only			8	20	ns
t_{PLZ}	Delay from Disable Input to High Impedance State (from Logic "0" Level)	C_L = 5.0 pF, *(Figures 1* and *2)* Driver Only			20	35	ns
t_{PZH}	Delay from Disable Input to Logic "1" Level (from High Impedance State)	C_L = 50 pF, *(Figures 1* and *2)* Driver Only			24	40	ns
t_{PZL}	Delay from Disable Input to Logic "0" Level (from High Impedance State)	C_L = 50 pF, *(Figures 1* and *2)* Driver Only			19	35	ns

AC Test Circuit

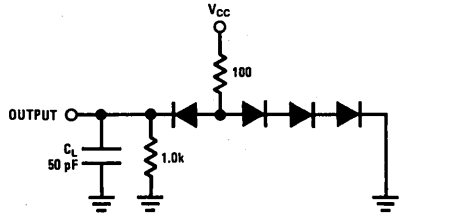


FIGURE 1. Driver Output Load

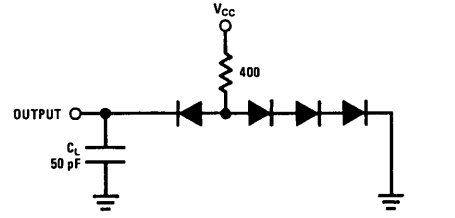
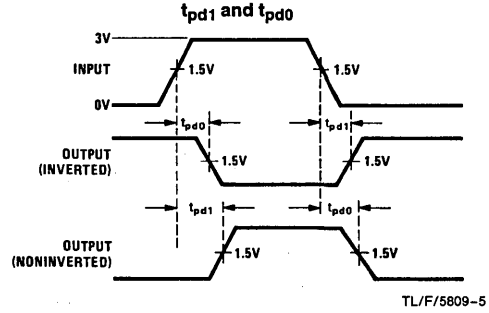


FIGURE 2. Receiver Output Load

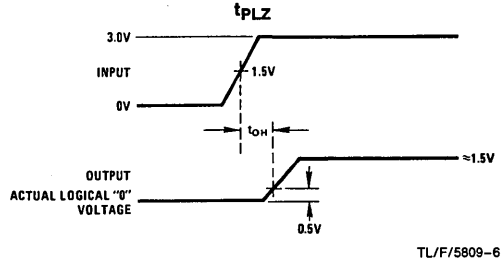
Switching Time Waveforms



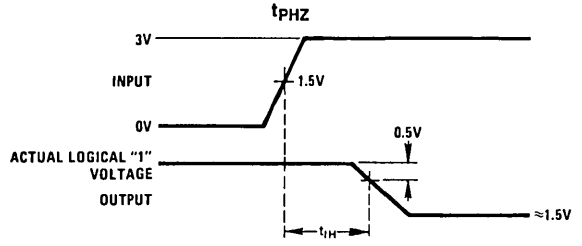
f = 1 MHz

$t_r = t_f \leq 10$ ns (10% to 90%)

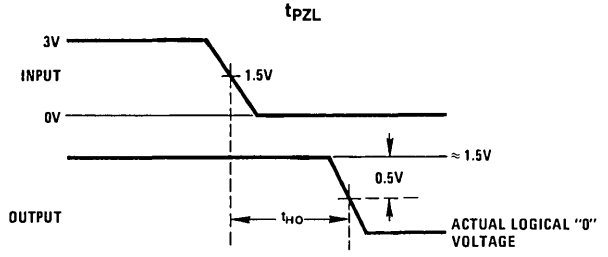
Duty Cycle = 50%



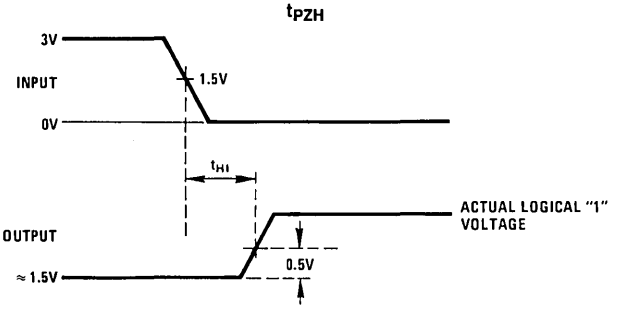
Switching Time Waveforms (Continued)



TL/F/5809–7



TL/F/5809–8



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Truth Table

Disable Input	Driver Input (IN_X)	Receiver Input/ Bus Output (BUS_X)	Receiver Output (OUT_X)	Mode of Operation
DS7834/DS8834				
1	X		$\overline{BUS}$	Receive Bus Signal
0	1	0	1	Drive Bus
0	0	1	0	Drive Bus
DS7839/DS8839				
1	X		BUS	Receive Bus Signal
0	1	1	1	Drive Bus
0	0	0	0	Drive Bus

X = Don't care

National Semiconductor Corporation

DS7836/DS8836 Quad NOR Unified Bus Receiver

General Description

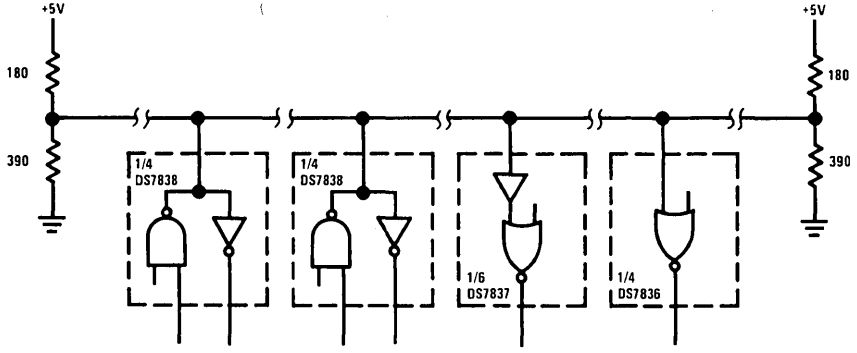
The DS7836/DS8836 are quad 2-input receivers designed for use in bus organized data transmission systems interconnected by terminated 120Ω impedance lines. The external termination is intended to be 180Ω resistor from the bus to the +5V logic supply together with a 390Ω resistor from the bus to ground. The design employs a built-in input hysteresis providing substantial noise immunity. Low input current allows up to 27 driver/receiver pairs to utilize a common bus. Performance is optimized for systems with bus rise and fall times ≤ 1.0 μs/V.

Features

- Low input current with normal V_{CC} or V_{CC} = 0V (15 μA typ)
- Built-in input hysteresis (1V typ)
- High noise immunity (2V typ)
- Temperature-insensitive input thresholds track bus logic levels
- TTL compatible output
- Matched, optimized noise immunity for "1" and "0" levels
- High speed (18 ns typ)

Typical Application

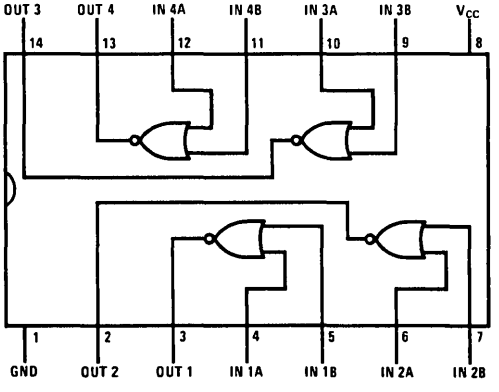
120Ω Unified Data Bus



TL/F/5810–1

Connection Diagram

Dual-In-Line Package



TL/F/5810–2

Top View

Order Number DS7836J, DS8836J or DS8836N
See NS Package Number J14A or N14A

Absolute Maximum Ratings

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7.0V
Current Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1308 mW
Molded Package	1207 mW
Lead Temperature (Soldering, 4 seconds)	260 °C

*Derate cavity package 8.7 mW/°C above 25°C; derate molded package 9.7 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
DS7836	4.5	5.5	V
DS8836	4.75	5.25	V
Temperature (T_A)			
DS7836	−55	+125	°C
DS8836	0	+70	°C

Electrical Characteristics

The following apply for $V_{MIN} \le V_{CC} \le V_{MAX}$, $T_{MIN} \le T_A \le T_{MAX}$, unless otherwise specified (Notes 2 and 3)

Symbol	Parameter	Conditions			Min	Typ	Max	Units
V_{TH}	High Level Input Threshold	V_{CC} = Max		DS7836	1.65	2.25	2.65	V
				DS8836	1.80	2.25	2.50	V
V_{IL}	Low Level Input Threshold	V_{CC} = Min		DS7836	0.97	1.30	1.63	V
				DS8836	1.05	1.30	1.55	V
I_{IN}	Maximum Input Current	V_{IN} = 4	V_{CC} = Max			15	50	μA
			V_{CC} = 0V			1	50	μA
V_{OH}	Logical "1" Output Voltage	V_{IN} = 0.5V, I_{OUT} = −400 μA			2.4			V
V_{OL}	Logical "0" Output Voltage	V_{IN} = 4V, I_{OUT} = 16 mA				0.25	0.4	V
I_{SC}	Output Short Circuit Current	V_{IN} = 0.5V, V_{OUT} = 0V, V_{CC} = Max, (Note 4)			−18		−55	mA
I_{CC}	Power Supply Current	V_{IN} = 4V, (Per Package)				25	40	mA
V_{CL}	Input Clamp Diode Voltage	I_{IN} = −12 mA, T_A = 25°C				−1	−1.5	V

Switching Characteristics V_{CC} = 5V, T_A = 25°C unless otherwise specified

Symbol	Parameter	Conditions		Min	Typ	Max	Units
t_{pd}	Propagation Delays	(Notes 4 and 5)	Input to Logical "1" Output		20	30	ns
			Input to Logical "0" Ouptut		18	30	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS7836 and across the 0°C to +70°C range for the DS8836. All typical values are for T_A = 25°C and V_{CC} = 5V.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Fan-out of 10 load, C_{LOAD} = 15 pF total, measured from V_{IN} = 1.3V to V_{OUT} = 1.5V, V_{IN} = 0V to 3V pulse.

Note 5: Fan-out of 10 load, C_{LOAD} = 15 pF total, measured from V_{IN} = 2.3V to V_{OUT} = 1.5V, V_{IN} = 0V to 3V pulse.

National Semiconductor Corporation

DS7837/DS8837 Hex Unified Bus Receiver

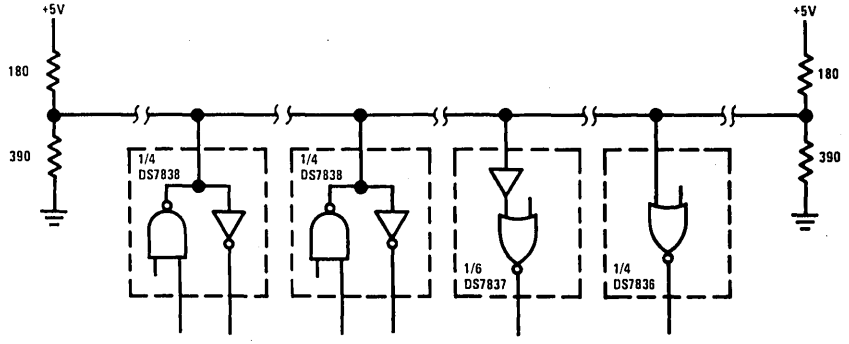
General Description

The DS7837/DS8837 are high speed receivers designed for use in bus organized data transmission systems interconnected by terminated 120Ω impedance lines. The external termination is intended to be 180Ω resistor from the bus to the +5V logic supply together with a 390Ω resistor from the bus to ground. The receiver design employs a built-in input hysteresis providing substantial noise immunity. Low input current allows up to 27 driver/receiver pairs to utilize a common bus. Disable inputs provide time discrimination. Disable inputs and receiver outputs are TTL compatible. Performance is optimized for systems with bus rise and fall times ≤1.0 μs/V.

Features

- Low receiver input current for normal V_{CC} or V_{CC} = 0V (15 μA typ)
- Six separate receivers per package
- Built-in receiver input hysteresis (1V typ)
- High receiver noise immunity (2V typ)
- Temperature insensitive receiver input thresholds track bus logic levels
- TTL compatible disable and output
- Molded or cavity dual-in-line or flat package
- High speed

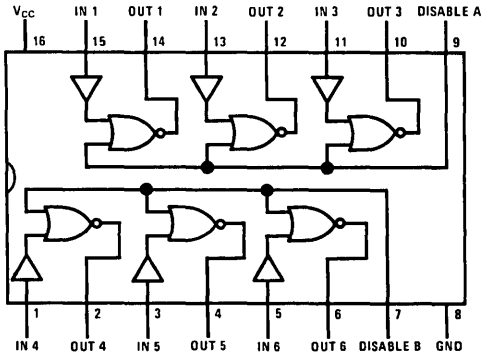
Typical Application



TL/F/5811–1

Connection Diagram

Dual-In-Line Package



TL/F/5811–2

Top View

Order Number DS7837J, DS8837J, DS8837M or DS8837N
See NS Package Number J16A, M16A or N16A

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5.5V
Operating Temperature Range	
DS7837	−55°C to +125°C
DS8837	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1433 mW
Molded DIP Package	1362 mW
SO Package	1002 mW
Lead Temperature (Soldering, 4 seconds)	260°C

*Derate cavity package 9.6 mW/°C above 25°C; derate molded DIP package 10.9 mW/°C above 25°C; derate SO package 8.01 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage, (V_{CC})			
DS7837	4.5	5.5	V
DS8837	4.75	5.25	V
Temperature (T_A)			
DS7837	−55	+125	°C
DS8837	0	+70	°C

Electrical Characteristics

The following apply for $V_{MIN} \le V_{CC} \le V_{MAX}$, $T_{MIN} \le T_A \le T_{MAX}$, unless otherwise specified (Notes 2 and 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{TH}	High Level Receiver Threshold	V_{CC} = Max	DS7837	1.65	2.25	2.65	V
			DS8837	1.80	2.25	2.50	V
V_{TL}	Low Level Receiver Threshold	V_{CC} = Min	DS7837	0.97	1.30	1.63	V
			DS8837	1.05	1.30	1.55	V
I_{IH}	Maximum Receiver Input Current	V_{IN} = 4V	$V_{CC} = V_{MAX}$		15.0	50.0	μA
			V_{CC} = 0V		1.0	50.0	μA
I_{IL}	Logical "0" Receiver Input Current	V_{IN} = 0.4V, $V_{CC} = V_{MAX}$			1.0	50.0	μA
V_{IH}	Logical "1" Input Voltage		Disable	2.0			V
V_{IL}	Logical "0" Input Voltage		Disable			0.8	V
I_{IH}	Logical "1" Input Current	Disable Input	V_{IND} = 2.4V			80.0	μA
			V_{IND} = 5.5V			2.0	mA
I_{IL}	Logical "0" Input Current	V_{IN} = 4V, V_{IND} = 0.4V, Disable Input				−3.2	mA
V_{OH}	Logical "1" Output Voltage	V_{IN} = 0.5V, V_{IND} = 0.8V, I_{OH} = −400 μA		2.4			V
V_{OL}	Logical "0" Output Voltage	V_{IN} = 4V, V_{IND} = 0.8V, I_{OH} = 16 mA			0.25	0.4	V
I_{OS}	Output Short Circuit Current	V_{IN} = 0.5V, V_{IND} = 0V, V_{OS} = 0V, $V_{CC} = V_{MAX}$, (Note 4)		−18.0		−55.0	mA
I_{CC}	Power Supply Current	V_{IN} = 4V, V_{IND} = 0V, (Per Package)			45.0	60.0	mA
V_{CL}	Input Clamp Diode	V_{IN} = −12 mA, V_{IND} = −12 mA, T_A = 25°C			−1.0	−1.5	V

Switching Characteristics T_A = 25°C, nominal power supplies unless otherwise noted

Symbol	Parameter	Conditions		Min	Typ	Max	Units
t_{pd}	Propagation Delays	V_{IND} = 0V, Receiver	Input to Logical "1" Output, (Note 5)		20	30	ns
			Input to Logical "0" Output, (Note 6)		18	30	ns
		Input = 0V, Disable, (Note 7)	Input to Logical "1" Output		9	15	ns
			Input to Logical "0" Output		4	10	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS7837 and across the 0°C to +70°C range for the DS8837. All typical values are for T_A = 25°C and V_{CC} = 5V.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Only one output at a time should be shorted.

Note 5: Fan-out of 10 load, C_{LOAD} = 15 pF total. Measured from V_{IN} = 1.3V to V_{OUT} = 1.5V, V_{IN} = 0V to 3V pulse.

Note 6: Fan-out of 10 load, C_{LOAD} = 15 pF total. Measured from V_{IN} = 2.3V to V_{OUT} = 1.5V, V_{IN} = 0V to 3V pulse.

Note 7: Fan-out of 10 load, C_{LOAD} = 15 pF total. Measured from V_{IN} = 1.5V to V_{OUT} = 1.5V, V_{IN} = 0V to 3V pulse.

National Semiconductor Corporation

DS7838/DS8838 Quad Unified Bus Transceiver

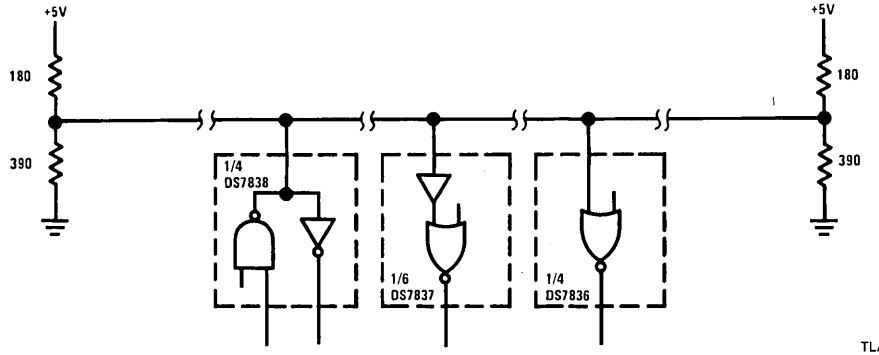
General Description

The DS7838/DS8838 are quad high speed drivers/receivers designed for use in bus organized data transmission systems interconnected by terminated 120Ω impedance lines. The external termination is intended to be 180Ω resistor from the bus to the +5V logic supply together with a 390Ω resistor from the bus to ground. The bus can be terminated at one or both ends. Low bus pin current allows up to 27 driver/receiver pairs to utilize a common bus. The bus loading is unchanged when V_{CC} = 0V. The receivers incorporate hysteresis to greatly enhance bus noise immunity. One two-input NOR gate is included to disable all drivers in a package simultaneously. Receiver performance is optimized for systems with bus rise and fall times ≤ 1.0 μs/V.

Features

- 4 totally separate driver/receiver pairs per package
- 1V typical receiver input hysteresis
- Receiver hysteresis independent of receiver output load
- Guaranteed minimum bus noise immunity of 1.3V, 2V typ.
- Temperature-insensitive receiver thresholds track bus logic levels
- 20 μA typical bus terminal current with normal V_{CC} or with V_{CC} = 0V
- Open collector driver output allows wire-OR connection
- High speed
- Series 74 TTL compatible driver and disable inputs and receiver outputs

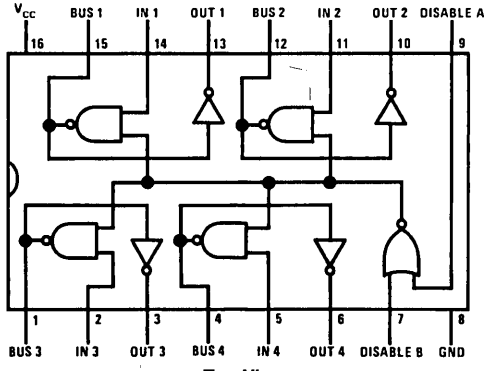
Typical Application



TL/F/5812-1

Connection Diagram

Dual-In-Line Package



TL/F/5812-2

Top View

Order Number DS7838J, DS8838J, DS8838M or DS8838N
See NS Package Number J16A, M16A or N16A

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input and Output Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Lead Temperature, (Soldering, 4 sec.)	260°C

*Derate cavity package 9.6 mW/°C above 25°C; derate molded DIP package 10.9 mW/°C above 25°C; derate SO package 8.01 mW/°C above 25°C.

Maximum Power Dissipation* at 25°C	
Cavity Package	1433 mW
Molded DIP Package	1362 mW
SO Package	1002 mW
Operating Temperature Range	
DS7838	−55°C to +125°C
DS8838	0°C to +70°C

Electrical Characteristics

DS7838/DS8838: The following apply for $V_{MIN} \le V_{CC} \le V_{MAX}$, $T_{MIN} \le T_A \le T_{MAX}$, unless otherwise specified (Notes 2 and 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
DRIVER AND DISABLE INPUTS							
V_{IH}	Logical "1" Input Voltage			2.0			V
V_{IL}	Logical "0" Input Voltage					0.8	V
I_I	Logical "1" Input Current	$V_{IN} = 5.5V$				1	mA
I_{IH}	Logical "1" Input Current	$V_{IN} = 2.4V$				40	μA
I_{IL}	Logical "0" Input Current	$V_{IN} = 0.4V$				−1.6	mA
V_{CL}	Input Diode Clamp Voltage	$I_{DIS} = -12$ mA, $I_{IN} = -12$ mA, $I_{BUS} = -12$ mA, $T_A = 25°C$			−1	−1.5	V
DRIVER OUTPUT/RECEIVER INPUT							
V_{OLB}	Low Level Bus Voltage	$V_{DIS} = 0.8V$, $V_{IN} = 2V$, $I_{BUS} = 50$ mA			0.4	0.7	V
I_{IHB}	Maximum Bus Current	$V_{IN} = 0.8V$, $V_{BUS} = 4V$, $V_{CC} = V_{MAX}$			20	100	μA
I_{ILB}	Maximum Bus Current	$V_{IN} = 0.8V$, $V_{BUS} = 4V$, $V_{CC} = 0V$			2	100	μA
V_{IH}	High Level Receiver Threshold	$V_{IND} = 0.8V$, $I_{OL} = 16$ mA, V_{CC} = Max	DS7838	1.65	2.25	2.65	V
			DS8838	1.80	2.25	2.50	V
V_{IL}	Low Level Receiver Threshold	$V_{IND} = 0.8V$, $V_{OH} = -400$ μA, V_{CC} = Min	DS7838	0.97	1.30	1.63	V
			DS8838	1.05	1.30	1.55	V
RECEIVER OUTPUT							
V_{OH}	Logical "1" Output Voltage	$V_{IN} = 0.8V$, $V_{BUS} = 0.5V$, $I_{OH} = -400$ μA		2.4			V
V_{OL}	Logical "0" Output Voltage	$V_{IN} = 0.8V$, $V_{BUS} = 4V$, $I_{OL} = 16$ mA			0.25	0.4	V
I_{OS}	Output Short Circuit Current	$V_{DIS} = 0.8V$, $V_{IN} = 0.8V$, $V_{BUS} = 0.5V$, $V_{OS} = 0V$, $V_{CC} = V_{MAX}$, (Note 4)		−18		−55	mA
I_{CC}	Supply Current	$V_{DIS} = 0V$, $V_{IN} = 2V$, (Per Package)			50	70	mA

Electrical Characteristics

DS7838/DS8838: The following apply for $V_{MIN} \leq V_{CC} \leq V_{MAX}$, $T_{MIN} \leq T_A \leq T_{MAX}$, unless otherwise specified (Notes 2 and 3) (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
RECEIVER OUTPUT (Continued)						
t_{pd}	Propagation Delays (Note 8)					
	Disable to Bus "1"	(Note 5)		19	30	ns
	Disable to Bus "0"	(Note 5)		15	23	ns
	Driver Input to Bus "1"	(Note 5)		17	25	ns
	Driver Input to Bus "0"	(Note 5)		9	15	ns
	Bus to Logical "1" Receiver Output	(Note 6)		20	30	ns
	Bus to Logical "0" Receiver Output	(Note 7)		18	30	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS7838 and across the 0°C to +70°C range for the DS8838. All typical values are for $T_A = 25°C$ and $V_{CC} = 5V$.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Only one output at a time should be shorted.

Note 5: 91Ω from bus pin to V_{CC} and 200Ω from bus pin to ground, $C_{LOAD} = 15$ pF total. Measured from $V_{IN} = 1.5V$ to $V_{BUS} = 1.5V$, $V_{IN} = 0V$ to 3.0V pulse.

Note 6: Fan-out of 10 load, $C_{LOAD} = 15$ pF total. Measured from $V_{IN} = 1.3V$ to $V_{OUT} = 1.5V$, $V_{IN} = 0V$ to 3.0V pulse.

Note 7: Fan-out of 10 load, $C_{LOAD} = 15$ pF total. Measured from $V_{IN} = 2.3V$ to $V_{OUT} = 1.5V$, $V_{IN} = 0V$ to 3.0V pulse.

Note 8: These apply for $V_{CC} = 5V$, $T_A = 25°C$ unless otherwise speicified.

National Semiconductor Corporation

DS8T26A/DS8T26AM/DS8T28/DS8T28M 4-Bit Bidirectional Bus Transceivers

General Description

The DS8T26A, DS8T28 consist of 4 pairs of TRI-STATE® logic elements configured as quad bus drivers/receivers along with separate buffered receiver enable and driver enable lines. This single IC quad transceiver design distinguishes the DS8T26A, DS8T28 from conventional multi-IC implementations. In addition, the DS8T26A, DS8T28's ultra high speed while driving heavy bus capacitance (300 pF) makes these devices particularly suitable for memory systems and bidirectional data buses.

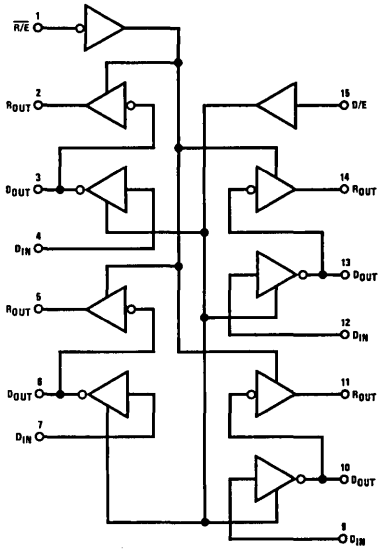
Both the driver and receiver gates have TRI-STATE outputs and low current PNP inputs. PNP inputs reduce input loading to 200 μA maximum.

Features

- Inverting outputs in the DS8T26A
- Non-inverting outputs in the DS8T28
- TRI-STATE outputs
- Low current PNP inputs
- Fast switching times (20 ns)
- Advanced Schottky processing
- Driver glitch free power up/down
- Non-overlapping TRI-STATE

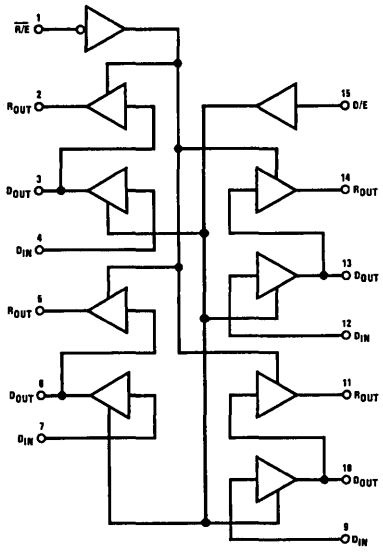
Logic and Connection Diagrams

DS8T26A



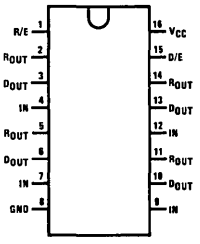
TL/F/5813–1

DS8T28



TL/F/5813–2

Dual-In-Line Package



TL/F/5813–3

Top View

Order Number DS8T26AJ, DS8T26AMJ, DS8T28J, DS8T28MJ, DS8T26AN or DS8T28N

See NS Package Number J16A or N16A

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

All Output and Supply Voltages	−0.5V to +7V
All Input Voltages	−1V to +5.5V
Output Currents	±150 mA
Storage Temperature	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1509 mW
Molded Package	1476 mW
Lead Temperature (Soldering, 4 seconds)	260°C

*Derate cavity package 10.1 mW/°C above 25°C; derate molded package 11.8 mW/°C above 25°C.

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
DS8T26A, DS8T28	4.75	5.25	V
DS8T26AM, DS8T28M	4.5	5.5	V
Temperature (T_A)			
DS8T26A, DS8T28	0	70	°C
DS8T26AM, DS8T28M	−55	+125	°C

Electrical Characteristics (Notes 2, 3 and 4)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRIVER						
I_{IL}	Low Level Input Current	V_{IN} = 0.4V			−200	μA
I_{IL}	Low Level Input Current (Disabled)	V_{IN} = 0.4V			−25	μA
I_{IH}	High Level Input Current (D_{IN}, D_E)	V_{IN} = V_{CC} Max			25	μA
V_{OL}	Low Level Output Voltage (Pins 3, 6, 10, 13)	I_{OUT} = 48 mA			0.5	V
V_{OH}	High Level Output Voltage, (Pins 3, 6, 10, 13)	I_{OUT} = −10 mA	2.4			V
I_{OS}	Short-Circuit Output Current, (Pins 3, 6, 10, 13)	V_{OUT} = 0V, V_{CC} = V_{CC} Max	−50		−150	mA
RECEIVER						
I_{IL}	Low Level Input Current	V_{IN} = 0.4V			−200	μA
I_{IH}	High Level Input Current (R_E)	V_{IN} = V_{CC} Max			25	μA
V_{OL}	Low Level Output Voltage	I_{OUT} = 20 mA			0.5	V
V_{OH}	High Level Output Voltage, (Pins 2, 5, 11, 14)	I_{OUT} = −100 μA	3.5			V
		I_{OUT} = − 2 mA	2.4			V
I_{OS}	Short-Circuit Output Current, (Pins 2, 5, 11, 14)	V_{OUT} = 0V, V_{CC} = V_{CC} Max	−30		−75	mA
BOTH DRIVER AND RECEIVER						
V_{TL}	Low Level Input Threshold Voltage	V_{CC} = Min, V_{IN} = 0.8V, I_{OL} = Max	0.85			V
V_{TH}	High Level Input Threshold Voltage	V_{CC} = Max, V_{IN} = 0.8V, I_{OH} = Max			2	V
I_{OZ}	Low Level Output OFF Leakage Current	V_{OUT} = 0.5V			−100	μA
I_{OZ}	High Level Output OFF Leakage Current	V_{OUT} = 2.4V			100	μA
V_I	Input Clamp Voltage	I_{IN} = −12 mA			−1.0	V
I_{CC}	Power Supply Current DS8T26A	V_{CC} = V_{CC} Max			87	mA
	DST28	V_{CC} = V_{CC} Max			110	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: Unless otherwise specified, min/max limits apply across the −55°C to +125°C temperature range for the DS8T26AM, DS8T28M and across the 0°C to +70°C range for the DS8T26A, DS8T28. All typicals are given for V_{CC} = 5V and T_A = 25°C.

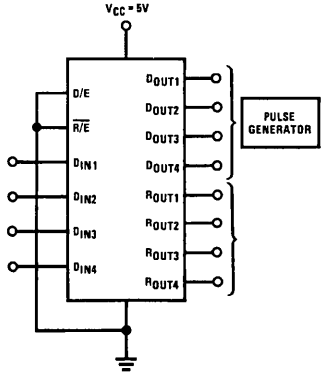
Note 3: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified.

Note 4: Only one output at a time should be shorted.

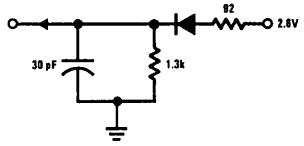
Switching Characteristics V_{CC} = 5V, T_A = 25°C

Symbol	Parameter	Conditions	DS8T26A Max	DS8T28 Max	Units
Propagation Delay					
t_{ON}	D_{OUT} to R_{OUT}, *(Figure 1)*	C_L = 30 pF	14	17	ns
t_{OFF}	D_{OUT} to R_{OUT}, *(Figure 1)*		14	17	ns
t_{ON}	D_{IN} to D_{OUT}, *(Figure 2)*	C_L = 300 pF	14	17	ns
t_{OFF}	D_{IN} to D_{OUT}, *(Figure 2)*		14	17	ns
Data Enable to Data Output					
t_{PZL}	High Z to O, *(Figure 3)*	C_L = 300 pF	25	28	ns
t_{PLZ}	O to High Z, *(Figure 3)*		20	23	ns
Receiver Enable to Receiver Output					
t_{PZL}	High Z to O, *(Figure 4)*	C_L = 30 pF	20	23	ns
t_{PLZ}	O to High Z, *(Figure 4)*		15	18	ns

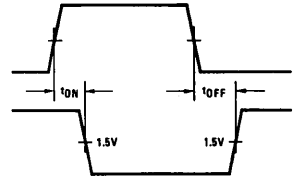
AC Test Circuits and Switching Time Waveforms



TL/F/5813-4



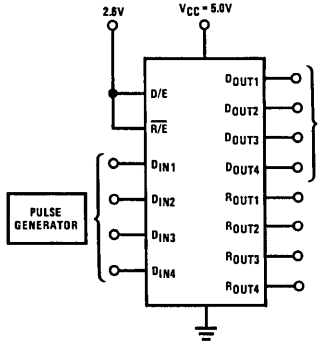
TL/F/5813-5



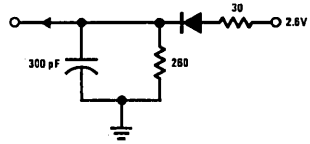
TL/F/5813-6

Input pulse:
$t_r = t_f$ = 5 ns (10% to 90%)
Freq = 10 MHz (50% duty cycle)
Amplitude = 2.6V

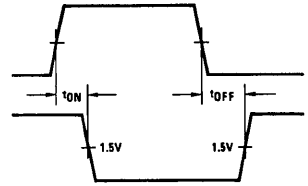
FIGURE 1. Propagation Delay (D_{OUT} to R_{OUT})



TL/F/5813-7



TL/F/5813-8

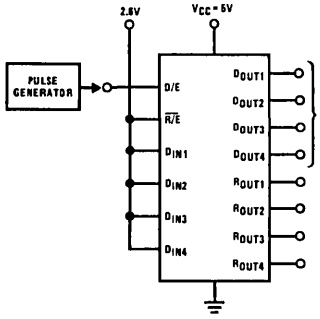


TL/F/5813-9

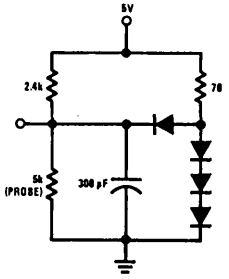
Input pulse:
$t_r = t_f$ = 5 ns (10% to 90%)
Freq = 10 MHz (50% duty cycle)
Amplitude = 2.6V

FIGURE 2. Propagation Delay (D_{IN} to D_{OUT})

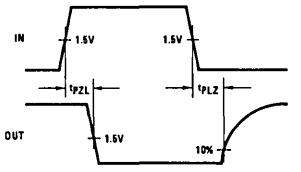
AC Test Circuits and Switching Time Waveforms (Continued)



TL/F/5813–10



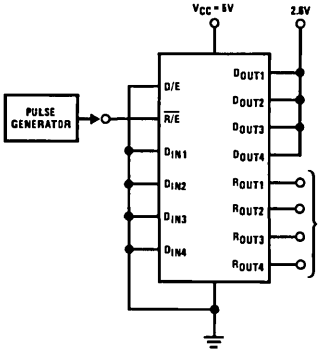
TL/F/5813–11



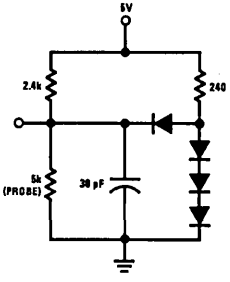
TL/F/5813–12

Input pulse:
$t_r = t_f = 5$ ns (10% to 90%)
Freq = 5 MHz (50% duty cycle)
Amplitude = 2.6V

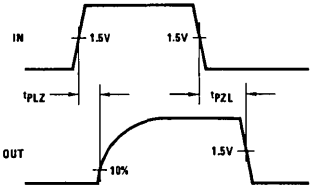
FIGURE 3. Propagation Delay (Data Enable to Data Output)



TL/F/5813–13



TL/F/5813–14



TL/F/5813–15

Input pulse:
$t_r = t_f = 5$ ns (10% to 90%)
Freq = 5 MHz (50% duty cycle)
Amplitude = 2.6V

FIGURE 4. Propagation Delay ($\overline{\text{Receive/Enable}}$ to Receive Output)

National Semiconductor Corporation

PRELIMINARY

DS8940/DS8941 9-Bit Bi-Directional Registers

General Description

The DS8940 and DS8941 are nine-bit TRI-STATE® bi-directional REGISTERS designed to provide a high performance bus interface capable of driving high capacitive loads. These devices eliminate the extra packages required to buffer existing registers while providing extra width for wider address, or for data in byte-plus-parity oriented systems.

The DS8940 offers separate positive edge triggered clocks while the DS8941 has separate gated positive edge triggered clocks.

Both devices have independent output control functions for maximum versatility. Inputs are compatible with TTL and CMOS.

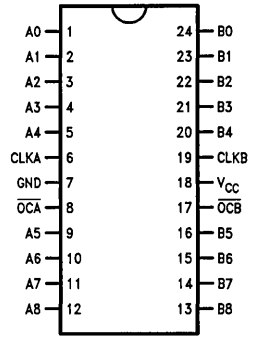
Power up/down circuitry is featured which will TRI-STATE the outputs and prevent erroneous glitches on the bus during system power up or power down operations.

Features

- Advanced oxide-isolated Schottky TTL process
- High speed parallel registers
- 48 mA/300 pF bus drive capability
- Glitch free power Up/Down
- PNP input design reduces input loading

Connection Diagrams

DS8940 Dual-In-Line Package

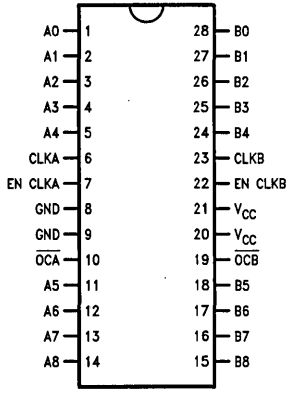


TL/F/8763-1

Top View

Order Number DS8940J or DS8940N
See NS Package Number J24A or N24A

DS8941 Dual-In-Line Package

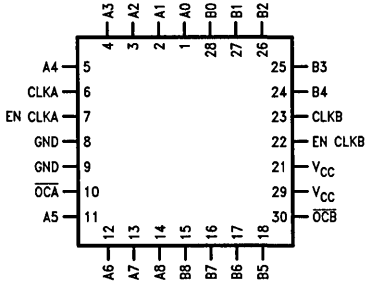


TL/F/8763-2

Top View

Order Number DS8941J or DS8941N
See NS Package Number J28A or N28B

DS8941 Plastic Chip Carrier



TL/F/8763-3

Top View

Order Number DS8941V
See NS Package Number V28A

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	
All Inputs	−0.5V to 7V
I/O Ports	−0.5V to 5.5V
Input Current	−18 mA to +0.1 mA
Output Sink Current	64 mA
Storage Temperature Range	−65°C to +165°C
Lead Temperature (Soldering, 4 seconds)	260°C
Maximum Power Dissipation* at 25°C	TBD

*Derate cavity package—mW/°C above 25°C; Derate molded package—mW/°C above 25°C; Reference Application Note AN-336.

Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
V_{CC}	Supply Voltage	4.5		5.5	V
V_{IH}	High-Level Input Voltage	2.0			V
V_{IL}	Low-Level Input Voltage			0.8	V
I_{OH}	High-Level Output Current			−15	mA
I_{OL}	Low-Level Output Current			48	mA
t_S	Data to CLK ↑, Set-Up	6			ns
t_H	Data to CLK ↑, Hold	0			ns
t_W	CLK Pulse Duration, HI	4			ns
	CLK Pulse Duration, LOW	6			ns
T_A	Temperature	0		70	°C

Electrical Characteristics (Notes 2, 3, and 4)

Symbol	Conditions		Min	Typ	Max	Units
I_{IL}	V_{CC} = Max, V_{IN} = 0.4V	Input & I/O			−250	μA
		CLK Inputs			−500	μA
I_{IH}	V_{CC} = Max, V_{IN} = 2.7V	Inputs			20	μA
		I/O Ports			50	μA
I_I	V_{CC} = Max, V_{IN} = 7.0V	Inputs			100	μA
	V_{CC} = Max, V_{IN} = 5.5V	I/O Ports			100	μA
V_{CL}	V_{CC} = Min, I_{IN} = −18 mA				−1.2	V
V_{OH}	V_{CC} = Min, I_{OH} = Max		2.5			V
V_{OL}	V_{CC} = Min, I_{OL} = Max				0.5	V
I_{OZH}	V_{CC} = Max, V_{OUT} = 2.7V				50	μA
I_{OZL}	V_{CC} = Max, V_{OUT} = 0.4V				−250	μA
I_O	V_{CC} = Max, V_{OUT} = 2.25V (Note 4)		−30		−150	mA
CIN Bus	V_{CC} = Max				20	pF
V_{CC} PU/D	(Note 5)			3		V
I_{CC}	V_{CC} = Max	Active A Port Only			180	mA
		Active B Port Only			180	mA
		A & B Port TRI-STATE			<180	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All currents into device pins are shown as positive values; all currents out of the device are shown as negative; all voltages are referenced to ground unless otherwise specified. All values shown as max or min are classified on absolute value basis.

Note 3: Unless otherwise specified, min/max limits apply across the supply and temperature range specified in the table of "Recommended Operating Conditions". All typical values are V_{CC} = 5V, T_A = 25°C.

Note 4: Only one output at a time should be shorted.

Note 5: V_{CC} PU/D is defined as the maximum value of V_{CC} at which the output remains at TRI-STATE during a Power Up operation from 0V; and the minimum value of V_{CC} at which the outputs go into TRI-STATE during a Power Down operation from the normal operating V_{CC} range.

Switching Characteristics Over Recommended Operating Free-Air Temperature Range

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
DS8940						
t_{pLH}	CLKA ↑ to A Ports	CL = 50 pF R1 = 500Ω S1 Open		6		ns
t_{pHL}				7		ns
t_{pLH}	CLKB ↑ to B Ports	CL = 300 pF R1 = 500Ω S1 Open		9		ns
t_{pHL}				11		ns
t_{pZH}	$\overline{OCA}$ to A Ports	CL = 50 pF R1 = 500Ω S1 Open		8		ns
t_{pHZ}				6		ns
t_{pZH}	$\overline{OCB}$ to B Ports	CL = 300 pF R1 = 500Ω S1 Open		12		ns
t_{pZL}	$\overline{OCA}$ to A Ports	CL = 50 pF R1 = R2 = 500Ω S1 Closed		9		ns
t_{pLZ}				8		ns
t_{pZL}	$\overline{OCB}$ to B Ports	CL = 300 pF R1 = R2 = 500Ω S1 Closed		13		ns
DS8941						
t_{pLH}	CLKA ↑ or EN CLKA ↑ to A Ports	CL = 50 pF R1 = 500Ω S1 Open		7		ns
t_{pHL}				8		ns
t_{pLH}	CLKB ↑ or EN CLKB ↑ to B Ports	CL = 300 pF R1 = 500Ω S1 Open		10		ns
t_{pHL}				12		ns
t_{pZH}	$\overline{OCA}$ to A Ports	CL = 50 pF R1 = 500Ω S1 Open		8		ns
t_{pHZ}				6		ns
t_{pZH}	$\overline{OCB}$ to B Ports	CL = 300 pF R1 = 500Ω S1 Open		12		ns
t_{pZL}	$\overline{OCA}$ to A Ports	CL = 50 pF R1 = R2 = 500Ω S1 Closed		9		ns
t_{pLZ}				8		ns
t_{pZL}	$\overline{OCB}$ to B Ports	CL = 300 pF R1 = R2 = 500Ω S1 Closed		13		ns

DS8940 Function Table

Control Inputs				A Ports		B Ports	
$\overline{OCA}$	$\overline{OCB}$	CLKA	CLKB	Mode	A0–A8	Mode	B0–B8
L	H	(Note 2)	↑	Output	1	Input	0
			↑		0		1
			H		Latched		X
			L		Latched		X
H	H	(Note 3)		Device Disabled State			
H	L	↑	(Note 2)	Input	1	Output	0
		↑			0		1
		H			X		Latched
		L			X		Latched

Note 1:
"L" Denotes logic LOW level
"H" Denotes logic HIGH level
"X" Denotes a DON'T CARE condition
"↑" Denotes a positive transition of the CLK input
Note 2: In this mode the clock may be used to latch the output data for "read back" verification.
Note 3: Data can be latched while the outputs are disabled; refer to Input Mode function.

DS8941 Function Table

Control Inputs						A Ports		B Ports	
$\overline{OCA}$	$\overline{OCB}$	CLKA	EN CLKA	CLKB	EN CLKB	Mode	A0–A8	Mode	B0–B8
L	H	(Note 2)	(Note 2)	↑	H	Output	1	Input	0
				↑	H		0		1
				H	H		Latched		X
				L	X		Latched		X
				H	↑		1		0
				H	↑		0		1
				X	L		Latched		X
H	H	(Note 3)				Device Disabled State			
H	L	↑	H	(Note 2)	(Note 2)	Input	1	Output	0
		↑	H				0		1
		H	H				X		Latched
		L	X				X		Latched
		H	↑				1		0
		H	↑				0		1
		X	L				X		Latched

Note 1:
"L" Denotes logic LOW level
"H" Denotes logic HIGH level
"X" Denotes a DON'T CARE condition
"↑" Denotes a positive transition of the CLK input
Note 2: In this mode the clock may be used to latch the output data for "read back" verification.
Note 3: Data can be latched while the outputs are disabled; refer to Input Mode function.

Section 3

Peripheral/Power Drivers

Section Contents

*Also available processed to various Military screening levels. Refer to Section 9.

Peripheral/Power Drivers

Peripheral/power drivers is a broad definition given to interface power devices. The devices generally have open-collector output transistors that can switch hundreds of milliamps at high voltage and are driven by standard logic gates. They serve many applications including relay drivers, printer hammer drivers, lamp drivers, bus drivers, core memory drivers, voltage level translators, stepper motor drivers and solenoid drivers.

Unlike standard logic devices, peripheral drivers have many varied load situations depending on the application. This requires the design engineer to interpret device specifications in greater detail. Designers at National Semiconductor have incorporated many technically advanced and useful features into their broad line of peripheral driver devices.

Some of these features include:

- Short circuit protection at individual outputs
- Glitch-free power up/down
- Fail-safe operation
- Inductive fly-back protection
- Negative transient protection
- High input impedance for CMOS/NMOS compatibility

For further information on National Semiconductor's broad line of peripheral drivers, refer to the selection guide to follow and application notes within this section.

PERIPHERAL/POWER DRIVERS

Device Number and Temperature Range		Drivers/ Package	Logic Function (Driver On)	Input Compatibility (Logic)	Output High Voltage (V)	Latch-Up Voltage (Note 3) (V)	Output Low Voltage (V)	Output Low Current (mA)	Propagation Delay Typ (ns)	On Power Supply Current (mA)	Page No.
0°C to +70°C	−55°C to +125°C										
DP8310	DP7310	8	(Note 5)	TTL	30		0.5	100	40	152	3-5
DP8311	DP7311	8	(Note 6)	TTL	30		0.5	100	40	125	3-5
DS3631	DS1631	2	AND	CMOS	56	40	1.4	300	150	8	3-12
DS3632	DS1632	2	NAND	CMOS	56	40	1.4	300	150	8	3-12
DS3633	DS1633	2	OR	CMOS	56	40	1.4	300	150	8	3-12
DS3634	DS1634	2	NOR	CMOS	56	40	1.4	300	150	8	3-12
DS3654		10	(Note 2)	(Note 2)	(Note 1)	45	1.6	250	1000	70	3-17
DS3656		4	NAND	TTL/LS	65	30	1.5	600		65	3-21
DS3658		4	NAND	TTL/LS	70	35	0.7	600	2430	65	3-23
DS3668		4	NAND	TTL/LS	70	(Note 7)	1.5	600	2000	80	3-26
DS3669		4	AND	TTL/LS	70	35	0.7	600		65	3-29
DS3680		4	(Note 4)	TTL/CMOS	−2.1	−60	−60	−50	10,000	4.4	3-32
DS3686		2	NAND	TTL/CMOS	(Note 1)	56	1.3	300	1000	28	3-35
DS3687	DS1687	2	NAND	TTL/CMOS	(Note 1)	−56	−1.3	300	1000	2.8	3-38
DS75450		2	AND	TTL	30	20	0.7	300	31	55	3-41
DS75451	DS55451	2	AND	TTL	30	20	0.7	300	31	55	3-41
DS75452	DS55452	2	NAND	TTL	30	20	0.7	300	31	55	3-41
DS75453	DS55453	2	OR	TTL	30	20	0.7	300	31	55	3-41
DS75454	DS55454	2	NOR	TTL	30	20	0.7	300	31	55	3-41
DS75461	DS55461	2	AND	TTL	35	30	0.7	300	33	55	3-57
DS75462	DS55462	2	NAND	TTL	35	30	0.7	300	33	55	3-57
DS75463	DS55463	2	OR	TTL	35	30	0.7	300	33	55	3-57
DS75464	DS55464	2	NOR	TTL	35	30	0.7	300	33	55	3-57
MM74C908, MM74C918		2	AND	CMOS	13.5	15	V_{CC} − 1.8	300	150	0.015	CMOS CMOS

Note 1: The DS3686, DS3687 and DS3654 contain an internal inductive fly-back clamp circuit connected from the output to ground. As an example, DS3686 driving a relay solenoid connected to 28V would clamp the output voltage fly-back transient at 56V caused by the solenoid's stored inductive current. This clamp protects the circuit output and quenches the fly-back.

Note 2: The DS3654 is a 10-bit shift register followed by 10 enabled drivers. The input circuit is equivalent to a 4k resistor to ground, and the logic input thresholds are 2.8V and 0.8V. The recommended power supply voltage is 7.5V to 9.5V. The circuit can be cascaded to be a 20 or 30-bit shift register.

Note 3: Latch-up voltage is the maximum voltage the output can sustain when switching an inductive load.

Note 4: DS3680 has a differential input circuit.

Note 5: DS8310 inverting, positive edge latching.

Note 6: DS8311 inverting, fall through latch.

Note 7: DS3668 35V, latch-up with output fault protection.

National Semiconductor Corporation

DP7310/DP8310/DP7311/DP8311 Octal Latched Peripheral Drivers

General Description

The DP7310/8310, DP7311/8311 Octal Latched Peripheral Drivers provide the function of latching eight bits of data with open collector outputs, each driving up to 100 mA DC with an operating voltage range of 30V. Both devices are designed for low input currents, high input/output voltages, and feature a power up clear (outputs off) function.

The DP7310/8310 are positive edge latching. Two active low write/enable inputs are available for convenient data bussing without external gating.

The DP7311/8311 are positive edge latches. The active low strobe input latches data or allows fall through operation when held at logic "0". The latches are cleared (outputs off) with a logic "0" on the clear pin.

Features

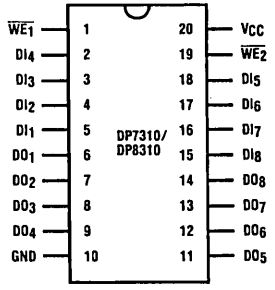
- High current, high voltage open collector outputs
- Low current, high voltage inputs
- All outputs simultaneously sink rated current "DC" with no thermal derating at maximum rated temperature
- Parallel latching or buffering
- Separate active low enables for easy data bussing
- Internal "glitch free" power up clear
- 10% V_{CC} tolerance

Applications

- High current high voltage drivers
- Relay drivers
- Lamp drivers
- LED drivers
- TRIAC drivers
- Solenoid drivers
- Stepper motor drivers
- Level translators
- Fiber-optic LED drivers

Connection Diagrams

Dual-In-Line Package



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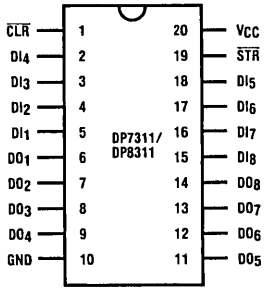
Top View

Dual-In-Line Package



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Top View

Order Number DP7310J, DP7311J, DP8310J, DP8311J, DP8310N or DP8311N
See NS Package Number J20A or N20A

3

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7.0V
Input Voltage	35V
Output Voltage	35V
Maximum Power Dissipation* at 25°C	
Cavity Package	1821 mW
DP8310/DP8311	2005 mW
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 4 sec.)	260°C

*Derate cavity package 12.1 mW/°C above 25°C; derate molded package 16.0 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	5.5	V
Temperature			
DP7310/DP7311	−55	+125	°C
DP8310/DP8311	0	+70	°C
Input Voltage		30	V
Output Voltage		30	V

DC Electrical Characteristics DP7310/DP8310, DP7311/DP8311 (Notes 2 and 3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	Logical "1" Input Voltage		2.0			V
V_{IL}	Logical "0" Input Voltage				0.8	V
V_{OL}	Logical "0" Output Voltage	Data outputs latched to logical "0", V_{CC} = min.				
	DP7310/DP7311	I_{OL} = 75 mA			0.4	V
	DP8310/DP8311	I_{OL} = 100 mA		0.35	0.5	V
I_{OH}	Logical "1" Output Current	Data outputs latched to logical "1", V_{CC} = min.				
	DP7310/DP7311	V_{OH} = 25V			500	μA
	DP8310/DP8311	V_{OH} = 30V		2.5	250	μA
I_{IH}	Logical "1" Input Current	V_{IH} = 2.7V, V_{CC} = max		0.1	25	μA
I_I	Input Current at Maximum Input Voltage	V_{IN} = 30V, V_{CC} = max		1	250	μA
I_{IL}	Logical "0" Input Current	V_{IN} = 0.4V, V_{CC} = max		−215	−300	μA
V_{clamp}	Input Clamp Voltage	I_{IN} = 12 mA		−0.8	−1.5	V
I_{CC0}	Supply Current, Outputs On	Data outputs latched to a logical "0". All Inputs are at logical "1", V_{CC} = max.				
	DP7310			100	125	mA
	DP8310			100	152	mA
	DP7311			88	117	mA
	DP8311			88	125	mA
I_{CC1}	Supply Current, Outputs Off	Data outputs latched to a logic "1". Other conditions same as I_{CC0}.				
	DP7310			40	47	mA
	DP8310			40	57	mA
	DP7311			25	34	mA
	DP8311			25	36	mA

AC Electrical Characteristics DP7310/DP8310: V_{CC} = 4.5V, T_A = −55°C to +125°C

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd0}	High to Low Propagation Delay Write Enable Input to Output	*(Figure 1)*		40	120	ns
t_{pd1}	Low to High Propagation Delay Write Enable Input to Output	*(Figure 1)*		70	150	ns
t_{SETUP}	Minimum Set-Up Time Data in to Write Enable Input	t_{HOLD} = 0 ns *(Figure 1)*	45	20		ns
t_{pWH}, t_{pWL}	Minimum Write Enable Pulse Width	*(Figure 1)*	60	25		ns
t_{THL}	High to Low Output Transition Time	*(Figure 1)*		16	35	ns
t_{TLH}	Low to High Output Transition Time	*(Figure 1)*		38	70	ns
C_{IN}	"N" Package (Note 4)			5	15	pF

AC Electrical Characteristics DP7311/DP8311: V_{CC} = 5V, T_A = 25°C

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd0}	High to Low Propagation Delay Data In to Output	*(Figure 2)*		30	60	ns
t_{pd1}	Low to High Propagation Delay Data to Output	*(Figure 2)*	70	100		ns
t_{SETUP}	Minimum Set-Up Time Data in to Strobe Input	t_{HOLD} = 0 ns *(Figure 2)*	0	−25		ns
t_{pWL}	Minimum Strobe Enable Pulse Width	*(Figure 2)*	60	35		ns
t_{pdC}	Propagation Delay Clear to Data Output	*(Figure 2)*		70	135	ns
t_{pWC}	Minimum Clear Input Pulse Width	*(Figure 2)*	60	25		ns
t_{THL}	High to Low Output Transition Time	*(Figure 2)*		20	35	ns
t_{TLH}	Low to High Output Transition Time	*(Figure 2)*		38	60	ns
C_{IN}	Input Capacitance—Any Input	(Note 4)		5	15	pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DP7310/DP7311 and across the 0°C to +70°C for the DP8310/DP8311. All typical values are for T_A = 25°C, V_{CC} = 5V.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted.

Note 4: Input capacitance is guaranteed by periodic testing. f_{TEST} = 10 kHz at 300 mV, T_A = 25°C.

Logic Table

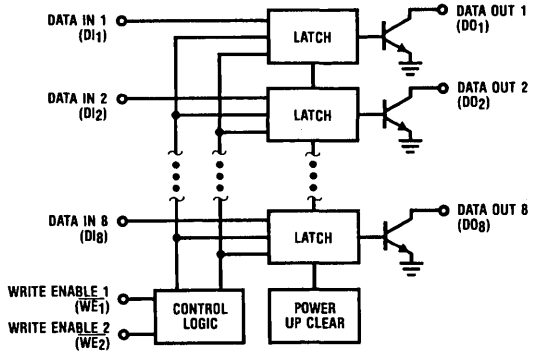
DP7310/DP8310			
Write Enable 1 $\overline{WE}_1$	Write Enable 2 $\overline{WE}_2$	Data Input DI_{1-8}	Data Output DO_{1-8}
0	0	X	Q
0	↓	0	1
0	↓	1	0
↓	0	0	1
↓	0	1	0
0	1	X	Q
1	0	X	Q
1	1	X	Q

DP7311/DP8311			
Clear $\overline{CLR}$	Strobe $\overline{STR}$	Data Input DI_{1-8}	Data Output DO_{1-8}
1	1	X	Q
1	0	0	1
1	0	1	0
0	X	X	1

X = Don't Care
1 = Outputs Off
0 = Outputs On
Q = Pre-existing Output
↓ = Positive Edge Transition

Block Diagrams

DP7310/DP8310



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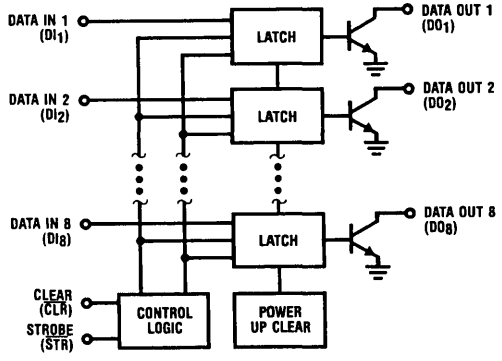
DP7311/DP8311



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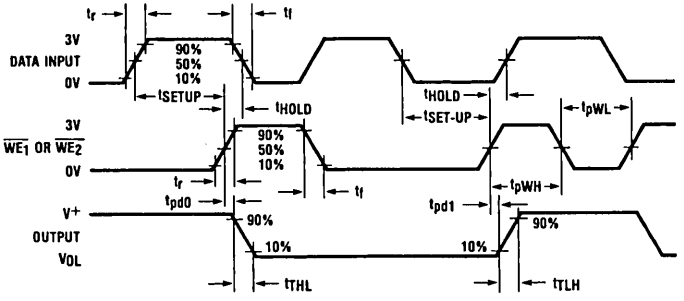
Switching Time Waveforms

DP7310/DP8310



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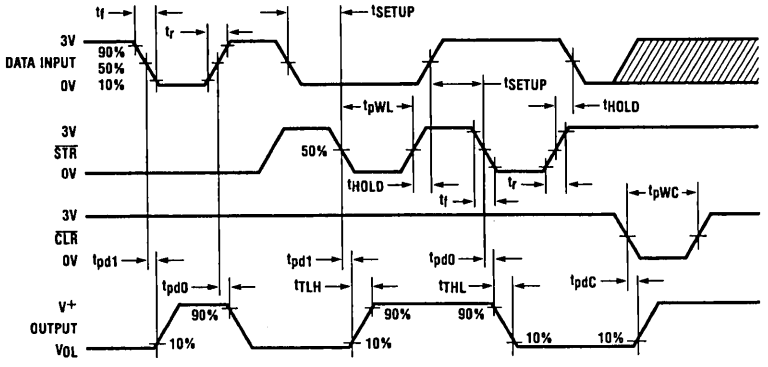
DP7311/DP8311



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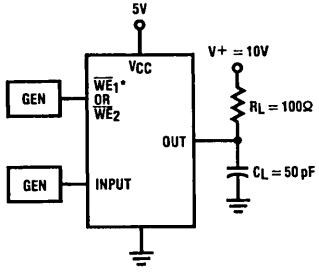
Switching Time Test Circuits



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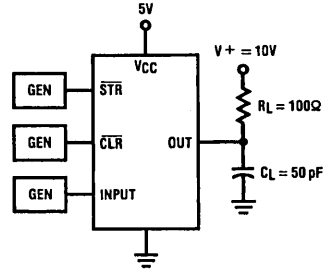
*$\overline{WE}_1$ = 0V When the Input = $\overline{WE}_2$

FIGURE 1. DP7310/DP8310



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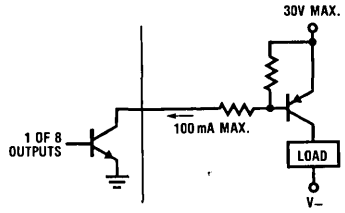
Pulse Generator Characteristics:
$Z_O = 50\Omega$, $t_r = t_f = 5$ ns

FIGURE 2. DP7311/DP8311

3

Typical Applications DP8310/11 Buffering High Current Device (Notes 1 and 2)

PNP High Current Driver



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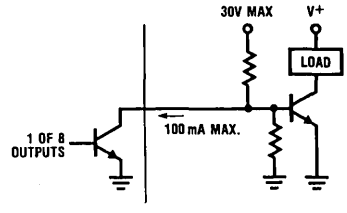
NPN High Current Driver



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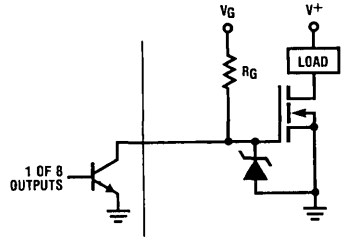
VMOS High Current Driver



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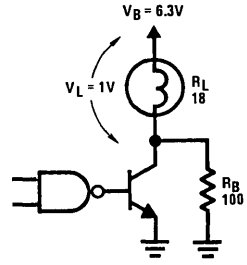
Circuit Used to Reduce Peak Transient Lamp Current



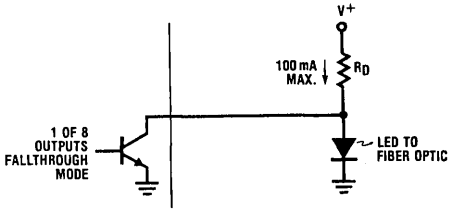
$$R_B = \left(\frac{V_B - V_L}{V_L}\right) R_L$$

$$R_B = \left(\frac{6.3 - 1}{1}\right) 18\Omega = 95.4 \approx 100\Omega$$

TL/F/5246–12

Eight Output/Four Output Fiber Optic LED Driver

DP8311 100 mA Drivers



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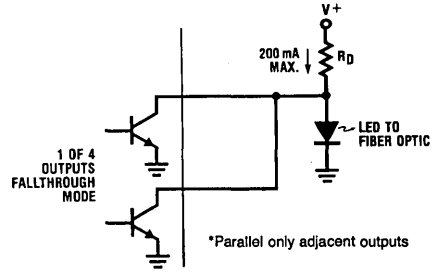
DP8311 Parallel Outputs (200 mA) Drivers*



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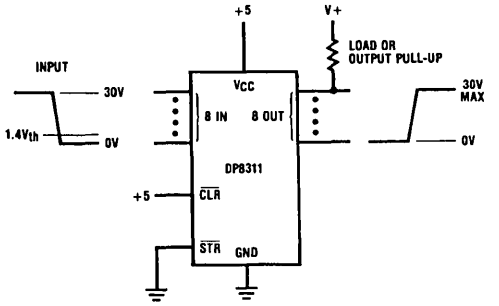
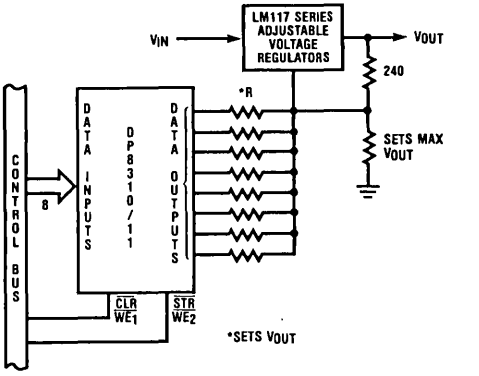
Typical Applications (Continued)

8-Bit Level Translator-Driver



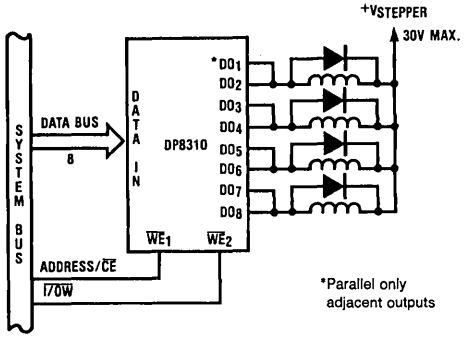
TL/F/5246–15

Digital Controlled 256 Level Power Supply from 1.2V to 30V



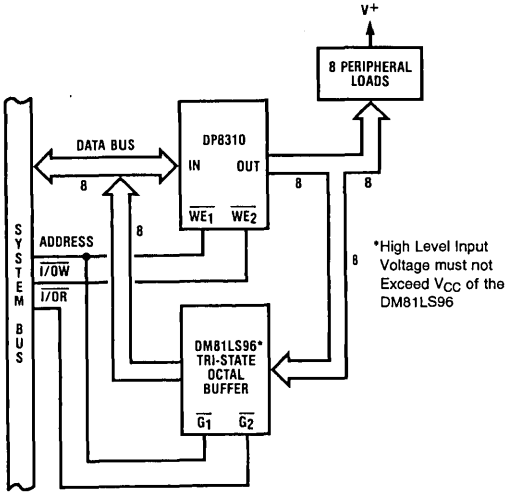
TL/F/5246–16

200 mA Drive for a 4 Phase Bifilar Stepper Motor



TL/F/5246–17

Reading the State of the Latched Peripherals



TL/F/5246–18

Note 1: Always use good V_{CC} bypass and ground techniques to suppress transients caused by peripheral loads.

Note 2: Printed circuit board mounting is required if these devices are operated at maximum rated temperature and current (all outputs on DC).

National Semiconductor Corporation

DS1631/DS3631/DS1632/DS3632/DS1633/DS3633/ DS1634/DS3634 CMOS Dual Peripheral Drivers

General Description

The DS1631 series of dual peripheral drivers was designed to be a universal set of interface components for CMOS circuits.

Each circuit has CMOS compatible inputs with thresholds that track as a function of V_{CC} (approximately ½ V_{CC}). The inputs are PNPs providing the high impedance necessary for interfacing with CMOS.

Outputs have high voltage capability, minimum breakdown voltage is 56V at 250 μA.

The outputs are Darlington connected transistors. This allows high current operation (300 mA max) at low internal V_{CC} current levels since base drive for the output transistor is obtained from the load in proportion to the required loading conditions. This is essential in order to minimize loading on the CMOS logic supply.

Typical V_{CC} = 5V power is 28 mW with both outputs ON. V_{CC} operating range is 4.5V to 15V.

The circuit also features output transistor protection if the V_{CC} supply is lost by forcing the output into the high impedance OFF state with the same breakdown levels as when V_{CC} was applied.

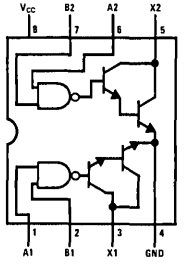
Pin-outs are the same as the respective logic functions found in the following popular series of circuits: DS75451, DS75461, DS3611. This feature allows direct conversion of present systems to the MM74C CMOS family and DS1631 series circuits with great power savings.

The DS1631 series is also TTL compatible at V_{CC} = 5V.

Features

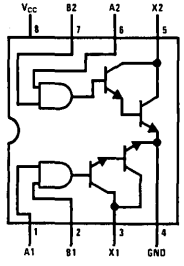
- CMOS compatible inputs
- TTL compatible inputs
- High impedance inputs — PNP's
- High output voltage breakdown — 56V min
- High output current capability — 300 mA max
- Same pin-outs and logic functions as DS75451, DS75461 and DS3611 series circuits
- Low V_{CC} power dissipation (28 mW both outputs "ON" at 5V)

Connection Diagrams (Dual-In-Line and Metal Can Packages)



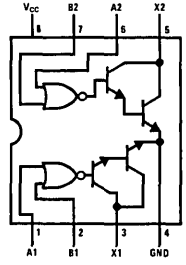
TL/F/5816–1

Top View
Order Number DS1631J-8, DS3631J-8 or DS3631N



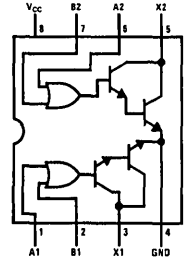
TL/F/5816–2

Top View
Order Number DS1632J-8, DS3632J-8 or DS3632N



TL/F/5816–3

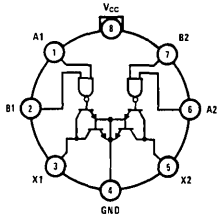
Top View
Order Number DS1633J-8, DS3633J-8 or DS3633N



TL/F/5816–4

Top View
Order Number DS1634J-8, DS3634J-8 or DS3634N

See NS Package Number J08A or N08E

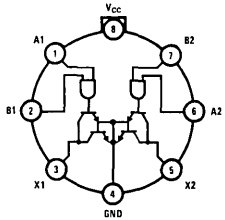


TL/F/5816–5

Top View

(Pin 4 is electrically connected to the case.)

Order Number DS1631H or DS3631H

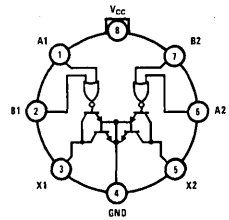


TL/F/5816–6

Top View

(Pin 4 is electrically connected to the case.)

Order Number DS1632H or DS3632H

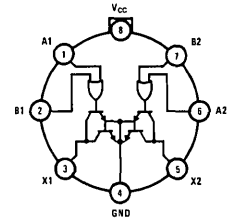


TL/F/5816–7

Top View

(Pin 4 is electrically connected to the case.)

Order Number DS1633H or DS3633H



TL/F/5816–8

Top View

(Pin 4 is electrically connected to the case.)

Order Number DS1634H or DS3634H

See NS Package Number H08C

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	16V
Voltage at Inputs	−0.3V to V_{CC} + 0.3V
Output Voltage	56V
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1133 mW
Molded Package	1022 mW
TO-5 Package	787 mW
Lead Temperature (Soldering, 4 sec.)	260°C

*Derate cavity package 7.6 mW/°C above 25°C; derate molded package 8.2 mW/°C above 25°C; derate TO-5 package 5.2 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage, V_{CC}			
DS1631/DS1632/ DS1633/DS1634	4.5	15	V
DS3631/DS3632/ DS3633/DS3634	4.75	15	V
Temperature, T_A			
DS1631/DS1632/ DS1633/DS1634	−55	+125	°C
DS3631/DS3632/ DS3633/DS3634	0	+70	°C

Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions			Min	Typ	Max	Units
ALL CIRCUITS								
V_{IH}	Logical "1" Input Voltage	(*Figure 1*)	V_{CC} = 5V		3.5	2.5		V
			V_{CC} = 10V		8.0	5		V
			V_{CC} = 15V		12.5	7.5		V
V_{IL}	Logical "0" Input Voltage	(*Figure 1*)	V_{CC} = 5V			2.5	1.5	V
			V_{CC} = 10V			5.5	2.0	V
			V_{CC} = 15V			7.5	2.5	V
I_{IH}	Logical "1" Input Current	V_{CC} = 15V, V_{IN} = 15V, (*Figure 2*)				0.1	10	μA
I_{IL}	Logical "0" Input Current	V_{IN} = 0.4V, (*Figure 3*)	V_{CC} = 5V			−50	−120	μA
			V_{CC} = 15V			−200	−360	μA
V_{OH}	Output Breakdown Voltage	V_{CC} = 15V, I_{OH} = 250 μA, (*Figure 1*)			56	65		V
V_{OL}	Output Low Voltage	V_{CC} = Min, (*Figure 1*), DS1631, DS1632, DS1633, DS1634	I_{OL} = 100 mA			0.85	1.1	V
			I_{OL} = 300 mA			1.1	1.4	V
		V_{CC} = Min, (*Figure 1*), DS3631, DS3632, DS3633, DS3634	I_{OL} = 100 mA			0.85	1.0	V
			I_{OL} = 300 mA			1.1	1.3	V
DS1631/DS3631								
$I_{CC(0)}$	Supply Currents	V_{IN} = 0V, (*Figure 4*)	V_{CC} = 5V	Output Low		7	11	mA
			V_{CC} = 15V	Both Drivers		14	20	mA
$I_{CC(1)}$		(*Figure 4*)	V_{CC} = 5V, V_{IN} = 5V	Output High		2	3	mA
			V_{CC} = 15V, V_{IN} = 15V	Both Drivers		7.5	10	mA
t_{PD1}	Propagation to "1"	V_{CC} = 5V, T_A = 25°C, C_L = 15 pF, R_L = 50Ω, V_L = 10V, (*Figure 5*)				200		ns
t_{PD0}	Propagation to "0"	V_{CC} = 5V, T_A = 25°C, C_L = 15 pF, R_L = 50Ω, V_L = 10V, (*Figure 5*)				150		ns
DS1632/DS3632								
$I_{CC(0)}$	Supply Currents	(*Figure 4*)	V_{CC} = 5V, V_{IN} = 5V	Output Low		8	12	mA
			V_{CC} = 15V, V_{IN} = 15V			18	23	mA
$I_{CC(1)}$		V_{IN} = 0V, (*Figure 4*)	V_{CC} = 5V	Output High		2.5	3.5	mA
			V_{CC} = 15V			9	14	mA
t_{PD1}	Propagation to "1"	V_{CC} = 5V, T_A = 25°C, C_L = 15 pF, R_L = 50Ω, V_L = 10V, (*Figure 5*)				500		ns
t_{PD0}	Propagation to "0"	V_{CC} = 5V, T_A = 25°C, C_L = 15 pF, R_L = 50Ω, V_L = 10V, (*Figure 5*)				750		ns

3

Electrical Characteristics (Notes 2 and 3) (Continued)

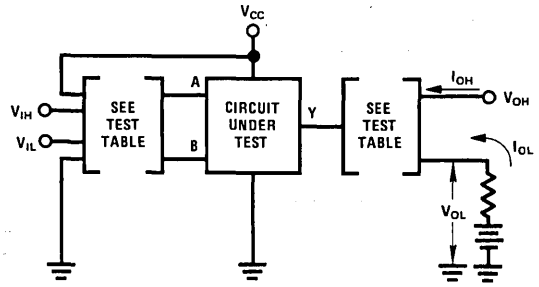
Symbol	Parameter	Conditions			Min	Typ	Max	Units
DS1633/DS3633								
$I_{CC(0)}$	Supply Currents	V_{IN} = 0V, (*Figure 4*)	V_{CC} = 5V	Output Low		7.5	12	mA
			V_{CC} = 15V			16	23	mA
$I_{CC(1)}$		(*Figure 4*)	V_{CC} = 5V, V_{IN} = 5V	Output High		2	4	mA
			V_{CC} = 15V, V_{IN} = 15V			7.2	15	mA
t_{PD1}	Propagation to "1"	V_{CC} = 5V, T_A = 25°C, C_L = 15 pF, R_L = 50Ω, V_L = 10V, (*Figure 5*)				500		ns
t_{PD0}	Propagation to "0"	V_{CC} = 5V, T_A = 25°C, C_L = 15 pF, R_L = 50Ω, V_L = 10V, (*Figure 5*)				750		ns
DS1634/DS3634								
$I_{CC(0)}$	Supply Currents	(*Figure 4*)	V_{CC} = 5V, V_{IN} = 5V	Output Low		7.5	12	mA
			V_{CC} = 15V, V_{IN} = 15V			18	23	mA
$I_{CC(1)}$		V_{IN} = 0V, (*Figure 4*)	V_{CC} = 5V	Output High		3	5	mA
			V_{CC} = 15V			11	18	mA
t_{PD1}	Propagation to "1"	V_{CC} = 5V, T_A = 25°C, C_L = 15 pF, R_L = 50Ω, V_L = 10V, (*Figure 5*)				500		ns
t_{PD0}	Propagation to "0"	V_{CC} = 5V, T_A = 25°C, C_L = 15 pF, R_L = 50Ω, V_L = 10V, (*Figure 5*)				750		ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS1631, DS1632, DS1633 and DS1634 and across the 0°C to +70°C range for the DS3631, DS3632, DS3633 and DS3634. All typical values are for T_A = 25°C.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Test Circuits



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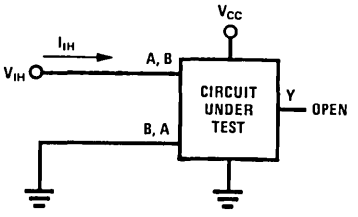
Circuit	Input Under Test	Other Input	Output	
			Apply	Measure
DS3631	V_{IH} V_{IL}	V_{IH} V_{CC}	I_{OH} I_{OL}	V_{OH} V_{OL}
DS3632	V_{IH} V_{IL}	V_{IH} V_{CC}	I_{OL} I_{OH}	V_{OL} V_{OH}
DS3633	V_{IH} V_{IL}	GND V_{IL}	I_{OH} I_{OL}	V_{OH} V_{OL}
DS3634	V_{IH} V_{IL}	GND V_{IL}	I_{OL} I_{OH}	V_{OL} V_{OH}

Note: Each input is tested separately.

FIGURE 1. V_{IH}, V_{IL}, V_{OH}, V_{OL}

Test Circuits (Continued)



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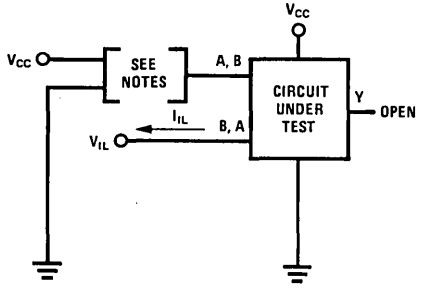
Each input is tested separately.

FIGURE 2. I_{IH}



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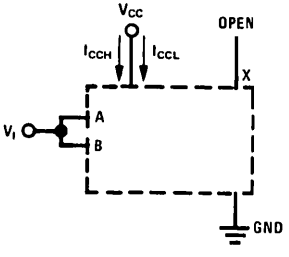
Note A: Each input is tested separately.

Note B: When testing DS1633 and DS1634 input not under test is grounded. For all other circuits it is at V_{CC}.

FIGURE 3. I_{IL}



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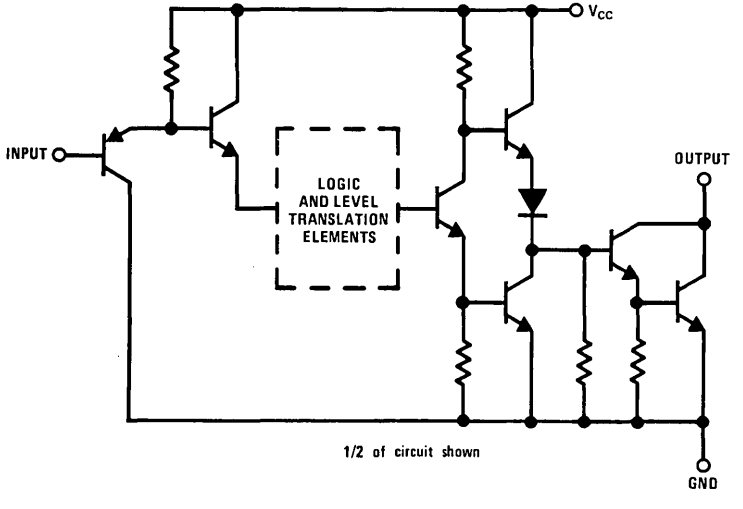
Both gates are tested simultaneously.

FIGURE 4. I_{CC} for AND and NAND Circuits

Schematic Diagram (Equivalent Circuit)



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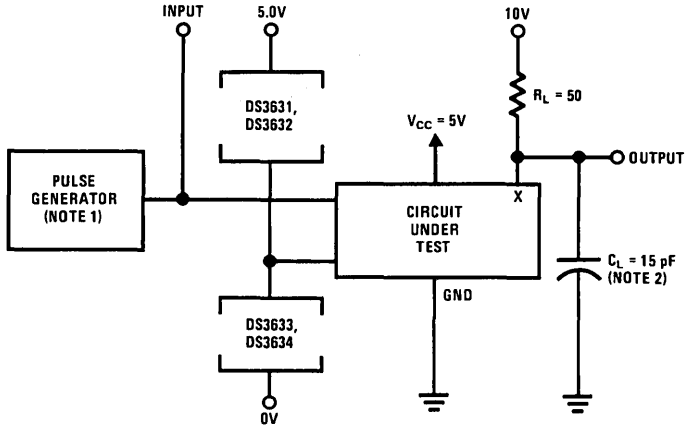
Switching Time Waveforms



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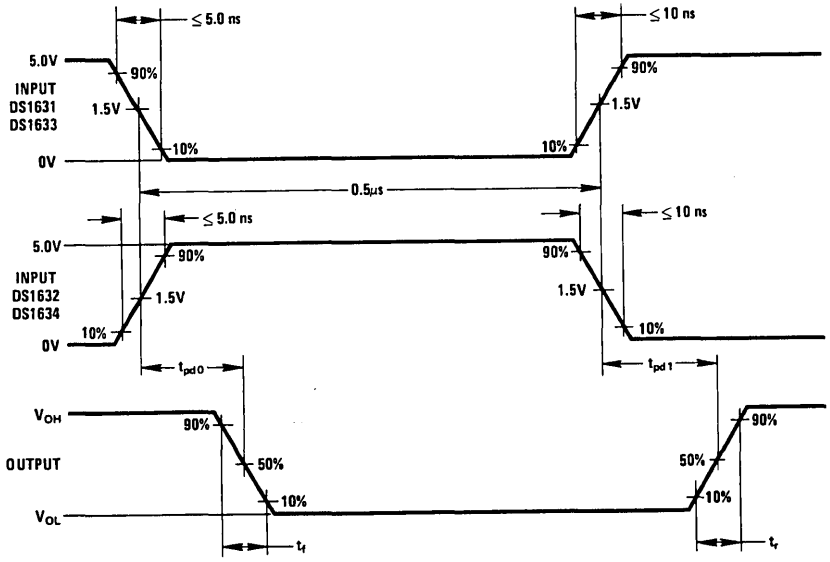

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Note 1: The pulse generator has the following characteristics: PRR = 500 kHz, $Z_{OUT} \approx 50\Omega$

Note 2: C_L includes probe and jig capacitance

FIGURE 5. Switching Times

National Semiconductor Corporation

DS3654 Printer Solenoid Driver

General Description

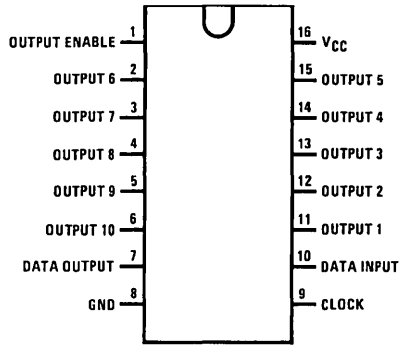
The DS3654 is a serial-to-parallel 10-bit shift register with a clock and data input, a data output from the tenth bit, and 10 open-collector clamped relay driver outputs suitable for driving printer solenoids.

Timing for the circuit is shown in *Figure 1*. Data input is sampled on the positive clock edge. Data output changes on the negative clock edge, and is always active. Enable transfers data from the shift register to the open-collector outputs. Internal circuitry inhibits output enable for power supply voltage less than 6V.

Each output sinks 250 mA and is internally clamped to ground at 50V to dissipate energy stored in inductive loads.

Connection Diagram

Dual-In-Line Package



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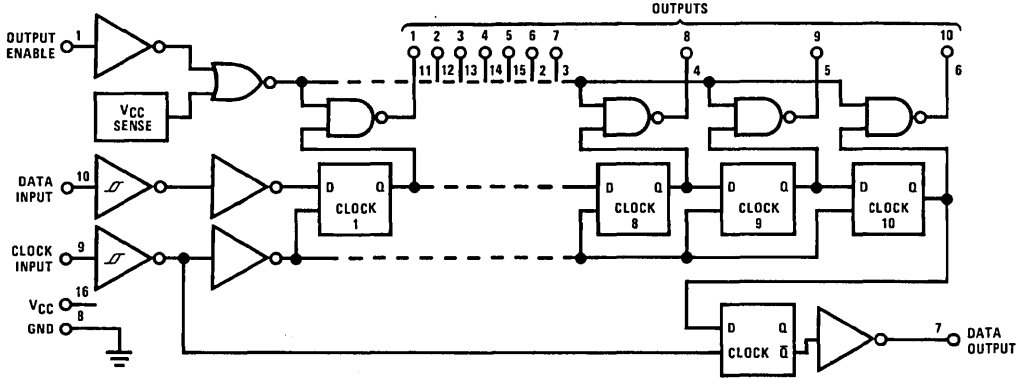
Top View

Order Number DS3654J or DS3654N
See NS Package Number J16A or N16A

Pin Descriptions

Pin No.	Function
1	Output Enable
2	Output 6
3	Output 7
4	Output 8
5	Output 9
6	Output 10
7	Data Output
8	Ground
9	Clock Input
10	Data Input
11	Output 1
12	Output 2
13	Output 3
14	Output 4
15	Output 5
16	V_{CC}

Logic Diagram



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Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage, V_{CC}	9.5V Max
Input Voltage	−0.5V Min. 9.5V Max
Output Supply, Vp-p	45V Max
Storage Temperature Range	−65°C to +150°C
Output Current (Single Output)	0.4A
Ground Current	4.0A
Peak Power Dissipation t < 10 ms, Duty Cycle < 5%	4.5W Max

Maximum Power Dissipation* at 25°C	
Cavity Package	1635 mW
Molded Package	1687 mW
Lead Temperature (Soldering, 4 seconds)	260°C

*Derate cavity package 10.9 mW/°C above 25°C; derate molded package 13.5 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	7.5	9.5	V
Temperature (T_A)	0	+70	°C
Output Supply (Vp-p)		40	V

Electrical Characteristics (Notes 2, 3 and 4) Vp-p = 30V unless otherwise noted

Parameter	Conditions	Min	Typ	Max	Units
Logical "1" Input Voltage		2.6			V
Logical "0" Input Voltage				0.8	V
Logical "1" Output Voltage Clamp	I_{CLAMP} = 0.1A, V_{EN} = 0V	45	50	65	V
Logical "1" Output Current	V_{OH} = 40V, V_{EN} = 0			1.0	mA
Logical "0" Output Current	I_{OL} = 250 mA, V_{EN} = 2.6V			1.6	V
Logical "1" Input Current					
Clock	T_A = 70°C, V_{CL} = 2.6V	0.2	0.33		mA
Enable	T_A = 70°C, V_{EN} = 2.6V	0.2	0.33		mA
Data	T_A = 70°C, V_D = 2.6V	0.3	0.57		mA
Clock	T_A = 0°C, V_{CL} = 2.6V		0.33	0.5	mA
Enable	T_A = 0°C, V_{EN} = 2.6V		0.33	0.5	mA
Data	T_A = 0°C, V_D = 2.6V		0.57	0.75	mA
Logical "0" Input Current					
Clock	T_A = 70°C, V_{CL} = 1V		125		μA
Enable	T_A = 70°C, V_{EN} = 1V		125		μA
Data	T_A = 70°C, V_D = 1V		220		μA
Input Pull-Down Resistance					
Clock	T_A = 25°C, V_{CL} < V_{CC}		8		kΩ
Enable	T_A = 25°C, V_{EN} < V_{CC}		8		kΩ
Data	T_A = 25°C, V_D < V_{CC}		4.5		kΩ
Supply Current (I_{CC})					
Outputs Disabled	$T_A \geq$ 25°C, V_{EN} = 0, V_{DO} = 0, V_{CC} = 9.5V		27	40	mA
Outputs Enabled	$T_A \geq$ 25°C, V_{EN} = 2.6, I_{OL} = 250 mA Each Bit		55	70	mA
Data Output Low (V_{DOL})	V_D = 0, I_{OL} = 0		0.01	0.5	V
Data Output High (V_{DOH})	V_D = 2.6, I_{OH} = −0.75 mA	2.6	3.4		V
Data Output Pull-Down Resistance	V_D = 0, V_{D0} = 1V		14		kΩ

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: Unless otherwise specified, min/max limits apply across the 0°C to +70°C temperature range and the 7.5V to 9.5V power supply range. All typical values given are for V_{CC} = 8.5V and T_A = 25°C.

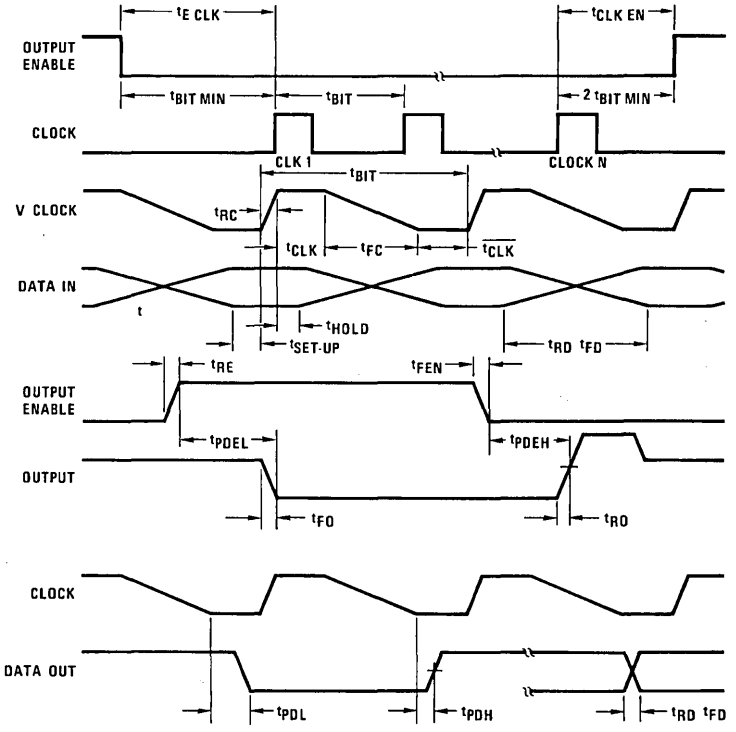
Note 3: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified.

Note 4: Only one output at a time should be shorted.

Switching Characteristics 0°C to +70°C, T_A = 25°C, nominal power supplies unless otherwise noted

Parameter	Conditions	Min	Typ	Max	Units
Clk, Data and Enable Inputs	*(Figure 1)*				
t_{FC}				2.0	μs
t_{RC}	$t_{BIT} \geq 10\ \mu s$			2.0	μs
$t_{\overline{CLK}}$		2			μs
t_{CLK}		3.5			μs
t_{HOLD}				1.0	μs
$t_{SET\text{-}UP}$				1.0	μs
t_{RE}, $t_{RD\ IN}$				1.0	μs
t_{FE}, $t_{FD\ IN}$				5.0	μs
Output 1–10	Vp-p = 20V				
t_{RO}	$R_L = 100\Omega$, $C_L < 100$ pF		1.2		μs
t_{FO}	$R_L = 100\Omega$, $C_L < 100$ pF		1.2		μs
t_{PDEH}			3.5		μs
t_{PDEL}			3.0		μs
Data Output					
t_{PDH}, t_{PDL}	$R_L = 5\ k\Omega$, $C_L \leq 10$ pF		0.8	2.5	μs
t_{RD}			0.4		μs
t_{FD}			0.4		μs
Clock to Enable Delay					
t_{CE}		$2\ t_{BIT}$			μs
Enable to Clock Delay		t_{BIT}			μs

Switching Time Waveforms



TL/F/5817–3

FIGURE 1. Shift Timing

Definition of Terms

V_{P-P}: Output power supply voltage. The return for open-collector relay driver outputs.

t_{BIT}: Period of the incoming clock.

V_{CLK}: The voltage at the clock input.

t_{CLK}: The portion of t_{BIT} when $V_{CLK} \geq 2.6V$

$\overline{t_{CLK}}$: The portion of t_{BIT} when $V_{CLK} \leq 0.8V$

t_{SET-UP}: The time prior to the end of $\overline{t_{CLK}}$ required to insure valid data at the shift register input for subsequent clock transitions.

t_{HOLD}: The time following the start of t_{CLK} required to transfer data within the shift register.

National Semiconductor Corporation

DS3656 Quad Peripheral Driver

General Description

The DS3656 is a quad peripheral driver designed for use in automotive applications. Logically it is an open collector NAND function with all inputs compatible with 74LS and CMOS series products. An enable input is provided that is common to each driver. When taken to a logic zero level all outputs will turn off. Also, overvoltage is detected.

The DS3656 has features associated with the output structure that make it highly versatile to many applications. Each output is capable of 600 mA sink currents and offers 65V standoff voltage in non-inductive applications. A clamp network capable of handling 800 mA is incorporated in each output which eliminates the need of an external network to quench the high voltage backswing caused when switching inductive loads up to 30V (reference AN-213).

The DS3656 is intended to operate from a 12V automotive battery. Internal to the device is its own voltage regulator which permits the device to operate during the wide voltage variation seen in many automotive applications. An overvoltage-protection circuit is incorporated that will cause the outputs to turn off when the supply exceeds 30V. The circuit is designed to withstand worst case fault conditions that occur in automotive applications, such as high voltage transients and reverse battery connection. In this type of environment an external 100Ω resistor must be connected in series with the V_{CC} line.

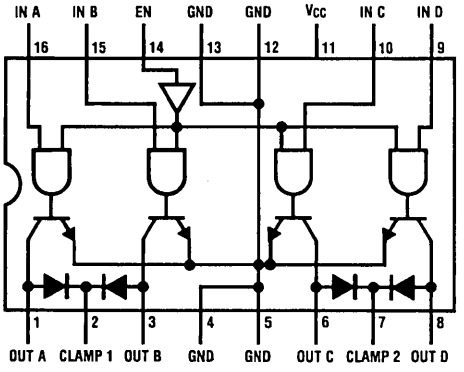
The molded package is specifically constructed to allow increased power dissipation over conventional packages. The four ground pins are directly connected to the device chip with a special copper lead frame. When the quad driver is soldered into a copper PC board the power rating of the device will significantly improve.

Features

- Quad automotive peripheral driver
- 600 mA output current capability
- High voltage outputs—65V
- Clamp diode provided for inductive loads
- Built in regulator
- Overvoltage failsafe
- TTL/LS/CMOS compatible diode clamped inputs
- High power dissipation package
- Guaranteed to withstand worst case fault conditions

Connection Diagram

Dual-In-Line Package



TL/F/5818–1

Top View

Order Number DS3656N
See NS Package Number N16A

Truth Table

Enable	In X	Out X
H	H	L
H	L	H
L	X	H

H = High level L = Low level X = Irrelevant

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage, V_{CC} (Note 2)	65V
Input Voltage	7V
Output Voltage	65V
Continuous Output Current	1.2A
Junction Temperature	150°C
Thermal Resistance (Junction to Ambient)	
DS3656N Plugged in a Socket	60°C/W
DS3656N Soldered in a PC Board	35°C/W
DS3656N Soldered in a PC Board with 6 in^2 Cn Foil	20°C/W
Lead Temperature (Soldering, 4 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage, V_{CC}	10.5	17.0	V
Temperature	−40	105	°C

Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions	Min	Max	Units
V_{CC}	Power Supply Voltage		10.5	17	V
I_{CC}	Power Supply Current			65	mA
V_{IH}	High Level Input Voltage		2.0		V
V_{IL}	Low Level Input Voltage			0.8	V
I_{IH}	High Level Input Current	V_{IN} = 2.7V		20	μA
I_{IL}	Low Level Input Current	V_{IN} = 0.4V		−360	μA
V_{ICL}	Input Clamp Voltage	I_{IN} = −10 mA		−1.5	V
V_{OL}	Low Level Output Voltage	I_L = 600 mA, V_{CC} = 10.5V		1.5	V
I_{OH}	High Level Leakage Current	V_{OH} = 65V		1.0	mA
V_F	Output Diode Forward Voltage	I_F = 800 mA		2.5	V
I_R	Output Diode Reverse Leakage	V_R = 65V		1.0	mA
B_{VCER}	V_{OH1} Switching Capacitive or Resistive Load			65	V
L_{VCEO}	V_{OH2} Switching Inductive Clamped Load			30	V

Switching Characteristics V_{CC} = 13.2V, T_A = 25°C

Symbol	Parameter	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	V_{CC} = 13.2V, R_L = 30Ω, C_L = 15 pF		10	μs
t_{PHL}	Propagation Delay Time High to Low Level Output	V_{CC} = 13.2V, R_L = 30Ω, C_L = 15 pF		10	μs
t_{TLH}	Transition Time Low to High Level Output	V_{CC} = 13.2V, R_L = 30Ω, C_L = 15 pF		500	ns
t_{THL}	Transition Time High to Low Level Output	V_{CC} = 13.2V, R_L = 30Ω, C_L = 15 pF		500	ns
t_{PLH}	Enable to Output	V_{CC} = 13.2V, R_L = 30Ω, C_L = 15 pF		10	μs
t_{PHL}	Enable to Output	V_{CC} = 13.2V, R_L = 30Ω, C_L = 15 pF		10	μs

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Voltage values are with respect to network ground terminal unless otherwise specified.

Note 3: Unless otherwise specified min/max limits apply across the −40°C to +105°C temperature range.

National Semiconductor Corporation

DS3658 Quad High Current Peripheral Driver

General Description

The DS3658 quad peripheral driver is designed for those applications where low operating power, high breakdown voltage, high output current and low output ON voltage are required. A unique input circuit combines TTL compatibility with high impedance. In fact, its extreme low input current allows it to be driven directly by a CMOS device.

The outputs are capable of sinking 600 mA each and offer a 70V breakdown. However, for inductive loads the output should be clamped to 35V or less to avoid latch-up during turn off (inductive fly back protection—refer AN-213). An on-chip clamp diode capable of handling 800 mA is provided at each output for this purpose. In addition, the DS3658 incorporates circuitry that guarantees glitch-free power up or down operation and a fail-safe feature which puts the output in a high impedance state when input is open.

The molded package is specifically constructed to allow increased power dissipation over conventional packages. The four ground pins are directly connected to the device chip with a special copper lead frame. When the quad driver is soldered into a PC board, the power rating of the device improves significantly.

Applications

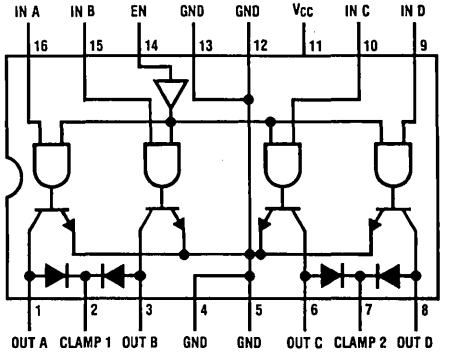
- Relay drivers
- Lamp drivers
- Solenoid drivers
- Hammer drivers
- Stepping motor drivers
- Triac drivers
- LED drivers
- High current, high voltage drivers
- Level translators
- Fiber optic LED drivers

Features

- Single saturated transistor outputs
- Low standby power, 10 mW typical
- High impedance TTL compatible inputs
- Outputs may be tied together for increased current capacity
- High output current
  - 600 mA per output
  - 2.4A per package
- No output latch-up at 35V
- Low output ON voltage (350 mV typ @ 600 mA)
- High breakdown voltage (70V)
- Open collector outputs
- Output clamp diodes for inductive fly back protection
- NPN inputs for minimal input currents (1 μA typical)
- Low operating power
- Standard 5V power supply
- Power up/down protection
- Fail safe operation
- 2W power package
- Pin-for-pin compatible with SN75437

Connection Diagram

Dual-In-Line Package



TL/F/5819–1

Top View

Order Number DS3658N
See NS Package Number N16A

Truth Table

IN	EN	OUT
H	H	L
L	H	Z
H	H	Z
L	L	Z

H = High state
L = Low state
Z = High impedance state

3

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	15V
Output Voltage	70V
Output Current	1.5A
Continuous Power Dissipation @ 25°C Free-Air (Note 5)	2075 mW
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 4 sec.)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage	4.75	5.25	V
Ambient Temperature	0	70	°C

Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	Input High Voltage		2.0			V
V_{IL}	Input Low Voltage				0.8	V
I_{IH}	Input High Current	V_{IN} = 5.25V, V_{CC} = 5.25V		1.0	10	μA
I_{IL}	Input Low Current	V_{IN} = 0.4V			±10	μA
V_{IK}	Input Clamp Voltage	I_I = −12 mA		−0.8	−1.5	V
V_{OL}	Output Low Voltage	I_L = 300 mA		0.2	0.4	V
		I_L = 600 mA (Note 4)		0.35	0.7	V
I_{CEX}	Output Leakage Current	V_{CE} = 70V, V_{IN} = 0.8V			100	μA
V_F	Diode Forward Voltage	I_F = 800 mA		1.0	1.6	V
I_R	Diode Leakage Current	V_R = 70V			100	μA
I_{CC}	Supply Current	All Inputs High		50	65	mA
		All Inputs Low		2	4	mA

Switching Characteristics (Note 2)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{HL}	Turn On Delay	R_L = 60Ω, V_L = 30V		226	500	ns
t_{LH}	Turn Off Delay	R_L = 60Ω, V_L = 30V		2430	8000	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

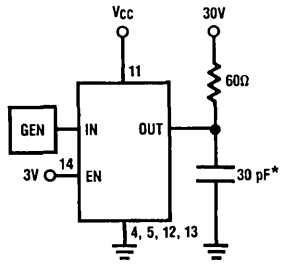
Note 2: Unless otherwise specified, min/max limits apply across the 0°C to +70°C temperature range and the 4.75V to 5.25V power supply range. All typical values are for T_A = 25°C and V_{CC} = 5.0V.

Note 3: All currents into device pins are shown as positive; all currents out of device pins are shown as negative; all voltages are referenced to ground, unless otherwise specified. All values shown as max or min are so classified on absolute value basis.

Note 4: All sections of this quad circuit may conduct rated current simultaneously; however, power dissipation averaged over a short interval of time must fall within specified continuous dissipation ratings.

Note 5: For operation over 25°C free-air temperature, derate linearly to 1328 mW @ 70°C @ the rate of 16.6 mW/°C.

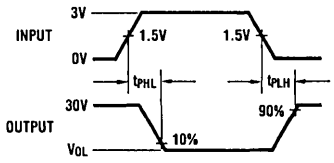
AC Test Circuit



TL/F/5819–2

*Includes probe and jig capacitance

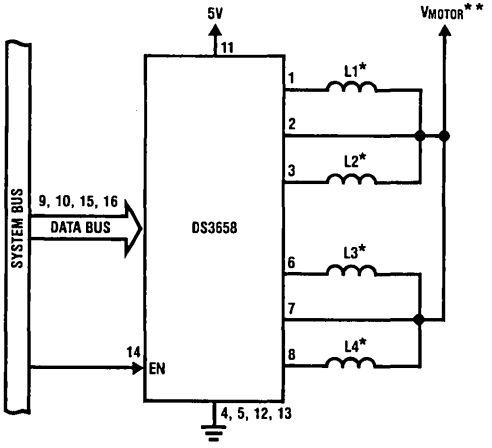
Switching Waveforms



TL/F/5819–3

Typical Applications

Stepping Motor Driver

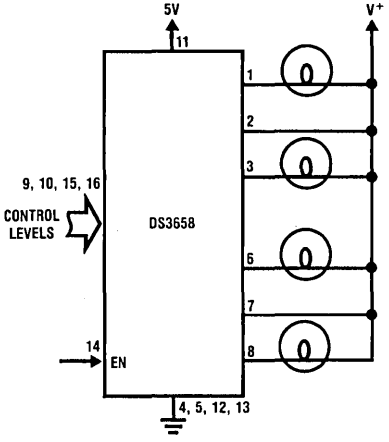


TL/F/5819–4

*L1, L2, L3, L4 are the windings of a bifilar stepping motor

**V_{MOTOR} is the supply voltage of the motor

Lamp Driver



TL/F/5819–5

National Semiconductor Corporation

DS3668 Quad Fault Protected Peripheral Driver

General Description

The DS3668 quad peripheral driver is designed for those applications where low operating power, high breakdown voltage, high output current and low output ON voltage are required. Unlike most peripheral drivers available, a unique fault protection circuit is incorporated on each output. When the load current exceeds 1.0A (approximately) on any output for more than a built-in delay time, nominally 12 μs, that output will be shut off by its protection circuitry with no effect on other outputs. This condition will prevail until that protection circuitry is reset by toggling the corresponding input or the enable pin low for at least 1.0 μs. This built-in delay is provided to ensure that the protection circuitry is not triggered by turn-on surge currents associated with certain kinds of loads.

The DS3668's inputs combine TTL compatibility with high input impedance. In fact, its extreme low input current allows it to be driven directly by a MOS device. The outputs are capable of sinking 600 mA each and offer a 70V breakdown. However, for inductive loads the output should be clamped to 35V or less to avoid latch up during turn off (inductive fly-back protection — refer AN-213). An on-chip clamp diode capable of handling 800 mA is provided at each output for this purpose. In addition, the DS3668 incorporates circuitry that guarantees glitch-free power up or down operation and a fail-safe feature which puts the output in a high impedance state when the input is open.

The molded package is specifically constructed to allow increased power dissipation over conventional packages. The four ground pins are directly connected to the device chip with a special copper lead frame. When the quad driver is soldered into a PC board, the power rating of the device improves significantly.

Applications

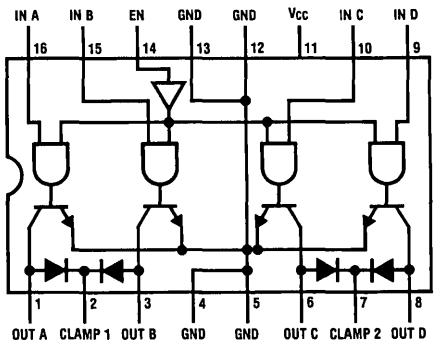
- Relay drivers
- Solenoid drivers
- Hammer drivers
- Stepping motor drivers
- Triac drivers
- LED drivers
- High current, high voltage drivers
- Level translators
- Fiber optic LED drivers

Features

- Output fault protection
- High impedance TTL compatible inputs
- High output current—600 mA per output
- No output latch-up at 35V
- Low output ON voltage (550 mV typ @ 600 mA)
- High breakdown voltage (70V)
- Open collector outputs
- Output clamp diodes for inductive fly-back protection
- NPN inputs for minimal input currents (1 μA typical)
- Low operating power
- Standard 5V power supply
- Power up/down protection
- Fail-safe operation
- 2W power package
- Pin-for-pin compatible with SN75437

Connection Diagram

Dual-In-Line Package



TL/F/5225–1

Top View

Truth Table

IN	EN	OUT
H	H	L
L	H	Z
H	L	Z
L	L	Z

H = High state
L = Low state
Z = High impedance state

Order Number DS3668N
See NS Package Number N16A

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7.0V
Input Voltage	15V
Output Voltage	70V
Continuous Power Dissipation @ 25°C Free-Air(5)	2075 mW
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 4 seconds)	260

Operating Conditions

	Min	Max	Units
Supply Voltage	4.75	5.25	V
Ambient Temperature	0	70	°C

Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	Input High Voltage		2.0			V
V_{IL}	Input Low Voltage				0.8	V
I_{IH}	Input High Current	V_{IN} = 5.25V, V_{CC} = 5.25V		1.0	20	μA
I_{IL}	Input Low Current	V_{IN} = 0.4V			±10	μA
V_{IK}	Input Clamp Voltage	I_I = −12 mA		−0.8	−1.5	V
V_{OL}	Output Low Voltage	I_L = 300 mA		0.2	0.7	V
		I_L = 600 mA (Note 4)		0.55	1.5	V
I_{CEX}	Output Leakage Current	V_{CE} = 70V, V_{IN} = 0.8V			100	μA
V_F	Diode Forward Voltage	I_F = 800 mA		1.2	1.6	V
I_R	Diode Leakage Current	V_R = 70V			100	μA
I_{CC}	Supply Current	All Inputs High		62	80	mA
		All Inputs Low		20		mA
I_{TH}	Protection Circuit Threshold Current			1	1.4	A

Switching Characteristics (Note 2)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{HL}	Turn On Delay	R_L = 60Ω, V_L = 30V		0.3	1.0	μs
t_{LH}	Turn Off Delay	R_L = 60Ω, V_L = 30V		2	10.0	μs
t_{FZ}	Protection Enable Delay (after Detection of Fault)		6	12		μs
t_{RL}	Input Low Time for Protection Circuit Reset		1.0			μs

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

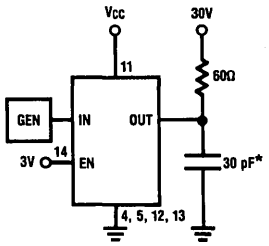
Note 2: Unless otherwise specified, min/max limits apply across the 0°C to +70°C temperature range and the 4.75V to 5.25V power supply range. All typical values are for T_A = 25°C and V_{CC} = 5.0V.

Note 3: All currents into device pins are shown as positive; all currents out of device pins are shown as negative; all voltages are referenced to ground, unless otherwise specified. All values shown as max or min are so classified on absolute value basis.

Note 4: All sections of this quad circuit may conduct rated current simultaneously; however, power dissipation averaged over a short interval of time must fall within specified continuous dissipation ratings.

Note 5: For operation over 25°C free-air temperature, derate linearly to 1328 mW @ 70°C @ the rate of 16.6 mW/°C.

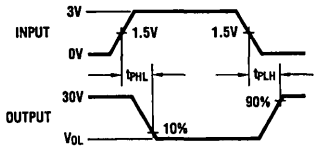
AC Test Circuit



TL/F/5225–2

*Includes probe and jig capacitance.

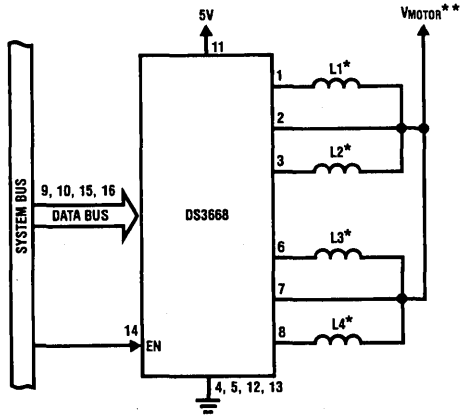
Switching Waveforms



TL/F/5225–3

Typical Application

Stepping Motor Driver

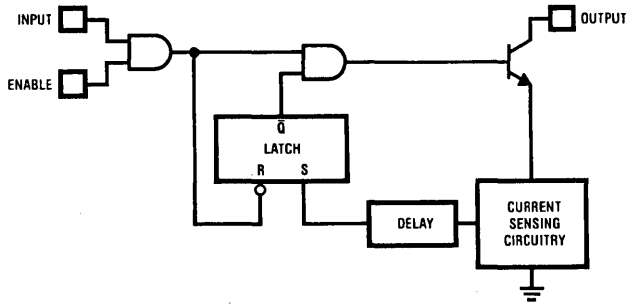


TL/F/5225–4

*L1, L2, L3, L4 are the windings of a bifilar stepping motor.

**V_{MOTOR} is the supply voltage of the motor.

Protection Circuit Block Diagram



TL/F/5225–5

National Semiconductor Corporation

DS3669 Quad High Current Peripheral Driver

General Description

The DS3669 is a non-inverting quad peripheral driver similar to the DS3658. These drivers are designed for those applications where low operating power, high breakdown voltage, high output current and low output ON voltage are required. A unique input circuit combines TTL compatibility with high impedance. In fact, its extreme low input current allows it to be driven directly by a CMOS device.

The outputs are capable of sinking 600 mA each and offer a 70V breakdown. However, for inductive loads the output should be clamped to 35V or less to avoid latch-up during turn off (inductive fly back protection—refer AN-213). An on-chip clamp diode capable of handling 800 mA is provided at each output for this purpose. In addition, the DS3669 incorporates circuitry that guarantees glitch-free power up or down operation.

The molded package is specifically constructed to allow increased power dissipation over conventional packages. The four ground pins are directly connected to the device chip with a special copper lead frame. When the quad driver is soldered into a PC board, the power rating of the device improves significantly.

Applications

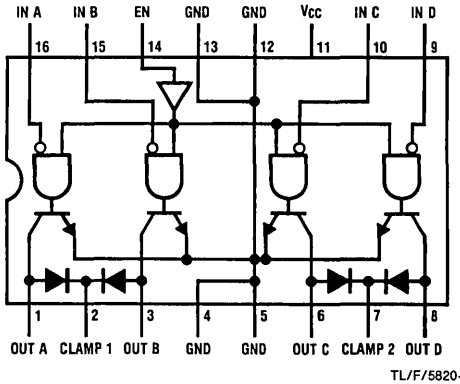
- Relay drivers
- Lamp drivers
- Solenoid drivers
- Hammer drivers
- Stepping motor drivers
- Triac drivers
- LED drivers
- High current, high voltage drivers
- Level translators
- Fiber optic LED drivers

Features

- Single saturated transistor outputs
- Low standby power, 10 mW typical
- High impedance TTL compatible inputs
- Outputs may be tied together for increased current capacity
- High output current
  - 600 mA per output
  - 2.4A per package
- No output latch-up at 35V
- Low output ON voltage (350 mV typ @600 mA)
- High breakdown voltage (70V)
- Open collector outputs
- Output clamp diodes for inductive fly back protection
- NPN inputs for minimal input currents (1 μA typical)
- Low operating power
- Standard 5V power supply
- Power up/down protection
- 2W power package

Connection Diagram

Dual-In-Line Package



TL/F/5820–1

Top View

Order Number DS3669N
See NS Package Number N16A

Truth Table

IN	EN	OUT
L	H	L
H	H	Z
L	L	Z
H	L	Z

H = High state
L = Low state
Z = High impedance state

3

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7.0V
Input Voltage	15V
Output Voltage	70V
Output Current	1.5A
Continuous Power Dissipation @25°C Free-Air (Note 5)	2075 mW
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 4 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage	4.75	5.25	V
Ambient Temperature	0	70	°C

Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	Input High Voltage		2.0			V
V_{IL}	Input Low Voltage				0.8	V
I_{IH}	Input High Current	V_{IN} = 5.25V, V_{CC} = 5.25V		1.0	10	μA
I_{IL}	Input Low Current	V_{IN} = 0.4V			±10	μA
V_{IK}	Input Clamp Voltage	I_I = −12 mA		−0.8	−1.5	V
V_{OL}	Output Low Voltage	I_L = 300 mA		0.2	0.4	V
		I_L = 600 mA (Note 4)		0.35	0.7	V
I_{CEX}	Output Leakage Current	V_C = 70V, V_{IN} = 2V, V_{EN} = 0.8V			100	μA
V_F	Diode Forward Voltage	I_F = 800 mA		1.0	1.6	V
I_R	Diode Leakage Current	V_R = 70V			100	μA
I_{CC}	Supply Current	All Inputs Low EN=2.0V		50	65	mA
		All Inputs High		2	4	mA

Switching Characteristics (Note 2)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{HL}	Turn On Delay	R_L = 60Ω, V_L = 30V		226	500	ns
t_{LH}	Turn Off Delay	R_L = 60Ω, V_L = 30V		2430	8000	ns

Note 1: "Absolute Maximium Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

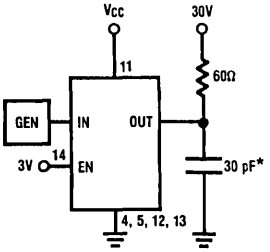
Note 2: Unless otherwise specified, min/max limits apply across the 0°C to +70°C temperature range and the 4.75V to 5.25V power supply range. All typical values are for T_A=25°C and V_{CC}=5.0V.

Note 3: All currents into device pins are shown as positive; all currents out of device pins are shown as negative; all voltages are referenced to ground, unless otherwise specified. All values shown as max or min are so classified on absolute value basis.

Note 4: All sections of this quad circuit may conduct rated current simultaneously; however, power dissipation averaged over a short interval of time must fall within specified continuous dissipation ratings.

Note 5: For operation over 25°C free-air temperature, derate linearly to 1328 mW @70°C @ the rate of 16.6 mW/°C.

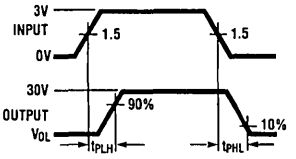
AC Test Circuit



TL/F/5820–2

*Includes probe and jig capacitance

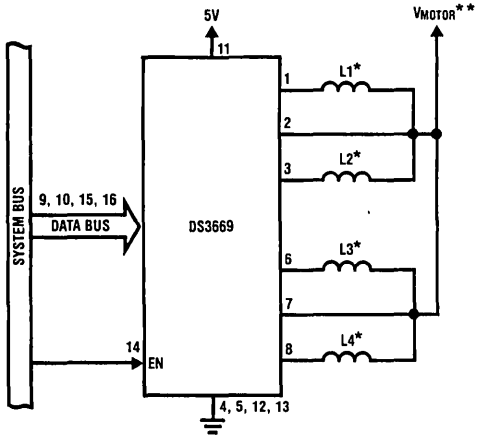
Switching Waveforms



TL/F/5820–3

Typical Applications

Stepping Motor Driver

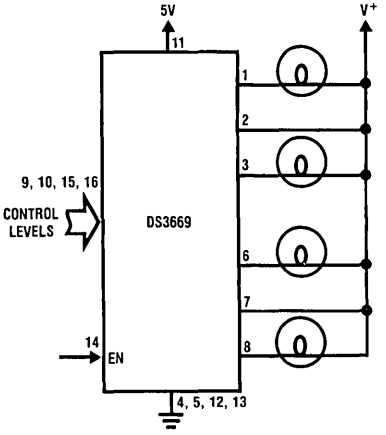


TL/F/5820–4

*L1, L2, L3, L4 are the windings of a bifilar stepping motor.

**V_{MOTOR} is the supply voltage of the motor.

Lamp Driver



TL/F/5820–5

National Semiconductor Corporation

DS3680 Quad Negative Voltage Relay Driver

General Description

The DS3680 is a quad high voltage negative relay driver designed to operate over wide ranges of supply voltage, common-mode voltage, and ambient temperature, with 50 mA sink capability. These drivers are intended for switching the ground end of loads which are directly connected to the negative supply, such as in telephone relay systems.

Since there may be considerable noise and IR drop between logic ground and negative supply ground in many applications, these drivers are designed to operate with a high common-mode range (±20V referenced to negative supply ground). Each driver has a common-mode range separate from the other drivers in the package, which pemits input signals from more than one element of the system.

With low differential input current requirements (typically 100 μA), these drivers are compatible with TTL, LS and CMOS logic. Differential inputs permit either inverting or non-inverting operation.

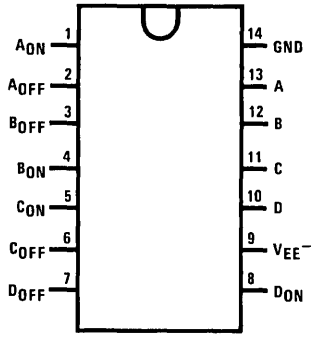
The driver outputs incorporate transient suppression clamp networks, which eliminate the need for external networks when used in applications of switching inductive loads. A fail-safe feature is incorporated to insure that, if the V_{ON} input or both inputs are open, the driver will be OFF.

Features

- −10V to −60V operation
- Quad 50 mA sink capability
- TTL/LS/COMS or voltage comparator input
- High input common-mode voltage range
- Very low input current
- Fail-safe disconnect feature
- Built-in output clamp diode

Connection Diagram

Dual-In-Line Package

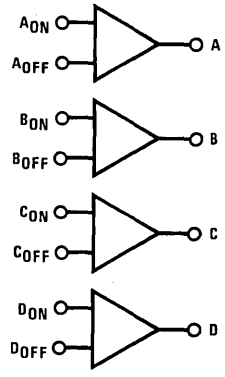


TL/F/5821–1

Top View

Order Number DS3680J, DS3680M or DS3680N
See NS Package Number J14A, M14A, N14A

Logic Diagram



TL/F/5821–2

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage (GND to $V_{EE}-$, and Any Pin)	−70V
Positive Input Voltage (Input to GND)	20V
Negative Input Voltage (Input to $V_{EE}-$)	−5V
Differential Voltage (V_{ON} to V_{OFF})	±20V
Inductive Load	$L_L \leq 5h$
	$I_L \leq 50$ mA
Output Current	−100 mA
Storage Temperature	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1433 mW
Molded Dip Package	1398 mW
SO Package	1002 mW
Lead Temperature (Soldering, 4 seconds)	260°C

* Derate cavity package 9.6 mW/°C above 25°C; derate molded dip package 11.2 mW/°C above 25°C; derate SO package 8.02 mW/°C above 25°C.

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage (GND to $V_{EE}-$)	−10	−60	V
Input Voltage (Input to GND)	−20	20	V
Logic ON Voltage (V_{ON}) Referenced to V_{OFF}	2	20	V
Logic OFF Voltage (V_{ON}) Referenced to V_{OFF}	−20	0.8	V
Temperature Range	−25	+85	°C

Electrical Characteristics (Notes 2 and 3)

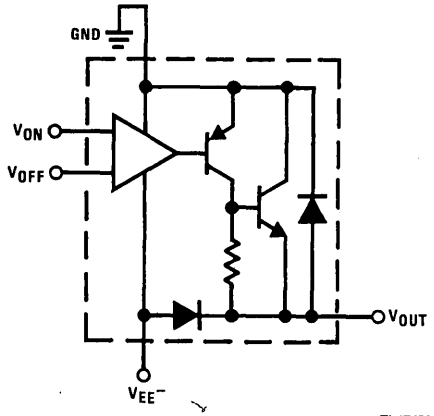
Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	Logic "1" Input Voltage		2.0	1.3		V
V_{IL}	Logic "0" Input Voltage			1.3	0.8	V
I_{INH}	Logic "1" Input Current	V_{IN} = 2V V_{IN} = 7V		40 375	100 1000	μA μA
I_{INL}	Logic "0" Input Current	V_{IN} = 0.4V V_{IN} = −7V		−0.01 −1	−5 −100	μA μA
V_{OL}	Output ON Voltage	I_{OL} = 50 mA		−1.6	−2.1	V
I_{OFF}	Output Leakage	$V_{OUT} = V_{EE}-$		−2	−100	μA
I_{FS}	Fail-Safe Output Leakage	$V_{OUT} = V_{EE}-$ (Inputs Open)		−2	−100	μA
I_{LC}	Output Clamp Leakage Current	V_{OUT} = GND		2	100	μA
V_C	Output Clamp Voltage	I_{CLAMP} = −50 mA Referenced to $V_{EE}-$		−2	−1.2	V
V_P	Positive Output Clamp Voltage	I_{CLAMP} = 50 mA Referenced to GND		0.9	1.2	V
$I_{EE(ON)}$	ON Supply Current	All Drivers ON		−2	−4.4	mA
$I_{EE(OFF)}$	OFF Supply Current	All Drivers OFF		−1	−100	μA
$t_{PD(ON)}$	Propagation Delay to Driver ON	L = 1h, R_L = 1k, V_{IN} = 3V Pulse		1	10	μs
$t_{PD(OFF)}$	Propagation Delay to Driver OFF	L = 1h, R_L = 1k, V_{IN} = 3V Pulse		1	10	μs

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range", they are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

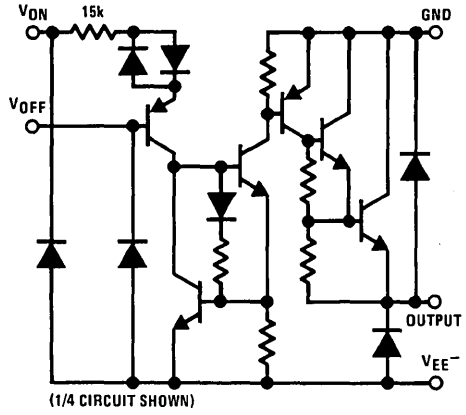
Note 2: Unless otherwise specified, the min/max limits of the table of "Electrical Characteristics" apply within the range of the table of "Operating Conditions". All typical values are given for $V_{EE}-$ = 52V, and T_A = 25°C.

Note 3: All current into device pins shown as positive, out of the device as negative. All voltages are referenced to ground unless otherwise noted.

Schematic Diagrams



TL/F/5821–3



TL/F/5821–4

National Semiconductor Corporation

DS3686 Dual Positive Voltage Relay Driver

General Description

The DS3686 is a high voltage/current positive voltage relay driver having many features not available in present relay drivers.

PNP inputs provide both TTL/LS compatibility and high input impedance for low input loading.

Output leakage is specified over temperature at an output voltage of 54V. Minimum output breakdown (ac/latch breakdown) is specified over temperature at 5 mA. This clearly defines the actual breakdown of the device since the circuit has incorporated in it an internal reference which does not allow output breakdown latching found in existing relay drivers. Additionally, this internal reference circuit feature will eliminate the need in most cases of an external clamping (inductive transient voltage protection) diode. When the output is turned "OFF" by input logic conditions the resulting inductive voltage transient seen at the output is detected by an internal zener reference. The reference then momentarily activates the output transistor long enough so that the relay energy is discharged. This feature eliminates the need of external circuit protection components and insures output transistor protection.

The outputs are Darlington connected transistors, which allow high current operation at low internal V_{CC} current levels—base drive for the output transistor is obtained from the load in proportion to the required loading conditions. Typical V_{CC} power with both outputs "ON" is 90 mW.

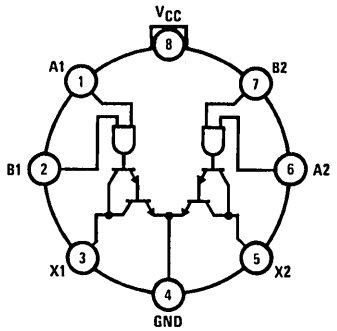
The circuit also features output transistor protection if the V_{CC} supply is lost by forcing the output into the high impedance "OFF" state with the same breakdown levels as when V_{CC} was applied.

Features

- TTL/LS/CMOS compatible inputs
- High impedance inputs (PNP's)
- High output voltage breakdown (65V typ)
- High output current capability (300 mA max)
- Internal protection circuit eliminates need for output protection diode
- Output breakdown protection if V_{CC} supply is lost
- Low V_{CC} power dissipation (90 mW (typ) both outputs "ON")
- Voltage and current levels compatible for use in telephone relay applications

Connection Diagrams

Metal Can Package



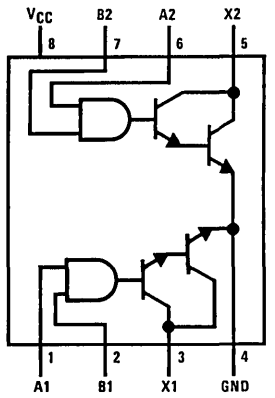
TL/F/5822–1

Top View

Pin 4 is in electrical contact with the case

Order Number DS3686H
See NS Package Number H08C

Dual-In-Line Package



TL/F/5822–2

Top View

Order Number DS3686J-8 or DS3686N
See NS Package Number J08A or N08E

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	15V
Output Voltage	56V
Storage Temperature Range	−65°C to +150°C

Maximum Power Dissipation* at 25°C	
Cavity Package	1133 mW
Molded Package	1022 mW
TO-5 Package	787 mW
Lead Temperature (Soldering, 4 seconds)	260°C

*Derate cavity package 7.6 mW/°C above 25°C; derate molded package 8.2 mW/°C above 25°C; derate TO-5 package 5.2 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage, V_{CC}	4.75	5.25	V
Temperature, T_A	0	±70	°C

Electrical Characteristics (Notes 2 and 3)

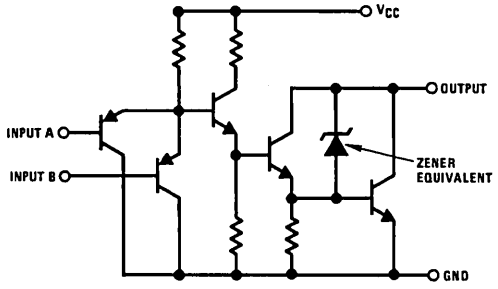
Symbol	Parameter	Conditions			Min	Typ	Max	Units
V_{IH}	Logical "1" Input Voltage	$R_L = 180\Omega$, $V_L = 54V$, $V_O \leq 2.5V$			2.0			V
I_{IH}	Logical "1" Input Current	V_{CC} = Max, $V_{IN} = 5.5V$				0.01	40	μA
V_{IL}	Logical "0" Input Voltage	$R_L = 180\Omega$, $V_L = 54V$, $V_O \leq 53.8V$					0.8	V
I_{IL}	Logical "0" Input Current	V_{CC} = Max, $V_{IN} = 0.4V$				−150	−250	μA
V_{CD}	Input Clamp Voltage	$V_{CC} = 5V$, $I_{CLAMP} = -12$ mA, $T_A = 25°C$				−1.0	−1.5	V
V_{OH}	Output Breakdown	V_{CC} = Max, $V_{IN} = 0V$, $I_{OUT} = 5$ mA			56	65		V
I_{OH}	Output Leakage	V_{CC} = Max, $V_{IN} = 0.4V$, $V_{OUT} = 54V$				0.5	250	μA
V_{OL}	Output ON Voltage	V_{CC} = Min, $V_{IN} = 2.4V$	DS3686	$I_{OL} = 100$ mA		0.85	1.0	V
				$I_{OL} = 300$ mA		1.0	1.2	V
$I_{CC(1)}$	Supply Current (Both Drivers)	V_{CC} = Max, $V_{IN} = 0V$, Outputs Open				2	4	mA
$I_{CC(0)}$	Supply Current (Both Drivers)	V_{CC} = Max, $V_{IN} = 3V$, Outputs Open				18	28	mA
t_{PD0}	Propagation Delay to a Logical "0" (Output Turn ON)	$C_L = 15$ pF, $V_L = 10V$, $R_L = 50\Omega$, $T_A = 25°C$, $V_{CC} = 5V$				50		ns
t_{PD1}	Propagation Delay to a Logical "1" (Output Turn OFF)	$C_L = 15$ pF, $V_L = 10V$, $R_L = 50\Omega$, $T_A = 25°C$, $V_{CC} = 5V$				1		μs

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C range for the DS3686. All typicals are given for $V_{CC} = 5V$ and $T_A = 25°C$.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Schematic Diagram



TL/F/5822-3

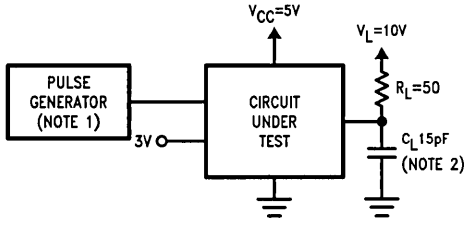
Truth Table

Positive logic: $\overline{AB} = X$

A	B	Output X
0	0	1
1	0	1
0	1	1
1	1	0

Logic "0" output "ON"
Logic "1" output "OFF"

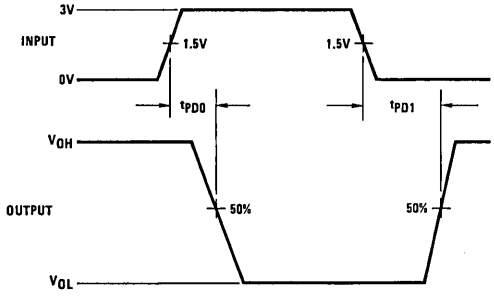
AC Test Circuit and Switching Time Waveforms



TL/F/5822-4

Note 1: The pulse generator has the following characteristics: PRR = 100 kHz, 50% duty cycle, $Z_{OUT} = 50\Omega$, $t_r = t_f \leq 10$ ns.

Note 2: C_L includes probe and jig capacitance.



TL/F/5822-5

National Semiconductor Corporation

DS1687/DS3687 Negative Voltage Relay Driver

General Description

The DS1687/DS3687 is a high voltage/current negative voltage relay driver having many features not available in present relay drivers.

PNP inputs provide both TTL/LS compatibility and high input impedance for low input loading.

Output leakage is specified over temperature at an output voltage of −54V. Minimum output breakdown (ac/latch breakdown) is specified over temperature at −5 mA. This clearly defines the actual breakdown of the device since the circuit has incorporated in it an internal reference which does not allow output breakdown latching found in existing relay drivers. Additionally, this internal reference circuit feature will eliminate the need in most cases of an external clamping (inductive transient voltage protection) diode. When the output is turned "OFF" by input logic conditions the resulting inductive voltage transient seen at the output is detected by an internal zener reference. The reference then momentarily activates the output transistor long enough so that the relay energy is discharged. This feature eliminates the need of external circuit protection components and insures output transistor protection.

The outputs are Darlington connected transistors, which allow high current operation at low internal V_{CC} current levels—base drive for the output transistor is obtained from the load in proportion to the required loading conditions. Typical V_{CC} power with both outputs "ON" is 90 mW.

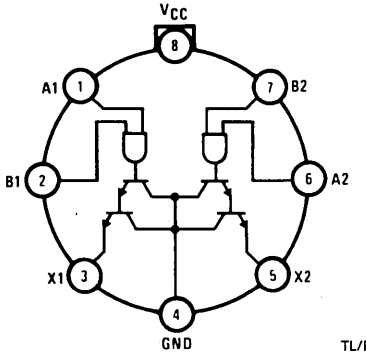
The circuit also features output transistor protection if the V_{CC} supply is lost by forcing the output into the high impedance "OFF" state with the same breakdown levels as when V_{CC} was applied.

Features

- TTL/LS/CMOS compatible inputs
- High impedance inputs (PNP's)
- High output voltage breakdown (−65V typ)
- High output current capability (300 mA max)
- Internal protection circuit eliminates need for output protection diode
- Output breakdown protection if V_{CC} supply is lost
- Low V_{CC} power dissipation (90 mW (typ) both outputs "ON")
- Voltage and current levels compatible for use in telephone relay applications

Connection Diagrams

Metal Can Package



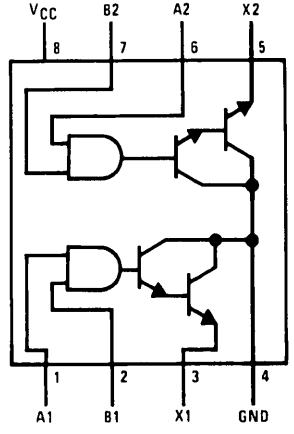
TL/F/5823-1

Top View

Pin 4 is in electrical with the case

Order Number DS1687H or DS3687H
See NS Package Number H08C

Dual-In-Line Package



TL/F/5823-2

Top View

Order Number DS1687J-8,
DS3687J-8 or DS3687N
See NS Package Number J08A or N08E

Truth Table

Positive logic: $\overline{AB} = X$

A	B	Output X
0	0	1
1	0	1
0	1	1
1	1	0

Logic "0" output "ON"
Logic "1" output "OFF"

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	15V
Output Voltage	56V
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1133 mW
Molded Package	1022 mW
TO-5 Package	787 mW
Lead Temperature (Soldering, 4 seconds)	260°C

*Derate cavity package 7.6 mW/°C above 25°C; derate molded package 8.2 mW/°C above 25°C; derate TO-5 package 5.2 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage, V_{CC}			
DS1687	4.5	5.5	V
DS3687	4.75	5.25	V
Temperature, T_A			
DS1687	−55	+125	°C
DS3687	0	+70	°C

Electrical Characteristics (Note 2 and 3)

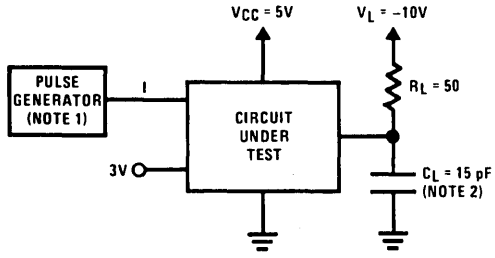
Symbol	Parameter	Conditions			Min	Typ	Max	Units
V_{IH}	Logical "1" Input Voltage				2.0			V
I_{IH}	Logical "1" Input Current	V_{CC} = Max, V_{IN} = 5.5V				1.0		μA
V_{IL}	Logical "0" Input Voltage						0.8	V
I_{IL}	Logical "0" Input Current	V_{CC} = Max, V_{IN} = 0.4V				−150	−250	μA
V_{CD}	Input Clamp Voltage	V_{CC} = 5V, I_{CLAMP} = −12 mA, T_A = 25°C				−1.0	−1.5	V
V_{OH}	Output Breakdown	V_{CC} = Max, V_{IN} = 0V, I_{OUT} = −5 mA			−56	−65		V
I_{OH}	Output Leakage	V_{CC} = Max, V_{IN} = 0V, V_{OUT} = −54V				−0.5	−250	μA
V_{OL}	Output ON Voltage	V_{CC} = Min, V_{IN} = 2V	DS1687	I_{OL} = −100 mA		−0.9	−1.1	V
				I_{OL} = −300 mA		−1.0	−1.3	V
			DS3687	I_{OL} = −100 mA		−0.9	−1.0	V
				I_{OL} = −300 mA		−1.0	−1.2	V
$I_{CC(1)}$	Supply Current (Both Drivers)	V_{CC} = Max, V_{IN} = 0V, Outputs Open				2	4	mA
$I_{CC(0)}$	Supply Current (Both Drivers)	V_{CC} = Max, V_{IN} = 3V, Outputs Open				18	28	mA
$t_{PD(ON)}$	Propagation Delay to a Logical "0" (Output Turn ON)	C_L = 15 pF, V_L = −10V, R_L = 50Ω, T_A = 25°C, V_{CC} = 5V				50		ns
$t_{PD(OFF)}$	Propagation Delay to a Logical "1" (Output Turn OFF)	C_L = 15 pF, V_L = −10V, R_L = 50Ω, T_A = 25°C, V_{CC} = 5V				1.0		μs

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperture range for the DS1687 and across the 0°C to +70°C range for the DS3687. All typicals are given for V_{CC} = 5V and T_A = 25°C.

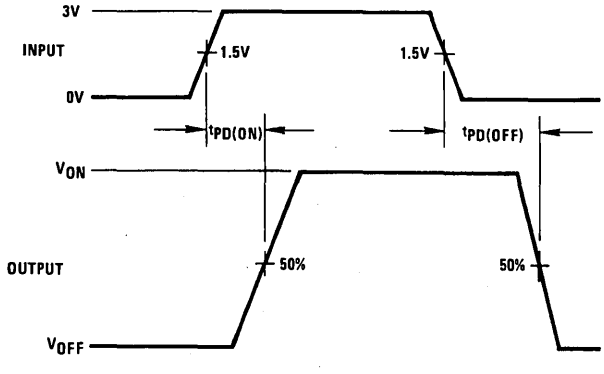
Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min or absolute value basis.

AC Test Circuit and Switching Time Waveforms



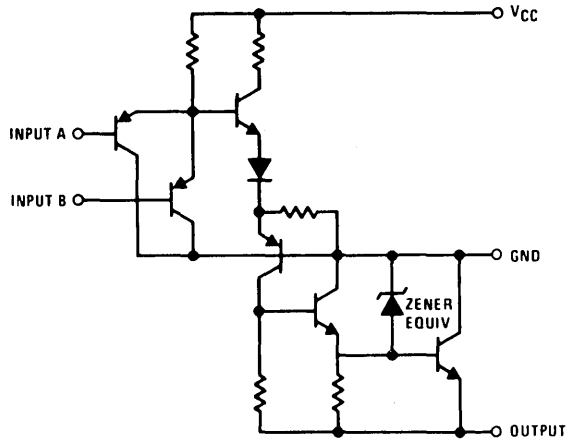
TL/F/5823–4

Note 1: The pulse generator has the following characteristics:
PRR = MHz, 50% duty cycle, $Z_{OUT} \cong 50\Omega$, $t_r = t_f \leq 10$ ns.
Note 2: C_L includes probe and jig capacitance.



TL/F/5823–5

Schematic Diagram



TL/F/5823–3

National Semiconductor Corporation

DS55451/2/3/4, DS75450/1/2/3/4 Series Dual Peripheral Drivers

General Description

The DS75450 series of dual peripheral drivers is a family of versatile devices designed for use in systems that use TTL logic. Typical applications include high speed logic buffers, power drivers, relay drivers, lamp drivers, MOS drivers, bus drivers and memory drivers.

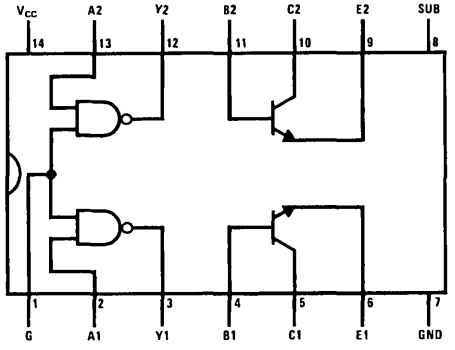
The DS75450 is a general purpose device featuring two standard Series 54/74 TTL gates and two uncommitted, high current, high voltage NPN transistors. The device offers the system designer the flexibility of tailoring the circuit to the application.

The DS55451/DS75451, DS55452/DS75452, DS55453/DS75453 and DS55454/DS75454 are dual peripheral AND, NAND, OR and NOR drivers, respectively, (positive logic) with the output of the logic gates internally connected to the bases of the NPN output transistors.

Features

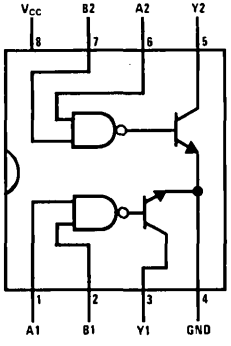
- 300 mA output current capability
- High voltage outputs
- No output latch-up at 20V
- High speed switching
- Choice of logic function
- TTL compatible diode-clamped inputs
- Standard supply voltages
- Replaces TI "A" and "B" series

Connection Diagrams (Dual-In-Line and Metal Can Packages)



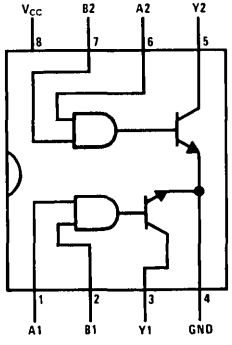
TL/F/5824–1

Top View
Order Number DS75450J or DS75450N
See NS Package Number J14A or N14A



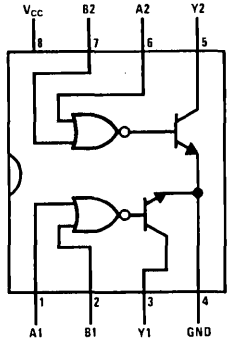
TL/F/5824–2

Top View
Order Number DS55451J-8, DS75451J-8, DS75451M or DS75451N



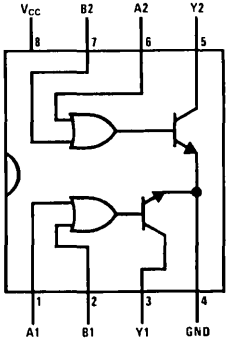
TL/F/5824–3

Top View
Order Number DS55452J-8, DS75452J-8, DS75452M or DS75452N



TL/F/5824–4

Top View
Order Number DS55453J-8, DS75453J-8, DS75453M or DS75453N



TL/F/5824–5

Top View
Order Number DS55454J-8, DS75454J-8 or DS75454N

See NS Package Numbers J08A, M08A* or N08E

*See Note 6 and AN-336 regarding S.O. package power dissipation constraints.

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage, (V_{CC}) (Note 2)	7.0V
Input Voltage	5.5V
Inter-Emitter Voltage (Note 3)	5.5V
V_{CC}-to-Substrate Voltage DS75450	35V
Collector-to-Substrate Voltage DS75450	35V
Collector-Base Voltage DS75450	35V
Collector-Emitter Voltage (Note 4) DS75450	30V
Emitter-Base Voltage DS75450	5.0V
Output Voltage (Note 5) DS55451/DS75451, DS55452/DS75452, DS55453/DS75453, DS55454/DS75454	30V
Collector Current (Note 6) DS75450	300 mA
Output Current (Note 6) DS55451/DS75451, DS55452/DS75452, DS55453/DS75453, DS55454/DS75454	300 mA
DS75450 Maximum Power (Note 6) Dissipation* at 25°C	
Cavity Package	1308 mW
Molded Package	1207 mW
DS75451/2/3/4 Maximum Power (Note 6) Dissipation† at 25°C	
Cavity Package	1090 mW
Molded DIP Package	957 mW
TO-5 Package	760 mW
SO Package	632 mW
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 4 sec.)	260°C

Operating Conditions (Note 7)

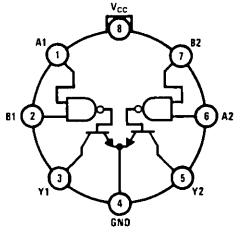
	Min	Max	Units
Supply Voltage, (V_{CC})			
DS5545X	4.5	5.5	V
DS7545X	4.75	5.25	V
Temperature, (T_A)			
DS5545X	−55	+125	°C
DS7545X	0	+70	°C

*Derate cavity package 8.7 mW/°C above 25°C; derate molded package 9.7 mW/°C above 25°C.

†Derate cavity package 7.3 mW/°C above 25°C; derate molded package 7.7 mW/°C above 25°C; derate TO-5 package 5.1 mW/°C above 25°C; derate SO package 7.56 mW/°C above 25°C.

See App Note AN-336 for further information on Understanding Package Power Dissipation.

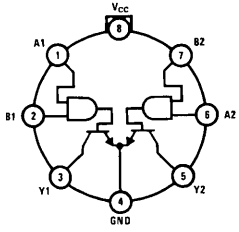
Connection Diagrams (Dual-In-Line and Metal Can Packages) (Continued)



TL/F/5824-6

Top View

Order Number DS55451H or DS75451H

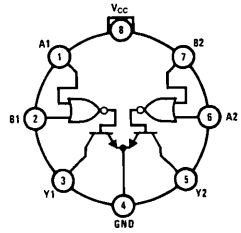


TL/F/5824-7

Top View

(Pin 4 is in Electrical Contact with the Case)

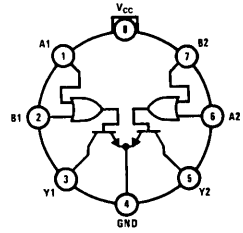
Order Number DS55452H or DS75452H



TL/F/5824-8

Top View

Order Number DS55453H or DS75453H



TL/F/5824-9

Top View

Order Number DS55454H or DS75454H

See NS Package Number H08C

Electrical Characteristics DS75450 (Notes 8 and 9)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
TTL GATES							
V_{IH}	High Level Input Voltage	*(Figure 1)*		2			V
V_{IL}	Low Level Input Voltage	*(Figure 2)*				0.8	V
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA, *(Figure 3)*				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IL} = 0.8V, I_{OH} = −400 μA, *(Figure 2)*		2.4	3.3		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, I_{OL} = 16 mA *(Figure 1)*			0.22	0.4	V
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5V, *(Figure 4)*	Input A			1	mA
			Input G			2	mA

Electrical Characteristics DS75450 (Notes 8 and 9) (Continued)

Symbol	Parameter	Conditions			Min	Typ	Max	Units
TTL GATES (Continued)								
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V, *(Figure 4)*		Input A			40	μA
				Input G			80	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V, *(Figure 3)*		Input A			−1.6	mA
				Input G			−3.2	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max, *(Figure 5)*, (Note 10)			−18		−55	mA
I_{CCH}	Supply Current	V_{CC} = Max, V_I = 0V, Outputs High, *(Figure 6)*				2	4	mA
I_{CCL}	Supply Current	V_{CC} = Max, V_I = 5V, Outputs Low, *(Figure 6)*				6	11	mA
OUTPUT TRANSISTORS								
$V_{(BR)CBO}$	Collector-Base Breakdown Voltage	I_C = 100 μA, I_E = 0 μA			35			V
$V_{(BR)CER}$	Collector-Emitter Breakdown Voltage	I_C = 100 μA, R_{BE} = 500Ω			30			V
$V_{(BR)EBO}$	Emitter-Base Breakdown Voltage	I_E = 100 μA, I_C = 0 μA			5			V
h_{FE}	Static Forward Current Transfer Ratio	V_{CE} = 3V, (Note 11)	T_A = +25°C	I_C = 100 mA	25			
				I_C = 300 mA	30			
			T_A = 0°C	I_C = 100 mA	20			
				I_C = 300 mA	25			
V_{BE}	Base-Emitter Voltage	(Note 11)		I_B = 10 mA, I_C = 100 mA		0.85	1	V
				I_B = 30 mA, I_C = 300 mA		1.05	1.2	V
$V_{CE(SAT)}$	Collector-Emitter Saturation Voltage	(Note 11)		I_B = 10 mA, I_C = 100 mA		0.25	0.4	V
				I_B = 30 mA, I_C = 300 mA		0.5	0.7	V

Electrical Characteristics (Continued)

DS55451/DS75451, DS55452/DS75452, DS55453/DS75453, DS55454/DS75454 (Notes 8 and 9)

Symbol	Parameter	Conditions				Min	Typ	Max	Units
V_{IH}	High-Level Input Voltage	*(Figure 7)*				2			V
V_{IL}	Low-Level Input Voltage							0.8	V
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA						−1.5	V
V_{OL}	Low-Level Output Voltage	V_{CC} = Min, *(Figure 7)*	V_{IL} = 0.8V	I_{OL} = 100 mA	DS55451, DS55453		0.25	0.5	V
					DS75451, DS75453		0.25	0.4	V
				I_{OL} = 300 mA	DS55451, DS55453		0.5	0.8	V
					DS75451, DS75453		0.5	0.7	V
			V_{IH} = 2V	I_{OL} = 100 mA	DS55452, DS55454		0.25	0.5	V
					DS75452, DS75454		0.25	0.4	V
				I_{OL} = 300 mA	DS55452, DS55454		0.5	0.8	V
					DS75452, DS75454		0.5	0.7	V
I_{OH}	High-Level Output Current	V_{CC} = Min, *(Figure 7)*	V_{OH} = 30V	V_{IH} = 2V	DS55451, DS55453			300	μA
					DS75451, DS75453			100	μA
				V_{IL} = 0.8V	DS55452, DS55454			300	μA
					DS75452, DS75454			100	μA
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5V, *(Figure 9)*						1	mA

Electrical Characteristics (Continued)

DS55451/DS75451, DS55452/DS75452, DS55453/DS75453, DS55454/DS75454 (Notes 8 and 9) (Continued)

Symbol	Parameter	Conditions			Min	Typ	Max	Units
I_{IH}	High-Level Input Current	V_{CC} = Max, V_I = 2.4V, *(Figure 9)*					40	μA
I_{IL}	Low-Level Input Current	V_{CC} = Max, V_I = 0.4V, *(Figure 8)*				−1	−1.6	mA
I_{CCH}	Supply Current, Outputs High	V_{CC} = Max, *(Figure 10)*	V_I = 5V	DS55451/DS75451		7	11	mA
			V_I = 0V	DS55452/DS75452		11	14	mA
			V_I = 5V	DS55453/DS75453		8	11	mA
			V_I = 0V	DS55454/DS75454		13	17	mA
I_{CCL}	Supply Current, Outputs Low	V_{CC} = Max, *(Figure 10)*	V_I = 0V	DS55451/DS75451		52	65	mA
			V_I = 5V	DS55452/DS75452		56	71	mA
			V_I = 0V	DS55453/DS75453		54	68	mA
			V_I = 5V	DS55454/DS75454		61	79	mA

Switching Characteristics DS75450 (V_{CC} = 5V, T_A = 25°C)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	C_L = 15 pF	R_L = 400Ω, TTL Gates, *(Figure 12)*		12	22	ns
			R_L = 50Ω, $I_C \approx$ 200 mA, Gates and Transistors Combined, *(Figure 14)*		20	30	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	C_L = 15 pF	R_L = 400Ω, TTL Gates, *(Figure 12)*		8	15	ns
			R_L = 50Ω, $I_C \approx$ 200 mA, Gates and Transistors Combined, *(Figure 14)*		20	30	ns
t_{TLH}	Transition Time, Low-to-High Level Output	C_L = 15 pF, R_L = 50Ω, $I_C \approx$ 200 mA, Gates and Transistors Combined, *(Figure 14)*			7	12	ns
t_{THL}	Transition Time, High-to-Low Level Output	C_L = 15 pF, R_L = 50Ω, $I_C \approx$ 200 mA, Gates and Transistors Combined, *(Figure 14)*			9	15	ns
V_{OH}	High-Level Output Voltage after Switching	V_S = 20V, $I_C \approx$ 300 mA, R_{BE} = 500Ω, *(Figure 15)*		V_S − 6.5			mV
t_D	Delay Time	I_C = 200 mA, $I_{B(1)}$ = 20 mA, I_B = −40 mA, $V_{BE(OFF)}$ = −1V, C_L = 15 pF, R_L = 50Ω, *(Figure 13)*, (Note 12)			8	15	ns
t_R	Rise Time				12	20	ns
t_S	Storage Time				7	15	ns
t_F	Full Time				6	15	ns

Switching Characteristics (Continued)

DS55451/DS75451, DS55452/DS75452, DS55453/DS75453, DS55454/DS75454 (V_{CC} = 5V, T_A = 25°C)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	C_L = 15 pF, R_L = 50Ω, $I_O \approx$ 200 mA, *(Figure 14)*	DS55451/DS75451		18	25	ns
			DS55452/DS75452		26	35	ns
			DS55453/DS75453		18	25	ns
			DS55454/DS75454		27	35	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	C_L = 15 pF, R_L = 50Ω, $I_O \approx$ 200 mA, *(Figure 14)*	DS55451/DS75451		18	25	ns
			DS55452/DS75452		24	35	ns
			DS55453/DS75453		16	25	ns
			DS55454/DS75454		24	35	ns
t_{TLH}	Transition Time, Low-to-High Level Output	C_L = 15 pF, R_L = 50Ω, $I_O \approx$ 200mA, *(Figure 14)*			5	8	ns
t_{THL}	Transition Time, High-to-Low Level Output	C_L = 15 pF, R_L = 50Ω, $I_O \approx$ 200 mA, *(Figure 14)*			7	12	ns
V_{OH}	High-Level Output Voltage after Switching	V_S = 20V, $I_O \approx$ 300 mA, *(Figure 15)*		V_S − 6.5			mV

Switching Characteristics (Continued)

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Voltage values are with respect to network ground terminal unless otherwise specified.

Note 3: The voltage between two emitters of a multiple-emitter transistor.

Note 4: Value applies when the base-emitter resistance (R_{BE}) is equal to or less than 500Ω.

Note 5: The maximum voltage which should be applied to any output when it is in the "OFF" state.

Note 6: Both halves of these dual circuits may conduct rated current simultaneously; however, power dissipation averaged over a short time interval must fall within the continuous dissipation rating.

Note 7: For the DS75450 only, the substrate (pin 8) must always be at the most-negative device voltage for proper operation.

Note 8: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS55450 series and across the 0°C to +70°C range for the DS75450 series. All typicals are given for V_{CC} = +5V and T_A = 25°C.

Note 9: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 10: Only one output at a time should be shorted.

Note 11: These parameters must be measured using pulse techniques. t_W = 300 μs, duty cycle < 2%.

Note 12: Applies to output transistors only.

Truth Tables (H = high level, L = low level)

DS55451/DS75451

A	B	Y
L	L	L (ON State)
L	H	L (ON State)
H	L	L (ON State)
H	H	H (OFF State)

DS55453/DS75453

A	B	Y
L	L	L (ON State)
L	H	H (OFF State)
H	L	H (OFF State)
H	H	H (OFF State)

DS55452/DS75452

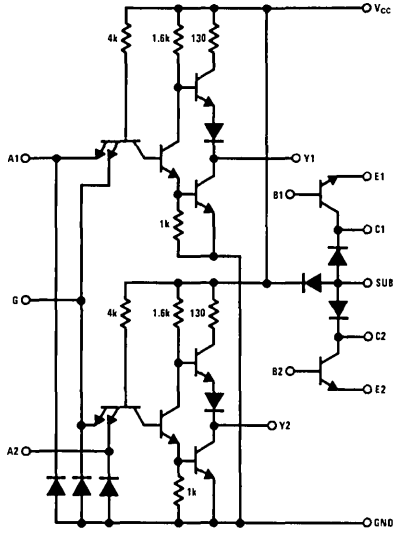
A	B	Y
L	L	H (OFF State)
L	H	H (OFF State)
H	L	H (OFF State)
H	H	L (ON State)

DS55454/DS75454

A	B	Y
L	L	H (OFF State)
L	H	L (ON State)
H	L	L (ON State)
H	H	L (ON State)

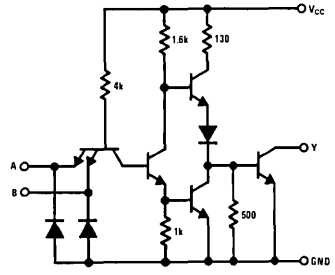
Schematic Diagrams

DS75450



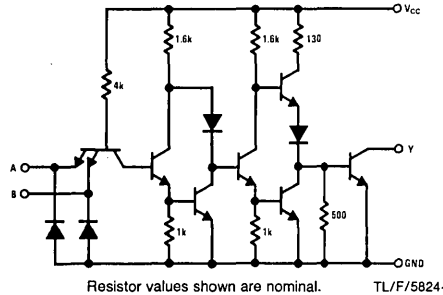
Resistor values shown are nominal. TL/F/5824–10

DS55451/DS75451



Resistor values shown are nominal. TL/F/5824–11

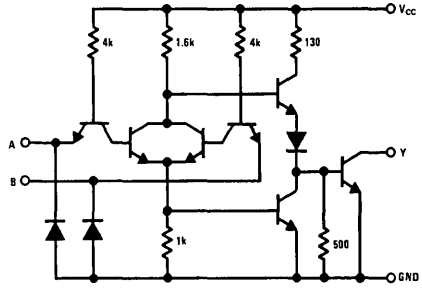
DS55452/DS75452



Resistor values shown are nominal. TL/F/5824–12

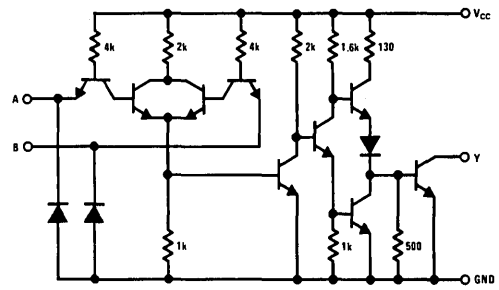
Schematic Diagrams (Continued)

DS55453/DS75453



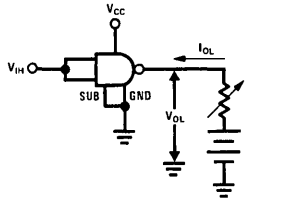
Resistor values shown are nominal. TL/F/5824–13

DS55454/DS75454



Resistor values shown are nominal. TL/F/5824–14

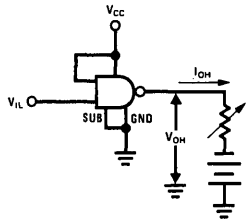
DC Test Circuits



TL/F/5824–15

Both inputs are tested simultaneously.

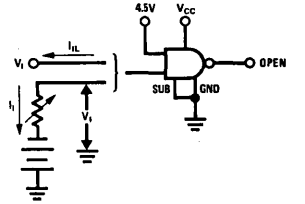
FIGURE 1. V_{IH}, V_{OL}



TL/F/5824–16

Each input is tested separately.

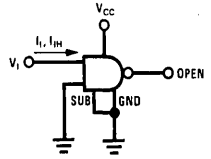
FIGURE 2. V_{IL}, V_{OH}



TL/F/5824–17

Each input is tested separately.

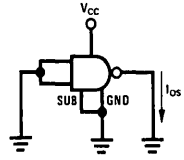
FIGURE 3. V_I, I_{IL}



TL/F/5824–18

Each input is tested separately.

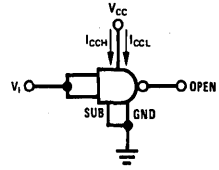
FIGURE 4. I_I, I_{IH}



TL/F/5824–19

Each input is tested separately.

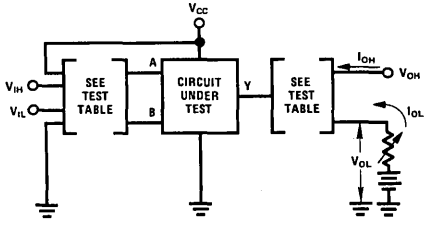
FIGURE 5. I_{OS}



TL/F/5824–20

Both gates are tested simultaneously.

FIGURE 6. I_{CCH}, I_{CCL}

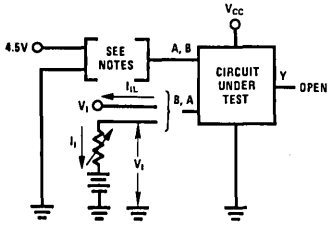


TL/F/5824–21

Circuit	Input Under Test	Other Input	Output	
			Apply	Measure
DS55451	V_{IH}	V_{IH}	V_{OH}	I_{OH}
	V_{IL}	V_{CC}	I_{OL}	V_{OL}
DS55452	V_{IH}	V_{IH}	I_{OL}	V_{OL}
	V_{IL}	V_{CC}	V_{OH}	I_{OH}
DS55453	V_{IH}	Gnd	V_{OH}	I_{OH}
	V_{IL}	V_{IL}	I_{OL}	V_{OH}
DS55454	V_{IH}	Gnd	I_{OL}	V_{OL}
	V_{IL}	V_{IL}	V_{OH}	I_{OH}

FIGURE 7. V_{IH}, V_{IL}, I_{OH}, V_{OL}

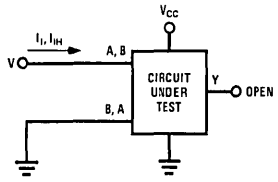
DC Test Circuits (Continued)



Note A: Each input is tested separately.
Note B: When testing DS55453/DS75453, DS55454/DS75454, input not under test is grounded.
For all other circuits it is at 4.5V.

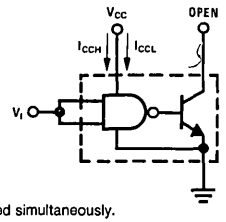
TL/F/5824-22

FIGURE 8. V_I, V_{IL}



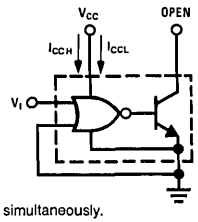
Each input is tested separately. TL/F/5824-23

FIGURE 9. I_I, I_{IH}



Both gates are tested simultaneously. TL/F/5824-24

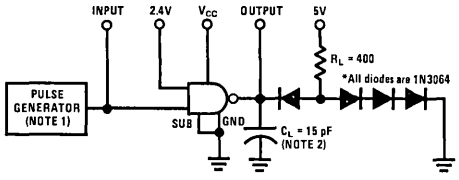
FIGURE 10. I_{CCH}, I_{CCL} for AND, NAND Circuits



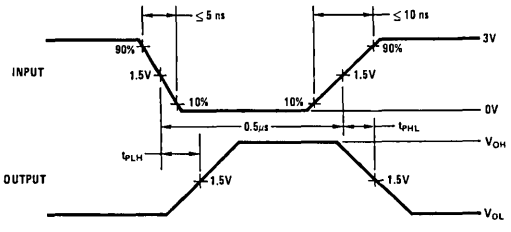
Both gates are tested simultaneously. TL/F/5824-25

FIGURE 11. I_{CCH}, I_{CCL} for OR, NOR Circuits

AC Test Circuits and Switching Time Waveforms



TL/F/5824-26



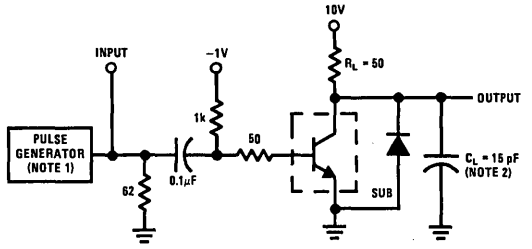
TL/F/5824-27

Note 1: The pulse generator has the following characteristics: PRR = 1 MHz, $Z_{OUT} \approx 50\Omega$.
Note 2: C_L includes probe and jig capacitance.

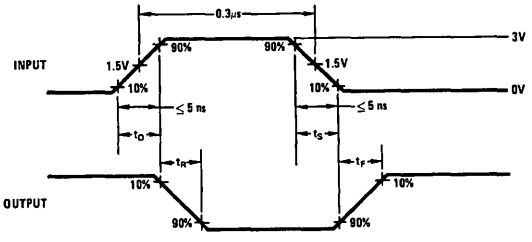
FIGURE 12. Propagation Delay Times, Each Gate (DS75450 Only)

3

AC Test Circuits and Switching Time Waveforms (Continued)



TL/F/5824-28

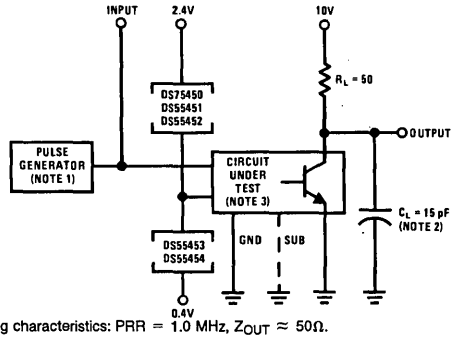


TL/F/5824-29

Note 1: The pulse generator has the following characteristics: duty cycle ≤ 1%, $Z_{OUT} \approx 50\Omega$.

Note 2: C_L includes probe and jig capacitance.

FIGURE 13. Switching Times, Each Transistor (DS75450 Only)

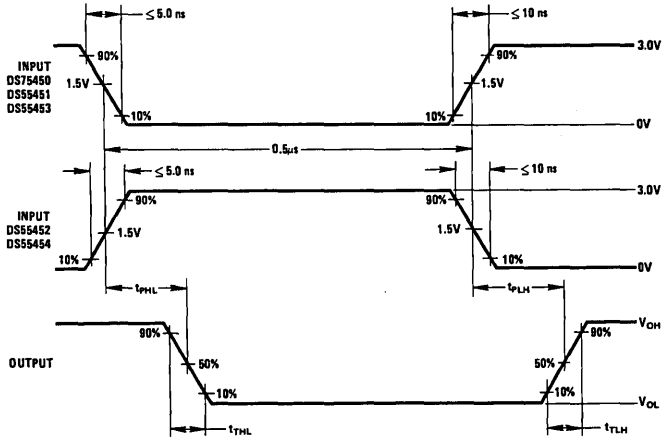


Note 1: The pulse generator has the following characteristics: PRR = 1.0 MHz, $Z_{OUT} \approx 50\Omega$.

TL/F/5824-30

Note 2: C_L includes probe and jig capacitance.

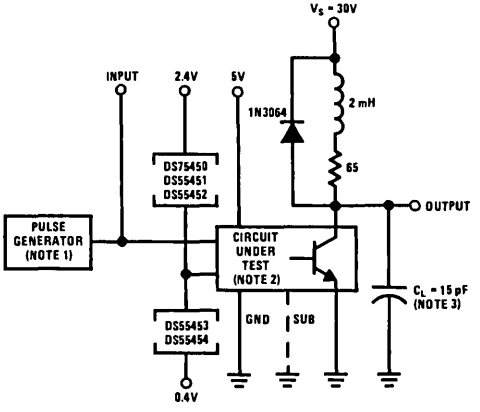
Note 3: When testing DS75450, connect output V to transistor base and ground the substrate terminal.



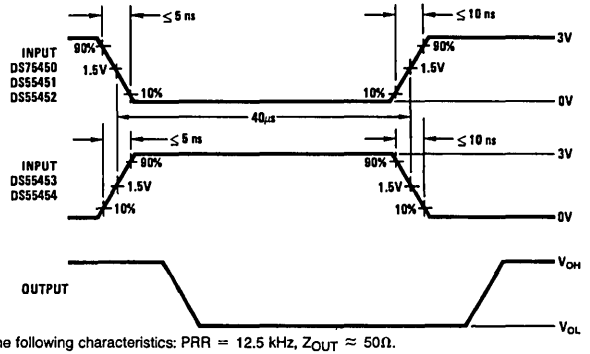
TL/F/5824-31

FIGURE 14. Switching Times of Complete Drivers

AC Test Circuits and Switching Time Waveforms (Continued)



TL/F/5824-32



TL/F/5824-33

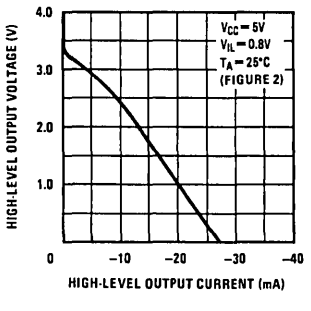
Note 1: The pulse generator has the following characteristics: PRR = 12.5 kHz, $Z_{OUT} \approx 50\Omega$.

Note 2: When testing DS75450, connect output V to transistor base with a 600Ω resistor from there to ground and ground the substrate terminal.

Note 3: C_L includes probe and jig capacitance.

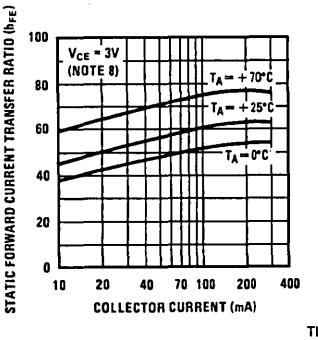
FIGURE 15. Latch-UP Test of Complete Drivers

Typical Performance Characteristics



TL/F/5824-34

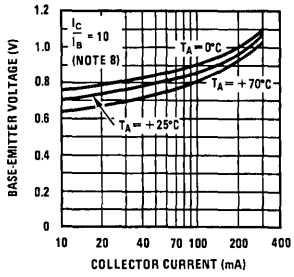
FIGURE 16. DS75450 TTL Gate High-Level Output Voltage vs High-Level Output Current



TL/F/5824-35

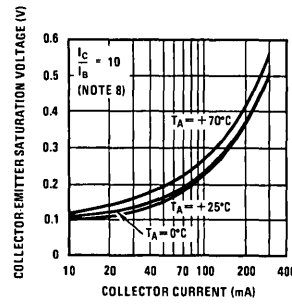
FIGURE 17. DS75450 Transistor Static Forward Current Transfer Ratio vs Collector Current

Typical Performance Characteristics (Continued)



TL/F/5824–36

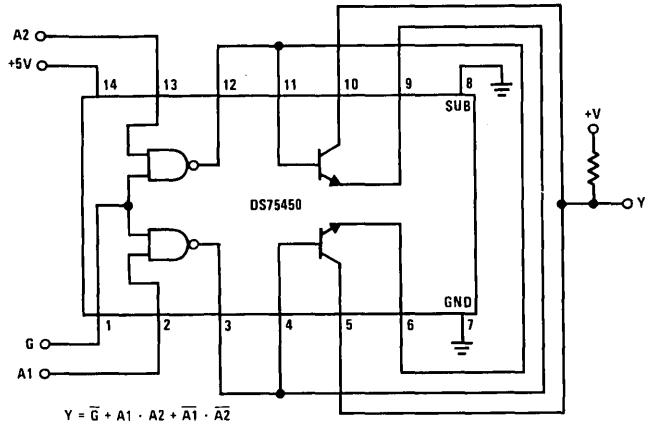
FIGURE 18. DS75450 Transistor Base-Emitter Voltage vs Collector Current



TL/F/5824–37

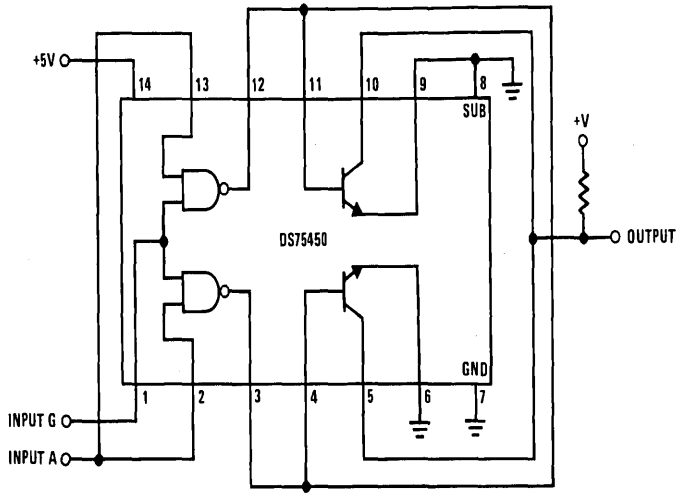
FIGURE 19. Transistor Collector-Emitter Saturation Voltage vs Collector Current

Typical Applications



TL/F/5824–38

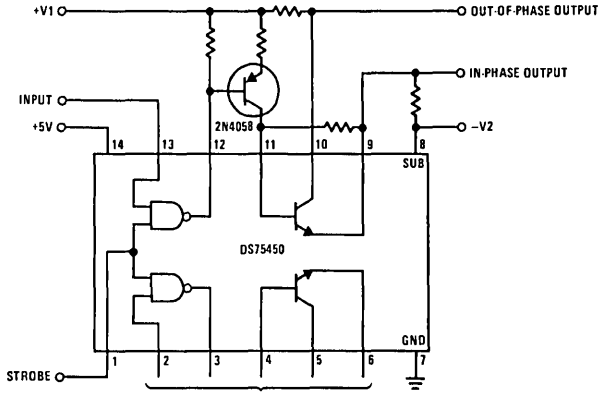
FIGURE 20. Gated Comparator



TL/F/5824–39

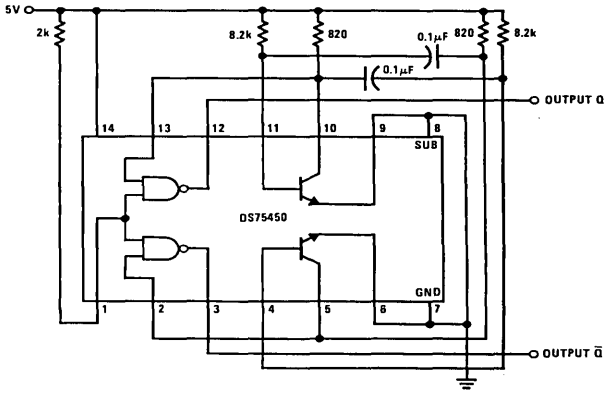
FIGURE 21. 500 mA Sink

Typical Applications (Continued)



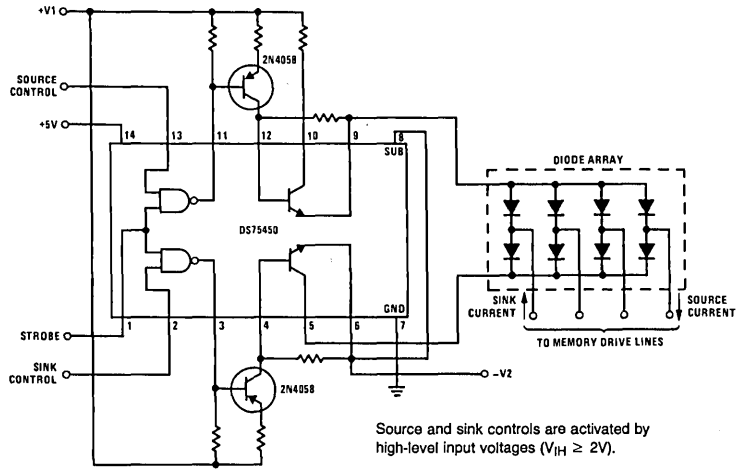
TL/F/5824–40

FIGURE 22. Floating Switch



TL/F/5824–41

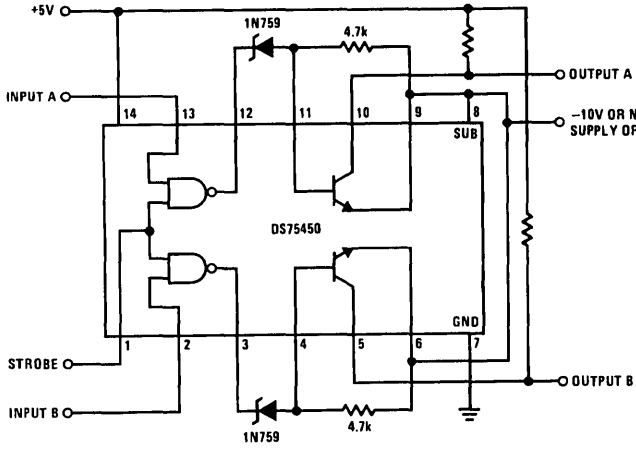
FIGURE 23. Square-Wave Generator



TL/F/5824–42

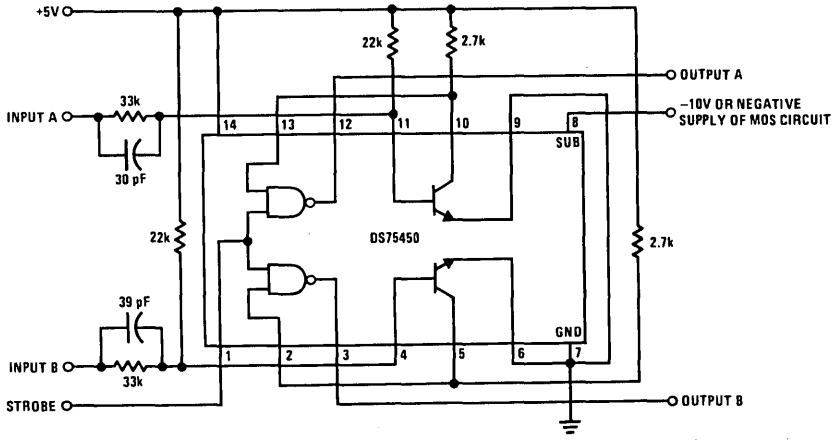
FIGURE 24. Core Memory Driver

Typical Applications (Continued)



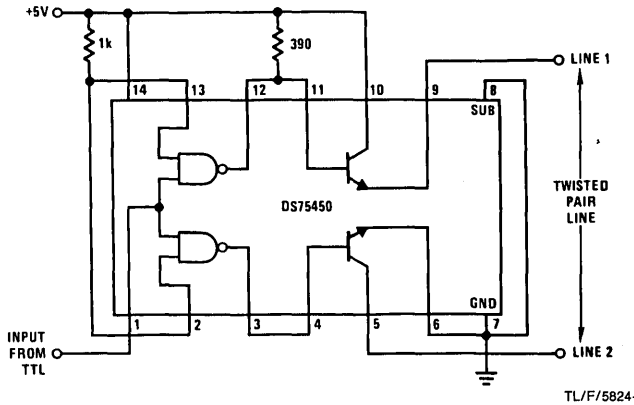
TL/F/5824–43

FIGURE 25. Dual TTL-to-MOS Driver



TL/F/5824–44

FIGURE 26. Dual MOS-to-TTL Driver

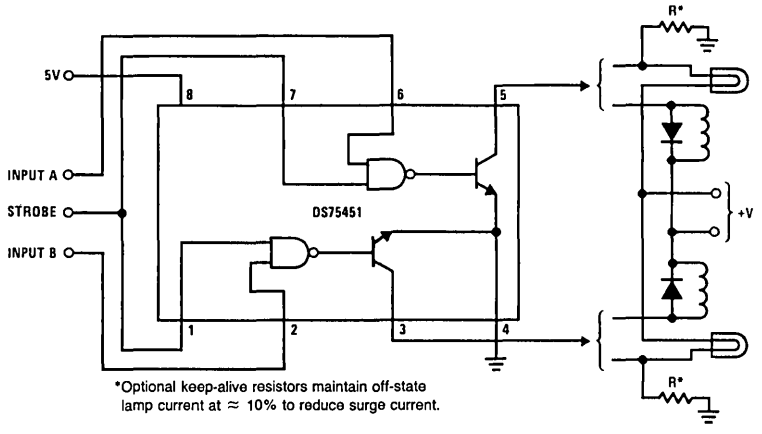


Termination is made at the receiving end as follows:
Line 1 is terminated to ground through Z_O/Z;
Line 2 is terminated to +5V through Z_O/Z;
where Z_O is the line impedance.

TL/F/5824–45

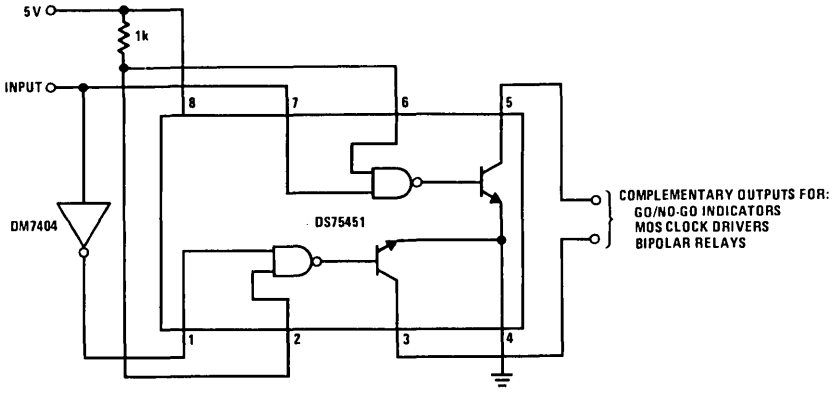
FIGURE 27. Balanced Line Driver

Typical Applications (Continued)



TL/F/5824–46

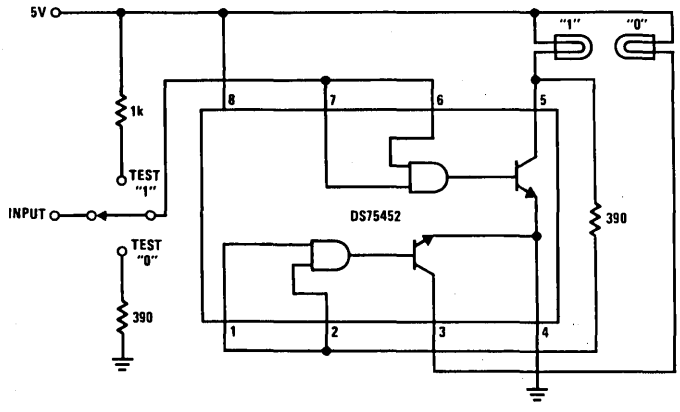
FIGURE 28. Dual Lamp or Relay Driver



TL/F/5824–47

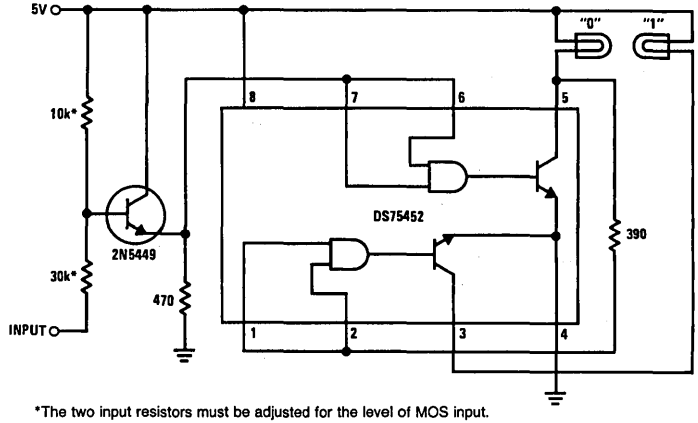
FIGURE 29. Complementary Driver

Typical Applications (Continued)



TL/F/5824–48

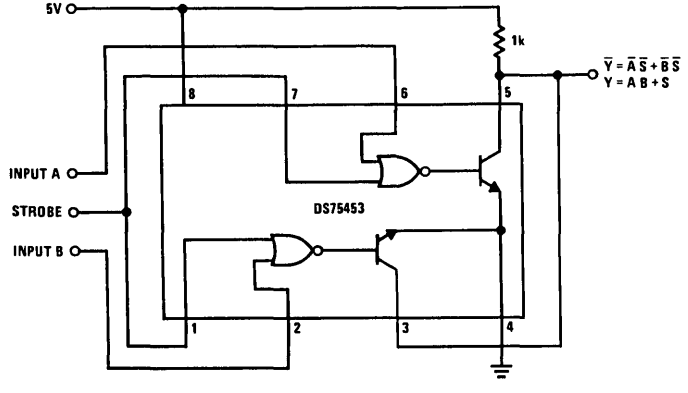
FIGURE 30. TTL or DTL Positive Logic-Level Detector



*The two input resistors must be adjusted for the level of MOS input.

TL/F/5824–49

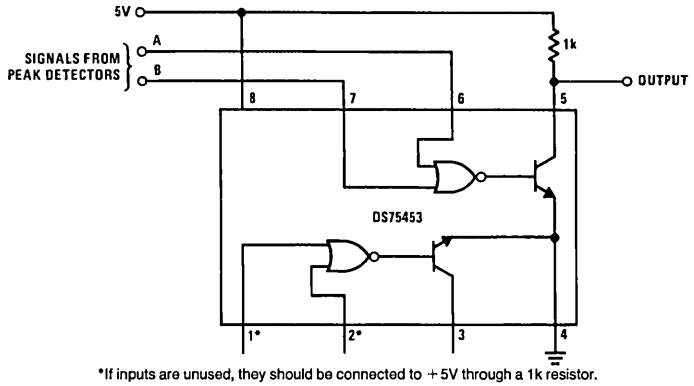
FIGURE 31. MOS Negative Logic-Level Detector



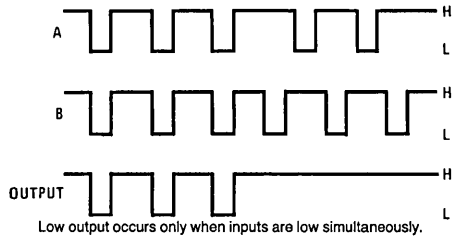
TL/F/5824–50

FIGURE 32. Logic Signal Comparator

Typical Applications (Continued)

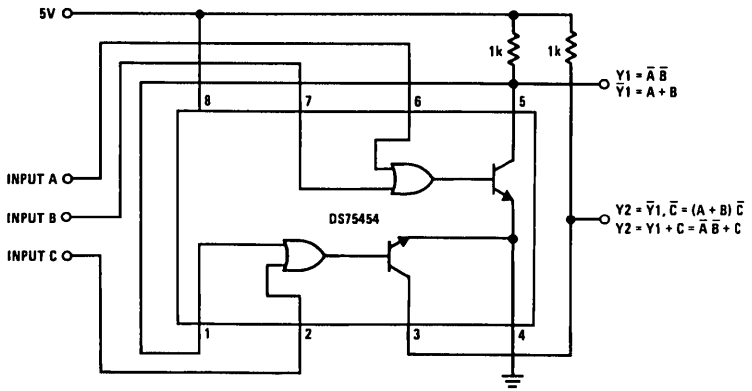


*If inputs are unused, they should be connected to +5V through a 1k resistor. TL/F/5824–51



Low output occurs only when inputs are low simultaneously. TL/F/5824–52

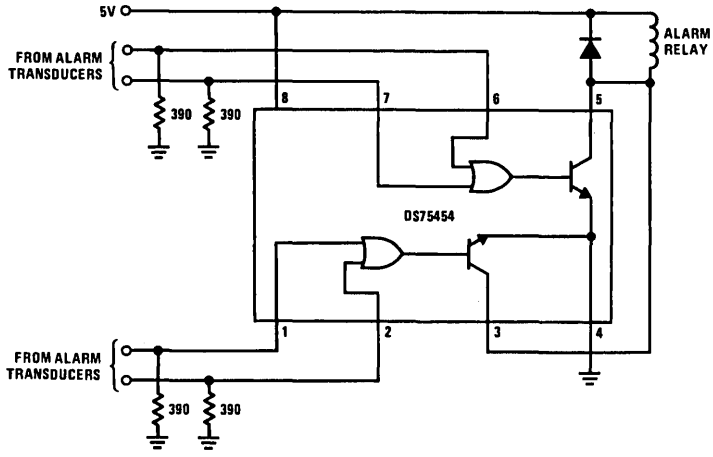
FIGURE 33. In-Phase Detector



TL/F/5824–53

FIGURE 34. Multifunction Logic-Signal Comparator

Typical Applications (Continued)



TL/F/5824–54

FIGURE 35. Alarm Detector

National Semiconductor Corporation

DS55461/2/3/4, DS75461/2/3/4 Series Dual Peripheral Drivers

General Description

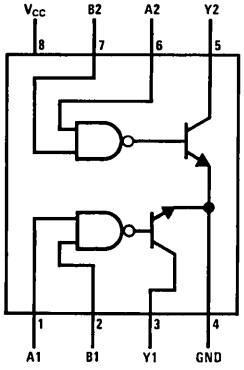
The DS55461/2/3/4 series of dual peripheral drivers are functionally interchangeable with DS55451/2/3/4 series peripheral drivers, but are designed for use in systems that require higher breakdown voltages at the expense of slightly slower switching speeds. Typical applications include power drivers, logic buffers, lamp drivers, relay drivers, MOS drivers, line drivers and memory drivers.

The DS55461/DS75461, DS55462/DS75462, DS55463/DS75463 and DS55464/DS75464 are dual peripheral AND, NAND, OR and NOR drivers, respectively, (positive logic) with the output of the logic gates internally connected to the bases of the NPN output transistors.

Features

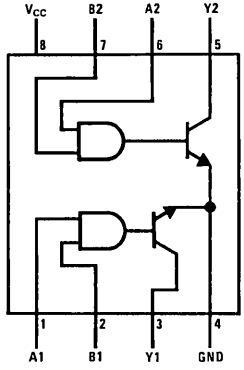
- 300 mA output current capability
- High voltage outputs
- No output latch-up at 30V
- Medium speed switching
- Circuit flexibility for varied applications and choice of logic function
- TTL compatible diode-clamped inputs
- Standard supply voltages

Connection Diagrams (Dual-In-Line and Metal Can Packages)



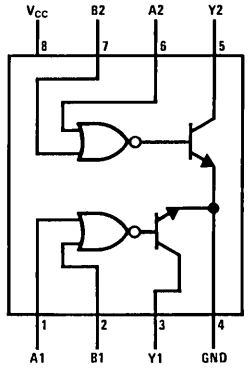
TL/F/5825-1

Top View
Order Number DS55461J-8, DS75461J-8 or DS75461N



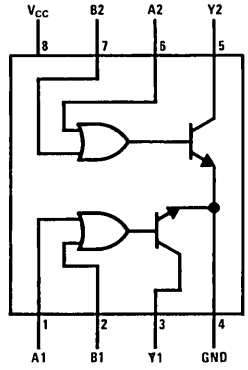
TL/F/5825-2

Top View
Order Number DS55464J-8, DS75464J-8 or DS75464N



TL/F/5825-3

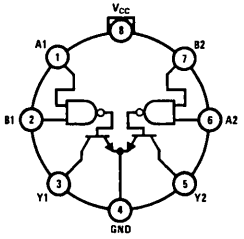
Top View
Order Number DS55463J-8, DS75463J-8 or DS75463N



TL/F/5825-4

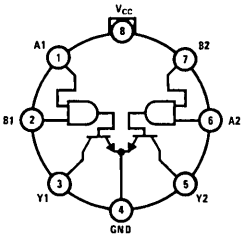
Top View
Order Number DS55462J-8, DS75462J-8 or DS75462N

See NS Package Numbers J08A or N08E



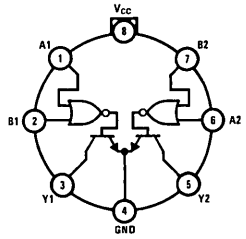
TL/F/5825-5

Top View
Pin 4 is in electrical contact with the case.
Order Number DS55461H or DS75461H



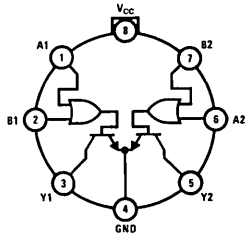
TL/F/5825-6

Top View
Pin 4 is in electrical contact with the case.
Order Number DS55462H or DS75462H



TL/F/5825-7

Top View
Pin 4 is in electrical contact with the case.
Order Number DS55463H or DS75463H



TL/F/5825-8

Top View
Pin 4 is in electrical contact with the case.
Order Number DS55464H or DS75464H

See NS Package Number H08C

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage (Note 2)	7V
Input Voltage	5.5V
Inter-emitter Voltage (Note 3)	5.5V
Output Voltage (Note 4) DS55461/DS75461, DS55462/DS75462, DS55463/DS75463, DS55464/DS75464	35V
Output Current (Note 5) DS55461/DS75461, DS55462/DS75462, DS55463/DS75463, DS55464/DS75464	300 mA
Maximum Power Dissipation* at 25°C	
Cavity Package	1090 mW
Molded Package	957 mW
TO-5 Package	760 mW

*Derate cavity package 7.3 mW/°C above 25°C; derate molded package 7.7 mW/°C above 25°C; derate TO-5 package 5.1 mW/°C above 25°C.

Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 4 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
DS5546X	4.5	5.5	V
DS7546X	4.75	5.25	V
Temperature (T_A)			
DS5546X	−55	+125	°C
DS7546X	0	+70	°C

Electrical Characteristics

DS55461/DS75461, DS55462/DS75462, DS55463/DS75463, DS55464/DS75464 (Notes 6 and 7)

Symbol	Parameter	Conditions			Min	Typ	Max	Units
V_{IH}	High Level Input Voltage	*(Figure 1)*			2			V
V_{IL}	Low Level Input Voltage	*(Figure 1)*					0.8	V
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.2	−1.5	V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, *(Figure 1)*	DS55461, V_{IL} = 0.8V	I_{OL} = 100 mA		0.15	0.5	V
				I_{OL} = 300 mA		0.36	0.8	V
			DS55462, V_{IH} = 2V	I_{OL} = 100 mA		0.16	0.5	V
				I_{OL} = 300 mA		0.35	0.8	V
			DS55463, V_{IL} = 0.8V	I_{OL} = 100 mA		0.18	0.5	V
				I_{OL} = 300 mA		0.39	0.8	V
			DS55464, V_{IH} = 2V	I_{OL} = 100 mA		0.17	0.5	V
				I_{OL} = 300 mA		0.38	0.8	V
			DS75461, V_{IL} = 0.8V	I_{OL} = 100 mA		0.15	0.4	V
				I_{OL} = 300 mA		0.36	0.7	V
			DS75462, V_{IH} = 2V	I_{OL} = 100 mA		0.16	0.4	V
				I_{OL} = 300 mA		0.35	0.7	V
			DS75463, V_{IL} = 0.8V	I_{OL} = 100 mA		0.18	0.4	V
				I_{OL} = 300 mA		0.39	0.7	V
			DS75464, V_{IH} = 2V	I_{OL} = 100 mA		0.17	0.4	V
				I_{OL} = 300 mA		0.38	0.7	V
I_{OH}	High Level Output Current	V_{CC} = Min, V_{OH} = 35V, *(Figure 1)*	V_{IH} = 2V	DS55461, DS55463			300	μA
				DS75461, DS75463			100	μA
			V_{IL} = 0.8V	DS55462, DS55464			300	μA
				DS75462, DS75464			100	μA

Electrical Characteristics

DS55461/DS75461, DS55462/DS75462, DS55463/DS75463, DS55464/DS75464 (Notes 6 and 7) (Continued)

Symbol	Parameter	Conditions			Min	Typ	Max	Units
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5V, *(Figure 3)*					1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V, *(Figure 3)*					40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V, *(Figure 2)*				−1	−1.6	mA
I_{CCH}	Supply Current	V_{CC} = Max, Outputs High, (*Figures 4* and *5*)	V_I = 5V	DS55461/ DS75461, DS55463/ DS75463		8	11	mA
			V_I = 0V	DS55462/ DS75462		13	17	mA
				DS55464/ DS75464		14	19	mA
I_{CCL}	Supply Current	V_{CC} = Max, Outputs Low, (*Figures 4* and *5*)	V_I = 0V	DS55461/ DS75461		61	76	mA
				S55463/ DS75463		63	76	mA
			V_I = 5V	DS55462/ DS75462		65	76	mA
				DS55464/ DS75464		72	85	mA

Switching Characteristics

DS55461/DS75461, DS55462/DS75462, DS55463/DS75463, DS55464/DS75464 V_{CC} = 5V, T_A = 25°C

Symbol	Parameter	Conditions		Min	Typ	Max	Units
t_{PLH}	Propagation Delay Time, Low-To-High Level Output	$I_O \approx$ 200 mA, C_L = 15 pF, R_L = 50Ω, *(Figure 6)*	DS55461/ DS75461, DS55463/ DS75463		45	55	ns
			DS55462/ DS75462, DS55464/ DS75464		50	65	ns
t_{PHL}	Propagation Delay Time High-To-Low Level Output	$I_o \approx$ 200 mA, C_L = 15 pF, R_L = 50Ω, *(Figure 6)*	DS55461/ DS75461, DS55463/ DS75463		30	40	ns
			DS55462/ DS75462, DS55464/ DS75464		40	50	ns

3

Switching Characteristics

DS55461/DS75461, DS55462/DS75462, DS55463/DS75463, DS55464/DS75464 V_{CC} = 5V, T_A = 25°C (Continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
t_{TLH}	Transition Time, Low-To-High Level Output	$I_o \approx$ 200 mA, C_L = 15 pF, R_L = 50Ω, *(Figure 6)*	DS55461/ DS75461		8	20	ns
			DS55462/ DS75462		12	25	ns
			DS55463/ DS75463		8	25	ns
			DS55464/ DS75464		12	20	ns
t_{THL}	Transition Time, High-To-Low Level Output	$I_o = \approx$ 200 mA, C_L = 15 pF, R_L = 50Ω, *(Figure 6)*	DS55461/ DS75461		10	20	ns
			DS55462/ DS75462, DS55464/ DS75464		15	20	ns
			DS55463/ DS75463		10	25	ns
V_{OH}	High-Level Output Voltage After Switching	V_S = 30V, $I_o \approx$ 300 mA, *(Figure 7)*		V_S −10			mV

Note 1: "Absoulte Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Voltage values are with respect to network ground terminal unless otherwise specified.

Note 3: This is the voltage between two emitters of a multiple-emitter transistor.

Note 4: This is the maximum voltage which shoud be applied to any output when it is in the "OFF" state.

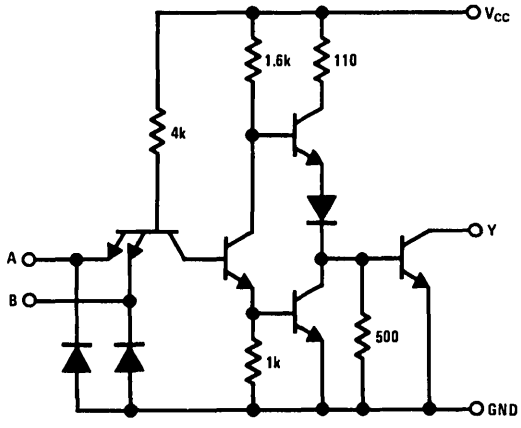
Note 5: Both halves of these dual circuits may conduct rated current simultaneously; however, power dissipation averaged over a short time interval must fall within the continuous dissipation rating.

Note 6: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS44XXX series and across the 0°C to +70°C range for the DS75XXX series. All typicals are given for V_{CC} = +5V and T_A = 25°C.

Note 7: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless othewise noted. All values shown as max or min on absolute value basis.

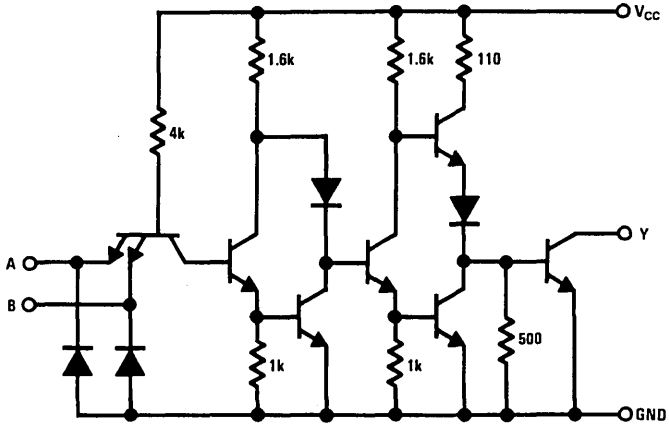
Schematic Diagrams

DS55461/DS75461



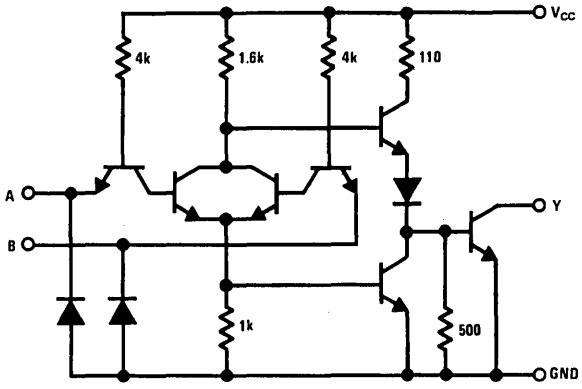
TL/F/5825–9

DS55462/DS75462



TL/F/5825–10

DS55463/DS75463



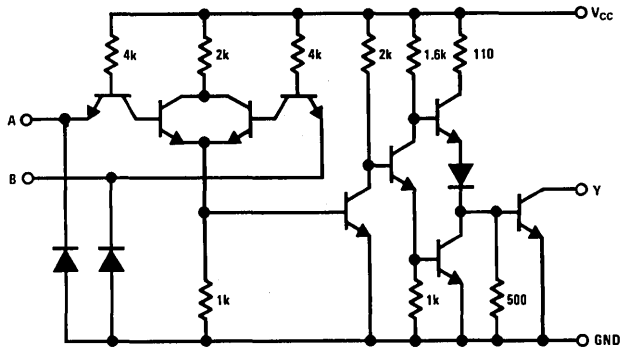
TL/F/5825–11

Resistor values shown are nominal.

3

Schematic Diagrams (Continued)

DS55464/DS75464



TL/F/5825–12

Resistor values shown are nominal.

Truth Tables (H = high level, L = low level)

DS55461/DS75461

A	B	Y
L	L	L (ON State)
L	H	L (ON State)
H	L	L (ON State)
H	H	H (OFF State)

DS55462/DS75462

A	B	Y
L	L	H (OFF State)
L	H	H (OFF State)
H	L	H (OFF State)
H	H	L (ON State)

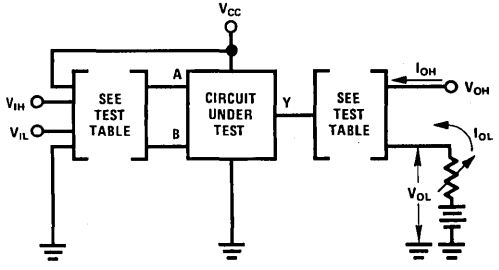
DS55463/DS75463

A	B	Y
L	L	L (ON State)
L	H	H (OFF State)
H	L	H (OFF State)
H	H	H (OFF State)

DS55464/DS75464

A	B	Y
L	L	H (OFF State)
L	H	L (ON State)
H	L	L (ON State)
H	H	L (ON State)

DC Test Circuits

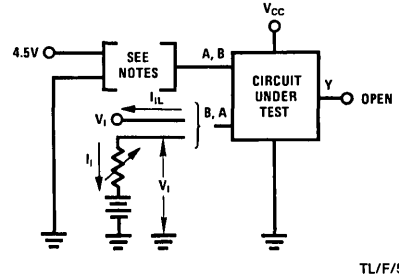


TL/F/5825–13

Circuit	Input Under Test	Other Input	Output	
			Apply	Measure
DS55461	V_{IH}	V_{IH}	V_{OH}	I_{OH}
	V_{IL}	V_{CC}	I_{OL}	V_{OL}
DS55462	V_{IH}	V_{IH}	I_{OL}	V_{OL}
	V_{IL}	V_{CC}	V_{OH}	I_{OH}
DS55463	V_{IH}	Gnd	V_{OH}	I_{OH}
	V_{IL}	V_{IL}	I_{OL}	V_{OL}
DS55464	V_{IH}	Gnd	I_{OL}	V_{OL}
	V_{IL}	V_{IL}	V_{OH}	I_{OH}

Each input is tested separately.

FIGURE 1. V_{IH}, V_{IL}, I_{OH}, V_{OL}

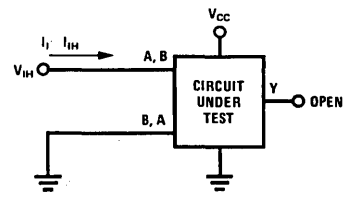


TL/F/5825–14

Note 1: Each input is tested separately.

Note 2: When testing DS55463/DS75463 and DS75464, input not under test is grounded. For all other circuits it is at 4.5V.

FIGURE 2. V_I, I_{IL}

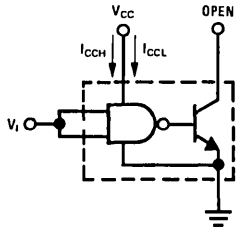


TL/F/5825–15

Each input is tested separately.

FIGURE 3. I_I, I_{IH}

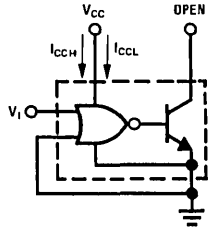
DC Test Circuits (Continued)



TL/F/5825–16

Both gates are tested simultaneously.

FIGURE 4. I_{CCH}, I_{CCL} for AND, NAND Circuits

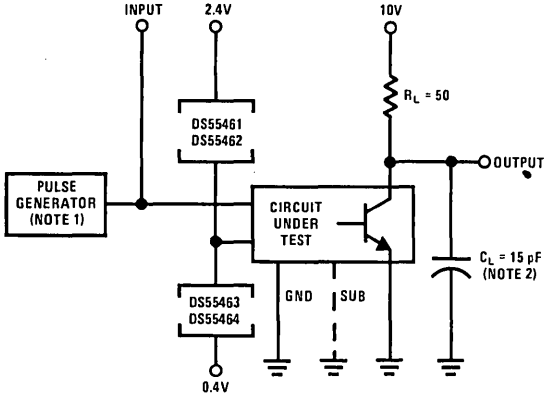


TL/F/5825–17

Both gates are tested simultaneously.

FIGURE 5. I_{CCH}, I_{CCL} for OR, NOR Circuits

Switching Characteristics

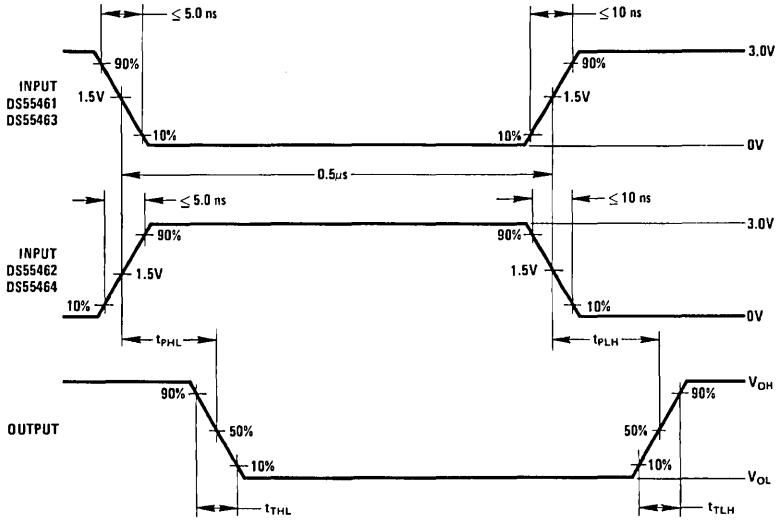


TL/F/5825–18

Note 1: The pulse generator has the following characteristics:

PRR = 1 MHz, $Z_{OUT} \approx 50\Omega$.

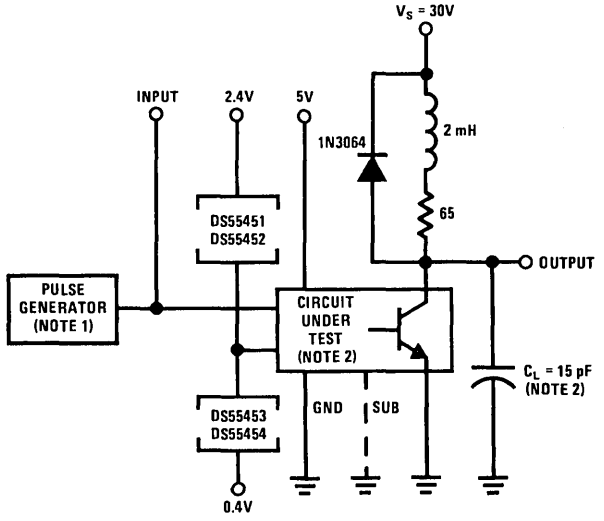
Note 2: C_L includes probe and jig capacitance.



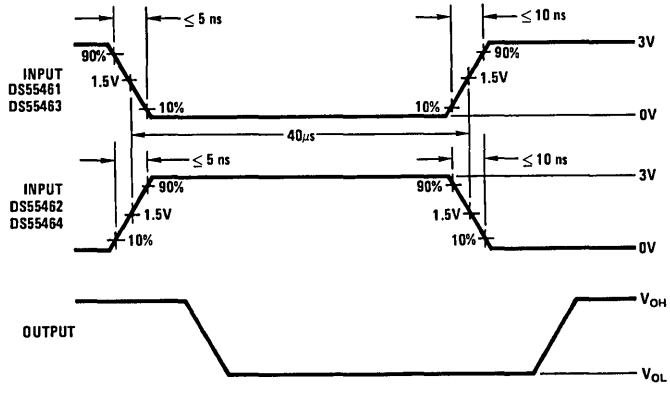
TL/F/5825–19

FIGURE 6. Switching Times of Complete Drivers

Switching Characteristics (Continued)



TL/F/5825–20



TL/F/5825–21

Note 1: The pulse generator has the following characteristics:

PRR = 1.25 kHz, $Z_{OUT} \approx 50\Omega$.

Note 2: C_L includes probe and jig capacitance.

FIGURE 7. Latch-Up Test of Complete Drivers

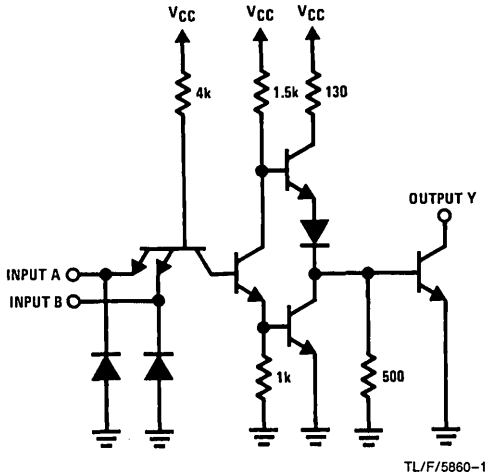
Safe Operating Areas for Peripheral Drivers

National Semiconductor Corp.
Application Note 213
Bill Fowler

Peripheral Drivers is a broad definition given to Interface Power devices. The devices generally have open-collector output transistors that can switch hundreds of milliamps at high voltage, and are driven by standard Digital Logic gates. They serve many applications such as: Relay Drivers, Printer Hammer Drivers, Lamp Drivers, Bus Drivers, Core Memory Drivers, Voltage Level Transistors, and etc. Most IC devices have a specified maximum load such as one TTL gate can drive ten other TTL gates. Peripheral drivers have many varied load situations depending on the application, and requires the design engineer to interpret the limitations of the device vs its application. The major considerations are *Peak Current, Breakdown Voltage,* and *Power Dissipation.*

OUTPUT CURRENT AND VOLTAGE CHARACTERISTICS

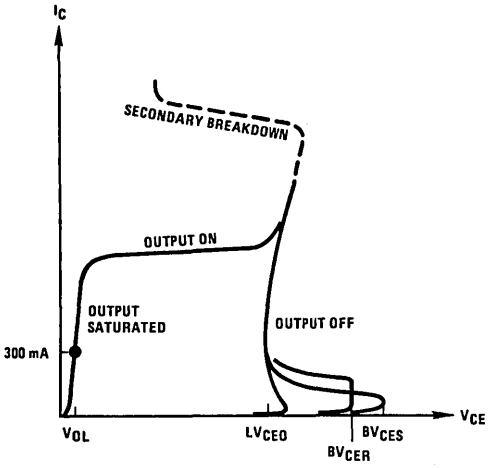
Figure 1 shows the circuit of a typical peripheral driver, the DS75451. The circuit is equivalent to a TTL gate driving a 300 mA output transistor. *Figure 2* shows the characteristics of the output transistor when it is ON and when it is OFF. The output transistor is capable of sinking more than one amp of current when it is ON, and is specified at a V_{OL} = 0.7V at 300 mA. The output transistor is also specified to operate with voltages up to 30V without breaking down, but there is more to that as shown by the breakdown voltages labeled BVCES, BVCER, and LVCEO.



TL/F/5860–1

FIGURE 1. Typical Peripheral Driver DS75451

BVCES corresponds to the breakdown voltage when the output transistor is held off by the lower output transistor of the TTL gate, as would happen if the power supply (V_{CC}) was 5V. BVCER corresponds to the breakdown voltage when the output transistor is held off by the 500 resistor, as would happen if the power supply (V_{CC}) was off (0V). LVCEO corresponds to the breakdown voltage of the output transistor if it could be measured with the base open. LVCEO can be measured by exceeding the breakdown voltage BVCES and measuring the voltage at output currents of 1 to 10 mA on a transistor curve tracer (LVCEO is sometimes measured in an Inductive Latch-Up Test). Observe that all breakdown voltages converge on LVCEO at high currents, and that destructive secondary breakdown voltage occurred (shown as dotted line) at high currents and high voltage corresponding to exceeding the power dissipation of the device. The characteristics of secondary breakdown voltage vary with the length of time the condition exists, device temperature, voltage, and current.



TL/F/5860–2

FIGURE 2. Output Characteristics ON and OFF

OUTPUT TRANSFER CHARACTERISTICS VS INDUCTIVE AND CAPACITIVE LOADS

Figure 3 shows the switching transfer characteristics superimposed on the DC characteristics of the output transistor for an inductive load. *Figure 4* shows the switching transfer characteristics for a capacitor load. In both cases in these examples, the load voltage (V_B) exceeds LVCEO. When the output transistor turns on with an inductive load the initial current through the load is 0 mA, and the transfer curve switches across to the left (V_{OL}) and slowly charges the inductor. When the output transistor turns off with an inductive load, the initial current is I_{OL}, which is sustained by the inductor and the transistor curve switches across to the right (V_B) through a high current and high voltage area which exceeds LVCEO and instead of turning off (shown as dotted line) the device goes into secondary breakdown. It is generally not a good practice to let the output transistor's voltage exceed LVCEO with an inductive load.

In a similar case with a capacitive load shown in *Figure 4*, the switching transfer characteristics rotate counter-clockwise through the DC characteristics, unlike the inductive load which rotated clockwise. Even though the switching transfer curve exceeds LVCEO, it didn't go into secondary breakdown. Therefore, it is an acceptable practice to let the output transistor voltage exceed LVCEO, but not exceed BVCER with a capacitive load.

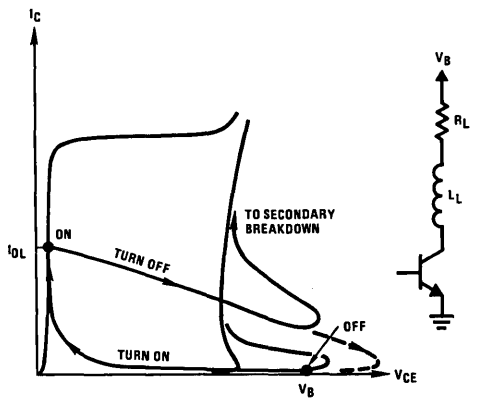


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FIGURE 3. Inductive Load Transfer Characteristics

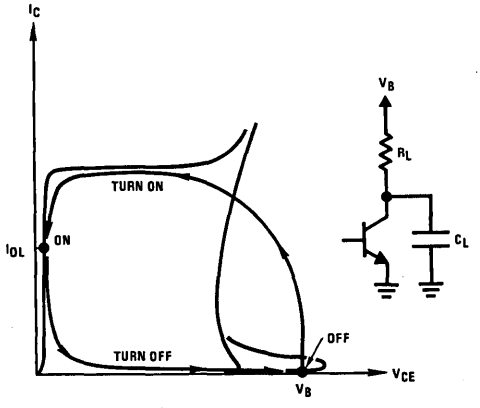

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FIGURE 4. Capacitive Load Transfer Characteristics

Figure 5 shows an acceptable application with an inductive load. The load voltage (V_B) is less than LVCEO, and the inductive voltage spike caused by the initial inductive current is quenched by a diode connected to V_B.

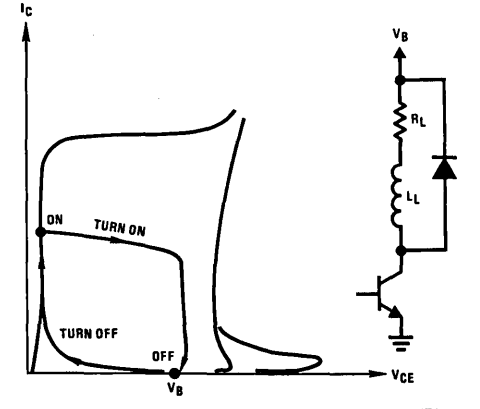

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FIGURE 5. Inductive Load Transfer Characteristics Clamped by Diode

Figure 6 shows the switching transfer characteristics of a capacitive load which leads to secondary breakdown. This condition occurs due to high sustained currents, not breakdown voltage. In this example, the large capacitor prevented the output transistor from switching fast enough through the high current and high voltage region; in turn the power dissipation of the device was exceeded and the output transistor went into secondary breakdown.

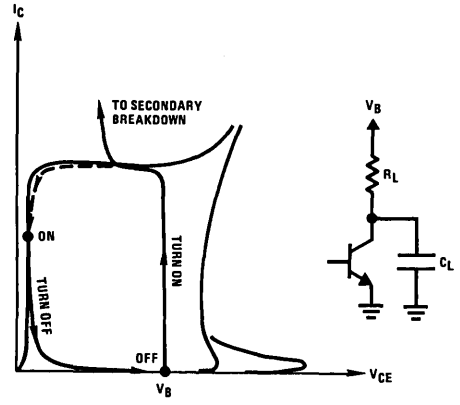

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FIGURE 6. Capacitive Load Transfer Characteristics

Figure 7 shows another method of quenching the inductive voltage spike caused by the initial inductive current. This method dampens the switching response by the addition of R_D and C_D. The values of R_D and C_D are chosen to critically dampen the values of R_L and L_L; this will limit the output voltage to $2 \times V_B$.

$$\frac{L_L}{(R_L + R_D)0} \times \sqrt{\frac{1}{L_L C_D}} \leq 0.5$$

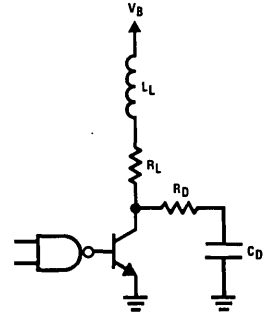

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FIGURE 7. Inductive Load Dampened by Capacitor

Figure 8 shows a method of reducing high sustaining currents in a capacitive load. R_D in series with the capacitor (C_L) will limit the switching transistor without affecting final amplitude of the output voltage, since the IR drop across R_D will be zero after the capacitor is charged.

As an additional warning, beware of parasitic reactance. If the driver's load is located some distance from the driver (as an example: on the inclosure panel or through a con-

necting cable) there will be additional inductance and capacitance which may cause ringing on the driver output which will exceed LVCEO or transient current that exceeds the sustaining current of the driver. A 300 mA current through a small inductor can cause a good size transient voltage, as compared with 20 mA transient current observed with TTL gates. For no other reason than to reduce the noise associated with these transients, it is good practice to dampen the driver's output.

In conclusion, transient voltage associated with inductive loads can damage the peripheral driver, and transient currents associated with capacitive loads can also damage the driver. In some instances the device may not exhibit failure with the first switching cycle, but its conditions from ON to OFF will worsen after many cycles. In some cases the device will recover after the power has been turned off, but its long term reliability may have been degraded.

POWER DISSIPATION

Power Dissipation is limited by the IC Package Thermal Reactance and the external thermal reactance of the environment (PC board, heat sink, circulating air, etc.). Also, the power dissipation is limited by the maximum allowable junction temperature of the device. There are two contributions to the power: the internal bias currents and voltage of the device, and the power on the output of the device due to the Driver Load.

POWER LIMITATIONS OF PACKAGE

Figure 9 shows the equivalent circuit of a typical power device in its application. Power is shown equivalent to electrical current, thermal resistance is shown equivalent to electrical resistance, the electrical reactance C and L are equivalent to the capacity to store heat, and the propagation delay through the medium. There are two mediums of heat transfer: conduction through mass and radiant convection. Convection is insignificant compared with conduction and isn't shown in the thermal resistance circuits. From the point power is generated (device junction) there are three possible paths to the ultimate heat sink: 1) through the device leads; 2) through the device surface by mechanical connection; and 3) through the device surface to ambient air. In all cases, the thermal paths are like delay lines and have a corresponding propagation delay. The thermal resistance is proportional to the length divided by the cross sectional area of the material. The Thermal Inductance is proportional to the length of the material (copper, molding compound, etc.) and inversely proportional to the cross sectional area. The thermal capacity is proportional to the volume of the material.

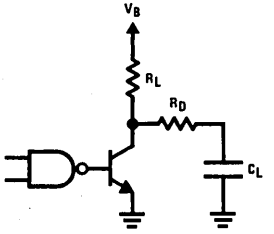

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FIGURE 8. Capacitive Load with Current Limiting Resistor

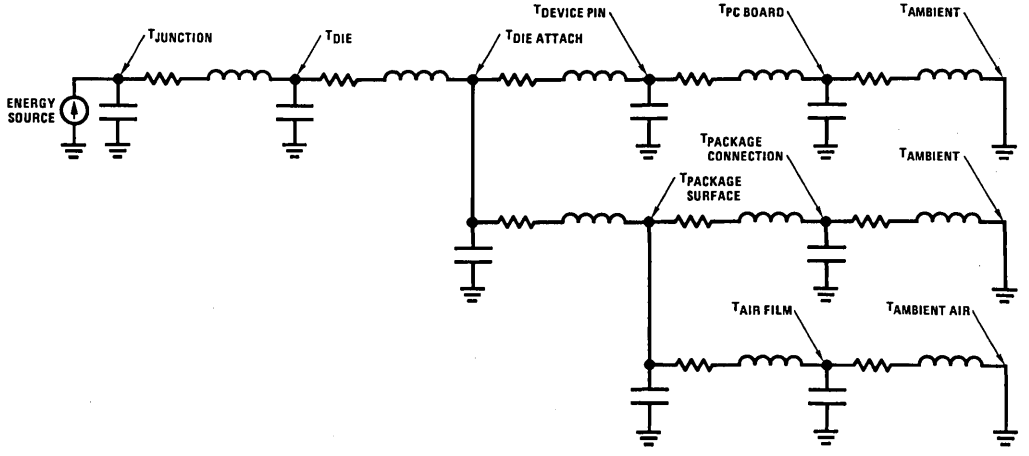

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FIGURE 9. Thermal Reactance from Junction to Ambient

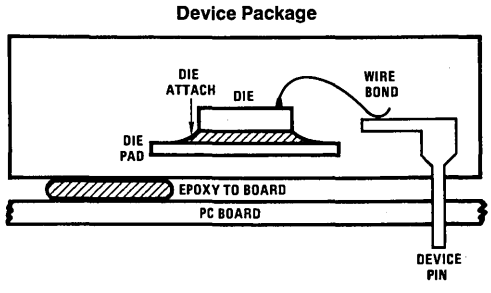

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FIGURE 10. Components of Thermal Reactance for a Typical IC Package

National Semiconductor specifies the thermal resistance from device junction through the device leads soldered in a small PC board, measured in one cubic foot of still air. *Figure 11* shows the maximum package power rating for an 8 pin Molded, an 8 pin Ceramic, 14 pin Molded and a 14 pin Ceramic package. The slope of the line corresponds to thermal resistance ($\phi_{JA} = \Delta P/\Delta T$).

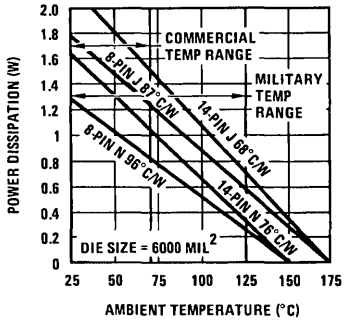

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FIGURE 11. Maximum Package Power Rating

The maximum allowable junction temperature for ceramic packages is 175°C; operation above this temperature will reduce the reliability and life of the device below an acceptable level. At a temperature of 500°C the aluminum metallization paths on the die start to melt. The maximum allowable junction temperature for a molded device is 150°C, operations above this may cause the difference in thermal expansion between the molding compound and package lead frame to sheer off the wire bonds from the die to the package lead. The industry standard for a molded device is 150°C, but National further recommends operation below 135°C if the device in its application will encounter a lot of thermal cycling (such as powered on and off over its life).

The way to determine the maximum allowable power dissipation from *Figure 11*, is to project a line from the maximum ambient temperature (T_A) of the application vertically (shown dotted in *Figure 12*), until the line intercepts the diagonal line of the package type, and then project a line (shown dotted) horizontally until the line intercepts the Power Dissipation Axis (P_{MAX}).

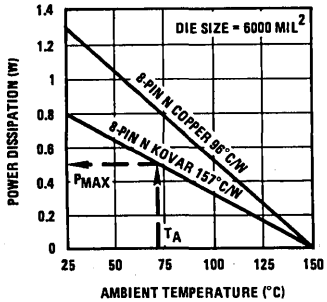

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FIGURE 12. Maximum Package Rating Copper vs Kovar Lead Frame Packages

Figure 11 shows that 14 pin packages have less thermal resistance than 8 pin packages; which should be expected since it has more pins to conduct heat and has more surface area. Something that may not be expected is that the Thermal Resistance of the molded devices is comparable to the ceramic devices. The reason for the lower thermal resistance of the molded devices is the Copper lead frame, which is a better thermal conductor than the Kovar lead frame of the ceramic package. Almost all the peripheral drivers made by National Semiconductor are constructed with Copper lead frames (refer to ϕ_{JA} on the specific devices data sheet). The difference between the thermal resistance of Copper and Kovar in a molded package is shown in *Figure 12*.

Another variance in thermal resistance is the size of the IC die. If the contact area to the lead frame is greater, then the thermal resistance from the Die to the Lead Frame is reduced. This is shown in *Figure 13*. The thermal resistance shown in *Figure 11* corresponds to die that are 6000 mil^2 in area.

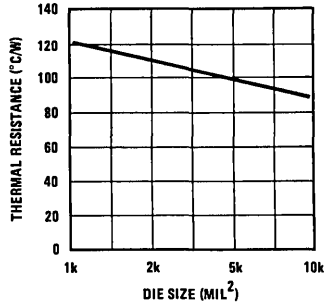

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FIGURE 13. Thermal Resistance vs Die Size

In most applications the prime medium for heat conduction is through the device leads to the PC board, but the thermal resistance can be significantly improved by cooling air driven across the surface of the package. The conduction to air is limited by a stagnant film of air at the surface of the package. The film acts as an additional thermal resistance. The thickness of the film is proportional to its resistance. The thickness of the film is reduced by the velocity of the air

across the package as shown in *Figure 14*. In most cases, the thermal resistance is reduced 25% to 250 linear feet/min, and 30% at 500 linear feet/min, above 500 linear feet/min the improvement flattens out.

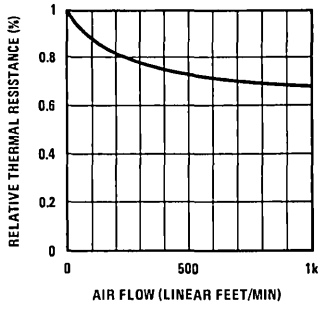

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FIGURE 14. Thermal Resistance vs Air Velocity

The thermal resistance can also be improved by connecting the package to the PC board copper or by attaching metal wings to the package. The improvement by these means is outside the control of the IC manufacturer, but is available from the manufacturer of the heat sink device. If the IC is mounted in a socket rather than soldered to a PC board, the thermal resistance through the device leads will worsen. In most cases, the thermal resistance is increased by 20%; again this is a variable subject to the specific socket type.

The maximum package rating shown in this note corresponds to a 90% confidence level that the package will have thermal resistance equal to or less than the value shown. The thermal resistance varies ±5% about the mean due to variables in assembly and package material.

CALCULATIONS OF POWER DISSIPATION

Most IC devices (such as T^2L) operate at power levels well below the device package rating, but peripheral drivers can easily be used at power levels that exceed the package rating unknowingly, if the power dissipation isn't calculated. As an example, the DS3654 Ten Bit Printer Driver could dissipate 3 watts (DC and, even more AC), and it is only in a 0.8 watt package. In this example, the device would be destroyed in moments, and may even burn a hole in the PC board it is mounted on. The DS3654 data sheet indicated that the 10 outputs could sink 300 mA with a V_{OL} of 1 volt, but it wasn't intended that all the outputs would be sinking this current at the same time, and if so, not for a long period. The use of the DS3654 requires that the power be calculated vs the duty cycle of the outputs.

The DC power dissipation is pretty obvious, but in another example, a customer used the DS3686 relay driver to drive 6.5h inductive load. The DS3687 has an internal clamp network to quench the inductive back swing at 60V. At 5 Hz the device dissipates 2 watts, with transient peaks up to 11 watts. After 15 minutes of operation, the driver succumbs to thermal overload and becomes non-functional. The DS3687 was intended for telephone relay, which in most applications switches 20 times a day.

Peripheral driver will dissipate peak power levels that greatly exceed the average DC power. This is due to the capacity of the die and package to consume the transient energy while still maintaining the junction temperature at a safe level. This capacity is shown as a capacitor in *Figure 9*. In the lab (under a microscope) a device may be observed to glow orange around the parameter of the junction under excessive peak power without damage to the device. *Figure 15* shows a plot of maximum peak power vs applied time for the DS3654, and the same information plotted as energy vs applied time. To obtain these curves, the device leakage current when it switches off was used to monitor device limitation. Note in *Figure 15* there is a transition in the curve about 10 μs. At this point, the thermal capacity of the die has been exceeded. The thermal delay to the next thermal capacity (the package) was too long, and limited the peak power. These levels are not suggested operating levels, but an example of a Peripheral Driver to handle peak transient power.

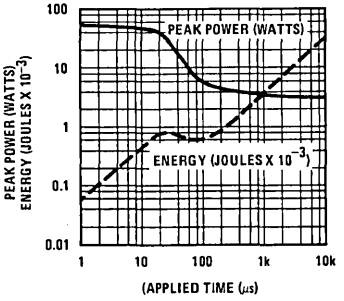

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FIGURE 15. Peak Power and Energy vs the Period of Time the Power was Applied

To calculate power dissipation, the only information available to the design engineer is the parametric limits in the device data sheet, and the same information about the load reactance. If the calculations indicate the device is within its limits of power dissipation, then using those parametric limits is satisfactory. If the calculation of power dissipation is marginal, the parametric limits used in the calculations might be worst case at low temperature instead of high temperature due to a positive temperature coefficient (T_C) of resistance. IC resistors and resistors associated with the load generally have a positive T_C. On the other hand, diodes and transistor emitter base voltages have a negative T_C; which may in some circuits negate the effect of the resistors T_C. Peripheral output transistors have a positive T_C associated with V_{OL}; while output Darlington transistors have a negative T_C at low currents and may be flat at high currents. *Figure 16* shows an example of power dissipation vs temperature; note that the power dissipation at the application's maximum temperature (T_A) was less than the power dissipation at lower temperatures. Since maximum junction temperature is the concern of the calculation, then maximum ambient temperature power should be used. The junction temperature may be determined by projecting a line (shown dotted in *Figure 16*), with a slope proportional to ϕ_{JA} back to the horizontal axis (shown as T_J). If the point is below the curve then T_J will be less than 150°C. T_J must not exceed the maximum junction temperature for that package type. In this example, T_J is less than 150°C as required by a molded package. To calculate the power vs temperature, it is necessary to characterize the device parameters vs temperature. Unfortunately, this information is not always provided by IC manufacturers in the device data sheets. A method to calcu-

late I_{CC} vs temperature is to measure a device, then normalize the measurements vs the typical value for I_{CC} in the data sheet, then worst case the measurements by adding 30%. Thirty percent is normally the worst-case resistor tolerance that IC devices are manufactured to.

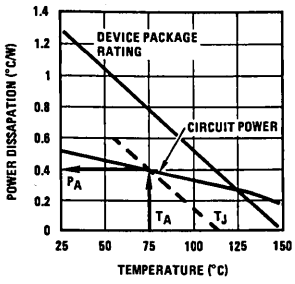

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FIGURE 16. IC Power Dissipation vs Temperature

CALCULATION OF OUTPUT POWER WITH AN INDUCTIVE LOAD

For this example, the device output circuit is similar to the DS3654 (10-Bit Printer Solenoid Driver) and the DS3686 and DS3687 (Telephone Relay Driver) as shown in *Figure 17*. Special features of the circuit type are the Darlington output transistors Q1 and Q2 and the zener diode from the collector of Q2 to the base of Q2. The Darlington output requires very little drive from the logic gate driving it and in turn dissipates less power when the output is turned ON and OFF, than a single saturating transistor output would. The zener diode (D_Z) quenches the inductive backswing when the output is turned OFF.

Device and Load Characteristics Used for Power Calculation

V_{OL}	Output Voltage ON	1.5V
V_C	Output Clamp Voltage	65V
V_B	Load Voltage	30V
R_L	Load Resistance	120Ω
L_L	Load Inductance	5h
T_{ON}	Period ON	100 ms
T_{OFF}	Period OFF	100 ms
T	Total Period	200 ms

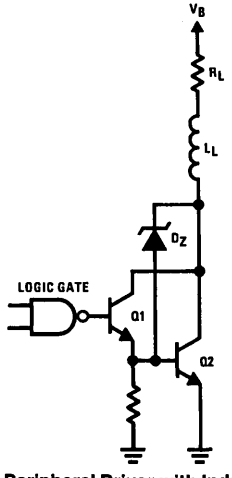

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FIGURE 17. Peripheral Driver with Inductive Load

Refer to *Figure 18* voltage and current waveforms corresponding to the power dissipation calculated for this example of an inductive load.

P_{ON} = Average power dissipation in device output when device is ON during total period (T)

$$\tau = \frac{L_L}{R_L} = \frac{5h}{120\Omega} = 41.7\ ms$$

$$I_L = \frac{V_B - V_{OL}}{R_L} = \frac{30 - 1.5}{120} = 237.5\ mA$$

$$I_P = I_L (1 - e^{-T_{ON}/\tau})$$

$$I_P = 237.5\ mA\ (1 - e^{-100\ ms/41.7\ ms})$$

$$I_P = 215.9\ mA$$

$$P_{ON} = V_{OL} \times I_L \times \frac{T_{ON}}{T}\left[1 - \int_0^{T_{ON}} \frac{e^{-t/\tau}\,dt}{T_{ON}}\right]$$

$$P_{ON} = V_{OL} \times I_L \times \frac{T_{ON}}{T}\left[1 - \frac{\tau}{T_{ON}}(1 - e^{-T_{ON}/\tau})\right]$$

$$P_{ON} = 1.5 \times 237.5\ mA \times \frac{100}{200}\left[1 - \frac{41.7}{100}(1 - e^{-100/41.7})\right]$$

$$P_{ON} = 110.6\ mW$$

P_{OFF} = Average power dissipation in device output when device is OFF during total period (T)

$$I_R = \frac{V_C - V_B}{R_L} = \frac{65 - 30}{120\Omega} = 291.7\ mA$$

$$t_x = \tau\, \ell n \left(\frac{I_P + I_R}{I_R}\right)$$

$$t_x = 41.7\ ms\ \ell n \left(\frac{215.9 + 291.7}{291.7}\right) = 23.1\ ms$$

$$P_{OFF} = V_C \times \frac{t_x}{T}\left[(I_P + I_R)\int_0^{t_x} \frac{e^{-t/\tau}\,dt}{t_x} - I_R\right]$$

$$P_{OFF} = V_C \times \frac{t_x}{T}\left[(I_P + I_R) \times s\frac{\tau}{t_x}(1 - e^{-t_x/\tau}) - I_R\right]$$

$$P_{OFF} = 65 \times \frac{23.1}{200}\left[(215.9\ mA + 291.7\ mA)\frac{41.7}{23.1}\right.$$

$$\left.(1 - e^{-23.1/41.7}) - 291.7\ mA\right]$$

$$P_{OFF} = 736\ mW$$

P_O = Average power dissipation in device output

$$P_O = P_{ON} + P_{OFF} = 110.6 + 736 = 846.6\ mW$$

In the above example, driving a 120Ω inductive load at 5 Hz, the power dissipation exceeded a more simple calculation of power dissipation, which would have been:

$$P_O = \frac{V_{OL}(V_B - V_{OL})}{R_L} \times \frac{T_{ON}}{T}$$

$$P_O = \frac{1.5\,(30 - 1.5)}{120} \times \frac{100\ ms}{200\ ms} = 182.5\ mW$$

An error 460% would have occurred by not including the reactive load. The total power dissipation must also include other outputs (if the device has more than one output), and the power dissipation due to the device power supply currents. This is an example where the load will most likely exceed the device package rating. If the load is fixed, the power can be reduced by changing the period (T) and duty rate (T_{ON}/T_{OFF}).

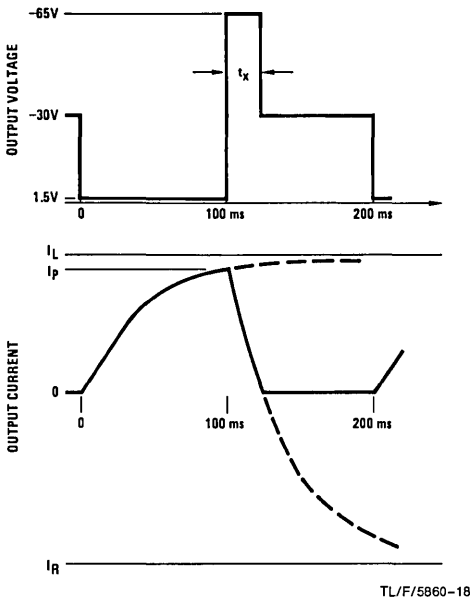

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FIGURE 18. Voltage and Current Waveforms Corresponding to Inductive Load

CALCULATION OF OUTPUT POWER WITH AN INCANDESCENT LAMP

An incandescent lamp is equivalent to a reactive load. The reactance is related to the period of time required to heat the lamp and the filaments positive temperature coefficient of resistance. *Figure 19* shows the transient response for a typical lamp used on instrument panels, and the equivalent electrical model for the lamp. Much like IC packages the lamp has a thermal circuit and its associated propagation delay. This lamp filament has an 8 ms time constant, and a longer 250 ms time constant from the lamp body to ambient. The DC characteristics are shown in *Figure 20*. Note the knee in the characteristics at 2 volts; this is where power starts to be dissipated in the form of light. This subject is important, since more peripheral drivers are damaged by lamps than any other load.

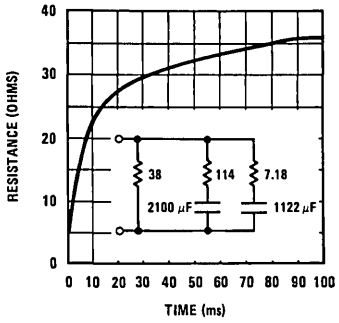

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FIGURE 19. Transient Response of an Incandescent Lamp

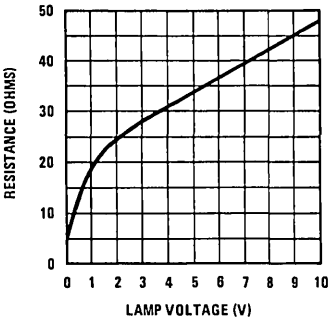

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FIGURE 20. DC Characteristics of an Incandescent Lamp

Figure 21 shows the transient response of a driver similar to a DS75451 driving the lamp characterized in *Figures 19* and *20*. The equivalent load doesn't include the reactance of the lamp base to ambient, which has a 250 ms time constant, since 10 ms to an IC is equivalent to DC. The peak transient current was 1 amp, settling to 200 ms, with an 8 ms time constant. Observe the peak current is clamped at 1 amp, by the sinking ability of the driver; otherwise the peak current may have been 1.2 amps. The DS75451 is only rated at 300 mA, but it is reasonable to assume it could sink 1 amp because of the designed force β required for switching response and worst case operating temperature.

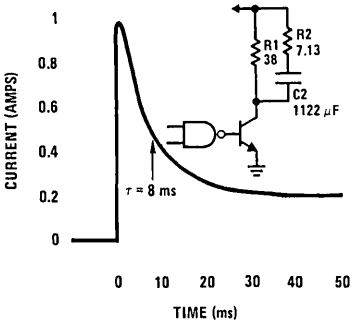

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FIGURE 21. Transient Incandescent Lamp Current

Calculation of the energy dissipated by a peripheral driver for the transient lamp current shown in *Figure 21* is shown above, and the plot of energy vs time is shown in *Figure 22*. *Figure 22* also includes as a reference the maximum peak energy from *Figure 15*. It can be seen from *Figure 22* that in this example there is a good safety margin between the lamp load and the reference max peak energy. If there were more drivers than one per package under the same load, the margin would have been reduced. Also, if the peripheral driver couldn't saturate because it couldn't sink the peak transient lamp current, then the energy would also reduce the margin of safe operation.

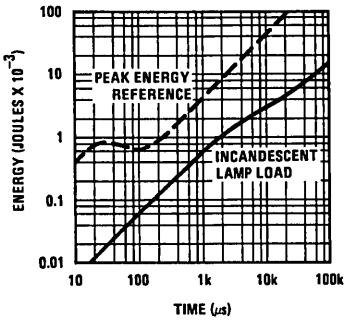

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FIGURE 22. Energy vs Time for a Peripheral Driver with an Incandescent Lamp Load

CALCULATION OF ENERGY IN AN INCANDESCENT LAMP

$$\text{Energy} = \int_0^t V_{OL}\,(I_{R1} + I_{R2})\,dt$$

$$i_{R1} = \frac{V_B - V_{OL}}{R1} = I_{R1}$$

$$i_{R2} = \left(\frac{V_B - V_{OL}}{R2}\right) e^{-t/\tau}$$

$$= I_{R2}\, e^{-t/\tau} \quad \tau = R2C2$$

$$\text{Energy} = \int_0^t V_{OL}\,(I_{R1} + I_{R2}\, e^{-t/\tau})\,dt$$

$$= V_{OL}\,[I_{R1}t + I_{R2}\tau\,(i - e^{-t/\tau})]$$

Given: $V_{OL} = 0.6V$

$I_{R1} = 0.2$ Amps

$I_{R1} + I_{R2} = 1$ Amp

A common technique used to reduce the 10 to 1 peak to DC transient lamp current is to bias the lamp partially ON, so the lamp filament is warm. This can be accomplished as shown in *Figure 23*. From *Figure 20* it can be seen that the lamp resistance at 0V is 5.7Ω, but at 1V the resistance is 18Ω. At 1V the lamp dosen't start to emit light. Using a lamp resistance of 100Ω and lamp voltage of 1V, R_B was calculated to be approximately 100Ω. This circuit will reduce the peak lamp current from 1 amp to 316 mA.

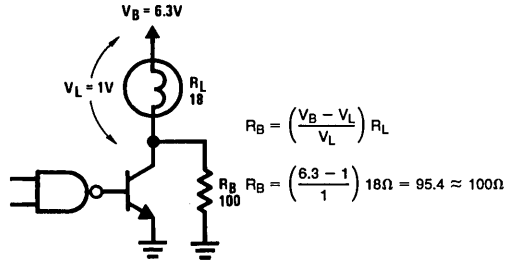

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FIGURE 23. Circuit Used to Reduce Peak Transient Lamp Current

PERIPHERAL DRIVER SECTION

National Semiconductor has a wide selection of peripheral drivers as shown in this section's guide. The DS75451, DS75461, DS3631 and the DS3611 series have the same selection of logic function in an 8-pin package. The DS75461 is a high voltage selection of the DS75451 and may switch slower. The DS3611 and DS3631 are very high voltage circuits and were intended for slow relay applications. The DS3680, DS3686, and DS3687 were intended for 56V telephone relay applications. The DS3654 contains a 10-bit shift register followed by ten 250 mA clamped drivers. The DS3654 was intended for printer solenoid applications.

High current and high voltage peripheral drivers find many applications associated with digital systems, and it is the intention of the application note to insure that reliability and service life of peripheral drivers equal or exceed the performance of the other logic gates made by National.

For additional information, please contact the Interface Marketing Department at National or one of the many field application engineers world-wide.

Section 4

Display Controllers/Drivers

Section Contents

*Also available processed to various Military screening levels. Refer to Section 9.

Display Controllers/Drivers

DP8350 Series of CRT Display Controllers

The DP8350 Series CRT Controllers are designed to be dedicated CRT display refresh circuits. All necessary video timing signals are provided by the DP8350, including the high-speed dot timing which is generated from an on-chip crystal oscillator. This is possible because of its bipolar processing which allows Schottky circuitry to be used for high speed logic and analog I/O functions while I^2L circuitry is used for lower speed internal logic functions.

A typical DP8350 series application is a data terminal with a raster scan monitor. The DP8350 can be used in systems with or without line buffers, using character ROMs or DM86S64 latch/ROM/shift register circuits. Graphics are possible using either character generator or memory mapped graphics techniques.

The DP8350 series CRT controllers are mask programmable. Mask programmibility simplifies the function and reduces external hardware and software overhead. A list of programmable variables follows.

Mask programmability is an advantage as long as the screen format does not need to change and an existing part (ROM variation) can be used, or production quantities justify a new ROM variation. In addition to the ROM programmable variables, three on-chip registers provide for external control of the row starting address, cursor address and top-of-page address.

Standard parts are the DP8350, DP8352 and DP8353 whose sync signals are compatible with Ball Brothers TV-12 or TV-110, RS170 and Motorola M3000 series respectively.

Display Drivers

Simply stated, a display driver is an element which is used to amplify the output of a logic device in order to activate a visual display. Specific display drivers are designed to activate common anode light emitting diodes (LEDs), common cathode LEDs, gas discharge tubes and vacuum fluorescent displays.

National Semiconductor produces a variety of display drivers for all the major display technologies. Refer to the selection guide and application notes within this section.

DP8350 CRT CONTROLLER SERIES SELECTION GUIDE

Item No.	Parameter		DP8350 Value		DP8352 Value		DP8353 Value	
1	Character Font Size (Reference Only)	Dots per Character (Width)	(5)		(7)		(7)	
2		Scan Lines per Character (Height)	(7)		(9)		(9)	
3	Character Field Cell Size	Dots per Character (Width)	7		9		9	
4		Scan Lines per Character (Height)	10		12		12	
5	Number of Video Characters per Row		80		32		80	
6	Number of Video Character Rows per Frame		24		16		25	
7	Number of Video Scan Lines (Item 4 × Item 6)		240		192		300	
8	Frame Refresh Rate (Hz)		f1 = 60	f0 = 50	f1 = 60	f0 = 50	f1 = 60	f0 = 50
9	Delay after Vertical Blank Start to Start of Vertical Sync (Number of Scan Lines)		4	30	27	53	0	32
10	Vertical Sync Width (Number of Scan Lines)		10	10	3	3	3	3
11	Interval Between Vertical Blank Start and Start of Video (Number of Scan Lines of Video Blanking)		20	72	68	120	20	84
12	Total Scan Lines per Frame (Item 7 + Item 11)		260	312	260	312	320	384
13	Horizontal Scan Frequency (Line Rate) (Item 8 × Item 12)		15.6 kHz		15.6 kHz		19.20 kHz	
14	Number of Character Times per Scan Line		100		50		102	
15	Character Clock Rate (Item 13 × Item 14)		1.56 MHz		0.78 MHz		1.9584 MHz	
16	Character Time (1 ÷ Item 15)		641 ns		1282 ns		510.6 ns	
17	Delay after Horizontal Blank Start to Horizontal Sync Start		0		6		5	
18	Horizontal Sync Width (Character Times)		43		4		9	
19	Dot Frequency (Item 3 × Item 15)		10.92 MHz		7.02 MHz		17.6256 MHz	
20	Dot Time (1 ÷ Item 19)		91.6 ns		142.4 ns		56.7 ns	
21	Vertical Blanking Output Stop before Start of Video (Number of Scan Lines)		1		0		1	
22	Cursor Enable on All Scan Lines of a Row? (Yes or No)		Yes		Yes		Yes	
23	Does the Horizontal Sync Pulse Have Serrations during Vertical Sync? (Yes or No)		No		Yes		No	
24	Width of Line Buffer Clock Logic "0" State within a Character Time (Number of Dot Time Increments)		4		5		5	
25	Serration Pulse Width, if Used (Character Times)		—		4		—	
26	Horizontal Sync Pulse Active State Logic Level (1 or 0)		1		0		1	
27	Vertical Sync Pulse Active State Logic Level (1 or 0)		0		0		1	
28	Vertical Blanking Pulse Active State Logic Level (1 or 0)		1		1		1	

Video Monitor Format: Ball Brothers TV-12, TV-120 or Equivalent. (DP8350)

Video Monitor Format: RS-170-Compatible (Standard American TV). (DP8352)

Video Monitor Format: Motorola M3003 or Equivalent. (DP8353)

DP8350 SERIES OPTION FORMAT ABSTRACT

Device/Option Designation	Status	Video Format (Char x Row)	Field Size (Dot x Line)	Dot Rate (MHz)	Character Rate (MHz)	Horizontal Rate Scan (kHz)	Frame Rate Refresh (Hz) f_1/f_0
DP8350	STD	80 x 24	7 x 10	10.92000	1.5600	15.60	60/50
DP8352	STD	32 x 16	9 x 12	7.02000	0.7800	15.60	60/50
DP8353	STD	80 x 25	9 x 12	17.62560	1.9600	19.20	60/50
A	STD	80 x 25	9 x 14	19.98000	2.2200	22.20	60/50
B	STD	80 x 25	10 x 12	19.44000	1.9440	19.44	60/50
C	STD	80 x 25	8 x 9	12.48000	1.5600	15.60	60/50
D	STD	80 x 25	11 x 16	25.00000	2.2727	22.065	51/51
E	STD	80 x 25	9 x 16	23.02344	2.5600	25.08	50/60
F	STD	80 x 33	11 x 13	25.00000	2.2727	22.065	48.5/48.5
G	STD	80 x 44	11 x 10	25.00000	2.2727	22.065	48/48
H	STD	80 x 24	7 x 10	10.92000	1.5600	15.60	60/50
I	STD	80 x 26	9 x 15	25.77150	2.8600	24.90	60/50
J	STD	80 x 25	10 x 15	25.00000	2.5000	23.81	60/50
K	STD	80 x 25	7 x 10	12.24720	1.7496	16.20	60/50

LED DISPLAY SEGMENT DRIVERS

Device Number		Drivers/ Package	I_O/Segment (mA)		V_{MAX} (V)		Comments	Page No.
0°C to +70°C	−55°C to +125°C		Sink* (Common Anode)	Source (Common Cathode)	Input	Supply		
DS75491		4	50	50	15	10		4-110
DS8859A		6	32		5.5	7	Programmable Output, Active High Latch	4-122
DS8867		8		18	10	7	Constant Current Output	4-128
DS8654		8		50	36	36		4-115

*Digit drivers with output sink capability may be used to drive segments of "common anode" displays

LED DISPLAY DIGIT DRIVERS

Device Number		Drivers/ Package	I_O/Digit (mA)		V_{MAX} (V)		Comments	Page No.
0°C to +70°C	−55°C to +125°C		Sink (Common Anode)	Source (Common Cathode)	Input	Supply		
DS75491		4		50	10	10		4-110
DS75494	DS55494	6	150		10	10	Enable Control	4-113
DS75492		6	250		10	10		4-110
DS8870		6	350		10	10	DS75492 Pinout, Darlington Output	4-130
DS8863		8	500		15	10		4-125
DS8963			500		23	18		4-125
DS8654				50	36	36		4-115
DS8874			50		10	10	Serial Shift Register Input	4-132
DS8973			100		10	10	3-Cell Operation—Low Battery Indicator	4-149
DS3654		10	400		9.5	45	Serial Input	3-17

GAS DISCHARGE DISPLAY DRIVERS

Device Number		Device Type	Drivers/ Package	Comments	Page No.
0°C to +70°C	−55°C to +125°C				
DS8880	DS7880	Cathode Drivers	7	BCD to 7-Segment	4-134
DS8884A			7	BCD to 7-Segment with Comma and DP	4-142
DS8897A	DS7897A		8	Active Low Inputs	4-145

VACUUM FLUORESCENT DISPLAY DRIVERS

Device Number		Device Type	Drivers/ Package	Comments	Page No.
0°C to +70°C	−55°C to +125°C				
DS8654		Ground Driver (segments)	8	7-Segment plus DP	4-115
DS8654		Anode Driver	8		4-115
DS8881		(digit)	16	4 Line BCD Input	4-138

PRINTER DRIVERS

Device Number		Device Type	Drivers/ Package	Description	Page No.
0°C to +70°C	−55°C to +125°C				
DS3680		Mechanical Printer		Relay Hammer	3-32
DS3654				10 Hammer Serial Input Driver	3-17
DS8654				8-Digit Driver	4-115

National Semiconductor Corporation

DP8350 Series CRT Controllers

General Description

The DP8350 Series of CRT Controllers are single-chip bipolar (I^2L technology) circuits in a 40-pin package. They are designed to be dedicated CRT display refresh circuits. Three standard products are available, designated DP8350, DP8352, DP8353. Custom devices, however, are available in a broad range of mask programmable options.

The CRT Controller (CRTC) provides an internal dot rate crystal controlled oscillator for ease of system design. For systems where a dot rate clock is already provided, an external clock may be inputted to the CRTC. In either case system synchronization is made possible with the use of the buffered Dot Rate Clock Output.

The DP8350 Series has 11 character generation related timing outputs. These outputs are compatible for systems with or without line buffers, using character ROMs, or DM86S64-type latch/ROM/shift register circuits.

12 bits (4k) of bidirectional TRI-STATE® character memory addresses are provided by the CRTC for direct interface to character memory.

Three on-chip registers provide for external loading of the row starting address, cursor address, and top-of-page address.

A complete set of video outputs is available including cursor enable, vertical blanking, horizontal sync, and vertical sync.

The DP8350 Series CRTC provides for a wide range of programmability using internal mask programmable ROMs:

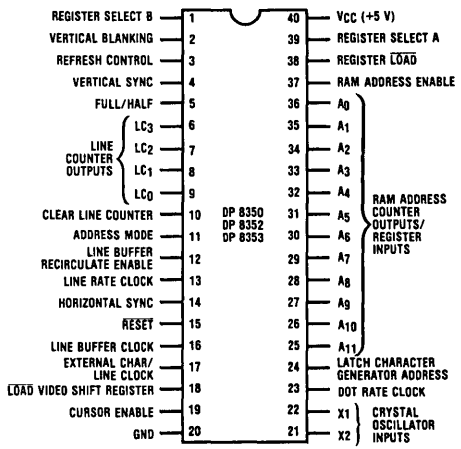
- Character Field (both number of dots/character and number of scan lines/character)
- Characters per Row
- Character Rows per Video Frame
- Format of Video Outputs

The CRTC also provides system sync and program inputs including Refresh Control, Reset, and Address Mode.

Features

- Internal crystal controlled dot rate oscillator
- External dot rate clock input
- Buffered dot rate clock output
- Timing pulses for character generation
- Character memory address outputs (12 bits)
- Internal cursor address register
- Internal row starting address register
- Internal top-of-page address register (for scrolling)
- Programmable horizontal and vertical sync outputs
- Programmable cursor enable output
- Programmable vertical blanking output
- 2 programmable refresh rates, pin selectable
- Programmable characters/row (128 max.)
- Programmable character field size (up to 16 dots x 16 scan line field size)
- Programmable scan lines/frame (512 max.)
- Programmable character rows/frame
- Single +5V power supply
- Inputs and outputs TTL compatible
- Direct interface with DM86S64 character generator
- Ease of system design/application

Connection Diagram



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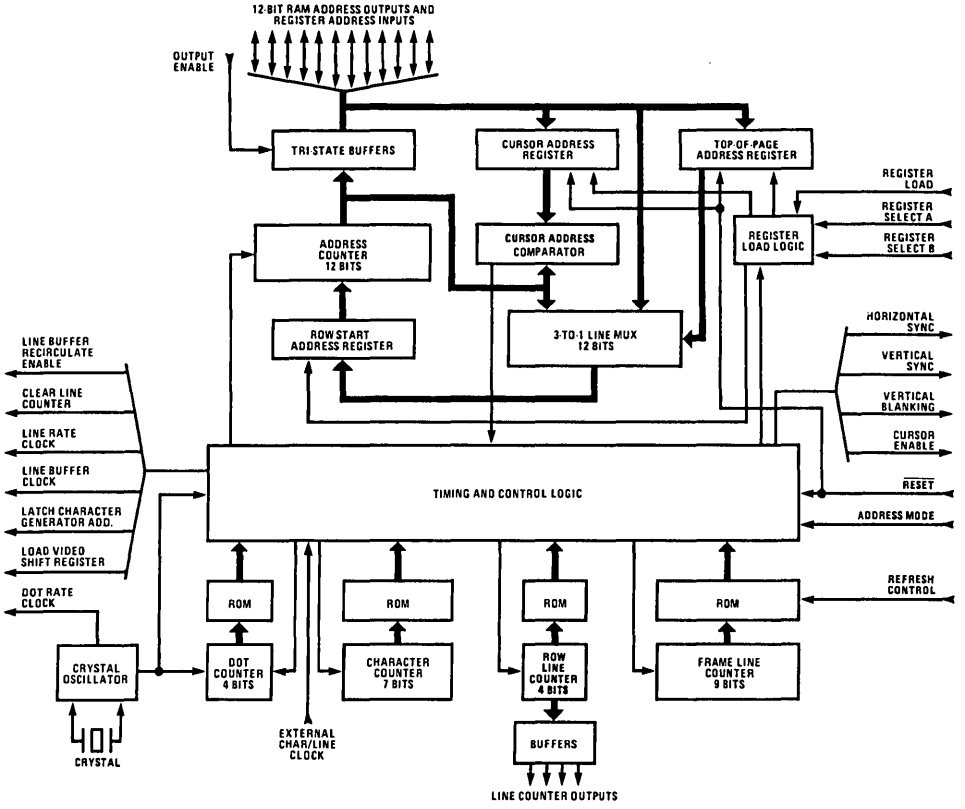
Order Number DP8350J or N
See NS Package Number J40A or N40A

Block Diagram



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The Video Display

Discussion of the CRT Controller necessitates an understanding of the video display as presented by a raster scan monitor. The resolution of the data displayed on the monitor screen is a function of the dot size. As shown in *Figure 1*, the dot size is determined by the frequency of the system dot clock. The visible size of the dot can be modified to less than 100% by external gating of the serial video data. The CRT Controller organizes the dots into cell groupings that define video rows. These cells are accessed by a specific horizontal address output (4096 maximum) and are resolved by a row scan-line-counter output (16 maximum) as shown in *Figure 2*. The relation of the video portion of a frame to the horizontal blanking and vertical blanking intervals is shown in *Figure 3* in a two-dimensional format.

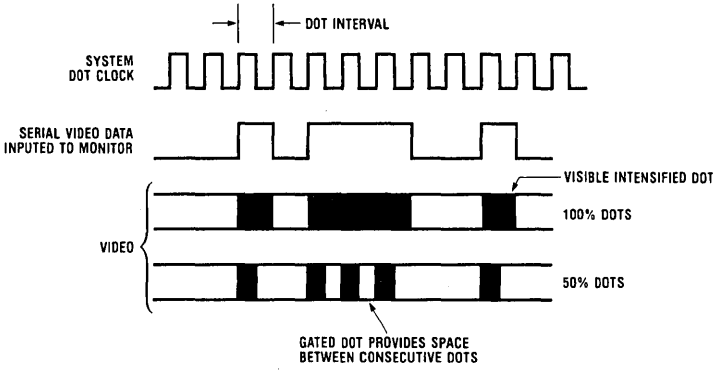

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FIGURE 1. Dot Definition

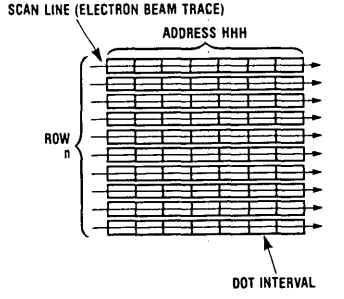

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FIGURE 2. Character Cell Definition (Example Shown Is a 7 x 10 Character Cell)

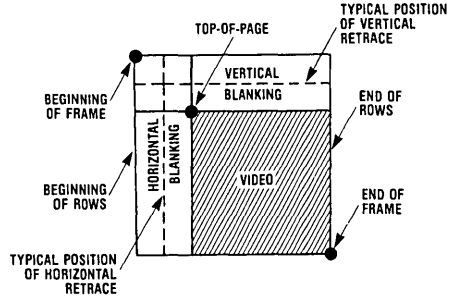

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FIGURE 3. Frame Format Definition

Character Generation/Timing Outputs

The CRT controller provides 11 interface timing outputs for line buffers, character generator ROMs, DM86S64-type latch/ROM/shift register combination character generators, and system status timing. All outputs are buffered to provide TTL compatible direct interface to popular system circuits such as:

- DM86S64 Series Character Generators
- MM52116 Series Character ROMs
- DM74166 Dot Shift Register
- MM5034, MM5035 Octal 80-Bit Shift Registers (Line Buffers)

Dot Rate Clock: This output is provided for use in system synchronization and interface to the dot shift register used in character generation. This output is non-inverting with respect to an external clock applied to the X1 oscillator input (see *Figure 6*). The dot rate clock output exhibits a 50% duty cycle. All CRTC output logic transitions are synchronous with the rising edge of the Dot Rate Clock output.

Latch Character Generator Address (Character Rate Clock): This output provides an active clock pulse at character rate frequency which is active at all times. The rising edge of this pulse is synchronous with the beginning of each character cell. This output is intended for direct interface to character/video generation data latch registers.

Line Rate Clock: This output provides an active clock pulse at scan-line rate frequency (horizontal frequency), which is active at all times. The falling edge of this pulse is synchronous with the beginning of horizontal blanking. This output is intended for direct interface to character generation scan line counters.

Load Video Shift Register: This output provides a character rate signal intended for direct interface to the video dot shift register used in character generation. Active low pulses are outputted only during video time. As a result of the inactive time, horizontal and vertical video blanking can be derived from this output signal.

Clear Line Counter: This output signal is active only during the first scan line of all rows.It exhibits an active low pulse identical and synchronous to the Line Rate Clock and is provided for direct interface to character generation scan line counters.

Line Counter Outputs (LC_0 to LC_3): These outputs clock at line rate frequency, synchronous with the falling edge of the line rate clock, and provide a consecutive binary count for each scan line within a row. These outputs are provided for system designs that require decoded information indicating the present scan line position within a row. These outputs are always active, however, the next to the last row during vertical blanking will exhibit an invalid line count as a function of internal frame synchronization.

Line Buffer Clock: This output directly interfaces to data shift registers when they are incorporated as line buffers in a system design (see *Figure 16*). This signal is active at character rate frequency and is intended for shift registers that shift on a falling edge clock. This output is inactive during all horizontal blanking intervals yielding the number of active clocks per scan line equal to the number of video characters per row. For custom requirements, the duty cycle of this output is mask programmable.

Line Buffer Recirculate Enable: This output is provided to control the input loading mode of the data shift register (line buffer) when used in a system design. The format of this output is intended for shift registers that load external data into the input with the mode control in the low state, and load output data into the input (recirculate) with the mode control in the high state. This output will transition to the low state, synchronous with the line rate clock falling edge, for one complete scan line of each row. The position of this scan line will either be the first scan line of the addressed row, or the last scan line of the previous row depending upon the logic level of the address mode input (pin 11), tabulated in Table III.

Memory Address Outputs/Inputs and Registers

Address Outputs (A_0-A_{11}): These 12 address bits (4k) are bi-directional TRI-STATE outputs that directly interface to the system RAM memory address bus.

In the output mode (enabled), these outputs will exhibit a specific 12-bit address for each video character cell to be displayed on the CRT screen. This 12-bit address increments sequentially at character rate frequency and is valid at the address bus 2 character times prior to the addressed character appearing as video on the CRT screen. This pipelining by 2 characters is provided to allow sufficient time for first, accessing the RAM memory, and second, accessing the character generation memory with the RAM memory data. Since a character cell is comprised of several scan lines of the CRT beam, the sequential address output string for a given video row is identically repeated for each scan line within the row. The starting address for each video scan line is stored within an internal 12-bit register called the Row Start Register. At the beginning of each video scan line, the internal address counter logic is preset with the contents of the Row Start Register (see *Figure 4*). To accomplish row by row sequential addressing, internal logic updates the Row Start Register at the beginning of the first scan line of a video row with the last address + 1 of the last scan line of the previous video row. Since the number of address locations on the video screen display is typically much less than the 4k dimension of the 12-bit address bus, an internal 12-bit register called the Top Of Page Register, contains the starting address of the first video row. Internal logic loads the contents of this top of page register into the Row Start Register at the beginning of the first scan line of the first video row. The Top Of Page Register is loaded with address zero whenever the Reset input is pulsed to the logic "0" state.

In the input mode (disabled), external addresses can be loaded into the internal 12-bit registers by external control of the register select A, register select B, and register $\overline{\text{load}}$ inputs (see Table I). As a result of specific external loading of the contents of the Row Start Register, Top Of Page Register, and the Cursor Register, row by row page scrolling, non-sequential row control, and cursor location control, can easily be accomplished.

During the non-video intervals, the address output operation is modified. During all horizontal blanking intervals, the incrementing of the address counter is inhibited and the address count is held constant at the last video address + 1. For example, if a video row has an 80 character cell format and addressing for the video portion of a given scan line

Memory Address Outputs/Inputs and Registers (Continued)

starts at address 1, the address counter will increment up through address 81. Address 81 is held constant during the horizontal blanking interval until 3 character times before the next video scan line. At this point, the address counter is internally loaded with the contents of the Row Start Register which may contain address 1 or 81 as a function of internal control, or a new address that was loaded from the external bus. During vertical blanking, however, this loading of the internal address counter with the contents of the Row Start Register is inhibited providing scan line by scan line sequential address incrementing. This allows minimum access time to the CRTC when the address counter outputs are being used for dynamic RAM refresh.

RAM Address Enable Input: At all times the status of the bi-directional address outputs is controlled externally by the logic level of the enable input. A 'low' logic level at this input places the address outputs in the TRI-STATE (disabled) input mode. A 'high' logic level at this input places the address outputs in the active (enabled) output mode.

Register $\overline{\text{Load}}$/Select Inputs: When the Register $\overline{\text{Load}}$ input is pulsed to the logic 'low' state, the Top Of Page, Row Start, or Cursor Register will be loaded with a 12-bit address which originates from either the internal address counter or the external address bus (refer to discussion on register loading constraints). The destination register is selected prior to the load pulse by setting the register select inputs to the appropriate state as defined in Table I.

TABLE I. Register Load Truth Table

Register Select A (Pin 39)	Register Select B (Pin 1)	Register Load Input (Pin 38)	Register Loading Destination
0	0	0	No Select
0	1	0	Top-of-Page
1	0	0	Row-Start*
1	1	0	Cursor
X	X	1	No Load

*During the vertical blanking interval, a load to this register is internally routed to the Top-Of-Page register.

Internal Registers and Loading Constraints: There are 3 internal 12-bit registers that facilitate video screen management with respect to row-by-row page scrolling, non-sequential row control and cursor location. These registers can be loaded with addresses from the external address bus while the address outputs are disabled (RAM address enable input in the low state), by controlling the register select and load inputs within the constraints of each register.

The Row-Start Register (RSR) holds the starting address for each scan line of the video portion of a frame. The video addressing format is completely determined by the contents of this register. With no external loading, the RSR is automatically loaded by internal control such that row-by-row sequential addressing is achieved. Referring to *Figure 4*, the RSR is loaded automatically once for each video row during the first addressed scan line. The source of the loaded address is internally controlled such that the RSR load for the first video row comes from the Top-Of-Page Register. The RSR load for all subsequent video rows comes from the address counter which holds the last displayed address + 1. If non-sequential row formatting is desired, the RSR can be loaded externally with a 12-bit address. However, this external load must be made prior to the internal automatic load. Generally speaking, the external load to the RSR should be made during the video domain of the last addressed scan line of the previous row. *Figure 4* indicates the internal automatic loading intervals which must be avoided, if the load must be made during the horizontal blanking interval. Once an external address has been loaded to the RSR, the next occurring internal automatic RSR load will be inhibited by internal detection logic. If an external load is made to the RSR during the vertical blanking interval, the 12-bit address is loaded into the Top-Of-Page Register instead of the RSR as a result of internal control. This internal function is performed due to the fact that the address loaded into the RSR for the first video row can only come from the Top-Of-Page Register.

The Top-Of-Page register (TOPR) holds the address of the first character of the first video row. As a function of internal control the contents of this register are loaded into the RSR at the beginning of the first addressed scan line of the first video row (see *Figure 4*). This loading operation is strictly a function of internal control and cannot be overridden by an external load to the RSR. For this reason, any external load to the RSR during the vertical blanking interval is interpreted internally as TOPR load. When the Reset input is pulsed to the logic "0" state, the TOPR register is loaded with address zero by internal control. This yields a video page display with the first row of sequential addressing beginning at zero. Page scrolling can be accomplished by externally loading a new address into the TOPR. This loading operation can be performed at any time during the frame prior to the interval where the TOPR is loaded automatically into the RSR (see *Figure 4*). Once the TOPR has been loaded, it does not have to be accessed again until the contents are to be modified.

The Cursor Register (CR) holds the present address of the cursor location. A true comparison of the address counter outputs and the contents of the CR results in a Cursor Enable output signal delayed by two character times. When the $\overline{\text{Reset}}$ input is pulsed to the logic "0" state, the contents of the CR are set to address zero by internal control. Modifying the contents of the CR is accomplished by external loading at any time during this frame. Typically, loading is performed only during intervals when the address outputs are not actively controlling the video display. Once the CR has been loaded, it does not have to be accessed again until the contents are to be modified.

Video-Related Outputs

Horizontal Sync: This output provides the necessary scan line rate sync signal for direct interface to either three-terminal or composite sync monitors. The pulse width, position, and logic polarity are mask programmable, in character time increments, for custom requirements. This output may also be mask programmed to have RS-170 compatible serration pulses during the vertical sync interval (refer to DP8352 format and *Figure 15*).

Video-Related Outputs (Continued)

Vertical Sync: This output provides the necessary frame rate sync signal for direct interface to either three-terminal or composite sync monitors. The pulse width, position, and logic polarity are mask programmable, in scan line increments, for custom requirements.

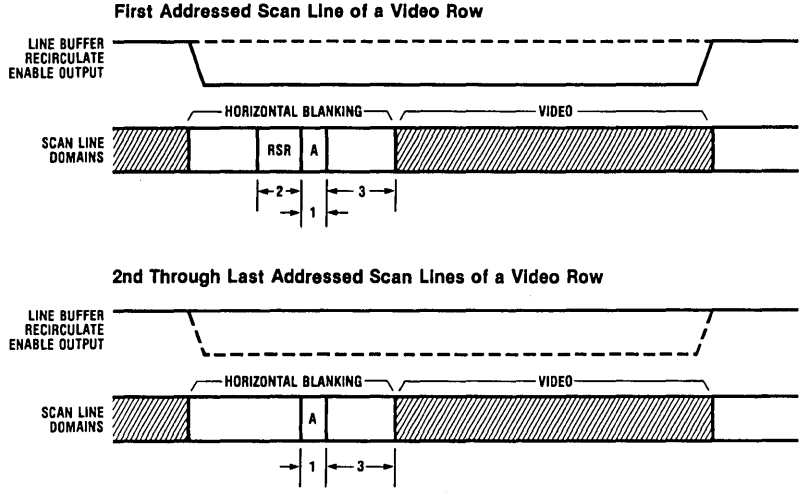
Cursor Enable: This output provides a signal that is intended to be combined with the video signal to display a cursor attribute which serves as a visual pointer for video RAM location. Internally, the 12-bit address count is continuously being compared with the 12-bit address stored in the Cursor Register. When a true compare is detected, an active high level signal will be present at the Cursor Enable output, delayed by 2 character times after the corresponding address bus output. The signal is delayed by 2 character times so that it will be coincident with the video information resulting from the corresponding address. Mask programmability allows the cursor enable output signal to be formatted such that a signal will be outputted for all addressed scan lines of a video character cell or any single scan line of that cell. The cursor enable output signal is inhibited during the horizontal and vertical blanking intervals so that video blanking is maintained. When the addressing is advanced by setting the address mode input (pin 11) in the logic "0" state, the cursor enable signal will also be shifted with respect to the scan line count. Specifically, for a character cell with the cursor output active on all addressed scan lines of the cell, the first scan line of the cursor signal will occur at the last scan line count of the previous video row, and the last scan line count of the addressed character cell will have no cursor output signal. This mode of operation gives rise to a unique situation for the first video row where the first addressed scan line of a character cell has no cursor output signal since its advanced scan line position is inhibited by the vertical blanking interval.

CRT System Control Functions

Refresh Control Input: This input provides a logic level selectable CRT system refresh rate. Typically, this input will select either a 60 Hz or 50 Hz refresh rate to provide geographical marketing flexibility. However, mask programmability provides the capability of a wide range of frequencies for custom requirements. For definition of the input logic truth table and the refresh rate format, refer to Table II and the standard device type format tables.

Table II. Refresh Rate Select Truth Table

Refresh Control (Pin 3) Logic Level	Frame Refresh Rate			
	Symbol	DP8350	DP8352	DP8353
1	f1	60 Hz	60 Hz	60 Hz
0	f0	50 Hz	50 Hz	50 Hz



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Note 1: Dimensions are in character time intervals.

Note 2: "A" denotes the interval that the address counter is preset with the contents of the Row Start Register.

Note 3: "RSR" denotes the interval that the Row Start Register is internally loaded with either the contents of the Top-Of-Page Register (1st video row) or the last video address + 1 from the address counter.

FIGURE 4. Automatic Internal Loading Intervals

CRT System Control Functions (Continued)

Vertical Blanking Output: This output provides a signal that transitions at the end of the last video scan line of the last video row and indicates the beginning of the vertical blanking interval. This signal transitions back to the inactive state during the row of scan lines just prior to the first video row. The transition position within this last row of vertical blanking, as well as the active logic polarity, is a function of the particular device format (item 21 of the format tables) or is mask programmable for custom requirements.

Address Mode: When a system utilizes a line buffer shift register, the scan line of addressing for a row is used to load the shift register. As a result of this loading operation, addressing for a particular row will not begin accessing the video RAM until the second scan line of addressing for the row. It also follows that the first scan line of a row can only exhibit addressed data for the previous video row that is in the shift register. This offset in addressing becomes a problem for character generation designs that output video on the first scan line of a row (with respect to the line counter outputs). The result is invalid data being displayed for the first scan line. One solution would be to utilize a character generation design that began outputting video on the second scan line of a row. However, since most single chip character generators begin video on the first scan line, the DP8350 series CRT controller provides a pin selectable advanced addressing mode which will compensate for addressing shifts resulting from shift register loading. Referring to Table III, a high logic level at this input will cause addressing to be coincident with the scan line counter positions of a row, and a low logic level at this input will cause addressing to start on the last scan line counter position of the previous row. This shifted alignment of the addressing, with respect to the designated scan lines of a row, is diagrammed in *Figure 5*. Characteristically, it follows that, when addressing is advanced by one scan line, the Line Buffer Recirculate Enable output and the Cursor Enable output are also advanced by one scan line. This advanced position of the Cursor Enable output may deserve special consideration depending upon the system design.

Table III. Address Mode Truth Table

Address Mode Input (Pin 11) (Logic Level)	New Row Addressing At Address Outputs and Line Buffer Recirculate Enable Logic Low Level (Scan Line Position)
0	Last scan line of previous row
1	First scan line of row

Full/Half Row Control: This control input is provided for applications that require the option of half-page addressing. As an example, if the normal video page format is 80 characters/row by 24 rows, setting this input to the logic "0" state will cause the video format to become evenly spaced at 80 characters/row by 12 rows. Specifically, when this input is in the logic "0" state, row addressing is repeated for every other row. This yields successive groups of two rows of identical addressing. The second row of addressing, however, has the Load Video Shift Register output and the Cursor Enable output internally inhibited to provide the necessary video blanking. Setting this input to the logic "1" state yields normal frame addressing.

External Character/Line Rate Clock: This input is intended to aid testing of the CRTC and is not meant to be used as an active input in a CRT system. When this input is left open, it is guaranteed not to interfere with normal operation.

$\overline{\text{Reset}}$ Input: This input is provided for power-up synchronization. When brought to the logic "0" state, device operation is halted. Internal logic is set at the beginning of vertical blanking, and the Top-Of-Page Register and the Cursor Register are loaded with address zero. When this input returns to the logic "1" state, device operation resumes at the vertical blanking interval followed by video addressing which begins at zero. This input has hysteresis and may be connected through a resistor to V_{CC} and through a capacitor to ground to accomplish a power-up Reset. The logic "0" state should be maintained for a minimum of 250 ns.

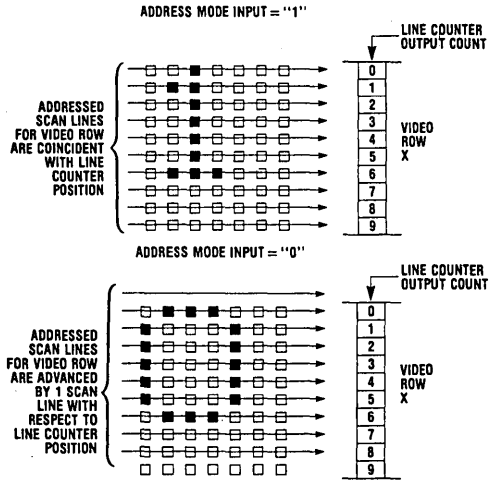

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FIGURE 5. Address Mode Functionality

Crystal Inputs X1 and X2: The "Pierce"-type oscillator is controlled by an external crystal providing parallel resonant operation. Connection of external bias components is made to pin 22 (X1) and pin 21 (X2) as shown in *Figure 6*. It is important that the crystal be mounted in close proximity to the X1 and X2 pins to ensure that printed circuit trace lengths are kept to an absolute minimum. Typical specifications for the crystal are shown in Table IV for each of the standard products, DP8350, DP8352, and DP8353. When customer mask options require higher frequencies, it may be necessary to change the crystal specifications and biasing components. If the CRTC is to be clocked by an external system dot clock, pin 22 (X1) should be driven directly by Schottky family logic while pin 21 (X2) is left open. The typical threshold for pin 22 (X1) is $V_{CC}/2$.

CRT System Control Functions (Continued)

Table IV. Typical Crystal Specifications

Parameter	Specification		
	DP8350	DP8352	DP8353
Type	At-Cut		
Frequency	10.92 MHz	7.02 MHz	17.6256 MHz
Tolerance	0.005% at 25°C		
Stability	0.01% from 0°C to +70°C		
Resonance	Fundamental, Parallel		
Maximum Series Resistance	50Ω		
Load Capacitance	20 pF		

Custom Order Mask Programmability: The DP8350 Series CRT controller is available in three standard options designated DP8350, DP8352, and DP8353. The functional format of these devices was selected to meet the typical needs of CRT terminal designs. In order to accommodate specific customer formats, the DP8350 series CRT controller is mask programmable with a diverse range of options available. The items listed in the program table worksheet indicate the available options, while Table V tabulates the programming constraints.

Table V. Mask Programming Limitations

Designation	Parameter		Min Value	Max Value
f_{DOT}	Dot Rate Frequency		DC	30 MHz
f_{CHAR}	Character Rate Frequency		DC	2.5 MHz
—	Line Buffer Clock Logic "0" Width (Item 20 × Item 24)		200 ns	
Item 3	Dots per Character Field Width		4	16
Item 4	Scan Lines per Character Field		2	16
Item 12	Scan Lines per Frame			512
Item 14	Character Times per Row	Video	5	122
		Blanking	6	123
Item 11	Scan Lines per Vertical Blanking		(Item 4) +2	
If the cursor enable output, Item 22, is active on only one line of a character row, then Item 21 value must be either "1" or "0" or equivalent to the line selected for the cursor enable output.				

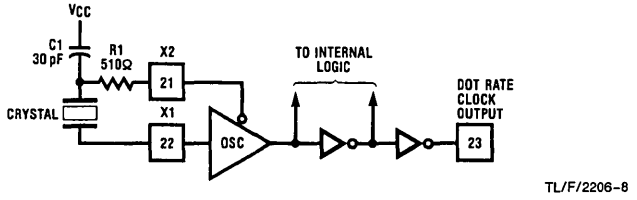

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FIGURE 6. Dot Clock Oscillator Configuration with Typical External Bias Circuitry Shown

DP8350 Series Custom Order Format Table

This table is provided as a worksheet to aid in determining the programmed configuration for custom mask options. Refer to Table V for a list of programming limitations.

Item No.	Parameter		Value	
1	Character Font Size (Reference Only)	Dots per Character (Width)		
2		Scan Lines per Character (Height)		
3	Character Field Block Size	Dots per Character (Width)		
4		Scan Line per Character (Height)		
5	Number of Video Characters per Row			
6	Number of Video Character Rows per Frame			
7	Number of Video Scan Lines (Item 4 x Item 6)			
8	Frame Refresh Rate (Hz) (two pin selectable frequencies allowed) (Item 13 ÷ Item 12)		f1 =	f0 =
9	Delay after Vertical Blank start to start of Vertical Sync (Number of Scan Lines)			
10	Vertical Sync Width (Number of Scan Lines)			
11	Interval between Vertical Blank start and start of Video (Number of Scan Lines of Video Blanking)			
12	Total Scan Lines per Frame (Item 7 + Item 11)			
13	Horizontal Scan Frequency (Line Rate) (kHz) (Item 8 x Item 12)			
14	Number of Character Times per Scan Line			
15	Character Clock Rate (MHz) (Item 13 x Item 14)			
16	Character Time (ns) (1 ÷ Item 15)			
17	Delay after Horizontal Blank start to Horizontal Sync start (Character Times)			
18	Horizontal Sync Width (Character Times)			
19	Dot Frequency (MHz) (Item 3 x Item 15)			
20	Dot Time (ns) (1 ÷ Item 19)			
21	Vertical Blanking Output Stop before start of Video (Number of Scan Lines) (Range = Item 4 − 1 line to 0 lines)			
22	Cursor Enable on all Scan Lines of a Row? (Yes or No) If not, which Line?			
23	Does the Horizontal Sync Pulse have Serrations during Vertical Sync? (Yes or No)			
24	Width of Line Buffer Clock logic "0" state within a Character Time (Number of Dot Time increments) (Typically ½ Item 3 rounded up)			
25	Serration Pulse Width, if used (Character Times) (See *Figure 13*)			
26	Horizontal Sync Pulse Active state logic level (1 or 0)			
27	Vertical Sync Pulse Active state logic level (1 or 0)			
28	Vertical Blanking Pulse Active state logic level (1 or 0)			

Video Monitor: Manufacturer and Model No. (For Engineering Reference)

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage, V_{CC}	7.0V
Input Voltage	5.5V
Output Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Lead Temp. (soldering, 10 seconds)	300°C

Operating Conditions (Note 6)

	Min.	Max.	Units
V_{CC}, Supply Voltage	4.75	5.25	V
T_A, Ambient Temperature	0	+70	°C

Electrical Characteristics V_{CC} = 5V ± 5%, T_A = 0°C to +70°C (Notes 2, 3, and 5)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	Logic "1" Input Voltage All Inputs Except X1, X2 $\overline{RESET}$ $\overline{RESET}$		2.0 2.6			V V
V_{IL}	Logic "0" Input Voltage All Inputs Except X1, X2				0.8	V
V_{HYS}	$\overline{RESET}$ Input Hysteresis			0.4		V
V_{clamp}	Input Clamp Voltage All Inputs Except X1, X2	I_{IN} = −12 mA		−0.8	−1.2	V
I_{IH}	Logic "1" Input Current A_0-A_{11}	Enable Input = 0V, V_{CC} = 5.25V, V_{IN} = 5.25V		10	100	μA
	All Other Inputs Except X1, X2	V_{CC} = 5.25V, V_{IN} = 5.25V		2.0	20	μA
I_{IL}	Logic "0" Input Current A_0-A_{11}	Enable Input = 0V, V_{CC} = 5.25V, V_{IN} = 0.5V		−20	−100	μA
	All Other Inputs Except X1, X2	V_{CC} = 5.25V, V_{IN} = 0.5V		−20	−100	μA
V_{OH}	Logic "1" Output Voltage	I_{OH} = −100 μA	3.2	4.1		V
		I_{OH} = −1 mA	2.5	3.3		V
V_{OL}	Logic "0" Output Voltage	I_{OL} = 5 mA		0.35	0.5	V
I_{OS}	Output Short Circuit Current	V_{CC} = 5V, V_{OUT} = 0V (Note 4)	10	40	100	mA
I_{CC}	Power Supply Current (Note 10)	V_{CC} = 5.25V		220	300	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified, min./max. limits apply across the 0°C to +70°C temperature range and the 4.75V to 5.25V power supply range. All typical values are for T_A = 25°C and V_{CC} = 5.0V and are intended for reference only.

Note 3: All currents into device pins are shown as positive; all currents out of device pins are shown as negative; all voltages are referenced to ground, unless otherwise specified. All values shown as max. or min. are so classified on absolute value basis.

Note 4: Only one output at a time should be shorted.

Note 5: Electrical specifications do not apply to pin 17, external char/line clock, as this pin is used for production testing only.

Note 6: Functional operation of device is not guaranteed when operated beyond specified operating condition limits.

Switching Characteristics V_{CC} = 5.0V ± 5%, T_A = 25°C (Note 7)

Symbol	Parameter	Load Circuit	Notes	Min	Typ	Max	Units
Symmetry	Dot Rate Clock Output High Symmetry With Crystal Control	1		50% − 4	50% − 2	50% + 1	ns
t_{pd1}	XI Input to Dot Rate Clock Output Positive Edge	1			17	22	ns
t_{pd0}	XI Input to Dot Rate Clock Output Negative Edge	1			21	26	ns
t_{D1}	Dot Clock to Load Video Shift Register Negative Edge	1			6.0	10	ns
t_{D2}	Dot Clock to Load Video Shift Register Positive Edge	1			11	15	ns
t_{D3}	Dot Clock to Latch Character Generator Positive Edge	1			8.0	13	ns
t_{D4}	Dot Clock to Latch Character Generator Negative Edge	1			6.0	10	ns
t_{D2}-t_{D3}	Latch Character Generator Positive Edge to Load Video Shift Register Positive Edge	1		0	3.0		ns
t_{D5}	Dot Clock to Line Buffer Clock Negative Edge	1			23	35	ns
t_{PW1}	Line Buffer Clock Pulse Width	1	8,9	N(DT)	N(DT) + 8	N(DT) + 12	ns
t_{D6}	Dot Clock to Cursor Enable Output Transition	1			24	36	ns
t_{D7}	Dot Clock to Valid Address Output	1			15	25	ns
t_{D8_0}	Latch Character Generator to Line Rate Clock Neg. Transition	1	8,10		425 + DT	500 + DT	ns
t_{D8_1}	Latch Character Generator to Line Rate Clock Pos. Transition	1	8,10		300 + DT	400 + DT	ns
t_{D9_0}	Latch Character Generator to Clear Line Counter Neg. Transition	1	8,10		525 + DT	700 + DT	ns
t_{D9_1}	Latch Character Generator to Clear Line Counter Pos. Transition	1	8,10		290 + DT	400 + DT	ns
t_{D8_1}-t_{D9_1}	Clear Line Counter Pos. Transition to Line Rate Clock Pos. Transition	1	10		10	60	ns
t_{D10}	Line Rate Clock to Line Counter Output Transition	1			60	120	ns
t_{D11}	Line Rate Clock to Line Buffer Recirculate Enable Transition	1			195	300	ns
t_{D12}	Line Rate Clock to Vertical Blanking Transition	1			160	300	ns
t_{D13}	Line Rate Clock to Vertical Sync Transition	1			220	300	ns
t_{D14}	Latch Character Generator to Horizontal Sync Transition	1			96	150	ns

Switching Characteristics V_{CC} = 5.0V ±5%, T_A = 25°C (Note 7) (Continued)

Symbol	Parameter	Load Circuit	Notes	Min	Typ	Max	Units
t_{S1}	Register Select Set-up Before Register Load Negative Edge			0			ns
t_{H1}	Register Select Hold After Register Load Positive Edge			0			ns
t_{S2}	Valid Address Input Set-Up Before Register Load Positive Edge			250			ns
t_{H2}	Valid Address Hold Time After Register Load Positive Edge			0			ns
t_{PW2}	Register Load Required Pulse Width			150	65		ns
t_{LZ}, t_{HZ}	Delay from Enable Input to Address Output High Impedance State from Logic "0" and Logic "1"	2			15	30	ns
t_{ZL}, t_{ZH}	Delay from Enable Input to Logic "0" and Logic "1" from Address Output High Impedance State	2			17	30	ns

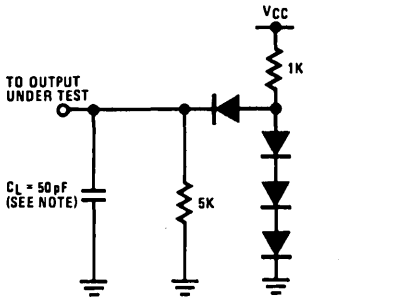
Note 7: Typical values are for V_{CC} = 5.0V and T_A = 25°C and are meant for reference only.

Note 8: "DT" denotes dot rate clock period time, item 20 from option format table.

Note 9: "N" denotes value of item 24 from option format table.

Note 10: Revised since last issue.

Switching Load Circuits



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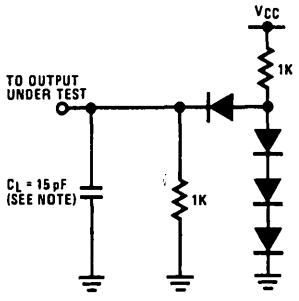
Load Circuit 1



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Load Circuit 2

Note: C_L includes probe and jig capacitance. All diodes are 1N914 or equivalent.

Switching Waveforms

SYMMETRY = $\frac{T_H}{T_P} \times 100\%$

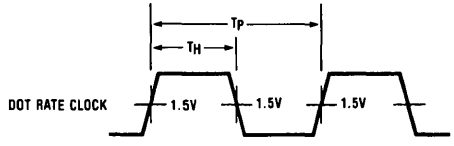

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FIGURE 7. Dot Rate Clock Output Waveform Symmetry with Crystal Control

[$t_r = t_f \leq 10$ ns
X2 (PIN 21) = OPEN]

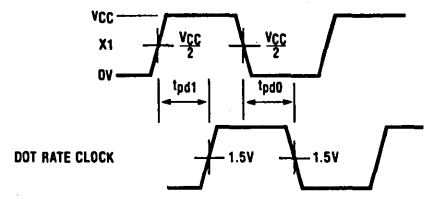

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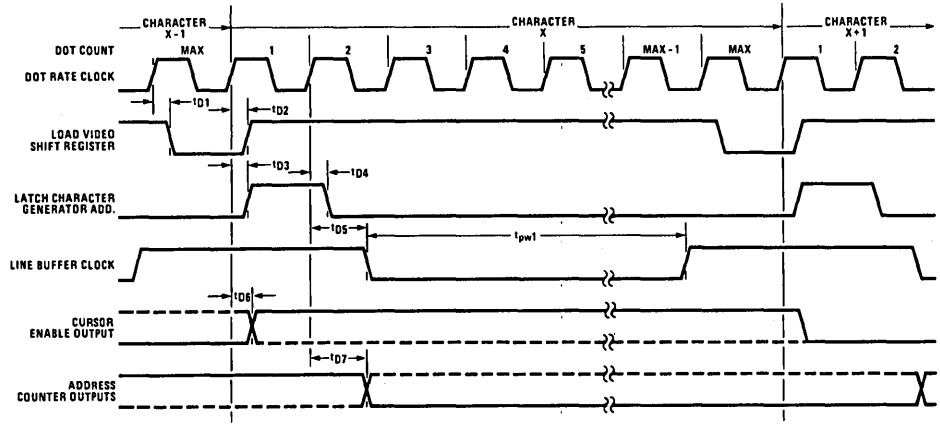
FIGURE 8. X1 Input to Dot Rate Clock Output Propagation Delay



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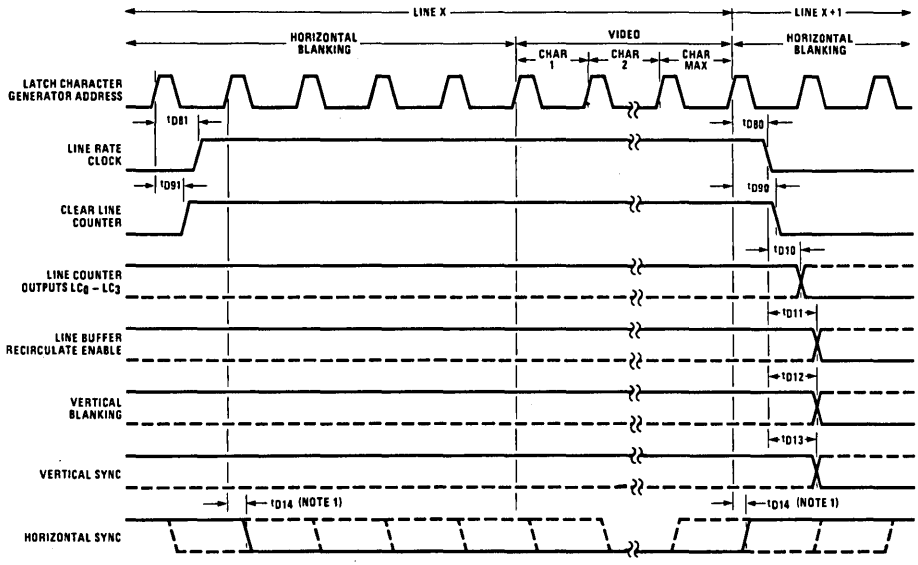
Note 1: All measurement points are 1.5V

FIGURE 9. Dot/Character Rate Timing



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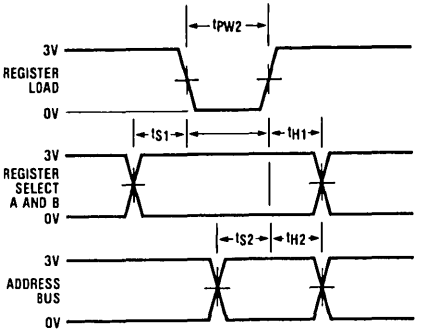
Note 1: Actual polarity and position of the horizontal sync start and stop points is a function of the particular device format.

Note 2: All measurement points are 1.5V.

FIGURE 10. Character/Line Rate Timing

Switching Waveforms (Continued)



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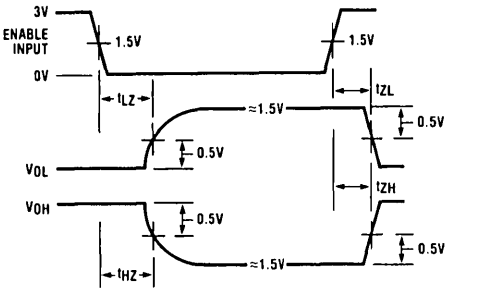

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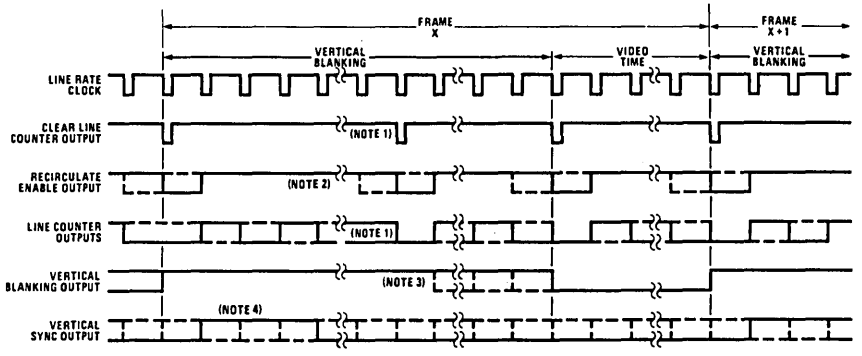
FIGURE 12. Address Output Enable/Disable Waveforms

Note 1: All measurement points are 1.5V.
Note 2: $t_r = t_f \leq 10$ ns.
Note 3: Address enable (pin 37) = 0V.

FIGURE 11. Register Select and Load Waveforms

Timing Diagrams



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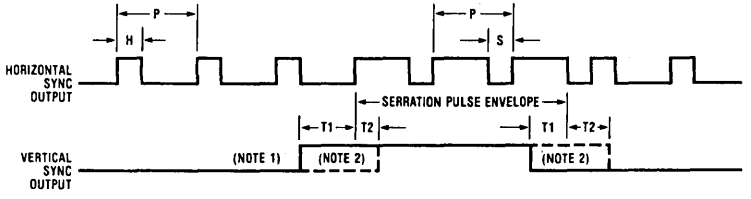
Note 1: One full row before start of video the line counter is set to zero state—this provides line counter synchronization in cases where the number of lines in vertical blanking are not even multiples of the number of lines per row.

Note 2: The position of the line buffer recirculate enable logic low level is a function of the logic level of the address mode input (see Table III).

Note 3: The stop point of the vertical blanking output active signal is a function of device type or custom option, and will always be within one row prior to video.

Note 4: The transition start and stop points of the vertical sync output signal are a function of device type or custom option.

FIGURE 14. Line/Frame Rate Functional Diagram



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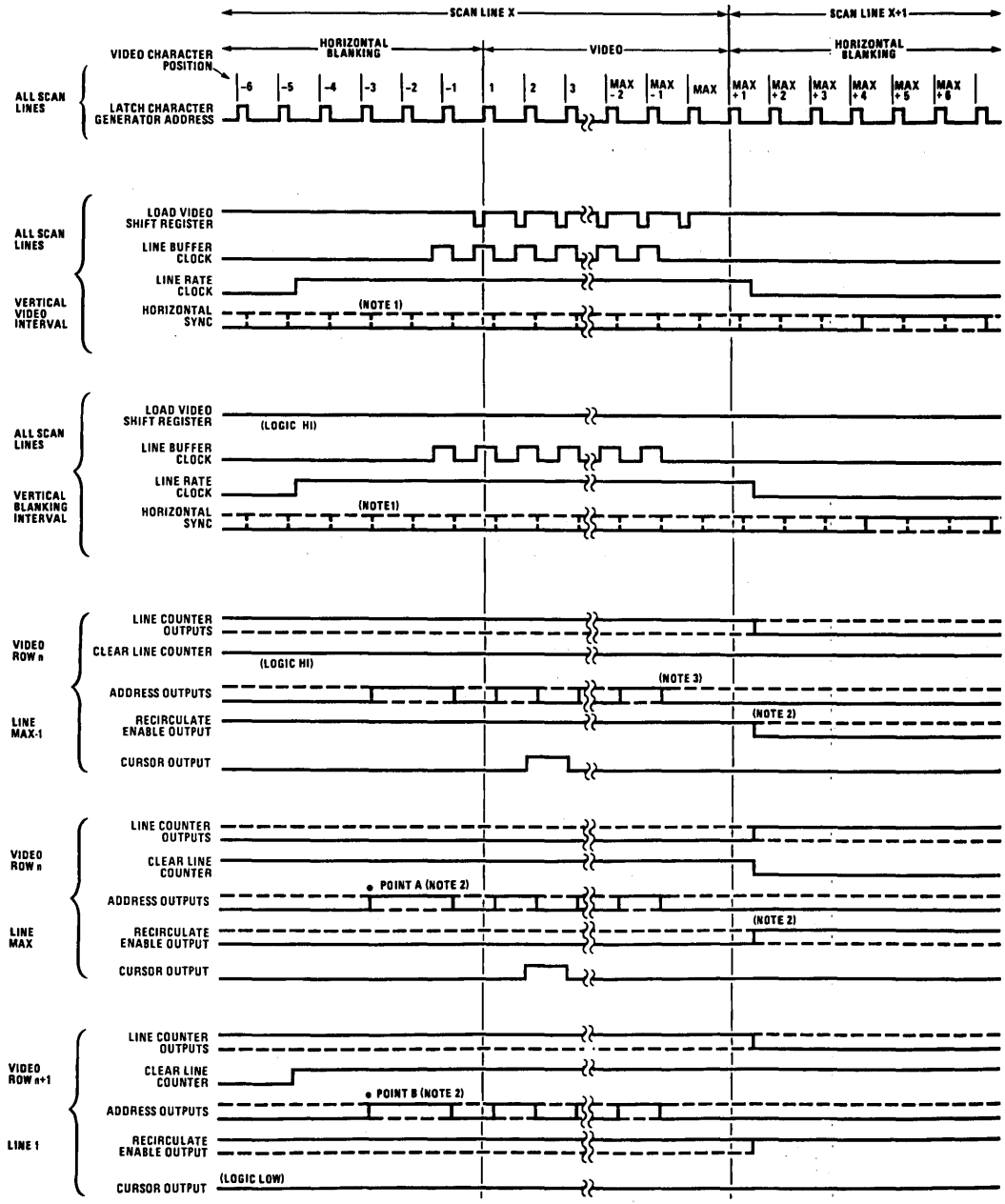
P = HORIZONTAL SCAN TIME PERIOD (ITEM 14 FROM PROGRAM TABLE)
H = HORIZONTAL SYNC WIDTH (ITEM 18 FROM PROGRAM TABLE)
S = SERRATION PULSE WIDTH (ITEM 25 FROM PROGRAM TABLE)
T1 = P-H (MAX)
T2 = H-1 CHARACTER TIME (MAX)

Note 1: The vertical sync transition point is always coincident with the beginning of horizontal blanking.

Note 2: T1 and T2 intervals represent the range of alignment offset between the vertical sync pulse and the serration pulse envelope and is a function of the horizontal sync position with respect to the beginning of horizontal blanking.

FIGURE 15. Serration Pulse Format

Timing Diagrams (Continued)



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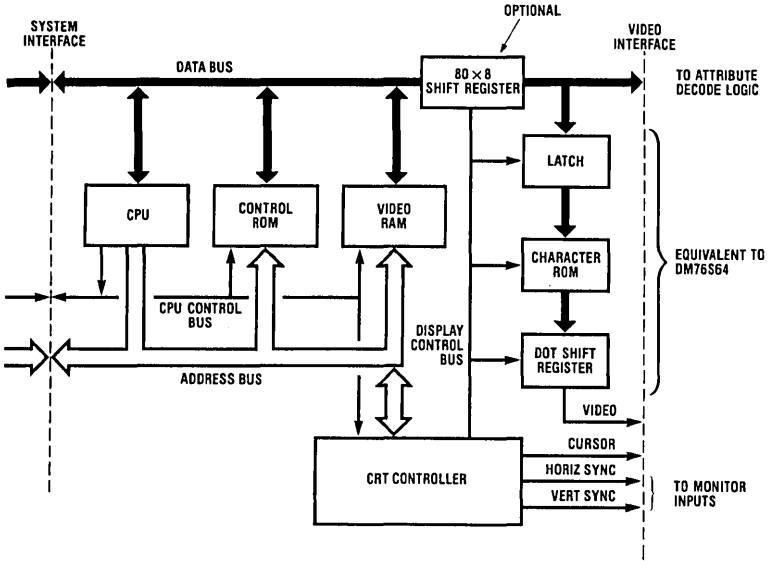
Note 1: The horizontal sync output start and stop point positions are a function of device type or custom option.

Note 2: The position of the recirculate enable output logic "0" level is dependent on the state of the address mode input. When address mode = "0", recirculate enable occurs on the max. line of a character row (solid line) and the address counter outputs all over to the new row address at point A. When address mode = "1", recirculate enable occurs on the first line of a character row (dashed line) and the address counter outputs roll over to the new row address at point B.

Note 3: The address counter outputs clock to the address of the last character of a video row plus 1. This address is then held during the horizontal blanking interval until video minus three character times. At this point the outputs are modified to the contents of the Row Start Register (RSR).

FIGURE 13. Character/Line Rate Functional Diagram

Applications



TL/F/2206–20

FIGURE 16. General System Block Diagram

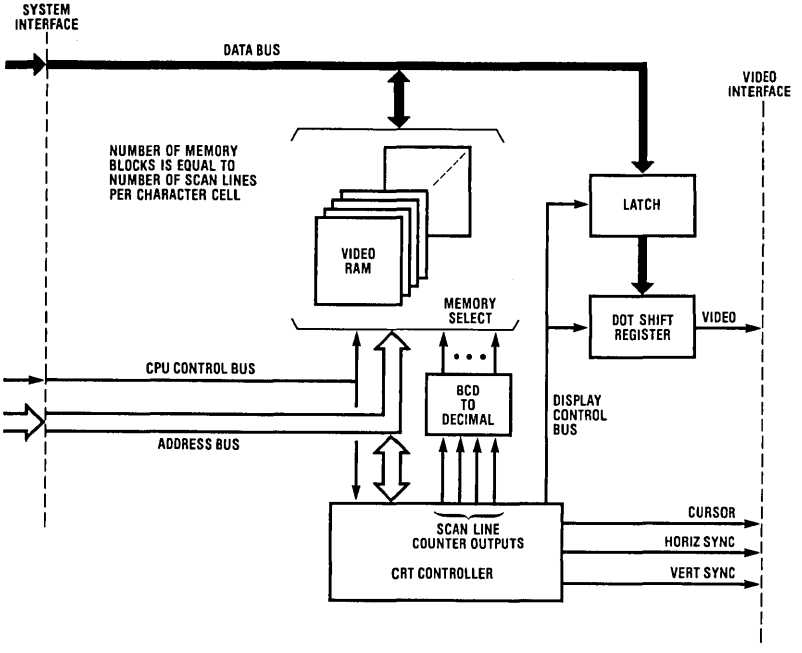


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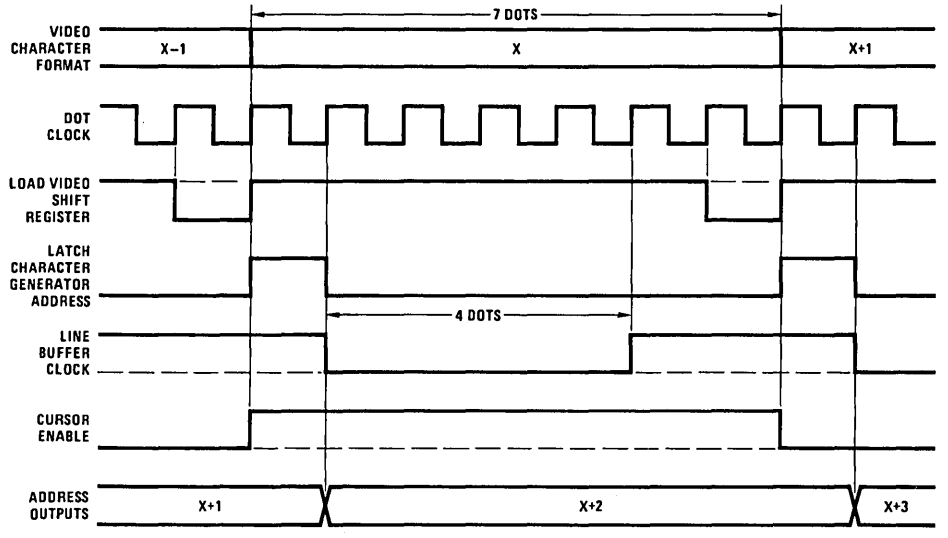
FIGURE 17. Dot-By-Dot Graphics Block Diagram

DP8350 CRT Controller

TABLE VI. Characteristic Format

Item No.	Parameter		Value	
1	Character Font Size (Reference Only)	Dots per Character (Width)	(5)	
2		Scan Lines per Character (Height)	(7)	
3	Character Field Cell Size	Dots per Character (Width)	7	
4		Scan Lines per Character (Height)	10	
5	Number of Video Characters per Row		80	
6	Number of Video Character Rows per Frame		24	
7	Number of Video Scan Lines (Item 4 x 6 Item 6)		240	
8	Frame Refresh Rate (Hz)		f1 = 60	f0 = 50
9	Delay after Vertical Blank start to start of Vertical Sync (Number of Scan Lines)		4	30
10	Vertical Sync Width (Number of Scan Lines)		10	10
11	Interval between Vertical Blank start and start of Video (Number of Scan Lines of Video Blanking)		20	72
12	Total Scan Lines per Frame (Item 7 + Item 11)		260	312
13	Horizontal Scan Frequency (Line Rate) (Item 8 x Item 12)		15.6 kHz	
14	Number of Character Times per Scan Line		100	
15	Character Clock Rate (Item 13 x Item 14)		1.56 MHz	
16	Character Time (1 ÷ Item 15)		641 ns	
17	Delay after Horizontal Blank start to Horizontal Sync start (Character Times)		0	
18	Horizontal Sync Width (Character Times)		43	
19	Dot Frequency (Item 3 x Item 15)		10.92 MHz	
20	Dot Time (1 ÷ Item 19)		91.6 ns	
21	Vertical Blanking Output Stop before start of Video (Number of Scan Lines)		1	
22	Cursor Enable on all Scan Lines of a Row? (Yes or No)		Yes	
23	Does the Horizontal Sync Pulse have Serrations during Vertical Sync? (Yes or No)		No	
24	Width of Line Buffer Clock logic "0" state within a Character Time (Number of Dot Time increments)		4	
25	Serration Pulse Width, if used (Character Times)		—	
26	Horizontal Sync Pulse Active state logic level (1 or 0)		1	
27	Vertical Sync Pulse Active state logic level (1 or 0)		0	
28	Vertical Blanking Pulse Active state logic level (1 or 0)		1	

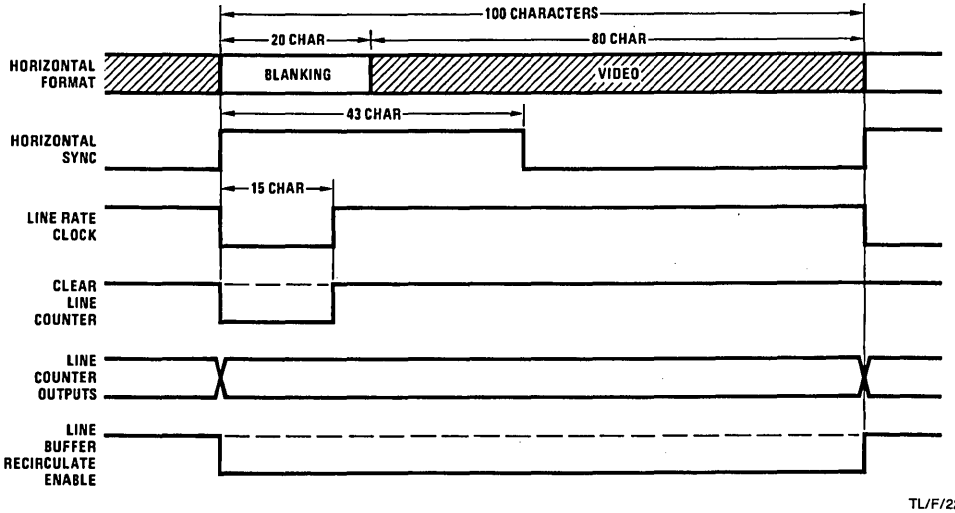
Video Monitor Format: Ball Brothers TV-12, TV-120 or Equivalent.



TL/F/2206-22

Note: Dashed lines in waveforms denote inactive state logic levels.

FIGURE 18. DP8350 Video Character Signals



TL/F/2206-23

Note: Dashed lines in waveforms denote inactive state logic levels.

FIGURE 19. DP8350 Scan Line Signals

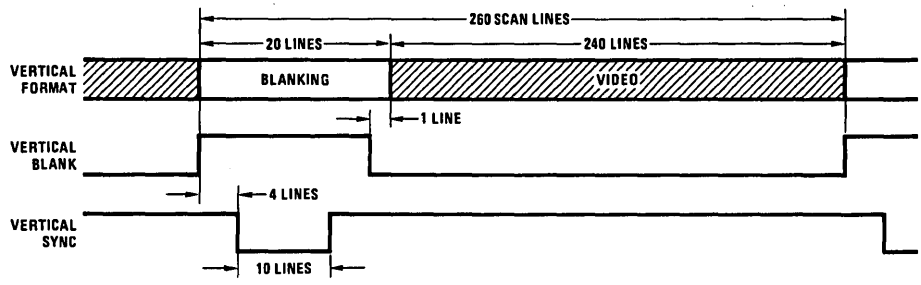


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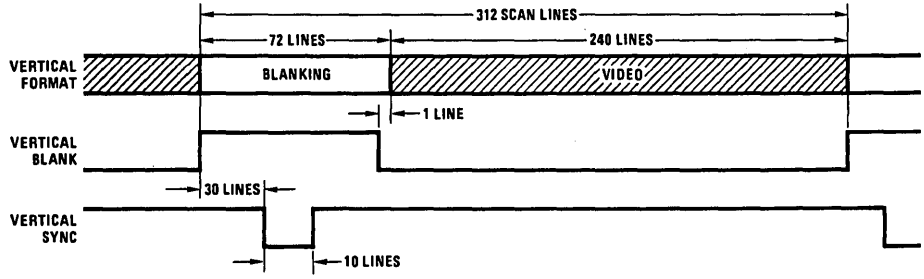
FIGURE 20. DP8350 60 Hz Refresh Rate Frame Signals



TL/F/2206–25

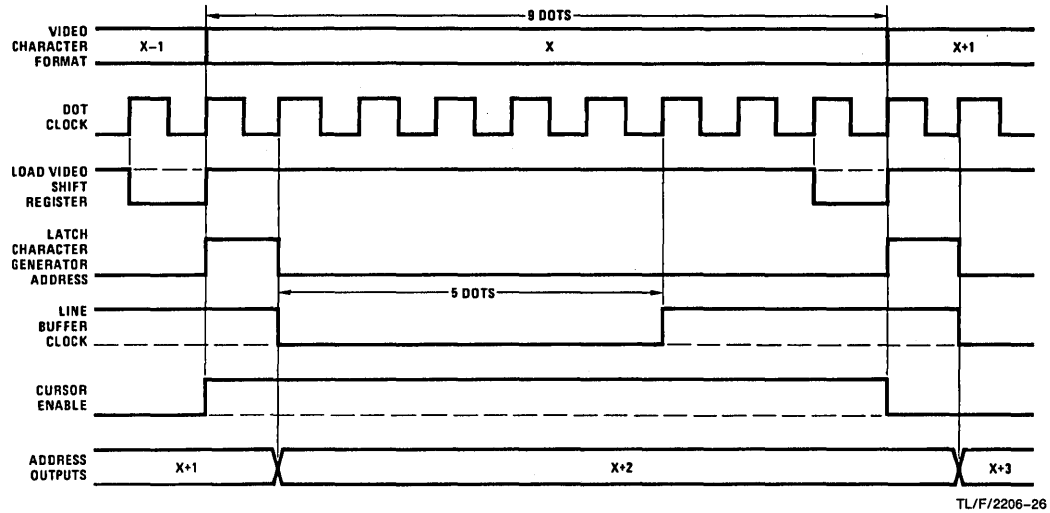
FIGURE 21. DP8350 50 Hz Refresh Rate Frame Signals

DP8352 CRT Controller

TABLE VII. Characteristic Format

Item No.	Parameter		Value	
1	Character Font Size (Reference Only)	Dots per Character (Width)	(7)	
2		Scan Lines per Character (Height)	(9)	
3	Character Field Cell Size	Dots per Character (Width)	9	
4		Scan Line per Character (Height)	12	
5	Number of Video Characters per Row		32	
6	Number of Video Character Rows per Frame		16	
7	Number of Video Scan Lines (Item 4 x Item 6)		192	
8	Frame Refresh Rate (Hz)		f1 = 60	f0 = 50
9	Delay after Vertical Blank start to start of Vertical Sync (Number of Scan Lines)		27	53
10	Vertical Sync Width (Number of Scan Lines)		3	3
11	Interval between Vertical Blank start and start of Video (Number of Scan Lines of Video Blanking)		68	120
12	Total Scan Lines per Frame (Item 7 + Item 11)		260	312
13	Horizontal Scan Frequency (Line Rate) (Item 8 x Item 12)		15.6 kHz	
14	Number of Character Times per Scan Line		50	
15	Character Clock Rate (Item 13 x Item 14)		0.78 MHz	
16	Character Time (1 ÷ Item 15)		1282 ns	
17	Delay after Horizontal Blank start to Horizontal Sync start (Character Times)		6	
18	Horizontal Sync Width (Character Times)		4	
19	Dot Frequency (Item 3 x Item 15)		7.02 MHz	
20	Dot Time (1 ÷ Item 19)		142.4 ns	
21	Vertical Blanking Output Stop before start of Video (Number of Scan Lines)		0	
22	Cursor Enable on all Scan Lines of a Row? (Yes or No)		Yes	
23	Does the Horizontal Sync Pulse have Serrations during Vertical Sync? (Yes or No)		Yes	
24	Width of Line Buffer Clock logic "0" state within a Character Time (Number of Dot Time increments)		5	
25	Serration Pulse Width, if used (Character Times)		4	
26	Horizontal Sync Pulse Active state logic level (1 or 0)		0	
27	Vertical Sync Pulse Active state logic level (1 or 0)		0	
28	Vertical Blanking Pulse Active state logic level (1 or 0)		1	

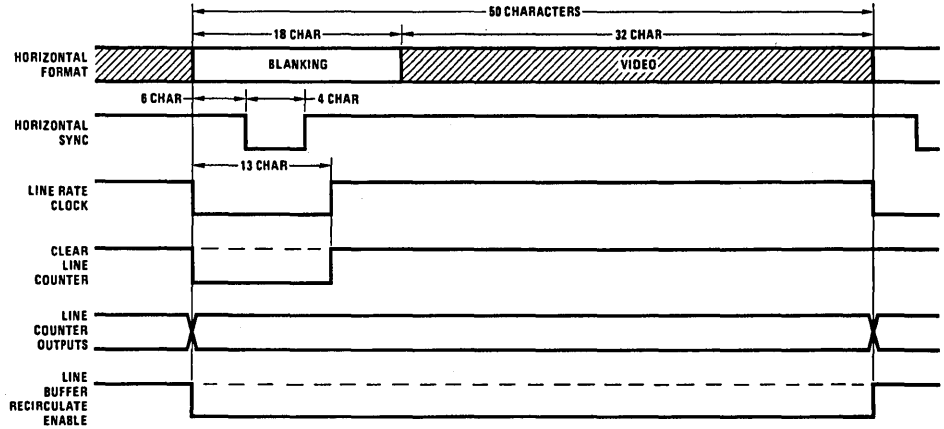
Video Monitor Format: RS-170-Compatible (Standard American TV).



TL/F/2206-26

Note: Dashed lines in waveforms denote inactive state logic levels.

FIGURE 22. DP8352 Video Character Signals



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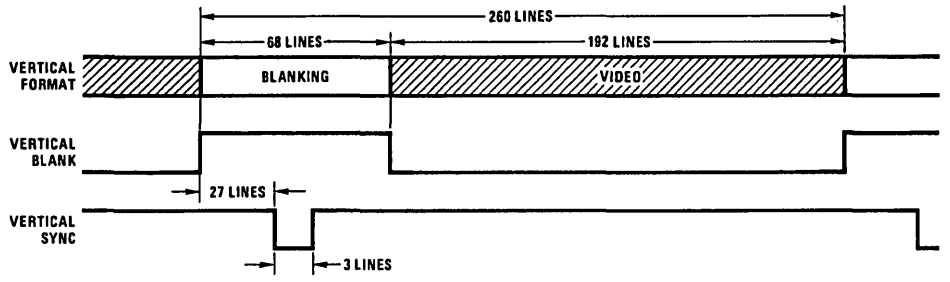
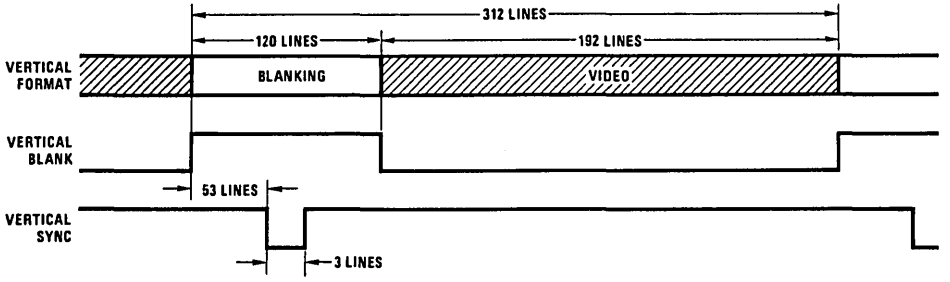
Note: Dashed lines in waveforms denote inactive state logic levels.

FIGURE 23. DP8352 Scan Line Signals



TL/F/2206-28

FIGURE 24. DP8352 60 Hz Refresh Rate Frame Signals



TL/F/2206-29

FIGURE 25. DP8352 50 Hz Refresh Rate Frame Signals

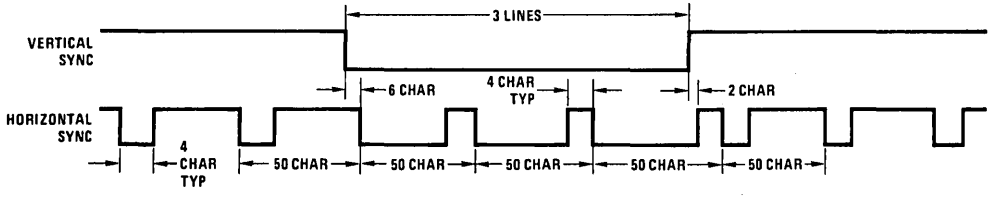


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FIGURE 26. DP8352 Serration Pulse Format

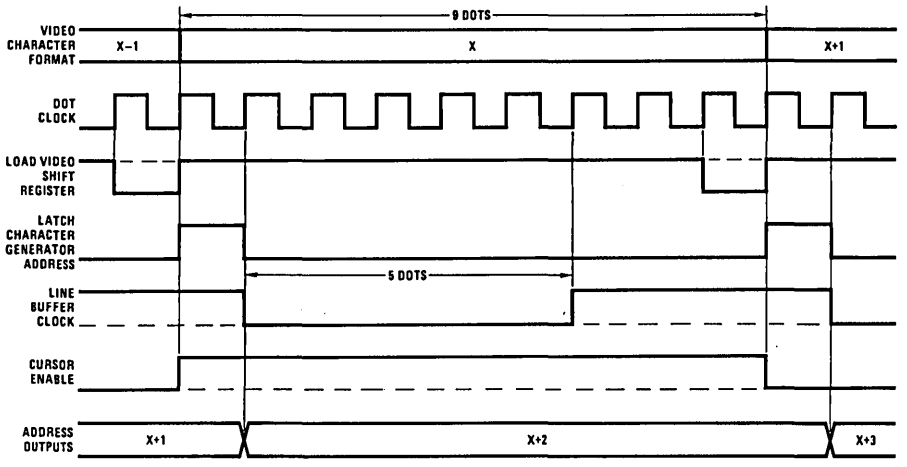
4

DP8353 CRT Controller

TABLE VIII. Characteristic Format

Item No.	Parameter		Value	
1	Character Font Size (Reference Only)	Dots per Character (Width)	(7)	
2		Scan Lines per Character (Height)	(9)	
3	Character Field Cell Size	Dots per Character (Width)	9	
4		Scan Lines per Character (Height)	12	
5	Number of Video Characters per Row		80	
6	Number of Video Character Rows per Frame		25	
7	Number of Video Scan Lines (Item 4 x Item 6)		300	
8	Frame Refresh Rate (Hz)		f1 = 60	f0 = 50
9	Delay after Vertical Blank start to start of Vertical Sync (Number of Scan Lines)		0	32
10	Vertical Sync Width (Number of Scan Lines)		3	3
11	Interval between Vertical Blank start and start of Video (Number of Scan Lines of Video Blanking)		20	84
12	Total Scan Lines per Frame (Item 7 + Item 11)		320	384
13	Horizontal Scan Frequency (Line Rate) (Item 8 x Item 12)		19.20 kHz	
14	Number of Character Times per Scan Line		102	
15	Character Clock Rate (Item 13 x Item 14)		1.9584 MHz	
16	Character Time (1 ÷ Item 15)		510.6 ns	
17	Delay after Horizontal Blank start to Horizontal Sync start (Character Times)		5	
18	Horizontal Sync Width (Character Times)		9	
19	Dot Frequency (Item 3 x Item 15)		17.6256 MHz	
20	Dot Time (1 ÷ Item 19)		56.7 ns	
21	Vertical Blanking Output Stop before start of Video (Number of Scan Lines)		1	
22	Cursor Enable on all Scan Lines of a Row? (Yes or No)		Yes	
23	Does the Horizontal Sync Pulse have Serrations during Vertical Sync? (Yes or No)		No	
24	Width of Line Buffer Clock logic "0" state within a Character Time (Number of Dot Time increments)		5	
25	Serration Pulse Width, if used (Character Times)		—	
26	Horizontal Sync Pulse Active state logic level (1 or 0)		1	
27	Vertical Sync Pulse Active state logic level (1 or 0)		1	
28	Vertical Blanking Pulse Active state logic level (1 or 0)		1	

Video Monitor Format: Motorola M3003 or Equivalent.



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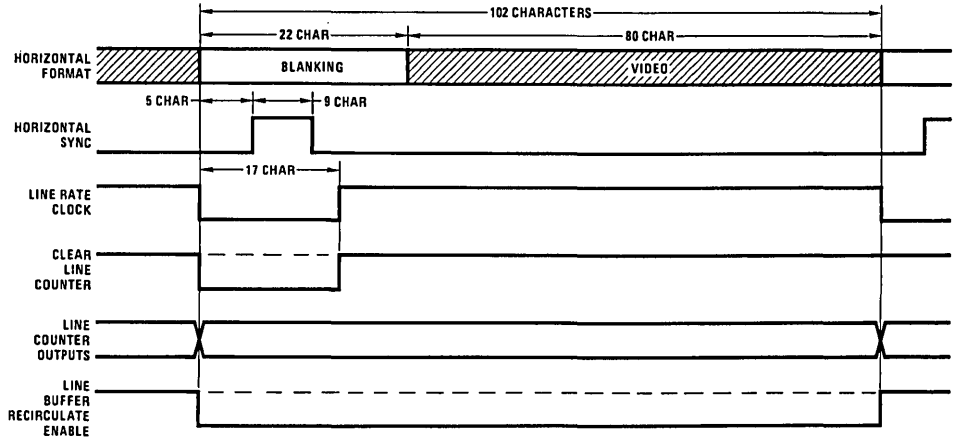
Note: Dashed lines in waveforms denote inactive state logic levels.

FIGURE 27. DP8353 Video Character Signals



TL/F/2206-32

Note: Dashed lines in waveforms denote inactive state logic levels.

FIGURE 28. DP8353 Scan Line Signals

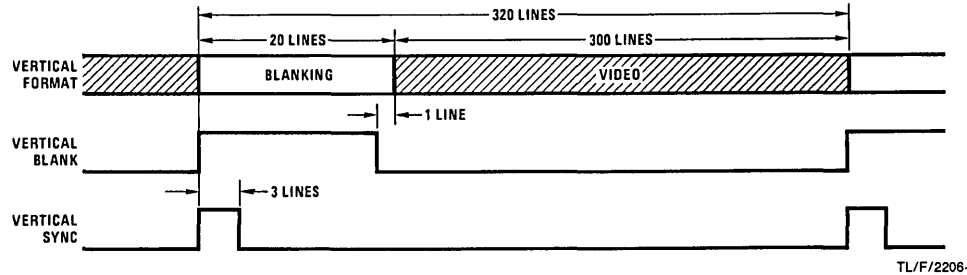


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FIGURE 29. DP8353 60 Hz Refresh Rate Frame Signals

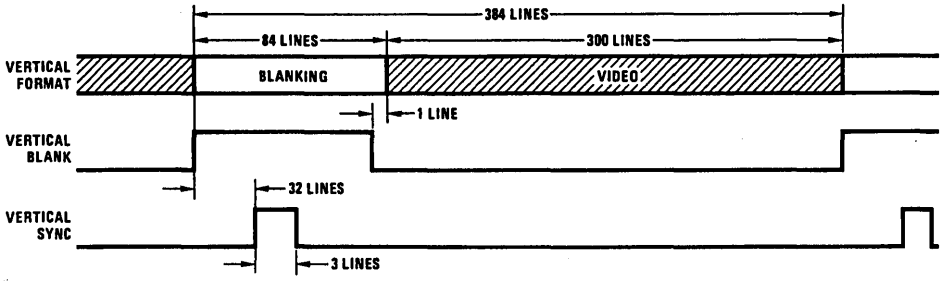

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FIGURE 30. DP8353 50 Hz Refresh Rate Frame Signals

A Low Component Count Video Data Terminal Using the DP8350 CRT Controller and the 8080 CPU

National Semiconductor Corp.
Application Note 199
Al Brilliot

INTRODUCTION

The DP8350 is an I^2L—LS technology integrated circuit, designed to provide all control signals for a cathode ray tube (CRT) display system. This application note explains a system using the DP8350 and the 8080 microprocessor. The design philosophy shows how the DP8350 interfaces to the 8080, completing the function of a video data terminal with a minimum component count. After reading and understanding this application note the reader will realize the ease and flexibility of designing video terminals with the DP8350*. To thoroughly understand this application note the reader must be familiar with the DP8350 and the 8080 microprocessor.

The video data terminal described is divided into the following sections, *(Figure 1)*.

The DP8350 CRT controller (CRTC).

The 8080 μP system which includes ROM, RAM, interrupt instruction port, oscillator, and control support chips.

The character generator.

The communication element.

The keyboard and baud rate select ports.

THE CRTC

The DP8350 generates all the required control and timing signals for displaying video information on the video monitor. Here is a summary of the controller's functions:

Dot clock, control, and counter outputs for the character generator.

Bidirectional RAM address refresh counter for refreshing the video RAM and allowing microprocessor loading to the internal DP8350 registers.

Direct drive horizontal and vertical sync signal outputs.

Direct cursor address location output. The cursor is internally delayed or pipelined, allowing for the access time of video RAM and the character generator ROM, *(Figure 1)*.

THE CPU

The microprocessor provides CRTC, operator, and external machine control for the system. When the CRT controller is not actively refreshing the video RAM, (i.e., during vertical retrace or blank scan lines), the microprocessor is enabled for system housekeeping, *(Figure 2)*. This method of multiplexing the RAM with the CPU and the CRTC eliminates the need for line buffers.

THE CHARACTER GENERATOR

The character generator consists of 3 elements: an address latch to hold the input address to the character ROM allowing for the access time of the ROM; the character ROM that stores the ASCII character in a form for parallel to serial conversion by the shift register; the shift register converts the character ROMs parallel output to serial form. The serial output from the shift register is the true video output, modulating the video monitors electron beam which writes characters on the screen.

*The DP8350 is equivalent to the INS8276.

THE COMMUNICATION ELEMENT

The INS8250 is the asynchronous communication element (ACE) for the data terminal. The ACE allows the CPU portion of the data terminal communication with peripherals or host computers at the correct baud rate, *(Figure 1)*. The ACE is programmed by the CPU to send and receive serial data at the standard baud rates from 110 to 4800 baud. The ACE, in conjunction with the DS1488 and DS1489 line drivers and receivers, also provides full RS-232C synchronous communication if higher baud rates are desired. System communication speed must always be considered to insure the baud rate does not exceed the time required for the CPU to process a data byte. Asynchronous communication at baud rates higher than 4800 are possible by adding a line buffer.

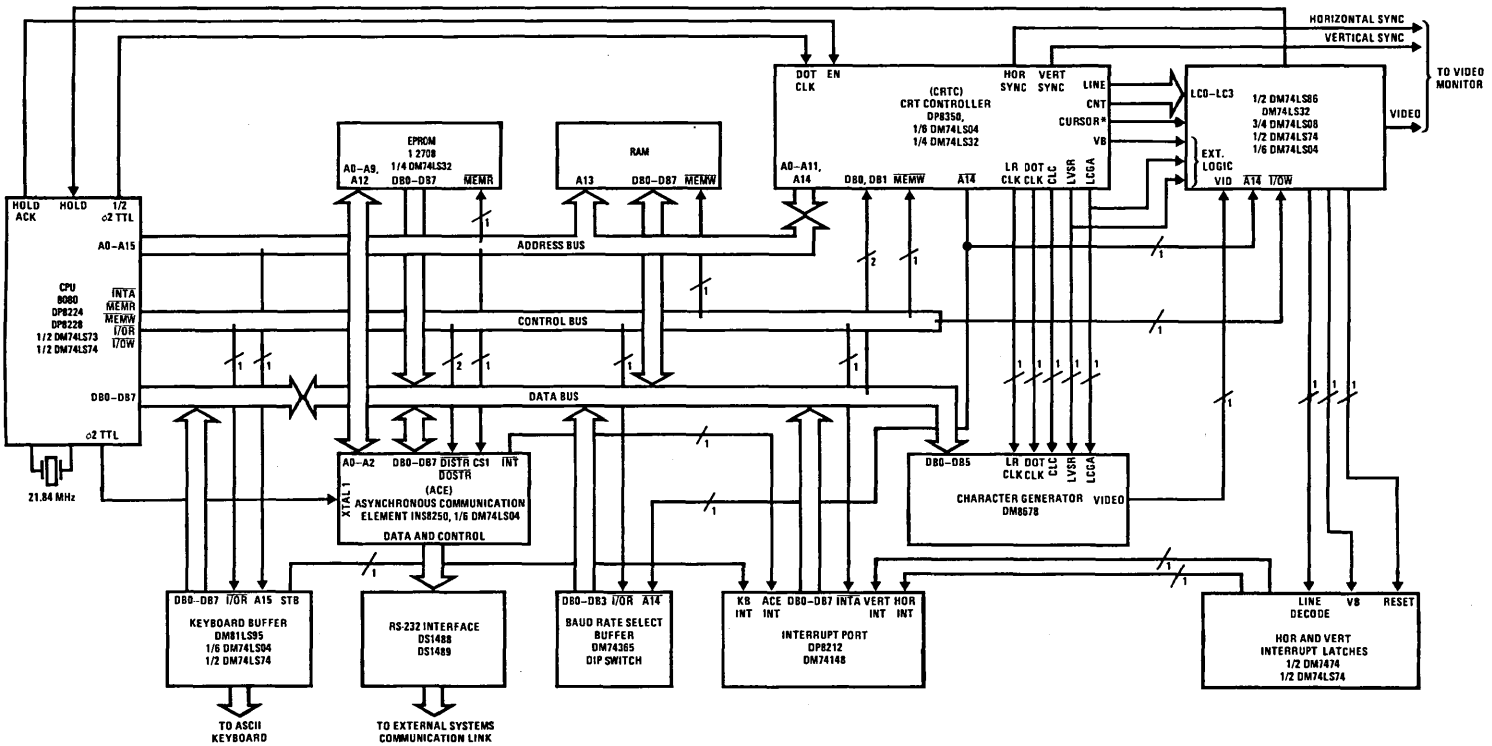
SYSTEM INITIALIZATION

Application of the terminal's power supply resets the microprocessor, the communication element, and the CRT controller. Resetting the ACE is necessary to clear the interrupt. Resetting the CRTC is not absolutely necessary since the microprocessor loads the cursor and top of page registers in the initialization routine.

Following the reset all interrupts are disabled to avoid unwanted interrupts from the CRTC, ACE, or I/O ports. Refer to the initialization routine in the flowchart.

The stack pointer is loaded to the bottom of scratch pad RAM (3FFFH) for use as the register save pointer, *(Figure 3)*.

The entire RAM is written with ASCII spaces generating a cleared screen. After completion of the screen clear loop the CPU writes 000H to the cursor and the top of page registers in the DP8350 CRTC. The routine homes the cursor to the upper left corner of the screen. The top of the page register was loaded with 000H, therefore, the video RAM is refreshed by the CRTC from that starting address to the last address on the screen of video RAM (1920 characters).



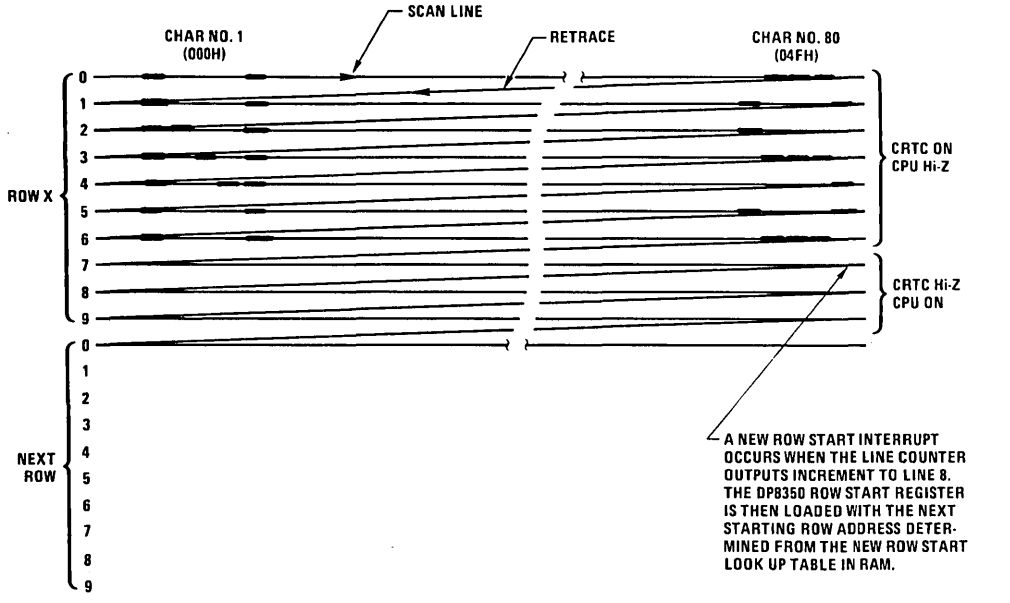
TL/F/5866–1

*The cursor is internally pipelined by the CRTC to allow for access time of the RAM and the character generator.

Abbreviations:

LR CLK	Line Rate Clock
CLC	Clear Line Counter
LVSR	Load Video Shift Register
LCGA	Latch Character Generator Address
Line CNT	Line Counter
EN	Enable
VID	Video
KB INT	Keyboard Interrupt
VB	Vertical Blanking

FIGURE 1. Video Data Terminal Detailed Block Diagram



TL/F/5866–2

FIGURE 2. Row Start Interrupting and Multiplexing the 8080 with the DP8350

The CPU is ready to perform the communication element (ACE) load routine. First, the baud rate divisor for the ACE must be determined. The baud rate select switch is read providing a code which corresponds to the appropriate 16-bit divisor for the ACE. This divisor determines the baud rate at which the ACE will communicate. Any additional programming requirements needed for the ACE to communicate with host computer systems could also be done at this time. The software in this system does not contain any additional programming for the ACE. There are many programming modes related to the ACE. Details of these modes are beyond the scope of this application note.

The row start look-up table, *(Figure 4),* is loaded up by a simple algorithm that loads and adds the data for referencing a row number to that row's starting address. The reference table, *(Figure 5),* is initialized next by direct loading. This table provides the CPU with top of page, bottom of page, next row load, cursor row, and scratch row numbers for system housekeeping.

Finally, the new row start and vertical interrupt latches are cleared, *(Figure 6).* The register pointers are loaded and the CPU is forced in a wait loop with interrupts enabled.

NON-SEQUENTIAL ADDRESSING

The data terminal described here was designed for non-sequential starting row addressing. In many systems sequential row addressing is used. If a character row consists of 10 scan lines the RAM is addressed 10 repetitive times from 000H through 04FH, *(Figure 2).* The next row is refreshed in the same manner from 050H to 09FH. The starting row address is sequential 000H, 050H, 0A0H–EB0H for row numbers 0H, 1H, 2H, −2FH, respectively. Non-sequential row addressing would be equivalent to 050H, 000H, 0A0H–EB0H for row numbers 1H, 0H, −2FH, respectively, *(Figure 3).*

In conjunction with the CPU, non-sequential row addressing is quite easily accomplished with the DP8350 since this is one of the features designed into the part. Accomplishing this task basically requires the following sequence of events. Assume the CRTC has finished writing a video row in the middle of the monitor's screen. This system has a 5 x 7 character font in a 7 x 10 field, *(Figure 2).* At the completion of the last video scan line 7 the CRTC line counters continue to count the last 3 lines. Video is not present since the character is only 7 scan lines high. The blank scan lines are 7, 8, and 9 permitting the CRTC address outputs to be at TRI-STATE®, allowing the CPU to run. When the line counter outputs increment to scan line 8 an interrupt signals the CPU. The interrupt occurring is the new row start interrupt. The interrupt routine fetches the next CRTC row number from the reference table *(Figure 5).* This number is converted to the new starting row address, explained later, and loaded to the CRTC row start register. The CPU finishes the routine by clearing the interrupt, readying itself for the next new row start interrupt. The entire routine takes 1 scan line of time, approximately 64 μs. The CRTC continues to scan the video RAM from that new starting address on for the next 7 repetitive scan lines of the next row. Many advantages become apparent using the non-sequential addressing scheme. Scrolling up or down with the cursor always on the screen may be done faster and easier from a hardware/software standpoint. Exchanging one row with another row is fast since it is not necessary to rewrite the video RAM. Row swapping is useful for higher end terminals requiring row editing functions.

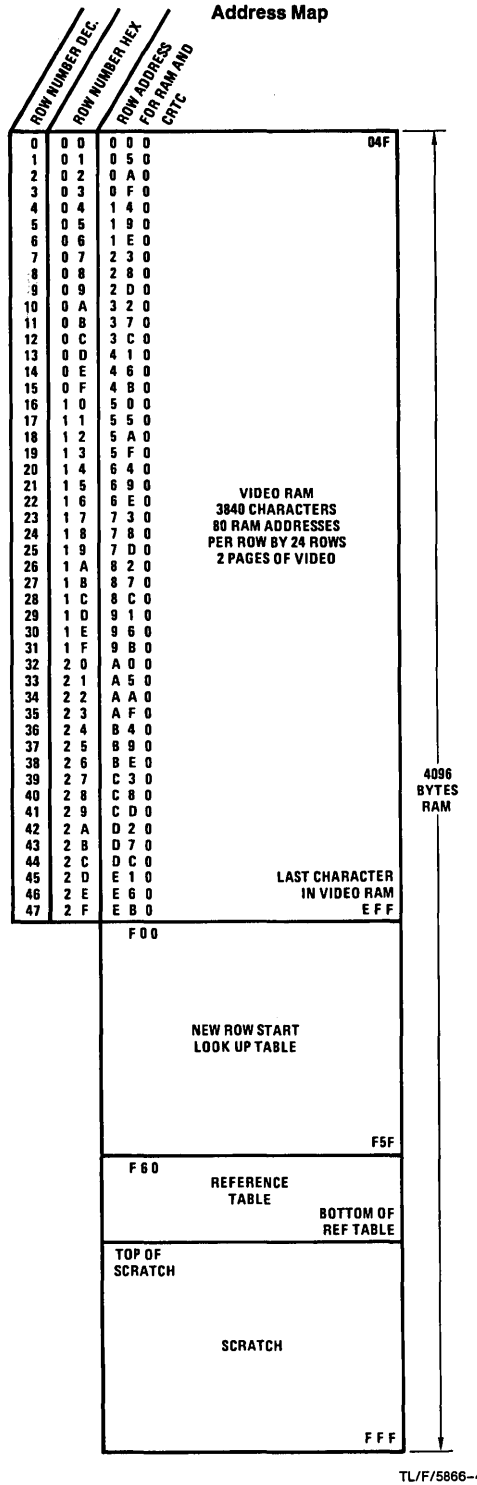


FIGURE 3. RAM Organization

Memory Reference Tables

Page 1

Row Number		NRS High						NRS Low					
		Address				Row Data		Address				Row Data	
Dec	Hex												
0	0 0	3	F	0	0	3	0	3	F	3	0	0	0
1	0 1	3	F	0	1	3	0	3	F	3	1	5	0
2	0 2	3	F	0	2	3	0	3	F	3	2	A	0
3	0 3	3	F	0	3	3	0	3	F	3	3	F	0
4	0 4	3	F	0	4	3	1	3	F	3	4	4	0
5	0 5	3	F	0	5	3	1	3	F	3	5	9	0
6	0 6	3	F	0	6	3	1	3	F	3	6	E	0
7	0 7	3	F	0	7	3	2	3	F	3	7	3	0
8	0 8	3	F	0	8	3	2	3	F	3	8	8	0
9	0 9	3	F	0	9	3	2	3	F	3	9	D	0
10	0 A	3	F	0	A	3	3	3	F	3	A	2	0
11	0 B	3	F	0	B	3	3	3	F	3	B	7	0
12	0 C	3	F	0	C	3	3	3	F	3	C	C	0
13	0 D	3	F	0	D	3	4	3	F	3	D	1	0
14	0 E	3	F	0	E	3	4	3	F	3	E	6	0
15	0 F	3	F	0	F	3	4	3	F	3	F	B	0
16	1 0	3	F	1	0	3	5	3	F	4	0	0	0
17	1 1	3	F	1	1	3	5	3	F	4	1	5	0
18	1 2	3	F	1	2	3	5	3	F	4	2	A	0
19	1 3	3	F	1	3	3	5	3	F	4	3	F	0
20	1 4	3	F	1	4	3	6	3	F	4	4	4	0
21	1 5	3	F	1	5	3	6	3	F	4	5	9	0
22	1 6	3	F	1	6	3	6	3	F	4	6	E	0
23	1 7	3	F	1	7	3	7	3	F	4	7	3	0

Page 2

Row Number		NRS High						NRS Low					
		Address				Row Data		Address				Row Data	
Dec	Hex												
24	1 8	3	F	1	8	3	7	3	F	4	8	8	0
25	1 9	3	F	1	9	3	7	3	F	4	9	D	0
26	1 A	3	F	1	A	3	8	3	F	4	A	2	0
27	1 B	3	F	1	B	3	8	3	F	4	B	7	0
28	1 C	3	F	1	C	3	8	3	F	4	C	C	0
29	1 D	3	F	1	D	3	9	3	F	4	D	1	0
30	1 E	3	F	1	E	3	9	3	F	4	E	6	0
31	1 F	3	F	1	F	3	9	3	F	4	F	B	0
32	2 0	3	F	2	0	3	A	3	F	5	0	0	0
33	2 1	3	F	2	1	3	A	3	F	5	1	5	0
34	2 2	3	F	2	2	3	A	3	F	5	2	A	0
35	2 3	3	F	2	3	3	A	3	F	5	3	F	0
36	2 4	3	F	2	4	3	B	3	F	5	4	4	0
37	2 5	3	F	2	5	3	B	3	F	5	5	9	0
38	2 6	3	F	2	6	3	B	3	F	5	6	E	0
39	2 7	3	F	2	7	3	C	3	F	5	7	3	0
40	2 8	3	F	2	8	3	C	3	F	5	8	8	0
41	2 9	3	F	2	9	3	C	3	F	5	9	D	0
42	2 A	3	F	2	A	3	D	3	F	5	A	2	0
43	2 B	3	F	2	B	3	D	3	F	5	B	7	0
44	2 C	3	F	2	C	3	D	3	F	5	C	C	0
45	2 D	3	F	2	D	3	E	3	F	5	D	1	0
46	2 E	3	F	2	E	3	E	3	F	5	E	6	0
47	2 F	3	F	2	F	3	E	3	F	5	F	B	0

FIGURE 4. New Row Start Look Up Table

Function	Address	Data	Initialized Data
Last Row #	3F60	XY	17
8080 Row #	3F61	XY	00
First Row #	3F62	XY	00
Character #	3F63	XY	00
CRTC Row #	3F64	XY	00
Row Save #	3F65	XY	00
Temp. 1	3F66	XY	00
Temp. 2	3F67	XY	00

FIGURE 5. Reference Table

Command		Function
OUT	40	Clear new row start and vertical interrupt latches
IN	80	Read keyboard
IN	40	Read baud rate select switch

FIGURE 6. Input/Output Space

Device	Address
ROM	0000 to 0FFF
RAM	3000 to 3FFF
CRTC	5000 to 5FFF
ACE	9000 to 9007

*Direct device selecting was used to minimize the system component count.

FIGURE 7. CPU Addressing Space

Row Number		NRS High						NRS Low					
		Address				Row Data		Address				Row Data	
Dec	Hex												
32	2 0	3	F	2	0	3	A	3	F	5	0	0	0

Row Start Address for Row 20H.

3XXX Selects RAM.

5XXX Selects CRTC.

FIGURE 8. Example from the New Row Start Look Up Table

ROW LOADING DETAILS

Obtaining the next starting row address for the CRT controller is accomplished by an addressing and adding scheme from the new row start look-up table. The same scheme is used to determine any needed address, given the row number.

Figure 8 shows a row number and address taken from the new row start look-up table.

The row number is loaded from the reference table in RAM to a register. The CPU determines the starting address from the row number and stores it in a 16-bit pointer register. The higher order 4 bits contain address for the RAM or the CRT controller, *(Figure 7)*.

Here are the details of how this is accomplished. Refer to the new row start interrupt in the software listing the *Figure 8*.

The CPU D-E registers are loaded to point to a row number in the reference table. The number is put in the accumulator and moved into the E register. The D-E register in this example now contains 3F20 which points to NRS HIGH ROW DATA (3A). The addressed data is moved to the accumulator and then to the H register. If it was desired to point to the CRTC then 20H would have been added to it first. The D-E register still contains 3F20H. To obtain the NRS LOW ROW DATA the E register is moved to the accumulator and 30H is added to it. Now the D-E register contains 3F50H and points to NRS LOW ROW DATA (00H). The data is loaded to the accumulator and then to the L register. The H-L registers contain 3A00H which is the starting row address for row number 20H. The method just described is used throughout the terminals program to move the cursor, load the top of page, and load the new starting row address in the CRTC.

VERTICAL INTERRUPT

The vertical interrupt occurs when the CRTC has completed refreshing a video page (1920 characters) of information. Vertical blanking identifies that condition and interrupts the CPU forcing it to the vertical interrupt routine. Refer to the vertical interrupt in the flow chart. The routine moves the first row number to the CRTC row number, updating it so the next new row start load occurs with the top of the page address or the first row of the video screen.

KEYBOARD INTERRUPT

The external keyboard requirements are ASCII outputs with a suitable strobe to interrupt the CPU for keyboard servicing. Refer to the keyboard interrupt in the flow chart. After the keyboard buffer is read the data byte is tested for a (CNTL E), new baud rate command. If the test fails the CPU writes the data byte to the ACE. Passing the test forces the CPU to read the baud switch and load the ACE with the new baud rate.

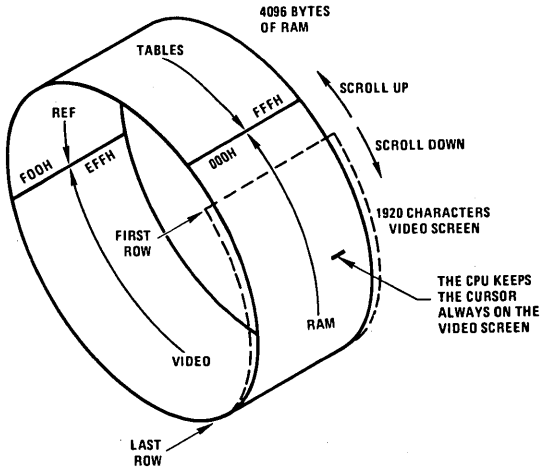
ACE INTERRUPT

As mentioned above, a data byte read from the keyboard that is not a baud rate command enters the accumulator. The CPU writes the data byte from the accumulator to the transmitter holding register in the ACE. The ACE proceeds to shift out the data byte, with the appropriate start and stop bits, serially from the (SOUT) output. The data is shifted to the serial input (SIN) of the ACE and loaded into the receiver holding register. When the register is full the ACE interrupts the CPU, initializating the ACE service routine. Refer to the ACE interrupt in the flow chart.

The CPU reads the receiver holding register in the ACE. Reading the ACE resets the interrupt. The data byte now resides in the accumulator. The CPU tests for a control or an escape function. The function is executed if test conditions are met. Refer to the keyboard interrupt routine in the software listing. The data byte is written to the video RAM at the cursor address which appears on the monitor screen. The cursor and character numbers are incremented as long as it is not at the end of a row. A character at the end of a row requires further testing to recognize the following situations. Is it the last row on the monitor's screen? Or is it on the maximum row of the video RAM? Essentially, the cursor is forced to stay visible on the video monitor's screen and video RAM is always kept out of scratch pad RAM, *(Figure 9)*.

FULL/HALF DUPLEX OPERATION

The data terminal and a host computer in the full duplex mode of operation would receive the serial information, process it, and send it back to the SIN input of ACE. Using the terminal in a stand-alone mode for testing, the serial out SOUT is tied to the serial in SIN of the ACE. In the half duplex mode a data byte is sent to the host computer at the same time it is sent to the terminal. When the data terminal is set up to communicate with a host computer the full duplex mode of operation is desirable.



The video screen is allowed to scroll only through the video RAM (000H to EFFH). The CPU keeps the video screen within these bounds by loading the new row start register with that address range only (row 00H to 2FH).

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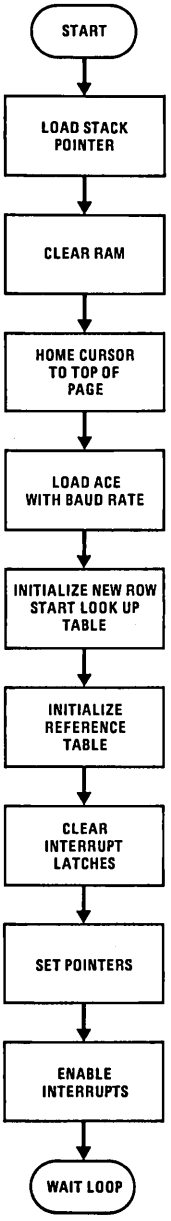
FIGURE 9. Drum Analogy for the RAM

DP8350/8080 Video Data Terminal Basic Software Flow Chart

Initialization



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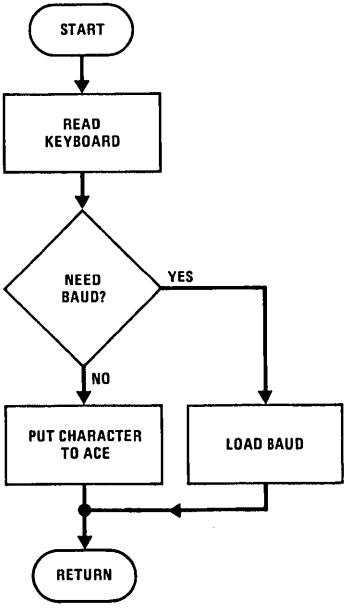
Keyboard Interrupt



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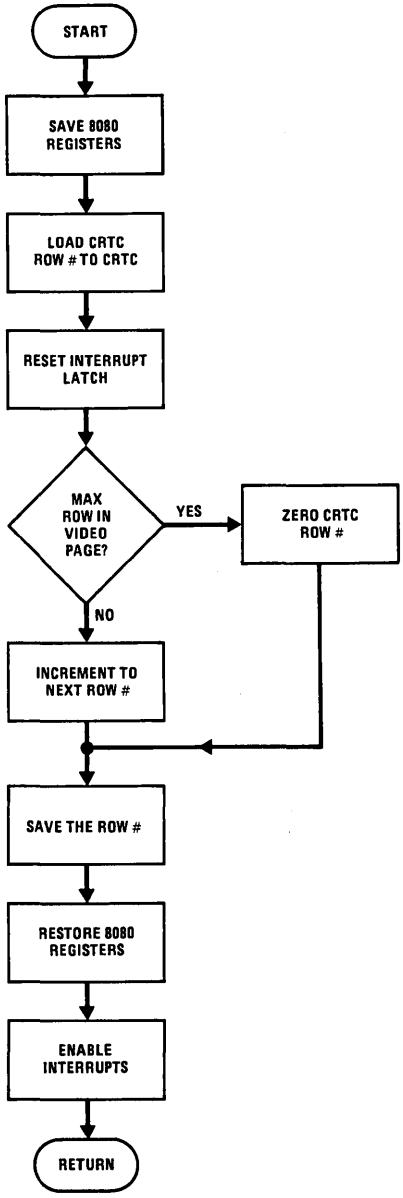
DP8350/8080 Video Data Terminal Basic Software Flow Chart (Continued)

New Row Start Interrupt



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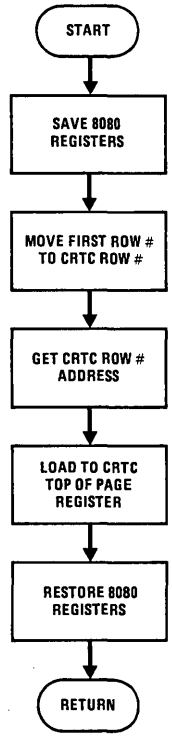
Vertical Interrupt



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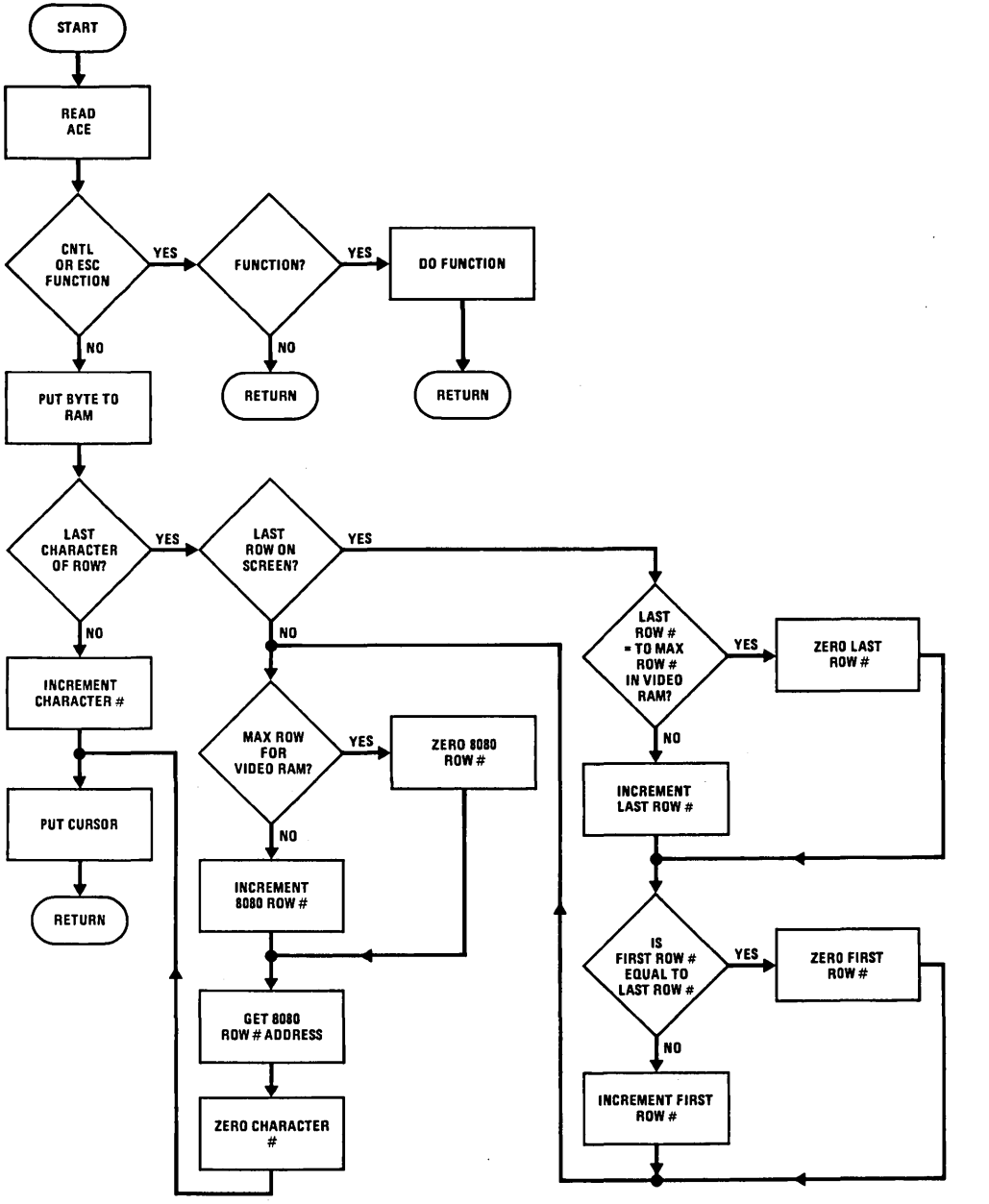
DP8350/8080 Video Data Terminal Basic Software Flow Chart (Continued)

ACE Interrupt



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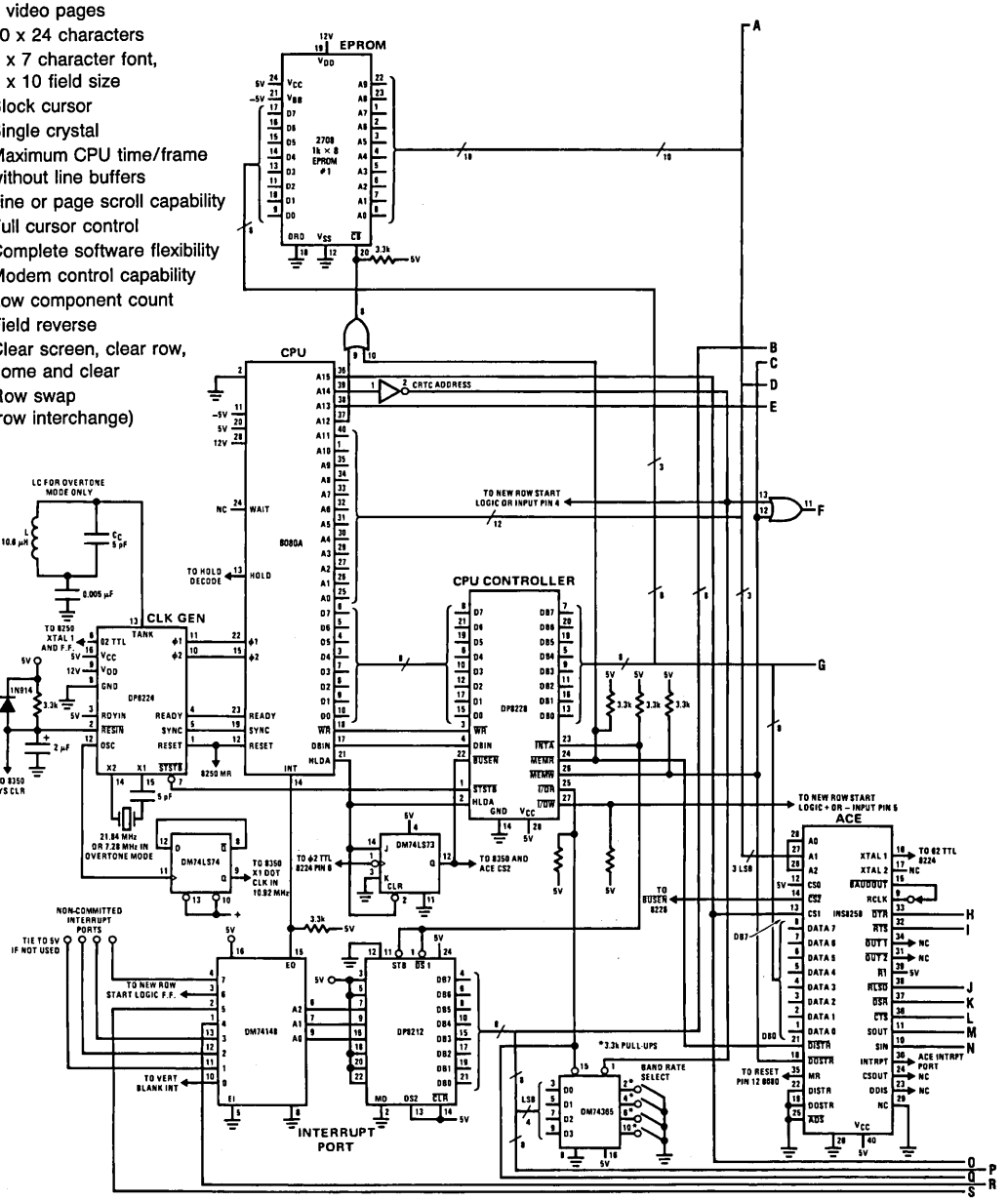
FEATURES

- Keyboard input port
- Serial I/O up to 9600 baud
  - 4 kbytes RAM
  - 1 kbyte ROM
- 2 video pages
- 80 x 24 characters
- 5 x 7 character font, 7 x 10 field size
- Block cursor
- Single crystal
- Maximum CPU time/frame without line buffers
- Line or page scroll capability
- Full cursor control
- Complete software flexibility
- Modem control capability
- Low component count
- Field reverse
- Clear screen, clear row, home and clear
- Row swap (row interchange)



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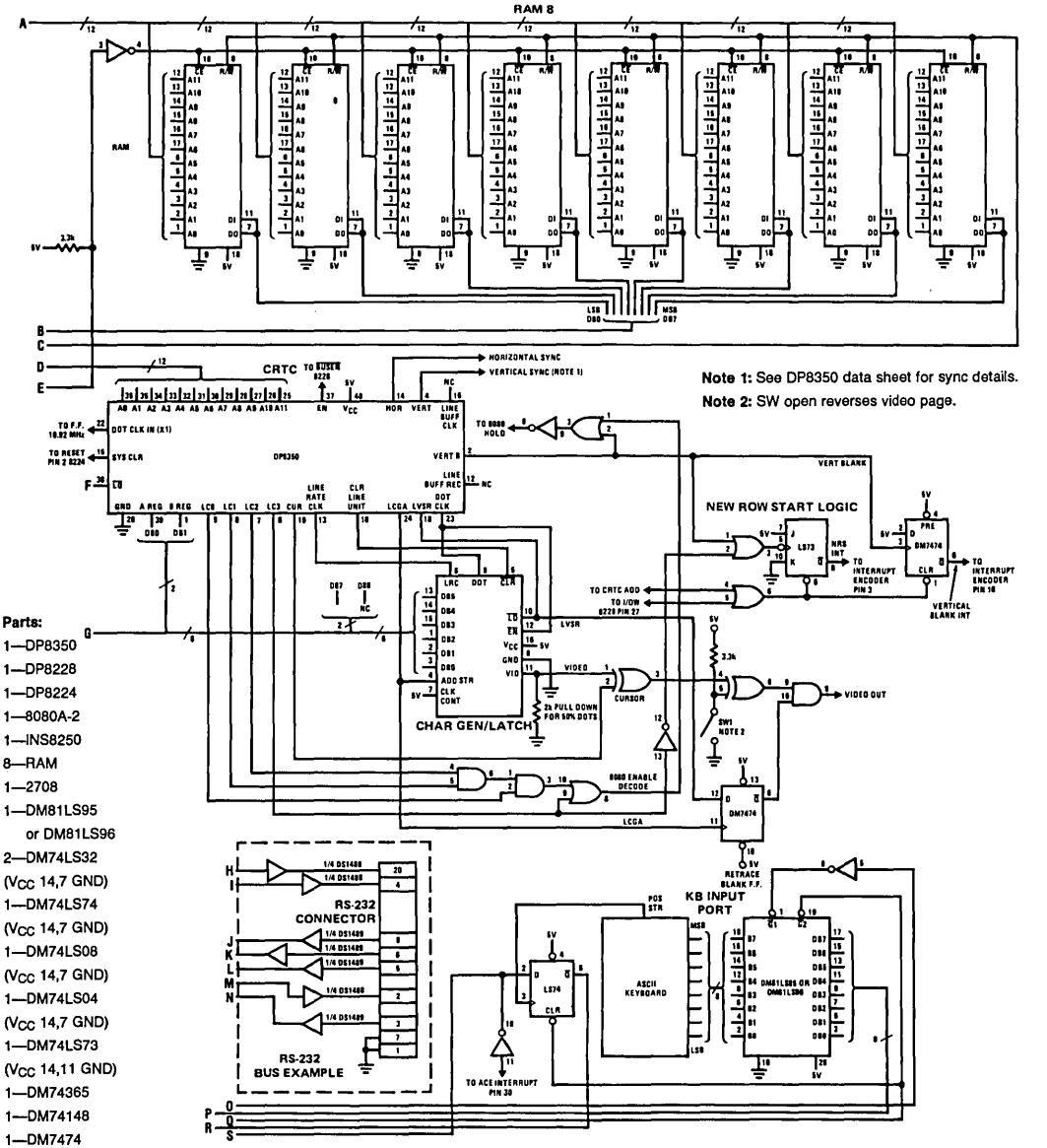

Note 1: See DP8350 data sheet for sync details.

Note 2: SW open reverses video page.

Parts:

1—DP8350
1—DP8224
1—8080A-2
1—INS8250
8—RAM
1—2708
1—DM81LS95
or DM81LS96
2—DM74LS32
(V_{CC} 14,7 GND)
1—DM74LS74
(V_{CC} 14,7 GND)
1—DM74LS08
(V_{CC} 14,7 GND)
1—DM74LS04
(V_{CC} 14,7 GND)
1—DM74LS73
(V_{CC} 14,11 GND)
1—DM74365
1—DM74148
1—DM7474
1—DP8212
1—DM74LS86
1—char. gen/latch
2—Res. arrays,
3.3k
1—21.84 MHz
Xtal
Bypass capacitors
on all parts

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```
1                       .TITLE CRTC ,'8080A 02/15/78'
2
3                 ;** NATIONAL SEMICONDUCTOR'S
4                 ;   SERIES PROGRAMMABLE CRT CONTROLLER BOARD **
5
6                 ;AL BRILLIOTT-JIM TROUTNER
7
8       0060              LASTROW =               060
9       0061              ROW8080 =               061
10      0062              FIRSTRO =               062
11      0063              CHARNUM =               063
12      0064              CRTCROW =               064
13      0065              ROWSAVE =               065
14      0066              TEMP1   =               066
15      0067              TEMP2   =               067
16      0068              IMASK   =               068
17
18 0000                   .=0000
19 0000 F3        START:  DI                      ;DISABLE INTERRUPTS
20 0001 31FF3F            LXI     SP,03FFF        ;LOAD STACK POINTER
21 0004 C33B00            JMP     INIT            ;JUMP TO INITILIZE ROUTINE
22 0007                   .=0008
23 0008 C32502            JMP     NEWRO           ;NEW ROW START INTERRUPT
24 000B                   .=0010
25 0010 C34A01            JMP     INTACE          ;ACE INTERUPT
26 0013                   .=0018
27 0018 C33601            JMP     INTKB           ;KEYBOARD INTERUPT
28 001B                   .=0038
29 0038 C34F02            JMP     VERTI           ;VERTICAL INTERUPT
30 003B 210030 INIT:      LXI     H,03000         ;1ST RAM ADDRESS
31 003E 0E20              MVI     C,020           ;ASCII SPACE INTO C REG
32 0040 3E3F              MVI     A,03F           ;MAX RAM ADDRESS
33 0042 71        CLRAM:  MOV     M,C             ;ASCII SPACE INTO MEM
34 0043 23                INX     H               ;NEXT RAM ADDRESS
35 0044 BC                CMP     H               ;MAX RAM ADDRESS?
36 0045 C24200            JNZ     CLRAM           ;IF NO THEN NEXT ADD.
37 0048 0E00              MVI     C,000
38 004A 3E40              MVI     A,040
39 004C 71        CLRAM1: MOV     M,C
40 004D 23                INX     H
41 004E BC                CMP     H
42 004F C24C00            JNZ     CLRAM1
43 0052 CD8700            CALL    HMCUR           ;GO TO CUR HOME ROUTINE
44 0055 CD9300            CALL    BAUD            ;GO TO BAUD LOAD ROUTINE
45
46                        ;NEW ROW START LOOK UP TABLE GENERATION
47
48 0058 21003F            LXI     H,03F00         ;N.R.S. HIGH ADDRESS
49 005B 11303F            LXI     D,03F30         ;N.R.S. LOW ADDRESS
50 005E 010030            LXI     B,03000         ;N.R.S. ADDRESS DATA
51 0061 70        NRS:    MOV     M,B             ;STORE TO N.R.S. DATA TABLE "
52 0062 79                MOV     A,C             ;N.R.S. DATA LOW TO ACC.
53 0063 12                STAX    D               ;STORE TO N.R.S. DATA TABLE L
54 0064 C650              ADI     050             ;ACC READY FOR NEXT LOAD
55 0066 4F                MOV     C,A             ;ACC TO N.R.S. DATA HIGH
56 0067 78                MOV     A,B             ;N.R.S. DATA TO ACC
57 0068 CE00              ACI     000             ;ADD CARRY BIT TO DATA HIGH
58 006A 47                MOV     B,A             ;MOVE RESULT TO N.R.S. DATA H
59 006B 2C                INR     L               ;INCREMENT N.R.S. HIGH ADD
60 006C 1C                INR     E               ;INCREMENT N.R.S. LOW ADD
61 006D 7B                MOV     A,E             ;N.R.S. ADD LOW TO ACC
62 006E FE60              CPI     LASTROW         ;MAX TABLE ADDRESS
63 0070 C26100            JNZ     NRS             ;IF FALSE JUMP
64
65                        ;REFERENCE TABLE INITILIZE
66
67 0073 3E17              MVI     A,017           ;LAST ROW NUMBER TO ACC.
68 0075 12                STAX    D               ;STORE TO REFERENCE TABLE
69
70                        ;CLEAR PERIPHERAL INTERRUPT FLOPS
71
72 0076 D340              OUT     040             ;N.R.S. INTERRUPT CLEAR
73 0078 DB80              IN      080             ;KEYBOARD INTERRUPT CLEAR
74
75                        ;SET UP POINTERS
76
77 007A 11603F            LXI     D,03F60         ;POINT D-E TO REFERENCE TABLE
78 007D 210030            LXI     H,03000         ;POINT H-L TO 1ST RAM LOCATI^
79 0080 010090            LXI     B,09000         ;POINT B-C TO ACE
80
81                        ;WAIT LOOP FOR INTERUPTS
82
83 0083 FB        BACK:   EI                      ;ENABLE INTERRUPTS
84 0084 C38300            JMP     BACK            ;LOOP UNTIL INTERRUPTED
85
86                        ;HOME UP CURSOR
87
88 0087 210050 HMCUR:     LXI     H,05000         ;POINT B-C TO CRTC
89 008A 3E02              MVI     A,002           ;T.O.P. REGISTER SELECT
90 008C 77                MOV     M,A             ;T.O.P. LOAD
91 008D 3C                INR     A               ;CURSOR REGISTER SELECT
92 008E 77                MOV     M,A             ;CURSOR LOADS TO T.O.P.
93 008F 210030            LXI     H,03000         ;POINT H-L TO 1ST RAM ADD.
94 0092 C9                RET                     ;RETURN
95
```

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```
                        ;BAUD RATE SELECT
                        ;
0093 D5       BAUD:     PUSH    D             ;SAVE D-E REGISTERS
0094 DB40               IN      040           ;READ BAUD SELECT CODE
0096 E60F               ANI     00F           ;ZERO THE HIGH ORDER 4 BITS
0098 FE00               CPI     000
009A CAD400             JZ      B110          ;110 BAUD ROUTINE
009D FE01               CPI     001
009F CADA00             JZ      B150          ;150 BAUD ROUTINE
00A2 FE02               CPI     002
00A4 CAE000             JZ      B300          ;300 BAUD ROUTINE
00A7 FE03               CPI     003
00A9 CAE600             JZ      B600          ;600 BAUD ROUTINE
00AC FE04               CPI     004
00AE CAEC00             JZ      B1200         ;1200 BAUD ROUTINE
00B1 FE05               CPI     005
00B3 CAF200             JZ      B1800         ;1800 BAUD ROUTINE
00B6 FE06               CPI     006
00B8 CAF800             JZ      B2000         ;2000 BAUD ROUTINE
00BB FE07               CPI     007
00BD CAFE00             JZ      B2400         ;2400 BAUD ROUTINE
00C0 FE08               CPI     008
00C2 CA0401             JZ      B3600         ;3600 BAUD ROUTINE
00C5 FE09               CPI     009
00C7 CA0A01             JZ      B4800         ;4800 BAUD ROUTINE
00CA FE0A               CPI     00A
00CC CA1001             JZ      B7200         ;7200 BAUD ROUTINE
00CF FE0B               CPI     00B
00D1 CA1601             JZ      B9600         ;9600 BAUD ROUTINE
                        ;
                        ;BAUD RATE SET UP ROUTINES
                        ;
00D4 116305 B110:       LXI     D,00563       ;110 BAUD DIVISOR
00D7 C31C01             JMP     ACELD         ;GO TO ACE LOAD ROUTINE
00DA 11F303 B150:       LXI     D,003F3       ;150 BAUD DIVISOR
00DD C31C01             JMP     ACELD
00E0 11F901 B300:       LXI     D,001F9       ;300 BAUD DIVISOR
00E3 C31C01             JMP     ACELD
00E6 11FC00 B600:       LXI     D,000FC       ;600 BAUD DIVISOR
00E9 C31C01             JMP     ACELD
00EC 117E00 B1200:      LXI     D,0007E       ;1200 BAUD DIVISOR
00EF C31C01             JMP     ACELD
00F2 115400 B1800:      LXI     D,00054       ;1800 BAUD DIVISOR
00F5 C31C01             JMP     ACELD
00F8 114C00 B2000:      LXI     D,0004C       ;2000 BAUD DIVISOR
00FB C31C01             JMP     ACELD
00FE 113F00 B2400:      LXI     D,0003F       ;2400 BAUD DIVISOR
0101 C31C01             JMP     ACELD
0104 112A00 B3600:      LXI     D,0002A       ;3600 BAUD DIVISOR
0107 C31C01             JMP     ACELD
010A 112000 B4800:      LXI     D,00020       ;4800 BAUD DIVISOR
010D C31C01             JMP     ACELD
0110 111500 B7200:      LXI     D,00015       ;7200 BAUD DIVISOR
0113 C31C01             JMP     ACELD
0116 111000 B9600:      LXI     D,00010       ;9600 BAUD DIVISOR
0119 C31C01             JMP     ACELD
                        ;
                        ;ACE LOAD ROUTINE
                        ;
011C 010390 ACELD:      LXI     B,09003       ;POINT B C TO ACE
011F 3E83               MVI     A,083         ;INIT BAUD LOAD - 8 BITS
0121 02                 STAX    B             ;DO INIT BAUD LOAD
0122 0E01               MVI     C,001         ;POINT TO BAUD HIGH
0124 7A                 MOV     A,D           ;GET BAUD HIGH
0125 02                 STAX    B             ;STORE BAUD HIGH TO ACE
0126 0E00               MVI     C,000         ;POINT ACE TO BAUD LOW
0128 7B                 MOV     A,E           ;GET BAUD LOW
0129 02                 STAX    B             ;STORE BAUD LOW TO ACE
012A 0E03               MVI     C,003         ;RESET DLAB TO ZERO
012C 79                 MOV     A,C           ;INIT ACE T/R
012D 02                 STAX    B             ;PUT TO ACE
012E 0E01               MVI     C,001         ;INTERRUPT ENABLE REG
0130 79                 MOV     A,C           ;SELECT RECEIVED DATA INTERR''
0131 02                 STAX    B             ;LOAD IT
0132 0E00               MVI     C,000         ;RESTORE B-C ACE POINTER
0134 D1                 POP     D             ;RESTORE D-E REGISTERS
0135 C9                 RET                   ;RETURN
                        ;
                        ;KEYBOARD INTERRUPT ROUTINE
                        ;
0136 DB80     INTKB:    IN      080           ;READ KEYBOARD
0138 FB                 EI                    ;ENABLE INTERRUPTS
0139 FE05               CPI     005           ;NEED BAUD RATE? (CNTL E)
013B CA9300             JZ      BAUD          ;IF YES GO TO BAUD ROUTINE
013E FE12               CPI     012           ;INVERT NEXT CNTL R
0140 CA4803             JZ      IVERTN
0143 FE13               CPI     013           ;INVERT ROW CNTL S
0145 CA5403             JZ      IVERTR
0148 02                 STAX    B             ;STORE BYTE TO ACE
0149 C9                 RET                   ;RETURN
```

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```
187                             ;ACE INTERUPT ROUTINE
188
189 014A 0A       INTACE:  LDAX    B              ;LOAD ACE DATA BYTE TO ACC.
190 014B FB                EI                     ;ENABLE INTERRUPTS
191 014C FE7E              CPI     07E
192 014E CA7001            JZ      FUNC           ;TEST FOR ESC COMAMD
193 0151 FE7F              CPI     07F            ;TEST FOR DEL COMAND
194 0153 CA7001            JZ      FUNC
195 0156 5F                MOV     E,A            ;SAVE CHAR IN REG E
196 0157 E660              ANI     060            ;MASK OUT BITS FOR CNTL TEST
197 0159 CA7001            JZ      FUNC           ;IF ZERO JMP TO CNTL FUNC
198 015C 3A683F            LDA     03F68          ;LOAD INVERT MASK
199 015F B3                ORA     E              ;OR MASK AND CHAR
200 0160 77                MOV     M,A            ;STORE DATA BYTE TO RAM
201
202                             ;ADVANCE CURSOR
203
204 0161 1E63     ADCUR:   MVI     E,CHARNUM      ;POINT B-C TO CHAR #
205 0163 1A                LDAX    D              ;LOAD CHAR # TO ACC.
206 0164 23                INX     H              ;NEXT CHAR LOCATION
207 0165 FE4F              CPI     04F            ;LAST CHAR OF ROW?
208 0167 CABE01            JZ      NXRO           ;IF TRUE JUMP TO NEXT ROW
209 016A C601              ADI     001            ;INCREMENT CHAR #
210 016C 12                STAX    D              ;STORE CHAR # TO RAM REF.
211 016D C3B301            JMP     PCUR           ;PUT CURSOR
212
213                             ;TEST FOR FUNCTION
214
215 0170 7B       FUNC:    MOV     A,E
216 0171 FE01              CPI     001            ;HOME AND CLEAR CNTL A (SOH)
217 0173 CA0000            JZ      START          ;
218 0176 FE0D              CPI     00D            ;CARRAGE RETURN
219 0178 CA6E02            JZ      CR
220 017B FE11              CPI     011            ;SAVE ROW # CNTL Q (DC1)
221 017D CA7B02            JZ      SAVRO
222 0180 FE0C              CPI     00C            ;ADVANCE CURSOR CNTL L (FF)
223 0182 CA6101            JZ      ADCUR
224 0185 FE02              CPI     002            ;HOME UP CNTL B (STX)
225 0187 CAA402            JZ      HOME
226 018A FE1A              CPI     01A            ;SWAP   CNTL Z (SUB)
227 018C CAB502            JZ      SWAP
228 018F FE0A              CPI     00A            ;LINEFEED
229 0191 CA8D02            JZ      LF
230 0194 FE08              CPI     008            ;BACKSPACE CNTL H (BS)
231 0196 CAE002            JZ      BS
232 0199 FE0B              CPI     00B            ;UP CURSOR CNTL K (VT)
233 019B CAF102            JZ      UPCUR
234 019E FE18              CPI     018            ;CLEAR ROW CNTL X (CAN)
235 01A0 CA3003            JZ      CLROW
236 01A3 FE07              CPI     007            ;RING BELL CNTL G (BEL)
237 01A5 CA4503            JZ      BELL
238 01A8 FE12              CPI     012            ;INVERT NEXT CNTL R (DC2)
239 01AA CA4803            JZ      IVERTN
240 01AD FE13              CPI     013            ;INVERT ROW CNTL S (DC3)
241 01AF CA5403            JZ      IVERTR
242 01B2 C9                RET                    ;RETURN
243
244                             ;STORE CURSOR TO CRTC FROM H-L REGISTERS
245
246 01B3 7C       PCUR:    MOV     A,H            ;H REG TO ACC.
247 01B4 C620              ADI     020            ;SET H-L REG TO CRTC ADD.
248 01B6 67                MOV     H,A            ;H IS CRTC ADD.
249 01B7 3603              MVI     M,003          ;CURSOR REGISTER SELECT
250 01B9 7C                MOV     A,H            ;H REG SET BACK TO VIDIO RAM
251 01BA D620              SUI     020            ;ADDRESS
252 01BC 67                MOV     H,A
253 01BD C9                RET                    ;RETURN
254
255
256                             ;LAST ROW ON SCREEN
257
258 01BE CDDC01   NXRO:    CALL    NXRO1          ;GO TO NEXT ROW SUBROUTINE
259 01C1 CDF301            CALL    ZCHAR          ;ZERO CHARACTER
260 01C4 E5       CLROW3:  PUSH    H              ;SAVE H,L
261 01C5 1E60              MVI     E,LASTROW      ;POINT D,E TO LASTROW
262 01C7 1A                LDAX    D
263 01C8 C601              ADI     001            ;POINT AC TO FIRST ROW OFF SC
264 01CA FE30              CPI     030            ;CK IF LAST ROW IN RAM
265 01CC CAD701            JZ      ROZERO
266 01CF CD8302   LOOP5:   CALL    LDHL1          ;LOAD H,L WITH ADD. OF LASTRO
267 01D2 CD3B03            CALL    CLROW2
268 01D5 E1                POP     H              ;RESTORE H,L
269 01D6 C9                RET
270
271 01D7 3E00     ROZERO:  MVI     A,000          ;LOAD ROW ZERO
272 01D9 C3CF01            JMP     LOOP5
273
```

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```
                        ;NEXT ROW
                        ;
01DC 1E60   NXRO1:  MVI     E,LASTROW       ;POINT D-E REG TO LAST ROW
01DE 1A             LDAX    D               ;PUT LAST ROW # TO ACC.
01DF EB             XCHG                    ;EXCHANGE H-L WITH D-E
01E0 23             INX     H               ;H-L IS NOW AT 8080 ROW #
01E1 BE             CMP     M               ;COMPARE LAST ROW # WITH
01E2 CA0502         JZ      SCROLL          ;8080 ROW # IF TRUE SCROLL
                        ;
                        ;INCREMENT 8080 ROW #
                        ;
01E5 3E2F   INCRO:  MVI     A,02F           ;TEST FOR MAX ROW AND
01E7 BE             CMP     M               ;JUMP TO ZERO ROW IF TRUE
01E8 CAFB01         JZ      ZROW            ;ZERO ROW
01EB 34             INR     M               ;INCREMENT THE 8080 ROW #
01EC EB             XCHG                    ;POINT H-L TO CHAR #
01ED 1E61           MVI     E,ROW8080
01EF CD8202         CALL    LDHL
01F2 C9             RET                     ;RETURN
                        ;
                        ;ZERO CHARACTER
                        ;
01F3 3E00   ZCHAR:  MVI     A,000           ;PUT CHAR # TO ZERO
01F5 32633F         STA     03F63           ;AND STORE
01F8 C3B301         JMP     PCUR            ;GO TO PUT CURSOR ROUTINE
                        ;
                        ;ZERO 8080 ROW #
                        ;
01FB 3600   ZROW:   MVI     M,000           ;8080 ROW # TO ZERO
01FD 2E00           MVI     L,000           ;N.R.S. ADDRESS HIGH
01FF 56             MOV     D,M             ;N.R.S. DATA HIGH TO D REG
0200 2E30           MVI     L,030           ;N.R.S. ADDRESS LOW
0202 5E             MOV     E,M             ;N.R.S. DATA LOW TO E REG
0203 EB             XCHG                    ;EXCHANGE H-L WITH D-E
0204 C9             RET                     ;RETURN
                        ;
                        ;ROW SCROLL
                        ;
0205 2B     SCROLL: DCX     H               ;POINT H-L TO LAST ROW#
0206 3E2F           MVI     A,02F           ;BEFORE SCRATCH TABLES.
0208 BE             CMP     M               ;TEST FOR THE LAST ROW.
0209 CA1902         JZ      ZLRO            ;JUMP TO ZERO LAST ROW IF TR
020C 34             INR     M               ;INCREMENT TO NEXT ROW.
                        ;
                        ;
                        ;
020D 2E62   ROLO:   MVI     L,FIRSTRO       ;POINT H-L TO FIRST ROW#
020F BE             CMP     M               ;IS FIRST LOW = TO LAST ROW.
0210 CA1E02         JZ      ZFRO            ;JUMP TO ZERO FIRST R
0213 34             INR     M               ;INCREMENT TO NEXT ROW
0214 2E61           MVI     L,ROW8080       ;POINT H-L TO 8080 ROW
0216 C3E501         JMP     INCRO           ;GO TO INCREMENT ROW ROUTINE
                        ;
                        ;
                        ;
0219 3600   ZLRO:   MVI     M,000           ;PUT LAST ROW# TO ZERO
021B C30D02         JMP     ROLO            ;GO TO ROUTINE FOR FIRST ROW
                        ;
                        ;
021E 3600   ZFRO:   MVI     M,000           ;PUT FIRST ROW# TO ZERO
0220 2E61           MVI     L,ROW8080       ;POINT H-L TO 8080 ROW
0222 C3E501         JMP     INCRO           ;GO TO INCREMENT ROW ROUTINE
                        ;
                        ;NEW ROW START INTERRUPT
                        ;
0225 F5     NEWRO:  PUSH    PSW             ;SAVE ACC AND FLAGS
0226 E5             PUSH    H               ;SAVE H-L REG
0227 D5             PUSH    D
0228 11643F         LXI     D,03F64         ;POINT D-E TO CRTCROW #
022B 1A             LDAX    D               ;LOAD ACC WITH CRTC ROW #
022C 5F             MOV     E,A             ;N.R.S. DATA ADD HIGH TO E
022D 1A             LDAX    D               ;ROW DATA HIGH INTO ACC
022E C620           ADI     020
0230 67             MOV     H,A             ;N.R.S. DATA ADD HIGH INTO H
0231 7B             MOV     A,E
0232 C630           ADI     030             ;ACC TO N.R.S. DATA LOW
0234 5F             MOV     E,A             ;N.R.S. DATA ADD LOW TO E REG
0235 1A             LDAX    D               ;ROW DATA LOW TO ACC
0236 6F             MOV     L,A             ;N.R.S DATA ADD LOW INTO L
0237 3601           MVI     M,001           ;STORE N.R.S. TO CRTC
0239 D340           OUT     040             ;RESET N.R.S. AND VERT INTER
023B 1E64           MVI     E,CRTCROW
023D 1A             LDAX    D
023E FE2F           CPI     02F             ;TEST FOR CRTC MAX ROW
0240 CA4A02         JZ      ZCRTC           ;IF TRUE ZERO ACC
0243 3C             INR     A               ;INCREMENT TO NEXT ROW
0244 12     LOOP:   STAX    D               ;STORE NEXT ROW NUMBER
0245 D1             POP     D
0246 E1             POP     H               ;RESTORE H-L REG
0247 F1             POP     PSW             ;RESTORE ACC AND FLAGS
0248 FB             EI
0249 C9             RET                     ;RETURN
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```
368                             ;ZERO CRTCROW
369
370 024A 3E00    ZCRTC:  MVI     A,000           ;ZERO ACC
371 024C C34402          JMP     LOOP
372
373                             ;VERTICAL INTERRUPT
374
375 024F F5      VERTI:  PUSH    PSW             ;SAVE ACC AND FLAGS
376 0250 E5              PUSH    H               ;SAVE H REG
377 0251 D5              PUSH    D
378 0252 1E62            MVI     E,FIRSTRO       ;POINT D-E TO FIRST ROW #
379 0254 1A              LDAX    D               ;LOAD 1ST ROW # INTO ACC
380 0255 1E64            MVI     E,CRTCROW       ;POINT D-E TO CRTCROW #
381 0257 12              STAX    D               ;UPDATE CRTCROW #
382 0258 E63F            ANI     03F             ;REMOVE MARKER
383 025A 5F              MOV     E,A             ;POINT H L TO CRTC FIRST ROW
384 025B 1A              LDAX    D
385 025C C620            ADI     020
386 025E 67              MOV     H,A
387 025F 7B              MOV     A,E
388 0260 C630            ADI     030
389 0262 5F              MOV     E,A
390 0263 1A              LDAX    D
391 0264 6F              MOV     L,A
392 0265 3602            MVI     M,002           ;STORE TOP OF PAGE
393 0267 D340            OUT     040
394 0269 D1              POP     D
395 026A E1              POP     H
396 026B F1              POP     PSW             ;RESTORE ACC AND FLAGS
397 026C FB              EI
398 026D C9              RET                     ;RETURN
399
400                             ;CARRAGE RETURN
401
402 026E 1E63    CR:     MVI     E,CHARNUM       ;POINT D-E TO CHAR #
403 0270 3E00            MVI     A,000
404 0272 12              STAX    D
405 0273 1E61            MVI     E,ROW8080
406 0275 CD8202          CALL    LDHL
407 0278 C3B301          JMP     PCUR            ;CURSOR TO THE BEGINNING OF R
408
409                             ;SAVE ROW
410
411 027B 1E61    SAVRO:  MVI     E,ROW8080       ;POINT D-E TO 8080 ROW#
412 027D 1A              LDAX    D               ;PUT 8080 ROW # TO ACC
413 027E 1E65            MVI     E,ROWSAVE       ;POINT D-E TO ROW SAVE
414 0280 12              STAX    D               ;STORE ROW SAVE # IN REF TAB'
415 0281 C9              RET                     ;RETURN
416
417             ;               H-L ROW DATA LOAD ROUTINE
418
419 0282 1A      LDHL:   LDAX    D               ;LOAD ACC WITH D-E DATA
420 0283 5F      LDHL1:  MOV     E,A             ;POINT D-E TO N. R. S.  DATA HI
421 0284 1A              LDAX    D               ;ROW # TO N. R. S.  DATA HIGH
422 0285 67              MOV     H,A             ;ROW # TO H REG
423 0286 7B              MOV     A,E             ;PUT 1ST ROW # TO ACC
424 0287 C630            ADI     030             ;ACC TO N. R. S.  ADD LOW
425 0289 5F              MOV     E,A             ;POINT D-E TO N. R. S.  DATA LOW
426 028A 1A              LDAX    D               ;ROW # TO N. R. S. DATA LOW
427 028B 6F              MOV     L,A             ;ROW # TO L REG
428 028C C9              RET                     ;RETURN
429
430                             ;LINEFEED
431
432 028D CDDC01 LF:      CALL    NXRO1           ;DO NEXT ROW SUBROUTINE
433 0290 CDC401          CALL    CLROW3          ;OFF SCREEN CLEAR ROW ROUTINE
434 0293 1E61            MVI     E,ROW8080       ;MOVE REFERENCE ROW # TO H-L
435 0295 CD8202          CALL    LDHL            ;LOAD H-L
436 0298 3A633F ADDCH:   LDA     03F63           ;CHAR # TO ACC
437 029B 85              ADD     L               ;ADD THE CHAR # TO THE
438 029C 6F              MOV     L,A             ;FIRST ROW ADDRESS.
439 029D 7C              MOV     A,H             ;IF A CARRY OCCURED ADD TO
440 029E CE00            ACI     000             ;THE DATA HIGH.
441 02A0 67              MOV     H,A             ;H-L POINTS TO LINE FED ROW
442 02A1 C3B301          JMP     PCUR            ;PUT CURSOR TO LINE FED ROW
443
444                             ;HOME CURSOR TO T. O. P.
445
446 02A4 1E62    HOME:   MVI     E,FIRSTRO       ;POINT D-E TO 1ST ROW
447 02A6 1A              LDAX    D               ;STORE FIRSTROW TO ROW8080
448 02A7 1E61            MVI     E,ROW8080
449 02A9 12              STAX    D
450 02AA CD8302          CALL    LDHL1           ;MOVE REFERENCE ROW TO H-L
451 02AD 3E00            MVI     A,000           ;PUT CHAR # BACK
452 02AF 32633F          STA     03F63           ;TO ZERO
453 02B2 C3B301          JMP     PCUR            ;PUT CURSOR HOME
454
```

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```
                        ;SWAP ROWS
02B5 1E65   SWAP:   MVI     E,ROWSAVE       ;POINT D-E TO ROW SAVE # AND
02B7 CD8202         CALL    LDHL            ;PUT IN H-L REG.
02BA 22663F         SHLD    03F66           ;STORE ROW SAVE # TO TEMP 1 *
02BD 1E61           MVI     E,ROW8080       ;POINT D-E TO 8080 ROW # AND
02BF CD8202         CALL    LDHL            ;PUT ADDRESS IN H-L REG
02C2 1E65           MVI     E,ROWSAVE       ;POINT D-E TO ROW SAVE # AND
02C4 1A             LDAX    D               ;PUT IN ACC
02C5 5F             MOV     E,A             ;8080 ROW # TO ADD HIGH
02C6 7C             MOV     A,H             ;STORE 8080 ROW # TO N.R.S.
02C7 12             STAX    D               ;DATA HIGH.
02C8 7B             MOV     A,E
02C9 C630           ADI     030
02CB 5F             MOV     E,A             ;PUT 8080 ROW # TO
02CC 7D             MOV     A,L             ;N.R.S. DATA LOW
02CD 12             STAX    D               ;8080 ROW # IS NOW IN ROW SA'
02CE 2A663F         LHLD    03F66           ;PUT ROW SAVE # BACK TO H-L
02D1 1E61           MVI     E,ROW8080       ;COMENT SAME AS ABOVE
02D3 1A             LDAX    D
02D4 5F             MOV     E,A
02D5 7C             MOV     A,H
02D6 12             STAX    D
02D7 7B             MOV     A,E
02D8 C630           ADI     030
02DA 5F             MOV     E,A
02DB 7D             MOV     A,L
02DC 12             STAX    D
02DD C39802         JMP     ADDCH           ;JUMP TO ADD CHAR.

                        ;BACK SPACE

02E0 1E63   BS:     MVI     E,CHARNUM       ;POINT THE D-E REG TO CHAR #
02E2 1A             LDAX    D               ;AND PUT IN ACC
02E3 FE00           CPI     000             ;TEST FOR THE CHAR # =
02E5 CAEE02         JZ      UPROW           ;TO ZERO. JUMP IF TRUE
02E8 3D             DCR     A               ;DECREMENT CHAR #
02E9 12             STAX    D               ;STORE DECREMENTED CHAR #
02EA 2B             DCX     H               ;DEC H-L FOR NEW CURSOR LOCA'
02EB C3B301         JMP     PCUR            ;PUT CURSOR IN DECREMENTED LO

                        ;NEXT ROW UP

02EE 3E4F   UPROW:  MVI     A,04F           ;MOVE THE CHAR #
02F0 12             STAX    D               ;TO 50H AND STORE IT.

                        ;MOVE CURSOR UP

02F1 EB     UPCUR:  XCHG                    ;POINT H-L TO 8080 ROW AND D-
02F2 2E61           MVI     L,ROW8080       ;TO NEW CURSOR LOCATION.
02F4 7E             MOV     A,M             ;TEST IF NEXT UP CURSOR WILL
02F5 23             INX     H               ;BE ON THE FIRST ROW.
02F6 BE             CMP     M               ;IF TRUE JUMP TO
02F7 CA0803         JZ      UPSCL           ;UP SCROLL ROUTINE.
02FA 2B             DCX     H               ;POINT H-L BACK TO 8080 ROW #

02FB FE00   BACK1:  CPI     000             ;IF 8080 ROW # IS EQUAL TO
02FD CA1E03         JZ      RO48            ;ZERO JUMP TO ROW 48 ROUTINE.
0300 35             DCR     M               ;DECREMENT 8080 ROW #

0301 EB     LOOP1:  XCHG                    ;POINT H-L TO NEW CURSOR LOCA
0302 CD8202         CALL    LDHL            ;AND D-E TO 8080 ROW #. JUMP
0305 C39802         JMP     ADDCH           ;TO ADD CHARACTER ROUTINE.

0308 7E     UPSCL:  MOV     A,M             ;PUT FIRST ROW # INTO ACC.
0309 FE00           CPI     000             ;TEST IF FIRST ROW # IS = TO
030B CA2403         JZ      FRO48           ;ZERO. IF TRUE JUMP TO ROW
030E 35             DCR     M               ;48 ROUTINE.

030F 2E60   LOOP2:  MVI     L,LASTROW
0311 7E             MOV     A,M
0312 FE00           CPI     000
0314 CA2A03         JZ      LRO48
0317 35             DCR     M

0318 2E61   LOOP3:  MVI     L,ROW8080       ;POINT H-L TO 8080 ROW #
031A 7E             MOV     A,M             ;AND LOAD TO ACC
031B C3FB02         JMP     BACK1

031E 3E2F   RO48:   MVI     A,02F           ;CHANGE 8080 ROW #
0320 77             MOV     M,A             ;TO 23D AND STORE
0321 C30103         JMP     LOOP1           ;JUMP TO POINTER EXCHANGE ROU

0324 3E2F   FRO48:  MVI     A,02F           ;
0326 77             MOV     M,A
0327 C30F03         JMP     LOOP2

032A 3E2F   LRO48:  MVI     A,02F           ;PUT THE 1ST ROW TO
032C 77             MOV     M,A             ;17H.
032D C31803         JMP     LOOP3           ;JUMP TO 8080 ROW # STORE
```

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```
546                             ;CLEAR ROW ROUTINE
547
548 0330 CD3603 CLROW:  CALL    CLROW1
549 0333 C36E02         JMP     CR
550
551 0336 1E61   CLROW1: MVI     E,ROW8080
552 0338 CD8202         CALL    LDHL            ;PUT ROW DATA IN H-L REG
553 033B 3E50   CLROW2. MVI     A,050           ;INTILIZE LOOP COUNTER.
554 033D 3620   LOOP4:  MVI     M,020           ;STORE ASCII SPACE IN MEM.
555 033F 3D             DCR     A               ;DECREMENT LOOP COUNTER.
556 0340 C8             RZ                      ;RETURN IF ZERO BIT IS SET.
557 0341 23             INX     H               ;NEXT LOCATION
558 0342 C33D03         JMP     LOOP4           ;CLEAR NEXT LOCATION.
559
560 0345 D301   BELL:   OUT     001             ;RING BELL
561 0347 C9             RET
562
563 0348 AF     IVERTN: XRA     A
564 0349 1E68           MVI     E,IMASK         ;POINT D,E TO MASK
565 034B 1A             LDAX    D
566 034C 17             RAL                     ;CK BIT 8 STATUS
567 034D DA5203         JC      RESET
568 0350 3E80           MVI     A,080           ;INVERT BIT 8
569 0352 12     RESET:  STAX    D               ;STORE OUT NEW MASK
570 0353 C9             RET
571
572 0354 E5     IVERTR: PUSH    H
573 0355 1E61           MVI     E,ROW8080
574 0357 CD8202         CALL    LDHL            ;LOAD 1ST ADD. OF 8080ROW TO
575 035A 1E50           MVI     E,050           ;SET COUNTER
576 035C 7E     LOOP6:  MOV     A,M             ;GET CHAR.
577 035D 17             RAL                     ;CK BIT 8 STATUS AND INVERT
578 035E DA7003         JC      RESET1
579 0361 1F             RAR
580 0362 F680           ORI     080             ;MASK BIT 8 HIGH
581 0364 77     BACK2:  MOV     M,A             ;STORE MOD. CHAR TO MEM
582 0365 23             INX     H               ;POINT TO NEXT MEM
583 0366 7B             MOV     A,E
584 0367 FE01           CPI     001
585 0369 CA7603         JZ      DONE            ;RETURN IF COUNT = ZERO
586 036C 1D             DCR     E               ;DEC. COUNTER
587 036D C35C03         JMP     LOOP6
588
589 0370 1F     RESET1: RAR
590 0371 E67F           ANI     07F             ;RESET BIT 8
591 0373 C36403         JMP     BACK2
592
593 0376 E1     DONE:   POP     H
594 0377 C9             RET
595      0000           .END    START
```

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```
A       0007    ACELD   011C    ADCUR   0161    ADDCH   0298
B       0000    B110    00D4    B1200   00EC    B150    00DA
B1800   00F2    B2000   00F8    B2400   00FE    B300    00E0
B3600   0104    B4800   010A    B600    00E6    B7200   0110
B9600   0116    BACK    0083    BACK1   02FB    BACK2   0364
BAUD    0093    BELL    0345    BS      02E0    C       0001
CHARNU  0063    CLRAM   0042    CLRAM1  004C    CLROW   0330
CLROW1  0336    CLROW2  033B    CLROW3  01C4    CR      026E
CRTCR0  0064    D       0002    DONE    0376    E       0003
FIRSTR  0062    FR048   0324    FUNC    0170    H       0004
HMCUR   0087    HOME    02A4    IMASK   0068    INCRO   01E5
INIT    003B    INTACE  014A    INTKB   0136    IVERTN  0348
IVERTR  0354    L       0005    LASTRO  0060    LDHL    0282
LDHL1   0283    LF      028D    LOOP    0244    LOOP1   0301
LOOP2   030F    LOOP3   0318    LOOP4   033D    LOOP5   01CF
LOOP6   035C    LR048   032A    M       0006    NEWRO   0225
NRS     0061    NXR0    01BE    NXR01   01DC    PCUR    01B3
PSW     0006    RESET   0352    RESET1  0370    R048    031E
ROLO    020D    ROW808  0061    ROWSAV  0065    ROZERO  01D7
SAVRO   027B    SCROLL  0205    SP      0006    START   0000
SWAP    02B5    TEMP1   0066 *  TEMP2   0067 *  UPCUR   02F1
UPROW   02EE    UPSCL   0308    VERTI   024F    ZCHAR   01F3
ZCRTC   024A    ZFRO    021E    ZLRO    0219    ZROW    01FB

 NO ERROR LINES
SOURCE CHECKSUM = 403F
OBJECT CHECKSUM = 0F51
INPUT FILE     1:CRT80A.SRC ON JIMFM
OBJECT FILE    1:CRT80A.LM ON JIMFM
```

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DEFINITIONS

ACE—Asynchronous communication element
CRTC—Cathode ray tube controller
Video Page —Visible screen data
Video RAM—Entire portion of RAM used only for display
First Row #—Address for top row of video page
Last Row #—Address for bottom row of video page
CRTC Row #—Address for next row load
8080 Row #—Address for cursor row
Character #—Character location in a row
XXXH are hexidecimal numbers

REFERENCES

National Semiconductor Data Sheets:

DP8350 Series Programmable CRT Controllers
INS8250 Asynchronous Communications Element

National Semiconductor Application Notes:

Simplify CRT Terminal Design with the DP8350, AN-198

Data Bus and Differential Line Drivers and Receivers, AN-83

Transmission Line Characteristics, AN-108

Hardware Reference Manual BLC 80/10 Board Level Computer. National Semiconductor Microcomputer Systems Chapter 6—System Interfacing.

Graphics Using the DP8350 Series of CRT Controllers

National Semiconductor Corp.
Application Note 212
Charles Carinalli

The DP8350 CRT Controller series is a versatile building block for both low and high-end CRT terminal applications. This application note demonstrates how the DP8350 may be used in CRT graphics applications. Although this presentation is general, when specific examples are given the DP8350 ROM programmed version of the DP8350 series will be used (80 characters per row, 24 character rows, 5 x 7 character, 7 x 10 character field size.)

BACKGROUND INFORMATION

The basic function of the DP8350 controller is to control the elements of the "video loop" (*Figure 1*). A memory address generated by the CRT controller is presented to the CRT memory, which stores a record of what appears on the CRT display. The character generator converts this stored information into serial video data to the CRT monitor. The intensity of the CRT electron beam is modulated by this video data and its position is controlled by the horizontal and vertical sync pulses generated by the CRT controller.

The CRT screen video area is divided into character cells (*Figure 2*). Each cell has a unique CRT memory address. The DP8350 must present the correct character cell address to the CRT memory at the appropriate CRT beam location. Use of the line counter outputs of the DP8350 make possible the subdivision of each character cell address into the unique scan line of the present CRT beam location.

For the DP8350 and its unique internal ROM program format, each character cell is composed of 70 dots (7 dots wide and 10 dots high) *Figure 3*. When using the DP8350, each of these dots may be active video data. Typically however, in alphanumeric display systems, the character generator will provide cell to cell character spacing on the CRT screen by blanking some number of rows and columns of dots. That is why the DP8350's 7 x 10 dot field is used with a 5 x 7 character generator (2 horizontal and 3 vertical dot spaces).

In fact, it is the character generator that restricts the use of the full character cell dot field, not the DP8350! Using a character generator which allows video on every scan line and all dots of the cell width, makes graphic capability possible. This type of graphic display generation is called "character generator graphics."

All of the dots on the CRT display may also be independently controlled by a separate CRT memory address location; this is called "memory mapped graphics."

Both of these graphics display generation techniques will be discussed here, with demonstrations of how the DP8350 series may be used to reduce total component count.

CHARACTER GENERATOR GRAPHICS

In this graphics system (*Figure 4*) the character generator block contains a ROM that has been programmed with

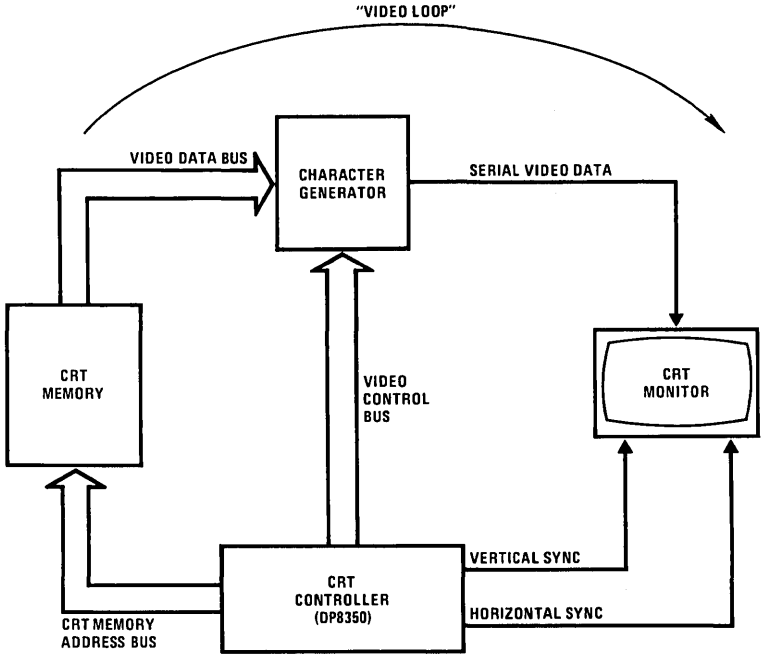

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FIGURE 1. Elements of the "Video Loop"

graphic symbols whose size is contained within the character cell size. This ROM may at the same time contain alphanumeric characters that do not use the full character cell size.

The block representation and operation of this system is the same as the alphanumeric's system previously described. The CRT memory presents the same character cell data to the character generator on every scan line of that character cell address. The character generator ROM is organized with addresses defining a particular symbol and address defining which scan line of a character row the CRT electron beam is currently on; thus defining the video data for that scan line of the symbol. The scan line address data comes directly from the DP8350. The parallel data that results is video data for that screen address cell width. This data is then serially shifted to the CRT monitor with a parallel to serial shift register.

This system allows every scan line of a character row to have active video information; thus the graphics symbol may be programmed to all sides of the character cell providing continuity from cell to cell both horizontally and vertically. At the same time, the alphanumeric's character may be programmed with cell to cell spacing.

Character generator graphics is the simplest most cost-effective approach to CRT graphics. It requires a minimum of software development and hardware support. The DP8350 CRT controller provides all the required timing and control pulses for the CRT memory, character generator, and CRT monitor.

Graphics capability with this system, however, is somewhat limited since individual dot control is not possible; only character cell symbol control is available. This system does apply well in such applications as bar graphs, circuit schematics, or flow charts and when these need to be combined with alphanumeric data.

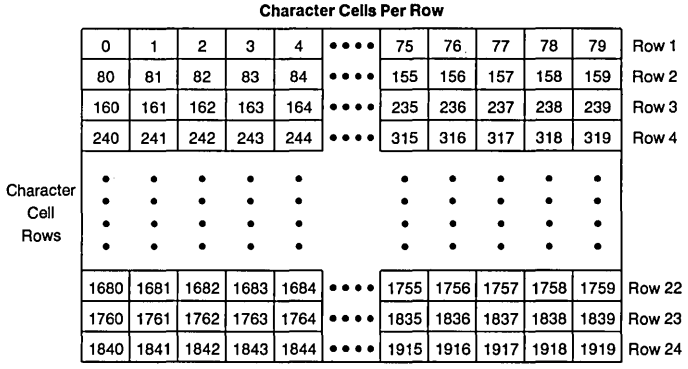

FIGURE 2. CRT Screen Cell Address Map Presented to CRT Memory by the DP8350 (Top of Page Register Contains Address 0) Character Cells Per Row = 80 Character Rows Per Frame = 24

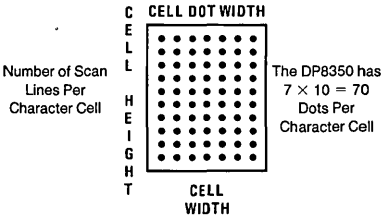

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FIGURE 3. The DP8350 Character Cell Is 7 Dots Wide and 10 Dots High

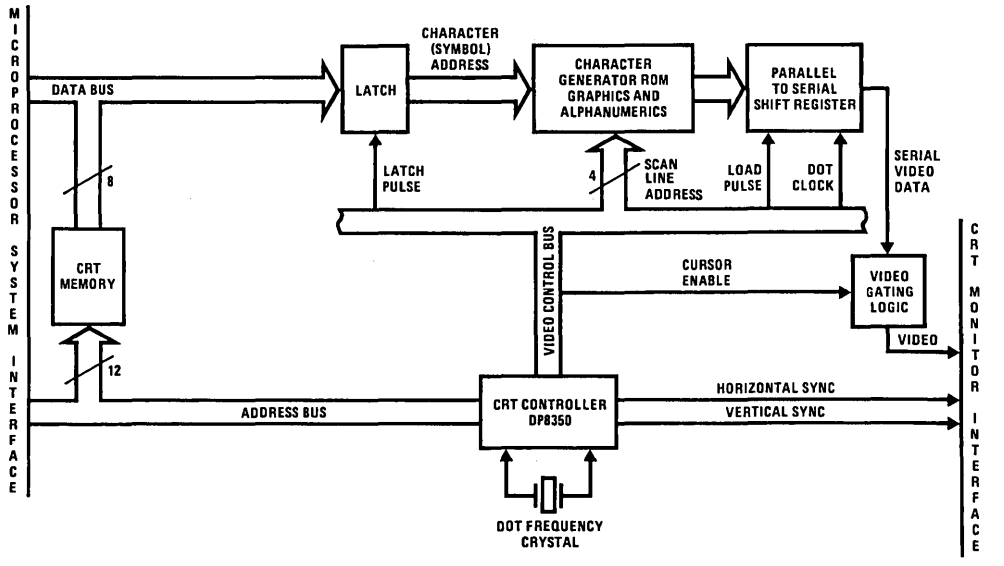

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FIGURE 4. Character Generator Graphics

CHARACTER GENERATOR GRAPHICS—WITH LINE BUFFERS

Modification of the character generator graphics block diagram is possible with the addition of a recirculating line buffer placed between the CRT memory and the character generator (*Figure 5*). In this case the character generator addresses for a character row are loaded serially into this shift register on the scan line before the first video scan line of a character row. These addresses are then recirculated for the number of scan lines per character row minus one (then the next character row of addresses is loaded). This system allows access to the CRT memory by the system controller on all but one scan line of a video character row. In contrast, the system previously described would have allowed access only during blanking intervals. In systems that require heavy access to the CRT memory to update screen information, this approach is very attractive.

In this case, as before, all the required control pulses for the "video loop" are provided by the DP8350 CRT controller.

MEMORY MAPPED GRAPHICS

If a very high resolution graphics display is required, every dot of the CRT display may be independently controlled. In this case, every dot of the CRT screen may be mapped to a specific CRT memory data bit—thus the name Memory Mapped Graphics. This type of system is obviously a more costly type of graphics, since to control every dot not only is there a need for more CRT memory, but the microprocessor overhead is such a system will be greater—both software and hardware. In any case, the DP8350 easily adapts to such a system as demonstrated in *Figure 6*.

In this approach, if you subdivide each character cell such that each scan line of the cell may be independently addressed, then from the CRT memory block instead of 8 bits of data defining a character cell code to the character generator, you get 8 bits of direct video data. Then the CRT memory block serves double duty—CRT memory storage and symbol or character generator. All that is left to do is convert this parallel video data to serial video data as before.

In the case of the DP8350 internal ROM format program, each cell is 7 dots wide; thus only 7 bits of video data are needed per character cell/scan line address. The DP8350 addresses the memory block as before with the character cell address, but in this case also with the scan line address. In this manner, the DP8350 series has a maximum address capability of 16 bits (64k).

VARIATIONS

If memory mapped graphics is desirable but standard alphanumerics is also required, combination of these techniques is possible. For example, if only a small portion of the CRT screen need be memory mapped and the remainder can be character generator alphanumerics and/or graphic symbols. In this case a higher order data bit from CRT memory defines whether the lower order data bits are graphics video data or ASCII and graphics symbol code. *Figure 7* is a block diagram of such a system.

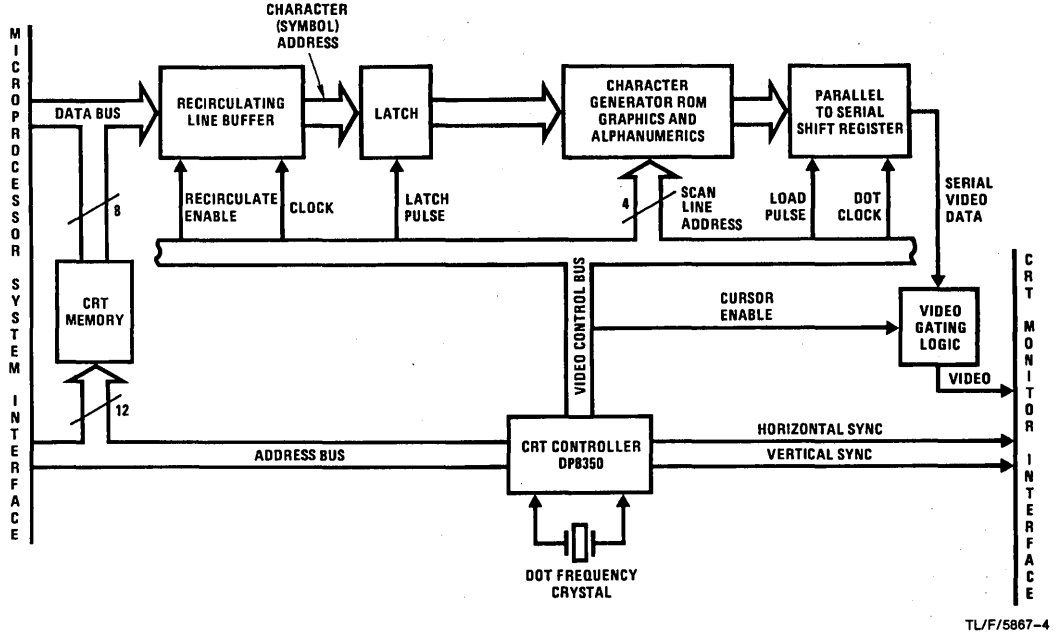

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FIGURE 5. Character Generator Graphics (with line buffer)

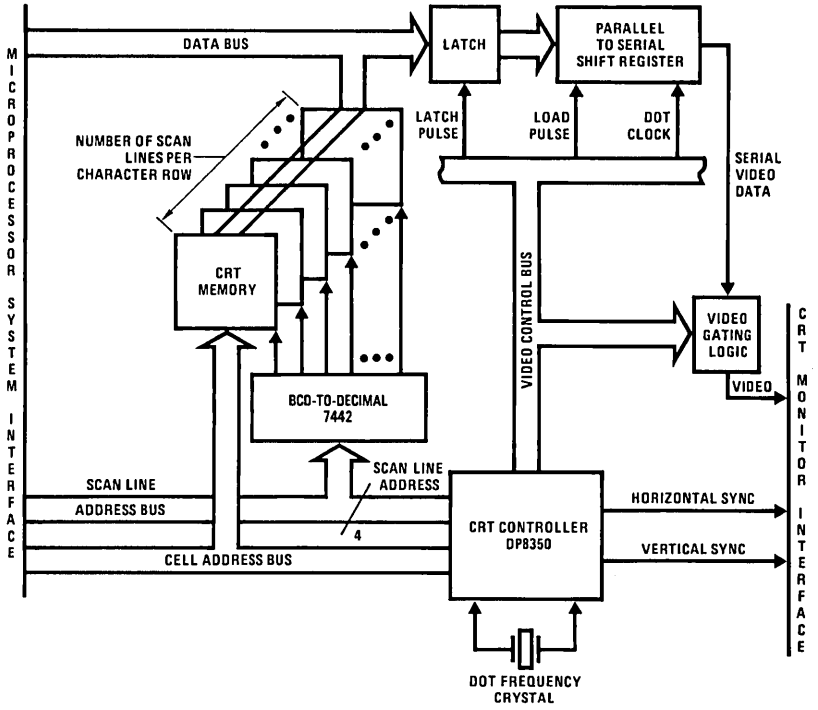

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FIGURE 6. Dot by Dot (Memory Mapped) Graphics

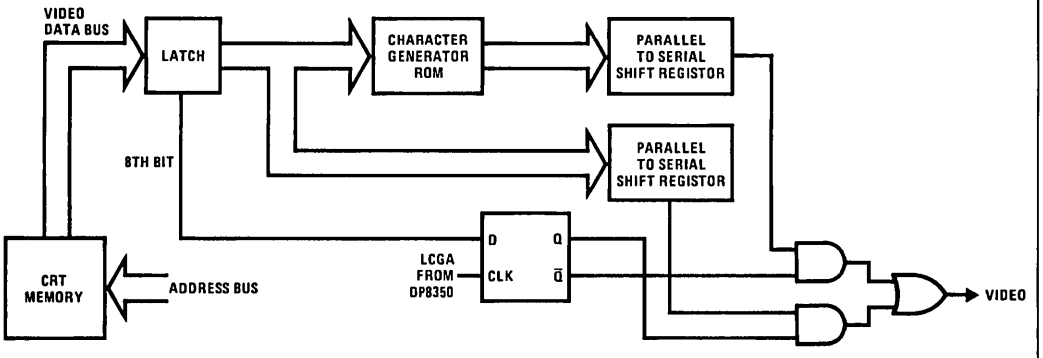

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FIGURE 7. Combined Character Generator and Memory Mapped Graphics

4

SUMMARY

This application note has demonstrated 2 basic graphics techniques that may be implemented using the DP8350 CRT controller. Variations to these techniques are possible such as changing character cell sizes and subdividing the character cell into dot blocks. In most cases, these variations are done to decrease hardware or software overhead. Since the DP8350 series of CRT controllers offer display format flexibility through internal ROM program variations—the device adapts equally well to these graphics variations as it does to the standard applications.

The fact that all the required control functions for the "video loop" are contained within the same chip—the DP8350—makes it very effective in these types of applications; as a result it will produce the minimum chip count and cost.

Graphics/Alphanumerics Systems Using the DP8350

National Semiconductor Corp.
Application Note 243
Mike Evans

This Application Note summarizes some CRT terminal circuits, each with an increasing degree of graphics capability, and then goes into detail to describe a system having full graphics capability, with all dots individually programmable. All these applications use the DP8350 CRT Controller.

Here are some of the features of the full graphics system.

Hardware Features

- The hardware is designed for a 24 row by 80 column display, with 7 dots per column and 10 lines per row
- All ICs are made by National Semiconductor
- Low I.C. cost, all parts readily available
- Fits on one standard BLC80 (SBC80) card
- System performance only limited by software
- 8080 Mnemonics—usable with STARPLEX™ or Intellec® Development Systems
- All graphics programs very fast
  Example: One dot takes 500 μs maximum to plot
- During display time, each 7-dot cycle may be shared by the microprocessor
- 8-bit word comprises MSB as attribute and next 7 bits as 7 dot word of a character line
- Can input display data serially or parallel
- Can output display data serially or parallel
- Baud rate programmable from 110 to 56k baud
- Can be used as slave to main system
- Can copy characters from alphanumeric ROM or symbol EPROM
- 13 kbytes of RAM available for user software or back-up display storage
- Analog inputs—joystick or waveforms
- Easily expandable to color graphics

Software Features

- The software is programmed for any display configuration of rows, columns, dots per column and lines per row. The hardware is designed for a 24 row by 80 column display, with 7 dots per column and 10 lines per row
- Can perform most dumb terminal functions, including scrolling
- Simultaneous display of alphanumerics and graphics
- Identical terminals can display same information with inputs from either
- Can save displays in computer storage
- Can load displays from computer storage
- Can erase any part of display or all of it
- Can draw a rectangle linking any 2 horizontal and 2 vertical coordinates
- Can transfer in 1/10th second max any area of display to any other area or to/from backup display storage
- Smooth movement of subject in any direction
- Immediate display of fixed diagrams
- In-system emulation of programs available

The DP8350 CRT Controller provides incrementing video addresses starting from the Top of Page address, or from a new Row Start address. These addresses and the Cursor address are loaded into their respective registers from the address bus. All video control signals are provided by the 8350, so that apart from the crystal oscillator, no extra video circuitry is required.

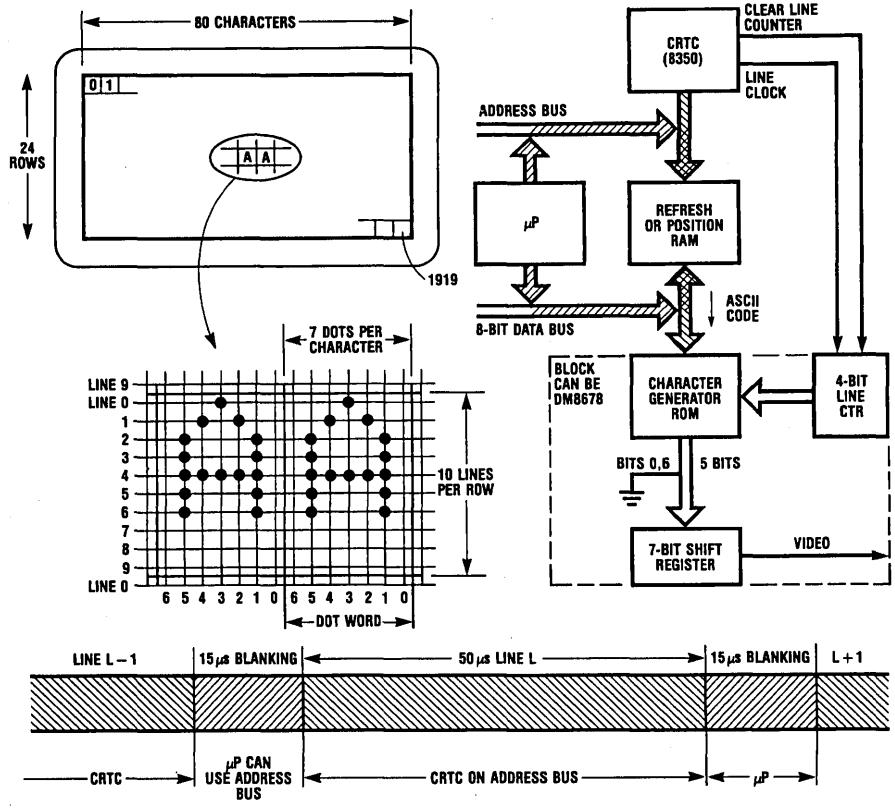
The DP8350 has so far been considered to be useable only in dumb terminals, whereas in fact it is easy to adapt it to more complex terminals with full graphics capability. Following is a summary of the functions of the various combinations of alphanumerics/graphics displays beginning with a dumb terminal using a monitor with 24 x 80 characters.

Dumb Terminal

The basic dumb terminal design is shown in *Figure 1*. Usually the microprocessor loads the Character Position RAM (or Refresh RAM) only during horizontal or vertical blanking, or during the last 3 lines of a row. The CRTC then sequentially addresses this RAM during display time. The ASCII data from this RAM (for the character selected) is outputted to the ROM of the Character Generator. The 7-dot word of this character for the line being displayed is then loaded into a shift register, and shifted out as video to the monitor during the next 7-dot cycle.

The logical choice of CRT Controller for this simple CRT terminal is the DP8350. The most common application is for a 24 row by 80 column display with the character field comprised of 10 lines each of 7 dots. The character itself occupies 7 lines each of 5 dots, leaving 3 lines for vertical character spacing, and 2 dots for horizontal character spacing.

Refer to AN-198 and AN-199 for further information on alphanumeric applications of CRTs.



Disadvantages for Graphics

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- Only Characters in the Character Generator ROM can be selected.
- Characters not continuous to adjacent fields.
- Microprocessor thru-put 30% of maximum—not desirable for graphics.

FIGURE 1. Simplest CRT Terminal

Alphanumeric Characters with Extra Symbols

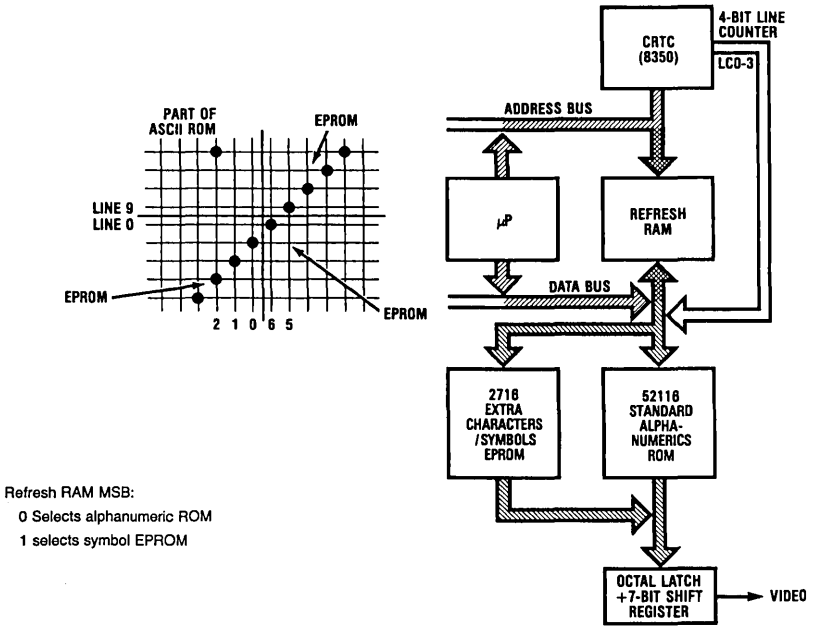
When characters or symbols are required that are different from those in the ROM, then an extra EPROM such as the 2716 can be added as shown in *Figure 2*. The standard characters can be selected from a separate ROM such as the 52116 which contains all 128 standard ASCII characters. The EPROM is preprogrammed with additional characters or symbols. The 8350 outputs sequential addresses to the Refresh RAM, and each address is two dot cycles ahead of the shifting dot word.

The data out from the RAM must be valid 150 ns after each address change. The MSB of the data selects ROM or EPROM, and the remaining 7 bits select the character. The line of the character is decoded from the 4-bit line counter outputs coming from the 8350. The ROM/EPROM now has 640–150 ns (>450 ns) to output the valid dot word. This has to be latched into an octal latch and held for one dot cycle before it can be loaded into the 7-bit shift register. The dots are then shifted out in the dot cycle.

Limited Graphics Terminal

To be able to generate any graphics symbol, a character RAM must replace the fixed ROM characters. Characters or symbols can be loaded into the RAM as required from a ROM or a pre-programmed EPROM like the 2716 (refer to *Figure 3*). But now, new graphics characters can be written into the RAM from the Microprocessor. These can either be derived internally from the μP or obtained directly from peripherals (such as serially to an Asynchronous Communications Element like the INS8250, or parallel from an external I/O port).

This limited graphics application thus requires two RAMs, the Refresh RAM (or Character Position RAM), and the Character RAM. The Refresh RAM outputs the selected character address, and the 8350 line counter outputs select the line in the Character RAM. The 7 dots outputted from this RAM are latched into the Octal Latch and held for one dot cycle. The 8th bit of data can be used as an attribute control bit. The 7 LSBs are then loaded into the 7-bit shift register.



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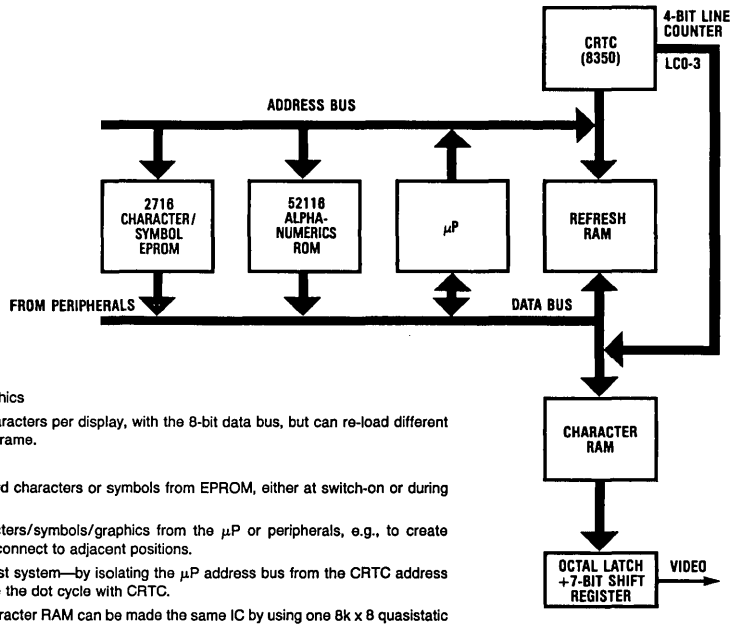
Disadvantages for Graphics

- Fixed graphics possible with continuous display, but limited to 128 different characters, and 128 standard alphanumerics, for all 1920 positions.
- Also it is possible to change characters/symbols once the EPROM has been programmed.
- The Microprocessor is still slow thru-put.

FIGURE 2. Fixed Character ROM + Symbol EPROM



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Disadvantages for Graphics

- Only 256 possible characters per display, with the 8-bit data bus, but can re-load different characters for a new frame.

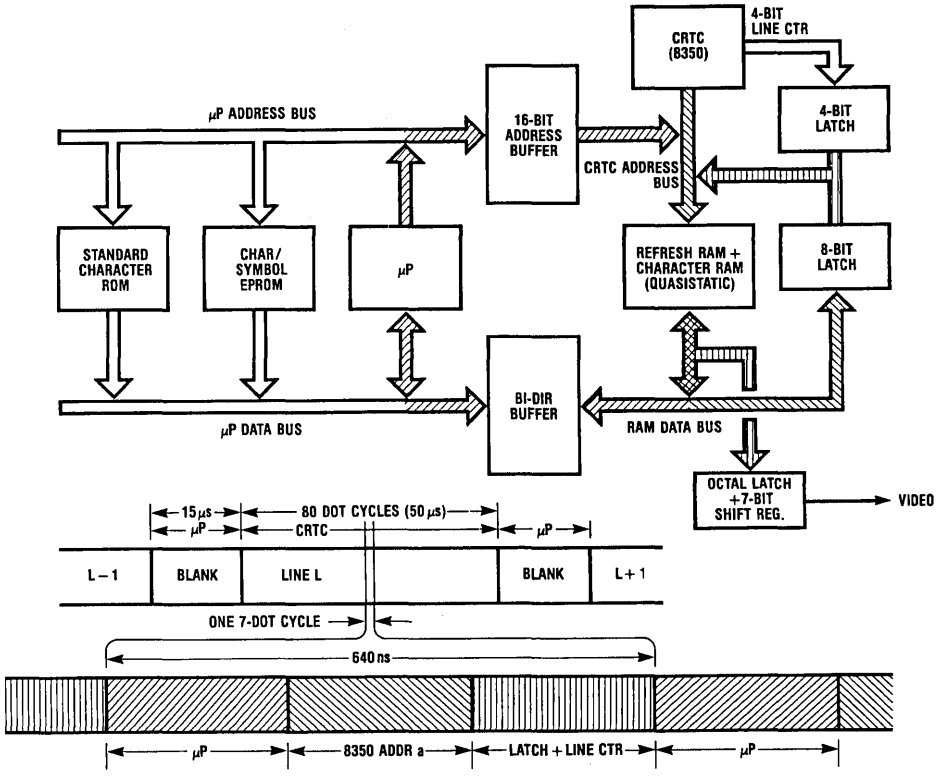
Advantages

- Can now load standard characters or symbols from EPROM, either at switch-on or during normal running.
- Can also load characters/symbols/graphics from the μP or peripherals, e.g., to create graphics drawings to connect to adjacent positions.
- Can now be a very fast system—by isolating the μP address bus from the CRTC address bus, the μP can share the dot cycle with CRTC.
- Refresh RAM and character RAM can be made the same IC by using one 8k x 8 quasistatic RAM.

FIGURE 3. Character RAM with ROM/EPROM Look-Up

The first quarter of an 8k x 8 RAM can be used as a Refresh RAM for the 1920 character positions. The RAM data outputs containing the character address can then be latched into an octal TRI-STATE latch. If the 8350 address bus is then disabled, the octal TRI-STATE latch can feed back to the RAM second half address inputs, along with the enabled 8350 line counter outputs. The data out from the RAM now contains the next 7-dot word to be displayed and this is then loaded into the shift register. This takes the last two thirds of the dot cycle, the first third is for the μP. With the fast cycle time of the quasistatic RAMs this 3 part cycle can easily be accomplished in one 7-dot cycle. (Refer to *Figure 4*).

With the method just described it is only possible to display 256 different characters for any one page, because each character consists of 10 lines, almost filling the second half of the quasistatic RAM. If this is acceptable, then a limited graphics terminal can be easily implemented using a microprocessor, with one 2716 instruction set EPROM, one 52116 character ROM, one 2716 symbol EPROM, one DP8350 CRT Controller, the NMC4864 quasistatic RAM, and a DM74166 shift register. The logic and drive circuitry required to control the sequencing comprises a further 15 SSI ICs. This application has not yet been built, awaiting availability of the quasistatic RAMs.



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Advantages

- Only one IC, an 8k x 8 quasistatic RAM, used for both the refresh RAM and character RAM.
- Fast, although μP may be in the wait state for a maximum of 600 ns. This is no problem because the fastest μP instruction cycle is 1 μs, so there will be no effect on maximum thru-put.

Disadvantages

- No quasistatics available at the time of writing.
- Full graphics capability not possible.

FIGURE 4. Limited Graphics Using a Buffered CRTC Address Bus and a Quasistatic RAM

Full Graphics Capability

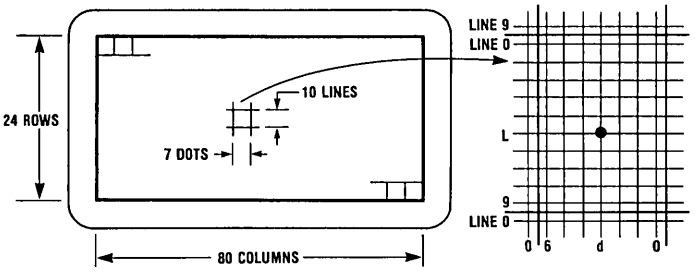
We need to be able to select any dot on the display, for full graphics capability, while still using the CRT controller to sequence every line of every row, as it does in the simple terminal (See *Figure 5*).

With the standard 24 x 80 character display, full graphics can be achieved by using a 24 (rows) by 80 (columns) by 10 (lines) address RAM, and selecting the 7 dots as the data word for the character position on the display and the line of that character position.

This means that alphanumeric characters can be displayed in exactly the same format as with a simple terminal, by copying the character from ROM or EPROM into the selected 10 line by 7-dot field, line by line.

Full graphics capability is also easily implemented once the relevant software algorithms have been determined.

So for full graphics, every dot is one bit of memory. There is no refresh RAM, refer to *Figure 6*. The CRTC scans through the Display RAM, a line at a time for each row on the CRT, causing the RAM outputs to be read every 7-dot cycle. The RAM output is shifted out two dot cycles later. The microprocessor may write into the Display RAM each 7-dot word, with "1's" representing dots.



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Dot is at Line L, Dot d character position is at Row r, Column c.

FIGURE 5. Full Graphics Capability Requires Individual Dot Selection

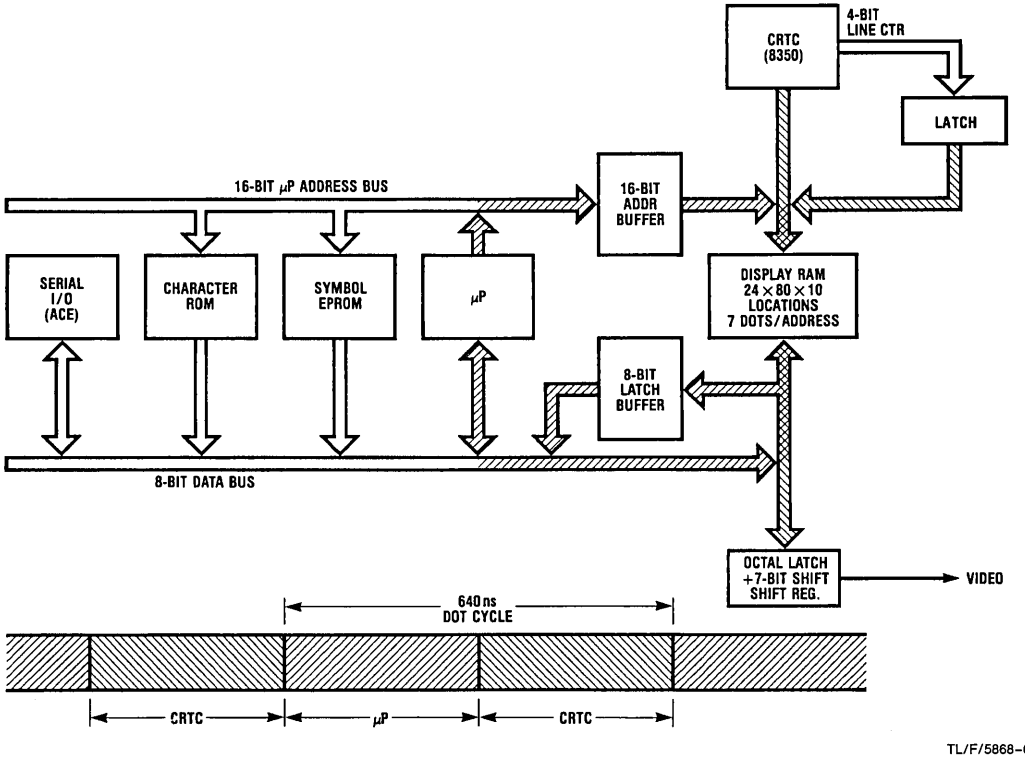

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FIGURE 6. Full Graphics System

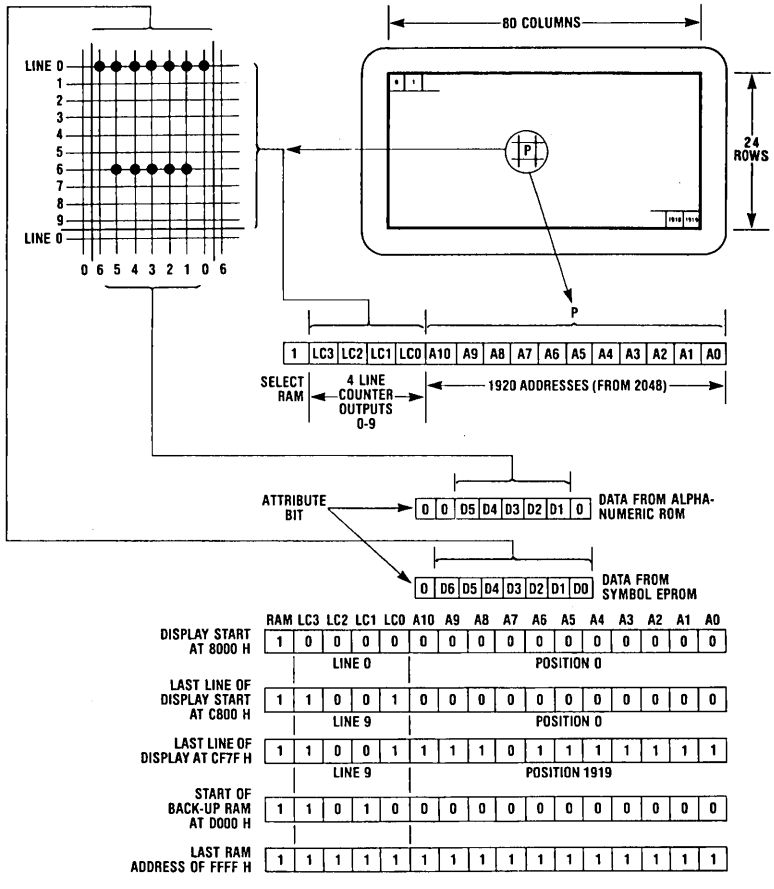

FIGURE 7. RAM Addressing

CRTC Address Bus Configuration

The particular RAM address to be written into is determined by its 10 x 7 character field position and the selected line of that field; refer to *Figure 7*.

The 11 least significant addresses A_0 to A_{10} contain character position information from position 0 to 1919, and the next 4 addresses A_{11} to A_{14} are the 8350 line counter outputs via a TRI-STATE buffer. The most significant bit, A_{15} is used to select the RAM when HI, and the EPROM's and peripherals when LO.

Graphics Design Criteria

In the simple CRT applications, the microprocessor is used mainly to re-write the Refresh RAM as new information is fed in, either from the keyboard, or from the main computer (via ACE). The μP can still be used in this application for alphanumerics/graphics, but it is also desirable if it can perform graphics computations, such as drawing, lines from the inputted coordinates.

This requires the microprocessor to be able to write 7 dot words quickly to the Display RAM. The best way to implement this is to time multiplex the dot cycle with the CRTC so that whenever the μP requires access to the Display RAM, it merely waits for its slot in the next dot cycle, which could be up to 640 ns later. The information is either written or read after 360 ns, that is a maximum of 1 μs after the memory access request, which is fast enough. Now the μP no longer has to wait for blanking to be able to operate, it continues its normal operation and only enters the WAIT state during RAM access. Although this is for up to 1 μs, in fact it is in general invisible because the μP memory access takes at least 700 ns.

The Microprocessor

The 8080A-2 was chosen for the following reasons:

- FAST—Takes 21.84 MHz (2 x 8350 frequency) divided by 9 (in the 8224), to give a clock cycle of 2.427 MHz, i.e., 0.41 μs per microcycle, or 1.6 μs for a short instruction
- Software can be developed on STARPLEX™ or Intellec Development Systems
- 8080A-2, DP8224 and DP8238 are low cost
- Associated circuitry previously designed in Application Note AN-199

Note the DP8238 has advanced MEMW more—desirable so that the microprocessor can go into the WAIT state earlier in the write cycle.

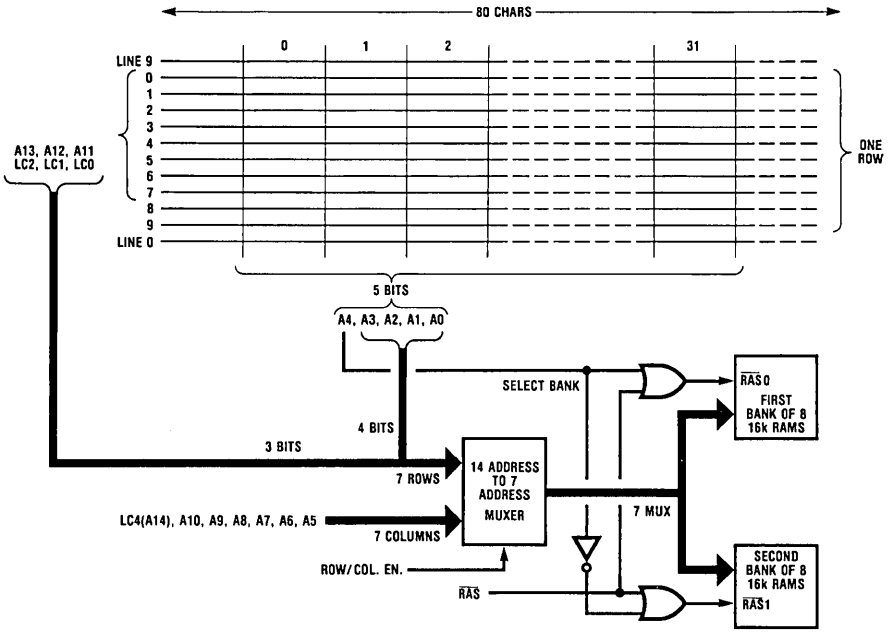

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FIGURE 8. Automatic RAM Refresh

Interrupts

The INS8259 is ideal as an Interrupt Controller, because most interrupt signals in the system are positive going, saving D-type flip-flops. It can also be used to mask off interrupts when necessary.

Interrupt Priority

1) *Horizontal Sync* from the 8350, highest priority if row start has to be quickly changed, normally masked off
2) *Paralleled 8-Bit I/O Port,* highest priority if CRTC card is part of a master system, otherwise masked off
3) *Vertical Sync* from the 8350, normally highest priority, need to quickly change the Top of Page register for scrolling, to change the display before the new frame begins
4) *ACE,* INS8250—during serial block transfers this will take highest priority
5) *Keyboard*—the time to press the keys is much longer than the interrupt wait time so can be low priority
6) *A/D Converter*—time for conversion is 100 μs so again can be low priority

Display RAM

The system requires a RAM with 24 x 80 x 10 addresses, each of 8 bits (representing 7 + 1 attribute bit), and a cycle time of 640 ns/2 or 320 ns. Using static RAMs 19.2 kbytes would require 40 ICs, whereas using dynamic RAMs 16 ICs are necessary, totaling 32 kbytes. This leaves 13 kbytes available as spare RAM.

Advantages of Dynamic RAMs

- Only 16, 16-pin packages instead of 40, 18-pin packages
- Less than $10 for 16,000 bits
- Fast access and cycle times using the MM5290-2 (average cycle time is 320 ns). Even faster times with the 5V only 16k MM5295
- Standby current only 5% of operating current
- Less average power dissipation than for static RAMs

This means average power dissipation is 30 mA x 12V x ½ x ½ x 16 or 1.5W for all 16 packages (only one bank is accessed per cycle by the CRTC for half the dot cycle time). For 40, 4k x 1 static RAMs, average power is 80 mA x 50V x 40 or 16W. Note that if the MM5295 5V, 16k x 1 dynamic RAM is selected, power dissipation will be even further reduced, with access and cycle times about half the 3 rail version.

Disadvantages

- Not easy to interface to
- Need to be refreshed every 2 ms—see "Refreshing of Dynamic RAMs"
- 3 supply rails needed, +12V, +5V, −5V, but these are already required for the 8080

Refreshing of the Dynamic RAMs

With 16k dynamic RAMs all 128 rows of every RAM have to be refreshed every 2 ms maximum to maintain valid data. It is possible to manipulate the addressing of the CRTC address bus to the dynamic RAM multiplexed address bus, so that there is no need for a separate refresh counter. This is because for any display row, the 8350 sequences all 80 characters, starting at line 0 and ending at line 9. Thus we can use the 3 least significant bits of the line counter outputs (A_{11}, A_{12}, A_{13}, from LC0, LC1, LC2) for three of the dynamic RAM row address bits, (corresponding to lines 0 to 7 of each display row), and the four least significant bits of the character position address (A_0 to A_3) for the remaining four RAM row address bits. See *Figure 8.*

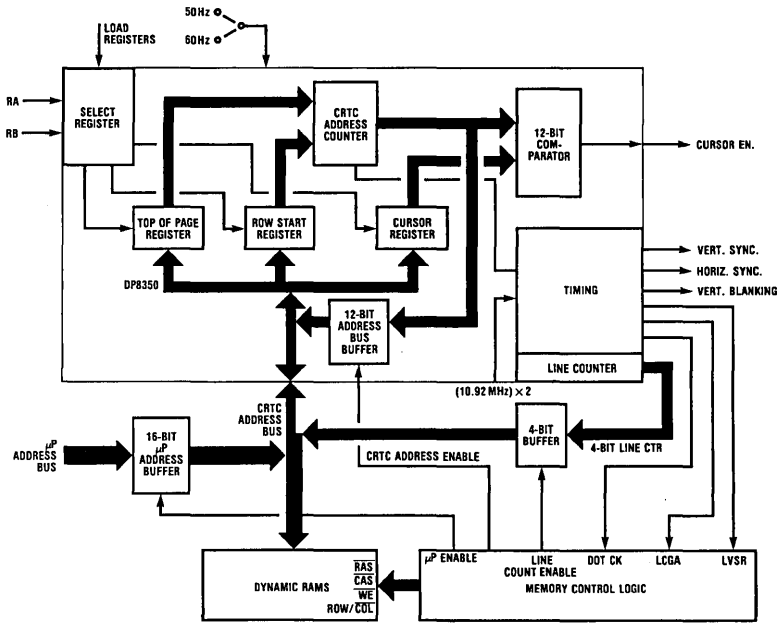

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FIGURE 9. 8350 Block Diagram

Unfortunately, because 19k addresses are required, it is necessary to use two banks of RAM (8 RAMs in each bank), giving a total of 32k x 8. This leaves 13 kbytes available for scratch pad, display storage, and in-system emulation of programs. Therefore each row of this second bank of dynamic RAMs also has to be refreshed. By using address bit A_4 to select the bank, all rows of the dynamic RAMs are therefore refreshed every 32 characters, which in fact is eight lines, or in effect one row of the display. The worst case is when the 32 characters are split over two display rows. There is no problem during the vertical blanking because the 8350 still outputs incrementing addresses and LCGA continues to activate the control logic. So refreshing still continues during blanking. Thus the longest period any RAM row goes without a refresh cycle is 65 μs per line x 10 lines per row x 2 rows = 1.3 ms, which is still within the 2 ms maximum at 70°C. *In other words, dynamic RAM refreshing is automatically performed by the 8350 sequencing the address and no extra circuitry is required.*

CRT Controller

A graphics/alphanumeric CRT Controller requires the following (See *Figure 9*):

1) All monitor signals provided—the 8350 provides Vert/Horiz sync and vertical blanking
2) Cursor signal—the 8350 has cursor enable
3) Fast dot clock, a 7-dot cycle clock continuous, and a shift register clock only during display—the 8350 has dot clock, LCGA and LVSR
4) Line counter output 4-bit, TRI-STATE—the 8350 has line counter output (but not TRI-STATE)
5) Ability to set top of page, row start and cursor reg at any time—the 8350 can do this using LD REG, RA and RB inputs during the time the μP is on the CRCT address bus. RA and RB can be data bus bits DB0 and DB1, and LD REG can be decoded from the address bus
6) 50 Hz or 60 Hz capability—the 8350 has a frequency select input
7) Incrementing position address, TRI-STATE—the 8350 has this, with a maximum enable/disable time of 30 ns

   This parameter is important in this application where it is necessary to switch the memory from the CRTC address to the microprocessor address, and back to the CRTC address all in one 7 dot cycle of 640 ns. Other CRT controllers are not capable of enabling and disabling the CRTC address so quickly.

Hence the DP8350 requires no extra circuitry apart from a Quad Latch to disable the Line Counter outputs. The 8350 has internal ROMs which determine how many rows (24), columns (80), lines per row (10), and dots per column (7). Versions of the 8350 are available with other combinations.

System Timing

The standard timing for the dumb terminal type of application is shown in the timing section of *Figure 1*, with the microprocessor inactive during display time. This is undesirable for graphics applications where full use of the micro-

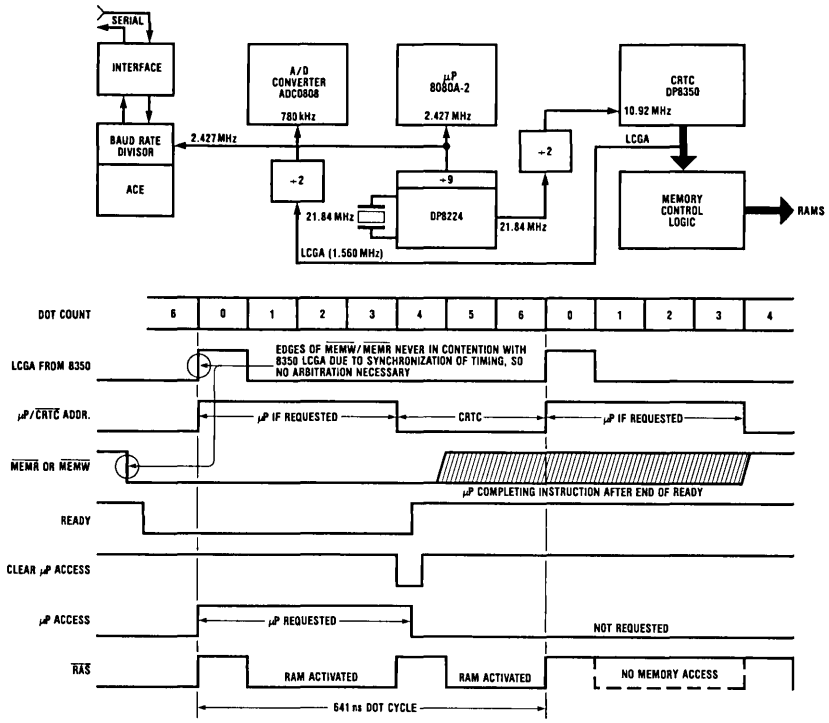

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FIGURE 10. System Timing Control Circuit and Diagram

processor is required for computations and peripheral control with very fast baud rate. To determine the timing sequence it is first necessary to calculate the CRTC frequency required for the dot clock.

CRTC Frequency = d × [c + (characters during horizontal blanking)] × [(r × l) + (lines during vertical blanking)] × (line input frequency)

where d = dot per character,

c = columns on display

r = rows on display

l = lines per row

For the standard 8350,

$$f = 7 \times (80 + 20) \times [(24 \times 10) + 20] \times 60\ \text{Hz}$$

$$= 7 \times 100 \times 260 \times 60\ \text{Hz} = 10.92\ \text{MHz}$$

This is too slow for the DP8224 which divides the crystal frequency by 9 to provide the clock to the microprocessor. The 8224 frequency can therefore be 21.84 MHz as in *Figure 10*, and this is divided by 2 to provide the 8350 dot clock of 10.92 MHz, or 91.6 ns per dot. A 7-dot cycle is 641 ns or 1.560 MHz. This is divided by 2, i.e., 780 kHz, to provide a clock frequency for the A/D converter.

The 8080 frequency is 21.84/9 MHz or 2.427 MHz. This frequency is also applied to the ACE to provide the clock for the Baud Rate divider. The baud rate is determined from 2.427 MHz/(16 x Baud Divisor).

7 Dot Cycle Timing

Figure 11 shows how the 7-dot cycle time of 641 ns can be time multiplexed into two separate control sequences; Microprocessor and CRTC. It is necessary that the new 7-dot word to be displayed, is available at the commencement of the dot cycle shift. Therefore the 8350 must access the CRTC address bus for the second half of the 7-dot cycle, in fact for the last 3 dots of the cycle. This allows the time period taken by the first 4 dots to be used by the microprocessor, so that the microprocessor address output appears on the CRTC address bus for the first four dots, but only if a μP access is requested.

The CRTC 15-bit address is timed multiplexed into 7 rows and 7 columns to be applied to the dynamic RAMs, using multiplexer-drivers, with bit A4 selecting the bank. It is therefore necessary to latch in first the rows with RAS (Row Address Strobe), and then the columns with CAS (Column Address Strobe), for both the μP half-cycle and the CRTC half-cycle. All the set-up and hold times are met by the circuitry of *Figure 12*. If the μP is not requesting RAM access during its half-cycle, the RAS does not occur, although CAS still does. This is because RAS enables CAS internally in the dynamic RAM's, so that if RAS does not occur, the CAS has no effect and the RAM remains in standby mode. This is also the case in selecting the banks with RAS0 or RAS1.

In the second half-cycle, the CRTC always reads the RAM, so WE remains HI, but in the first half-cycle the μP may request a READ or WRITE. WE remains HI for READ, and for WRITE remains LO while RAS is low. Note that the 8350 outputs the address word two dot cycles in advance, and therefore it is necessary to latch and then hold the dot word for one dot cycle. It is then latched into the 7-bit parallel-in serial-out shift register. The 8th bit from the latch can be used as an attribute bit.

Simple Alphanumeric Display

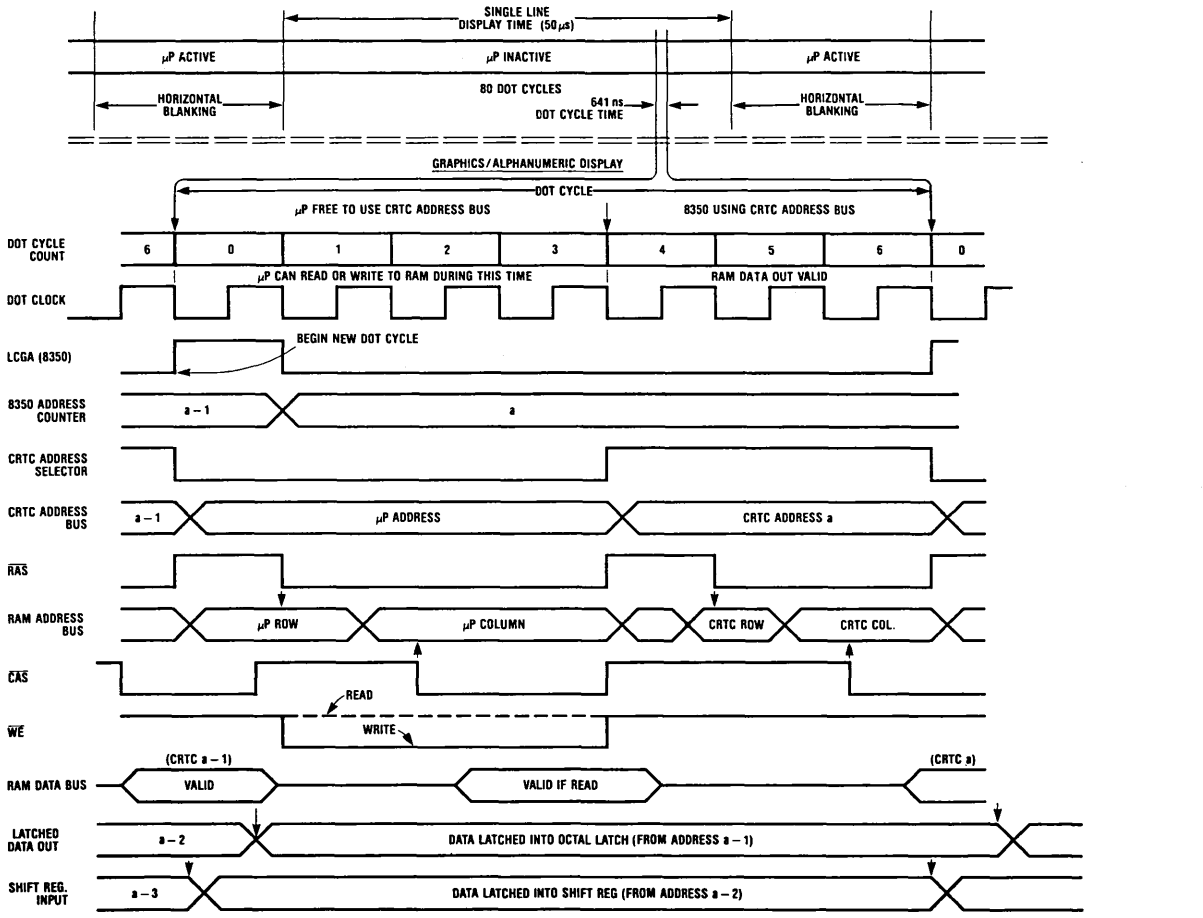

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FIGURE 11. Memory Control Logic Timing Diagram

Figure 12 shows the Memory Control Logic required to correctly sequence the control signals and busses to the dynamic RAMs and associated components. The interfacing from the 8080 microprocessor (via signals MEMR and MEMW) is such that whenever the μP requests to read or write to the dynamic RAMS, the μP Access Flip-flops access the RAMs at the start of the next μP cycle. At the end of these four dots, the information has either been latched into an 8-bit latch (for READ), or written into the RAMS (for WRITE). The READY signal goes active at this time which ensures that valid information is read at the end of the μP cycle; refer to *Figure 10*. Also the fact that MEMR and MEMW occur at fixed intervals relative to the dot cycle signal, LCGA, means that system contention cannot occur. Therefore there is no need for arbitration between these two signals when a microprocessor cycle is requested.

This also applies when selecting the 8350 to change Top of Page, Row Start and Cursor. To select any of these 3 registers, the μP data bus bits D0 and D1 are connected to R_A and R_B to select the required register.

The information to be latched into the selected register has to be valid on the CRTC address bus. Because this is time shared with the 8350 address counter, which outputs the incrementing display addresses during the second half of every 7-dot cycle, the CRTC register information has to be valid for the first half of the next dot cycle. The CRTC is selected with DS6/7 and MEMW, so that REGISTER LOAD occurs just after the CRTC register information becomes valid on the CRTC address bus. The 8350 spec requires that the address be valid 250 ns before REGISTER LOAD trailing edge (old data sheets do not state this), and that R_A and R_B are valid at the leading edge. Note that the 8350 internal address counter can be enabled or disabled within 30 ns of the ADDRESS ENABLE changing state.

All the Logic for Memory Control is Schottky, due to the very fast timing required in the system. Note that the cycle time of the CRTC half-cycle is 270 ns, which is less than the 320 ns specified for the MM5290-2. This parameter is specified at 320 ns for power dissipation reasons, and because the μP is not fast enough to use its half-cycle every 7-dot cycle or 641 ns, the average cycle time is greater than 320 ns.

System Configuration

Figures 13 and *14* together show the system block diagram. The peripheral components of *Figure 13* are used with the microprocessor circuitry of *Figure 14*. The right hand half of *Figure 14* is equivlent to the circuitry of *Figure 12*.

The LS138 address decoder is used for both I/O and memory addressing. Referring to *Figure 15* address map, the peripherals are designated as I/O, and the EPROMs, ROM, CRTC and dynamic RAMs as memory. With address bit A15 HI, the 32k dynamic RAM block is selected. With address bits A14 and A15 LO, the LS138 outputs are selected. A11, A12, and A13 are decoded to select which one of the LS138 outputs goes LO, so that when memory is addressed, each section is 2 kbytes. This includes the CRTC which requires 4 kbytes from 3000H to 3FFFH for 2 pages. The top four address bits select the CRTC and the remaining 12 address bits are latched into the selected register.

When addressing I/O, address bits A0–A7 also appear respectively on A8 to 15, so that with A6 and A7 LO, i.e., I/O address 00H to 3FH, each LS138 output is now 8 bytes selected by A3, A4, and A5. Bits A0, A1, and A2 are then connected as required to the peripherals, to select the addressed byte.

PERIPHERALS

I/O Port

In 00H or OUT 00H select the 8-bit parallel I/O port, which basically is two octal latches with TRI-STATE outputs. The 8 output bits may be connected to a master 8-bit data bus. When an external 8-bit data word is latched into the input octal latch, an interrupt causes this to be enabled on the μP data bus, when acknowledged with the instruction IN 00H. To output to the master databus, OUT 00H causes the μP data to be latched into the output latch and this also provides an external interrupt to the master system. The master can then read this data by enabling the output octal latch. Data can be transferred fast because the I/O port normally has the highest priority interrupt (IR 3 of the 8259), when required.

Interrupt Controller INS8250

This was also mentioned in an earlier section. At initialization, it is set up to remain in the fully nested mode, so that only higher priority interrups may interrupt an existing interrupt. Otherwise a lower priority interrupt has to wait for the higher one to finish. Normally the horizontal sync interrupt to IR2 is masked off if there is no need to change ROW START or soft scroll display data off the screen line by line. The I/O address to select the 8259 can be either 10H or 11H; refer to the 82569 data sheet and the software to determine whether A0 is '0' or '1'. Each interrupt routine has to end with a SET END OF INTERRUPT instruction.

Keyboard

The instruction IN 18H reads ASCII data on the keyboard after a keyboard interrupt has been acknowledged.

Serial I/O Using the ACE INS8250

The 8250 with its associated EIA RS 232 interface allows serial data to be received or transmitted 8 bits at a time, with the instructions IN 20H or OUT 20H. The baud rate is previously determined as described in the software section. Other ACE registers may be accessed, by connecting A0, A1 and A2 of the μP address bus to the same designations on ACE, so that ACE addresses are from 20H to 26H. During block transfers, such as dumping a picture on the screen into an external memory, or loading from the memory, the higher priority inputs can be masked off for fast transfers.

Baud Rate Switch

See 'Baud Rate' for application, the instruction OUT 28H will read the 4 switch positions.

A/D Converter ADC0808

This 8 analog channel, 8-bit A/D converter, has first to be initialized to commence a conversion on one of the channels. Address bits A0, A1 and A2 are used to select the channel, so that instruction OUT 3 nH starts a conversion on INPUT n. The conversion takes about 100 μs with the 780 kHz clock, so the μP can continue operating during conversion. The END OF CONVERSION signal then interrupts the μP, which when acknowledged reads the 8-bit data with the instruction IN 3 nH, although n is not important in reading the A/D.

The A/D converter being only one 28-pin chip, is ideal for demonstrating the graphics capabilities of the system. For instance, an x-y joystick can be connected to INPUT 0 and INPUT 1, so that the movement of the joystick draws on the screen.

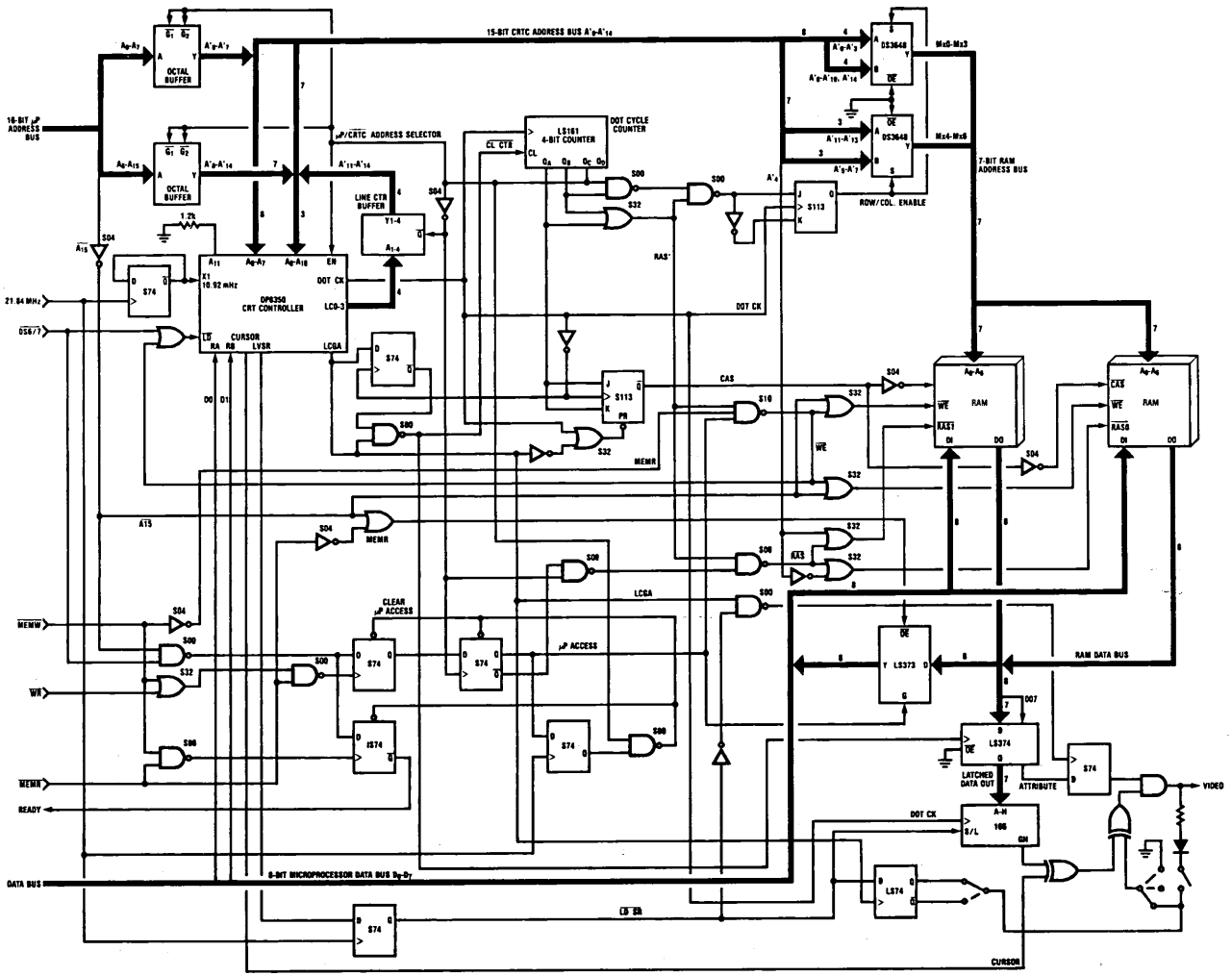

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FIGURE 12. 8350 Graphics Memory Control Logic

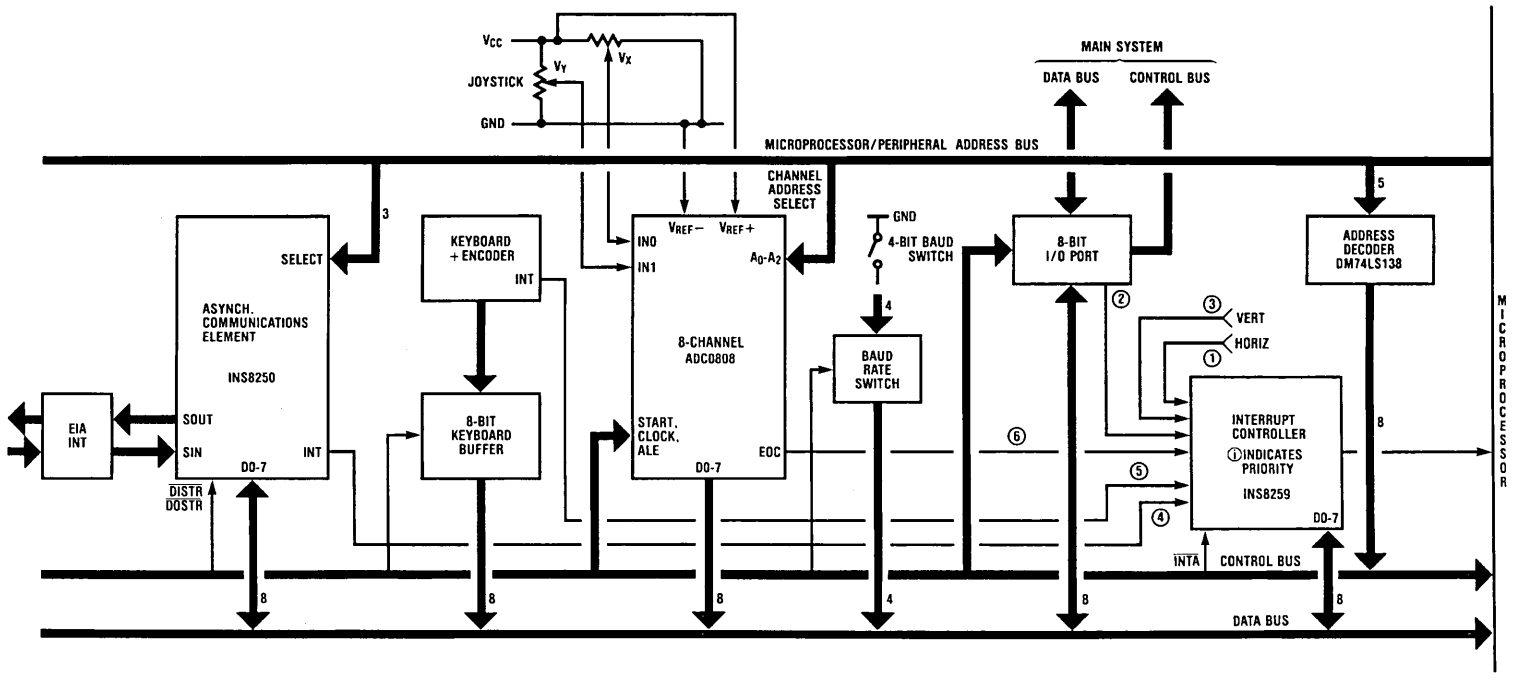

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FIGURE 13. Interfacing to Various Peripheals

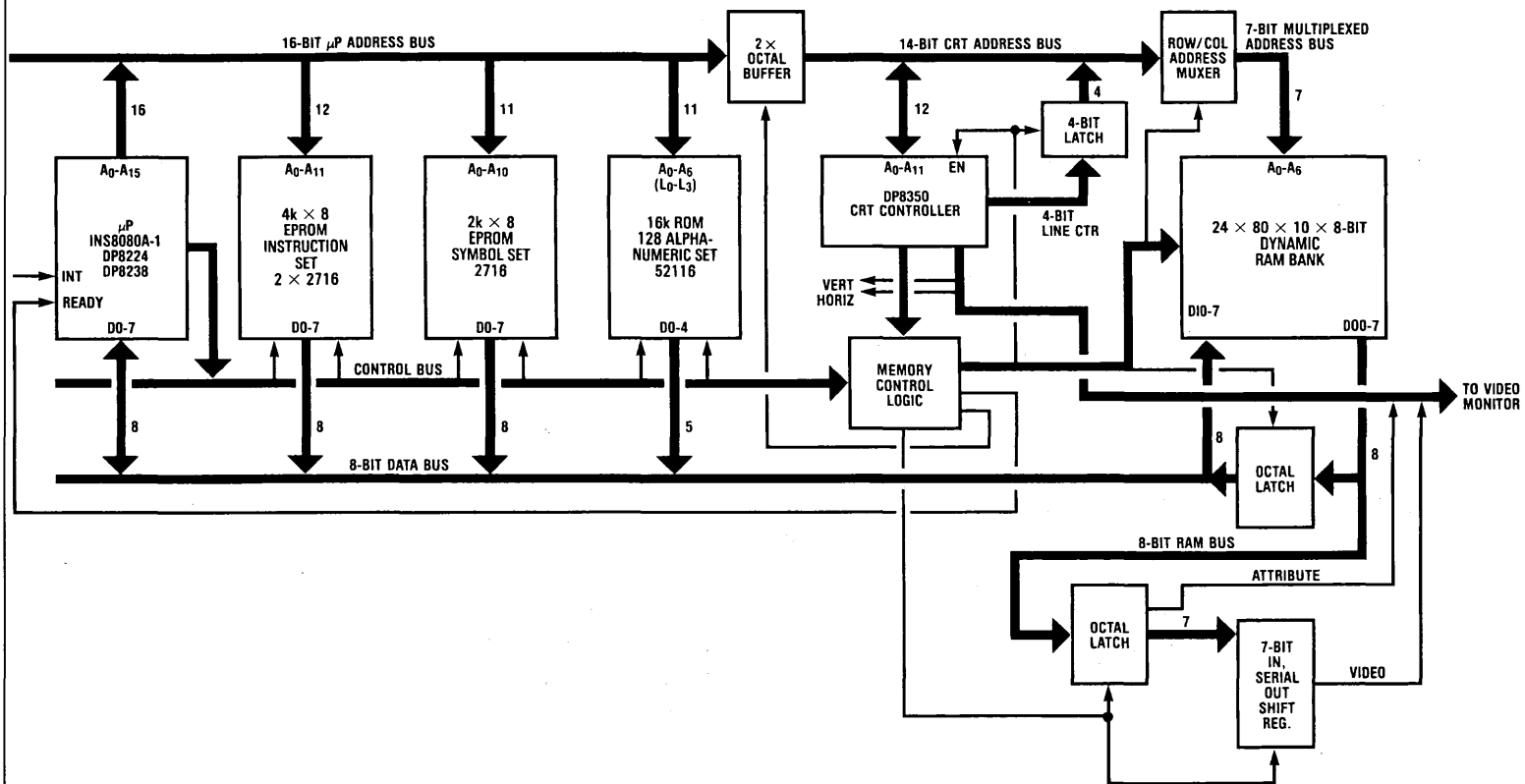

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FIGURE 14. Complex Alphanumeric/Graphics/Symbol Display Terminal

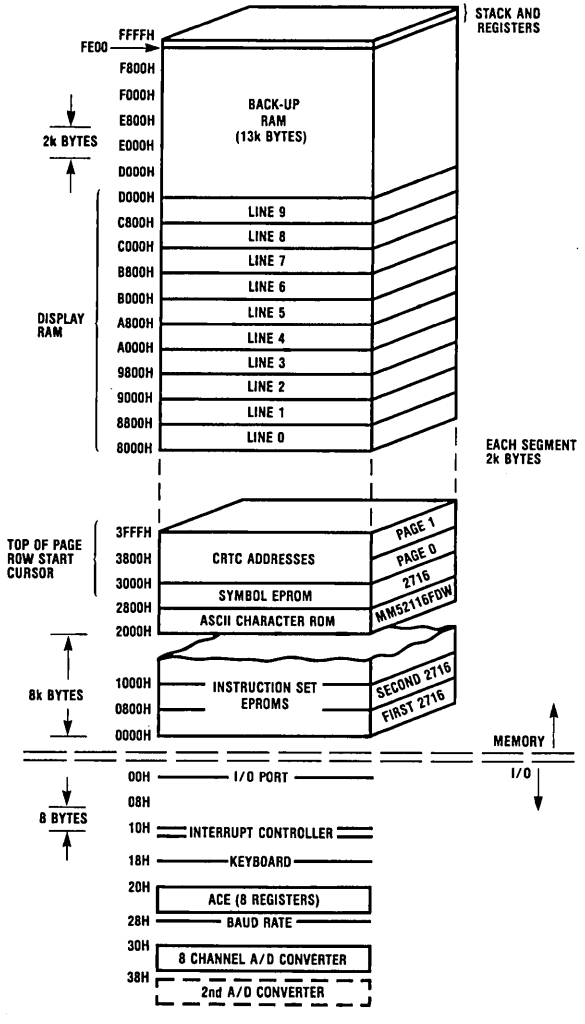

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FIGURE 15 I/O and Memory Map

System Operation and Software

The software was developed purely for demonstration purposes to show the versatility and power of the system. All the software has been tested, but the system could be much more powerful with additional software. The 13 kbytes of back-up RAM are also useful in this respect. The software was developed on National's STARPLEX Development System. The instruction set so far is just under 4 kbytes, so two 2716's are used, but these may be replaced by 2732's if the chip select pins are reconnected, so that extension up to 8 kbytes is possible with no extra IC sockets.

Parameter Definitions

The software is structured as in *Figure 16*. The philosophy was to make it versatile, easy to understand, and easy to modify or add to.

The registers are stored in the dynamic RAMs starting at FE00H in the non-display section. The Top of Stack is also in the RAMs at the highest location, FFFFH. This allows for about 240 nested two-byte PUSHes or CALLs, which is comfortable. Any register may easily be relocated merely by changing its address, similarly any new registers may be added to the list.

The addresses of the various memory and I/O locations are also listed and defined in the front section so these can be changed as desired.

For complete versatility, the display parameters are also listed in the front section so that any different value of parameters from those listed need be changed only in this section. The values of the parameters or constants are those of the standard DP8350 around which the hardware has been designed.

Thus by defining most parameters in the software once, at the beginning, the subsequent routines/subroutines will be valid for different applications and should not need to be altered, merely added to. Not many macros were used in order to save EPROM instruction space.

Interrupt Entry Locations

These are in 8-byte increments beginning at 0010H. The 16 bytes before this are saved for power-up initialization to disable interrupts and set Top of Stack.

Each interrupt location calls that interrupt subroutine. At the end of the subroutine, the system returns to output an END OF INTERRUPT to the 8259, and then returns to the original subroutine in progress when the higher priority interrupt occurred. If no interrupt was in progress, the program returns to the WAIT LOOP which enables all unmasked interrupts to the μP.

Look-Up Tables

This has three sections. First, the BAUD RATE DIVISOR look-up table contains all the 16-bit divisors required for baud rates from 110 baud to 19k baud.

The next look-up table contains PROGRAM LABELS, used in the SEARCH FOR PROGRAM subroutine. The first row contains all the first characters of the program labels, the second row contains the second character, up to the fourth row contains the fourth character. Each program consists of four characters.

The third table is the address list so that once the SEARCH subroutine has located the desired label, it alters the program counter to the equivalent section of this table, which then calls up the program requested.

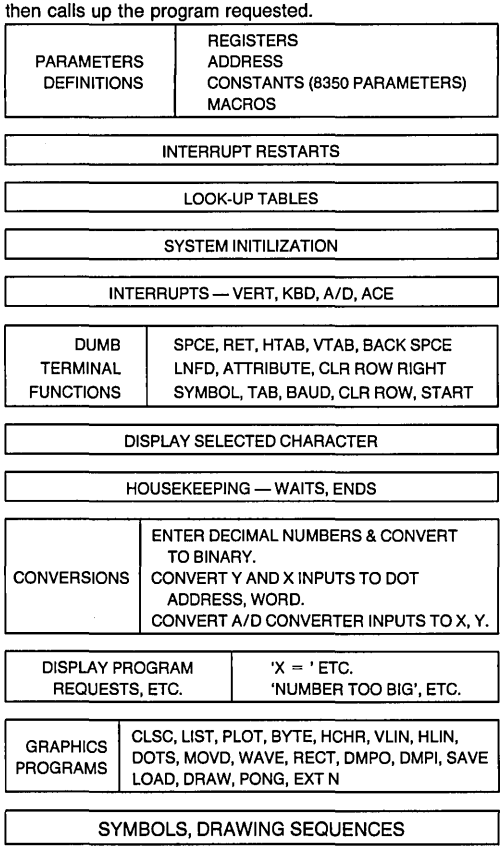

FIGURE 16. Graffiti — Software Structure

System Initialization

After disabling interrupts and setting Top of Stack, the 32k addresses of RAM are cleared one byte at a time, so that the screen is blank within half a second of switch-on. The cursor is then homed to the first character position. First the Top of Page register is set to 0 in the CRTC and then the cursor register is set to 0, both in the RAM and the CRTC. The column count is also reset.

The ACE is next set up including the baud rate (see Baud Rate section). Next, the Interrupt Controller is set up, and after this the system enters the WAIT LOOP system, enabling the interrupts to wait for an interrupt.

Interrupts

1) *Horizontal Interrupt* is normally masked off but may be unmasked for two reasons: either during scrolling, so that each row can be soft scrolled off the screen a line at a time, or during editing to delete a row, so that a jump in ROW START to the next row has to occur every frame at this new row. This new row must be loaded after horizontal blanking of the last line before the jump row is to begin.

   Note that if the ROW START register is not loaded, each row start address is the last display address incremented.

2) *Port Interrupt* is normally masked off, but must be unmasked if transfer of data to a master system is necessary.

3) *Vertical Interrupt* is used for two purposes. One is to scroll the display by one row, once the scroll semaphore bit has been set in one of the associated subroutines, this is begun at vertical interrupt so that screen flicker does not occur. The other is to change a graphics display every frame so that smooth transition of a subject across the screen is attained. An example of this is the program PONG. The flow chart for Vertical Interrupt is shown in *Figure 17*.

4) *ACE Interrupt* is by far the most complex because data received by this chip then has to be operated on to determine what action to take. The flow chart for ACE Interrupt is shown in *Figure 18*. Assuming the interrupt is because ACE has received data available, the ASCII data is checked for a function input. If not a function, but a program is already in progress awaiting inputted data, then this character is saved in the Input Character register. If the character was entered while the cursor was in the first four positions of a row, then the character is saved in a register determined by the column position of the cursor. This saves the character to recall it in a look-up comparison later, while searching for a program. Unless the ASCII code was a function, the character is displayed in the cursor position (see Displaying Characters).

   If the ASCII code entered is a function, then first CARRIAGE RETURN is checked for. If negative, then all the other functions are checked for and if positive, that particular function is executed. If the input is in fact a carriage return, then a check is made to see if the cursor was in the 5th position, signifying a four character graphics program has been requested. The system then goes to search in a look-up table for a program corresponding to the four ASCII characters entered in order. If a program is found, the system then calls the requested graphics program and executes it. If not, then a carriage return is executed.

5) *Keyboard Interrupt* in most systems is a simple subroutine, merely accepting the ASCII data word from the keyboard and outputting it to the ACE (see Displaying Characters).

6) *A/D Converter Interrupt* sets the A/D semaphore bit.

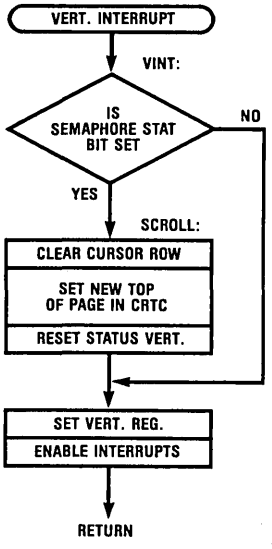

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FIGURE 17. Vertical Interrupt Flow Chart

Functions

A number of dumb terminal functions are available with the present software: carriage return, line feed, advance cursor, backspace, up cursor, tab 8 positions, clear row, clear row right of cursor, scroll up one row, and selecting attributes. Attributes available are half-intensity characters and character inversion. Each 7-dot location has its own attribute bit.

Baud Rate

The 4-bit BAUD SWITCH is used to select the BAUD RATE at switch on, or during operation if CTL E is entered. The μP then reads the switch setting and loads the corresponding 16-bit BAUD RATE DIVISOR into the INS8250 Asynchronous Communications Element. Baud rates from 110 to 19k are available, and up to 56k is feasible if the 8080A-2 μP is selected for fast data rates.

Displaying Characters

When a key is depressed, the keyboard outputs the ASCII code of the key selected, which is read by the μP when the keyboard interrupt is acknowledged. The μP then outputs the same ASCII data to the INS8250 ACE to be transmitted serially via the RS232 interface. This can be connected to a main computer, or an identical terminal, or back to the serial input of the ACE. When the ACE receives the returning 8 bits, it outputs a RECEIVED DATA AVAILABLE INTERRUPT or RCDA. The received data is then read by the μP, which selects the ASCII character from the 128 character ROM using the ASCII code as address. The alphanumeric character is copied line by line into the dynamic RAM in the position of the cursor.

Initially all RAM locations are '0' and the dots are written as '1', in a 7-dot word. See *Figure 19*. Then every frame, as the 8350 scans each line, the 7-dot word for each character position is latched from the RAM into the 7-bit shift register, and outputted serially during the next 7-dot cycle so that each '1' appears s a dot. The standard ASCII characters are displayed in a 7 line by 5 dot format or font. The 7 lines are copied line by line into the first 7 lines of the 10 line character field, leaving lines 7 through 9 as vertical spacing between characters. Data bits 1 through 5 are used for characters, leaving dots 0 and 6 as spacing between adjacent characters. The keyed character then appears on the screen and the cursor is incremented to the next position.

Additional Symbols

An additional 2716 EPROM with pre-programmed electronic symbols can be selected instead of the ROM, so that circuit diagrams can be drawn on the screen. Each symbol in the EPROM can be 10 lines of up to 7 dots so that each character may be continuous into the next—a necessity for circuit diagrams. The EPROM is selected by typing CTL Z on the keyboard and then a key, which can be either upper or lower case. This then displays the appropriate symbol in a similar manner to an alphanumeric character. To return to alphanumerics again, another CTL Z is required from the keyboard.

Two sequences are also stored in this EPROM, at addresses 1D00H and 1E00H. When either of these are called up by the program DRAW, a circuit diagram is drawn on the screen. This is an efficient way of storing circuit diagrams. Each circuit sequence, requires about 200 bytes, which is not a lot to cover most of the screen, much less than the 19 kbytes normally required to save every dot.

Although the symbol EPROM was programmed for electronic symbols, other kinds of symbols may be programmed into this EPROM, such as mechanical symbols.

Programming this EPROM is not easy. Assuming ASCII characters are to be used to select each symbol, then the addresses A_6, A_5, A_4 must be 100, 101, 110, 111 corresponding to ASCII codes 4XH to 7XH, where X is address A_3, A_2, A_1, A_0. The 4 lines LC 3, LC 2, LC 1 and LC 0 go to address bits A_{10}, A_9, A_8, A_7. The EPROM is selected with 00011B to A_{15}, A_{14}, A_{13}, A_{12}, A_{11}. In other words, to select the first line of character (41H), the address would be 1841H, and for the second line 18CH etc.

Locating the Position of a Dot

The standard DP8350 displays 80 horizontal characters for each of 24 rows, each character field comprising 10 lines of 7 dots. Thus there are 80 x 7 or 560 horizontal dots and 24 x 10 or 240 vertical dots in the display. Let the value of the horizontal dot position be x, where $0 \leq x < 560$, and y be the vertical dot position, where $0 \leq y < 240$. Refer to *Figure 20*.

If the x and y values are inputted to the microprocessor, it can then compute the character position, the line number and the dot position number. First, the Row Number r is INTEGER (y/10). This then has to be multiplied by 80 to produce the ROW START number. The Column Number then has to be added to this to obtain the Character Position Number, where the Column Position c is INTEGER (x/7). The line of the row is (y − r), and the dot number is (x − c) for the computed character position.

For the 8080 microprocessor, multiplication and division of numbers is laborious and time consuming. It is therefore easier to use the program subroutine shown in *Figure 21* to compute the character position, line number, and dot number. A separate subroutine then computes the dot word from the dot number. This 7-dot word is then ORed with the word already in the computed dynamic RAM location. All this can be demonstrated using the program PLOT.

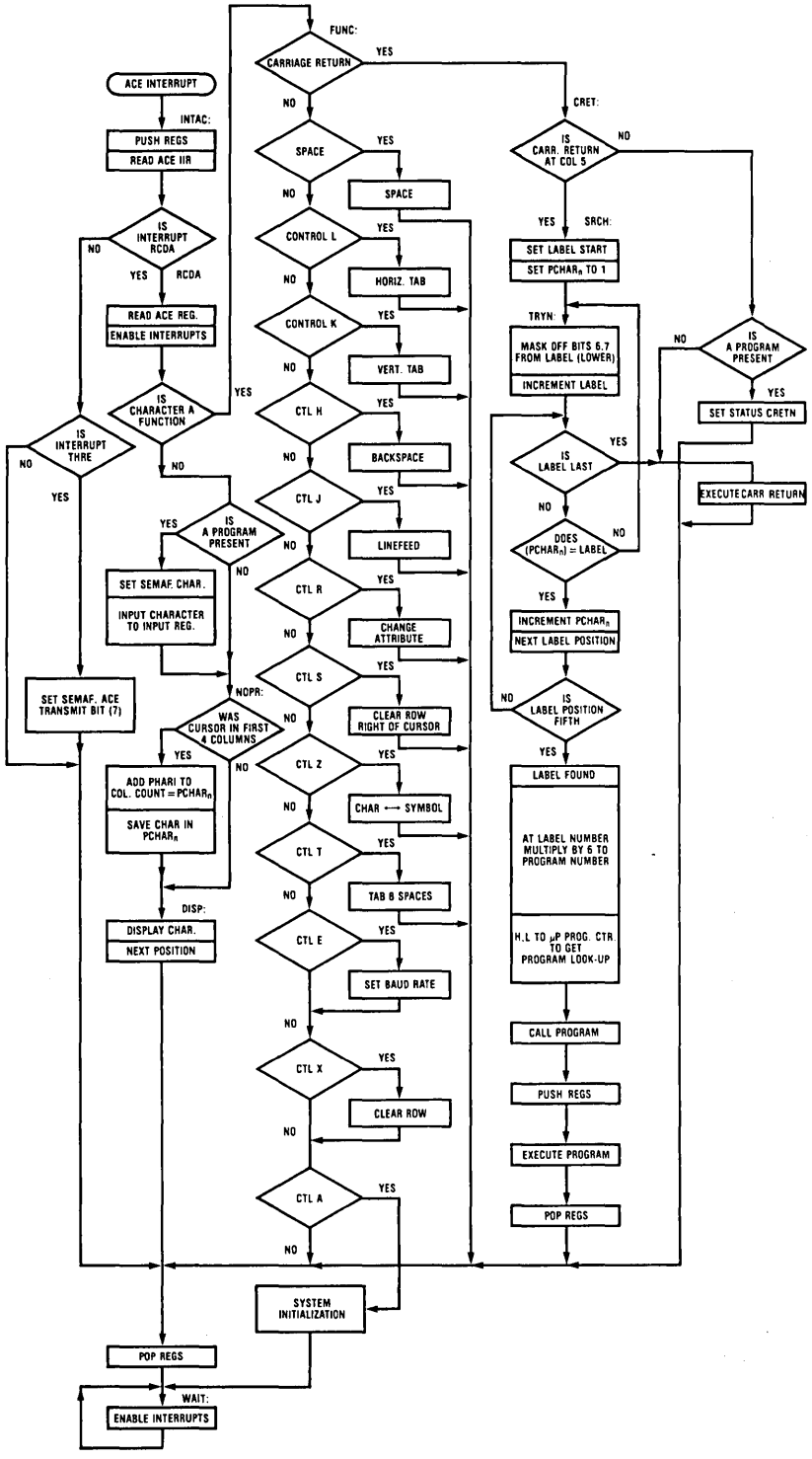

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FIGURE 18. ACE Interrupt Flow Chart

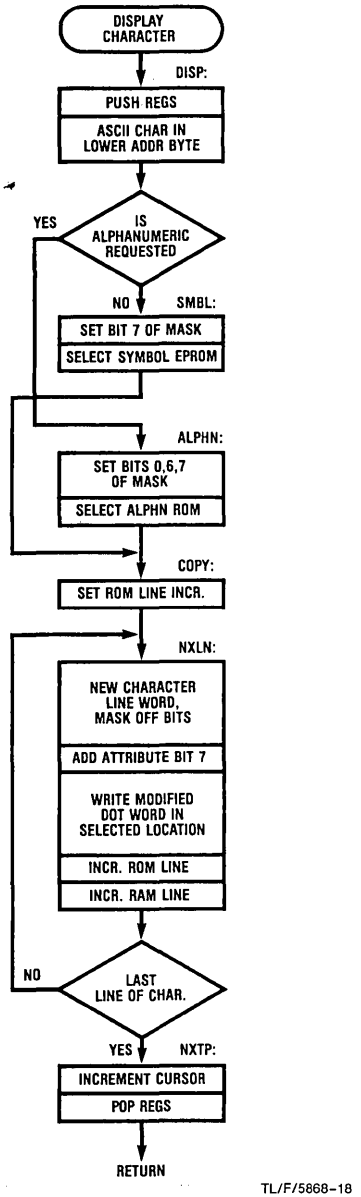

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FIGURE 19. Displaying Character

This computation takes an average of 300 μs and a maximum of 500 μs. Hence up to 3,000 dots can be plotted per second for any values of x and y to create a graphics display.

A good demonstration of the graphics capability is to connect an x–y joystick to two analog inputs of the A/D converter and by selecting the program MOVD (move dot), moving the joystick. The joystick can be moved quickly from one extreme to another and all dots on the way are displayed. This program can also use a dot as the cursor, using the joystick to select its position, and then to depress keys whenever a desired character is required at the character position of the dot.

Dot Word Transfers

With the use of the ACE, it is possible to unload the contents of the RAM into either an identical terminal to copy the display, or to store it in a main computer. It can then be recalled from the computer at a later date and re-loaded into the RAM to be displayed. Or if desired, sections of the display can be transferred. Copying from or to the display can be fast, because 7 dots are read or written at a time. An example of this is to use the programs SAVE and LOAD. A section of the display (such as a circuit diagram) can be saved in the back-up RAM, and then loaded back on to the display in a different area. The diagram appears almost instantly.

This extra 13 kbytes of back-up RAM can also be used as additional memory for in system emulation of programs, or for powerful computing capability for graphics calculations.

Graphics Programs

To perform various graphics functions it was decided to select the necessary software with four letter program labels, followed by a carriage return. As long as the label derived starts at the first column of a row, the program requested is called up and executed. Some programs request information from the operator. PLOT is an example of this, where the values Y1 and X1 are requested by the display. The user types in the desired values in normal decimal, signifying the end of the number with a carriage return. After both y and x have been entered, the program continues, in this case plotting a dot at Y1, X1.

Conversion of Entered Decimal Numbers

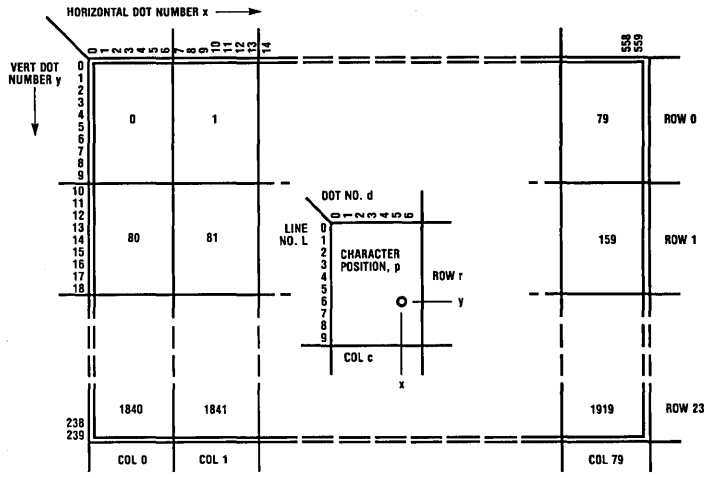
The conversion of the decimal numbers entered and saved in the Input Number registers, is performed by the subroutine ENTR. First the last decimal number entered (obviously units) is tested for ASCII number units and then saved. The second number (tens) if entered, is then tested and decremented until 0 is reached, and each decrement, 10 is added to the total number. Then the third number (hundreds) is tested and decremented to 0, each time 100 is added to the total. At the end of the conversion, H, L register contains the total number in binary. This is then saved in the respective register.

Conversion of 2 Hexadecimal Characters to an 8-Bit Word

This subroutine takes 2 ASCII characters each in the range 0 to 9, A to F, and converts them to a binary word. First, the 3 ASCII code bits are masked off the number first entered. This is shifted left 4 times and added to the masked off 4 bits of the second number entered. This 8-bit word is now 7 dots plus one attribute bit. With this method, it is easy to write/read words quickly on to the display, in the selected location. This can be demonstrated with the program DMPI (dump-in) as in the next two sections.

Display Loading

The starting address is first entered (anywhere from 8000 H to FDFFH) by keying in the first two hex numbers when requested by B = (byte), no carriage return, then the last two hex numbers. This is repeated for the end address. The bytes are then entered 2 ASCII characters at a time. If the addresses are between 8000H and CFFFH, the words will appear on the display. For example, 7F will appear as 7 dots, or 83 will appear as the 2 right-hand dots with attribute. In this way a picture can be loaded on the display.



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ROW r = INTEGER (y/10), LINE L = y−r

COLUMN c = INTEGER (X/7), DOT NUMBER d = x−c

DOT AT LOCATION x, y IS IN CHARACTER POSITION p, LINE L, DOT NO. d, WHERE p = 80r + c

FIGURE 20. CRT Display/8350 Character Address Positions

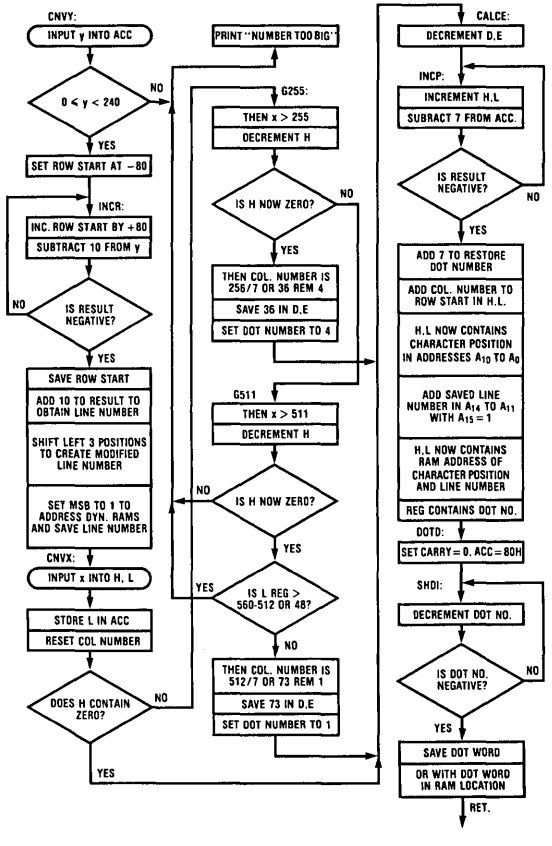

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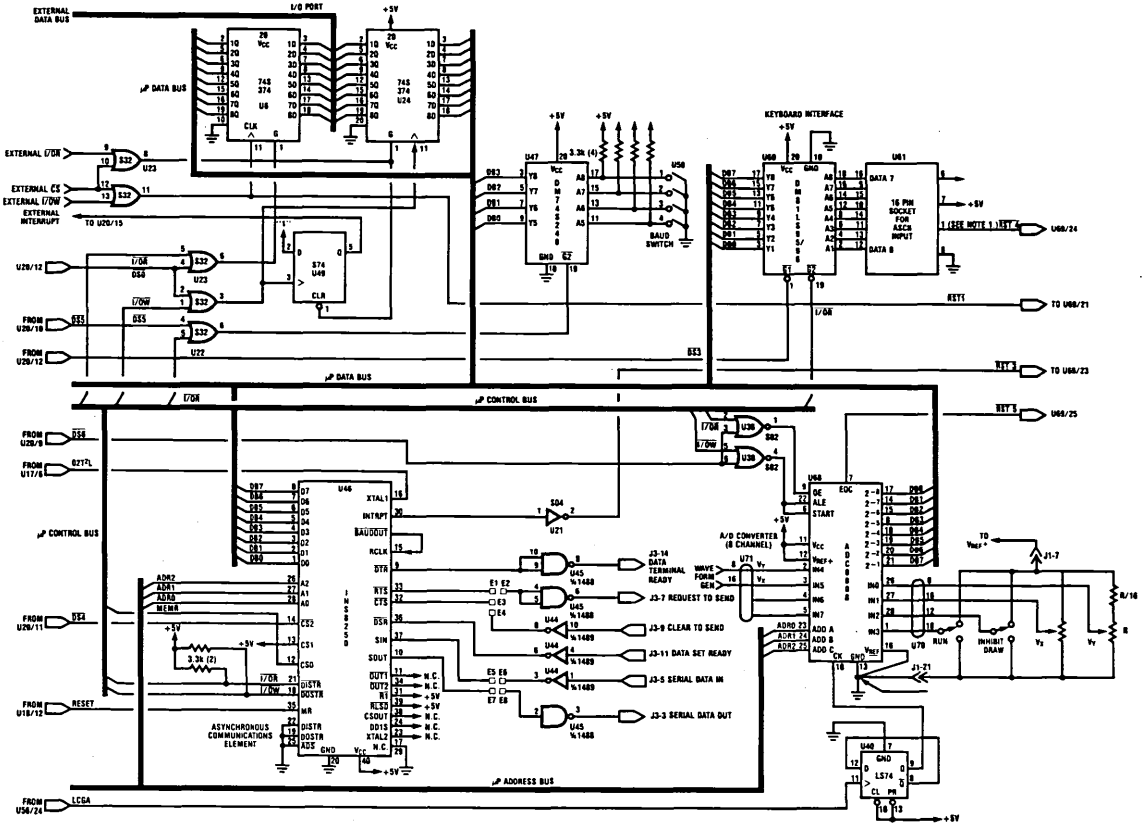
FIGURE 21. Flow Chart to Add Dot x, y to Display



Note 1: Strobe Input must be positive (+)

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Note 2: All devices bypassed with 0.1 μF 50 VDC capacitors between supply voltages and ground.

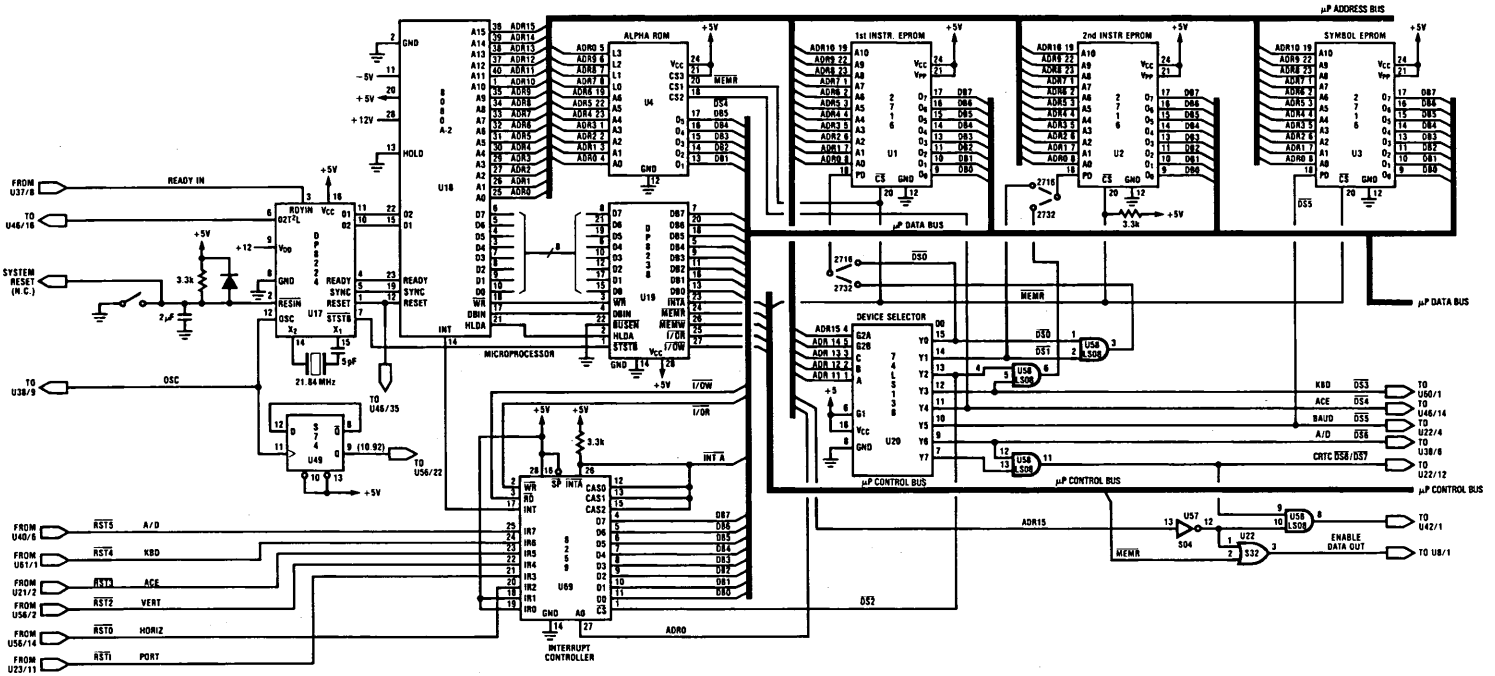
Note 3: Unless otherwise specified, SSI Logic Power as follows:

V_{CC} = Pin 14

GND = Pin 7

Note 4: For serial transfer to other systems Link E1–E2, E3–E4, E5–E6 and E7–E8 for stand alone use, connect E1–E3 and E5–E7.

DP8350/INS8080 Full Graphics Video Terminal System—Peripheral Interface Block



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Note: (Unless otherwise specified)

Note 1: Resistor values are in Ω. ¼ watt, 5%.

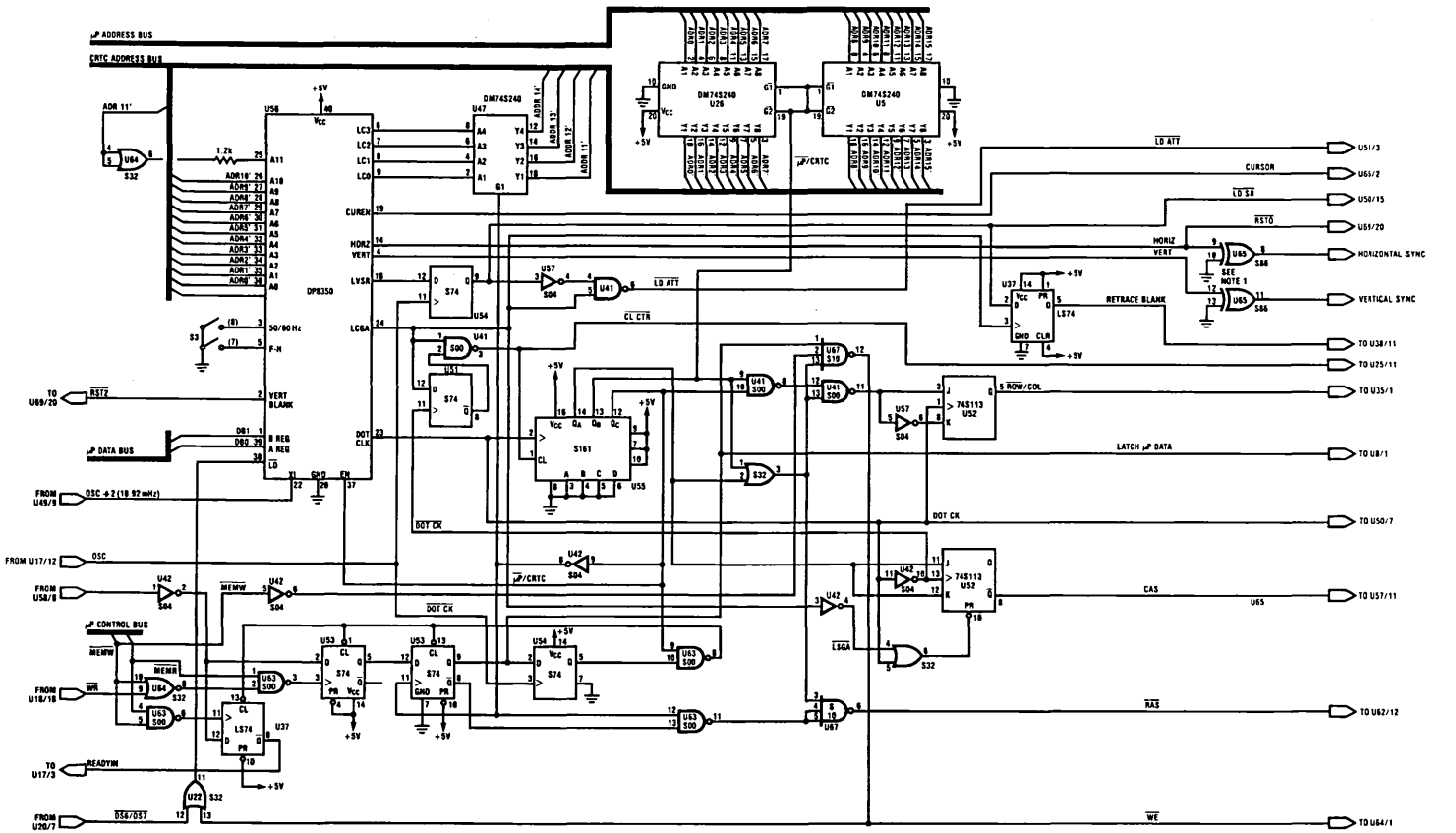
Note 2: All devices bypassed with 0.1µF 50 V_{DC} capacitor between V_{CC}

Note 3: All SSI Logic Powered as follows:

V_{CC} = Pin 14

GND = Pin 7

DP8350/INS8080 Full Graphics Video Terminal System—CPU, EPROM and Interrupt Block



Note 1: Strobe input must be positive (+).

Note 2: All devices bypassed with 0.1 μF 50 VDC capacitors between supply voltages and ground.

Note 3: Unless otherwise specified, SSI Logic Powered as follows:

V_{CC} = Pin 14 V_{CC} = Pin 18

GND = Pin 7 GND = Pin 8

DP8350/INS8080 Full Graphics Video Terminal System—Memory Control

Use of Back-Up RAM

If the DMPI addresses are between D000H and FDFFH, the information is stored in the back-up RAM. This is useful for in-system emulation, for example. By calling up the program EXT0 (External 0), if a program has previously been loaded in the back-up RAM, starting at address D000H, this program will then be executed after EXT0, carriage return. Another use of this section of RAM is the storage of different sequences of circuit diagrams other than those in the symbol EPROM. The program DRAW can then call up the starting address.

Additional Software

The power and versatility of this system is easily demonstrated with the existing software. This can be added to as required with new software, calling up existing subroutines where possible. Up to 4 kbytes of additional software can be incorporated without any hardware modifications (other than moving two links to select 2732s instead of 2716s).

Conclusion

So using all National Semiconductor ICs, at a cost of a few hundred dollars, the hardware for an intelligent terminal with full graphics capability can be fitted on one BLC80/SBC80 size card. The design is easily expandable to systems requiring color. The biggest modification is to the memory; instead of one bit per dot. 3 bits ae required for blue, green, and red, to give 8 possible combinations per dot. A small number of extra logic ICs are required, as are minor additions to the software. To select the color, a CTL key can be used followed by the code of the color. This color will then be written until changed by the CTL key. A differential CTL key followed by a number could previously have set the background.

Present Capabilities of Alphanumerics/Graphics System

Dumb Terminal Functions

**All 128 ASCII Characters Displayable	
**Space	
**Carriage Return	
**Horizontal Tab	(→) or (CTL L)
**Backspace	(←) or (CTL H)
**Linefeed	(↓) or (CTL I)
**Vertical Tab	(↑) or (CTL K)
**Select/Deselect Attribute	CTL R) with SW-1 or S-3
**Tab 8 Spaces	(Tab)(CTL T)
**Clear Cursor Row	(CTL X)
**Clear Row Right of Cursor	(CTL S)
**Initialize System	(CTL A)
**Select Baud Rate from 110 to 19,200 Using S-1 and CTL E	
**Scrolling Upwards	

Non-Standard Character/Symbol Selection

**By selecting CTL Z, symbols can be displayed for each key of the keyboard, including shifted and control keys. Also can deselect back to standard ASCII characters with CTL Z.

Graphics Programs

*CLSC: Clears screen only, leaving 13k back-up RAM unaffected

*LIST: Lists all graphics programs.

*PLOT: Plots a dot at X, Y, X is the number of horizontal dot positions from the left of screen, from 0 to 7 x 80 for the 8350, i.e., $0 \leq x \leq 559$. Y is the number of vertical dots from the top of the screen, from 0 to 10 x 24, i.e., $\leq 0 \leq y$ 239. The operator keys in the decimal values of Y and then X when requested by the display.

*VLIN: Draws a vertical line between Y1 and Y2 at X. These values are entered decimally by keyboard when requested by the display.

*HLIN: Draws a horizontal line between X1 and X2 at Y1. These values are entered decimally by keyboard when requested by the display.

*RECT: Draws a rectangle linking lines X1, X2, Y1, and Y2.

*PONG: Bounces a dot around the screen between the four walls of the display.

*DRAW: Draws a diagram on the screen from a sequence of operations saved in ASCII code in memory. The START address of the sequence is determined by the first four hexadecimal characters entered on the keyboard. The address 1D00H selects a DC voltage restoring circuit sequence located in the symbol EPROM. Address 1E00H selects a logic circuit and waveforms. Test sequences can be loaded into back-up RAM using program 'DMPI' at the starting and end address entered. This start address is then called up by the 'DRAW.' The end address must contain 0 (zero).

*SAVE: Saves in the back-up RAM a section of display contained within rows R1 to R2, and columns C1 to C2. These values are entered decimally by keyboard when requested by display. The start address in the back-up RAM is selected by the first four hexadecimal characters entered on the keyboard.

*LOAD: Loads from the back-up RAM to a section of display bounded by R1, R2, C1, C2. These values are entered decimally by keyboard when requested by the display. The back-up RAM start address is selected as in SAVE.

*DOTS: Plots N dots on any line Y1 at positions X1, Y1; ... XN, Y1; and then any new line entered in decimal by the operator. Ends the program by entering 0 (zero) when the next Y1 is requested.

*MOVD: Uses the 8-channel 8-bit A/D converter to monitor the voltages on X–Y joystick, an inhibit-draw switch, and an exit-program switch. In the DRAW mode consecutive dots are plotted to create a picture as described by the movement of the joystick. All these input signals are connected to the first A/D socket. In the inhibit DRAW mode the dot is moved around by the joystick as a cursor, and by keying in from the keyboard the desired character, this character will appear in the character field of the dot. This moving dot can be used to erase existing dots, or erase characters by keying 'SPACE' in the desired position. To exit the program, set the EXIT program switch in EXIT-DRAW mode with the Inhibit-Draw Switch in INHIBIT.

*WAVE: Uses the A/D Converter to create waveforms on the screen when the signals are connected to the second A/D socket.

*DMPO: Unloads any part of RAM to an external system starting at an address keyed in by the operator in hexadecimal characters (four) and ending at another similarly entered address. The RAM is unloaded 7 dots at a time per line of character and converted to two ASCII characters and then transmitted serially.

*DMPI: Loads any part of RAM from an external source (or the keyboard) starting at an address-selected by the first four hexadecimal characters entered on the keyboard and ending at another similarly entered address. The RAM is loaded 7 dots at a time per line of character, keyed in by two hexadecimal characters, for each word. The addresses selected can be display addresses 8000H to CFFFH or back-up RAM addresses D000 to FFFFH (warning: FE00H upwards are registers and FFFFH downwards are stack). Thus a complete picture could be loaded on to the display. Alternately a program could be loaded into back-up RAM at EXT0 (D000H), EXT1 (D800H), EXT2 (E000H), or EXT3 (F000H). The characters 'EXTn' can then be typed in on the keyboard and this will then select the instructions beginning at address EXTn. Thus in-system emulation is easily accomplished.

*EXT0: Executes a program beginning at RAM address D000H. The program must previously have been entered using DMPI selecting D000H as the starting address.

*EXT1: As EXT0 but starts at D800H.

*EXT2: As EXT0 but starts at E000H.

*EXT3: As EXT0 but starts at F000H.

Software Design for a 38.4 kbaud Data Terminal

National Semiconductor Corp.
Application Note 270
Wong Hee
Nick Samaras

INTRODUCTION

This Application Note describes a CRT terminal designed around the DP8350 CRT controller and the INS8080 microprocessor. The hardware is a modified version of the circuit described in Application Note AN-199. The software was redesigned and optimized for terminal speed and function. In its present form it is upwards compatible with the Hazeltine 1500 video terminal and has a limited graphics capability. Furthermore, it is able to communicate with a host computer via an RS-232 port, at 38.4 kbaud, without using fill-in characters or handshaking. One 2k by 8 EPROM contains all the software required to implement the terminal. An optional EPROM can be used to add features such as menu display or to transform the terminal into a calculator (in the local mode). The absence of the second EPROM does not affect the operation of the terminal as the software checks for its presence.

DATA TERMINAL FEATURES

- Modes: remote/local
- Limited graphics
- Window scrolling
- Line transmitting and local editing
- Hazeltine 1500 compatible*
- Video display: two pages, 24 x 80 characters/page
- Upper/lower case
- Scrolling plus screen roll up/roll down
- Cursor: blinking (two rates)
- Line, character insert/delete
- Attributes: dual intensity/inverse video
- Full duplex RS-232 port; 110-38400 baud
- Keyboard input: 7-bit parallel
- Full cursor control and addressing
- Cursor enable/disable
- Single board (BLC/SBC) compatible design

*The majority of the software written for the Hazeltine 1500 will run with no modification. However, there are differences.

UNIQUE FEATURES

Graphics Capability: The graphics capability of this terminal, although limited by the number of symbols (34), proves to be very helpful. Typical uses include digital waveform generation (e.g., logic analyzer display), and graph oriented displays such as histograms. A graphics menu is available in the local mode. Entering ↑Q† from the keyboard will result in a two line menu display. Line 23 displays upper and lower case characters, while line 24 displays the corresponding graphics symbols (see *Figure 3*). In local, entering ↑B will switch the terminal to the graphics mode; the ESC key can be used to exit. In remote mode, the format requirements for graphics display generation are summarized by the flowchart shown at the bottom of this page.

The same flowchart can be used in local, if the "lead-in"‡ block is omitted.

Typical transmission sequences are:

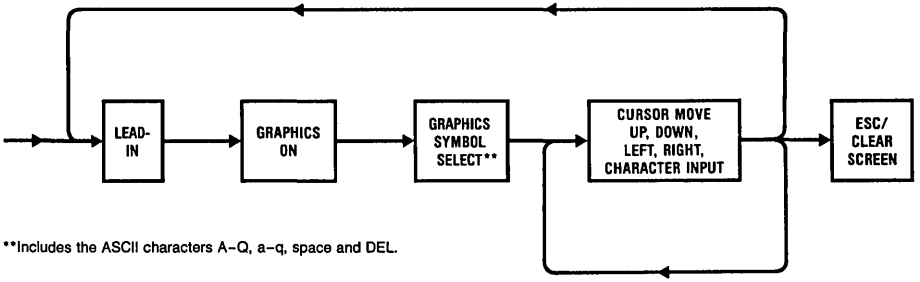
7E, 02, 42, 10, 1B
7E, 02, 63, 10, 10, 10, . . . ,10, 1B
7E, 02, 42, 8, 8, 8, 4A, 7E, 0C, 7E, 0C, 1B

All the graphics symbols, along with the upper and lower case characters, are coded into one 2716 EPROM. As a result, both the character set and the graphics symbols may be customized. The total number of available fonts is 128. The field on each displayed character is 7 rows by 10 columns. The alphanumeric symbols occupy a 5 by 7 subfield typically, except for those requiring descenders; they occupy a 5 by 9 section, while the graphics symbols utilize the whole 7 by 10 field.

Transmit: The data terminal can transmit one line of text upon receipt of the 14H code from the keyboard in local mode. Alternately, the host CPU can request transmission by sending 14H prefixed by the 7E lead-in code.

†Note that ↑ indicates a control key entry.

‡Lead-in code: 7E.



**Includes the ASCII characters A–Q, a–q, space and DEL.

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The same function can be used in a relatively unconventional way when programming in BASIC. The majority of BASIC interpreters used in small business systems or home computers incorporate a line-oriented editor, almost adequate for most of the tasks they have to perform. The basic problem with such editors is that they cannot change the flow of the program easily. In other words they cannot change line numbers. This is a shortcoming, as it is both annoying and tedious having to retype segments of text in order to change the program flow, just because the editor cannot handle altering line numbers only.

This terminal offers an efficient solution to this problem. Simply stated, it allows changing line numbers only. Here is a brief description of a typical sequence leading to text and/or line number modification. Let us assume that a BASIC interpreter is used and that the program that needs to be changed is in memory. Using the list command, the program lines to be modified can be displayed. Now, while in the Command Mode of BASIC, the terminal is switched to local. The user has effectively at his disposal a screen-oriented editor. The cursor can be moved about and text changed as desired; that, of course, includes line numbers. When the editing is completed, the user positions the cursor on the line that was altered and types ↑T. In response, the cursor scans the line, inverting the attributes. At the same time the line is transmitted to the host CPU in the same order as it was scanned, from left to right. Attribute inversion serves as feedback to the user. After the last character of each line has been transmitted, the cursor returns to the beginning of the following line. As a result, consecutive ↑T keyboard entries transmit successive lines. Thus, altering the flow of a BASIC program involves entering the local mode, changing line numbers, transmitting the modified program lines, and switching back to on-line operation. All this can be accomplished at a fraction of the time usually required otherwise. Finally, entering similar lines of text such as the ones found in "PRINT" statements, can be accomplished easily by switching to local, typing the first line and transmitting it; then moving the cursor up one line, changing the line number along with parts of the text that are different, retransmitting the line, and so on. In this way the user can create a long program segment while operating repetitively on one line.

Insert/Delete with Range: This is a rather unusual function that can assist in generating pseudo "screen window" effects. Specifically, a pre-selected number of display lines can scroll while the rest of the display remains fixed. Each "window" is defined as N lines by 80 characters, where: $1<N<48$, counting from the current cursor location to the end of page. The brief BASIC program that follows demonstrates the use of this function. In this example the display lines 1 through 4, and 19 through 24 remain "frozen". The message (100 lines long) is displayed on lines 5 through 18, demonstrating the scrolling of a section of the display.

```
100 PRINT CHR$(&H7E) + CHR$(&H11) + "d";
110 FOR I = 1 TO 100
120 PRINT CHR$(&H7E) + CHR$(&H1D)
    + CHR$(&H49)  + CHR$(12);
130 PRINT, "WINDOW SCROLLING LINE:",I,
    CHR$(&H0D)
140 NEXT I
```

80 Character Software FIFO: This is one of the key items that allows terminal communication at 38.4 kbaud without handshaking. An 80 character first-in, first-out software buffer is used. The incoming characters are stored temporarily in this buffer, while the microprocessor is servicing interrupts. As time becomes available, the characters are retrieved from the FIFO and processed. That includes performing a terminal function or moving an ASCII character to the video memory. The software allows for a large number of concurrent service requests such as row start, keyboard, as well as multiple ACE interrupts.

Fast Service Routine for Row Start Interrupt: Conventional row start address look-up and loading are not done during the row start interrupt time; instead, a simple row counting routine is used. The terminal count (a software counter) generates a triggering signal for video RAM wrap-around address loading. The use of this technique improves the system throughput substantially. Cursor and Top of the Page address loading (i.e., writing to the appropriate DP8350's registers) is done during the vertical retrace interval.

Keyboard Controlled Mode Selection: The operating mode of the terminal can be selected from the keyboard. To aid the user in identifying which mode the terminal is in, two cursor blinking rates are used. The low rate indicates remote mode; a high rate indicates local.

Other functions that can be selected from the keyboard are:

1) Upper/lower case. The default mode upon power up is determined by reading the SW3 switch setting.
2) Next page. A software switch that selects for display page one or two.

Read Cursor: In the local mode the present cursor location can be displayed on line 24, columns 79–80. For example, if the cursor is located on line 8, column 66, entering ↑E from the keyboard will result in a display of "Ag" at the bottom right hand corner of the screen. This can save time in looking up the ASCII equivalent codes of the X, Y cursor coordinates to be used in cursor addressing. (Note that, ↑E = ENQ = 05H.)

The following is an example of how this could be used in a BASIC program.

```
PRINT CHR$ (&H7E) + CHR$ (&H11) + "Ag"
```

Upon execution of the above statement, the cursor will move to line 8, column 66.

Menu Display: In the local mode the user has access to a menu display that summarizes the terminal's functions, along with the corresponding control codes (see *Figure 1*). This feature is optional and resides in EPROM #2. The important thing to note is that various kinds of menu/HELP displays can be implemented easily in this fashion. This function can be accessed from the keyboard. Alternately, a dedicated HELP key (that generates the 1D code) can be used.

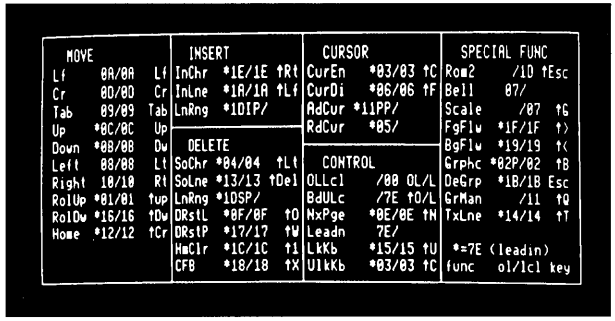

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FIGURE 1. Sample Menu Display

Character Generator Fonts

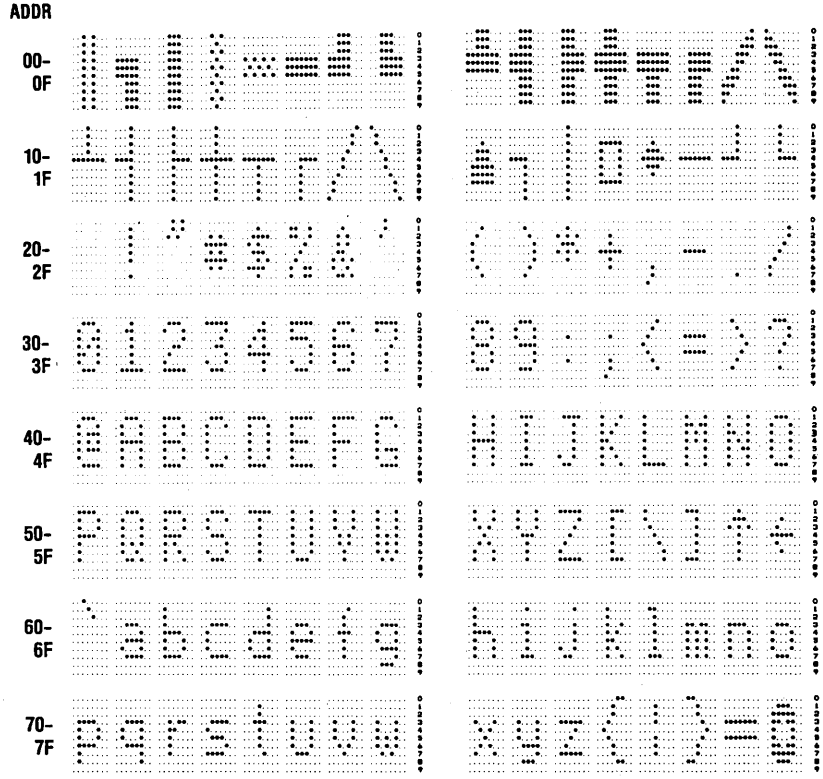

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FIGURE 2. Sample Character Font

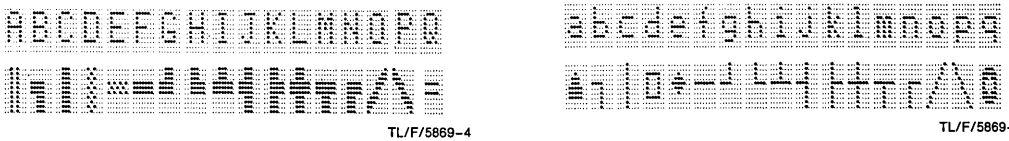

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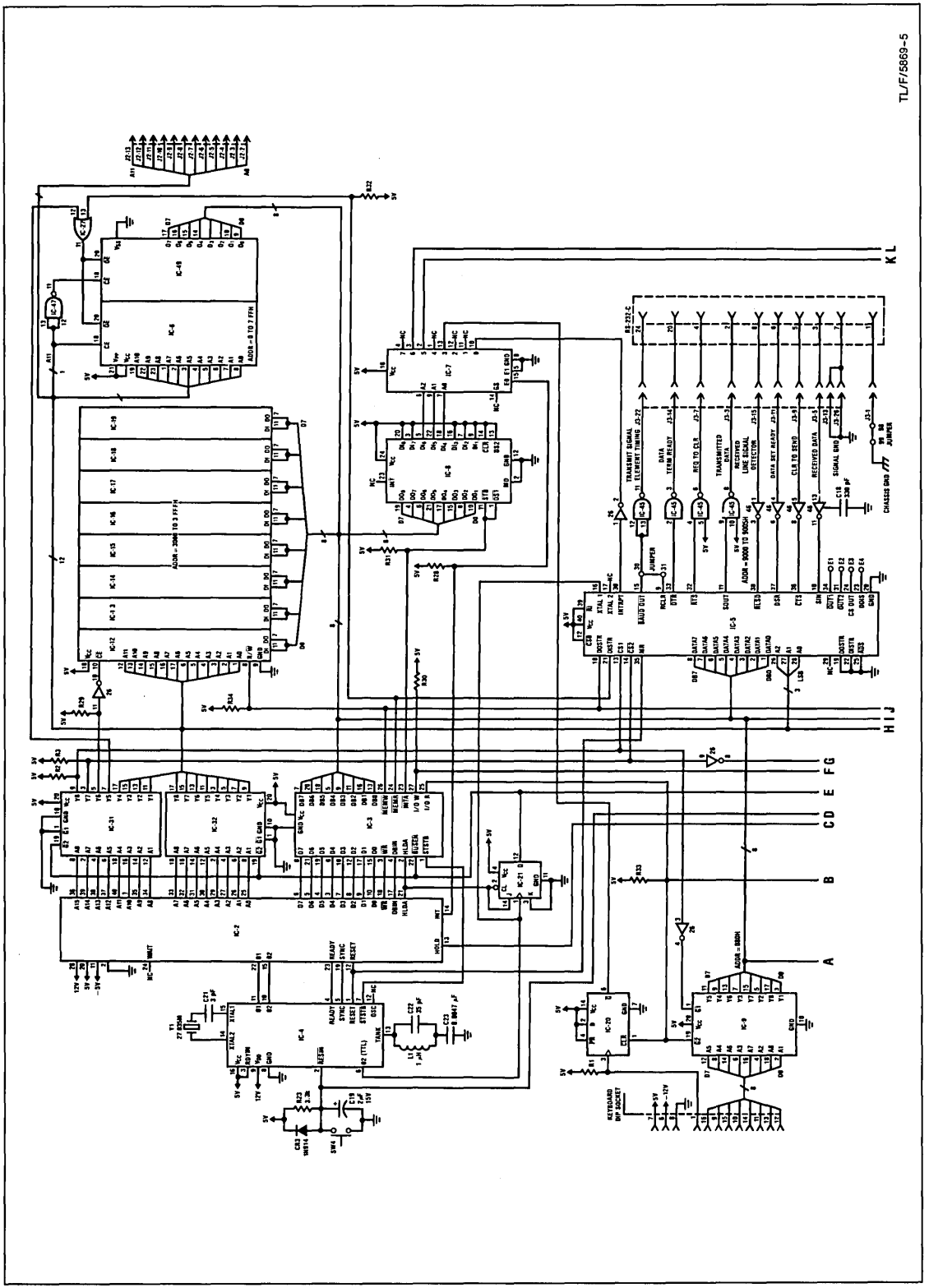
FIGURE 3. Graphics Menu Shown at the Bottom of the Screen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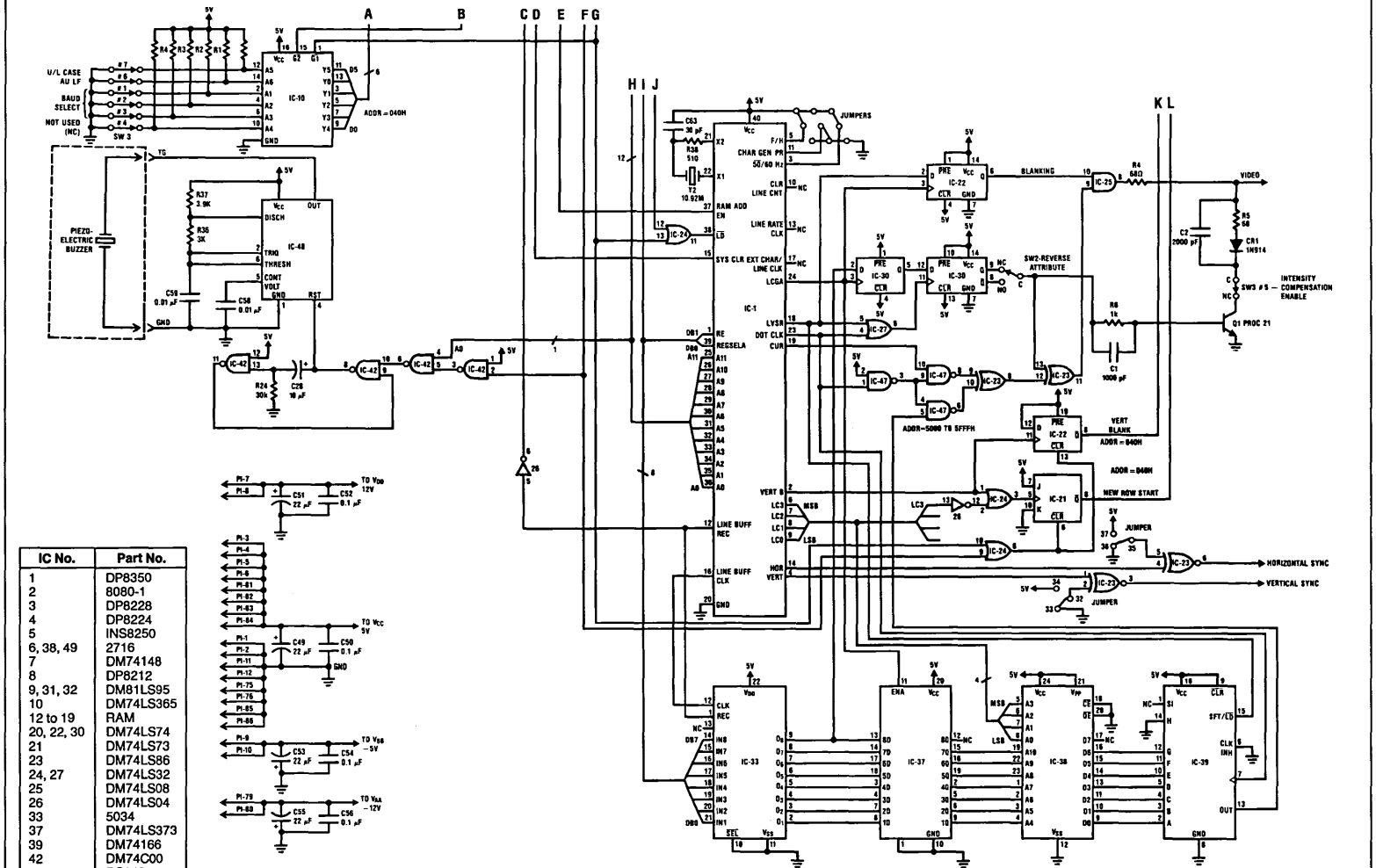

IC No.	Part No.
1	DP8350
2	8080-1
3	DP8228
4	DP8224
5	INS8250
6, 38, 49	2716
7	DM74148
8	DP8212
9, 31, 32	DM81LS95
10	DM74LS365
12 to 19	RAM
20, 22, 30	DM74LS74
21	DM74LS73
23	DM74LS86
24, 27	DM74LS32
25	DM74LS08
26	DM74LS04
33	5034
37	DM74LS373
39	DM74166
42	DM74C00
45	DS1488
46	DS1489
47	DM74LS00
48	LM555

All pull-up resistors = 4.7k ¼W

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Control Functions Summary

Functions	On-Line / Local	Remarks
Cursor Move/Control		
Line Feed	0A / 0A	
Carriage Return	0D / 0D	
Tab	09 / 09	
Cursor Up	7E, 0C / 0C	
Cursor Down	7E, 0B / 0B	
Cursor Left	08 / 08	
Cursor Right	10 / 10	
Home	7E, 12 / 12	
Home and Clear	7E, 1C / 1C	
Enable Cursor	7E, 03 / 03	
Disable Cursor	7E, 06 / 06	
Address Cursor	7E, 11, X, Y /	Remote Only
Read Cursor	7E, 05 / 05	
Insert		
Character Insert	7E, 1E / 1E	
Line Insert	7E, 1A / 1A	
Line Insert with Range	7E, 1D, 49, Y	Remote Only
Delete		
Character Strip	7E, 04 / 04	
Character Delete	7F / 7F	
Line Delete	7E, 13 / 13	
Line Delete with Range	7E, 1D, 53, Y /	Remote Only
Clear to End of Line	7E, 0F / 0F	
Clear to End of Page	7E, 17 / 17	
Miscellaneous		
Local/Remote	/ 00	Local Only
Upper/Lower Case	/ 7E	Local Only
Next Page	7E, 0E / 0E	
Keyboard Lock	7E, 15 / 15	
Keyboard Unlock	7E, 03 / 03	
Bell	07 /	Remote Only
Special Functions		
Function Menu	/ 1D	A summary of available functions and their corresponding codes (local mode only).
Graphics On	7E, 02 / 02	Enter graphics mode.
Graphics Off	7E, 1B / 1B	Exit graphics mode.
Graphics Menu	/ 11	Line 23 displays upper and lower case characters and line 24 the corresponding graphics symbols (local).
Line Transmit	7E, 14 / 14	Transmits the cursor line and inverts its attributes.
Foreground Follows	7E, 1F / 1F	
Background Follows	7E, 19 / 19	
Clear Foreground	7E, 18 / 18	
Scale	/ 07	The line above the cursor becomes a scale (1–80). This is an aid for graphics and text alignment (local).
Roll Up	7E, 01 / 01	
Roll Down	7E, 16 / 16	

Character Generator Hex Dump

ADDR	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	14	14	14	14	14	14	14	14	14	14	0	0	0	0	0	0
10	0	0	0	7C	7C	7C	1C	1C	1C	1C	0	0	0	0	0	0
20	1C	1C	1C	1C	1C	1C	1C	1C	1C	1C	0	0	0	0	0	0
30	14	8	14	8	14	8	14	8	14	8	0	0	0	0	0	0
40	0	0	0	55	2A	55	0	0	0	0	0	0	0	0	0	0
50	0	0	0	7F	7F	7F	0	0	0	0	0	0	0	0	0	0
60	1C	1C	1C	7C	7C	7C	0	0	0	0	0	0	0	0	0	0
70	1C	1C	1C	1F	1F	1F	0	0	0	0	0	0	0	0	0	0
80	1C	1C	1C	7F	7F	7F	0	0	0	0	0	0	0	0	0	0
90	1C	1C	1C	7C	7C	7C	1C	1C	1C	1C	0	0	0	0	0	0
A0	1C	1C	1C	1F	1F	1F	1C	1C	1C	1C	0	0	0	0	0	0
B0	1C	1C	1C	7F	7F	7F	1C	1C	1C	1C	0	0	0	0	0	0
C0	0	0	0	7F	7F	7F	1C	1C	1C	1C	0	0	0	0	0	0
D0	0	0	0	1F	1F	1F	1C	1C	1C	1C	0	0	0	0	0	0
E0	1	3	7	E	C	1B	38	70	60	40	0	0	0	0	0	0
F0	40	60	70	38	18	C	E	7	3	1	0	0	0	0	0	0

ADDR	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
100	0	0	8	1C	1C	3E	3E	3E	0	0	0	0	0	0	0	0
110	0	0	0	0	7B	8	8	8	8	8	0	0	0	0	0	0
120	8	8	8	8	8	8	8	8	8	8	0	0	0	0	0	0
130	0	0	3E	22	22	22	22	3E	0	0	0	0	0	0	0	0
140	0	0	8	1C	3E	1C	8	0	0	0	0	0	0	0	0	0
150	0	0	0	0	7F	0	0	0	0	0	0	0	0	0	0	0
160	8	8	8	8	78	0	0	0	0	0	0	0	0	0	0	0
170	8	8	8	8	F	0	0	0	0	0	0	0	0	0	0	0
180	8	8	8	8	7F	0	0	0	0	0	0	0	0	0	0	0
190	8	8	8	8	78	8	8	8	8	8	0	0	0	0	0	0
1A0	8	8	8	8	F	8	8	8	8	8	0	0	0	0	0	0
1B0	8	8	8	8	7F	8	8	8	8	8	0	0	0	0	0	0
1C0	0	0	0	0	7F	8	8	8	8	8	0	0	0	0	0	0
1D0	0	0	0	0	F	8	8	8	8	8	0	0	0	0	0	0
1E0	1	2	2	4	8	8	10	20	20	40	0	0	0	0	0	0
1F0	40	20	20	10	8	8	4	2	2	1	0	0	0	0	0	0

ADDR	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
200	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
210	0	8	8	8	8	8	0	8	0	0	0	0	0	0	0	0
220	A	A	14	0	0	0	0	0	0	0	0	0	0	0	0	0
230	0	0	14	3E	14	3E	14	0	0	0	0	0	0	0	0	0
240	0	8	1E	28	1C	A	3C	8	0	0	0	0	0	0	0	0
250	0	32	32	4	8	10	26	26	0	0	0	0	0	0	0	0
260	0	8	14	14	18	2A	24	1A	0	0	0	0	0	0	0	0
270	8	8	10	0	0	0	0	0	0	0	0	0	0	0	0	0
280	0	8	10	20	20	20	10	8	0	0	0	0	0	0	0	0
290	0	8	4	2	2	2	4	8	0	0	0	0	0	0	0	0
2A0	0	8	2A	1C	2A	8	0	0	0	0	0	0	0	0	0	0
2B0	0	0	8	8	3E	8	8	0	0	0	0	0	0	0	0	0
2C0	0	0	0	0	0	0	8	8	10	0	0	0	0	0	0	0
2D0	0	0	0	0	3E	0	0	0	0	0	0	0	0	0	0	0
2E0	0	0	0	0	0	0	0	8	0	0	0	0	0	0	0	0
2F0	0	2	2	4	8	10	20	20	0	0	0	0	0	0	0	0

ADDR	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
300	0	1C	22	26	2A	32	22	1C	0	0	0	0	0	0	0	0
310	0	8	18	8	8	8	8	3E	0	0	0	0	0	0	0	0
320	0	1C	22	2	C	10	20	3E	0	0	0	0	0	0	0	0
330	0	3E	2	4	C	2	22	1C	0	0	0	0	0	0	0	0
340	0	4	C	14	24	3E	4	4	0	0	0	0	0	0	0	0
350	0	3E	20	3C	2	2	22	1C	0	0	0	0	0	0	0	0
360	0	1C	22	20	3C	22	22	1C	0	0	0	0	0	0	0	0
370	0	3E	22	2	4	8	8	8	0	0	0	0	0	0	0	0
380	0	1C	22	22	1C	22	22	1C	0	0	0	0	0	0	0	0
390	0	1C	22	22	1E	2	2	1C	0	0	0	0	0	0	0	0
3A0	0	0	0	8	0	0	8	0	0	0	0	0	0	0	0	0
3B0	0	0	0	8	0	0	8	8	10	0	0	0	0	0	0	0
3C0	0	4	8	10	20	10	8	4	0	0	0	0	0	0	0	0
3D0	0	0	0	3E	0	3E	0	0	0	0	0	0	0	0	0	0
3E0	0	10	8	4	2	4	8	10	0	0	0	0	0	0	0	0
3F0	0	1C	22	2	4	8	0	8	0	0	0	0	0	0	0	0

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Character Generator Hex Dump (Continued)

ADDR	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
400	0	1C	22	2E	2A	2E	20	1E	0	0	0	0	0	0	0	0
410	0	1C	22	22	3E	22	22	22	0	0	0	0	0	0	0	0
420	0	3C	22	22	3C	22	22	3C	0	0	0	0	0	0	0	0
430	0	1C	22	20	20	20	22	1C	0	0	0	0	0	0	0	0
440	0	3C	22	22	22	22	22	3C	0	0	0	0	0	0	0	0
450	0	3E	20	20	3C	20	20	3E	0	0	0	0	0	0	0	0
460	0	3E	20	20	3C	20	20	20	0	0	0	0	0	0	0	0
470	0	1C	22	20	20	2E	22	1E	0	0	0	0	0	0	0	0
480	0	22	22	22	3E	22	22	22	0	0	0	0	0	0	0	0
490	0	1C	8	8	8	8	8	1C	0	0	0	0	0	0	0	0
4A0	0	1E	4	4	4	4	24	18	0	0	0	0	0	0	0	0
4B0	0	22	24	28	30	28	24	22	0	0	0	0	0	0	0	0
4C0	0	20	20	20	20	20	20	3E	0	0	0	0	0	0	0	0
4D0	0	22	36	2A	2A	22	22	22	0	0	0	0	0	0	0	0
4E0	0	22	22	32	2A	26	22	22	0	0	0	0	0	0	0	0
4F0	0	1C	22	22	22	22	22	1C	0	0	0	0	0	0	0	0

ADDR	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
500	0	3C	22	22	3C	20	20	20	0	0	0	0	0	0	0	0
510	0	1C	22	22	22	2A	24	1A	0	0	0	0	0	0	0	0
520	0	3C	22	22	3C	28	24	22	0	0	0	0	0	0	0	0
530	0	1C	22	20	1C	2	22	1C	0	0	0	0	0	0	0	0
540	0	3E	8	8	8	8	8	8	0	0	0	0	0	0	0	0
550	0	22	22	22	22	22	22	1C	0	0	0	0	0	0	0	0
560	0	22	22	22	14	14	8	8	0	0	0	0	0	0	0	0
570	0	22	22	22	2A	2A	2A	14	0	0	0	0	0	0	0	0
580	0	22	22	14	8	14	22	22	0	0	0	0	0	0	0	0
590	0	22	22	22	1C	8	8	8	0	0	0	0	0	0	0	0
5A0	0	3E	2	4	8	10	20	3E	0	0	0	0	0	0	0	0
5B0	0	E	8	8	8	8	8	E	0	0	0	0	0	0	0	0
5C0	0	20	20	10	8	4	2	2	0	0	0	0	0	0	0	0
5D0	0	38	8	8	8	8	8	38	0	0	0	0	0	0	0	0
5E0	0	8	1C	2A	8	8	8	8	0	0	0	0	0	0	0	0
5F0	0	0	8	10	3E	10	8	0	0	0	0	0	0	0	0	0

ADDR	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
600	10	8	4	0	0	0	0	0	0	0	0	0	0	0	0	0
610	0	0	0	1C	2	1E	22	1E	0	0	0	0	0	0	0	0
620	0	20	20	20	3C	22	22	3C	0	0	0	0	0	0	0	0
630	0	0	0	1E	20	20	20	1E	0	0	0	0	0	0	0	0
640	0	2	2	2	1E	22	22	1E	0	0	0	0	0	0	0	0
650	0	0	0	1C	22	3E	20	1C	0	0	0	0	0	0	0	0
660	0	4	8	8	1C	8	8	8	0	0	0	0	0	0	0	0
670	0	0	0	1E	22	22	1E	2	1C	0	0	0	0	0	0	0
680	0	20	20	20	3C	22	22	22	0	0	0	0	0	0	0	0
690	0	8	0	18	8	8	8	1C	0	0	0	0	0	0	0	0
6A0	0	4	0	4	4	4	24	18	0	0	0	0	0	0	0	0
6B0	0	10	10	12	14	18	14	12	0	0	0	0	0	0	0	0
6C0	0	18	8	8	8	8	8	1C	0	0	0	0	0	0	0	0
6D0	0	0	0	36	2A	2A	2A	2A	0	0	0	0	0	0	0	0
6E0	0	0	0	3C	22	22	22	22	0	0	0	0	0	0	0	0
6F0	0	0	0	1C	22	22	22	1C	0	0	0	0	0	0	0	0

ADDR	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
700	0	0	0	3C	22	22	3C	20	20	0	0	0	0	0	0	0
710	0	0	0	1E	22	22	1E	2	2	0	0	0	0	0	0	0
720	0	0	0	16	18	10	10	10	0	0	0	0	0	0	0	0
730	0	0	0	1E	20	1C	2	3C	0	0	0	0	0	0	0	0
740	0	8	8	1C	8	8	8	4	0	0	0	0	0	0	0	0
750	0	0	0	22	22	22	22	1C	0	0	0	0	0	0	0	0
760	0	0	0	22	22	22	14	8	0	0	0	0	0	0	0	0
770	0	0	0	22	22	2A	2A	14	0	0	0	0	0	0	0	0
780	0	0	0	22	14	8	14	22	0	0	0	0	0	0	0	0
790	0	0	0	22	22	22	1E	2	1C	0	0	0	0	0	0	0
7A0	0	0	0	3E	4	8	10	3E	0	0	0	0	0	0	0	0
7B0	6	8	8	10	20	10	8	8	6	0	0	0	0	0	0	0
7C0	0	8	8	8	0	8	8	8	0	0	0	0	0	0	0	0
7D0	30	8	8	4	2	4	8	8	30	0	0	0	0	0	0	0
7E0	0	0	0	7F	0	7F	0	0	0	0	0	0	0	0	0	0
7F0	0	1C	3E	36	22	22	36	3E	1C	0	0	0	0	0	0	0

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```
 STARPLEX MACRO-ASSEMBLER V2.0          PAGE    1
CRT801

                              TITLE CRT801
                        ;May 1980
  0000'                 ASEG
                        ORG     00000h
                        ;constants
  000A                  LF      equ     0Ah
  000D                  CR      equ     0Dh
  0020                  SPC     equ     020h
  007E                  LINC    equ     07Eh    ;leadin code
  0060                  RWRG    equ     low RR48-low RR1+2
  0003                  KULCDE  equ     03h     ;kbd unlock code
                        ;I/O ports
  0080                  KBDPRT  equ     080h    ;keyboard
  0040                  ROWPRT  equ     040h    ;row interrupt
  0040                  VERPRT  equ     040h    ;vertical interrupt
  0040                  SETSW   equ     040h    ;baud sel,autolf,u/lcase
  0002                  LCLIND  equ     2       ;local indicator
  0001                  BELPRT  equ     1       ;bell
                        ;ace
  9000                  ACEDTA  equ     09000h  ;data
  9001                  ACEITR  equ     ACEDTA+1;interrupt mask
  9003                  ACECTL  equ     ACEDTA+3;control
  9005                  ACESTU  equ     ACEDTA+5;transmit status

                        ;ram assignment
  3FFF                  FROWH   equ     03FFFh  ;first row reg pair
  3FFE                  FROW    equ     FROWh-1 ;
  3FFD                  LROWH   equ     FROWh-2 ;last row reg pair
  3FFC                  LROW    equ     FROWh-3 ;
  3FFB                  CROWH   equ     FROWh-4 ;cursor row reg pair
  3FFA                  CROW    equ     FROWh-5 ;
  3FF9                  CURH    equ     CROW-1  ;cursor reg pair
  3FF8                  CUR     equ     CROW-2  ;
  3FF7                  TOPH    equ     CUR-1   ;top of page reg pair
  3FF6                  TOP     equ     CUR-2   ;
  3FF5                  NRW     equ     TOP-1   ;row counter
  3FF4                  VCALEN  equ     TOP-2   ;vert calc routine enable
  3FF3                  GSYMBL  equ     VCALEN-1;graphics symbol
  3FF2                  AULF    equ     GSYMBL-1;auto linefeed,0=auto lf
  3FF1                  LOCLM   equ     AULF-1  ;local mode,0=remote
  3FF0                  ULCASE  equ     AULF-2  ;upper/lower case,0=lower
  3FEF                  GECNTL  equ     AULF-3  ;graphic enable,0=disable
  3FEE                  KBDLCK  equ     AULF-4  ;keyboard lock,0=unlock
  3FED                  RTECTL  equ     KBDLCK-1;cursor blink rate cntl
  3FEC                  CUREN   equ     KBDLCK-2;cursor enable,0=off
  3FEB                  CURTMR  equ     KBDLCK-3;cursor blinking timer
  3FEA                  FFWCT   equ     KBDLCK-4;ace fifo word count
  3FE9                  LEADIN  equ     KBDLCK-5;leadin mode,0=no leadin

  3FE8                  ICMD    equ     KBDLCK-6;insert char mode,0=insert
  3FE7                  CPYCTL  equ     ICMD-1  ;row copy direction cntl
  3FE6                  FFWRT   equ     CPYCTL-1;fifo write pointer
  3FE5                  FFRD    equ     CPYCTL-2;fifo read pointer
  3FE5                  STK     equ     FFRD    ;stack      3FE4h down
  3FA3                  LINP    equ     FFEND+4 ;leadin parameter storage
  3FA2                  LINWCT  equ     FFEND+3 ;leadin word count

 STARPLEX MACRO-ASSEMBLER V2.0          PAGE    2
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  3FA1                  LINFH   equ     FFEND+2 ;leadin func jmp addr high
  3FA0                  LINF    equ     FFEND+1 ;leadin func jmp addr low
  3F9F                  FFEND   equ     03F9Fh  ;ace fifo end
  3F50                  FFSTRT  equ     03F50h  ;ace fifo start 3F50/3F9Fh
  3F20                  FBG     equ     03F20h  ;fore/background cntl
  3F00                  DMYROW  equ     03F00h  ;dummy row  3F00/3F4Fh
  3780                  FCHR2   equ     03780h  ;page 2, 1st char

                        ;INTERRUPTS
                        ;***********************************************
  0000  F3              START:  DI                      ;restart 0
  0001  21 3F00                 LXI     H,DMYROW        ;clr non video ram
  0004  F9                      SPHL
  0005  C3 00E2                 JMP     INIT
                        ;---------------------------------------
                        ;row interrupt
  0008  F5              ROW:    PUSH    PSW             ;restart 1
  0009  0C                      INR     C
  000A  C2 0066                 JNZ     NOWRAP          ;no wrap arroud
  000D  C3 0061                 JMP     VRWRAP          ;do wrap arround
                        ;---------------------------------------
                        ;vertical interrupt
  0010  E5              VERT:   PUSH    H               ;restart 2
  0011  21 3FF5                 LXI     H,NRW
  0014  4E                      MOV     C,M             ;load NRW
  0015  C3 07AE                 JMP     VTSUB
                        ;---------------------------------------
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```
                        ;ace duplicate interrupt
0018    C3 0038         ACEDUP: JMP     ACE             ;restart 3
                        ;{FUNCTION} disable cursor
0018    21 3FEC         DICUR:  LXI     H,CUREN         ;disable cursor
001E    77                      MOV     M,A             ;a=0
001F    C9                      RET
                        ;---------------------------------------
                        ;keyboard interrupt
0020    E5              KBD:    PUSH    H               ;restart 4
0021    F5                      PUSH    PSW
0022    21 3FEE                 LXI     H,KBDLCK        ;keyboard lock cntl
0025    C3 02C9                 JMP     KBDINT
                        ;---------------------------------------
                        ;row duplicate interrupt
0028    F5              ROWDP:  PUSH    PSW             ;restart 5
0029    0C                      INR     C
002A    C2 0066                 JNZ     NOWRAP
002D    C3 0061                 JMP     VRWRAP
                        ;---------------------------------------
                        ;vertical duplicate interrupt
0030    C3 0010         VERTDP: JMP     VERT            ;restart 6
0033    EB              TABSTP: XCHG                    ;hl=crow
0034    D1                      POP     D               ;remove call
0035    D1                      POP     D
0036    73                      MOV     M,E             ;return org crow
0037    C9                      RET
                        ;---------------------------------------
                        PAGE

 STARPLEX MACRO-ASSEMBLER V2.0          PAGE    3
CRTB01
  0038
                        ;ACE INTERRUPT
                        ;*********************************************
0038    E5              ACE:    PUSH    H
0039    F5                      PUSH    PSW
003A    21 3FEB                 LXI     H,CURTMR
003D    D5                      PUSH    D
003E    AF                      XRA     A
003F    77                      MOV     M,A     ;reset cursor timer
0040    2B                      DCX     H       ;FFWCT
0041    34                      INR     M       ;fifo empty?
0042    C2 0244                 JNZ     STFIFO  ;no, store to fifo

0045    2B                      DCX     H       ;leadin
0046    B6                      ORA     M
0047    3A 9000                 LDA     ACEDTA  ;read ace
004A    FB                      EI
004B    C2 0283                 JNZ     LINMDE  ;leadin mode

004E    E6 7F           FIFACE: ANI     07Fh
0050    11 0267                 LXI     D,FFCHK
0053    D5                      PUSH    D       ;pseudo call
0054    FE 0A                   CPI     LF
0056    CA 03B1                 JZ      LFEED
0059    CD 015C                 CALL    CALJMP
005C    E6 87                   ANI     087h    ;leadin+jmp addr high
005E    F8                      RM              ;leadin required, return
005F    67              LCLFUN: MOV     H,A     ;jmp addr high
0060    E9                      PCHL            ;do function


                        ;row interrupt continue
                        ;*********************************************
0061    3E 01           VRWRAP: MVI     A,1
0063    32 5000                 STA     05000h  ;wrap arround addr
0066    D3 40           NOWRAP: OUT     ROWPRT  ;clr row flip/flop
0068    F1                      POP     PSW
0069    FB                      EI
006A    C9                      RET


                        ;WRITE TO ACE
                        ;*********************************************
006B    3E 0D           SNDCR:  MVI     A,CR
006D    57              WTACEA: MOV     D,A

006E    3A 9005         WTACED: LDA     ACESTU  ;check status
0071    FE 60                   CPI     060h    ;hold/tx register
0073    DA 006E                 JC      WTACED  ;not ready
0076    CD 075E                 CALL    $DLY    ;delay

0079    7A              OUTACE: MOV     A,D
007A    32 9000                 STA     ACEDTA  ;write to ace
007D    C9                      RET
                        PAGE
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 STARPLEX MACRO-ASSEMBLER V2.0          PAGE    4
CRT801
  007E
                        ;ROW START LOOKUP TABLE     (start addr=7Eh)
                        ;*********************************************
  007E    3EB0          ROW47D: dw      03EB0h
  0080    3000          ROW48D: dw      03000h
  0082    3050          ROW1:   dw      03050h
  0084    30A0          ROW2:   dw      030A0h
  0086    30F0          ROW3:   dw      030F0h
  0088    3140          ROW4:   dw      03140h
  008A    3190          ROW5:   dw      03190h
  008C    31E0          ROW6:   dw      031E0h
  008E    3230          ROW7:   dw      03230h
  0090    3280          ROW8:   dw      03280h
  0092    32D0          ROW9:   dw      032D0h
  0094    3320          ROW10:  dw      03320h
  0096    3370          ROW11:  dw      03370h
  0098    33C0          ROW12:  dw      033C0h
  009A    3410          ROW13:  dw      03410h
  009C    3460          ROW14:  dw      03460h
  009E    34B0          ROW15:  dw      034B0h
  00A0    3500          ROW16:  dw      03500h
  00A2    3550          ROW17:  dw      03550h
  00A4    35A0          ROW18:  dw      035A0h
  00A6    35F0          ROW19:  dw      035F0h
  00A8    3640          ROW20:  dw      03640h
  00AA    3690          ROW21:  dw      03690h
  00AC    36E0          ROW22:  dw      036E0h
  00AE    3730          ROW23:  dw      03730h
  00B0    3780          ROW24:  dw      03780h
  00B2    37D0          ROW25:  dw      037D0h
  00B4    3820          ROW26:  dw      03820h
  00B6    3870          ROW27:  dw      03870h
  00B8    38C0          ROW28:  dw      038C0h
  00BA    3910          ROW29:  dw      03910h
  00BC    3960          ROW30:  dw      03960h
  00BE    39B0          ROW31:  dw      039B0h
  00C0    3A00          ROW32:  dw      03A00h
  00C2    3A50          ROW33:  dw      03A50h
  00C4    3AA0          ROW34:  dw      03AA0h
  00C6    3AF0          ROW35:  dw      03AF0h
  00C8    3B40          ROW36:  dw      03B40h
  00CA    3B90          ROW37:  dw      03B90h
  00CC    3BE0          ROW38:  dw      03BE0h
  00CE    3C30          ROW39:  dw      03C30h
  00D0    3C80          ROW40:  dw      03C80h
  00D2    3CD0          ROW41:  dw      03CD0h
  00D4    3D20          ROW42:  dw      03D20h
  00D6    3D70          ROW43:  dw      03D70h
  00D8    3DC0          ROW44:  dw      03DC0h
  00DA    3E10          ROW45:  dw      03E10h
  00DC    3E60          ROW46:  dw      03E60h
  00DE    3EB0          ROW47:  dw      03EB0h
  00E0    3F00          ROW48:  dw      03F00h
                        PAGE

 STARPLEX MACRO-ASSEMBLER V2.0          PAGE    5
CRT801
  00E2
                        ;INITIALIZE
                        ;*********************************************
  00E2    3E 20         INIT:   MVI     A,SPC   ;space
  00E4    16 E9                 MVI     D,low LEADIN;byte count
  00E6    CD 04C7               CALL    DRLLP   ;store spaces
  00E9    AF                    XRA     A
  00EA    32 3FA2               STA     LINWCT  ;zero leadin word count
  00ED    16 17                 MVI     D,256-low LEADIN;byte count
  00EF    CD 04C7               CALL    DRLLP   ;store zeros
  00F2    31 3FE7               LXI     SP,STK+2
  00F5    21 5050               LXI     H,05050h
  00F8    E5                    PUSH    H       ;set up fifo rd/wrt ptrs
  00F9    CD 04AE               CALL    CURULK  ;enable cursor,unlock kbd
  00FC    32 3FEA               STA     FFWCT   ;zero fifo word count(FFh)
  00FF    23                    INX     H       ;RTECTL
  0100    36 1C                 MVI     M,01Ch  ;cursor blink cntl
  0102    2E FC                 MVI     L,low LROW;last row
  0104    36 B0                 MVI     M,low RR24
  0106    2E FE                 MVI     L,low FROW;first row
  0108    36 82                 MVI     M,low RR1
  010A    DB 80                 IN      KBDPRT  ;clear keyboard intr
  010C    CD 04CE               CALL    CLRSCN  ;clear screen
  010F    CD 07BF               CALL    ACESW   ;init ace, read setsw
  0112    3E 3F         PATTN:  MVI     A,03Fh
  0114    21 37B0               LXI     H,FCHR2 ;1st byte of page 2
  0117    75            PTNLP:  MOV     M,L     ;write pattern
  0118    23                    INX     H
  0119    BC                    CMP     H
```

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```
 011A    C2 0117              JNZ     PTNLP
 011D    D3 01                OUT     BELPRT  ;ring bell for ready

                      ;CALCULATE SCREEN ADDR AFTER VERTICAL INTERRUPT
 011F    2E EB        VCAL:   MVI     L,low CURTMR
 0121    7E                   MOV     A,M
 0122    2F                   CMA
 0123    34                   INR     M       ;cursor timer
 0124    23                   INX     H       ;cursor enable
 0125    A6                   ANA     M
 0126    23                   INX     H       ;rate cntl
 0127    A6                   ANA     M       ;blink rate mask
 0128    C4 0174              CNZ     CURLOC  ;cursor on
 012B    3E 20                MVI     A,020h  ;8350 offset
 012D    84                   ADD     H       ;offset addr high
 012E    67                   MOV     H,A     ;=5Fh if cursor off
 012F    E5                   PUSH    H       ;save cursor
 0130    2A 3FFE              LHLD    FROW
 0133    2B                   DCX     H       ;fetch row start
 0134    7E                   MOV     A,M
 0135    C6 20                ADI     020h    ;offset addr high
 0137    57                   MOV     D,A
 0138    2B                   DCX     H
                      PAGE

 STARPLEX MACRO-ASSEMBLER V2.0          PAGE    6
CRT801
 0139
 0139    5E                   MOV     E,M     ;de=top of page
 013A    7D                   MOV     A,L     ;calc row wrap constant
 013B    0F                   RRC             ;divide by 2
 013C    C6 8F                ADI     08Fh    ;add offset
 013E    E1                   POP     H       ;cursor location
 013F    F3                   DI
 0140    22 3FF8              SHLD    CUR     ;update cursor
 0143    EB                   XCHG
 0144    22 3FF6              SHLD    TOP     ;update top of page
 0147    21 3FF5              LXI     H,NRW
 014A    77                   MOV     M,A     ;row wrap constant
 014B    2B                   DCX     H       ;VCALEN
 014C    36 00                MVI     M,0     ;disable VCAL routine
 014E    FB           WAIT:   EI
 014F    76                   HLT
 0150    7E                   MOV     A,M     ;VCALEN
 0151    B7                   ORA     A       ;check from vert intr
 0152    CA 014E              JZ      WAIT    ;no
 0155    C3 011F              JMP     VCAL    ;do screen calculations

                      ;CALCULATE JMP ADDR
 0158    2E E9        CJMP:   MVI     L,low LEADIN
 015A    E6 7F                ANI     07Fh    ;mask 1st bit
 015C    FE 20        CALJMP: CPI     SPC
 015E    DA 0168              JC      FUNC    ;0-1Fh, func
 0161    FE 7E                CPI     07Eh
 0163    DA 0372              JC      CHAR    ;20-7Dh, char input
 0166    D6 5E                SUI     05Eh    ;7E/7Fh to 20/21h
 0168    2B           FUNC:   DCX     H       ;insert mode
 0169    74                   MOV     M,H     ;h<>0,defeat insert mode
 016A    07           JMPADD: RLC             ;*2, msb=0
 016B    5F                   MOV     E,A     ;d=02h (jmp tbl)
 016C    1A                   LDAX    D       ;fetch jmp addr low
 016D    6F                   MOV     L,A
 016E    13                   INX     D
 016F    1A                   LDAX    D       ;fetch jmp addr high
 0170    C9                   RET

                      ;CALCULATE CUR LOC AND CUR TO END DIFF
 0171    3E 50        DFCLOC: MVI     A,80
 0173    90                   SUB     B       ;cursor to end difference

                      ;CALCULATE CURSOR LOCATION
 0174    2A 3FFA      CURLOC: LHLD    CROW
 0177    2B                   DCX     H
 0178    56                   MOV     D,M
 0179    2B                   DCX     H
 017A    5E                   MOV     E,M
 017B    68                   MOV     L,B
 017C    19                   DAD     D       ;hl=cursor address
 017D    C9                   RET
                      PAGE

 STARPLEX MACRO-ASSEMBLER V2.0          PAGE    7
CRT801
 017E
                      ;ROW WRAP AROUND LOOKUP TABLE   (start addr=17Eh)
                      ;***********************************************
 017E    00E0         RR47D:  dw      00E0h
 0180    0082         RR48D:  dw      0082h
 0182    0084         RR1:    dw      0084h
```

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```
0184    0086          RR2:    dw      0086h
0186    0088          RR3:    dw      0088h
0188    008A          RR4:    dw      008Ah
018A    008C          RR5:    dw      008Ch
018C    008E          RR6:    dw      008Eh
018E    0090          RR7:    dw      0090h
0190    0092          RR8:    dw      0092h
0192    0094          RR9:    dw      0094h
0194    0096          RR10:   dw      0096h
0196    0098          RR11:   dw      0098h
0198    009A          RR12:   dw      009Ah
019A    009C          RR13:   dw      009Ch
019C    009E          RR14:   dw      009Eh
019E    00A0          RR15:   dw      00A0h
01A0    00A2          RR16:   dw      00A2h
01A2    00A4          RR17:   dw      00A4h
01A4    00A6          RR18:   dw      00A6h
01A6    00A8          RR19:   dw      00A8h
01A8    00AA          RR20:   dw      00AAh
01AA    00AC          RR21:   dw      00ACh
01AC    00AE          RR22:   dw      00AEh
01AE    00B0          RR23:   dw      00B0h
01B0    00B2          RR24:   dw      00B2h
01B2    00B4          RR25:   dw      00B4h
01B4    00B6          RR26:   dw      00B6h
01B6    00B8          RR27:   dw      00B8h
01B8    00BA          RR28:   dw      00BAh
01BA    00BC          RR29:   dw      00BCh
01BC    00BE          RR30:   dw      00BEh
01BE    00C0          RR31:   dw      00C0h
01C0    00C2          RR32:   dw      00C2h
01C2    00C4          RR33:   dw      00C4h
01C4    00C6          RR34:   dw      00C6h
01C6    00C8          RR35:   dw      00C8h
01C8    00CA          RR36:   dw      00CAh
01CA    00CC          RR37:   dw      00CCh
01CC    00CE          RR38:   dw      00CEh
01CE    00D0          RR39:   dw      00D0h
01D0    00D2          RR40:   dw      00D2h
01D2    00D4          RR41:   dw      00D4h
01D4    00D6          RR42:   dw      00D6h
01D6    00D8          RR43:   dw      00D8h
01D8    00DA          RR44:   dw      00DAh
01DA    00DC          RR45:   dw      00DCh
01DC    00DE          RR46:   dw      00DEh
01DE    00E0          RR47:   dw      00E0h
01E0    0082          RR48:   dw      0082h
01E2    0084          RR1D:   dw      0084h

 STARPLEX MACRO-ASSEMBLER V2.0          PAGE    8
CRT801
                      ;JUMP ADDRESS CONSTANTS
                      ;*****************************************
                      ;A15    :- 0=no leadin required
                      ;A14/A12:- parameter count
                      ;A11    :- 0=local function
 1000                 W1      equ     01000h  ;one para adder
 2000                 W2      equ     02000h  ;two para adder
 8000                 LIN     equ     08000h  ;leadin adder
 0800                 NLC     equ     00800h  ;not local adder

 0A5F                 F1      equ     RTN+NLC
 03B9                 F2      equ     CARRTN
 03B1                 F3      equ     LFEED
 0C34                 F4      equ     BELL+NLC
 060A                 F5      equ     TAB
 0437                 F6      equ     FS
 041F                 F7      equ     BS

 844E                 F8      equ     UPCUR+LIN
 8460                 F9      equ     DWNCUR+LIN
 84D8                 F10     equ     HOMCUR+LIN
 85F3                 F11     equ     NPAGE+LIN
 8472                 F12     equ     ROLUP+LIN
 848C                 F13     equ     ROLDWN+LIN

 84AE                 F14     equ     CURULK+LIN
 8DD1                 F15     equ     RDCUR+LIN+NLC
 ADA2                 F16     equ     ADDCUR+LIN+NLC+W2

 84F1                 F17     equ     FGNDF+LIN
 84F7                 F18     equ     BGNDF+LIN

 836B                 F19     equ     INSCHAR+LIN
 8358                 F20     equ     STOFCH+LIN
 8505                 F21     equ     INSLNE+LIN
 8512                 F22     equ     STOFLNE+LIN
 AD26                 F23     equ     ISLRG+LIN+NLC+W2
 9E8A                 F24     equ     GRAPH+LIN+NLC+W1
```

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```
0419                    F25     equ     DEL
83DB                    F26     equ     DCROW+LIN
84C0                    F27     equ     DRTLN+LIN
84BA                    F28     equ     DRTPG+LIN
8642                    F29     equ     CFB+LIN
84CE                    F30     equ     CLRSCN+LIN

8CB6                    F31     equ     KBLK+LIN+NLC
801B                    F32     equ     DICUR+LIN
871D                    F33     equ     SNDLNE+LIN
87BF                    F34     equ     ACESW+LIN
0AC5                    F35     equ     LINSET+NLC
86BC                    F36     equ     DEGRPH+LIN
                        PAGE

 STARPLEX MACRO-ASSEMBLER V2.0          PAGE    9
CRT801
 01E4
                        ;PUT A WORD TO ACE
 01E4   57              KBDACE: MOV     D,A
 01E5   3A 9005                 LDA     ACESTU
 01E8   E6 20                   ANI     020h
 01EA   CA 01E5                 JZ      KBDACE+1;not ready
 01ED   C3 0079                 JMP     OUTACE

                        ;ACE BAUD RATE CONSTANTS
 01F0   06AB            B110:   dw      1707    ;       0
 01F2   0139            B600:   dw      313     ;       1
 01F4   009C            B1200:  dw      156     ;0.3%   2
 01F6   004E            B2400:  dw      78      ;0.3%   3
 01F8   0027            B4800:  dw      39      ;0.3%   4
 01FA   0014            B9600:  dw      20      ;2.3%   5
 01FC   000A            B19200: dw      10      ;2.3%   6
 01FE   0005            B38400: dw      5       ;2.3%   7

                        ;FUNCTION JUMP TABLE    (start addr=200h)
                        ;*********************************************
 0200   0A5F            TBLJMP: dw      F1      ;null/toggle local
 0202   8472                    dw      F12     ;A:roll up
 0204   9E8A            CB:     dw      F24     ;B:graphics mode
 0206   84AE                    dw      F14     ;C:on cursor/unlock kbd
 0208   8358                    dw      F20     ;D:strip off character
 020A   8DD1            CE:     dw      F15     ;E:read cursor
 020C   801B                    dw      F32     ;F:disable cursor
 020E   0C34            CG:     dw      F4      ;G:bell/scale
 0210   041F                    dw      F7      ;H:cursor left
 0212   060A                    dw      F5      ;I:tab
 0214   03B1                    dw      F3      ;J:line feed
 0216   8460                    dw      F9      ;K:cursor down
 0218   844E                    dw      F8      ;L:cursor up
 021A   03B9                    dw      F2      ;M:carriage return
 021C   85F3                    dw      F11     ;N:next page
 021E   84C0                    dw      F27     ;O:delete rest of line
 0220   0437                    dw      F6      ;P:cursor right
 0222   ADA2            CQ:     dw      F16     ;Q:address cursor/menu
 0224   84D8                    dw      F10     ;R:home cursor
 0226   8512                    dw      F22     ;S:strip off a line
 0228   871D                    dw      F33     ;T:transmit a line
 022A   8CB6            CU:     dw      F31     ;U:lock keyboard
 022C   848C                    dw      F13     ;V:roll down
 022E   84BA                    dw      F28     ;W:delete rest of page
 0230   8642                    dw      F29     ;X:clear fore/background
 0232   84F7                    dw      F18     ;Y:background follows
 0234   8505                    dw      F21     ;Z:insert line
 0236   86BC                    dw      F36     ;1B:esc/defeat graphics
 0238   84CE                    dw      F30     ;1C:home and clear screen
 023A   AD26            C1D:    dw      F23     ;1D:insert/strip lne/rng
 023C   836B                    dw      F19     ;1E:insert character
 023E   84F1                    dw      F17     ;1F:foreground follows
 0240   0AC5            C7E:    dw      F35     ;7E:leadin/ace,u/l-case
 0242   0419                    dw      F25     ;7F:delete

 STARPLEX MACRO-ASSEMBLER V2.0          PAGE    10
CRT801
                        ;STORE A WORD TO ACE FIFO
 0244   3E 50           STFIFO: MVI     A,80
 0246   BE                     CMP     M       ;exceeding 80 words?
 0247   3A 9000                 LDA     ACEDTA  ;read ace
 024A   DA 032C                 JC      OVRNG   ;more than 80 words
 024D   2E E6                   MVI     L,low FFWRT
 024F   54                      MOV     D,H     ;set up write pointer high
 0250   5E                      MOV     E,M     ;set up write pointer low
 0251   12                     STAX    D       ;store to fifo
 0252   7B                     MOV     A,E
 0253   3C                     INR     A       ;advance pointer
 0254   FE A0                  CPI     low FFEND+1;exceeding 80 words?
 0256   DA 025A                JC      WFFRNG  ;less than 80 words
 0259   1F                     RAR             ;fifo start again
```

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```
025A   77          WFFRNQ: MOV     M,A     ;advance write pointer
025B   FB                  EI

025C   D1          CMRTN:  POP     D
025D   F1                  POP     PSW
025E   E1                  POP     H

                   ;{FUNCTION} unused keys
025F   C9          RTN:    RET


                   ;KEY BOARD RETURN, addr high=2h
0260   AF          KLCRTN: XRA     A       ;enable keyboard
0261   32 3FEE             STA     KBDLCK
0264   C3 025C             JMP     CMRTN

                   ;CHECK FIFO AND RETURN, addr high=2h
0267   21 3FEA     FFCHK:  LXI     H,FFWCT ;fifo word count
026A   35                  DCR     M       ;fifo empty?
026B   FA 025C             JM      CMRTN   ;empty


                   ;READ A WORD FROM ACE FIFO
026E   2E E5       RDFIFO: MVI     L,low FFRD
0270   54                  MOV     D,H     ;set up read pointer high
0271   5E                  MOV     E,M     ;set up read pointer low
0272   7B                  MOV     A,E
0273   3C                  INR     A       ;advance read pointer
0274   FE A0               CPI     low FFEND+1;exceeding 80 words?
0276   DA 027A             JC      RFFRNQ  ;less than 80 words
0279   1F                  RAR             ;fifo start again
027A   77          RFFRNQ: MOV     M,A     ;store read pointer
027B   2E E9               MVI     L,low LEADIN
027D   7E                  MOV     A,M
027E   B7                  ORA     A       ;leadin mode=0?
027F   1A                  LDAX    D       ;read fifo word
0280   CA 004E             JZ      FIFACE  ;not leadin, normal entry
                   PAGE
 STARPLEX MACRO-ASSEMBLER V2.0          PAGE    11
CRT801
0283

                   ;LEADIN MODE
0283   E6 7F       LINMDE: ANI     07Fh    ;mask input
0285   11 0267             LXI     D,FFCHK
0288   D5                  PUSH    D       ;pseudo call
0289   2E A2               MVI     L,low LINWCT
028B   5E                  MOV     E,M     ;leadin word count
028C   1D                  DCR     E       ;word count=0?
028D   F2 02B3             JP      LINPRA  ;parameter entries
0290   FE 20               CPI     SPC     ;control codes?
0292   D2 02C2             JNC     ILELIN  ;not cntl code, error
0295   CD 016A             CALL    JMPADD  ;fetch jmp address
0298   B7                  ORA     A
0299   F2 02C2             JP      ILELIN  ;code requires no leadin
029C   E6 77               ANI     077h    ;word count/jmp addr high
029E   67                  MOV     H,A     ;save
029F   E6 70               ANI     070h    ;mask word count
02A1   CA 02BE             JZ      LINEXE  ;do function

02A4   0F          LINPFN: RRC             ;right justify word count
02A5   0F                  RRC
02A6   0F                  RRC
02A7   0F                  RRC
02A8   32 3FA2             STA     LINWCT  ;store to word count reg
02AB   3E 07               MVI     A,07h
02AD   A4                  ANA     H       ;get jmp addr high
02AE   67                  MOV     H,A
02AF   22 3FA0             SHLD    LINF    ;save function jmp addr
02B2   C9                  RET

02B3   73          LINPRA: MOV     M,E     ;leadin word count-1
02B4   16 00               MVI     D,0     ;d=0,e=word count-1
02B6   23                  INX     H       ;LINP
02B7   19                  DAD     D       ;hl=para pointer
02B8   77                  MOV     M,A     ;store word
02B9   C0                  RNZ             ;word count<>0, next word
02BA   2A 3FA0             LHLD    LINF    ;load leadin jmp address
02BD   AF                  XRA     A

02BE   32 3FE9     LINEXE: STA     LEADIN  ;defeat leadin
02C1   E9                  PCHL            ;do function

02C2   D3 01       ILELIN: OUT     BELPRT  ;illegal code after leadin
02C4   AF                  XRA     A       ;a=0, reset leadin
```

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```
                        ;(FUNCTION) set leadin mode
  02C5  32 3FE9         LINSET: STA     LEADIN  ;a<>0. set leadin
  02C8  C9                      RET


                        PAGE

 STARPLEX MACRO-ASSEMBLER V2.0          PAGE    12
CRTB01
  02C9
                        ;keyboard interrupt continue
  02C9  AF              KBDINT: XRA     A
  02CA  32 3FEB                 STA     CURTMR  ;reset cursor blink timer
  02CD  B6                      ORA     M       ;keyboard locked?
  02CE  DB 80                   IN      KBDPRT  ;read keyboard
  02D0  FB                      EI
  02D1  D5                      PUSH    D
  02D2  C2 0327                 JNZ     KNACTV  ;keyboard not active

  02D5  B7                      ORA     A
  02D6  CA 0333                 JZ      TGLCL   ;toggle local
                                                ;defeat graphics
  02D9  77                      MOV     M,A     ;lock keyboard
  02DA  11 0260                 LXI     D,KLCRTN
  02DD  D5                      PUSH    D       ;generate pseudo call

  02DE  23                      INX     H       ;GECNTL
  02DF  B6                      ORA     M
  02E0  23                      INX     H       ;ULCASE
  02E1  FE 61                   CPI     061h
  02E3  DA 02EC                 JC      NLCSE   ;not lower case
  02E6  FE 7B                   CPI     07Bh
  02E8  D2 02EC                 JNC     NLCSE   ;not lower case
  02EB  96                      SUB     M       ;u/l case cntl,m=20h/0

  02EC  23              NLCSE:  INX     H       ;local
  02ED  5E                      MOV     E,M
  02EE  1C                      INR     E       ;local mode?
  02EF  C2 01E4                 JNZ     KBDACE  ;write to ace

  02F2  FE A0           LCL:    CPI     0A0h    ;parameter entry?
  02F4  D2 068D                 JNC     LGPARA  ;yes

  02F7  CD 0158                 CALL    CJMP    ;get jmp addr
  02FA  E6 0F                   ANI     0Fh
  02FC  FE 08                   CPI     08h     ;local?
  02FE  DA 005F                 JC      LCLFUN  ;do local function
  0301  7B                      MOV     A,E     ;read lookup tbl ptr
  0302  FE 05                   CPI     low CB+1;cntl B?
  0304  CA 06B7                 JZ      ENGRPH  ;enable graphics mode
  0307  FE 0B                   CPI     low CE+1;cntl E?
  0309  CA 0773                 JZ      LRDCUR  ;display cursor location
  030C  FE 0F                   CPI     low CQ+1;cntl Q?
  030E  CA 0784                 JZ      SCALE   ;put scale
  0311  FE 23                   CPI     low CQ+1;cntl Q?
  0313  CA 06D5                 JZ      PGM     ;put graphics menu
  0316  FE 41                   CPI     low C7E+1
  0318  CA 07CD                 JZ      ATGUL   ;init ace,toggle u/l case
  031B  FE 3B                   CPI     low C1D+1
  031D  CA 034F                 JZ      ROM2    ;do rom2 functions
  0320  FE 2B                   CPI     low CU+1;cntl U?
                        PAGE

 STARPLEX MACRO-ASSEMBLER V2.0          PAGE    13
CRTB01
  0322
  0322  C0                      RNZ             ;unused keys
  0323  D1                      POP     D       ;pseudo rtn+lock kbd
  0324  C3 0261                 JMP     KLCRTN+1


  0327  EE 03           KNACTV: XRI     KULCDE  ;lock/unlock kbd?
  0329  CA 025A                 JZ      CMRTN-2 ;unlock keyboard
  032C  3E 50           OVRNG:  MVI     A,80    ;for FFWCT
  032E  D3 01                   OUT     BELPRT
  0330  C3 025A                 JMP     CMRTN-2 ;lock kbd

  0333  23              TGLCL:  INX     H       ;GECNTL
  0334  77                      MOV     M,A     ;disable graphics mode
  0335  32 3FE9                 STA     LEADIN  ;reset leadin
  0338  2E F1                   MVI     L,low LOCLM
  033A  7E                      MOV     A,M
  033B  2F                      CMA             ;toggle local
  033C  77                      MOV     M,A
  033D  CD 07E8                 CALL    EDACE   ;en/disable ace
  0340  C2 0345                 JNZ     ONLINE
  0343  3E 1E                   MVI     A,03h XOR 01Dh
  0345  EE 1D           ONLINE: XRI     01Dh
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```
0347    00                      nop             ;out lclprt
0348    00                      nop
0349    32 3FED                 STA     RTECTL  ;select blink rate
034C    C3 025C                 JMP     CMRTN

                        ;JMP TO ROM2
034F    3A 0800         ROM2:   LDA     0800h   ;check presence of rom2
0352    FE 55                   CPI     055h    ;=55h?
0354    C0                      RNZ             ;not exist
0355    C3 0801                 JMP     0801h   ;ok, do jmp


                        ;(FUNCTION) stripe off a character
0358    CD 0171         STOFCH: CALL    DFCLOC  ;get cur loc and diff
035B    3D                      DCR     A
035C    CA 0434                 JZ      BELL    ;last column, error
035F    23              STOFLP: INX     H
0360    56                      MOV     D,M
0361    2B                      DCX     H
0362    72                      MOV     M,D     ;do copy
0363    23                      INX     H
0364    3D                      DCR     A
0365    C2 035F                 JNZ     STOFLP
0368    C3 03A4                 JMP     PSPC    ;put a space

                        ;(FUNCTION) insert character
036B    AF              INSCHAR:XRA     A
036C    32 3FE8                 STA     ICMD    ;enable insert mode
036F    C3 038D                 JMP     INSCHR
                        PAGE

 STARPLEX MACRO-ASSEMBLER V2.0          PAGE    14
CRT801
  0372
                        ;CHARACTER INPUT
0372    D1              CHAR:   POP     D       ;pseudo return
0373    2E 20                   MVI     L,low FBQ
0375    AE                      XRA     M       ;add attribute
0376    AD                      XRA     L       ;remove space code

0377    2A 3FFA                 LHLD    CROW    ;calculate cursor loc
037A    2B                      DCX     H
037B    56                      MOV     D,M
037C    2B                      DCX     H
037D    5E                      MOV     E,M
037E    68                      MOV     L,B     ;row start+cursor
037F    19                      DAD     D       ;hl=cursor address
0380    77                      MOV     M,A     ;write to screen

0381    3E 4F                   MVI     A,79
0383    A8                      XRA     B       ;last column?
0384    CA 03C0                 JZ      LSTCHR  ;last, do scroll
0387    04              MIDCHR: INR     B       ;else advance cursor
0388    3A 3FE8                 LDA     ICMD    ;insert mode?
038B    B7                      ORA     A
038C    C0                      RNZ             ;not insert mode

038D    3E 4F           INSCHR: MVI     A,79
038F    90                      SUB     B       ;byte counter
0390    CA 03AB                 JZ      ILCHAR  ;cursor at last column

0393    2A 3FFA                 LHLD    CROW
0396    5E                      MOV     E,M
0397    23                      INX     H
0398    56                      MOV     D,M     ;d=row end+1
0399    1B                      DCX     D       ;row end
039A    EB                      XCHG
039B    2B              INSLP:  DCX     H
039C    56                      MOV     D,M
039D    23                      INX     H
039E    72                      MOV     M,D     ;do copy
039F    2B                      DCX     H
03A0    3D                      DCR     A
03A1    C2 039B                 JNZ     INSLP

03A4    3E 80           PSPC:   MVI     A,080h
03A6    A2                      ANA     D       ;get character attribute
03A7    F6 20                   ORI     SPC     ;add space
03A9    77                      MOV     M,A
03AA    C9                      RET

03AB    3C              ILCHAR: INR     A       ;make a<>0
03AC    D3 01                   OUT     BELPRT
03AE    C3 03CE                 JMP     DICMD   ;defeat insert char mode
                        PAGE
```

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```
 STARPLEX MACRO-ASSEMBLER V2.0          PAGE    15
CRT801
  03B1
                        ;{FUNCTION} line feed
  03B1    3A 3FF2       LFEED:  LDA     AULF    ;auto line feed?
  03B4    B7                    ORA     A
  03B5    C2 03C1               JNZ     LFD     ;do line feed
  03B8    C9                    RET

                        ;{FUNCTION} carriage return
  03B9    3A 3FF2       CARRTN: LDA     AULF    ;auto line feed?
  03BC    B7                    ORA     A
  03BD    C2 04DE               JNZ     ZROCUR  ;do cr only


  03C0    47            LSTCHR: MOV     B,A     ;set cursor to 1st col

  03C1    11 3FFC       LFD:    LXI     D,LROW
  03C4    2A 3FFA               LHLD    CROW
  03C7    24                    INR     H
  03C8    1A                    LDAX    D
  03C9    BD                    CMP     L       ;crow=lrow?
  03CA    7E                    MOV     A,M     ;next row
  03CB    32 3FFA               STA     CROW    ;crow+1
  03CE    32 3FE8       DICMD:  STA     ICMD    ;defeat insert char mode
  03D1    C0                    RNZ             ;not last row

  03D2    EB            LFSCR:  XCHG            ;last row, do scroll
  03D3    F3                    DI
  03D4    77                    MOV     M,A     ;lrow+1
  03D5    2E FE                 MVI     L,low FROW
  03D7    5E                    MOV     E,M     ;de=row wrap arround tbl
  03D8    1A                    LDAX    D
  03D9    77                    MOV     M,A     ;frow+1
  03DA    FB                    EI


                        ;{FUNCTION} clear cursor row
  03DB    2A 3FFA       DCROW:  LHLD    CROW

  03DE    EB            CLRROW: XCHG
  03DF    21 0000               LXI     H,0
  03E2    39                    DAD     SP
  03E3    EB                    XCHG
  03E4    F3                    DI
  03E5    F9                    SPHL
  03E6    E1                    POP     H       ;lookup row start
  03E7    F9                    SPHL            ;sp=row start
  03E8    FB                    EI
  03E9    2A 3F20               LHLD    FBG     ;space + attribute
                        PAGE
 STARPLEX MACRO-ASSEMBLER V2.0          PAGE    16
CRT801
  03EC
  03EC    E5            PUSHSP: PUSH    H       ;do clear row
  03ED    E5                    PUSH    H
  03EE    E5                    PUSH    H
  03EF    E5                    PUSH    H
  03F0    E5                    PUSH    H
  03F1    E5                    PUSH    H
  03F2    E5                    PUSH    H
  03F3    E5                    PUSH    H
  03F4    E5                    PUSH    H
  03F5    E5                    PUSH    H       ;10
  03F6    E5                    PUSH    H
  03F7    E5                    PUSH    H
  03F8    E5                    PUSH    H
  03F9    E5                    PUSH    H
  03FA    E5                    PUSH    H
  03FB    E5                    PUSH    H
  03FC    E5                    PUSH    H
  03FD    E5                    PUSH    H
  03FE    E5                    PUSH    H
  03FF    E5                    PUSH    H       ;20
  0400    E5                    PUSH    H
  0401    E5                    PUSH    H
  0402    E5                    PUSH    H
  0403    E5                    PUSH    H
  0404    E5                    PUSH    H
  0405    E5                    PUSH    H
  0406    E5                    PUSH    H
  0407    E5                    PUSH    H
  0408    E5                    PUSH    H
  0409    E5                    PUSH    H       ;30
  040A    E5                    PUSH    H
  040B    E5                    PUSH    H
  040C    F3                    DI
```

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```
 040D    E5                     PUSH    H
 040E    E5                     PUSH    H
 040F    E5                     PUSH    H
 0410    E5                     PUSH    H
 0411    E5                     PUSH    H
 0412    E5                     PUSH    H
 0413    E5                     PUSH    H
 0414    E5                     PUSH    H       ;40
 0415    EB                     XCHG
 0416    F9                     SPHL
 0417    FB             BSRTN:  EI
 0418    C9                     RET


                        ;{FUNCTION} delete
 0419    3E 20          DEL:    MVI     A,SPC
 041B    CD 06CB                CALL    STSP    ;store space
 041E    AF                     XRA     A       ;do back space
                        PAGE

 STARPLEX MACRO-ASSEMBLER V2.0          PAGE    17
CRT801
 041F
                        ;{FUNCTION} back space
 041F    C4 06C1        BS:     CNZ     CHKGM   ;check graphics mode
 0422    F3             BS1:    DI
 0423    05                     DCR     B       ;cursor-1
 0424    F2 0417                JP      BSRTN   ;not 1st column
 0427    04                     INR     B
 0428    FB                     EI
 0429    3A 3FEF                LDA     GECNTL
 042C    B7                     ORA     A       ;graphics mode?
 042D    C0                     RNZ             ;defeat wrap arround
 042E    CD 0451                CALL    UCUR1   ;up cursor one row
 0431    C8                     RZ              ;crow=frow?
 0432    06 4F                  MVI     B,79    ;set cursor to last col
 0434    D3 01          BELL:   OUT     BELPRT
 0436    C9                     RET

                        ;{FUNCTION} forward cursor
 0437    CD 06C1        FS:     CALL    CHKGM   ;check graphics mode
 043A    3E 4F                  MVI     A,79
 043C    B8                     CMP     B       ;last column?
 043D    C2 03B7                JNZ     MIDCHR  ;not last column
 0440    3A 3FEF                LDA     GECNTL
 0443    B7                     ORA     A       ;graphics mode?
 0444    C0                     RNZ             ;defeat wrap arround
 0445    CD 0463                CALL    DCUR1   ;down cursor one row
 0448    C8                     RZ              ;crow=lrow?
 0449    06 00                  MVI     B,0     ;set cursor to 1st col
 044B    D3 01                  OUT     BELPRT
 044D    C9                     RET

                        ;{FUNCTION} up cursor one row
 044E    CD 06C1        UPCUR:  CALL    CHKGM   ;check graphics mode
 0451    11 3FFA        UCUR1:  LXI     D,CROW
 0454    2A 3FFE                LHLD    FROW
 0457    1A                     LDAX    D       ;crow
 0458    24                     INR     H       ;hl=row wrap arround tbl
 0459    BD                     CMP     L       ;crow=frow?
 045A    C2 04A7                JNZ     $4
 045D    D3 01                  OUT     BELPRT  ;crow=frow, ring bell
 045F    C9                     RET

                        ;{FUNCTION} down cursor one row
 0460    CD 06C1        DWNCUR: CALL    CHKGM   ;check graphics mode
 0463    11 3FFA        DCUR1:  LXI     D,CROW
 0466    2A 3FFC                LHLD    LROW
 0469    1A                     LDAX    D       ;crow
 046A    24                     INR     H       ;hl=row wrap arroud tbl
 046B    BD                     CMP     L       ;crow=lrow?
 046C    C2 04A9                JNZ     $5
 046F    D3 01                  OUT     BELPRT  ;crow=lrow, ring bell
 0471    C9                     RET
                        PAGE

 STARPLEX MACRO-ASSEMBLER V2.0          PAGE    18
CRT801
 0472
                        ;{FUNCTION} roll up
 0472    11 3FFA        ROLUP:  LXI     D,CROW
 0475    2A 3FFE                LHLD    FROW
 0478    1A                     LDAX    D
 0479    24                     INR     H       ;hl=row wrap arround tbl
 047A    BD                     CMP     L       ;crow=frow?
 047B    7E                     MOV     A,M     ;next row
 047C    F3                     DI
 047D    32 3FFE                STA     FROW    ;frow+1
 0480    C2 0484                JNZ     RUNEQ
```

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```
0483    12                      STAX    D       ;crow+1
0484    EB              RUNEQ:  XCHG            ;d=1,h=3Fh
0485    2E FC                   MVI     L,low LROW
0487    5E                      MOV     E,M     ;de=row wrap arround tbl
0488    1A                      LDAX    D       ;next row
0489    77                      MOV     M,A     ;lrow+1
048A    FB                      EI
048B    C9                      RET

                        ;{FUNCTION} roll down
048C    11 3FFA         ROLDWN: LXI     D,CROW
048F    3A 3FFC                 LDA     LROW
0492    D6 04                   SUI     4       ;up one row
0494    6F                      MOV     L,A
0495    26 01                   MVI     H,1     ;hl=row wrap arround tbl
0497    1A                      LDAX    D       ;crow
0498    D6 04                   SUI     4
049A    BD                      CMP     L       ;crow=lrow?
049B    7E                      MOV     A,M     ;up one row
049C    F3                      DI
049D    32 3FFC                 STA     LROW    ;lrow-1
04A0    C2 04A4                 JNZ     RDNEQ
04A3    12                      STAX    D       ;crow-1
04A4    1E FE           RDNEQ:  MVI     E,low FROW
04A6    1A                      LDAX    D
04A7    D6 04           $4:     SUI     4
04A9    6F              $5:     MOV     L,A     ;hl=row wrap arround tbl
04AA    7E                      MOV     A,M
04AB    12                      STAX    D       ;frow-1
04AC    FB                      EI
04AD    C9                      RET

                        ;{FUNCTION} enable cursor, unlock keyboard
04AE    AF              CURULK: XRA     A
04AF    32 3FEE                 STA     KBDLCK  ;unlock keyboard
04B2    2F                      CMA             ;enable cursor
04B3    C3 001B                 JMP     DICUR

                        ;{FUNCTION} lock keyboard
04B6    32 3FEE         KBLK:   STA     KBDLCK  ;lock keyboard
04B9    C9                      RET
                        PAGE
 STARPLEX MACRO-ASSEMBLER V2.0          PAGE    19
CRTB01
 04BA
                        ;{FUNCTION} delete rest of page
04BA    3A 3FFA         DRTPG:  LDA     CROW
04BD    CD 04E9                 CALL    CTLRW2  ;clear crow+1 to lrow

                        ;{FUNCTION} delete rest of line
04C0    CD 0171         DRTLN:  CALL    DFCLOC  ;get cursor loc and diff
04C3    57                      MOV     D,A     ;save
04C4    3A 3F20                 LDA     FBG
04C7    77              DRLLP:  MOV     M,A     ;store space/attribute
04C8    23                      INX     H
04C9    15                      DCR     D
04CA    C2 04C7                 JNZ     DRLLP   ;until end of line
04CD    C9                      RET

                        ;{FUNCTION} clear screen
04CE    CD 06BC         CLRSCN: CALL    DEGRPH  ;defeat graphics mode
04D1    2A 3FFE                 LHLD    FROW
04D4    7D                      MOV     A,L
04D5    CD 04E6                 CALL    CTLRW1  ;clear frow to lrow

                        ;{FUNCTION} home cursor
04D8    3A 3FFE         HOMCUR: LDA     FROW
04DB    32 3FFA                 STA     CROW    ;crow=frow
04DE    06 00           ZROCUR: MVI     B,0     ;set cursor to 1st col
04E0    C9                      RET

                        ;CLEAR TO LAST ROW
04E1    16 01           CLRWLP: MVI     D,1
04E3    5F                      MOV     E,A     ;de=row wrap arround tbl
04E4    1A                      LDAX    D       ;next row
04E5    6F                      MOV     L,A
04E6    CD 03DE         CTLRW1: CALL    CLRROW  ;clear whole row
04E9    2A 3FFC         CTLRW2: LHLD    LROW
04EC    BD                      CMP     L       ;row=lrow?
04ED    C2 04E1                 JNZ     CLRWLP  ;until last row
04F0    C9                      RET


                        ;{FUNCTION} foreground follows
04F1    11 2020         FGNDF:  LXI     D,02020h;foreground spaces
04F4    C3 04FA                 JMP     LDFGD
```

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```
                        ;{FUNCTION} background follows
 04F7   11 A0A0     BGNDF:  LXI     D,0A0A0h;background spaces
 04FA   21 0000     LDFGD:  LXI     H,0
 04FD   39                  DAD     SP
 04FE   EB                  XCHG
 04FF   31 3F50             LXI     SP,DMYROW+80
 0502   C3 03EC             JMP     PUSHSP  ;store in dummy row
                    PAGE

 STARPLEX MACRO-ASSEMBLER V2.0          PAGE    20
CRT801
  0505
                        ;{FUNCTION} insert a line
 0505   CD 0590     INSLNE: CALL    CRLR    ;calc crow/lrow diff
 0508   21 3FFA             LXI     H,CROW
 050B   73                  MOV     M,E     ;set crow=lrow
 050C   C2 054B             JNZ     MOVDWN  ;move row contents
 050F   C3 058C             JMP     DRWZCU  ;else, del lrow/zero cur

                        ;{FUNCTION} strip off a line
 0512   CD 0590     STOFLNE:CALL    CRLR    ;get crow/lrow diff
 0515   CA 058C             JZ      DRWZCU  ;del lrow/zero cursor
 0518   E5           SLNERG: PUSH    H       ;else do move
 0519   21 3FE7             LXI     H,CPYCTL
 051C   36 00               MVI     M,0     ;copy upward
 051E   CD 0550             CALL    MOVROW  ;move row contents
 0521   E1                  POP     H       ;get original crow
 0522   22 3FFA             SHLD    CROW    ;back to crow
 0525   C9                  RET

                        ;{FUNCTION} insert/strip off line with range
 0526   2A 3FFA     ISLRG:  LHLD    CROW
 0529   3A 3FA3             LDA     LINP    ;read 2nd parameter
 052C   3D                  DCR     A
 052D   E6 3F               ANI     03Fh    ;40/7Fh offset to 0/3Fh
 052F   FE 38               CPI     038h
 0531   D0                  RNC             ;error
 0532   FE 17               CPI     017h
 0534   DA 053C             JC      ISNPA
 0537   FE 20               CPI     020h
 0539   D8                  RC              ;error
 053A   D6 09               SUI     9
 053C   3C           ISNPA:  INR     A
 053D   57                  MOV     D,A
 053E   3A 3FA4             LDA     LINP+1  ;read 1st parameter
 0541   FE 53               CPI     "S"     ;strip off?
 0543   7A                  MOV     A,D
 0544   CA 0518             JZ      SLNERG  ;do strip off line
 0547   CD 05C1     ILNERG: CALL    IRWOS   ;offset row by para
 054A   7A                  MOV     A,D     ;return para
 054B   21 3FE7     MOVDWN: LXI     H,CPYCTL
 054E   36 04               MVI     M,4     ;copy downward

                        ;MOVE ROW CONTENTS,UP/DOWN CNTL BY CPYCTL
 0550   F5           MOVROW: PUSH    PSW     ;save row count
 0551   2A 3FFA             LHLD    CROW
 0554   5E                  MOV     E,M
 0555   23                  INX     H
 0556   56                  MOV     D,M
 0557   1B                  DCX     D       ;crow end
 0558   D5                  PUSH    D       ;save
 0559   21 3FE7             LXI     H,CPYCTL;direction control
 055C   11 3FFA             LXI     D,CROW
 055F   1A                  LDAX    D       ;read crow
 0560   96                  SUB     M       ;direction cntl
                    PAGE

 STARPLEX MACRO-ASSEMBLER V2.0          PAGE    21
CRT801
  0561
 0561   6F                  MOV     L,A
 0562   26 01               MVI     H,1     ;hl=row wrap arround tbl
 0564   7E                  MOV     A,M     ;lookup +/- one row
 0565   12                  STAX    D       ;update crow
 0566   6F                  MOV     L,A
 0567   25                  DCR     H       ;hl=row start table
 0568   5E                  MOV     E,M
 0569   23                  INX     H
 056A   56                  MOV     D,M
 056B   1B                  DCX     D       ;+/- row end
 056C   E1                  POP     H       ;rtn current row last loc
 056D   06 10               MVI     B,80/5  ;copy 80 characters
 056F   1A           CPLP:   LDAX    D       ;read
 0570   77                  MOV     M,A     ;copy
 0571   2B                  DCX     H       ;next byte
 0572   1B                  DCX     D       ;next byte
 0573   1A                  LDAX    D       ;do 5 times for speed
 0574   77                  MOV     M,A
```

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```
0575  2B                        DCX     H
0576  1B                        DCX     D
0577  1A                        LDAX    D       ;3
0578  77                        MOV     M,A
0579  2B                        DCX     H
057A  1B                        DCX     D
057B  1A                        LDAX    D       ;4
057C  77                        MOV     M,A
057D  2B                        DCX     H
057E  1B                        DCX     D
057F  1A                        LDAX    D       ;5
0580  77                        MOV     M,A
0581  2B                        DCX     H
0582  1B                        DCX     D
0583  05                        DCR     B
0584  C2 056F                   JNZ     CPLP    ;finish 80 bytes?
0587  F1                        POP     PSW     ;row count
0588  3D                        DCR     A
0589  C2 0550                   JNZ     MOVROW  ;next row
058C  47              DRWZCU:   MOV     B,A     ;zero cursor
058D  C3 03DB                   JMP     DCROW   ;and delete cursor row

                      ;CALCULATE ROW DIFFERENCE
0590  2A 3FFA         CRLR:     LHLD    CROW    ;calc crow to lrow
0593  3A 3FFC                   LDA     LROW
0596  5F              FRCR:     MOV     E,A
0597  95                        SUB     L       ;get the difference
0598  D2 05A0                   JNC     $2      ;within range
059B  3E 60           $D2:      MVI     A,RWRG  ;over range
059D  83                        ADD     E
059E  95                        SUB     L
059F  B7                        ORA     A       ;clear carry
05A0  1F              $2:       RAR             ;row diff /2
05A1  C9                        RET
                      PAGE

 STARPLEX MACRO-ASSEMBLER V2.0          PAGE    22
CRT801
 05A2
                      ;{FUNCTION} address cursor
05A2  2A 3FA3         ADDCUR:   LHLD    LINP    ;read leadin parameter
05A5  7C                        MOV     A,H

05A6  11 5010         CALCX:    LXI     D,05010h;calc x coordinate
05A9  BA                        CMP     D
05AA  DA 05B3                   JC      CX4FD   ;00/4Fh=loc 0/79
05AD  92                        SUB     D       ;50/7Fh offset to 0/2F
05AE  BB                        CMP     E
05AF  DA 05B3                   JC      CX4FD   ;50/5Fh offset to 0/15
05B2  93                        SUB     E       ;60/7Fh offset to 0/31
05B3  47              CX4FD:    MOV     B,A     ;then set cursor

05B4  3E 1F           CALCY:    MVI     A,01Fh
05B6  A5                        ANA     L       ;0/1F,20/3F,40/5F,60/7Fh
05B7  FE 18                     CPI     018h    ;offset to 00/1Fh
05B9  DA 05BE                   JC      CY17D   ;00/17h=row 0/23
05BC  D6 18                     SUI     018h    ;18/1Fh=row 0/7
05BE  2A 3FFE         CY17D:    LHLD    FROW    ;offset first row

05C1  07              IRWOS:    RLC             ;diff*2,msb=0
05C2  85                        ADD     L       ;frow+offset
05C3  DA 05CB                   JC      ROSFFU  ;>FFh
05C6  FE E1                     CPI     low RR48+1
05C8  DA 05CD                   JC      ROSEOD  ;less than E0h,ok
05CB  D6 60           ROSFFU:   SUI     RWRG    ;row range
05CD  32 3FFA         ROSEOD:   STA     CROW    ;then update crow
05D0  C9                        RET


                      ;{FUNCTION} read cursor
05D1  CD 05E0         RDCUR:    CALL    RDX     ;read cursor x coord
05D4  CD 006D                   CALL    WTACEA  ;write to ace

05D7  CD 05E7                   CALL    RDY     ;read cursor y coord
05DA  CD 006D                   CALL    WTACEA  ;write to ace

05DD  C3 074A                   JMP     CRACE   ;cr for termination

05E0  78              RDX:      MOV     A,B
05E1  FE 20                     CPI     020h    ;if 0/1Fh add offset
05E3  D0                        RNC             ;20/4Fh=cursor loc 32/79
05E4  C6 60                     ADI     060h    ;60/7Fh=cursor loc 0/31
05E6  C9                        RET
```

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```
05E7    2A 3FFE       RDY:    LHLD    FROW
05EA    3A 3FFA               LDA     CROW
05ED    CD 0596               CALL    FRCR    ;calc frow/crow diff
05F0    C6 60                 ADI     060h    ;60/77h=row 0/23
05F2    C9                    RET
                      PAGE

 STARPLEX MACRO-ASSEMBLER V2.0          PAGE    23
CRT801
  05F3
                      ;{FUNCTION} next page
05F3    16 30         NPAGE:  MVI     D,030h  ;page offset
05F5    21 3FFA               LXI     H,CROW
05F8    F3                    DI
05F9    7E            NPLP:   MOV     A,M
05FA    FE B1                 CPI     0B1h
05FC    DA 0601               JC      NPLT    ;a< B1,B2-B0h
05FF    92                    SUB     D       ;a>=B1,B2-E0h
0600    92                    SUB     D
0601    82            NPLT:   ADD     D
0602    77                    MOV     M,A
0603    2C                    INR     L       ;do crow/lrow/frow
0604    2C                    INR     L
0605    FA 05F9               JM      NPLP    ;if pass frow, end
0608    FB                    EI
0609    C9                    RET

                      ;{FUNCTION} tab
060A    2A 3FFA       TAB:    LHLD    CROW
060D    E5                    PUSH    H       ;save crow
060E    CD 0667               CALL    SCATT

0611    13            TDAOSP: INX     D       ;next character
0612    2D                    DCR     L       ;end of row?
0613    CC 067A               CZ      DRCFL   ;down one row, get 1st loc
0616    1A                    LDAX    D       ;read character
0617    84                    ADD     H       ;check attribute
0618    FA 0635               JM      TSATT   ;diff, find same attrib
061B    FE 20                 CPI     SPC     ;space?
061D    C2 0611               JNZ     TDAOSP  ;loop until space
0620    13            TSANSP: INX     D       ;next character
0621    2D                    DCR     L       ;end of row?
0622    CC 067A               CZ      DRCFL   ;down one row, get 1st loc
0625    1A                    LDAX    D       ;read character
0626    84                    ADD     H       ;check attribute
0627    FA 0635               JM      TSATT   ;diff, find same attrib
062A    FE 20                 CPI     SPC     ;non space?
062C    CA 0620               JZ      TSANSP  ;loop until non space
062F    D1            TMCUR:  POP     D       ;remove saved crow
0630    3E 50                 MVI     A,80
0632    95                    SUB     L       ;calc cursor location
0633    47                    MOV     B,A     ;move cursor
0634    C9                    RET
0635    13            TSATT:  INX     D       ;next character
0636    2D                    DCR     L       ;end of row?
0637    CC 067A               CZ      DRCFL   ;down one row,get 1st loc
063A    1A                    LDAX    D       ;read character
063B    84                    ADD     H       ;check attribute
063C    FA 0635               JM      TSATT   ;loop until same attrib
063F    C3 062F               JMP     TMCUR   ;move cursor
                      PAGE

 STARPLEX MACRO-ASSEMBLER V2.0          PAGE    24
CRT801
  0642
                      ;{FUNCTION} clear fore/background to space
0642    2A 3FFA       CFB:    LHLD    CROW
0645    24                    INR     H
0646    E5                    PUSH    H       ;save
0647    CD 0667               CALL    SCATT
064A    1A            CFBLP:  LDAX    D       ;read character
064B    84                    ADD     H       ;test attribute
064C    FA 0653               JM      CFBDIF  ;diff attrib
064F    3E 20                 MVI     A,SPC   ;if same attrib,
0651    B4                    ORA     H       ;put a space
0652    12                    STAX    D
0653    13            CFBDIF: INX     D       ;next character
0654    2D                    DCR     L       ;character counter-1
0655    C2 064A               JNZ     CFBLP   ;until finish 80 char
0658    E1                    POP     H       ;saved crow
0659    3A 3FFC               LDA     LROW
065C    BD                    CMP     L       ;row=lrow?
065D    C8                    RZ              ;no more
065E    6E                    MOV     L,M     ;else next row
065F    E5                    PUSH    H       ;save
0660    CD 0681               CALL    $3
0663    C3 064A               JMP     CFBLP
0666    C9                    RET
```

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```
                        ;SET UP CHAR COUNTER AND ATTRIB
 0667    CD 0174        SCATT:  CALL    CURLOC  ;get cursor location
 066A    EB                     XCHG            ;put in de
 066B    21 8050                LXI     H,08050h;mask/char count
 066E    3A 3F20                LDA     FBQ
 0671    A4                     ANA     H
 0672    67                     MOV     H,A
 0673    22 3FA5                SHLD    LINP+2  ;save count,attrib
 0676    7D                     MOV     A,L
 0677    90                     SUB     B       ;get cur to end diff
 0678    6F                     MOV     L,A     ;put in l
 0679    C9                     RET

                        ;DOWN ONE ROW AND GET ADDR ON 1ST COLUMN
 067A    CD 0463        DRCFL:  CALL    DCUR1   ;down cursor one row
 067D    CA 0033                JZ      TABSTP  ;crow=lrow, no tab
 0680    6E                     MOV     L,M     ;next row
 0681    25             $3:     DCR     H
 0682    2B             $1:     DCX     H
 0683    56                     MOV     D,M     ;addr high
 0684    2B                     DCX     H
 0685    5E                     MOV     E,M     ;addr low
 0686    2A 3FA5                LHLD    LINP+2  ;count and attrib
 0689    C9                     RET
                        PAGE

 STARPLEX MACRO-ASSEMBLER V2.0          PAGE    25
CRT801
 068A
                        ;{FUNCTION} graphics
 068A    3A 3FA3        GRAPH:  LDA     LINP    ;read leadin parameter
 068D    21 107E        LGPARA: LXI     H,0107Eh
 0690    3D                     DCR     A
 0691    E6 3F                  ANI     03Fh
 0693    BC                     CMP     H       ;h=010h
 0694    DA 06AD                JC      $Q1     ;"A" to "P"
 0697    FE 3E                  CPI     03Eh    ;delete
 0699    CA 06B2                JZ      $Q3
 069C    94                     SUB     H       ;h=010h
 069D    FE 0F                  CPI     0Fh     ;space?
 069F    CA 06B2                JZ      $Q3     ;space
 06A2    BC                     CMP     H       ;h=010h
 06A3    DA 06AC                JC      $Q2     ;> "Q"
 06A6    FE 20                  CPI     020h
 06A8    DA 06AD                JC      $Q1     ;"a" to "p"
 06AB    2C                     INR     L       ;set l to 7Fh
 06AC    7D             $Q2:    MOV     A,L     ;L=7Eh or 7Fh
 06AD    CD 06D0        $Q1:    CALL    STSCN   ;put symbol to screen
 06B0    C6 1E                  ADI     01Eh
 06B2    D6 1E          $Q3:    SUI     01Eh
 06B4    32 3FF3                STA     QSYMBL  ;for non/destructive move

 06B7    3E 80          ENGRPH: MVI     A,080h
 06B9    C3 06BD                JMP     DEGRPH+1

                        ;{FUNCTION} defeat graphics
 06BC    AF             DEGRPH: XRA     A
 06BD    32 3FEF                STA     GECNTL
 06C0    C9                     RET



                        ;CHECK GRAPHICS MODE AND PUT SYMBOL TO SCREEN
 06C1    3A 3FEF        CHKGM:  LDA     GECNTL
 06C4    B7                     ORA     A       ;graphics mode?
 06C5    C8                     RZ              ;no, rtn to func
 06C6    3A 3FF3                LDA     QSYMBL
 06C9    B7                     ORA     A       ;non destructive move?
 06CA    F8                     RM              ;yes
 06CB    21 3F20        STSP:   LXI     H,FBQ
 06CE    AE                     XRA     M       ;get attribute
 06CF    AD                     XRA     L       ;remove space code
 06D0    CD 0174        STSCN:  CALL    CURLOC
 06D3    77                     MOV     M,A     ;write to screen
 06D4    C9                     RET
                        PAGE

 STARPLEX MACRO-ASSEMBLER V2.0          PAGE    26
CRT801
 06D5
                        ;PUT GRAPHIC MENU TO SCREEN (LOCAL)
 06D5    CD 070C        PGM:    CALL    RUADD

 06D8    CD 06F3                CALL    P38SYM  ;print ascii A/Q
 06DB    CD 06F3                CALL    P38SYM  ;print ascii a/q
```

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```
06DE    CD 070C             CALL    RUADD

06E1    CD 0700             CALL    P32SYM  ;print ascii 0h/Fh
06E4    F6 7E               ORI     07Eh    ;print ascii 7Eh
06E6    CD 06F7             CALL    P6SYM   ;4 spaces
06E9    EE 30               XRI     030h    ;print ascii 10/1Fh
06EB    CD 0700             CALL    P32SYM
06EE    F6 7F               ORI     07Fh    ;print ascii 7Fh
06F0    C3 06F7             JMP     P6SYM   ;4 spaces

06F3    F6 41       P38SYM: ORI     041h    ;change symbol
06F5    16 10               MVI     D,16    ;counter
06F7    14          P6SYM:  INR     D
06F8    CD 0702             CALL    PGMLP
06FB    16 04       P4SP:   MVI     D,4
06FD    C3 04C4             JMP     DRLLP-3 ;put 4 spaces

0700    16 10       P32SYM: MVI     D,16    ;print 32 symbols

0702    77          PGMLP:  MOV     M,A
0703    23                  INX     H
0704    73                  MOV     M,E     ;FBG
0705    23                  INX     H
0706    3C                  INR     A       ;next symbol
0707    15                  DCR     D
0708    C2 0702             JNZ     PGMLP
070B    C9                  RET


070C    CD 0472     RUADD:  CALL    ROLUP   ;up one row
070F    26 00               MVI     H,0
0711    6F                  MOV     L,A     ;hl=lrow
0712    CD 0682             CALL    $1      ;lrow 1st loc
0715    EB                  XCHG
0716    CD 06FB             CALL    P4SP    ;put 4 spaces
0719    5F                  MOV     E,A     ;FBG
071A    E6 80               ANI     080h    ;get attribute
071C    C9                  RET
                    PAGE

 STARPLEX MACRO-ASSEMBLER V2.0          PAGE    27
CRTB01
  071D

                    ;{FUNCTION} transmit a line
071D    06 00       SNDLNE: MVI     B,0     ;set cursor to 1st loc
071F    CD 0174             CALL    CURLOC  ;get row start
0722    E5                  PUSH    H       ;save row start
0723    11 004F             LXI     D,79    ;find row end
0726    19                  DAD     D       ;hl=row end, clear carry
0727    16 40               MVI     D,040h  ;rotated space
0729    7E          LENDLP: MOV     A,M     ;read char
072A    17                  RAL             ;mask out msb
072B    AA                  XRA     D       ;space? , clear carry
072C    C2 0734             JNZ     LNSP    ;until find a non-space
072F    2B                  DCX     H
0730    1D                  DCR     E
0731    C2 0729             JNZ     LENDLP  ;repeat loop
0734    E1          LNSP:   POP     H       ;hl=row start again
0735    56          SNDLP:  MOV     D,M     ;read character
0736    3E 60               MVI     A,060h  ;screen all cntl codes
0738    A2                  ANA     D
0739    C2 073E             JNZ     SNCNTL  ;not control code
073C    16 2A               MVI     D,"*"   ;cntl code,send "*" instead
073E    CD 006E     SNCNTL: CALL    WTACED  ;write to ace
0741    7E                  MOV     A,M     ;read char again
0742    EE 80               XRI     080h    ;invert attribute
0744    77                  MOV     M,A     ;store back
0745    23                  INX     H       ;next character
0746    1D                  DCR     E
0747    F2 0735             JP      SNDLP   ;until end of line

074A    CD 006B     CRACE:  CALL    SNDCR   ;send cr for termination
074D    3A 3FF1             LDA     LOCLM
0750    B7                  ORA     A       ;local?
0751    C8                  RZ              ;remote,no time delay

0752    CD 075E     $D3:    CALL    $DLY    ;do delay
0755    15                  DCR     D       ;d was 0Dh
0756    C2 0752             JNZ     $D3
0759    D3 01               OUT     BELPRT  ;delay done,ring bell
075B    C3 0463             JMP     DCUR1   ;move cursor to next row
075E    E5          $DLY:   PUSH    H
075F    D5                  PUSH    D
```

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```
0760    CD 07F0             CALL    LUBD    ;lookup baud constant
0763    3E 1F               MVI     A,01Fh  ;chg delay at high bauds
0765    B3                  ORA     E
0766    5F                  MOV     E,A
0767    CD 059B     $D1:    CALL    $D2
076A    1B                  DCX     D
076B    15                  DCR     D
076C    14                  INR     D
076D    F2 0767             JP      $D1
0770    D1                  POP     D
0771    E1                  POP     H
0772    C9                  RET
                    PAGE

 STARPLEX MACRO-ASSEMBLER V2.0          PAGE    28
CRT801
 0773
                    ;DISPLAY CURSOR LOCATION (LOCAL)
0773    CD 05E7     LRDCUR: CALL    RDY     ;y coordinate
0776    2A 3FFC             LHLD    LROW    ;get print out loc
0779    5E                  MOV     E,M
077A    23                  INX     H
077B    56                  MOV     D,M
077C    1B                  DCX     D       ;lrow last location
077D    12                  STAX    D       ;put to screen
077E    CD 05E0             CALL    RDX     ;x coordinate
0781    1B                  DCX     D
0782    12                  STAX    D       ;put to screen
0783    C9                  RET

                    ;SCALE (LOCAL)
0784    21 3FFE     SCALE:  LXI     H,FROW
0787    3A 3FFA             LDA     CROW
078A    BE                  CMP     M       ;frow=crow
078B    CC 048C             CZ      ROLDWN  ;if equ,roll down
078E    2A 3FFA             LHLD    CROW    ;get print out loc
0791    2B                  DCX     H
0792    2B                  DCX     H
0793    CD 0682             CALL    $1
0796    EB                  XCHG            ;hl=loc
0797    1E 31               MVI     E,"1"

0799    16 B1       SCLLP1: MVI     D,"1"+080h
079B    3E BA               MVI     A,"9"+081h
079D    72          SCLLP2: MOV     M,D
079E    14                  INR     D       ;"1" to "9"
079F    23                  INX     H       ;next location
07A0    BA                  CMP     D       ;exceeding "9"?
07A1    C2 079D             JNZ     SCLLP2
07A4    3E 39               MVI     A,"9"
07A6    73                  MOV     M,E
07A7    1C                  INR     E       ;"1" to "8"
07A8    23                  INX     H       ;next location
07A9    BB                  CMP     E       ;exceeding "8"?
07AA    C2 0799             JNZ     SCLLP1
07AD    C9                  RET

                    ;VERTICAL INTERRUPT CONTINUE
                    ;*********************************************
07AE    2B          VTSUB:  DCX     H       ;VCALEN
07AF    74                  MOV     M,H     ;h<>0, enable VCAL routine
07B0    2A 3FF8             LHLD    CUR     ;get cursor
07B3    36 03               MVI     M,3     ;write to DP8350
07B5    2A 3FF6             LHLD    TOP     ;top of page
07B8    36 02               MVI     M,2     ;write to DP8350
07BA    D3 40               OUT     VERPRT  ;clr vert intr flip/flop
07BC    E1                  POP     H
07BD    FB                  EI
07BE    C9                  RET
                    PAGE

 STARPLEX MACRO-ASSEMBLER V2.0          PAGE    29
CRT801
 07BF
                    ;{FUNCTION} ace, auto line feed, upper/lower case
07BF    DB 40       ACESW:  IN      SETSW   ;read switch settings
07C1    E6 10               ANI     010h
07C3    32 3FF2             STA     AULF    ;set auto lf flag

07C6    DB 40               IN      SETSW   ;read switch again
07C8    E6 20               ANI     020h
07CA    C3 07D2             JMP     STUL    ;set u/l case flag
```

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```
                                ;INIT ACE, TOGGLE ULCASE (LOCAL)
07CD    3A 3FF0         ATGUL:  LDA     ULCASE
07D0    EE 20                   XRI     020h    ;toggle u/l case
07D2    32 3FF0         STUL:   STA     ULCASE

07D5    CD 07F0                 CALL    LUBD    ;lookup baud constant

07D8    21 9003                 LXI     H,ACECTL
07DB    74                      MOV     M,H     ;set DLAB

07DC    2E 01                   MVI     L,1
07DE    72                      MOV     M,D     ;set baud high
07DF    2B                      DCX     H
07E0    73                      MOV     M,E     ;set baud low

07E1    2E 03                   MVI     L,3
07E3    36 02                   MVI     M,2     ;7 bit,1 stop bit

07E5    3A 3FF1                 LDA     LOCLM   ;local?
07E8    3C              EDACE:  INR     A
07E9    21 9000                 LXI     H,ACEDTA
07EC    5E                      MOV     E,M     ;remove ace input
07ED    23                      INX     H       ;ACEITR mask
07EE    77                      MOV     M,A     ;en/disable ace intr
07EF    C9                      RET

07F0    DB 40           LUBD:   IN      SETSW   ;lookup baud constant
07F2    E6 0E                   ANI     0Eh
07F4    C6 F0           BADDR:  ADI     low B110;add base addr
07F6    6F                      MOV     L,A
07F7    26 01                   MVI     H,1
07F9    5E                      MOV     E,M     ;get baud low
07FA    23                      INX     H
07FB    56                      MOV     D,M     ;get baud high
07FC    C9                      RET
                                END     START

 STARPLEX MACRO-ASSEMBLER V2.0          PAGE    30
CRT801
Macros:

Symbols:
$1      0682    $2      05A0    $3      0681    $4      04A7
$5      04A9    $D1     0767    $D2     059B    $D3     0752
$DLY    075E    $G1     06AD    $G2     06AC    $G3     06B2
ACE     0038    ACECTL  9003    ACEDTA  9000    ACEDUP  001B
ACEITR  9001    ACESTU  9005    ACESW   07BF    ADDCUR  05A2
ATGUL   07CD    AULF    3FF2    B110    01F0    B1200   01F4
B19200  01FC    B2400   01F6    B38400  01FE    B4800   01F8
B600    01F2    B9600   01FA    BADDR   07F4    BELL    0434
BELPRT  0001    BGNDF   04F7    BS      041F    BS1     0422
BSRTN   0417    C1D     023A    C7E     0240    CALCX   05A6
CALCY   05B4    CALJMP  015C    CARRTN  03B9    CB      0204
CE      020A    CFB     0642    CFBDIF  0653    CFBLP   064A
CG      020E    CHAR    0372    CHKGM   06C1    CJMP    0158
CLRROW  03DE    CLRSCN  04CE    CLRWLP  04E1    CMRTN   025C
CPLP    056F    CPYCTL  3FE7    CR      0222    CR      000D
CRACE   074A    CRLR    0590    CROW    3FFA    CROWH   3FFB
CTLRW1  04E6    CTLRW2  04E9    CU      022A    CUR     3FF8
CUREN   3FEC    CURH    3FF9    CURLOC  0174    CURTMR  3FEB
CURULK  04AE    CX4FD   05B3    CY17D   05BE    DCROW   03DB
DCUR1   0463    DEGRPH  06BC    DEL     0419    DFCLOC  0171
DICMD   03CE    DICUR   001B    DMYROW  3F00    DRCFL   067A
DRLLP   04C7    DRTLN   04C0    DRTPG   04BA    DRWZCU  058C
DWNCUR  0460    EDACE   07E8    ENGRPH  06B7    F1      0A5F
F10     84D8    F11     85F3    F12     8472    F13     848C
F14     84AE    F15     8DD1    F16     ADA2    F17     84F1
F18     84F7    F19     836B    F2      03B9    F20     835B
F21     8505    F22     8512    F23     AD26    F24     9E8A
F25     0419    F26     83DB    F27     84C0    F28     84BA
F29     8642    F3      03B1    F30     84CE    F31     8CB6
F32     801B    F33     871D    F34     87BF    F35     0AC5
F36     86BC    F4      0C34    F5      060A    F6      0437
F7      041F    F8      844E    F9      8460    FBG     3F20
FCHR2   3780    FFCHK   0267    FFEND   3F9F    FFRD    3FE5
FFSTRT  3F50    FFWCT   3FEA    FFWRT   3FE6    FGNDF   04F1
FIFACE  004E    FRCR    0596    FROW    3FFE    FROWH   3FFF
FS      0437    FUNC    0168    GECNTL  3FEF    GRAPH   068A
GSYMBL  3FF3    HOMCUR  04DB    ICMD    3FE8    ILCHAR  03AB
ILELIN  02C2    ILNERG  0547    INIT    00E2    INSCHA  036B
INSCHR  038D    INSLNE  0505    INSLP   039B    IRWOS   05C1
ISLRG   0526    ISNPA   053C    JMPADD  016A    KBD     0020
KBDACE  01E4    KBDINT  02C9    KBDLCK  3FEE    KBDPRT  0080
KBLK    04B6    KLCRTN  0260    KNACTV  0327    KULCDE  0003
LCL     02F2    LCLFUN  005F    LCLIND  0002    LDFGD   04FA
LEADIN  3FE9    LENDLP  0729    LF      000A    LFD     03C1
LFEED   03B1    LFSCR   03D2    LGPARA  068D    LIN     8000
LINC    007E    LINEXE  02BE    LINF    3FA0    LINFH   3FA1
LINMDE  0283    LINP    3FA3    LINPFN  02A4    LINPRA  02B3
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```
LINSET  02C5    LINWCT  3FA2    LNSP    0734    LOCLM   3FF1
LRDCUR  0773    LROW    3FFC    LROWH   3FFD    LSTCHR  03C0
LUBD    07F0    MIDCHR  0387    MOVDWN  054B    MOVROW  0550
NLC     0B00    NLCSE   02EC    NOWRAP  0066    NPAGE   05F3
NPLP    05F9    NPLT    0601    NRW     3FF5    ONLINE  0345

 STARPLEX MACRO-ASSEMBLER V2.0          PAGE    31
CRT801
OUTACE  0079    OVRNQ   032C    P32SYM  0700    P38SYM  06F3
P4SP    06FB    P6SYM   06F7    PATTN   0112    PQM     06D5
PQMLP   0702    PSPC    03A4    PTNLP   0117    PUSHSP  03EC
RDCUR   05D1    RDFIFO  026E    RDNEQ   04A4    RDX     05E0
RDY     05E7    RFFRNQ  027A    ROLDWN  048C    ROLUP   0472
ROM2    034F    ROSEOD  05CD    ROSFFU  05CB    ROW     0008
ROW1    0082    ROW10   0094    ROW11   0096    ROW12   0098
ROW13   009A    ROW14   009C    ROW15   009E    ROW16   00A0
ROW17   00A2    ROW18   00A4    ROW19   00A6    ROW2    0084
ROW20   00A8    ROW21   00AA    ROW22   00AC    ROW23   00AE
ROW24   00B0    ROW25   00B2    ROW26   00B4    ROW27   00B6
ROW28   00B8    ROW29   00BA    ROW3    0086    ROW30   00BC
ROW31   00BE    ROW32   00C0    ROW33   00C2    ROW34   00C4
ROW35   00C6    ROW36   00C8    ROW37   00CA    ROW38   00CC
ROW39   00CE    ROW4    0088    ROW40   00D0    ROW41   00D2
ROW42   00D4    ROW43   00D6    ROW44   00D8    ROW45   00DA
ROW46   00DC    ROW47   00DE    ROW47D  007E    ROW48   00E0
ROW48D  0080    ROW5    008A    ROW6    008C    ROW7    008E
ROW8    0090    ROW9    0092    ROWDP   0028    ROWPRT  0040
RR1     0182    RR10    0194    RR11    0196    RR12    0198
RR13    019A    RR14    019C    RR15    019E    RR16    01A0
RR17    01A2    RR18    01A4    RR19    01A6    RR1D    01E2
RR2     0184    RR20    01A8    RR21    01AA    RR22    01AC
RR23    01AE    RR24    01B0    RR25    01B2    RR26    01B4
RR27    01B6    RR28    01B8    RR29    01BA    RR3     0186
RR30    01BC    RR31    01BE    RR32    01C0    RR33    01C2
RR34    01C4    RR35    01C6    RR36    01C8    RR37    01CA
RR38    01CC    RR39    01CE    RR4     0188    RR40    01D0
RR41    01D2    RR42    01D4    RR43    01D6    RR44    01D8
RR45    01DA    RR46    01DC    RR47    01DE    RR47D   017E
RR48    01E0    RR48D   01B0    RR5     018A    RR6     018C
RR7     018E    RR8     0190    RR9     0192    RTECTL  3FED
RTN     025F    RUADD   070C    RUNEQ   0484    RWRG    0060
SCALE   0784    SCATT   0667    SCLLP1  0799    SCLLP2  079D
SETSW   0040    SLNERG  0518    SNCNTL  073E    SNDCR   006B
SNDLNE  071D    SNDLP   0735    SPC     0020    START   0000
STFIFO  0244    STK     3FE5    STOFCH  0358    STOFLN  0512
STOFLP  035F    STSCN   06D0    STSP    06CB    STUL    07D2
TAB     060A    TABSTP  0033    TBLJMP  0200    TDADSP  0611
TQLCL   0333    TMCUR   062F    TOP     3FF6    TOPH    3FF7
TSANSP  0620    TSATT   0635    UCUR1   0451    ULCASE  3FF0
UPCUR   044E    VCAL    011F    VCALEN  3FF4    VERPRT  0040
VERT    0010    VERTDP  0030    VRWRAP  0061    VTSUB   07AE
W1      1000    W2      2000    WAIT    014E    WFFRNQ  025A
WTACEA  006D    WTACED  006E    ZROCUR  04DE

No  Fatal error(s)
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TL/F/5869–26

National Semiconductor Corporation

DS75491 MOS-to-LED Quad Segment Driver
DS75492 MOS-to-LED Hex Digit Driver

General Description

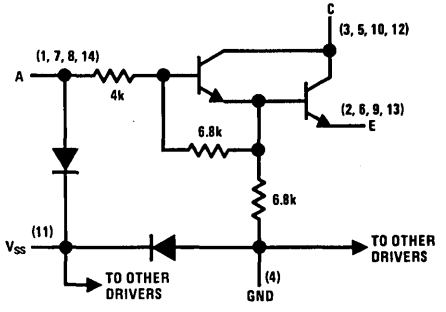
The DS75491 and DS75492 are interface circuits designed to be used in conjunction with MOS integrated circuits and common-cathode LEDs in serially addressed multi-digit displays. The number of drivers required for this time-multiplexed system is minimized as a result of the segment-address-and-digit-scan method of LED drive.

Features

- 50 mA source or sink capability per driver (DS75491)
- 250 mA sink capability per driver (DS75492
- MOS compatability (low input current)
- Low standby power
- High-gain Darlington circuits

Schematic and Connection Diagrams

DS75491 (each driver)



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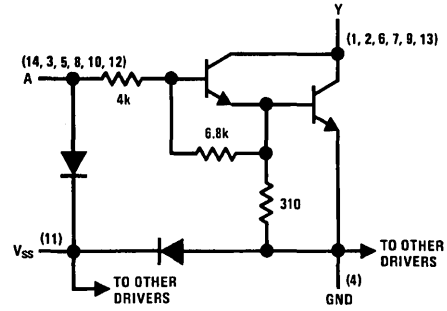
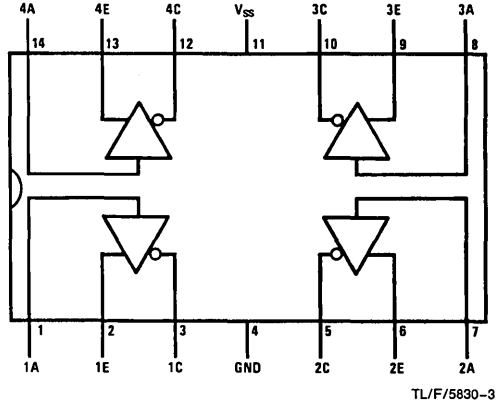
DS75492 (each driver)



TL/F/5830–2

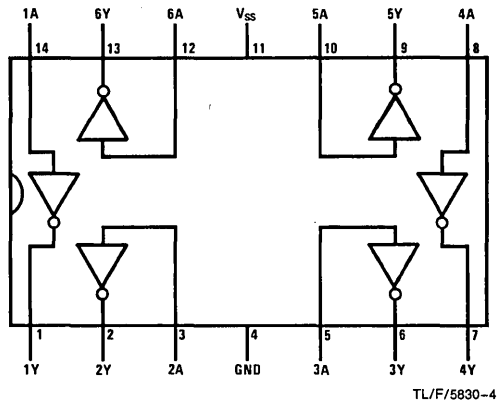
DS75491 Dual-In-Line Package



TL/F/5830–3

Top View

DS75492 Dual-In-Line Package



TL/F/5830–4

Top View

Order Number DS75491J, DS75492J, DS75491N or DS75492N
See NS Package Number J14A or N14A

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

	DS75491	DS75492
Input Voltage Range (Note 4)	−5V to V_{SS}	
Collector Output Voltage (Note 5)	10V	10V
Collector Output to Input Voltage	10V	10V
Emitter to Ground Voltage ($V_I \geq 5V$)	10V	
Emitter to Input Voltage	5V	
Voltage at V_{SS} Terminal with Respect to any Other Device Terminal	10V	10V
Collector Output Current		
Each Collector Output	50 mA	250 mA
All Collector Outputs	200 mA	600 mA

	DS75491	DS75492
Continuous Total Dissipation	600 mW	600 mW
Operating Temperature Range	0°C to +70°C	
Storage Temperature Range	−65°C to +150°C	
Lead Temp. (Soldering, 10 sec)	300°C	300°C
Maximum Power Dissipation at 25°C		
Cavity Package	1308 mW*	1364 mW†
Molded Package	1207 mW*	1280 mW†

*Derate cavity package 8.72 mW/°C above 25°C; derate molded package 9.66 mW/°C above 25°C.

†Derate cavity package 9.09 mW/°C; derate molded package 10.24 mW/°C above 25°C.

Electrical Characteristics V_{SS} = 10V, T_A = 0°C to +70°C unless otherwise noted (Notes 2 and 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
DS75491							
$V_{CE\ ON}$	"ON" State Collector Emitter Voltage	Input = 8.5V through 1 kΩ, V_E = 5V, I_C = 50 mA	T_A = 25°C		0.9	1.2	V
			T_A = 0–70°C			1.5	V
$I_{C\ OFF}$	"OFF" State Collector Current	V_C = 10V, V_E = 0V	I_{IN} = 40 μA			100	μA
			V_{IN} = 0.7V			100	μA
I_I	Input Current at Maximum Input Voltage	V_{IN} = 10V, V_E = 0V, I_C = 20 mA			2.2	3.3	mA
I_E	Emitter Reverse Current	V_{IN} = 0V, V_E = 5V, I_C = 0 mA				100	μA
I_{SS}	Current Into V_{SS} Terminal					1	mA
DS75492							
V_{OL}	Low Level Output Voltage	Input = 6.5V through 1 kΩ, I_{OUT} = 250 mA	T_A = 25°C		0.9	1.2	V
			T_A = 0–70°C			1.5	V
I_{OH}	High Level Output Current	V_{OH} = 10V	I_{IN} = 40 μA			200	μA
			V_{IN} = 0.5V			200	μA
I_I	Input Current at Maximum Input Voltage	V_{IN} = 10V, I_{OL} = 20 mA			2.2	3.3	mA
I_{SS}	Current Into V_{SS} Terminal					1	mA

Switching Characteristics V_{SS} = 7.5V, T_A = 25°C

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DS75491						
t_{PLH}	Propagation Delay Time, Low-to-High Level Output (Collector)	V_{IH} = 4.5V, V_E = 0,		100		ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output (Collector)	R_L = 200Ω, C_L = 15 pF		20		ns
DS75492						
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	V_{IH} = 7.5V, R_L = 39Ω,		300		ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	C_L = 15 pF		30		ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C temperature range for the DS75491 and DS75492.

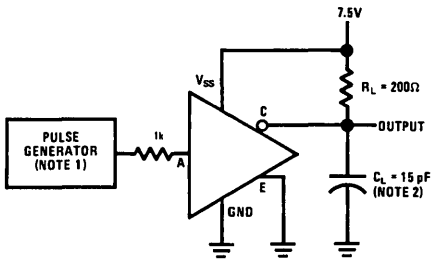
Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: The input is the only device terminal which may be negative with respect to ground.

Note 5: Voltage values are with respect to network ground terminal unless otherwise noted.

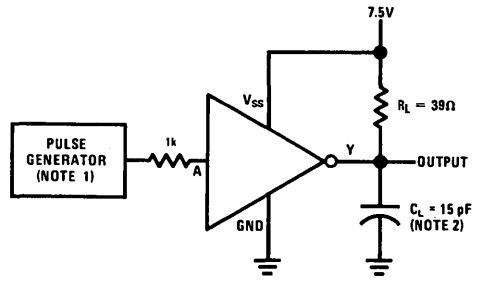
AC Test Circuits and Switching Time Waveforms

DS75491

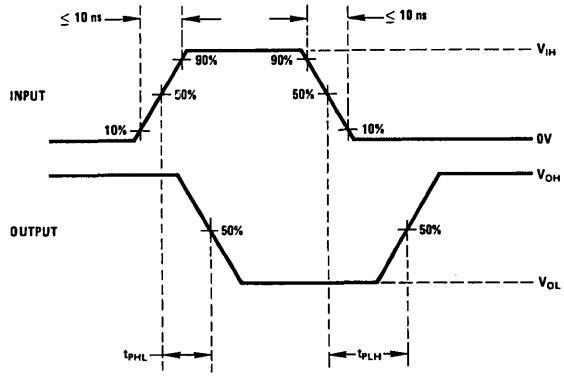


TL/F/5830–5

DS75492



TL/F/5830–6



TL/F/5830–7

Note 1: The pulse generator has the following characteristics: Z_{OUT} = 50Ω, PRR = 100 kHz, t_W = 1 μs.

Note 2: C_L includes probe and jig capacitance.

National Semiconductor Corporation

DS55494/DS75494 Hex Digit Driver

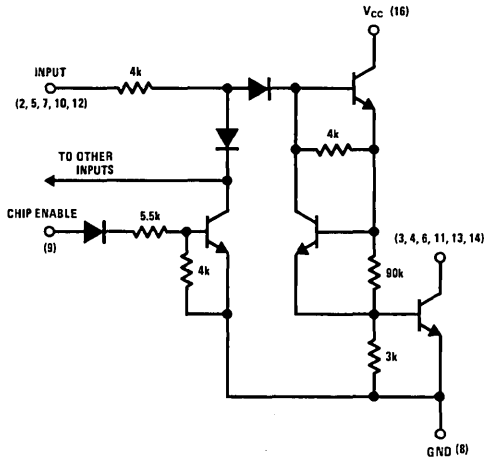
General Description

The DS55494/DS75494 is a hex digit driver designed to interface between most MOS devices and common cathodes configured LED's with a low output voltage at high operating currents. The enable input disables all the outputs when taken high.

Features

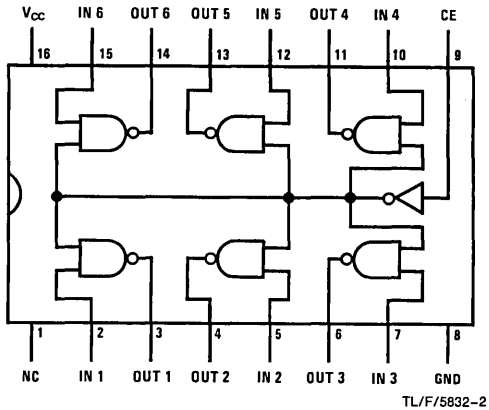
- 150 mA sink capability
- Low voltage operation
- Low inupt current for MOS compatibility
- Low standby power
- Display blanking capability
- Low voltage saturating outputs
- Hex high gain circuits

Schematic and Connection Diagrams



TL/F/5832–1

Dual-In-Line Package



TL/F/5832–2

Top View
Order Number DS55494J, DS75494J or DS75494N
See NS Package Number J16A or N16A

Truth Table

Enable	V_{IN}	V_{OUT}
0	0	1
0	1	0
1	X	1

X = don't care

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Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	10V
Input Voltage	10V
Output Voltage	10V
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1433 mW
Molded Package	1362 mW
Lead Temperature (Soldering 4 seconds)	260°C

*Derate cavity package 9.55 mW/°C above 25°C; derate molded package 10.9 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage, V_{CC}	3.2	8.8	V
Temperature, T_A			
DS75494	0	+70	°C
DS55494	−55	+125	°C

Electrical Characteristics (Notes 2 and 3)

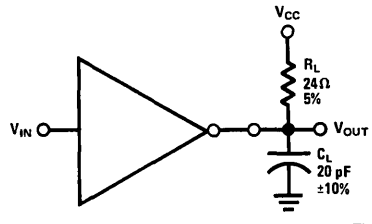
Symbol	Parameter	Conditions				Min	Typ	Max	Units
I_{IH}	Logical "1" Input Current	V_{CC} = Min, V_{IN} = 8.8V	V_{CE} = 8.8V through 100k					2.0	mA
			V_{CE} = 8.8V					2.7	mA
I_{IL}	Logical "0" Input Current	V_{CC} = Max, V_{IN} = −5.5V						−20	μA
I_{OH}	Logical "1" Output Current	V_{CC} = Max, V_{OH} = 8.8V	V_{IN} = 8.8V through 100k, V_{CE} = 0V					400	μA
			V_{IN} = 8.8V, V_{CE} = 6.5V through 1.0k					400	μA
V_{OL}	Logical "0" Output Voltage	V_{CC} = Min, I_{OL} = 150 mA, V_{IN} = 6.5V through 1.0k, V_{CE} = 8.8V through 100k			DS75494		0.25	0.35	V
					DS55494		0.25	0.4	V
I_{CC}	Supply Currents	V_{CC} = Max	One Driver "ON", V_{IN} = 8.8V		DS75474			8.0	mA
					DS55494			10.0	mA
			All Other Pins to GND	V_{CE} = 6.5V through 1.0k				100	μA
				V_{IN} = 8.8V through 100k				100	μA
			All Other Pins to GND					40	μA
t_{OFF}	Output "OFF" Time	C_L = 20 pF, R_L = 24Ω, V_{CC} = 4.0V, See AC Test Circuits					0.04	1.2	μs
t_{ON}	Output "ON" Time	C_L = 20 pF, R_L = 24Ω, V_{CC} = 4.0V, See AC Test Circuits					13	100	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

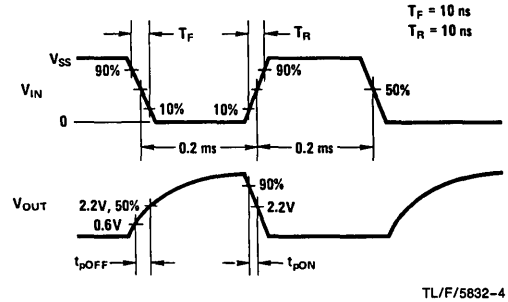
Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C range for the DS75494 and across the −55°C to +125°C range for the DS55494.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

AC Test Circuit and Switching Time Waveforms



TL/F/5832–3



TL/F/5832–4

National Semiconductor Corporation

DS8654 8-Output Display Driver (LED, VF, Thermal Printer)

General Description

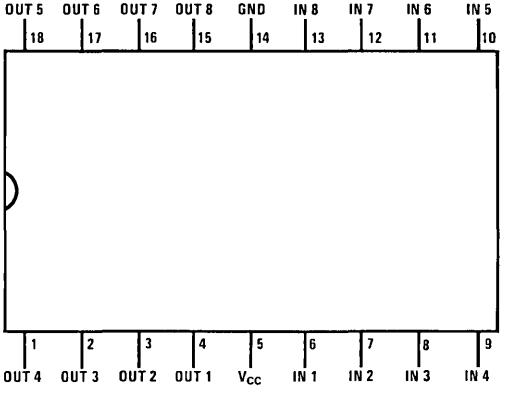
DS8654 is an 8-digit driver with emitter/follower outputs. It can source up to 50 mA at a low impedance, and operates with a constant internal drive current over a wide range of power supply—from 4.5V to 33V. The DS8654 can be used to drive electrical or mechanical, multiplexed or unmultiplexed display systems. It can be used as a segment driver for common cathode displays with external current limiting resistors or can drive incandescent or fluorescent displays directly, both digits (anodes) and segments (grids). It will be necessary to run the device at a lower duty cycle, to keep the maximum package dc power dissipation less than 600 mW while operating all 8 outputs at high supply voltage and large source current. The inputs are MOS compatible and eliminate the need for level shifting since inputs are referenced to the most negative supply of system.

System Description

The DS8654 is specifically designed to operate a thermal printing head for calculator or other uses. In this application the same segment in each digit is selected at the same time, reducing the overall time for a complete print cycle. The DS8654 is an 8-digit driver. With a 15-digit print head, two of the DS8654 are required.

Connection Diagram

Dual-In-Line Package



TL/F/5833–1

Top View

Order Number DS8654N

See NS Package Number N18A

4

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	36V
Input Voltage	36V
Output Voltage	V_{CC} − 36V
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C Molded Package	1563 mW
Lead Temperature (Soldering, 4 seconds)	260°C

*Derate molded package 12.5 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	33	V
Temperature (T_A)	0	+70	°C

Electrical Characteristics (Notes 2 and 3)

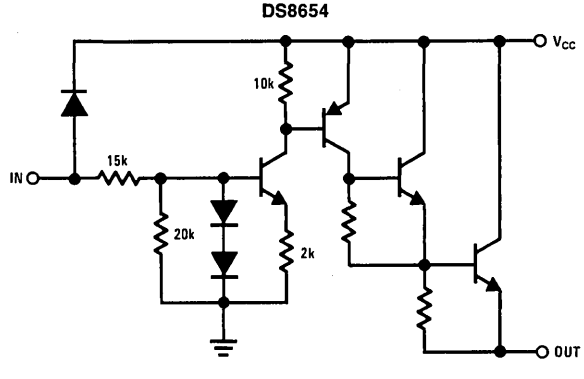
Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{IH}	Logical "1" Input Current	V_{CC} = Max, V_{IN} = 6.5V		390	500	μA
I_{IL}	Logical "0" Input Current	V_{CC} = Max, V_{IN} = 0.4V		13	40	μA
I_{OFF}	"Off" State Leakage Current	V_{OUT} = V_{CC} − 33V		0.01	−100	μA
V_{ON}	"On" State Output Voltage	V_{CC} = Max, I_{IN} = 500 μA, I_{OH} = −50 mA		V_{CC} − 1.8	V_{CC} − 2.5	V
$I_{CC(OFF)}$	Supply Current	V_{CC} = Max, V_{IN} = V_{OUT} = GND		0.01	1.0	mA
$I_{CC(ON)}$	Supply Current (All Outputs "ON")	V_{CC} = Max, V_{IN} = 6.5V, I_{OUT} = 0 mA		7.5	10	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C range for the DS8654. All typicals are given for V_{CC} = 30V and T_A = 25°C.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

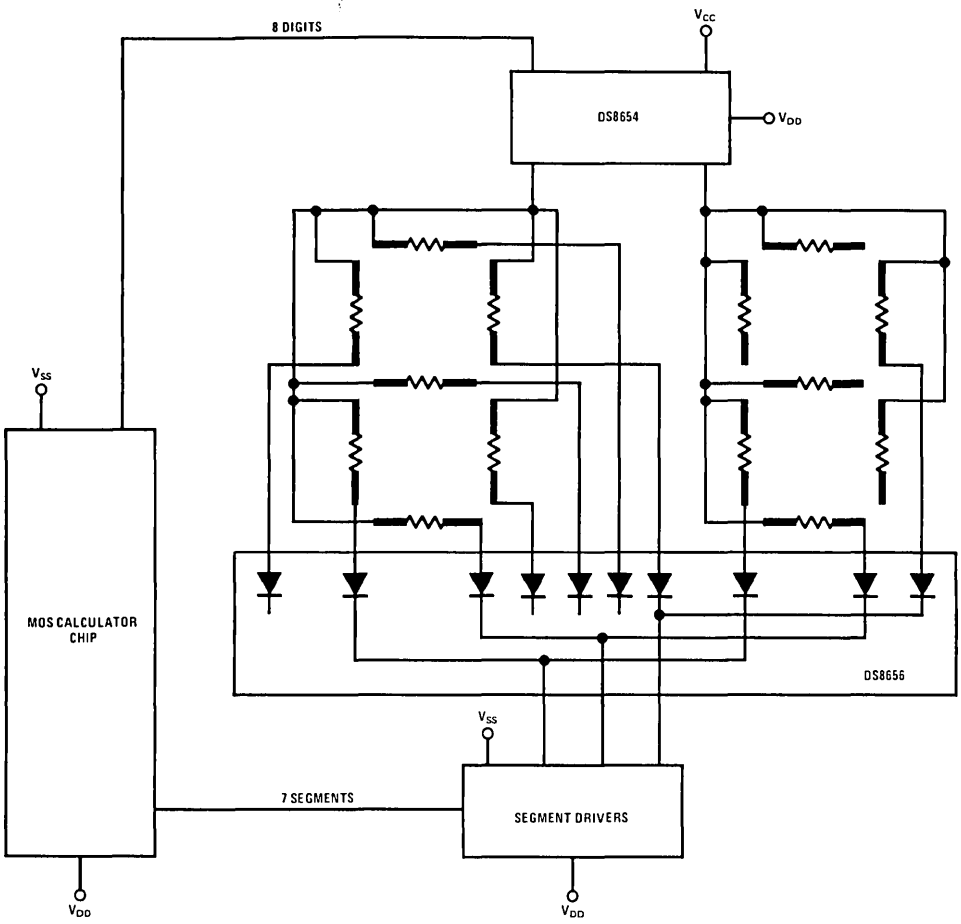
Schematic Diagram



TL/F/5833–2

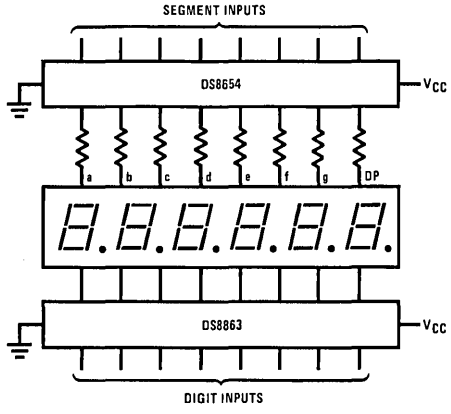
Typical Applications

Thermal Printer



TL/F/5833–3

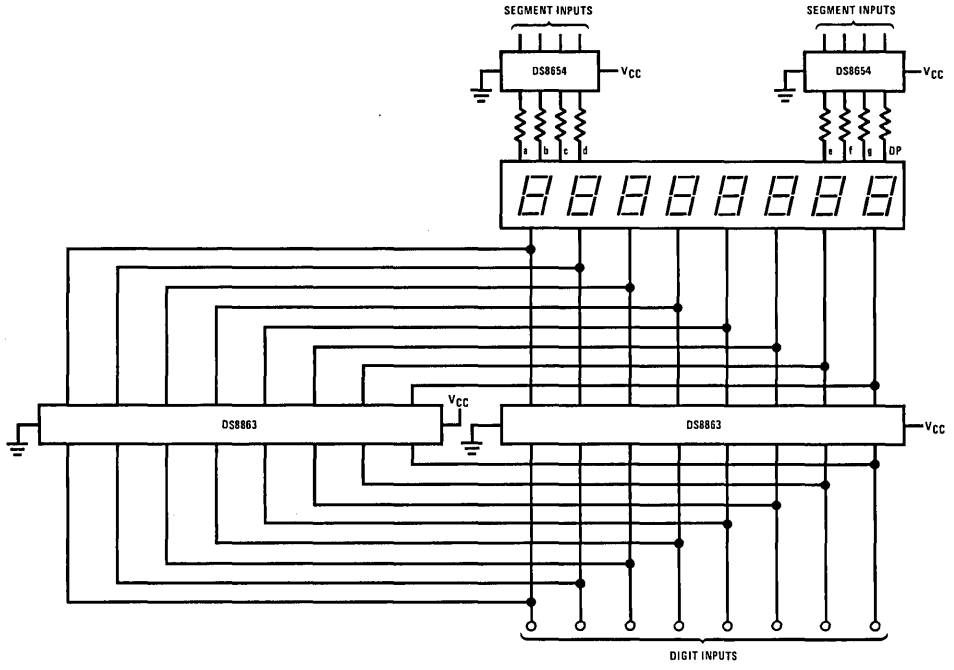
LED Display—0 mA to 50 mA Peak Segment Current



TL/F/5833–4

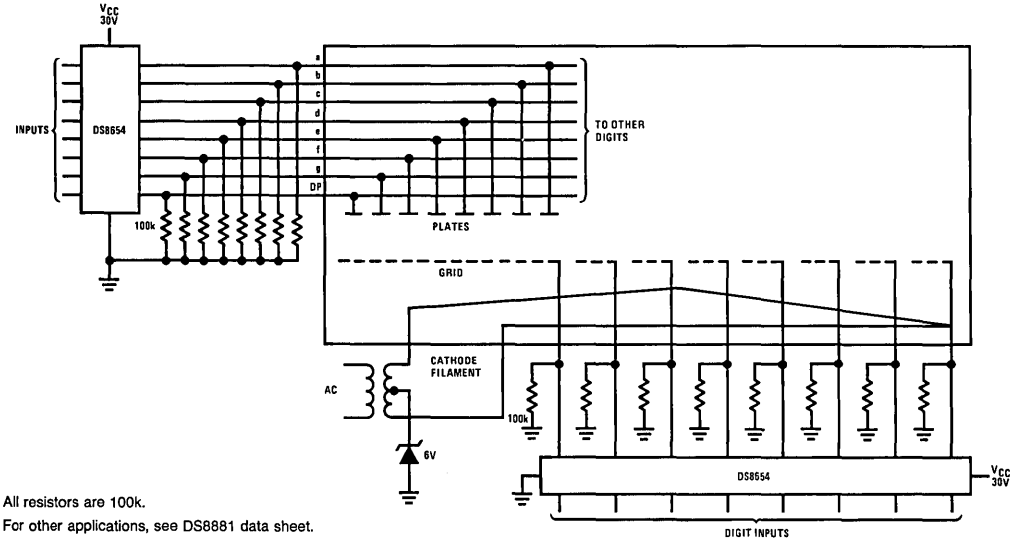
Typical Applications (Continued)

LED Display—50 mA to 100 mA Peak Segment Current



TL/F/5833–5

VF Display



All resistors are 100k.

For other applications, see DS8881 data sheet.

TL/F/5833–6

National Semiconductor Corporation

DS8669 2-Digit BCD to 7-Segment Decoder/Driver

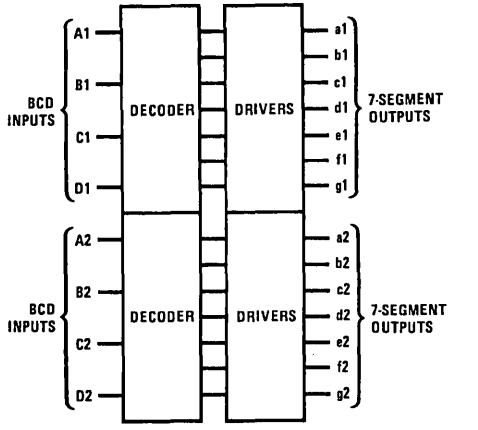
General Description

The DS8669 is a 2-digit BCD to 7-segment decoder/driver for use with common anode LED displays. The DS8669 drives 2 7-segment LED displays without multiplexing. Outputs are open-collector, and capable of sinking 25 mA/segment. Applications include TV and CB channel displays.

Features

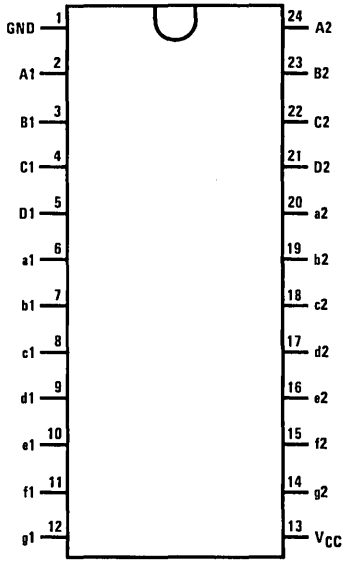
- Direct 7-segment drive
- 25 mA/segment current sink capability
- Low power requirement—16 mA typ
- Very low input currents—2 μA typ
- Input clamp diodes to both V_{CC} and ground
- No multiplexing oscillator noise

Logic and Connection Diagrams



TL/F/5836–1

Dual-In-Line Package



TL/F/5836–2

Top View

Order Number DS8669N
See NS Package Number N24A

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Current	20 mA
Output Voltage	12V
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C Molded Package	2005 mW
Lead Temperature (Soldering, 10 seconds)	300°C

*Derate molded package 16.04 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	6.0	V
Temperature (T_A)	0	+70	°C

Electrical Characteristics V_{CC} = 5.25V, (Note 2)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	Logical "1" Input Voltage	V_{CC} = Min	2.0		V_{CC} + 0.6	V
V_{IL}	Logical "0" Input Voltage	V_{CC} = Min	−0.3		0.8	V
I_O	Logical "1" Output Leakage Current	V_{CC} = Max, V_{OUT} = 10V			50	μA
V_{OL}	Logical "0" Output Voltage	I_{OL} = 25 mA, V_{CC} = Min		0.4	0.8	V
I_{IH}	Logical "1" Input Current	V_{IN} = V_{CC} = Max		2.0	10	μA
I_{IL}	Logical "0" Input Current	V_{IN} = 0V, V_{CC} = Max		−0.1	−10	μA
I_{CC}	Supply Current	All Outputs Low, V_{CC} = Max		16	25	mA
V_{IC}	Input Clamp Voltage	I_{IN} = 10 mA			V_{CC} + 1.5V	V
		I_{IN} = −10 mA			−1.5V	V
t_{pd0}	Propagation Delay to a Logical "0" from Any Input to Any Output	R_L = 400Ω, C_L = 50 pF, T_A = 25°C			10	μs
t_{pd1}	Propagation Delay to a Logical "1" from Any Input to Any Output				10	μs

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C range for the DS8669. All typicals are given for V_{CC} = 5.25V and T_A = 25°C.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

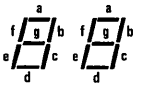
Truth Table

INPUT LEVELS				SEGMENT OUTPUTS														
D_N	C_N	B_N	A_N	a1	b1	c1	d1	e1	f1	g1	a2	b2	c2	d2	e2	f2	g2	DISPLAY 1	DISPLAY 2
0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	0	0
0	0	0	1	1	0	0	1	1	1	1	1	0	0	1	1	1	1	1	1
0	0	1	0	0	0	1	0	0	1	0	0	0	1	0	0	1	0	2	2
0	0	1	1	0	0	0	0	1	1	0	0	0	0	0	1	1	0	3	3
0	1	0	0	1	0	0	1	1	0	0	1	0	0	1	1	0	0	4	4
0	1	0	1	0	1	0	0	1	0	0	0	1	0	0	1	0	0	5	5
0	1	1	0	0	1	0	0	0	0	0	0	1	0	0	0	0	0	6	6
0	1	1	1	0	0	0	1	1	1	1	0	0	0	1	1	1	1	7	7
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	8	8
1	0	0	1	0	0	0	0	1	0	0	0	0	0	0	1	0	0	9	9
1	0	1	0	0	1	1	0	0	0	1	1	0	0	1	0	0	0	C	H
1	0	1	1	0	0	0	1	0	0	0	1	0	0	0	0	1	1	A	J
1	1	0	0	0	0	1	1	0	0	0	1	1	1	0	0	0	1	P	L
1	1	0	1	0	1	1	0	0	0	0	0	1	1	1	0	0	0	E	F
1	1	1	0	1	1	1	1	1	1	0	1	1	1	1	1	1	0	-	-
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	(Blank)	(Blank)

"0" = Segment ON
"1" = Segment OFF

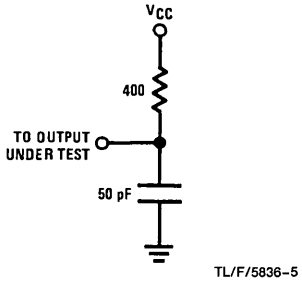
TL/F/5836–3

Display Segment Notation



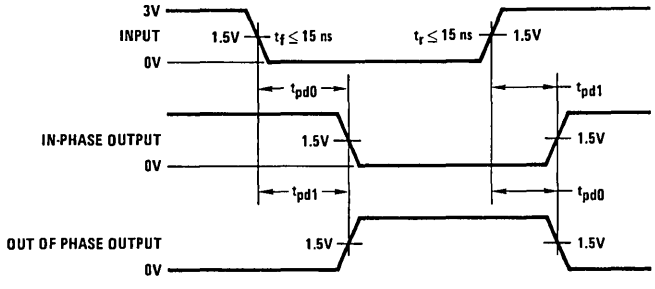
TL/F/5836–4

AC Test Circuit



TL/F/5836–5

Switching Time Waveforms



TL/F/5836–6

National Semiconductor Corporation

DS8859A Open Collector Hex Latch LED Driver

General Description

The DS8859A is a TTL compatible open collector hex latch LED driver with programmable current sink outputs. The sink current is nominally set at 14 mA but may be adjusted by external resistors for any value between 0–32 mA. This device contains six latches which may be set by input data terminals. An active low strobe common to all six latches enables the data input terminals. The DS8859A current sink outputs are switched on by entering a high level into the latches.

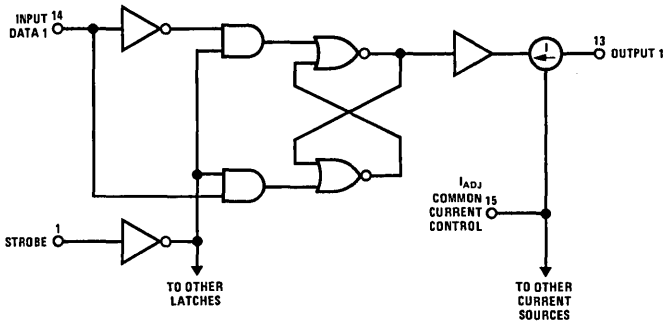
This device is available in either a molded or cavity package. In order not to damage the device there is a limit placed on the power dissipation allowable for each package type. This information is shown in the graph included in this data sheet.

Features

- Built-in latch
- Programmable output current
- TTL compatible inputs
- 32 mA output sink

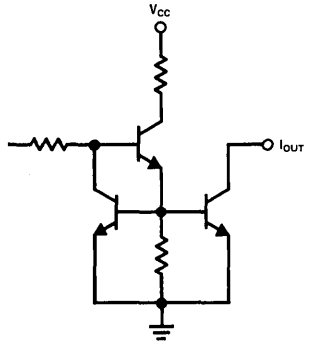
Logic Diagram

DS8859A



TL/F/5838–1

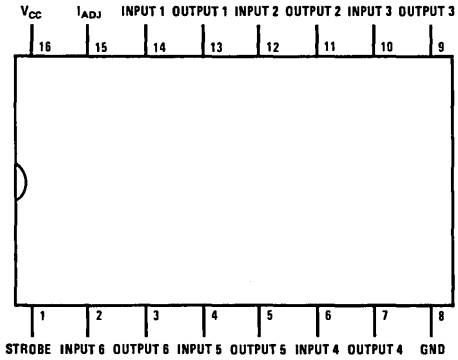
Output Circuit



TL/F/5838–2

Connection Diagram

Dual-In-Line Package



TL/F/5838–3

Top View

Order Number DS8859AJ or DS8859AN
See NS Package Number J16A or N16A

Truth Table

Common Strobe	Input Data	DS8859A Output (t + 1)
0	0	OFF
0	1	ON
1	X	OUTPUT (t)

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5.5V
Output Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1433 mW
Molded Package	1362 mW
Lead Temperature (Soldering, 4 seconds)	260°C

*Derate cavity package 9.55 mW/°C above 25°C; derate molded package 10.9 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage, V_{CC}	4.75	5.25	V
Temperature, T_A	0	+70	°C

Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IH}	Logical "1" Input Voltage	V_{CC} = Min		2.0			V
I_{IH}	Logical "1" Input Current	V_{CC} = Max, V_{IN} = 2.4V				40	μA
V_{IL}	Logical "0" Input Voltage	V_{CC} = Min				0.8	V
I_{IL}	Logical "0" Input Current	V_{CC} = Max, V_{IN} = 0.4V			−1.0	−1.6	mA
V_{CD}	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −12 mA			−1.1	−1.5	V
I_{OH}	Logical "1" Output Current	V_{CC} = Min, V_{IL} = 0.8V, V_{OH} = 5.5V, V_{IH} = 2.0V				250	μA
V_{OL}	Logical "0" Output Voltage	V_{CC} = Min, V_{IL} = 0.8V, I_{OL} = 16 mA, V_{IH} = 2V, V_{IADJ} = V_{CCMIN}				0.4	V
I_{CC}	Supply Current	V_{CC} = Max, Current Sources "OFF," (See Truth Table), (Note 4)				50	mA
I_{SINK}	Output Current	V_{CC} = 5.0V, V_{OUT} = 2.0V, T_A = 25°C (Note 4)	V_{IADJ} = 5V	32			mA
			I_{ADJ} = Open	9	14	26	mA

Switching Characteristics T_A = 25°C, V_{CC} = 5V

Symbol	Parameter	Conditions		Min	Typ	Max	Units
t_{pd0}	Propagation Delay to a Logical "0"	C_{OUT} = 15 pF, R_L = 390Ω, (Note 5)	Data to Output			36	ns
			Strobe to Output			50	ns
t_{pd1}	Propagation Delay to a Logical "1"		Data to Output			150	ns
			Strobe to Output			150	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −0°C to +70°C temperature range. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

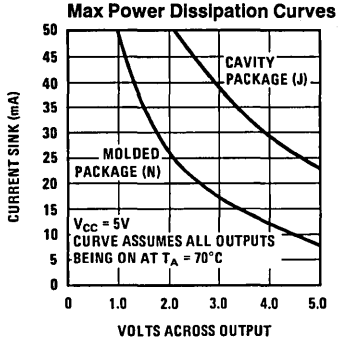
Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: See graphs for changes in I_{SINK} versus changes in temperature and V_{CC}.

Note 5: C_{OUT} includes device output capacitance of approximately 8.5 pF and wiring capacitance.

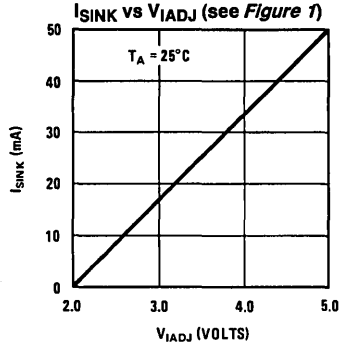
Typical Performance Characteristics

Max Power Dissipation Curves



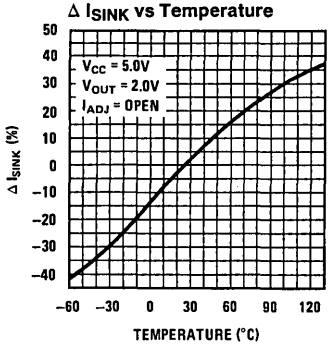
TL/F/5838–4

I_{SINK} vs V_{IADJ} (see *Figure 1*)



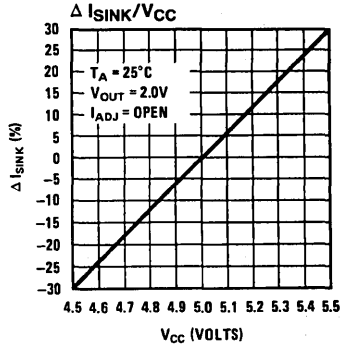
TL/F/5838–5

Δ I_{SINK} vs Temperature



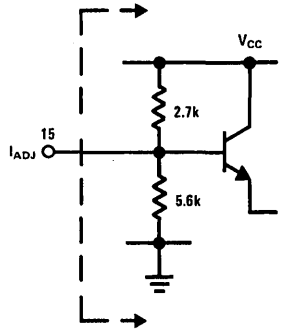
TL/F/5838–6

Δ I_{SINK}/V_{CC}



TL/F/5838–7

I_{SINK} Adjustment Circuit



TL/F/5838–8

I_{ADJ} may be programmed by a voltage source or by resistors.

FIGURE 1

National Semiconductor Corporation

DS8863/DS8963 MOS-to-LED 8-Digit Driver

General Description

The DS8863 and DS8963 are designed to be used in conjunction with MOS integrated circuits and common-cathode LED's in serially addressed multi-digit displays.

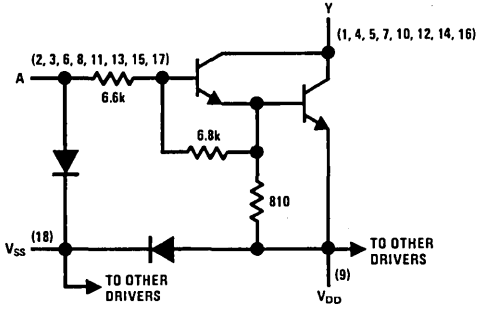
The DS8863 is an 8-digit driver. Each driver is capable of sinking up to 500 mA.

The DS8963 is identical to the DS8863 except it is intended for operation at up to 18V.

Features

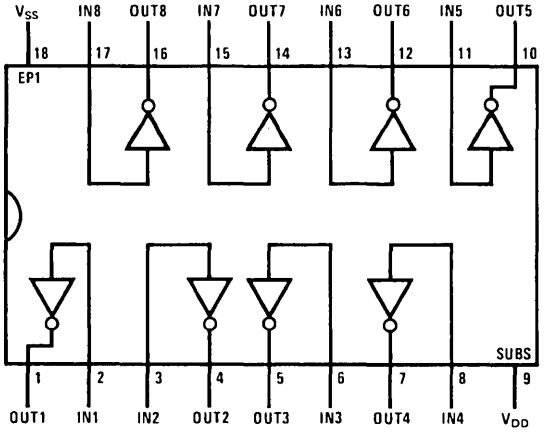
- 500 mA sink capability per driver, DS8863, DS8963
- MOS compatibility (low input current)
- Low standby power
- High gain Darlington circuits

Schematic and Connection Diagrams



TL/F/5839–1

Dual-In-Line Package



TL/F/5839–2

Top View

Order Number DS8863N or DS8963N
See NS Package Number N18A

Absolute Maximum Ratings

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

	DS8863	DS8963
Input Voltage Range (Note 1)	−5V to V_{SS}	−5V to V_{SS}
Collector (Output) Voltage (Note 2)	10V	18V
Collector (Output)-to-Input Voltage	10V	18V
Emitter-to-Ground Voltage ($V_I \geq 5V$)		
Emitter-to-Input Voltage		
Voltage at V_{SS} Terminal With Respect to Any Other Device Terminal	10V	18V

	DS8863	DS8963
Collector (Output) Current		
Each Collector (Output)	500 mA	500 mA
All Collectors (Output)	600 mA	600 mA
Continuous Total Dissipation	800 mW	800 mW
Operating Temperature Range	0°C to +70°C	0°C to +70°C
Storage Temperature Range	−65°C to +150°C	
Maximum Power Dissipation at 25°C		
Molded Package	1563 mW†	1563 mW†
Lead Temperature (Soldering, 4 sec.)	260°C	260°C

†Derate molded package 12.5 mW/°C above 25°C.

Electrical Characteristics V_{SS} = 10V, T_A = 0°C to +70°C unless otherwise noted

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{OL}	Low Level Output Voltage	V_{IN} = 7V, I_{OUT} = 500 mA	T_A = 25°C			1.5	V
						1.6	V
I_{OH}	High Level Output Current	V_{OH} = 10V*	I_{IN} = 40 μA			250	μA
			V_{IN} = 0.5V			250	μA
I_I	Input Current at Maximum Input Voltage	V_{IN} = 10V, I_{OL} = 20 mA				2	mA
I_{SS}	Current into V_{SS} Terminal					1	mA

*18V for the DS8963

Switching Characteristics V_{SS} = 7.5V, T_A = 25°C

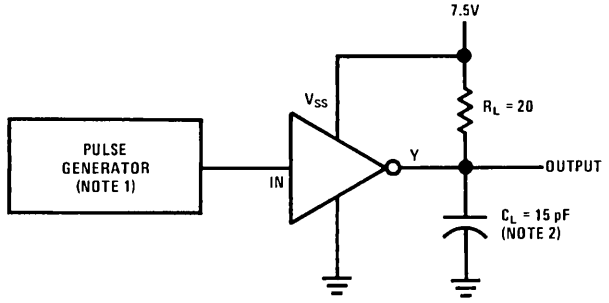
Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	V_{IH} = 8V, R_L = 20Ω, C_L = 15 pF		300		ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output			30		ns

Note 1: The input is the only device terminal which may be negative with respect to ground.

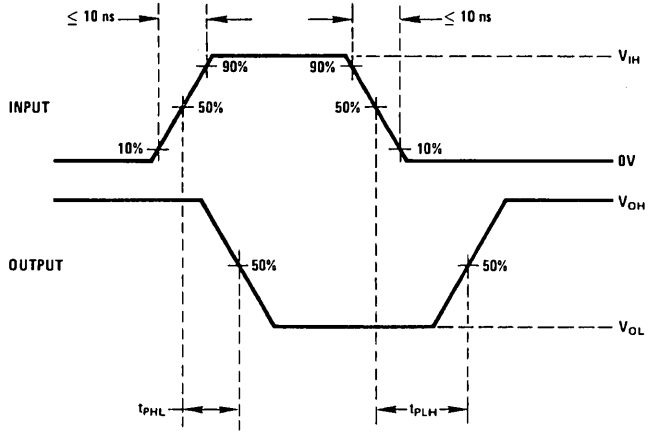
Note 2: Voltage values are with respect to network ground terminal unless otherwise noted.

AC Test Circuits and Waveforms

DS8863



TL/F/5839–3



TL/F/5839–4

Note 1: The pulse generator has the following characteristics: Z_{OUT} = 50Ω, PRR = 100 KHz, t_W = 1μs.

Note 2: C_L includes probe and jig capacitance.

National Semiconductor Corporation

DS8867 8-Segment Constant Current Driver

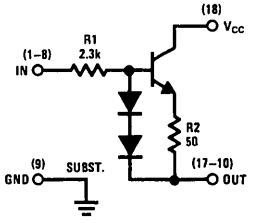
General Description

The DS8867 is an 8-segment driver designed to be driven from MOS circuits operating at 8V ±10% minimum V_{SS} supply and will supply 14 mA typically to an LED display. The output current is insensitive to V_{CC} variations.

Features

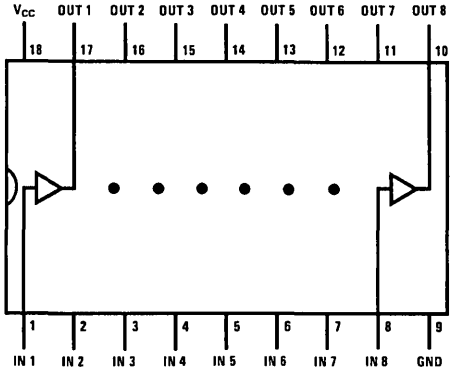
- Internal current control—no external resistors
- 100% efficient, no standby power
- Operates in three and four cell battery systems
- Inputs and outputs grouped for easy PC layout

Schematic and Connection Diagrams



TL/F/5840–1

Dual-In-Line Package



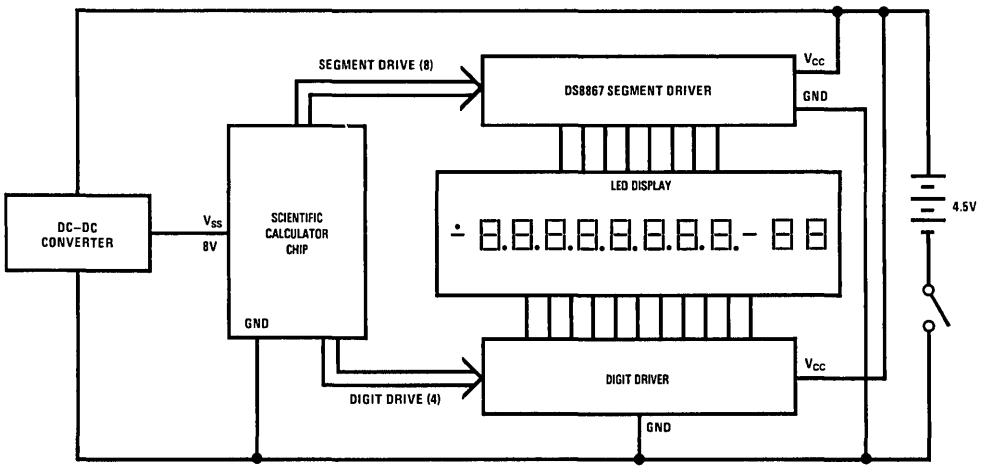
TL/F/5840–2

Top View

Order Number DS8867N
See NS Package Number N18A

Typical Application

Typical 3 Cell Scientific Calculator Circuit



TL/F/5840–3

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	10V
Output Voltage	10V
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C Molded Package	1345 mW
Lead Temperature (Soldering, 4 seconds)	260°C

*Derate molded package 10.76 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage, V_{CC}	3.3	6.0	V
Temperature, T_A	0	+70	°C

Electrical Characteristics (Note 2)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IH}	Logical "1" Input Voltage	V_{CC} = Min, V_{OH} = 2.3V, I_{IH} = 500 μA			4.9	5.4	V
I_{IL}	Logical "0" Input Current	V_{CC} = Max, V_{OL} = 1.8V, V_{IL} = 2.0V			0.1	10	μA
I_{OH}	Logical "1" Output Current	V_{CC} = Min, V_{OH} = 2.3V, I_{IH} = 500 μA		−8	−14	−18	mA
I_{OL}	Logical "0" Output Current	V_{CC} = Max, V_{OL} = 1.0V, V_{IL} = 1.3V			−0.5	−10	μA
$I_{CC\ OFF}$	Supply Current	V_{CC} = Max	All V_{OL} = 1.0V, V_{IL} = 1.3V, (Standby)		4	50	μA
$I_{CC\ ON}$			All V_{OH} = 2.3V, V_{IH} = 7.8V		112	150	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C range.

National Semiconductor Corporation

DS8870 Hex LED Digit Driver

General Description

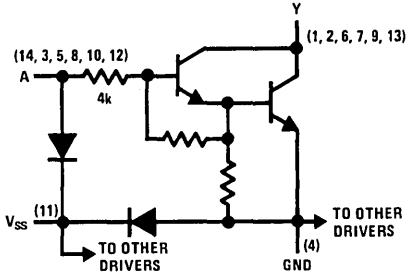
The DS8870 is an interface circuit designed to be used in conjunction with MOS integrated circuits and common-cathode LED's in serially addressed multi-digit displays. The number of drivers required for this time-multiplexed system is minimized as a result of the segment-address-and-digit-scan method of LED drive.

Features

- Sink capability per driver—350 mA
- MOS compatibility (low input current)
- Low standby power
- High-gain Darlington circuits

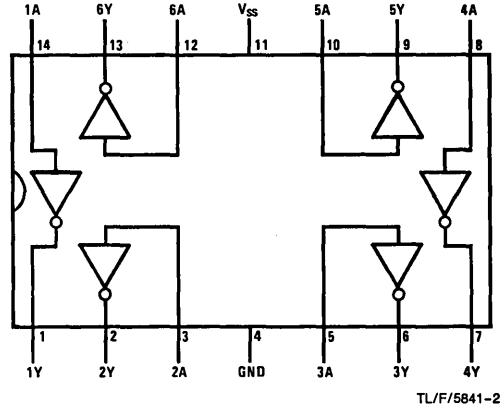
Schematic and Connection Diagrams

DS8870 (Each Driver)



TL/F/5841–1

Dual-In-Line Package



TL/F/5841–2

Order Number DS8870J or DS8870N
See NS Package Number J14A or N14A

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Input Voltage Range (Note 4)	−5V to V_{SS}
Collector Output Voltage	10V
Collector Output to Input Voltage	10V
Voltage at V_{SS} Terminal with Respect to Any Other Device Terminal	10V
Collector Output Current	
Each Collector Output	350 mA
All Collector Outputs	600 mA
Continuous Total Dissipation	800 mW
Operating Temperature Range	0° to +70°C
Storage Temperature	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1308 mW
Molded Package	1207 mW
Lead Temperature (Soldering, 4 seconds)	260°C

*Derate cavity package 8.72 mW/°C above 25°C; derate molded package 9.66 mW/°C above 25°C.

Electrical Characteristics V_{SS} = 10V (Notes 2 and 3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OL}	Low Level Output Voltage	Input = 6.5V through kΩ, I_{OUT} = 350 mA, T_A = 25°C		1.2	1.4	V
V_{OL}	Low Level Output Voltage	Input = 6.5V through 1 kΩ, I_{OUT} = 350 mA			1.6	V
I_{OH}	High Level Output Current	V_{OH} = 10V, I_{IN} = 40 μA			200	μA
I_{OH}	High Level Output Current	V_{OH} = 10V, V_{IN} = 0.5V			200	μA
I_I	Input Current at Maximum Input Voltage	V_{IN} = 10V, I_{OL} = 20 μA		2.2	3.3	mA
I_{SS}	Current into V_{SS} Terminal				1	mA

Switching Characteristics V_{SS} = 7.5V, T_A = 25°C

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	V_{IH} = 7.5V, R_L = 39Ω, C_L = 15 pF		300		ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	V_{IH} = 7.5V, R_L = 39Ω, C_L = 15 pF		30		ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C temperature range.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: The input is the only device terminal which may be negative with respect to ground.

National Semiconductor Corporation

DS8874 9-Digit Shift Input LED Driver

General Description

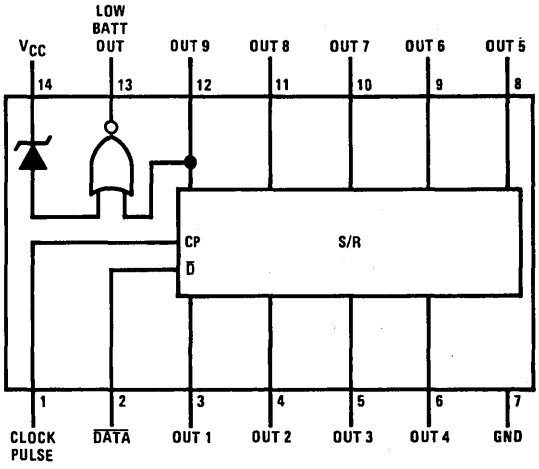
The DS8874 is a 9-digit LED driver which incorporates a shift register input decoding circuit and a low battery indicator. Outputs will sink 110 mA at less than 0.5V drop when sequentially selected. When the V_{CC} supply falls below 6.5V typical, segment current will be furnished at digit 9 time to indicate a low battery condition. Pin 13 is generally connected to the decimal point segment on the display so that when a low battery condition exists, the left-most decimal point lights up.

Features

- 110 mA digit sink
- Low battery indicator
- Minimum number of connections
- MOS compatible inputs

Connection Diagram

Dual-In-Line Package

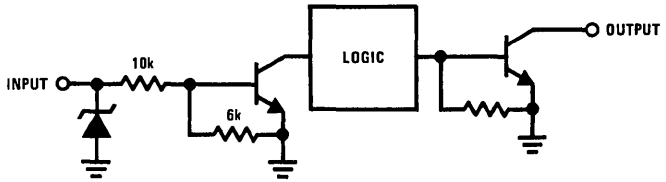


TL/F/5843–1

Top View

Order Number DS8874N
See NS Package Number N14A

Equivalent Schematic



TL/F/5843–2

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	10V
Input Voltage	3V
Output Voltage	10V
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Molded Package	1280 mW
Lead Temperature (Soldering, 4 sec.)	260°C

*Derate molded package 10.24 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	6.0	9.5	V
Temperature (T_A)	0	+70	°C

Electrical Characteristics (Notes 2 and 3)

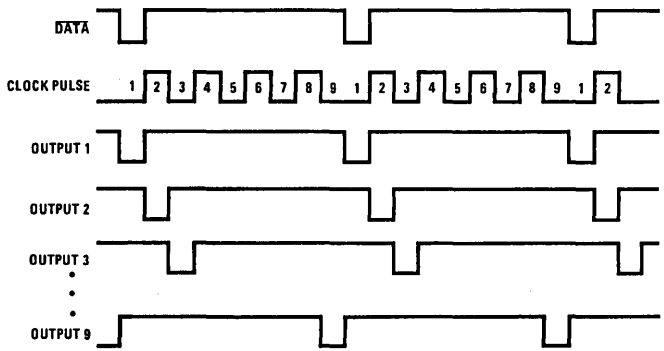
Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{IH}	Logical "1" Input Current	V_{CC} = Max, V_{IN} = 3V		0.25	0.4	mA
I_{IL}	Logical "0" Input Current	V_{CC} = Max, V_{IN} = 0.8V		0.05	0.1	mA
V_{CCL}	Decimal Point "ON"	V_{dp} = 2.3V, I_{dp} = −4 mA, O9 = V_{OL}			6.0	V
V_{CCH}	Decimal Point "OFF"	V_{dp} = 1V, I_{dp} = −10 μA, O9 = V_{OL}	7.0			V
I_{OH}	Logical "1" Output Current	V_{CC} = Max, Output Not Selected			100	μA
V_{OL}	Logical "0" Output Voltage	V_{CC} = Min, Output Selected, I_{O1} = 80 mA		0.45	1	V
		V_{CC} = Max, Output Selected, I_{O1} = 110 mA		0.6	1.5	V
I_{CC}	Supply Current	V_{CC} = Max, One Output Selected		13	19	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C range. All typicals are given for T_A = 25°C.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Timing Diagram (Upper Level More Positive)



TL/F/5843–4

National Semiconductor Corporation

DS7880/DS8880 High Voltage 7-Segment Decoder/Driver

General Description

The DS7880/DS8880 is custom designed to decode four lines of BCD and drive a gas-filled seven-segment display tube.

Each output constitutes a switchable, adjustable current sink which provides constant current to the tube segment, even with high tube anode supply tolerance or fluctuation. These current sinks have a voltage compliance from 3V to at least 80V; typically the output current varies 1% for output voltage changes of 3 to 50V. Each bit line of the decoder switches a current sink on or off as prescribed by the input code. Each current sink is ratioed to the b-output current as required for even illumination of all segments.

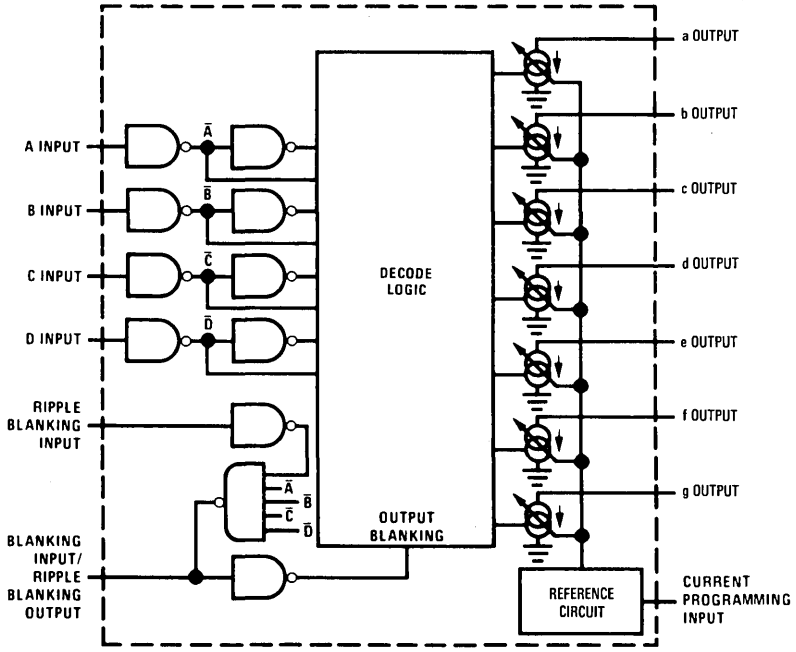
Output currents may be varied over the 0.2 to 1.5 mA range for driving various tube types or multiplex operation. The output current is adjusted by connecting an external program resistor (R_P) from V_{CC} to the Program input in accordance with the programming curve. The circuit design provides a one-to-one correlation between program input current and b-segment output current.

The Blanking Input provides unconditional blanking of any output display, while the Ripple Blanking pins allow simple leading- or trailing-zero blanking.

Features

- Current sink outputs
- Adjustable output current—0.2 to 1.5 mA
- High output breakdown voltage—110V typ
- Suitable for multiplex operation
- Blanking and Ripple Blanking provisions
- Low fan-in and low power

Logic Diagram



TL/F/5845–1

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

V_{CC}	7V
Input Voltage (Except BI)	6V
Input Voltage (BI)	V_{CC}
Segment Output Voltage	80V
Power Dissipation	600 mW
Maximum Power Dissipation* at 25°C	
Cavity Package	1509 mW
Molded Package	1476 mW

*Derate cavity package 10.06 mW/°C above 25°C; derate molded package 11.81 mW/°C above 25°C.

Transient Segment Output Current (Note 4)	50 mA
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 4 sec.)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
DS7880	4.5	5.5	V
DS8880	4.75	5.25	V
Temperature (T_A)			
DS7880	−55	+125	°C
DS8880	0	+70	°C

Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IH}	Logical "1" Input Voltage	V_{CC} = Min		2.0			V
V_{IL}	Logical "0" Input Voltage	V_{CC} = Min				0.8	V
V_{OH}	Logical "1" Output Voltage	V_{CC} = Min, I_{OUT} = −200 μA, RBO		2.4	3.7		V
V_{OL}	Logical "0" Output Voltage	V_{CC} = Min, I_{OUT} = 8 mA, RBO			0.13	0.4	V
I_{IH}	Logical "1" Input Current	V_{CC} = Max, Except BI	V_{IN} = 2.4V		2	15	μA
			V_{IN} = 5.5V		4	400	μA
I_{IL}	Logical "0" Input Current	V_{CC} = Max, V_{IN} = 0.4V	Except BI		−300	−600	μA
			BI		−1.2	−2.0	mA
I_{CC}	Power Supply Current	V_{CC} = Max, R_p = 2.2k, All Inputs = 0V			27	43	mA
V_{CD}	Input Diode Clamp Voltage	V_{CC} = Max, T_A = 25°C, I_{IN} = 12 mA			−0.9	−1.5	V
I_O	SEGMENT OUTPUTS "ON" Current Ratio	All Outputs = 50V, I_{OUT}b = Ref.	Outputs a, f, and g	0.84	0.93	1.02	
			Outut c	1.12	1.25	1.38	
			Output d	0.90	1.00	1.10	
			Output e	0.99	1.10	1.21	
I_b ON	Output b "ON" Current	V_{CC} = 5V, V_{OUT}b = 50V, All Other Outputs ≥ 5V, T_A = 25°C	R_p = 18.1k	0.15	0.20	0.25	mA
			R_p = 7.03k	0.45	0.50	0.55	mA
			R_p = 3.40k	0.90	1.00	1.10	mA
			R_p = 2.20k	1.35	1.50	1.65	mA
V_{SAT}	Output Saturation Voltage	V_{CC} = Min, R_p = 1k±5%, I_{OUT}b = 2 mA, (Note 5)			0.8	2.5	V
I_{CEX}	Output Leakage Current	V_{OUT} = 75V, BI = 0V, R_p = 2.2k			0.003	3	μA
V_{BR}	Output Breakdown Voltage	I_{OUT} = 250 μA, BI = 0V, R_p = 2.2k		80	110		V
t_{pd}	Propagation Delays BCD Input to Segment Output	V_{CC} = 5V, T_A = 25°C			0.4	10	μS
	BI to Segment Output				0.4	10	μs
	RBI to Segment Output				0.7	10	μs
	RBI to RBO				0.4	10	μs

Note 1: "Absolute Maximum Rating" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS7880 and across the 0°C to +70°C range for the DS8880. All typical values are for T_A = 25°C and V_{CC} = 5V.

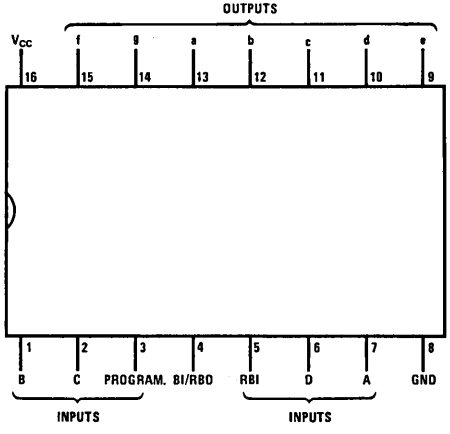
Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min or absolute value basis.

Note 4: In all applications transient segment output current must be limited to 50 mA. This may be accomplished in dc applications by connecting a 2.2k resistor from the anode-supply filter capacitor to the display anode, or by current limiting the anode driver in multiplex applications.

Note 5: For saturation mode the segment output currents are externally limited and ratioed.

Connection Diagram

Dual-In-Line Package



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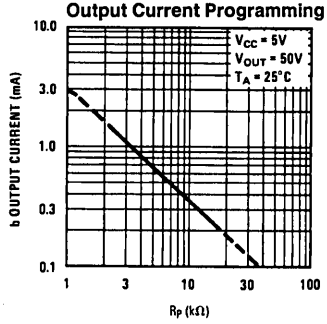
Top View

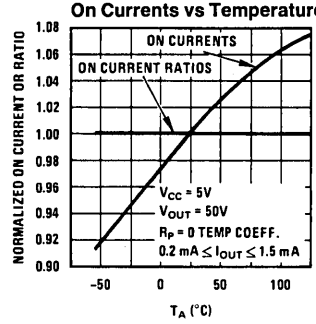
Order Number DS7880J, DS8880J or DS8880N
See NS Package Number J16A or N16A

Typical Performance Characteristics

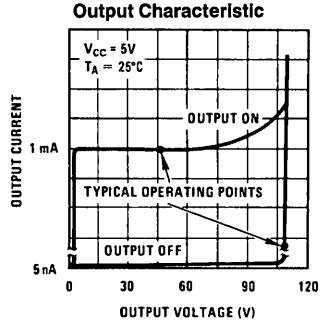
Output Current Programming



On Currents vs Temperature



Output Characteristic



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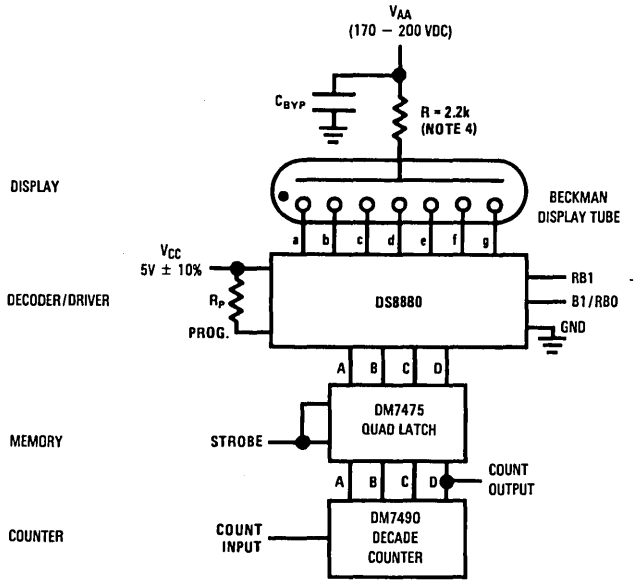
Typical Application



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Truth Table

DECIMAL OR FUNCTION	RBI†	D	C	B	A	BI/RBO	a	b	c	d	e	f	g	DISPLAY
0	1	0	0	0	0	1	0	0	0	0	0	0	1	0
1	X	0	0	0	1	1	1	0	0	1	1	1	1	1
2	X	0	0	1	0	1	0	0	1	0	0	1	0	2
3	X	0	0	1	1	1	0	0	0	0	1	1	0	3
4	X	0	1	0	0	1	1	0	0	1	1	0	0	4
5	X	0	1	0	1	1	0	1	0	0	1	0	0	5
6	X	0	1	1	0	1	0	1	0	0	0	0	0	6
7	X	0	1	1	1	1	0	0	0	1	1	1	1	7
8	X	1	0	0	0	1	0	0	0	0	0	0	0	8
9	X	1	0	0	1	1	0	0	0	0	1	0	0	9
10	X	1	0	1	0	1	0	0	0	1	0	0	0	A
11	X	1	0	1	1	1	1	1	0	0	0	0	0	b
12	X	1	1	0	0	1	0	1	1	0	0	0	1	C
13	X	1	1	0	1	1	1	0	0	0	0	1	0	d
14	X	1	1	1	0	1	0	1	1	0	0	0	0	E
15	X	1	1	1	1	1	0	1	1	1	0	0	0	F
BI*	X	X	X	X	X	0*	1	1	1	1	1	1	1	
RBI	0	0	0	0	0	0	1	1	1	1	1	1	1	

*BI/RBO used as input only

†X = Don't care

SEGMENT IDENTIFICATION

TL/F/5845–5

National Semiconductor Corporation

DS8881 Vacuum Fluorescent Display Driver

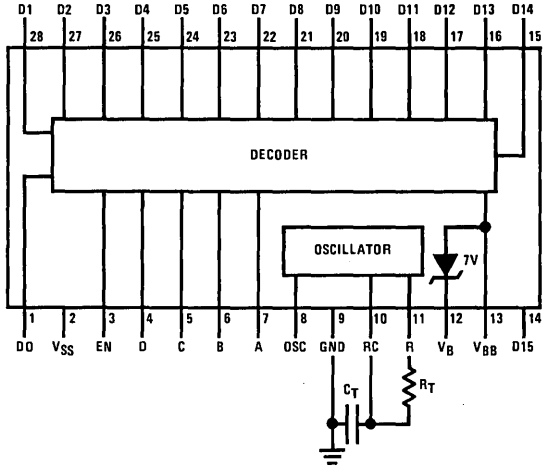
General Description

The DS8881 vacuum fluorescent display driver will drive 16-digit grids of a vacuum fluorescent display. The decode inputs select one of the sixteen outputs to be pulled high. The device contains an oscillator for supplying clock signals to the MOS circuit, the filament bias zener and 50 kΩ pull-down resistors for each grid. Outputs will source up to 7 mA. The DS8881 is designed for 9V operation. If the enable input is pulled low, all outputs are disabled.

Features

- Oscillator frequency accuracy and stability allows maximum system speed
- Interdigit blanking with the enable input provides ghost-free display operation
- 50 kΩ pull-down resistors for each grid
- 7V filament bias zener

Connection Diagram



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Top View

Order Number DS8881N
See NS Package Number N28B

Truth Table All inputs now shown high are off (low)

Inputs					Digit Outputs														
E_N	D	C	B	A	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
H	L	L	L	L	H															
H	L	L	L	H		H														
H	L	L	H	L			H													
H	L	L	H	H				H												
H	L	H	L	L					H											
H	L	H	L	H						H										
H	L	H	H	L							H									
H	L	H	H	H								H								
H	H	L	L	L									H							
H	H	L	L	H										H						
H	H	L	H	L											H					
H	H	L	H	H												H				
H	H	H	L	L													H			
H	H	H	L	H														H		
H	H	H	H	L															H	
H	H	H	H	H																H
L	X	X	X	X	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage ($V_{SS}-V_{BB}$)	38V
Input Current	10 mA
Output Current	−20 mA
Storage Temperature	−65°C to +150°C
Maximum Power Dissipation* at 25°C Molded Package	2168 mW
Lead Temperature (Soldering, 4 sec.)	260°C

*Derate molded package 17.35 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage			
V_{SS}	5.0	9.5	V
V_{BB}	Gnd	−26	V
Temperature (T_A)	0	+70	°C

Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions				Min	Typ	Max	Units
V_{IH}	Logical "1" Input Voltage	V_{SS} = Max	Enable	I_{IN} = 260 μA				5.1	V
			A, B, C, D	I_{IN} = 1400 μA				1.5	V
I_{IH}	Logical "1" Input Current	V_{SS} = Max	Enable A, B, C, D					260	μA
V_{IL}	Logical "0" Input Voltage	V_{SS} = Max	Enable					1.0	V
			A, B, C, D					0.3	V
I_{IL}	Logical "0" Input Current	V_{SS} = Max	Enable	V_{IN} = 0V				−1.0	V
			A, B, C, D	V_{IN} = $V_{IL(MAX)}$		25			μA
V_{OH}	Logical "1" Output Voltage	Digit Output, I_{OH} = −7 mA				V_{SS} − 2.5			V
I_{OH}	Logical "1" Output Current	V_{SS} = Max, Osc. Output, V_{RC} = 0.6V, V_{OH} = 10V						50	μA
I_{OS}	Output Short-Circuit Current	V_{SS} = Min, Pin R, V_{RC} = 0.6V, V_R = 0V				−150		−450	μA
R_{OUT}	Output Pull-Down Resistor	V_{SS} = Min, Digit Output				30	50	85	kΩ
V_{OL}	Logical "0" Output Voltage	V_{SS} = Min	Osc	V_{RC} = 1.6V	I_{OL} = 6 mA			0.5	V
			Pin R		I_{OL} = 60 μA			0.2	V
		V_{SS} = Max	Digit Output	V_{ENABLE} = 1V	I_{OL} = 10 μA			V_{BB} + 1.4	V
I_{SS}	Supply Current	V_{SS} = 9.5V	I_{OH} = 0	V_{ENABLE} = 5.1V			9.0	12.5	mA
				V_{ENABLE} = 1V			5.0	9.0	mA
I_{BB}	Supply Current	V_{SS} = 9.5V, V_{BB} = −26V	I_B = 0, I_{IN} = 300 μA (Note 4)	V_{ENABLE} = 1V			−0.8	−1.5	mA
				V_{ENABLE} = 5.1V			−3.0	−5.0	mA
V_B	Filament Bias Voltage	I_B = 10 mA				V_{BB} + 6.4	V_{BB} + 6.9	V_{BB} + 7.4	V

4

Switching Characteristics $T_A = 25°C$ unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd0}	Propagation Delay to a Logical "0" from Enable Input to Digit Output	$R_L = 4.7\ k\Omega$, $C_L = 50\ pF$, $V_{BB} = -23V$, $V_{SS} = 8V$			1	μs
t_{pd0}	Propagation Delay to a Logical "0" A, B, C, D to Digit Output				1	μs
t_{pd1}	Propagation Delay to a Logical "1" from Enable Input to Digit Output				300	ns
t_{pd1}	Propagation Delay to a Logical "1" from A, B, C, D to Digit Output				500	ns
t_{FALL}	Oscillator Output Transition Time from 1 to 0	$V_{SS} = 9.5V$, $R_L = 6k$ to V_{SS}, $C_L = 25\ pF$			50	ns
f_{OSC}	Oscillator Frequency	$7V < V_{SS} < 9.5V$, $R_T = 27\ k\Omega \pm 2\%$, $R_L = 1.3k$, $C_T = 100\ pF$, $\pm 5\%$, $C_L = 50\ pF$	320	360	400	kHz
dc	Oscillator Duty Cycle		46	56	66	%

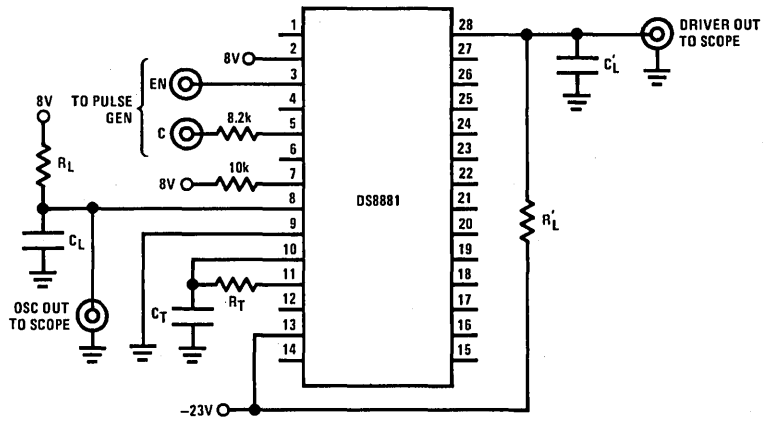
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C for the DS8881. All typicals are given for $V_{CC} = 5V$ and $T_A = 25°C$.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

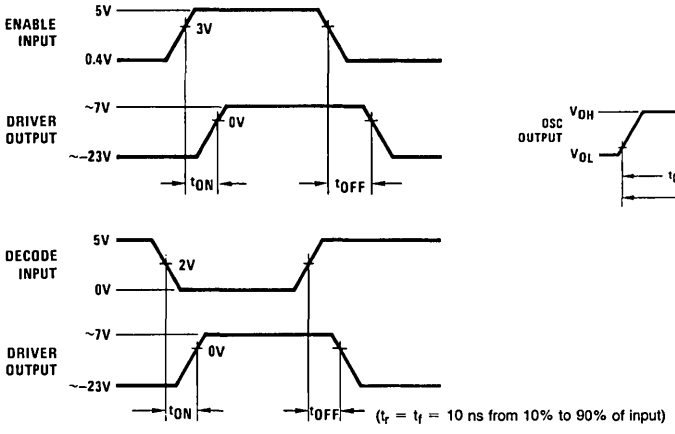
Note 4: Approximately 50% of input current on pins 4, 5, 6, 7 is shunted to V_{BB}. If minimum I_{BB} is desired, then I_{IN} should be minimized by using resistors in series with the inputs.

AC Test Circuit



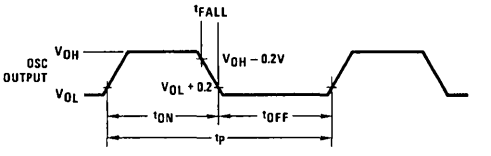
TL/F/5846–2

Switching Time Waveforms



($t_r = t_f = 10$ ns from 10% to 90% of input)

TL/F/5846-3

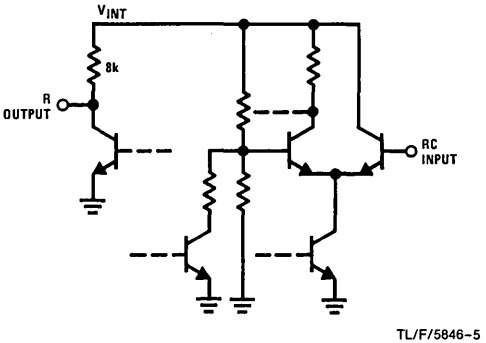


TL/F/5846-4

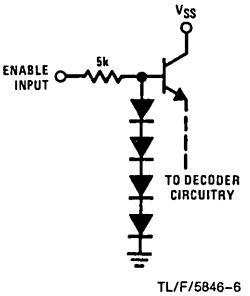
$$\text{Duty Cycle} = \frac{t_{ON}}{t_p}$$

$$\text{Frequency} = \frac{1}{t_p}$$

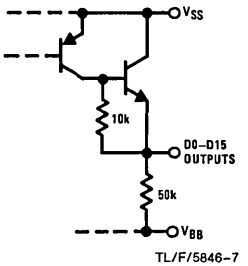
Input-Output Schematics



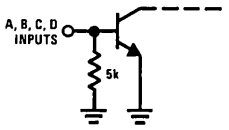
TL/F/5846-5



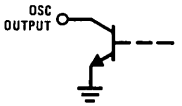
TL/F/5846-6



TL/F/5846-7



TL/F/5846-8



TL/F/5846-9

National Semiconductor Corporation

DS8884A High Voltage Cathode Decoder/Driver

General Description

The DS8884A is designed to decode four lines of BCD input and drive seven-segment digits of gas-filled readout displays.

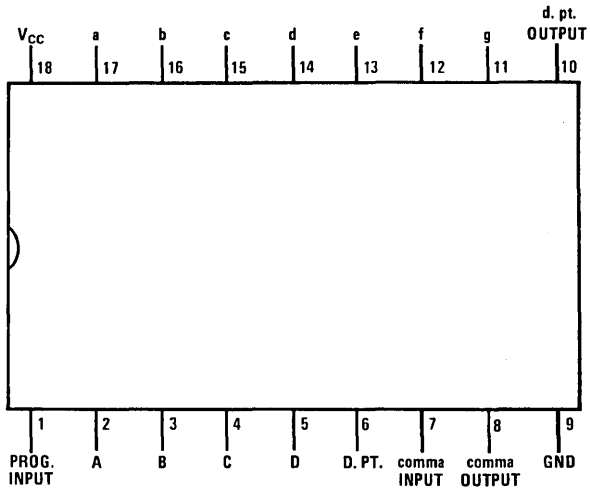
All outputs consist of switchable and programmable current sinks which provide constant current to the tube cathodes, even with high tube anode supply tolerance. Output currents may be varied over the 0.2 mA to 1.2 mA range for multiplex operation. The output current is adjusted by connecting an external program resistor (R_P) from V_{CC} to the program input in accordance with the programming curve. Unused outputs must be tied to V_{CC}.

Features

- Usable with AC or DC input coupling
- Current sink outputs
- High output breakdown voltage
- Low input load current
- Intended for multiplex operation
- Input pullups increase noise immunity
- Comma/d.pt. drive

Connection Diagram

Dual-In-Line Package



TL/F/5847–2

Top View

Order Number DS8884AN
See NS Package Number N18A

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

V_{CC}	7V
Input Voltage (Note 4)	V_{CC}
Segment Output Voltage	80V
Power Dissipation	600 mW
Transient Segment Output Current (Note 5)	50 mA
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C Molded Package	1714 mW

*Derate molded package 13.71 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.75	5.25	V
Temperature (T_A)	0	+70	°C

Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions		Min	Max	Units
V_{IH}	Logical "1" Input Voltage	V_{CC} = 4.75V		2.0		V
V_{IL}	Logical "0" Input Voltage	V_{CC} = 4.75V			1.0	V
I_{IH}	Logical "1" Input Current	V_{CC} = 5.25V, V_{IN} = 2.4V			15	μA
I_{IL}	Logical "0" Input Current	V_{CC} = 5.25V, V_{IN} = 0.4V			−250	μA
I_{CC}	Power Supply Current	V_{CC} = 5.25V, R_P = 2.8k, All Inputs = 5V			40	mA
V_{I+}	Positive Input Clamp Voltage	V_{CC} = 4.75V, I_{IN} = 1 mA		5.0		V
V_{I-}	Negative Input Clamp Voltage	V_{CC} = 5V, I_{IN} = −12 mA, T_A = 25°C			−1.5	V
ΔI_O	SEGMENT OUTPUTS "ON" Current Ratio	All Outputs = 50V, I_{OUT} b = Ref., All Outputs		0.9	1.1	
$I_{b\,ON}$	Output b "ON" Current	V_{CC} = 5V, V_{OUT} b = 50V, T_A = 25°C	R_P = 18.1k	0.15	0.25	mA
			R_P = 7.03k	0.45	0.55	mA
			R_P = 3.40k	0.90	1.10	mA
			R_P = 2.80k	1.08	1.32	mA
I_{CEX}	Output Leakage Current	V_{OUT} = 75V			5	μA
V_{BR}	Output Breakdown Voltage	I_{OUT} = 250 μA		80		V
t_{pd}	Propagation Delay of Any Input to Segment Output	V_{CC} = 5V, T_A = 25°C			10	μs

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

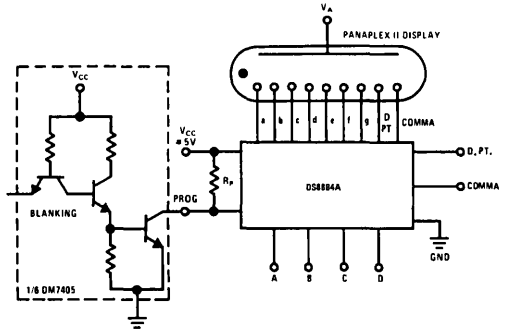
Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C temperature range for the DS8884A. All typical values are for T_A = 25°C and V_{CC} = 5V.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: This limit can be higher for a current limiting voltage source.

Note 5: In all applications transient segment output current must be limited to 50 mA. This may be accomplished in DC applications by connecting a 2.2k resistor from the anode-supply filter capacitor to the display anode, or by current limiting the anode driver in multiplex applications.

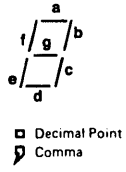
Typical Application



TL/F/5847–4

Truth Table

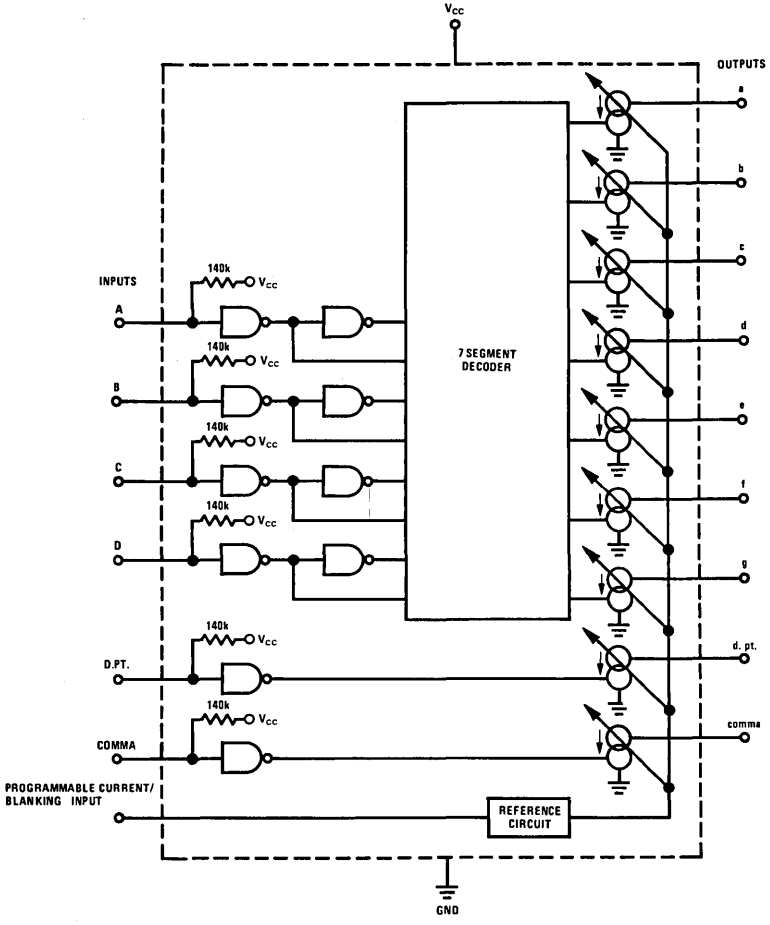
FUNCTION	D.PT.	COMMA	D	C	B	A	a	b	c	d	e	f	g	DISPLAY
0	1	1	0	0	0	0	0	0	0	0	0	0	1	0
1	1	1	0	0	0	1	1	0	0	1	1	1	1	1
2	1	1	0	0	1	0	0	0	1	0	0	1	0	2
3	1	1	0	0	1	1	0	0	0	0	1	1	0	3
4	1	1	0	1	0	0	1	0	0	1	1	0	0	4
5	1	1	0	1	0	1	0	1	0	0	1	0	0	5
6	1	1	0	1	1	0	0	1	0	0	0	0	0	6
7	1	1	0	1	1	1	0	0	0	1	1	1	1	7
8	1	1	1	0	0	0	0	0	0	0	0	0	0	8
9	1	1	1	0	0	1	0	0	0	0	1	0	0	9
10	1	1	1	0	1	0	1	1	0	0	0	1	1	□
11	1	1	1	0	1	1	1	1	0	0	0	1	0	□
12	1	1	1	1	0	0	0	0	1	1	1	0	0	□
13	1	1	1	1	0	1	0	1	1	0	0	0	0	□
14	1	1	1	1	1	0	1	1	1	1	1	1	0	□
15	1	1	1	1	1	1	1	1	1	1	1	1	1	
*D.PT.	0	1	X	X	X	X	X	X	X	X	X	X	X	▫
*Comma	0	0	X	X	X	X	X	X	X	X	X	X	X	❡



TL/F/5847–3

*Decimal point and comma can be displayed with or without any numeral.

Logic Diagram



TL/F/5847–1

National Semiconductor Corporation

DS7889/DS8889 8-Segment High-Voltage Cathode Driver (Active-High Inputs)
DS7897A/DS8897A 8-Digit High-Voltage Anode Driver (Active-Low Inputs)

General Description

The DS7897A/DS8897A is designed to drive the individual anodes of a 7-segment (cathodes) high-voltage gas discharge panel in a time multiplexed fashion.

When driven with appropriate input signals, the driver will switch voltage and impedance levels at the anode. This will allow or prevent ionization of gas around selected cathode in order to form a numeric display. This main application is to interface with MOS outputs (fully-decoded) and the anodes of a gas-discharge panel, since the devices can source up to 16 mA at a low impedance and can tolerate more than 55V in the "OFF" state.

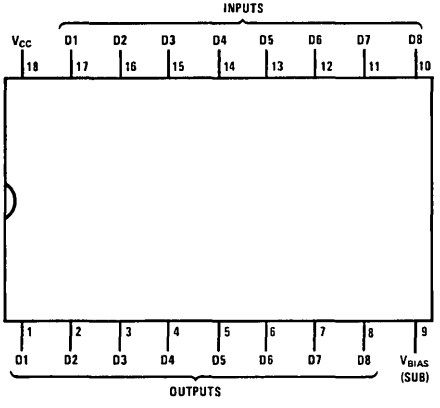
The DS7889/DS8889 is capable of driving 8 segments of a high-voltage display tube with a constant output sink current, which can be adjusted by external program resistor, R_P. The program current is half that of output "ON" current. In the "OFF" state the outputs can tolerate more than 80V. The ratio of "ON" output currents is within ±10%. Inputs have negative clamp diodes. Active high input logic. The main application of the device is to interface MOS circuits to high-voltage displays. Unused outputs should have corresponding inputs connected to V_{EE}.

Features

- Versatile circuits for a wide range of display applications
- High breakdown voltages
- Low power dissipation

Connection Diagrams (Dual-In-Line Packages)

DS7897A/DS8897A



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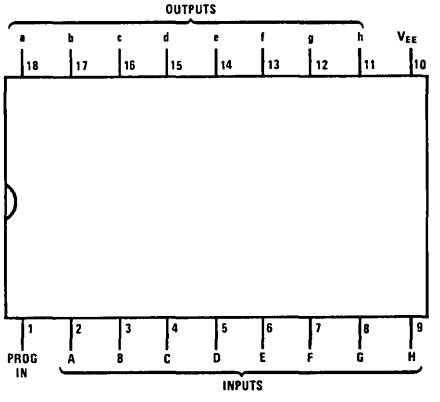
Top View

Order Number DS7897AJ, DS8897AJ or DS8897AN
See NS Package Numbers J18A or N18A

DS7889/DS8889



TL/F/5849–2

Top View

Order Number DS7889J, DS8889J or DS8889N
See NS Package Numbers J18A or N18A

4

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage (V_{CC} − V_{BIAS}) (Note 2)
DS7897A, DS8897A −60V

Input Voltage
DS7897A/DS8897A −20V
DS7899/DS8889 (Note 3) 35V

Output Voltage
DS7897A/DS8897A −65V
DS7889/DS8889 85V

Storage Temperature Range −65°C to +150°C

Maximum Power Dissipation* at 25°C
DS7889/DS8889
Cavity Package 1436 mW
Molded Package 1563 mW

Maximum Power Dissipation† at 25°C
DS7897A/DS8897A
Cavity Package 1496 mW
Molded Package 1714 mW

Lead Temperature (Soldering, 4 seconds) 260°C

*Derate cavity package 11.49 mW/°C above °25C; derate molded package 12.5 mW/°C above 25°C.

†Derate cavity package 11.97 mW/°C above 25°C; derate molded package 13.71 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC} − B_{IAS}) DS7897A/DS8897A	−40	−60	V
Temperature (T_A)			
DS7889, DS7897A	−55	+125	°C
DS8889, DS8897A	0	+70	°C

Electrical Characteristics (Notes 2, 3 and 4)

Symbol	Parameter	Conditions			Min	Typ	Max	Units
DS7897A/DS8897A								
I_{IH}	Logical "1" Input Current	V_{OUT} = −1.4V, I_{OUT} = −16 mA, DS8897A, DS7897A			−300			μA
I_{IL}	Logical "0" Input Current	V_{OUT} = −60V, I_{OUT} = −100 μA, DS8897A, DS7897A					−10	μA
I_I	Input Current	DS7897A, DS8897A, V_{IN} = −12V			−0.45		−1.5	mA
$V_{OUT\ OFF}$	Output "OFF" Voltage	I_{OUT} = −100 μA, I_{IN} = 0 μA			−60	−77		V
$I_{OUT\ OFF}$	Output "OFF" Current	V_{OUT} = −55V, I_{IN} = 0 μA				−0.03	−5.0	μA
$V_{OUT\ ON}$	Output "ON" Voltage	I_{OUT} = −16 mA	V_{IN} = −2.0V			−1.0	−1.4	V
			I_{IN} = −300 μA, DS8897A, DS7897A				−1.4	V
I_{BIAS}	V_{BIAS} Current	I_{OUT} = −16 mA, V_{BIAS} = −60V	V_{IN} = −1.0V			−2.2	−4.0	mA
			I_{IN} = −300 μA, DS8897A, DS7897A (One Driver Only)				−1.0	mA
DS7889/DS8889								
I_I	Input Current	V_{IN} = 6.0V			150	250	350	μA
I_{IL}	Logical "0" Input Current	I_{OUT} = 5.0 μA, V_{OUT} = 75V					7.0	μA
I_{IH}	Logical "1" Input Current	I_{OUT} = 1.4 mA, I_{IP} = 850 μA, V_{OUT} = 50V			80			μA
V_I	Input Clamp Voltage	I_{IN} = −1.0 mA, T_A = 25°C				−0.68	−0.85	V
V_{OH}	Output Breakdown Voltage	I_{OUT} = 100 μA, I_{IN} = 0 μA			80			V
I_{CEX}	Output Leakage Current	V_{OUT} = 75V, −0.1 mA ≤ I_{IN} ≤ 7.0 μA				0.02	5.0	μA
I_{PROG}	Prog. Input Voltage	I_{IP} = 150 μA			1.8	2.3		V
		I_{IP} = 850 μA				4.0	4.5	V
I_{OL}	Logical "0" Output Current	V_{OUT} = 50V, 80 μA ≤ I_{IN} ≤ I_{IP}	I_{IP} = 150 μA	DS7889	210	300	390	μA
				DS8889	240	300	360	μA
			I_{IP} = 400 μA	DS7889	660	800	940	μA
				DS8889	680	800	920	μA
			I_{IP} = 850 μA	DS7889	1.45	1.7	1.95	mA
				DS8889	1.53	1.7	1.87	mA
ΔI_O	Output Current Ratio	I_{OUT} b Ref = 1.7 mA, V_{OUT} = 50V			0.9	1.0	1.1	

Switching Characteristics T_A = 25°C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DS7889/DS8889						
t_{pd0}	Propagation Delay to a Logical "0" from Input to Output	R_P = 6.0k to 6.0V, R_{OUT} = 1.0k TO 6.0V		37	100	ns
t_{pd1}	Propagation Delay to a Logical "1" from Input to Output	Input Ramp Rate ≤ 15 ns, Freq = 1.0 MHz dc = 50%, Amplitude = 6.0V		92	200	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

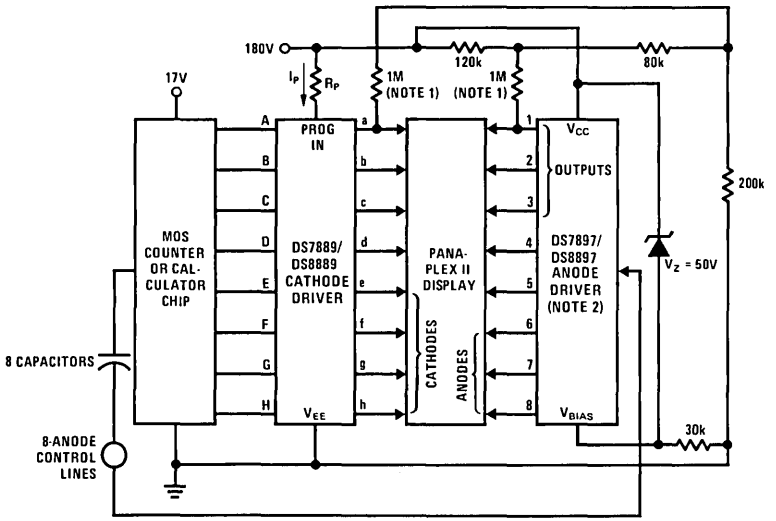
Note 2: All voltage shown for DS7897A/DS8897A with respect to V_{CC} = 0V. All currents into device pins shown as positive, out of device pins as negative. All values shown as max or min on absolute value basis.

Note 3: All voltages for DS7889/DS8889 with respect to V_{EE} = 0V.

Note 4: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS7889 and DS7897A, and across the 0°C to +70°C range for the DS8889 and DS8897A. All typicals are given for T_A = 25°C.

Note 5: Supply currents specified for any one input = −1.0V. All other inputs = −5.5V and selected output having 16 mA load.

Typical Application



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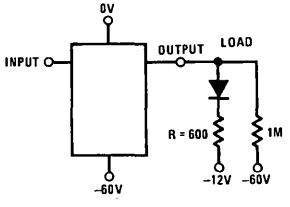
Note 1: All outputs of both cathode and anode driver have loads as shown for output a and digit 1.

Note 2: Use DS8887 for active-high inputs and DS8897 for active-low inputs.

AC Test Circuit & Switching Time Waveforms



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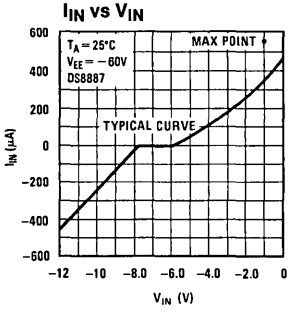
Typical Performance Characteristics



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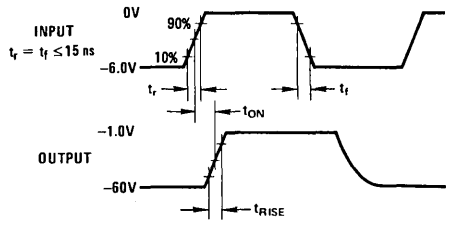
AC Test Circuit & Switching Time Waveforms (Continued)



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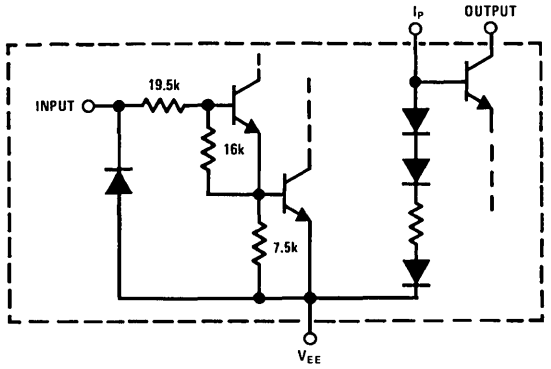
Logic Diagrams

DS7889/DS8889



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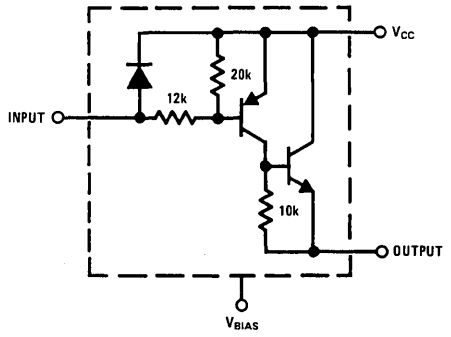
DS7897A/DS8897A



TL/F/5849–8

National Semiconductor Corporation

DS8973 9-Digit LED Driver

General Description

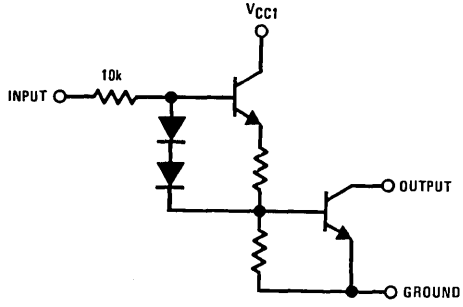
The DS8973 is a 9-digit driver designed to operate from 3-cell battery supplies. Each driver will sink 100 mA to less than 0.7V when driven by only 0.1 mA. Each input is blocked by diodes so that the input can be driven below ground with virtually no current drain. This is especially important in calculator systems employing a DC-to-DC converter on the negative side of the battery. If the converter were on the positive side of the battery, the converter would have to handle all of the display current, as well as the MOS calculator chip current. But if it is on the negative side, it only has to handle the MOS current. The DS8973 is designed for the more efficient operating mode.

Features

- Nine complete digit drivers
- Built-in low battery indicator
- High current outputs—100 mA
- Straight through pin out for easy board layout

Equivalent Circuit Diagrams

Typical Driver Circuit



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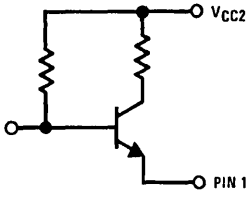
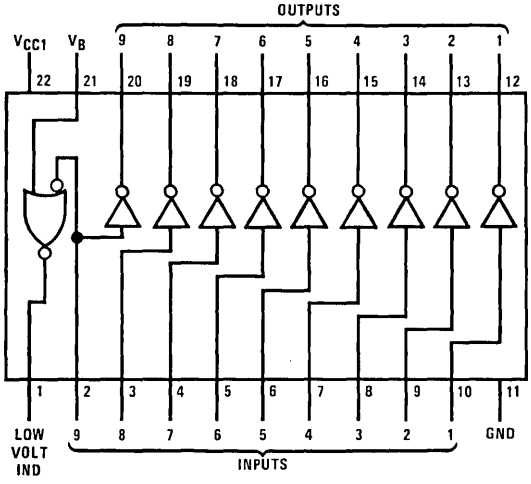
Typical D.P. Out Circuit



TL/F/5851–2

Connection Diagram

Dual-In-Line Package



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Top View

Order Number DS8973N
See NS Package Number N22A

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	10V
Input Voltage	10V
Output Voltage	10V
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C Molded Package	1673 mW
Lead Temperature (Soldering, 4 seconds)	260°C

*Derate molded package 13.39 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_B)	3.0	5.5	V
Supply Voltage (V_{CC1})	3.0	9.5	V
Temperature (T_A)	0	+70	°C

Electrical Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IH}	Logical "1" Input Voltage	V_{CC} = Max		3.9			V
I_{IH}	Logical "1" Input Current	V_{CC} = Max, V_{IH} = 3.9V		0.1		0.3	mA
V_{IL}	Logical "0" Input Voltage	V_{CC} = Max				0.5	V
I_{IL}	Logical "0" Input Current	V_{CC} = Max, V_{IL} = 0.5V				40	μA
V_{BH}	High Battery Threshold	V_{OT} (Pin 1) = 1V, $I_{OT} \leq -50$ μA, T_A = 25°C, V_{IH} (Pin 2) = 3.9V	DS8973	3.6			V
V_{BL}	Low Battery Threshold	V_{OT} (Pin 1) = 2.1V, $I_{OT} \leq -6$ mA, T_A = 25°C, V_{IH} (Pin 2) = 3.9V	DS8973			3.2	V
I_{CEX}	Logical "1" Output Current	V_{CC} = Min, V_{OH} = 9.5V, V_{IL} = 0.5V				50	μA
V_{OL}	Logical "0" Output Voltage	V_{CC} = Min, I_{OL} = 100 mA, V_{IH} = 3.9V				0.7	V
I_{CC1}	Supply Current	V_{CC} = Max, One Input "ON"				6	mA
I_B	Pin 21 (High Battery Supply)	V_{CC} = Max, V_B = Max				1.2	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified, min/max limits apply across the 0°C to +70°C range. All typicals are given for T_A = 25°C.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Driving 7-Segment Gas Discharge Display Tubes with National Semiconductor Drivers

National Semiconductor Corp.
Application Note 84

INTRODUCTION

Circuitry for driving high voltage cold cathode gas discharge 7-segment displays, such as Sperry Information Displays* and Burroughs Panaplex II, is greatly simplified by two monolithic integrated circuits from National Semiconductor. They are: DS8880 high voltage cathode decoder/driver and DS8884A high voltage cathode decoder/driver.

In addition to satisfying all the displays' parameter requirements, including high output breakdown voltage, these circuits have capability of programming segment current, and providing constant current sinking for the display segments. This feature alleviates the problem of achieving uniformity of brightness with unregulated display anode voltage. The National cirucits can drive the displays directly.

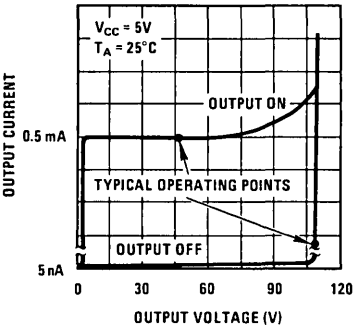
Sperry Information Display* and Burroughs Panaplex II are used principally in calculators and digital instruments. These 7-segment, multi-digit displays form characters by passing controlled currents through the appropriate anode/segment combinations. The cathode in any digit will glow when a voltage greater than the ionization voltage is applied between it (the cathode) and the anode for that digit. In the multiplexed mode of operation, a digit position is selected by driving the anode for that digit with a positive voltage pulse. At the same time, the selected cathode segments are driven with a negative current pulse. This causes the potential between the anode and the selected cathodes to exceed the ionization level, causing a visible glow discharge.

Generally, these displays exhibit the following characteristics: low "on" current per segment—from 200 μA (in DC mode) to 1.2 mA (in multiplex mode); high tube anode supply voltage—180V to 200V; and moderate ionization voltage—170V. Once the element fires, operating voltage drops to approximately 150V and light output becomes a direct function of current, which is controlled by current limiting or current regulating cathode circuits. Current regulation therefore is most desirable since brightness will then be constant for large anode voltage changes. Tube anode to cathode "off" voltage is approximately 100V; and maximum "off" cathode leakage is 3 μA to 5 μA.

Correspondingly, specifications for the cathode driver must be complimentary, approximately as follows: A high "off" output breakdown voltage 80V minimum; typical "on" output voltage of 50V; maximum "on" output current of 1.5 mA per segment; and maximum "off" leakage current of 3 μA to 5 μA.

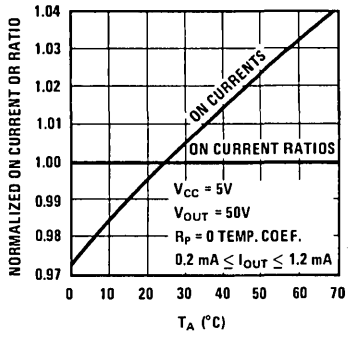
*Now called Beckman Displays

To allow operation without anode voltage regulation, the cathode driver must be able to sink a constant current in each output, with the output "on" voltage ranging from 5V to 50V (see *Figure 1*). The following is a brief description of the circuits now offered by National:



TL/F/5871–1

(a) Cathode Driver Output Characteristic



TL/F/5871–2

(b) On Currents vs Temperature

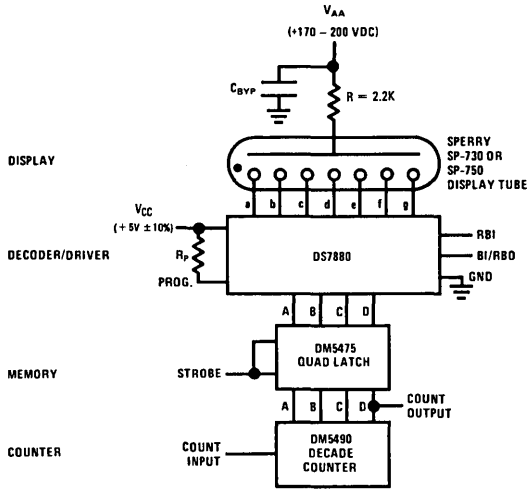
FIGURE 1

DS8880 HIGH VOLTAGE CATHODE DECODER/DRIVER

The DS8880 offers 7-segment outputs with high output breakdown voltage of 80V minimum; constant current-sink outputs; and programmable output current from 0.2 mA to 1.5 mA.

APPLICATION

The circuit has a built-in BCD decoder and can interface directly to Sperry and Panaplex II displays, minimizing external components *(Figure 2)*. The inputs can be driven by TTL or MOS outputs directly. It is optimized for use in systems with 5V supplies.

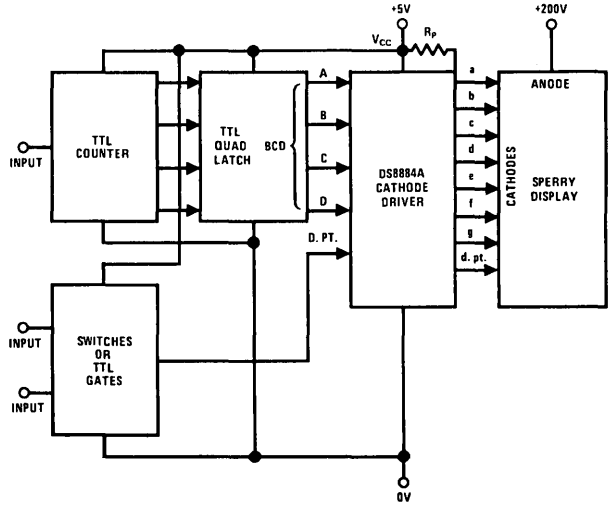


TL/F/5871–3

FIGURE 2. DC Operation From TTL

The DS8880 decoder/driver provides for unconditional as well as leading and trailing zero blanking. It utilizes negative input voltage clamp diodes. Typically, output current varies only 1% for output voltage changes of 3V to 50V. Operating power supply voltage is 5V. The device can be used for multiplexed or DC operation.

Available in 16-pin cavity DIP packages, the DS7880 is guaranteed over the full military operating temperature range of −55°C to +125°C; the DS8880 in molded DIP over the industrial range of 0°C to +70°C.



TL/F/5871–4

FIGURE 3. Interfacing Directly With TTL Output

DS8884A HIGH VOLTAGE CATHODE DECODER/DRIVER

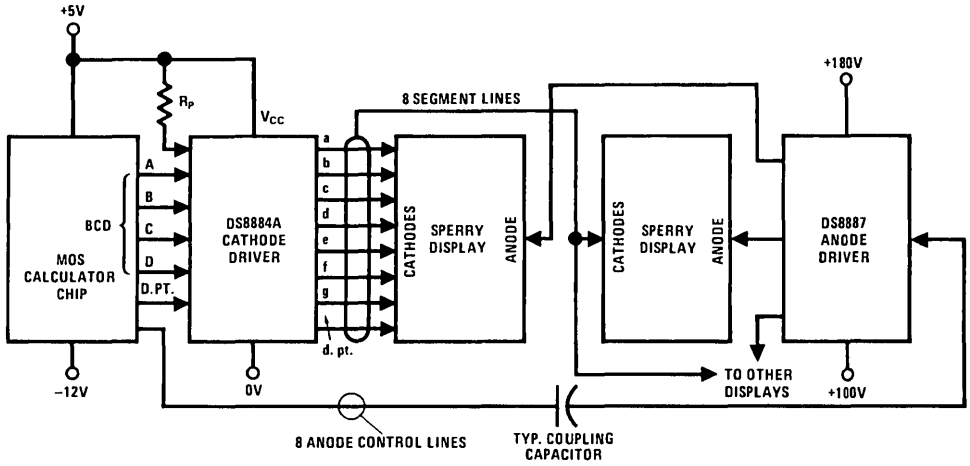
The DS8884A offers 9-segment outputs with high output breakdown voltage of 80V minimum; constant current-sink outputs, programmable from 0.2 mA to 1.2 mA. It also offers input negative and positive voltage clamp diodes for DC restoring, and low input load current of −0.25 mA maximum.

APPLICATION

DS8884A decodes four lines of BCD input and drives 7-segment digits of gas-filled displays. There are two separate inputs and two additional outputs for direct control of decimal point and comma cathodes. The inputs can be DC coupled to TTL *(Figure 3)* or MOS outputs *(Figure 4)*, or AC-coupled to TTL or MOS outputs *(Figure 5)* using only a capacitor. This means the device is useful in applications where level shifting is required. It can be used in multiplexed operation, and is available in an 18-pin molded DIP package.

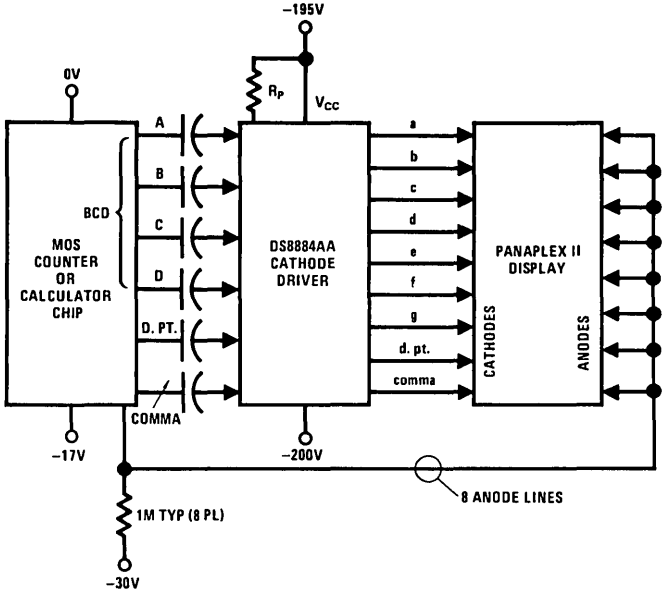
Other advantages of the DS8884A are: typical output current variation of 1% for output voltage changes of 3V to 50V; and operating power supply voltage of 5V. Inputs have pull-up resistors to increase noise immunity in AC coupled applications.

The DS8884A is guaranteed over the 0°C to +70°C operating temperature range.



TL/F/5871–5

FIGURE 4. BCD Data Interfacing Directly With MOS Output



TL/F/5871–6

Note: Capacitive coupling between the logic and the segment drivers may be used only when the segment drivers are turned "OFF" during digit-to-digit transistions.

FIGURE 5. Cathode BCD Data AC Coupled From MOS-Output

Section 5
Memory Support

Section Contents

*Also available processed to various Military screening levels. Refer to Section 9.

Memory Support

MOS memory devices today can be found in a variety of configurations, giving design engineers more flexibility than ever before. National Semiconductor offers a variety of key devices that will allow a user to easily implement memory designs which meet his or her particular requirements.

National's memory support circuits include clock drivers, 4k and 16k RAM address drivers, data I/O circuits, and timing and control drivers. In addition to further information on the specific device types outlined on the next page, a useful application note on "Applying Modern Clock Drivers to MOS Memories", (AN-76) is located at the end of this section.

National Semiconductor Corporation

DP84240/DP84244 Octal TRI-STATE® MOS Drivers

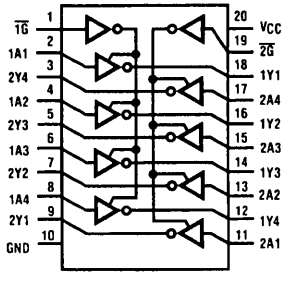
General Description

The DP84240 and DP84244 are octal TRI-STATE drivers which are designed for heavy capacitive load applications such as fast data buffers or as memory address drivers. The DP84240 is an inverting driver which is pin-compatible with both the 74S240 and AM2965. The DP84244 is a non-inverting driver which is pin-compatible with the 74S244 and AM2966. These parts are fabricated using an oxide isolation process, for much faster speeds, and are specified for 250 pF and 500 pF load capacitances.

Features

- t_{pd} specified with 250 pF and 500 pF loads
- Output specified from 0.8V to 2.7V
- Designed for symmetric rise and fall times at 500 pF
- Outputs glitch free at power up and power down
- PNP inputs reduce DC loading on bus lines
- Low static and dynamic input capacitance
- Low skew times between edges and pins
- AC parameters specified with all outputs switching simultaneously

Connection Diagram



TL/F/5219–1

Top View

Order Number DP84240J or DP84240N
See NS Package Numbers J20A or N20A

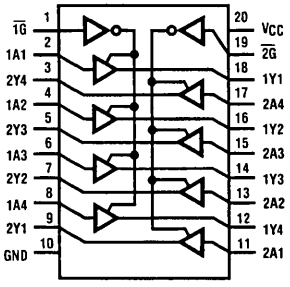
Truth Table

DP84240

Inputs $\overline{G}$	Inputs A	Outputs Y
H	X	Z
L	L	H
L	H	L

H = High Level
L = Low Level
X = Don't Care
Z = High Impedance

DP84244



TL/F/5219–2

Top View

Order Number DP84244J or DP84244N
See NS Package Numbers J20A or N20A

Inputs $\overline{G}$	Inputs A	Outputs Y
H	X	Z
L	L	L
L	H	H

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage, V_{CC}	7.0V
Logical "1" Input Voltage	7.0V
Logical "0" Input Voltage	−1.5V
Storage Temperature Range	−65°C to +150°C
Power Dissipation	
Cavity Package	1150 mW
Molded Package	1300 mW
Lead Temperature (soldering, 10 sec.)	300°C

Operating Conditions

	Min	Max	Units
V_{CC} Supply Voltage	4.5	5.5	V
T_A Ambient Temperature	0	+70	°C

Electrical Characteristics V_{CC} = 5V ±10%, 0 ≤ T_A ≤ 70°C. (Notes 2 and 3.)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$V_{IN(1)}$	Logical "1" Input Voltage		2.0			V
$V_{IN(0)}$	Logical "0" Input Voltage				0.8	V
$I_{IN(1)}$	Logical "1" Input Current	V_{IN} = 2.7V		0.1	20	μA
		V_{IN} = 7.0V			100	μA
$I_{IN(0)}$	Logical "0" Input Current	0 ≤ V_{IN} ≤ 0.4V		−50	−200	μA
V_{CLAMP}	Input Clamp Voltage	I_{IN} = −18 mA		−1	−1.2	V
V_{OH}	Logical "1" Output Voltage	I_{OH} = −100 μA I_{OH} = −1 mA	V_{CC}−1.15 V_{CC} −1.5	4.3 3.9		V
V_{OL}	Logical "0" Output Voltage	I_{OL} = 10 μA I_{OL} = 12 mA		0.2 0.3	0.4 0.5	V
I_{1D}	Logical "1" Drive Current	V_{OUT} = 1.5V	−75	−250		mA
I_{0D}	Logical "0" Drive Current	V_{OUT} = 1.5V	+100	+150		mA
Hi-Z	TRI-STATE Output Current	0.4V ≤ V_{OUT} ≤ 2.7V	−100		+100	μA
I_{CC}	Supply Current DP84240	All Outputs Open All Outputs High All Outputs Low All Outputs Hi-Z		 16 74 80	 50 125 125	mA
	DP84244	All Outputs High All Outputs Low All Outputs Hi-Z		40 100 115	75 130 150	

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All currents into device pins shown as positive; all currents out of device pins shown as negative; all voltages referenced to ground unless otherwise noted. All values shown as max. or min. are on an absolute value basis.

Note 3: Typical characteristics are taken at V_{CC} = 5.0V and T_A = 25°C.

Note 4: The output-to-output skew is primarily a function of the number of outputs switching and the capacitive loading on those outputs. See *Figures 5* and *6* for the switching time variations.

Switching Characteristics V_{CC} = 5V ±10%, 0 ≤ T_A ≤ 70°C, all outputs loaded with specified load capacitance and all eight outputs switching simultaneously. (Note 3.)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
t_{PLH}	Propagation Delay from LOW-to-HIGH Output	*Figures 1 & 3*	CL = 250 pF C_L = 500 pF	9 10	16 20	27 33	ns
t_{PHL}	Propagation Delay from HIGH-to-LOW Output		C_L = 250 pF C_L = 500 pF	9 12	16 20	25 31	ns
t_{PLZ}	Output Disable Time from LOW	*Figures 2 & 4*, S = 1, C_L = 50 pF			11	24	ns
t_{PHZ}	Output Disable Time from HIGH	*Figures 2 & 4*, S = 2, C_L = 50 pF			12	24	ns
t_{PZL}	Output Enable Time to LOW	*Figures 2 & 4*, S = 1, C_L = 500 pF			30	45	ns
t_{PZH}	Output Enable Time to HIGH	*Figures 2 & 4*, S = 2, C_L = 500 pF			23	35	ns
t_{SKEW}	Output-to-Output Skew (Note 4)	*Figures 1 & 3*, C_L = 500 pF			3		ns

Capacitance T_A = 25°C, f = 1 MHz, V_{CC} = 5V ±10%. (Note 3.)

Parameter	Conditions	Typ	Units
C_{IN}	All Other Inputs Tied Low	6	pF
C_{OUT}	Output in TRI-STATE Mode	20	pF

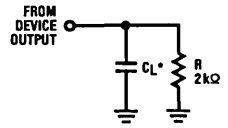
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All currents into device pins shown as positive; all currents out of device pins shown as negative; all voltages referenced to ground unless otherwise noted. All values shown as max. or min. are on an absolute value basis.

Note 3: Typical characteristics are taken at V_{CC} = 5.0V and T_A = 25°C.

Note 4: The output-to-output skew is primarily a function of the number of outputs switching and the capacitive loading on those outputs. See *Figures 5* and *6* for the switching time variations.

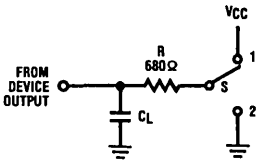
Switching Test Circuits



TL/F/5219–3

*C_L INCLUDES PROBE AND JIG CAPACITANCES

FIGURE 1. Capacitive Load Switching

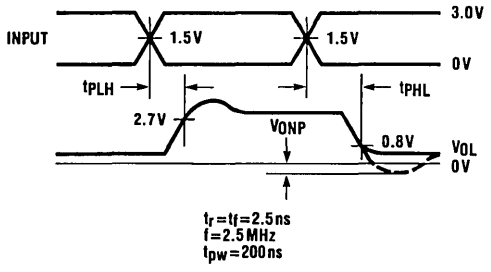


TL/F/5219–4

FIGURE 2. TRI-STATE Enable/Disable

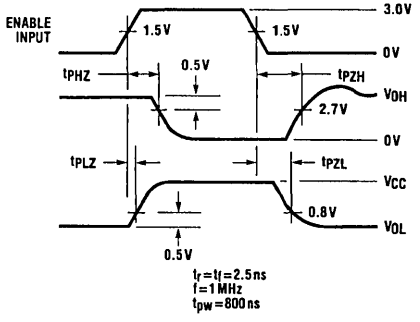
Typical Switching Characteristics

Voltage Waveforms



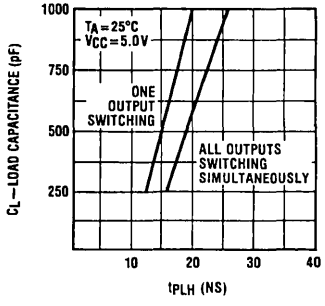
TL/F/5219–5

FIGURE 3. Output Drive Levels



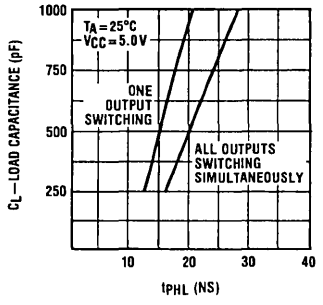
TL/F/5219–6

FIGURE 4. TRI-STATE Control Levels



TL/F/5219–7

FIGURE 5. t_{PLH} Measured to 2.7V on Output vs. C_L

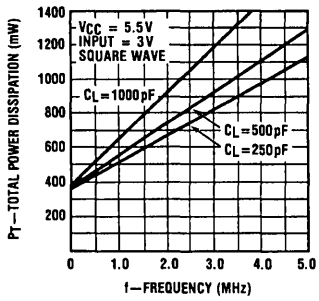


TL/F/5219–8

FIGURE 6. t_{PHL} Measured to 0.8V on Output vs. C_L

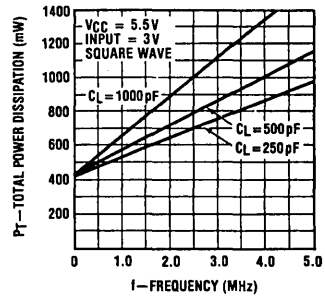
5

Typical Switching Characteristics (Continued)



TL/F/5219–9

FIGURE 7. Typical Power Dissipation for DP84240 at V_{CC} = 5.5V (All 8 drivers switching simultaneously)

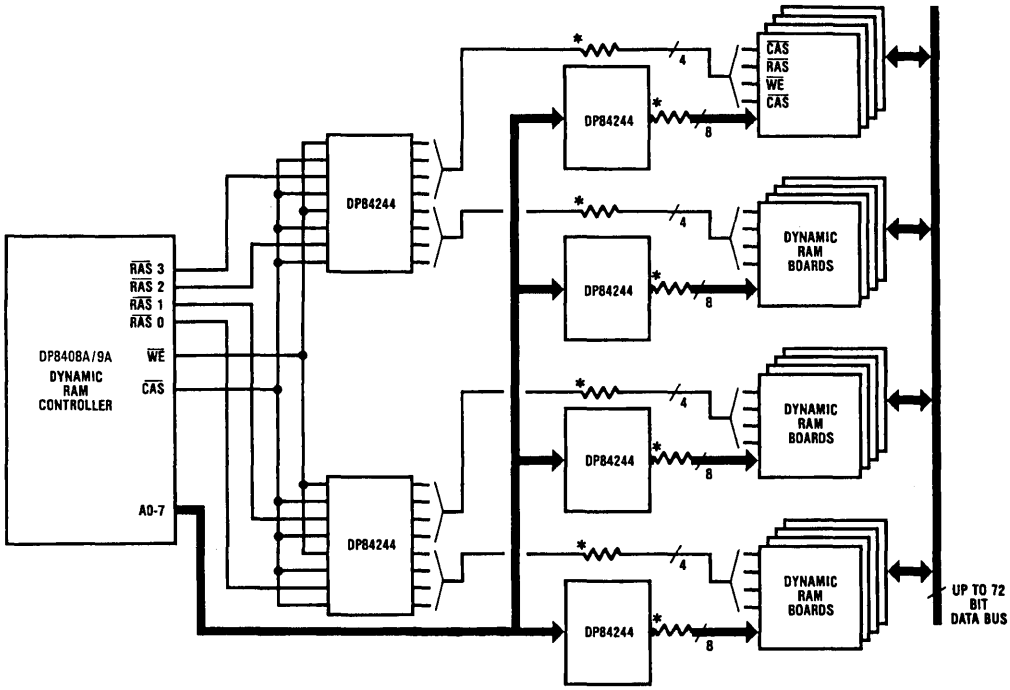


TL/F/5219–10

FIGURE 8. Typical Power Dissipation for DP84244 at V_{CC} = 5.5V (All 8 drivers switching simultaneously)

Typical Application

DP84244 used as a buffer in a large memory array (greater than 88 dynamic RAMs)



TL/F/5219–11

National Semiconductor Corporation

PRELIMINARY

DS0025C Two Phase MOS Clock Driver

General Description

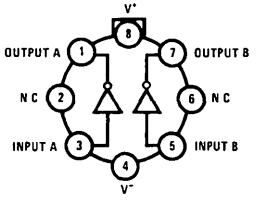
The DS0025C is a monolithic, low cost, two phase MOS clock driver that is designed to be driven by TTL line drivers or buffers such as the DS8830 or DM7440. Two input coupling capacitors are used to perform the level shift from TTL to MOS logic levels. Optimum performance in turn-off delay and fall time are obtained when the output pulse is logically controlled by the input. However, output pulse width may be set by selection of the input capacitor eliminating the need for tight input pulse control.

Features

- 8-lead TO-5 or 8-lead or 14-lead dual-in-line package
- High Output Voltage Swings—up to 25V
- High Output Current Drive Capability—up to 1.5A
- Rep. Rate: 1.0 MHz into > 1000 pF
- Driven by DS8830, DM7440
- "Zero" Quiescent Power

Connection Diagrams

Metal Can Package



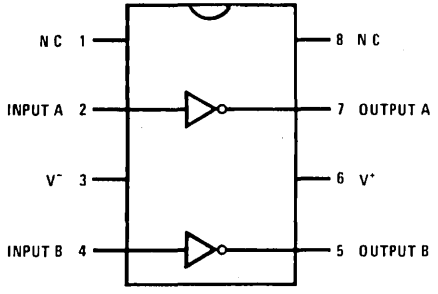
TL/F/5852-1

Note: Pin 4 connected to case.

Top View

Order Number DS0025CH
See NS Package Number H08C

Dual-In-Line Package

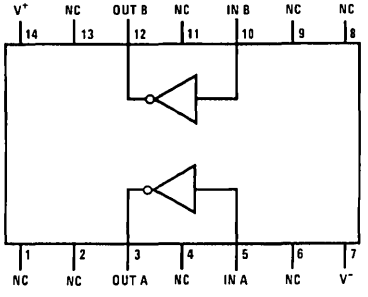


TL/F/5852-2

Top View

Order Number DS0025CJ-8
or DS0025CN
See NS Package Number J08A or N08E

Dual-In-Line Package



TL/F/5852-3

Top View

Order Number DS0025CJ
See NS Package Number J14A

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

$(V^+ - V^-)$Voltage Differential	25V
Input Current	100 mA
Peak Output Current	1.5A
Storage Temperature	−65°C to +150°C
Operating Temperature	0°C to +85°C
Lead Temperature (Soldering, 10 sec)	300°C

Recommended Operating Conditions

V^+ V^- Differential Voltage 20V

	Min	Max
Temperature	0	70
Maximum Power Dissipation* at 25°C		
8-Pin Cavity Package		1150 mW
14-Pin Cavity Package		1410 mW
Molded Package		1080 mW
Metal Can (TO-5) Package		670 mW

* Derate 8-pin cavity package 7.8 mW/°C above 25°C; derate 14-pin cavity package 9.5 mW/°C above 25°C; derate molded package 8.7 mW/°C above 25°C; derate metal can (TO-5) package 4.5 mW/°C above 25°C.

Electrical Characteristics (Notes 2 and 3) See test circuit.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
$t_{d\,ON}$	Turn-On Delay Time	C_{IN} = 0.001 μF, R_{IN} = 0Ω, C_L = 0.001 μF			15	30	ns
t_{RISE}	Rise Time	C_{IN} = 0.001 μF, R_{IN} = 0Ω, C_L = 0.001 μF			25	50	ns
$t_{d\,OFF}$	Turn-Off Delay Time	C_{IN} = 0.001 μF, R_{IN} = 0Ω, C_L = 0.001 μF (Note 4)			30	60	ns
t_{FALL}	Fall Time	C_{IN} = 0.001 μF, R_{IN} = 0Ω, C_L = 0.001 μF	(Note 4)	60	90	120	ns
			(Note 5)	100	150	250	ns
PW	Pulse Width (50% to 50%)	C_{IN} = 0.001 μF, R_{IN} = 0Ω, C_L = 0.001 μF (Note 5)			500		ns
V_{O+}	Positive Output Voltage Swing	V_{IN} = 0V, I_{OUT} = −1 mA		$V^+ - 1.0$	$V^+ - 0.7V$		V
V_{O-}	Negative Output Voltage Swing	I_{IN} = 10 mA, I_{OUT} = 1 mA			$V^- + 0.7V$	$V^- + 1.5V$	V

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

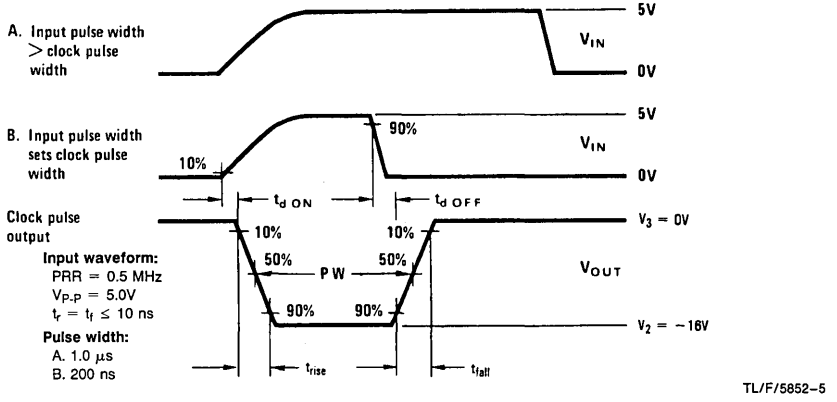
Note 2: Unless otherwise specified min/max limits apply across the 0°C to 70°C range for the DS0025C.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Parameter values apply for clock pulse width determined by input pulse width.

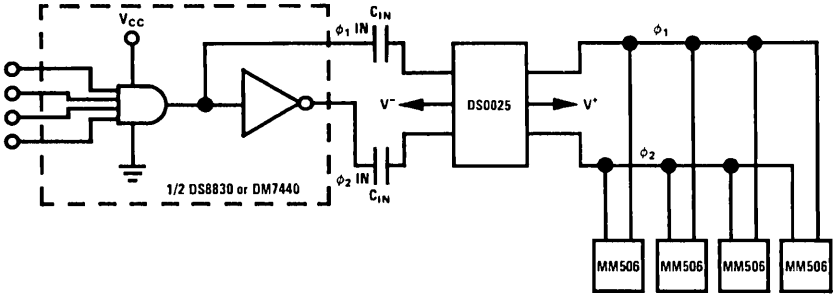
Note 5: Parameter values for input width greater than output clock pulse width.

Timing Diagram



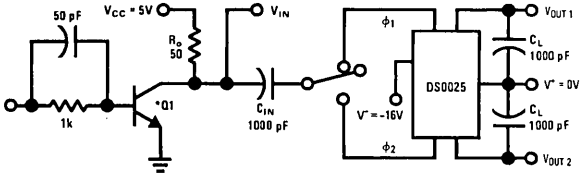
TL/F/5852–5

Typical Application



TL/F/5852–4

AC Test Circuit

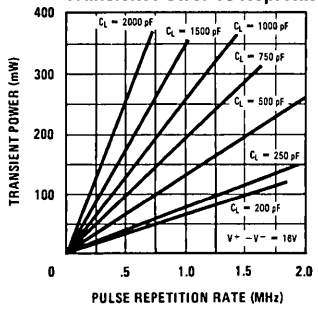


TL/F/5852–6

*Q1 is selected high speed NPN switching transistor.

Typical Performance

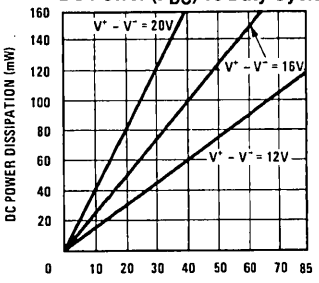
Transient Power vs Rep. Rate



TL/F/5852–7

$$P_{AC} = (V^+ - V^-)^2 f C_L$$

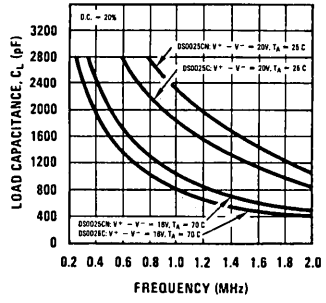
DC Power (P_{DC}) vs Duty Cycle



TL/F/5852–8

$$P_{DC} = \frac{V^+ - V^-)^2 (DC)}{1k}$$

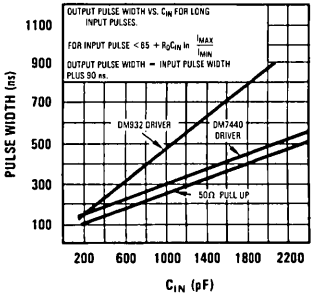
Maximum Load Capacitance



TL/F/5852–9

$$C_L < \frac{(P_{MAX})\,(1k) - (V^+ - V^-)^2\,(DC)}{(f)\,(1k)\,(V^+ - V^-)^2} < \frac{(I_{pk})\,(t_r)}{V^+ - V^-}$$

Output PW Controlled by C_{IN}



TL/F/5852–10

I_{MAX} = Peak Current delivered by driver

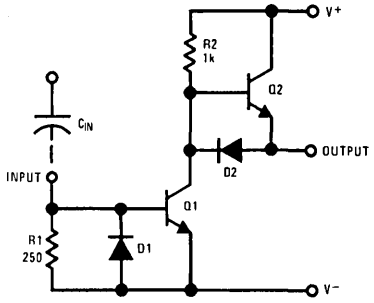
$$I_{MIN}\,\frac{V_{BE}}{R1} = \frac{0.6}{1k}$$

Applications Information

Circuit Operation

Input current forced into the base of Q_1 through the coupling capacitor C_{IN} causes Q_1 to be driven into saturation, swinging the output to $V^- + V_{CE}(sat) + V_{Diode}$.

When the input current has decayed, or has been switched, such that Q_1 turns off, Q_2 receives base drive through R_2, turning Q_2 on. This supplies current to the load and the output swings positive to $V^+ - V_{BE}$.



TL/F/5852–11

FIGURE 1. DS0025 Schematic (One-Half Circuit)

It may be noted that Q_1 must switch off before Q_2 begins to supply current, hence high internal transients currents from V^- to V^+ cannot occur.

Fan-Out Calculation

The drive capability of the DS0025 is a function of system requirements, i.e. speed, ambient temperature, voltage swing, drive circuitry, and stray wiring capacity.

The following equations cover the necessary calculations to enable the fan-out to be calculated for any system condition.

Transient Current

The maximum peak output current of the DS0025 is given as 1.5A. Average transient current required from the driver can be calculated from:

$$I = \frac{C_L (V^+ - V^-)}{t_r} \quad (1)$$

Typical rise times into 1000 pF load is 25 ns. For $V^+ - V^- = 20V$, $I = 0.8A$.

Transient Output Power

The average transient power (P_{ac}) dissipated, is equal to the energy needed to charge and discharge the output capacitive load (C_L) multiplied by the frequency of operation (f).

$$P_{AC} = C_L \times (V^+ - V^-)^2 \times f \quad (2)$$

For $V^+ - V^- = 20V$, $f = 1.0$ MHz, $C_L = 1000$ pF, $P_{AC} = 400$ mW.

Internal Power

"0" State Negligible (<3 mW)

"1" State

$$P_{int} = \frac{(V^+ - V^-)^2}{R_2} \times \text{Duty Cycle} \quad (3)$$

$= 80$ mW for $V^+ - V^- = 20V$, DC = 20%

Package Power Dissipation

Total average power = transient output power + internal power.

Example Calculation

How many MM506 shift registers can be driven by a DS0025CN driver at 1 MHz using a clock pulse width of 200 ns, rise time 30–50 ns and 16V amplitude over the temperature range 0°–70°C?

Power Dissipation:

At 70°C the DS0025CN can dissipate 870 mW when soldered into printed circuit board.

Transient Peak Current Limitation:

From equation (1), it can be seen that at 16V and 30 ns, the maximum load that can be driven is limited to 2800 pF.

Average Internal Power:

Equation (3), gives an average power of 50 mW at 16V and a 20% duty cycle.

For one-half of the DS0025C, 870 mW ÷ 2 can be dissipated.

435 mW = 50 mW + transient output power.

385 mW = transient output power.

Using equation (2) at 16V, 1 MHz and 350 mW, each half of the DS0025CN can drive a 1367 pF load. This is less than the load imposed by the transient current limitation of equation (1) and so a maximum load of 1367 pF would prevail.

From the data sheet for the MM506, the average clock pulse load is 80 pF. Therefore the number of devices driven is 1367/80 or 17 registers.

For further information please refer to National Semiconductors Application Note AN-76.

National Semiconductor Corporation

DS0026/DS0056 5 MHz Two Phase MOS Clock Drivers

General Description

DS0026/DS0056 are low cost monolithic high speed two phase MOS clock drivers and interface circuits. Unique circuit design provides both very high speed operation and the ability to drive large capacitive loads. The device accepts standard TTL outputs and converts them to MOS logic levels. They may be driven from standard 54/74 series and 54S/74S series gates and flip-flops or from drivers such as the DS8830 or DM7440. The DS0026 and DS0056 are intended for applications in which the output pulse width is logically controlled; i.e., the output pulse width is equal to the input pulse width.

The DS0026/DS0056 are designed to fulfill a wide variety of MOS interface requirements. As a MOS clock driver for long silicon-gate shift registers, a single device can drive over 10k bits at 5 MHz. Six devices provide input address and precharge drive for a 8k by 16-bit 1103 RAM memory system. Information on the correct usage of the DS0026 in these as well as other systems is included in the application note AN-76.

The DS0026 and DS0056 are identical except each driver in the DS0056 is provided with a V_{BB} connection to supply a higher voltage to the output stage. This aids in pulling up the output when it is in the high state. An external resistor tied between these extra pins and a supply higher than V^+ will cause the output to pull up to ($V^+ - 0.1V$) in the off state.

For DS0056 applications, it is required that an external resistor be used to prevent damage to the device when the driver switches low. A typical V_{BB} connection is shown on the next page.

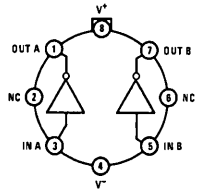
These devices are available in 8-lead TO-5, one watt copper lead frame 8-pin mini-DIP, and one and a half watt ceramic DIP, and TO-8 packages.

Features

- Fast rise and fall times—20 ns 1000 pF load
- High output swing—20V
- High output current drive—±1.5 amps
- TTL compatible inputs
- High rep rate—5 to 10 MHz depending on power dissipation
- Low power consumption in MOS "0" state—2 mW
- Drives to 0.4V of GND for RAM address drive

Connection Diagrams (Top Views)

TO-5 Package

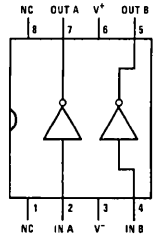


TL/F/5853-1

Note: Pin 4 connected to case.

Order Number DS0026H or DS0026CH See NS Package Number H08C

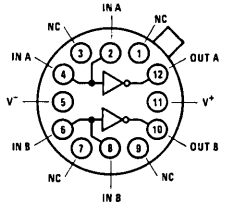
Dual-In-Line Package



TL/F/5853-2

Order Number DS0026CJ-8, or DS0026CN See NS Package Number J08A or N08E

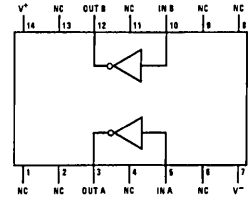
TO-8 Package



TL/F/5853-3

Order Number DS0026G or DS0026CG See NS Package Number G12C

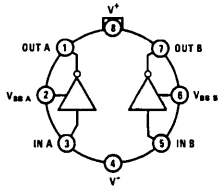
Dual-In-Line Package



TL/F/5853-4

Order Number DS0026J or DS0026CJ See NS Package Number J14A

TO-5 Package

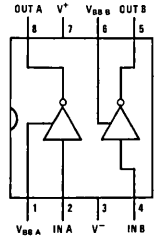


TL/F/5853-5

Note: Pin 4 connected to case.

Order Number DS0056H or DS0056CH See NS Package Number H08C

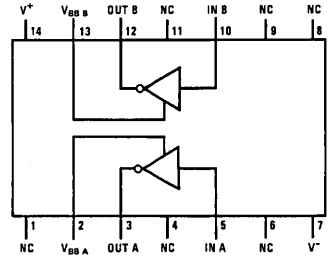
Dual-In-Line Package



TL/F/5853-6

Order Number DS0056J-8, DS0056CJ-8 or DS0056CN See NS Package Number J08A or N08E

Dual-In-Line Package



TL/F/5853-7

Order Number DS0056J or DS0056CJ See NS Package Number J14A

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

$V^+ - V^-$ Differential Voltage	22V
Input Current	100 mA
Input Voltage ($V_{IN} - V^-$)	5.5V
Peak Output Current	1.5A
Maximum Power Dissipation* at 25°C	
Cavity Package (8-Pin)	1150 mW
Cavity Package (14-Pin)	1380 mW
Molded Package	1040 mW
Metal Can (TO-5)	660 mW
Operating Temperature Range	
DS0026, DS0056	−55°C to +125°C
DS0026C, DS0056C	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	300°C

* Derate 8-pin cavity package 7.7 mW/°C above 25°C; derate 14-pin cavity package 9.3 mW/°C above 25°C; derate molded package 8.4 mW/°C above 25°C; derate metal can (TO-5) package 4.4 mW/°C above 25°C.

Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IH}	Logic "1" Input Voltage	$V^- = 0V$		2	1.5		V
I_{IH}	Logic "1" Input Current	$V_{IN} - V^- = 2.4V$			10	15	mA
V_{IL}	Logic "0" Input Voltage	$V^- = 0V$			0.6	0.4	V
I_{IL}	Logic "0" Input Current	$V_{IN} - V^- = 0V$			−3	−10	μA
V_{OL}	Logic "1" Output Voltage	$V_{IN} - V^- = 2.4V$, $I_{OL} = 1$ mA			$V^- + 0.7$	$V^- + 1.0$	V
V_{OH}	Logic "0" Output Voltage	$V_{IN} - V^- = 0.4V$, $V_{SS} \geq V^+ + 1.0V$, $I_{OH} = -1$ mA	DS0026	$V^+ - 1.0$	$V^+ - 0.8$		V
			DS0056	$V^+ - 0.3$	$V^+ - 0.1$		V
$I_{CC(ON)}$	"ON" Supply Current (one side on)	$V^+ - V^- = 20V$, $V_{IN} - V^- = 2.4V$ (Note 6)	DS0026		30	40	mA
			DS0056		12	30	mA
$I_{CC(OFF)}$	"OFF" Supply Current	$V^+ - V^- = 20V$, $V_{IN} - V^- = 0V$	70°C		10	100	μA
			125°C		10	500	μA

Switching Characteristics ($T_A = 25°C$) (Notes 5 and 7)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
t_{ON}	Turn-On Delay	*(Figure 1)*		5	7.5	12	ns
		(Figure 2)			11		ns
t_{OFF}	Turn-Off Delay	*(Figure 1)*			12	15	ns
		(Figure 2)			13		ns
t_r	Rise Time	*(Figure 1)*, (Note 5)	$C_L = 500$ pF		15	18	ns
			$C_L = 1000$ pF		20	35	ns
		(Figure 2), (Note 5)	$C_L = 500$ pF		30	40	ns
			$C_L = 1000$ pF		36	50	ns
t_f	Fall Time	*(Figure 1)*, (Note 5)	$C_L = 500$ pF		12	16	ns
			$C_L = 1000$ pF		17	25	ns
		(Figure 2), (Note 5)	$C_L = 500$ pF		28	35	ns
			$C_L = 1000$ pF		31	40	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics provides conditions for actual device operation.

Note 2: These specifications apply for $V^+ - V^- = 10V$ to 20V, $C_L = 1000$ pF, over the temperature range of −55°C to +125°C for the DS0026, DS0056 and 0°C to +70°C for the DS0026C, DS0056C.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

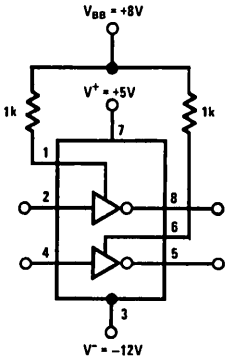
Note 4: All typical values for $T_A = 25°C$.

Note 5: Rise and fall time are given for MOS logic levels; i.e., rise time is transition from logic "0" to logic "1" which is voltage fall.

Note 6: I_{BB} for DS0056 is approximately $(V_{BB} - V^-)/1$ kΩ (for one side) when output is low.

Note 7: The high current transient (as high as 1.5A) through the resistance of the internal interconnecting V^- lead during the output transition from the high state to the low state can appear as negative feedback to the input. If the external interconnecting lead from the driving circuit to V^- is electrically long, or has significant dc resistance, it can subtract from the switching response.

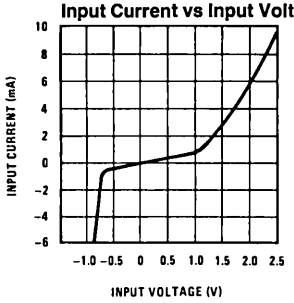
Typical V_{BB} Connection



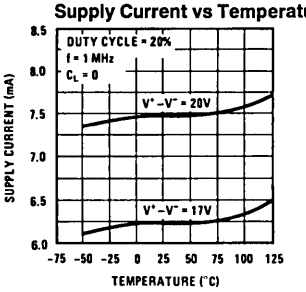
TL/F/5853–8

Typical Performance Characteristics

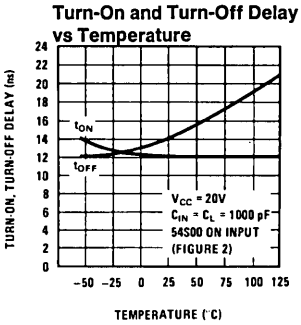
Input Current vs Input Voltage



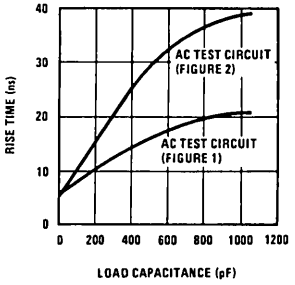
Supply Current vs Temperature



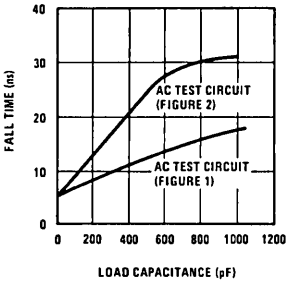
Turn-On and Turn-Off Delay vs Temperature



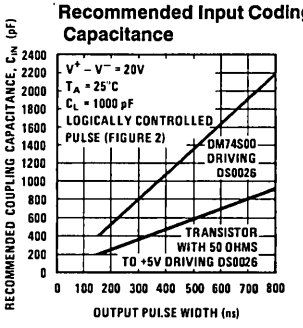
Rise Time vs Load Capacitance



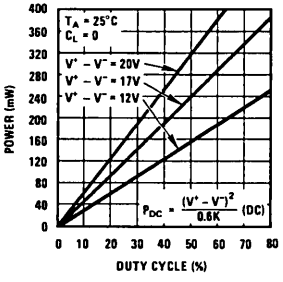
Fall Time vs Load Capacitance



Recommended Input Coding Capacitance



DC Power (P_{DC}) vs Duty Cycle

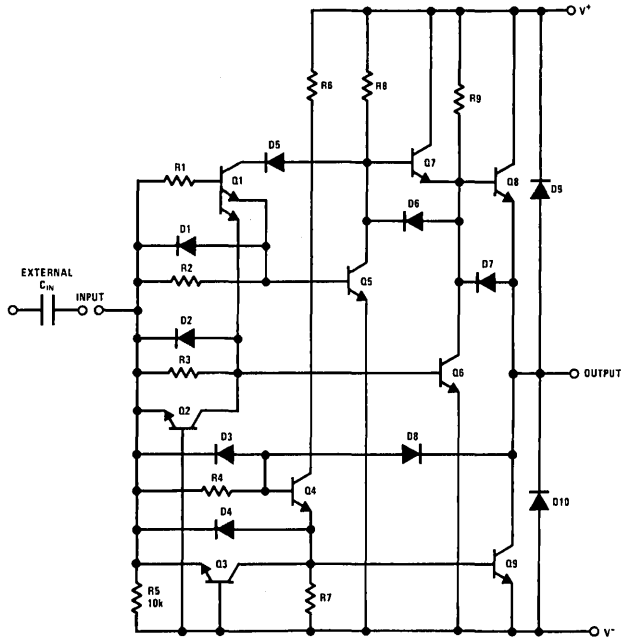


TL/F/5853–9

5

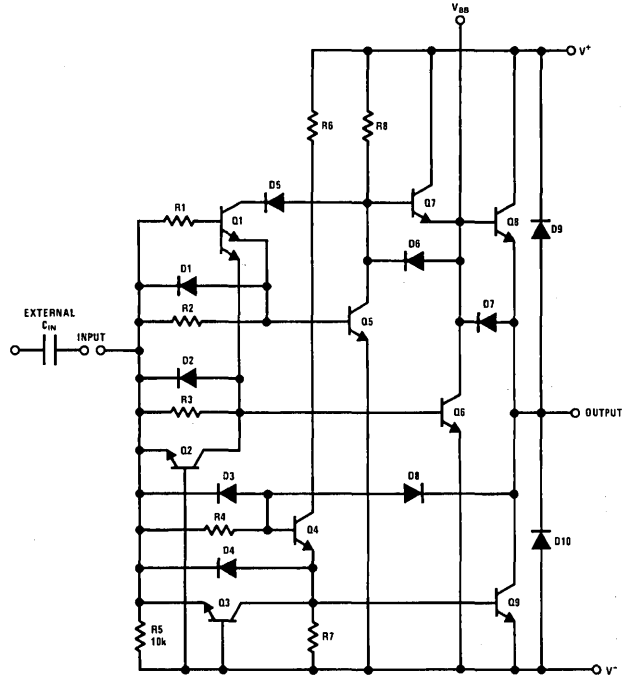
Schematic Diagrams

1/2 DS0026



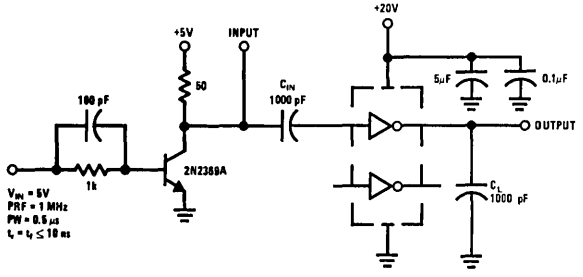
TL/F/5853–10

1/2 DS0056

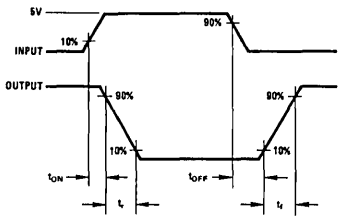


TL/F/5853–11

AC Test Circuits and Switching Time Waveforms

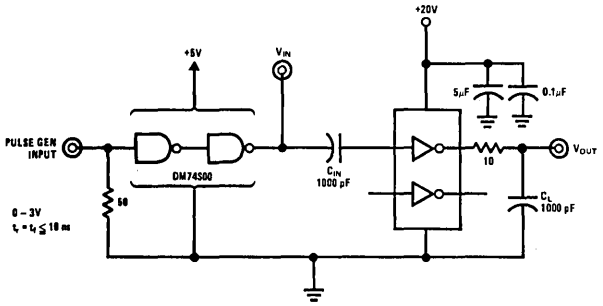


TL/F/5853–12

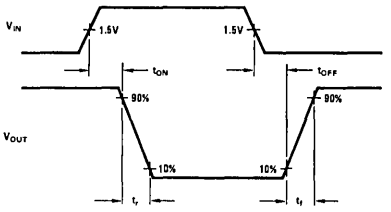


TL/F/5853–13

FIGURE 1



TL/F/5853–14

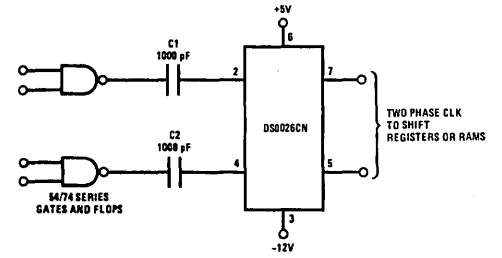


TL/F/5853–15

FIGURE 2

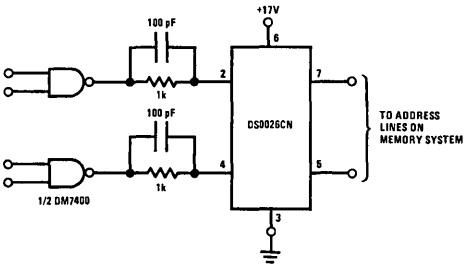
Typical Applications

AC Coupled MOS Clock Driver



TL/F/5853–16

DC Coupled RAM Memory Address or Precharge Driver (Positive Supply Only)



TL/F/5853–17

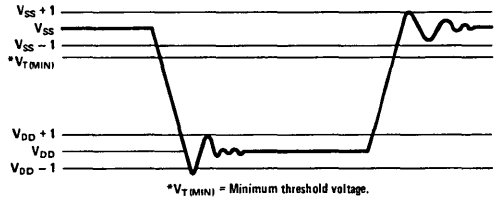
Application Hints

DRIVING THE MM5262 WITH THE DS0056 CLOCK DRIVER

The clock signals for the MM5262 have three requirements which have the potential of generating problems for the user. These requirements, high speed, large voltage swing and large capacitive loads, combine to provide ample opportunity for inductive ringing on clock lines, coupling clock signals to other clocks and/or inputs and outputs and generating noise on the power supplies. All of these problems have the potential of causing the memory system to malfunction. Recognizing the source and potential of these problems early in the design of a memory system is the most critical step. The object here is to point out the source of these problems and give a quantitative feel for their magnitude.

Application Hints (Continued)

Line ringing comes from the fact that at a high enough frequency any line must be considered as a transmission line with distributed inductance and capacitance. To see how much ringing can be tolerated we must examine the clock voltage specification. *Figure 6* shows the clock specification, in diagram form, with idealized ringing sketched in. The



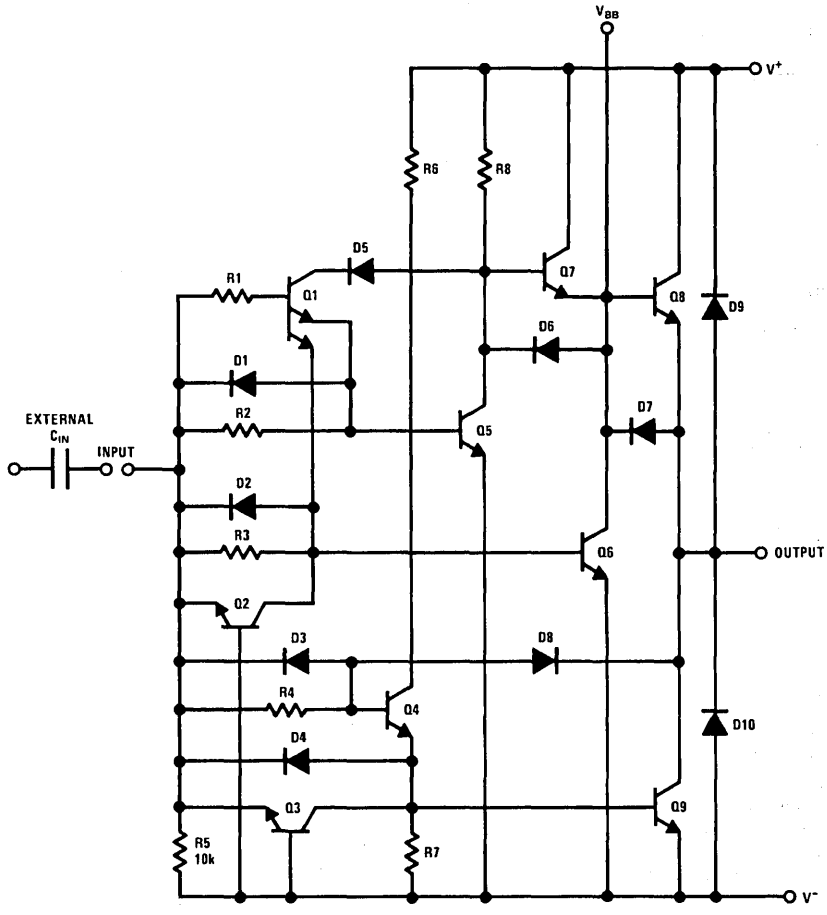
TL/F/5853–18

FIGURE 6. Clock Waveform

ringing of the clock about the V_{SS} level is particularly critical. If the $V_{SS} - 1$ V_{OH} is not maintained, at *all* times, the information stored in the memory could be altered. Referring to *Figure 1*, if the threshold voltage of a transistor were −1.3V, the clock going to $V_{SS} - 1$ would mean that all the devices, whose gates are tied to that clock, would be only 300 mV from turning on. The internal circuitry needs this noise margin and from the functional description of the RAM it is easy to see that turning a clock on at the wrong time can have disastrous results.

Controlling the clock ringing is particularly difficult because of the relative magnitude of the allowable ringing, compared to magnitude of the transition. In this case it is 1V out of 20V or only 5%. Ringing can be controlled by damping the clock driver and minimizing the line inductance.

Damping the clock driver by placing a resistance in series with its output is effective, but there is a limit since it also slows down the rise and fall time of the clock signal. Because the typical clock driver can be much faster than the worst case driver, the damping resistor serves the useful function of limiting the minimum rise and fall time. This is very important because the faster the rise and fall times, the worse the ringing problem becomes. The size of the damp-



TL/F/5853–11

FIGURE 7. Schematic of 1/2 DS0056

Application Hints (Continued)

ing resistor varies because it is dependent on the details of the actual application. It must be determined empirically. In practice a resistance of 10Ω to 20Ω is usually optimum.

Limiting the inductance of the clock lines can be accomplished by minimizing their length and by laying out the lines such that the return current is closely coupled to the clock lines. When minimizing the length of clock lines it is important to minimize the distance from the clock driver output to the furthest point being driven. Because of this, memory boards are usually designed with clock drivers in the center of the memory array, rather than on one side, reducing the maximum distance by a factor of 2.

Using multilayer printed circuit boards with clock lines sandwiched between the V_{DD} and V_{SS} power plains minimizes the inductance of the clock lines. It also serves the function of preventing the clocks from coupling noise into input and output lines. Unfortunately multilayer printed circuit boards are more expensive than two sided boards. The user must make the decision as to the necessity of multilayer boards. Suffice it to say here, that reliable memory boards can be designed using two sided printed circuit boards.

The recommended clock driver for use with the MM4262/MM5262 is the DS0056/DS0056C dual clock driver. This device is designed specifically for use with dynamic circuits using a substrate, V_{BB}, supply. Typically it will drive a 1000 pF load with 20 ns rise and fall times. *Figure 7* shows a schematic of a single driver.

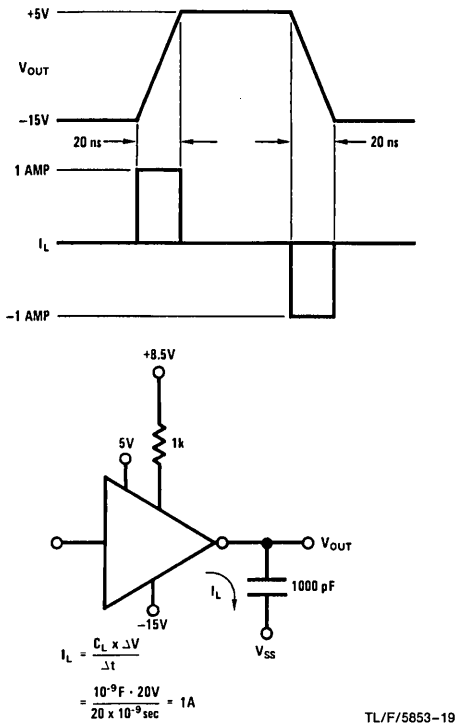
In the case of the MM5262, V^+ is a +5V and V_{BB} is +8.5V. V_{BB} should be connected to the V_{BB} pin shown in *Figure 7* through a 1 kΩ resistor. This allows transistor Q8 to saturate, pulling the output to within a $V_{CE(SAT)}$ of the V^+ supply. This is critical because as was shown before, the V_{SS} − 1.0V clock level must not be exceeded at any time. Without the V_{BB} pull up on the base of Q8 the output at best will be 0.6V below the V^+ supply and can be 1V below the V^+ supply reducing the noise margin on this line to zero.

Because of the amount of current that the clock driver must supply to its capacitive load, the distribution of power to the clock driver must be considered. *Figure 8* gives the idealized voltage and current waveforms for a clock driver driving a 1000 pF capacitor with 20 ns rise and fall time.

As can be seen the current is significant. This current flows in the V_{DD} and V_{SS} power lines. Any significant inductance in the lines will produce large voltage transients on the power supplies. A bypass capacitor, as close as possible to the clock driver, is helpful in minimizing this problem. This bypass is most effective when connected between the V_{SS} and V_{DD} supplies. A bypass capacitor for each DS0056 is recommended. The size of the bypass capacitor depends on the amount of capacitance being driven. Using a low inductance capacitor, such as a ceramic or silver mica, is most effective. Another helpful technique is to run the V_{DD} and V_{SS} lines, to the clock driver, adjacent to each other. This tends to reduce the lines inductance and therefore the magnitude of the voltage transients.

While discussing the clock driver, it should be pointed out that the DS0056 is a relatively low input impedance device. It is possible to couple current noise into the input without seeing a significant voltage. Since the noise is difficult to detect with an oscilloscope it is often overlooked.

Lastly, the clock lines must be considered as noise generators. *Figure 9* shows a clock coupled through a parasitic coupling capacitor, C_C, to eight data input lines being driven by a 7404. A parasitic lumped line inductance, L, is also shown. Let us assume, for the sake of argument, that C_C is 1 pF and that the rise time of the clock is high enough to completely isolate the clock transient from the 7404 because of the inductance, L.



TL/F/5853–19

FIGURE 8. Clock Waveforms (Voltage and Current)

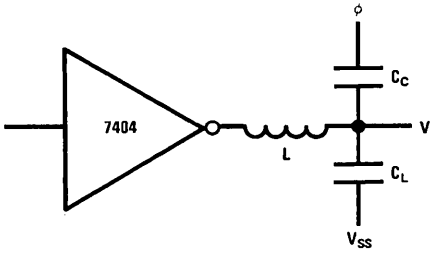


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FIGURE 9. Clock Coupling

With a clock transition of 20V the magnitude of the voltage generated across C_L is:

$$V = 20V \times \frac{C_C}{C_L + C_C} = 20V \times \left(\frac{1}{56+1}\right) = 0.35V$$

This has been a hypothetical example to emphasize that with 20V low rise/fall time transitions, parasitic elements can not be neglected. In this example, 1 pF of parasitic capacitance could cause system malfunction, because a 7404 without a pull up resistor has typically only 0.3V of

Application Hints (Continued)

noise margin in the "1" state at 25°C. Of course it is stretching things to assume that the inductance, L, completely isolates the clock transient from the 7404. However, it does point out the need to minimize inductance in input/output as well as clock lines.

The output is current, so it is more meaningful to examine the current that is coupled through a 1 pF parasitic capacitance. The current would be:

$$I = C_C \times \frac{\Delta V}{\Delta t} = \frac{1 \times 10^{-12} \times 20}{20 \times 10^{-9}} = 1\ mA$$

This exceeds the total output current swing so it is obviously significant.

Clock coupling to inputs and outputs can be minimized by using multilayer printed circuit boards, as mentioned previously, physically isolating clock lines and/or running clock lines at right angles to input/output lines. All of these techniques tend to minimize parasitic coupling capacitance from the clocks to the signals in question.

In considering clock coupling it is also important to have a detailed knowledge of the functional characteristics of the device being used. As an example, for the MM5262, coupling noise from the $\phi 2$ clock to the address lines is of no particular consequence. On the other hand the address inputs will be sensitive to noise coupled from $\phi 1$ clock.

National Semiconductor Corporation

DS3245 Quad MOS Clock Driver

General Description

The DS3245 is a quad bipolar-to-MOS clock driver with TTL compatible inputs. It is designed to provide high output current and voltage capabilities necessary for optimum driving of high capacitance N-channel MOS memory systems.

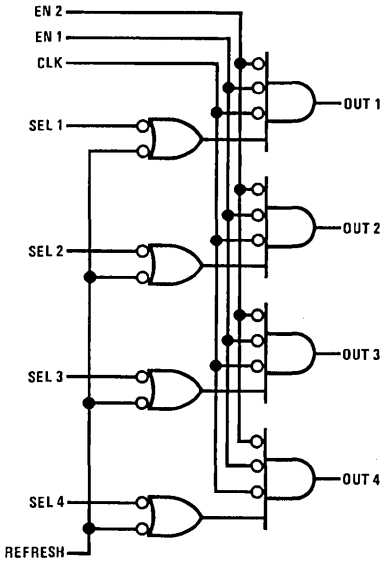
Only 2 supplies, 5 V_{DC} and 12 V_{DC}, are required without compromising the usual high V_{OH} specification obtained by circuits using a third supply.

The device features 2 common enable inputs, a refresh input, and a clock control input for simplified system designs. The circuit was designed for driving highly capacitive loads at high speeds and uses Schottky-clamped transistors. PNP transistors are used on all inputs, thereby minimizing input loading.

Features

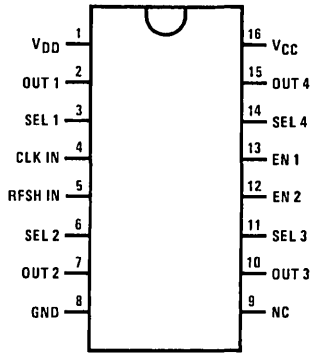
- TTL compatible inputs
- Operates from 2 standard supplies: 5 V_{DC}, 12 V_{DC}
- Internal bootstrap circuit eliminates need for external PNP's
- PNP inputs minimize loading
- High voltage/current outputs
- Input and output clamping diodes
- Control logic optimized for use with MOS memory systems
- Pin and function equivalent to Intel 3245

Logic and Connection Diagrams



TL/F/5873–1

Dual-In-Line Package



TL/F/5873–2

Top View

Order Number DS3245J or DS3245N
See NS Package Number J16A or N16A

5

Absolute Maximum Ratings

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Temperature Under Bias	−10°C to +85°C
Storage Temperature	−65°C to +150°C
Supply Voltage, V_{CC}	−0.5V to +7V
Supply Voltage, V_{DD}	−0.5V to +14V
All Input Voltages	−1.0V to V_{DD}
Outputs for Clock Driver	−1.0V to V_{DD} + 1V
Maximum Power Dissipation* at 25°C	
Cavity Package	1509 mW
Molded Package	1476 mW

*Derate cavity package 10.1 mW/°C above 25°C; derate molded package 11.8 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage, V_{CC}	4.75	5.25	V
Supply Voltage, V_{DD}	11.4	12.6	V
Operating Temperature $9T_A$	0	75	°C

Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{FD}	Select Input Load Current	V_F = 0.45V			−0.25	mA
I_{FE}	Enable Input Load Current	V_F = 0.45V			−1.0	mA
I_{RD}	Select Input Leakage Current	V_R = 5V			10	μA
I_{RE}	Enable Input Leakage Current	V_R = 5V			40	μA
V_{OL}	Output Low Voltage	I_{OL} = 5 mA, V_{IH} = 2V			0.45	V
		I_{OL} = −5 mA	−1.0			V
V_{OH}	Output High Voltage	I_{OH} = −1 mA, V_{IL} = 0.8V	V_{DD} − 0.50			V
		I_{OH} = 5 mA			V_{DD} + 1.0	V
V_{IL}	Input Low Voltage, All Inputs				0.8	V
V_{IH}	Input High Voltage, All Inputs		2			V
V_{CLAMP}	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −12 mA		−1.0	−1.5	V

Power Supply Current Drain

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{CC}	Current from V_{CC} Output in High State	V_{CC} = 5.25V, V_{DD} = 12.6V		26	34	mA
I_{DD}	Current from V_{DD} Output in High State	V_{CC} = 5.25V, V_{DD} = 12.6V		23	30	mA
I_{CC}	Current from V_{CC} Output in Low State	V_{CC} = 5.25V, V_{DD} = 12.6V		29	39	mA
I_{DD}	Current from V_{DD} Output in Low State	V_{CC} = 5.25V, V_{DD} = 12.6V		13	19	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +°C range. All typical values are for T_A = 25°C and V_{CC} = 5V and V_{DD} = 12V.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Switching Characteristics $T_A = 0°C$ to $+75°C$, $V_{CC} = 5V \pm 5\%$, $V_{DD} = 12V \pm 5\%$

Symbol	Parameter	Conditions	Min(1)	Typ(2,4)	Max(3)	Units
t_{-+}	Input to Output Delay	$R_{SERIES} = 0$	5	11		ns
t_{DR}	Delay Plus Rise Time	$R_{SERIES} = 0$		20	32	ns
t_{+-}	Input to Output Delay	$R_{SERIES} = 0$	3	7		ns
t_{DF}	Delay Plus Fall Time	$R_{SERIES} = 0$		18	32	ns
t_T	Output Transition Time	$R_{SERIES} = 20\Omega$	10	17	25	ns
t_{DR}	Delay Plus Rise Time	$R_{SERIES} = 20\Omega$		27	38	ns
t_{DF}	Delay Plus Fall Time	$R_{SERIES} = 20\Omega$		25	38	ns

Capacitance $T_A = 25°C$(5)

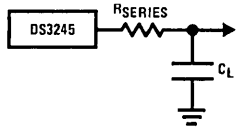
Symbol	Parameter	Conditions	Min	Typ	Max	Units
C_{IN}	Input Capacitance, $\overline{I_1}$, $\overline{I_2}$, $\overline{I_3}$, $\overline{I_4}$			5	8	pF
C_{IN}	Input Capacitance, $\overline{R}$, $\overline{C}$, $\overline{E1}$, $\overline{E2}$			8	12	pF

Note 1: $C_L = 150$ pF
Note 2: $C_L = 200$ pF
Note 3: $C_L = 250$ pF
} These values represent a range of total stray plus clock capacitance for nine 4k RAMs.

Note 4: Typical values are measured at 25°C.

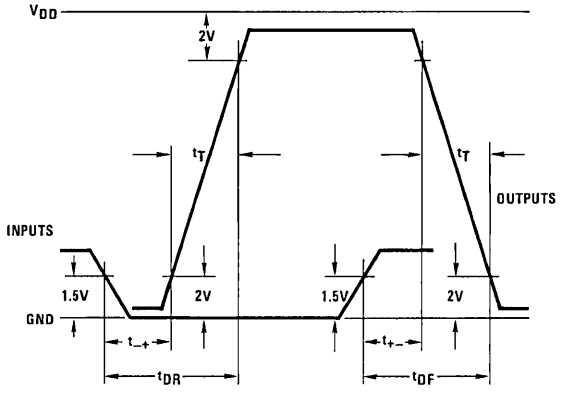
Note 5: This parameter is periodically sampled and is not 100% tested. Condition of measurement is f = 1 MHz, $V_{BIAS} = 2V$, $V_{CC} = 0V$, and $T_A = 25°C$.

AC Test Circuit and Switching Time Waveforms



Input pulse amplitudes: 3V
Input pulse rise and fall times:
5 ns between 1V and 2V
Measurements points: see waveforms

TL/F/5873-3



TL/F/5873-4

National Semiconductor Corporation

DS1628/DS3628 Octal TRI-STATE® MOS Drivers

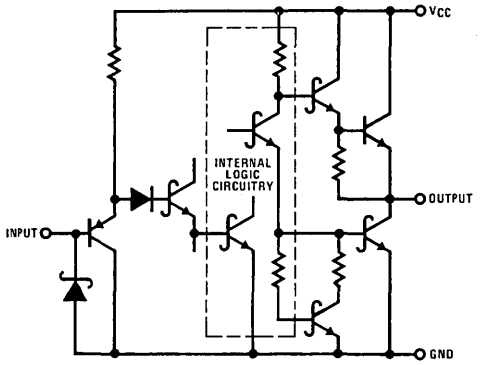
General Description

The DS1628/DS3628 are octal Schottky memory drivers with TRI-STATE outputs designed to drive high capacitive loads associated with MOS memory systems. The drivers' output (V_{OH}) is specified at 3.4V to provide additional noise immunity required by MOS inputs. A PNP input structure is employed to minimize input currents. The circuit employs Schottky-clamped transistors for high speed. A NOR gate of two inputs, DIS1 and DIS2, controls the TRI-STATE mode.

Features

- High speed capabilities
  - Typical 5 ns driving 50 pF & 8 ns driving 500 pF
- TRI-STATE outputs
- High V_{OH} (3.4V min)
- High density
  - Eight drivers and two disable controls for TRI-STATE in a 20-pin package
- PNP inputs reduce DC loading on bus lines
- Glitch-free power up/down

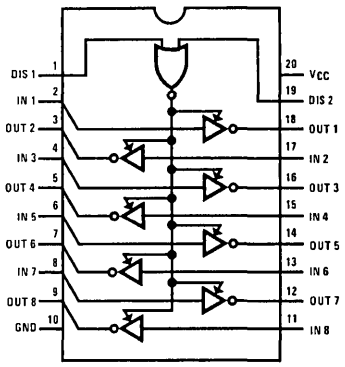
Schematic and Connection Diagrams



TL/F/5875–1

(Equivalent Input/Output Circuit)

Dual-In-Line Package



Top View

TL/F/5875–2

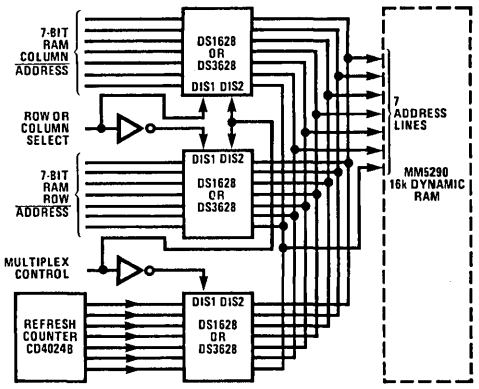
Order Number
DS1628J, DS3628J, DS3628N
See NS Package Number J20A or N20A

Truth Table

Disable Input		Input	Output
DIS 1	DIS 2		
H	H	X	Z
H	X	X	Z
X	H	X	Z
L	L	H	L
L	L	L	H

H = high level
L = low level
X = don't care
Z = high impedance (off)

Typical Application



TL/F/5875–3

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7.0V
Logical "1" Input Voltage	7.0V
Logical "0" Input Voltage	−1.5V
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1667 mW
Molded Package	1832 mW
Lead Temperature (Soldering, 10 seconds)	300°C

*Derate cavity package 11.1 mW/°C above 25°C; derate molded package 14.7 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply voltage (V_{CC})	4.5	5.5	V
Temperature (T_A)			
DS1628	−55	+125	°C
DS3628	0	+70	°C

Electrical Characteristics (Notes 2, 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
$V_{IN(1)}$	Logical "1" Input Voltage			2.0			V
$V_{IN(0)}$	Logical "0" Input Voltage					0.8	V
$I_{IN(1)}$	Logical "1" Input Current	V_{CC} = 5.5V V_{IN} = 5.5V			0.1	40	μA
$I_{IN(0)}$	Logical "0" Input Current	V_{CC} = 5.5V V_{IN} = 5.5V			−180	−400	μA
V_{CLAMP}	Input Clamp Voltage	V_{CC} = 4.5V I_{IN} = −18 mA			−0.7	−1.2	V
V_{OH}	Logical "1" Output Voltage (No Load)	V_{CC} = 4.5V, I_{OH} = −10 μA	DS1628	3.4	4.3		V
			DS3628	3.5	4.3		V
V_{OL}	Logical "0" Output Voltage (No Load)	V_{CC} = 4.5V, I_{OL} = 10 μA	DS1628		0.25	0.4	V
			DS3628		0.25	0.35	V
V_{OH}	Logical "1" Output Voltage (With Load)	V_{CC} = 4.5V, I_{OH} = −1.0 mA	DS1628	2.5	3.9		V
			DS3628	2.7	3.9		V
V_{OL}	Logical "0" Output Voltage (With Load)	V_{CC} = 4.5V, I_{OL} = 20 mA	DS1628/DS3628		0.35	0.5	V
I_{ID}	Logical "1" Drive Current	V_{CC} = 4.5V, V_{OUT} = 0V, (Note 6)			−150		mA
I_{OD}	Logical "0" Drive Current	V_{CC} = 4.5V, V_{OUT} = 4.5V, (Note 6)			150		mA
Hi-Z	TRI-STATE Output Current	V_{OUT} = 0.4V to 2.4V, DIS1 or DIS2 = 2.0V		−40	0.1	40	μA
I_{CC}	Power Supply Current	V_{CC} = 5.5V	One DIS Input = 3.0V All Other Inputs = X, Outputs at Hi-Z		90	120	mA
			DIS1, DIS2 = 0V, Others = 3V Outputs on		70	100	mA
			All Inputs = 0V, Outputs Off		25	50	mA

Switching Characteristics (V_{CC} = 5V, T_A = 25°C) (Note 6)

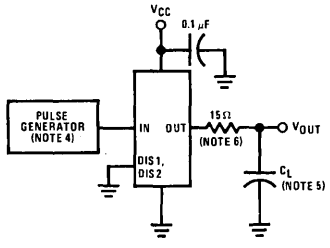
Symbol	Parameter	Conditions		Min	Typ	Max	Units
t_{S+-}	Storage Delay Negative Edge	(*Figure 1*)	C_L = 50 pF		4.0	5.0	ns
			C_L = 500 pF		6.5	8.0	
t_{S-+}	Storage Delay Positive Edge	(*Figure 1*)	C_L = 50 pF		4.2	5.0	ns
			C_L = 500 pF		6.5	8.0	
t_F	Fall Time	(*Figure 1*)	C_L = 50 pF		4.2	6.0	ns
			C_L = 500 pF		19	22	
t_R	Rise Time	(*Figure 1*)	C_L = 50 pF		5.2	7.0	ns
			C_L = 500 pF		20	24	
t_{ZL}	Delay from Disable Input to Logical "0" Level (from High Impedance State)	C_L = 50 pF to GND	R_L = 2 kΩ to V_{CC} (*Figure 2*)		19	25	ns
t_{ZH}	Delay from Disable Input to Logical "1" Level (from High Impedance State)	C_L = 50 pF to GND	R_L = 2 kΩ to GND (*Figure 2*)		13	20	ns

Switching Characteristics (Continued) (V_{CC} = 5V, T_A = 25°C) (Note 6)

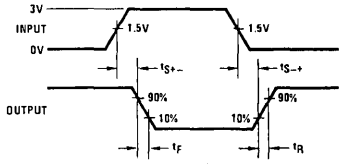
Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{LZ}	Delay from Disable Input to High Impedance State (from Logical "0" Level)	C_L = 50 pF to GND R_L = 400Ω to V_{CC} (*Figure 3*)		18	25	ns
t_{HZ}	Delay from Disable Input to High Impedance State (from Logical "1" Level)	C_L = 50 pF to GND R_L = 400Ω to GND (*Figure 3*)		8.5	15	ns

AC Test Circuits and Switching Time Waveforms

t_{S+-}, t_{S-+}, t_r, t_f



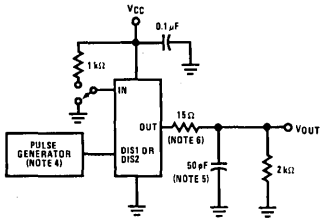
TL/F/5875–4



TL/F/5875–5

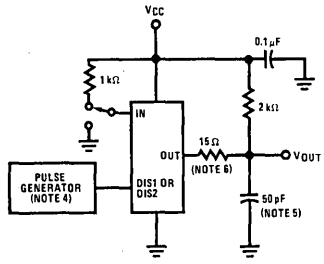
FIGURE 1

t_{ZH}

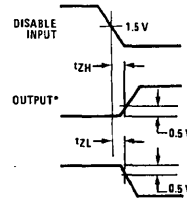


TL/F/5875–6

t_{ZL}



TL/F/5875–7

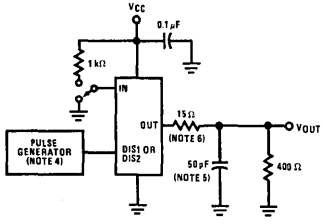


TL/F/5875–8

*ANY ONE OF EIGHT OUTPUTS

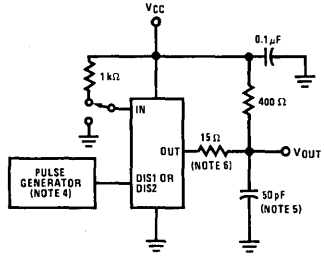
FIGURE 2

t_{HZ}

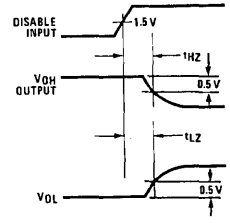


TL/F/5875–9

t_{LZ}



TL/F/5875–10



TL/F/5875–11

FIGURE 3

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified, min/max limits apply across the −55°C to +125°C temperature range for the DS1628 and across the 0°C to +70°C range for the DS3628. All typical values are for T_A = 25°C and V_{CC} = 5V.

Note 3: All currents into device pins shown as positive; all currents out of device pins shown as negative; all voltages references to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: The pulse generator has the following characteristics: Z_{OUT} = 50Ω and PRR ≤ 1 mHz. Rise and fall times between 10% and 90% points ≤ 5 ns.

Note 5: C_L includes probe and jig capacitance.

Note 6: When measuring output drive current and switching response for the DS1628 and DS3628 a 15Ω resistor should be placed in series with each output.

National Semiconductor Corporation

DS1645/DS3645/DS1675/DS3675 Hex TRI-STATE® TTL to MOS Latches/Drivers

General Description

The DS1645/DS3645 and DS1675/DS3675 are hex MOS latches/drivers with outputs designed to drive large capacitive loads up to 500 pF associated with MOS memory systems. PNP input transistors are used to reduce input currents, allowing the large fan-out to these drivers needed in memory systems. The circuit has Schottky-clamped transistor logic for minimum propagation delay, and TRI-STATE outputs which allow bus operation.

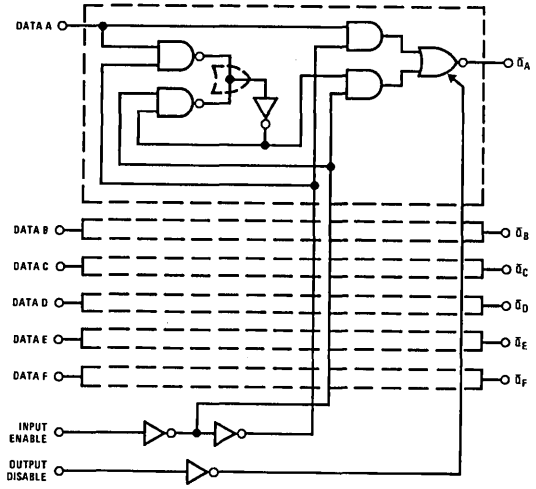
The DS1645/DS3645 has a 15Ω resistor in series with the outputs to dampen transients caused by the fast switching output circuit. The DS1675/DS3675 has a direct, low impedance output for use with or without an external resistor.

The circuit employs a fall-through-latch which captures the data in parallel with the output, thereby eliminating the delay normally encountered in other latch circuits. The DS1645/DS3645 and DS1675/DS3675 may be used for input address lines or input/output data lines of a MOS memory system.

Features

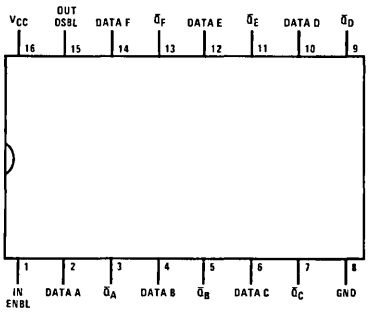
- TTL compatible inputs
- PNP inputs minimize loading
- Capacitance-driving outputs
- TRI-STATE outputs
- Built-in damping resistor (DS1645/DS3645)

Logic and Connection Diagrams



TL/F/7504–1

Dual-In-Line Package



TL/F/7504–2

Top View
Order Number DS1645J, DS1675J, DS3645J, DS3675J, DS3645N or DS3675N
See NS Package Number J16A or N16A

Truth Table

Input Enable	Output Disable	Data	Output	Operation
1	0	1	0	Data Feed-Through
1	0	0	1	Data Feed-Through
0	0	X	Q	Latched to Data Present when Enable Went Low
X	1	X	Hi-Z	High Impedance Output

X = Don't Care
Hi-Z = TRI-STATE Mode

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Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage, V_{CC}	7V
Logical "1" Input Voltage	7V
Logical "0" Input Voltage	−1.5V
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1433 mW
Molded Package	1362 mW
Lead Temperature (Soldering, 10 sec.)	300°C

*Derate cavity package 9.6 mW/°C above 25°C; derate molded package 10.9 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage V_{CC}	4.5	5.5	V
Temperature T_A			
DS1645, DS1675	−55	+125	°C
DS3645, DS3675	0	+70	°C

Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions			Min	Typ	Max	Units
$V_{IN(1)}$	Logical "1" Input Voltage				2.0			V
$V_{IN(0)}$	Logical "0" Input Voltage						0.8	V
$I_{IN(1)}$	Logical "1" Input Current	V_{IN} = 5.5V, V_{CC} = 5.5V	Enable Inputs			0.1	40	μA
			Data Inputs			0.2	80	μA
$I_{IN(0)}$	Logical "0" Input Current	V_{IN} = 0.5V, V_{CC} = 5.5V	Enable Inputs			−50	−250	μA
			Data Inputs			−100	−500	μA
V_{CLAMP}	Input Clamp Voltage	V_{CC} = 4.5V, I_{IN} = −18 mA				−0.75	−1.2	V
V_{OH}	Logical "1" Output Voltage (No Load)	V_{CC} = 4.5V, I_{OH} = −10 μA		DS1645, DS1675	2.7	3.6		V
				DS3645, DS3675	2.8	3.6		V
V_{OL}	Logical "0" Output Voltage (No Load)	V_{CC} = 4.5V, I_{OL} = −10 μA		DS1645, DS1675		0.25	0.4	V
				DS3645, DS3675		0.25	0.35	V
V_{OH}	Logical "1" Output Voltage (With Load)	V_{CC} = 4.5V, I_{OH} = −1.0 mA		DS1645	2.4	3.5		V
				DS1675	2.5	3.5		V
				DS3645	2.6	3.5		V
				DS3675	2.7	3.5		V
V_{OL}	Logical "0" Output Voltage (With Load)	V_{CC} = 4.5V, I_{OL} = 20 mA		DS1645		0.6	1.1	V
				DS1675		0.4	0.5	V
				DS3645		0.6	1.0	V
				DS3675		0.4	0.5	V
I_D	Logical "1" Drive Current	V_{CC} = 4.5V, V_{OUT} = 0V (Note 4)				−250		mA
I_{OD}	Logical "0" Drive Current	V_{CC} = 4.5V, V_{OUT} = 4.5V (Note 4)				150		mA
I_{HZ}	TRI-STATE Output Current	V_{OUT} = 0.4V to 2.4V, Output Disable = 2.0V			−40		40	μA
I_{CC}	Power Supply Current	V_{CC} = 5.5V	Output Disable = 3V All Other Inputs = 0V			60	100	mA
			Input Enable = 3V All Other Inputs = 0V			40	80	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified, min/max limits apply across the −55°C to +125°C temperature range for the DS1645 and DS1675 and across the 0°C to +70°C range for the DS3645 and DS3675. All typical values are for T_A = 25°C and V_{CC} = 5V.

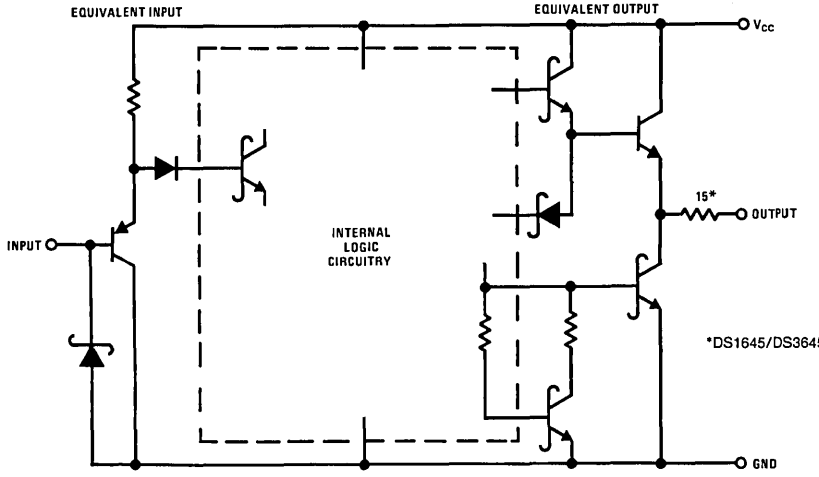
Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: When measuring output drive current and switching response for the DS1675 and DS3675, a 15Ω resistor should be placed in series with each output. This resistor is internal to the DS1645/DS3645, and need not be added.

Switching Characteristics V_{CC} = 5V, T_A = 25°C, unless otherwise noted. (Note 4)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
t_{S+-}	Storage Delay Negative Edge	*(Figure 1)*	C_L = 50 pF		4.5	7	ns
			C_L = 500 pF		8	12	ns
t_{S-+}	Storage Delay Positive Edge	*(Figure 1)*	C_L = 50 pF		6	8	ns
			C_L = 500 pF		9	13	ns
t_F	Fall Time	*(Figure 1)*	C_L = 50 pF		5	8	ns
			C_L = 500 pF		21	35	ns
t_R	Rise Time	*(Figure 1)*	C_L = 50 pF		6	9	ns
			C_L = 500 pF		22	35	ns
t_{SET-UP}	Set-Up Time on Data Input before Input Enable Goes Low			10	0		ns
t_{HOLD}	Hold Time on Data Input after Input Enable Goes Low			15	5		ns
t_W	Minimum Width of Enable Pulse to Latch Data			20	5		ns
t_{ZL}	Delay from Disable Input to Logical "0" Level (from High Impedance State)	C_L = 50 pF, R_L = 2 kΩ to V_{CC} *(Figure 2)*			10	15	ns
t_{ZH}	Delay from Disable Input to Logical "1" Level (from High Impedance State)	C_L = 50 pF, R_L = 2 kΩ to Ground, *(Figure 2)*			10	15	ns
t_{LZ}	Delay from Disable Input to High Impedance State (from Logical "0" Level)	C_L = 50 pF, R_L = 400Ω to V_{CC} *(Figure 3)*			16	25	ns
t_{HZ}	Delay from Disable Input to High Impedance State (from Logical "1" Level)	C_L = 50 pF, R_L = 400Ω to Ground, *(Figure 3)*			16	25	ns

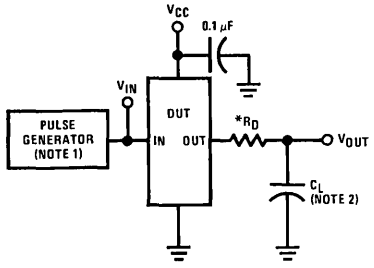
Schematic Diagram

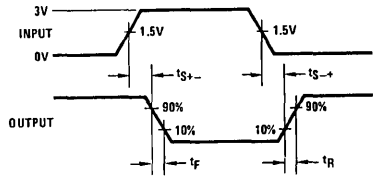


TL/F/7504–3

AC Test Circuits and Switching Time Waveforms

t_{S+-}, t_{S-+}, t_R, t_F





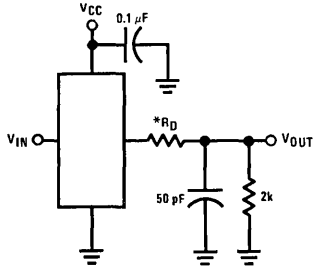
TL/F/7504–5

TL/F/7504–4

Note 1: The pulse generator has the following characteristics: Z_{OUT} = 50Ω and PRR ≤ 1 MHz. Rise and falll times between 10% and 90% points ≤ 5 ns.
Note 2: C_L includes probe and jig capacitance.

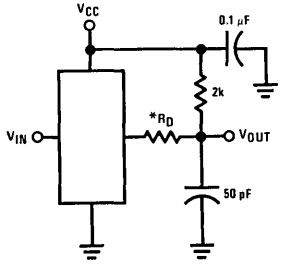
FIGURE 1

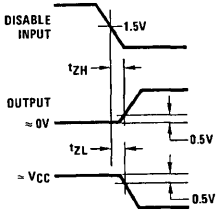
t_{ZH}



TL/F/7504–6

t_{ZL}





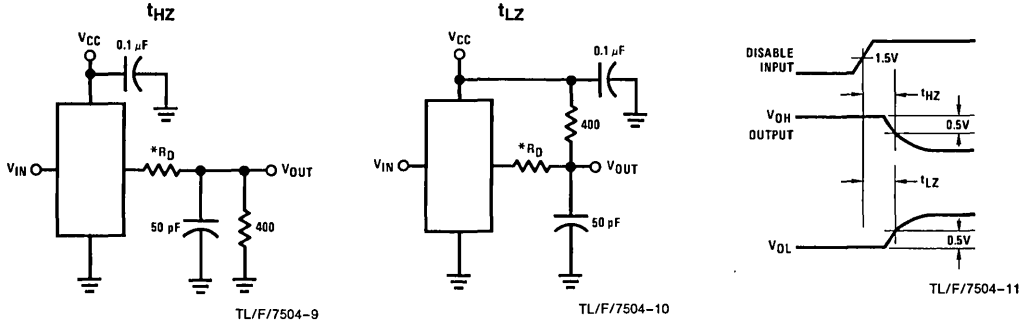
TL/F/7504–8

TL/F/7504–7

*Internal on DS1645 and DS3645

FIGURE 2

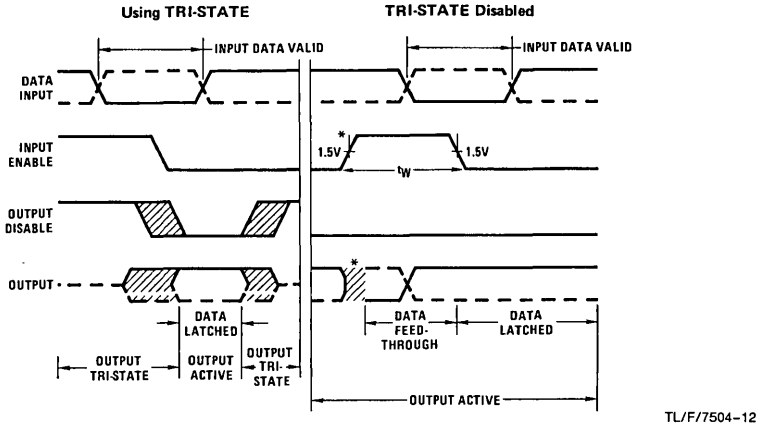
AC Test Circuits and Switching Time Waveforms (Continued)



*Internal on DS1645 and DS3645

FIGURE 3

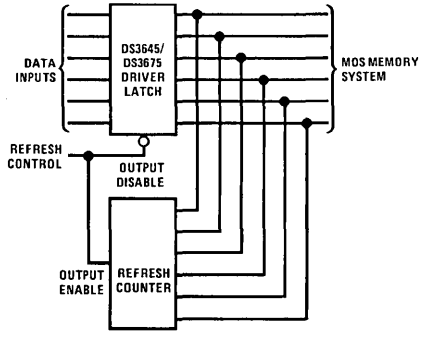
Operating Waveforms



*When the Input Enable makes a positive transition the output will be indeterminate for a short duration. The positive transition of the Input Enable normally occurs during a don't care timing state at the output.

Typical Applications

The DS3645 and DS3675 latch/driver has TRI-STATE outputs, which allows the outputs to be tied with those of another TRI-STATE driver. The DS3645 and DS3675 can be disabled while the alternate driver controls the address lines into the memory system.



5

National Semiconductor Corporation

DS3647A Quad TRI-STATE® MOS Memory I/O Register

General Description

The DS3647A is a 4-bit I/O buffer register intended for use in MOS memory systems. This circuit employs a fall-through latch for data storage. This method of latching captures the data in parallel with the output, thus eliminating the delays encountered in other designs. This circuit uses Schottky-clamped transistor logic for minimum propagation delay and employs PNP input transistors so that input currents are low, allowing a large fan-out for this circuit which is needed in a memory system.

Two pins per bit are provided, and data transfer is bi-directional so that the register can handle both input and output data. The direction of data flow is controlled through the input enables. The latch control, when taken low, will cause the register to hold the data present at that time and display it at the outputs. Data can be latched into the register independent of the output disables or EXPANSION input. Either or both of the outputs may be taken to the high-impedance state with the output disables. The EXPANSION pin disables both outputs to facilitate multiplexing with other I/O registers on the same data lines.

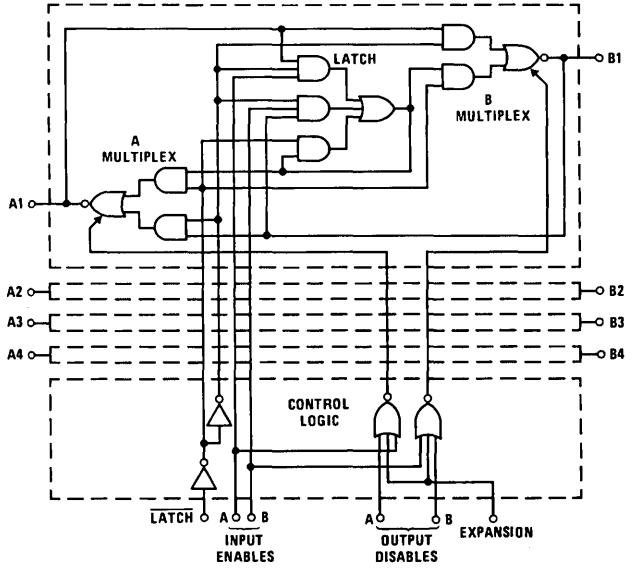
The DS3647A features TRI-STATE outputs. The "B" port outputs are designed for use in bus organized data transmission systems and can sink 80 mA and source −5.2 mA.

Data going from port "A" to port "B" and from "B" to port "A" is inverted in the DS3647A.

Features

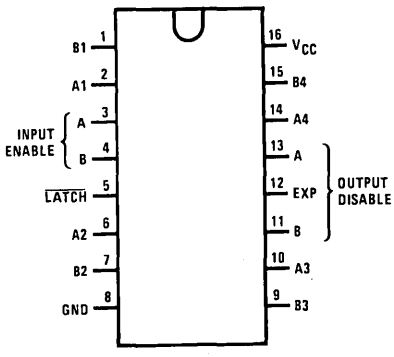
- PNP inputs minimize loading
- Fall-through latch design
- Propagation delay of only 15 ns
- TRI-STATE outputs
- EXPANSION control
- Bi-directional data flow
- TTL compatible
- Transmission line driver output

Logic and Connection Diagrams



TL/F/8354–1

Dual-In-Line Package



TL/F/8354–2

Top View

Order Number DS3647AD or DS3647AN
See NS Package Number D16C or N16A

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	−1.5V to +7V
Storage Temperature Range	−65° to +150°C
Maximum Power Dissipation* at 25°C	
Molded Package	1476 mW
Lead Temperature (Soldering, 10 seconds)	300°C

*Derate molded package 10.0 mW/° C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	5.5	V
Temperature (T_A)			
DS3647A	0	+70	°C

Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
$V_{IN(1)}$	Logic "1" Input Voltage			2.0			V
$V_{IN(0)}$	Logic "0" Input Voltage					0.8	V
$I_{IN(1)}$	Logic "1" Input Current	V_{CC}=5.5V, V_{IN}=5.5V	Latch, Disable Inputs		0.1	40	μA
			Expansion		0.2	80	μA
			A Ports, B Ports		0.2	100	μA
			Enable Inputs		0.4	200	μA
$I_{IN(0)}$	Logic "0" Input Current	V_{CC}=5.5V, V_{IN}=0.5V	Latch, Disable Inputs		−25	−250	μA
			Expansion		−50	−500	μA
			A Ports, B Ports		−50	−500	μA
			Enable, Inputs		−0.1	−1.25	mA
V_{CLAMP}	Input Clamp Voltage	V_{CC}=4.5V, I_{IN}=−18 mA			−0.6	−1.2	V
$V_{OL(A)}$	Logic "0" Output Voltage A Ports	V_{CC}=4.5V, I_{OL}=20 mA			0.4	0.5	V
$V_{OL(B)}$	Logic "0" Output Voltage B Ports	V_{CC}=4.5V	I_{OL}=30 mA		0.3	0.4	V
			I_{OL}=50 mA		0.4	0.5	V
$V_{OH(A)}$	Logic "1" Output Voltage A Ports	I_{OH}=−1 mA	V_{CC}=5V	3.0	3.4		V
			V_{CC}=4.5V	2.5	3.4		V
$V_{OH(B)}$	Logic "1" Output Voltage B Ports	I_{OH}=−5.2 mA, (Note 4)	V_{CC}=5V	2.9	3.3		V
			V_{CC}=4.5V	2.4	3.3		V
$I_{OS(A)}$	Output Short-Circuit Current A Port	V_{CC}=4.5V to 5.5V, V_{OUT}=0V, (Note 4)		−50	−80	−120	mA
$I_{OS(B)}$	Output Short-Circuit Current B Port	V_{CC}=4.5V to 5.5V, V_{OUT}=0V, (Note 4)		−70	−120	−180	mA
I_{CC}	Power Supply Current	Exp=3V, A Ports=0V, B Ports Open, All Other Pins=0V	DS3647A		100	140	mA
		Enable A, Latch=3V, A Ports=0V, B Ports Open, All Other Pins=0V	DS3647A		70	105	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C range. All typicals are given for V_{CC}=5V and T_A=25°C.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted.

Note 4: Only one output at a time should be shorted.

Switching Characteristics (V_{CC} = 5V, T_A = 25°C)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DATA TRANSFER B PORT TO A PORT						
t_{pd0}	Propagation Delay to a Logic "0"	CL = 50 pF, R_L = 280Ω, *(Figures 1 and 4)*		7.5	15	ns
t_{pd1}	Propagation Delay to a Logic "1"	C_L = 50 pF, R_L = 280Ω, *(Figures 1 and 4)*		6.0	12	ns
A PORT CONTROL FROM OUTPUT DISABLE A INPUT						
t_{LZ}	Delay to High Impedance from Logic "0"	*(Figures 1 and 5)*		13	20	ns
t_{HZ}	Delay to High Impedance from Logic "1"	*(Figures 1 and 6)*		14	20	ns
t_{ZL}	Delay to Logic "0" from High Impedance	*(Figures 1 and 7)*		10	15	ns
t_{ZH}	Delay to Logic "1" from High Impedance	*(Figures 1 and 8)*		25	35	ns
DATA TRANSFER A PORT TO B PORT, DS3647A						
t_{pd0}	Propagation Delay to a Logic "0"	C_L = 50 pF, R_L = 100 Ω, *(Figures 2 and 4)*		6.5	12	ns
t_{pd1}	Propagation Delay to a Logic "1"	C_L = 50 pF, R_L = 100 Ω, *(Figures 2 and 4)*		8.0	15	ns
B PORT CONTROL FROM OUTPUT DISABLE B INPUT, DS3647A						
t_{LZ}	Delay to High Impedance from Logic "0"	*(Figures 2 and 5)*		15	25	ns
t_{HZ}	Delay to High Impedance from Logic "1"	*(Figures 2 and 6)*		14	20	ns
t_{ZL}	Delay to Logic "0" from High Impedance	*(Figures 2 and 7)*		10	16	ns
t_{ZH}	Delay to Logic "1" from High Impedance	*(Figures 2 and 8)*		25	35	ns
LATCH SET-UP AND HOLD TIMES, ALL DEVICES						
t_{SET-UP}	Set-Up Time of Data Input Before $\overline{\text{Latch}}$ Goes Low		5	0		ns
t_{HOLD}	Hold Time of Data Input After $\overline{\text{Latch}}$ Goes Low		10	5		ns

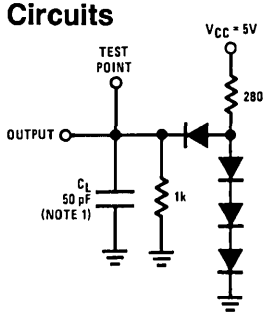
Product Description

Device Number	B Port To A Port Function	A Port To B Port Function	A Port Outputs	B Port Outputs
DS3647A	Inverting	Inverting	TRI-STATE	TRI-STATE

Truth Table

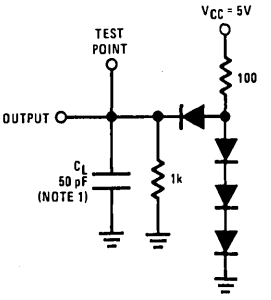
Input Enables		$\overline{\text{Latch}}$	Output Disables		Expansion	A Ports A1-A4	B Ports B1-B4	Comments
A	B		A	B				
1	0	1	0	0	0	Hi-Z	$\overline{A}$	Data in on A, output to B
0	1	1	0	0	0	$\overline{B}$	Hi-Z	Data in on B, output to A
1	0	0	0	0	0	Hi-Z	$\overline{A}$	Data stored which is present when $\overline{\text{latch}}$ goes low
0	1	0	0	0	0	$\overline{B}$	Hi-Z	Data stored which is present when $\overline{\text{latch}}$ goes low
1	0	x	0	1	0	Hi-Z	Hi-Z	Both A and B in Hi-Z state, Data in on A, may be latched
0	1	x	1	0	0	Hi-Z	Hi-Z	Both A and B in Hi-Z state, Data in on B, may be latched
x	x	x	x	x	1	Hi-Z	Hi-Z	Both A and B in Hi-Z state

AC Test Circuits



TL/F/8354–3

FIGURE 1. A Port Load

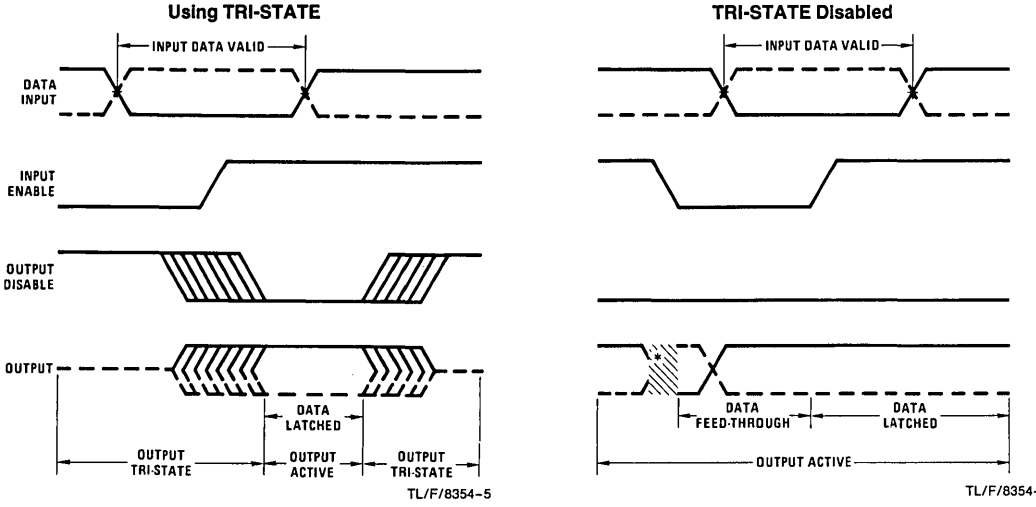


TL/F/8354–4

FIGURE 2. B Port Load

Note 1: C_L includes probe and jig capacitance.

Operating Waveforms



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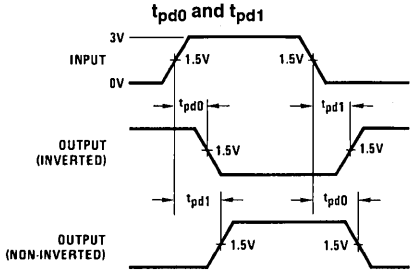
TL/F/8354–6

*When the Input Enable makes a negative transition, the output will be indeterminate for a short duration. The negative transition of the Input Enable normally occurs during a don't-care timing state at the output.

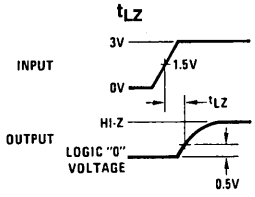
Switching Time Waveforms



TL/F/8354–7

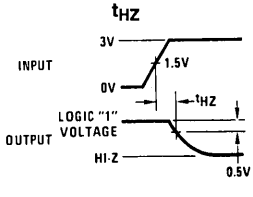
Input Characteristics: f = 1 MHz, $t_R = t_F \leq 5$ ns (10% to 90% points), duty cycle = 50%, $Z_{OUT} = 50\ \Omega$

FIGURE 4



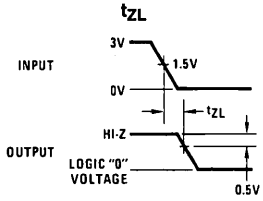
TL/F/8354–8

FIGURE 5



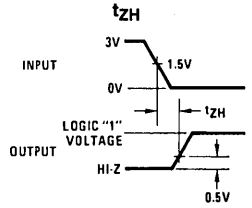
TL/F/8354–10

FIGURE 6



TL/F/8354–9

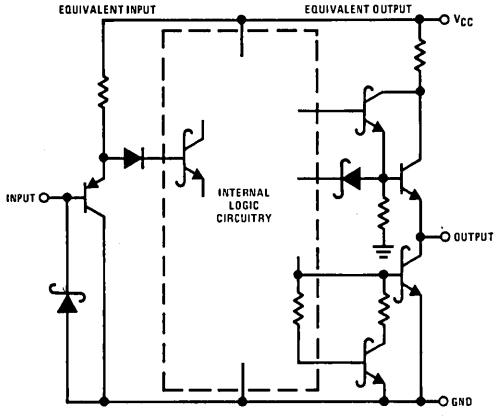
FIGURE 7



TL/F/8354–11

FIGURE 8

Schematic Diagram



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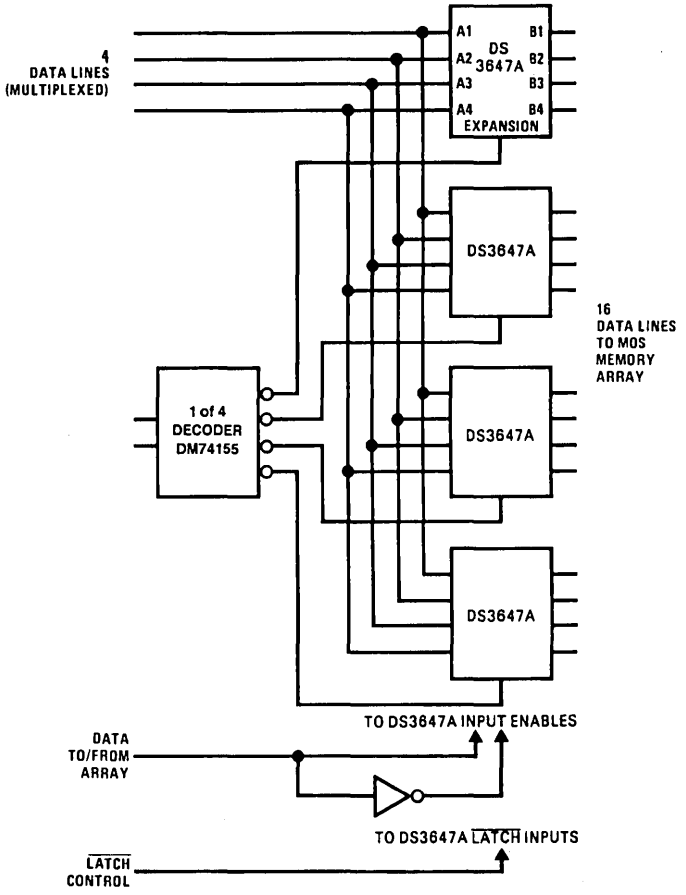
Note. Data pins A1–A4 and B1–B4 consist of an input and an output tied together.

Typical Application

The diagram below shows how the DS3647A can be used as a register capable of multiplexing data lines.



TL/F/8354–13

National Semiconductor Corporation

DS1648/DS3648/DS1678/DS3678 TRI-STATE® TTL to MOS Multiplexers/Drivers

General Description

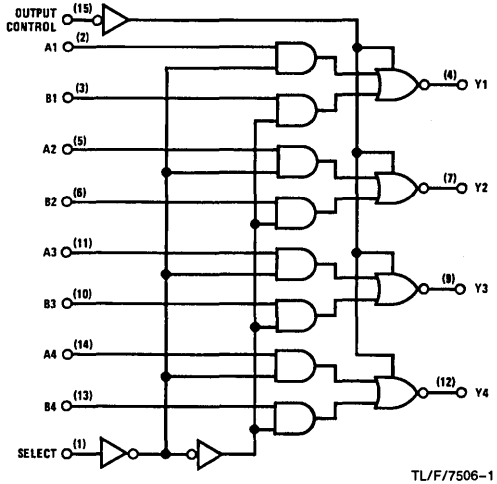
The DS1648/DS3648 and DS1678/DS3678 are quad 2-input multiplexers with TRI-STATE outputs designed to drive the large capacitive loads (up to 500 pF) associated with MOS memory systems. A PNP input structure is employed to minimize input currents so that driver loading in large memory systems is reduced. The circuit employs Schottky-clamped transistors for high speed and TRI-STATE outputs for bus operation.

The DS1648/DS3648 has a 15Ω resistor in series with the outputs to dampen transients caused by the fast-switching output. The DS1678/DS3678 has a direct, low impedance output for use with or without an external resistor.

Features

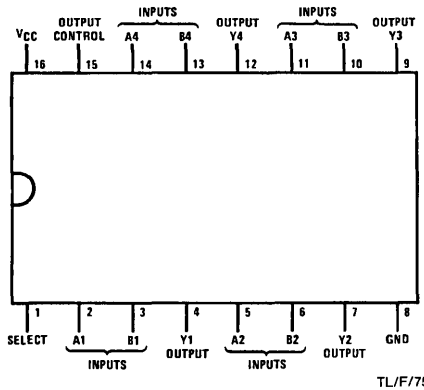
- TRI-STATE outputs interface directly with system-bus
- Schottky-clamped for better ac performance
- PNP inputs to minimize input loading
- TTL compatible
- High-speed capacitive load drivers
- Built-in damping resistor (DS1648/DS3648 only)

Logic and Connection Diagrams



TL/F/7506–1

Dual-In-Line Package



TL/F/7506–2

Top View

Order Number DS1648J, DS3648J, DS1678J
DS3678J, DS3648N or DS3678N
See NS Package Number J16A or N16A

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Logical "1" Input Voltage	7V
Logical "0" Input Voltage	−1.5V
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1433 mW
Molded Package	1362 mW
Lead Temperature (Soldering, 10 seconds)	300°C

* Derate cavity package 9.6 mW/°C above 25°C; derate molded package 10.9 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	5.5	V
Temperature (T_A)			
DS1648, DS1678	−55	+125	°C
DS3648, DS3678	0	+70	°C

Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
$V_{IN(1)}$	Logical "1" Input Voltage			2.0			V
$V_{IN(0)}$	Logical "0" Input Voltage					0.8	V
$I_{IN(1)}$	Logical "1" Input Current	V_{CC} = 5.5V, V_{IN} = 5.5V			0.1	40	μA
$I_{IN(0)}$	Logical "0" Input Current	V_{CC} = 5.5V, V_{IN} = 0.5V			−50	−250	μA
V_{CLAMP}	Input Clamp Voltage	V_{CC} = 4.5V, I_{IN} = −18 mA			−0.75	−1.2	V
V_{OH}	Logical "1" Output Voltage (No Load)	V_{CC} = 4.5V, I_{OH} = −10 μA	DS1648/DS1678	2.7	3.6		V
			DS3648/DS3678	2.8	3.6		V
V_{OL}	Logical "0" Output Voltage (No Load)	V_{CC} = 4.5V, I_{OL} = 10 μA	DS1648/DS1678		0.25	0.4	V
			DS3648/DS3678		0.25	0.35	V
V_{OH}	Logical "1" Output Voltage (With Load)	V_{CC} = 4.5V, I_{OH} = −1.0 mA	DS1648	2.4	3.5		V
			DS1678	2.5	3.5		V
			DS3648	2.6	3.5		V
			DS3678	2.7	3.5		V
V_{OL}	Logical "0" Output Voltage (With Load)	V_{CC} = 4.5V, I_{OL} = 20 mA	DS1648		0.6	1.1	V
			DS1678		0.4	0.5	V
			DS3648		0.6	1.0	V
			DS3678		0.4	0.5	V
I_{1D}	Logical "1" Drive Current	V_{CC} = 4.5V, V_{OUT} = 0V, (Note 4)			−250		mA
I_{0D}	Logical "0" Drive Current	V_{CC} = 4.5V, V_{OUT} = 4.5V, (Note 4)			150		mA
I_{Hi-Z}	TRI-STATE Output Current	V_{OUT} = 0.4V to 2.4V, Output Control = 2.0V		−40		40	μA
I_{CC}	Power Supply Current	V_{CC} = 5.5V	Output Control = 3V All Other Inputs at 0V		42	60	mA
			All Inputs at 0V		20	32	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS1648 and DS1678 and across the 0°C to +70°C range for the DS3648 and DS3678. All typical values for T_A = 25°C and V_{CC} = 5V.

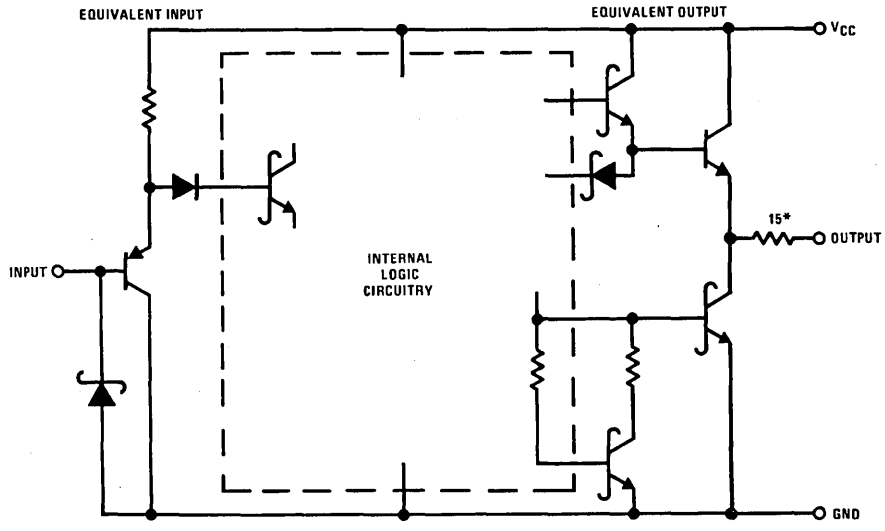
Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: When measuring output drive current and switching response for the DS1678 and DS3678 a 15Ω resistor should be placed in series with each output. This resistor is internal to the DS1648/DS3648 and need not be added.

Switching Characteristics V_{CC} = 5V, T_A = 25°C (Note 4)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
$t_{S\pm}$	Storage Delay Negative Edge	*(Figure 1)*	C_L = 50 pF		5	7	ns
			C_L = 500 pF		9	12	ns
$t_{S\mp}$	Storage Delay Positive Edge	*(Figure 1)*	C_L = 50 pF		6	8	ns
			C_L = 500 pF		9	13	ns
t_F	Fall Time	*(Figure 1)*	C_L = 50 pF		5	8	ns
			C_L = 500 pF		22	35	ns
t_R	Rise Time	*(Figure 1)*	C_L = 50 pF		6	9	ns
			C_L = 500 pF		22	35	ns
t_{ZL}	Delay from Output Control Input to Logical "0" Level (from High Impedance State)	C_L = 50 pF, R_L = 2 kΩ to V_{CC}, *(Figure 2)*			10	15	ns
t_{ZH}	Delay from Output Control Input to Logical "1" Level (from High Impedance State)	C_L = 50 pF, R_L = 2 kΩ to GND *(Figure 2)*			8	15	ns
t_{LZ}	Delay from Output Control Input to High Impedance State (from Logical "0" Level)	C_L = 50 pF, R_L = 400Ω to V_{CC}, *(Figure 3)*			15	25	ns
t_{HZ}	Delay from Output Control Input to High Impedance State (from Logical "1" Level)	C_L = 50 pF, R_L = 400Ω to GND, *(Figure 3)*			10	25	ns
$t_{S\pm}$	Propagation Delay to Logical "0" Transition When Select Selects A	C_L = 50 pF, *(Figure 1)*			12	15	ns
$t_{S\mp}$	Propagation Delay to Logical "1" Transition When Select Selects A	C_L = 50 pF, *(Figure 1)*			14	17	ns
$t_{S\pm}$	Propagation Delay to Logical "0" Transition When Select Selects B	C_L = 50 pF, *(Figure 1)*			16	20	ns
$t_{S\mp}$	Propagation Delay to Logical "1" Transition When Select Selects B	C_L = 50 pF, *(Figure 1)*			14	20	ns

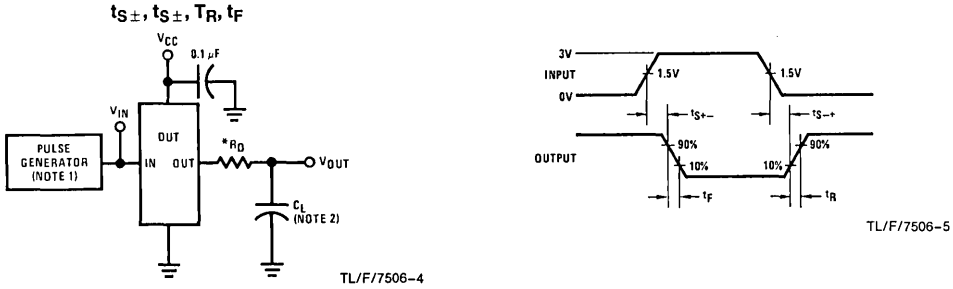
Schematic Diagram



TL/F/7506–3

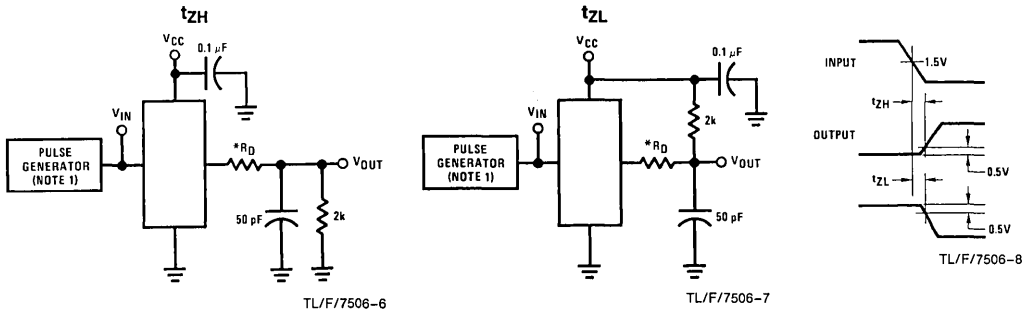
*DS1648/DS3648 only

AC Test Circuits and Switching Time Waveforms



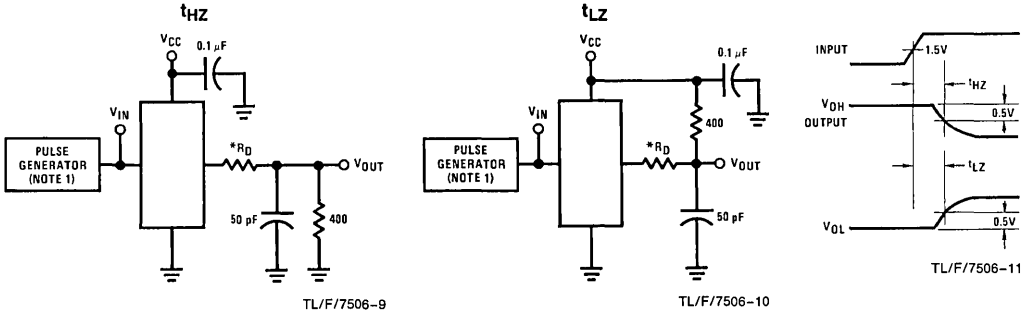
Note 1: The pulse generator has the following characteristics: Z_{OUT} = 50Ω and PRR ≤ 1 MHz. Rise and fall times between 10% and 90% points ≤ 5 ns.
Note 2: C_L includes probe and jig capacitance.

FIGURE 1



*Internal on DS1648 and DS3648

FIGURE 2



*Internal on DS1648 and DS3648

FIGURE 3

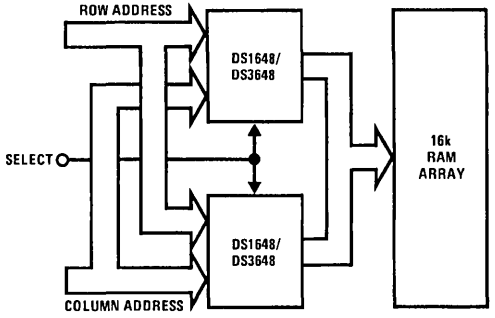
Truth Table

Output Control	Inputs			Outputs
	Select	A	B	
H	X	X	X	Hi-Z
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

H = High level
L = Low level
X = Don't care
Hi-Z = TRI-STATE mode

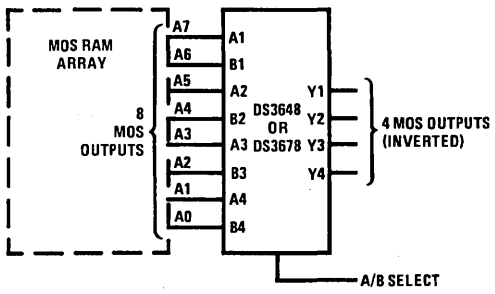
Typical Applications

Addressing 16k RAM



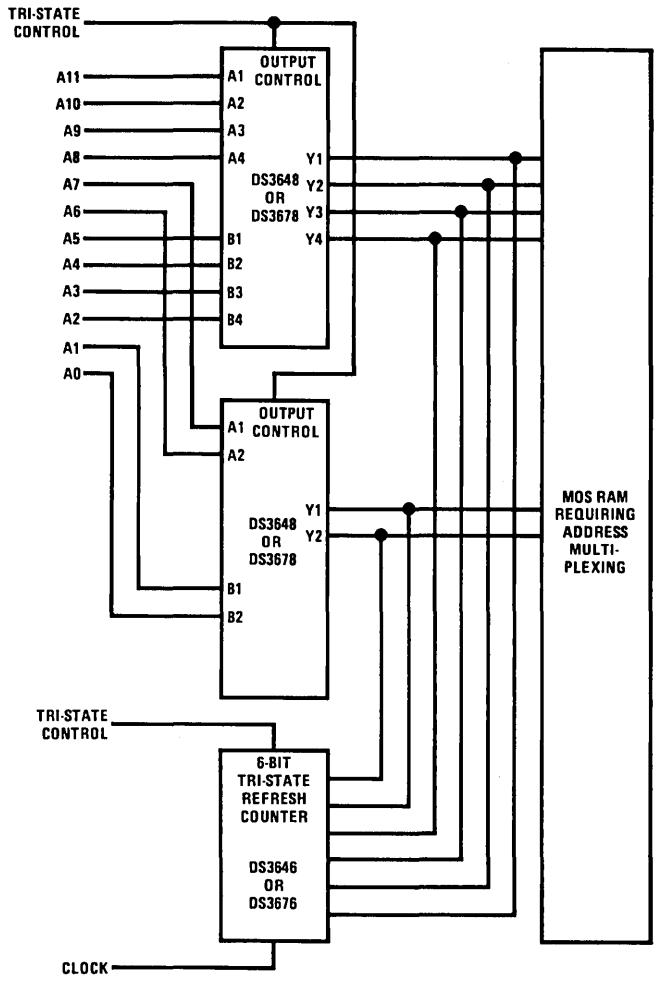
TL/F/7506–12

2:1 Multiplexing of RAM Outputs



TL/F/7506–14

Refreshing Using TRI-STATE Counter



TL/F/7506–13

National Semiconductor Corporation

DS1649/DS3649/DS1679/DS3679 Hex TRI-STATE® TTL to MOS Drivers

General Description

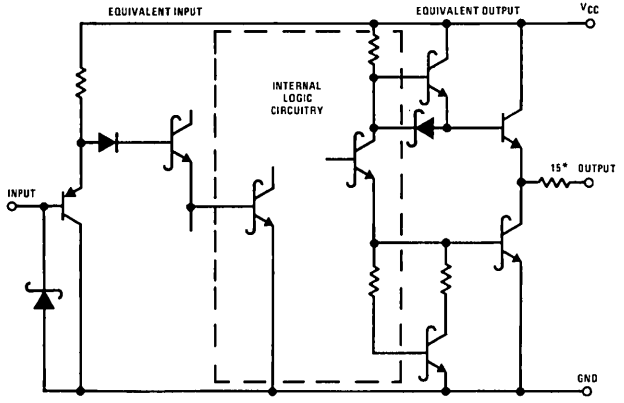
The DS1649/DS3649 and DS1679/DS3679 are Hex TRI-STATE MOS drivers with outputs designed to drive large capacitive loads up to 500 pF associated with MOS memory systems. PNP input transistors are employed to reduce input currents allowing the large fan-out to these drivers needed in memory systems. The circuit has Schottky-clamped transistor logic for minimum propagation delay, and TRI-STATE outputs for bus operation.

The DS1649/DS3649 has a 15Ω resistor in series with the outputs to dampen transients caused by the fast-switching output. The DS1679/DS3679 has a direct low impedance output for use with or without an external resistor.

Features

- High speed capabilities
  - Typ 9 ns driving 50 pF
  - Typ 30 ns driving 500 pF
- TRI-STATE outputs for data bussing
- Built-in 15Ω damping resistor (DS1649/DS3649)
- Same pin-out as DM8096 and DM74366

Schematic Diagram



*DS1649/DS3649 only

TL/F/7515–1

Truth Table

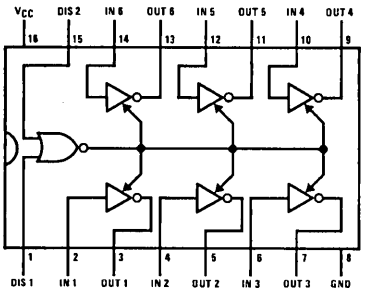
Disable Input		Input	Output
DIS 1	DIS 2		
0	0	0	1
0	0	1	0
0	1	X	Hi-Z
1	0	X	Hi-Z
1	1	X	Hi-Z

X = Don't care

Hi-Z = TRI-STATE mode

Connection Diagram

Dual-In-Line Package

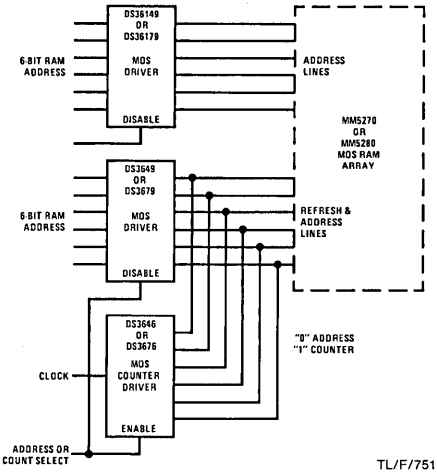


TL/F/7515–2

Top View

Order Number DS1649J, DS3649J, DS1679J, DS3679J, DS3649N or DS3679N
See NS Package Number J16A or N16A

Typical Application



TL/F/7515–3

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7.0V
Logical "1" Input Voltage	7.0V
Logical "0" Input Voltage	−1.5V
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1371 mW
Molded Package	1280 mW
Lead Temperature (Soldering, 10 sec.)	300°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC}	4.5	5.5	V
Temperature (T_A)			
DS1649, DS1679	−55	+125	°C
DS3649, DS3679	0	+70	°C

*Derate cavity package 9.1 mW/°C above 25°C; derate molded package 10.2 mW/°C above 25°C.

Electrical Characteristics (Note 2 and 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
$V_{IN(1)}$	Logical "1" Input Voltage			2.0			V
$V_{IN(0)}$	Logical "0" Input Voltage					0.8	V
$I_{IN(1)}$	Logical "1" Input Current	V_{CC} = 5.5V, V_{IN} = 5.5V			0.1	40	μA
$I_{IN(0)}$	Logical "0" Input Current	V_{CC} = 5.5V, V_{IN} = 0.5V			−50	−250	μA
V_{CLAMP}	Input Clamp Voltage	V_{CC} = 4.5V, I_{IN} = −18 mA			−0.75	−1.2	V
V_{OH}	Logical "1" Output Voltage (No Load)	V_{CC} = 4.5V, I_{OH} = −10 μA	DS1649/DS1679	2.7	3.6		V
			DS3649/DS3679	2.8	3.6		
V_{OL}	Logical "0" Output Voltage (No Load)	V_{CC} = 4.5V, I_{OL} = 10 μA	DS1649/DS1679		0.25	0.4	V
			DS3649/DS3679		0.25	0.35	V
V_{OH}	Logical "1" Output Voltage (With Load)	V_{CC} = 4.5V, I_{OH} = −1.0 mA	DS1649	2.4	3.5		V
			DS1679	2.5	3.5		V
			DS3649	2.6	3.5		V
			DS3679	2.7	3.5		V
V_{OL}	Logical "0" Output Voltage (With Load)	V_{CC} = 4.5V, I_{OL} = 20 mA	DS1649		0.6	1.1	V
			DS1679		0.4	0.5	V
			DS3649		0.6	1.0	V
			DS3679		0.4	0.5	V
I_{1D}	Logical "1" Drive Current	V_{CC} = 4.5V, V_{OUT} = 0V (Note 4)			−250		mA
I_{0D}	Logical "0" Drive Current	V_{CC} = 4.5V, V_{OUT} = 4.5V (Note 4)			150		mA
Hi-Z	TRI-STATE Output Current	V_{OUT} = 0.4V to 2.4V, DIS1 or DIS2 = 2.0V		−40		40	μA
I_{CC}	Power Supply Current	V_{CC} = 5.5V	One DIS Input = 3.0V All Other Inputs = X		42	75	mA
			All Inputs = 0V		11	20	mA

Switching Characteristics (V_{CC} = 5V, T_A = 25°C) (Note 4)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
$t_{S\pm}$	Storage Delay Negative Edge	(*Figure 1*)	C_L = 50 pF		4.5	7	ns
			C_L = 500 pF		7.5	12	ns
$t_{S\pm}$	Storage Delay Positive Edge	(*Figure 1*)	C_L = 50 pF		5	8	ns
			C_L = 500 pF		8	13	ns
t_F	Fall Time	(*Figure 1*)	C_L = 50 pF		5	8	ns
			C_L = 500 pF		22	35	ns
t_R	Rise Time	(*Figure 1*)	C_L = 50 pF		6	9	ns
			C_L = 500 pF		21	35	ns
t_{ZL}	Delay from Disable Input to Logical "0" Level (from High Impedance State)	C_L = 50 pF R_L = 2 kΩ to V_{CC} (*Figure 2*)			10	15	ns
t_{ZH}	Delay from Disable Input to Logical "1" Level (from High Impedance State)	C_L = 50 pF R_L = 2 kΩ to GND (*Figure 2*)			8	15	ns
t_{LZ}	Delay from Disable Input to High Impedance State (from Logical "0" Level)	C_L = 50 pF R_L = 400Ω to V_{CC} (*Figure 3*)			15	25	ns
t_{HZ}	Delay from Disable Input to High Impedance State (from Logical "1" Level)	C_L = 50 pF R_L = 400Ω to GND (*Figure 3*)			10	25	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

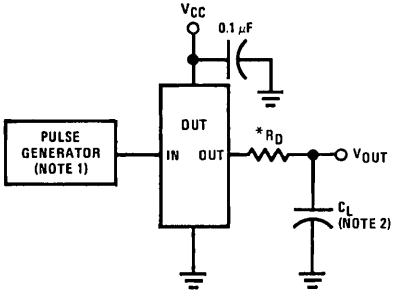
Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS1649 and DS1679 and across the 0°C to +70°C range for the DS3649 and DS3679. All typical values are for T_A = 25°C and V_{CC} = 5V.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

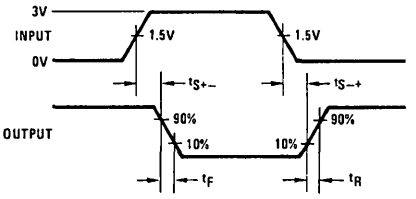
Note 4: When measuring output drive current and switching response for the DS1679 and DS3679 a 15Ω resistor should be placed in series with each output. This resistor is internal to the DS1649/DS3649 and need not be added.

AC Test Circuits and Switching Time Waveforms

$t_{S\pm}$, $t_{S\mp}$, t_R, t_F



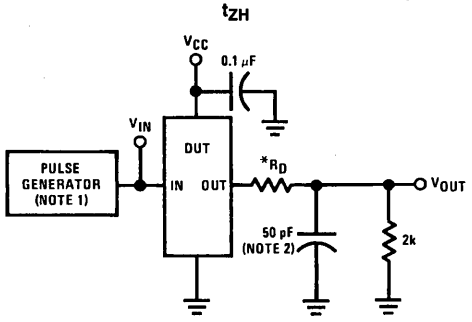
TL/F/7515–4



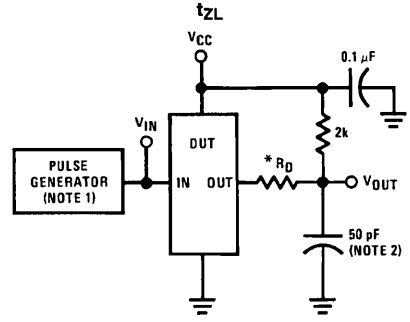
TL/F/7515–5

FIGURE 1

AC Test Circuits and Switching Time Waveforms (Continued)



TL/F/7515-6



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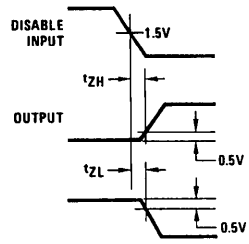
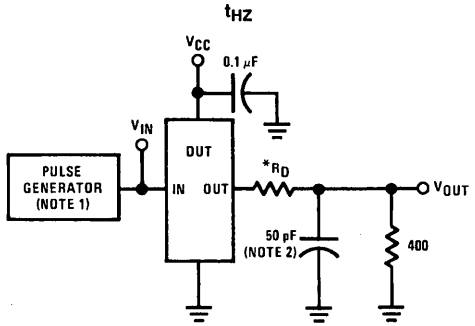
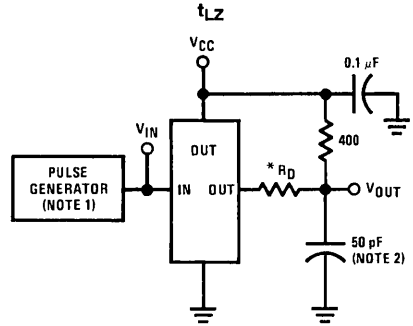


TL/F/7515-8

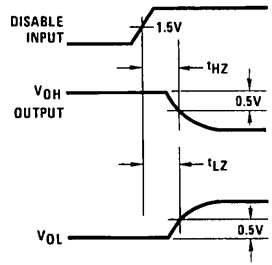
FIGURE 2



TL/F/7515-9



TL/F/7515-10



*Internal on DS1649 and DS3649

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FIGURE 3

Note 1: The pulse generator has the following characteristics: Z_{OUT} = 50Ω and PRR ≤ 1 MHz. Rise and fall times between 10% and 90% points ≤ 5 ns.
Note 2: C_L includes probe and jig capacitance.

National Semiconductor Corporation

DS1651/DS3651
Quad High Speed MOS Sense Amplifiers

General Description

The DS1651/DS3651 is TTL compatible high speed circuits intended for sensing in a broad range of MOS memory system applications. Switching speeds have been enhanced over conventional sense amplifiers by application of Schottky technology, and TRI-STATE® strobing is incorporated, offering a high impedance output state for bused organization.

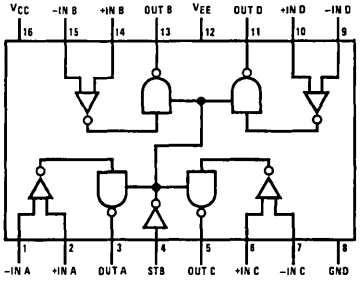
The DS1651/DS3651 has active pull-up outputs and offers open collector outputs providing implied "AND" operations.

Features

- High speed
- TTL compatible
- Input sensitivity — ±7 mV
- TRI-STATE outputs for high speed buses
- Standard supply voltages — ±5V
- Pin and function compatible with MC3430

Connection Diagram

Dual-In-Line Package



Top View TL/F/7528-1

Order Number DS1651J, DS3651J or DS3651N
See NS Package Number J16A or N16A

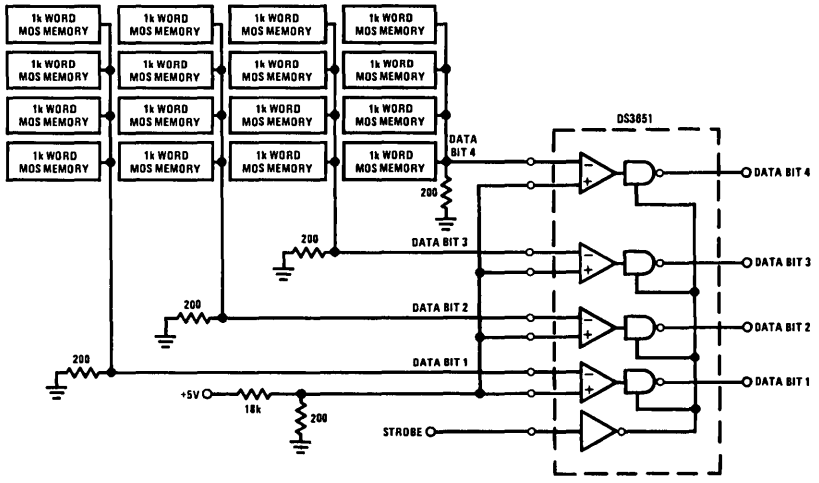
Truth Table

Input	Strobe	Output
		DS3651
$V_{ID} \geq 7$ mV $T_A = 0°C$ to $+70°C$	L H	H Open
-7 mV $\leq V_{ID} \leq +7$ mV $T_A = 0°C$ to $+70°C$	L H	X Open
$V_{ID} \geq -7$ mV $T_A = 0°C$ to $+70°C$	L H	L Open

L = Low logic state
H = High logic state
Open = TRI-STATE
X = Indeterminate state

Typical Applications

A Typical MOS Memory Sensing Application for a 4k word by 4-bit memory arrangement employing 1103 type memory devices



Note: Only 4 devices are required for a 4k word by 16-bit memory system. TL/F/7528-2

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Power Supply Voltages	
V_{CC}	+7 V_{DC}
V_{EE}	−7 V_{DC}
Differential-Mode Input Signal Voltage Range, V_{IDR}	±6 V_{DC}
Common-Mode Input Voltage Range, V_{ICR}	±5 V_{DC}
Strobe Input Voltage, $V_{I(S)}$	5.5 V_{DC}
Strobe Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1509 mW
Molded Package	1476 mW
Lead Temp. (Soldering, 10 seconds)	300°C

* Derate cavity package 10.1 mW/°C above 25°C; derate molded package 11.8 mW/°C above 25°C.

Operating Conditions

	Min	Max	Unit
Supply Voltage (V_{CC})			
DS1651	4.5	5.5	V
DS3651	4.75	5.25	V
Supply Voltage (V_{EE})			
DS1651	−4.5	−5.5	V
DS3651	−4.75	−5.25	V
Operating Temperature (T_A)			
DS1651	−55	+125	°C
DS3651	0	+70	°C
Output Load Current, (I_{OL})		16	mA
Differential Mode Input Voltage Range, (V_{IDR})	−5.0	+5.0	V
Common-Mode Input Voltage Range, (V_{ICR})	−3.0	+3.0	V
Input Voltage Range (Any Input to GND), (V_{IR})	−5.0	+3.0	V

Electrical Characteristics

V_{CC} = 5 V_{DC}, V_{EE} = −5 V_{DC}, Min ≤ T_A ≤ Max, unless otherwise noted (Notes 2 and 3)

Symbol	Parameter	Conditions			Min	Typ	Max	Unit
V_{IS}	Input Sensitivity, (Note 5) (Common-Mode Voltage Range) VICR = −3V ≤ V_{IN} ≤ +3V)	Min ≤ V_{CC} ≤ Max Min ≥ V_{EE} ≥ Max					±7.0	mV
V_{IO}	Input Offset Voltage					2		mV
I_{IB}	Input Bias Current	V_{CC} = Max, V_{EE} = Max					20	μA
I_{IO}	Input Offset Current					0.5		μA
$V_{IL(S)}$	Strobe Input Voltage (Low State)						0.8	V
$V_{IH(S)}$	Strobe Input Voltage (High State)				2			V
$I_{IL(S)}$	Strobe Current (Low State)	V_{CC} = Max, V_{EE} = Max, V_{IN} = 0.4V					−1.6	mA
$I_{IL(S)}$	Strobe Current (High State)	V_{CC} = Max,	V_{IN} = 2.4V	DS3651			40	μA
		V_{EE} = Max	V_{IN} = V_{CC}				1	mA
			V_{IN} = 2.4V	DS1651			100	μA
			V_{IN} = V_{CC}				1	mA
V_{OH}	Output Voltage (High States)	V_{CC} = Min, V_{EE} = Min	I_O = −400 μA	DS1651/DS3651	2.4			V
V_{OL}	Output Voltage (Low State)	V_{CC} = Min,	I_O = 16 mA	DS3651			0.45	V
		V_{EE} = Min		DS1651			0.50	
I_{OS}	Output Current Short Circuit	V_{CC} = Max, V_{EE} = Max, (Note 4)		DS1651/DS3651	−18		−70	mA
I_{OFF}	Output Disable Leakage Current	V_{CC} = Max, V_{EE} = Max		DS3651			40	μA
				DS1651			100	μA
I_{CC}	High Logic Level Supply Current	V_{CC} = Max, V_{EE} = Max				45	60	mA
I_{EE}	High Logic Level Supply Current	V_{CC} = Max, V_{EE} = Max				−17	−30	mA

Switching Characteristics $V_{CC} = 5\ V_{DC}$, $V_{EE} = -5\ V_{DC}$, $T_A = 25°C$ unless otherwise noted.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
$t_{PHL(D)}$	High-to-Low Logic Level Propagation Delay Time (Differential Inputs)	5 mV + V_{IS}, (*Figure 3*)	DS1651/ DS3651		23	45	ns
$t_{PLH(D)}$	Low-to-High Logic Level Propagation Delay Time (Differential Inputs)	5 mV + V_{IS}, (*Figure 3*)	DS1651/ DS3651		22	55	ns
$t_{POH(S)}$	TRI-STATE to High Logic Level Propagation Delay Time (Strobe)	(*Figure 1*)	DS1651/ DS3651		16	21	ns
$t_{PHO(S)}$	High Logic Level to TRI-STATE Propagation Delay Time (Strobe)	(*Figure 1*)	DS1651/ DS3651		7	18	ns
$t_{POL(S)}$	TRI-STATE to Low Logic Level Propagation Delay Time (Strobe)	(*Figure 1*)	DS1651/ DS3651		19	27	ns
$t_{PLO(S)}$	Low Logic Level to TRI-STATE Propagation Delay Time (Strobe)	(*Figure 1*)	DS1651/ DS3651		14	29	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

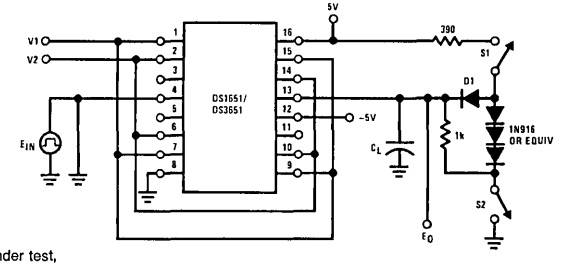
Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C range for the DS3651 and across the −55°C to +125°C range for the DS1651. All typical values are for $T_A = 25°C$, $V_{CC} = 5V$ and $V_{EE} = -5V$.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Only one output at a time should be shorted.

Note 5: A parameter which is of primary concern when designing with sense amplifiers is, what is the minimum differential input voltage required at the sense amplifier input terminals to guarantee a given output logic state. This parameter is commonly referred to as threshold voltage. It is well known that design considerations of threshold voltage are plagued by input offset currents, bias currents, network source resistances, and voltage gain. As a design convenience, the DS1651 and DS3651 are specified to a parameter called input sensitivity (V_{IS}). This parameter takes into consideration input offset currents and bias currents, and guarantees a minimum input differiential voltage to cause a given output logic state with respect to a maximum source impedance of 200Ω at each input.

Switching Time Waveform



Note: Output of channel B shown under test, other channels are tested similarly.

TL/F/7528-3

Delay	V1	V2	S1	S2	C_L
$t_{PLO(S)}$	100 mV	GND	Closed	Closed	15 pF
$t_{POL(S)}$	100 mV	GND	Closed	Open	50 pF
$t_{PHO(S)}$	GND	100 mV	Closed	Closed	15 pF
$t_{POH(S)}$	GND	100 mV	Open	Closed	50 pF

C_L includes jig and probe capacitance.

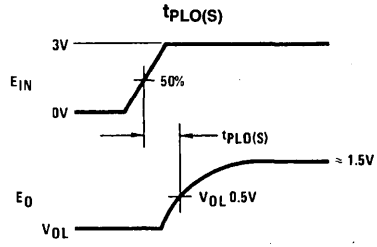
E_{IN} waveform characteristics: t_{TLH} and $t_{THL} \leq 10$ ns measured 10% to 90%

PRR = 1 MHz

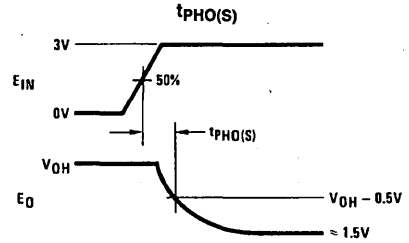
Duty cycle = 50%

5

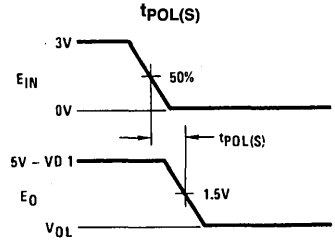
AC Test Circuits



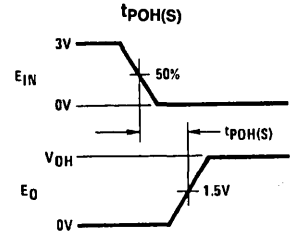
TL/F/7528-4



TL/F/7528-5

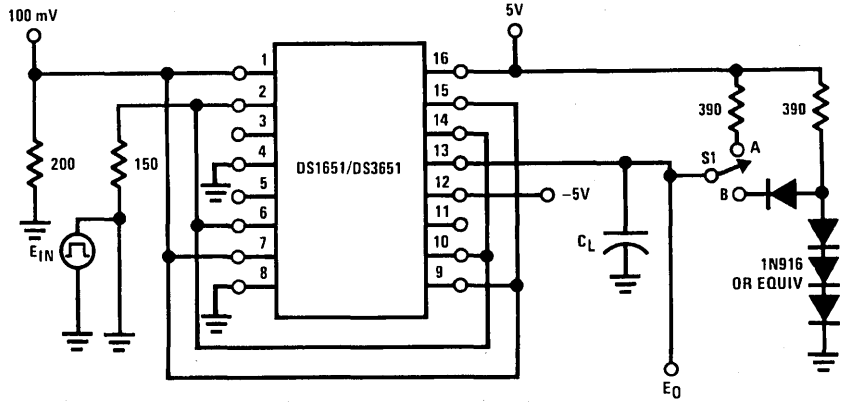


TL/F/7528-6



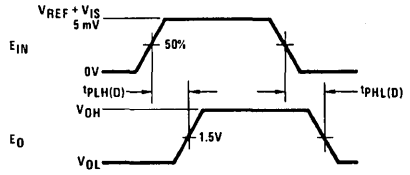
TL/F/7528-7

FIGURE 1. Strobe Propagation Delay $t_{PLO(S)}$, $t_{POL(S)}$, $t_{PHL(S)}$ and $t_{POH(S)}$



TL/F/7528-10

Note: Output of channel B shown under test, other channels are tested similarly.
S1 at "B" for DS1651/DS3651, C_L = 50 pF total for DS1651/DS3651



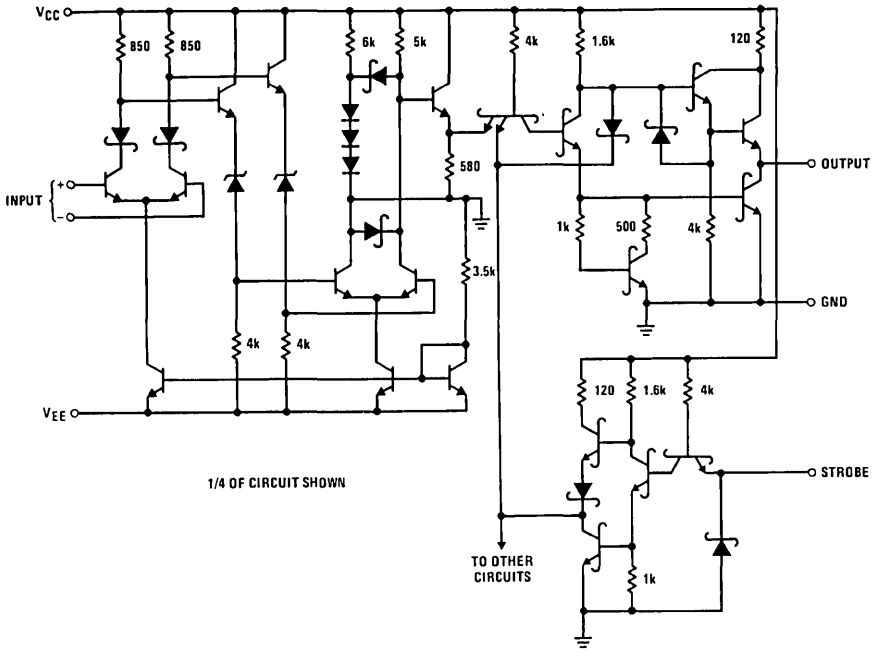
TL/F/7528-11

E_{IN} waveform characteristics:
t_{TLH} and $t_{THL} \leq$ 10 ns measured 10% to 90%
PRR = 1 MHz, duty cycle = 500 ns

FIGURE 2. Differential Input Propagation Delay $t_{PLH(D)}$ and $t_{PHL(D)}$

Schematic Diagrams

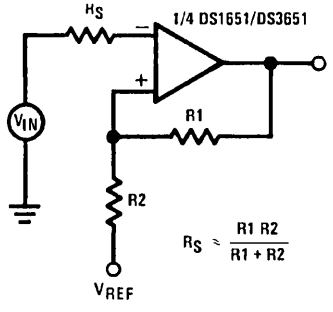
DS1651/DS3651



TL/F/7528-12

Typical Applications

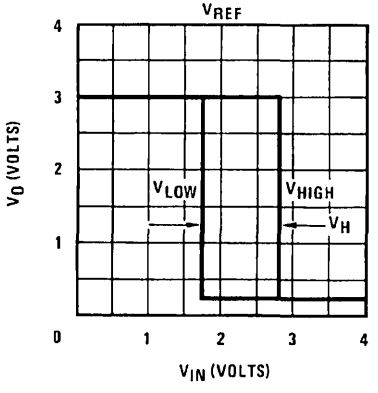
Level Detector with Hysteresis



$$R_S \approx \frac{R1\ R2}{R1 + R2}$$

TL/F/7528-15

Transfer Characteristics and Equations for Level Detector with Hysteresis



TL/F/7528-16

$$V_{HIGH} = V_{REF} + \frac{R2\,[V_{O(MAX)} - V_{REF}]}{R1 + R2}$$

$$V_{LOW} = V_{REF} + \frac{R2\,[V_{O(MIN)} - V_{REF}]}{R1 + R2}$$

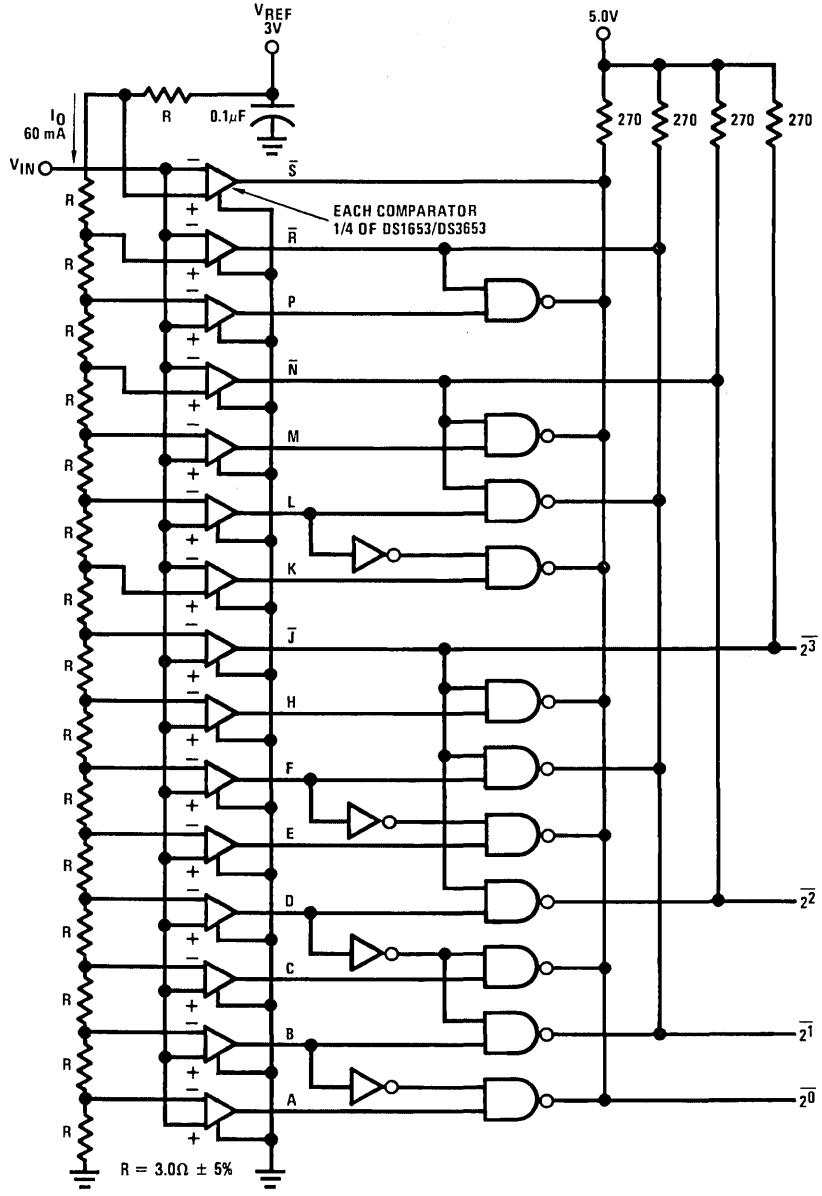
Hysteresis Loop (V_H)

$$V_H = V_{HIGH} - V_{LOW} = \frac{R2}{R1 + R2}\,[V_{O(MAX)} - V_{O(MIN)}]$$

5

Typical Applications (Continued)

4-Bit Parallel A/D Converter



$\overline{2^0} = (\overline{A} + B)(\overline{C} + D)(\overline{E} + F)(\overline{H} + J)(\overline{K} + L)(\overline{M} + N)(\overline{P} + R)(\overline{S})$

$\overline{2^1} = (\overline{B} + D)(\overline{F} + J)(\overline{L} + N)(\overline{R})$

$\overline{2^2} = (\overline{D} + J)(\overline{N})$

$\overline{2^3} = \overline{J}$

Conversion time ≅ 50 ns

National Semiconductor Corporation

DS1674/DS3674 Quad TTL to MOS Clock Drivers

General Description

The DS1674/DS3674 is a quad bipolar-to-MOS clock driver with TTL compatible inputs. It is designed to provide high output current and voltage capabilities necessary for optimum driving of high capacitance N-channel MOS memory systems.

The device features two common enable inputs, a refresh input, and a clock control input for simplified system designs. The circuit was designed for driving highly capacitive loads at high speeds and uses Schottky-clamped transistors. PNP transisitors are used on all inputs thereby minimizing input loading.

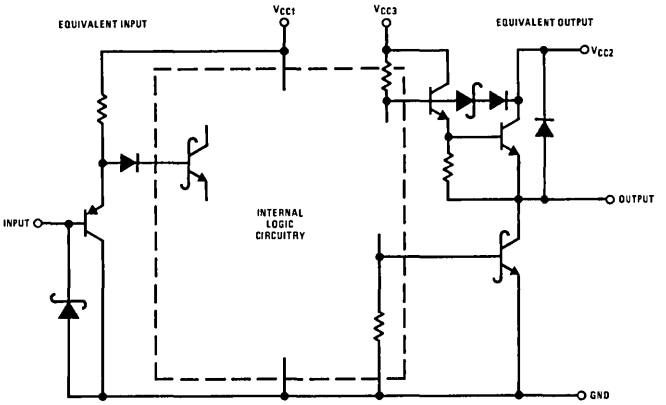
The circuit may be connected to provide a 12V clock output amplitude as required by 4k RAMs or a 5V clock output amplitude as required by 16k RAMs.

The DS1674/DS3674 has a direct, low impedance output for use with or without an external damping resistor.

Features

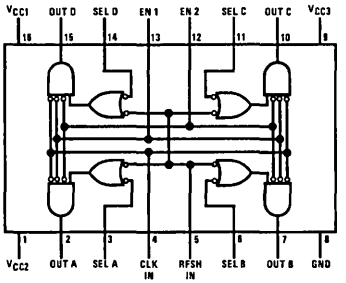
- TTL compatible inputs
- 12V clock or 5V clock driver
- Operates from standard bipolar and MOS supplies
- PNP inputs minimize loading
- High voltage/current outputs
- Input and output clamping diodes
- Control logic optimized for use with MOS memory systems
- Pin and function compatible with MC3460 and 3235

Schematic and Connection Diagrams



TL/F/5876–1

Dual-In-Line Package



TL/F/5876–2

Top View

Order Number DS3674J or DS3674N
See NS Package Number J16A or N16A

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	
V_{CC1}	7V
V_{CC2}	13.5V
V_{CC3}	16V
Input Voltage	−1.0V to +7V
Output Voltage	−1.0V to +16V
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1509 mW
Molded Package	1476 mW
Lead Temperature (Soldering, 10 sec.)	300°C

* Derate cavity package 10.1 mW/°C above 25°C; derate molded package 11.8 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage			
V_{CC1}			
DS1674	4.5	5.5	V
DS3674	4.75	5.25	V
V_{CC2}			
DS1674	4.5	13.2	V
DS3674	4.75	12.6	V
V_{CC3}			
DS1674	V_{CC2}	16.5	V
DS3674	V_{CC2}	15.75	V
Temperature, T_A			
DS1674	−55	+125	°C
DS3674	0	+70	°C

Electrical Characteristics

5V operation, (V_{CC1} = V_{CC2} = 5V, V_{CC3} = 12V); 12V operation, (V_{CC1} = 5V, V_{CC2} = 12V, V_{CC3} = V_{CC2} + (3V ±10%)); DS1674, ±10% power supply tolerances; DS3674, ±5% power supply tolerances, unless otherwise noted. (Notes 2, 3 and 4).

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IH}	Logical "1" Input Voltage			2			V
V_{IL}	Logical "0" Input Voltage					0.8	V
I_{IH}	Logical "1" Input Current	V_{IN} = 5.5V	Select Inputs		0.01	10	μA
			All Other Inputs		0.04	40	μA
I_{IL}	Logical "0" Input Current	V_{IN} = 0.4V	Select Inputs		−40	−250	μA
			All Other Inputs		−0.16	−1.0	mA
V_{CD}	Input Clamp Voltage	I_I = −12 mA			−0.8	−1.5	V
V_{OH}	Logical "1" Output Voltage	I_{OH} = −1 mA, V_{IL} = 0.8V		V_{CC2} −0.5	V_{CC2} −0.2		V
V_{OL}	Logical "0" Output Voltage	I_{OL} = 5 mA, V_{IH} = 2.0V			0.3	0.5	V
V_{OC}	Output Clamp Voltage	I_{OC} = 5 mA, V_{IL} = 0.8V			V_{CC2} +0.8	V_{CC2} +1.5	V
I_{CCH}	Supply Current Output High						
	I_{CC1}	All Inputs V_{IN} = 0V Outputs Open	V_{CC1} = Max		18	27	mA
	I_{CC2}		12V Operation		−2	−4	mA
	I_{CC3}				2	4	mA
	I_{CC2}		5V Operation		−8	−16	mA
	I_{CC3}				8	16	mA
I_{CCL}	Supply Currents Outputs Low						
	I_{CC1}	All Inputs V_{IN} = 5V Outputs Open	V_{CC1} = 5.25V		25	40	mA
	I_{CC2}		V_{CC2} = 12.6V			3	mA
	I_{CC3}		V_{CC3} = 15.75V		16	25	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS1674 and across the 0°C to +70°C range for the DS3674. All typicals are given for T_A = 25°C.

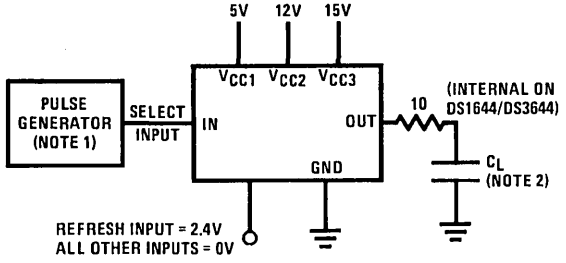
Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: For AC measurements, a 10Ω resistor must be placed in series with the output of the DS1674/DS3674.

Switching Characteristics T_A = 25°C unless otherwise noted, (Note 4), (*Figures 1, 2, 3 and 4*)

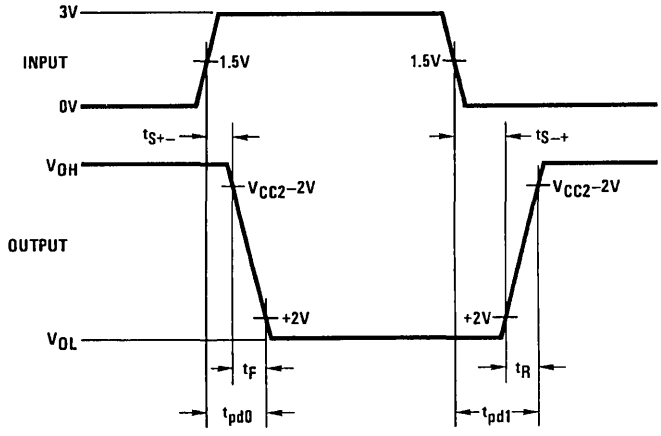
Symbol	Parameter	Conditions		Min	Typ	Max	Units
t_{s+-}	Storage Delay Negative Edge	R_D = 10Ω	C_L = 100 pF		8	11	ns
			C_L = 400 pF		12	16	ns
t_{s-+}	Storage Delay Positive Edge	R_D = 10Ω	C_L = 100 pF		10	13	ns
			C_L = 400 pF		13	16	ns
t_F	Fall Time	R_D = 10Ω	C_L = 100 pF		9	16	ns
			C_L = 400 pF		17	24	ns
t_R	Rise Time	R_D = 10Ω	C_L = 100 pF		8	12	ns
			C_L = 400 pF		13	19	ns
t_{pd0}	Propagation Delay to a Logical "0"	R_D = 10Ω	C_L = 100 pF		17	27	ns
			C_L = 400 pF		29	40	ns
t_{pd1}	Propagation Delay to a Logical "1"	R_D = 10Ω	C_L = 100 pF		18	25	ns
			C_L = 400 pF		26	35	ns

AC Test Circuits and Switching Time Waveforms



TL/F/5876–3

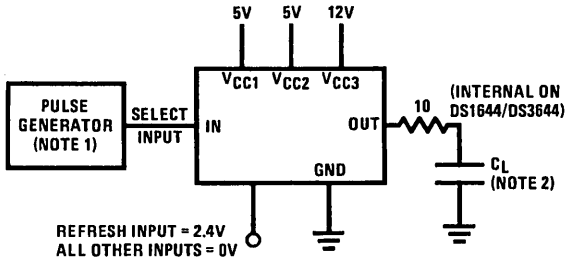
FIGURE 1. 12V Operation



TL/F/5876–4

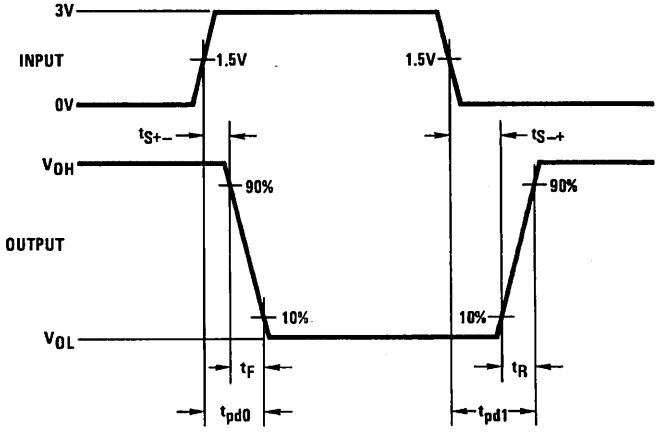
FIGURE 2. 12V Operation

AC Test Circuits and Switching Time Waveforms (Continued)



TL/F/5876–5

FIGURE 3. 5V Operation



TL/F/5876–6

FIGURE 4. 5V Operation

Note 1: The pulse generator has the following characteristics. PPR = 1 MHz, $t_R \leq 10$ ns, $Z_{OUT} = 50\Omega$.

Note 2: C_L includes probe and jig capacitance.

Truth Table

Input					Output
Enable 1	Enable 2	Select Input	Clock Input	Refresh Input	
1	X	X	X	X	0
X	1	X	X	X	0
X	X	X	1	X	0
X	X	1	X	1	0
0	0	0	0	X	1
0	0	X	0	0	1

National Semiconductor Corporation

DS16149/DS36149, DS16179/DS36179 Hex MOS Drivers

General Description

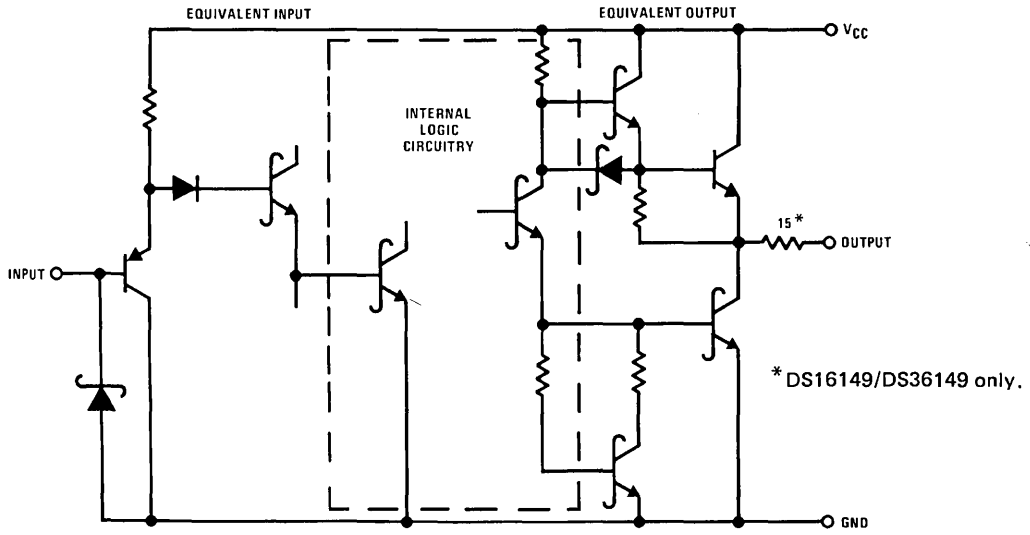
The DS16149/DS36149 and DS16179/DS36179 are Hex MOS drivers with outputs designed to drive large capacitive loads up to 500 pF associated with MOS memory systems. PNP input transistors are employed to reduce input currents allowing the large fan-out to these drivers needed in memory systems. The circuit has Schottky-clamped transistor logic for minimum propagation delay, and a disable control that places the outputs in the logic "1" state (see truth table). This is especially useful in MOS RAM applications where a set of address lines has to be in the logic "1" state during refresh.

The DS16149/DS36149 has a 15 Ω resistor in series with the outputs to dampen transients caused by the fast-switching output. The DS16179/DS36179 has a direct low impedance output for use with or without an external resistor.

Features

- High speed capabilities
  - Typ 9 ns driving 50 pF
  - Typ 29 ns driving 500 pF
- Built-in 15 Ω damping resistor (DS16149/DS36149)
- Same pin-out as DM8096 and DM74366

Schematic Diagram



TL/F/7553–1

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7.0V
Logical "1" Input Voltage	7.0V
Logical "0" Input Voltage	−1.5V
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1371 mW
Molded Package	1280 mW
Lead Temperature (Soldering 10 seconds)	300°C

*Derate cavity package 9.1 mW/°C above 25°C; derate molded package 10.2 m/W°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	5.5	V
Temperature (T_A)			
DS16149, DS16179	−55	+125	°C
DS36149, DS36179	0	+70	°C

DC Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
$V_{IN}(1)$	Logical "1" Input Voltage			2.0			V
$V_{IN}(0)$	Logical "0" Input Voltage					0.8	V
$I_{IN}(1)$	Logical "1" Input Current	V_{CC} = 5.5V, V_{IN} = 5.5V			0.1	40	μA
$I_{IN}(0)$	Logical "0" Input Current	V_{CC} = 5.5V, V_{IN} = 0.5V			−50	−250	μA
V_{CLAMP}	Input Clamp Voltage	V_{CC} = 4.5V, I_{IN} = −18 mA			−0.75	−1.2	V
V_{OH}	Logical "1" Output Voltage (No Load)	V_{CC} = 4.5V, I_{OH} = −10 μA	DS16149/DS16179	3.4	4.3		V
			DS36149/DS36179	3.5	4.3		V
V_{OL}	Logical "0" Output Voltage (No Load)	V_{CC} = 4.5V, I_{OL} = 10 μA	DS16149/DS16179		0.25	0.4	V
			DS36149/DS36179		0.25	0.35	V
V_{OH}	Logical "1" Output Voltage (With Load)	V_{CC} = 4.5V, I_{OH} = −1.0 mA	DS16149	2.4	3.5		V
			DS16179	2.5	3.5		V
			DS36149	2.6	3.5		V
			DS36179	2.7	3.5		V
V_{OL}	Logical "0" Output Voltage (With Load)	V_{CC} = 4.5V, I_{OL} = 20 mA	DS16149		0.6	1.1	V
			DS16179		0.4	0.5	V
			DS36149		0.6	1.0	V
			DS36179		0.4	0.5	V
I_{ID}	Logical "1" Drive Current	V_{CC} = 4.5V, V_{OUT} = 0V, (Note 4)			−250		mA
I_{OD}	Logical "0" Drive Current	V_{CC} = 4.5V, V_{OUT} = 4.5V, (Note 4)			150		mA
I_{CC}	Power Supply Current	V_{CC} = 5.5V	Disable Inputs = 0V, All Other Inputs = 3V		33	60	mA
			All Inputs = 0V	14		20	mA

Switching Characteristics (V_{CC} = 5V, T_A = 25°C) (Note 4)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
$t_{S\pm}$	Storage Delay Negative Edge	(*Figure 1*)	C_L = 50 pF		4.5	7	ns
			C_L = 500 pF		7.5	12	ns
$t_{S\mp}$	Storage Delay Positive Edge	(*Figure 1*)	C_L = 50 pF		5	8	ns
			C_L = 500 pF		8	13	ns
t_F	Fall Time	(*Figure 1*)	C_L = 50 pF		5	8	ns
			C_L = 500 pF		22	35	ns

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Switching Characteristics (V_{CC} = 5V, T_A = 25°C) (Note 4) (Continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
t_R	Rise Time	(*Figure 1*)	C_L = 50 pF		6	9	ns
			C_L = 500 pF		26	35	ns
t_{LH}	Delay from Disable Input to Logical "1"	R_L = 2 kΩ to Gnd, C_L = 50 pF, (*Figure 2*)			15	22	ns
t_{HL}	Delay from Disable Input to Logical "0"	R_L = 2 kΩ to V_{CC}, C_L = 50 pF, (*Figure 3*)			11	18	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

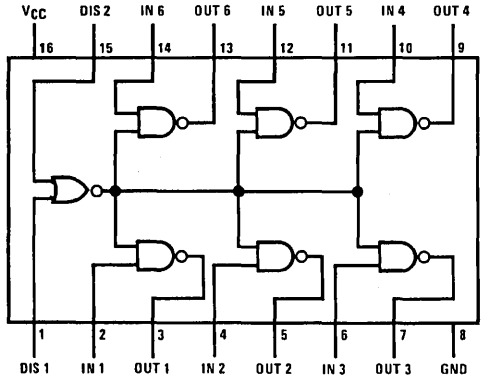
Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS16149 and DS16179 and across the 0°C to +70°C range for the DS36149 and DS36179. All typical values are for T_A = 25°C and V_{CC} = 5V.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: When measuring output drive current and switching response for the DS16179 and DS36179 a 15 Ω resistor should be placed in series with each output. This resistor is internal to the DS16149/DS36149 and need not be added.

Connection Diagram

Dual In-Line Package



TL/F/7553–2

Top View

Order Number DS16149J, DS36149J, DS16179J, DS36179J, DS36149N or DS36179N
See NS Package Number J16A or N16A

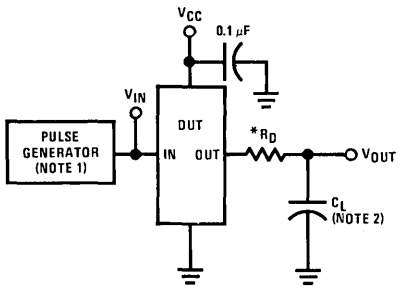
Truth Table

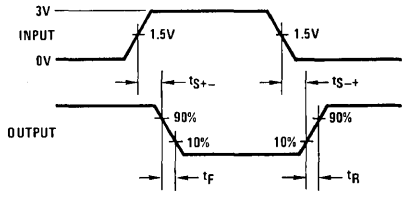
Disable Input		Input	Output
DIS 1	DIS2		
0	0	0	1
0	0	1	0
0	1	X	1
1	0	X	1
1	1	X	1

X = Don't care

AC Test Circuits and Switching Time Waveforms

$t_{S\pm}$, $t_{S\pm}$, t_R, t_F

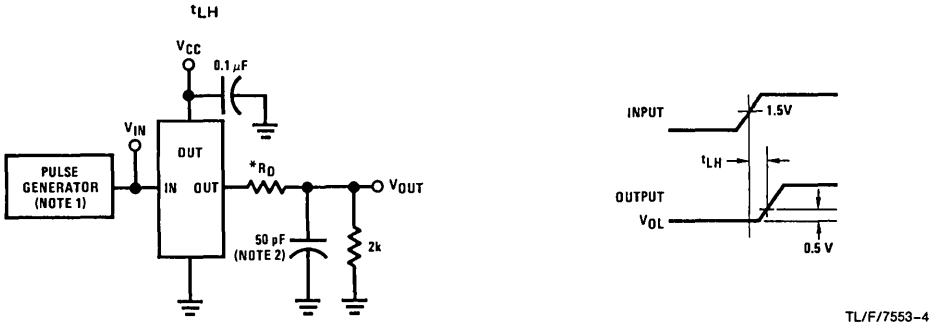




TL/F/7553–3

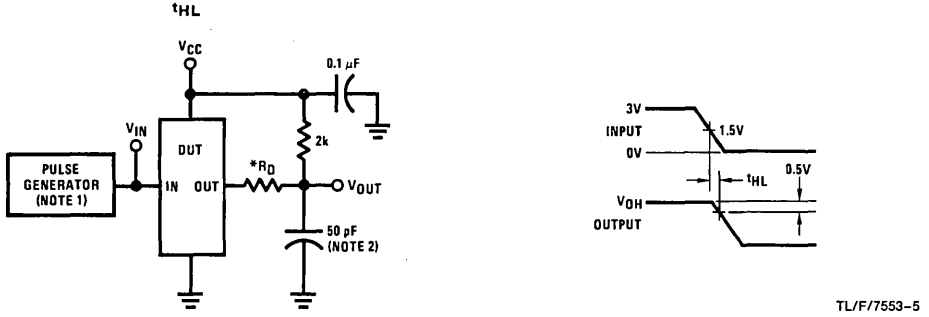
FIGURE 1

AC Test Circuits and Switching Time Waveforms (Continued)



TL/F/7553–4

FIGURE 2



TL/F/7553–5

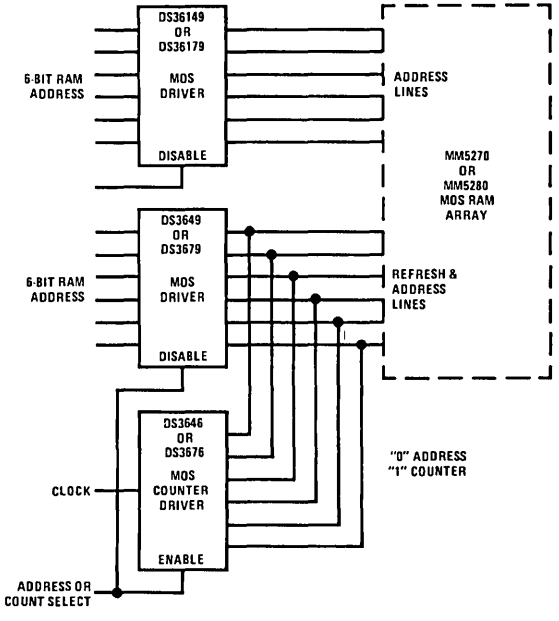
FIGURE 3

*Internal on DS16149 and DS36149

Note 1: The pulse generator has the following characteristics: Z_{OUT} = 50 Ω and PRR ≤ 1 MHz. Rise and fall times between 10% and 90% points ≤ 5 ns.

Note 2: C_L includes probe and jig capacitance.

Typical Applications



TL/F/7553–6

National Semiconductor Corporation

DS75361 Dual TTL-to-MOS Driver

General Description

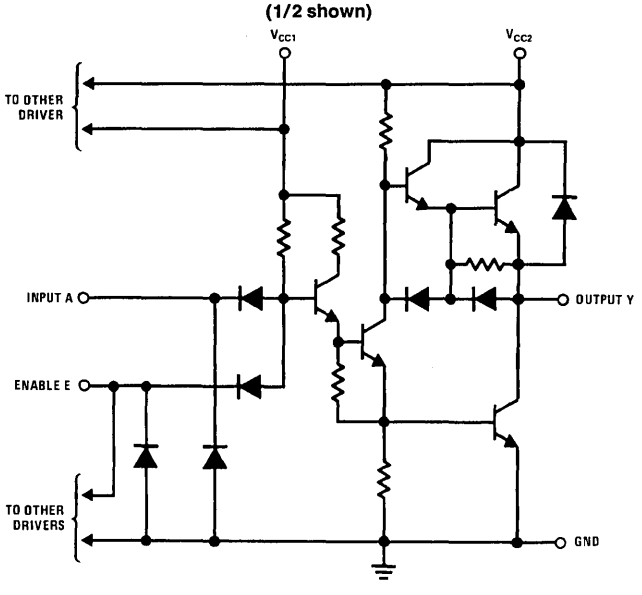
The DS75361 is a monolithic integrated dual TTL-to-MOS driver interface circuit. The device accepts standard TTL input signals and provides high-current and high-voltage output levels for driving MOS circuits. It is used to drive address, control, and timing inputs for several types of MOS RAMs including the 1103 and MM5270 and MM5280.

The DS75361 operates from standard TTL 5V supplies and the MOS V_{SS} supply in many applications. The device has been optimized for operation with V_{CC2} supply voltage from 16V to 20V; however, it is designed for use over a much wider range of V_{CC2}.

Features

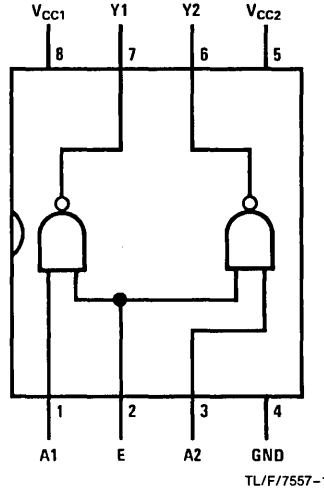
- Capable of driving high-capacitance loads
- Compatible with many popular MOS RAMs
- V_{CC2} supply voltage variable over wide range to 24V
- Diode-clamped inputs
- TTL compatible
- Operates from standard bipolar and MOS supplies
- High-speed switching
- Transient overdrive minimizes power dissipation
- Low standby power dissipation

Schematic and Connection Diagrams



TL/F/7557-3

Dual-In-Line Package



TL/F/7557-1

Top View

Order Number DS75361J or DS75361N
See NS Package Number J08A or N08E

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage Range of V_{CC1} (Note 1)	−0.5 to 7V
Supply Voltage Range of V_{CC2}	−0.5V to 25V
Input Voltage	5.5V
Inter-Input Voltage (Note 4)	5.5V
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Molded Package	1022 mW
Lead Temperature 1/16 inch from Case for 60 Seconds: J Package	300°C
Lead Temperature 1/16 inch from Case for 10 Seconds: N or P Package	200°C

Derate molded package 8.2 mW/ above about 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC1})	4.75	5.25	V
Supply Voltage (V_{CC2})	4.75	24	V
Operating Temperature (T_A)	0	+70	°C

Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IH}	High-Level Input Voltage			2			V
V_{IL}	Low-Level Input Voltage					0.8	V
V_I	Input Clamp Voltage	$I_I = -12$ mA				−1.5	V
V_{OH}	High-Level Output Voltage	$V_{IL} = 0.8V$, $I_{OH} = -50\ \mu A$		$V_{CC2} - 1$	$V_{CC2} - 0.7$		V
		$V_{IL} = 0.8V$, $I_{OH} = -10$ mA		$V_{CC2} - 2.3$	$V_{CC2} - 1.8$		V
V_{OL}	Low-Level Output Voltage	$V_{IH} = 2V$, $I_{OL} = 10$ mA			0.15	0.3	V
		$V_{CC2} = 15V$ to 24V, $V_{IH} = 2V$, $I_{OL} = 40$ mA			0.25	0.5	V
V_O	Output Clamp Voltage	$V_I = 0V$, $I_{OH} = 20$ mA				$V_{CC2} + 1.5$	V
I_I	Input Current at Maximum Input Voltage	$V_I = 5.5V$				1	mA
I_{IH}	High-Level Input Current	$V_I = 2.4V$	A Inputs			40	μA
			E Input			80	μA
I_{IL}	Low-Level Input Current	$V_I = 0.4V$	A Inputs		−1	−1.6	mA
			E Input		−2	−3.2	mA
$I_{CC1(H)}$	Supply Current from V_{CC1}, Both Outputs High	$V_{CC1} = 5.25V$, All Inputs at 0V,	$V_{CC2} = 24V$, No Load		2	4	mA
$I_{CC2(H)}$	Supply Current from V_{CC2}, Both Outputs High					0.5	mA
$I_{CC1(L)}$	Supply Current from V_{CC1}, Both Outputs Low	$V_{CC1} = 5.25V$, All Inputs at 5V,	$V_{CC2} = 24V$, No Load		16	24	mA
$I_{CC2(L)}$	Supply Current from V_{CC2}, Both Outputs Low				7	11	mA
$I_{CC2(S)}$	Supply Current from V_{CC2}, Stand-by Condition	$V_{CC1} = 0V$, All Inputs at 5V,	$V_{CC2} = 24V$, No Load			0.5	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C range for the DS75361. All typical values are for $T_A = 25°C$ and $V_{CC1} = 5V$ and $V_{CC2} = 20V$.

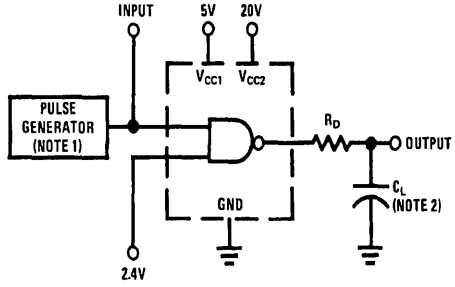
Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: This rating applies between the A input of either driver and the common E input.

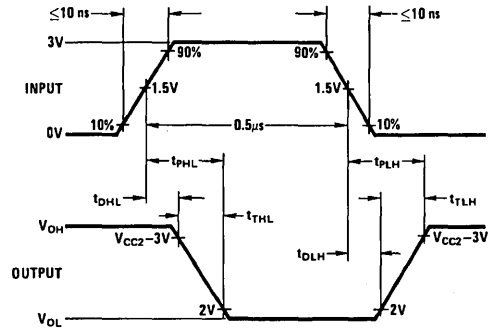
Switching Characteristics V_{CC1} = 5V, V_{CC2} = 20V, T_A = 25°C

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{DLH}	Delay Time, Low-to-High Level Output	C_L = 390 pF, R_D = 10Ω *(Figure 1)*		11	20	ns
t_{DHL}	Delay Time, High-to-Low Level Output			10	18	ns
t_{TLH}	Transition Time, Low-to-High Level Output			25	40	ns
t_{THL}	Transition Time, High-to-Low Level Output			21	35	ns
tPLH	Propagation Delay Time, Low-to-High Level Output		10	36	55	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output		10	31	47	ns

AC Test Circuit and Switching Time Waveforms



TL/F/7557–4



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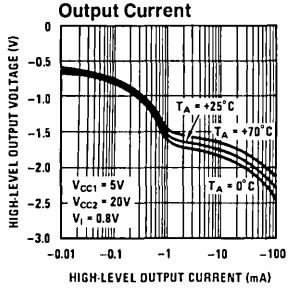
Note 1: The pulse generator has the following characteristics: PRR = 1 MHz, Z_{OUT} = 50Ω.

Note 2: C_L includes probe and jig capacitance.

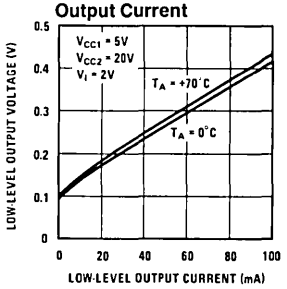
FIGURE 1. Switching Times, Each Driver

Typical Performance Characteristics

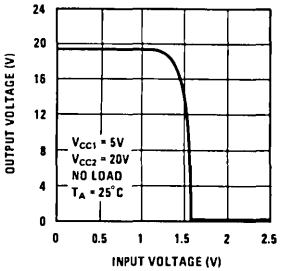
High-Level Output Voltage vs Output Current



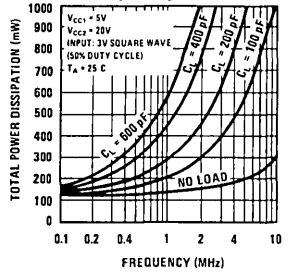
Low-Level Output Voltage vs Output Current



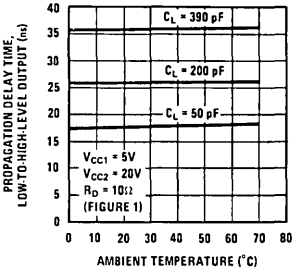
Voltage Transfer Characteristics



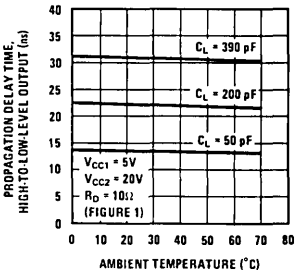
Total Dissipation (Both Drivers) vs Frequency



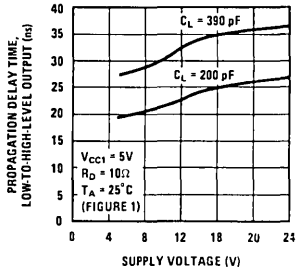
Propagation Delay Time, Low-to-High Level Output vs Ambient Temperature



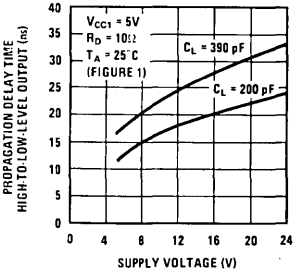
Propagation Delay Time, High-to-Low Level Output vs Ambient Temperature



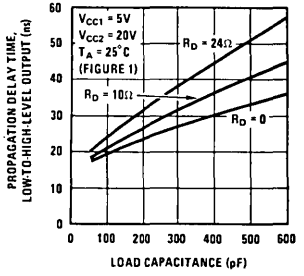
Propagation Delay Time, Low-to-High Level Output vs V_{CC2} Supply Voltage



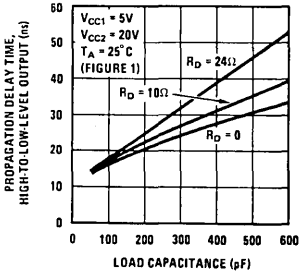
Propagation Delay Time, High-to-Low Level Output vs V_{CC2} Supply Voltage



Propagation Delay Time, Low-to-High Level Output vs Load Capacitance



Propagation Delay Time, High-to-Low Level Output vs Load Capacitance



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Typical Applications

The fast switching speeds of this device may produce undesirable output transient overshoot because of load or wiring inductance. A small series damping resistor may be used to reduce or eliminate this output transient overshoot. The optimum value of the damping resistor to use depends on the specific load characteristics and switching speed. A typical value would be between 10Ω and 30Ω *(Figure 3)*.

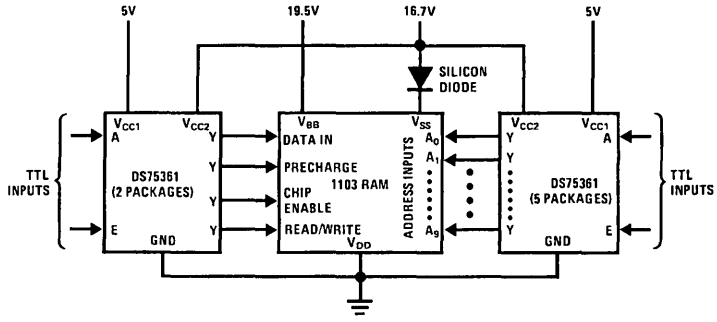

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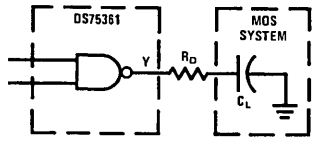
FIGURE 2. Interconnection of DS75361 Devices with 1103 RAM



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Note: $R_D \approx 10\Omega$ to 30Ω (Optional).

FIGURE 3. Use of Damping Resistor to Reduce or Eliminate Output Transient Overshoot in Certain DS75361 Applications

Thermal Information

POWER DISSIPATION PRECAUTIONS

Significant power may be dissipated in the DS75361 driver when charging and discharging high-capacitance loads over a wide voltage range at high frequencies. The total dissipation curve shows the power dissipated in a typical DS75361 as a function of load capacitance and frequency. Average power dissipated by this driver can be broken into three components:

$$P_{T(AV)} = P_{DC(AV)} + P_{C(AV)} + P_{S(AV)}$$

where $P_{DC(AV)}$ is the steady-state power dissipation with the output high or low, $P_{C(AV)}$ is the power level during charging or discharging of the load capacitance, and $P_{S(AV)}$ is the power dissipation during switching between the low and high levels. None of these include energy transferred to the load and all are averaged over a full cycle.

The power components per driver channel are:

$$P_{DC(AV)} = \frac{P_L t_L + P_H t_H}{T}$$

$$P_{C(AV)} \approx C V_C^2 f$$

$$P_{S(AV)} = \frac{P_{LH} t_{LH} + P_{HL} t_{HL}}{T}$$

where the times are defined in *Figure 4*.

P_L, P_H, P_{LH}, and P_{HL} are the respective instantaneous levels of power dissipation and C is load capacitance.

The DS75361 is so designed that P_S is a negligible portion of P_T in most applications. Except at very high frequencies, $t_L + t_H \gg t_{LH} + t_{HL}$ so that P_S can be neglected. The total dissipation curve for no load demonstrates this point. The power dissipation contributions from both channels are then added together to obtain total device power.

The following example illustrates this power calculation technique. Assume both channels are operating identically with C = 200 pF, f = 2 MHz, V_{CC1} = 5V, V_{CC2} = 20V, and duty cycle = 60% outputs high ($t_H/T = 0.6$). Also, assume V_{OH} = 19.3V, V_{OL} = 0.1V, P_S is negligible, and that the current from V_{CC2} is negligible when the output is high.

On a per-channel basis using data sheet values:

$$P_{DC(AV)} = \left[(5V)\left(\frac{2\text{ mA}}{2}\right) + (20V)\left(\frac{0\text{ mA}}{2}\right) \right](0.6) + \left[(5V)\left(\frac{16\text{ mA}}{2}\right) + (20V)\left(\frac{7\text{ mA}}{2}\right) \right](0.4)$$

$P_{DC(AV)}$ = 47 mW per channel

$P_{C(AV)} \approx$ (200 pF) $(19.2V)^2$ (2 MHz)

$P_{C(AV)} \approx$ 148 mW per channel.

For the total device dissipation of the two channels:

$P_{T(AV)} \approx 2\,(47 + 148)$

$P_{T(AV)} \approx$ 390 mW typical for total package.

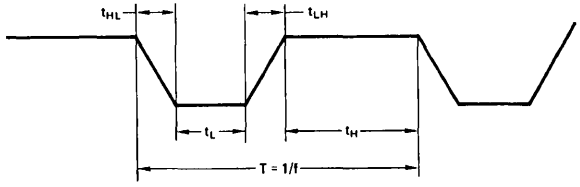

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FIGURE 4. Output Voltage Waveform

National Semiconductor Corporation

PRELIMINARY

DS75365 Quad TTL-to-MOS Driver

General Description

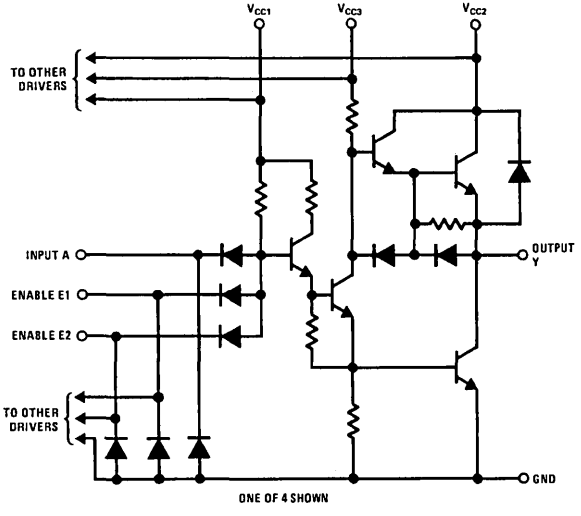
The DS75365 is a quad monolithic integrated TTL-to-MOS driver and interface circuit that accepts standard TTL input signals and provides high-current and high-voltage output levels suitable for driving MOS circuits. It is used to drive address, control, and timing inputs for several types of MOS RAMs including the 1103.

The DS75365 operates from the TTL 5V supply and the MOS V_{SS} and V_{BB} supplies in many applications. This device has been optimized for operation with V_{CC2} supply voltage from 16V to 20V, and with nominal V_{CC3} supply voltage from 3V to 4V higher than V_{CC2}. However, it is designed so as to be usable over a much wider range of V_{CC2} and V_{CC3}. In some applications the V_{CC3} power supply can be eliminated by connecting the V_{CC3} to the V_{CC2} pin.

Features

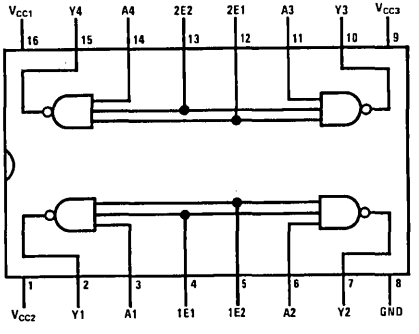
- Quad positive-logic NAND TTL-to-MOS driver
- Versatile interface circuit for use between TTL and high-current, high-voltage systems
- Capable of driving high-capacitance loads
- Compatible with many popular MOS RAMs
- Interchangeable with Intel 3207
- V_{CC2} supply voltage variable over side range to 24V maximum
- V_{CC3} supply voltage pin available
- V_{CC3} pin can be connected to V_{CC2} pin in some applications
- TTL compatible diode-clamped inputs
- Operates from standard bipolar and MOS supply voltages
- Two common enable inputs per gate-pair
- High-speed switching
- Transient overdrive minimizes power dissipation
- Low standby power dissipation

Schematic and Connection Diagrams



TL/F/7560–1

Dual-In-Line Package



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Top View
Positive Logic: $Y = \overline{A \cdot E1 \cdot E2}$

Order Number DS75365J or DS75365N
See NS Package Number J16A or N16A

5

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage Range of V_{CC1}	−0.5V to 7V
Supply Voltage Range of V_{CC2}	−0.5V to 25V
Supply Voltage Range of V_{CC3}	−0.5V to 30V
nput Voltage	5.5V
Inter-Input Voltage (Note 4)	5.5V
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1509 mW
Molded Package	1476 mW
Lead Temperature (Soldering, 10 sec)	300°C

* Derate cavity package 10.1 mW/°C above 25°C; derate molded package 11.8 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC1})	4.75	5.25	V
Supply Voltage (V_{CC2})	4.75	24	V
Supply Voltage (V_{CC3})	V_{CC2}	28	V
Voltage Difference Between Supply Voltages: $V_{CC3}-V_{CC2}$	0	10	V
Operating Ambient Temperature Range (T_A)	0	70	°C

Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IH}	High-Level Input Voltage			2			V
V_{IL}	Low-Level Input Voltage					0.8	V
V_I	Input Clamp Voltage	$I_I = -12$ mA				−1.5	V
V_{OH}	High-Level Output Voltage	$V_{CC3} = V_{CC2} + 3V$, $V_{IL} = 0.8V$, $I_{OH} = -100\ \mu A$		$V_{CC2} - 0.3$	$V_{CC2} - 0.1$		V
		$V_{CC3} = V_{CC2} + 3V$, $V_{IL} = 0.8V$, $I_{OH} = -10$ mA		$V_{CC2} - 1.2$	$V_{CC2} - 0.9$		V
		$V_{CC3} = V_{CC2}$, $V_{IL} = 0.8V$, $I_{OH} = -50\ \mu A$		$V_{CC2} - 1$	$V_{CC2} - 0.7$		V
		$V_{CC3} = V_{CC2}$, $V_{IL} = 0.8V$, $I_{OH} = -10$ mA		$V_{CC2} - 2.3$	$V_{CC2} - 1.8$		V
V_{OL}	Low-Level Output Voltage	$V_{IH} = 2V$, $I_{OL} = 10$ mA			0.15	0.3	V
		$V_{CC3} = 15V$ to 28V, $V_{IH} = 2V$, $I_{OL} = 40$ mA			0.25	0.5	V
V_O	Output Clamp Voltage	$V_I = 0V$, $I_{OH} = 20$ mA				$V_{CC2} + 1.5$	V
I_I	Input Current at Maximum Input Voltage	$V_I = 5.5V$				1	mA
I_{IH}	High-Level Input Current	$V_I = 2.4V$	A Inputs			40	μA
			E1 and E2 Inputs			80	μA
I_{IL}	Low-Level Input Current	$V_I = 0.4V$	A Inputs		−1	−1.6	mA
			E1 and E2 Inputs		−2	−3.2	mA
$I_{CC1(H)}$	Supply Current from V_{CC1}, All Outputs High	$V_{CC1} = 5.25V$, $V_{CC2} = 24V$ $V_{CC3} = 28V$, All Inputs at 0V, No Load			4	8	mA
$I_{CC2(H)}$	Supply Current from V_{CC2}, All Outputs High				−2.2	+0.25	mA
					−2.2	−3.2	mA
$I_{CC3(H)}$	Supply Current from V_{CC3}, All Outputs High				2.2	3.5	mA
$I_{CC1(L)}$	Supply Current from V_{CC1}, All Outputs Low	$V_{CC1} = 5.25V$, $V_{CC2} = 24V$ $V_{CC3} = 28V$, All Inputs at 5V, No Load			31	47	mA
$I_{CC2(L)}$	Supply Current from V_{CC2}, All Outputs Low					3	mA
$I_{CC3(L)}$	Supply Current from V_{CC3}, All Outputs Low				16	25	mA
$I_{CC2(H)}$	Supply Current from V_{CC2}, All Outputs High	$V_{CC1} = 5.25V$, $V_{CC2} = 24V$ $V_{CC3} = 24V$, All Inputs at 0V, No Load				0.25	mA
$I_{CC3(H)}$	Supply Current from V_{CC3}, All Outputs High					0.5	mA

Electrical Characteristics (Notes 2, 3) (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$I_{CC2(S)}$	Supply Current from V_{CC2}, Stand-By Condition	V_{CC1} = 0V, V_{CC2} = 24V V_{CC3} = 24V, All Inputs at 5V, No Load			0.25	mA
$I_{CC3(S)}$	Supply Current from V_{CC3}, Stand-By Condition				0.5	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified, min/max limits apply across the 0°C to +70°C range for the DS75365. All typical values are for T_A = 25°C and V_{CC1} = 5V and V_{CC2} = 20V and V_{CC3} = 24V.

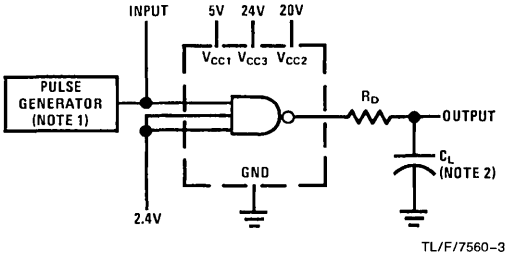
Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: This rating applies between any two inputs of any one of the gates.

Switching Characteristics V_{CC1} = 5V, V_{CC2} = 20V, V_{CC3} = 24V, T_A = 25°C

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{DLH}	Delay Time, Low-to-High Level Output	C_L = 200 pF R_D = 24Ω (*Figure 1*)		11	20	ns
t_{DHL}	Delay Time, High-to-Low Level Output			10	18	ns
t_{TLH}	Transition Time, Low-to-High Level Output			20	33	ns
t_{THL}	Transition Time, High-to-Low Level Output			20	33	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output		10	31	48	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output		10	30	46	ns

AC Test Circuit and Switching Time Waveforms



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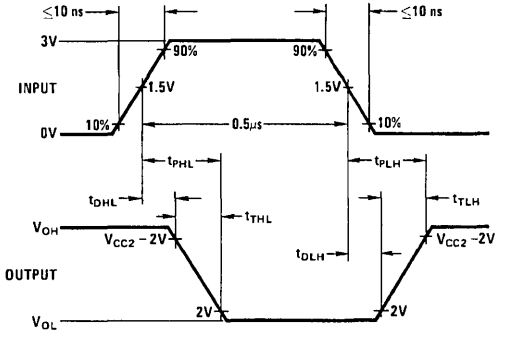

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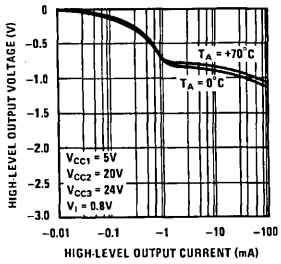
Note 1: The pulse generator has the following characteristics: PRR = 1 MHz, Z_{OUT} = 58Ω.

Note 2: C_L includes probe and jig capacitance.

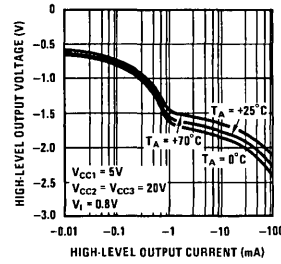
FIGURE 1. Switching Times, Each Driver

Typical Performance Characteristics

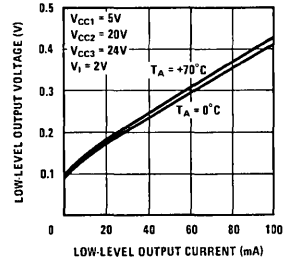
High-Level Output Voltage vs Output Current



High-Level Output Voltage vs Output Current



Low-Level Output Voltage Output Current



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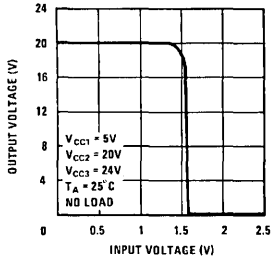
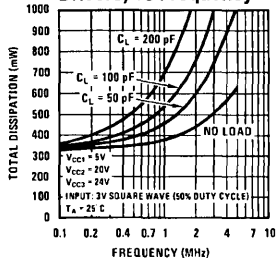
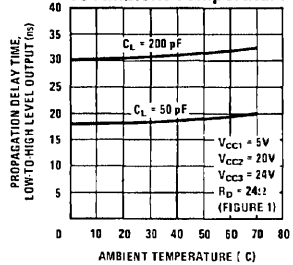
Voltage Transfer Characteristics



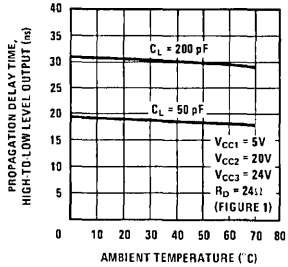
Total Dissipation (All Four Drivers) vs Frequency



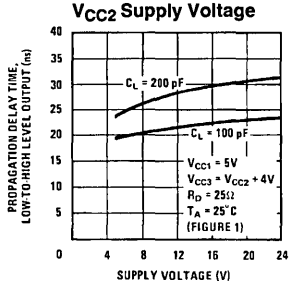
Propagation Delay Time, Low-to-High Level Output vs Ambient Temperature



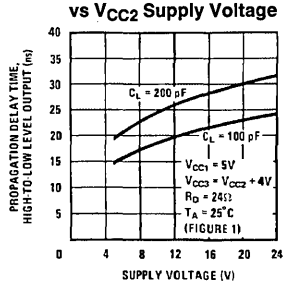
Propagation Delay Time, High-to-Low Level Output vs Ambient Temperature



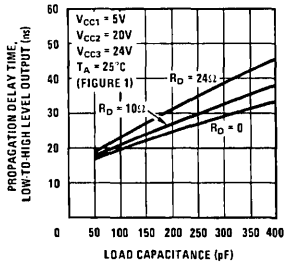
Propagation Delay Time, Low-to-High Level Output vs V_{CC2} Supply Voltage



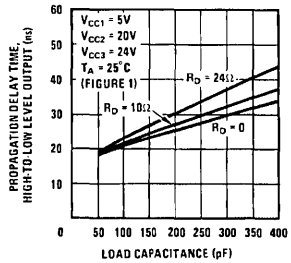
Propagation Delay Time, High-to-Low Level Output vs V_{CC2} Supply Voltage



Propagation Delay Time, Low-to-High Level Output vs Load Capacitance



Propagation Delay Time, High-to-Low Level Output vs Load Capacitance



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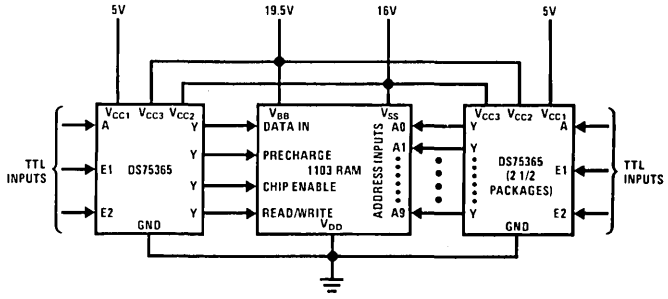
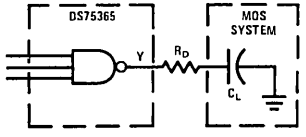


TL/F/7560-7

FIGURE 2. Interconnection of DS75365 Devices with 1103-Type Silicon-Gate MOS RAM

Typical Applications

The fast switching speeds of this device may produce undesirable output transient overshoot because of load or wiring inductance. A small series damping resistor may be used to reduce or eliminate this output transient overshoot. The optimum value of the damping resistor depends on the specific load characteristics and switching speed. A typical value would be between 10Ω and 30Ω (*Figure 3*).



Note: $R_D \cong 10\Omega$ to 30Ω (Optional)

TL/F/7560-8

FIGURE 3. Use of Damping Resistor to Reduce or Eliminate Output Transient Overshoot in Certain DS75365 Applications

Thermal Information

POWER DISSIPATION PRECAUTIONS

Significant power may be dissipated in the DS75365 driver when charging and discharging high-capacitance loads over a wide voltage range at high frequencies. The total dissipation curve shows the power dissipated in a typical DS75365 as a function of load capacitance and frequency. Average power dissipation by this driver can be broken into three components:

$$P_{T(AV)} = P_{DC(AV)} + P_{C(AV)} + P_{S(AV)}$$

where $P_{DC(AV)}$ is the steady-state power dissipation with the output high or low, $P_{C(AV)}$ is the power level during charging or discharging of the load capacitance, and $P_{S(AV)}$ is the power dissipation during switching between the low and high levels. None of these include energy transferred to the load and all are averaged over a full cycle.

The power components per driver channel are:

$$P_{DC(AV)} = \frac{P_L t_L + P_H t_H}{T}$$

$$P_{C(AV)} \cong C\,V_C{}^2 f$$

$$P_{S(AV)} = \frac{P_{LH} t_{LH} + P_{HL} t_{HL}}{T}$$

where the times are as defined in *Figure 4*.

P_L, P_H, P_{LH}, and P_{HL} are the respective instantaneous levels of power dissipation and C is load capacitance.

The DS75365 is so designed that P_S is a negligible portion of P_T in most applications. Except at very high frequencies, $t_L + t_H \gg t_{LH} + t_{HL}$ so that P_S can be neglected. The total dissipation curve for no load demonstrates this point. The power dissipation contributions from all four channels are then added together to obtain total device power.

The following example illustrates this power calculation technique. Assume all four channels are operating identically with C = 100 pF, f = 2 MHz, V_{CC1} = 5V, V_{CC2} = 20V, V_{CC3} = 24V and duty cycle = 60% outputs high (t_H/T = 0.6). Also, assume V_{OH} = 20V, V_{OL} = 0.1V, P_S is negligible, and that the current from V_{CC2} is negligible when the output is low.

On a per-channel basis using data sheet values:

$$P_{DC(AV)} = \left[(5V)\left(\frac{4\text{ mA}}{4}\right) + (20V)\left(\frac{-2.2\text{ mA}}{4}\right) + (24V)\left(\frac{2.2\text{ mA}}{4}\right)\right](0.6) + \left[(5V)\left(\frac{31\text{ mA}}{4}\right) + (20V)\left(\frac{0\text{ mA}}{4}\right) + (24V)\left(\frac{16\text{ mA}}{4}\right)\right](0.4)$$

$P_{DC(AV)}$ = 58 mW per channel

$P_{C(AV)} \cong$ (100 pF) (19.9V)^2 (2 MHz)

$P_{C(AV)} \cong$ 79 mW per channel.

For the total device dissipation of the four channels:

$P_{T(AV)} \cong 4\,(58 + 79)$

$P_{T(AV)} \cong$ 548 mW typical for total package.

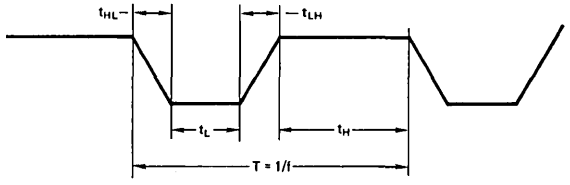


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FIGURE 4. Output Voltage Waveform

Applying Modern Clock Drivers to MOS Memories

National Semiconductor Corp.
Application Note 76
B. Siegel
M. Scott

INTRODUCTION

MOS memories present unique system and circuit challenges to the engineer since they require precise timing of input waveforms. Since these inputs present large capacitive loads to drive circuits, it is often that timing problems are not discovered until an entire system is constructed. This paper covers the practical aspects of using modern clock drivers in MOS memory systems. Information includes selection of packages and heat sinks, power dissipation, rise and fall time considerations, power supply decoupling, system clock line ringing and crosstalk, input coupling techniques, and example calculations. Applications covered include driving various types shift registers and RAMs (Random Access Memories) using logical control as well as other techniques to assure correct non-overlap of timing waveforms.

Although the information given is generally applicable to any type of driver, monolithic integrated circuit drivers, the DS0025, DS0026 and DS0056 are selected as examples because of their low cost.

The DS0025 was the first monolithic clock driver. It is intended for applications up to one megacycle where low cost is of prime concern. Table I illustrates its performance while Appendix I describes its circuit operation. Its monolithic, rather than hybrid or module construction, was made possible by a new high voltage gold doped process utilizing a collector sinker to minimize $V_{CE\ SAT}$.

The DS0026 is a high speed, low cost, monolithic clock driver intended for applications above one megacycle. Table II illustrates its performance characteristics while its unique circuit design is presented in Appendix II. The DS0056 is a variation of the DS0026 circuit which allows the system designer to modify the output performance of the circuit. The DS0056 can be connected (using a second power supply) to increase the positive output voltage level and reduce the effect of cross coupling capacitance between the clock lines in the system. Of course the above are just examples of the many different types that are commercially available. Other National Semiconductor MOS interface circuits are listed in Appendix III.

The following section will hopefully allow the design engineer to select and apply the best circuit to his particular application while avoiding common system problems.

PRACTICAL ASPECTS OF USING MOS CLOCK DRIVERS

Package and Heat Sink Selection

Package type should be selected on power handling capability, standard size, ease of handling, availability of sockets, ease or type of heat sinking required, reliability and cost. Power handling capability for various packages is illustrated in Table III. The following guidelines are recommended:

TABLE I. DS0025 Characteristics

Parameter	Conditions ($V^+ - V^-$) = 17V	Value	Units
t_{ON}		15	ns
t_{OFF}	C_{IN} = 0.0022 μF, R_{IN} = 0Ω	30	ns
t_r	C_L = 0.0001 μF, R0 = 50Ω	25	ns
t_f		150	ns
Positive Output Voltage Swing	$V_{IN} - V^-$ = 0V, I_{OUT} = −1 mA	$V^+ - 0.7$	V
Negative Output Voltage Swing	I_{IN} = 10 mA, I_{OUT} = 1 mA	$V^- + 1.0$	V
On Supply Current (V^+)	I_{IN} = 10 mA	17	mA

TABLE II. DS0026 Characteristics

Parameter	Conditions ($V^+ - V^-$) = 17V	Value	Units
t_{ON}		7.5	ns
t_{OFF}	C_{IN} = 0.001 μF, R_{IN} = 0Ω	7.5	ns
t_r	R0 = 50Ω, C_L = 1000 pF	25	ns
t_f		25	ns
Positive Output Voltage Swing	$V_{IN} - V^-$ = 0V, I_{OUT} = −1 mA	$V^+ - 0.7$	V
Negative Output Voltage Swing	I_{IN} = 10 mA, I_{OUT} = 1 mA	$V^- + 0.5$	V
On Supply Current (V^+)	I_{IN} = 10 mA	28	mA

The TO-5 ("H") package is rated at 750 mW still air (derate at 200°C/W above 25°C) soldered to PC board. This popular cavity package is recommended for small systems. Low cost (about 10 cents) clip-on heat sink increases driving capability by 50%.

The 8-pin ("N") molded mini-DIP is rated at 600 mW still air (derate at 90°C/W above 25°C soldered to PC board (derate at 1.39W). Constructed with a special copper lead frame, this package is recommended for medium size commercial systems particularly where automatic insertion is used. (Please note for prototype work, that this package is only rated at 600 mW when mounted in a socket and not one watt until it is soldered down.)

The TO-8 ("G") package is rated at 1.5W still air (derate at 100°C/W above 25°C) and 2.3W with clip-on heat sink (Wakefield type 215-1.9 or equivalent—derate at 15 mW/°C). Selected for its power handling capability and moderate cost, this hermetic package will drive very large systems at the lowest cost per bit.

Power Dissipation Considerations

The amount of registers that can be driven by a given clock driver is usually limited first by internal power dissipation. There are four factors:

1. Package and heat sink selection
2. Average dc power, P_{DC}
3. Average ac power, P_{AC}
4. Numbers of drivers per package, n

From the package heat sink, and maximum ambient temperature one can determine P_{MAX}, which is the maximum internal power a device can handle and still operate reliably. The total average power dissipated in a driver is the sum of dc power and ac power in each driver times the number of drivers. The total of which must be less than the package power rating.

$$P_{DISS} = n \times (P_{AC} + P_{DC}) \leq P_{MAX} \quad (1)$$

Average dc power has three components: input power, power in the "OFF" state (MOS logic "0") and power in the "ON" state (MOS logic "1").

$$P_{DC} = P_{IN} + P_{OFF} + P_{ON} \quad (2)$$

For most types of clock drivers, the first two terms are negligible (less than 10 mW) and may be ignored.

Thus:

$$P_{DC} \cong P_{ON} = \frac{(V^+ - V^-)^2}{Req} \times (DC)$$

where:

$V^+ - V^-$ = Total voltage across the driver

Req = Equivalent device resistance in the "ON" state

$$= V^+ - V^-/I_{S(ON)} \quad (3)$$

DC = Duty Cycle

$$= \frac{\text{"ON" Time}}{\text{"ON" Time} + \text{"OFF" Time}}$$

For the DS0025, Req is typically 1 kΩ while Req is typically 600Ω for the DS0026. Graphical solutions for P_{DC} appear in *Figure 1*. For example if $V^+ = +5V$, $V^- = -12V$, Req = 500Ω, and DC = 25%, then P_{DC} = 145 mW. However, if the duty cycle was only 5%, P_{DC} = 29 mW. Thus to maximize the number of registers that can be driven by a given clock driver as well as minimizing average system power, the minimum allowable clock pulse width should be used for the particular type of MOS register.

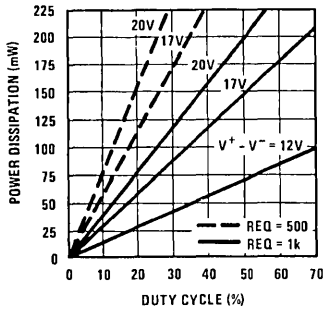

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FIGURE 1. P_{DC} vs Duty Cycle

In addition to P_{DC}, the power driving a capacitive load is given approximately by:

$$P_{AC} = (V^+ - V^-)^2 \times f \times C_L \quad (4)$$

where:

f = Operating frequency

C_L = Load capacitance

Graphical solutions for P_{AC} are illustrated in *Figure 2*. Thus, any type of clock driver will dissipate internally 290 mW per MHz per thousand pF of load. At 5 MHz, this would be 1.5W for a 1000 pF load. For long shift register applications, the driver with the highest package power rating will drive the largest number of bits.

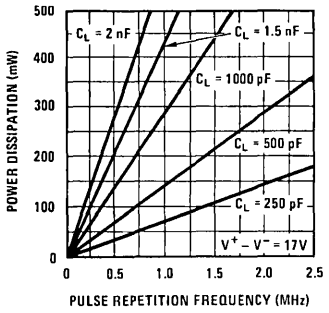

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FIGURE 2. P_{AC} vs PRF

Combining equations (1), (2), (3) and (4) yields a criterion for the maximum load capacitance which can be driven by a given driver:

$$C_L \leq \frac{1}{f}\left[\frac{P_{MAX}}{n(V^+ - V^-)^2} - \frac{(DC)}{Req}\right] \quad (5)$$

As an example, the DS0025CN can dissipate 890 mW at T_A = 70°C when soldered to a printed circuit board. Req is approximately equal to 1k. For $V^+ = 5V$, $V^- = -12V$, f = 1 MHz, and dc = 20%, C_L is:

$$C_L \leq \frac{1}{10^6}\left[\frac{(890 \times 10^{-3})}{(2)(17)^2} - \frac{0.2}{1 \times 10^3}\right]$$

$C_L \leq 1340$ pF (each driver)

A typical application might involve driving an MM5013 triple 64-bit shift register with the DS0025. Using the conditions above and the clock line capacitance of the MM5013 of 60 pF, a single DS0025 can drive 1340 pF/60 pF, or approximately 20 MM5013's.

In summary, the maximum capacitive load that any clock driver can drive is determined by package type and rating, heat sink technique, maximum system ambient temperature, ac power (which depends on frequency, voltage across the device, and capacitive load) and dc power (which is principally determined by duty cycle).

Rise and Fall Time Considerations

In general rise and fall times are determined by (a) clock driver design, (b) reflected effects of heavy external load, and (C) peak transient current available. Details of these are included in Appendixes I and II. *Figures AI-3, AI-4, AII-2* and *AIII-3* illustrate performance under various operating conditions. Under light loads, performance is determined by internal design of the driver; for moderate loads, by load C_L being reflected (usually as $C_{L/\beta}$) into the driver; and for large loads by peak output current where:

$$\frac{\Delta V}{\Delta T} = \frac{I_{OUT\ PEAK}}{C_L}$$

Logic rise and fall times must be known in order to assure non-overlap of system timing.

Note the definition of rise and fall times in this application note follow the convention that rise time is the transition from logic "0" to logic "1" levels and vice versa for fall times. Since MOS logic is inverted from normal TTL, "rise time" as used in this note is "voltage fall" and "fall time" is "voltage rise".

Power Supply Decoupling

Although power supply decoupling is a wide spread and accepted practice, the question often rises as to how much and how often. Our own experience indicates that each clock driver should have at least 0.1 μF decoupling to ground at the V^+ and V^- supply leads. Capacitors should be located as close as is physically possible to each driver. Capacitors should be non-inductive ceramic discs. This decoupling is necessary because currents in the order of 0.5 to 1.5 amperes flow during logic transitions.

There is a high current transient (as high as 1.5A) during the output transition from high to low through the V^- lead. If the external interconnecting wire from the driving circuit to the V^- lead is electrically long or has significant dc resistance, the current transient will appear as negative feedback and subtract from the switching response. To minimize this effect, short interconnecting wires are necessary and high frequency power supply decoupling capacitors are required if V^- is different from the ground of the driving circuit.

Clock Line Overshoot and Cross Talk

Overshoot: The output waveform of a clock driver can, and often does, overshoot. It is particularly evident on faster drivers. The overshoot is due to the finite inductance of the clock lines. Since most MOS registers require that clock signals not exceed V_{SS}, some method must be found in large systems to eliminate overshoot. A straightforward approach is shown in *Figure 3*. In this instance, a small damping resistor is inserted between the output of the clock driver and the load. The critical value for R_S is given by:

$$R_S = 2\sqrt{\frac{L_S}{C_L}} \qquad (6)$$

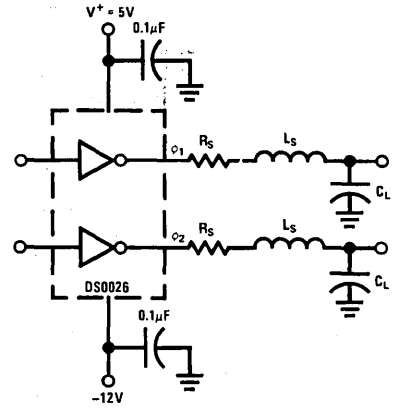

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FIGURE 3. Use of Damping Resistor to Eliminate Clock Overshoot

In practice, analytical determination of the value for R_S is rather difficult. However, R_S is readily determined empirically, and typical values range in value between 10 and 50Ω.

Use of the damping resistor has the added benefit of essentially unloading the clock driver; hence a greater number of loads may often be driven by a given driver. In the limit, however, the maximum value that may be used for R_S will be determined by the maximum allowable rise and fall time needed to assure proper operation of the MOS register. In short:

$$t_{r(MAX)} = t_{f(MAX)} \leq 2.2\ R_S\ C_L \qquad (7)$$

One last word of caution with regard to use of a damping resistor should be mentioned. The power dissipated in R_S can approach $(V^+ - V^-)^2\ fC_L$ and accordingly the resistor wattage rating may be in excess of 1W. There are, obviously, applications where degradation of t_r and t_f by use of damping resistors cannot be tolerated. *Figure 4* shows a practical circuit which will limit overshoot to a diode drop. The clamp network should physically be located in the center of the distributed load in order to minimize inductance between the clamp and registers.

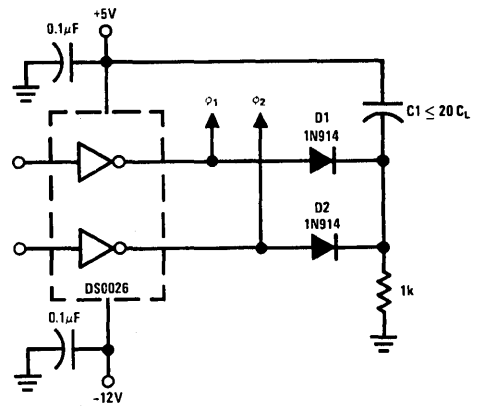

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FIGURE 4. Use of High Speed Clamp to Limit Clock Overshoot

Cross Talk: Voltage spikes from ϕ_1 may be transmitted to ϕ_2 (and vice versa) during the transition of ϕ_1 to MOS logic "1". The spike is due to mutual capacitance between clock lines and is, in general, aggravated by long clock lines when numerous registers are being driven. *Figure 5* illustrates the problem.

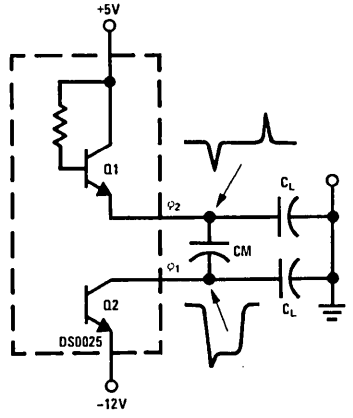

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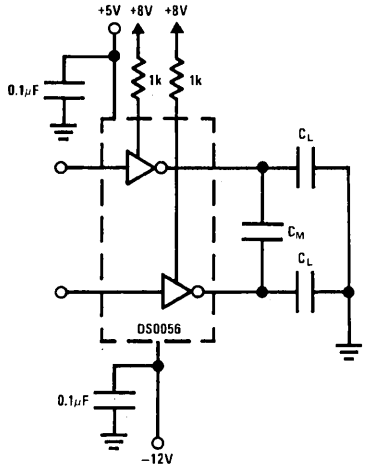
FIGURE 5. Clock Line Cross Talk

The negative going transition of ϕ_1 (to MOS logic "1") is capacitively coupled via C_M to ϕ_2. Obviously, the larger C_M is, the larger the spike. Prior to ϕ_1's transition, Q1 is "OFF" since only μA are drawn from the device.

The DS0056 connected as shown in *Figure 6* will minimize the effect of cross talk. The external resistors to the higher power supply pull base of a Q1 up to a higher level and forward bias the collector base junction of Q1. In this bias condition the output impedance of the DS0056 is very low and will reduce the amplitude of the spikes.



TL/F/7322-6

FIGURE 6. Use of DS0056 to Minimize Clock Line Cross Talk

Input Capacitive Coupling

Generally, MOS shift registers are powered from +5V and −12V supplies. A level shift from the TTL levels (+5V) to MOS levels (−12V) is therefore required. The level shift could be made utilizing a PNP transistor or zener diode. The disadvantage to dc level shifting is the increased power dissipation and propagation delay in the level shifting device. Both the DS0025, DS0026 and DS0056 utilize input capacitors when level shifting from TTL to negative MOS capacitors. Not only do the capacitors perform the level shift function without inherent delay and power dissipation, but as will be shown later, the capacitors also enhance the performance of these circuits.

CONCLUSION

The practical aspects of driving MOS memories with low cost clock drivers has been discussed in detail. When the design guide lines set forth in this paper are followed and reasonable care is taken in circuit layout, the DS0025, DS0026 and DS0056 provide superior performance for most MOS input interface applications.

REFERENCES

1. Bert Mitchell, *"New MOS Clock Driver for MOS Shift Registers,"* National Semiconductor, AN-18, March 1969.
2. John Vennard, *"MOS Clock Drivers,"* National Semiconductor, MB-9, December 1969.
3. Dale Mrazek, *"MOS Delay Lines,"* National Semiconductor, AN-25, April 1969.
4. Dale Mrazek, *"MOS Clock Savers,"* National Semiconductor, MB-5.
5. Dale Mrazek, *"Silicon Disc's Challenge Magnetic Disc Memories,"* EDN/EEE Magazine, Sept. 1971.
6. Richard Percival, *"Dynamic MOS Shift Registers Can Also Simulate Stack and Silo Memories,"* Electronics Magazine, November 8, 1971.
7. Bapat and Mrazek, *"Dynamic MOS Random Access Memory System Considerations,"* National Semiconductor, AN-50, August 1971.
8. Don Femling, *"Using the MM5704 Keyboard Interface in Keyboard Systems,"* National Semiconductor, AN-52.

APPENDIX I

DS0025 Circuit Operation

The schematic diagram of the DS0025 is shown in *Figure 7*. With the TTL driver in the logic "0" state Q1 is "OFF" and Q2 is "ON" and the output is at approximately one V_{BE} below the V^+ supply.

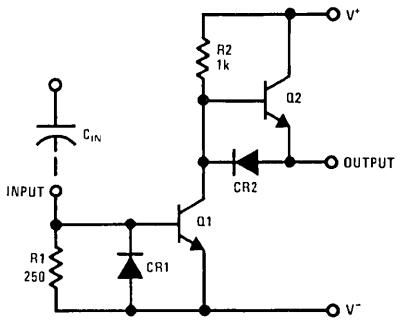


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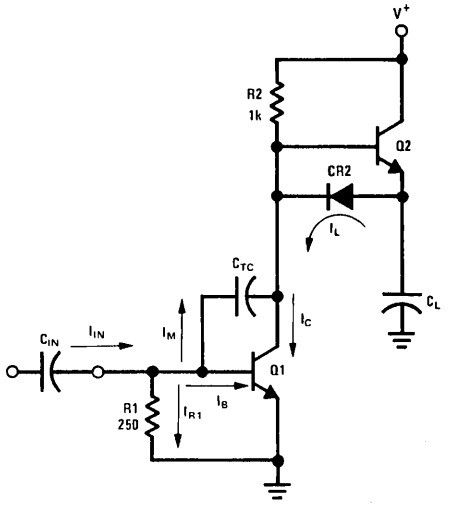
FIGURE 7. DS0025 Schematic (One-Half Circuit)

When the output of the TTL driver goes high, current is supplied to the base of Q1, through C_{IN}, turning it "ON." As the collector of Q1 goes negative, Q2 turns "OFF." Diode CR2 assures turn-on of Q1 prior to Q2's turn-off minimizing current spiking on the V^+ line, as well as providing a low impedance path around Q2's base emitter junction.

The negative voltage transition (to MOS logic "1") will be quite linear since the capacitive load will force Q1 into its linear region until the load is discharged and Q1 saturates. Turn-off begins when the input current decays to zero or the output of the TTL driver goes low. Q1 turns "OFF" and Q2 turns "ON" charging the load to within a V_{BE} of the V^+ supply.

Rise Time Considerations

The logic rise time (voltage fall) of the DS0025 is primarily a function of the ac load, C_L, the available input current and total voltage swing. As shown in *Figure 8*, the input current



TL/F/7322–8

FIGURE 8. Rise Time Model for the DS0025

must charge the Miller capacitance of Q1, C_{TC}, as well as supply sufficient base drive to Q1 to discharge C_L rapidly. By inspection:

$$I_{IN} = I_M + I_B + I_{R1} \quad \text{(AI-1)}$$

$$I_{IN} \cong I_M + I_B, \text{ for } I_M \gg I_{R1} \text{ and } I_B \gg I_{R1}$$

$$I_B = I_{IN} - C_{TC}\frac{\Delta V}{\Delta t} \quad \text{(AI-2)}$$

If the current through R2 is ignored,

$$I_C = I_B h_{FEQ1} = I_L + I_M \quad \text{(AI-3)}$$

where:

$$I_L = C_L\frac{\Delta V}{\Delta t}$$

Combining equations AI-1, AI-2, and AI-3 yields:

$$\frac{\Delta V}{\Delta t}[C_L + C_{TC}(h_{FEQ1} + 1)] = h_{FEQ1} I_{IN} \quad \text{(AI-4)}$$

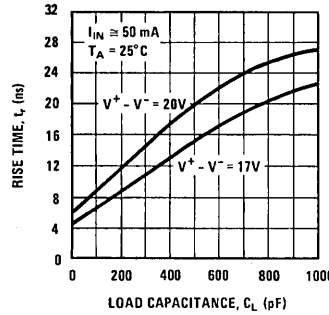
or

$$t_r \cong \frac{[C_L + (h_{FEQ1} + 1)C_{TC}]\,\Delta V}{h_{FEQ1} I_{IN}} \quad \text{(AI-5)}$$

Equation (AI-5) may be used to predict t_r as a function of C_L and ΔV. Values for C_{TC} and h_{FE} are 10 pF and 25 pF respectively. For example, if a DM7440 with peak output current of 50 mA were used to drive a DS0025 loaded with 1000 pF, rise times of:

$$\frac{(1000\text{ pF} + 250\text{ pF})\,(17\text{V})}{(50\text{ mA})\,(20)}$$

or 21 ns may be expected for $V^+ = 5.0\text{V}$, $V^- = -12\text{V}$. *Figure 9* gives rise time for various values of C_L.

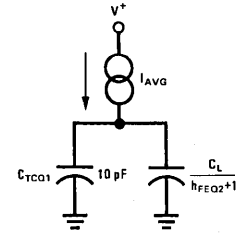


TL/F/7322–9

FIGURE 9. Rise Time vs C_L for the DS0025

Fall Time Considerations

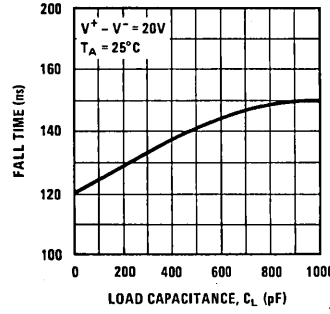
The MOS logic fall time (voltage rise) of the DS0025 is dictated by the load, C_L, and the output capacitance of Q1. The fall time equivalent circuit of DS0025 may be approximated



TL/F/7322–10

FIGURE 10. Fall Time Equivalent Circuit

with the circuit of *Figure 10*. In actual practice, the base drive to Q2 drops as the output voltage rises toward V^+. A rounding of the waveform occurs as the output voltage reaches to within a volt of V^+. The result is that equation (AI-7) predicts conservative values of t_f for the output voltage at the beginning of the voltage rise and optimistic values at the end. *Figure 11* shows t_f as function of C_L.



TL/F/7322–11

FIGURE 11. DS0025 Fall Time vs C_L

Assuming h_{FE2} is a constant of the total transition:

$$\frac{\Delta V}{\Delta t} = \frac{\left(\frac{V^+ - V^-}{2R2}\right)}{C_{TCQ1} + C_L/h_{FEQ1+1}} \quad \text{(AI-6)}$$

or

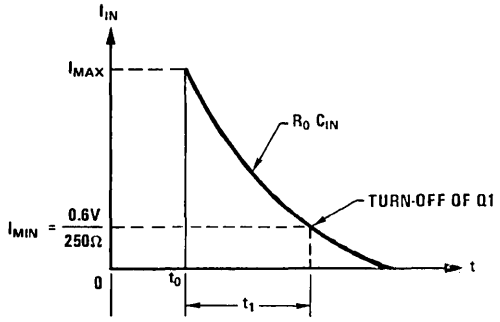
$$t_f \cong 2R2\left(C_{TCQ1} + \frac{C_L}{h_{FEQ+1}}\right) \quad \text{(AI-7)}$$

DS0025 Input Drive Requirements

Since the DS0025 is generally capacitively coupled at the input, the device is sensitive to current not input voltage. The current required by the input is in the 50–60 mA region. It is therefore a good idea to drive the DS0025 from TTL line drivers, such as the DM7440 or DM8830. It is possible to drive the DS0025 from standard 54/74 series gates or flip-flops but t_{ON} and t_r will be somewhat degraded.

Input Capacitor Selection

The DS0025 may be operated in either the logically controlled mode (pulse width out ≅ pulse width in) or C_{IN} may be used to set the output pulse width. In the latter mode a long pulse is supplied to the DS0025.



TL/F/7322–12

FIGURE 12. DS0025 Input Current Waveform

The input current is of the general shape as shown in *Figure 12*. I_{MAX} is the peak current delivered by the TTL driver into a short circuit (typically 50–60 mA). Q1 will begin to turn-off when I_{IN} decays below $V_{BE}/R1$ or about 2.5 mA. In general:

$$I_{IN} = I_{MAX}\, e^{-t/R0\, C_{IN}} \quad \text{(AI-8)}$$

where:

R0 = Output impedance of the TTL driver

C_{IN} = Input coupling capacitor

Substituting $I_{IN} = I_{MIN} = \frac{V_{BE}}{R1}$ and solving for t_1 yields:

$$t_1 = R0C_{IN} \ln \frac{I_{MAX}}{I_{MIN}} \quad \text{(AI-9)}$$

The total pulse width must include rise and fall time considerations. Therefore, the total expression for pulse width becomes:

$$t_{PW} \cong \frac{t_r + t_f}{2} + t_1$$

$$= \frac{t_r + t_f}{2} + R0C_{IN} \ln \frac{I_{MAX}}{I_{MIN}} \quad \text{(AI-10)}$$

The logic "1" output impedance of the DM7440 is approximately 65Ω and the peak current (I_{MAX}) is about 50 mA. The pulse width for C_{IN} = 2,200 pF is:

$$t_{PW} \cong \frac{25\text{ ns} + 150\text{ ns}}{2} + (65\Omega)(2200\text{ pF}) \ln$$

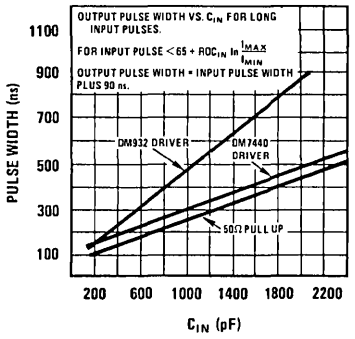
$$\frac{50\text{ mA}}{2.5\text{ mA}} = 517\text{ ns}$$

A plot of pulse width for various types of drivers is shown in *Figure 13*. For applications in which the output pulse width is logically controlled, C_{IN} should be chosen 2 to 3 times larger than the maximum pulse width dictated by equation (AI-10).

DC Coupled Operation

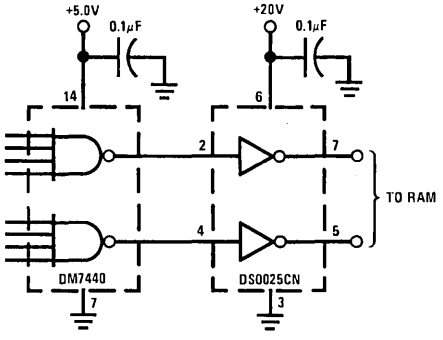
The DS0025 may be direct-coupled in applications when level shifting to a positive value only. For example, the MM1103 RAM typically operates between ground and +20V. The DS0025 is shown in *Figure 14* driving the address or precharge line in the logically controlled mode.

If DC operation to a negative level is desired, a level translator such as the DS7800 or DH0034 may be employed as shown in *Figure 15*. Finally, the level shift may be accomplished using PNP transistors are shown in *Figure 16*.



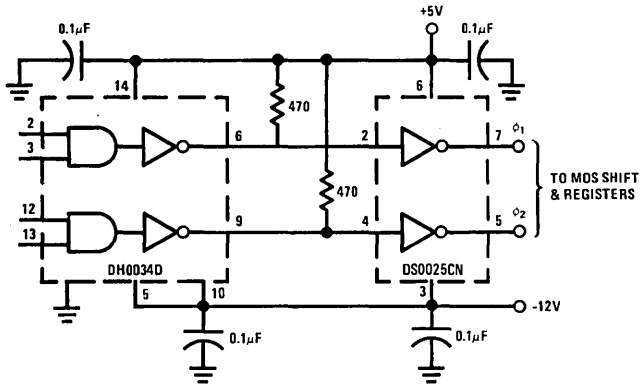
TL/F/7322–13

FIGURE 13. Output PW Controlled by C_{IN}



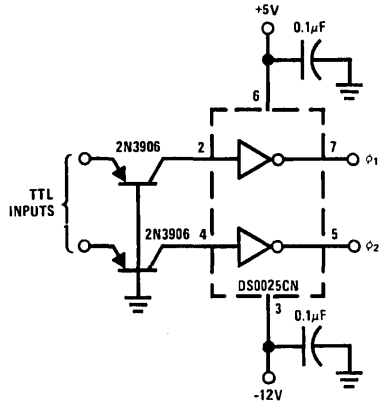
TL/F/7322–14

FIGURE 14. DC Coupled DS0025 Driving 1103 RAM



TL/F/7322–15

FIGURE 15. DC Coupled Clock Driver Using DH0034



TL/F/7322–16

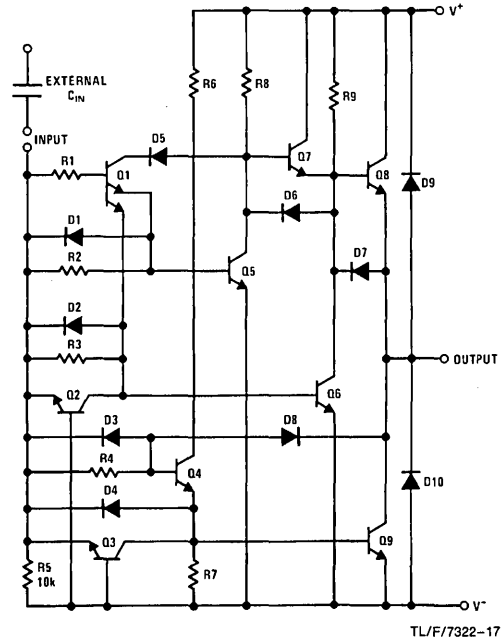
FIGURE 16. Transistor Coupled DS0025 Clock Driver

APPENDIX II

DS0026 Circuit Operation

The schematic of the DS0026 is shown in *Figure 17.* The device is typically AC coupled on the input and responds to input current as does the DS0025. Internal current gain allows the device to be driven by standard TTL gates and flip-flops.

With the TTL input in the low state Q1, Q4, Q5, and Q6 are "OFF" allowing Q7 and Q8 to come "ON." R9 assures that the output will pull up to within a V_{BE} of V^+ volts. When the TTL input starts toward logic "1," current is supplied via C_{IN} to the bases of Q5 and Q6 turning them "ON." Simultaneously, Q7 and Q8 are snapped "OFF." As the input voltage rises (to about 1.2V), Q1 and Q4 turn-on. Multiple emitter transistor Q1 provides additional base drive to Q5 and Q6 assuring their complete and rapid turn-on. Since Q7 and Q8 were rapidly turned "OFF" minimal power supply current spiking will occur when Q9 comes "ON."



TL/F/7322–17

FIGURE 17. DS0026 Schematic (One-Half Circuit)

Q4 now provides sufficient base drive to Q9 to turn it "ON." The load capacitance is then rapidly discharged toward V^-. Diodes D6 and D7 prevent avalanching Q7's and Q8's base-emitter junction as the collectors of Q5 and Q6 go negative. The output of the DS0026 continues negative stopping about 0.5V more positive than V^-.

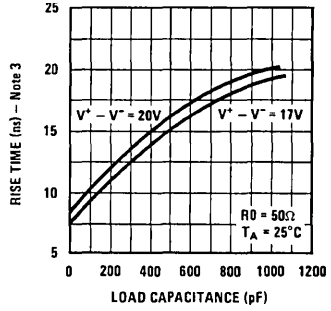
When the TTL input returns to logic "0," the input voltage to the DS0026 goes negative by an amount proportional to the charge on C_{IN}. Transistors Q2 and Q3 turn-on, pulling stored base charge out of Q4 and Q9 assuring their rapid turn-off. With Q1, Q5, Q6 and Q9 "OFF," Darlington connected Q7 and Q8 turn-on and rapidly charge the load to within a V_{BE} of V^+.

Rise Time Considerations

Predicting the MOS logic rise time (voltage fall) of the DS0026 is considerably involved, but a reasonable approximation may be made by utilizing equation (AI-5), which reduces to:

$$t_r \cong [C_L + 250 \times 10^{-12}]\,\Delta V \qquad \text{(AII-1)}$$

For C_L = 1000 pF, V^+ = 5.0V, V^- = −12V, $t_r \cong$ 21 ns. *Figure 18* shows DS0026 rise times vs C_L.



TL/F/7322–18

FIGURE 18. Rise Time vs Load Capacitance

Fall Time Considerations

The MOS logic fall time of the DS0026 is determined primarily by the capacitance Miller capacitance of Q5 and Q1 and R5. The fall time may be predicted by:

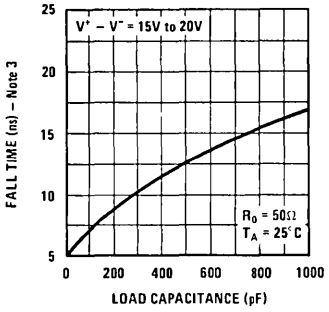
$$t_f \cong (2.2)(R5)\left(C_S + \frac{C_L}{h_{FE}{}^2}\right) \cong (4.4 \times 10^3)\left(C_S + \frac{C_L}{h_{FE}{}^2}\right) \qquad \text{(AII-2)}$$

where:

C_S = Capacitance to ground seen at the base of Q3
= 2 pF

$h_{FE}{}^2 = (h_{FEQ3} + 1)\,(h_{FEQ4} + 1)$
$\cong$ 500

For the values given and C_L = 1000 pF, $t_f \cong$ 17.5 ns. *Figure 19.* gives t_f for various values of C_L.

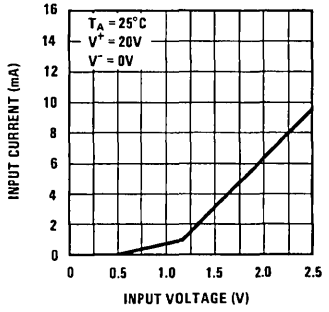


TL/F/7322–19

FIGURE 19. Fall Time vs Load Capacitance

DS0026 Input Drive Requirements

The DS0026 was designed to be driven by standard 54/74 elements. The device's input characteristics are shown in *Figure 20.* There is breakpoint at $V_{IN} \cong$ 0.6V which corresponds to turn-on of Q1 and Q2. The input current then rises with a slope of about 600Ω (R2 || R3) until a second breakpoint at approximately 1.2V is encountered, corresponding to the turn-on of Q5 and Q6. The slope at this point is about 150Ω (R1 || R2 || R3 || R4).



TL/F/7322–20

FIGURE 20. Input Current vs Input Voltage

The current demanded by the input is in the 5–10 mA region. A standard 54/74 gate can source currents in excess of 20 mA into 1.2V. Obviously, the minimum "1" output voltage of 2.5V under these conditions cannot be maintained. This means that a 54/74 element must be dedicated to driving 1/2 of a DS0026. As far as the DS0026 is concerned, the current is the determining turn-on mechanism not the voltage output level of the 54/74 gate.

Input Capacitor Selection

A major difference between the DS0025 and DS0026 is that the DS0026 requires that the output pulse width be logically controlled. In short, the input pulse width $\cong$ output pulse width. Selection of C_{IN} boils down to choosing a capacitor small enough to assure the capacitor takes on nearly full charge, but large enough so that the input current does not drop below a minimum level to keep the DS0026 "ON." As before:

$$t_1 = R0 C_{IN} \ln \frac{I_{MAX}}{I'' MIN} \qquad \text{(AII-3)}$$

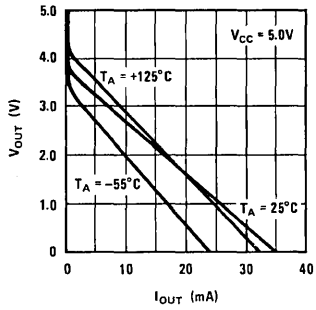
or

$$C_{IN} = \frac{t_1}{R0 \ln \frac{I_{MAX}}{I_{MIN}}} \qquad \text{(AII-4)}$$

5

In this case R0 equals the sum of the TTL gate output impedance plus the input impedance of the DS0026 (about 150Ω). I_{MIN} from *Figure 21* is about 1 mA. A standard 54/74 series gate has a high state output impedance of about 150Ω in the logic "1" state and an output (short circuit) current of about 20 mA into 1.2V. For an output pulse width of 500 ns,

$$C_{IN} = \frac{500 \times 10^{-9}}{(150\Omega + 150\Omega)\ln\frac{20\text{ mA}}{1\text{ mA}}} = 560\text{ pF}$$

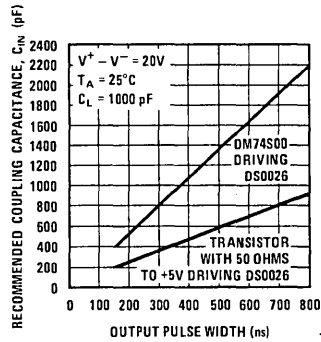


TL/F/7322-21

FIGURE 21. Logical "1" Output Voltage vs Source Current

In actual practice it's a good idea to use values of about twice those predicted by equation (AII-4) in order to account for manufacturing tolerances in the gate, DS0026 and temperature variations.

A plot of optimum value for C_{IN} vs desired output pulse width is shown in *Figure 22*.

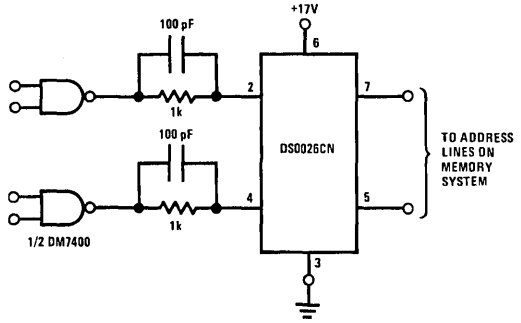


TL/F/7322-22

FIGURE 22. Suggested Input Capacitance vs Output Pulse Width

DC Coupled Applications

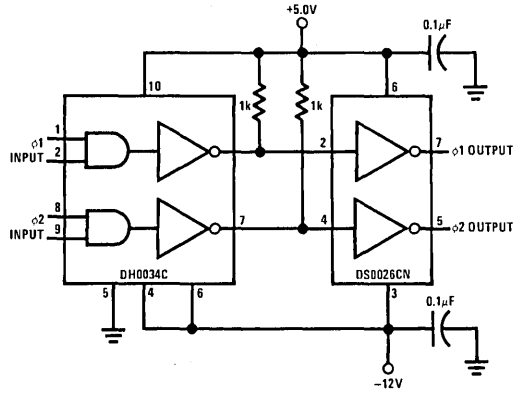
The DS0026 may be applied in direct coupled applications. *Figure 23* shows the device driving address or pre-charge lines on an MM1103 RAM.



TL/F/7322-23

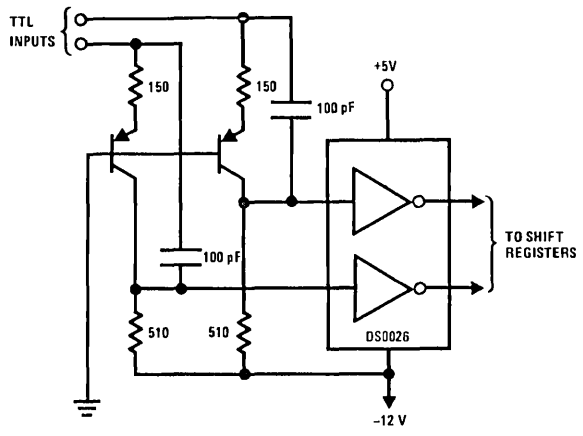
FIGURE 23. DC Coupled RAM Memory Address or Precharge Driver (Positive Supply Only)

For applications requiring a dc level shift, the circuits of *Figure 24* or *25* are recommended.



TL/F/7322-24

FIGURE 24. Transistor Coupled MOS Clock Driver



TL/F/7322–25

FIGURE 25. DC Coupled MOS Clock Driver

APPENDIX III

MOS Interface Circuits

MOS Clock Drivers

MH0007 Direct coupled, single phase, TTL compatible clock driver.

MH0009 Two phase, direct or ac coupled clock driver.

MH0012 10 MHz, single phase direct coupled clock driver.

MH0013 Two phase, ac coupled clock driver.

DS0025C Low cost, two phase clock driver.

DS0026C Low cost, two phase, high speed clock driver.

DS3674 Quad MOS clock driver.

DS75361 Dual TTL-to-MOS driver.

DS75365 Quad TTL-to-MOS driver.

MOS RAM Memory Address and Precharge Drivers

DS0025C Dual address and precharge driver.

DS0026C Dual high speed address and precharge driver.

TTL to MOS Interface

DH0034 Dual high speed TTL to negative level converter.

DS8800
DS8819 Dual TTL to negative level converter.

DS88L12 Active pull-up TTL to positive high level MOS converter gates.

DS3645/DS3675 Hex TRI-STATE® MOS driver.

DS3647A Quad TRI-STATE MOS driver I/O register.

DS3648/DS3678 TRI-STATE MOS driver multiplexer.

DS3649/DS3679 Hex TRI-STATE MOS driver.

DS36149/
DS36179 Hex TRI-STATE MOS driver.

MOS to TTL Converters and Sense Amps

DS75107,
DS75207 Dual sense amp for MM1103 1k MOS RAM memory.

Voltage Regulators for MOS Systems

LM309, LM340 Series Positive regulators.

LM320 Series Negative regulators.

LM325 Series Dual ± regulators.

Section 6

Microprocessor Support

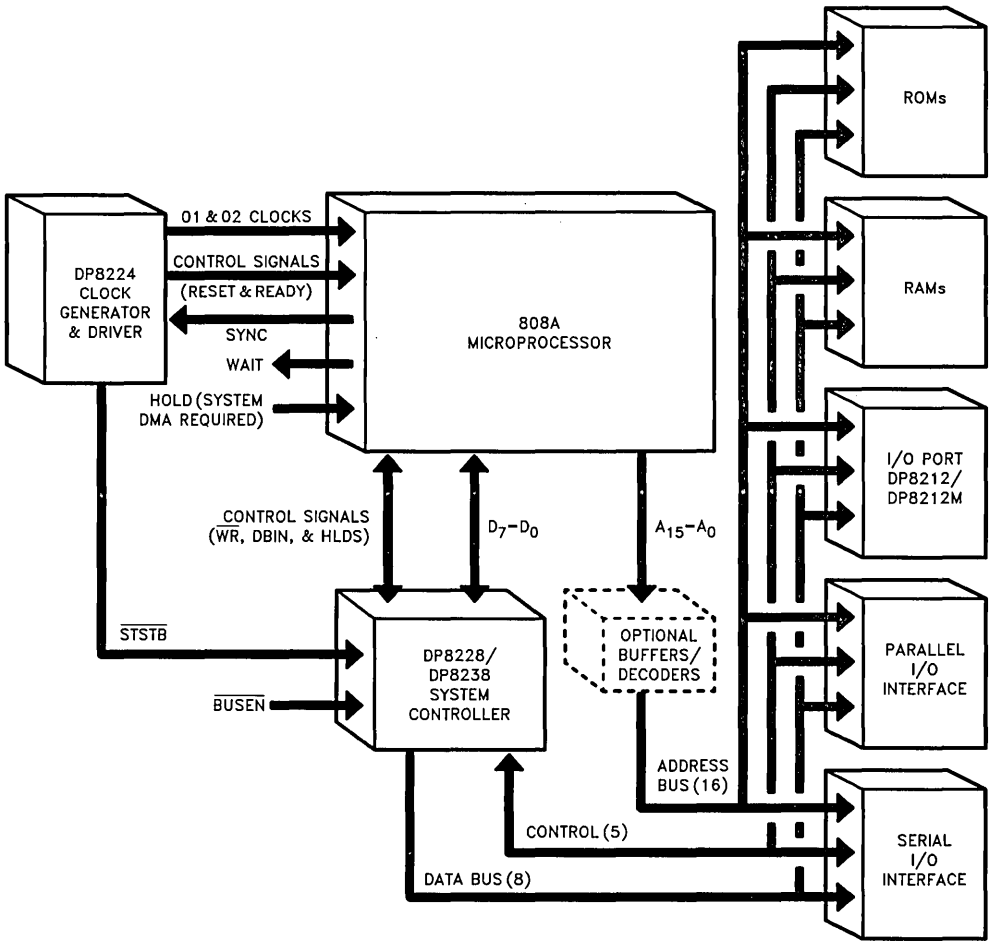
Section Contents

*Also available processed to various Military screening levels. Refer to Section 9.

Microprocessor Support

National offers a selection of high quality circuits designed specifically to interface with, and support, the very popular 8-bit 8080A microprocessor. National's family of 8080A support circuits includes clock/generator driver, system controller, I/O port and databus transceivers, all of which make it easy to add microprocessor capability to any system design. For further information on these devices, refer to the enclosed selection guide.

National's 8080A Support Circuits



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Microprocessor Support Circuits

Temperature Range		8080 CPU	General Purpose	Description	Page Number
−55°C to +125°C	0°C to +70°C				
DP8212M	DP8212	•	•	8-Bit I/O Port	6-5
DP8216M,	DP8216,	•	•	4-Bit Parallel Receiver/Driver	6-13
DP8226M	DP8226				6-13
	DP8224	•		Clock Generator/Driver	6-18
DP8228M,	DP8228,	•		System Controller/Bus Driver	6-24
DP8238M	DP8238				6-24
	DP8303A		•	8-Bit 48 mA Bus Transceiver	2-6
DP7304B	DP8304B		•	8-Bit 48 mA Bus Transceiver	2-11
	DP8307A		•	8-Bit 48 mA Bus Transceiver	2-21
DP7308	DP8308		•	8-Bit 48 mA Bus Transceiver	2-25
	DP8350	•	•	CRT Controller	4-8
MM54C373	MM74C373		•	Octal D-Type Latch	CMOS
MM54C374	MM74C374		•	Octal D-Type Flip-Flop	CMOS
MM54C922	MM74C922		•	16-Key Encoder	CMOS
MM54C923	MM74C923		•	20-Key Encoder	CMOS
DM54LS373	DM74LS373		•	Octal Transparent D Latch	LOGIC
DM54LS374	DM74LS374		•	Octal Edge-Triggered D Flip-Flop	LOGIC

National Semiconductor Corporation

DP8212/DP8212M 8-Bit Input/Output Port

General Description

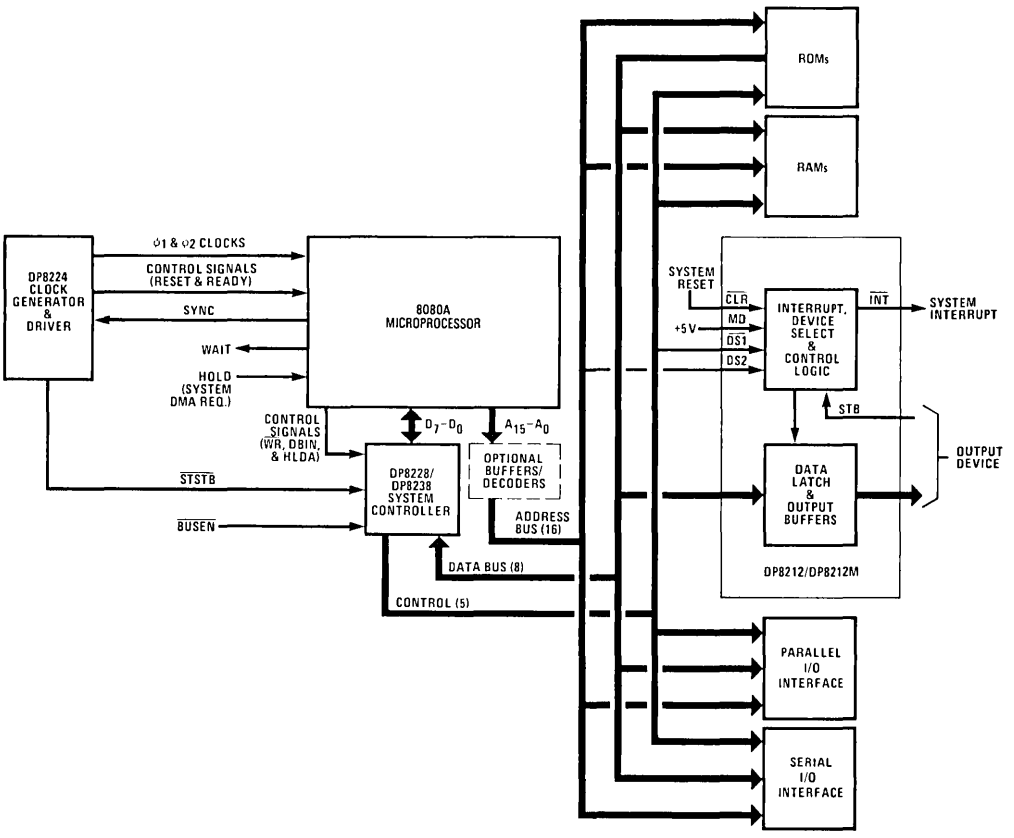
The DP8212/DP8212M is an 8-bit input/output port contained in a standard 24-pin dual-in-line package. The device, which is fabricated using Schottky Bipolar technology, is part of National Semiconductor's 8080A support family. The DP8212/DP8212M can be used to implement latches, gated buffers, or multiplexers. Thus, all of the major peripheral and input/output functions of a microcomputer system can be implemented with this device.

The DP8212/DP8212M includes an 8-bit latch with TRI-STATE® output buffers, and device selection and control logic. Also included is a service request flip-flop for the generation and control of interrupts to the microprocessor.

Features

- 8-Bit data latch and buffer
- Service request flip-flop for generation and control of interrupts
- 0.25 mA input load current
- TRI-STATE TTL output drive capability
- Outputs sink 15 mA
- Asynchronous latch clear
- 3.65V output for direct interface to INS8080A
- Reduces system package count by replacing buffers, latches, and multiplexers in microcomputer systems

8080A Microcomputer Family Block Diagram



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Absolute Maximum Ratings

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Storage Temperature	−65°C to +160°C
All Output or Supply Voltages	−0.5V to +7V
All Input Voltages	−1.0V to 5.5V
Output Currents	125 mA
Maximum Power Dissipation* at 25°C	
Cavity Package	1903 mW
Molded Package	2005 mW

*Derate cavity package 12.7 mW/°C above 25°C; derate molded package 16.0 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
DP8212M	4.50	5.50	V_{DC}
DP8212	4.75	5.25	V_{DC}
Operating Temperaure (T_A)			
DP8212M	−55	+125	°C
DP8212	0	+75	°C

Note: *Maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended and should be limited to those conditions specified under DC electrical characteristics.*

Electrical Characteristics Min ≤ T_A ≤ Max, Min ≤ V_{CC} ≤ Max, unless otherwise noted

Symbol	Parameter	Conditions		Min	Typ	Max	Units
I_F	Input Load Current, STB, DS2, $\overline{CLR}$, DI_1–DI_8 Inputs	V_F = 0.45V				−0.25	mA
I_F	Input Load Current, MD Input	V_F = 0.45V				−0.75	mA
I_F	Input Load Current, $\overline{DS1}$ Input	V_F = 0.45V				−1.0	mA
I_R	Input Leakage Current STB, DS2, $\overline{CLR}$, DI_1–DI_8 Inputs	V_R = V_{CC} Max				10	μA
I_R	Input Leakage Current, MD Input	V_R = V_{CC} Max				30	μA
I_R	Input Leakage Current, $\overline{DS1}$ Input	V_R = V_{CC} Max				40	μA
V_C	Input Forward Voltage Clamp	I_C = −5 mA				−1	V
V_{IL}	Input "Low" Voltage		DP8212M			0.08	V
			DP8212			0.85	V
V_{IH}	Input "High" Voltage			2.0			V
V_{OL}	Output "Low" Voltage	I_{OL} = 10 mA	DP8212M			0.45	V
		I_{OL} = 15 mA	DP8212			0.45	V
V_{OH}	Output "High" Voltage	I_{OH} = 0.5 mA	DP8212M	3.40	4.0		V
		I_{OH} = 1.0 mA	DP8212	3.65	4.0		V
I_{SC}	Short-Circuit Output Current	V_O = 0V, V_{CC} = 5V		−15		−75	mA
$\|I_O\|$	Output Leakage Current, High Impedance State	V_O = 0.45V/V_{CC} Max				20	μA
I_{CC}	Power Supply Current		DP8212M		90	145	mA
			DP8212		90	130	mA

Capacitance* F = 1 MHz, V_{BIAS} = 2.5V, V_{CC} = 5V, T_A = 25°C

Symbol	Parameter	Min	Typ	Max	Units
C_{IN}	DS1, MD Input Capacitance		9	12	pF
C_{IN}	DS2, $\overline{CLR}$, STB, DI_1–DI_8 Input Capacitance		5	9	pF
C_{OUT}	DO1–DO8 Output Capacitance		8	12	pF

*This parameter is sampled and not 100% tested.

Switching Characteristics Min ≤ T_A ≤ Max, Min ≤ V_{CC} ≤ Max

Symbol	Parameter	Conditions	DP8212M		DP8212		Units
			Min	Max	Min	Max	
t_{PW}	Pulse Width		40		30		ns
t_{PD}	Data to Output Delay	(Note 1)		30		30	ns
t_{WE}	Write Enable to Output Delay	(Note 1)		50		40	ns
t_{SET}	Data Set-Up Time		20		15		ns
t_H	Data Hold Time		30		20		ns
t_R	Reset to Output Delay	(Note 1)		55		40	ns
t_S	Set to Output Delay	(Note 1)		35		30	ns
t_E	Output Enable/Disable Time	(Note 2)		50		45	ns
t_C	Clear to Output Delay	(Note 1)		65		55	ns

Note 1: C_L = 30 pF

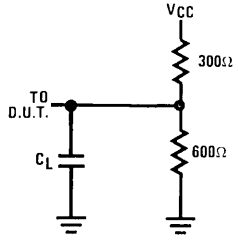
Note 2: C_L = 30 pF except for DP8212M

$t_{E\ (DISABLE)}$ C_L = 5 pF

Switching Conditions

1. Input Pulse Amplitude = 2.5V.
2. Input Rise and Fall Times = 5 ns.
3. Between 1V and 2V Measurements made at 1.5V with 15 mA & 30 pF Test Load.
4. C_L includes jig and probe capacitance.
5. C_L = 30 pF.
6. C_L = 30 pF except for DP8212M $t_{E\ (DISABLE)}$ C_L = 5 pF

Test Load



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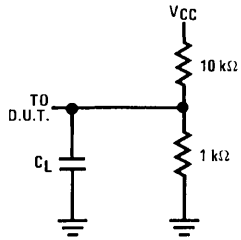
Alternate Test Load
(Refer to Timing Diagram)



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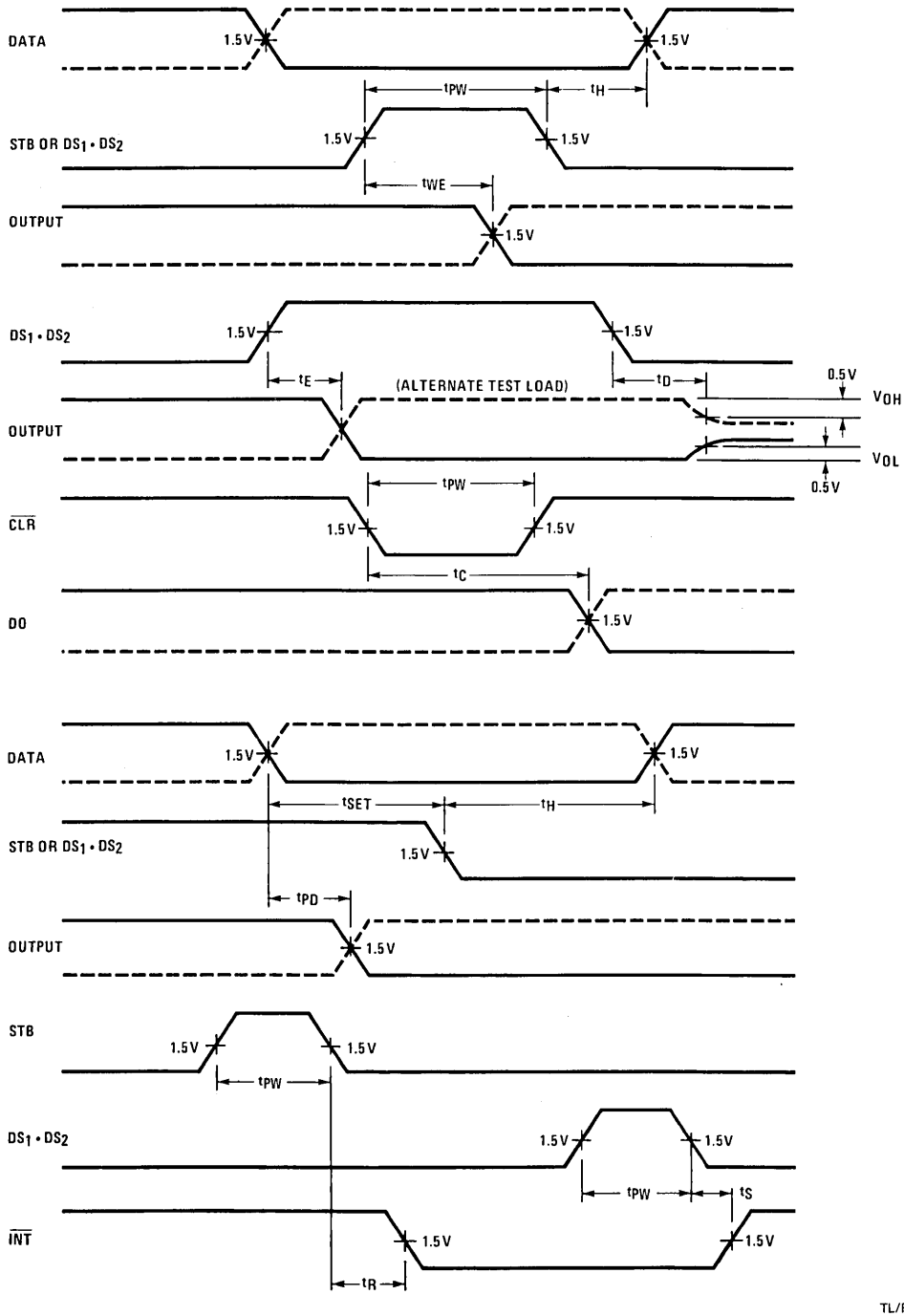
Timing Diagram



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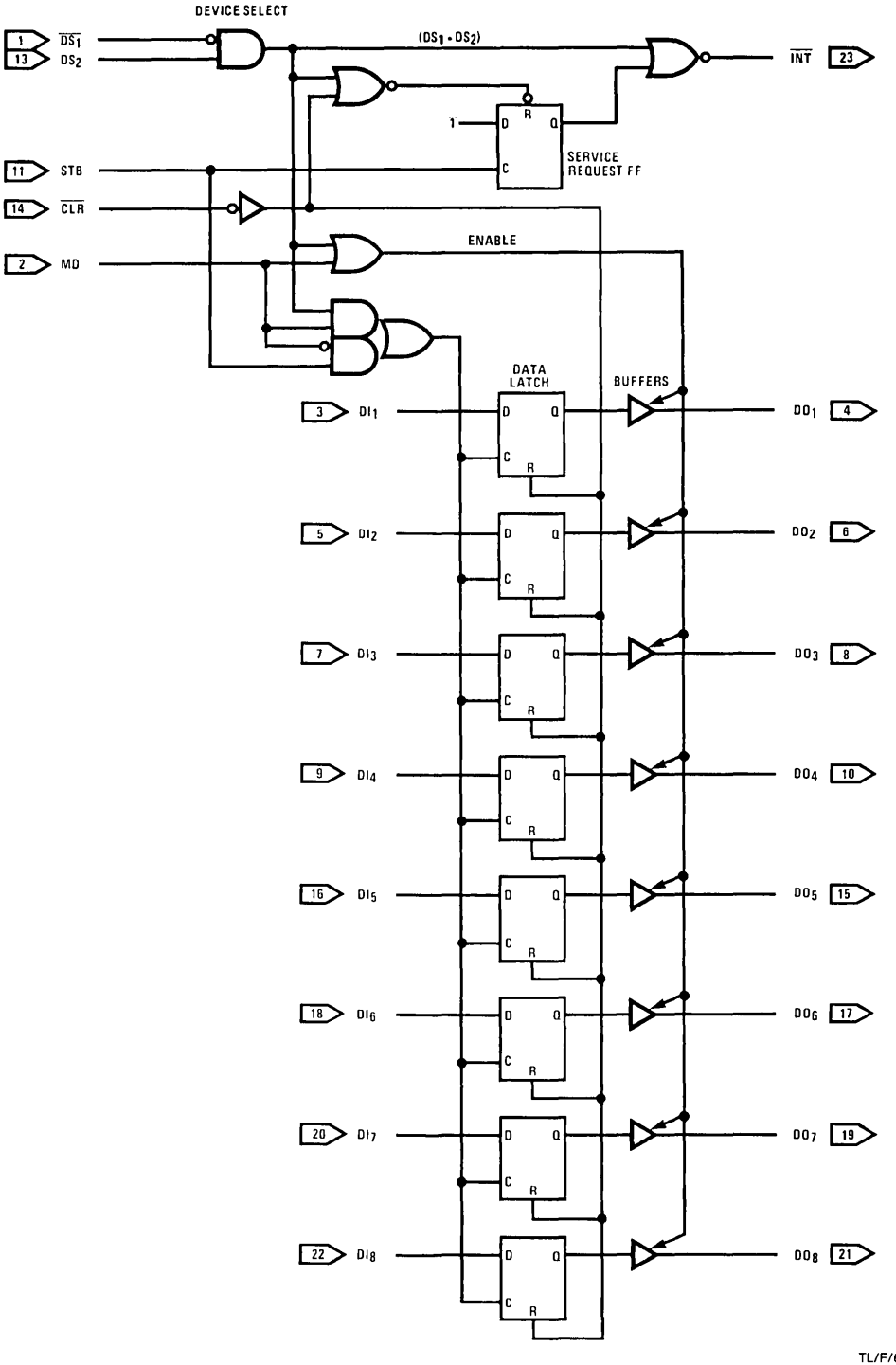
Logic Diagram



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Logic Tables

Logic Table A

STB	MD	(DS_1•DS_2)	Data Out Equals
0	0	0	TRI-STATE
1	0	0	TRI-STATE
0	1	0	DATA LATCH
1	1	0	DATA LATCH
0	0	1	DATA LATCH
1	0	1	DATA IN
0	1	1	DATA IN
1	1	1	DATA IN

$\overline{CLR}$ ⌝ resets data latch to the output low state.

The data latch clock is level sensitive, a low level clock latches the data.

Logic Table B

$\overline{CLR}$	(DS_1•DS_2)	STB	Q*	$\overline{INT}$
0 RESET	0	0	0	1
1	0	0	0	1
1	0	⌝	1	0
1	1 RESET	0	0	0
1	0	0	0	1

*Internal Service Request flip-flop.

Functional Pin Definitions

The following describes the function of all the DP8212/ DP8212M input/output pins. Some of these descriptions reference internal circuits.

INPUT SIGNALS

Device Select ($\overline{DS_1}$, DS_2): When $\overline{DS_1}$ is low and DS_2 is high, the device is selected. The output buffers are enabled and the service request flip-flop is asynchronously reset (cleared) when the device is selected.

Mode (MD): When high (output mode), the output buffers are enabled and the source of the data latch clock input is the device selection logic (DS_1 • DS_2). When low (input mode), the state of the output buffers is determined by the device selection logic (DS_1 • DS_2) and the source of the data latch clock input is the strobe (STB) input.

Strobe (STB): Used as data latch clock input when the mode (MD) input is low (input mode). Also used to synchronously set the service request flip-flop, which is negative edge triggered.

Data In (DI_1–DI_8): Eight-bit data input to the data latch, which consists of eight D-type flip-flops. Incorporating a level sensitive clock while the data latch clock input is high, the Q output of each flip-flop follows the data input. When the clock input returns low, the data latch stores the data input. The clock input high overrides the clear ($\overline{CLR}$) input data latch reset.

Clear ($\overline{CLR}$): When low, asynchronously resets (clears) the data latch and the service request flip-flop. The service request flip-flop is in the non-interrupting state when reset.

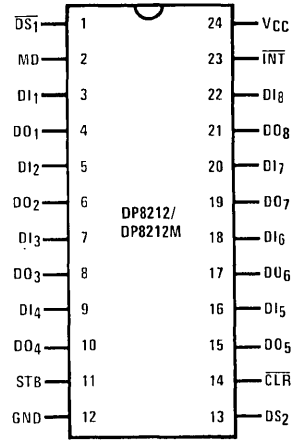
OUTPUT SIGNALS

Interrupt ($\overline{INT}$): Goes low (interrupting state) when either the service request flip-flop is synchronously set by the strobe (STB) input or the device is selected.

Data Out (DO_1–DO_8): Eight-bit data output of data buffers, which are TRI-STATE, non-inverting stages. These buffers have a common control line that either enables the buffers to transmit the data from the data latch outputs or disables the buffers by placing them in the high-impedance state.

Connection Diagram

Dual-In-Line Package



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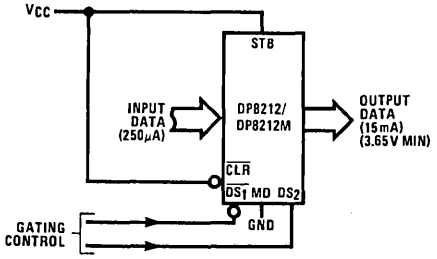
Top View

Order Number DP8212J, DP8212N or DP8212MJ

See NS Package Number J24A or N24A

Applications in Microcomputer Systems

Gated Buffer (TRI-STATE)



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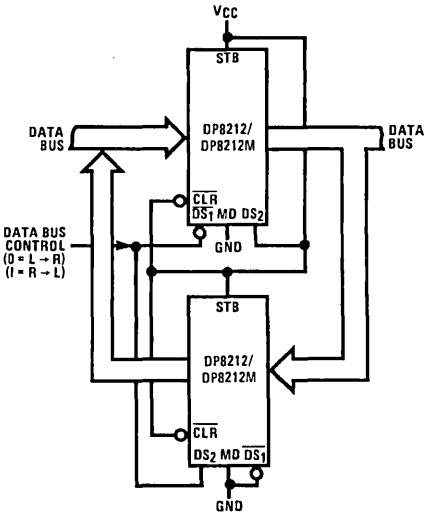

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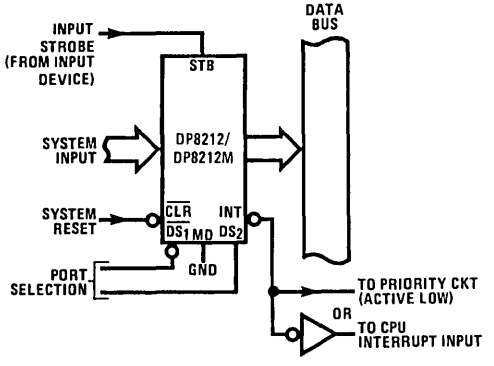
Interrupting Input Port



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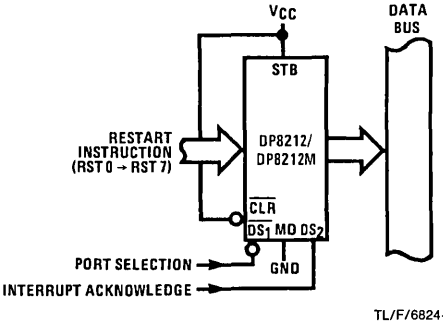
Interrupt Instruction Port



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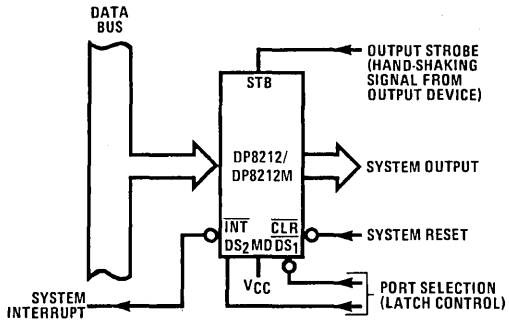
Applications in Microcomputer Systems (Continued)

Output Port (with Hand-Shanking)



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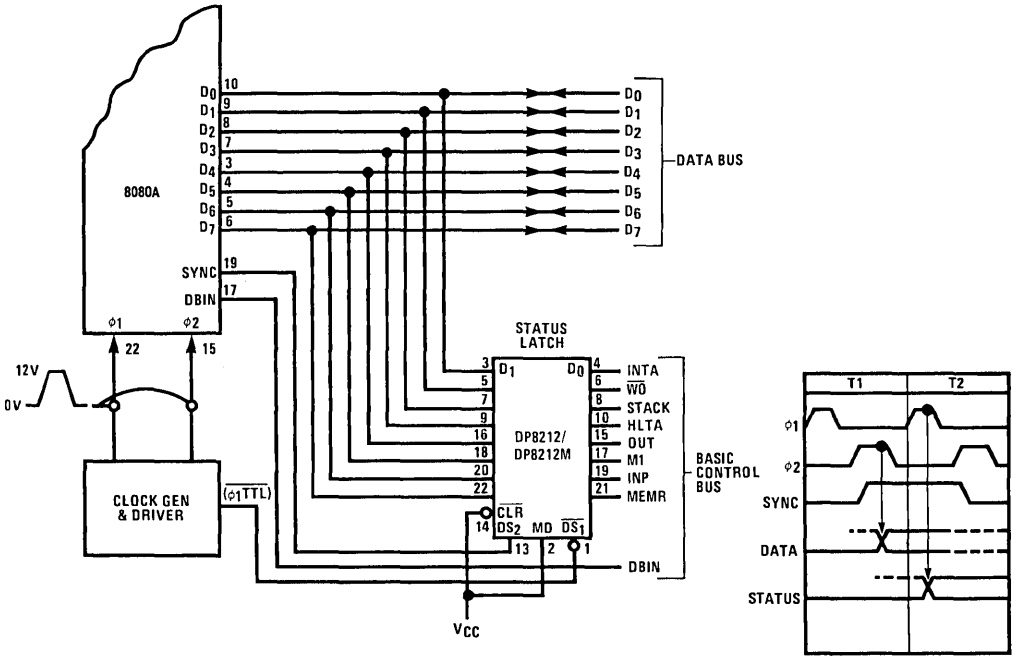
INS8080A Status Latch



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National Semiconductor Corporation

DP8216/DP8216M/DP8226/DP8226M 4-Bit Bidirectional Bus Transceivers

General Description

The DP8216/DP8216M and DP8226/DP8226M are 4-bit bidirectional bus drivers to use in bus oriented applications. The non-inverting DP8216/DP8216M and inverting DP8226/DP8226M drivers are provided for flexibility in system design.

Each buffered line of the four-bit drivers consists of two separate buffers that are TRI-STATE® to achieve direct bus interface and bidirectional capability. On one side of the driver the output of one buffer and the input of another are tied together (DB); this side is used to interface to the system side components such as memories, I/O, etc., because its interface is TTL compatible and it has high driver (50 mA). On the other side of the driver the inputs and outputs are separated to provide maximum flexibility. Of course, they can be tied together so that the driver can be used to buffer a true bidirectional bus. The DO outputs on this side of the driver have a special high voltage output drive capability so that direct interface to the 8080 type CPUs is achieved with an adequate amount of noise immunity.

The CS input is a device enable. When it is "high" the output drivers are all forced to their high-impedance state. When it is a "low" the device is enabled and the direction of the data flow is determined by the DIEN input.

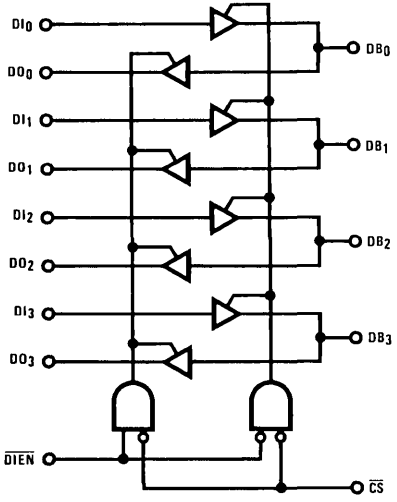
The DIEN input controls the direction of data flow, which is accomplished by forcing one of the pair of buffers into its high-impedance state and allowing the other to transmit its data. A simple two-gate circuit is used for this function.

Features

- Data bus buffer driver to 8080 type CPUs
- Low input load current—0.25 mA maximum
- High output drive capability for driving system data bus—50 mA at 0.5V
- Power up-down protection
- DP8216/DP8216M have non-inverting outputs
- DP8226/DP8226M have inverting outputs
- Output high voltage compatible with direct interface to MOS
- TRI-STATE outputs
- Advanced Schottky processing
- Available in military and commercial temperature

Logic Diagrams

DP8216/DP8216M



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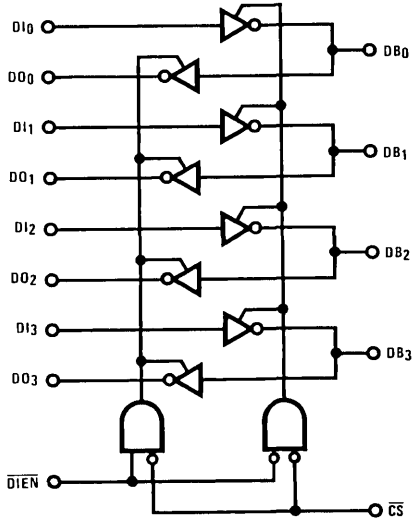
DP8226/DP8226M



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Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

	Min	Max	Units
All Output and Supply Voltages	−0.5	+7.0	V
All Input Voltages	−1.0	+5.5	V
Output Currents		125	mA
Maximum Power Dissipation* at 25°C			
Cavity Package		1509	mW
Molded Package		1476	mW

Note: *Derate cavity package 10.1 mW/°C above 25°C; derate molded package 11.8 mW/°C above 25°C.

	Min	Max	Units
Storage Temperature	−65	+150	°C
Lead Temperature (soldering, 4 seconds)		260	°C

Operating Conditions

	Min	Max	Units
Supply Voltage, V_{CC}			
DP8216M, DP8226M	4.5	5.5	V
DP8216, DP8226	4.75	5.25	V
Temperature, T_A			
DP8216M, DP8226M	−55	+125	°C
DP8216, DP8226	0	+70	°C

Electrical Characteristics DP8216, DP8226 V_{CC} = 5V ±5% (Notes 2, 3, and 4)

Symbol	Parameter	Conditions	Limits			Units
			Min	Typ	Max	
DRIVERS						
V_{IL}	Input Low Voltage				0.95	V
V_{IH}	Input High Voltage		2			V
I_F	Input Load Current	V_F = 0.45V		−0.03	−0.25	mA
I_R	Input Leakage Current	V_R = 5.25V			10	μA
V_C	Input Clamp Voltage	I_C = −5 mA			−1.2	V
V_{OL1}	Output Low Voltage	I_{OL} = 25 mA		0.3	0.45	V
V_{OL2}	Output Low Voltage	DP8216 I_{OL} = 55 mA DP8226 I_{OL} = 50 mA		0.5	0.6	V
V_{OH}	Output High Voltage	I_{OH} = −10 mA	2.4	3.0		V
I_{SC}	Output Short Circuit Current	V_{CC} = 5V	−30	−75	−120	mA
$\|I_O\|$	Output Leakage Current TRI-STATE	V_O = 0.45V/5.5V			100	μA
RECEIVERS						
V_{IL}	Input Low Voltage				0.95	V
V_{IH}	Input High Voltage		2			V
I_F	Input Load Current	V_F = 0.45V		−0.08	−0.25	mA
V_C	Input Clamp Voltage	I_C = −5 mA			−1.2	V
V_{OL}	Output Low Voltage	I_{OL} = 15 mA		0.3	0.45	V
V_{OH1}	Output High Voltage	I_{OH} = −1 mA	3.65	4.0		V
I_{SC}	Output Short Circuit Current	V_{CC} = 5V	−15	−35	−65	mA
$\|I_O\|$	Output Leakage Current TRI-STATE	V_O = 0.45V/5.5V			20	μA
CONTROL INPUTS ($\overline{CS}$, $\overline{DIEN}$)						
V_{IL}	Input Low Voltage				0.95	V
V_{IH}	Input High Voltage		2			V
I_F	Input Load Current	V_F = 0.45V		−0.15	−0.5	mA
I_R	Input Leakage Current	V_R = 5.25V			20	μA
I_{CC}	Power Supply Current					
	DP8216			95	130	mA
	DP8226			85	120	mA

Electrical Characteristics (Continued) DP8216M, DP8226M $V_{CC} = 5V \pm 10\%$ (Notes 2, 3 and 4)

Symbol	Parameter	Conditions	Limits			Units
			Min	Typ	Max	
DRIVERS						
V_{IL}	Input Low Voltage DP8216M DP8226M				 0.95 0.90	 V V
V_{IH}	Input High Voltage		2			V
I_F	Input Load Current	$V_F = 0.45V$		−0.08	−0.25	mA
I_R	Input Leakage Current	$V_R = 5.5V$			40	μA
V_C	Input Clamp Voltage	$I_C = -5$ mA			−1.2	V
V_{OL1}	Output Low Voltage	$I_{OL} = 25$ mA		0.3	0.45	V
V_{OL2}	Output Low Voltage	$I_{OL} = 45$ mA		0.5	0.6	V
V_{OH}	Output High Voltage	$I_{OH} = -5$ mA	2.4	3.0		V
I_{SC}	Output Short Circuit Current	$V_{CC} = 5.0V$	−30	−75	−120	mA
$\|I_O\|$	Output Leakage Current TRI-STATE	$V_O = 0.45V/5.5V$			100	μA
RECEIVERS						
V_{IL}	Input Low Voltage DP8216M DP8226M				 0.95 0.9	 V V
V_{IH}	Input High Voltage		2			V
I_F	Input Load Current	$V_F = 0.45V$		−0.08	−0.25	mA
V_C	Input Clamp Voltage	$I_C = -5$ mA			−1.2	V
V_{OL}	Output Low Voltage	$I_{OL} = 15$ mA		0.3	0.45	V
V_{OH1}	Output High Voltage	$I_{OH} = -0.5$ mA	3.4	3.8		V
V_{OH2}	Output High Voltage	$I_{OH} = -2$ mA	2.4			V
I_{SC}	Output Short Circuit Current	$V_{CC} = 5.0V$	−15	−35	−65	mA
$\|I_O\|$	Output Leakage Current TRI-STATE	$V_O = 0.45V/5.5V$			20	μA
CONTROL INPUTS ($\overline{CS}$, $\overline{DIEN}$)						
V_{IL}	Input Low Voltage DP8216M DP8226M				 0.95 0.9	 V V
V_{IH}	Input High Voltage		2			V
I_F	Input Load Current	$V_F = 0.45V$		−0.15	−0.5	mA
I_R	Input Leakage Current	$V_R = 5.5V$			80	μA
I_{CC}	Power Supply Current DP8216M DP8226M			 95 85	 130 120	 mA mA

Switching Characteristics (Notes 2, 3 and 4)

Symbol	Parameter	Conditions	Limits			Units
			Min	Typ	Max	
DP8216M, DP8226M, V_{CC} = 5V ±10%						
t_{PD1}	Input to Output Delay, DO Outputs	C_L = 30 pF, R_1 = 300Ω, R_2 = 600Ω		15	25	ns
t_{PD2}	Input to Output Delay, DB Outputs DP8216M DP8226M	C_L = 300 pF, R_1 = 90Ω, R_2 = 180Ω		 19 16	 33 25	 ns ns
t_E	Output Enable Time DP8216M DP8226M	DO Outputs: C_L = 30 pF, R_1 = 300Ω/10 kΩ, R_2 = 600Ω/1 kΩ DB Outputs: C_L = 300 pF, R_1 = 90Ω/10 kΩ, R_2 = 180Ω/1 kΩ		 42 36	 75 62	 ns ns
t_D	Output Disable Time DP8216M DP8226M	DO Outputs: C_L = 5 pF, R_1 = 300Ω/10 kΩ, R_2 = 600Ω/1 kΩ DB Outputs: C_L = 5 pF, R_1 = 90Ω/10 kΩ, R_2 = 180Ω/1 kΩ		 16 16	 40 38	 ns ns
DP8216, DP8226 V_{CC} = 5.0V ±5%						
t_{PD1}	Input to Output Delay, DO Outputs	C_L = 30 pF, R_1 = 300Ω, R_2 = 600Ω		15	25	ns
t_{PD2}	Input to Output Delay, DB Outputs DP8216 DP8226	C_L = 300 pF, R_1 = 90Ω, R_2 = 180Ω		 20 16	 30 25	 ns ns
t_E	Output Enable Time DP8216 DP8226	DO Outputs: C_L = 30 pF, R_1 = 300Ω/10 kΩ, R_2 = 600Ω/1 kΩ DB Outputs: C_L = 300 pF, R_1 = 90Ω/10 kΩ, R_2 = 180Ω/1 kΩ		 45 35	 65 54	 ns ns
t_D	Output Disable Time	DO Outputs: C_L = 5 pF, R_1 = 300Ω/10 kΩ, R_2 = 600Ω/1 kΩ DB Outputs: C_L = 5 pF, R_1 = 90Ω/10 kΩ, R_2 = 180Ω/1 kΩ		20	35	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: Unless otherwise specified, min/max limits apply across the −55°C to +125°C temperature range for the DP8216M and DP8226M and across the 0°C to +70°C temperature range for the DP8216 and DP8226. All typical values are given for V_{CC} = 5V and T_A = 25°C.

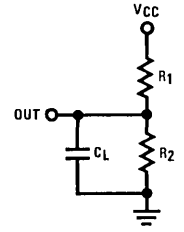
Note 3: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified.

Note 4: Only one output at a time should be shorted.

Test Conditions

Input pluse amplitude of 2.5V.
Input rise and fall times of 5.0 ns between 1.0V and 2.0V.
Output loading is 5.0 mA and 10 pF.
Speed measurements are made at 1.5V levels.

Test Load Circuit



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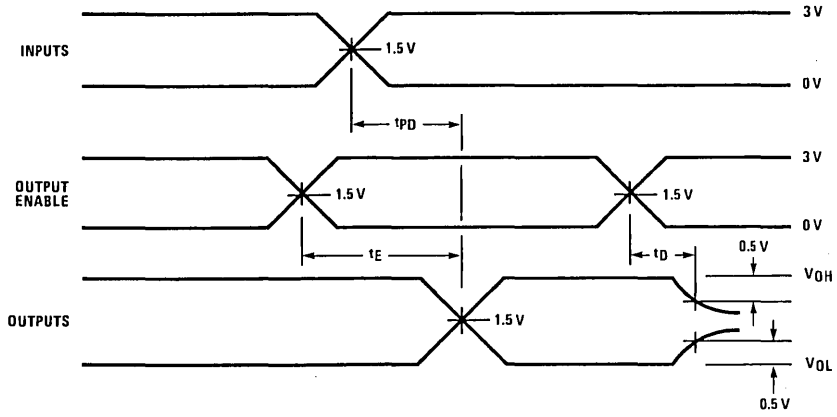
Switching Time Waveforms



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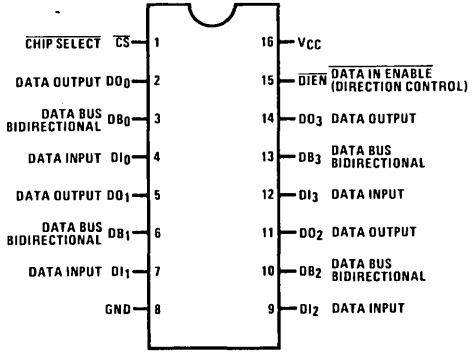
Connection Diagram

Dual-In-Line Package



TL/F/8753-3

Order Number DP8216J, DP8216N, DP8226J, DP8226N, DP8216MJ or DP8226MJ
See NS Package Number J16A or N16A

Capacitance $T_A = 25°C$

Symbol	Parameter	Limit			Unit
		Min	Typ	Min	
C_{IN}	Input Capacitance		4	6	pF
C_{OUT}	Output Capacitance				
	DO Outputs		6	10	pF
	DO Outputs		13	18	pF

Note: This parameter is periodically sampled and is not 100% tested. Condition of measurement is f = 1 MHz, V_{BIAS} = 2.5V, V_{CC} = 5.0V, and T_A = 25°C.

National Semiconductor Corporation

DP8224 Clock Generator and Driver

General Description

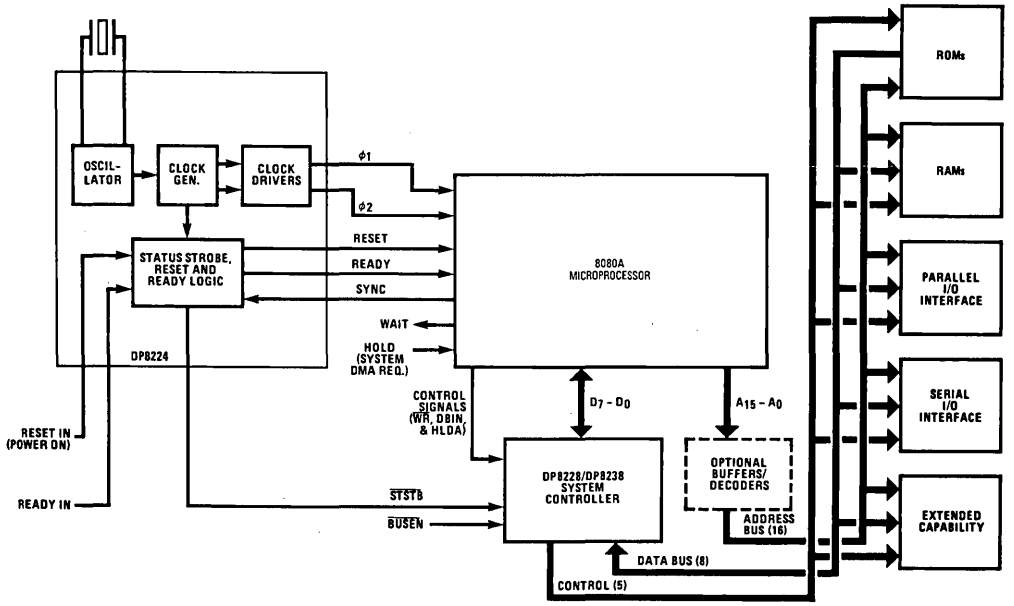
The DP8224 is a clock generator/driver contained in a standard, 16-pin dual-in-line package. The chip, which is fabricated using Schottky Bipolar technology, generates clocks and timing for the 8080A microcomputer family.

Included in the DP8224 is an oscillator circuit that is controlled by an external crystal, which is selected by the designer to meet a variety of system speed requirements. Also included in the chip are circuits that provide: a status strobe for the DP8228 or DP8238 system controllers, power-on reset for the 8080A microprocessor, and synchronization of the READY input to the 8080A.

Features

- Crystal-controlled oscillator for stable system operation
- Single chip clock generator and driver for 8080A microprocessor
- Provides status strobe for DP8228 or DP8238 system controllers
- Provides power-on reset for 8080A microprocessor
- Synchronizes READY input to 8080A microprocessor
- Provides oscillator output for synchronization of external circuits
- Reduces system component count

8080A Microcomputer Family Block Diagram



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Absolute Maximum Ratings (Note 2)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	
V_{CC}	7V
V_{DD}	15V
Input Voltage	−1V to +5.5V
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1509 mW
Molded Package	1476 mW
Lead Temperature (Soldering, 4 seconds)	260°C

*Derate cavity package 10.1 mW/°C above 25°C; derate molded package 11.8 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage			
V_{CC}	4.75	5.25	V
V_{DD}	11.4	12.6	V
Temperature (T_A)	0	+70	°C

Electrical Characteristics (Note 3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_F	Input Current Loading	V_F = 0.45V			−0.25	mA
I_R	Input Leakage Current	V_R = 5.25V			10	μA
V_C	Input Forward Clamp Voltage	I_C = −5 mA			−1.0	V
V_{IL}	Input "Low" Voltage	V_{CC} = 5V			0.8	V
V_{IH}	Input "High" Voltage	$\overline{RESIN}$ Input	2.6			V
		All Other Inputs	2.0			V
$V_{IH}-V_{IL}$	$\overline{RESIN}$ Input Hysteresis	V_{CC} = 5V	0.25			V
V_{OL}	Output "Low" Voltage					
	(φ1, φ2), Ready, Reset $\overline{STSTB}$	I_{OL} = 2.5 mA			0.45	V
	Osc., φ2 (TTL)	I_{OL} = 10 mA			0.45	V
	Osc., φ2 (TTL)	I_{OL} = 15 mA			0.45	V
V_{OH}	Output "High" Voltage					
	φ1, φ2	I_{OH} = −100 μA	9.4			V
	Ready, Reset	I_{OH} = −100 μA	3.6			V
	Osc., φ2 (TTL), $\overline{STSTB}$	I_{OH} = −1 mA	2.4			V
I_{SC}	Output Short-Circuit Current (All Low Voltage Outputs Only), (Note 1)	V_O = 0V, V_{CC} = 5V	−10		−60	mA
I_{CC}	Power Supply Current				115	mA
I_{DD}	Power Supply Current				12	mA

Note 1: Caution −φ1 and φ2 output drivers do not have short circuit protection.

Note 2: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 3: Unless otherwise specified min/max limits apply across the 0°C to +70°C range for the DP8224. All typical values are for T_A = 25°C, V_{CC} = 5V, and V_{DD} = 12V.

Crystal Requirements*

Tolerance	0.005% at 0°C to +70°C	Equivalent Resistance	75Ω to 20Ω
Resonance	Fundamental	Power Dissipation (Min)	4 mW
Load Capacitance	20 pF to 30 pF		

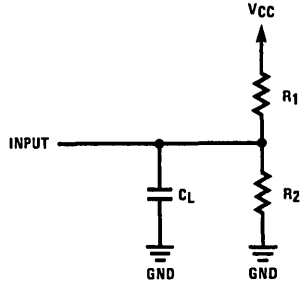
*It is good design practice to ground the case of the crystal

**With tank circuit, use 3rd overtone mode

Switching Characteristics (Note 3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$t_{\phi 1}$	$\phi 1$ Pulse Width	C_L = 20 pF to 50 pF	$\frac{2t_{CY}}{9} - 20$			ns
$t_{\phi 2}$	$\phi 2$ Pulse Width		$\frac{5t_{CY}}{9} - 35$			ns
t_{D1}	$\phi 1$ to $\phi 2$ Delay		0			ns
t_{D2}	$\phi 2$ to $\phi 1$ Delay		$\frac{2t_{CY}}{9} - 14$			ns
t_{D3}	$\phi 1$ to $\phi 2$ Delay		$\frac{2t_{CY}}{9}$		$\frac{2t_{CY}}{9} + 20$	ns
t_r	$\phi 1$ and $\phi 2$ Rise Time				20	ns
t_f	$\phi 1$ and $\phi 2$ Fall Time				20	ns
$t_{D\phi 2}$	$\phi 2$ to $\phi 2$ (TTL) Delay	$\phi 2$ TTL, C_L = 30 pF, R1 = 300Ω, R2 = 600Ω	−5		15	ns
t_{DSS}	$\phi 2$ to $\overline{STSTB}$ Delay	$\overline{STSTB}$, C_L = 15 pF R1 = 2 kΩ, R2 = 4 kΩ	$\frac{6t_{CY}}{9} - 30$		$\frac{6t_{CY}}{9}$	ns
t_{PW}	$\overline{STSTB}$ Pulse Width		$\frac{t_{CY}}{9} - 15$			ns
t_{DRS}	RDYIN Set-Up Time to Status Strobe		$50 - \frac{4t_{CY}}{9}$			ns
t_{DRH}	RDYIN Hold Time After $\overline{STSTB}$		$\frac{4t_{CY}}{9}$			ns
t_{DR}	READY or RESET to $\phi 2$ Delay	Ready and Reset, C_L = 10 pF, R1 = 2 kΩ, R2 = 4 kΩ	$\frac{4t_{CY}}{9} - 25$			ns
t_{CLK}	CLK Period			$\frac{t_{CY}}{9}$		ns
f_{MAX}	Maximum Oscillating Frequency		27			MHz
C_{IN}	Input Capacitance	V_{CC} = 5V, V_{DD} = 12V, V_{BIAS} = 2.5V, f = 1 MHz			8	pF

Test Circuit



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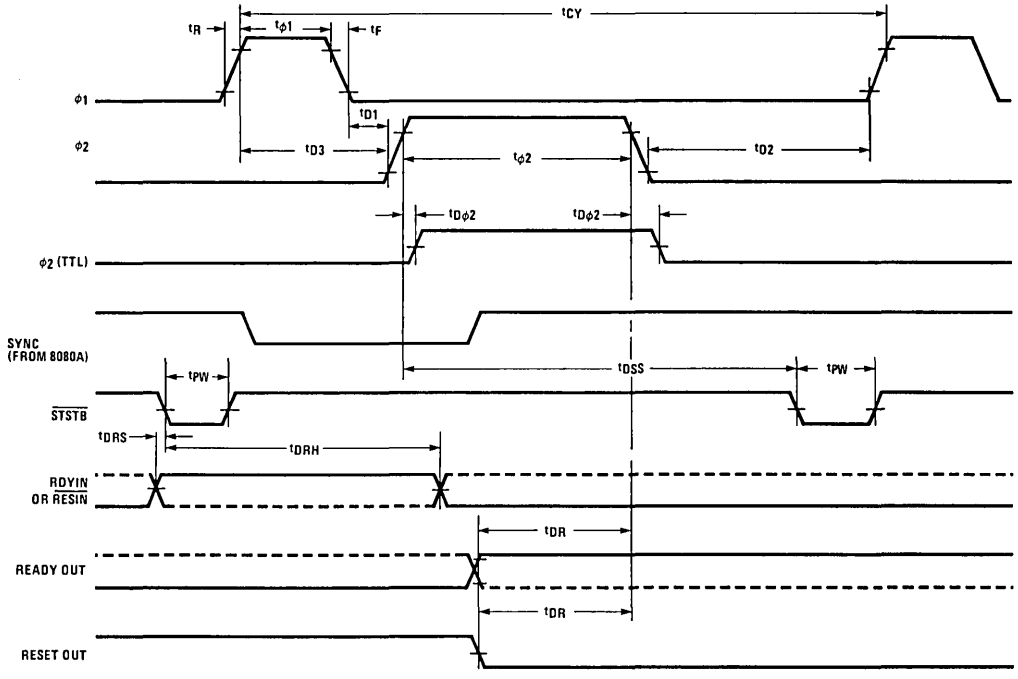
Waveforms



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Voltage Measurement Points: $\phi 1$, $\phi 2$ Logic "0" = 1.0V, Logic "1" = 8.0V. All other signals measured at 1.5V.

Switching Characteristics (For t_{CY} = 488.28 ns)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$t_{\phi 1}$	$\phi 1$ Pulse Width	$\phi 1$ and $\phi 2$ Loaded to C_L = 20 to 50 pF Ready and Reset Loaded to 2 mA/10 pF All Measurements Referenced to 1.5V unless Specified Otherwise	89			ns
$t_{\phi 2}$	$\phi 2$ Pulse Width		236			ns
t_{D1}	Delay $\phi 1$ to $\phi 2$		0			ns
t_{D2}	Delay $\phi 2$ to $\phi 1$		95			ns
t_{D3}	Delay $\phi 1$ to $\phi 2$ Leading Edges		109		129	ns
t_r	Output Rise Time				20	ns
t_f	Output Fall Time				20	ns
t_{DSS}	$\phi 2$ to $\overline{STSTB}$ Delay		296		326	ns
$t_{D\phi 2}$	$\phi 2$ to $\phi 2$ (TTL) Delay		−5		15	ns
t_{PW}	Status Strobe Pulse Width		40			ns
t_{DRS}	RDYIN Set-Up Time to $\overline{STSTB}$		−167			ns
t_{DRH}	RDYIN Hold Time after $\overline{STSTB}$		217			ns
t_{DR}	READY or RESET to $\phi 2$ Delay		192			ns
f_{MAX}	Oscillator Frequency				18.432	MHz

6

Functional Pin Definitions

The following describes the function of all of the DP8224 input/output pins. Some of these descriptions reference internal circuits.

INPUT SIGNALS

Crystal Connections (XTAL 1 and XTAL 2): Two inputs that connect an external crystal to the oscillator circuit of the DP8224. Normally, a fundamental mode crystal is used to determine the basic operating frequency of the oscillator. However, overtone mode crystals may also be used. The crystal frequency is 9 times the desired microprocessor speed (that is, crystal frequency equals $1/t_{CY} \times 9$). When the crystal frequency is above 10 MHz, a selected capacitor (3 to 10 pF) may have to be connected in series with the crystal to produce the exact desired frequency. *Figure A.*

Tank: Allows the use of overtone mode crystals with the oscillator circuit. When an overtone mode crystal is used, the tank input connects to a parallel LC network that is ac coupled to ground. The formula for determining the resonant frequency of this LC network is as follows:

$$F = \frac{1}{2\pi\sqrt{LC}}$$

Synchronizing (SYNC) Signal: When high, indicates the beginning of a new machine cycle. The 8080A microprocessor outputs a status word (which describes the current machine cycle) onto its data bus during the first state (SYNC interval) of each machine cycle.

Reset In ($\overline{\text{RESIN}}$): Provides an automatic system reset and start-up upon application of power as follows. The $\overline{\text{RESIN}}$ input, which is obtained from the junction of an external RC network that is connected between V_{CC} and ground, is routed to an internal Schmitt Trigger circuit. This circuit converts the slow transition of the power supply rise into a sharp, clean edge when its input reaches a predetermined value. When this occurs, an internal D-type flip-flop is synchronously reset, thereby providing the RESET output signal discussed below.

For manual system reset, a momentary contact switch that provides a low (ground) when closed is also connected to the $\overline{\text{RESIN}}$ input.

Ready In (RDYIN): An asynchronous READY signal that is re-clocked by a D-type flip-flop of the DP8224 to provide the synchronous READY output discussed below.

+5 Volts: V_{CC} supply.

+12 Volts: V_{DD} supply.

Ground: 0 volt reference.

OUTPUT SIGNALS

Oscillator (OSC): A buffered oscillator signal that can be used for external timing purposes.

ϕ_1 and ϕ_2 Clocks: Two non-TTL compatible clock phases that provide nonoverlapping timing references for internal storage elements and logic circuits of the 8080A microprocessor. The two clock phases are produced by an internal clock generator that consists of a divide-by-nine counter and the associated decode gating logic. *Figure B.*

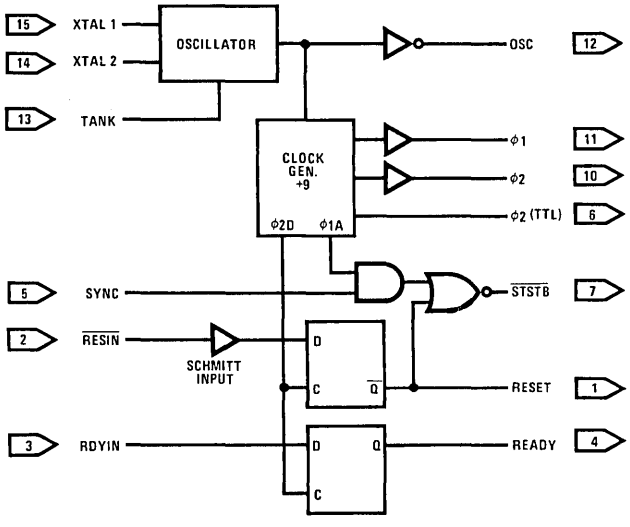
ϕ_2 (TTL) Clock: A TTL ϕ_2 clock phase that can be used for external timing purposes.

Status Strobe ($\overline{\text{STSTB}}$): Activated (low) at the start of each new machine cycle. The $\overline{\text{STSTB}}$ signal is generated by gating a high-level SYNC input with the ϕ_{1A} timing signal from the internal clock generator of the DP8224. The $\overline{\text{STSTB}}$ signal is used to clock status information into the status latch of the DP8228 system controller and bus driver.

Reset: When the RESET signal is activated, the content of the program counter of the 8080A is cleared. After RESET, the program will start at location 0 in memory.

Ready: The READY signal indicates to the 8080A that valid memory or input data is available. This signal is used to synchronize the 8080A with slower memory or input/output devices.

Logic and Connection Diagrams



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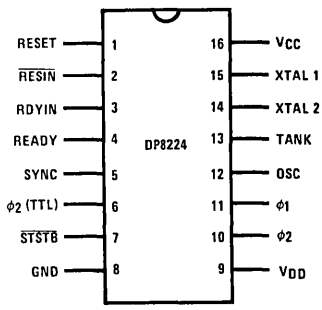
Dual-In-Line Package



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Top View

Order Number DP8224J or DP8224N
See NS Package Number
J16A or N16A

Applications Information

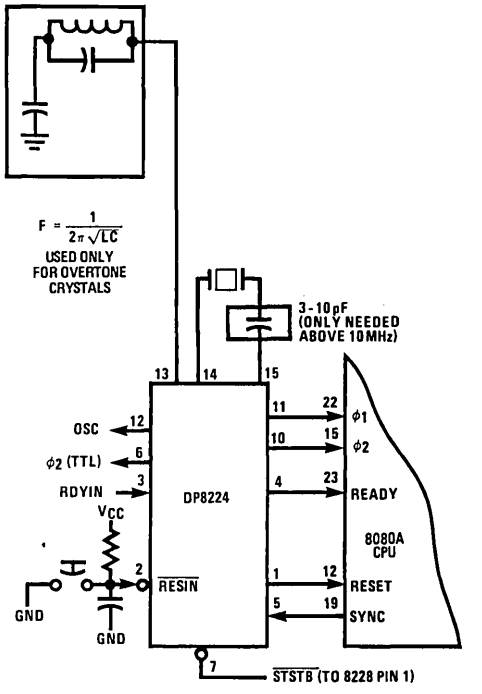

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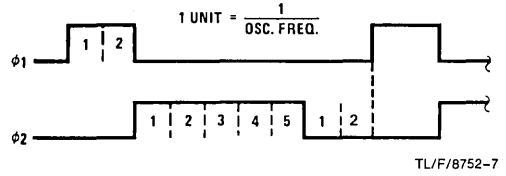
FIGURE A. DP8224 Connection Diagram



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EXAMPLE: (8080 t_{CY} = 500 ns)
OSC = 18 MHz/55 ns
ϕ_1 = 110 ns (2 × 55 ns)
ϕ_2 = 275 ns (5 × 55 ns)
ϕ_2-ϕ_1 = 110 ns (2 × 55 ns)

FIGURE B. DP8224 Clock Generator Waveforms

National Semiconductor Corporation

DP8228/DP8228M/DP8238/DP8238M System Controller and Bus Driver

General Description

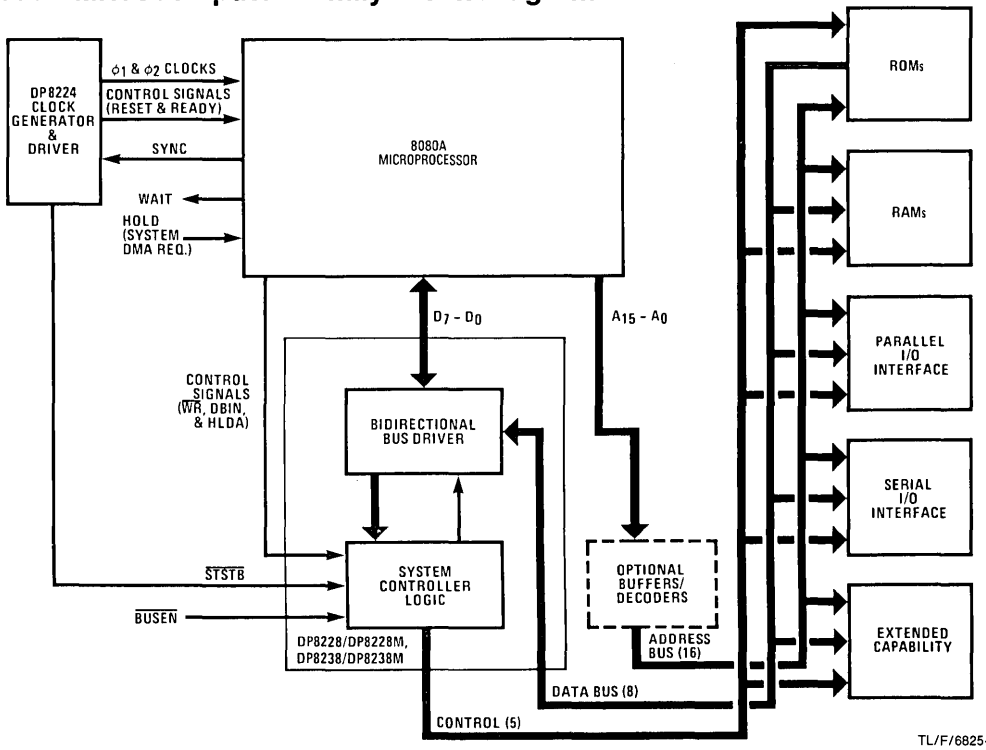
The DP8228/DP8228M, DP8238/DP8238M are system controller/bus drivers contained in a standard, 28-pin dual-in-line package. The chip, which is fabricated using Schottky Bipolar technology, generates all the read and write control signals required to directly interface the memory and input/output components of the 8080A microcomputer family. The chip also provides drive and isolation for the bidirectional data bus of the 8080A microprocessor. Data bus isolation enables the use of slower memory and input/output components in a system, and provides for enhanced system noise immunity.

A user-selected signal-level interrupt vector (RST 7) is provided by the device for use in the interrupt structure of small systems that need only one basic vector. No additional components (such as an interrupt instruction port) are required to use the single interrupt vector in these systems. The devices also generate an Interrupt Acknowledge ($\overline{INTA}$) control signal for each byte of a multibyte CALL instruction when an interrupt is acknowledged by the 8080A. This feature permits the use of a multilevel priority interrupt structure in large, interrupt-driven systems.

Features

- Single chip system controller and bus driver for 8080A Microcomputer Systems
- Allows use of multibyte CALL instructions for Interrupt Acknowledge
- Provides user-selected single-level interrupt vector (RST 7)
- Provides isolation of data bus
- Supports a wide variety of system bus structures
- Reduces system component count
- DP8238/DP8238M provides advanced Input/Output Write and Memory Write control signals for large system timing control

8080A Microcomputer Family Block Diagram



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Absolute Maximum Ratings

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Storage Temperature	−65°C to +150°C
Supply Voltage, V_{CC}	−0.5 to +7V
Input Voltage	−1.5V to +7V
Output Current	100 mA
Maximum Power Dissipation* at 25°C	
Cavity Package	2179 mW
Molded Package	2361 mW

*Derate cavity package 14.5 mW/°C above 25°C; derate molded package 18.9 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
DP8228M, DP8238M	4.50	5.50	V_{DC}
DP8228, DP8238	4.75	5.25	V_{DC}
Operating Temperature (T_A)			
DP8228M, DP8238M	−55	+125	°C
DP8228, DP8238	0	+70	°C

Note: *Maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended and should be limited to those conditions specified under DC electrical characteristics.*

Electrical Characteristics Min ≤ T_A ≤ Max, Min ≤ V_{CC} ≤ Max, unless otherwise noted

Symbol	Parameter		Conditions		Min	Typ (Note 1)	Max	Units
V_C	Input Clamp Voltage, All Inputs		V_{CC} = Min, I_C = −5 mA			0.6	−1.0	V
I_F	Input Load Current	$\overline{STSTB}$	V_{CC} = Max V_F = 0.45V for DP8228, DP8238 V_F = 0.40V for DP8228M, DP8238M				500	μA
		D2 and D6					750	μA
		D0, D1, D4, D5 and D7					250	μA
		All Other Inputs					250	μA
I_R	Input Leakage Current	DB0–DB7	V_{CC} = Max, V_R = V_{CC}				20	μA
		All Other Inputs					100	μA
V_{TH}	Input Threshold Voltage, All Inputs		V_{CC} = 5V		0.8		2.0	V
I_{CC}	Power Supply Current		V_{CC} = Max	DP8228, DP8238		160	190	mA
				DP8228M, DP8238M		160	210	mA
V_{OL}	Output Low Voltage	D0–D7	V_{CC} = Min, I_{OL} = 2 mA	DP8228M, DP8238M			0.50	V
				DP8228, DP8238			0.45	V
		All Other Outputs	V_{CC} = Min, I_{OL} = 10 mA	DP8228M, DP8238M			0.50	V
				DP8228, DP8238			0.45	V
V_{OH}	Output High	D0–D7	V_C = Min, I_{OL} = −10 μA	DP8228M, DP8238M	3.3	3.8		V
				DP8228, DP8238	3.6	3.8		V
		All Other Outputs	V_{CC} = Min, I_{OH} = −1 mA		2.4	3.8		V
I_{OS}	Short Circuit Current, All Outputs		V_{CC} = 5V, V_O = 0V		15		90	mA
$I_{O(OFF)}$	OFF State Output Current All Control Outputs		V_{CC} = Max, V_O = V_{CC}				100	μA
			V_{CC} = Max, V_O = 0.45V				−100	μA
I_{INT}	INTA Current		(See Test Conditions, *Figure 3*)				5	mA

Note 1: Typical values are for T_A = 25°C and typical supply voltages.

Capacitance* V_{BIAS} = 2.5V, V_{CC} = 5.0V, T_A = 25°C, f = 1 MHz

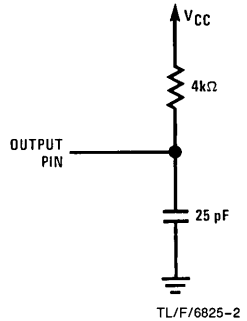
Symbol	Parameter	Min	Typ (Note 1)	Max	Units
C_{IN}	Input Capacitance		8	12	pF
C_{OUT}	Output Capacitance Control Signals		7	15	pF
I/O	I/O Capacitance (D or DB)		8	15	pF

*This parameter is periodically sampled and not 100% tested.

Switching Characteristics Min ≤ V_{CC} ≤ Max, Min ≤ T_A ≤ Max

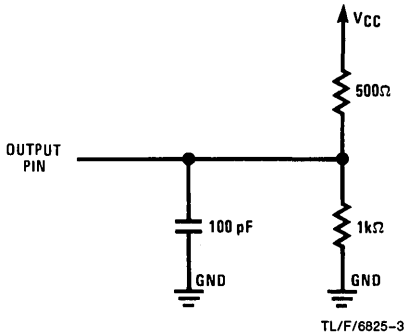
Symbol	Parameter	Conditions	DP8228M, DP8238M		DP8228, DP8238		Units
			Min	Max	Min	Max	
t_{PW}	Width of Status Strobe		25		22		ns
t_{SS}	Set-Up Time, Status Inputs D0–D7		8		8		ns
t_{SH}	Hold Time, Status Inuts D0–D7		5		5		ns
t_{DC}	Delay from $\overline{STSTB}$ to Any Control Signal	*(Figure 2)*	20	75	20	60	ns
t_{RR}	Delay from DBIN to Control Outputs	*(Figure 2)*		30		30	ns
t_{RE}	Delay from DBIN to Enable/ Disable 8080 Bus	*(Figure 1)*		45		45	ns
t_{RD}	Delay from System Bus to 8080 Bus During Read	*(Figure 1)*		45		30	ns
t_{WR}	Delay from $\overline{WR}$ to Control Outputs	*(Figure 2)*	5	60	5	45	ns
t_{WE}	Delay to Enable System Bus DB0–DB7 after $\overline{STSTB}$	*(Figure 2)*		30		30	ns
t_{WD}	Delay from 8080 Bus D0–D7 to System Bus DB0–DB7 During Write	*(Figure 2)*	5	40	5	40	ns
t_E	Delay from System Bus Enable to System Bus DB0–DB7	*(Figure 2)*		30		30	ns
t_{HD}	HLDA to Read Status Outputs	*(Figure 2)*		25		25	ns
t_{DS}	Set-Up Time, System Bus Inputs to HLDA		10		10		ns
t_{DH}	Hold Time, System Bus Inputs to HLDA		20		20		ns

Test Conditions



TL/F/6825-2

FIGURE 1. Test Load



TL/F/6825-3

FIGURE 2. Test Load

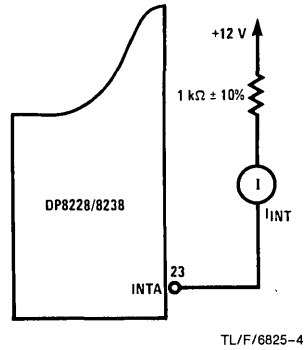


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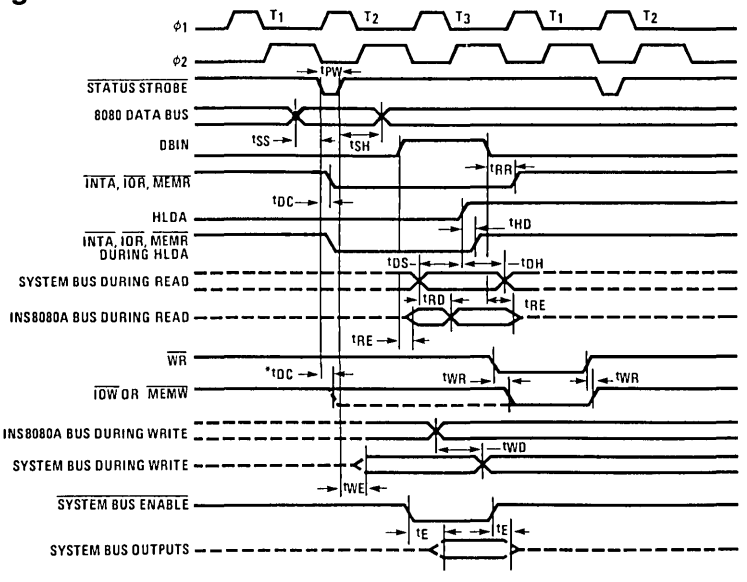
FIGURE 3. INTA Test Circuit (For RST 7)

Timing Diagram



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VOLTAGE MEASUREMENT POINTS: D_0–D_7 (when outputs) Logic "0" = 0.8V, Logic "0" = 0.8V, Logic "1" = 3.0V. All other signals measured at 1.5V.
*Advanced $\overline{I/OW}$ $\overline{MEMW}$ for 8238 only.

Functional Pin Definitions

The following describes the function of all of the DP8228/DP8228M, DP8238/DP8238M pinouts. Some of these descriptions reference internal circuits.

INPUT SIGNALS

Status Strobe ($\overline{STSTB}$): Activated (low) at the start of each new machine cycle. The $\overline{STSTB}$ input is used to store a status word (refer to chart) from the 8080A microprocessor into the internal status latch of the DP8228, DP8238. The status word is latched when the $\overline{STSTB}$ returns to the high state. The 8080A outputs this status word onto its data bus during the first state (SYNC interval) of each machine cycle.

Data Bus In (DBIN): When high, indicates that the 8080A data bus is in the input mode. The DBIN signal is used to gate data from memory or an input/output device onto the data bus.

Write ($\overline{WR}$): When low, indicates that the data on the 8080A data bus are stable for WRITE memory or output operation.

Hold Acknowledge (HLDA): When high, indicates that the 8080A data and address buses will go to their high impedance state. When in the data bus read mode, DBIN input in the high state, a high HLDA input will latch the data bus information into the driver circuits and gate off the applicable control signal $\overline{I/OR}$, $\overline{MEMR}$, or $\overline{INTA}$ (return to the output high state).

Bus Enable ($\overline{BUSEN}$): Asynchronous DMA input to the internal gating array. When low, normal operation of the internal bidirectional bus driver and gating array occurs. When high, the bus driver and gating array are driven to their high impedance state.

V_{CC} Supply: +5V.

Ground: 0V reference.

OUTPUT SIGNALS

Memory Read ($\overline{MEMR}$): When low, signals data to be loaded in from memory. The $\overline{MEMR}$ signal is generated by strobing in status word 1, 2, or 4. (Refer to status word chart.)

Memory Write ($\overline{MEMW}$): When low, signals data to be stored in memory. The $\overline{MEMW}$ signal is generated for the DP8238 by strobing in status word 3 or 5. (Refer to status word chart.) For the DP8228, the $\overline{MEMW}$ signal is generated by gating a low-level $\overline{WR}$ input with the strobed in status word 3 or 5.

Input/Output Read ($\overline{I/OR}$): When low, signals data to be loaded in from an addressed input/output device. The $\overline{I/OR}$ signal is generated by strobing in status word 6.

Input/Output Write ($\overline{I/OW}$): When low, signals data to be transferred to an addressed input/output device. The $\overline{I/OW}$ signal for the DP8238 is generated by strobing in status word 7. For the DP8238 the $\overline{I/OW}$ signal is generated by gating in a low-level $\overline{WR}$ input with the strobed in status word 7.

Interrupt Acknowledge ($\overline{INTA}$): When low, indicates that an interrupt has been acknowledged by the 8080A microprocessor. The $\overline{INTA}$ signal is generated by strobing in staus word 8 or 10.

Signal Level Interrupt (RST 7): When the $\overline{INTA}$ output is tied to 12V through a 1 kΩ resistor, strobing in status word 8 or 10 will cause the CPU data bus outputs, when active, to go to the high state.

INPUT/OUTPUT SIGNALS

CPU Data (D_7–D_0) Bus: This bus comprises eight TRI-STATE® input/output lines that connect to the 8080A microprocessor. The bus provides bidirectional communica-

Functional Pin Definitions (Continued)

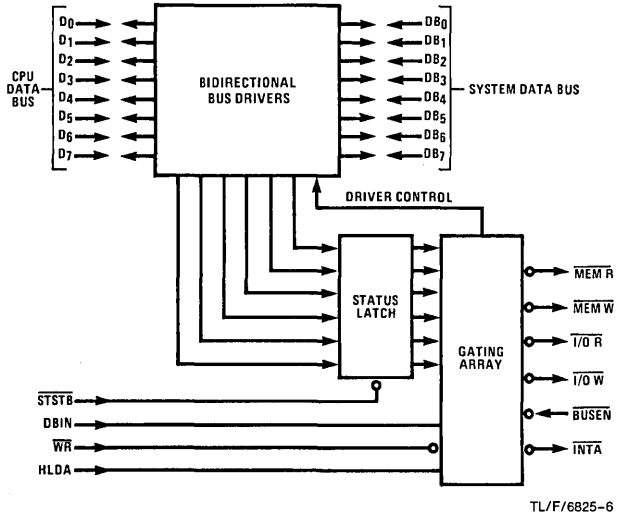
tion between the CPU, memory, and input/output devices for instructions and data transfers. A status word (which describes the current machine cycle) is also outputted on this data bus during the first microcycle of each machine cycle (SYNC = logic 1).

System Data (DB_7–DB_0) Bus: This bus comprises eight TRI-STATE input/output lines that connect to the memory and input/output components of the system. The internal bidirectional bus driver isolates the DB_7–DB_0 Data Bus from the D_7–D_0 Data Bus.

Status Word Chart

Machine Cycle	Status Word	Data Bus Bit								Control Signal
		D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
Instruction Fetch	1	1	0	1	0	0	0	1	0	$\overline{MEMR}$
Memory Read	2	1	0	0	0	0	0	1	0	$\overline{MEMR}$
Memory Write	3	0	0	0	0	0	0	0	0	$\overline{MEMW}$
Stack Read	4	1	0	0	0	0	1	1	0	$\overline{MEMR}$
Stack Write	5	0	0	0	0	0	1	0	0	$\overline{MEMW}$
Input Read	6	0	1	0	0	0	0	1	0	$\overline{I/OR}$
Output Write	7	0	0	0	1	0	0	0	0	$\overline{I/OW}$
Interrupt Acknowledge	8	0	0	1	0	0	0	1	1	$\overline{INTA}$
Halt Acknowledge	9	1	0	0	0	1	0	1	0	(none)
Interrupt Acknowledge While Halt	10	0	0	1	0	1	0	1	1	$\overline{INTA}$

Block and Connection Diagrams



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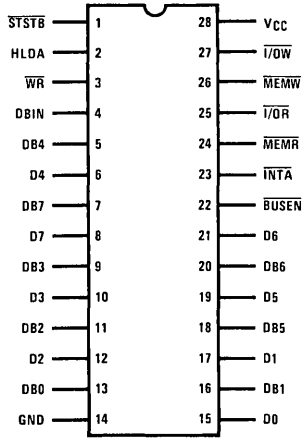
Dual-In-Line Package



TL/F/6825-7

Order Number DP8228J, DP8228MJ, DP8228N, DP8238J, DP8238MJ or DP8238N
See NS Package Number J28A or N28B

Section 7

Level Translators/Buffers

Section Contents

*Also available processed to various Military screening levels. Refer to Section 9.

Level Translators/Buffers

Several different families of logic circuits are available today, each offering advantages in certain applications. This wide selection of circuit types allows the design engineer to more easily construct functions and systems which meet his specific requirements.

Each of these logic "families", however, is produced using different processes, and their specific electrical characteristics are almost always different. Interfacing between these logic families can, at times, be difficult.

National Semiconductor offers a selection of level translators which can greatly simplify this task. The following selection guide outlines the level translator circuits available.

Level Translators/Buffers

Device Number		Logic Function	Output Characteristics	Output	Input	Page Number
0°C to +70°C	−55°C to +125°C					
DP8480		Inverting	TRI-STATE Fall Through Latch	TTL	10k ECL	7-5
DP8481		Inverting	Gated Fall Through Latch	10k ECL	TTL	7-8
DP8482		Inverting	TRI-STATE Fall Through Latch	TTL	10k ECL	7-11
DP8483		Inverting	Gated Fall Through Latch	100k ECL	TTL	7-14
DS3630	DS1630	Hex Buffer	50 ns Prop. Delay at 500 pF	CMOS	CMOS	7-17
DS8800	DS7800	Dual 2-Input Gate	Open-Collector −30V to 30V	PMOS	TTL	7-21
DS88L12	DS78L12	Hex Inverter	Active Pull-Up 0.4V to 14V	MOS	TTL	7-24
MM74C901	MM54C901	Hex Inverter	Active Pull-Up 0.4V @ 2.6 mA	TTL	CMOS	CMOS
MM74C902	MM54C902	Hex Buffer	Active Pull-Up 0.4V @ 3.2 mA	TTL	CMOS	CMOS
MM74C903	MM54C903	Hex Inverter	Active Pull-Up 0V to 15V	PMOS	CMOS	CMOS
MM74C904	MM54C904	Hex Buffer	Active Pull-Up 0V to 15V	PMOS	CMOS	CMOS
MM74C906	MM54C906	Hex Buffer	Open Drain 0V to 15V	NMOS	CMOS	CMOS
MM74C907	MM54C907	Hex Buffer	Open Drain V_{CC} to V_{CC} − 15V	PMOS	CMOS	CMOS

National Semiconductor Corporation

DP8480 10k ECL to TTL Level Translator with Latch

General Description

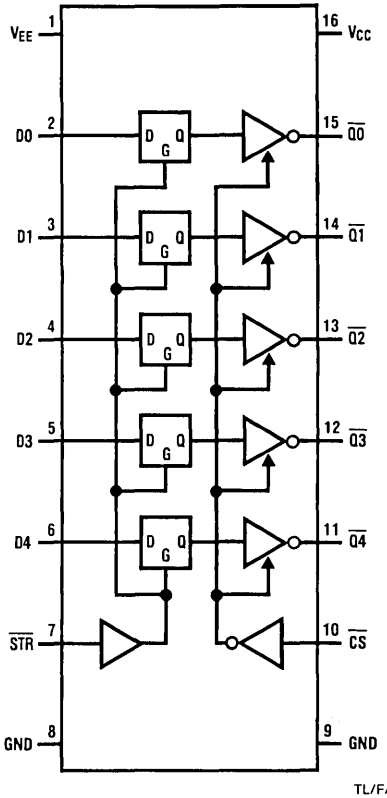
This circuit translates ECL input levels to TTL output levels and provides a fall-through latch. The TRI-STATE® outputs are designed to drive standard 50 pF loads. The strobe and chip select inputs operate at ECL levels.

Features

- 16-pin flat-pack or DIP
- TRI-STATE outputs
- ECL control inputs
- 8 ns typical propagation delay with 50 pF load
- Outputs are TRI-STATE during power up/down for glitch free operation
- 10k ECL input compatible

Logic and Connection Diagram

Dual-In-Line Package



TL/F/5861–1

Top View

Truth Table

D	$\overline{Q}$	$\overline{STR}$	$\overline{CS}$
H	L	L	L
L	H	L	L
X	$\overline{Q}$	H	L
X	Hi-Z	X	H

H = high level (most positive)
L = low level (most negative)
X = don't care

Order Number DP8480F, DP8480J or DP8480N
See NS Package F16B, J16A or N16A

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

V_{EE} Supply Voltage	−8V
V_{CC} Supply Voltage	7V
Input Voltage	GND to V_{EE}
Output Voltage	5.5V

Maximum Power Dissipation* at 25°C	
Molded Package	1476 mW
Storage Temperature	−65°C to +150°C

*Derate molded package 11.8 mW/°C above 25°C.

Recommended Operating Conditions

V_{EE} Supply Voltage	−5.2V ±10%
V_{CC} Supply Voltage	5.0V ±10%
T_A, Ambient Temperature	0°C to 75°C

Electrical Characteristics (TTL Logic) Notes 2, 3 and 4

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OL}	Output Low Voltage	I_{OL} = 12 mA			0.5	V
V_{OH}	Output High Voltage	I_{OH} = −10 mA	V_{CC} −2V			V
I_{AV}	Output Low Drive Current	Force 2.5V	70	150		mA
I_{OS}	Output High Drive Current	Force 0V	−70	−150	−350	mA
I_{OZ}	TRI-STATE Output Current		−50	1	+50	μA
I_{CC}	Supply Current				35	mA

Electrical Characteristics (ECL Logic) Notes 2 and 3

Symbol	Parameter	Conditions	T_A	Min	Typ	Max	Units
V_{IL}	Input Low Voltage	V_{EE} = −5.2V	0° C 25°C 75°C	−1870 −1850 −1830		−1490 −1475 −1450	mV
V_{IH}	Input High Voltage	V_{EE} = −5.2V	0°C 25°C 75°C	− 1145 −1105 −1045		−840 −810 −720	mV
I_{IL}	Input Low Current				50	85	μA
I_{IH}	Input High Current				75	350	μA
I_{EE}	Supply Current					−50	mA

Switching Characteristics Notes 2 and 5

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PD1}	Strobe to Output Delay	C_L = 50 pF	4	9	15	ns
t_{PD2}	Data to Output Delay	C_L = 50 pF	3.5	8	15	ns
t_S	Data Set-Up Time	(Note 6)	3.0	1.0		ns
t_H	Data Hold Time	(Note 6)	3.0	1.0		ns
t_{PW}	Strobe Pulse Width	(Note 6)	5.0	3.0		ns
t_{ZE}	Delay from Chip Select to Active State from Hi-Z State	C_L = 50 pF	6	15	25	ns
t_{EZ}	Delay from Chip Select to Hi-Z State from Active State	C_L = 50 pF	4.5	12	22	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified, min/max limits apply across the 0°C to 75°C ambient temperature range in still air and across the specified supply variations. All typical values are for T_A = 25°C and nominal supply. Maximum propagation delays are specified with all outputs switching simultaneously.

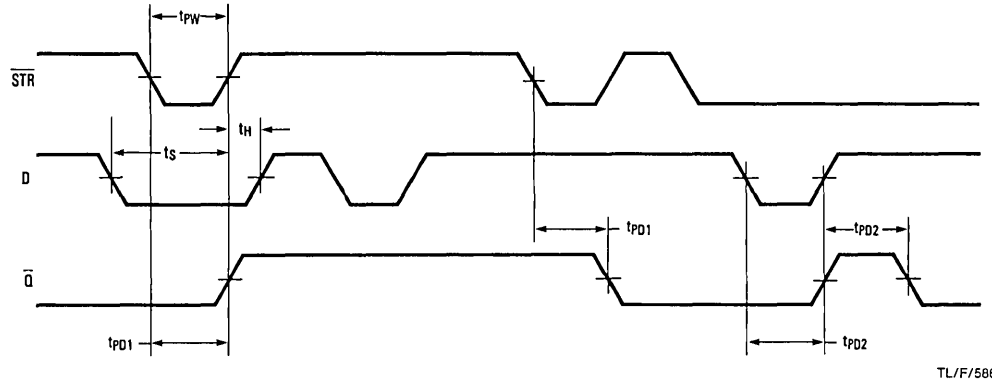
Note 3: All currents into device pins are shown as positive; all currents out of device pins are shown as negative. All voltages are referenced to ground, unless otherwise specified.

Note 4: When DC testing I_{AV} or I_{OS}, only one output should be tested at a time and the current limited to 120 MA max.

Note 5: Unless otherwise specified, all AC measurements are referenced from the 50% level of the ECL input to the 0.8V level on negative transitions or the 2.4V level on positive transitions of the output. ECL input rise and fall times are 2.0 ns ± 0.2 ns from 20% to 80%.

Note 6: Caution should be used when latching data while the outputs are switching. TTL outputs generate severe ground noise when switching. This noise can be sufficient to cause the ECL latch to loose data. Board mounting and good supply decoupling are desirable. The worst case conductions are with all outputs switching low simultaneously, the maximum capacitive loading on the outputs and the maximum V_{CC} supply voltage applied.

Switching Time Waveforms



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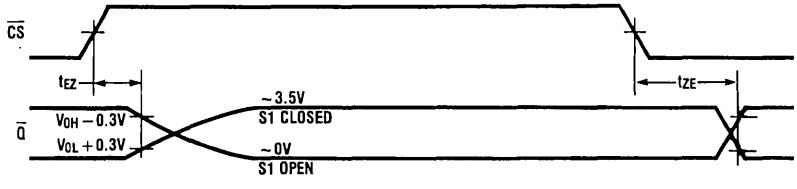
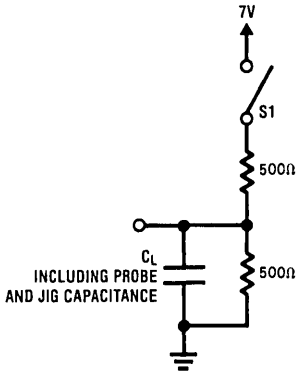
S1 open



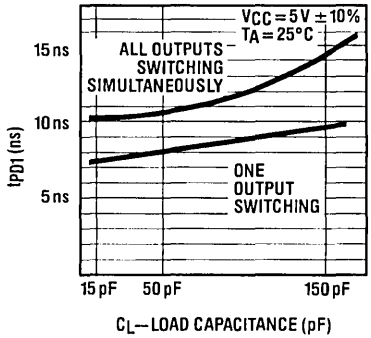
TL/F/5861–3

Test Load

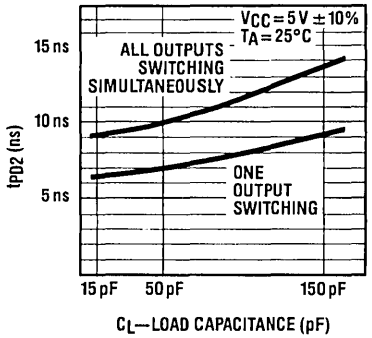


TL/F/5861–4

Typical Performance Versus CL



TL/F/5861–5



TL/F/5861–6

National Semiconductor Corporation

DP8481 TTL to 10k ECL Level Translator with Latch

General Description

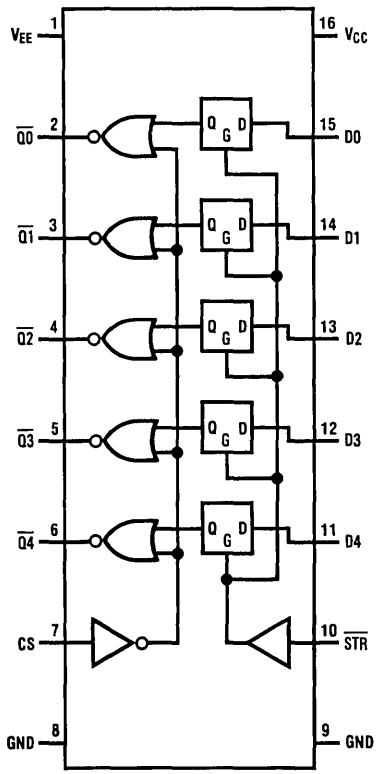
This circuit translates TTL input levels to ECL output levels and provides a fall-through latch. The outputs are gated with CS providing for wire ORing of outputs. The strobe and chip select inputs operate at ECL levels.

Features

- 16-pin flat-pack or DIP
- ECL control inputs
- CS provided for wire ORing of output bus
- 10k ECL I/O compatible
- 3.0 ns typical propagation delay

Logic and Connection Diagram

Dual-In-Line Package



TL/F/5862–1

Top View

Truth Table

D	$\overline{Q}$	$\overline{STR}$	CS
H	L	L	H
L	H	L	H
X	$\overline{Q}$	H	H
X	L	X	L

H = high level (most positive)
L = low level (most negative)
X = don't care

Order Number
DP8481F, DP8481J or DP8481N
See NS Package
F16B, J16A or N16A

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

V_{EE} Supply Voltage	−8V
V_{CC} Supply Voltage	7V
Input Voltage (ECL)	GND to V_{EE}
Input Voltage (TTL)	−1V to 5.5V
Output Current	50 mA
Maximum Power Dissipation* at 25°C Molded Package	1476 mW
Storage Temperature	−65°C to +150°C

*Derate molded package 11.8 mW/°C above 25°C.

Recommended Operating Conditions

V_{EE} Supply Voltage	−5.2V ±10%
V_{CC} Supply Voltage	5.0V ±10%
T_A, Ambient Temperature	0°C to 75°C

Electrical Characteristics (TTL Logic) (Notes 2 and 3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IL}	Input Low Voltage				0.8	V
V_{IH}	Input High Voltage		2.0			V
I_{IL}	Input Low Current	V_{IN} = 0.5V		−25	−200	μA
I_{IH}	Input High Current	V_{IN} = 2.5V		1.0	40	μA
V_{CLAMP}	Input Clamp Voltage	I_{IN} = −12 mA		−0.9	−1.2	V
I_{CC}	Supply Current	V_{CC} = 5.5V		10	20	mA

Electrical Characteristics (ECL Logic) (Notes 2 and 3)

Symbol	Parameter	Conditions	T_A	Min	Typ	Max	Units
V_{IL}	Input Low Voltage	V_{EE} = −5.2V	0°C 25°C 75°C	−1870 −1850 −1830		−1490 −1475 −1450	mV
V_{IH}	Input High Voltage	V_{EE} = −5.2V	0°C 25°C 75°C	−1145 −1105 −1045		−840 −810 −720	mV
I_{IL}	Input Low Current	V_{IN} = −1.8V			55	150	μA
I_{IH}	Input High Current	V_{IN} = −0.8V			85	200	μA
V_{OL}	Output Low Voltage	V_{EE} = −5.2V	0°C 25°C 75°C	−1870 −1850 −1830		−1665 −1650 −1625	mV
V_{OH}	Output High Voltage	V_{EE} = −5.2V	0°C 25°C 75°C	−1000 −960 −900		−840 −810 −720	mV
V_{OLC}	Output Low Voltage	V_{EE} = −5.2V	0°C 25°C 75°C			−1645 −1630 −1605	mV
V_{OHC}	Output High Voltage	V_{EE} = −5.2V	0°C 25°C 75°C	−1020 −980 −920			mV
I_{EE}	Supply Current	V_{EE} = −5.7V			−70	−90	mA

Switching Characteristics (Notes 2 and 4)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PD1}	Strobe To Output Delay		1.5	3.0	6.0	ns
t_{PD2}	Data To Output Delay		2.5	4.5	7.5	ns
t_S	Data Set-Up Time to Strobe		5.0	2.0		ns
t_H	Data Hold Time		1.0	0		ns
t_{PW}	Strobe Pulse Width		5.0	3.0		ns
t_{PD3}	Chip Select to Output Delay		1.0	2.5	4.0	ns
t_{SCS}	Data Set-Up Time to Chip Select		5.5	3.0		ns

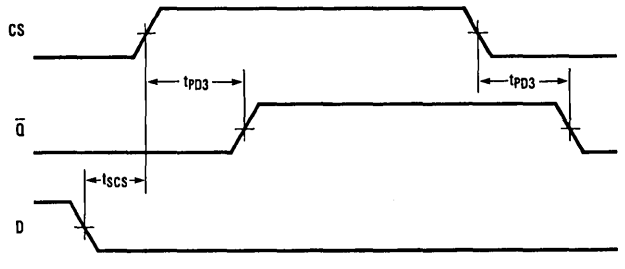
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified, min/max limits apply across the 0°C to 75°C ambient temperature range in still air and across the specified supply variations. All typical values are for 25°C and nominal supply.

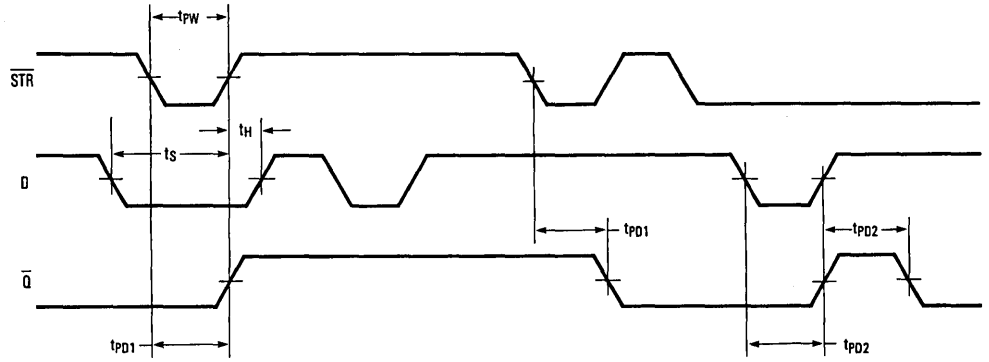
Note 3: All currents into device pins are shown as positive; all currents out of device pins are shown as negative. All voltages are referenced to ground, unless otherwise specified.

Note 4: Unless otherwise specified, all AC measurements are referenced from the 1.5V level of the TTL input and to/from the 50% point of the ECL signal and a 50Ω resistor to −2V is the load. ECL input rise and fall times are 2.0 ns ±0.2 ns from 20% to 80%. TTL input characteristic is 0V to 3V with $t_r = t_f \leq 3$ ns measured from 10% to 90%.

Switching Time Waveforms



TL/F/5862-2



TL/F/5862-3

National Semiconductor Corporation

DP8482 100k ECL to TTL Level Translator with Latch

General Description

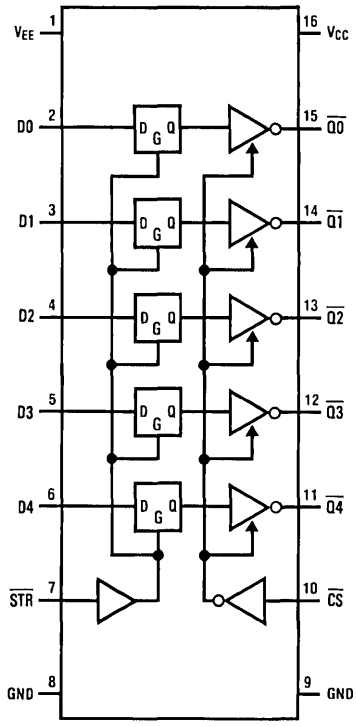
This circuit translates ECL input levels to TTL output levels and provides a fall-through latch. The TRI-STATE® outputs are designed to drive standard 50 pF loads. The strobe and chip select inputs operate at ECL levels.

Features

- 16-pin flat-pack or DIP
- TRI-STATE outputs
- ECL control inputs
- 8 ns typical propagation delay with 50 pF load
- Outputs are TRI-STATE during power up/down for glitch free operation
- 100k ECL input compatible

Logic and Connection Diagram

Dual-In-Line Package



TL/F/5863–1

Top View

Truth Table

D	$\overline{Q}$	$\overline{STR}$	$\overline{CS}$
H	L	L	L
L	H	L	L
X	$\overline{Q}$	H	L
X	Hi-Z	X	H

H = high level (most positive)
L = low level (most negative)
X = don't care

Order Number DP8482F, DP8482J or DP8482N
See NS Package Number F16B, J16A or N16A

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

V_{EE} Supply Voltage	−8V
V_{CC} Supply Voltage	7V
Input Voltage	GND to V_{EE}
Output Voltage	5.5V
Maximum Power Dissipation* at 25°C	
Molded Package	1476 mW
Storage Temperature	−65°C to +150°C

*Derate molded package 11.8 mW/°C above 25°C.

Recommended Operating Conditions

V_{EE} Supply Voltage	−4.5V ± 7%
V_{CC} Supply Voltage	5.0V ± 10%
T_A, Ambient Temperature	0°C to 85°C

Electrical Characteristics (TTL Logic) (Notes 2, 3 and 4)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OL}	Output Low Voltage	I_{OL} = 12 mA			0.5	V
V_{OH}	Output High Voltage	I_{OH} = −10 mA	V_{CC} − 2V			V
I_{AV}	Output Low Drive Current	Force 2.5V	70	150		mA
I_{OS}	Output High Drive Current	Force 0V	−70	−150	−350	mA
I_{OZ}	TRI-STATE Output Current		−50	1	+50	μA
I_{CC}	Supply Current				35	mA

Electrical Characteristics (ECL Logic) (Notes 2 and 3)

Symbol	Parameter	Conditions	T_A	Min	Typ	Max	Units
V_{IL}	Input Low Voltage	V_{EE} = −4.5V		−1810		−1475	mV
V_{IH}	Input High Voltage	V_{EE} = −4.5V		−1165		−880	mV
I_{IL}	Input Low Current				50	85	μA
I_{IH}	Input High Current				75	500	μA
I_{EE}	Supply Current					−50	mA

Switching Characteristics (Notes 2 and 5)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PD1}	Strobe to Output Delay	C_L = 50 pF	4	9	15	ns
t_{PD2}	Data to Output Delay	C_L = 50 pF	3.5	8	15	ns
t_S	Data Set-Up Time	(Note 6)	3.0	1.0		ns
t_H	Data Hold Time	(Note 6)	3.0	1.0		ns
t_{PW}	Strobe Pulse Width	(Note 6)	5.0	3.0		ns
t_{ZE}	Delay from Chip Select to Active State from Hi-Z State	C_L = 50 pF	6	15	25	ns
t_{EZ}	Delay from Chip Select to Hi-Z State from Active State	C_L = 50 pF	4.5	12	22	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified, min/max limits apply across the 0°C to 85°C ambient temperature range in still air and across the specified supply variations. All typical values are for T_A = 25°C and nominal supply. Maximum propagation delays are specified with all outputs switching simultaneously.

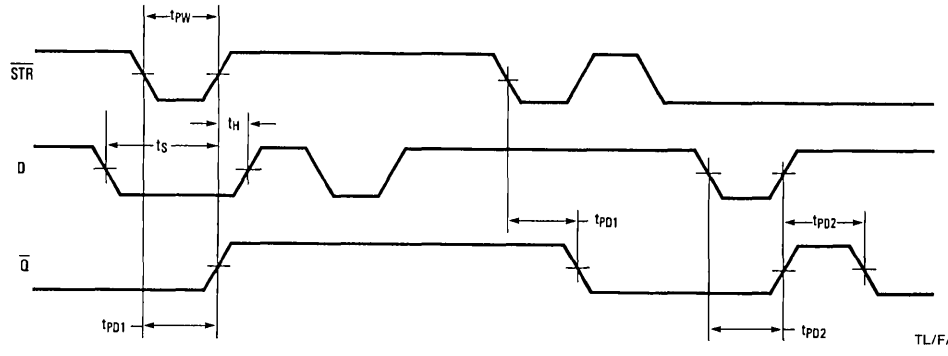
Note 3: All currents into device pins are shown as positive; all currents out of device pins are shown as negative. All voltages are referenced to ground, unless otherwise specified.

Note 4: When DC testing I_{AV} or I_{OS}, only one output should be tested at a time and the current limited to 120 mA max.

Note 5: Unless otherwise specified, all AC measurements are referenced from the 50% level of the ECL input to the 0.8V level on negative transitions or the 2.4V level on positive transitions of the output. ECL input rise and fall times are 0.7 ns ± 0.1 ns from 20% to 80%.

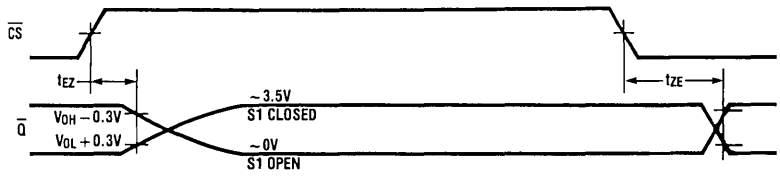
Note 6: Caution should be used when latching data while the outputs are switching. TTL outputs generate severe ground noise when switching. This noise can be sufficient to cause the ECL latch to lose data. Board mounting and good supply decoupling are desirable. The worst case conditions are with all outputs switching low simultaneously, the maximum capacitive loading on the outputs and the maximum V_{CC} supply voltage applied.

Switching Time Waveforms



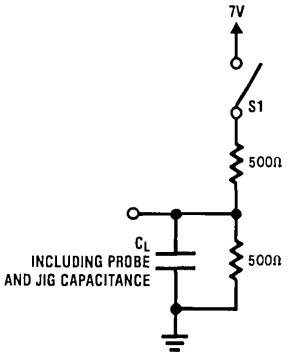
TL/F/5863-2

S1 open



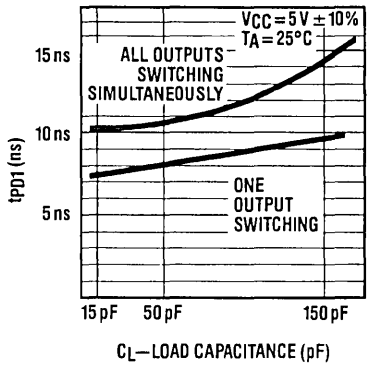
TL/F/5863-3

Test Load

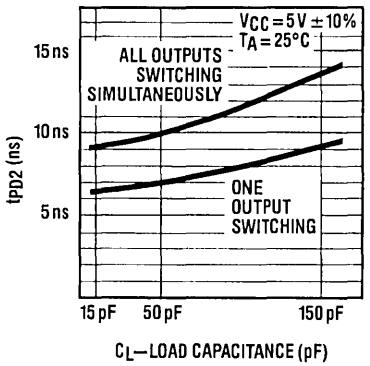


TL/F/5863-4

Typical Performance Versus C_L



TL/F/5863-5



TL/F/5863-6

National Semiconductor Corporation

DP8483 TTL to 100k ECL Level Translator with Latch

General Description

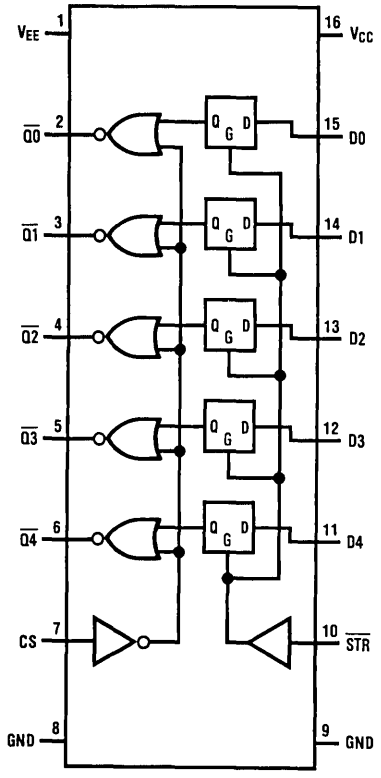
This circuit translates TTL input levels to ECL output levels and provides a fall-through latch. The outputs are gated with CS providing for wire ORing of outputs. The strobe and chip select inputs operate at ECL levels.

Features

- 16-pin flat-pack or DIP
- ECL control inputs
- CS provided for wire ORing of output bus
- 100k ECL I/O compatible
- 3.0 ns typical propagation delay

Logic and Connection Diagram

Dual-In-Line Package



Top View

Truth Table

D	$\overline{Q}$	$\overline{STR}$	CS
H	L	L	H
L	H	L	H
X	$\overline{Q}$	H	H
X	L	X	L

H = high level (most positive)
L = low level (most negative)
X = don't care

Order Number DP8483F, DP8483J or DP8483N
See NS Package Number F16B, J16A or N16A

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

V_{EE} Supply Voltage	−8V
V_{CC} Supply Voltage	7V
Input Voltage (ECL)	GND to V_{EE}
Input Voltage (TTL)	−1V to 5.5V
Output Current	50 mA
Maximum Power Dissipation* at 25°C	
Molded Package	1476 mW
Storage Temperature	−65°C to +150°C

*Derate molded package 11.8 mW/°C above 25°C.

Recommended Operating Conditions

V_{EE} Supply Voltage	−4.5V +7%
V_{CC} Supply Voltage	5.0V ±10%
T_A, Ambient Temperature	0°C to 85°C

Electrical Characteristics (TTL Logic) (Notes 2 and 3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IL}	Input Low Voltage				0.8	V
V_{IH}	Input High Voltage		2.0			V
I_{IL}	Input Low Current	$V_{IN}=0.5V$		−25	−200	μA
I_{IH}	Input High Current	$V_{IN}=2.5V$		1.0	40	μA
V_{CLAMP}	Input Clamp Voltage	$I_{IN}=-12$ mA		−0.9	−1.2	V
I_{CC}	Supply Current	$V_{CC}=5.5V$		10	20	mA

Electrical Characteristics (ECL Logic) (Notes 2 and 3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IL}	Input Low Voltage	$V_{EE}=-4.5V$	−1810		−1475	mV
V_{IH}	Input High Voltage	$V_{EE}=-4.5V$	−1165		−880	mV
I_{IL}	Input Low Current	$V_{IN}=-1.8V$		45	150	μA
I_{IH}	Input High Current	$V_{IN}=-0.8V$		75	200	μA
V_{OL}	Output Low Voltage	$V_{EE}=-4.5V$	−1810	−1705	−1620	mV
V_{OH}	Output High Voltage	$V_{EE}=-4.5V$	−1025	−955	−880	mV
V_{OLC}	Output Low Voltage	$V_{EE}=-4.5V$			−1610	mV
V_{OHC}	Output High Voltage	$V_{EE}=-4.5V$	−1035			mV
I_{EE}	Supply Current	$V_{EE}=-4.8V$		−65	−85	mA

Switching Characteristics (Notes 2 and 4)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PD1}	Strobe To Output Delay	(Note 4)	1.5	3.0	6.0	ns
t_{PD2}	Data To Output Delay		2.5	4.5	7.5	ns
t_S	Data Set-Up Time to Strobe		5.0	2.0		ns
t_H	Data Hold Time		1.0	0		ns
t_{PW}	Strobe Pulse Width		5.0	3.0		ns
t_{PD3}	Chip Select to Output Delay		1.0	2.5	4.0	ns
t_{SCS}	Data Set-Up Time to Chip Select		5.5	3.0		ns

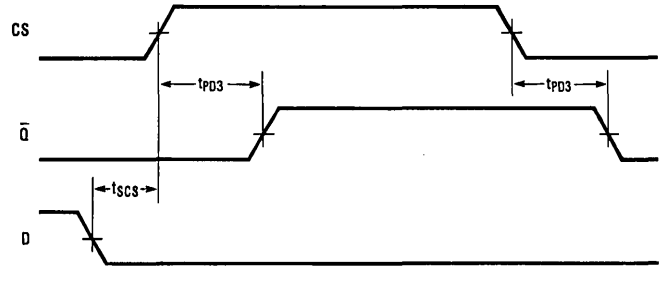
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified, min/max limits apply across the 0°C to 85°C ambient temperature range in still air and across the specified supply variations. All typical values are for 25°C and nominal supply.

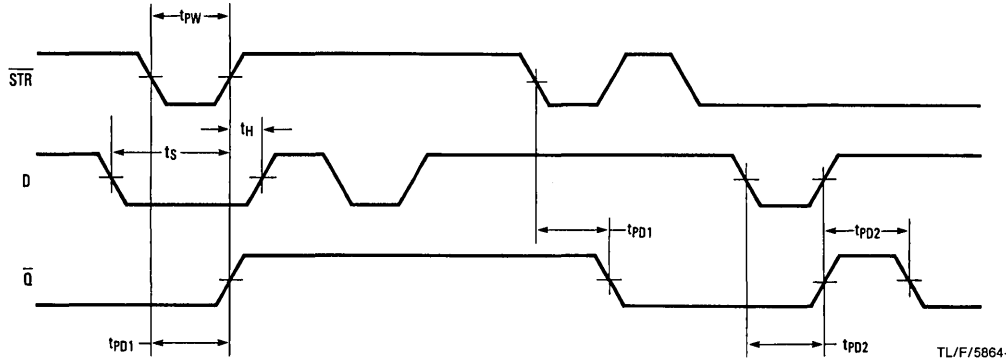
Note 3: All currents into device pins are shown as positive; all currents out of device pins are shown as negative. All voltages are referenced to ground, unless otherwise specified.

Note 4: Unless otherwise specified, all AC measurements are referenced from the 1.5V level of the TTL input and to/from the 50% point of the ECL signal and a 50Ω resistor to −2V is the load. ECL input rise and fall times are 0.7 ns ±0.1 ns from 20% to 80%. TTL input characteristics is 0V to 3V with $t_r=t_f\leq 3$ ns measured from 10% to 90%.

Switching Time Waveforms



TL/F/5864–2



TL/F/5864–3

National Semiconductor Corporation

DS1630/DS3630 Hex CMOS Compatible Buffer

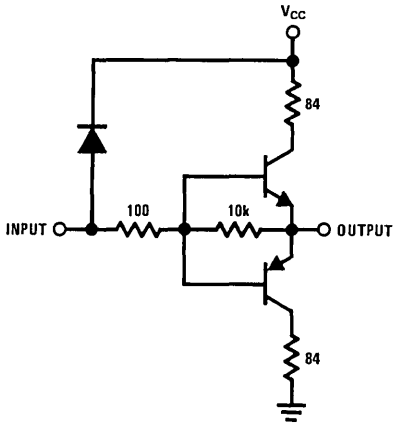
General Description

The DS1630/DS3630 is a high current buffer intended for use with CMOS circuits interfacing with peripherals requiring high drive currents. The DS1630/DS3630 features low quiescent power consumption (typically 50 μW) as well as high-speed driving of capacitive loads such as large MOS memories. The design of the DS1630/DS3630 is such that V_{CC} current spikes commonly found in standard CMOS circuits cannot occur, thereby, reducing the total transient and average power when operating at high frequencies.

Features

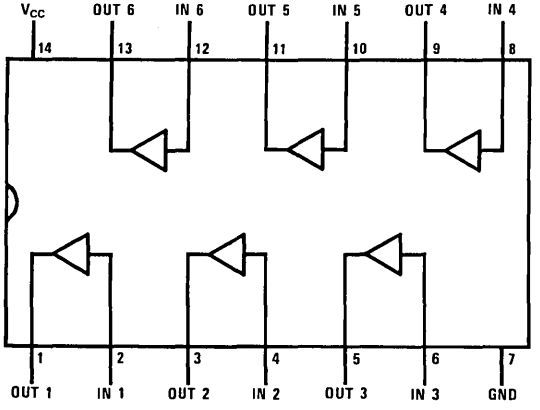
- High-speed capacitive driver
- Wide supply voltage range
- Input/output may interface to TTL
- Input/output CMOS compatibility
- No internal transient V_{CC} current spikes
- 50 μW typical standby power

Equivalent Schematic and Connection Diagrams



TL/F/5826-1

Dual-In-Line Package



TL/F/5826-2

Top View

Order Number DS1630J, DS3630J or DS3630N
See NS Package Number J14A or N14A

Absolute Maximum Ratings

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	16V
Input Voltage	16V
Output Voltage	16V
Lead Temperature (Soldering, 4 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	3	15	V
Temperature (T_A)			
DS1630	−55	+125	°C
DS3630	0	+70	°C

Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
I_{INH}	Logical "1" Input Current	$V_{IN} = V_{CC}$, $I_{OUT} = -400\ \mu A$	DS1630		90	200	μA
			DS3630		90	200	μA
		$V_{IN} = V_{CC} - 2.0V$, $I_{OUT} = 16$ mA	DS1630		0.5	3.2	mA
			DS3630		0.5	1.5	mA
I_{INL}	Logical "0" Input Current	$V_{IN} = 0.4V$, $I_{OUT} = 16$ mA	DS1630		−0.15	−1	mA
			DS3630		$V_{CC} - 150$	−800	μA
V_{OH}	Logical "1" Output Voltage	$V_{IN} = V_{CC}$, $I_{OUT} = -400\ \mu A$	DS1630	$V_{CC} - 1$	$V_{CC} - 0.75$		V
			DS3630	$V_{CC} - 0.9$	$V_{CC} - 0.75$		V
		$V_{IN} = V_{CC} - 0.4V$, $I_{OUT} = -16$ mA	DS1630	$V_{CC} - 2.5$	$V_{CC} - 2.0$		V
			DS3630	$V_{CC} - 2.5$	$V_{CC} - 2.0$		V
V_{OL}	Logical "0" Output Voltage	$V_{IN} = 0V$, $I_{OUT} = 400\ \mu A$	DS1630		0.75	1	V
			DS3630		0.75	0.9	V
		$V_{IN} = 0V$, $I_{OUT} = 16$ mA	DS1630		0.95	1.3	V
			DS3630		0.95	1.3	V
		$V_{IN} = 0.4V$, $I_{OUT} = 16$ mA	DS1630		1.2	1.6	V
			DS3630		1.2	1.5	V

Switching Characteristics $V_{CC} = 5.0V$, $T_A = 25°C$ unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd0}	Propagation Delay to a Logical "0"	$C_L = 50$ pF		30	45	ns
		$C_L = 250$ pF		40	60	ns
		$C_L = 500$ pF		50	75	ns
t_{pd1}	Propagation Delay to a Logical "1"	$C_L = 50$ pF		15	25	ns
		$C_L = 250$ pF		35	50	ns
		$C_L = 500$ pF		50	75	ns

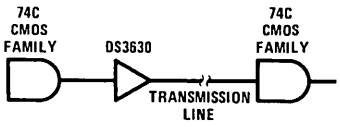
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for 'Operating Temperature Range" they are not meant to imply that the devices should be operating at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS1630 and across the 0°C to +70°C range for the DS3630. All typicals are given for $V_{CC} = 5.0V$ and $T_A = 25°C$.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

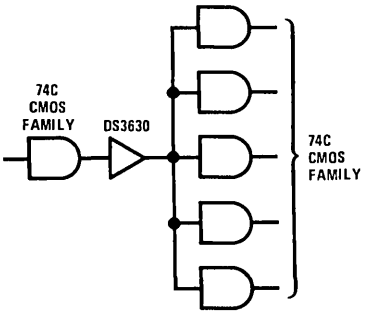
Typical Applications

CMOS to Transmission Line Interface



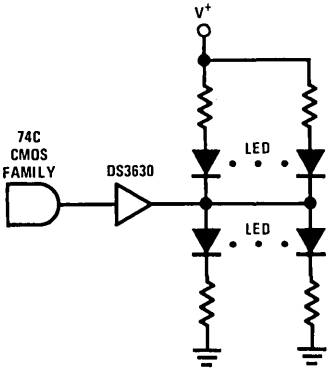
TL/F/5826-3

CMOS to CMOS Interface



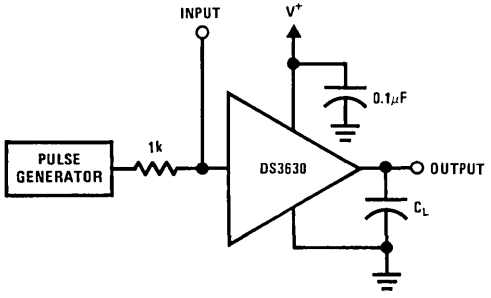
TL/F/5826-4

LED Driver



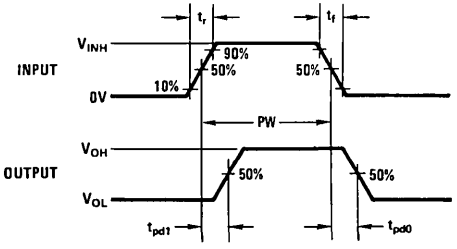
TL/F/5826-5

AC Test Circuit and Switching Time Waveforms



TL/F/5826-7

C_L includes probe and jig capacitance



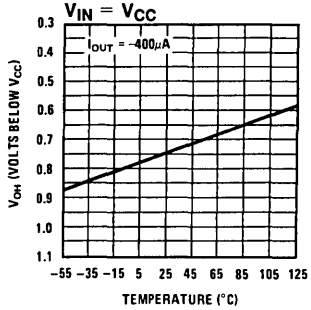
TL/F/5826-8

Pulse Generator characteristics: PRR = 1.0 MHz, PW = 500 ns, $t_r = t_f < 10$ ns, $V_{IN} = 0$ to V_{CC}

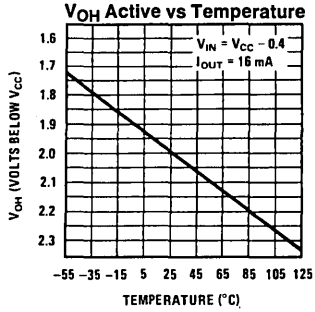
7

Typical Performance Characteristics

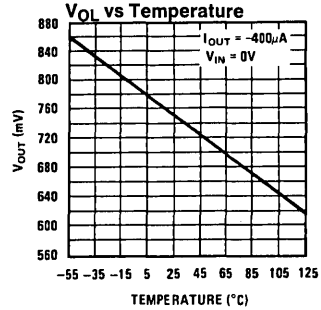
V_{OH} vs Temperature, $V_{IN} = V_{CC}$



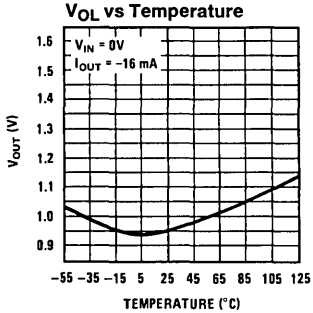
V_{OH} Active vs Temperature



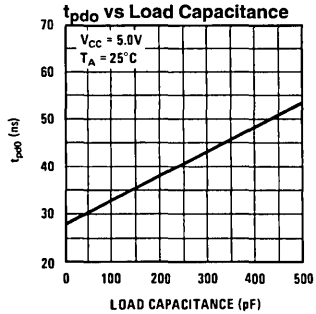
V_{OL} vs Temperature



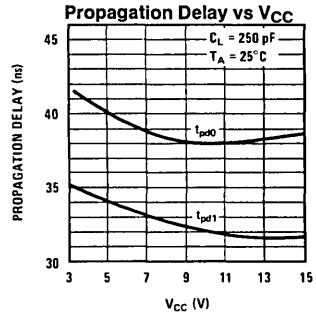
V_{OL} vs Temperature



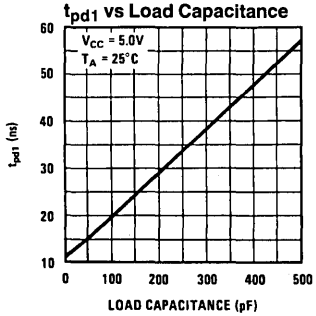
t_{pdo} vs Load Capacitance



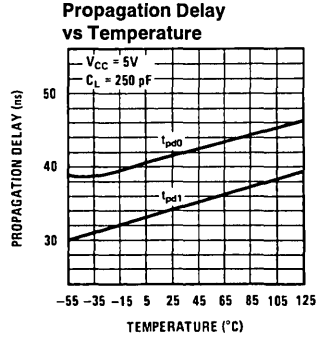
Propagation Delay vs V_{CC}



t_{pd1} vs Load Capacitance



Propagation Delay vs Temperature



TL/F/5826–6

National Semiconductor Corporation

DS7800/DS8800 Dual Voltage Level Translator

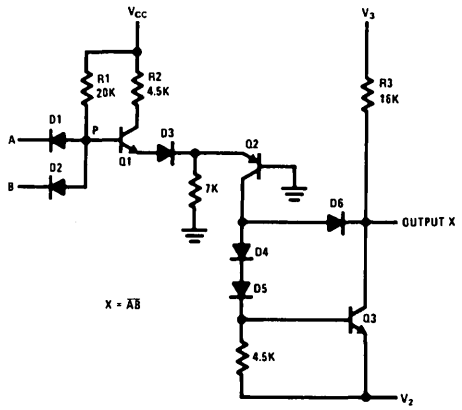
General Description

The DS7800/DS8800 are dual voltage translators designed for interfacing between conventional TTL or LS voltage levels and those levels associated with high impedance junction or MOS REF-type devices. The design allows the user a wide latitude in his selection of power supply voltages, thus providing custom control of the output swing. The translator is especially useful in analog switching; and since low power dissipation occurs in the "off" state, minimum system power is required.

Features

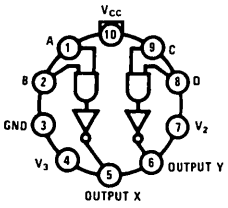
- 31 volt (max) output swing
- 1 mW power dissipation in normal state
- Standard 5V power supply
- Temperature range:
  - DS7800 −55°C to +125°C
  - DS8800 0°C to +70°C
- Compatible with all MOS devices

Schematic and Connection Diagrams



TL/F/5827–1

Metal Can Package

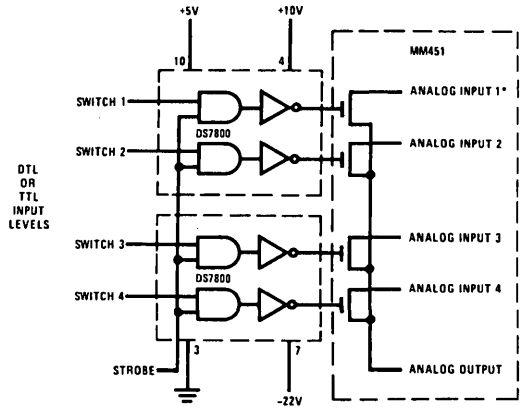


TL/F/5827–2

Top View
Order Number DS7800H or DS8800H
See NS Package Number H10C

Typical Applications

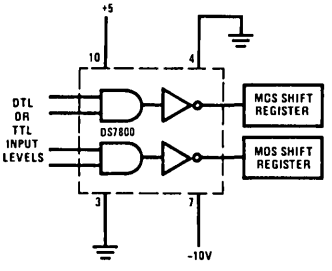
4-Channel Analog Switch



TL/F/5827–3

*Analog signals within the range of +8V to −8V.

Bipolar to MOS Interfacing



TL/F/5827–4

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

V_{CC} Supply Voltage	7.0V
V2 Supply Voltage	−30V
V3 Supply Voltage	30V
V3−V2 Voltage Differential	40V
Input Voltage	5.5V
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 4 seconds)	260°C
Maximum Power Dissipation* at 25°C	
Metal Can (TO-5) Package	690 mW

*Derate metal can package 4.6 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage, V_{CC}			
DS7800	4.5	5.5	V
DS8800	4.75	5.25	V
Temperature (T_A)			
DS7800	−55	+125	°C
DS8800	0	+70	°C

Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions		Min	Typ (Note 6)	Max	Units
V_{IH}	Logical "1" Input Voltage	V_{CC} = Min		2.0			V
V_{IL}	Logical "0" Input Voltage	V_{CC} = Min				0.8	V
I_{IH}	Logical "1" Input Current	V_{CC} = Max	V_{IN} = 2.4V			5	μA
			V_{IN} = 5.5V			1	mA
I_{IL}	Logical "0" Input Current	V_{CC} = Max, V_{IN} = 0.4V			−0.2	−0.4	mA
I_{OL}	Output Sink Current	V_{CC} = Min, V_{IN} = 2V,	DS7800	1.6			mA
		V3 Open	DS8800	2.3			mA
I_{OH}	Output Leakage Voltage	V_{CC} = Max, V_{IN} = 0.8V (Notes 4 and 7)				10	μA
R_O	Output Collector Resistor	T_A = 25°C		11.5	16.0	20.0	kΩ
V_{OL}	Logical "0" Output Voltage	V_{CC} = Min, V_{IN} = 2.0V (Note 7)				V_2 + 2.0	V
$I_{CC(MAX)}$	Power Supply Current Output "ON" Per Gate	V_{CC} = Max, V_{IN} = 4.5V (Note 5)			0.85	1.6	mA
$I_{CC(MIN)}$	Power Supply Current Output "OFF" Per Gate	V_{CC} = Max, V_{IN} = 0V (Note 5)			0.22	0.41	mA

Switching Characteristics T_A = 25°C, nominal power supplies unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd0}	Transition Time to Logical "0" Output	T_A = 25°C, C = 15 pF (Note 8)	25	70	125	ns
t_{pd1}	Transition Time to Logical "1" Output	T_A = 25°C, C = 15 pF (Note 9)	25	62	125	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS7800 and across the 0°C to +70°C range for the DS8800.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Current measured is drawn from V_3 supply.

Note 5: Current measured is drawn from V_{CC} supply.

Note 6: All typical values are measured at T_A = 25°C with V_{CC} = 5.0V, V_2 = −22V, V_3 = +8V.

Note 7: Specification applies for all allowable values of V_2 and V_3.

Note 8: Measured from 1.5V on input to 50% level on output.

Note 9: Measured from 1.5V on input to logic "0" voltage, plus 1V.

Theory of Operation

The two input diodes perform the AND function on TTL input voltage levels. When at least one input voltage is a logical "0", current from V_{CC} (nominally 5.0V) passes through R_1 and out the input(s) which is at the low voltage. Other than small leakage currents, this current drawn from V_{CC} through the 20 kΩ resistor is the only source of power dissipation in the logical "1" output state.

When both inputs are at logical "1" levels, current passes through R_1 and diverts to transistor Q_1, turning it on and thus pulling current through R_2. Current is then supplied to the PNP transistor, Q_2. The voltage losses caused by current through Q_1, D_3, and Q_2 necessitate that node P reach a voltage sufficient to overcome these losses before current begins to flow. To achieve this voltage at node P, the inputs must be raised to a voltage level which is one diode potential lower than node P. Since these levels are exactly the same as those experienced with conventional TTL, the interfacing with these types of circuits is achieved.

Transistor Q_2 provides "constant current switching" to the output due to the common base connection of Q_2. When at least one input is at the logical "0" level, no current is delivered to Q_2; so that its collector supplies essentially zero current to the output stage. But when both inputs are raised to a logical "1" level current is supplied to Q_2.

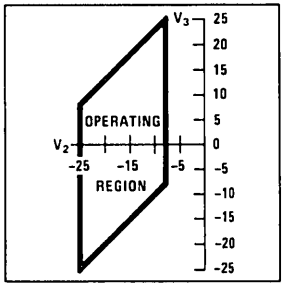
Selecting Power Supply Voltage

The graph shows the boundary conditions which must be used for proper operation of the unit. The range of operation for power supply V_2 is shown on the X axis. It must be between −25V and −8V. The allowable range for power supply V_3 is governed by supply V_2. With a value chosen for V_2, V_3 may be selected as any value along a vertical line passing through the V_2 value and terminated by the boundaries of the operating region. A voltage difference between power supplies of at least 5V should be maintained for adequate signal swing.

Since this current is relatively constant, the collector of Q_2 acts as a constant current source for the output stage. Logic inversion is performed since logical "1" input voltages cause current to be supplied to Q_2 and Q_3. And when Q_3 turns on the output voltage drops to the logical "0" level.

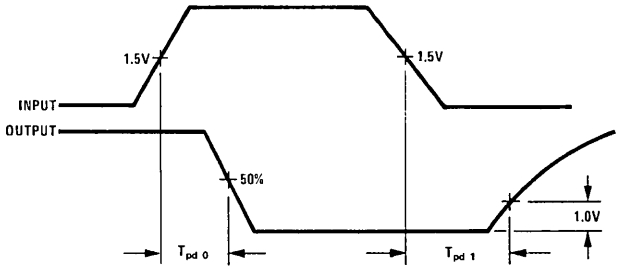
The reason for the PNP current source, Q_2, is so that the output stage can be driven from a high impedance. This allows voltage V_2 to be adjusted in accordance with the application. Negative voltages to −25V can be applied to V_2. Since the output will neither source nor sink large amounts of current, the output voltage range is almost exclusively dependent upon the values selected for V_2 and V_3.

Maximum leakage current through the output transistor Q_3 is specified at 10 μA under worst-case voltage between V_2 and V_3. This will result in a logical "1" output voltage which is 0.2V below V_3. Likewise the clamping action of diodes D_4, D_5, and D_6, prevents the logical "0" output voltage from falling lower than 2V above V_2, thus establishing the ouput voltage swing at typically 2 volts less than the voltage separation between V_2 and V_3.



TL/F/5827–5

Switching Time Waveforms



TL/F/5827–6

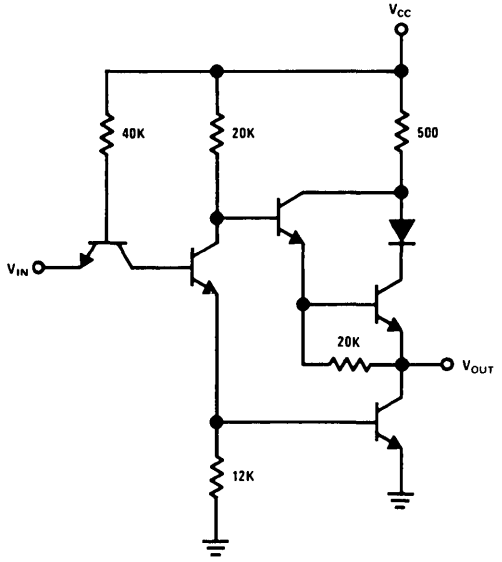
National Semiconductor Corporation

DS78L12/DS88L12 Hex TTL-MOS Inverter/Interface Gate

General Description

The DS78L12/DS88L12 is a low power TTL to MOS hex inverter element. The outputs may be "pulled up" to +14V in the logical "1" state, thus providing guaranteed interface between TTL and MOS logic levels. The gate may also be operated with V_{CC} levels up to +14V without resistive pull-ups at the outputs and still providing a guaranteed logical "1" level of V_{CC} − 2.2V with an output current of −200 μA.

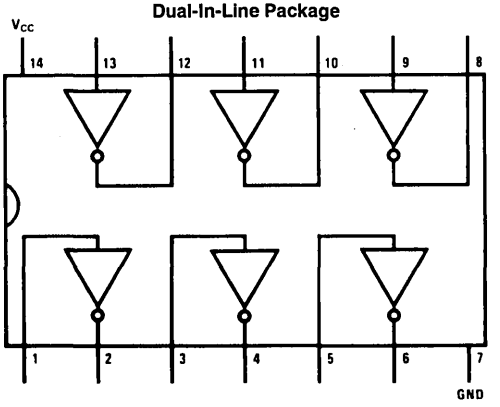
Schematic and Connection Diagrams



Note: Shown is schematic for each inverter.

TL/F/8584-1

Dual-In-Line Package



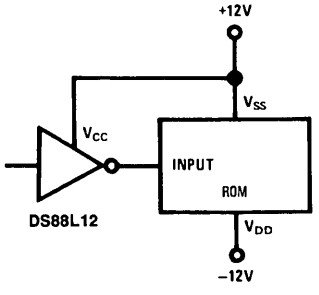
TL/F/8584-2

Top View

Order Number DS78L12J, DS88L12J, DS88L12N and DS78L12W
See NS Package Number J14A, N14A or W14B

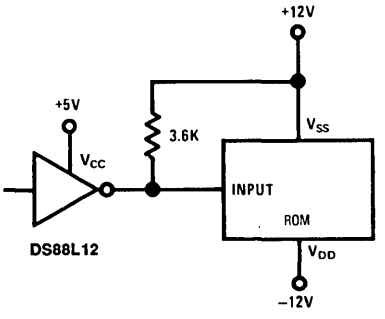
Typical Applications

TTL Interface to MOS ROM without Resistive Pull-Up



TL/F/8584-3

TTL Interface to MOS ROM with Resistive Pull-Up



TL/F/8584-4

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	15V
Input Voltage	5.5V
Output Voltage	15V
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1308 mW
Molded Package	1207 mW
Lead Temperature (Soldering, 4 sec.)	260°C

*Derate cavity package 8.72 mW/°C above 25°C; derate molded package 9.66 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
DS78L12	4.5	5.5	V
DS88L12	4.75	5.25	V
Temperature (T_A)			
DS78L12	−55	125	°C
DS88L12	0	70	°C

Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IH}	Logical "1" Input Voltage	V_{CC} = 14.0V		2.0	1.3		V
		V_{CC} = Min		2.0	1.3		V
V_{IL}	Logical "0" Input Voltage	V_{CC} = 14.0V			1.3	0.7	V
		V_{CC} = Min			1.3	0.7	V
V_{OH}	Logical "1" Output Voltage	V_{IN} = 0.7V	V_{CC} = 14.0V, I_{OUT} = −200 μA	11.8	12.0		V
			V_{CC} = Min, I_{OUT} = −200 μA	14.5	15.0		V
		V_{IN} = 0V, V_{CC} = Min, I_{OUT} = − 5.0 μA (Note 6)					V
V_{OL}	Logical "0" Output Voltage	V_{IN} = 2.0V	V_{CC} = 14.0V, I_{OUT} = 12 mA		0.5	1.0	V
			V_{CC} = Min, I_{OUT} = 3.6 mA		0.2	0.4	V
I_{IH}	Logical "1" Input Current	V_{IN} = 2.4V	V_{CC} = 14.0V		<1	20	μA
			V_{CC} = Max		<1	10	μA
		V_{IN} = 5.5V	V_{CC} = 14.0V		<1	100	μA
			V_{CC} = Max		<1	100	μA
I_{IL}	Logical "0" Input Current	V_{IN} = 0.4V	V_{CC} = 14.0V		−320	−500	μA
			V_{CC} = Max		−100	−180	μA
I_{SC}	Output Short Circuit Current	V_{OUT} = 0V (Note 4)	V_{CC} = 14.0V	−10	−25	−50	mA
			V_{CC} = Max	−3	−8	−15	mA
I_{CCH}	Supply Current—Logical "1" (Each Inverter)	V_{IN} = 0V	V_{CC} = 14.0V		0.32	0.50	mA
			V_{CC} = Max		0.11	0.16	mA
I_{CCL}	Supply Current—Logical "0" (Each Inverter)	V_{IN} = 5.25V	V_{CC} = 14.0V		1.0	1.5	mA
			V_{CC} = Max		0.3	0.5	mA

Switching Characteristics T_A = 25°C, nominal power supplies unless otherwise noted

Symbol	Parameter	Conditions		Min	Typ	Max	Units
t_{pd0}	Propagation Delay to a Logical "0" from Input to Output	T_A = 25°C	V_{CC} = 5.0V *(Figure 2)*		27	45	ns
			V_{CC} = 14.0V *(Figure 1)*		11	20	ns
t_{pd1}	Propagation Delay to a Logical "1" from Input to Output	T_A = 25°C	V_{CC} = 5.0V *(Figure 2)*, (Note 5)		79	100	ns
			V_{CC} = 14.0V *(Figure 1)*		34	55	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS78L12 and across the 0°C to +70°C range for the DS88L12.

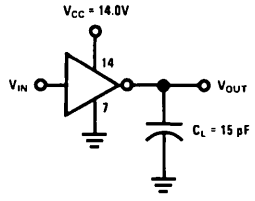
Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Only one output at a time should be shorted.

Note 5: t_{pd1} for V_{CC} = 5.0V is dependent upon the resistance and capacitance used.

Note 6: $V_{OH} = V_{CC} - 1.1V$ for the DS88L12 and $V_{CC} - 1.4V$ for the DS78L12.

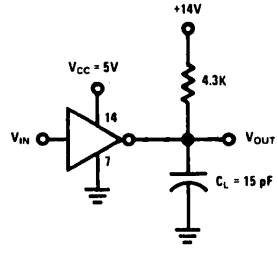
AC Test Circuits



For V_{CC} = 14V

TL/F/8584–5

FIGURE 1

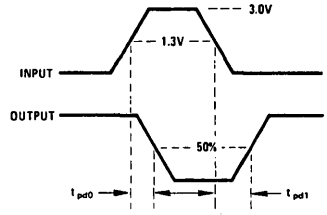


For V_{CC} = 5.0V

TL/F/8584–6

FIGURE 2

Switching Time Waveforms



f = 1 MHz

$t_r = t_f$ = 10 ns

PW = 100 ns

TL/F/8584–7

Section 8

Frequency Synthesis

Section Contents

Frequency Synthesis

Frequency synthesis is the process of generating a multitude of different frequencies from one reference frequency. A common application where the frequency synthesis concept is used is in electronically tuned radios and televisions.

Digital tuning systems are fast replacing the conventional mechanical systems in AM, FM and television receivers. The digital approach encompasses the following operational features:

- Precise tuning of station frequencies
- Exact digital frequency display
- Keyboard entry of desired frequency
- Virtually unlimited station memory
- Up/down scanning through the band
- Station "search" (stop on next active station)
- Power-on to the last station
- Easy option for time-of-day clock

In addition, recent developments in large-scale integrated circuit technology and new varactor diodes for the AM band have made the cost-benefit picture for digital tuning very attractive.

The heart of any digital tuning system is, of course, the phase locked loop (PLL) synthesizer. The basic subcomponents of a digital system are: a voltage controlled oscillator (VCO), a phase comparator and some programmable and fixed dividers. The PLL's basic function is to take two input signals and match them as illustrated in *Figure 1.* The output of the phase comparator of the PLL is an error signal which is filtered and fed back to the VCO as a DC control voltage. The DC control voltage adjusts the VCO until it causes the phase comparator's two inputs to match one another.

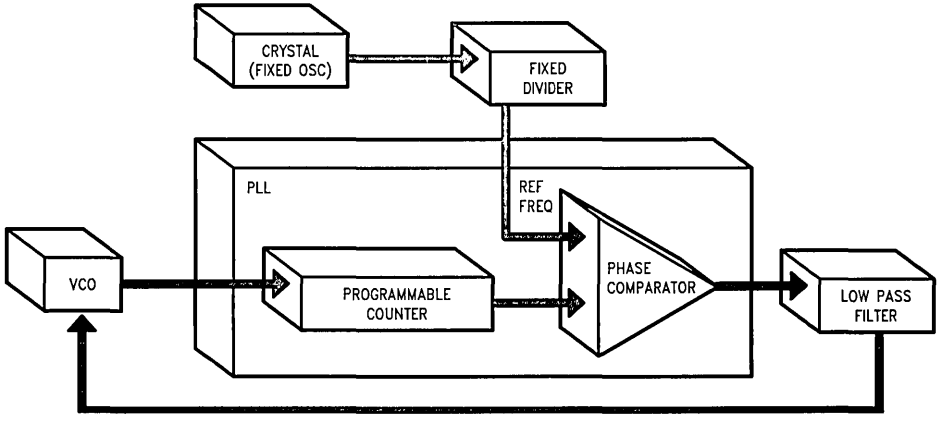
The weak point of this simple illustration is that many PLLs are fabricated using MOS processes which make them relatively incapable of receiving high frequency signals. In fact, state-of-the-art microCMOS devices are usually limited to 100 MHz operation. Even the FM band exceeds this limitation. As a result, a prescaler is almost always used in PLL tuning applications such as FM radios, police scanning radios, aircraft radios, etc. The prescaler is specifically designed to divide high frequency AC input signals down to a usable frequency for the PLL. The prescaler becomes an extension of the PLL's programmable counter as illustrated in *Figure 2.*

For less sophisticated tuning applications, a fixed division prescaler will make the VCO signal palatable to the PLL and be sufficient for general tuning characteristics. However, in some applications, a fixed division prescaler can cause significant undesirable side effects such as:

1. Increased channel spacing (step size) at the output of the PLL's counter; or
2. A forced decrease of the fixed oscillator reference frequency in order to obtain specific channel spacing which can lead to
   A. increased lock-on time,
   B. decreased scanning rates, and
   C. sidebands at undesirable frequencies.

AN-335 in this section explains in detail how these two shortcomings of fixed division prescaling are alleviated by using a dual modulus prescaler. A dual modulus prescaler is substituted for the fixed prescaler and is controlled by programmable counters in the dual modulus PLL, as illustrated by the dotted line in *Figure 2.*

In order to address the requirements of digital frequency synthesis applications, National has introduced a growing family of PLL synthesizers and prescalers. The DS8906, DS8907 and DS8908 are complete PLL synthesizers with features that go beyond those illustrated in *Figure 2.*

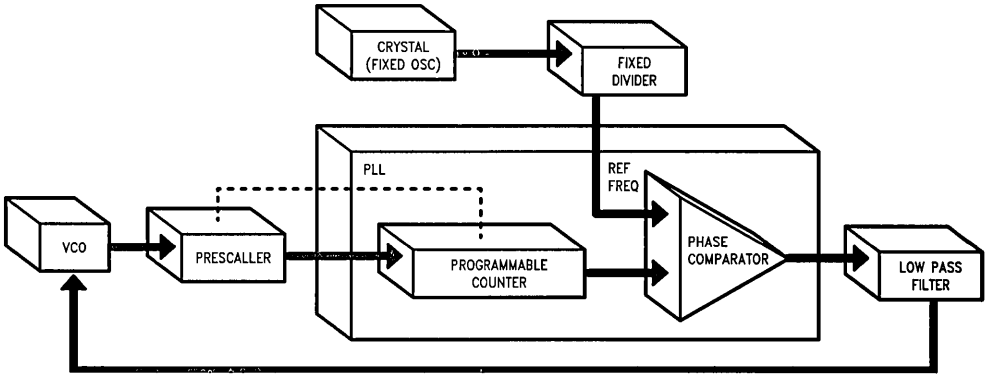


CI18-1

FIGURE 1

Highlights

- The DS8908 integrates a reference oscillator, phase comparator, charge pump, operational amplifier, 120 MHz ECL/I^2L dual modulus programmable divider, and a shift register/latch for serial data entry.
- The DS8614, DS8615, DS8616, DS8617, DS8627, and DS8628 represent a broad family of single and dual modulus prescalers for use in conjunction with other manufacturers' NMOS or CMOS PLLs. These low-power/high-speed prescalers are available with division ratios ranging from a fixed ÷20 up to a dual modulus ÷64/65. This array of products allows for the choice of a division ratio which is virtually tailored to the speed and tuning requirements of a particular frequency synthesis application.



CI18-2

FIGURE 2

Frequency Synthesizers Selection Guide

Product Type	Frequency Bands	Power (mA)	Tuning Resolution	Page No.
PLL FREQUENCY SYNTHESIZERS				
DS8906	AM/FM	160	500 Hz/12.5 kHz	8-23
DS8907	AM/FM	160	10 Hz/25 kHz	8-30
DS8908	AM/FM	160	1 kHz,9 kHz,10 kHz, 20 kHz	8-36
DS8911	AM/FM/VHF TV	35	FM; 10, 12.5, 25, 100 kHz AM; 1, 1.25, 2.5, 10 kHz	8-44
DS8912	AM/FM/VHF TV	35	FM; 10, 12.5, 25, 100 kHz AM; 0.5, 0.625, 1.25, 5 kHz	8-44
AN-335 Digital PLL Synthesis				8-53

Product Type	Divide Modulus	Power (mA)	f_{MAX}	Page No.
HIGH FREQUENCY PRESCALERS				
Single (Fixed) Modulus Dividers				
DS8627	÷24	7/10	130/225 MHz	8-17
DS8628	÷20	7/10	130/225 MHz	8-17
DS8621	÷64, ÷256	32	275 MHz, 1.2 GHZ	8-10
Dual-Modulus Dividers				
DS8614	÷20/21	7/10	130/225 MHz	8-6
DS8615	÷32/33	7/10	130/225 MHz	8-6
DS8616	÷40/41	7/10	130/225 MHz	8-6
DS8617	÷64/65	7/10	130/225 MHz	8-6
DS8622	÷126/128, ÷252/256	32	550 MHz, 1.2 GHz	8-13

National Semiconductor Corporation

DS8614/DS8615/DS8616/DS8617 130/225 MHz Low Power Dual Modulus Prescalers

General Description

The DS8614 series products are low power dual modulus prescalers which divide by 20/21, 32/33, 40/41, and 64/65, respectively. The modulus control (MC) input selects division by N when at a high TTL level and division by N + 1 when at a low TTL level. The clock inputs are buffered, providing 40/100 mVrms input sensitivity. The two outputs provide the user the option to wire either a totem-pole or open-collector output structure. Additionally, the user can wire a resistor between the two output pins to minimize edge transition emissions. The outputs are designed to drive positive edge triggered PLLs. These products can be operated from either an unregulated 5.5V to 13.5V source or regulated 5V ±10% source. Unregulated operation is obtained by connecting V_S to the source with V_{REG} open. Regulated operation is obtained by connecting both V_S and V_{REG} to the supply source.

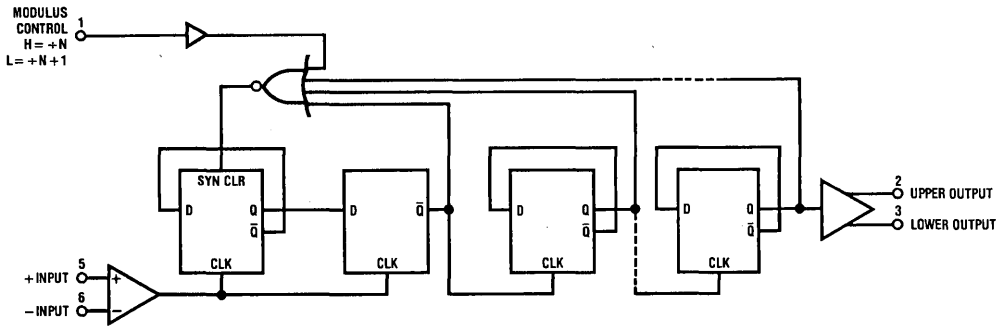
The device can be used in phase-locked loop applications such as FM radio or other communications bands to prescale the input frequency down to a more usable level. A digital frequency display system can also be derived separately or in conjunction with a phase-locked loop, and it can extend the useful range of many inexpensive frequency counters to 225 MHz.

Features

- Input frequency: 130 MHz (-4, -3); 225 MHz (-2, std)
- Low power: 10 mA (-4, -2); 7 mA (-3, std)
- Input sensitivity: 100 mVrms (-4, -3); 40 mVrms (-2, std)
- Pin compatible with Motorola MC12015-17 prescalers
- Unregulated/regulated power supply option

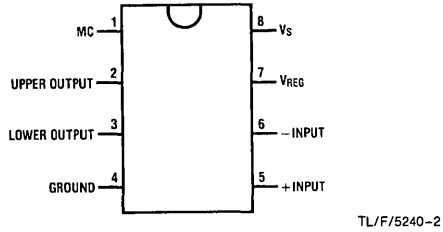
Logic and Connection Diagrams

Generalized ÷ N/N + 1



TL/F/5240–1

Dual-In-Line Package



TL/F/5240–2

Top View

Order Number DS8614N, DS8615N, DS8616N or DS8617N (-4, -3, -2)
See NS Package Number N08E

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

V_S, Unregulated Supply Voltage	15V
V_{REG}, Regulated Supply Voltage	7V
Modulus Control Input Voltage	7V
Open-Collector Output Voltage	7V
Operating Free Air Temperature Range	−30°C to +70°C
Storage Temperature Range	−65°C to +150°C

Recommended Operating Conditions

Symbol	Parameter	Conditions	DS8614-4 DS8615-4 DS8616-4 DS8617-4		DS8614-3 DS8615-3 DS8616-3 DS8617-3		DS8614-2 DS8615-2 DS8616-2 DS8617-2		DS8612 DS8615 DS8616 DS8617		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
V_S	Unregulated Supply Voltage	V_{REG} = Open	6.8	13.5	6.8	13.5	5.5	13.5	5.5	13.5	V
V_{REG}	Regulated Supply Voltage	V_S and V_{REG} Shorted	4.5	5.5	4.5	5.5	4.5	5.5	4.5	5.5	V
f_{MAX}	Toggle Frequency	V_{IN} = 100 mVrms	20	130	20	130		225		225	MHz
V_{IN}	Input Signal Amplitude		100	300	100	300	40	300	40	300	mVrms
V_{SLW}	Slew Rate		20		20		20		20		V/μs
I_{OH}	High Level Output Current			−400		−400		−400		−400	μA
I_{OL}	Low Level Output Current			2.0		2.0		2.0		2.0	mA

DC Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions	DS8614-4 DS8615-4 DS8616-4 DS8617-4		DS8614-3 DS8615-3 DS8616-3 DS8617-3		DS8614-2 DS8615-2 DS8616-2 DS8617-2		DS8612 DS8615 DS8616 DS8617		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High Level MC Input Voltage	V_S = 13.5V, V_{REG} = Open	2.0		2.0		2.0		2.0		V
V_{IL}	Low Level MC Input Voltage	V_{REG} = V_S = 4.5V		0.8		0.8		0.8		0.8	V
V_{OH}	High Level Output Voltage	I_{OH} = −0.4 mA, Pins 2 and 3 Shorted	V_{REG} −2		V_{REG} −2		V_{REG} −2		V_{REG} −2		V
I_{CEX}	Open-Collector High Level Output	Lower Output = 5.5V		100		100		100		100	μA
V_{OL}	Low Level Output Voltage	V_{REG} = 4.5V, I_{OL} = 2 mA		0.5		0.5		0.5		0.5	V
I_I	Max MC Input Current	V_S = 13.5V, V_{REG} = Open, V_{IH} = 7V		100		100		100		100	μA
I_{IH}	High Level MC Input Current	V_{REG} = 4.5V, V_{IH} = 2.7V		20		20		20		20	μA
I_{IL}	Low Level MC Input Current	V_S = 13.5V, V_{REG} = Open, V_{IL} = 0.4V		−200		−100		−200		−100	μA
I_S	Supply Current, Unregulated Mode	V_S = 13.5V, V_{REG} = Open		10		7		10		7	mA
I_{REG}	Supply Current, Regulated Mode	V_S = V_{REG} = 5.5V		10		7		10		7	mA

8

AC Electrical Characteristics V_{CC} = 5V ±10%, T_A = −30°C to +70°C

Symbol	Parameter		Conditions	Min	Max	Units
$t_{MODULUS}$	Modulus Set-Up Time (Notes 4 and 5)	DS8614			55	
		DS8615, DS8616			65	ns
		DS8617			75	
R_{IN}	AC Input Resistance		V_{IN} = 100 MHz and 50 mVrms	1.0		kΩ
C_{IN}	Input Capacitance		V_{IN} = 100 MHz and 50 mVrms	3	10	pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

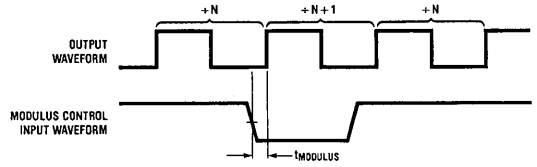
Note 2: Unless otherwise specified min/max limits apply across the −30°C to +70°C temperature range.

Note 3: All currents into device pins are shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: $t_{MODULUS}$ = the period of time the modulus control level must be defined prior to the positive transition of the prescaler output to ensure proper modulus selection.

Note 5: See Timing Diagrams.

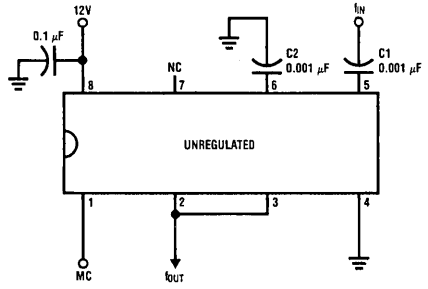
Timing Diagram



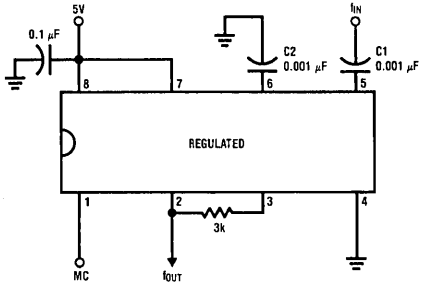
TL/F/5240–3

The logical state of the modulus control input just prior to the output's rising edge will determine the modulus ratio of the device immediately following that rising edge. The pulse width difference of N and N + 1 operation occurs during the output = HI conditions.

Typical Applications

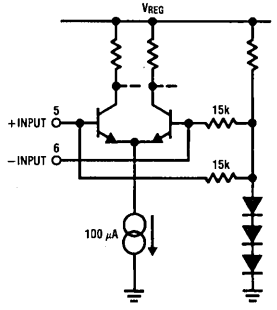


TL/F/5240–4

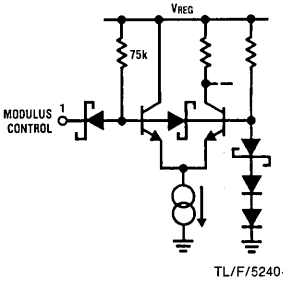


TL/F/5240–5

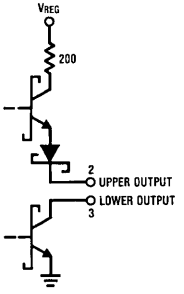
Schematic Diagrams



TL/F/5240–6



TL/F/5240–7



TL/F/5240–8

Application Hints

OPERATING NOTES

The signal source is usually capacitively coupled to the input. At higher frequencies a 0.001 μF input capacitor (C1) is usually sufficient, with larger values used at the lower frequencies. If the input signal is likely to be interrupted, it may be desirable to connect a 100 kΩ resistor between one input and ground to stabilize the device. In the single-ended mode, it is preferable to connect the resistor to the unused input. In the differential mode, the resistor can be connected to either input. The addition of the 100 kΩ pulldown resistor causes a loss of input sensitivity, but prevents circuit oscillations under no signal (open circuit) conditions. In addition, in the single ended mode, a capacitor of 0.001 μF (C2) should be connected between the unused input and the ground plane to provide a good high frequency bypass. The capacitor should be made larger for lower frequencies.

The input waveform may be sinusoidal, but below about 20 MHz the operation of the circuit becomes dependent on the slew rate of the input rather than amplitude. A square wave input with a slew rate of greater than 20 V/μs will permit correct operation down to lower frequencies, provided the proper input coupling capacitor is provided.

For regulated mode operation connect V_S to V_{REG} to ensure proper operation (see Typical Application diagram).

National Semiconductor Corporation

PRELIMINARY

DS8621 275 MHz/1.2 GHz VHF/UHF Prescaler

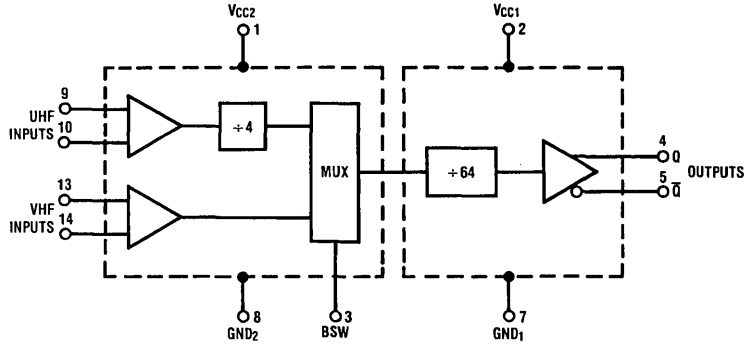
General Description

The DS8621 is a low power, high speed prescaler intended for use in frequency synthesized television tuners. The device performs division by 64 from the VHF input and division by 256 from the UNF input. The VHF and UHF inputs are buffered providing 50 mVrms sensitivity at frequencies in excess of 275 MHz and 1.2 GHz respectively. (The VHF and UHF input signals can be applied either single or double-ended.) The TTL compatible bandswitch (BSW) input selects the VHF inputs when at a low level and the UHF inputs when at a high level. The outputs are complementary ECL structures which have controlled edge-transition rates to minimize spurious harmonic emissions. The device operates from a 5V ±10% supply source. V_{CC2} and GND_2 power the VHF and UHF input stages while V_{CC1} and GND_1 power the remainder of the circuit, thus limiting internal feedback.

Features

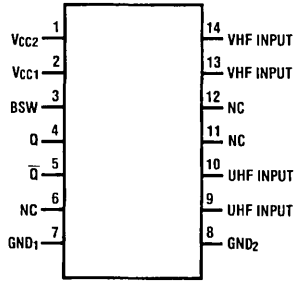
- Broadband operation
- High sensitivity
- Separate VHF and UHF inputs
- Low power
- Pin compatible with RCA (CA3179) and Motorola (MC12071)

Logic and Connection Diagrams



TL/F/7527–1

Dual-In-Line Package



Top View

TL/F/7527–2

Logic Truth Table

BSW	Input Mode	Modulus
0	VHF	64
1	UHF	256

Order Number DS8621N
See NS Package Number N14A

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

V_{CC1}, Supply Voltage 7V

V_{CC2}, Supply Voltage 7V

Input Voltage 7V

Operating Free Air Temperature Range −30°C to +70°C

Storage Temperature Range −65°C to +150°C

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Units
	Supply Voltages				
	V_{CC1}		4.5	5.5	V
	V_{CC2}		4.5	5.5	V
f_{MAX}	Toggle Frequency				
	VHF	V_{IN} = 100 mVrms	80	275	MHz
	UHF		80	1200	MHz
V_{IN}	Input Signal Sensitivity				
	VHF	80 MHz–275 MHz	20	500	mVrms
	UHF	80 MHz–450 MHz	100	500	mVrms
		450 MHz–1200 MHz	50	500	mVrms
	Input Slew Rate				
	VHF		20		V/μs
	UHF		20		V/μs
I_{OH}	High Level Output Current			−300	μA
I_{OL}	Low Level Output Current			300	μA

DC Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions	Min	Max	Units
V_{IH}	High Level BSW Input Voltage	V_{CC} = 5.5V	2.0		V
V_{IL}	Low Level BSW Input Voltage	V_{CC} = 4.5V		0.8	V
I_I	Max High Level BSW Input Current	V_{CC} = 4.5V V_{IH} = 7V		100	μA
I_{IH}	High Level BSW Input Current	V_{CC} = 4.5V V_{IH} = 2.7V		20	μA
I_{IL}	Low Level BSW Input Current	V_{CC} = 5.5V V_{IL} = 0.4V		−100	μA
	Output Voltage Range	Refer to Output Load Diagram	0.75	1.6	Vp-p
I_{CC}	Supply Current	V_{CC} = 5.5V		32.0	mA

AC Electrical Characteristics V_{CC} = 5V ±10%, T_A = −30°C to +70°C

Parameter	Conditions	Min	Max	Units
Output Rise/Fall Time	Refer to Output Load Diagram	40	110	ns

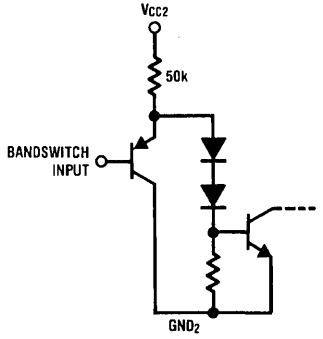
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply acros the −30°C to +70°C temperature range.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltage referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

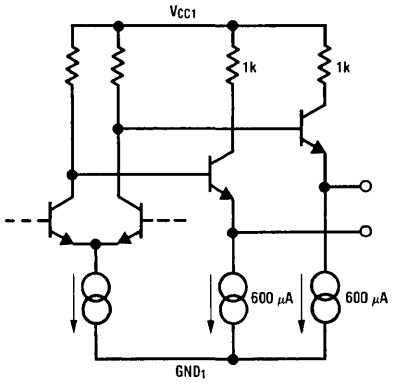
Typical Input/Output Schematics

Bandswitch Buffer



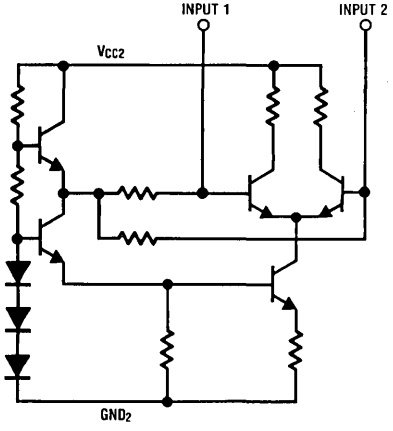
TL/F/7527–3

Output Buffer



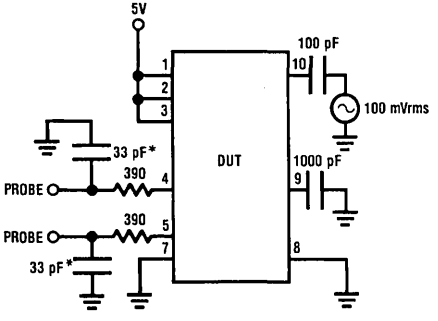
TL/F/7527–4

VHF/UHF Input Buffers



TL/F/7527–5

Output Load Diagram



TL/F/7527–6

*Includes capacitance of probes

National Semiconductor Corporation

DS8622 500 MHz/1.2 GHz Dual Modulus VHF/UHF Prescaler

General Description

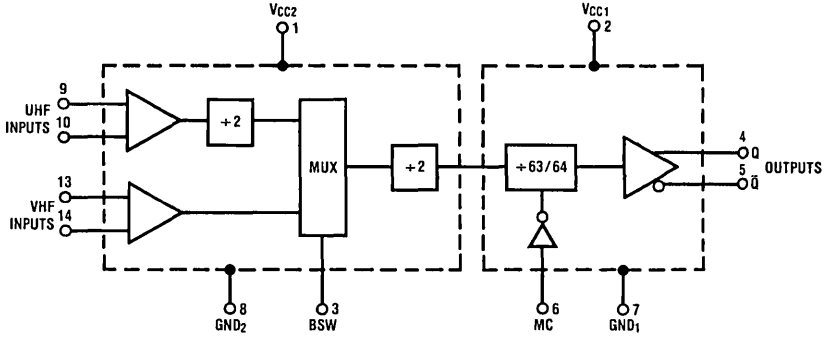
The DS8622 is a low power broadband dual modulus prescaler intended for use in frequency synthesized television tuners. The device features separate VHF and UHF buffered inputs, VHF input division by 126 or 128, UHF input division by 252 or 256, TTL compatible bandswitch and modulus control inputs, complementary ECL outputs, and 5V operation.

The VHF and UHF inputs cover a frequency range from 80 MHz to 1200 MHz and can be driven either single or double-ended. The bandswitch (BSW) input selects the VHF inputs when at a low level and the UHF inputs when at a high level. The modulus control (MC) input selects division by 126 or 252 when at a high level and division by 128 or 256 when at a low level. The dual modulus feature of this prescaler can provide frequency resolution steps of 3.9 kHz, 7.8 kHz, or 15.6 kHz as shown in the table of Possible Operating Conditions. The outputs are internally edge-transition controlled to minimize spurious harmonic emissions. The device operates from a standard 5V ±10% supply source. V_{CC2} and GND_2 power the VHF and UHF input stages, and V_{CC1} and GND_1 power the remainder of the circuit, thus limiting internal feedback.

Features

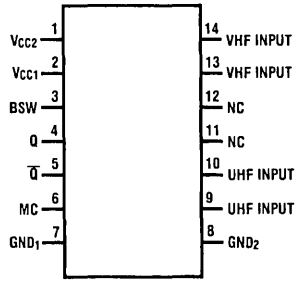
- Broadband operation
- Increased frequency resolution
- High input sensitivity
- Separate VHF and UHF inputs
- Low power

Logic and Connection Diagrams



TL/F/7538–1

Dual-In-Line Package



TL/F/7538–2

Top View

Logic Truth Table

BSW	MC	Input Mode	Modulus
0	0	VHF	128
0	1	VHF	126
1	0	UHF	256
1	1	UHF	252

Order Number DS8622N
See NS Package Number N14A

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

V_{CC1}, Supply Voltage	7V
V_{CC2}, Supply Voltage	7V
BSW, MC Input Voltage	7V
Operating Free Air Temperature Range	−30°C to +70°C
Storage Temperature Range	−65°C to +150°C

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Units
	Supply Voltages				
	V_{CC1}		4.5	5.5	V
	V_{CC2}		4.5	5.5	V
f_{MAX}	Toggle Frequency	V_{IN} = 100 mVrms			
	VHF		80	550	MHz
	UHF		80	1200	MHz
V_{IN}	Input Signal Sensitivity				
	VHF	80 MHz–550 MHz	50	500	mVrms
	UHF	80 MHz–550 MHz	100	500	mVrms
		550 MHz–1200 MHz	50	500	mVrms
	Input Slew Rate				
	VHF		20		V/μs
	UHF		20		V/μs
I_{OH}	High Level Output Current			−300	μA
I_{OL}	Low Level Output Current			300	μA

DC Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions	Min	Max	Units
V_{IH}	High Level Input Voltage (Note 4)	V_{CC} = 5.5V	2.0		V
V_{IL}	Low Level Input Voltage (Note 4)	V_{CC} = 4.5V		0.8	V
I_I	Max Input Current (Note 4)	V_{CC} = 4.5V V_{IH} = 7V		100	μA
I_{IH}	High Level Input Current (Note 4)	V_{CC} = 4.5V V_{IH} = 2.7V		20	μA
I_{IL}	Low Level Input Current (Note 4)	V_{CC} = 5.5V V_{IL} = 0.4V		−100	μA
	Output Voltage Range	Refer to Output Load Diagram	0.75	1.6	Vp-p
I_{CC}	Supply Current			32.0	mA

AC Electrical Characteristics V_{CC} = 5V ±10%, T_A = −30°C to +70°C

Symbol	Parameter	Conditions	Min	Max	Units
$t_{MODULUS}$	Modulus Set-up Time (Note 5)			65	ns
t_{SEL}	BSW Select Time			20	μs
	Output Rise/Fall Time	Refer to Output Load Diagram	40	110	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −30°C to +70°C temperature range.

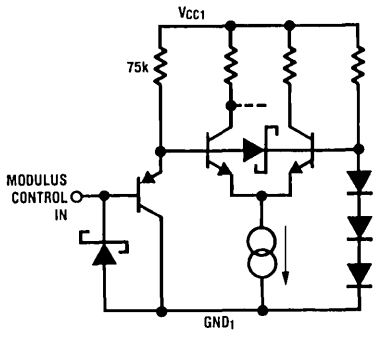
Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Applies to BSW and MC inputs.

Note 5: $t_{MODULUS}$ = the period of time the modulus control level must be defined prior to the positive transition of the prescale output to ensure proper modulus selection.

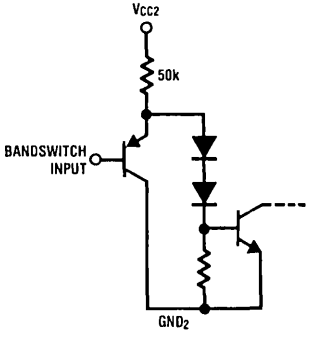
Typical Input/Output Schematics

Modulus Control Buffer



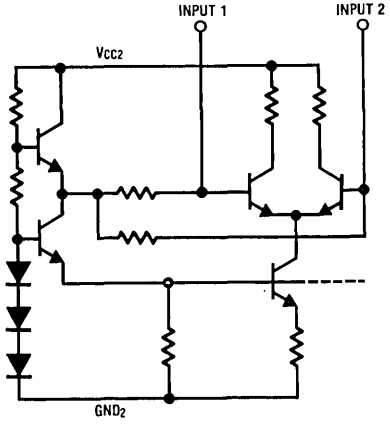
TL/F/7538–3

Bandswitch Buffer



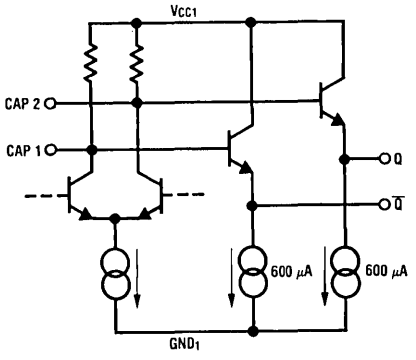
TL/F/7538–4

VHF/UHF Input Buffers



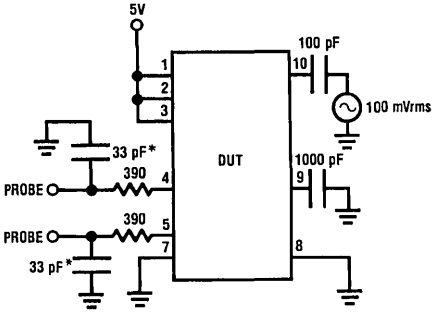
TL/F/7538–5

Output Buffer



TL/F/7538–6

Output Load Diagram



*Includes capacitance of probes.

TL/F/7538–7

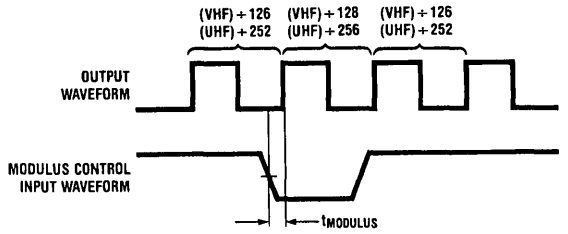
Possible Operating Conditions

Reference Frequency (kHz)	Mode	Frequency Resolution (kHz)	Min Lock Frequency* (MHz)
15.625	VHF	31.25	124.03125
	UHF	62.5	248.0625
7.8125	VHF	15.625	62.015625
	UHF	31.25	124.03125
3.90625	VHF	7.8125	31.0078
	UHF	15.625	62.015625

*Frequencies obtainable using minimum continuous N code.

8

Timing Diagram



TL/F/7538–8

The modulus control input level is sensed immediately prior to the output low-to-high level transition. The prescaler's modulus value will respond to the change in the modulus control input level immediately *after* that same output low-to-high level transition.

National Semiconductor Corporation

DS8627/DS8628 130/225 MHz Low Power Prescalers

General Description

The DS8627 and DS8628 are low power fixed ratio prescalers which divide by 24 and 20, respectively. The inputs can be driven either single or double-ended and they are buffered, providing 40/100 mVrms input sensitivity. The output provided is open-collector and is capable of interfacing with TTL and CMOS.

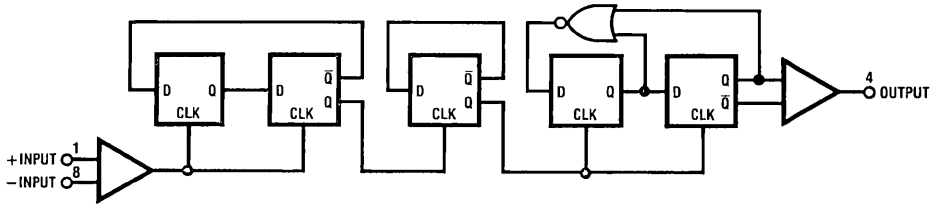
The device can be used in phase-locked loop applications such as FM radio or other communications bands to prescale the input frequency down to a more usable level. A digital frequency display system can also be derived separately or in conjunction with a phase-locked loop, and it can extend the useful range of many inexpensive frequency counters to 225 MHz.

Features

- Input frequency: 130 MHz (-4, -3); 225 mHz (-2, std)
- Low power: 10 mA (-4, -2); 7 mA (-3, std)
- Input sensitivity: 100 mVrms (-4, -3); 40 mVrms (-2, std)

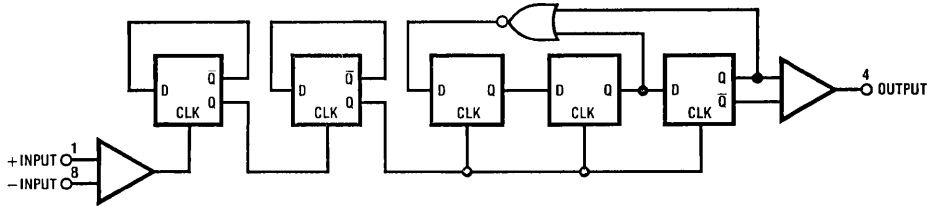
Logic and Connection Diagrams

DS8627 (÷ 24)



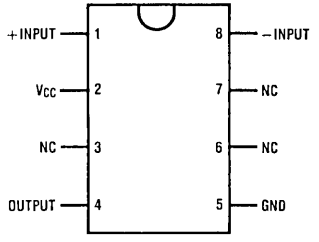
TL/F/5009–1

DS8628 (÷ 20)



TL/F/5009–2

Dual-In-Line Package



TL/F/5009–3

Top View
Order Number DS8627N or DS8628N (-4, -3, -2)
See NS Package Number N08E

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

V_{CC} Supply Voltage 7V

V_{IN} Input Voltage $< V_{CC}$

Open-Collector Output Voltage 7V

Operating Free Air Temperature Range −30°C to +70°C

Storage Temperature Range −65°C to +150°C

Recommended Operating Conditions

Symbol	Parameter	Conditions	DS8627-4 DS8628-4		DS8627-3 DS8628-3		DS8627-2 DS8628-2		DS8627 DS8628		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
V_{CC}	Supply Voltage		4.5	5.5	4.5	5.5	4.5	5.5	4.5	5.5	V
f_{MAX}	Toggle Frequency	V_{IN} = 100 mVrms	20	130	20	130	20	225	20	225	MHz
V_{IN}	Input Signal Amplitude		100	300	100	300	40	300	40	300	mVrms
V_{SLW}	Slew Rate		20		20		20		20		V/μs
I_{OL}	Low Level Output Current			3		3				3	mA

DC Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions	DS8627-4 DS8628-4		DS8627-3 DS8628-3		DS8627-2 DS8628-2		DS8627 DS8628		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
I_{CEX}	Open-Collector High Level Output	Output = 5.5V		100		100		100		100	μA
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, I_{OL} = 3 mA		0.4		0.4		0.4		0.4	V
I_{CC}	Supply Current	V_{CC} = 5.5V		10		7		10		7	mA

AC Electrical Characteristics V_{CC} = 5V ±10%, T_A = −30°C to +70°C

Symbol	Parameter	Conditions	Min	Max	Units
R_{IN}	AC Input Resistance	V_{IN} = 100 MHz and 50 mVrms	1.0		kΩ
C_{IN}	Input Capacitance		3	10	pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −30°C to +70°C temperature range.

Note 3: All currents into device pins are shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

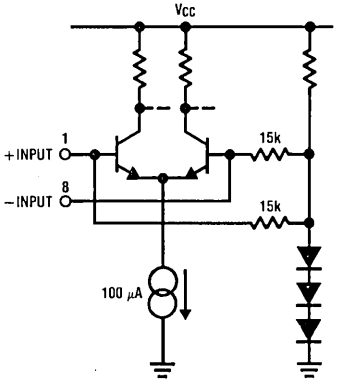
Application Hints

OPERATING NOTES

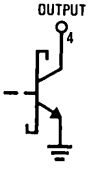
The signal source is usually capacitively coupled to the input. At higher frequencies a 0.001 μF input capacitor is usually sufficient, with larger values used at the lower frequencies. If the input signal is likely to be interrupted, it may be desirable to connect a 100 kΩ resistor between one input and ground to stabilize the device. In the single-ended mode, it is preferable to connect the resistor to the unused input. In the differential mode, the resistor can be connected to either input. The addition of the 100 kΩ pull-down resistor causes a loss of input sensitivity, but prevents circuit oscillations under no signal (open circuit) conditions. In addition, in the single ended mode, a capacitor of 0.001 μF should be connected between the unused input and the ground plane to provide a good high frequency bypass. The capacitor should be made larger for lower frequencies.

The input waveform may be sinusoidal, but below about 20 MHz the operation of the circuit becomes dependent on the slew rate of the input rather than amplitude. A square wave input with a slew rate of greater than 20 V/μs will permit correct operation down to lower frequencies, provided the proper input coupling capacitor is provided.

Schematic Diagrams

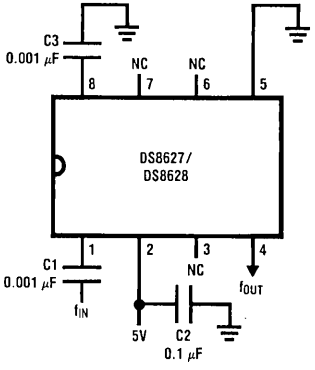


TL/F/5009–4



TL/F/5009–5

Typical Application



TL/F/5009–6

8

National Semiconductor Corporation

DS8629 120 MHz Divide-by-100 Prescaler

General Description

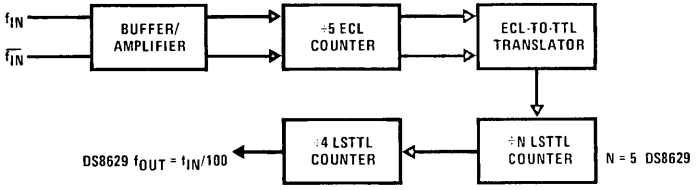
The DS8629 is a fixed ratio counter combining ECL and Low Power Schottky technology on a single monolithic substrate. This provides high frequency capability and TTL compatibility. A single 5.2V ±10% supply is needed.

The device can be operated in a single-ended or differential input mode, with the signal source typically capacitively coupled to the input. An input amplifier is included to allow use of extremely small amplitude, high frequency signals. The output of the device is a square wave of frequency $f_{OUT} = f_{IN}/100$ for the DS8629. The output is standard Low Power Schottky.

Features

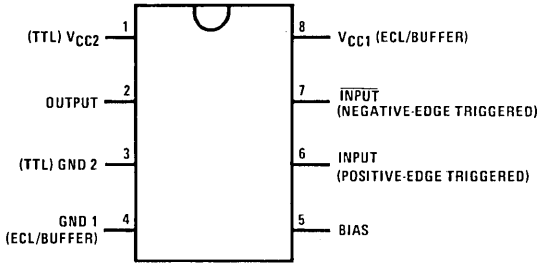
- High Frequency, dc—120 MHz—small input amplitude
- Sine wave input 30 MHz < f_{IN} < 120 MHz
- TTL compatible output
- May be used with TTL input
- Single supply operation 5.2V ±10%
- Single ended or differential input modes
- Positive or negative-edge triggered
- Count down sequence avoids broadcast FM IF harmonics

Logic and Connection Diagrams



TL/F/7539–1

Dual-In-Line Package

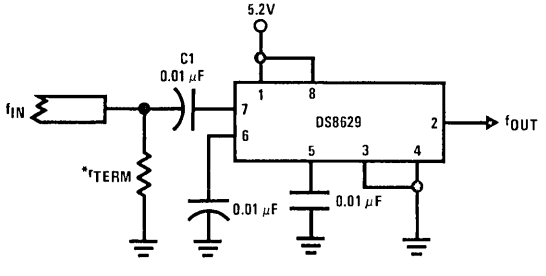


TL/F/7539–2

Order Number DS8629N
See NS Package Number N08E

Typical Applications

High Frequency—Single-Ended Input



TL/F/7539–3

*r_{TERM} is the termination impedance

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5V
Output Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	300°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.68	5.72	V
Temperature (T_A)	0	+70	°C

Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
$V_{IN1(p-p)}$	Input Voltage (Peak-To-Peak)	Single-Ended @ 120 MHz		200		1000	mV
$V_{IN2(p-p)}$	Input Voltage (Peak-To-Peak)	Differential @ 120 MHz		100		1000	mV
f_{SINE}	Input Frequency with Sine Wave	V_{IN} = 600 mVp-p		30		120	MHz
f_{TTL}	Input Frequency with TTL Input			0		120	MHz
dv	Minimum Slew Rate of Square Wave Input	V_{IN} = 600 mVp-p				100	V/μs
V_{OH}	Logical "1" Output Voltage	V_{CC} = Min, I_{OH} = −10 μA V_{CC} = Min, I_{OH} = −400 μA V_{CC} = Min, I_{OH} = −1.6 mA		2.9 2.4 2.0			V V V
I_{OS}	Output Short-Circuit Current	V_{CC} = Max		−10		−40	mA
V_{OL}	Logical "0" Output Voltage	V_{CC} = Min	I_{OL} = 8 mA DS8629			0.5	V
I_{CC}	Supply Current	V_{CC} = Max	DS8629		90	135	mA
Z_{IN}	Input Impedance	V_{IN} = 0.1 V_{p-p} to 1 V_{p-p} Freq. = 120 MHz		100	200	350	Ω

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified, min/max limits apply across the 0°C to 70°C range. All typical values are for T_A = 25°C and V_{CC} = 5.2V.

Note 3: All currents into device pins shown as positive, out of device pins negative, all voltage referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Application Hints

OPERATING NOTES

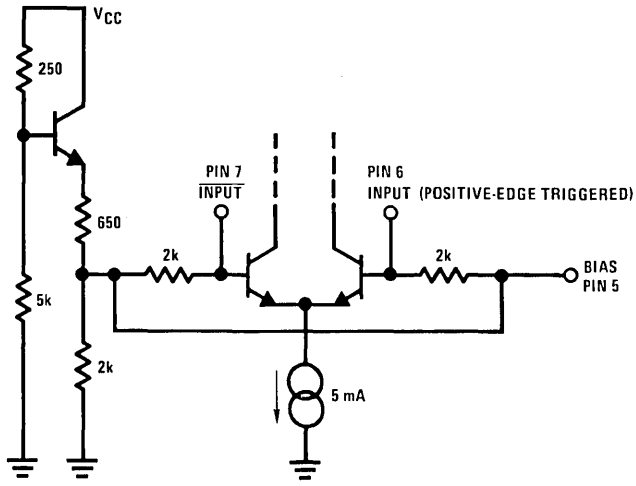
Two ground and two V_{CC} connections are provided separating the ECL and buffer/amplifier stages from the TTL section, isolating the noise transients inherent in the TTL structure. In most cases, shorting the two grounds externally to a good ground plane and the V_{CC}'s to a wide V_{CC} bus will provide sufficient isolation. All components used in the circuit layout should be suitable for the frequencies involved and leads should be kept short to minimize stray inductance. A well by-passed voltage source should be used.

The signal source is usually capacitively coupled to the input. At higher frequencies a 0.01 μF input capacitor (C1) is usually sufficient, with larger values used at the lower frequencies. If the input signal is likely to be interrupted, it may be desirable to connect a 100 kΩ resistor between one input and ground to stabilize the device. In the single-ended mode, it is preferable to connect the resistor to the unused input. In the differential mode, the resistor can be connected to either input. The addition of the 100 kΩ pull-down resistor causes a loss of input sensitivity, but prevents circuit oscillations under no signal (open circuit) conditions. In addition, in the single ended mode, a capacitor of 0.01 μF (C2) should be connected between the unused input and the ground plane to provide a good high frequency bypass. The capacitor should be made larger for lower frequencies.

The input waveform may be sinusoidal, but below about 30 MHz the operation of the circuit becomes dependent on the slew rate of the input rather than amplitude. A square wave input with a slew rate of greater than 100 V/μs will permit correct operation down to lower frequencies, provided the proper input coupling capacitor is provided. If it is desired to use a TTL input signal source, the unused input should have a 10 kΩ resistor added to ground and the input coupling capacitor should be eliminated with the TTL source dc coupled to the input.

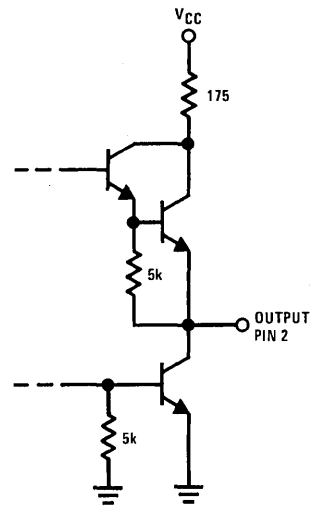
The device can be used in phase-locked loop applications such as FM radio or other communications bands to prescale the input frequency down to a more usable level. A digital frequency display system can also be derived separately or in conjunction with a phase-locked loop, and it can extend the useful range of many inexpensive frequency counters to 160 MHz (typically).

Input Configuration



TL/F/7539-4

Output Configuration



TL/F/7539-5

National Semiconductor Corporation

DS8906 AM/FM Digital Phase-Locked Loop Synthesizer

General Description

The DS8906 is a PLL synthesizer designed specifically for use in AM/FM radios. It contains the reference oscillator, a phase comparator, a charge pump, a 120 MHz ECL/I^2L dual modulus programmable divider, and a 20-bit shift register/latch for serial data entry. The device is designed to operate with a serial data controller generating the necessary division codes for each frequency, and logic state information for radio function inputs/outputs.

The Colpitts reference oscillator for the PLL operates at 4 MHz. A chain of dividers is used to generate a 500 kHz clock signal for the external controller. Additional dividers generate a 12.5 kHz reference signal for FM and a 500 Hz reference signal for AM/SW. One of these reference signals is selected by the data from the controller for use by the phase comparator. Additional dividers are used to generate a 50 Hz timing signal used by the controller for "time-of-day".

Data is transferred between the frequency synthesizer and the controller via a 3 wire bus system. This consists of a data input line, an enable line and a clock line. When the enable line is low, data can be shifted from the controller into the frequency synthesizer. When the enable line is transitioned from low to high, data entry is disabled and data present in the shift register is latched.

From the controller 22-bit data stream, the first 2 bits address the device permitting other devices to share the same bus. Of the remaining 20-bit data word, the next 14-bits are used for the PLL divide code. The remaining 6 bits are connected via latches to output pins. These 6 bits can be used to drive radio functions such as gain, mute, FM, AM, LW and SW only. These outputs are open collector. Bit 18 is used internally to select the AM or FM local oscillator input and to select between the 500 Hz and 12.5 kHz reference. A high level at bit 18 indicates FM and a low level indicates AM.

The PLL consists of a 14-bit programmable I^2L divider, an ECL phase comparator, an ECL dual modulus (p/p + 1) prescaler, and a high speed charge pump. The programmable divider divides by (N+1), N being the number loaded into the shift register (bits 1–14 after address). It is clocked by the AM input via an ECL ÷ 7/8 prescaler, or through a ÷ 63/64 prescaler from the FM input. The AM input will work at frequencies up to 8 MHz, while the FM input works up to 120 MHz. The AM band is tuned with a frequency resolution of 500 Hz and the FM band is tuned with a resolution of 12.5 kHz. The buffered AM and FM inputs are self-biased and can be driven directly by the VCO thru a capacitor. The ECL phase comparator produces very accurate resolution of the phase difference between the input signal and the reference oscillator.

The high speed charge pump consists of a switchable constant current source (−0.3 mA) and a switchable constant current sink (+0.3 mA). If the VCO frequency is low, the charge pump will source current, and sink current if the VCO frequency is high.

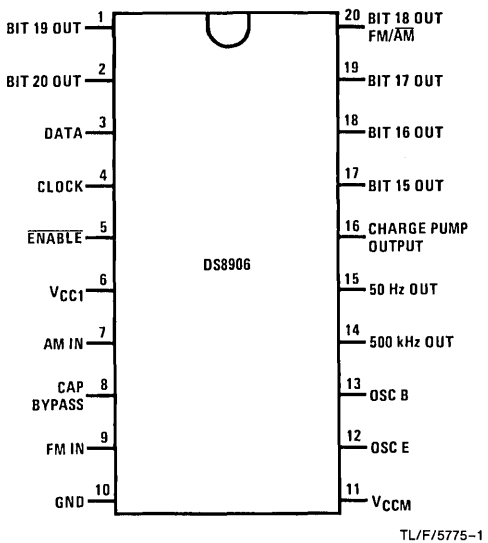
A separate V_{CCM} pin (typically drawing 1.5 mA) powers the oscillator and reference chain to provide controller clocking frequencies when the balance of the PLL is powered down.

Features

- Uses inexpensive 4 MHz reference crystal
- F_{IN} capability greater than 120 MHz allows direct synthesis at FM frequencies
- FM resolution of 12.5 kHz allows usage of 10.7 MHz ceramic filter distribution
- Serial data entry for simplified control
- 50 Hz output for "time-of-day" reference with separate low power supply (V_{CCM})
- 6-open collector buffered outputs for band switching and other radio functions
- Separate AM and FM inputs. AM input has 15 mV (typical) hysteresis

Connection Diagram

Dual-In-Line Package



TL/F/5775–1

Top View

Order Number DS8906N
See NS Package Number N20A

8

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage (V_{CC1})	7V
(V_{CCM})	7V
Input Voltage	7V
Output Voltage	7V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 4 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage, V_{CC}			
V_{CC1}	4.75	5.25	V
V_{CCM}	4.5	6.0	V
Temperature, T_A	0	70	°C

DC Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IH}	Logical "1" Input Voltage			2.1			V
I_{IH}	Logical "1" Input Current	$V_{IN} = V_{CC1}$			0	10	μA
V_{IL}	Logical "0" Input Voltage					0.7	V
I_{IL}	Logical "0" Input Current	Data, Clock and $\overline{\text{ENABLE}}$ INPUTS, $V_{IN} = 0V$			−5	−25	μA
I_{OH}	Logical "1" Output Current All Bit Outputs, 50 Hz Output	$V_{OH} = 5.25V$				50	μA
	500 kHz Output	$V_{OH} = 2.4V$, $V_{CCM} = 4.5V$				−250	μA
V_{OL}	Logical "0" Output Voltage All Bit Outputs	$I_{OL} = 5$ mA				0.5	V
	50 Hz Output, 500 kHz Output	$I_{OL} = 250$ μA				−0.5	V
I_{CC1}	Supply Current (V_{CC1})	All Bit Outputs High			90	160	mA
$I_{CCM(STANDBY)}$	V_{CCM} Supply Current	$V_{CCM} = 6.0V$, All Other Pins Open			1.5	4.0	mA
I_{OUT}	Charge Pump Output Current	$1.2V \le V_{OUT} \le V_{CCM} - 1.2V$, $V_{CCM} \le 6.0V$	Pump Up	−0.10	−0.30	−0.6	mA
			Pump Down	0.10	0.30	0.6	mA
			TRI-STATE®		0	±100	nA
$I_{CCM(OPERATE)}$	V_{CCM} Supply Current	$V_{CCM} = 6.0V$, $V_{CC1} = 5.25V$, All Other Pins Open			2.5	6.0	mA

AC Electrical Characteristics $V_{CC} = 5V$, $T_A = 25°C$, $t_r \le 10$ ns, $t_f \le 10$ ns

Symbol	Parameter	Conditions		Min	Typ	Max	Units
$V_{IN(MIN)(F)}$	F_{IN} Minimum Signal Input	AM and FM Inputs, $0°C \le T_A \le 70°C$			20	100	mV (rms)
$V_{IN(MAX)(F)}$	F_{IN} Maximum Signal Input	AM and FM Inputs, $0°C \le T_A \le 70°C$		1000	1500		mV (rms)
$F_{OPERATE}$	Operating Frequency Range (Sine Wave Input)	V_{IN} = 100 mV rms, $0°C \le T_A \le 70°C$	AM	0.4		8	MHz
			FM	60		120	MHz
R_{IN} (FM)	AC Input Resistance, FM	120 MHz, V_{IN} = 100 mV rms		300			Ω
R_{IN} (AM)	AC Input Resistance, AM	2 MHz, V_{IN} = 100 mV rms		1000			Ω
C_{IN}	Input Capacitance, FM and AM	V_{IN} = 120 MHz		3	6	10	pF
$t_{\overline{EN}1}$	Minimum $\overline{\text{ENABLE}}$ High Pulse Width				625	1250	ns
$t_{\overline{EN}0}$	Minimum $\overline{\text{ENABLE}}$ Low Pulse Width				375	750	ns
$t_{CLK\overline{EN}0}$	Minimum Time before ENABLE Goes Low that CLOCK must be Low				−50	0	ns
$t_{\overline{EN}0CLK}$	Minimum Time after ENABLE Goes Low that CLOCK must Remain Low				275	550	ns
$t_{CLK\overline{EN}1}$	Minimum Time before $\overline{\text{ENABLE}}$ Goes High that Last Positive CLOCK Edge May Occur				300	600	ns

AC Electrical Characteristics V_{CC} = 5V, T_A = 25°C, $t_r \leq 10$ ns, $t_f \leq 10$ ns (Continued)

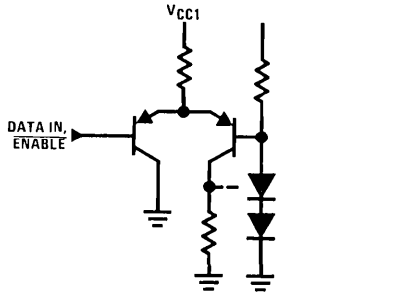
Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{EN1CLK}	Minimum Time After ENABLE Goes High Before an Unused Positive CLOCK Edge May Occur			175	350	ns
t_{CLKH}	Minimum CLOCK High Pulse Width			275	550	ns
t_{CLKL}	Minimum CLOCK Low Pulse Width			400	800	ns
t_{DS}	Minimum DATA Setup Time, Minimum Time Before CLOCK that DATA Must be Valid			150	300	ns
t_{DH}	Minimum DATA Hold Time, Minimum Time After CLOCK that DATA Must Remain Valid			400	800	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

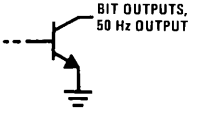
Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C temperature range for the DS8906.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Schematic Diagrams (DS8906 AM/FM PLL Typical Input/Output Schematics)



TL/F/5775–2



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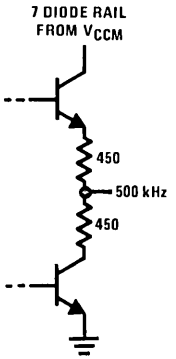

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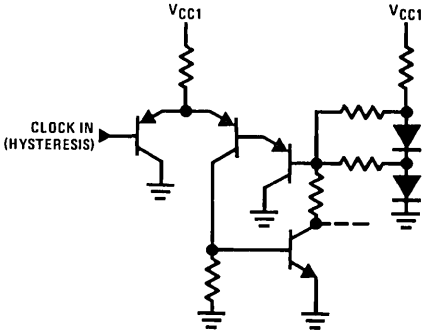
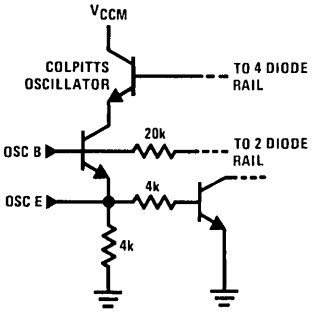
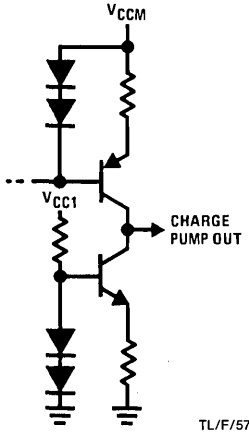


TL/F/5775–5



TL/F/5775–6

Schematic Diagrams (DS8906 AM/FM PLL Typical Input/Output Schematics) (Continued)



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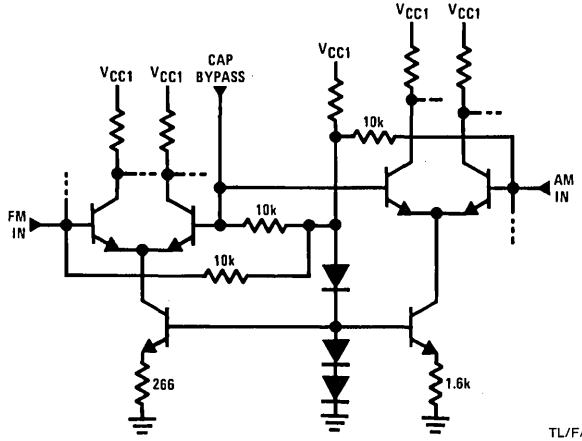
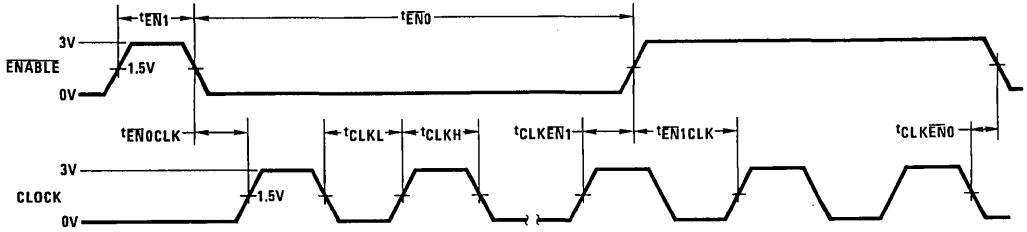


TL/F/5775–8

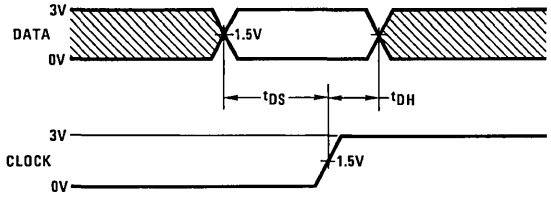
Timing Diagrams*

$\overline{\text{ENABLE}}$ vs CLOCK



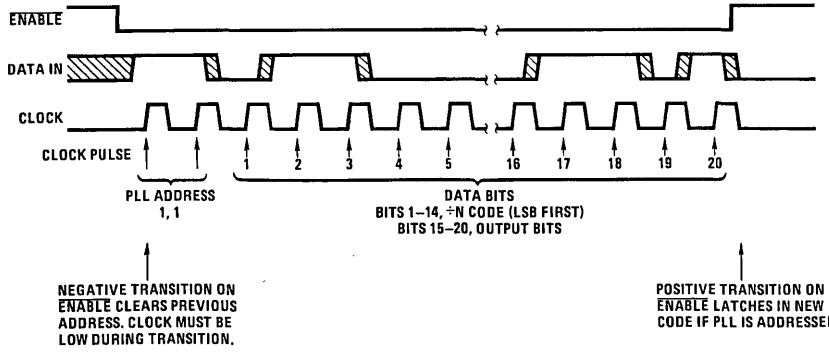
TL/F/5775–9

CLOCK vs DATA



TL/F/5775–10

AM/FM Frequency Synthesizer (Scan Mode)



*Timing diagrams are not drawn to scale. Scale within any one drawing may not be consistent, and intervals are defined positive as drawn.

TL/F/5775–11

Applications Information

SERIAL DATA ENTRY INTO THE DS8906

Serial information entry into the DS8906 is enabled by a low level on the $\overline{\text{ENABLE}}$ input. One binary bit is then accepted from the DATA input with each positive transition of the CLOCK input. The CLOCK input must be low for the specified time preceding and following the negative transition of the $\overline{\text{ENABLE}}$ input.

The first 2 bits accepted following the negative transition of the $\overline{\text{ENABLE}}$ input are interpreted as address. If these address bits are *not* 1,1, *no* further information will be accepted from the DATA inputs, and the internal data latches *will not* be changed when $\overline{\text{ENABLE}}$ returns high.

If these first 2 bits *are* 1,1, then all succeeding bits are *accepted* as data, and are shifted successively into the internal shift register as long as $\overline{\text{ENABLE}}$ remains low.

Any *data* bits preceding the 20th to last bit will be shifted out, and are thus irrelevant. Data bits are counted as any bits following 2 valid (1,1) address bits with the $\overline{\text{ENABLE}}$ low.

When the $\overline{\text{ENABLE}}$ input returns high, any further serial data input is inhibited. Upon this positive transition of the $\overline{\text{ENABLE}}$, the data in the internal shift register is transferred into the internal data latches.

Note that until this time, the states of the internal data latches have remained unchanged.

These data bits are interpreted as follows:

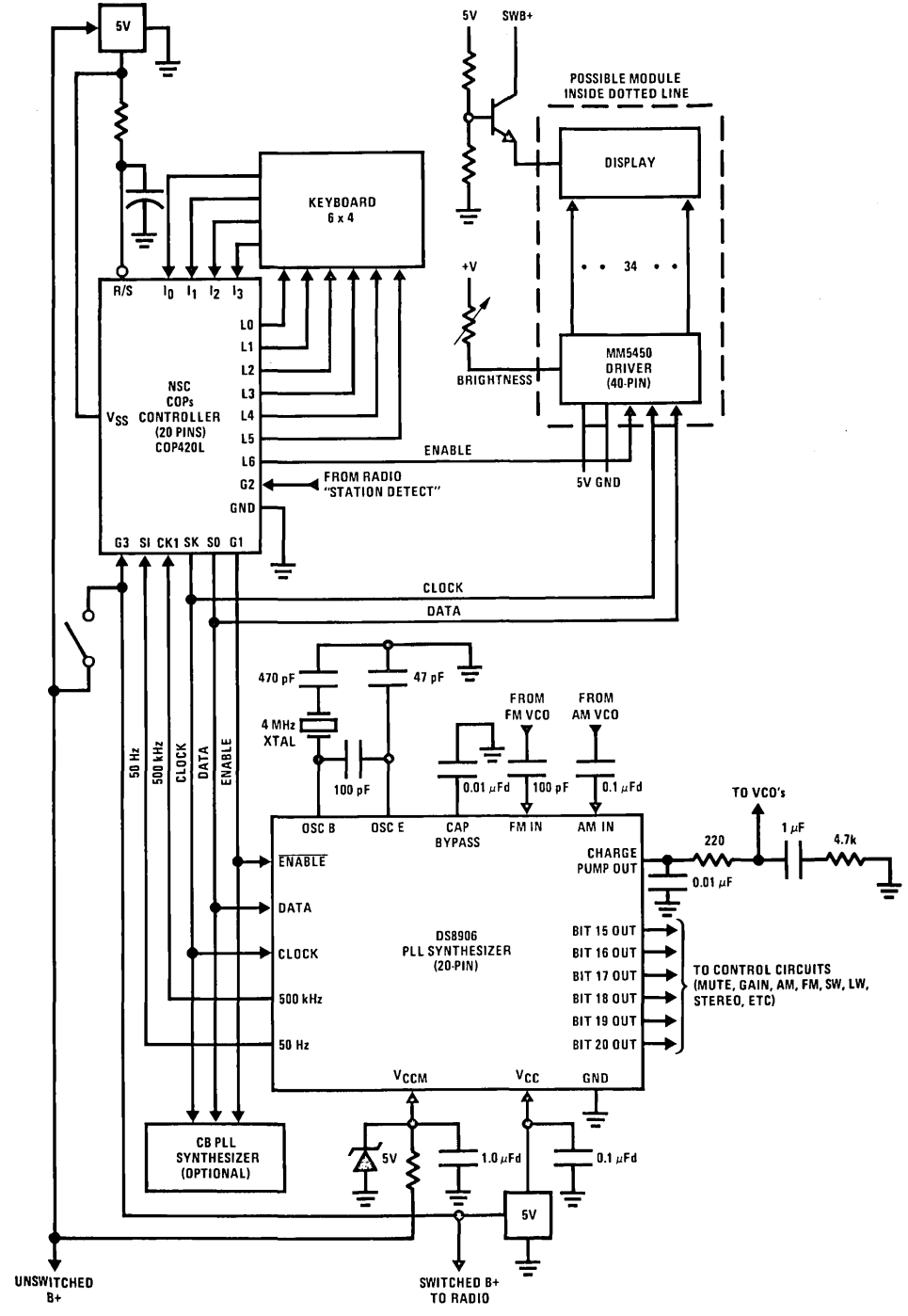
DATA BIT POSITION	DATA INTERPRETATION	
Last	Bit 20 Output (Pin 2)	
2nd to Last	Bit 19 Output (Pin 1)	
3rd to Last	Bit 18 Output (FM/$\overline{\text{AM}}$) (Pin 20)	
4th to Last	Bit 17 Output (Pin 19)	
5th to Last	Bit 16 Output (Pin 18)	
6th to Last	Bit 15 Output (Pin 17)	
7th to Last	MSB of N	(2^{13})
8th to Last		(2^{12})
9th to Last		(2^{11})
10th to Last		(2^{10})
11th to Last		(2^{9})
12th to Last		(2^{8})
13th to Last		(2^{7})
14th to Last		(2^{6})
15th to Last		(2^{5})
16th to Last		(2^{4})
17th to Last		(2^{3})
18th to Last		(2^{2})
19th to Last		(2^{1})
20th to Last	LSB of N	(2^{0})

$\div N$

Note. The actual divide code is N+1, i.e., the number loaded plus 1.

Typical Application

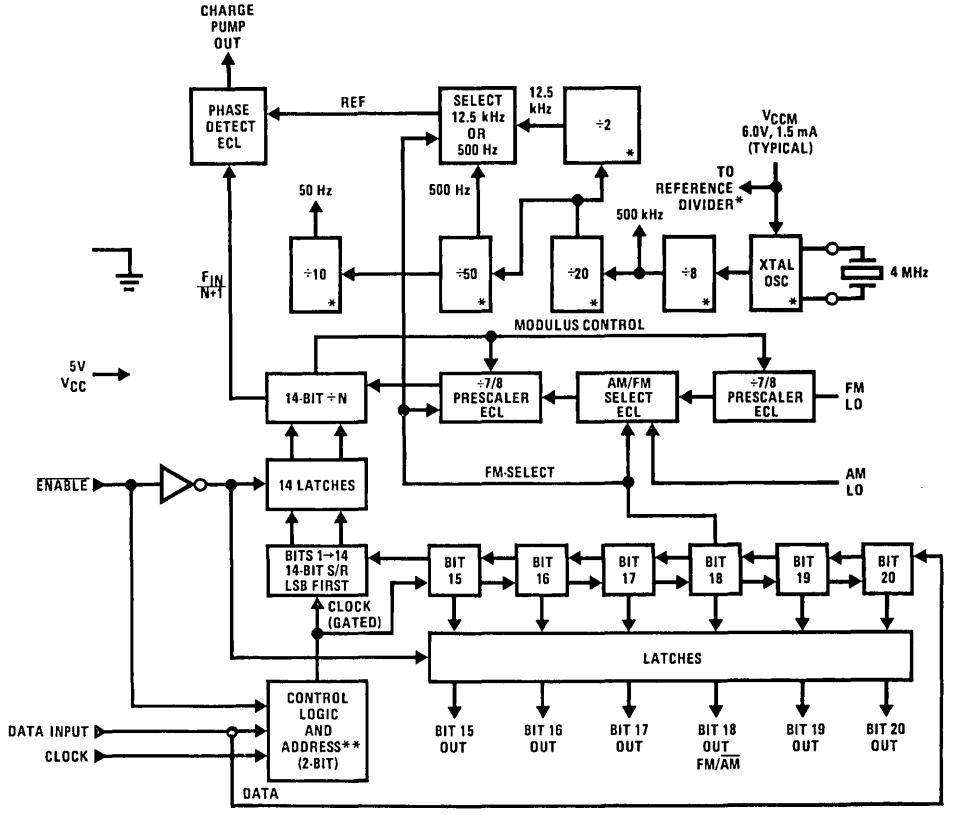
Electronically Tuned Radio Controller System; Direct Drive LED



TL/F/5775–12

Logic Diagram

AM/FM PLL Synthesizer



TL/F/5775–13

*Sections operating from V_{CCM} supply

**Address (1, 1)

8

National Semiconductor Corporation

DS8907 AM/FM Digital Phase-Locked Loop Frequency Synthesizer

General Description

The DS8907 is a PLL synthesizer designed specifically for use in AM/FM radios. It contains the reference oscillator, a phase comparator, a charge pump, a 120 MHz ECL/I^2L dual modulus programmable divider, and an 18-bit shift register/latch for serial data entry. The device is designed to operate with a serial data controller generating the necessary division codes for each frequency, and logic state information for radio function inputs/outputs.

The Colpitts reference oscillator for the PLL operates at 4 MHz. A chain of dividers is used to generate a 500 kHz clock signal for the external controller. Additional dividers generate a 25 kHz reference signal for FM and a 10 kHz reference signal for AM. One of these reference signals is selected by the data from the controller for use by the phase comparator.

Data is transferred between the frequency synthesizer and the controller via a 3 wire bus system. This consists of a data input line, an enable line, and a clock line. When the enable line is low, data can be shifted from the controller into the frequency synthesizer. When the enable line is transitioned from low to high, data entry is disabled and data present in the shift register is latched.

From the controller 20-bit data stream, the first 2 bits address the device permitting other devices to share the same bus. Of the remaining 18-bit data word, the next 13 bits are used for the PLL divide code. The remaining 5 bits are connected via latches to output pins. These 5 bits can be used to drive radio functions such as gain, mute, FM, AM and stereo only. These outputs are open collector. Bit 16 is used internally to select the AM or FM local oscillator input and to select between the 10 kHz and 25 kHz reference. A high level at bit 16 indicates FM and a low level indicates AM.

The PLL consists of a 13-bit programmable I^2L divider, an ECL phase comparator, an ECL dual modulus (p/p+1) prescaler, and a high speed charge pump. The programmable divider divides by (N+1), N being the number loaded into the shift register (bits 1–13 after address). It is clocked by the AM input via an ECL $\div 7/8$ prescaler, or through a $\div 63/64$ prescaler from the FM input. The AM input will work at frequencies up to 15 MHz, while the FM input works up to 120 MHz. The AM band is tuned with a frequency resolution of 10 kHz and the FM band is tuned with a resolution of 25 kHz. The buffered AM and FM inputs are self biased and can be driven directly by the VCO through a capacitor. The ECL phase comparator produces very accurate resolution of the phase difference between the input signal and the reference oscillator. The high speed charge pump consists of a switchable constant current source (−0.3 mA) and a switchable constant current sink (+0.3 mA). If the VCO frequency is low, the charge pump will source current, and sink current if the VCO frequency is high. When using an AFC the charge pump output may be forced into TRI-STATE® by applying a low level to the charge pump enable input.

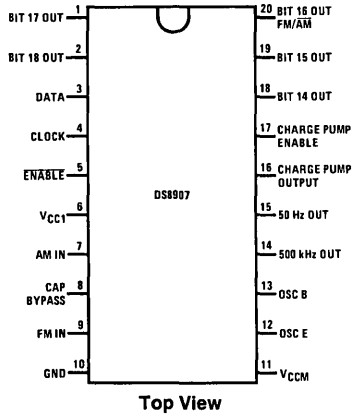
A separate V_{CCM} pin (typically drawing 1.5 mA) powers the oscillator and reference chain to provide controller clocking frequencies when the balance of the PLL is powered down.

Features

- Uses inexpensive 4 MHz reference crystal
- F_{IN} capability greater than 120 MHz allows direct synthesis at FM frequencies
- FM resolution of 25 kHz allows usage of 10.7 MHz ceramic filter distribution
- Serial data entry for simplified control
- 50 Hz output for "time-of-day" reference driven from separate low power V_{CCM}
- 5-open collector buffered outputs for controlling various radio functions
- Separate AM and FM inputs. AM input has 15 mV (typical) hysteresis

Connection Diagram

Dual-In-Line Package



Top View

TL/F/7511–1

Order Number DS8907N
See NS Package Number N20A

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	
(V_{CC1})	7V
(V_{CCM})	7V
Input Voltage	7V
Output Voltage	7V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 4 sec.)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage, V_{CC}			
V_{CC1}	4.75	5.25	V
V_{CCM}	4.5	6.0	V
Temperature, T_A	0	70	°C

DC Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IH}	Logical "1" Input Voltage			2.1			V
I_{IH}	Logical "1" Input Current	V_{IN} = 2.7V			0	10	μA
V_{IL}	Logical "0" Input Voltage					0.7	V
I_{IL}	Logical "0" Input Current	Data, Clock, and $\overline{\text{ENABLE}}$ Inputs, V_{IN} = 0V			−5	−25	μA
I_{IL}	Logical "0" Input Current	Charge Pump Enable, V_{IN} = 0V			−250	−450	μA
I_{OH}	Logical "1" Output Current All Bit Outputs, 50 Hz Output	V_{OH} = 5.25V				50	μA
	500 kHz Output	V_{OH} = 2.4V, V_{CCM} = 4.5V				−250	μA
V_{OL}	Logical "0" Output Voltage All Bit Outputs	I_{OL} = 5 mA				0.5	V
	50 Hz Output, 500 Hz Output	I_{OL} = 250 μA				0.5	V
I_{CC1}	Supply Current (V_{CC1})	All Bits Outputs High			90	160	mA
$I_{CCM(STANDBY)}$	V_{CCM} Supply Current	V_{CCM} = 6.0V, All Other Pins Open			1.5	4.0	mA
I_{OUT}	Charge Pump Ougtput Current	1.2V ≤ V_{OUT} ≤ V_{CCM} −1.2V	Pump Up	−0.10	−0.30	−0.6	mA
		V_{CCM} ≤ 6.0V	Pump Down	0.10	0.30	0.6	mA
			TRI-STATE		0	±100	nA
$I_{CCM(OPERATE)}$	V_{CCM} Supply Current	V_{CCM} = 6.0V, V_{CC1} = 5.25V, All Other Pins Open			2.5	6.0	mA

AC Electrical Characteristics V_{CC} = 5V, T_A = 25°C, t_r ≤ 10 ns, t_f ≤ 10 ns

Symbol	Parameter	Conditions		Min	Typ	Max	Units
$V_{IN(MIN)(F)}$	F_{IN} Minimum Signal Input	AM and FM Inputs, 0°C ≤ T_A ≤ 70°C			20	100	mV (rms)
$V_{IN(MAX)(F)}$	F_{IN} Maximum Signal Input	AM and FM Inputs, 0°C ≤ T_A ≤ 70°C		1000	1500		mV (rms)
$F_{OPERATE}$	Operating Frequency Range (Sine Wave Input)	V_{IN} = 100 mV rms 0°C ≤ T_A ≤ 70°C	AM	0.4		8	MHz
			FM	60		120	MHz
$R_{IN(FM)}$	AC Input Resistance, FM	120 MHz, V_{IN} = 100 mV rms		300			Ω
$R_{IN(AM)}$	AC Input Resistance, AM	2 MHz, V_{IN} = 100 mV rms		1000			Ω
C_{IN}	Input Capacitance, FM and AM	V_{IN} = 120 MHz		3	6	10	pF
$t_{\overline{EN}1}$	Minimum $\overline{\text{ENABLE}}$ High Pulse Width				625	1250	ns
$t_{\overline{EN}0}$	Minimum $\overline{\text{ENABLE}}$ Low Pulse Width				375	750	ns
$t_{CLK\overline{EN}0}$	Minimum Time Before ENABLE Goes Low That CLOCK Must Be Low				−50	0	ns
$t_{\overline{EN}0CLK}$	Minimum Time After ENABLE Goes Low That CLOCK Must Remain Low				275	550	ns
$t_{CLK\overline{EN}1}$	Minimum Time Before $\overline{\text{ENABLE}}$ Goes High That Last Positive CLOCK Edge May Occur				300	600	ns

AC Electrical Characteristics V_{CC} = 5V, T_A = 25°C, $t_r \leq 10$ ns, $t_f \leq 10$ ns (Continued)

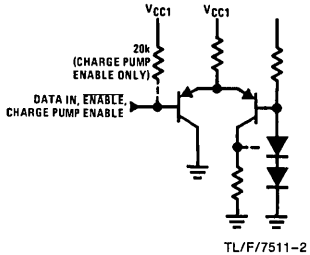
Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{EN1CLK}	Minimum Time After ENABLE Goes High Before an Unused Positive CLOCK Edge May Occur			175	350	ns
t_{CLKH}	Minimum CLOCK High Pulse Width			275	550	ns
t_{CLKL}	Minimum CLOCK Low Pulse Width			400	800	ns
t_{DS}	Minimum DATA Setup Time, Minimum Time before CLOCK That DATA Must Be Valid			150	300	ns
t_{DH}	Minimum DATA Hold Time, Minimum Time after CLOCK That DATA Must Remain Valid			400	800	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −40°C to +85°C temperature range for the DS8907.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Schematic Diagrams (DS8907 AM/FM PLL typical Input/Output Schematics)



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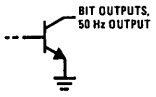

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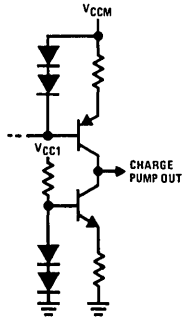

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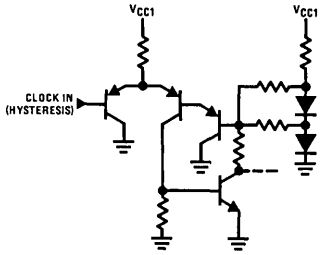

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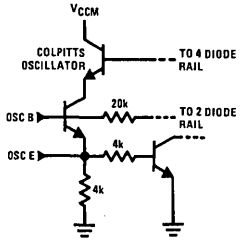

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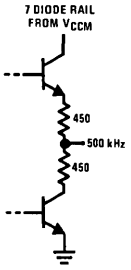

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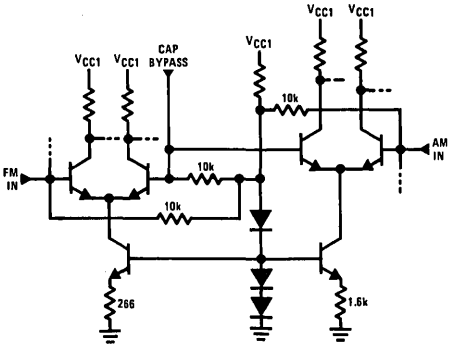

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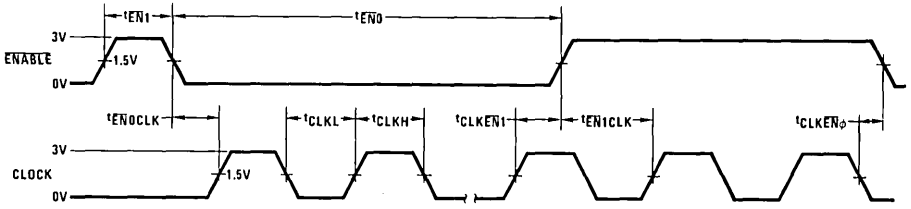
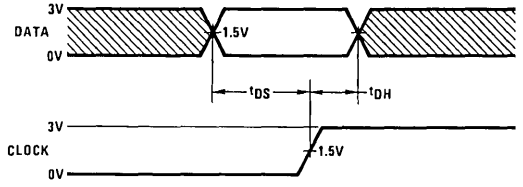
Timing Diagrams*

ENABLE vs CLOCK



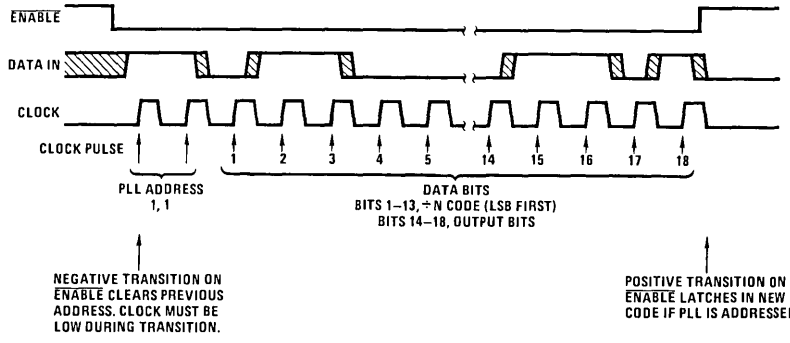
TL/F/7511-9

CLOCK vs DATA



TL/F/7511-10

AM/FM Frequency Synthesizer (Scan Mode)



TL/F/7511-11

*Timing diagrams are not drawn to scale. Scale within any one drawing may not be consistent, and intervals are defined positive as drawn.

SERIAL DATA ENTRY INTO THE DS8907

Serial information entry into the DS8907 is enabled by a low level on the $\overline{\text{ENABLE}}$ input. One binary bit is then accepted from the DATA input with each positive transition of the CLOCK input. The CLOCK input must be low for the specified time preceding and following the negative transition of the $\overline{\text{ENABLE}}$ input.

The first two bits accepted following the negative transition of the $\overline{\text{ENABLE}}$ input are interpreted as address. If these address bits are *not* 1,1 *no* further information will be accepted from the DATA inputs, and the internal data latches *will not* be changed when $\overline{\text{ENABLE}}$ returns high.

If these first two bits *are* 1,1, then all succeeding bits are *accepted* as data, and are shifted successively into the internal shift register as long as $\overline{\text{ENABLE}}$ remains low.

Any data bits preceding the 18th to last bit will be shifted out, and thus are irrelevant. Data bits are counted as any bits *following* two valid address bits (1,1) with the $\overline{\text{ENABLE}}$ low. When the $\overline{\text{ENABLE}}$ input returns high, any further serial data entry is inhibited. Upon this positive transition, the data in the internal shift register is transferred into the internal data latches. Note that until this time, the states of the internal data latches have remained unchanged.

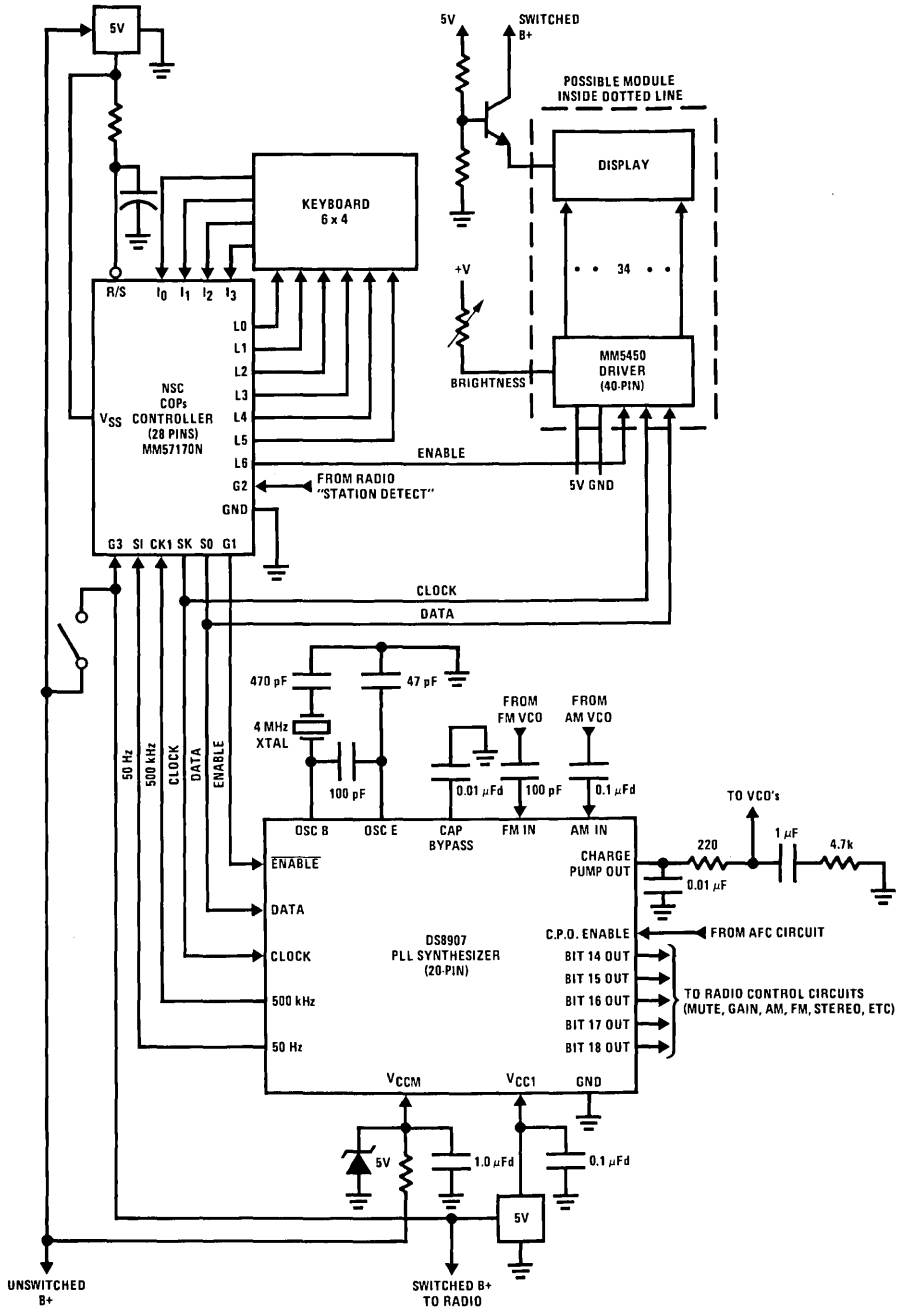
These data bits are interpreted as follows:

Data Bit Position	Data Interpretation
Last	Bit 18 Output (Pin 2)
2nd to Last	Bit 17 Output (Pin 1)
3rd to Last	Bit 16 Output (FM/$\overline{\text{AM}}$) (Pin 20)
4th to Last	Bit 15 Output (Pin 19)
5th to Last	Bit 14 Output (Pin 18)
6th to Last	MSB of ÷N (2^{12})
7th to Last	(2^{11})
8th to Last	(2^{10})
9th to Last	(2^{9})
10th to Last	(2^{8})
11th to Last	(2^{7})
12th to Last	(2^{6}) ÷N
13th to Last	(2^{5})
14th to Last	(2^{4})
15th to Last	(2^{3})
16th to Last	(2^{2})
17th to Last	(2^{1})
18th to Last	LSB of ÷N (2^{0})

Note: The actual divide code is N+1, i.e., the number loaded plus 1.

Typical Application

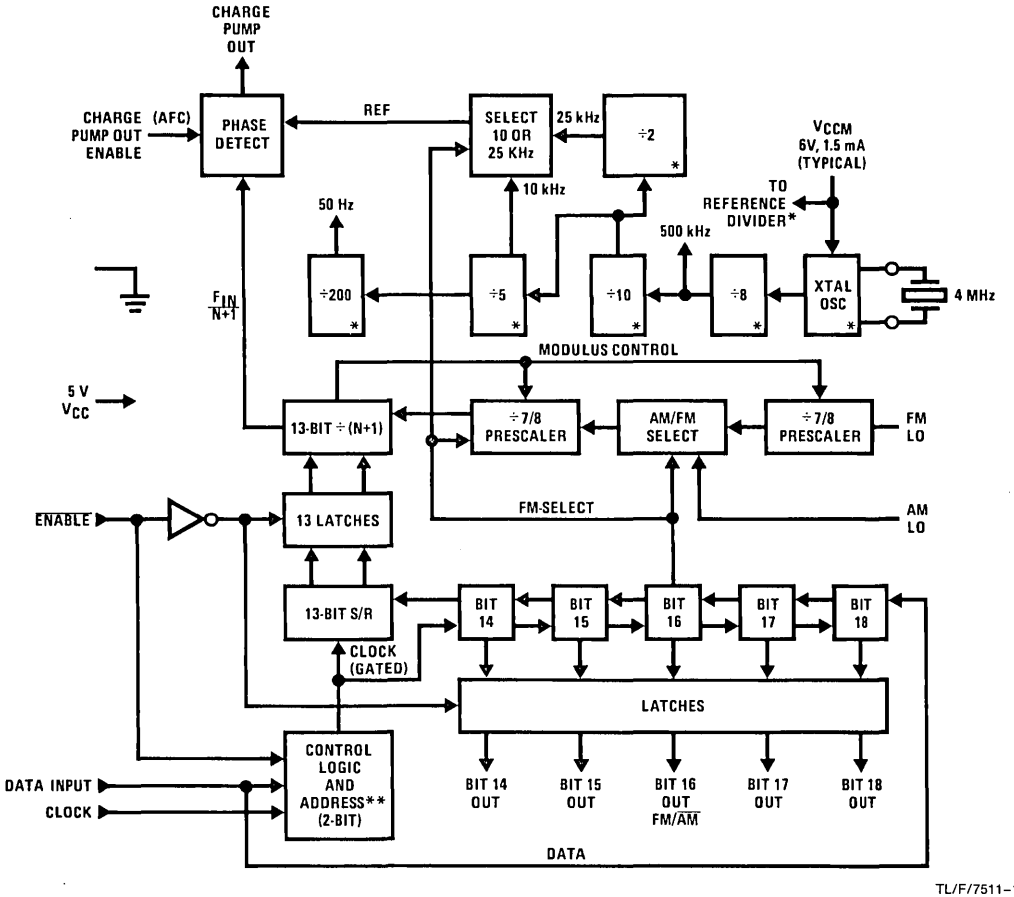
Electronically Tuned Radio Controller System; Direct Drive LED



TL/F/7511–12

Logic Diagram

AM/FM PLL/Synthesizer (Serial Data 20-Pin Package)



TL/F/7511–13

*Sections operating from V_{CCM} supply.

**Address (1, 1)

National Semiconductor Corporation

DS8908 AM/FM Digital Phase-Locked Loop Frequency Synthesizer

General Description

The DS8908 is a PLL synthesizer designed specifically for use in AM/FM radios. It contains the reference oscillator, a phase comparator, a charge pump, an operational amplifier, a 120 MHz ECL/I^2L dual modulus programmable divider, and a 19-bit shift register/latch for serial data entry. The device is designed to operate with a serial data controller generating the necesary division codes for each frequency, and logic state information for radio function inputs/outputs.

A 3.96 MHz pierce oscillator and divider chain generate a 1.98 MHz external controller clock, a 20 kHz, 10 kHz, 9 kHz, and a 1 kHz reference signals, and a 50 Hz time-of-day signal. The oscillator and divider chain are sourced by the V_{CCM} pin thus providing a low power controller clock drive and time-of-day indication when the balance of the PLL is powered down.

The 21-bit serial data steram is transferred between the frequency synthesizer and the controller via a 3-wire bus system comprised of a data line, a clock line, and an enable line.

The first 2 bits in the serial data stream address the synthesizer thus permitting other devices such as display drivers to share the same bus. The next 14 bits are used for the PLL(N+1) divide code. The 15th bit is used internally to select the AM or FM local oscillator input. A high level on this bit enables the FM input and a low level enables the AM input. The 16th and 17th bits are used to select one of the 4 reference frequencies. The 18th and 19th bits are connected via latches to open collector outputs. These outputs can be used to drive radio functions such as gain, mute, AM, FM, or charge pump current source levels.

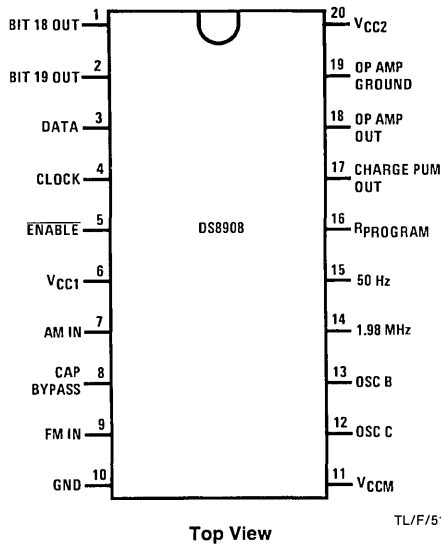
The PLL consists of a 14-bit programmable I^2L divider, an ECL phase comparator, an ECL dual modulus (p/p + 1) prescaler, a high speed charge pump, and an operational amplifier. The programmable divider divides by (N+1), N being the number loaded into the shift register. The programmable divider is clocked through a $\div 7/8$ prescaler by the AM input or through a $\div 63/64$ prescaler by the FM input. The AM input will work at frequencies up to 15 MHz, while the FM input works up to 120 MHz. The VCO can be tuned with a frequency resolution of either 1 kHz, 9 kHz, 10 kHz, or 20 kHz. The buffered AM and FM inputs are self-biased and can be driven directly by the VCO through a capacitor. The ECL phase comparator produces very accurate resolution of the phase difference between the input signal and the reference oscillator. The high speed charge pump consists of a switchable constant current source and sink. The charge pump can be programmed to deliver from 75 μA to 750 μA of constant current by connection of an external resistor from pin $R_{PROGRAM}$ to ground or the open collector bit outputs. Connection of programming resistors to the bit outputs enables the controller to adjust the loop gain for the particular reference frequency selected. The charge pump will source current if the VCO frequency is high and sink current if the VCO frequency is low. The low noise operational amplifier provided has a high impedance JFET input and a large output voltage range. The op amp's negative input is common with the charge pump output and its positive input is internally biased.

Features

- Uses inexpensive 3.96 MHz reference crystal
- F_{IN} capability greater than 120 MHz allows direct synthesis at FM frequencies
- FM resolution of either 10 kHz or 20 kHz allows usage of 10.7 MHz ceramic filter distribution
- Serial data entry for simplified control
- 50 Hz output for time-of-day reference driven from separate low power V_{CCM}
- 2 open collector buffered outputs for controlling various radio functions or loop gain
- Separate AM and FM inputs; AM input has 15 mV (typical) hysteresis
- Programmable charge pump current sources enable adjustment of system loop gain
- Operational amplifier provides high impedance load to charge pump output and a wide voltage range for the VCO input

Connection Diagram

Dual-In-Line Package



TL/F/5111-1

Top View
Order Number DS8908N
See NS Package Number N20A

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	
(V_{CC1}) (V_{CCM})	7V
(V_{CC2})	17V
Input Voltage	7V
Output Voltage	7V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 4 seconds)	260°C

Operating Conditions

	Min	Max	Units
V_{CC1}	4.5	5.5	V
V_{CC2}	V_{CC1} + 1.5	15.0	V
V_{CCM}	3.5	5.5	V
Temperature, T_A	−40	+85	°C

DC Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IH}	Logical "1" Input Voltage			2.0			V
I_{IH}	Logical "1" Input Current	V_{IN} = 2.7V			0	10	μA
V_{IL}	Logical "0" Input Voltage					0.8	V
I_{IL}	Logical "0" Input Current	Data, Clock, and $\overline{\text{ENABLE}}$ Inputs, V_{IN} = 0V			−5	−25	μA
I_{OH}	Logical "1" Output Current All Bit Outputs, 50 Hz Output	V_{OH} = 5.5V				50	μA
	1.98 MHz Output	V_{OH} = 2.4V, V_{CCM} = 4.5V				−250	μA
V_{OL}	Logical "0" Output Voltage All Bit Outputs	I_{OL} = 5 mA				0.5	V
	50 Hz Output, 1.98 MHz Output	I_{OL} = 250 μA				0.5	V
	1.98 MHz Output	I_{OL} = 20 μA, T_A > 70°C I_{OL} = 20 μA, T_A ≤ 70°C				0.3 0.4	V V
I_{CC1}	Supply Current (V_{CC1})	All Bit Outputs High				160	mA
I_{CCM}	V_{CCM} Supply Current	V_{CCM} = 5.5V, All Other Pins Open			2.5	4.0	mA
I_{OUT}	Charge Pump Ougtput Current	3.33k ≤ R_{PROG} ≤ 33.3k I_{OUT} Measured between Pin 17 and Pin 18 I_{PROG} = V_{CC1}/2 R_{PROG}	Pump Up	−20	I_{PROG}	+20	%
			Pump Down	−20	I_{PROG}	+20	%
			TRI-STATE®		0	11	nA
I_{CC2}	V_{CC2} Supply Current	V_{CCM} = 5V, V_{CC1} = 5.5V, V_{CC2} = 15V All Other Pins Open			6.7	11	mA
OP_{VOH}	Op Amp Minimum High Level	V_{CC1} = 4.5V, I_{OH} = −750 μA		V_{CC2} −0.4			V
OP_{VOL}	Op Amp Maximum Low Level	V_{CC1} = 5.5V, I_{OL} = 750 μA				0.6	V
CPO_{BIAS}	Charge Pump Bias Voltage Delta	CPO Shorted to Op Amp Output CPO = TRI-STATE Op Amp I_{OL}: 750 μA vs −750 μA				100	mV

AC Electrical Characteristics V_{CC} = 5V, T_A = 25°C, t_r ≤ 10 ns, t_f ≤ 10 ns

Symbol	Parameter	Conditions		Min	Typ	Max	Units
$V_{IN(MIN)(F)}$	F_{IN} Minimum Signal Input	AM and FM Inputs, −40°C ≤ T_A ≤ 85°C			20	100	mV(rms)
$V_{IN(MAX)(F)}$	F_{IN} Maximum Signal Input	AM and FM Inputs, −40°C ≤ T_A ≤ 85°C		1000	1500		mV(rms)
$F_{OPERATE}$	Operating Frequency Range (Sine Wave Input)	V_{IN} = 100 mV rms −40°C ≤ T_A ≤ 85°C	AM	0.5		15	MHz
			FM	80		120	MHz
$R_{IN(FM)}$	AC Input Resistance, FM	120 MHz, V_{IN} = 100 mV rms		600			Ω
$R_{IN(AM)}$	AC Input Resistance, AM	15 MHz, V_{IN} = 100 mV rms		1000			Ω
C_{IN}	Input Capacitance, FM and AM	V_{IN} = 120 MHz (FM), 15 MHz (AM)		3	6	10	pF
t_{EN1}	Minimum ENABLE High Pulse Width				625	1250	ns

AC Electrical Characteristics $V_{CC} = 5V, T_A = 25°C, t_r \leq 10$ ns, $t_f \leq 10$ ns (Continued)

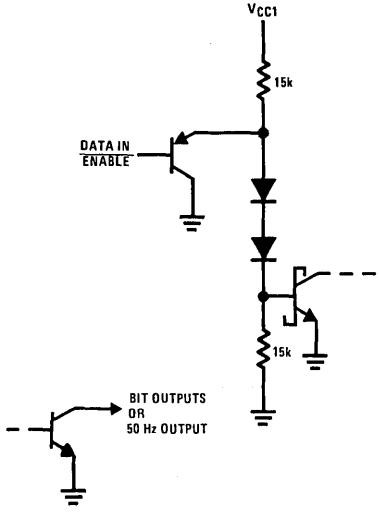
Symbol	Parameter	Conditions	Min	Typ	Max	Units
$t_{\overline{EN}0}$	Minimum $\overline{\text{ENABLE}}$ Low Pulse Width			375	750	ns
$t_{CLK\overline{EN}0}$	Minimum Time before $\overline{\text{ENABLE}}$ Goes Low That CLOCK Must Be Low			−50	0	ns
$t_{\overline{EN}0CLK}$	Minimum Time after $\overline{\text{ENABLE}}$ Goes Low That CLOCK Must Remain Low			275	550	ns
$t_{CLK\overline{EN}1}$	Minimum Time before $\overline{\text{ENABLE}}$ Goes High That Last Positive CLOCK Edge May Occur			300	600	ns
$t_{\overline{EN}1CLK}$	Minimum Time after $\overline{\text{ENABLE}}$ Goes High before an Unused Positive CLOCK Edge May Occur			175	350	ns
t_{CLKH}	Minimum CLOCK High Pulse Width			275	550	ns
t_{CLKL}	Minimum CLOCK Low Pulse Width			400	800	ns
t_{DS}	Minimum DATA Set-Up Time, Minimum Time before CLOCK That DATA Must Be Valid			150	300	ns
t_{DH}	Minimum DATA Hold Time, Minimum Time after CLOCK That DATA Must Remain Valid			400	800	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

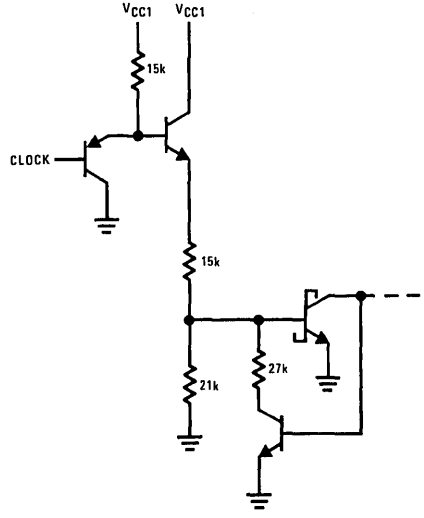
Note 2: Unless otherwise specified min/max limits apply across the −40°C to +85°C temperature range for the DS8908.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltage referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Schematic Diagrams (DS8908 AM/FM PLL Typical Input/Output Schematics)



TL/F/5111–2



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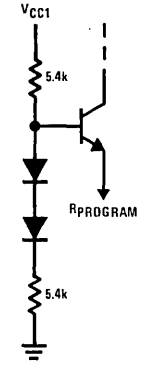

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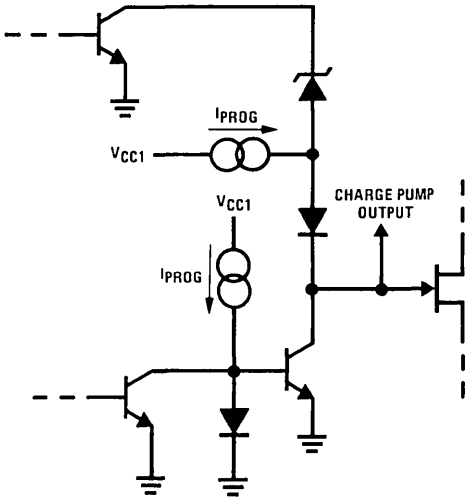
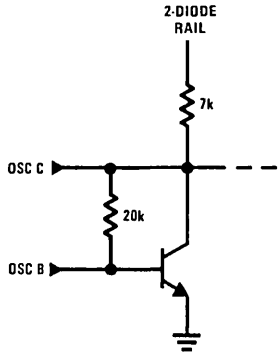
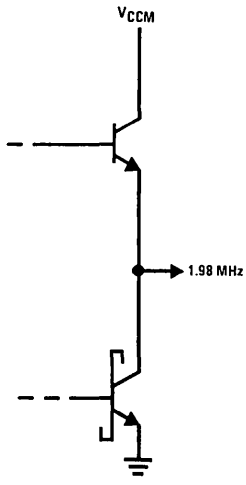
Schematic Diagrams (Continued)



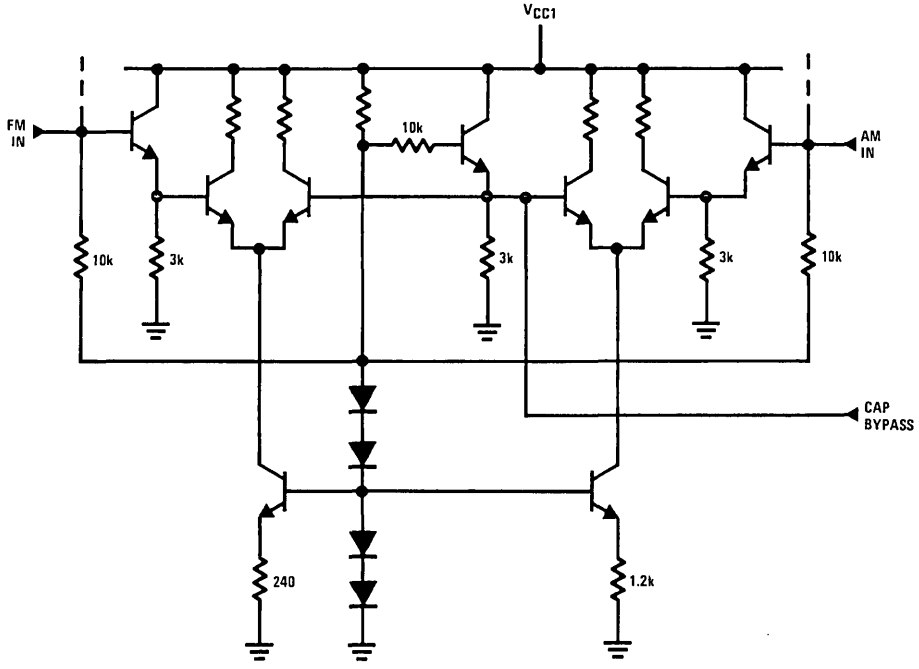
TL/F/5111–5



TL/F/5111–6

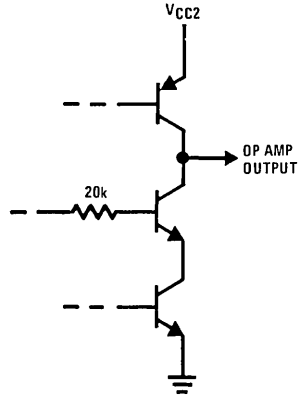


TL/F/5111–7



TL/F/5111–8

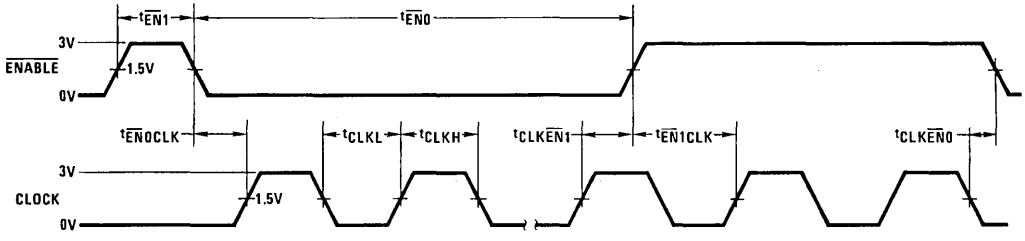
Schematic Diagrams (Continued)



TL/F/5111–9

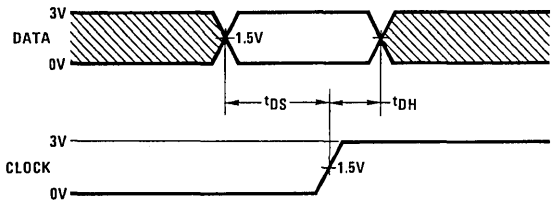
Timing Diagrams*

$\overline{\text{ENABLE}}$ vs CLOCK



TL/F/5111–10

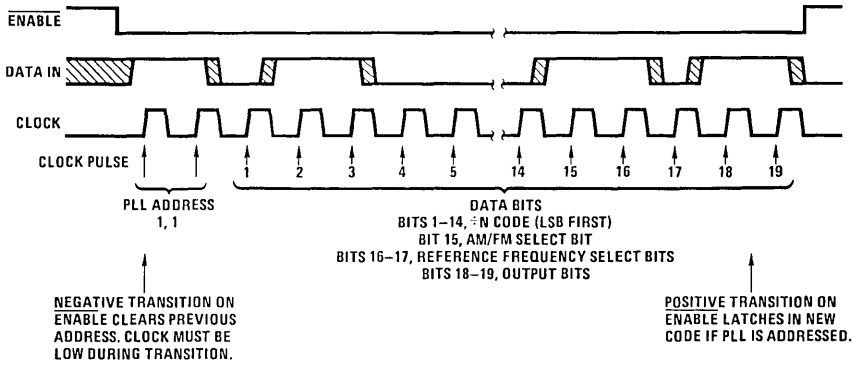
CLOCK vs DATA



TL/F/5111–11

Timing Diagrams*

AM/FM Frequency Synthesizer (Scan Mode)



TL/F/5111–12

*Timing diagrams are not drawn to scale. Scale within any one drawing may not be consistent, and intervals are defined positive as drawn.

SERIAL DATA ENTRY INTO THE DS8908

Serial information entry into the DS8908 is enabled by a low level on the $\overline{\text{ENABLE}}$ input. One binary bit is then accepted from the DATA input with each positive transition of the CLOCK input. The CLOCK input must be low for the specified time preceding and following the negative transition of the $\overline{\text{ENABLE}}$ input.

The first two bits accepted following the negative transition of the $\overline{\text{ENABLE}}$ input are interpreted as address. If these address bits are *not* 1,1 *no* further information will be accepted fromt he DATA inputs, and the internal data latches *will not* be changed when $\overline{\text{ENABLE}}$ returns high.

If these first two bits *are* 1,1, then all succeeding bits are *accepted* as data, and are shifted successively into the internal shift register as long as $\overline{\text{ENABLE}}$ remains low.

Any data bits preceding the 19th to last bit will be shifted out, and thus are irrelevant. Data bits are counted as any bits *following* two valid address bits (1,1) with the $\overline{\text{ENABLE}}$ low. When the $\overline{\text{ENABLE}}$ input returns high, any further serial data entry is inhibited. Upon this positive transition, the data in the internal shift register is transferred into the internal data latches. Note that until this time, the states of the internal data latches have remained unchanged.

These data bits are interpreted as follows:

Data Bit Position	Data Interpretation
Last	Bit 19 Output (Pin 2)
2nd to Last	Bit 18 Output (Pin 1)
3rd to Last	Ref. Freq. Select Bit(1) 17
4th to Last	Ref. Freq. Select Bit(1) 16
5th to Last	AM/FM Select Bit 15
6th to Last	(2^{13})
7th to Last	(2^{12})
8th to Last	(2^{11})
9th to Last	(2^{10})
10th to Last	(2^{9})
11th to Last	(2^{8})
12th to Last	(2^{7})
13th to Last	(2^{6})
14th to Last	(2^{5})
15th to Last	(2^{4})
16th to Last	(2^{3})
17th to Last	(2^{2})
18th to Last	(2^{1})
19th to Last	LSB of $\div N(2^{0})$

$\div N(2)$

Note 1: See Reference Frequency Select Truth Table.

Note 2: The actual divide code is N + 1, ie., the number loaded plus 1.

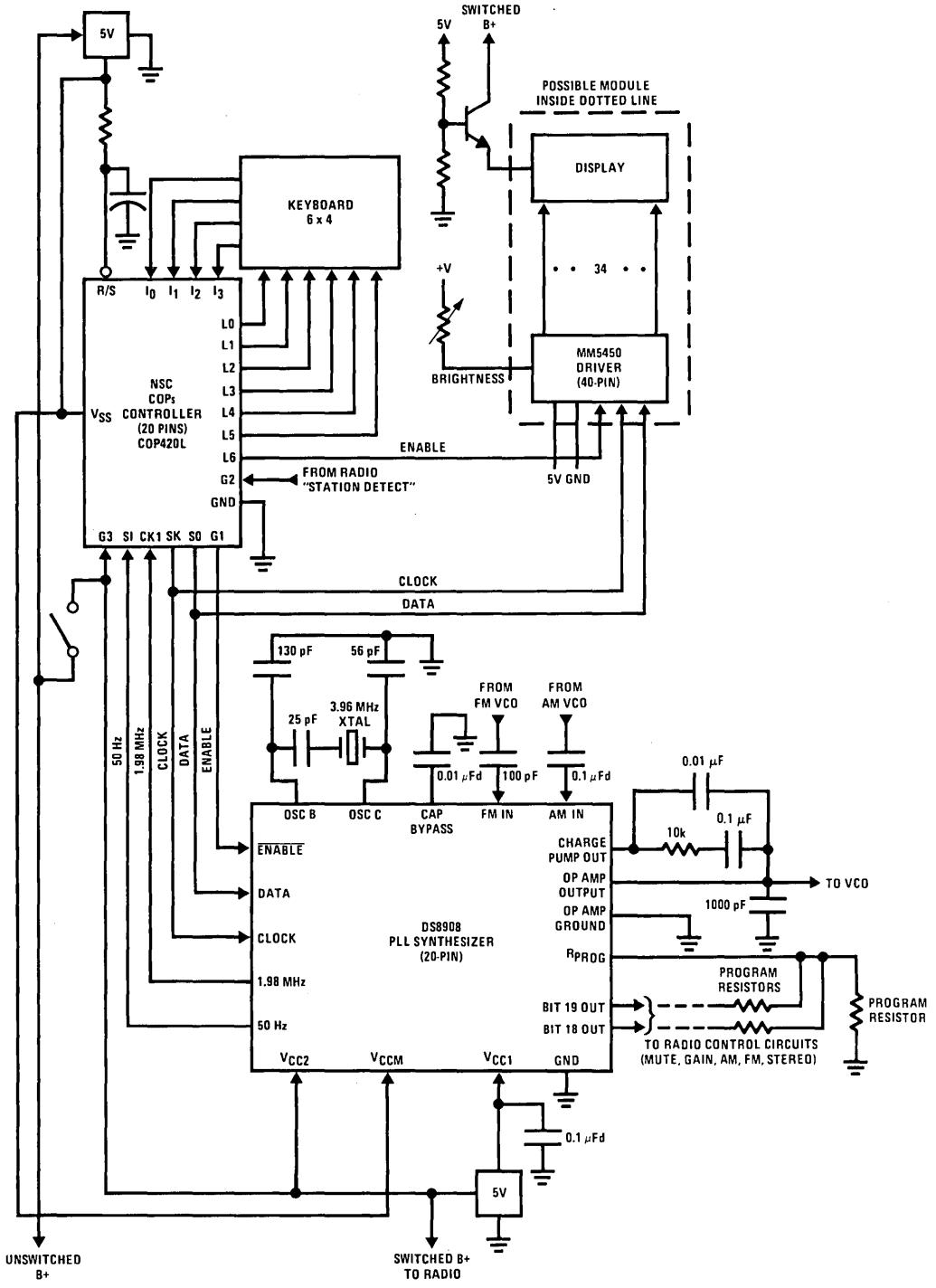
Truth Table

Reference Frequency Selection Truth Table

Serial Data		Reference Frequency
Bit 16	Bit 17	(kHz)
1	1	20
1	0	10
0	1	9
0	0	1

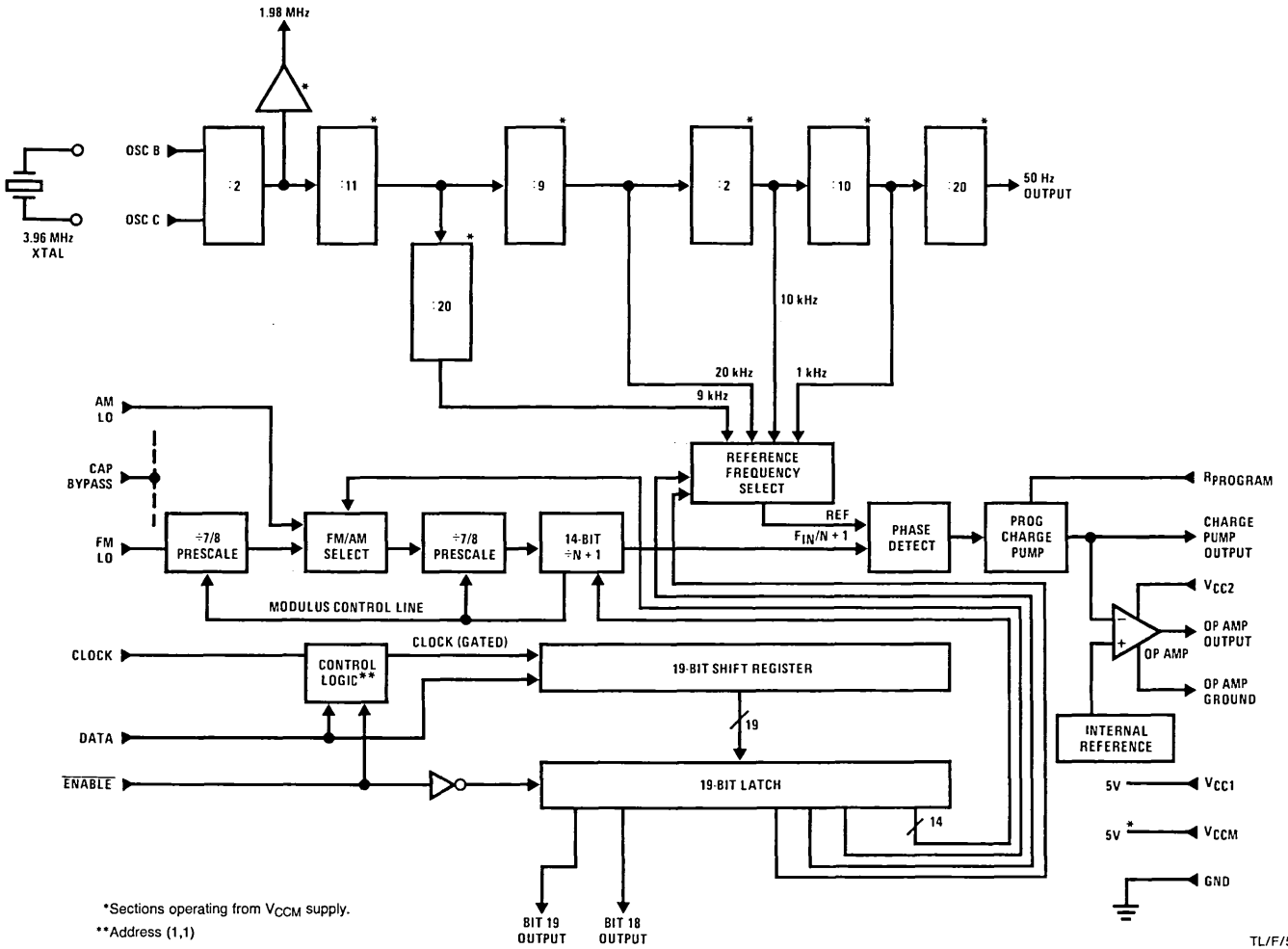
Typical Application Additional application notes are located at the back of section 11.

Electronically Tuned Radio Controller System; Direct Drive LED



TL/F/5111–13

AM/FM PLL/Synthesizer (Serial Data 20-Pin Package)



*Sections operating from V_{CCM} supply.

**Address (1,1)

TL/F/5111–14

National Semiconductor Corporation

PRELIMINARY

DS8911/DS8912 AM/FM/TV Sound Up-Conversion Frequency Synthesizers

General Description

The DS8911 and DS8912 are digital Phase-Locked Loop (PLL) frequency synthesizers intended for use as Local Oscillators (LO) in electronically tuned radios. The devices are used in conjunction with a serial data controller, a loop filter, some varactor diodes and several passive elements to provide the local oscillator function for both AM and FM tuning.

The conventional superheterodyne AM receiver utilizes a low IF or down conversion tuning approach whereby the IF is chosen to be below the frequencies to be received. The DS8911 and DS8912 PLL's on the other hand, utilize an up-conversion technique in the AM mode whereby the first IF frequency is chosen to be well above the RF frequency range to be tuned. This approach eliminates the need for tuned circuits in the AM frontend since the image, half IF, and other spurious responses occur far beyond the range of frequencies to be tuned. Sufficient selectivity and second IF image protection is provided by a crystal filter at the output of the first mixer.

A significant cost savings can be realized utilizing this up-conversion approach to tuning. Removal of the AM tuned circuits eliminates the cost of expensive matched varactor diodes and reduces the amount of labor required for alignment down from 6 adjustments to 2. Additional cost savings are realized because up-conversion enables both the AM and FM bands to be tuned using a single Voltage Controlled Oscillator (VCO) operating between 98 and 120 MHz. (The 2 to 1 LO tuning range found in conventional AM down conversion radios is reduced to a 10% tuning range; 9.94 MHz to 11.02 MHz).

Up-conversion AM tuning is accomplished by first dividing the VCO signal down by a modulus 10 (DS8911) or 20 (DS8912) to obtain the LO signal. This LO in turn is mixed on chip with the RF signal to obtain a first IF at the MIXER output pins. This first IF after crystal filtering is mixed (externally) with a reference frequency provided by the PLL to obtain a 450 kHz second IF frequency. The DS8911 derives the 450 kHz second IF by mixing an 11.55 MHz first IF with a 12.00 MHz reference frequency. The DS8912 derives the 450 kHz second IF by mixing a 4.45 MHz first IF with a 4.00 MHz reference frequency.

FM and WB (weather band) tuning is done using the conventional down conversion approach. Here the VCO signal is buffered to produce the LO signal and then mixed on chip with the RF signal to obtain an IF frequency at the MIXER output pins. This IF frequency is typically chosen to be 10.7 MHz although placement at 11.50 MHz can further enhance AM mode performance and minimize IF circuitry.

The DS8911 was designed to utilize an 11.55 MHz crystal filter because of its superior phase noise and temperature drift characteristics. The DS8912 on the other hand was designed to utilize a 4.45 MHz ceramic filter for cost savings in applications not requiring high performance.

Both PLLs provide phase comparator reference frequencies of 10, 12.5, 25, and 100 kHz. The tuning resolutions resulting from these reference frequencies are determined by dividing the reference by the premix modulus. Table II shows the tuning resolutions possible.

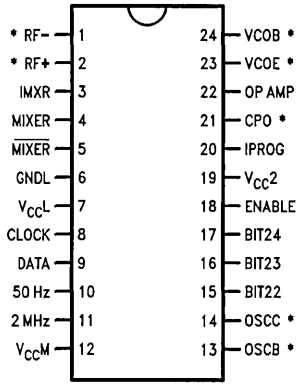
The DS8911 and DS8912 contain the following logic elements: a voltage controlled oscillator, a reference oscillator, a 14-bit programmable dual-modulus counter, a reference frequency divider chain, a premix divider, a mixer, a phase comparator, a charge pump, an operational amplifier, and control circuitry for latched serial data entry.

Features

- Direct synthesis of LW, MW, SW, FM, and WB frequencies
- Serial data entry for simplified processor control
- 10, 12.5, 25, and 100 kHz reference frequencies
- 8 possible tuning resolutions (see Table II)
- An op amp with high impedance inputs for loop filtering
- Programmable mixer with high dynamic range
- Fast-lock feature for Automatic Road Information (ARI) systems

Connection Diagrams

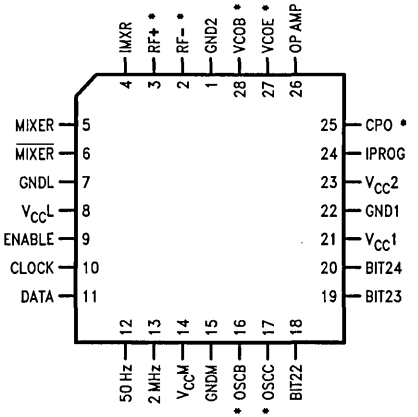
SO and Dual-In-Line Packages



TL/F/7398–7

Top View

Plastic Chip Carrier



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Top View

Order Number DS8911M, DS8911N, DS8911V, DS8912M, DS8912N or DS8912V
See NS Package Number M24B, N24C or V28A

Note: Device pins marked with an asterisk (*) are not guaranteed to meet the NSC standard requirement for Electrostatic Discharge (ESD) protection of 2000 volts. The functional requirements of the application prohibit the additional resistive or capacitive components required for ESD protection on these pins.

Pin Descriptions

V_{CC1}: The V_{CC1} pin provides a 5V supply source for all circuitry except the reference divider chain, op amp and mixer sections of the die.

V_{CC2}: The V_{CC2} pin provides a 12V supply source for the Op amp.

V_{CCL}: The V_{CCL} pin provides an isolated 5V supply source for the premix divider and mixer functions.

V_{CCM}: The V_{CCM} pin provides a 5V supply source for the reference oscillator and divider chain down through the 50 Hz output, thus enabling low standby current for time-of-day clock applications.

GND1, GND2, GNDL and GNDM: Provide isolated circuit ground for the various sections of the device.

DATA and CLOCK: The DATA and CLOCK inputs are for serial data entry from a controller. They are CMOS inputs with TTL logic thresholds. The 24-bit data stream is loaded into the PLL on the positive transition of the CLOCK. The first 14 bits of the data stream select PLL divide code in binary form MSB first. The 15th through 24th bits select the premix modulus, the reference frequency, the loop response mode, the bit output status, and the test/operate modes as shown in Tables I through V.

ENABLE: The ENABLE input is a CMOS input with a TTL logic threshold. The ENABLE input enables data when at a logic "one" and latches data on the transition to a logic "zero".

BIT Outputs: The open-collector BIT outputs provide either the status of shift register bits 22, 23, and 24 or enable access to key internal circuit test nodes. The mode for the bit outputs is controlled by shift register bits 20 and 21. In operation, the bit outputs are intended to drive radio functions such as gain, mute, and AM/FM status. These outputs can also be used to program the loop gain by connection of an external resistor to IPROG. Bit 24 output can also be used as a 300 millisecond timer under control of shift register bit 19. During service testing, these pins can be used for the purpose of either monitoring or driving internal logic points as indicated in the TEST MODES description under Table V.

VCOb and VCOe: The Voltage Controlled Oscillator inputs drive the 14-bit programmable counter and the premix divider. These inputs are the base and emitter leads of a transistor which require connection of a coil, varactor, and several capacitors to function as a Colpitts oscillator. The VCO is designed to operate up to 225 MHz. The VCO's minimum operating frequency may be limited by the choice of reference frequency and the 961 minimum modulus constraint of the 31/32 dual modulus counter.

RF+ and RF−: The Radio Frequency inputs are fed differentially into the mixer.

IMXR: The bias current for the mixer is programmed by connection of external resistors.

MIXER and $\overline{\text{MIXER}}$: The MIXER outputs are the collectors of the double balanced pair mixer transistors. They are intended to operate at voltages greater than V_{CC1}.

OSCb and OSCc: The Reference Oscillator inputs are part of an on-chip Pierce oscillator designed to work in conjunction with 2 capacitors and a crystal resonator. The DS8911 requires a 12 MHz crystal, while the DS8912 requires a 4 MHz crystal.

The OSC input signal is mixed externally with the 1st AM IF output to obtain a 450 kHz 2nd IF frequency in the AM mode.

2 MHz: The 2 MHz output is provided to drive a controller's clock input.

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Pin Descriptions (Continued)

50 Hz: The 50 Hz output is provided as a time reference for radios with time-of-day clocks.

IPROG: The IPROG pin enables the charge pump to be programmed from .5 mA to 1.5 mA by connection of an extenal resistor to ground.

CPO: The Charge Pump Output circuit sources current if the VCO frequency is high and sinks current if the VCO frequency is low. The CPO is wired directly to the negative input of the loop filter op amp.

OP AMP: The OP AMP output is provided for loop filtering. The op amp has high impedance PMOS gate inputs and is wired as a transconductance amplifier/filter. The op amp's positive input is internally referenced while it's negative input is common with the CPO output.

Reference Tables DS8911 (DS8912)

TABLE I

Bit 15	Premix Modulus
0	÷1
1	÷10 (÷20)

TABLE II

Bit		Reference Frequency	Tuning Resolution	
16	17		÷1 Premix	÷10 (÷20) Premix
0	0	10 kHz	10 kHz	1 (.5) kHz
0	1	12.5 kHz	12.5 kHz	1.25 (.625) kHz
1	0	25 kHz	25 kHz	2.5 (1.25) kHz
1	1	100 kHz	100 kHz	10 (5) kHz

TABLE III

Bit 18	Loop Response
0	Normal Lock
1	Fast Lock

FAST LOCK OPERATION

The fast lock mode provides a means of moving from one frequency selection to another frequency selection anywhere on the band in a very short time frame. This is accomplished by setting a bit in the microprocessor serial data stream when loading a new frequency. When fast lock is activated the charge pump output (CPO) is latched into the pump up or down state, which drives the CPO at the maximum rate to correct the VCO frequency. The PLL meanwhile operates in a frequency lock mode, constantly comparing the frequencies and reducing any phase discrepancies. When the VCO passes beyond the desired lock frequency the CPO unlatches and reverts back to the phase lock mode of operation. The frequency lock mode of operation (during CPO latchup) ensures that the phases are always close and will quickly settle into phase lock once the CPO unlatches.

TABLE IV

Bit 19	Timer
0	Bit 24 Status
1	$\overline{\text{Bit 24}}$ for 300 ms

TIMER OPERATION

The timer function is provided for use as a retriggerable "one shot" to enable muting for approximately 300 milliseconds after station changes. The timer is enabled at bit 24's output if the normal operating mode is selected (shift register bits 20 and 21 = "LOW") and shift register bit 19 data is latched as a "HI". The timer's output state will invert immediately upon latching bit 19 "HI" and remain inverted for approximately 300 milliseconds. If the user readdresses the device with bit 19 data "LOW" before the timer finishes its cycle the timer's BIT 24 output will finish out the 300 ms pulse. Readdressing the device with bit 19 "HI" before the timer finishes its cycle will extend the BIT 24 output pulse width by 300 ms. Addressing should be performed immediately after the 50 Hz output transitions "HI". BIT 24's output state is not guaranteed during the first 300 ms after V_{CC_1} power up as a result of a timer reset in progress.

TABLE V

Bit		FUNCTION OF PINS 3, 4, & 5
20	21	
0	0	Status of Bits 22-24
0	1	Test mode 1
1	0	Test mode 2
1	1	Test mode 3

TEST MODE OPERATION

Test Mode 1: Enables the BIT output pins to edge trigger the phase comparator inputs and monitor an internal lock detector. BIT 22 negative edge triggers the reference divider input of the phase comparator if the reference divider state is low. BIT 23 provides the open collector ORing of the phase comparator's pump up and down outputs. BIT 24 negative edge triggers the N counter input of the phase comparator if the N counter state is preconditioned low.

Test Mode 2: Enables the BIT outputs to clock the programmable N counter, monitor its output, and force either its load or count condition. BIT 22 provides the N counter output which negative edge triggers the phase comparator and which appears low one N counter clock pulse before it reloads. BIT 23 positive edge triggers the N counter's clock input if the prescaler's output is preconditioned HI. BIT 24 clears the N counter output so that loading will occur on the next N counter clock edge.

Test Mode 3: Enables the BIT outputs to clock the 50 Hz and 10 kHz reference dividers, monitor the reference divider input to the phase comparator, and reset the fast lock latch. BIT 22 positive edge clocks the 10 kHz reference divider chain if the 10 kHz output is preconditioned HI. BIT 22 also positive edge clears the fast lock latch condition. Bit 23 positive edge clocks the 50 Hz divider chain. BIT 24 is the reference divider negative edge trigger input to the phase comparator.

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage
- V_{CCM} 7V
- V_{CC1} 7V
- V_{CC2} 15V

Input Voltage 7V

Output Voltage
- Logic 7V
- Op Amp and Mixer Outputs 15V

Storage Temperature Range −65°C to +150°C

Lead Temp. (Soldering, 10 seconds) 300°C

Operating Conditions

	Min	Max	Units
V_{CCM}	3.5	5.5	V
V_{CC1}	4.5	5.5	V
V_{CC2}	7.0	12.0	V
Temperature, T_A	−40	+85	°C

DC Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter		Test Conditions		Min	Typ	Max	Units
V_{IH}	Logic "1" Input Voltage				2.0			V
V_{IL}	Logic "0" Input Voltage						0.8	V
I_{IH}	Logic "1" Input Current		V_{IN} = 5.5V				10	μA
I_{IL}	Logic "0" Input Current		Data, Clock and Enable Inputs, V_{IN} = 0V				−10	μA
V_{OH}	Logic "1" Output Voltage	2 MHz	I_{OH} = −20 μA		V_{CCM}−0.3			V
			I_{OH} = −400 μA		V_{CCM}−2			V
		Op Amp	I_{OH} = −1.5 mA		V_{CC_2}−1.5			V
V_{OL}	Logic "0" Output Voltage	2 MHz	I_{OL} = 20 μA				0.3	V
			I_{OL} = 400 μA				0.4	V
		50 Hz	I_{OL} = 250 μA				0.3	V
		Bit Outputs	I_{OL} = 1 mA				0.3	V
		Op Amp	I_{OL} = 1.5 mA				1.5	V
V_{BIAS}	Op Amp Input VΔ		Op Amp I/O Shorted, V_{CC1} = 5.5V, V_{CC2} = 12V, CPO = TRI-STATE®, Op Amp I_{OH} vs. I_{OL} Applied				150	mV
I_{CEX}	High Level Output Current	Bit Outputs	V_{CC_1} = 4.5V, V_O = 8.8V				100	μA
		50 Hz	V_{CC_M} = 3.5V, V_O = 5.5V				10	μA
		Mixers	V_{CC_L} = V_{CC_1} = 4.5V, V_O = 8.8V				100	μA
I_{CPO}	Charge Pump Program Current		0.5 mA < I_{CPO} < 1.5 mA 2 I_{PROG} = V_{CC_1}/R_{PROG}, Measured I_{PROG} to CPO	Pump-up	−20	2 I_{PROG}	+20	%
				Pump-down	−20	2 I_{PROG}	+20	%
				TRI-STATE		0	100	nA
I_{CCM}	V_{CCM} Supply Current		V_{CCM} = 5.5V			0.5	1.0	mA
I_{CC1} + I_{CCL}	V_{CC1} + V_{CCL} Supply Current		V_{CC} = 5.5V, Bits Hi, I_{MXR} and I_{PROG} Open			25	35	mA
I_{CC2}	V_{CC2} Supply Current		V_{CC2} = 12V			1.5	2.5	mA
R_{IN}	Mixer Input Impedance		I_{MXR} = 2.5 mA I_{MXR} = 7.5 mA			TBD TBD		Ω Ω
R_{OUT}	Mixer Output Impedance		I_{MXR} = 2.5 mA I_{MXR} = 7.5 mA			TBD TBD		Ω Ω
g_m	Mixer Transconductance		I_{MXR} = 2.5 mA I_{MXR} = 7.5 mA			TBD TBD		mhos mhos
NF	Noise Figure		I_{MXR} = 2.5 mA, R_S = 50Ω I_{MXR} = 7.5 mA, R_S = 10Ω			TBD TBD		dB dB
XMOD	Cross Modulation		I_{MXR} = 2.5 mA I_{MXR} = 7.5 mA			TBD TBD		mVRms mVRms
I_{MXR}	Mixer Current		V_{CC1} = 5.5V		1		7.5	mA
VCO_{MAX}	VCO_{MAX} frequency						225	MHz

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range", they are not meant to imply that the device should be operated at these limits.

Note 2: Unless otherwise specified, min/max limits apply across the −40°C to +85°C temperature range for DS8911 and DS8912.

Note 3: All currents into device pins are shown as positive, out of device pins as negative, all voltage referenced to ground unless otherwise noted. All values shown as maximum or minimum on absolute value basis.

AC Electrical Characteristics (Note 2)

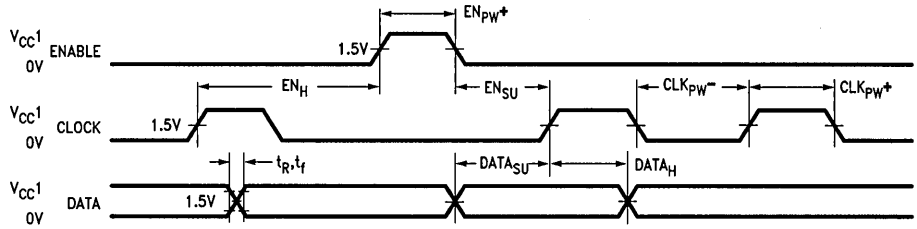
Symbol	Parameter	Conditions	Min	Max	Units
t_r	20%–80% Rise Time	V_{CC_1} = 4.5V to 5.5V		200	ns
t_f	80%–20% Fall Time			200	ns
$DATA_{SU}$	Data Setup Time		100		ns
$DATA_H$	Data Hold Time		100		ns
EN_{SU}	Enable Setup Time		100		ns
EN_H	Enable Hold Time		100		ns
EN_{PW+}	Enable Positive Pulse Width		200		ns
CLK_{PW+}	Clock Positive Pulse Width		200		ns
CLK_{PW-}	Clock Negative Pulse Width		200		ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range", they are not meant to imply that the device should be operated at these limits.

Note 2: Unless otherwise specified, min/max limits apply across the −40°C to +85°C temperature range for DS8911 and DS8912.

Note 3: All currents into device pins are shown as positive, out of device pins as negative, all voltage referenced to ground unless otherwise noted. All values shown as maximum or minimum on absolute value basis.

Timing Diagram



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MICROWIRE™ Bus Format

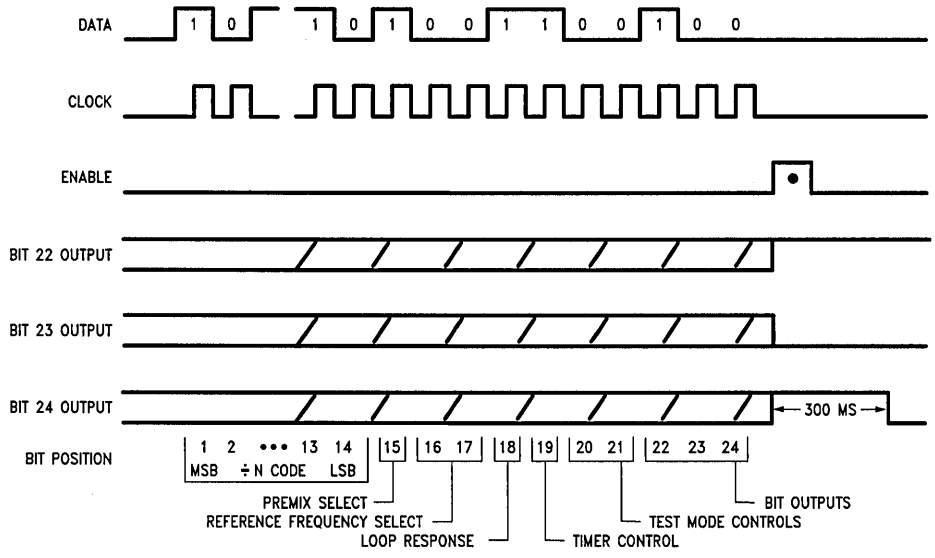

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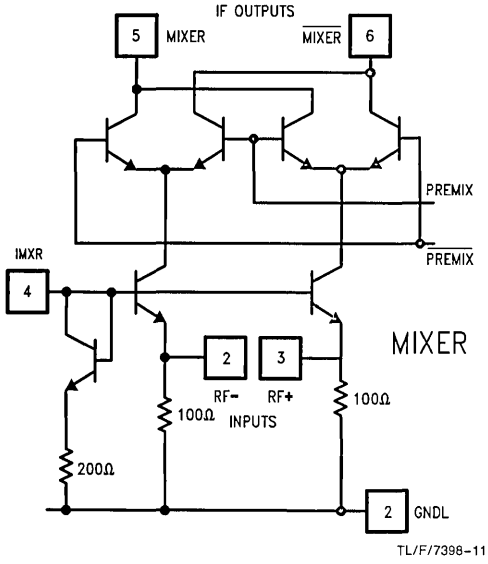
TABLE VI. DS8911 Tuning Characteristics

Mode	IF Frequency (MHz)	Tuning Range (MHz)	VCO Range (MHz)	Premix Modulus	Reference Frequency (kHz)	Tuning Resolution (kHz)	Image (MHz)
LW	11.55/.450	.145–.290	112.4–114.1	10	10	1	22–23
MW	11.55/.450	.515–1.61	99.4–110.2	10	10, 12.5, 25, 100	1, 1.25, 2.5, 10	21–23
SW	11.55/.450	5.94–6.2	53.5 to 56.1	10	10, 12.5, 25	1, 1.25, 2.5	28–30
FM	10.7	87.4–108.1	98.1–118.8	1	10, 12.5, 25, 100	10, 12.5, 25, 100	109–130
WB	10.7	162.4–162.6	151–152	1	12.5, 25	12.5, 25	140–142
TV_1	10.7	59.75–87.75	70.45–98.45	1	25	25	81–109
TV_2	10.7	179.75–215.75	169.1–205.1	1	25	25	158–194

TABLE VII. DS8912 Tuning Characteristics

Mode	IF Frequency (MHz)	Tuning Range (MHz)	VCO Range (MHz)	Premix Modulus	Reference Frequency (kHz)	Tuning Resolution (kHz)	Image (MHz)
LW	4.45/.450	.145–.290	91.9–94.8	20	10	.5	13–14
MW	4.45/.450	.515–1.61	99.6–121.2	20	10, 12.5, 25, 100	.5, .625, 1.25, 5	14–17
SW	4.45/.450	5.94–6.2	207.9–213.1	20	25, 100	1.25, 5	14–16
FM	10.7	87.4–108.1	98.1–118.8	1	10, 12.5, 25, 100	10, 12.5, 25, 100	109–130
WB	10.7	162.4–162.6	151–152	1	12.5, 25	12.5, 25	140–142

Input and Output Schematics



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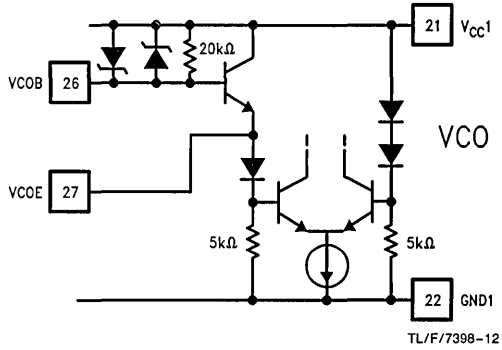

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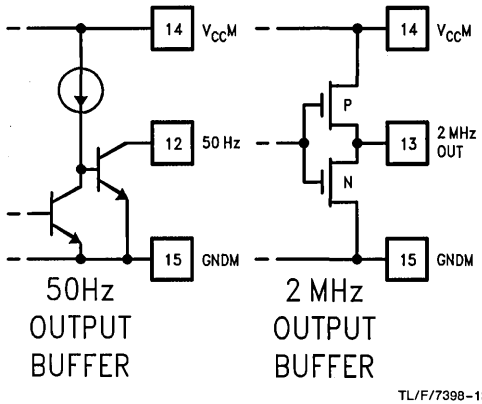
Input and Output Schematics (Continued)



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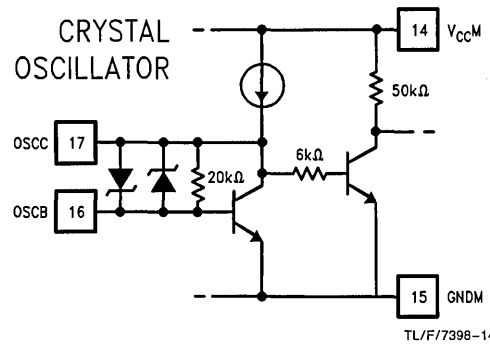

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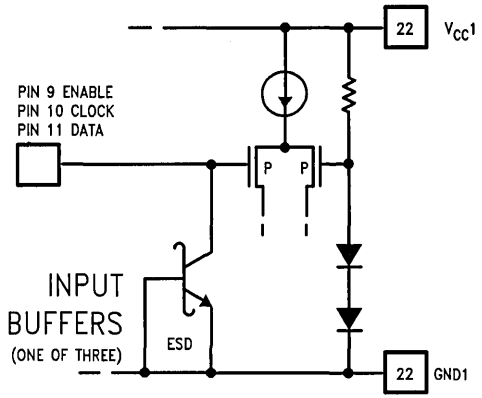

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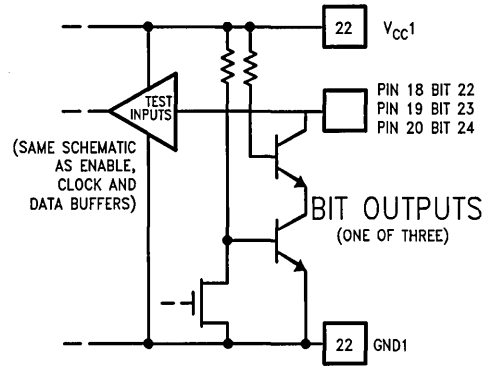

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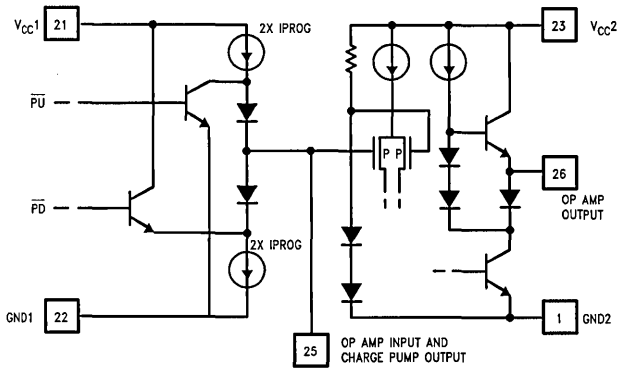

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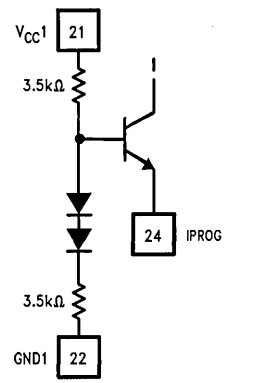

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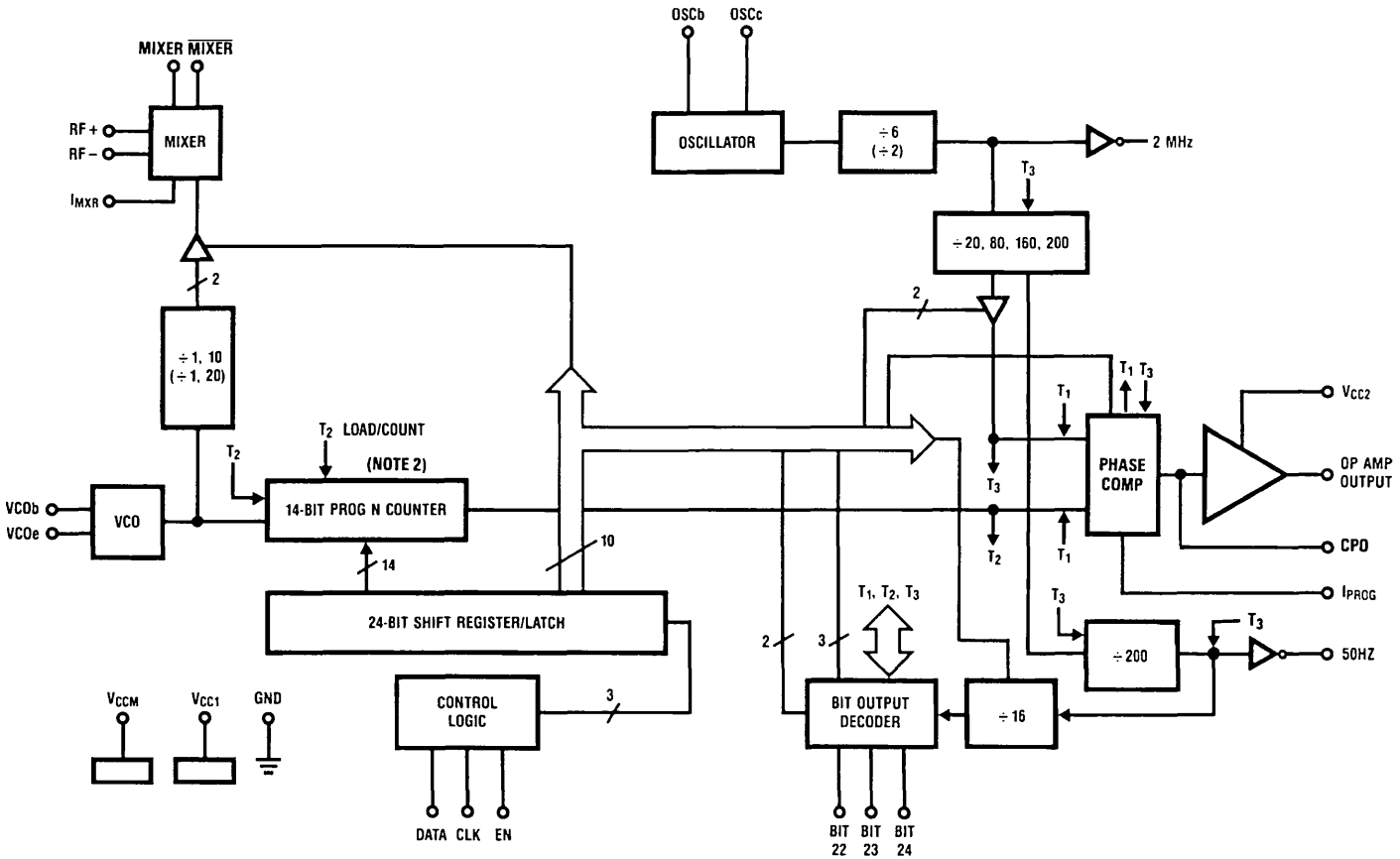
DS8911 (DS8912) PLL Synthesizer



Note 1: Logic labels (in parentheses) pertain to the DS8912 option.

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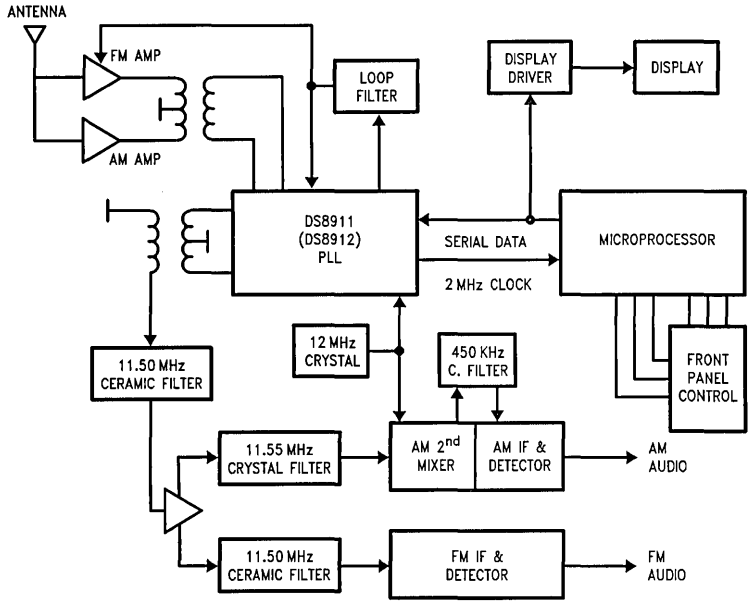
Note 2: The 14 bit programmable N counter is a dual modulus counter with 31/32 prescaler. The minimum continuous modulus of the N counter is 961. (There are a limited number of valid modulus codes below 961.)

Typical Application

AM/FM ETR Radio Application



TL/F/7398–5

Digital PLL Synthesis

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Application Note 335
Craig Davis
Tom Mills
Keith Mueller

I. System Concepts

INTRODUCTION

Digital tuning systems are fast replacing the conventional mechanical systems in AM/FM and television receivers. The desirability of the digital approach is mainly due to the following features:

- Precise tuning of station frequencies
- Exact digital frequency display
- Keyboard entry of desired frequency
- Virtually unlimited station memory
- Up/down scanning through the band
- Station "search" (stop on next active station)
- Power on to the last station
- Easy option for time-of-day clock

In addition, recent developments in large scale integrated circuit technology and new varactor diodes for the AM band have made the cost-benefit picture for digital tuning very attractive. System partitioning is extremely important in optimizing this cost-benefit picture, as will be discussed.

SYSTEM DESCRIPTION

A simplified block diagram of a typical digitally tuned receiver is shown in *Figure 1*. Notice this receiver could be one for AM, FM, marine radio, or television; it makes no difference. The frequency synthesizer block generates the local oscillator frequency for the receiver, just as a conventional mechanical tuner would. However, the phase-locked-loop (PLL) acts as an integral frequency multiplier of an accurate crystal controlled reference frequency while the mechanical type provides a continuously variable frequency output with no reference. Some method of controlling the value of the multiplier for channel tuning must be provided. The other RF, IF, and audio/video circuitry will be the same as in the mechanical tuning method.

There are many different ways to partition the frequency synthesizer system to perform the digital tuning function.

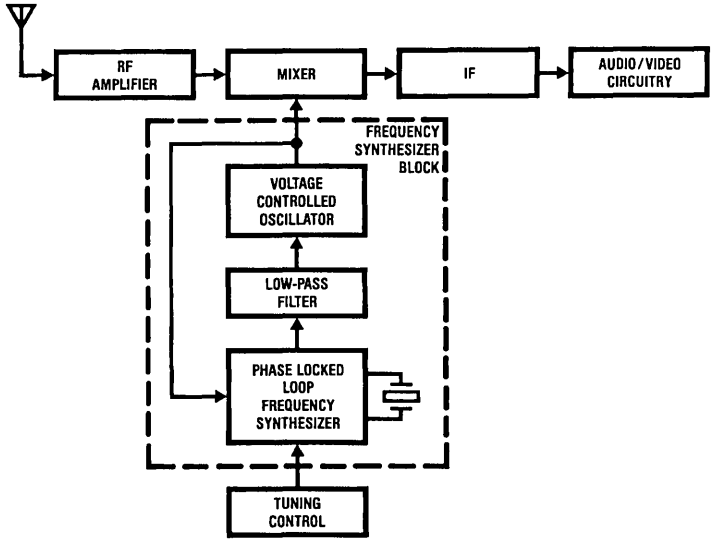

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FIGURE 1. Block Diagram of a Digitally Tuned Receiver

PROGRAMMABLE CONTROLLER FUNCTION

The most cost-effective application of different IC process technologies is shown in *Figure 2*. The controller is separate from the PLL. The controller can be as simple as a mask programmable microcontroller* or as complicated as a high-powered microprocessor system. It can be done most economically with NMOS technology because of the logic density possible and the small size of the RAM/ROM memory cells. It could also be CMOS for extremely low power consumption in standby mode.

BASIC PHASE-LOCKED-LOOP FUNCTION

The DS8906/7/8 series of PLLs utilize a dual-modulus frequency synthesis technique. The reasons for this and the PLL itself will now be discussed.

Figure 3 is a diagram of the most simple phase-locked-loop. A particular reference frequency is generated by a crystal oscillator and some fixed divider, and this goes into one side of a digital phase comparator. A voltage controlled oscillator (VCO) feeds directly into the other input of the phase comparator. The output of the phase comparator is an error signal which is filtered and fed back to the VCO as a DC control voltage.

In lock, the phase error must be zero, so f_{IN} equals f_{REF}. This system provides only one output frequency, that being equal to the reference frequency.

Figure 4 is basically the same but now a programmable divide-by-N counter is between the VCO and the phase comparator. The input to the phase comparator (f_{IN}) now becomes the output frequency of the VCO (f_{OUT}) divided by N, where N is the division code loaded into the programmable counter. This means f_{OUT}/N must equal f_{REF}. Thus, the VCO output frequency becomes $N \times f_{REF}$, and f_{OUT} can now be changed in integral steps of f_{REF} by merely changing N.

*Such as National's COP™ family.

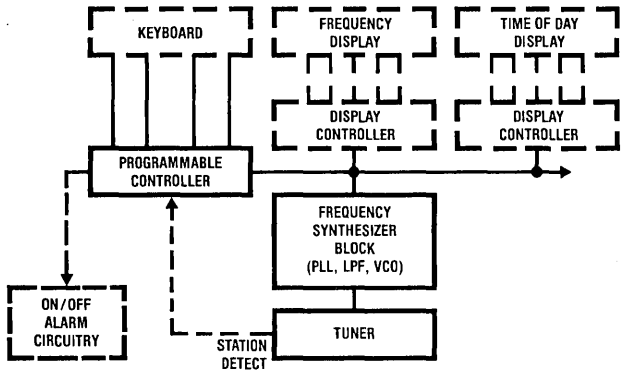

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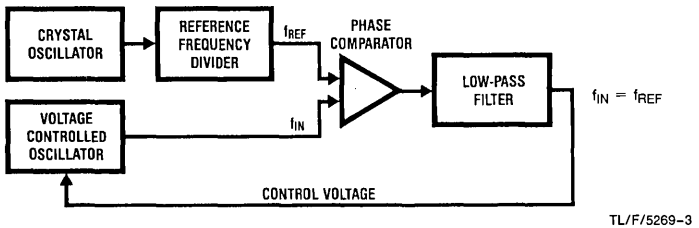
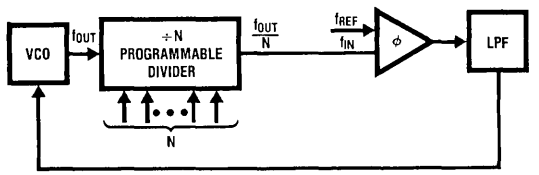
FIGURE 2. System Block Diagram



TL/F/5269-3

FIGURE 3. Basic Phase-Locked-Loop



$f_{IN} = f_{REF}$

$f_{IN} = \frac{f_{OUT}}{N}$

$\frac{f_{OUT}}{N} = f_{REF}$

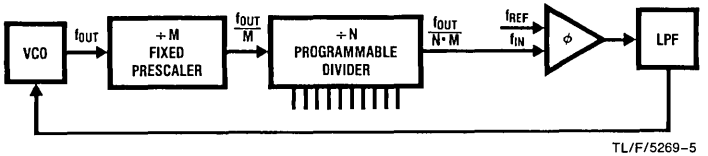
$f_{OUT} = N \times f_{REF} \rightarrow f_{STEP}$
$= f_{REF}$

TL/F/5269-4

FIGURE 4. Basic PLL Frequency Synthesizer

In applications where the output frequency desired exceeds the maximum clock frequency of available programmable dividers, a common solution is to add a prescaler preceding the programmable divider, as shown in *Figure 5*. In this case $f_{OUT} = N (M \times f_{REF})$ and so the output frequency step size becomes $M \times f_{REF}$. So, while this technique allows higher frequency operation, it does so at the expense of either increased channel spacing for a given reference frequency, or decreased reference frequency if a specific channel spacing is required. This latter limitation is often undesirable as it can cause increased lock-on time, decreased scanning rates, and sidebands at undesirable frequencies.

Figure 6 shows the basic dual-modulus scheme. Here, a dual-modulus prescaler is substituted for the fixed prescaler and the modulus is controlled by programmable counters. The advantage to this approach is that the step size is again equal to the reference frequency while the prescaling still allows the programmable counters to operate at lower frequencies. As in the fixed prescale technique, only the prescaler needs to be high speed. The DS8906/7/8 prescale by 7/8 for AM and in a similar fashion by 63/64 in FM.



$f_{IN} = f_{REF}$

$f_{IN} = \frac{f_{OUT}}{N \times M}$

$\frac{f_{OUT}}{N \times M} = f_{REF}$

$f_{OUT} = (N \times M) f_{REF}$

$f_{OUT} = N (M \times f_{REF}) \rightarrow f_{STEP} = M \times f_{REF}$

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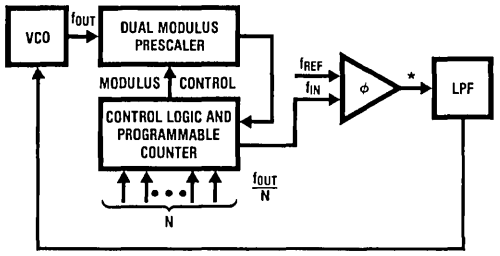
FIGURE 5. PLL Frequency Synthesizer with Fixed Prescaler



$f_{IN} = \frac{f_{OUT}}{N} = f_{REF}$

$f_{OUT} = N \times f_{REF} \rightarrow f_{STEP} = f_{REF}$

*if $f_{REF} = f_{IN}$, then "tuned"
if $f_{REF} \neq f_{IN}$, then "not tuned"

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FIGURE 6. Basic Dual-Modulus Frequency Synthesizer

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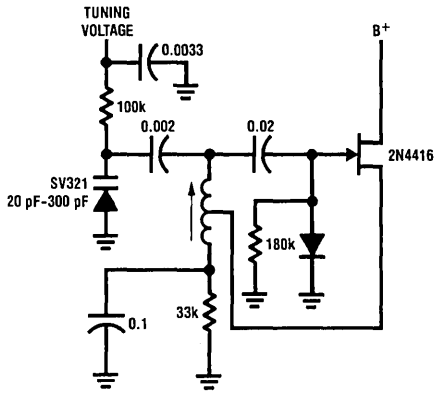
II. Application Hints

VOLTAGE CONTROLLED OSCILLATORS

In all radio and television applications, the voltage controlled oscillator (VCO) is a varactor tuned, LC type of circuit. The LC circuit is used over the various RC current controlled circuits because of their superior noise characteristics. *Figure 7* shows a collection of popular VCOs used in radio and television tuners. The AM VCO is a Hartley design chosen for wide tuning range. Commonly used varactors will show a capacitance change of 350 pF at 1V to 20 pF at 8V, which if used in a low capacitance oscillator circuit, can produce a tuning range approaching 3 to 1.

In the higher frequency ranges, above 50 MHz, Colpitts oscillators are used because stray circuit capacitance will be in parallel with desired feedback capacitance and not cause undesirable spurious resonances that might occur with the tapped coil Hartley design. The FM VCO shown is a grounded base design with feedback from collector to emitter. A UHF television oscillator is also shown. It too is a grounded base oscillator, but using a transmission line as the resonant element instead of a coil. The transmission line and tuning capacitors are arranged in π network which offers improved noise characteristics over a parallel tuned circuit. This circuit will tune over almost an octave.

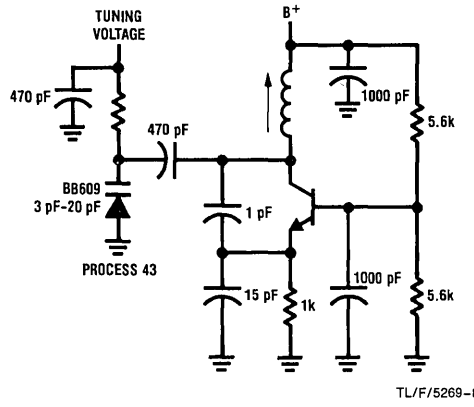
Hartley Oscillator



TL/F/5269–7

50 kHz ~ 15 MHz VCO
Tuning range ≅ 3:1

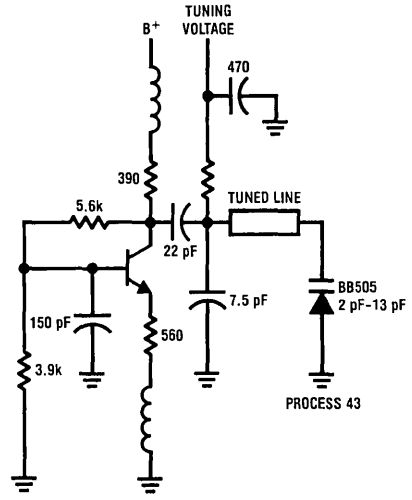
Colpitts Oscillator



TL/F/5269–8

50 MHz ~ 300 MHz VCO
Tuning range ≅ 2:1

Colpitts Oscillator



TL/F/5269–9

500 MHz ~ 1000 MHz VCO
Tuning range ≅ 1.8:1

FIGURE 7. Typical VCO Circuits (Typical Values Shown)

PLL LOOP FILTER CALCULATIONS

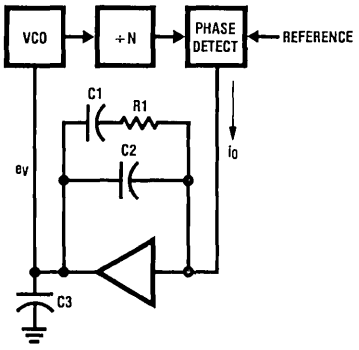
Andrzej Przedpelski, in two articles published in Electronic Design (#19, Sept. 13, 1978 and #10, May 10, 1978) explains how to calculate the three time constants associated with a third order type 2 loop which is typically used with the DS8906/7/8 series. *Figure 8* explains his method and shows a sample calculation. His articles illustrate how to calculate three time constants, and plot open loop gain and phase, and closed loop noise response.

It should be noted that VCO gain, K_V, is in terms of radians per second per volt, and phase detector gain, K_D, is in terms of amps per radian. The phase detector gain for the DS8906/7/8 series is $\pm I_{OUT}$ divided by 4π.

Figure 9 illustrates an example calculation of time constants, and a plot of open loop gain and phase based on the preceding analysis.

REFERENCES

1. Manassewitsch V., *"Frequency Synthesizers"* (Wiley, New York, 1976)
2. Rohde, A. L., *"Digital PLL Frequency Synthesizers"* (Prentice Hall, Englewood Cliffs, 1983)
3. Egan, W. F., *"Frequency Synthesis By Phase Lock"* (Wiley, New York, 1981)



$T1 = R1C1$

$T1 = R1C2$

$$\frac{e_V}{I_O} = \frac{1+ST1}{SC1\,(1+ST2)}$$

$$G(S) = \frac{K_D K_V}{NS^2C1}\left(\frac{1+ST1}{1+ST2}\right)$$

$$T2 = \frac{1-\tan\phi\cos\phi}{\omega_O\cos\phi}$$

$$T1 = \frac{1}{\omega_O{}^2T2}$$

$$C1 = \frac{K_D K_V}{N\omega_O{}^2}\left(\frac{-\omega_O T1-1}{\omega_O T2+1}\right)$$

where θ = desired phase margin

ω_O = loop natural frequency

$\approx$ closed loop bandwidth

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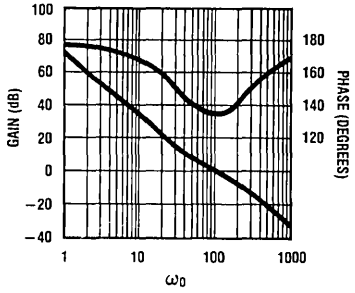
Note: DS8909 op amp required C3 $\approx$ 1000 pF for compensation.

FIGURE 8. Third Order Type 2 Loop



VHF loop, running at 100 MHz, ref = 10 kHz

K_V = 2.5 MHz/V = 15.7 Mrad/sec/V

$$K_D = \frac{400\ \mu A}{4\pi} = 31.8\ \mu A/\text{radian}$$

$$N = \frac{100\ MHz}{10\ kHz} = 10{,}000,\ \omega_O = 2\pi \times 100\ Hz$$

θ = 45° (desired phase margin)

$T2 = 6.6 \times 10^{-4}$ sec

$T1 = 3.84 \times 10^{-3}$ sec

$C1 = 0.3\ \mu F$

so $R1 = T1/C1 = 13\ k\Omega$

$C2 = T2/R1 = 0.05\ \mu F$

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FIGURE 9. Example of Gain and Phase Calculation

DUAL-MODULUS COUNTING RANGE LIMITATIONS

- Minimum count limitations
- Maximum count limitations

The DS8906/7/8 series PLLs utilize a dual-modulus counting scheme internally based on a 63/64 prescale modulus in FM mode in order that all of the U.S. FM frequency assignments could be reached using a 25 kHz reference. The counter modulus N = 64A + B where B is the 6 least significant bits of N and A is the 7th and greater significant bits of N.

$$N = 64A + B$$
$$N = 64A + \overline{63} - B \quad (B = 63 - \overline{B})$$
$$1 + N = 64A + 63 + 1 - 64\overline{B} + 63\overline{B}$$
$$1 + N = 64(A + 1 - \overline{B}) + 63\overline{B}$$

The last equation is in the final form used internally by the DS8906/7/8. The equation indicates that, if N is loaded into the device, it will solve for N + 1.

The minimum continuous N modulus (code) the equation dictates should occur when A = $\overline{B}$. $\overline{B}$ maximum = 63 implies A = $\overline{62}$, B = 63 should be an illegal N + 1 code (N + 1 = 3969). However, because this is just inside the lower FM band limits, extra circuitry was added to enable this particular code's operation. The actual minimum N + 1 code for these PLLs thus becomes the case when A = 61, $\overline{B}$ = 61, N + 1 minimum = 3907. There are legitimate N + 1 codes below this 3907 value, however, they are not continuous. (i.e., Starting at 3907 and counting down, one additional code is in error every 63 codes. Thereafter, these erroneous codes are the cases where A < $\overline{B}$.) The sequence of illegal codes is shown in *Figure 10*.

Loaded Value of N	A	$\overline{B}$	Status	Actual Locked N + 1 Value
3906	61	61	OK	3907
3905	61	62	illegal	3907
3904	61	63	illegal	3907
3903	60	0	OK	3904
•	•	•	•	•
•	•	•	•	•
•	•	•	•	•
3843	60	60	OK	3844
3842	60	61	illegal	3844
3841	60	62	illegal	3844
3840	60	63	illegal	3844
3839	59	0	OK	3840
•	•	•	•	•
•	•	•	•	•
•	•	•	•	•
3780	59	59	OK	3781
3779	59	60	illegal	3781
3778	59	61	illegal	3781
3777	59	62	illegal	3781
3776	59	63	illegal	3781
3775	58	0	OK	3776
•	•	•	•	•
•	•	•	•	•
•	•	•	•	•
3717	58	58	OK	3718
3716	58	59	illegal	3718
3715	58	59	illegal	3718
3714	58	60	illegal	3718
3713	58	61	illegal	3718
3712	58	63	illegal	3718
3711	57	0	OK	3712
•	•	•	•	•
•	•	•	•	•
•	•	•	•	•

FIGURE 10. FM Mode Dual-Modulus Counting Below the Minimum Continuous N Code of 3906

Maximum code limits for these dual-modulus PLLs are determined by the N code bit length. The DS8906 and DS8908 have a 14-bit N counter allowing 16,383 counts. The DS8907 has a 13-bit N node length, allowing a maximum N count of 8,191. See *Figure 11* for table operating ranges of the DS8906, DS8907 and DS8908 PLLs.

CONCLUSION

The major application for the DS8906/7/8 PLLs are synthesizers for AM-FM radios, and have been widely accepted in the marketplace. *Figure 12* shows the block diagram of such a radio. In this application the following performance relating to the PLL tuning system is realized.

PLL Loop Bandwidth	300 Hz
Reference Frequency Sidebands	>60 dB
Signal-to-Noise Ratio	
AM: 30% modulation	>50 dB
FM: 22.5 kHz deviation	>55 dB
Switching Speed (one channel)	<1.5 ms

Product	Input	Ref (Hz)	f_{IN} (Hz)	
			Min*	Max
DS8906	AM	500	24.5k	8.193M
	FM	12.5k	48.8375M	120M
DS8907	AM	10k	490k	15M
	FM	25k	97.675M	120M
DS8908	AM	1k	49k	15M
		9k	441k	15M
		10k	490k	15M
		20k	980k	15M
	FM	1k	3.907M	15M
		9k	35.163M	120M
		10k	39.07M	120M
		20k	78.14M	120M

*The minimum frequency shown is obtained when the minimum continuous N code is utilized and it assumes the edge rates >20V/μs.

FIGURE 11. Product Operating Frequency Range

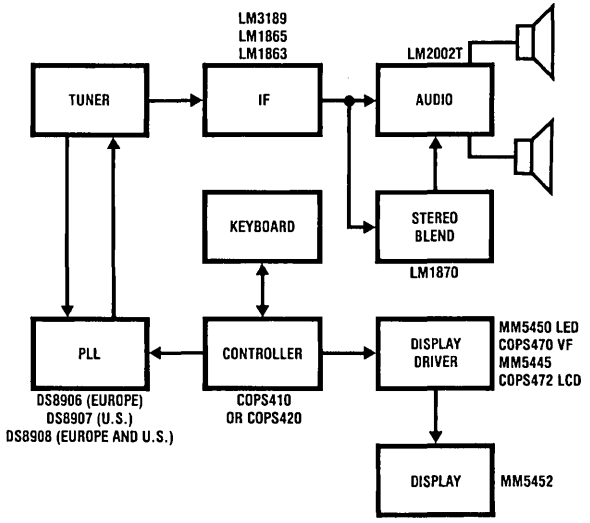

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FIGURE 12. AM-FM Digitally Tuned Radio System

Section 9

Appendices/ Physical Dimensions

Section Contents

Application Note Index

Technical Terms and Definitions

CURRENT

High-Level Input Current, I_{IH}

The current into* an input when a high-level voltage is applied to that input.

Input Current at Maximum Input Voltage, I_I

The current into* an input when maximum specified input voltage is applied.

Low-Level Input Current, I_{IL}

The current into* an input when a low-level voltage is applied to that input.

Low-Level Input Current HiZ, I_{ILZ}

The current into* an input when a low-level voltage is applied to the input with the device in the TRI-STATE condition.

High-Level Output Current, I_{OH}

The current into* an output with input conditions applied that, according to the product specification, will establish a logic high level at the output.

Low-Level Output Current, I_{OL}

The current into* an output with input conditions applied that, according to the product specification, will establish a logic low level at the output.

Off-State Output Current, I_O (I_{CEX})

The current flowing into* an output with input conditions applied that, according to the product specification, will cause the output switching element to be in the off state.

NOTE: This parameter is usually specified for open-collector outputs intended to drive devices other than logic circuits at a specified voltage usually greater then the V_{CC} supply.

Output Current of a TRI-STATE Device, I_{OZ}

The current into* a TRI-STATE output having input conditions applied that, according to the product specification, will establish the high-impedance state at the output.

Short-Circuit Output Current, I_{OS}

The current into* an output when that output is short-circuited to ground or any other specified potential, with input conditions applied to establish the output logic level farthest from ground potential or any other specified potential.

Supply Current, I_{CCH}

The current into* the V_{CC} supply terminal of an integrated circuit when the outputs are in a logic high state.

Supply Current, I_{CCL}

The current into* the V_{CC} supply terminal of an integrated circuit when the outputs are in a logic low state.

VOLTAGE

High-Level Input Voltage, V_{IH}

An input voltage within the more positive (less negative) of the two ranges of values used to represent the binary variables.

NOTE: A minimum is specified that is the least positive value of high-level input voltage for which operation of the logic element within specification limits is guaranteed.

*Current out of a terminal is given as a negative value.

Low-Level Input Voltage, V_{IL}

An input voltage level within the less positive (more negative) of the two ranges of values used to represent the binary variables.

NOTE: A maximum is specified that is the .nost positive value of low-level input voltage for which operation of the logic element within specification limits is guaranteed.

Positive-Going Threshold Voltage, V_{TH}

The voltage level at a transition-operated input that, causes operation of the logic element according to specification, as the input voltage rises from a level below the negative-going threshold voltage, V_{TL}.

Negative-Going Threshold Voltage, V_{TL}

The voltage level at a transition-operated input that, causes operation of the logic element according to specification, as the input voltage falls from a level above the positive-going threshold voltage, V_{TH}.

Hysteresis, V_{HYS}

The absolute difference in voltage value between the positive going threshold and negative going threshold.

Input Clamp Voltage, V_{IK}

An input voltage in a region of relatively low differential resistance that serves to limit the input voltage swing.

High-Level Output Voltage, V_{OH}

The voltage at an output terminal with input conditions applied that, according to the product specification, will establish a logic high level at the output.

Low-Level Output Voltage, V_{OL}

The voltage at an output terminal with input conditions applied that, according to the product specification, will establish a logic low level at the output.

Off-State Output Voltage, $V_{O(off)}$

The voltage at an output terminal with input conditions applied that, according to the product specification, will cause the output switching element to be in the off state.

NOTE: This characteristic is usually specified only for the outputs not having internal pull-up elements.

On-State Output Voltage, $V_{O(on)}$

The voltage at an output terminal with input conditions applied that, according to the product specification, will cause the output switching element to be in the on-state.

Output Clamp Voltage, V_{OK}

An output voltage in a region of low differential resistance that serves to limit the voltage swing.

PROPAGATION TIME

Propagation Delay Time, t_{PD}

The time between the specified reference points on the input and output voltage waveforms with the output changing from one logic level (high or low) to the other logic level.

Technical Terms and Definitions (Continued)

Propagation Delay Time, Low-to-High-Level Output, t_{PLH}

The time between the specified reference points on the input and output voltage waveforms with the output changing from the logic low level to the logic high level.

Propagation Delay Time, High-to-Low-Level Output, t_{PHL}

The time between the specified reference points on the input and output voltage waveforms with the output changing from the logic high level to the logic low level.

Transition Time LOW to HIGH, t_{TLH}

The time between two specified reference points on a waveform, normally specified between the 10% and 90% points, that is changing from LOW to HIGH.

Transition Time HIGH to LOW, t_{THL}

The time between two specified reference points on a waveform, normally specified between the 90% and 10% points, that is changing from HIGH to LOW.

TRI-STATE DELAYS

Output Enable Time, t_{PZL}

The propagation delay time between the specified reference points on the input and output voltage waveforms with the TRI-STATE output changing from a high-impedance (off) state to the logic low level.

Output Enable Time, t_{PZH}

The propagation delay time between the specified reference points on the input and output voltage waveforms with the TRI-STATE output changing from a high-impedance (off) state to the logic high level.

Output Disable Time, t_{PLZ}

The propagation delay time between the specified reference points on the input and output voltage waveforms with the TRI-STATE output changing from the logic low level to a high-impedance (off) state.

Output Disable Time, t_{PHZ}

The propagation delay time between the specified reference points on the input and output voltage waveforms with the TRI-STATE output changing from the logic high level to a high-impedance (off) state.

CLOCK FREQUENCY

Maximum Clock Frequency, f_{MAX}

The highest rate at which the clock input of a bistable circuit can be driven through its required sequence while maintaining stable transitions of logic level at the output with input conditions established that should cause changes of output logic level in accordance with the specification.

PULSE WIDTH

Pulse Width, t_W

The time interval between specified reference points on the leading and trailing edges of the pulse waveform.

SETUP AND HOLD TIME

Setup Time, t_{SU}

The time interval between the application of a signal that is maintained at a specified input terminal prior to a consecutive active transition at another specified input terminal.

Note 1: The setup time is defined as the time between two events and may be insufficient to accomplish the setup. A minimum value is specified that is the shortest interval for which proper operation of the logic element is guaranteed.

Note 2: The setup time may have a negative value in which case the minimum limit defines the longest interval of time between the active transition and the application of the other signal for which proper operation of the logic element is guaranteed.

Hold Time, t_h

The interval during which a signal is maintained at a specified input terminal after an active transition occurs at another specified input terminal.

Note 1: The hold time is defined as the time between two events and may be insufficient to accomplish the intended result. A minimum value is specified that is the shortest interval of time for which proper operation of the logic element is guaranteed.

Note 2: The hold time may have a negative value in which case the minimum limit defines the longest interval of time between the release of data and the active transition on the specified input for which proper operation of the logic element is guaranteed.

TRUTH TABLE EXPLANATIONS

Symbols generally associated with Functional Truth Tables.

H	= Logic high level (steady-state)
L	= Logic low level (steady-state)
↗	= Transition from a logic low to high level
↘	= Transition from a logic high to low level
X	= irrelevant (any input, including transitions)
Z	= off state (high-impedance) of a TRI-STATE output
a..h	= the level of steady-state inputs at inputs A through H respectively
Q_O	= level of Q before the indicated steady-state input conditions were established
$\overline{Q}_O$	= complement of Q_O or level of $\overline{Q}$ before the indicated steady-state input conditions were established
Q_n	= level of Q before the most recent active transition indicated by ↗ or ↘

NOTE: If, in the input columns, a row contains only the symbols H, L, and/or X, this means the indicated output is valid whenever the input configuration is achieved and regardless of the event sequence. The output logic state persists so long as the input configuration is maintained.

If, in the input columns, a row contains (H, L, and/or X) together with ↗ and/or ↘ this means the output is valid whenever the input configuration is achieved. However, the transition(s) must occur following the application of the steady-state levels. If the output is shown as a level (H, L, Q_O or $\overline{Q}_O$), it will be maintained so long as the steady-state input levels and the levels that terminate the defined transitions are maintained. Unless otherwise specified, input transitions in the opposite direction to those shown have no effect on the steady state output.

Interface Cross Reference Guide

National Semiconductor

NATIONAL'S INTERFACE TO AMD

Device Designation	National's Direct Replacement	National's Closest Replacement
AMD		
AM26LS30DC	DS3691J	
AM26LS30PC	DS3691N	
AM26LS31DC	DS26LS31CJ	
AM26LS31PC	DS26LS31CN	
AM26LS32DC	DS26LS32ACJ	DS26LS32CJ
AM26LS32PC	DS26LS32ACN	DS26LS32CN
AM26LS33DC	DS26LS33ACJ	DS26LS33CJ
AM26LS33PC	DS26LS33ACN	DS26LS33CN
AM26S10DC	DS26S10J	
AM26S10PC	DS26S10N	
AM26S11DC	DS26S11J	
AM26S11PC	DS26S11N	
AM26S12DC		DS8838J
AM26S12PC		DS8838N
AM2965DC		DP84240J
AM2965PC		DP84240N
AM2966DC		DP84244J
AM2966PC		DP84244N
N8T26AB	DS8T26AN	
N8T26AF	DS8T26AJ	
N8T28F	DS8T28J	
N8T28N	DS8T28N	
D8212	DP8212J	
P8212	DP8212N	
D8216	DP8216J	
P8216	DP8216N	
D8224	DP8224J	
AM8224PC	DP8224N	
D8226	DP8226J	
P8226	DP8226N	
AM8228PC	DP8228N	
D8228	DP8228J	
AM8238PC	DP8238N	
D8238	DP8238J	
DP8303J	DP8303J	
DP8303N	DP8303N	
DP8304BJ	DP8304BJ	
DP8304BN	DP8304BN	
DP8307J	DP8307J	
DP8307N	DP8307N	
DP8308J	DP8308J	
DP8308N	DP8308N	
DS8838J	DS8838J	
DS8838N	DS8838N	

The manufacturer's most current data sheets take precedence over this guide.

Interface Cross Reference Guide (Continued)

National Semiconductor

Device Designation	National's Direct Replacement	National's Closest Replacement
FAIRCHILD		
μA1488DC	DS1488J	
μA1488PC	DS1488N	
μA1489ADC	DS1489AJ	
μA1489APC	DS1489AN	
μA1489DC	DS1489J	
μA1489PC	DS1489N	
μA3680DC	DS3680J	
μA3680PC	DS3680N	
75107ADC	DS75107J	
75107APC	DS75107N	
75107BDC		DS75107J
75107BPC		DS75107N
75108ADC	DS75108J	
75108APC	DS75108N	
75108BDC		DS75108J
75108BPC		DS75108N
75150RC	DS75150J-8	
75150TC	DS75150N	
75154DC	DS75154J	
75154PC	DS75154N	
75450BDC	DS75450J	
75450BPC	DS75450N	
75451ARC	DS75451J-8	
75451ATC	DS75451N	
75451BRC	DS75451J-8	
75451BTC	DS75451N	
75452ARC	DS75452J-8	
75452ATC	DS75452N	
75452BRC	DS75452J-8	
75452BTC	DS75452N	
75453ARC	DS75453J-8	
75453ATC	DS75453N	
75453BRC	DS75453J-8	
75453BTC	DS75453N	
75461RC	DS75461J-8	
75461TC	DS75461N	
75462RC	DS75462J-8	
75462TC	DS75462N	
75471TC		DS3611N
75472TC		DS3612N
75491PC	DS75491N	
75492PC	DS75492N	
75492APC		DS75492N
μA8T26ADC	DS8T26AJ	
μA8T26APC	DS8T26AN	
μA8T28DC	DS8T28J	
μA8T28PC	DS8T28N	
9614DC	DS75114J	
9614PC	DS75114N	
9615DC	DS75115J	
9615PC	DS75115N	
9616DC		DS1488J
9616PC		DS1488N
9617DC		DS1489AJ
9617DC		DS1489J
9617PC		DS75154N
9636ARC		DS3691J
9636ATC		DS3691N
9637ARC		DS3486J
9637ATC		DS3486N
9640DC	DS26S10J	
9640PC	DS26S10N	
9643PC		DS75322N
9643TC		DS75322N
9645DC		DS3245J
9645PC		DS3245N

The manufacturer's most current data sheets take precedence over this guide.

Interface Cross Reference Guide (Continued)

National Semiconductor

Device Designation	National's Direct Replacement	National's Closest Replacement
MMI		
74S408N	DP8408N	
74S409N	DP8409N	
74S780N	DP8400N	

The manufacturer's most current data sheets take precedence over this guide.

NATIONAL'S INTERFACE TO MMI

Interface Cross Reference Guide (Continued)

National Semiconductor

Device Designation	National's Direct Replacement	National's Closest Replacement
INTEL		
D3245	DS3245J	
D8212	DP8212J	
P8212	DP8212N	
D8216	DP8216J	
P8216	DP8216N	
D8224	DP8224J	
D8224	DP8224N	
D8226	DP8226J	
P8226	DP8226N	
D8228	DP8228J	
D8228	DP8228N	
D8238	DP8238J	
P8238	DP8238N	
D8286	DP8304BJ	
P8286	DP8304BN	
D8287	DP8303J	
P8287	DP8303N	

The manufacturer's most current data sheets take precedence over this guide.

Interface Cross Reference Guide (Continued)

National Semiconductor

NATIONAL'S INTERFACE TO MOTOROLA

Device Designation	National's Direct Replacement	National's Closest Replacement
MOTOROLA		
MMH0026CG	DS0026CH	DS0026CG
MMH0026CL	DS0026CJ	
MMH0026CN	DS0026CN	
MMH0026CP1	DS0026CN	
MMH0026G	DS0026H	
MMH0026L	DS0026J	
MC12015P	DS8615N	
MC12016P	DS8616N	
MC12017P	DS8617N	
MC12071P	DS8621N	
MC1472P1		DS3612N
MC1472P1		DS3632N
MC1472U		DS3612J-8
MC1472U		DS3632J-8
MC1488L	DS1488J	
MC1488P	DS1488N	
MC1489AL	DS1489AJ	
MC1489AP	DS1489AN	
MC1489L	DS1489J	
MC1489P	DS1489N	
AM26LS31DC	DS26LS31CJ	
AM26LS31PC	DS26LS31CN	
MC26S10L	DS26S10J	
MC26S10P	DS26S10N	
MC3430L	DS3651J	
MC3430P	DS3651N	
MC3431L		DS3651J
MC3431P		DS3651N
MC3432L	DS3653J	
MC3432P	DS3653N	
MC3433L		DS3653J
MC3433P		DS3653N
MC3437L	DS8837J	
MC3437P	DS8837N	
MC3438L	DS8838J	
MC3438P	DS8838N	
MC3450L		DS3650J
MC3450P		DS3650N
MC3451P		DS3451N
MC3452P	DS3652N	
MC3486L	DS3486J	
MC3486P	DS3486N	
MC3487L	DS3487J	
MC3487P	DS3487N	
MC3490P		DS8887N
MC3491P		DS8889N
MC3494P		DS8897N
MC6880AL	DS8T26AJ	
MC6880AP	DS8T26AN	
MC6889L	DS8T28J	
MC6889P	DS8T28N	
MC75107L	DS75107J	
MC75107P	DS75107N	
MC75108L	DS75108J	
MC75108P	DS75108N	
MC75125L	DS75125J	
MC75125P	DS75125N	
MC75127L	DS75127J	
MC75127P	DS75127N	
MC75128L	DS75128J	
MC75128P	DS75128N	
MC75129L	DS75129J	
MC75129P	DS75129N	
MC75325L	DS75325J	
MC75491P	DS75491N	
MC75492P	DS75492N	
MC8T13L	DS75121J	
MC8T13P	DS75121N	
MC8T14L	DS75122J	
MC8T14P	DS75122N	
MC8T23L	DS75123J	
MC8T23P	DS75123N	
MC8T24L	DS75124J	
MC8T24P	DS75124N	
MC8T26AL	DS8T26AJ	DS8834J
MC8T26AP	DS8T26AN	DS8834N
MC8T28L	DS8T28J	
MC8T28P	DS8T28N	
DS8641N	DS8641N	
DS8641J	DS8641N	

The manufacturer's most current data sheets take precedence over this guide.

Interface Cross Reference Guide (Continued)

National Semiconductor

Device Designation	National's Direct Replacement	National's Closest Replacement
SIGNETICS		
MC1488F	DS1488J	
MC1488N	DS1488N	
MC1489AN	DS1489AN	
MC1489AF	DS1489AJ	
MC1489F	DS1489J	
MC1489N	DS1489N	
NE582F		DS75494J
NE582N		DS75494N
75S107F		DS75107J
75S107N		DS75107N
75S108F		DS75108J
75S108N		DS75108N
75S207F		DS75207J
75S207N		DS75207N
75S208F		DS75208J
75S208N		DS75208N
N8T13F	DS75121J	
N8T13N	DS75121N	
N8T14F	DS75122J	
N8T14N	DS75122N	
N8T15F		DS75150J-8
N8T15N		DS75150N
N8T23F	DS75123J	
N8T23N	DS75123N	
N8T24F	DS75124J	
N8T24N	DS75124N	
N8T26AF	DS8T26AJ	
N8T26AN	DS8T26AN	
N8T28F	DS8T28J	
N8T28N	DS8T28N	
N8T34F	DS8834J	
N8T34N	DS8834N	
N8T37F	DS8837J	
N8T37N	DS8837N	
N8T38F	DS8838J	
N8T38N	DS8838N	
N8T380F	DS8836J	DS8640J
N8T380N	DS8836N	DS8640N
*DS8820AF	DS8820AJ	
*DS8820AN	DS8820AN	
*DS8820F	DS8820J	
*DS8820N	DS8820N	
*DS8830F	DS8830J	
*DS8830N	DS8830N	
*DS8880F	DS8880J	
*DS8880N	DS8880N	

The manufacturer's most current data sheets take precedence over this guide.

*Signetics has announced plans to obsolete these products.

Interface Cross Reference Guide (Continued)

National Semiconductor

NATIONAL'S INTERFACE TO SPRAGUE

Device Designation	National's Direct Replacement	National's Closest Replacement
SPRAGUE		
UDN3611H	DS3611J-8	
UDN3611M	DS3611N	
UDN3612H	DS3612J-8	
UDN3612M	DS3612N	
UDN3613H	DS3613J-8	
UDN3613M	DS3613N	
UDN3614H	DS3614J-8	
UDN3614M	DS3614N	

The manufacturer's most current data sheets take precedence over this guide.

Interface Cross Reference Guide (Continued)

National Semiconductor

Device Designation	National's Direct Replacement	National's Closest Replacement
TEXAS INSTRUMENTS		
MC1488J	DS1488J	
MC1488N	DS1488N	
MC1489AJ	DS1489AJ	
MC1489AN	DS1489AN	
MC1489J	DS1489J	
MC1489N	DS1489N	
AM26LS31CJ	DS26LS31CJ	
AM26LS31CN	DS26LS31CN	
AM26LS32ACJ	DS26LS32ACJ	DS26LS32CJ
AM26LS32ACN	DS26LS32ACN	DS26LS32CN
AM26LS33AJ	DS26LS33ACJ	DS26LS33CJ
AM26LS33AN	DS26LS33ACN	DS26LS33CN
AM26S10CJ	DS26S10J	
AM26S10CN	DS26S10N	
AM26S11CJ	DS26S11J	
AM26S11CN	DS26S11N	
MC3486J	DS3486J	
MC3486N	DS3486N	
MC3487J	DS3487J	
MC3487N	DS3487N	
SN74LS424J	DP8224J	
SN74LS424N	DP8224N	
SN74S412J	DP8212J	
SN74S412N	DP8212N	
SN74S428N	DP8228N	
SN74S436N	DS36149N	
SN74S437N	DS36179N	
SN74S438N	DP8238N	
SN75107AJ		DS75107J
SN75107AN		DS75107N
SN75107BJ	DS75107J	
SN75107BN	DS75107N	
SN75108AJ		DS75108J
SN75108AN		DS75108N
SN75108BJ	DS75108J	
SN75108BN	DS75108N	
SN75113J	DS75113J	
SN75113N	DS75113N	
SN75114J	DS75114J	
SN75114N	DS75114N	
SN75115J	DS75115J	
SN75115N	DS75115N	
SN75121J	DS75121J	
SN75121N	DS75121N	
SN75122J	DS75122J	
SN75122N	DS75122N	
SN75123J	DS75123J	
SN75123N	DS75123N	
SN75124J	DS75124J	
SN75124N	DS75124N	
SN75125J	DS75125J	
SN75125N	DS75125N	
SN75127J	DS75127J	
SN75127N	DS75127N	
SN75128J	DS75128J	
SN75128N	DS75128N	
SN75129J	DS75129J	
SN75129N	DS75129N	
SN75150J	DS75150J-8	
SN75150N	DS75150N	
SN75154J	DS75154J	
SN75154N	DS75154N	
SN75160N	DS75160AN	
SN75160AN	DS75160AN	
SN75161N	DS75161AN	
SN75161AN	DS75161AN	
SN75162N	DS75162AN	
SN75162AN	DS75162AN	
SN75176A	DS75176A	
SN75176A	DS3695	
SN75182J	DS8820AJ	
SN75182N	DS8820AN	
SN75183J	DS8830J	
SN75183N	DS8830N	
SN75188J	DS1488J	
SN75188N	DS1488N	
SN75189AJ	DS1489AJ	
SN75189AN	DS1489AN	
SN75189J	DS1489J	
SN75189N	DS1489N	
SN75207BN	DS75207N	
SN75207J		DS75207J
SN75208BJ	DS75208J	
SN75208J		DS75208J
SN75208N		DS75208N
SN75325J	DS75325J	
SN75325N	DS75325N	
SN75361AJG	DS75361J-8	
SN75361AP	DS75361N	
SN75365J	DS75365J	
SN75365N	DS75365N	
SN75369J		DS0026CJ-8
SN75369N		DS0026CN
SN75437ANE	DS3658N	
SN75437NE	DS3658N	
SN75438NE	DS3658N	
SN75450BJ	DS75450J	
SN75450BN	DS75450N	
SN75451BJG	DS75451J-8	
SN75451BP	DS75451N	
SN75452BJG	DS75452J-8	
SN75452BP	DS75452N	
SN75453BJG	DS75453J-8	
SN75453BP	DS75453N	
SN75454BJG	DS75454J-8	
SN75454BP	DS75454N	
SN75461JG	DS75461J-8	
SN75461P	DS75461N	
SN75462JG	DS75462J-8	
SN75462P	DS75462N	
SN75463JG	DS75463J-8	
SN75463P	DS75463N	
SN75464JG	DS75464J-8	
SN75464P	DS75464N	
SN75471JG		DS3611J-8
SN75471P		DS3611N
SN75472JG		DS3612J-8
SN75472P		DS3612N
SN75473JG		DS3613J-8
SN75473P		DS3613N
SN75474JG		DS3614J-8
SN75474P		DS3614N
SN75477JG		DS3612J-8
SN75477P		DS3612N
SN75480N	DS8880N	
SN75491AN		DS75491N
SN75491N	DS75491N	
SN75492AN		DS75492N
SN75492J	DS75492J	
SN75492N	DS75492N	
SN75494N		DS75494N
N8T13J	DS75121J	
N8T13N	DS75121N	
N8T14J	DS75122J	
N8T14N	DS75122N	
N8T23J	DS75123J	
N8T23N	DS75123N	
N8T24J	DS75124J	
N8T24N	DS75124N	
N8T26AJ	DS8T26AJ	
N8T26AN	DS8T26AN	
DS8820AJ	DS8820AJ	
DS8820AN	DS8820AN	
DS8830J	DS8830J	
DS8830N	DS8830N	
DS8831J	DS8831J	
DS8831N	DS8831N	
DS8832J	DS8832J	
DS8832N	DS8832N	

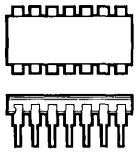
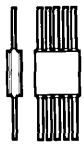
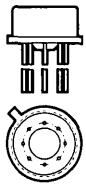
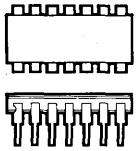
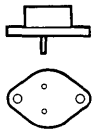
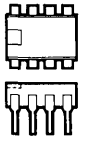
The manufacturer's most current data sheets take precedence over this guide.

TEXAS INSTRUMENTS TO NATIONAL'S INTERFACE

9

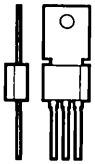
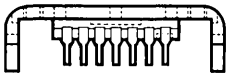
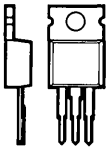
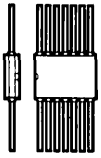
National Semiconductor

Industry Package Cross-Reference Guide

	NSC	Signetics	Fairchild	Motorola	TI	RCA	Silicon General	AMD	Raytheon
 14/16 Lead Glass/Metal DIP	D	I	D	L		D	D	D	D, M
 Glass/Metal Flat-Pack	F	Q	F	F	F, S	K	F	F	J, F, Q
 TO-99, TO-100, TO-5	H	T, K, L, DB	H	G	L	S*, V1**	T	H	T, H
 8, 14 and 16-Lead Low-Temperature Ceramic DIP	J	F	R, D	U	J				DC, DD
 TO-3 (Steel)	K			KS			K		K
TO-3 (Aluminum)	KC	DA	K	K	K		K		LK, TK
 8, 14 and 16-Lead Plastic DIP	N	V, A, B	T, P	P	P, N	E	M, N	PC	N, DN, DP, MP

*With dual-in-line formed leads.

**With radially formed leads.

	NSC	Signetics	Fairchild	Motorola	TI	RCA	Silicon General	AMD	Raytheon
 TO-202 (D-40, Durawatt)	P				KD				
 "SGS" Type Power DIP	S		BP						
 TO-220	T	U	U		KC				
 Low Temperature Glass Hermetic Flat Pack	W		F	F	W			FM	
 TO-92 (Plastic)	Z	S	W	P	LP				

Military Aerospace Programs from National Semiconductor

This appendix is intended to provide a brief overview of military products available from National Semiconductor. For further information, refer to our *1986 Reliability Handbook* which is expected to be available by mid 1986.

MIL-M-38510

The MIL-M-38510 Program, which is sometimes called the JAN IC Program, is administered by the Defense Electronics Supply Center (DESC). The purpose of this program is to provide the military community with standardized products that have been manufactured and screened to government-controlled specifications in government certified facilities. All 38510 manufacturers must be formally qualified and their products listed on DESC's Qualified Products List (QPL) before devices can be marked and shipped as JAN product.

There are two processing levels specified within MIL-M-38510: Classes S and B. Class S is typically specified for space flight applications, while Class B is used for aircraft and ground systems. National is a major supplier of both classes of devices. Screening requirements are outlined in Table III.

Tables I and II explain the JAN device marking system.

Copies of MIL-M-38510, the QPL, and other related documents may be obtained from:

Naval Publications and Forms Center
5801 Tabor Avenue
Philadelphia, PA 19120
(212) 697-2179

DESC Specifications

DESC specifications are issued to provide standardized versions of devices which are not yet available as JAN product. MIL-STD-883 Class B screening is coupled with tightly controlled electrical specifications which have been written to allow a manufacturer to use his standard electrical tests. A current listing of National's DESC specification offerings can be obtained from our franchised distributors, sales representatives, or DESC. DESC is located in Dayton, Ohio.

MIL-STD-883

Although originally intended to establish uniform test methods and procedures, MIL-STD-883 has also become the general specification for non-JAN military product. Revision C of this document defines the minimum requirements for a device to be marked and advertised as 883-compliant. Included are design and construction criteria, documentation controls, electrical and mechanical screening requirements, and quality control procedures. Details can be found in paragraph 1.2.1 of MIL-STD-883.

National offers both 883 Class B and 883 Class S product. The screening requirements for both classes of product are outlined in Table III.

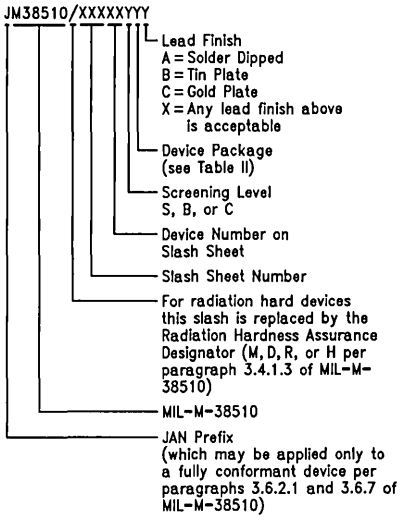
As with DESC specifications, a manufacturer is allowed to use his standard electrical tests provided that all critical parameters are tested. Also, the electrical test parameters, test conditions, test limits, and test temperatures must be clearly documented. At National Semiconductor, this information is available via our RETS (Reliability Electrical Test Specification Program). The RETS document is a complete description of the electrical tests performed and is controlled by our QA department. Individual copies are available upon request.

Some of National's older products are not completely compliant with MIL-STD-883, but are still required for use in military systems. These devices are screened to the same stringent requirements as 883 product, but are marked "-MIL".

Military Screening Program (MSP)

National's Military Screening Program was developed to make screened versions of advanced products such as gate arrays and microprocessors available more quickly than is possible for JAN and 883 devices. Through this program, screened product is made available for prototypes and breadboards prior to or during the JAN or 883 qualification activities. MSP products receive the 100% screening of Table III, but are not subjected to Group C and D quality conformance testing. Other criteria such as electrical testing and temperature range will vary depending upon individual device status and capability.

TABLE I. The MIL-M-38510 Part Marking



CI24-1

TABLE II. JAN Package Codes

38510 Package Designation	Microcircuit Industry Description
A	14-Pin 1/4" X 1/4" (metal) flat pack
B	14-Pin 3/16" X 1/4" flat pack
C	14-Pin 1/4" X 3/4" dual-in-line
D	14-Pin 1/4" X 3/8" (ceramic) flat pack
E	16-Pin 1/4" X 3/8" dual-in-line
F	16-Pin 1/4" X 3/8" (metal or ceramic) flat pack
G	8-pin TO-99 can or header
H	10-pin 1/4" x 1/4" (metal) flat pack
I	10-pin TO-100 can or header
J	24-pin 1/2" x 1-1/4" dual-in-line
K	24-pin 3/8" x 5/8" flat pack
L	24-pin 1/4" x 1-1/4" dual-in-line
M	12-pin TO-101 can or header
N	Note 1
P	8-pin 1/4" x 3/8" dual-in-line
Q	40-pin 3/16" x 2-1/16" dual-in-line
R	20-pin 1/4" x 1-1/16" dual-in-line
S	20-pin 1/4" x 1/2" flat pack
T	Note 1
U	Note 1
V	18-pin 3/8" x 15/16" dual-in-line
W	22-pin 3/8" x 1-1/8" dual-in-line
X	Note 1
Y	Note 1
Z	Note 1
2	20-terminal 0.350" x 0.350" chip carrier
3	28-terminal 0.450" x 0.450" chip carrier

Note 1: These letters are assigned to packages by individual detail specifications and may be assigned to different packages in different specifications.

TABLE III. 100% Screening Requirements

Screen	Class S		Class B	
	Method	Reqmt	Method	Reqmt
1. Wafer Lot Acceptance	5007	All Lots		- - -
2. Nondestructive Bond Pull	2023	100%		— —
3. Internal Visual (Note 1)	2010, Condition A	100%	2010, Condition B	100%
4. Stabilization Bake	1008, Condition C, 24 hrs. Min.	100%	1008, Condition C, 24 hrs. Min.	100%
5. Temp. Cycling (Note 2)	1010, Condition C	100%	1010, Condition C	100%
6. Constant Acceleration	2001, Condition E (Min.) Y_1 Orientation Only	100%	2001, Condition E, (Min.), Y_1 Orientation Only	100%
7. Visual Inspection (Note 3)		100%		100%
8. Particle Impact Noise Detection (PIND)	2020, Condition A (Note 4)	100%		— —
9. Serialization	(Note 5)	100%		— —
10. Interim (Pre-Burn-In) Electrical Parameters	Per Applicable Device Specification (Note 13)	100%	Per Applicable Device Specification (Note 6)	— —
11. Burn-In Test	1015 240 Hrs. @ 125°C Min. (Cond. F Not Allowed)	100%	1015 160 Hrs. @ 125°C Min.	100%
12. Interim (Post-Burn-In) Electrical Parameters	Per Applicable Device Specification (Note 13)	100%		
13. Reverse Bias Burn-In (Note 7)	1015; Test Condition A, C, 72 Hrs. @ 150°C Min. (Cond. F Not Allowed)	100%		— —
15. PDA Calculation	5% Parametric (Note 14), 3% Functional −25°C	All Lots	5% Parametric (Note 14)	All Lots
16. Final Electrical Test a) Static Tests	Per Applicable Device Specification		Per Applicable Device Specification	
1) 25°C (Subgroup 1, Table I, 5005)		100%		100%
2) Max & Min Rated Operating Temp. (Subgroups 2, 3, Table I, 5005)		100%		100%
b) Dynamic Tests & Switching Tests, 25°C (Subgroups 4, 9, Table I, 5005)		100%		100%
c) Functional Test, 25°C (Subgroup 7, Table I, 5005)		100%		100%

TABLE III. 100% Screening Requirements (Continued)

Screen	Class S		Class B	
	Method	**Reqmt**	**Method**	**Reqmt**
17. Seal Fine, Gross	1014	100%, (Note 8)	1014	100%, (Note 9)
18. Radiographic (Note 10)	2012 Two Views	100%		— —
19. Qualification or Quality Conformance Inspection Test Sample Selection	(Note 11)	Samp.	(Note 11)	Samp.
20. External Visual (Note 12)	2009	100%		100%

Note 1: Unless otherwise specified, at the manufacturer's option, test samples for Group B, bond strength (Method 5005) may be randomly selected prior to or following internal visual (Method 5004), prior to sealing provided all other specification requirements are satisfied (e.g. bond strength requirements shall apply to each inspection lot, bond failures shall be counted even if the bond would have failed internal visual).

Note 2: For Class B devices, this test may be replaced with thermal shock method 1011, test condition A, minimum.

Note 3: At the manufacturer's option, visual inspection for catastrophic failures may be conducted after each of the thermal/mechanical screens, after the sequence or after seal test. Catastrophic failures are defined as missing leads, broken packages, or lids off.

Note 4: The PIND test may be performed in any sequence after step 6 and prior to step 16. See MIL-M-38510, paragraph 4.6.3.

Note 5: Class S devices shall be serialized prior to interim electrical parameter measurements.

Note 6: When specified, all devices shall be tested for those parameters requiring delta calculations.

Note 7: Reverse bias burn-in is a requirement only when specified in the applicable device specification. The order of performing burn-in and reverse bias burn-in may be inverted.

Note 8: For Class S devices, the seal test may be performed in any sequence between step 16 and step 19, but it shall be performed after all shearing and forming operations on the terminals.

Note 9: For Class B devices, the fine and gross seal tests shall be performed separate or together in any sequence and order between step 6 and step 20 except that they shall be performed after all shearing and forming operations on the terminals. When 100% seal screen cannot be performed after shearing and forming (e.g. flatpacks and chip carriers) the seal screen shall be done 100% prior to these operations and a sample test (LTPD = 5) shall be performed on each inspection lot following these operations. If the sample fails, 100% rescreening shall be required.

Note 10: The radiographic screen may be performed in any sequence after step 19.

Note 11: Samples shall be selected for testing in accordance with the specific device class and lot requirements of Method 5005

Note 12: External Visual shall be performed on the lot any time after step 19 and prior to shipment.

Note 13: Read and Record when past burn-in delta measurements are specified.

Note 14: PDA shall apply to all static, dynamic, functional, and switching measurements at either 25°C or maximum rated operating temperature.

National's A+ Program

A+ Program: A comprehensive program that utilizes National's experience gained from participation in the many Military/Aerospace programs.

A program that not only assures high quality but also increases the reliability of molded integrated circuits.

The A+ program is intended for users who need better than usual incoming quality and higher reliability levels for their standard integrated circuits.

Users who specify A+ processed parts will find that the program:

- Eliminates incoming electrical inspection.
- Eliminates the need for, and thus the added cost of, independent testing laboratories.
- Reduces the cost of reworking assembled boards.
- Reduces field failures.
- Reduces equipment down time.
- Reduces the need for excess inventories due to yield loss incurred as a result of processing performed at independent testing laboratories.

The A+ Program Saves You Money

It is a widely accepted fact that down-time of equipment is costly not only in lost hours of machine usage but also costly in the repair and maintenance cycle. One of the added advantages of the A+ program is the burn-in screen, which is one of the most effective screening procedures in the semiconductor industry. Failure rates as a result of the burn-in can be decreased many times. The objective of burn-in is to stress the device much higher than it would be stressed during normal usage.

Reliability vs. Quality

The words "reliability" and "quality" are often used interchangeably, as though they connoted identical facets of a product's merit. But reliability and quality are different, and IC users must understand the essential difference between the two concepts in order to evaluate properly the various vendors' programs for products improvement that are generally available, and National's A+ program in particular.

The concept of quality gives us information about the population and faulty IC devices among good devices, and generally relates to the number of faulty devices that arrive at a user's plant. But looked at in another way, quality can instead relate to the number of faulty ICs that escape detection at the IC vendor's plant.

It is the function of a vendor's Quality Control arm to monitor the degree of success of that vendor in reducing the number of faulty ICs that escape detection. Quality Control does this by testing the outgoing parts on a sampled basis. The Acceptable Quality level (AQL) in turn determines the stringency of the sampling. As the AQL decreases it becomes more difficult for defective parts to escape detection, thus the quality of the shipped parts increases.

The concept of reliability, on the other hand, refers to how well a part that is initially good will withstand its environment. Reliability is measured by the percentage of parts that fail in a given period of time.

Thus the difference between quality and reliability means the ICs of high quality may, in fact be of low reliability, while those of low quality may be of high reliability.

Improving the Reliability of Shipped Parts

The most important factor that affects a part's reliability is its construction; the materials used and the method by which they are assembled.

Reliability cannot be tested into a part. Still, there are tests and procedures that an IC vendor can implement which will subject the IC to stresses in excess of those that it will endure in actual use, and which will eliminate marginal, short-life parts.

In any test of reliability the weaker parts will normally fail first. Further, stress tests will accelerate, or shorten, the time of failure of the weak parts. Because the stress tests cause weak parts to fail prior to shipment to the user, the population of shipped parts will in fact demonstrate a higher reliability in use.

National's A+ Program

National provides the A+ program as the best practical approach to maximum quality and reliability on molded devices. The following flow chart shows how we do it step by step.

SEM

Randomly selected wafers are taken from production regularly and subjected to SEM analysis.

Epoxy B Processing for All Molded Parts

At National, all molded semiconductors, including ICs, have been built by this process for some time now. All processing steps, inspections, and QC monitoring are designed to provide highly reliable products. (A reliability report is available that gives, in detail, the background of Epoxy B, the reason for its selection at National, and reliability data that proves its success.)

Six Hour, 150°C Bake

This stress places the die bond and all wire bonds into a combined tensile and shear stress mode, and helps eliminate marginal bonds and electrical connections.

Five Temperature Cycles (70°C to 100°C)

Exercising each device over a 100°C temperature range provides an additional die and package stress.

National's A+ Program (Continued)

High Temperature (100°C) Functional Electrical Test

A high temperature test with voltages applied places the die under the most severe stress possible. The test is actually performed at 100°C—15°C higher than the commercial ambient limit. All devices are thoroughly exercised at the 100°C ambient.

Electrical Testing

Every device is tested at 25°C for functional and DC parameters.

Burn-In Test

Each device is burned-in for 160 hours at a minimum junction temperature of +125°C or under equivalent conditions of time and temperature, as established by a time-temperature regression curve based on 0.96 eV activation energy. All burn-in done under steady-state conditions unless otherwise specified.

DC Functional and Parametric Tests

These room-temperature functional and parametric tests are the normal, final tests through which all National products pass.

Thermal Shock Monitor

Samples from each package type are selected at random each week and submitted to cycles of liquid to liquid thermal shock −65°C to +150°C. In addition, samples are selected every four weeks and subjected to 2000 temperature cycles of 0°C to +25°C.

Tighter-Than-Normal QC Inspection Plans

Most vendors sample inspect outgoing parts to a 0.3% AQL. When you specify the A+ program, we sample your parts to a 0.035% AQL at room temperature and 0.05% AQL at T_A Max. This eight times tightening (from 0.3 to 0.035% AQL) coupled with three 100% electrical tests, dramatically reduces the number of "escapes" and allows us to guarantee the AQLs listed below.

Ship Parts

Here are the QC sample plans used in our A+ test program:

Test	Temperature	AQL
Electrical Functionality	25°C	0.035%
Parametric, DC	25°C	
Parametric, AC	25°C	0.1%
Electrical Functionality	At each temperature extreme.	0.05%
Parametric, DC		
Mechanical		
Critical	—	0.01%
Major	—	0.28%

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INTUITIVE IC CMOS EVOLUTION—1984

Thomas M. Frederiksen's new book targets some of the most significant transitions in semiconductor technology since the change from germanium to silicon. *Intuitive IC CMOS Evolution* highlights the transition in the reduction in defect densities and the development of new circuit topologies. The author's latest book is a vital aid to engineers, and industry observers who need to stay abreast of the semiconductor industry.

INTUITIVE IC OP AMPS—1984

Thomas M. Frederiksen's new book, *Intuitive IC Op Amps,* explores the many uses and applications of different IC op amps. Frederiksen's detailed book differs from others in the way he focuses on the intuitive groundwork in the basic functioning concepts of the op amp. Mr. Frederiksen's latest book is a vital aid to engineers, designers, and industry observers who need to stay abreast of the computer industry.

LINEAR APPLICATIONS HANDBOOK—1986

The purpose of this handbook is to provide a fully indexed and cross-referenced collection of linear integrated circuit applications using both monolithic and hybrid circuits from National Semiconductor.

Individual application notes are normally written to explain the operation and use of one particular device or to detail various methods of accomplishing a given function. The organization of this handbook takes advantage of this innate coherence by keeping each application note intact, arranging them in numerical order, and providing a detailed Subject Index.

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Peripheral Control Components

Understanding Integrated Circuit Package Power Capabilities

National Semiconductor Corp.
Application Note 336
Charles Carinalli
Josip Huljev

INTRODUCTION

The short and long term reliability of National Semiconductor's interface circuits, like any integrated circuit, is very dependent on its environmental condition. Beyond the mechanical/environmental factors, nothing has a greater influence on this reliability than the electrical and thermal stress seen by the integrated circuit. Both of these stress issues are specifically addressed on every interface circuit data sheet, under the headings of Absolute Maximum Ratings and Recommended Operating Conditions.

However, through application calls, it has become clear that electrical stress conditions are generally more understood than the thermal stress conditions. Understanding the importance of electrical stress should never be reduced, but clearly, a higher focus and understanding must be placed on thermal stress. Thermal stress and its application to interface circuits from National Semiconductor is the subject of this application note.

FACTORS AFFECTING DEVICE RELIABILITY

Figure 1 shows the well known "bathtub" curve plotting failure rate versus time. Similar to all system hardware (mechanical or electrical) the reliability of interface integrated circuits conform to this curve. The key issues associated with this curve are infant mortality, failure rate, and useful life.

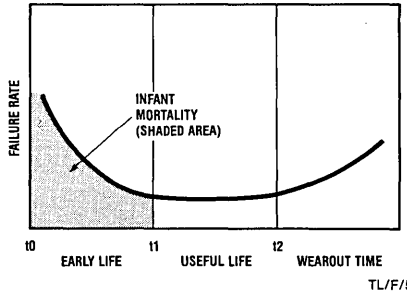

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FIGURE 1. Failure Rate vs Time

Infant mortality, the high failure rate from time t0 to t1 (early life), is greatly influenced by system stress conditions other than temperature, and can vary widely from one application to another. The main stress factors that contribute to infant mortality are electrical transients and noise, mechanical maltreatment and excessive temperatures. Most of these failures are discovered in device test, burn-in, card assembly and handling, and initial system test and operation. Although important, much literature is available on the subject of infant mortality in integrated circuits and is beyond the scope of this application note.

Failure rate is the number of devices that will be expected to fail in a given period of time (such as, per million hours). The mean time between failure (MTBF) is the average time (in hours) that will be expected to elapse after a unit has failed before the next unit failure will occur. These two primary "units of measure" for device reliability are inversely related:

$$\text{MTBF} = \frac{1}{\text{Failure Rate}}$$

Although the "bathtub" curve plots the overall failure rate versus time, the useful failure rate can be defined as the percentage of devices that fail per-unit-time during the flat portion of the curve. This area, called the useful life, extends between t1 and t2 or from the end of infant mortality to the onset of wearout. The useful life may be as short as several years but usually extends for decades if adequate design margins are used in the development of a system.

Many factors influence useful life including: pressure, mechanical stress, thermal cycling, and electrical stress. However, die temperature during the device's useful life plays an equally important role in triggering the onset of wearout.

FAILURE RATES vs TIME AND TEMPERATURE

The relationship between integrated circuit failure rates and time and temperature is a well established fact. The occurrence of these failures is a function which can be represented by the Arrhenius Model. Well validated and predominantly used for accelerated life testing of integrated circuits, the Arrhenius Model assumes the degradation of a performance parameter is linear with time and that MTBF is a function of temperature stress. The temperature dependence is an exponential function that defines the probability of occurrence. This results in a formula for expressing the lifetime or MTBF at a given temperature stress in relation to another MTBF at a different temperature. The ratio of these two MTBFs is called the acceleration factor F and is defined by the following equation:

$$F = \frac{X1}{X2} = \exp\left[\frac{E}{K}\left(\frac{1}{T2} - \frac{1}{T1}\right)\right]$$

Where: X1 = Failure rate at junction temperature T1
X2 = Failure rate at junction temperature T2
T = Junction temperature in degrees Kelvin
E = Thermal activation energy in electron volts (ev)
K = Boltzman's constant

However, the dramatic acceleration effect of junction temperature (chip temperature) on failure rate is illustrated in a plot of the above equation for three different activation energies in *Figure 2*. This graph clearly demonstrates the importance of the relationship of junction temperature to device failure rate. For example, using the 0.99 ev line, a 30° rise in junction temperature, say from 130°C to 160°C, results in a 10 to 1 increase in failure rate.

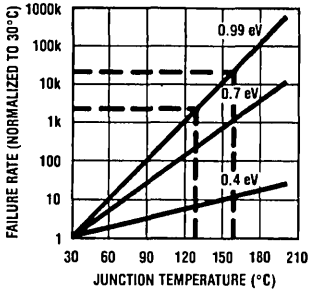

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FIGURE 2. Failure Rate as a Function of Junction Temperature

DEVICE THERMAL CAPABILITIES

There are many factors which affect the thermal capability of an integrated circuit. To understand these we need to understand the predominant paths for heat to transfer out of the integrated circuit package. This is illustrated by *Figures 3* and *4*.

Figure 3 shows a cross-sectional view of an assembled integrated circuit mounted into a printed circuit board.

Figure 4 is a flow chart showing how the heat generated at the power source, the junctions of the integrated circuit flows from the chip to the ultimate heat sink, the ambient environment. There are two predominant paths. The first is from the die to the die attach pad to the surrounding package material to the package lead frame to the printed circuit board and then to the ambient. The second path is from the package directly to the ambient air.

Improving the thermal characteristics of any stage in the flow chart of *Figure 4* will result in an improvement in device thermal characteristics. However, grouping all these characteristics into one equation determining the overall thermal capability of an integrated circuit/package/environmental condition is possible. The equation that expresses this relationship is:

$$T_J = T_A + P_D (\theta_{JA})$$

Where: T_J = Die junction temperature

T_A = Ambient temperature in the vicinity device

P_D = Total power dissipation (in watts)

θ_{JA} = Thermal resistance junction-to-ambient

θ_{JA}, the thermal resistance from device junction-to-ambient temperature, is measured and specified by the manufacturers of integrated circuits. National Semiconductor utilizes special vehicles and methods to measure and monitor this parameter. All interface circuit data sheets specify the thermal characteristics and capabilities of the packages available for a given device under specific conditions—these package power ratings directly relate to thermal resistance junction-to-ambient or θ_{JA}.

Although National provides these thermal ratings, it is critical that the end user understand how to use these numbers to improve thermal characteristics in the development of his system using interface components.

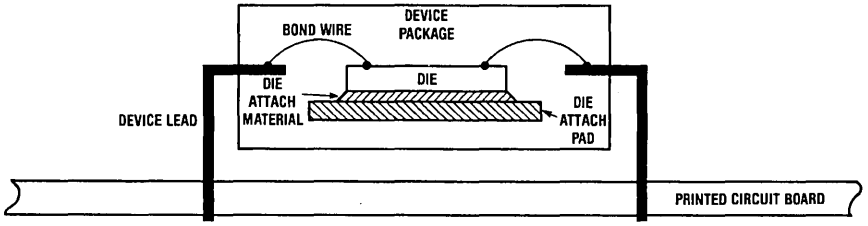

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FIGURE 3. Integrated Circuit Soldered into a Printed Circuit Board (Cross-Sectional View)

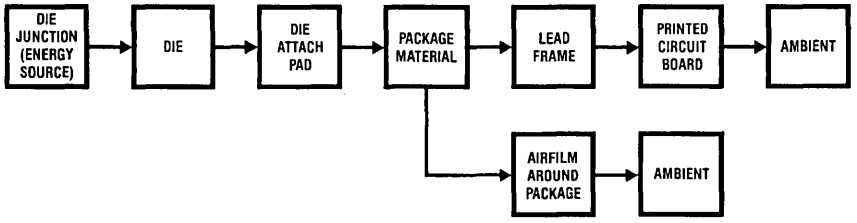

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FIGURE 4. Thermal Flow (Predominant Paths)

DETERMINING DEVICE OPERATING JUNCTION TEMPERATURE

From the above equation the method of determining actual worst-case device operating junction temperature becomes straightforward. Given a package thermal characteristic, θ_{JA}, worst-case ambient operating temperature, T_A(max), the only unknown parameter is device power dissipation, P_D. In calculating this parameter, the dissipation of the integrated circuit due to its own supply has to be considered, the dissipation within the package due to the external load must also be added. The power associated with the load in a dynamic (switching) situation must also be considered. For example, the power associated with an inductor or a capacitor in a static versus dynamic (say, 1 MHz) condition is significantly different.

The junction temperature of a device with a total package power of 600 mW at 70°C in a package with a thermal resistance of 63°C/W is 108°C.

$$T_J = 70°C + (63°C/W) \times (0.6W) = 108°C$$

The next obvious question is, "how safe is 108°C?"

MAXIMUM ALLOWABLE JUNCTION TEMPERATURES

What is an acceptable maximum operating junction temperature is in itself somewhat of a difficult question to answer. Many companies have established their own standards based on corporate policy. However, the semiconductor industry has developed some defacto standards based on the device package type. These have been well accepted as numbers that relate to reasonable (acceptable) device lifetimes, thus failure rates.

National Semiconductor has adopted these industry-wide standards. For devices fabricated in a molded package, the maximum allowable junction temperature is 150°C. For these devices assembled in ceramic or cavity DIP packages, the maximum allowable junction temperature is 175°C. The numbers are different because of the differences in package types. The thermal strain associated with the die package interface in a cavity package is much less than that exhibited in a molded package where the integrated circuit chip is in direct contact with the package material.

Let us use this new information and our thermal equation to construct a graph which displays the safe thermal (power) operating area for a given package type. *Figure 5* is an example of such a graph. The end points of this graph are easily determined. For a 16-pin molded package, the maximum allowable temperature is 150°C; at this point no power dissipation is allowable. The power capability at 25°C is 1.98W as given by the following calculation:

$$P_D @ 25°C = \frac{T_J(max) - T_A}{\theta_{JA}} = \frac{150°C - 25°C}{63°C/W} = 1.98W$$

The slope of the straight line between these two points is minus the inversion of the thermal resistance. This is referred to as the derating factor.

$$\text{Derating Factor} = -\frac{1}{\theta_{JA}}$$

As mentioned, *Figure 5* is a plot of the safe thermal operating area for a device in a 16-pin molded DIP. As long as the intersection of a vertical line defining the maximum ambient temperature (70°C in our previous example) and maximum device package power (600 mW) remains below the maximum package thermal capability line the junction temperature will remain below 150°C—the limit for a molded package. If the intersection of ambient temperature and package power fails on this line, the maximum junction temperature will be 150°C. Any intersection that occurs above this line will result in a junction temperature in excess of 150°C and is not an appropriate operating condition.

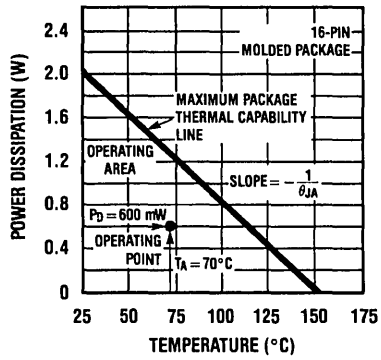

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FIGURE 5. Package Power Capability vs Temperature

The thermal capabilities of all interface circuits are expressed as a power capability at 25°C still air environment with a given derating factor. This simply states, for every degree of ambient temperature rise above 25°C, reduce the package power capability stated by the derating factor which is expressed in mW/°C. For our example—a θ_{JA} of 63°C/W relates to a derating factor of 15.9 mW/°C.

FACTORS INFLUENCING PACKAGE THERMAL RESISTANCE

As discussed earlier, improving any portion of the two primary thermal flow paths will result in an improvement in overall thermal resistance junction-to-ambient. This section discusses those components of thermal resistance that can be influenced by the manufacturer of the integrated circuit. It also discusses those factors in the overall thermal resistance that can be impacted by the end user of the integrated circuit. Understanding these issues will go a long way in understanding chip power capabilities and what can be done to insure the best possible operating conditions and, thus, best overall reliability.

Die Size

Figure 6 shows a graph of our 16-pin DIP thermal resistance as a function of integrated circuit die size. Clearly, as the chip size increases the thermal resistance decreases—this relates directly to having a larger area with which to dissipate a given power.

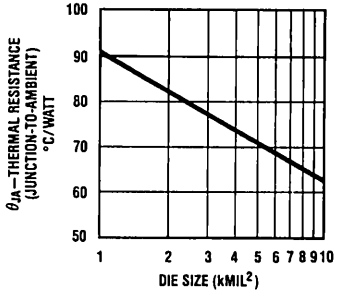

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FIGURE 6. Thermal Resistance vs Die Size

Lead Frame Material

Figure 7 shows the influence of lead frame material (both die attach and device pins) on thermal resistance. This graph compares our same 16-pin DIP with a copper lead frame, a Kovar lead frame, and finally an Alloy 43 type lead frame—these are lead frame materials commonly used in the industry. Obviously the thermal conductivity of the lead frame material has a significant impact in package power capability. Molded interface circuits from National Semiconductor use the copper lead frame exclusively.

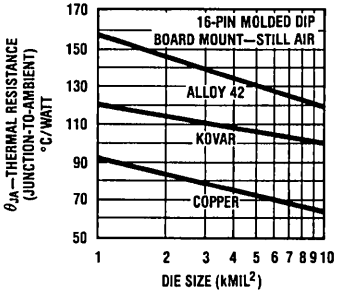

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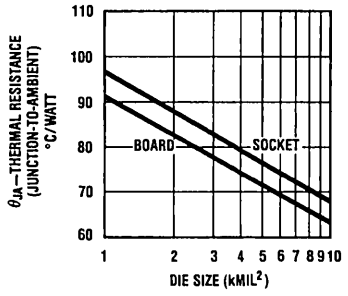
FIGURE 7. Thermal Resistance vs Lead Frame Material

Board vs Socket Mount

One of the major paths of dissipating energy generated by the integrated circuit is through the device leads. As a result of this, the graph of *Figure 8* comes as no surprise. This compares the thermal resistance of our 16-pin package soldered into a printed circuit board (board mount) compared to the same package placed in a socket (socket mount). Adding a socket in the path between the PC board and the device adds another stage in the thermal flow path, thus increasing the overall thermal resistance. The thermal capabilities of National Semiconductor's interface circuits are specified assuming board mount conditions. If the devices are placed in a socket the thermal capabilities should be reduced by approximately 5% to 10%.

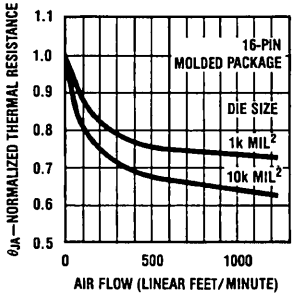


TL/F/5280–8

FIGURE 8. Thermal Resistance vs Board or Socket Mount

Air Flow

When a high power situation exists and the ambient temperature cannot be reduced, the next best thing is to provide air flow in the vicinity of the package. The graph of *Figure 9* illustrates the impact this has on thermal resistance. This graph plots the relative reduction in thermal resistance normalized to the still air condition for our 16-pin molded DIP. The thermal ratings on National Semiconductor's interface circuits data sheets relate to the still air environment.



TL/F/5280–9

FIGURE 9. Thermal Resistance vs Air Flow

Other Factors

A number of other factors influence thermal resistance. The most important of these is using thermal epoxy in mounting ICs to the PC board and heat sinks. Generally these techniques are required only in the very highest of power applications.

Some confusion exists between the difference in thermal resistance junction-to-ambient (θ_{JA}) and thermal resistance junction-to-case (θ_{JC}). The best measure of actual junction temperature is the junction-to-ambient number since nearly all systems operate in an open air environment. The only situation where thermal resistance junction-to-case is important is when the entire system is immersed in a thermal bath and the environmental temperature is indeed the case temperature. This is only used in extreme cases and is the exception to the rule and, for this reason, is not addressed in this application note.

NATIONAL SEMICONDUCTOR PACKAGE CAPABILITIES

Figures 10 and *11* show composite plots of the thermal characteristics of the most common package types in the National Semiconductor Interface Circuits product family. *Figure 10* is a composite of the copper lead frame molded package. *Figure 11* is a composite of the ceramic (cavity) DIP using poly die attach. These graphs represent board mount still air thermal capabilities. Another, and final, thermal resistance trend will be noticed in these graphs. As the number of device pins increase in a DIP the thermal resistance decreases. Referring back to the thermal flow chart, this trend should, by now, be obvious.

RATINGS ON INTERFACE CIRCUITS DATA SHEETS

In conclusion, all National Semiconductor Interface Products define power dissipation (thermal) capability. This information can be found in the Absolute Maximum Ratings section of the data sheet. The thermal information shown in this application note represents average data for characterization of the indicated package. Actual thermal resistance can vary from ±10% to ±15% due to fluctuations in assembly quality, die shape, die thickness, distribution of heat sources on the die, etc. The numbers quoted in the interface data sheets reflect a 15% safety margin from the average numbers found in this application note. Insuring that total package power remains under a specified level will guarantee that the maximum junction temperature will not exceed the package maximum.

The package power ratings are specified as a maximum power at 25°C ambient with an associated derating factor for ambient temperatures above 25°C. It is easy to determine the power capability at an elevated temperature. The power specified at 25°C should be reduced by the derating factor for every degree of ambient temperature above 25°C. For example, in a given product data sheet the following will be found:

Maximum Power Dissipation* at 25°C

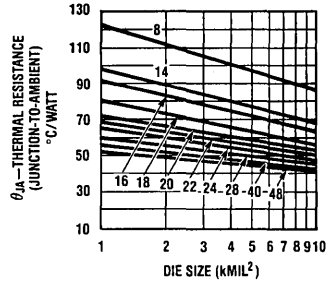
Cavity Package	1509 mW
Molded Package	1476 mW

* Derate cavity package at 10 mW/°C above 25°C; derate molded package at 11.8 mW/°C above 25°C.

If the molded package is used at a maximum ambient temperature of 70°C, the package power capability is 945 mW.

$$P_D \text{ @ } 70°C = 1476 \text{ mW} - (11.8 \text{ mW/°C}) \times (70°C - 25°C)$$
$$= 945 \text{ mW}$$

Molded (N Package) DIP* Copper Leadframe—HTP Die Attach Board Mount—Still Air

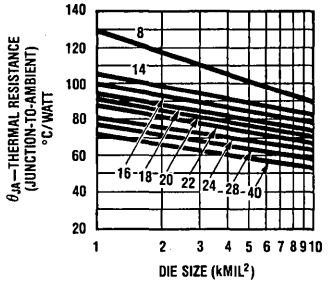


*Packages from 8- to 20-pin 0.3 mil width
22-pin 0.4 mil width
24- to 40-pin 0.6 mil width

TL/F/5280–10

FIGURE 10. Thermal Resistance vs Die Size vs Package Type (Molded Package)

Cavity (J Package) DIP* Poly Die Attach Board Mount—Still Air



*Packages from 8- to 20-pin 0.3 mil width
22-pin 0.4 mil width
24- to 48-pin 0.6 mil width

TL/F/5280–11

FIGURE 11. Thermal Resistance vs Die Size vs Package Type (Cavity Package)

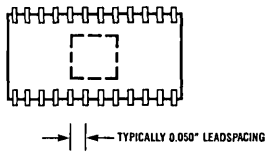
Small Outline (SO) Package Surface Mounting Methods-Parameters and Their Effect on Product Reliabilty

National Semiconductor Corp.
Application Note 450
Josip Huljev
W. K. Boey

The SO (small outline) package has been developed to meet customer demand for ever-increasing miniaturazation and component density.

COMPONENT SIZE COMPARISON

S.O. Package



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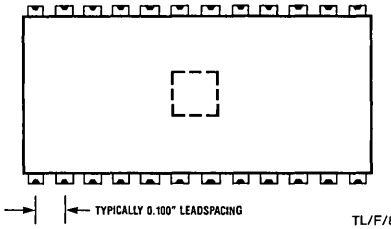
Standard DIP Package



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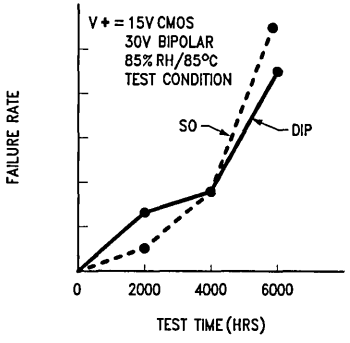
Because of its small size, reliability of the product assembled in SO packages needs to be carefully evaluated.

SO packages at National were internally qualified for production under the condition that they be of comparable reliability performance to a standard dual in line package under all accelerated environmental tests. *Figure A* is a summary of accelarated bias moisture test performance on 30V bipolar and 15V CMOS product assembled in SO and DIP (control) packages.



TL/F/8766–3

FIGURE A

In order to achieve reliability performance comparable to DIPs—SO packages are designed and built with materials and processes that effectively compensate for their small size.

All SO packages tested on 85%RA, 85°C were assembled on PC conversion boards using vapor-phase reflow soldering. With this approach we are able to measure the effect of surface mounting methods on reliability of the process. As illustrated in *Figure A* no significant difference was detected between the long term reliability performance of surface mounted S.O. packages and the DIP control product for up to 6000 hours of accelerated 85%/85°C testing.

SURFACE-MOUNT PROCESS FLOW

The standard process flowcharts for basic surface-mount operation and mixed-lead insertion/surface-mount operations, are illustrated on the following pages.

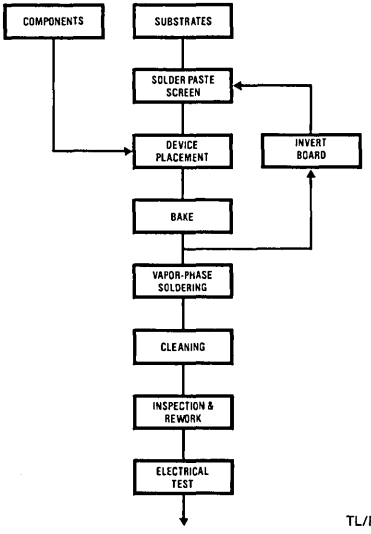
Usual variations encountered by users of SO packages are:

- Single-sided boards, surface-mounted components only.
- Single-sided boards, mixed-lead inserted and surface-mounted components.
- Double-sided boards, surface-mounted components only.
- Double-sided boards, mixed-lead inserted and surface-mounted components.

In consideration of these variations, it became necessary for users to utilize techniques involving wave soldering and adhesive applications, along with the commonly-used vapor-phase solder reflow soldering technique.

PRODUCTION FLOW

Basic Surface-Mount Production Flow



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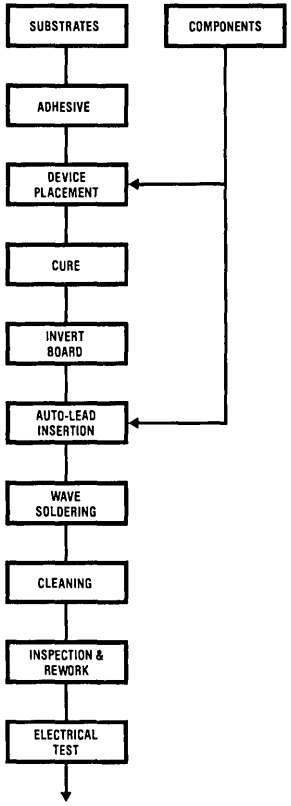
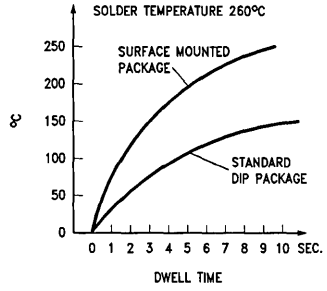
Mixed Surface-Mount and Axial-Leaded Insertion Components Production Flow



TL/F/8766–5

Thermal stress of the packages during surface-mounting processing is more severe than during standard DIP PC board mounting processes. *Figure B* illustrates package temperature versus wave soldering dwell time for surface mounted packages (components are immersed into the molten solder) and the standard DIP wave soldering process. (Only leads of the package are immersed into the molten solder).



TL/F/8766–6

FIGURE B

Figure C is a summary of accelerated bias moisture test performance on the 30V bipolar process.

Group 1 — Standard DIP package

Group 2 — SO packages vapor-phase reflow soldered on PC boards

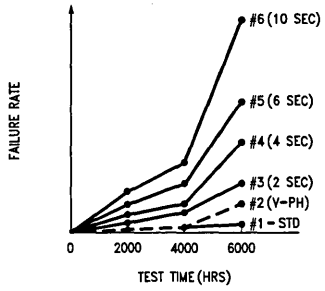
Group 3–6 SO packages wave soldered on PC boards

Group 3 — dwell time 2 seconds

4 — dwell time 4 seconds

5 — dwell time 6 seconds

6 — dwell time 10 seconds



TL/F/8766–7

FIGURE C

It is clear based on the data presented that SO packages soldered onto PC boards with the vapor phase reflow process have the best long term bias moisture performance and this is comparable to the performance of standard DIP packages. The key advantage of reflow soldering methods is the clean environment that minimized the potential for contamination of surface mounted packages, and is preferred for the surface-mount process.

When wave soldering is used to surface mount components on the board, the dwell time of the component under molten solder should be no more than 4 seconds, preferrably under 2 seconds in order to prevent damage to the component. Non-Halide, or (organic acid) fluxes are highly recommended.

PICK AND PLACE

The choice of automatic (all generally programmable) pick-and-place machines to handle surface mounting has grown considerably, and their selection is based on individual needs and degree of sophistication.

The basic component-placement systems available are classified as:

(a) In-line placement

— Fixed placement stations

— Boards indexed under head and respective components placed

(b) Sequential placement

— Either a X-Y moving table system or a θ, X-Y moving pickup system used

—Individual components picked and placed onto boards

(c) Simultaneous placement

— Multiple pickup heads

— Whole array of components placed onto the PCB at the same time

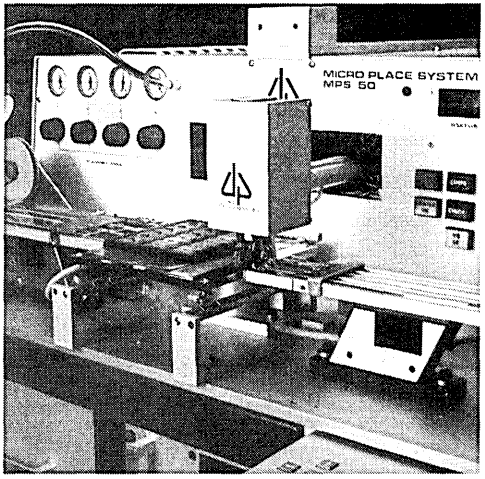
(d) Sequential/simultaneous placement

— X–Y moving table, multiple pickup heads system

— Components placed on PCB by successive or simultaneous actuation of pickup heads

The SO package is treated almost the same as surface-mount, passive components requiring correct orientation in placement on the board.

Pick and Place Action



TL/F/8766–8

BAKE

This is recommended, despite claims made by some solder paste suppliers that this step be omitted.

The functions of this step are:

- Holds down the solder globules during subsequent reflow soldering process and prevents expulsion of small solder balls.
- Acts as an adhesive to hold the components in place during handling between placement to reflow soldering.
- Holds components in position when a double-sided surface-mounted board is held upside down going into a vapor-phase reflow soldering operation.
- Removes solvents which might otherwise contaminate other equipment.
- Initiates activator cleaning of surfaces to be soldered.
- Prevents moisture absorption.

The process is moreover very simple. The usual schedule is about 20 minutes in a 65°C–95°C (dependent on solvent system of solder paste) oven with adequate venting. Longer bake time is not recommended due to the following reasons:

- The flux will degrade and affect the characteristics of the paste.
- Solder globules will begin to oxidize and cause solderability problems.
- The paste will creep and after reflow, may leave behind residues between traces which are difficult to remove and vulnerable to electro-migration problems.

REFLOW SOLDERING

There are various methods for reflowing the solder paste, namely:

- Hot air reflow
- Infrared heating (furnaces)
- Convectional oven heating
- Vapor-phase reflow soldering
- Laser soldering

For SO applications, hot air reflow/infrared furnace may be used for low-volume production or prototype work, but vapor-phase soldering reflow is more efficient for consistency and speed. Oven heating is not recommended because of "hot spots" in the oven and uneven melting may result. Laser soldering is more for specialized applications and requires a great amount of investment.

HOT GAS REFLOW/INFRARED HEATING

A hand-held or table-mount air blower (with appropriate orifice mask) can be used.

The boards are preheated to about 100°C and then subjected to an air jet at about 260°C. This is a slow process and results may be inconsistent due to various heat-sink properties of passive components.

Use of an infrared furnace is the next step to automating the concept, except that the heating is promoted by use of IR lamps or panels. The main objection to this method is that certain materials may heat up at different rates under IR radiation and may result in damage to these components (usually sockets and connectors). This could be minimized by using far-infrared (non-focused) system.

VAPOR-PHASE REFLOW SOLDERING

Currently the most popular and consistent method, vapor-phase soldering utilizes a fluoroinert fluid with excellent heat-transfer properties to heat up components until the solder paste reflows. The maximum temperature is limited by the vapor temperature of the fluid.

The commonly used fluids (supplied by 3M Corp) are:

- FC-70, 215°C vapor (most applications) or FX-38
- FC-71, 253°C vapor (low-lead or tin-plate)

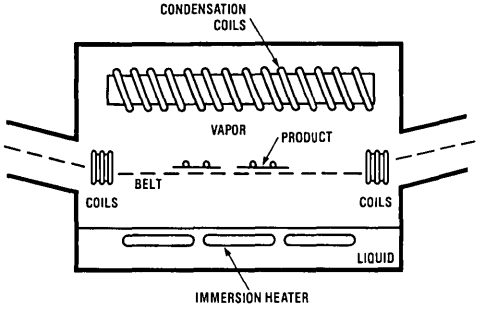
HTC, Concord, CA, manufactures equipment that utilizes this technique, with two options:

- Batch systems, where boards are lowered in a basket and subjected to the vapor from a tank of boiling fluid.
- In-line conveyorized systems, where boards are placed onto a continuous belt which transports them into a concealed tank where they are subjected to an environment of hot vapor.

Dwell time in the vapor is generally on the order of 15–30 seconds (depending on the mass of the boards and the loading density of boards on the belt).

The question of thermal shock is asked frequently because of the relatively sharp increase in component temperature

In-Line Conveyorized Vapor-Phase Soldering



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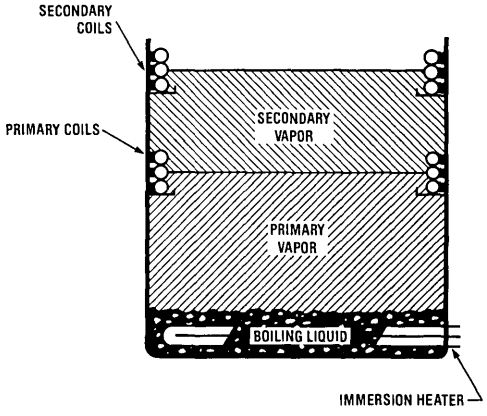
from room temperature to 215°C. SO packages mounted on representative boards have been tested and have shown little effect on the integrity of the packages. Various packages, such as cerdips, metal cans and TO-5 cans with glass seals, have also been tested.

Vapor-Phase Furnace

TL/F/8766–10

Batch-Fed Production Vapor-Phase Soldering Unit



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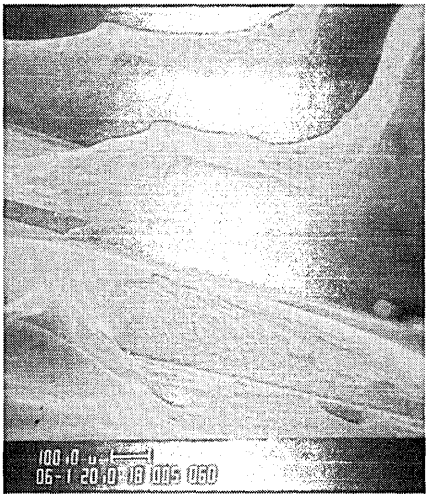
Solder Joints on a SO-14 Package on PCB



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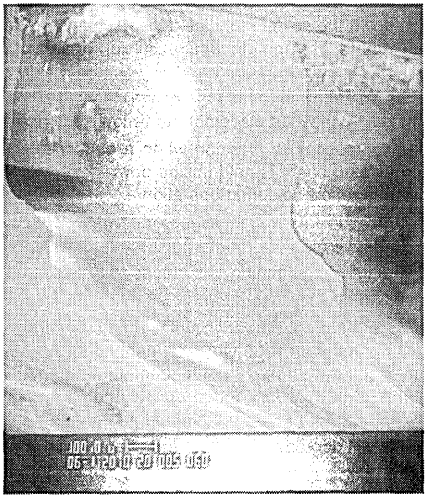
Solder Joints on a SO-14 Package on PCB



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PRINTED CIRCUIT BOARD

The SO package is molded out of clean, thermoset plastic compound and has no particular compatibility problems with most printed circuit board substrates.

The package can be reliably mounted onto substrates such as:

- G10 or FR4 glass/resin
- FR5 glass/resin systems for high-temperature applications
- Polymide boards, also high-temperature applications
- Ceramic substrates

General requirements for printed circuit boards are:

- Mounting pads should be solder-plated whenever applicable.

- Solder masks are commonly used to prevent solder bridging of fine lines during soldering.

  The mask also protects circuits from processing chemical contamination and corrosion.

  If coated over pre-tinned traces, residues may accumulate at the mask/trace interface during subsequent reflow, leading to possible reliability failures.

  Recommended application of solder resist on bare, clean traces prior to coating exposed areas with solder.

  General requirements for solder mask:

  — Good pattern resolution.

  — Complete coverage of circuit lines and resistance to flaking during soldering.

  — Adhesion should be excellent on substrate material to keep off moisture and chemicals.

  — Compatible with soldering and cleaning requirements.

SOLDER PASTE SCREEN PRINTING

With the initial choice of printed circuit lithographic design and substrate material, the first step in surface mounting is the application of solder paste.

The typical lithographic "footprints" for SO packages are illustrated below. Note that the 0.050" lead center-center spacing is not easily managed by commercially-available air pressure, hand-held dispensers.

Using a stainless-steel, wire-mesh screen stencilled with an emulsion image of the substrate pads is by far the most common and well-tried method. The paste is forced through the screen by a V-shaped plastic squeegee in a sweeping manner onto the board placed beneath the screen.

The setup for SO packages has no special requirement from that required by other surface-mounted, passive components. Recommended working specifications are:

- Use stainless-steel, wire-mesh screens, #80 or #120, wire diameter 2.6 mils. Rule of thumb: mesh opening should be approximately 2.5–5 times larger than the average particle size of paste material.
- Use squeegee of Durometer 70.
- Experimentation with squeegee travel speed is recommended, if available on machine used.
- Use solder paste of mesh 200–325.
- Emulsion thickness of 0.005" usually used to achieve a solder paste thickness (wet) of about 0.008" typical.
- Mesh pattern should be 90 degrees, square grid.
- Snap-off height of screen should not exceed $\frac{1}{8}$", to avoid damage to screens and minimize distortion.

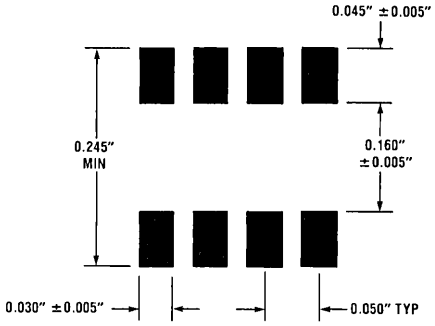
SOLDER PASTE

Selection of solder paste tends to be confusing, due to numerous formulations available from various manufacturers. In general, the following guidelines are sufficient to qualify a particular paste for production:

- Particle sizes (see photographs below). Mesh 325 (approximately 45 microns) should be used for general purposes, while larger (solder globules) particles are preferred for leadless components (LCC). The larger particles can easily be used for SO packages.
- Uniform particle distribution. Solder globules should be spherical in shape with uniform diameters and minimum amount of elongation (visual under 100/200 × magnification). Uneven distribution causes uneven melting and subsequent expulsion of smaller solder balls away from their proper sites.
- Composition, generally 60/40 or 63/37 Sn/Pb. Use 62/36 Sn/Pb with 2% Ag in the presence of Au on the soldering area. This formulation reduces problems of metal leaching from soldering pads.
- RMA flux system usually used.
- Use paste with aproximately 88–90% solids.

RECOMMENDED SOLDER PADS FOR SO PACKAGES

SO-8, SO-14, SO-16



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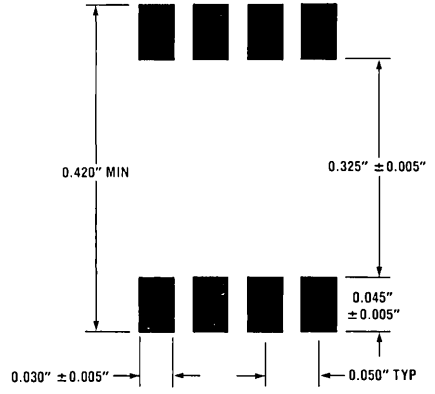
SO-16L, SO-20



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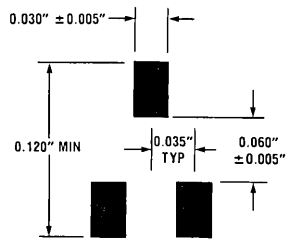
SOT-23



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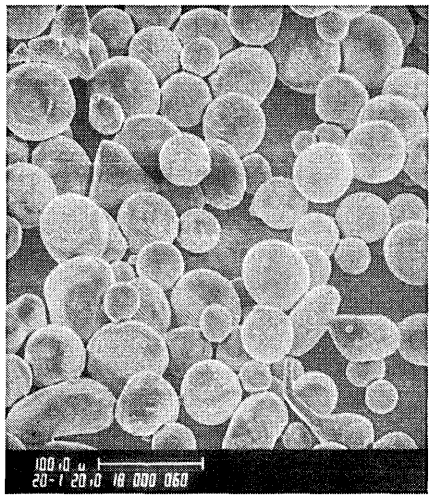
Comparison of Particle Size/Shape of Various Solder Pastes

200 × Alpha (62/36/2)



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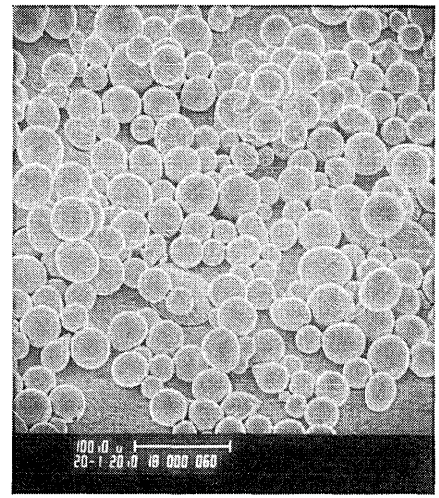
200 × Kester (63/37)



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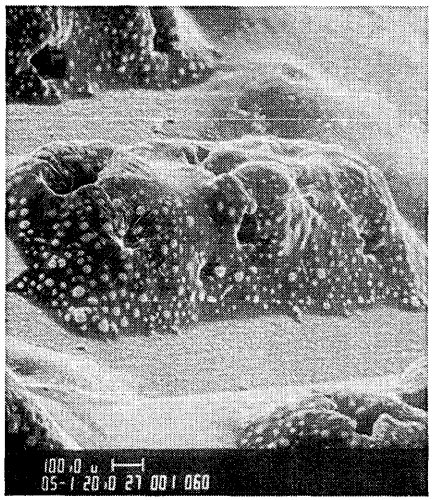
Solder Paste Screen on Pads



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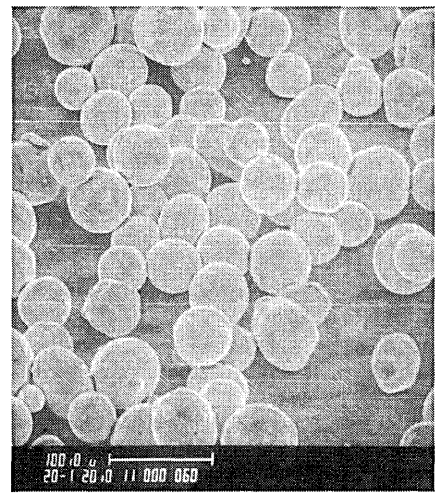
200 × Fry Metal (63/37)



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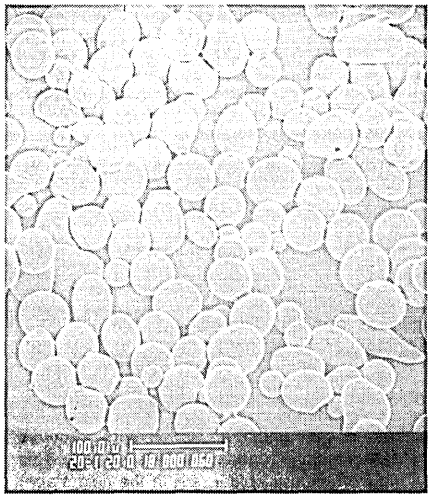
Comparison of Particle Size/Shape of Various Solder Pastes (Continued)

200 ESL (63/37)



TL/F/8766–21

CLEANING

The most critical process in surface mounting SO packages is in the cleaning cycle. The package is mounted very close to the surface of the substrate and has a tendency to collect residue left behind after reflow soldering.

Important considerations in cleaning are:

- Time between soldering and cleaning to be as short as possible. Residue should not be allowed to solidify on the substrate for long periods of time, making it difficult to dislodge.
- A low surface tension solvent (high penetration) should be employed. Solvents commercially available are:

  Freon TMS (general purpose)
  Freon TE35/TP35 (cold-dip cleaning)
  Freon TES (general purpose)

  It should also be noted that these solvents generally will leave the substrate surface hydrophobic (moisture repellent), which is desirable.

  Prelete or 1,1,1-Trichloroethane
  Kester 5120/5121
- A defluxer system which allows the workpiece to be subjected to a solvent vapor, followed by a rinse in pure solvent and a high-pressure spray lance are the basic requirments for low-volume production.
- For volume production, a conveyorized, multiple hot solvent spray/jet system is recommended.
- Rosin, being a natural occurring material, is not readily soluble in solvents, and has long been a stumbling block to the cleaning process. In recent developments, synthetic flux (SA flux), which is readily soluble in Freon TMS solvent, has been developed. This should be explored where permissible.

The dangers of an inadequate cleaning cycle are:

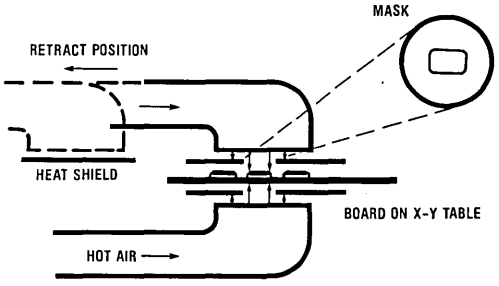
- Ion contamination, where ionic residue left on boards would cause corrosion to metallic components, affecting the performance of the board.
- Electro-migration, where ionic residue and moisture present on electrically-biased boards would cause dentritic growth between close spacing traces on the substrate, resulting in failures (shorts).

REWORK

Should there be a need to replace a component or re-align a previously disturbed component, a hot air system with appropriate orifice masking to protect surrounding components may be used.

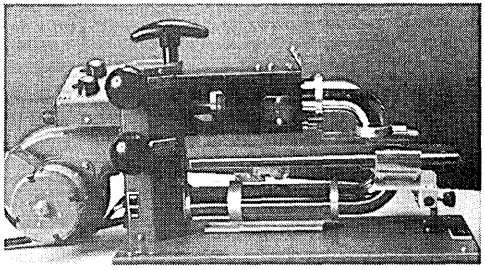
When rework is necessary in the field, specially-designed tweezers that thermally heat the component may be used to remove it from its site. The replacement can be fluxed at the lead tips or, if necessary, solder paste can be dispensed onto the pads using a varimeter. After being placed into position, the solder is reflowed by a hot-air jet or even a standard soldering iron.

Hot-Air Solder Rework Station



TL/F/8766–22

Hot-Air Rework Machine



TL/F/8766–23

WAVE SOLDERING

In a case where lead insertions are made on the same board as surface-mounted components, there is a need to include a wave-soldering operation in the process flow.

Two options are used:

- Surface mounted components are placed and vapor phase reflowed before auto-insertion of remaining components. The board is carried over a standard wave-solder system and the underside of the board (only lead-inserted leads) soldered.
- Surface-mounted components are placed in position, but no solder paste is used. Instead, a drop of adhesive about 5 mils maximum in height with diameter not exceeding 25% width of the package is used to hold down the package. The adhesive is cured and then proceeded to auto-insertion on the reverse side of the board (surface-mounted side facing down). The assembly is then passed over a "dual wave" soldering system. Note that the surface-mounted components are immersed into the molten solder.

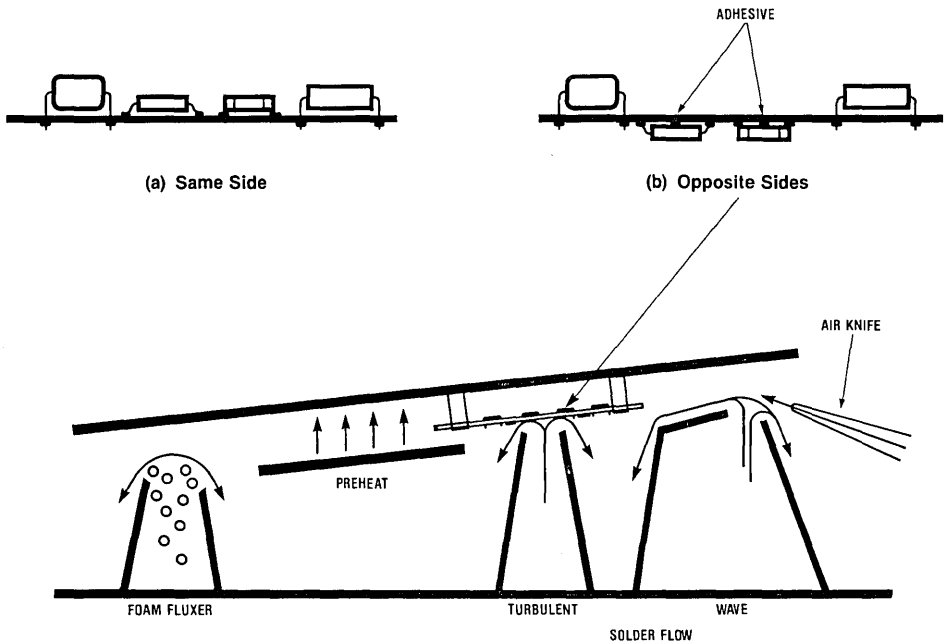
Lead trimming will pose a problem after soldering in the latter case, unless the leads of the insertion components are pre-trimmed or the board specially designed to localize certain areas for easy access to the trim blade.

The controls required for wave soldering are:

- Solder temperature to be 240–260°C. The dwell time of components under molten solder to be short (preferably kept under 2 seconds), to prevent damage to most components and semiconductor devices.
- RMA (Rosin Mildly Activated) flux or more aggressive OA (Organic Acid) flux are applied by either dipping or foam fluxing on boards prior to preheat and soldering. Cleaning procedures are also more difficult (aqueous, when OA flux is used), as the entire board has been treated by flux (unlike solder paste, which is more or less localized). Non-halide OA fluxes are highly recommended.
- Preheating of boards is essential to reduce thermal shock on components. Board should reach a temperature of about 100°C just before entering the solder wave.
- Due to the closer lead spacings (0.050″ vs 0.100″ for dual-in-line packages), bridging of traces by solder could occur. The reduced clearance between packages also causes "shadowing" of some areas, resulting in poor solder coverage. This is minimized by dual-wave solder systems.

A typical dual-wave system is illustrated below, showing the various stages employed. The first wave typically is in turbulence and given a transverse motion (across the motion of the board). This covers areas where "shadowing" occurs. A second wave (usually a broad wave) then proceeds to perform the standard soldering. The departing edge from the solder is such to reduce "icicles," and is still further reduced by an air knife placed close to the final soldering step. This air knife will blow off excess solder (still in the fluid stage) which would otherwise cause shorts (bridging) and solder bumps.

Mixed Surface Mount and Lead Insertion



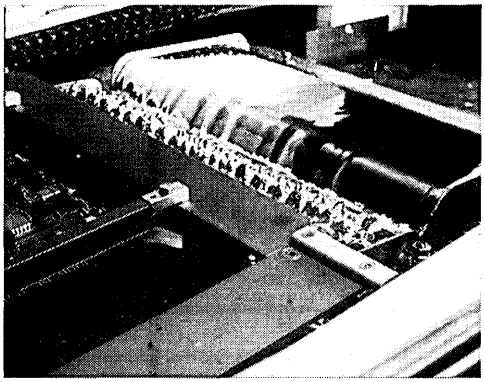
TL/F/8766–24

AQUEOUS CLEANING

- For volume production, a conveyorized system is often used with a heated recirculating spray wash (water temperature 130°C), a final spray rinse (water temperature 45–55°C), and a hot (120°C) air/air-knife drying section.
- For low-volume production, the above cleaning can be done manually, using several water rinses/tanks. Fast-drying solvents, like alcohols that are miscible with water, are sometimes used to help the drying process.
- Neutralizing agents which will react with the corrosive materials in the flux and produce material readily soluble in water may be used; the choice depends on the type of flux used.

- Final rinse water should be free from chemicals which are introduced to maintain the biological purity of the water. These materials, mostly chlorides, are detrimental to the assemblies cleaned because they introduce a fresh amount of ionizable material.

Dual Wave



TL/F/8766–25

CONFORMAL COATING

Conformal coating is recommended for high-reliability PCBs to provide insulation resistance, as well as protection against contamination and degradation by moisture.

Requirements:

- Complete coating over components and solder joints.
- Thixotropic material which will not flow under the packages or fill voids, otherwise will introduce stress on solder joints on expansion.
- Compatibility and possess excellent adhesion with PCB material/components.
- Silicones are recommended where permissible in application.

SMD Lab Support

FUNCTIONS

Demonstration—Introduce first-time users to surface-mounting processes.

Service—Investigate problems experienced by users on surface mounting.

Reliability Builds—Assemble surface-mounted units for reliability data acquisition.

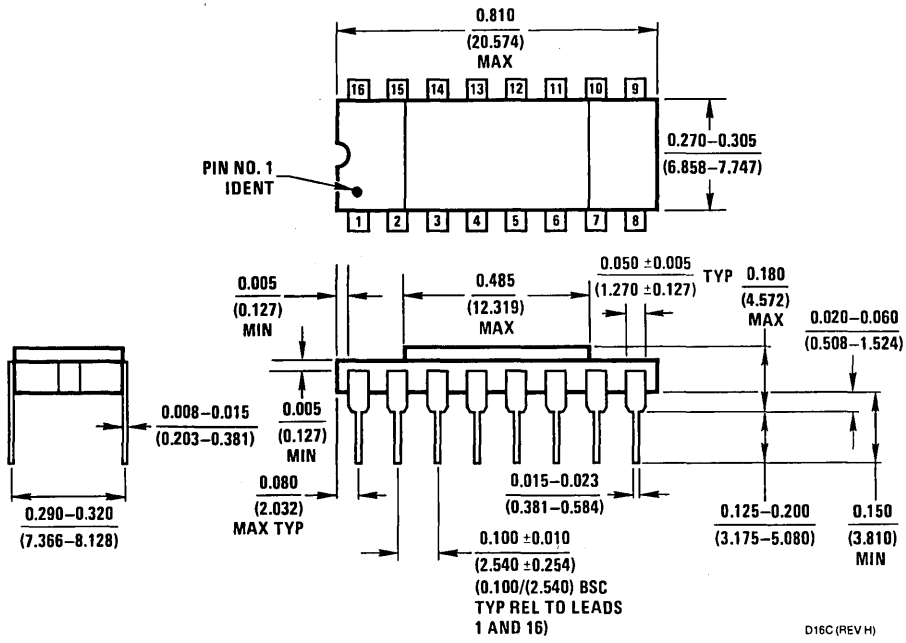
Techniques—Develop techniques for handling different materials and processes in surface mounting.

Equipment—In conjunction with equipment manufacturers, develop customized equipments to handle high density, new technology packages developed by National.

In-House Expertise—Availability of in-house expertise on semiconductor research/development to assist users on packaging queries.

National Semiconductor Corporation

All dimensions are in inches (millimeters)



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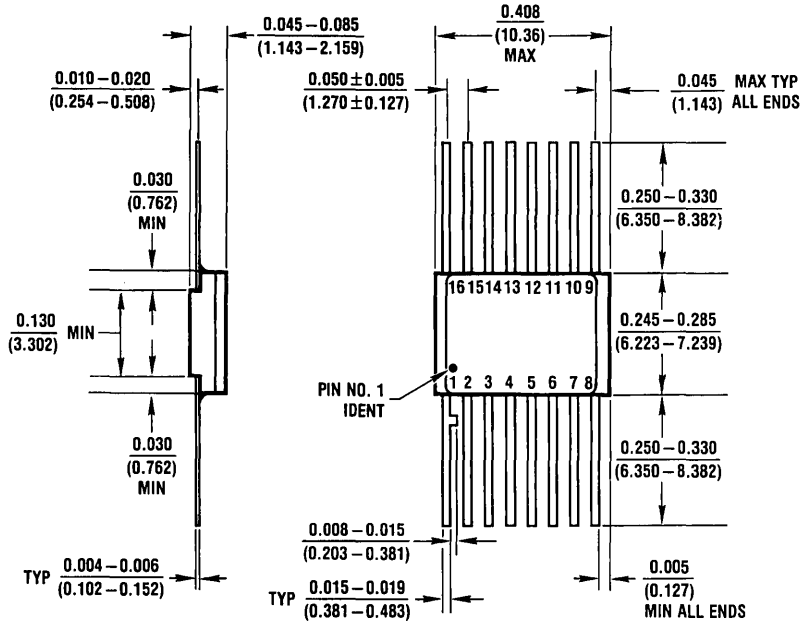

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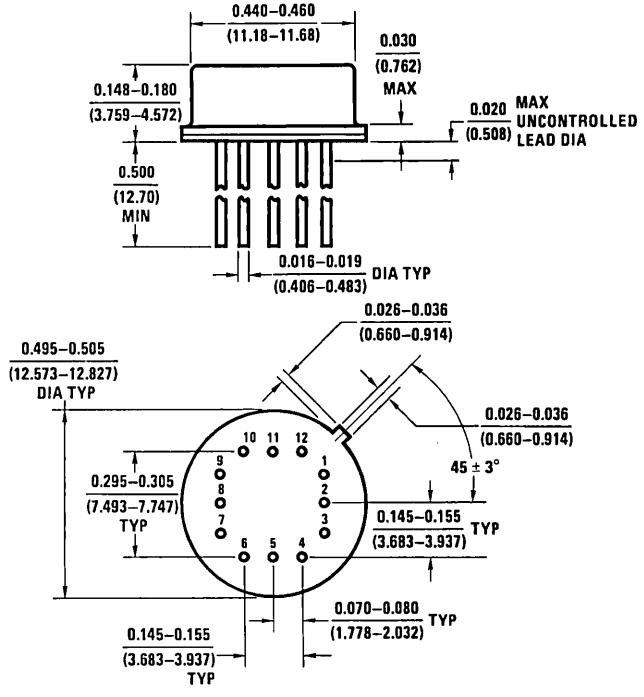

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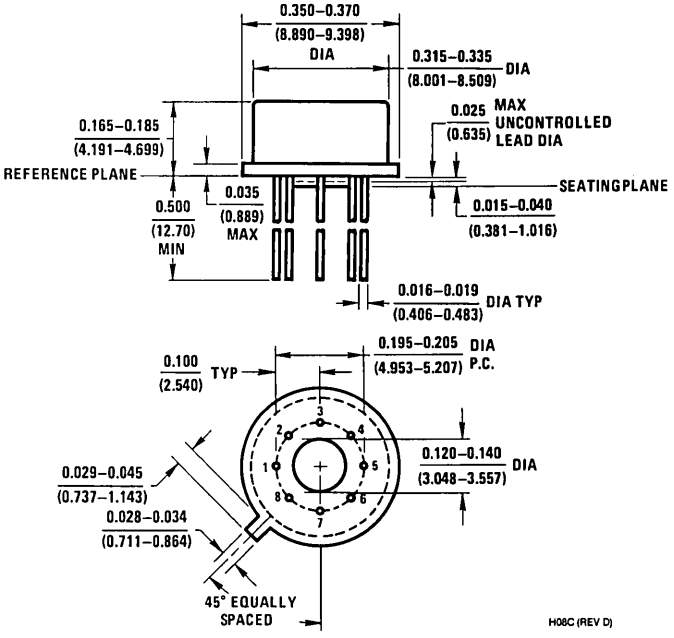

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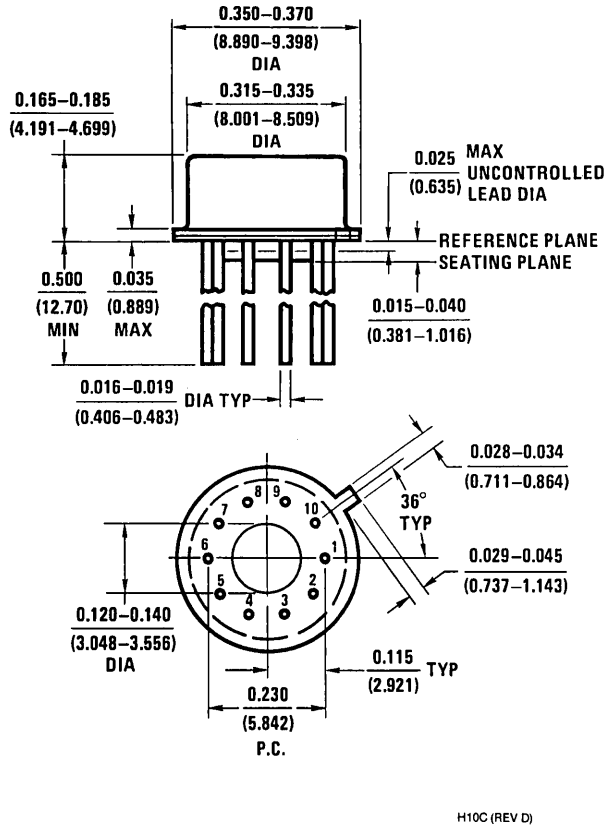

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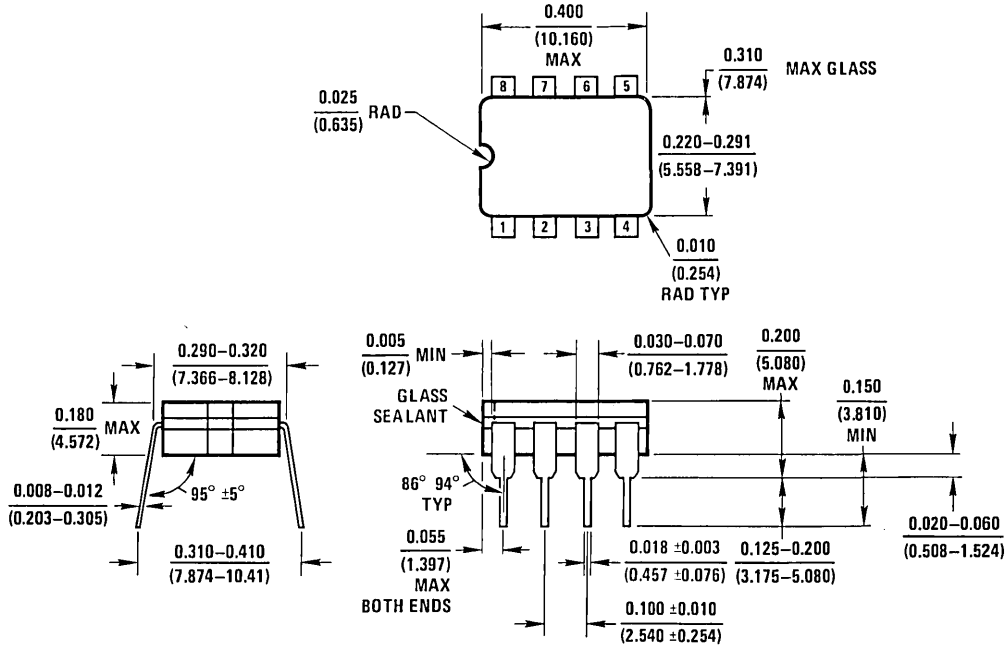

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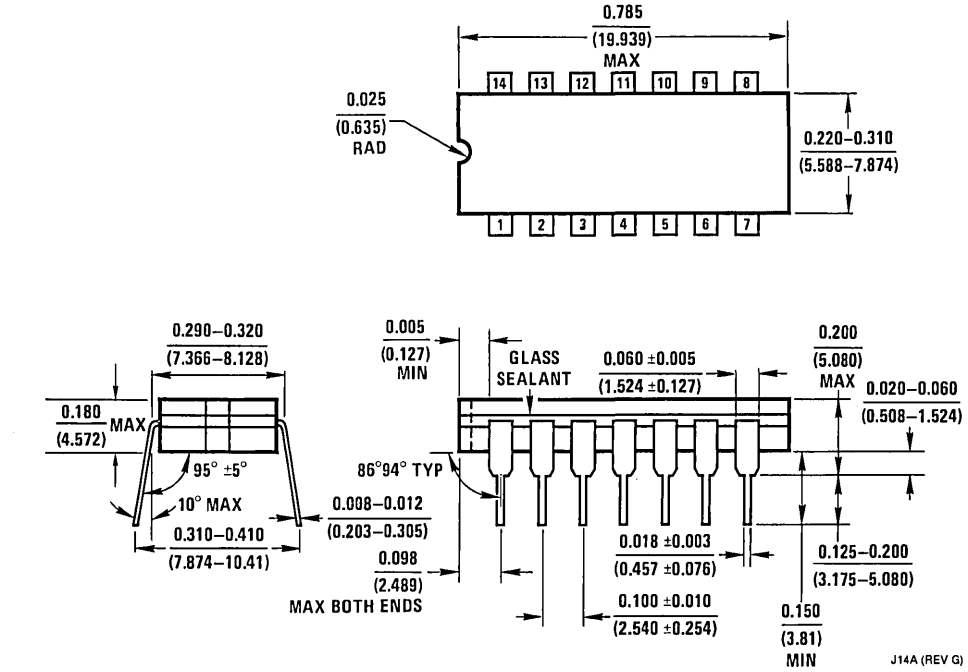

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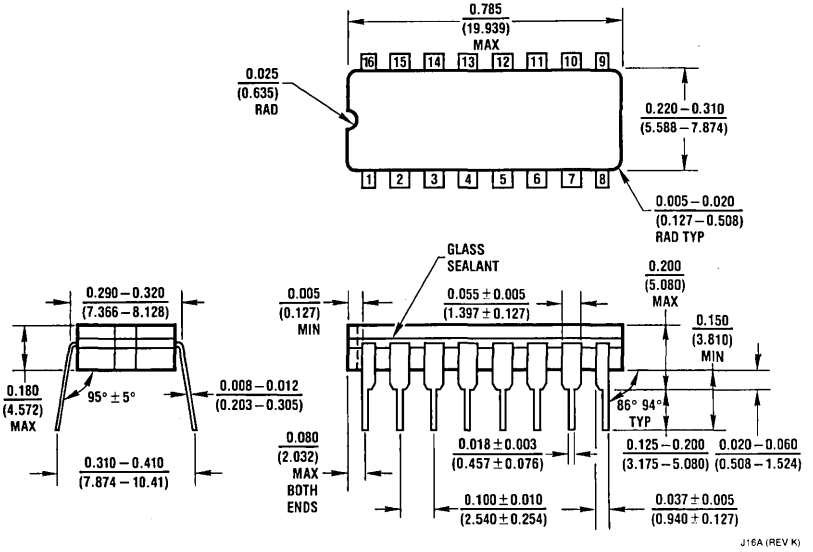

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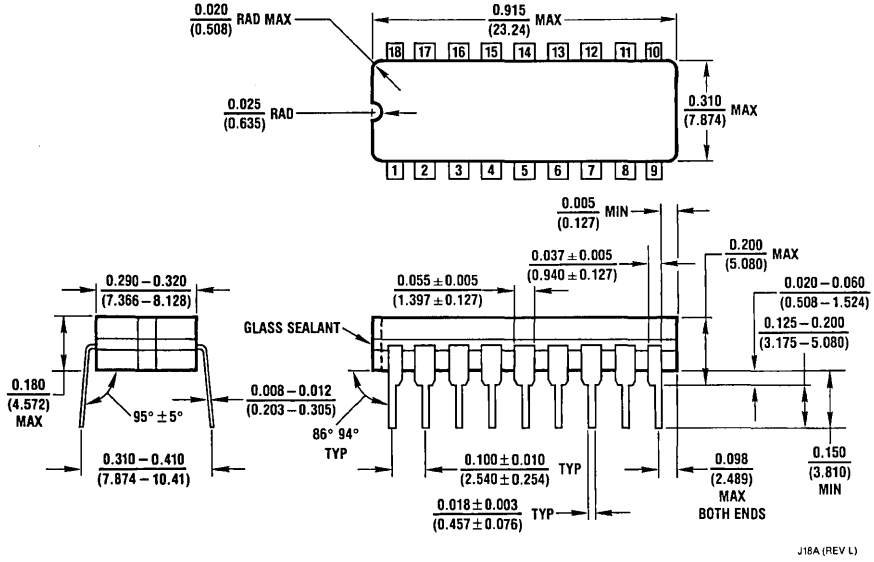

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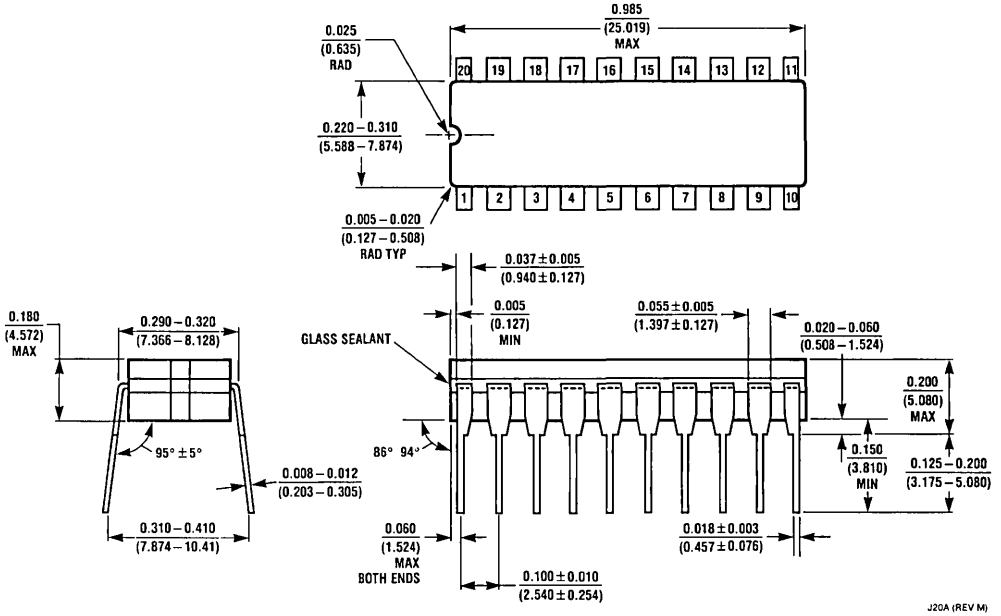

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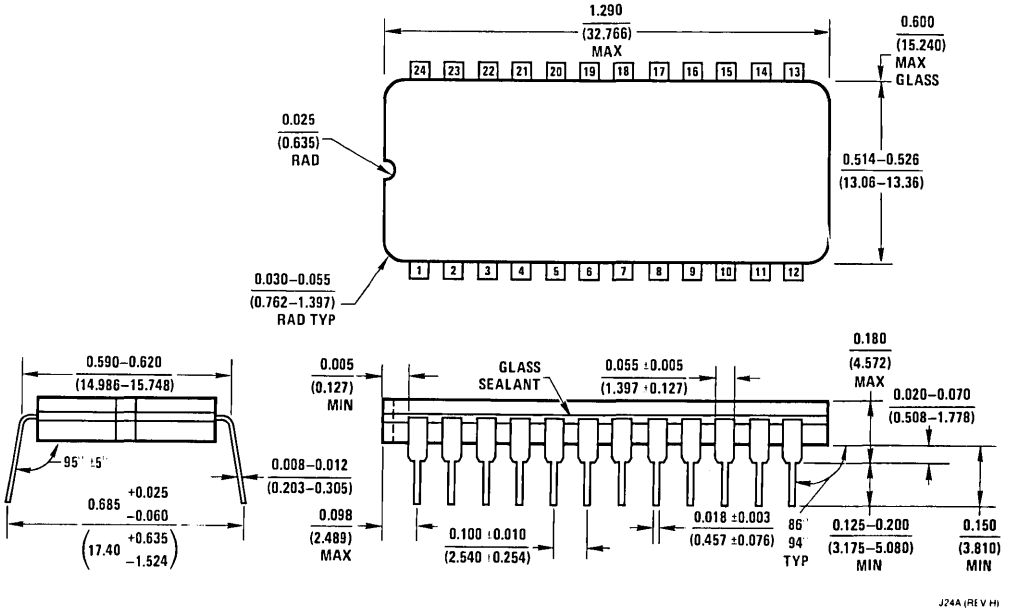

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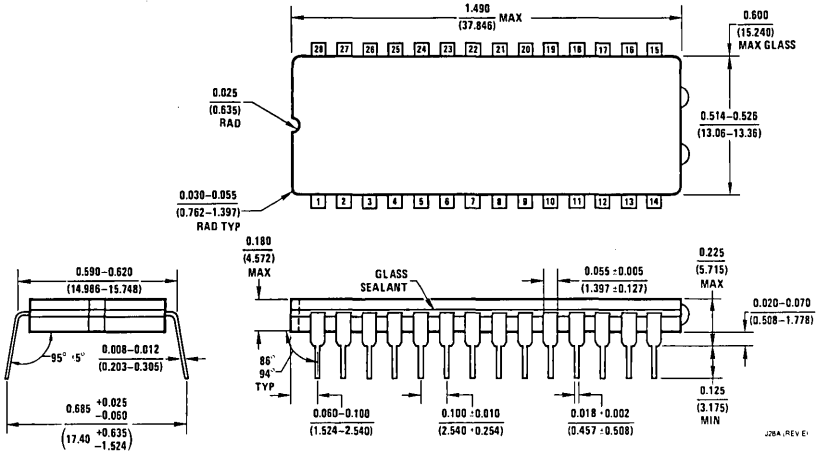

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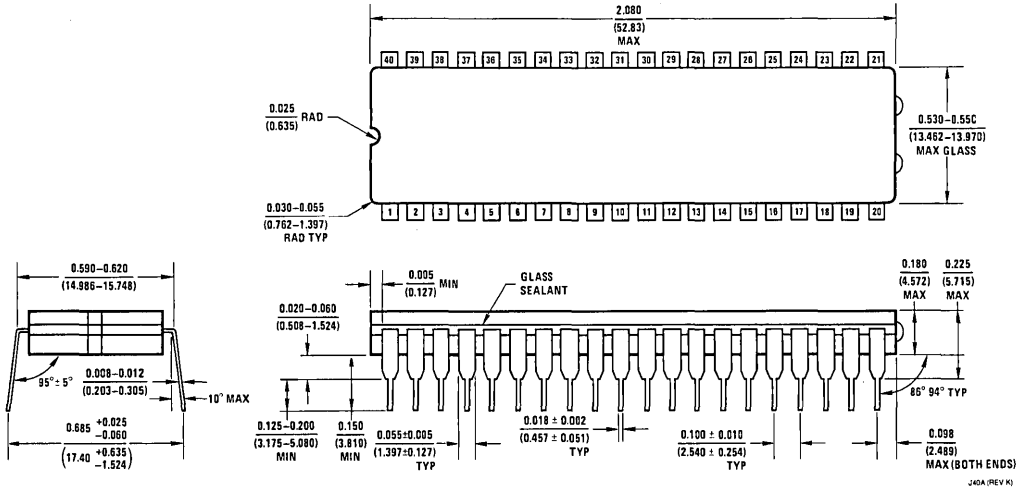

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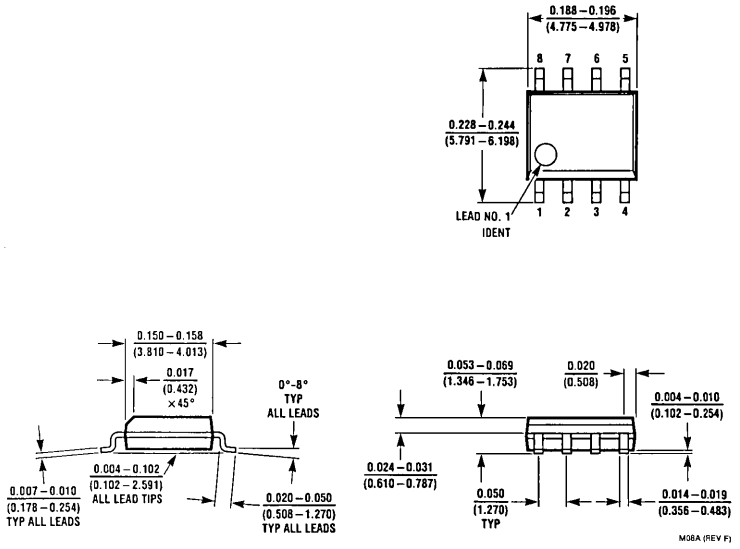

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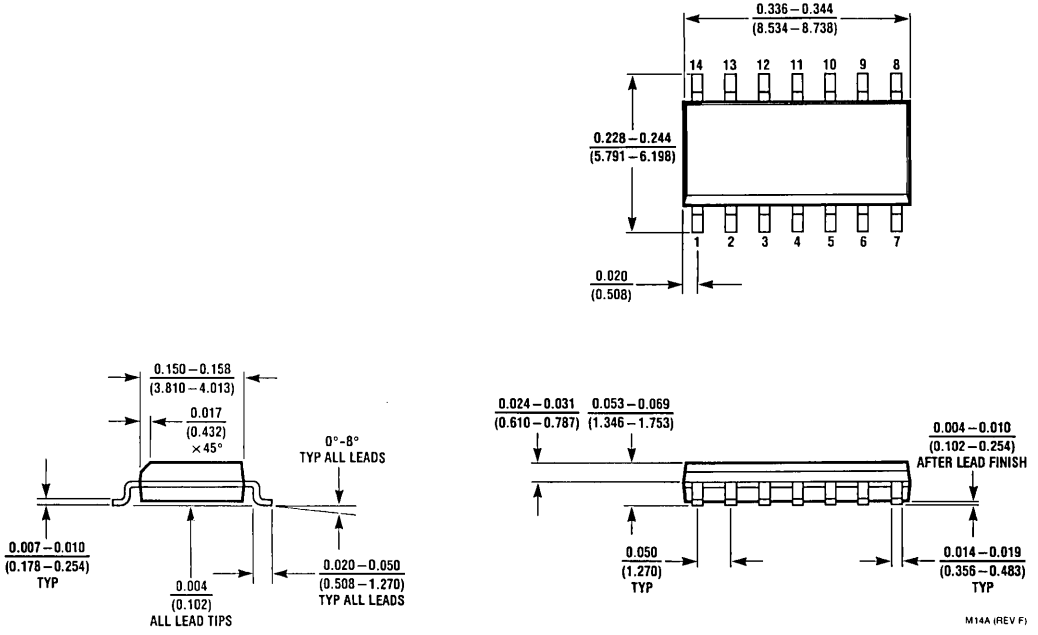

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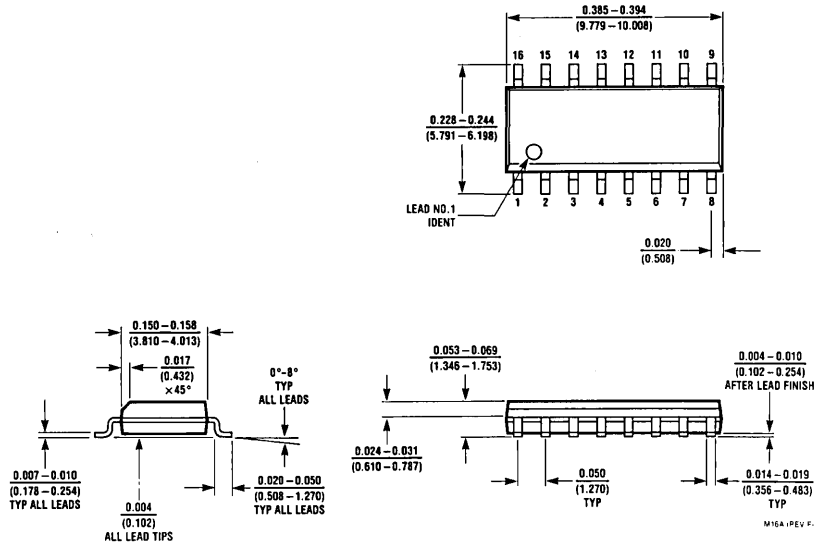

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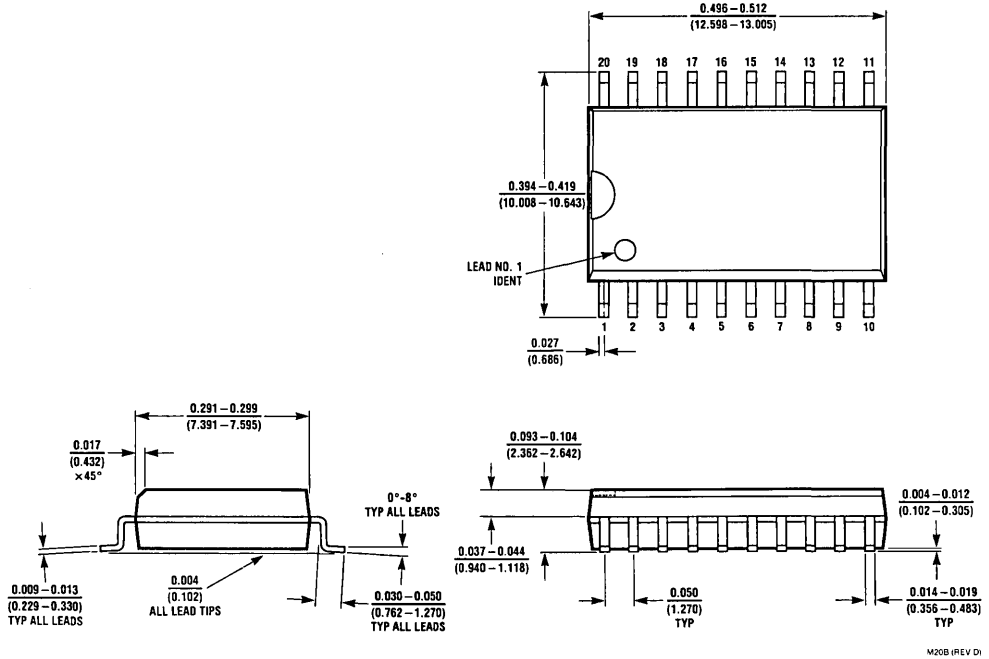

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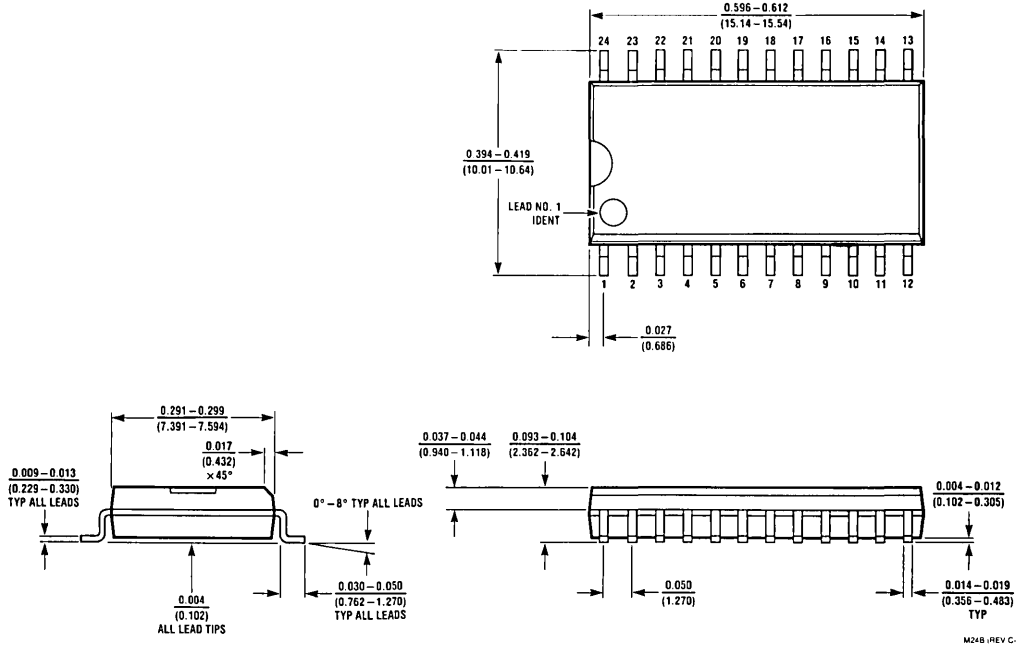

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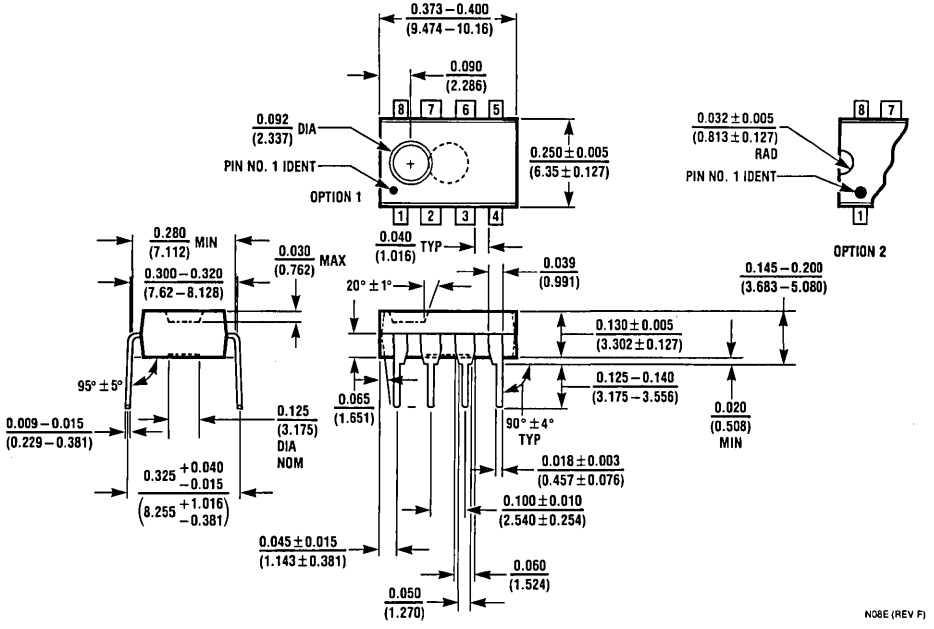

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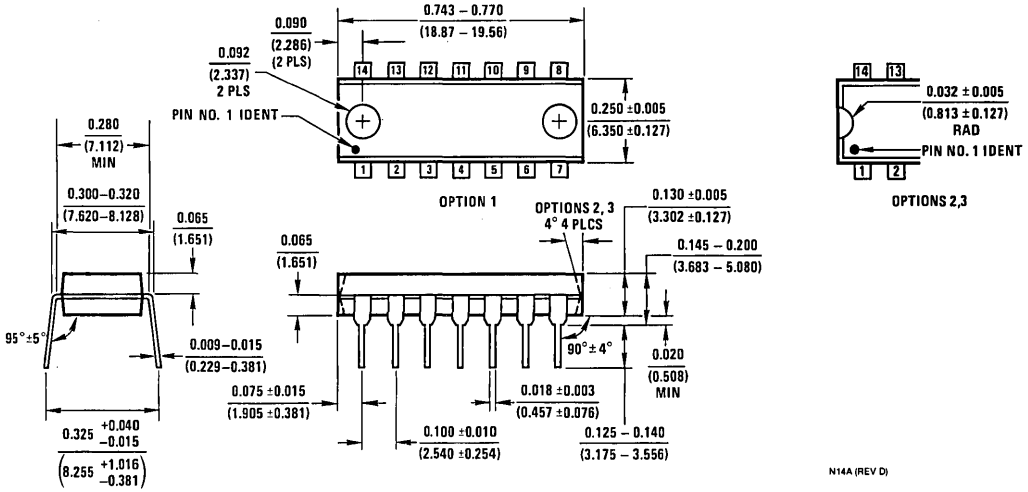

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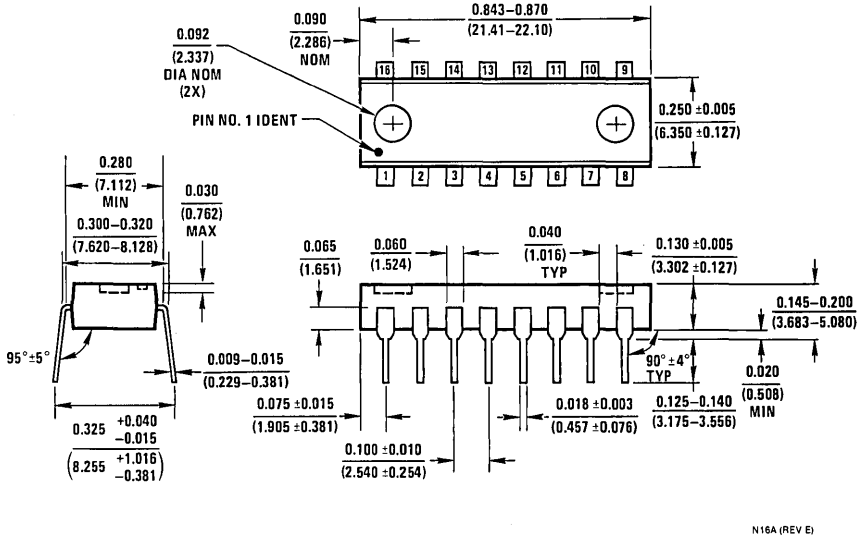

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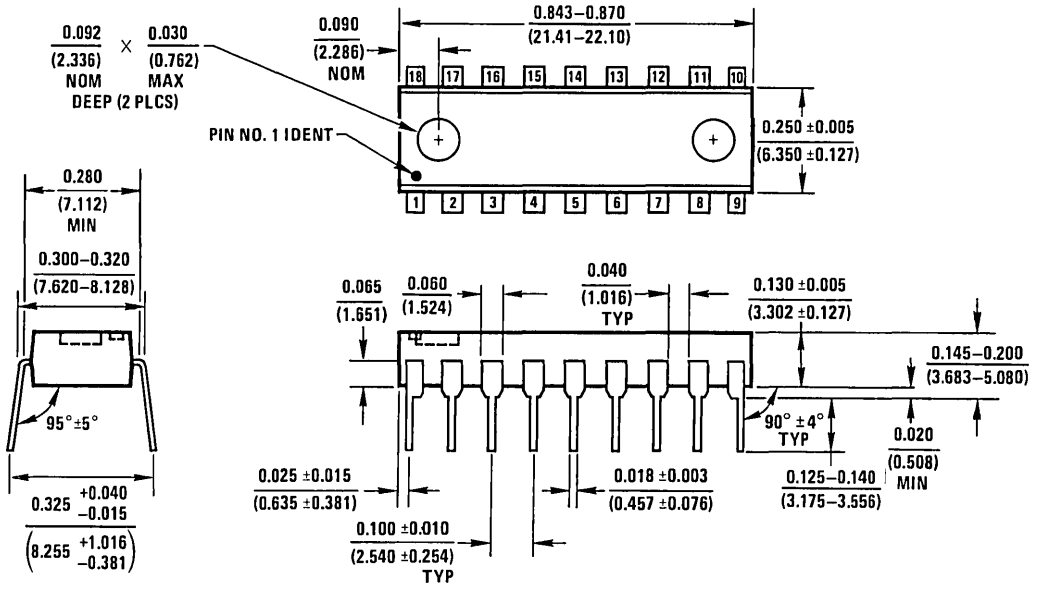

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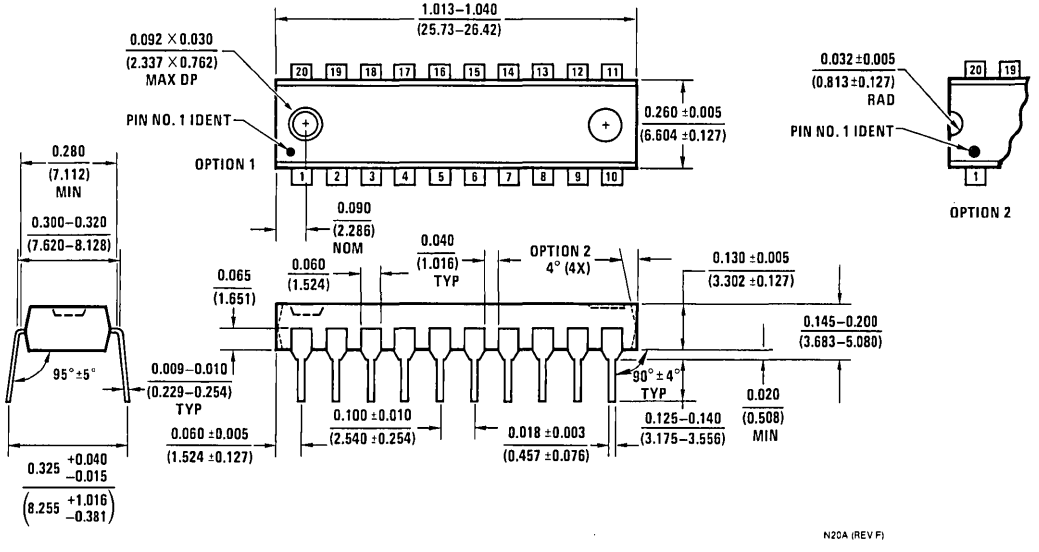

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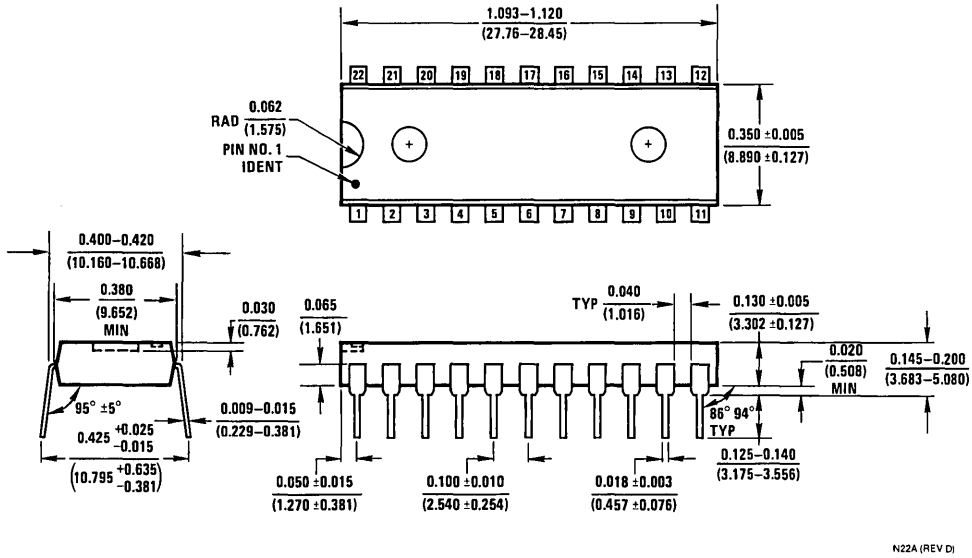

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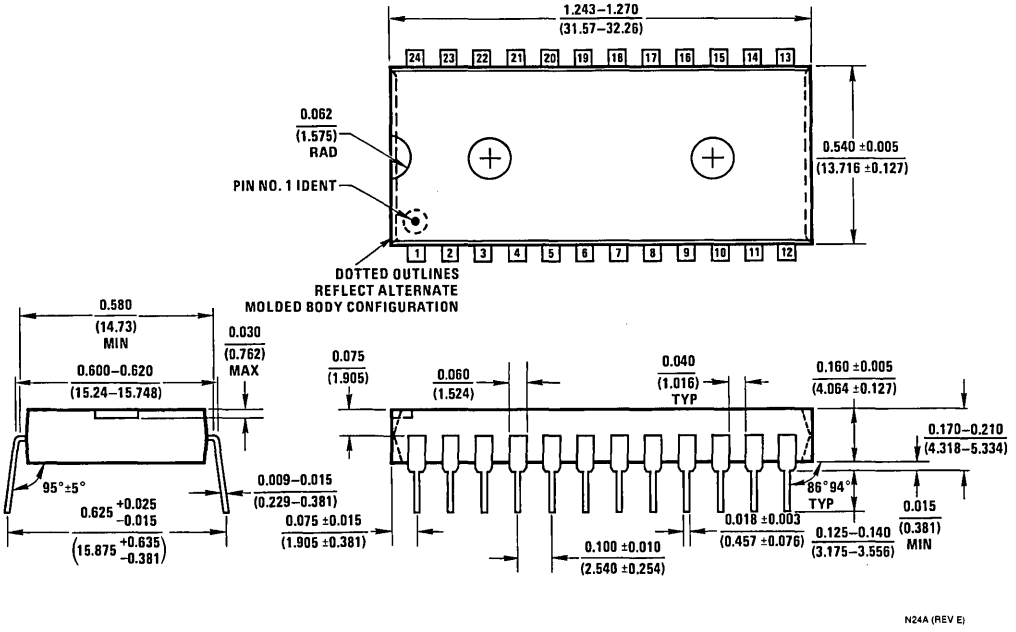

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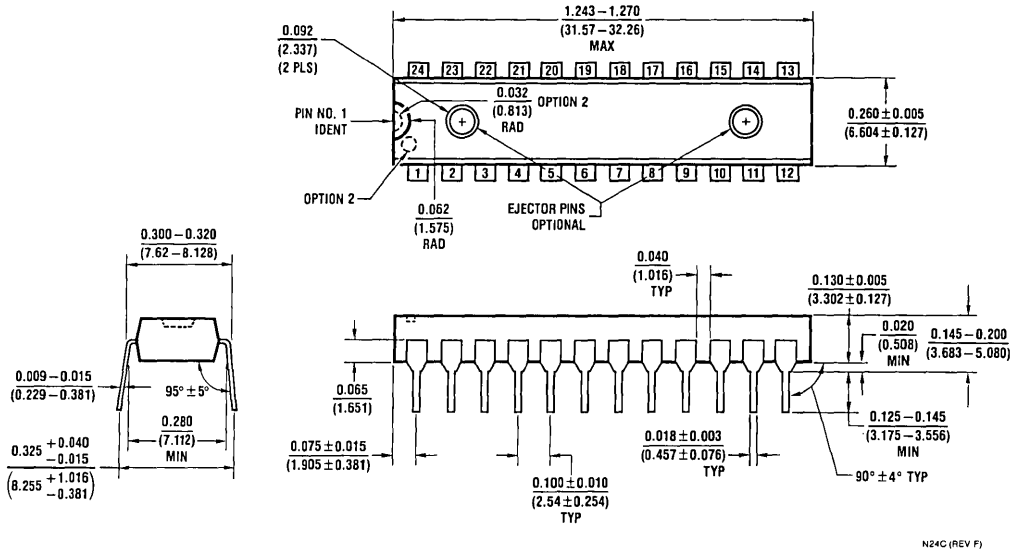

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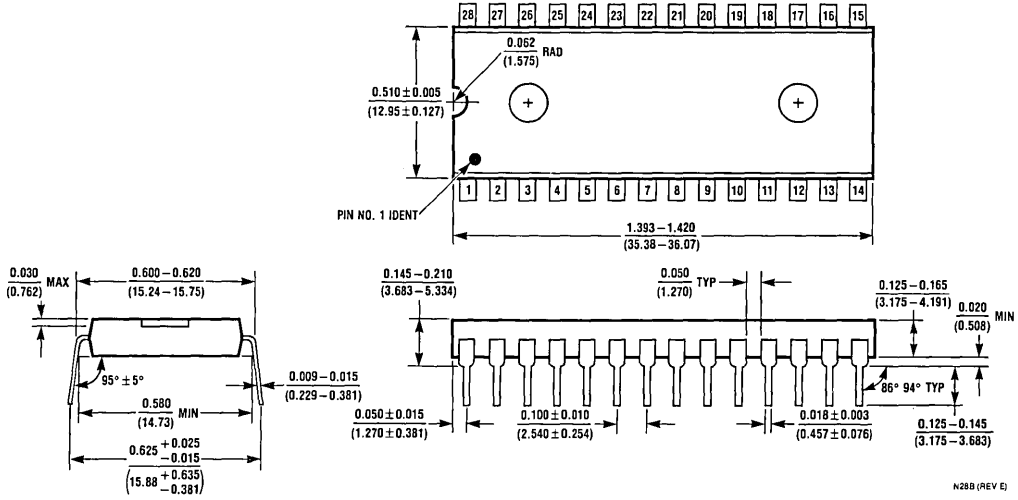

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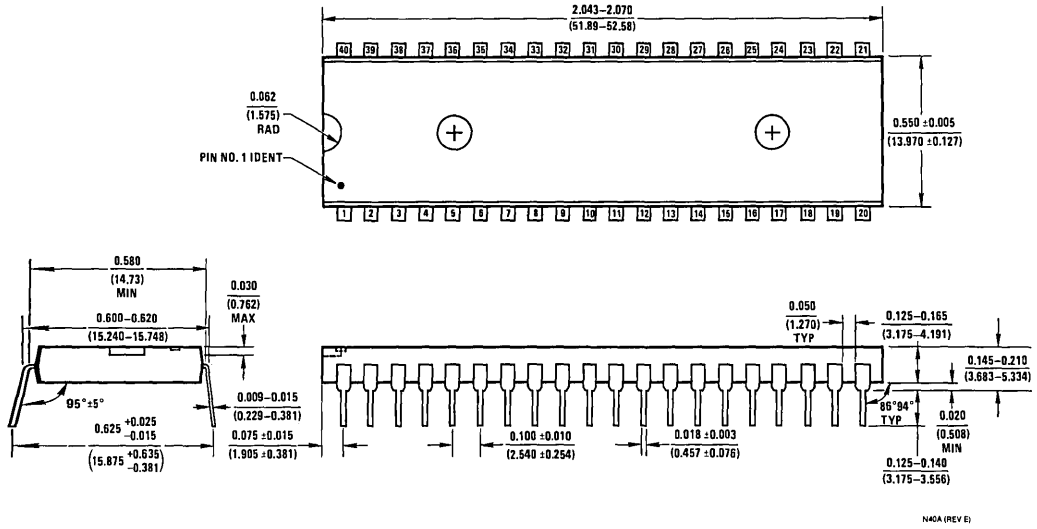

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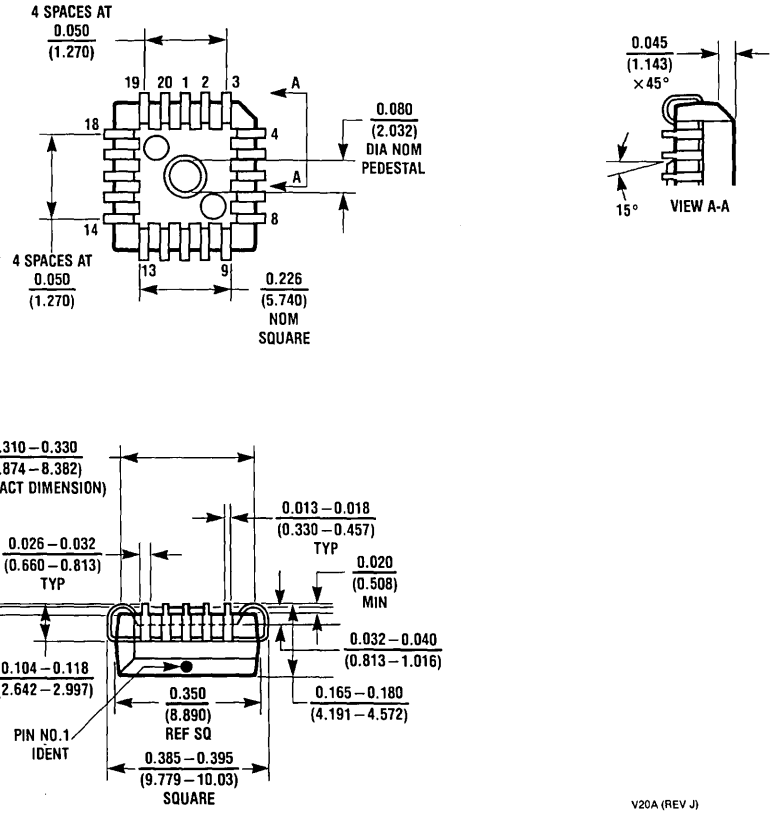

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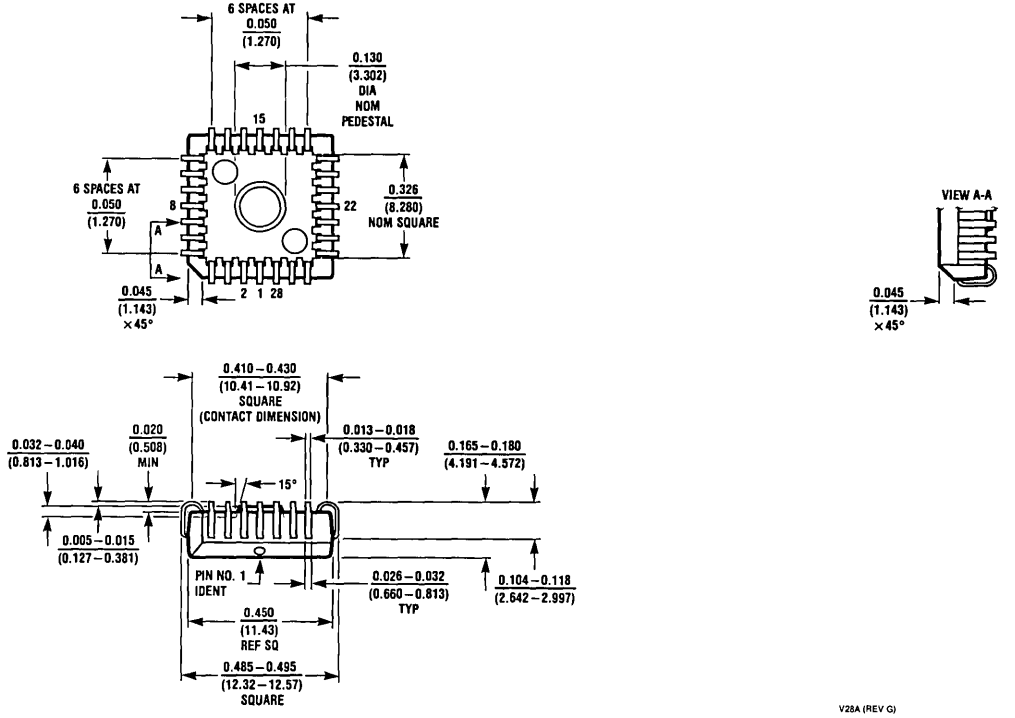

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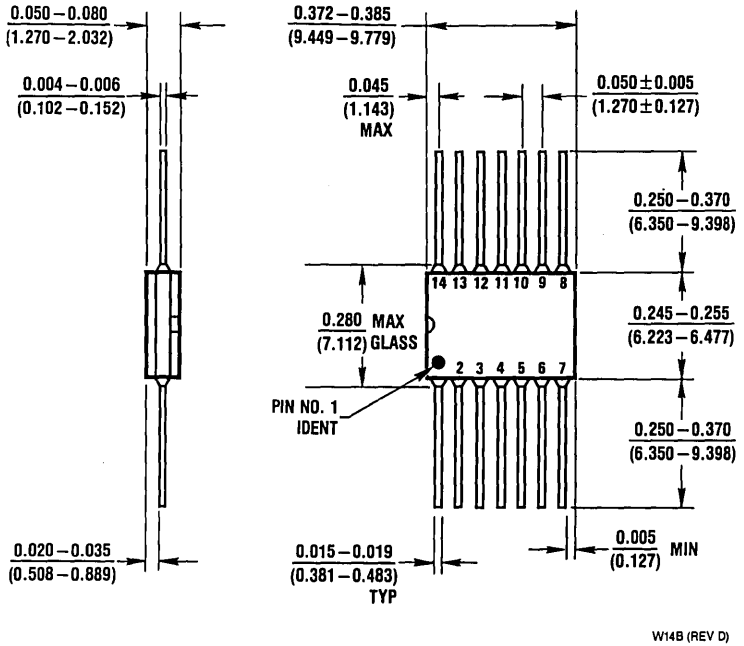

NS Package W14B

NOTES

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