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National Semiconductor

F100K ECL 300 Series Databook and Design Guide

F100K ECL
DATABOOK

1992 Edition

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Introduction

National Semiconductor's F100K 300 Series ECL Databook has been prepared to assist the experienced ECL designer as well as the first time ECL designer in everything from selecting the right logic function to using the proper termination technique in your design.

The 300 Series is designed to be an affordable high-performance logic family ideal for applications operating at frequencies above 50 MHz. F100K is still the favorite ECL technology for most high-end computer, telecommunication and test applications. The 300 Series is a much needed upgrade for these users. New users are also reaping the many benefits of the 300 Series. This family is designed to interface easily with other technologies as the types of systems mixing TTL, CMOS, and ECL expands. To assist designers with this multiple technology interface, the 300 Series offers a wide selection of translators, the ease and convenience of operation from +5V, and the availability of smaller, inexpensive, plastic packaging.

This Databook is designed to be an easy to use reference guide. Included are complete DC and AC characteristics for all package types (PCC, SOIC, PDIP, CDIP and CERPAK) and temperature ranges (commercial, industrial and military) with AC accuracy down to 10 ps. Device selection guides, circuit design basics, transmission line concepts, power distribution, thermal considerations and testing techniques are all discussed in detail to help in designing with ECL. A qualification guide is also included to aid in qualifying the 300 Series for use in your application.

A number of application notes, covering a wide range of subjects is included in this Handbook. These application notes cover such subjects as ECL backplanes and operating ECL from a positive +5V power supply. For more specific application assistance, please contact our applications staff at 1-800-341-0392.

F100K Data Book

Product Index and Selection Guide

The Product Index is a numerical list of all device types contained in this book. The Selection Guide groups the products by function and by family.

F100K Design Guide and Application Notes—Section 5

Alpha-Numeric Index

Alpha-Numeric Index (Continued)

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ECL Product Selection Guide

Gates

Function	Device	Inputs/ Gate	No. of Gates
OR/NOR Exclusive OR/NOR			
Low Power 2-Input OR/NOR Gate/Inverter	100201	2/1	2
Low Power Triple 5-Input OR/NOR	100301	5	3
Low Power Quint 2-Input OR/NOR	100302	2	5
Low Power Quint Exclusive OR/NOR	100307	2	5
AND/NAND			
Low Power Quint 2-Input AND/NAND	100304	2	5

Flip-Flops

Function	Device	Clock Edge	Direct Set	Direct Clear	Outputs
Low Power Triple D Flip-Flop	100331	⌐	Yes	Yes	Differential
Low Power Hex D Flip-Flop	100351	⌐	No	Yes	Differential

Latches

Function	Device	Enable Inputs	Inputs	Outputs	Direct Set	Direct Clear
Low Power Hex D Latch	100350	2(L)	Single-ended	Differential	Yes	Yes
Low Power Quad 2-Input Mux/Latch	100355	2(L)	Single-ended	Differential	Yes	Yes
Low Power 8-Bit Latch	100343	2(L)	Single-ended	Single-ended	No	No
Low Power 8-Bit Latch w/Cutoff Drivers and 25Ω Drive	100344	3(L)	Single-ended	Single-ended	No	No

Multiplexers/Demultiplexers/Decoders

Function	Device	Enable Inputs	Inputs	Outputs
Multiplexers/Decoders/Demultiplexers				
Low Power Quad 2-Input Mux/Latch	100355	2(L)	Single-ended	Differential
Low Power Dual 8-Input	100363		Single-ended	Single-ended
Low Power 16-Input	100364		Single-ended	Single-ended
Low Power Triple 4-Input	100371	1(L)	Single-ended	Differential
Decoders/Demultiplexers				
Low Power Dual 1-of-4/Single 1-of-8	100370	2(L) & 2(L)	Single-ended	Single-ended

Registers/Shift Registers

Function	Device	Clock Inputs	Inputs	Outputs
Registers				
Low Power 8-Bit Register	100353	⎍	Single-ended	Single-ended
Low Power 8-Bit Register w/Cutoff Drivers and 25Ω Drive	100354	⎍	Single-ended	Single-ended
Shift Registers				
Low Power 4-Bit Bidirectional Shift Register	100336	⎍	Single-ended	Differential
Low Power 8-Bit Shift Register	100341	⎍	Single-ended	Single-ended

Buffers/Drivers/Receivers

Function	Device	Inputs	Outputs	25Ω Drive	Output Cut-off
Buffers/Inverters					
Low Power 9-Bit Inverter	100321	Single-ended	Single-ended	No	No
Low Power 9-Bit Buffer	100322	Single-ended	Single-ended	No	No
Low Power 8-Bit Buffer	100352	Single-ended	Single-ended	Yes	Yes
Drivers/Bus Drivers					
Low Power Quad Line Driver	100313	Single-ended	Differential	No	No
Low Power Hex Bus Driver	100323	Single-ended	Single-ended	Yes	Yes
Low Power Quad Line Driver	100316	Single-ended	Differential	Yes	Yes
Low Power Hex Line Driver	100319	Differential	Differential	Yes	Yes
Receivers/Transceivers					
Low Power Quint Differential Line Receiver	100314	Differential	Differential	No	No

Counter

Function	Device	Parallel Entry	Reset	Up/Down
Low Power 4-Bit Binary Counter	100336	Sync	Sync/Async	Yes

Arithmetic Operator

Function	Device	Features
Low Power Dual 9-Bit Parity Checker/Generator	100360	Expandable

Clock Drivers

Function	Device	Clock Inputs	Single-ended Clock	Differential Clock
Low Power 2 to 8 Clock Driver	100310	2		2
Low Skew 1 to 9 Clock Driver	100311	1		1
Low Skew Quad Clock Driver	100315	2	1	1

Dual Supply Translators

Features	100324	100325	100328	100329	100393	100395	100397	100398
Data Bits	6	6	8	8	9	9	4	4
ECL-to-TTL		X	X	X	X	X	X	X
TTL-to-ECL	X		X	X			X	X
Flow-Thru	X	X						
Latched			X		X		X	X
Registered				X		X		
ECL Differential Input		X[1]					X	X
ECL Differential Output	X						X	X
ECL Output Drive (Ω)	50		50	50			25	25
ECL Cutoff (Hi Z)			X	X			X	X
TTL Output Drive (mA) (I_{OL}/I_{OH})		20/−2	23/−3	24/−3	64/−15	64/−15	64/−15	64/−15
TTL TRI-STATE®			X	X	X	X	X	X
ECL Control Pins			X	X	X	X	X	
TTL Control Pins	X				X			X
TPD E to T (ns Max)		4.8	5.9	7.7	5.3	6.4	5.8	5.8
TPD T to E (ns Max)	3.0		3.8	3.9			2.4	2.2
I_{EE} (mA Max)	−70	−37	−169	−199	−39	−67	−99	−99
I_{EE} (mA Max) (Cutoff)			−169	−199			−159	−159
I_{CC} (mA Max)	38	65	74	74	65	65	36	45

[1] V_{BB} provided for Single-ended Operation

Single Supply Translators

Features	100390	100391	100392	100389
Data Bits	6	6	5	6
ECL-to-TTL	X			
TTL-to-ECL		X		
CMOS-to-ECL			X	X
ECL Differential Input	X[2]			
ECL Differential Output		X	X	X
ECL Output Drive (Ω)		50	25	50
ECL Cutoff (Hi Z)			X	
TTL Output Drive (mA) (I_{OL}/I_{OH})	24/−3			
TTL TRI-STATE®	X			
TTL Control Pins	X	X		
CMOS Control Pins			X	X
TPD E to T (ns Max)	6.4			
TPD T to E (ns Max)		1.7		
TPD C to E (ns Max)			TBD	TBD
I_{EE} (mA Max) (Cutoff)			TBD	
I_{CC} (mA Max)	48	60	TBD	TBD

[2] V_{BB} provided for Single-ended Operation

ECL Package Selection Guide

Device	24-Lead CDIP	24-Lead PDIP	24-Lead QFP	24-Lead SOIC	28-Lead PCC	16-Lead SOIC
100301	X	X	X	X	X	
100302	X	X	X	X	X	
100304	X	X	X		X	
100307	X	X	X	X	X	
100310					X	
100311					X	
100313	X	X	X	X	X	
100314	X	X	X	X	X	
100315						X
100316	X	X			X	
100319	X	X			X	
100321	X	X	X		X	
100322	X	X	X		X	
100323	X	X	X		X	
100324	X	X	X	X	X	
100325	X	X	X	X	X	
100328	X	X	X	X	X	
100329	X	X	X		X	
100331	X	X	X	X	X	
100336	X	X	X	X	X	
100341	X	X	X	X	X	
100343	X	X	X		X	
100344	X	X	X		X	
100350	X	X	X		X	
100351	X	X	X	X	X	
100352	X	X	X		X	
100353	X	X	X		X	
100354	X	X	X		X	
100355	X	X	X		X	
100360	X	X	X		X	
100363	X	X	X		X	
100364	X	X	X		X	
100370		X			X	
100371	X	X	X	X	X	
100389		X		X	X	
100390	X	X	X	X	X	
100391		X		X	X	
100392		X			X	
100393					X	
100395					X	
100397		X			X	
100398		X			X	

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Product Status Definitions

Definition of Terms

Data Sheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This data sheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This data sheet contains preliminary data, and supplementary data will be published at a later date. National Semiconductor Corporation reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
No Identification Noted	Full Production	This data sheet contains final specifications. National Semiconductor Corporation reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Obsolete	Not In Production	This data sheet contains specifications on a product that has been discontinued by National Semiconductor Corporation. The data sheet is printed for reference information only.

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Section 1

Family Overview

Section 1 Contents

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Family Overview

Introduction

Precious few alternatives available offer the performance of ECL. Most designers recognize the advantages offered by ECL in high speed systems extend beyond just quick switching times. However, the use of ECL has been somewhat limited to those applications concerned with high speed and often little more. These applications usually had extravagant cooling systems and massive power sources to keep the signal moving. Rapid advancements in microprocessors and high resolution video equipment are now beginning to push preferred TTL and CMOS technologies to their limits. The need for functions with ECL-like speeds without ECL-like power for use in smaller but increasingly powerful systems is growing rapidly.

The problems with working with high speed systems are beginning to migrate downward from supercomputers to workstations as the performance of workstations moves upward. The benefits of using ECL in high-end applications have long been recognized by those designers familiar with it. Low propagation delays with moderate edge rates, negligible noise and ground bounce, constant power consumption over frequency and the ability to drive low impedance transmission lines have combined to make ECL the preferred technology for designers who have had previous experience with it. However, the majority of designers never had to consider ECL, until now. The increasing availability of high speed microprocessors is driving the need for faster busses and more accurate clocking.

ECL still has its drawbacks, but recent technological advances have made ECL a much more appealing and usable technology. With the growing need for high speed signal distribution, ECL is beginning to move more into high performance backplanes. Designers like and require the high speed, differential outputs, low impedance drive and transmission line-like characteristics of ECL. ECL is also being used increasingly in clock distribution trees because of its speed and inherently low skew. High resolution video graphics terminals with a display resolution of 1024 x 1024 pixels require a bandwidth of over 80 MHz, not an easy task for CMOS or TTL but well within the range of ECL. Broadband communication systems are also using a great deal of ECL as fiber optic data transfer moves into greater utilization.

National Semiconductor introduced the F100K 300 Series to allow ECL to be more usable in today's high performance systems. In developing this new family, much emphasis was placed on power, space and cost reductions. The 300 Series was designed to interact with other technologies, not to replace them. Many new designs are attempting to optimize the most efficient mix of speed, power and price with ECL, CMOS and TTL all working together. ECL will handle the speed critical applications, CMOS functions would keep the overall system power low and TTL would be included to keep costs down. The performance, power, packaging and functionality of the 300 Series make this family ideal for those applications operating above 50 MHz.

Much of what the 300 Series has evolved into, is a compilation of inputs received from designers who could not use the older F100K 100 Series for various reasons. This resulted in parts with lower operating power, significantly improved ESD protection, plastic surface mount packaging, additional AC testing including skew, easy interface with other technologies and increased functionality. This section will go into much greater detail about ECL and the evolution of the 300 Series.

F100K Design Philosophy

F100K was designed to meet four key requirements: high speed at reduced power, high level of on-chip integration, flexible logic functions, and optimum I/O pin assignment.

Subnanosecond Gate Delays

The subnanosecond internal gate delays of F100K 100 Series were obtained by the use of ECL design techniques and the advanced Isoplanar-Z process. Many circuit approaches were carefully considered prior to selecting the optimum gate configuation for the F100K family. The emitter-follower current-switch (E^2CL) and current-mode logic (CML) gates were eliminated mainly because of poor capacitive drive and lack of output wired-OR capability; the CML gate has low noise margins. The 2-½D, EFL, DCTTL and hysteresis gates were eliminated due to the lack of simultaneous complementary outputs along with difficult temperature and voltage compensation characteristics that lead to the loss of system noise immunity.

The choice narrowed down to the current-switch emitter-follower ECL gate which offers the following characteristics:

- High fan-out capability
- Simultaneous complementary outputs
- Excellent AC characteristics
- Compatibility with existing ECL logic and memories
- Internal series gating capability
- Good noise immunity
- Amenable full compensation and extended temperature characteristics
- External wired-OR capability

In order to ease drive requirements all circuit inputs were designed to have similar loading characteristics; i.e., buffers are incorporated where an input pin would normally drive more than one on-chip gate. The on-chip delay incurred by buffering is less than the system delay caused by an output which drives a capacitance of higher than three unit loads. Full compensation was selected for the F100K Family to provide improved switching characteristics. Full compensation results in relatively constant signal levels and thresh-

olds and in improved noise margins over temperature and voltage variations from chip to chip, and thus a tighter AC window in the system environment. A comparison of fully compensated ECL to conventional ECL shows a 2:1 improvement in system AC performance due solely to full compensation *(Figure 1-1)*. And, the improved speed has been achieved at reduced power. Power reduction is accomplished by the use of advanced process technology that reduces parasitic capacitances and improves tolerances, by optimum circuit designs using series gating and collector and emitter dotting, and by designing for the use of a −4.5V V_{EE} power supply. F100K 100 Series is specified at a V_{EE} power supply of −4.2V to −4.8V, but a −5.2V ±10% power supply can be used to interface with 2 ns ECL families.

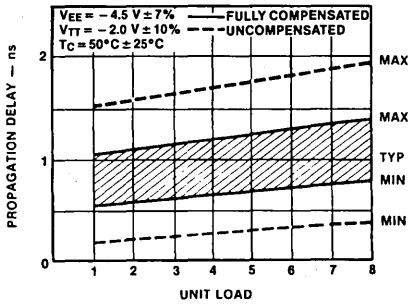

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FIGURE 1-1. Comparison of Propagation Delays

High On-Chip Integration

Higher on-chip integration is made possible by using the 24-pin package to increase the number of signal pins by 62% over the conventional 16-pin package. The emphasis in F100K is to minimize the number of SSI functions and maximize the use of MSI and LSI to reduce wiring delays and thus make more efficient use of the fast on-chip switching technology. Only 10 SSI functions are needed to serve the system needs presently requiring 25 functions in the ECL 10K family.

Flexibility and Pin Assignment

F100K was planned to minimize to total number of logic functions by increasing the flexibility of each function and by making use of more I/O pins. Since next-generation system performance and ease of system designs are major F100K goals, pin assignment is important and was planned to minimize crosstalk, noise coupling and feedthrough, to facilitate OR-ties and to ease power-bus routing. Some of the key considerations in selecting the F100K pin assignments were:

- Locate power pins in the center on opposite sides of the DIP package to ease system design and to provide low-inductance connections to the chip.
- Provide two V_{CC} pins, one for the internal circuit and one for the output buffers, to minimize noise coupling.
- Locate inverting outputs of logically independent gates adjacent to each other. This provides the ability to wire AND-OR-Invert functions with ease.
- When feasible, mode control pins are used to create multipurpose devices.

300 Series Design Philosophy

F100K 300 Series was designed to improve several performance parameters while still maintaining the speed and functionality requirements of the original F100K family. These new improvements enable 300 Series to be used in an even broader range of applications.

Most importantly, 300 Series products all meet F100K's optimized speeds and edge rates, while consuming up to 50% less power. These lower power designs, combined with the manufacturability of the FAST-LSI process (see Process Technology), enabled the 300 Series line to be reliably packaged in plastic leaded chip carrier (PCC) packages. A graph is shown comparing the power consumption of the F100124 and F100324 vs. supply voltage *(Figure 1-2)*. In addition, 300 Series is designed with a more stable voltage reference network, providing a single set of DC specifications across a wider supply voltage range (−4.2V to −5.7V), easing the design of 300 Series into systems which use −5.2V power supplies. Also, 300 Series products have been designed to comply with all MIL-STD-883C requirements, including operation over the full military temperature range of −55°C to +125°C. Finally, electrostatic discharge (ESD) protection diodes have been added to both input and output circuitry, guaranteeing a minimum of 2000V ESD protection for all 300 Series products.

Several new circuits were utilized to achieve the performance improvements. The stabilized DC characteristics across the −4.2V to −5.7V power supply range are achieved through use of an improved reference network *(Figure 1-3)*. This network replaces a resistor with a PNP transistor (Q_3). The collector-emitter voltage of Q_3 varies with V_{CC}, allowing the voltage at the base of Q_6 to remain constant as V_{CC} varies. This, in turn, stabilizes both V_{BB} and V_{CS}, so that as V_{EE} varies from −4.2V to −5.7V, V_{BB} varies no more than 15 mV–20 mV. (Variation of V_{BB} in F100K 100 Series products over this same voltage range can be as much as 70 mV–80 mV). The improved stability of 300 Series vs. V_{CC} is reflected in the single set of DC I/O specifications guaranteed across this wider voltage range. These specifications are identical to the F100K 100 Series specifications listed at −4.5V. As shown in *Figure 1-4*, they increase minimum noise margins guaranteed by 300 Series to 140 mV.

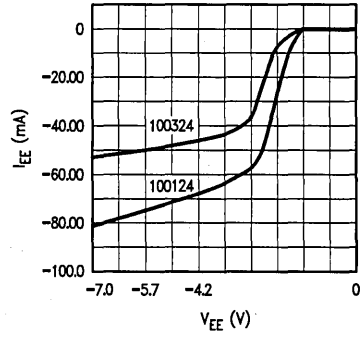

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FIGURE 1-2. 300 Series Power Reduction

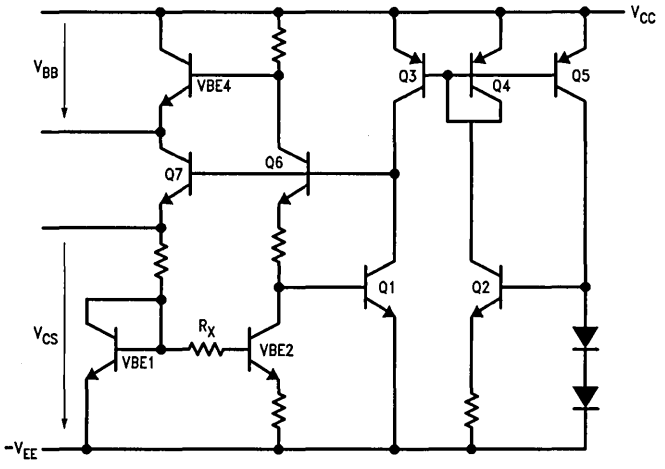

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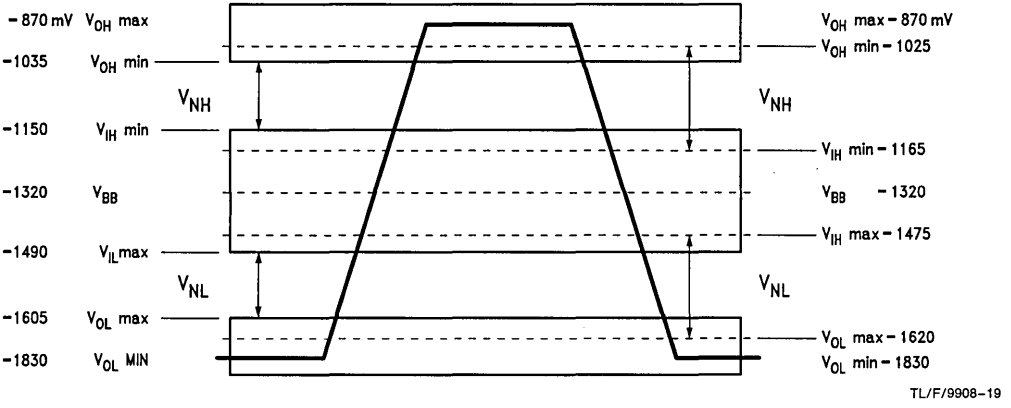
FIGURE 1-3. 300 Series Reference Network



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100 Series Logic

V_{NH} = 115 mV
V_{NL} = 115 mV
V_{EE} = −4.2V to −4.8V

$V_{NH} = V_{OH}$ Min − V_{IH} Min
$V_{NL} = V_{IL}$ Max − V_{OL} Max

300 Series Logic

V_{NH} = 140 mV
V_{NL} = 145 mV
V_{EE} = −4.2V to −5.7V

FIGURE 1-4. 300 Series Noise Margins

All 300 Series products are designed to operate over the full military temperature range. To achieve this, internal voltage swings were increased to guardband against transistor saturation at temperature extremes. The faster transistor speeds offered by the FAST-LSI process compensated for the increased delays introduced by the wider voltage swings. Some of the more complex products utilize multilevel series gating to achieve higher levels of logic complexity at while reducing gate delays and power consumption. These products employ a Widlar Current Sink *(Figure 1-5)* to compensate for V_{BE} shifts at −55°C. In this circuit, the emitter resistor is removed from the current source (Q_1), providing more voltage headroom at lower temperatures, and avoiding saturation of the current source at −55°C. A second transistor (Q_2), driven by a voltage biased at V_{CS} + V_{BE}, provides V_{CS} at its emitter to drive the current source. This minimizes power by reducing the loading on the reference generator. A temperature-compensated current mirror (Q_3) is employed to control the base voltage of the current source so that it doesn't move regardless of V_{EE} or temperature changes.

Electrostatic discharge (ESD) protection diodes were added to all 300 Series designs *(Figure 1-6)* specifically in the circuit paths that were most prone to ESD damage on F100K 100 Series products: input-to-V_{CC}, input-to-V_{EE}, and output-to-V_{CC}. These diodes (D_1, D_2, and D_3) are utilized to shunt the current caused by an ESD voltage pulse away from either the input or output circuitry. Depending on the polarity of the ESD voltage, the diodes either become forward-biased, directing the current into the supply, or go into reverse breakdown, directing the current into the substrate. Either way, the ESD-caused current is shunted away from the input and output transistors, avoiding damage to the circuitry. The diodes are designed to be rugged enough to guarantee 2000V of ESD protection on all 300 Series products (they typically withstand up to 4000V). Even in providing this protection level, these diodes have a negligible impact on input capacitance. Addition of these diodes typically adds only tenths of picofarads to each product's input capacitance.

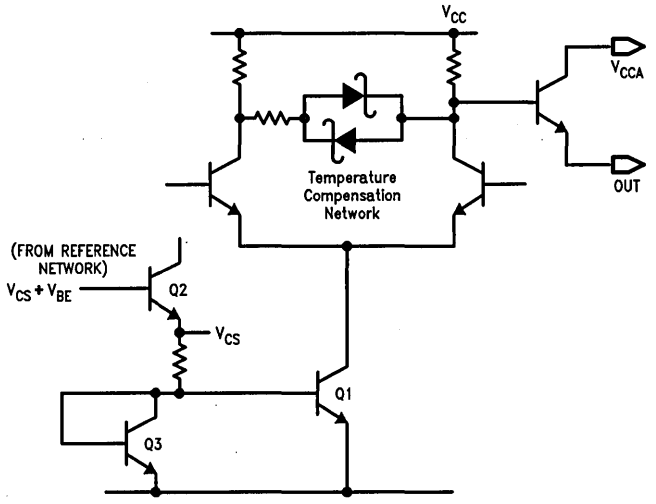

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FIGURE 1-5. 300 Series Widlar Current Sink

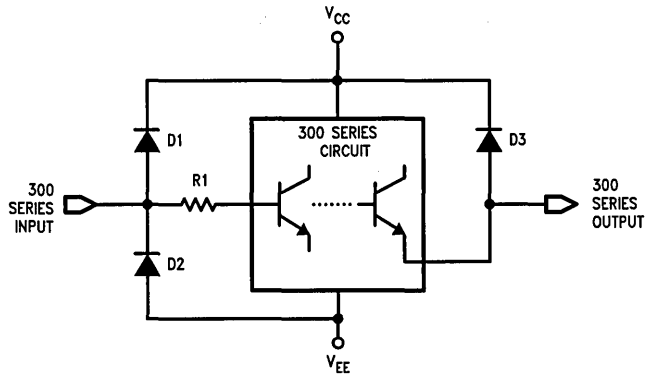

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FIGURE 1-6. 300 Series ESD Protection Diodes

Process Technology

FAST-LSI Process

The 300 Series family is fabricated using an advanced isoplanar technology called FAST-LSI. The FAST-LSI process is similar to FAST-Z, but also includes many improvements which enhance performance, manufacturability, and reliability. Metal alignments have been tightened, shortening the distance between base and emitter contacts. This reduces the base capacitance, giving F_Ts of 8 GHz vs 5 GHz for FAST-Z. Parasitic capacitances are also reduced, allowing products to be designed with lower power consumption.

The FAST-LSI process implements wafer planarization techniques to smooth the interconnect metal transitions, significantly reducing thermal stresses on the die when encapsulated in molded plastic packaging. In addition, these planarization techniques increase metal step coverage to typically 65% for first level metal and 75% for second level metal. Increased metal thicknesses over a step improve current density performance and circuit reliability. First layer metal step coverage is improved by the addition of bird's head planarization after the oxide isolation process. Second layer metal step coverage improvements are provided by a technique known as spun-on-glass, an interlayer dielectric planarization.

FAST-LSI is a fully ion-implanted process, providing more precise control over doping profiles. This not only improves device performance, but also allows tighter manufacturing tolerances on transistor gains and resistor values. These tighter tolerances were exploited in the design of F100K 300 Series to meet the same-speed, half-power targets for the product line. The field oxide in FAST-LSI is doped (vs. undoped in FAST-Z). This lowers current leakage even further while still maintaining the walled emitter structures featured in FAST-Z.

The metal structure of FAST-LSI is also improved. Platinum-silicide is used to provide ohmic contacts to N+ and P+ regions, as well as Schottky diode contacts to N− regions. The Schottky diodes are used in the design of the high-performance TTL output stages in the 300 Series ECL-TTL level translators. A titanium-tungsten layer is utilized as a diffusion barrier against aluminum migration into the underlying silicon. Finally, both first and second layer metal use a copper-doped aluminum metalization which enhances reliability by providing a high resistance to electromigration.

Compensation Network

The heart of F100K is fully compensated ECL.[1] The basic gate consists of three blocks—the current switch, the output emitter-followers, and the reference or bias network *(Figure 1-7)*. The current switch allows both conjunctive and disjunctive logic. The output emitter-followers provide high drive capability through impedance transformation and allows for increased logic swing. The bias network sets DC thresholds and current-source bias voltages. Temperature compensation at the gate output is achieved by incorporating a cross-connect branch between the complementary collector nodes of the current switch and driving the current source with a temperature insensitive bias network[2] *(Figure 1-8)*.

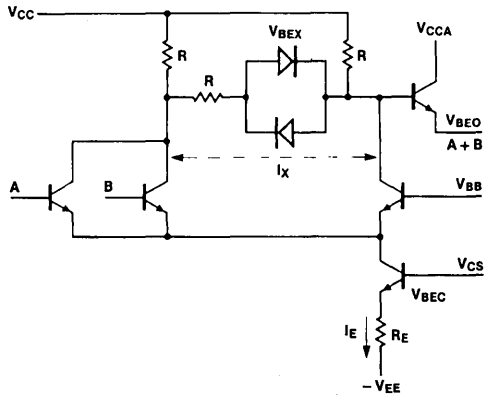

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FIGURE 1-8. Temperature Compensation

As junction temperature increases and the forward base-emitter voltage of the output emitter-follower decreases, the collector node of the current switch must become more negative. Since the current-source bias voltage, V_{CS}, is independent of temperature, the switch curent increases with temperature due to the temperature dependence of V_{BEC}. The combination of temperature controlled current, I_E, and the cross-connect branch current, I_X, forces the proper temperature coefficient at the collector node of the current switch to null out the V_{BEO} tracking coefficient.[3]

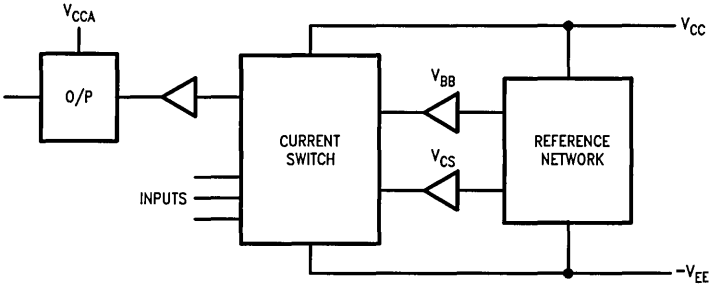

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FIGURE 1-7. ECL Gate

The schematic for the reference network displays a V_{BE1} amplifier in the bottom left corner *(Figure 1-9)*. Two base-emitter junctions are operated at different current densities, J1 and J2. The resulting voltage difference, V_{BE1} minus V_{BE2}, appears across R1 and is amplified by the ratio R2/R1. Note that R2 is used twice, once to generate V_{CS} and once to generate V_{BB}. The different current densities, J1 and J2, result in a positive temperature tracking coefficient across R2, which cancels the negative diode-tracking coefficient of V_{BE3} and V_{BE4}. The V_{CS} and the V_{BB} thus generated are temperature insensitive at the extrapolated bandgap voltage of silicon[1, 2] (approximately 1300 mV).[4] R_X in the V_{BE} amplifier compensates for process variations of β and ΔV_{BE}.[5] Voltage regulation is achieved through a shunt regulator shown at the right side of the schematic.

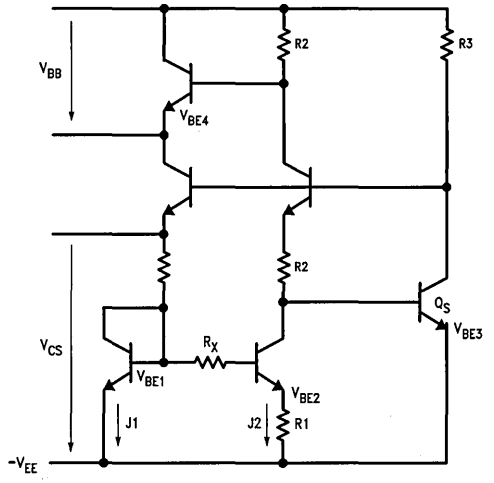

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FIGURE 1-9. Reference Network

Characteristics

F100K compatibility with existing ECL logic families and memories permit direct interface with slower logic families and ensures immediate memory availability. The typical logic swing is 800 mV *(Figure 1-10)* and all voltage levels are specified with a 50Ω load to −2V at all outputs to provide transmission line drive capability. However, the inherently low output impedance *(Figure 1-11)* and maximum specified output current, 50 mA, make 25Ω drive possible at any or all outputs. Alternately, of course, higher termination impedances or other termination schemes are also useful.

F100K exhibits relatively constant output levels and thresholds over the 0°C to +85°C specified temperature range and −4.2V to −4.8V specified voltage range *(Figure 1-12)*. V_{EE} power supply current is also constant over the specified voltage range *(Figure 1-13)*; therefore:

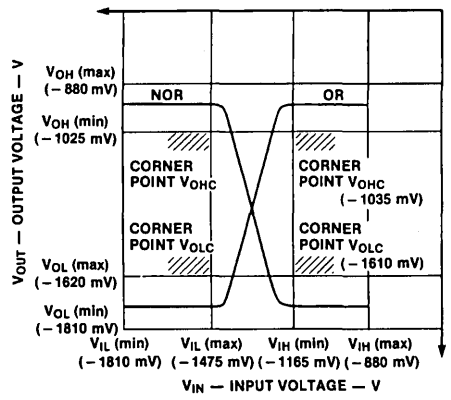

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FIGURE 1-10. Transfer Characteristics

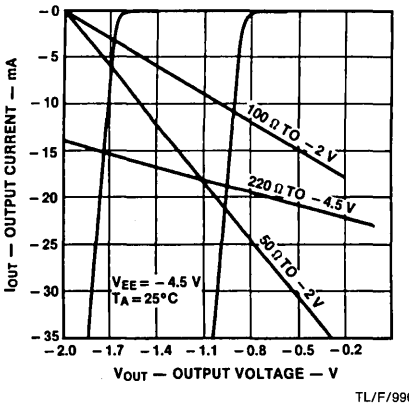

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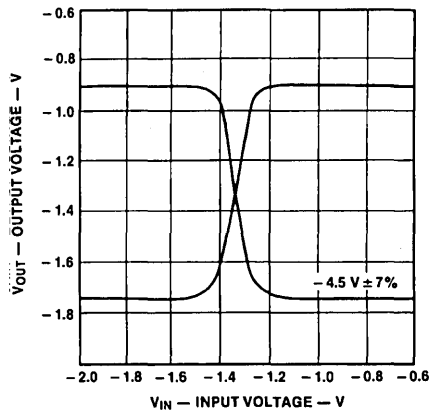
FIGURE 1-11. Output Characteristics vs Output Terminations

Fully Compensated ECL (over V_{EE} range)



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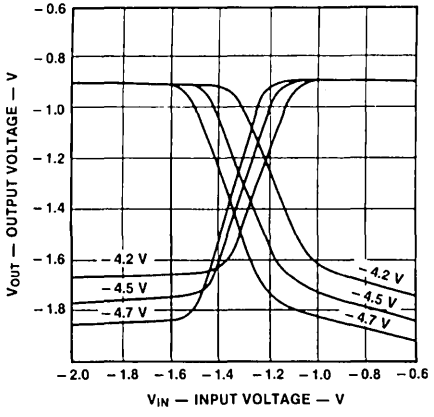
Uncompensated ECL (over V_{EE} range)



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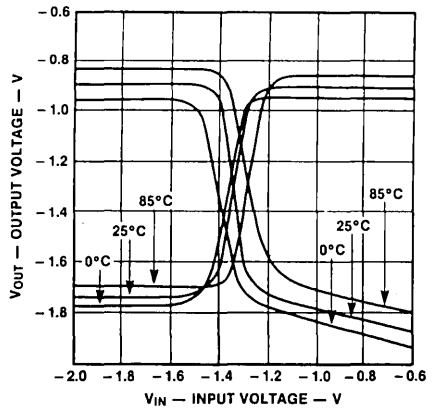
Uncompensated ECL (over temperature)



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Fully Compensated ECL (over temperature)

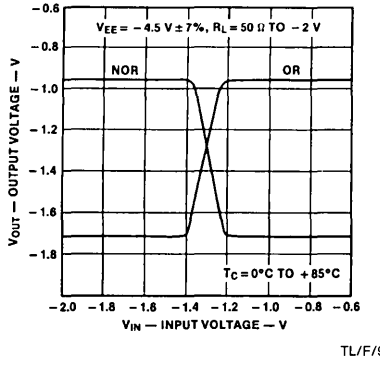

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FIGURE 1-12. Transfer Characteristics

- Propagation delay is relatively constant versus power supply voltage variations thus tightening the AC window.
- Power dissipation is a linear function of the supply voltage, reducing worst-case power consumption.

The typical propagation delay of an SSI gate function driving a 50Ω transmission line is 0.75 ns, including package, with a power dissipation of 40 mW resulting in a speed-power product of 30 pJ. For optimized MSI functions, the internal gates can dissipate < 10 mW with average propagation delay of < 0.5 ns, giving a power-speed product of < 5 pJ.

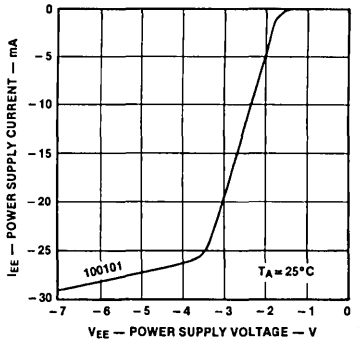

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FIGURE 1-13. Change in I_{EE} vs Change in V_{EE}

F100K has a tighter AC window over the wide range of environmental conditions; thus, the system timing requirements are eased and maximum system clock rates are increased. At the sacrifice of AC performance, the small-signal input impedance was conservatively designed to be positive-real over the frequency range encountered by any circuit input. This provides adequate damping to insure AC stability within the system.

Features

F100K ECL logic components are designed to be used in high-speed, low-noise systems and offer significant advantages over other logic families. Some of the important features and advantages are summarized below.

Low Propagation Delay

F100K ECL features gate delays that are typically 0.75 ns (750 picoseconds) with counters, registers and flip-flops operating in the 400–500 MHz range. When compared to other logic families such as Schottky TTL or slower ECL families, system performance can be doubled or tripled. Tighter AC distribution helps system timing requirements and increases system clock rates.

Moderate Edge Rates

Because of the nature of current mode switching which uses differential comparison techniques and avoids transistor storage delays, rise times can be controlled by internal time constants without sacrificing throughout delays. Slower rise times minimize ringing and reflections on interconnection wiring and simplify physical design. The typical edge rate for F100K ECL is 1V/ns, only about 80% of the edge rate of Schottky TTL. It can be shown that for ECL circuits, the natural rise and fall times are approximately equal to the propagation delay. This relationship is considered optimum for use in high-speed systems.

Wired-OR Capability

ECL outputs can be wired together where wiring rules permit, to form the positive logic-OR function, thus achieving an extra level of gating at no parts count expense. Data bussing and party line operations are facilitated by this features.

Complementary Outputs

A majority of F100K ECL logic elements have complementary outputs, providing numerous opportunities for reduction of package count and power consumption when mechanizing logic equations. Further, the system incurs no extra penalty in time delay since the complementary ECL outputs switch simultaneously.

A significant advantage to complementary outputs is that, since both the true and complement logic functions are available, I_{CC} imbalance can be minimized either by using both outputs in the design or merely terminating unused outputs. In this way, the constant current characteristic of ECL is not compromised and power supply noise is minimized.

Low Output Impedance, High Current Capacity

As operating speeds are increased to achieve the higher performance levels demanded of digital systems, ordinary wiring begins to exhibit distributed parameter characteristics, as opposed to a lumped capacitance nature at low speeds.

Characteristic impedances of normal wiring and printed circuit interconnections generally fall in the 50Ω to 250Ω range. With these low impedance lines and fast transitions, the signals are attenuated by the voltage divider action between the circuit output impedance and the characteristic impedance of the interconnection.

Voltage mode circuits have a HIGH state output impedance of from 50Ω to 150Ω and thus exhibit an output *stepped* characteristic, first reaching about 50% of final value and later reaching the final value in another *step*. F100K ECL output impedances under 10Ω insure a complete, full valued, signal into a transmission line. Also, F100K ECL outputs are specified to drive a 50Ω load (some devices are specified to drive a 25Ω load). Outputs are capable of supply 50 mA or more and can thus support the quiescent current required for passive terminations.

Convenient Data Transmission

The complementary high-current outputs of F100K ECL elements are well suited for driving twisted pair or other balanced lines in a differential mode, thereby enhancing field cancellation and minimizing crosstalk between subsystems.

High Common-Mode Noise Rejection

Differential line receivers provide common-mode noise rejection of 1V or more for induced and ground noise. Differential receiving requires less signal swing than single ended and thus allows more reliable interpretation of low signal swings.

Constant Supply Current

The supply current drain of F100K ECL elements is governed by one or more internal constant current sources supplying operating current for differential switches and level shifting networks. Since the current drain is the same regardless of the state of the switches, F100K ECL circuits present constant currents loads to power supplies *(see Complementary Outputs)*.

Low Power Loss in Stray Capacitance

Energy is consumed each time a capacitor is charged or discharged so the energy loss rate, or power, goes up with switching frequency. Since the energy stored in a capacitor is proportional to the square of the voltage and F100K ECL signal swings are four to five times less than those of TTL, power loss in stray capacitance may be an order of magnitude less than that of TTL.

Low Noise Generation

In ECL systems, power supply lines are not subjected to the large current spikes common with TTL designs. Inherently, ECL is a constant current family without the totem-pole structures found in TTL circuits which generate the large current spikes. Since ECL voltage swings are much smaller than TTL, the current spikes caused by charging and discharging stray capacitances are much smaller with ECL than with TTL of comparable edge rates.

Low Crosstalk

Induced noise signals are proportional to signal swings and edge rates. The lower swing and slower edge rate of F100K ECL results in low levels of crosstalk.

ESD Protection

The 300 Series is designed with Electrostatic Discharge (ESD) protection diodes. The diodes were designed to offer a minimum of 2000V (4000V typical) ESD protection on all devices. This protection is significantly higher than most other ECL families.

System Benefits

The National F100K ECL Family offers improvements over other ECL families such as voltage and temperature compensation, higher integration levels, improved packaging, planned pinouts, lower propagation delay and more complementary outputs. These improvements offer measurable advantages to the design(er) of high-performance systems.

Easier Engineering

Designers have increased confidence that designs realized in F100K will operate with good margins over voltage and temperature variations in prototypes, production models and field installations. Less effort need be expended doing detailed voltage and temperature calculations and testing. With noncompensated ECL, noise margins cannot be guaranteed unless both the receiving and transmitting circuit operate at the same temperature and V_{EE}. This can cause a problem when attempting to transfer a breadboard or prototype system to production.

Since output swings and input thresholds remain almost constant over temperature and V_{EE} variations, complex control systems for power supply levels and more-than-adquate cooling are not necessary with F100K. This results in a more economical and better operating system.

Circuit Design

F100K ECL benefits from sound, well-engineered circuit designs. All input pins exhibit *positive/real* input impedance to eliminate system oscillations. Input buffering is used to reduce loads on lines which drive multiple internal gates.

High Performance

The regulation and control of DC and AC parameters achieved by F100K ECL assures that signal timing and propagation delays in critical paths are relatively insensitive

to changes or gradients of temperature and supply voltage. Guardbands can be narrower, yet provide a higher degree of confidence due to the elimination of skew between output levels at one location and input threshold at another.

The consistency of response and security of noise margins permit operation at higher clock rates and thus increase system performance.

Easier Debugging

With F100K, debugging of systems can proceed more rapidly than with uncompensated ECL. When a cabinet or enclosure is opened for access in debugging, the resultant change in thermal conditions has almost no effect on F100K signal swings, propagation delays, edge rates or noise margins.

Flexibility

F100K is designed to operate at −4.5V for reduced power dissipation. If compatibility with other ECL families is a requirement, F100K 300 Series guarantees specifications between −4.2V and −5.7V due to its improved voltage compensation features.

Fan-In/Fan-Out

All F100K ECL outputs are specified to drive 50Ω transmission lines; this makes them suitable for driving very-high fanout loads. In addition, some F100K outputs are specified to drive 25Ω lines, which would be the case if a 50Ω party-line bus terminated at both ends were being driven.

System Design

F100K ECL was designed to be the ultimate standard packaged IC logic family. System design constraints were considered and the F100K family was designed for overall ease of system design and use while making the maximum use of the very fast propagation delay available.

Packaging

The F100K 300 Series ECL devices are offered in a wide variety of package options. The family was initially introduced with the F100K traditional 24-lead 400 mil wide, ceramic dual-in-line package (CDIP) and surface mount ceramic quad CERPAK (CQFP). These ceramic packages were needed for the now obsolete F100K 100 Series because of their excellent thermal performance.

The lower operating power of the 300 Series enabled plastic packaging to be used without the problem of exceeding the lower junction temperature required for those packages. The first plastic package to be introduced was the 28-lead plastic leaded chip carrier (PCC or PLCC). The four extra pins of this package were connected directly to the die paddle and used to improve the thermal performance.

A 24-lead plastic dual-in-line package (PDIP) was then introduced to offer a low cost alternative to the CDIP. The PDIP was designed to the same dimensions as the CDIP so that the same sockets could be utilized.

Finally, a 24-lead small outline package (SOIC) was introduced to round out the package options for the 300 Series. This package occupies approximately the same amount of board space as the PCC package, however, the package is much lower in height and the gull winged leads allow for easy visual inspection of solder joints.

The thermal operation for each of these packages varies slightly, for more detailed information please refer to the Power Distribution and Thermal considerations and the Qualification sections of this book.

Industrial Applications

The growing need for high performance logic in increasingly harsh environments has been addressed with an industrial grade version of the 300 Series ECL family. The industrial grade products offer the same high performance as the commercial grade products with additional testing conducted at −40°C, for a guaranteed operating temperature range of −40°C to +85°C. These products are ideal for industrial, fiber optic and communication applications which would be subjected to an uncontrolled environment.

Operation over the industrial temperature range is guaranteed by additional AC and DC testing. The DC levels of this family have been adjusted to reflect actual operation at −40°C (cold start) *Figure 1-14* shows the V_{OH}, V_{BB}, and V_{OL} Test Specification, the crosshatched area, and the actual data points taken on the 100301. These DC levels correspond to the entire family.

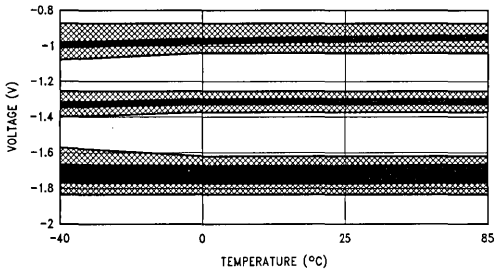

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FIGURE 1-14. DC Level Shift Over Temperature

The industrial grade products are only offered in an industry standard 28-lead PCC (PLCC) package. Additional AC and DC characteristic tables have been added to the individual device data sheets to specify extended temperature operation. Most of the 300 Series functions are available with industrial grade processing but check with your local National Semiconductor sales office for availability.

Military Applications

With the introduction of National's F100K ECL 300 Series comes the advent of F100K ECL in military applications. The special concerns addressed in the 300 Series design criteria enables this family to specify operation over the temperature range of −55°C to +125°C, and to comply fully with the requirements of MIL-STD-883.

As in the commercial world, with military systems becoming more complex, speed becomes a major consideration. Speeds which are pushing Schottky and CMOS technologies to their maximum performance limits, forcing designers to look to faster logic technologies. But speed, of course, is not the only consideration military designers have to contend with. Power consumption, package/function size, price, ESD susceptibility, radiation tolerance and operation in any of a number of harsh environments must be addressed by a military system designer, and all have been addressed in the design of the F100K 300 Series Family.

The relatively high speed-to-power product of the F100K ECL 300 Series Family allows these products to be used in a wide variety of applications. As systems begin to strain under the 30 MHz–40 MHz limits of some of the more conventional logic families, the 300 Series with its data rates exceeding 100 MHz, becomes a viable solution. The reduced power operation offered by the 300 Series product line eliminates the last barriers inhibiting the extensive usage of ECL in battery powered systems. Mixing F100K ECL 300 Series products with other logic families is also made easier with a variety of level translators and a wide operating voltage range of −4.2V to −5.7V.

Among the many other benefits this family offers is full temperature compensation and high noise immunity. Both of these features are extremely important in the environments military systems are subjected to, or standards to which they must comply. The temperature compensation circuit of F100K ECL ensures stable DC performance over temperature changes in the external environment, as well as temperature fluctuations within a system, or even on one circuit board. The high noise immunity provides clean operation and few system hiccups due to noise, even when operating in a noisy environment.

Standard Process Flow

In order to meet the strict processing and test requirements imposed by MIL-STD-883 and MIL-M-38510, National Semiconductor has developed the process flow shown in *Figure 1-15*. National subjects 100% of the F100K 300 Series ECL military-compliant products to this flow. All electrical tests are performed in compliance with National's published Table I electrical specifications. Although we make every effort to maintain the databook military electrical specifications, please contact your local sales office or Distributor for the current specifications.

Level S Capabilities

The most demanding environment for system applications is in space. Space systems are exposed to harsh physical and environmental conditions which can degrade system performance or alter functionality. Worse yet, these systems must endure this environment for many years with little—if any—opportunity for repair. System components must be highly reliable in order to meet these lifetime requirements.

National Semiconductor's facility in South Portland, Maine, has extensive experience in processing space-level prod-

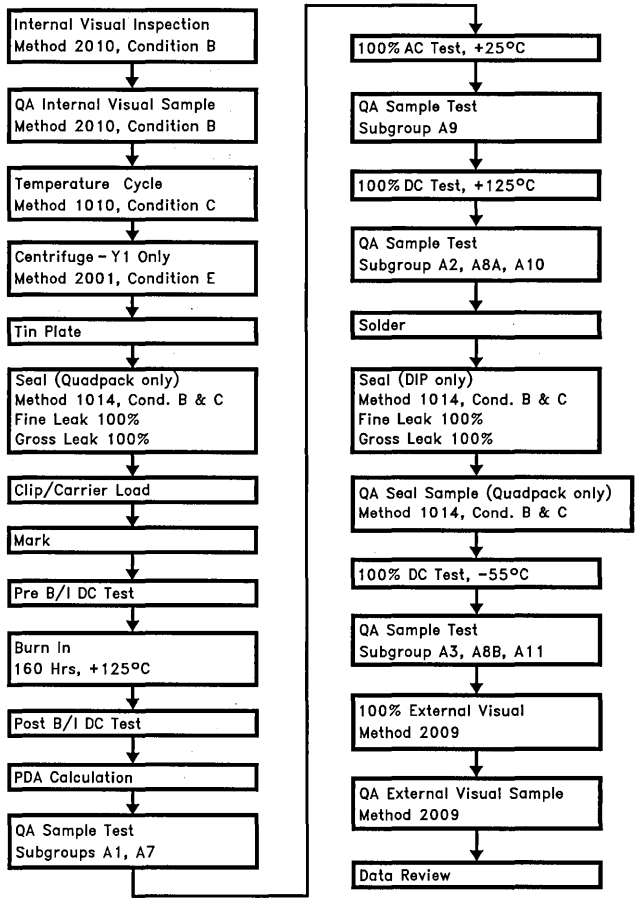

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FIGURE 1-15. MIL-STD-883 Process Flow

ucts. Years of designing, developing, and manufacturing space-level components has built an experienced team and facility dedicated to meeting the demands of space-level component processing.

DESC Level S-certified Fab, Assembly, and Test areas process JAN Level S-compliant devices as well as customer SCD space-level requirements. Flexible process flows for SCD requirements allow customers to tailor component processing to system requirements. Full SEM and WLA capabilities exist to ensure wafer-level compliancy to Level S requirements. PIND test, X-ray inspection, and radiation testing are performed in-house using dedicated laboratories. Read and record capability and delta calculations can be performed to provide data-to-document derating calculations for system life.

F100K 300 Series ECL is an excellent choice for space system designs with its low power operation, radiation tolerance, and suitability to harsh unregulated environments. To discuss your requirements for space system design, please contact your local sales office.

Radiation Capabilities and Test Results

Radiation survivability is a concern for many military, tactical, and space system designs. System exposure to man-made nuclear events and to naturally-occuring sources of radiation can result in transient and/or permanent changes to a device's material and electrical properties.

Starting at the conceptual stage is the most cost-effective approach to designing a radiation-hardened system. Utilizing product with inherent radiation tolerance eliminates the need for costly shielding.

National is an industry leader in radiation-resistant products. Its Mil/Aero logic Radiation Effects Laboratory (REL) in South Portland, Maine, certifies that products are resistant to defined levels of radiation. This lab is:

- Certified by NIST
- Licensed by the NRC to handle irradiated material
- Certified by DESC for Lab Suitability, which denotes that all testing and data generated is fully recognized and acceptable by all government agencies, their contractors, and sub-contractors.

Total dose testing is performed using a step-stressing methodology with National's AECL Gamma Cell 220 (Cobalt-60 source) in compliance with MIL-STD-883 Method 1019.3. Flexible process flows meet the needs of strategic, space, and tactical applications. Customer SCDs may specify either Level S or Level B process flows. Total dose radiation data and other data can be supplied with each order, certifying radiation resistance as specified in the applicable SCD.

National's F100K 300 Series ECL has undergone preliminary investigation to determine its minimum radiation hardness level. Total dose irradiation tests have been performed on the:

- 100355 Low Power Quad Multiplexer/Latch
- 100325 Low Power Hex ECL-to-TTL Translator

Preliminary radiation test results for both devices showed no functional failures and no parametric (AC and DC) failures up to the 1 Mrad(Si) level. All parametric results were within National's published Table I limits with minimal deltas.

Please note that these results are preliminary and based on limited testing of two device functions. We strongly recommend that total dose radiation-hardened-assured F100K 300 Series product be purchased only on a wafer-by-wafer basis.

For more detail about National's solutions to radiation hardness assurance, request a copy of National's *Radiation Resistance Guide* from your Distributor or local sales office.

Definitions of Symbols and Terms

AC SWITCHING PARAMETERS

Note: Skew parameter definitions can be found at the end of this section.

f_{COUNT} (Count Frequency/Toggle Frequency/Operating Frequency): The maximum repetition rate at which clock pulses may be applied to sequential circuit. Above this frequency the device may cease to function.

t_h (Hold Time): The interval immediately following the active transition of the timing pulse (usually the clock pulse) or following the transition of the control input to its latching level, during which the data to be recognized must be maintained at the input to ensure its continued recognition.

t_{PLH} (Propagation Delay Time): The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined LOW level to the defined HIGH level.

t_{PHL} (Propagation Delay Time): The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined HIGH level to the defined LOW level.

t_S (Setup Time): The interval immediately preceding the active transition of the timing pulse (usually the clock pulse) or preceding the transition of the control input to its latching level, during which the data to be recognized must be maintained at the input to ensure its recognition.

t_S (Release Time): The interval immediately preceding the active transition of the timing pulse (usually the clock pulse) or preceding the transition of the control input to its latching level, during which the master set or reset must be released (inactive) to ensure valid data is recognized.

t_{TLH} (Transition Time, LOW to HIGH): The time between two specified reference points on a waveform which is changing from LOW to HIGH.

t_{THL} (Transition Time, HIGH to LOW): The time between two specified reference points on a waveform which is changing from HIGH to LOW.

t_{pw} (Pulse Width): The time between 50 percent amplitude points on the leading and trailing edges of a pulse.

t_{PHZ} (Output Disable Time of a TRI-STATE® Output from High Level): The time between the 1.5V level on the input and a voltage 0.3V below the steady state output HIGH level with the TRI-STATE output changing from the defined HIGH level to a high impedance (OFF) state.

t_{PLZ} (Output Disable Time of a TRI-STATE Output from LOW Level): The time between the 1.5V level on the input and a voltage 0.3V above the steady state output LOW level with the TRI-STATE output changing from the defined LOW level to a high impedance (OFF) state.

t_{PZH} (Output Enable Time of a TRI-STATE Output to a HIGH Level): The time between the 1.5V levels of the input and output voltage waveforms with the TRI-STATE output changing from a high impedance (OFF) state to a HIGH level.

t_{PZL} (Output Enable Time of a TRI-STATE Output to a LOW Level): The time between the 1.5V levels of the input

and output voltage waveforms with the TRI-STATE output changing from a high impedance (OFF) state to a LOW level.

CURRENTS

Positive current is defined as conventional current flow *into* a device lead. Negative current is defined as conventional curent flow *out of* a device lead.

I_{EE} (Power Supply Current): The current required by each device from the V_{EE} supply. This value represents only the internal current required by the specified device, and does not include the current required for loads or terminations.

I_{TTL} (Supply Current): The current flowing into the V_{TTL} supply terminal of a circuit with the specified input conditions and the outputs open. When not specified, input conditions are chosen to guarantee worst-case operation.

I_{IH} (Input Current HIGH): The current flowing into a device lead with the specified V_{IH} applied to the input. This value represents the worst case DC input load that a device presents to a driving element.

I_{IL} (Input Current LOW): The current flowing into a device lead with the specified V_{IL} applied to the input.

I_{OH} (Output HIGH Current): The current flowing out of the output when it is in the HIGH state. For a turned-off open-collector output with a specified HIGH output voltage applied, the I_{OH} is the leakage current.

I_{OL} (Output LOW Current): The current flowing into an output when it is in the LOW state.

I_{OS} (Output Short Circuit Current): The current flowing out of a HIGH-state output when that output is short circuited to ground (or other specified potential).

I_{OZH} (Output OFF Current HIGH): The current flowing into a disable TRI-STATE output with a specified HIGH output voltage applied.

I_{OZL} (Output OFF Current LOW): The current flowing out of a disabled TRI-STATE output with a specified LOW output voltage applied.

VOLTAGES

All voltage values are referenced to V_{CC} (or ground) which is the most positive potential in an ECL system.

V_{BB} (Bias Voltage): The internally generated reference voltage which is used to set the input and output threshold levels.

V_{CC} (Circuit Ground): This is the most positive potential in the ECL system and it is used as the reference level for other voltages.

V_{CCA} (Separate Circuit Ground): The circuit ground for the buffered current switch. Outside the package, the V_{CC} and V_{CCA} leads should be connected to the common V_{CC} distribution. Internally, the separation of V_{CC} and V_{CCA} insures that any change in load currents during switching does not cause a change in V_{CC} through the small but finite inductance of the V_{CCA} bond wire and package lead.

V_{CS} (Current Source Voltage): The internally generated potential used to control the level of the active current source.

V_{EE} (Power Supply Voltage): This potential is the system power supply voltage and it is the most negative potential in the system.

V_{EES} (Substrate V_{EE}): These pins (on the PCC package only) provide extra thermal conduction paths, therefore reducing θ_{JA}. These pins must be connected to the V_{EE} plane or not connected at all.

V_{TTL} Supply Voltage: The range of the TTL power supply voltage over which the device is guaranteed to operate within the specified limits.

V_{IH} (Input Voltage HIGH): The range of input voltages that represents a logic HIGH level in the system.

$V_{IH\ (Max)}$: The most positive V_{IH}.

$V_{IH\ (Min)}$: The most negative V_{IH}. This value represents the guaranteed input HIGH threshold for the device.

V_{IL} (Input Voltage LOW): The range of input voltages that represents a logic LOW level in the system.

$V_{IL\ (Max)}$: The most positive V_{IL}. This value represents the guaranteed input LOW threshold for the device.

$V_{IL\ (Min)}$: The most negative V_{IL}.

V_{OH} (Output Voltage HIGH): The range of voltages at an output terminal with the specified output loading and with the inputs conditioned to establish a HIGH level at the output.

$V_{OH\ (Max)}$: The most positive V_{OH} under the specified input and loading conditions.

$V_{OH\ (Min)}$: The most negative V_{OH} under the specified input and loading conditions.

V_{OHC}: The output HIGH corner point or guaranteed HIGH threshold voltage with the inputs set to their respective threshold levels.

V_{OL} (Output Voltage LOW): The range of voltages at an output terminal with the specified output loading and with the inputs conditioned to establish a LOW level at the output.

$V_{OL\ (Max)}$: The most positive V_{OL} under the specified input and loading conditions.

$V_{OL\ (Min)}$: The most negative V_{OL} under the specified input and loading conditions.

V_{OLC}: The output LOW corner point or guaranteed LOW threshold voltage with the inputs set to their respective threshold levels.

V_{NH} (HIGH Level Noise Margin): Noise margin between the output HIGH level of a driving circuit and the input HIGH threshold level of its driven load. A conservative value for V_{NH} is the difference between V_{OHC} and $V_{IH\ (Min)}$.

V_{NL} (LOW Level Noise Margin): Noise margin between the output LOW level of a driving circuit and the input LOW threshold level of its driven load. A conservative value for V_{NL} is the difference between $V_{IL\ (Max)}$ and V_{OLC}.

References

1. H.H. Muller, W.K. Owens, and P.W.J. Verhofstadt, "Fully Compensated Emitter-Coupled Logic: Eliminating the Drawbacks of Conventional ECL", *IEEE Journal of Solid-State Circuits*, October 1973, pp. 362–367.
2. R.R. Marley, "On-Chip Temperature Compensation for ECL", *Electronic Products*, March 1, 1971.
3. V.A. Dhaka, J.E. Muschinske, and W.K. Owens, "Subnanosecond Emitter-Coupled Logic Gate Circuit Using Isoplanar II", *IEEE Journal of Solid-State Circuits*, October 1973, pp. 368–372.
4. R.J. Widlar, "New Developments in IC Voltage Regulators", *ISSCC Digital Technical Papers*, February 1970, pp. 157–159.
5. W.K. Owens, "Temperature Compensated Voltage Regulator Having Beta Compensating Means", United States Patent, No. 3,731,648, December 25, 1973.

National Semiconductor

Definitions of Output Skew Specifications

Test Philosophy

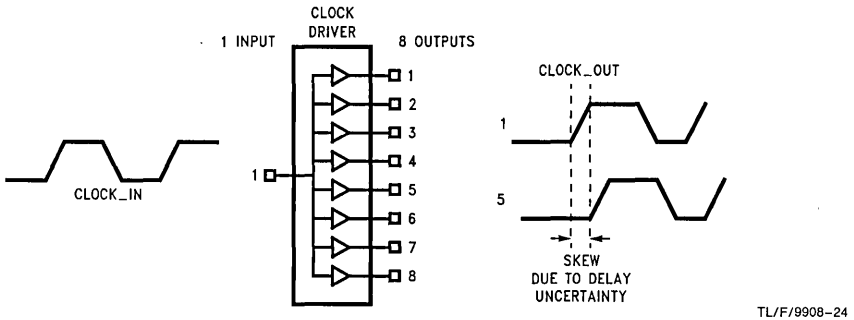
Minimizing output skew is a key design criteria in today's high-speed clocking schemes. National has incorporated new skew specifications into the F100K family of devices. National's test philosophy is to fully guarantee all the available skew specifications in order to help clock designers optimize their clock budgets.

CLOCK SKEW

Skew is the variation of propagation delay differences between output clock signal(s).

Example:

If signal appears at out #1 in 3 ns and in 4 ns at output #5, the skew is 1 ns.



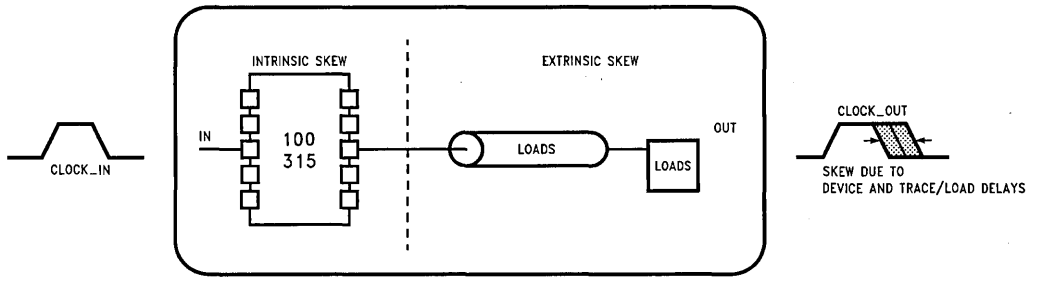
TL/F/9908–24

FIGURE 1-16. Clock Output Skew

Without skew specifications, a designer must approximate timing uncertainties. Skew specifications have been created to help clock designers define output propagation delay differences within a given device, duty cycle and device-to-device delay differences.

SOURCES OF CLOCK SKEW

Total system clock skew includes intrinsic and extrinsic skew. Intrinsic skew is defined as the differences in delays between the outputs of device(s). Extrinsic skew is defined as the differences in trace delays and loading conditions.



TL/F/9908–25

FIGURE 1-17. Sources of Clock Skew

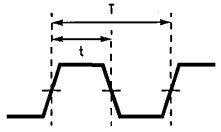
Example: 50 MHz Clock signal distribution on a PC Board.

50 MHz signals produces 20 ns clock cycles
Total system skew budget = 10% of clock cycle = 2 ns* → 2 ns
If extrinsic skew = 1 ns → − 1 ns
Device skew (intrinsic skew) must be less than 1 ns! ← 1 ns

*Clock Design *Rule of thumb.*

CLOCK DUTY CYCLE

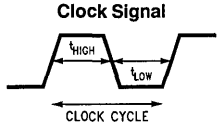
- Clock Duty Cycle is a measure of the amount of time a signal is *High* or *Low* in a given clock cycle.



TL/F/9908–26

Duty Cycle = t/T * 100%

FIGURE 1-18. Duty Cycle Calculation



TL/F/9908–27

FIGURE 1-19. Clock Cycle

- Clock skew effects the Duty Cycle of a signal.

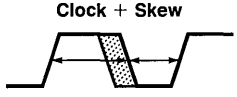


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FIGURE 1-20. Clock Skew

Example:

t_{HIGH} and t_{LOW} are each 50% of the clock cycle therefore the clock signal has a Duty Cycle of 50/50%.

Example: 50 MHz clock distribution on a PC board.

Skew must be guaranteed less than 1 ns at 50 MHz to achieve 55/45% Duty Cycle requirements of core silicon!

TABLE 1-I

System Frequency	Skew	t_{HIGH}	t_{LOW}	Duty Cycle		
50 MHz	0 ns	10 ns	10 ns	50/50%	←	Ideal Duty Cycle (50/50%) occurs for zero skew.
50 MHz	2 ns	12 ns	8 ns	60/40%		
50 MHz	1 ns	11 ns	9 ns	55/45%		
33 MHz	2 ns	17 ns	15 ns	55/45%	←	Note that at lower frequencies, the skew budget is not as tight and skew does not affect the Duty Cycle as severely as seen at higher frequencies.

Definition of Parameters

t_{OSLH}, t_{OSHL} (Common Edge Skew)

t_{OSHL} and t_{OSLH} are parameters which describe the delay from one driver to another on the same chip. This specification is the worst-case number of the delta between the fastest to the slowest path on the same chip. An example of where this parameter is critical is the case of the cache controller and the CPU, where both units use the same transition of the clock. In order for the CPU and the controller to be synchronized, $t_{OSLH/HL}$ needs to be minimized.

Definition

t_{OSHL}, t_{OSLH} (Output Skew for High-to-Low Transitions):

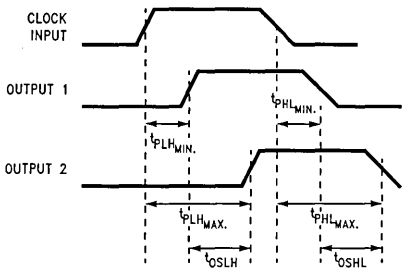
$t_{OSHL} = |t_{PHL_{MAX}} - t_{PHL_{MIN}}|$

Output Skew for Low-to-High Transitions:

$t_{OSLH} = |t_{PLH_{MAX}} - t_{PLH_{MIN}}|$

Propagation delays are measured across the outputs of any given device.

Example



TL/F/9908–29

FIGURE 1-21. t_{OSLH}, t_{OSHL}

Definition of Parameters (Continued)

t_{PS} (Pin Skew or Transition Skew)

t_{PS}, describes opposite edge skews, i.e., the difference between the delay of the low-to-high transition and the high-to-low transition on the same pin. This parameter is measured across all the outputs (drivers) on the same chip, the worst (largest delta) number is the guaranteed specification. Ideally this number needs to be 0 ns. Effectively, 0 ns means that there is no degradation of the input signal's Duty Cycle.

Many of today's microprocessors require a minimum of a 45:55 percent Duty Cycle. System clock designers typically achieve this in one of two ways. The first method is with an expensive crystal oscillator which meets the 45:55 percent Duty Cycle requirement. An alternative approach is to use a less expensive crystal oscillator and implement a divide by two function. Some microprocessors have addressed this by internally performing the divide by two.

Since Duty Cycle is defined as a percentage, the room for error becomes tighter as the system clock frequency increases. For example in a 25 MHz system clock with a 45:55 percent Duty Cycle requirement, t_{PS} cannot exceed a maximum of 4 ns (t_{PLH} of 18 ns and t_{PLH} of 22 ns) and still meet the Duty Cycle requirement. However for a 50 MHz system clock with a 45:55 percent Duty Cycle requirement, t_{PS} cannot exceed a maximum of 2 ns (t_{PLH} of 9 ns and t_{PHL} of 11 ns) and still meet the Duty Cycle requirement. This analysis assumes a perfect 50:50 percent Duty Cycle input signal.

Definition

t_{PS} (Pin Skew or Transition Skew):

$t_{PS} = |t_{PHL} - t_{PLH}|$

Both high-to-low and low-to-high propagation delays are measured at each output pin across the given device.

Example

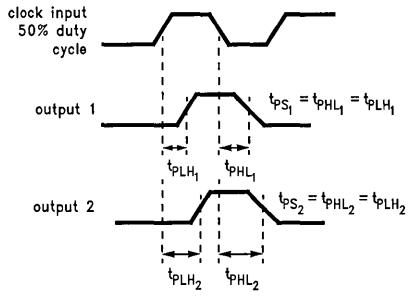


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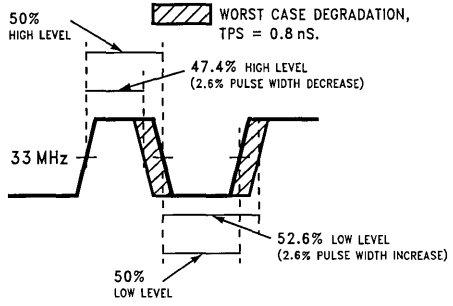
FIGURE 1-22. t_{PS}

Example: A 33 MHz, 50/50% duty cycle input signal would be degraded by 2.6% due to a t_{PS} = 0.8 ns. (See Table and Illustration below.)

Note: Output symmetry degradation also depends on input duty cycle.

TABLE 1-III. Duty Cycle Degradation of 33 MHz

f (MHz)	Input			Device	Output			% Δ DC Input to Output
	DC Input	t_{IN} (ns)	T_{IN} (ns)	t_{PS} (ns)	t_{OUT} (ns)	T_{OUT} (ns)	DC Output	
33	**50%/50%**	15.15/15.15	30.3	**0.8**	14.35/15.95	30.3	47.4%/52.6%	**2.6%**
	45%/55%	13.6/16.6	30.3	**1.5**	12.1/18.1	30.3	39.9%/60.1%	**5.1%**



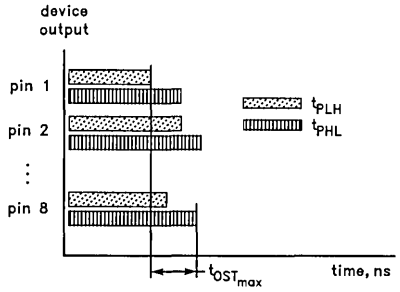
TL/F/9908–31

FIGURE 1-23. Pulse Width Degradation

Definition of Parameters (Continued)

t_{OST} (Opposite Edge Skew)

t_{OST} defines the difference between the fastest and the slowest of both transitions within a given chip. Given a specific system with two components, one being positive-edge triggered and one being negative-edge triggered, t_{OST} helps to calculate the required delay elements if synchronization of the positive- and negative-clock edges is required.



TL/F/9908–32

FIGURE 1-24. t_{OST}

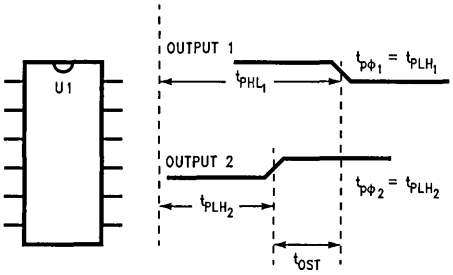
Definition

t_{OST} (Opposite Edge Skew):

$$t_{OST} = |t_{P\varphi m} - t_{P\varphi n}|$$

where φ is any edge transition (high-to-low or low-to-high) measured between any two outputs (m or n) within any given device.

Example



TL/F/9908–33

FIGURE 1-25. t_{OST}

Section 2

F100K 200 and 300 Series Datasheets

Section 2 Contents

National Semiconductor

PRELIMINARY

100201
Low Power 2-Input OR/NOR Gate/Inverter

General Description

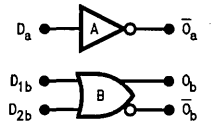
The 100201 is a 2-input OR/NOR Gate and a single Inverter Gate in an eight pin SOIC package. All inputs have 50 kΩ pull-down resistors and all outputs are buffered. The 100201 is ideal for single gate needs or for use as the feedback loop of a crystal oscillator circuit.

Features

- Small 8 lead 150 mil SOIC package
- 2000V ESD protection
- 300 MHz minimum F toggle
- Temperature compensated
- Voltage compensated operating range = −4.2V to −5.7V V_{EE}

Ordering Code: See Section 6

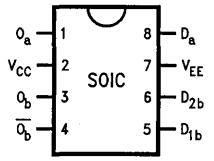
Logic Symbol



TL/F/11000–1

Pin Names	Description
D_a, D_{1b}, D_{2b}	Data Inputs
O_b	Data Outputs
$\overline{O}_a$, $\overline{O}_b$	Complementary Data Outputs

Pin Assignment



TL/F/11000–2

Absolute Maximum Ratings

Above which the useful life may be impaired (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature (T_{STG})	−65°C to +150°C
Maximum Junction Temperature (T_J)	
Ceramic	+175°C
Plastic	+150°C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Output Current (DC Output HIGH)	−50 mA
ESD (Note 2)	≥2000V

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: ESD testing conforms to MIL-STD-883, Method 3015.

Recommended Operating Conditions

Case Temperature (T_C)	
Commercial	0°C to +85°C
Industrial	−40°C to +85°C
Military	−55°C to +125°C
Supply Voltage (V_{EE})	−5.7V to −4.2V

Commercial Version

DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions	
V_{OH}	Output HIGH Voltage	−1025	−955	−870	mV	V_{IN} = $V_{IH(Max)}$ or $V_{IL(Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830	−1705	−1620	mV		
V_{OHC}	Output HIGH Voltage	−1035			mV	V_{IN} = $V_{IH(Min)}$ or $V_{IL(Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610	mV		
V_{IH}	Input HIGH Voltage	−1165		−870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1830		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL(Min)}$	
I_{IH}	Input HIGH Current			240	μA	V_{IN} = $V_{IH(Max)}$	
I_{EE}	Power Supply Current	−29	−17	−15	mA	Inputs Open	

Note 3: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

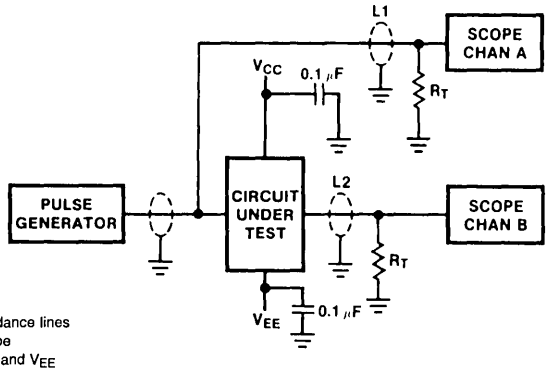
SOIC AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Data to Output	0.4	1.10	0.4	1.15	0.4	1.20	ns	*Figures 1* and *2* (Note 1)
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.40	1.20	0.40	1.20	0.40	1.20	ns	*Figures 1* and *2*

Note 1: The propagation delay specified is for single output switching. Delays may vary up to 100 ps with multiple outputs switching.

Test Circuitry

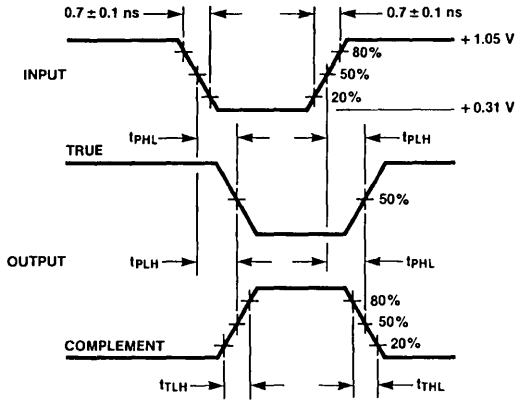


Notes:
V_{CC}, V_{CCA} = +2V, V_{EE} = −2.5V
L1 and L2 = equal length 50Ω impedance lines
R_T = 50Ω terminator internal to scope
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
All unused outputs are loaded with 50Ω to GND
C_L = Fixture and stray capacitance ≤ 3 pF

TL/F/11000–3

FIGURE 1. AC Test Circuit

Switching Waveforms



TL/F/11000–4

FIGURE 2. Propagation Delay and Transition Times

National Semiconductor

100301
Low Power Triple 5-Input OR/NOR Gate

General Description

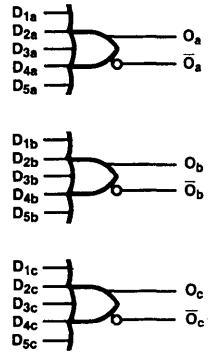
The 100301 is a monolithic triple 5-input OR/NOR gate. All inputs have 50 kΩ pull-down resistors and all outputs are buffered.

Features

- 23% power reduction of the 100101
- 2000V ESD protection
- Pin/function compatible with 100101
- Voltage compensated operating range = −4.2V to −5.7V
- Available to MIL-STD-883
- Available to industrial grade temperature range

Ordering Code: See Section 6

Logic Symbol

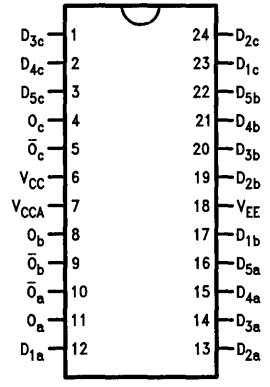


TL/F/10579–1

Pin Names	Description
D_{na}, D_{nb}, D_{nc}	Data Inputs
O_a, O_b, O_c	Data Outputs
$\overline{O}_a$, $\overline{O}_b$, $\overline{O}_c$	Complementary Data Outputs

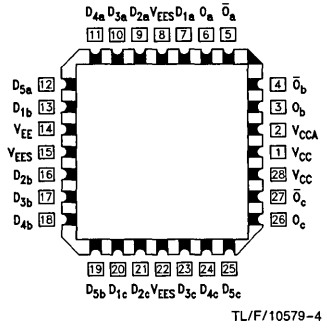
Connection Diagrams

24-Pin DIP/SOIC



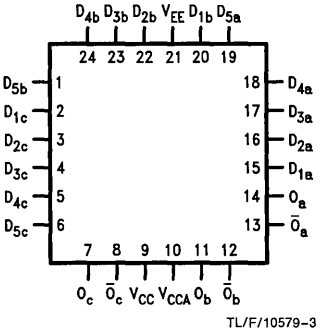
TL/F/10579–2

28-Pin PCC



TL/F/10579–4

24-Pin Quad Cerpak



TL/F/10579–3

Absolute Maximum Ratings

Above which the useful life may be impaired (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature (T_{STG})	−65°C to +150°C
Maximum Junction Temperature (T_J)	
Ceramic	+175°C
Plastic	+150°C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Output Current (DC Output HIGH)	−50 mA
ESD (Note 2)	≥2000V

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: ESD testing conforms to MIL-STD-883, Method 3015.

Recommended Operating Conditions

Case Temperature (T_C)	
Commercial	0°C to +85°C
Industrial	−40°C to +85°C
Military	−55°C to +125°C
Supply Voltage (V_{EE})	−5.7V to −4.2V

Commercial Version

DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions	
V_{OH}	Output HIGH Voltage	−1025	−955	−870	mV	V_{IN} = $V_{IH(Max)}$ or $V_{IL(Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830	−1705	−1620	mV		
V_{OHC}	Output HIGH Voltage	−1035			mV	V_{IN} = $V_{IH(Min)}$ or $V_{IL(Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610	mV		
V_{IH}	Input HIGH Voltage	−1165		−870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1830		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL(Min)}$	
I_{IH}	Input HIGH Current			240	μA	V_{IN} = $V_{IH(Max)}$	
I_{EE}	Power Supply Current	−29	−17	−15	mA	Inputs Open	

Note 3: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DIP AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Data to Output	0.50	1.10	0.50	1.15	0.50	1.20	ns	*Figures 1* and *2* (Note 1)
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.40	1.20	0.40	1.20	0.40	1.20	ns	*Figures 1* and *2*

Note 1: The propagation delay specified is for single output switching. Delays may vary up to 100 ps with multiple outputs switching.

Commercial Version (Continued)

SOIC, PCC and Cerpak AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Data to Output	0.50	1.00	0.50	1.05	0.50	1.10	ns	*Figures 1* and *2* (Note 2)
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.40	1.10	0.40	1.10	0.40	1.10	ns	*Figures 1* and *2*
t_{OSHL}	Maximum Skew Common Edge Output-to-Output Variation Data to Output Path		240		240		240	ps	PCC Only (Note 1)
t_{OSLH}	Maximum Skew Common Edge Output-to-Output Variation Data to Output Path		330		330		330	ps	PCC Only (Note 1)
t_{OST}	Maximum Skew Opposite Edge Output-to-Output Variation Data to Output Path		330		330		330	ps	PCC Only (Note 1)
t_{PS}	Maximum Skew Pin (Signal) Transition Variation Data to Output Path		230		230		230	ps	PCC Only (Note 1)

Note 1: Output-to-Output Skew is defined as the absolute value of the difference between the actual propagation delay for any outputs within the same packaged device. The specifications apply to any outputs switching in the same direction either HIGH to LOW (t_{OSHL}), or LOW to HIGH (t_{OSLH}), or in opposite directions both HL and LH (t_{OST}). Parameters t_{OST} and t_{PS} guaranteed by design.

Note 2: The propagation delay specified is for single output switching. Delays may vary up to 100 ps with multiple outputs switching.

Industrial Version

PCC DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = −40°C to +85°C (Note 3)

Symbol	Parameter	T_C = −40°C		T_C = 0°C to +85°C		Units	Conditions	
		Min	Max	Min	Max			
V_{OH}	Output HIGH Voltage	−1085	−870	−1025	−870	mV	V_{IN} = $V_{IH(Max)}$ or $V_{IL(Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830	−1575	−1830	−1620	mV		
V_{OHC}	Output HIGH Voltage	−1095		−1035		mV	V_{IN} = $V_{IH(Min)}$ or $V_{IL(Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage		−1565		−1610	mV		
V_{IH}	Input HIGH Voltage	−1170	−870	−1165	−870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1830	−1480	−1830	−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50		0.50		μA	V_{IN} = $V_{IL(Min)}$	
I_{IH}	Input HIGH Current		240		240	μA	V_{IN} = $V_{IH(Max)}$	
I_{EE}	Power Supply Current	−29	−15	−29	−15	mA	Inputs Open	

Note 3: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

Industrial Version (Continued)

PCC AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = −40°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Data to Output	0.40	1.00	0.50	1.05	0.50	1.10	ns	*Figures 1* and *2* (Note 1)
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.30	1.10	0.40	1.10	0.40	1.10	ns	*Figures 1* and *2*

Note 1: The propagation delay specified is for single output switching. Delays may vary up to 100 ps with multiple outputs switching.

Military Version

DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = −55°C to +125°C

Symbol	Parameter	Min	Max	Units	T_C	Conditions		Notes
V_{OH}	Output HIGH Voltage	−1025	−870	mV	0°C to +125°C	V_{IN} = $V_{IH(Max)}$ or V_{IL} (Min)	Loading with 50Ω to −2.0V	1, 2, 3
		−1085	−870	mV	−55°C			
V_{OL}	Output LOW Voltage	−1830	−1620	mV	0°C to +125°C			
		−1830	−1555	mV	−55°C			
V_{OHC}	Output HIGH Voltage	−1035		mV	0°C to +125°C	V_{IN} = $V_{IH(Min)}$ or V_{IL} (Max)	Loading with 50Ω to −2.0V	1, 2, 3
		−1085		mV	−55°C			
V_{OLC}	Output LOW Voltage		−1610	mV	0°C to +125°C			
			−1555	mV	−55°C			
V_{IH}	Input HIGH Voltage	−1165	−870	mV	−55°C to +125°C	Guaranteed HIGH Signal for All Inputs		1, 2, 3, 4
V_{IL}	Input LOW Voltage	−1830	−1475	mV	−55°C to +125°C	Guaranteed LOW Signal for All Inputs		1, 2, 3, 4
I_{IL}	Input LOW Current	0.50		μA	−55°C to +125°C	V_{EE} = −4.2V V_{IN} = $V_{IL(Min)}$		1, 2, 3
I_{IH}	Input HIGH Current		240	μA	0°C to +125°C	V_{EE} = −5.7V V_{IN} = V_{IH} (Max)		1, 2, 3
			340	μA	−55°C			
I_{EE}	Power Supply Current	−32	−12	mA	−55°C to +125°C	Inputs Open		1, 2, 3

Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals −55°C), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 2: Screen tested 100% on each device at −55°C, +25°C, and +125°C, Subgroups 1, 2, 3, 7, and 8.

Note 3: Sample tested (Method 5005, Table I) on each manufactured lot at −55°C, +25°C, and +125°C, Subgroups A1, 2, 3, 7, and 8.

Note 4: Guaranteed by applying specified input condition and testing V_{OH}/V_{OL}.

Military Version (Continued)

AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = −55°C		T_C = +25°C		T_C = +125°C		Units	Conditions	Notes
		Min	Max	Min	Max	Min	Max			
t_{PLH} t_{PHL}	Propagation Delay Data to Output	0.25	1.70	0.30	1.50	0.30	1.80	ns	*Figures 1* and *2*	1, 2, 3, 5
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.30	1.20	0.30	1.20	0.30	1.20	ns		4

Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals −55°C), then testing immediately after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

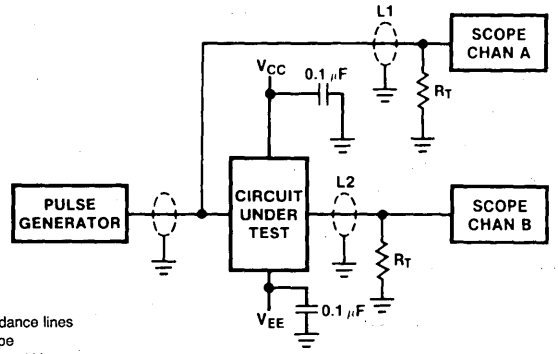
Note 2: Screen tested 100% on each device at +25°C temperature only, Subgroup A9.

Note 3: Sample tested (Method 5005, Table I) on each manufactured lot at +25°C, Subgroup A9, and at +125°C and −55°C temperatures, Subgroups A10 and A11.

Note 4: Not tested at +25°C, +125°C, and −55°C temperature (design characterization data).

Note 5: The propagation delay specified is for single output switching. Delays may vary up to 100 ps with multiple outputs switching.

Test Circuitry

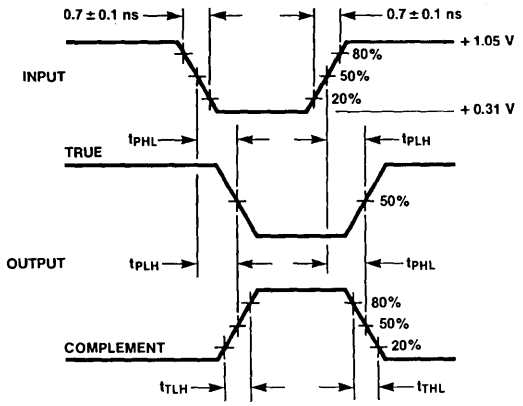


TL/F/10579–5

Notes:
V_{CC}, V_{CCA} = +2V, V_{EE} = −2.5V
L1 and L2 = equal length 50Ω impedance lines
R_T = 50Ω terminator internal to scope
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
All unused outputs are loaded with 50Ω to GND
C_L = Fixture and stray capacitance ≤ 3 pF

FIGURE 1. AC Test Circuit

Switching Waveforms



TL/F/10579–6

FIGURE 2. Propagation Delay and Transition Times

National Semiconductor

100302
Low Power Quint 2-Input OR/NOR Gate

General Description

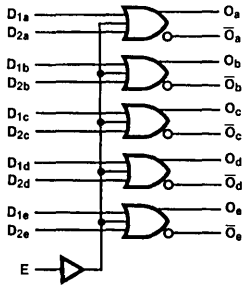
The 100302 is a monolithic quint 2-input OR/NOR gate with common enable. All inputs have 50 kΩ pull-down resistors and all outputs are buffered.

Features

- 43% power reduction of the 100102
- 2000V ESD protection
- Pin/function compatible with 100102
- Voltage compensated operating range = −4.2V to −5.7V
- Available to MIL-STD-883
- Available to industrial grade temperature range

Ordering Code: See Section 6

Logic Symbol



TL/F/10580–1

Pin Names	Description
D_{na}–D_{ne}	Data Inputs
E	Enable Input
O_a–O_e	Data Outputs
$\overline{O}_a$–$\overline{O}_e$	Complementary Data Outputs

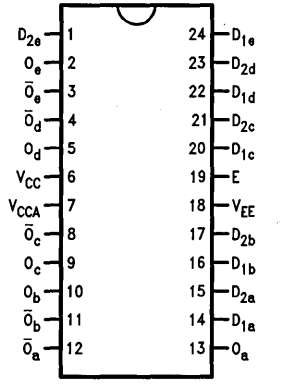
Truth Table

D_{1X}	D_{2X}	E	O_X	$\overline{O}_X$
L	L	L	L	H
L	L	H	H	L
L	H	L	H	L
L	H	H	H	L
H	L	L	H	L
H	L	H	H	L
H	H	L	H	L
H	H	H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level

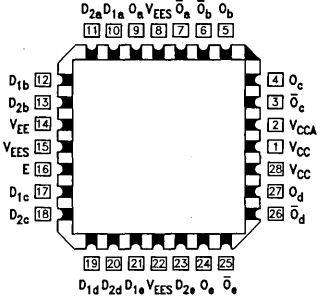
Connection Diagrams

24-Pin DIP/SOIC



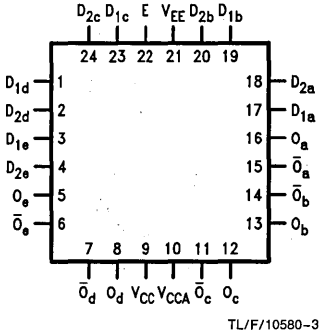
TL/F/10580–2

28-Pin PCC



TL/F/10580–4

24-Pin Quad Cerpak



TL/F/10580–3

Absolute Maximum Ratings

Above which the useful life may be impaired (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature (T_{STG})	−65°C to +150°C
Maximum Junction Temperature (T_J)	
Ceramic	+175°C
Plastic	+150°C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Output Current (DC Output HIGH)	−50 mA
ESD (Note 2)	≥2000V

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: ESD testing conforms to MIL-STD-883, Method 3015.

Recommended Operating Conditions

Case Temperature (T_C)	
Commercial	0°C to +85°C
Industrial	−40°C to +85°C
Military	−55°C to +125°C
Supply Voltage (V_{EE})	−5.7V to −4.2V

Commercial Version

DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions	
V_{OH}	Output HIGH Voltage	−1025	−955	−870	mV	V_{IN} = $V_{IH(Max)}$ or $V_{IL(Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830	−1705	−1620	mV		
V_{OHC}	Output HIGH Voltage	−1035			mV	V_{IN} = $V_{IH(Min)}$ or $V_{IL(Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610	mV		
V_{IH}	Input HIGH Voltage	−1165		−870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1830		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL(Min)}$	
I_{IH}	Input HIGH Current			240	μA	V_{IN} = $V_{IH(Max)}$	
I_{EE}	Power Supply Current	−45	−36	−20	mA	Inputs Open	

Note 3: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DIP AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Data to Output	0.50	1.15	0.50	1.15	0.50	1.25	ns	*Figures 1* and *2* (Note 1)
t_{PLH} t_{PHL}	Propagation Delay Enable to Output	0.70	1.90	0.70	1.90	0.80	2.00	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.40	1.20	0.40	1.20	0.40	1.20	ns	*Figures 1* and *2*

Note 1: The propagation delay specified is for single output switching. Delays may vary up to 100 ps with multiple outputs switching.

Commercial Version (Continued)

SOIC, PCC and Cerpak AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Data to Output	0.50	1.05	0.50	1.05	0.50	1.15	ns	*Figures 1* and *2* (Note 2)
t_{PLH} t_{PHL}	Propagation Delay Enable to Output	0.70	1.80	0.70	1.80	0.80	1.90	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.40	1.10	0.40	1.10	0.40	1.10	ns	*Figures 1* and *2*
t_{OSHL}	Maximum Skew Common Edge Output-to-Output Variation Data to Output Path		250		250		250	ps	PCC Only (Note 1)
t_{OSHL}	Maximum Skew Common Edge Output-to-Output Variation Enable to Output Path		310		310		310	ps	PCC Only (Note 1)
t_{OSLH}	Maximum Skew Common Edge Output-to-Output Variation Data to Output Path		200		200		200	ps	PCC Only (Note 1)
t_{OSLH}	Maximum Skew Common Edge Output-to-Output Variation Enable to Output Path		330		330		330	ps	PCC Only (Note 1)
t_{OST}	Maximum Skew Opposite Edge Output-to-Output Variation Data to Output Path		250		250		250	ps	PCC Only (Note 1)
t_{OST}	Maximum Skew Opposite Edge Output-to-Output Variation Enable to Output Path		330		330		330	ps	PCC Only (Note 1)
t_{PS}	Maximum Skew Pin (Signal) Transition Variation Data to Output Path		200		200		200	ps	PCC Only (Note 1)
t_{PS}	Maximum Skew Pin (Signal) Transition Variation Enable to Output Path		280		280		280	ps	PCC Only (Note 1)

Note 1: Output-to-Output Skew is defined as the absolute value of the difference between the actual propagation delay for any outputs within the same packaged device. The specifications apply to any outputs switching in the same direction either HIGH to LOW (t_{OSHL}), or LOW to HIGH (t_{OSLH}), or in opposite directions both HL and LH (t_{OST}). Parameters t_{OST} and t_{PS} guaranteed by design.

Note 2: The propagation delay specified is for single output switching. Delays may vary up to 100 ps with multiple outputs switching.

Industrial Version

PCC DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = −40°C to +85°C (Note 3)

Symbol	Parameter	T_C = −40°C		T_C = 0°C to +85°C		Units	Conditions	
		Min	Max	Min	Max			
V_{OH}	Output HIGH Voltage	−1085	−870	−1025	−870	mV	V_{IN} = $V_{IH(Max)}$ or $V_{IL(Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830	−1575	−1830	−1620			
V_{OHC}	Output HIGH Voltage	−1095		−1035		mV	V_{IN} = $V_{IH(Min)}$ or $V_{IL(Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage		−1565		−1610			
V_{IH}	Input HIGH Voltage	−1170	−870	−1165	−870	mV	Guaranteed HIGH Signal for ALL Inputs	
V_{IL}	Input LOW Voltage	−1830	−1480	−1830	−1475	mV	Guaranteed LOW Signal for ALL Inputs	
I_{IL}	Input LOW Current	0.05		0.05		μA	V_{IN} = $V_{IL(Min)}$	
I_{IH}	Input HIGH Current		300		240	μA	V_{IN} = $V_{IH(Max)}$	
I_{EE}	Power Supply Current	−45	−20	−45	−20	mA	Inputs Open	

Note 3: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under the "worst case" conditions.

Industrial Version (Continued)

PCC AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = −40°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Data to Output	0.40	1.05	0.50	1.05	0.50	1.15	ns	*Figures 1* and *2* (Note 1)
t_{PLH} t_{PHL}	Propagation Delay Enable to Output	0.70	1.80	0.70	1.80	0.80	1.90	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.30	1.10	0.40	1.10	0.40	1.10	ns	*Figures 1* and *2*

Note 1: The propagation delay specified is for single output switching. Delays may vary up to 200 ps with multiple outputs switching.

Military Version

DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = −55°C to +125°C (Note 3)

Symbol	Parameter	Min	Max	Units	T_C	Conditions		Notes
V_{OH}	Output HIGH Voltage	−1025	−870	mV	0°C to +125°C	V_{IN} = $V_{IH(Max)}$ or V_{IL} (Min)	Loading with 50Ω to −2.0V	1, 2, 3
		−1085	−870	mV	−55°C			
V_{OL}	Output LOW Voltage	−1830	−1620	mV	0°C to +125°C			
		−1830	−1555	mV	−55°C			
V_{OHC}	Output HIGH Voltage	−1035		mV	0°C to +125°C	V_{IN} = $V_{IH(Max)}$ or V_{IL} (Min)	Loading with 50Ω to −2.0V	1, 2, 3
		−1085		mV	−55°C			
V_{OLC}	Output LOW Voltage		−1610	mV	0°C to +125°C			
			−1555	mV	−55°C			
V_{IH}	Input HIGH Voltage	−1165	−870	mV	−55°C to +125°C	Guaranteed HIGH Signal for All Inputs		1, 2, 3, 4
V_{IL}	Input LOW Voltage	−1830	−1475	mV	−55°C to +125°C	Guaranteed LOW Signal for All Inputs		1, 2, 3, 4
I_{IL}	Input LOW Current	0.50		μA	−55°C to +125°C	V_{EE} = −4.2V V_{IN} = V_{IH} (Max)		1, 2, 3
I_{IH}	Input HIGH Current		240	μA	0°C to +125°C	V_{EE} = −5.7V V_{IN} = $V_{IL(Min)}$		1, 2, 3
			340	μA	−55°C			
I_{EE}	Power Supply Current	−48	−17	mA	−55°C to +125°C	Inputs Open		1, 2, 3

Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals −55°C), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 2: Screen tested 100% on each device at −55°C, +25°C, and +125°C, Subgroups 1, 2, 3, 7, and 8.

Note 3: Sample tested (Method 5005, Table I) on each manufactured lot at −55°C, +25°C, and +125°C, Subgroups A1, 2, 3, 7, and 8.

Note 4: Guaranteed by applying specified input condition and testing V_{OH}/V_{OL}.

Military Version (Continued)

AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = −55°C		T_C = +25°C		T_C = +125°C		Units	Conditions	Notes
		Min	Max	Min	Max	Min	Max			
t_{PLH} t_{PHL}	Propagation Delay Data to Output	0.30	1.80	0.40	1.50	0.40	1.70	ns	*Figures 1* and *2*	1, 2, 3, 5
t_{PLH} t_{PHL}	Propagation Delay Enable to Output	0.60	2.60	0.80	2.30	0.80	2.80	ns		
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.30	1.20	0.30	1.20	0.30	1.20	ns		4

Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals −55°C), then testing immediately after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

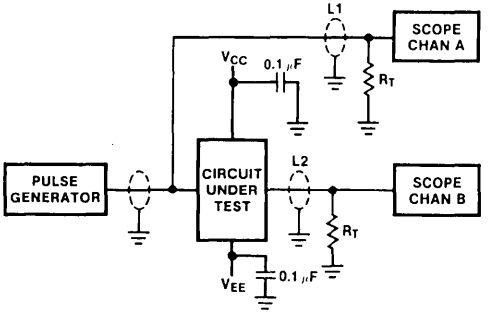
Note 2: Screen tested 100% on each device at +25°C temperature only, Subgroup A9.

Note 3: Sample tested (Method 5005, Table I) on each manufactured lot at +25°C, Subgroup A9, and at +125°C and −55°C temperatures, Subgroups A10 and A11.

Note 4: Not tested at +25°C, +125°C, and −55°C temperature (design characterization data).

Note 5: The propagation delay specified is for single output switching. Delays may vary up to 100 ps with multiple outputs switching.

Test Circuitry

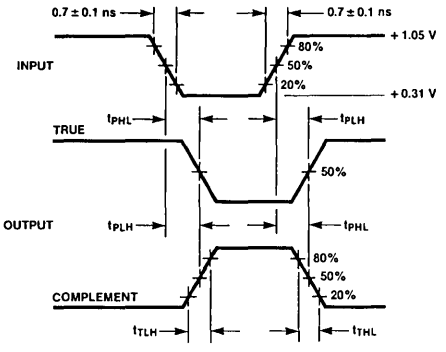


TL/F/10580–5

Notes:
V_{CC}, V_{CCA} = +2V, V_{EE} = −2.5V
L1 and L2 = equal length 50Ω impedance lines
R_T = 50Ω terminator internal to scope
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
All unused outputs are loaded with 50Ω to GND
C_L = Fixture and stray capacitance ≤ 3 pF

FIGURE 1. AC Test Circuit

Switching Waveforms



TL/F/10580–6

FIGURE 2. Propagation Delay and Transition Times

National Semiconductor

100304
Low Power Quint AND/NAND Gate

General Description

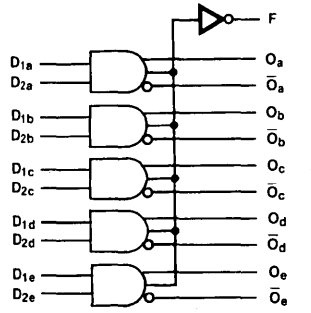
The 100304 is monolithic quint AND/NAND gate. The Function output is the wire-NOR of all five AND gate outputs. All inputs have 50 kΩ pull-down resistors.

Features

- Low Power Operation
- 2000V ESD protection
- Pin/function compatible with 100104
- Voltage compensated operating range = −4.2V to −5.7V
- Available to industrial grade temperature range
- Available to MIL-STD-883

Ordering Code: See Section 6

Logic Symbol



TL/F/10581–1

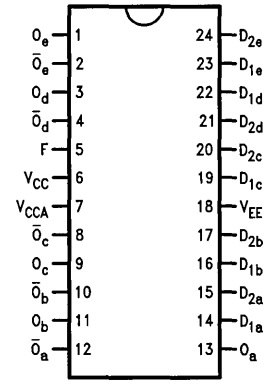
Logic Equation

$$F = \overline{(D_{1a} \bullet D_{2a}) + (D_{1b} \bullet D_{2b}) + D_{1c} \bullet D_{2c}) + (D_{1d} \bullet D_{2d})} + \overline{(D_{1e} \bullet D_{2e})}.$$

Pin Names	Description
D_{na}–D_{ne}	Data Inputs
F	Function Output
O_a–O_e	Data Outputs
$\overline{O}_a$–$\overline{O}_e$	Complementary Data Outputs

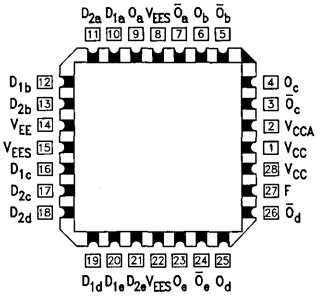
Connection Diagrams

24-Pin DIP



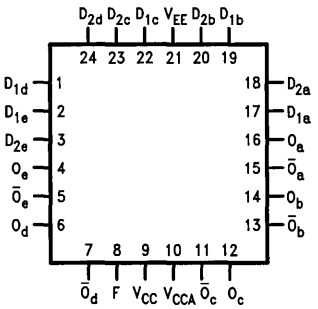
TL/F/10581–2

28-Pin PCC



TL/F/10581–4

24-Pin Quad Cerpak



TL/F/10581–3

Absolute Maximum Ratings

Above which the useful life may be impaired (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature (T_{STG})	−65°C to +150°C
Maximum Junction Temperature (T_J)	
Ceramic	+175°C
Plastic	+150°C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Output Current (DC Output HIGH)	−50 mA
ESD (Note 2)	≥2000V

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: ESD testing conforms to MIL-STD-883, Method 3015.

Recommended Operating Conditions

Case Temperature (T_C)	
Commercial	0°C to +85°C
Industrial	−40°C to +85°C
Military	−55°C to +125°C
Supply Voltage (V_{EE})	−5.7V to −4.2V

Commercial Version

DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions	
V_{OH}	Output HIGH Voltage	−1025	−955	−870	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830	−1705	−1620	mV		
V_{OHC}	Output HIGH Voltage	−1035			mV	V_{IN} = $V_{IH(Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610	mV		
V_{IH}	Input HIGH Voltage	−1165		−870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1830		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	
I_{IH}	Input High Current D_{2a}–D_{2e} D_{1a}–D_{1e}			 250 350	μA	V_{IN} = V_{IH}(Max)	
I_{EE}	Power Supply Current	−69	−43	−30	mA	Inputs open	

Note 3: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DIP AC Electrical Characteristics V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay D_{na}–D_{ne} to O, $\overline{O}$	0.40	1.75	0.40	1.65	0.40	1.75	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay Data to F	1.00	2.60	1.00	2.60	1.15	3.20	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.35	1.20	0.35	1.20	0.35	1.20	ns	

Commercial Version (Continued)

PCC and Cerpak AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay D_{na}–D_{ne} to O, $\overline{O}$	0.40	1.55	0.40	1.45	0.40	1.55	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay Data to F	1.00	2.40	1.00	2.40	1.15	3.00	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.35	1.10	0.35	1.15	0.35	1.10	ns	

Industrial Version

PCC DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = −40°C to +85°C (Note 1)

Symbol	Parameter	T_C = −40°C		T_C = 0°C to +85°C		Units	Conditions	
		Min	Max	Min	Max			
V_{OH}	Output HIGH Voltage	−1085	−870	−1025	−870	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830	−1575	−1830	−1620			
V_{OHC}	Output HIGH Voltage	−1095		−1035		mV	V_{IN} = $V_{IH(Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage		−1565		−1610			
V_{IH}	Input HIGH Voltage	−1170	−870	−1165	−870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1830	−1480	−1830	−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50		0.50		μA	V_{IN} = $V_{IL\ (Min)}$	
I_{IH}	Input HIGH Current D_{2a}–D_{2e} D_{1a}–D_{1e}		 250 350		 250 350	μA	V_{IN} = $V_{IH\ (Max)}$	
I_{EE}	Power Supply Current	−69	−30	−69	−30	mA	Inputs Open	

Note 1: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

Industrial Version (Continued)

PCC AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 40°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay D_{na}–D_{ne} to O, $\overline{O}$	0.35	1.55	0.40	1.45	0.40	1.55	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay Data to F	1.00	2.40	1.00	2.40	1.15	3.00	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.35	1.10	0.35	1.15	0.35	1.10	ns	

Military Version

DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = −55°C to +125°C

Symbol	Parameter	Min	Max	Units	T_C	Conditions		Notes
V_{OH}	Output HIGH Voltage	−1025	−870	mV	0°C to +125°C	V_{IN} = V_{IH} (Max) or V_{IL} (Min)	Loading with 50Ω0 to −2.0V	1, 2, 3
		−1085	−870	mV	−55°C			
V_{OL}	Output LOW Voltage	−1830	−1620	mV	0°C to +125°C			
		−1830	−1555	mV	−55°C			
V_{OHC}	Output HIGH Voltage	−1035		mV	0°C to +125°C	V_{IN} = V_{IH} (Min) or V_{IL} (Max)	Loading with 50Ω to −2.0V	1, 2, 3
		−1085		mV	−55°C			
V_{OLC}	Output LOW Voltage		−1610	mV	0°C to +125°C			
			−1555	mV	−55°C			
V_{IH}	Input HIGH Voltage	−1165	−870	mV	−55°C +125°C	Guaranteed HIGH Signal for All Inputs		1, 2, 3, 4
V_{IL}	Input LOW Voltage	−1830	−1475	mV	−55°C to +125°C	Guaranteed LOW Signal for All Inputs		1, 2, 3,4
I_{IL}	Input LOW Current	0.50		μA	−55°C to +125°C	V_{EE} = −4.2V V_{IN} = V_{IL} (Min)		1, 2, 3
I_{IH}	Input High Current D_{2a}–D_{2e} D_{1a}–D_{1e}		250 350	μA	0°C to +125°C	V_{EE} = −5.7V V_{IN} = V_{IH} (Max)		1, 2, 3
	D_{2a}–D_{2e} D_{1a}–D_{1e}		350 500	μA	−55°C			
I_{EE}	Power Supply Current	−75	−25	mA	−55°C to +125°C	Inputs Open		1, 2, 3

Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals −55°C), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 2: Screen tested 100% on each device at −55°C, +25°C, and +125°C, Subgroups, 1, 2 3, 7, and 8.

Note 3: Sample tested (Method 5005, Table I) on each manufactured lot at −55°C, +25°C, and +125°C, Subgroups A1, 2, 3, 7, and 8.

Note 4: Guaranteed by applying specified input condition and testing V_{OH}/V_{OL}.

Military Version (Continued)

AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = −55°C		T_C = +25°C		T_C = +125°C		Units	Conditions	Notes
		Min	Max	Min	Max	Min	Max			
t_{PLH} t_{PHL}	Propagation Delay D_{na}–D_{ne} to O, $\overline{O}$	0.30	1.90	0.40	1.80	0.30	2.30	ns	*Figures 1* and *2*	1, 2, 3
t_{PLH} t_{PHL}	Propagation Delay Data to F	0.80	2.90	0.90	2.80	0.90	3.40	ns		
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.20	1.80	0.30	1.60	0.20	2.00	ns		4

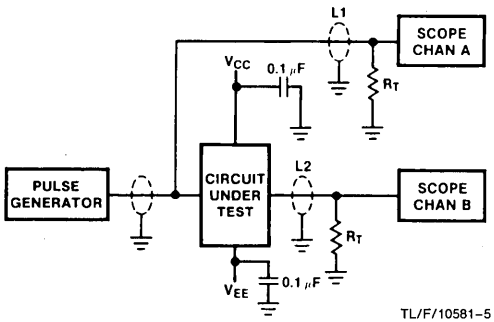
Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals −55°C), then testing immediately after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 2: Screen tested 100% on each device at +25°C temperature only, Subgroup A9.

Note 3: Sample tested (Method 5005, Table I) on each mfg. lot at +25°C, Subgroup A9, and at +125°C and −55°C temperatures, Subgroups A10 and A11.

Note 4: Not tested at +25°C, +125°C, and −55°C temperature (design characterization data).

Test Circuitry



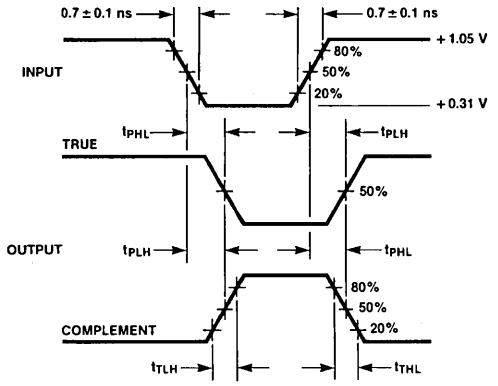
TL/F/10581–5

Notes:

V_{CC}, V_{CCA} = +2V, V_{EE} = −2.5V
L1 and L2 = equal length 50Ω impedance lines
R_T = 50Ω terminator internal to scope
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
All unused outputs are loaded with 50Ω to GND
C_L = Fixture and stray capacitance ≤ 3 pF

FIGURE 1. AC Test Circuit

Switching Waveforms



TL/F/10581–6

FIGURE 2. Propagation Delay and Transition Times

National Semiconductor

100307
Low Power Quint Exclusive OR/NOR Gate

General Description

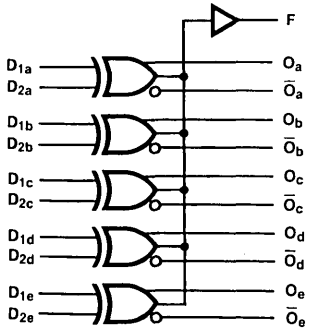
The 100307 is monolithic quint exclusive-OR/NOR gate. The Function output is the wire-OR of all five exclusive-OR outputs. All inputs have 50 kΩ pull-down resistors.

Features

- Low Power Operation
- 2000V ESD protection
- Pin/function compatible with 100107
- Voltage compensated operating range = −4.2V to −5.7V
- Available to industrial grade temperature range
- Available to MIL-STD-883

Ordering Code: See Section 6

Logic Symbol



TL/F/10582–1

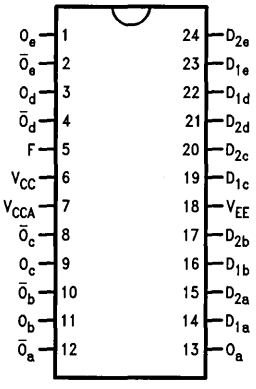
Logic Equation

$F = (D_{1a} \oplus D_{2a}) + (D_{1b} \oplus D_{2b}) + (D_{1c} \oplus D_{2c}) + (D_{1d} \oplus D_{2d}) + (D_{1e} \oplus D_{2e})$.

Pin Names	Description
D_{na}–D_{ne}	Data Inputs
F	Function Output
O_a–O_e	Data Outputs
$\overline{O}_a$–$\overline{O}_e$	Complementary Data Outputs

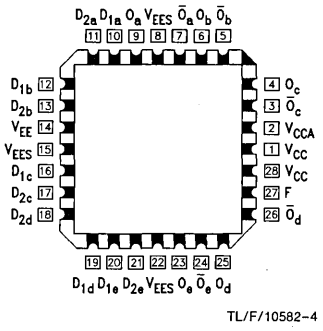
Connection Diagrams

24-Pin DIP/SOIC



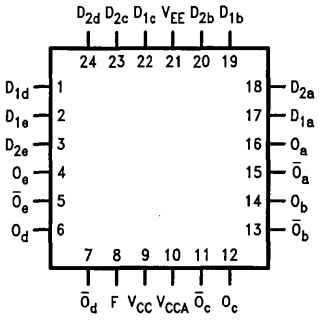
TL/F/10582–2

28-Pin PCC



TL/F/10582–4

24-Pin Quad Cerpak



TL/F/10582–3

Absolute Maximum Ratings

Above which the useful life may be impaired. (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature (T_{STG})	−65°C to +150°C
Maximum Junction Temperature (T_J)	
Ceramic	+175°C
Plastic	+150°C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Output Current (DC Output HIGH)	−50 mA
ESD (Note 2)	≥2000V

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: ESD testing conforms to MIL-STD-883, Method 3015.

Recommended Operating Conditions

Case Temperature (T_C)	
Commercial	0°C to +85°C
Industrial	−40°C to +85°C
Military	−55°C to +125°C
Supply Voltage (V_{EE})	−5.7V to −4.2V

Commercial Version

DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions	
V_{OH}	Output HIGH Voltage	−1025	−955	−870	mV	V_{IN} = V_{IH} (Max) or V_{IL} (Min)	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830	−1705	−1620	mV		
V_{OHC}	Output HIGH Voltage	−1035			mV	V_{IN} = V_{IH} (Min) or V_{IL} (Max)	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610	mV		
V_{IH}	Input HIGH Voltage	−1165		−870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1830		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = V_{IL} (Min)	
I_{IH}	Input HIGH Current D_{2a}–D_{2e} D_{1a}–D_{1e}			 250 350	μA	V_{IN} = V_{IH} (Max)	
I_{EE}	Power Supply Current	−69	−43	−30	mA	Inputs Open	

Note 3: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DIP AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay D_{2a}–D_{2e} to O, $\overline{O}$	0.55	1.90	0.55	1.80	0.55	1.90	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay D_{1a}–D_{1e} to O, $\overline{O}$	0.55	1.70	0.55	1.60	0.55	1.70	ns	
t_{PLH} t_{PHL}	Propagation Delay Data to F	1.15	2.75	1.15	2.75	1.15	3.00	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.35	1.20	0.35	1.20	0.35	1.20	ns	

Commercial Version (Continued)

SOIC, PCC and Cerpak AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay D_{2a}–D_{2e} to O, $\overline{O}$	0.55	1.70	0.55	1.60	0.55	1.70	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay D_{1a}–D_{1e} to O, $\overline{O}$	0.55	1.50	0.55	1.40	0.55	1.50	ns	
t_{PLH} t_{PHL}	Propagation Delay Data to F	1.15	2.55	1.15	2.55	1.15	2.80	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.35	1.10	0.35	1.10	0.35	1.10	ns	

Industrial Version

PCC DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = −40°C to +85°C (Note 1)

Symbol	Parameter	T_C = −40°C		T_C = 0°C to +85°C		Units	Conditions	
		Min	Max	Min	Max			
V_{OH}	Output HIGH Voltage	−1085	−870	−1025	−870	mV	V_{IN} = $V_{IH(Max)}$ or $V_{IL(Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830	−1575	−1830	−1620	mV		
V_{OHC}	Output HIGH Voltage	−1095		−1035		mV	V_{IN} = $V_{IH(Min)}$ or $V_{IL(Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage		−1565		−1610	mV		
V_{IH}	Input HIGH Voltage	−1170	−870	−1165	−870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1830	−1480	−1830	−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50		0.50		μA	V_{IN} = $V_{IL(Min)}$	
I_{IH}	Input HIGH Current D_{2a}–D_{2e} D_{1a}–D_{1e}		250 350		250 350	μA	V_{IN} = $V_{IH(Max)}$	
I_{EE}	Power Supply Current	−69	−30	−69	−30	mA	Inputs Open	

Note 1: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

Industrial Version (Continued)

PCC AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = −40°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay D_{2a}–D_{2e} to O, $\overline{O}$	0.45	1.70	0.55	1.60	0.55	1.70	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay D_{1a}–D_{1e} to O, $\overline{O}$	0.45	1.50	0.55	1.40	0.55	1.50	ns	
t_{PLH} t_{PHL}	Propagation Delay Data to F	1.05	2.55	1.15	2.55	1.15	2.80	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.35	1.10	0.35	1.10	0.35	1.10	ns	

Military Version

DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = −55°C to +125°C

Symbol	Parameter	Min	Max	Units	T_C	Conditions		Notes
V_{OH}	Output HIGH Voltage	−1025	−870	mV	0°C to +125°C	V_{IN} = V_{IH} (Max) or V_{IL} (Min)	Loading with 50Ω to −2.0V	1, 2, 3
		−1085	−870	mV	−55°C			
V_{OL}	Output LOW Voltage	−1830	−1620	mV	0°C to +125°C			
		−1830	−1555	mV	−55°C			
V_{OHC}	Output HIGH Voltage	−1035		mV	0°C to +125°C	V_{IN} = V_{IH} (Min) or V_{IL} (Max)	Loading with 50Ω0 to −2.0V	1, 2, 3
		−1085		mV	−55°C			
V_{OLC}	Output LOW Voltage		−1610	mV	0°C to +125°C			
			−1555	mV	−55°C			
V_{IH}	Input HIGH Voltage	−1165	−870	mV	−55°C to +125°C	Guaranteed HIGH Signal for All Inputs		1, 2, 3, 4
V_{IL}	Input LOW Voltage	−1830	−1475	mV	−55°C to +125°C	Guaranteed LOW Signal for All Inputs		1, 2, 3,4
I_{IL}	Input LOW Current	0.50		μA	−55°C to +125°C	V_{EE} = −4.2V V_{IN} = V_{IL} (Min)		1, 2, 3
I_{IH}	Input High Current D_{2a}–D_{2e} D_{1a}–D_{1e}		250 350	μA	0°C to +125°C	V_{EE} = −5.7V V_{IN} = V_{IH} (Max)		1, 2, 3
	D_{2a}–D_{2e} D_{1a}–D_{1e}		350 500	μA	−55°C			
I_{EE}	Power Supply Current	−75	−25	mA	−55°C to +125°C	Inputs Open		1, 2, 3

Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals −55°C), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 2: Screen tested 100% on each device at −55°C, +25°C, and +125°C, Subgroups 1, 2 3, 7, and 8.

Note 3: Sample tested (Method 5005, Table I) on each manufactured lot at −55°C, +25°C, and +125°C, Subgroups A1, 2, 3, 7, and 8.

Note 4: Guaranteed by applying specified input condition and testing V_{OH}/V_{OL}.

Military Version (Continued)

AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = −55°C		T_C = +25°C		T_C = +125°C		Units	Conditions	Notes
		Min	Max	Min	Max	Min	Max			
t_{PLH} t_{PHL}	Propagation Delay D_{2a}–D_{2e} to O, $\overline{O}$	0.30	2.10	0.40	1.90	0.40	2.40	ns	*Figures 1* and *2*	1, 2, 3
t_{PLH} t_{PHL}	Propagation Delay D_{1a}–D_{1e} to O, $\overline{O}$	0.30	1.90	0.40	1.80	0.40	2.20	ns		
t_{PLH} t_{PHL}	Propagation Delay Data to F	0.80	2.90	0.90	2.80	0.90	3.40	ns		
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.20	1.70	0.30	1.60	0.20	1.70	ns		4

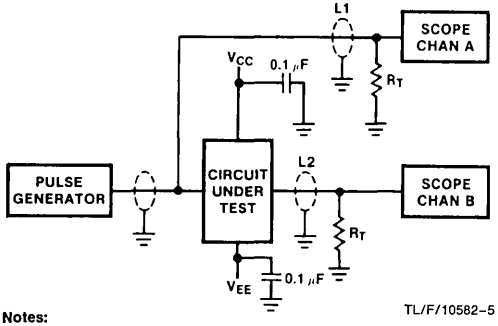
Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals −55°C), then testing immediately after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 2: Screen tested 100% on each device at +25°C temperature only, Subgroup A9.

Note 3: Sample tested (Method 5005, Table I) on each mfg. lot at +25°C, Subgroup A9, and at +125°C and −55°C temperatures, Subgroups A10 and A11.

Note 4: Not tested at +25°C, +125°C, and −55°C temperature (design characterization data).

Test Circuitry



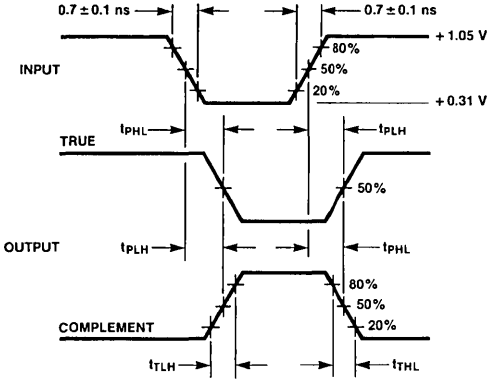
TL/F/10582–5

Notes:

V_{CC}, V_{CCA} = +2V, V_{EE} = −2.5V
L1 and L2 = equal length 50Ω impedance lines
R_T = 50Ω terminator internal to scope
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
All unused outputs are loaded with 50Ω to GND
C_L = Fixture and stray capacitance ≤ 3 pF

FIGURE 1. AC Test Circuit

Switching Waveforms



TL/F/10582–6

FIGURE 2. Propagation Delay and Transition Times

National Semiconductor

100310
Low Skew 2:8 Differential Clock Driver

General Description

The 100310 is a low skew 8-bit differential clock driver which is designed to select between two separate differential clock inputs. The low output to output skew (< 50 ps) is maintained for either clock input. A LOW on the select pin (SEL) selects CLKINA, $\overline{\text{CLKINA}}$ and a HIGH on the SEL pin selects the CLKINB, $\overline{\text{CLKINB}}$ inputs.

The 100310 is ideal for those applications that need the ability to freely select between two clocks, or to maintain the ability to switch to an alternate or backup clock should a problem arise with the primary clock source.

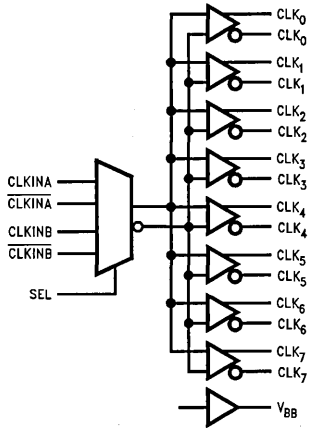
A V_{BB} output is provided for single-ended operation.

Features

- Low output to output skew
- Differential inputs and outputs
- Allows multiplexing between two clock inputs
- Voltage compensated operating range: −4.2V to −5.7V

Ordering Code: See Section 6

Logic Symbol



TL/F/10943–1

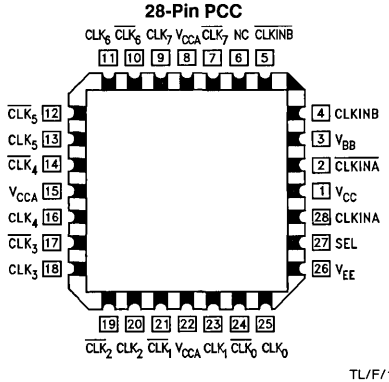
Pin Names	Description
$CLKIN_n$, $\overline{CLKIN}_n$	Differential Clock Inputs
SEL	Select
CLK_{0-7}, $\overline{CLK}_{0-8}$	Differential Clock Outputs
V_{BB}	V_{BB} Output
NC	No Connect

Truth Table

CLKINA	$\overline{\text{CLKINA}}$	CLKINB	$\overline{\text{CLKINB}}$	SEL	CLK_n	$\overline{CLK}_n$
H	L	X	X	L	H	L
L	H	X	X	L	L	H
X	X	H	L	H	H	L
X	X	L	H	H	L	H

Connection Diagram

28-Pin PCC



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Absolute Maximum Ratings

Above which the useful life may be impaired (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature (T_{STG})	−65°C to +150°C
Maximum Junction Temperture (T_J)	
Plastic	+150°C
Pin Potential to Ground Pin (V_{EE})	−7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Output Current (DC Output HIGH)	−50 mA
ESD (Note 2)	≥2000V

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: ESD testing conforms to MIL-STD-883, Method 3015.

Recommended Operating Conditions

Case Temperature (T_C)	
Commercial	0°C to +85°C
Industrial	−40°C to +85°C
Supply Voltage (V_{EE})	−5.7V to −4.2V

Commercial Version

DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions	
V_{OH}	Output HIGH Voltage	−1025	−955	−870	mV	V_{IN} = V_{IH} (Max) or V_{IL} (Min)	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830	−1705	−1620	mV		
V_{OHC}	Output HIGH Voltage	−1035			mV	V_{IN} = V_{IH} or V_{IL} (Max)	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610	mV		
V_{BB}	Output Reference Voltage	−1380	−1320	−1260	mV	I_{VBB} = −250 μA	
V_{DIFF}	Input Voltage Differential	150			mV	Required for Full Output Swing	
V_{CM}	Common Mode Voltage	V_{CC} − 2.0		V_{CC} − 0.5	V		
V_{IH}	Input High Voltage	−1165		−870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input Low Voltage	−1830		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = V_{IL} (Min)	
I_{IH}	Input HIGH Current			240	μA	V_{IN} = V_{IH} (Max)	
I_{CBO}	Input Leakage Current	−10			μA	V_{IN} = V_{EE}	
I_{EE}	Power Supply Current	−100		−40	mA	Inputs Open	

Note 3: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

Commercial Version (Continued)

AC Electrical Characteristics V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C			T_C = +25°C			T_C = +85°C			Units	Conditions
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
f_{MAX}	Max Toggle Frequency											
	CLKIN A/B to Q_n	750			750			750			MHz	
	SEL to Q_n	575			575			575			MHz	
t_{PLH} t_{PHL}	Propagation Delay, $CLKIN_n$ to CLK_n											
	Differential	0.80	0.90	1.00	0.82	0.92	1.02	0.89	1.01	1.09	ns	*Figure 3*
	Single-Ended	0.80	0.96	1.20	0.82	0.98	1.22	0.89	1.06	1.29		
t_{PLH} t_{PHL}	Propagation Delay, SEL to Output	0.75	0.99	1.20	0.80	1.02	1.25	0.85	1.10	1.35	ns	*Figure 2*
t_{PS}	LH-HL Skew		10	30		10	30		10	30	ps	(Notes 1, 4)
t_{OSLH}	Gate-Gate Skew LH		20	30		20	50		20	50		(Notes 2, 4)
t_{OSHL}	Gate-Gate Skew HL		20	50		20	50		20	50		(Notes 2, 4)
t_{OST}	Gate-Gate LH-HL Skew		30	60		30	60		30	60		(Notes 3, 4)
t_S	Setup Time SEL to $CLKIN_n$	300			300			300			ps	
t_H	Setup Time SEL to $CLKIN_n$	0			0			0			ps	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	275	510	750	275	500	750	275	480	750	ps	*Figure 4*

Note 1: t_{PS} describes opposite edge skews, i.e. the difference between the delay of a differential output signal pair's low to high and high to low propagation delays. With differential signal pairs, a low to high or high to low transition is defined as the transition of the true output or input pin.

Note 2: t_{OSLH} describes in-phase gate-to-gate differential propagation skews with all differential outputs going low to high; t_{OSHL} describes the same conditions except with the outputs going high to low.

Note 3: t_{OST} describes the maximum worst case difference in any of the t_{PS}, t_{OSLH} or t_{OST} delay paths combined.

Note 4: The skew specifications pertain to differential I/O paths.

Industrial Version

DC Electrical Characteristics V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND (Note 1)

Symbol	Parameter	T_C = −40°C		T_C = 0°C to +85°C		Units	Conditions	
		Min	Max	Min	Max			
V_{OH}	Output HIGH Voltage	−1085	−870	−1025	−870	mV	V_{IN} = V_{IH} (Max) or V_{IL} (Min)	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830	−1575	−1830	−1620	mV		
V_{OHC}	Output HIGH Voltage	−1095		−1035		mV	V_{IN} = V_{IH} or V_{IL} (Min)	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage		−1565		−1610	mV		
V_{BB}	Output Reference Voltage	−1395	−1255	−1380	−1260	mV	I_{VBB} = −250 μA	
V_{DIFF}	Input Voltage Differential	150		150		mV	Required for Full Output Swing	
V_{CM}	Common Mode Voltage	V_{CC} − 2.0	V_{CC} − 0.5	V_{CC} − 2.0	V_{CC} − 0.5	V		
V_{IH}	Input High Voltage	−1170	−870	−1165	−870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input Low Voltage	−1830	−1480	−1830	−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50		0.50		μA	V_{IN} = V_{IL} (Min)	
I_{IH}	Input HIGH Current		240		240	μA	V_{IN} = V_{IH} (Max)	
I_{CBO}	Input Leakage Current	−10		−10		μA	V_{IN} = V_{EE}	
I_{EE}	Power Supply Current	−100	−40	−100	−40	mA	Inputs Open	

Note 1: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

Industrial Version (Continued)

AC Electrical Characteristics V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = −40°C			T_C = +25°C			T_C = +85°C			Units	Conditions
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
f_{MAX}	Max Toggle Frequency											
	CLKIN A/B to Q_n	750			750			750			MHz	
	SEL to Q_n	575			575			575			MHz	
t_{PLH} t_{PHL}	Propagation Delay, $CLKIN_n$, to CLK_n											
	Differential	0.78	0.88	0.98	0.82	0.92	1.02	0.89	1.01	1.09	ns	*Figure 3*
	Single-Ended	0.78	0.95	1.18	0.82	0.98	1.22	0.89	1.06	1.29		
t_{PLH} t_{PHL}	Propagation Delay SEL to Output	0.70	0.99	1.20	0.80	1.02	1.25	0.85	1.10	1.35	ns	*Figure 2*
t_{PS}	LH-HL Skew		10	30		10	30		10	30	ps	(Notes 1, 4)
t_{OSLH}	Gate-Gate Skew LH		20	50		20	50		20	50		(Notes 2, 4)
t_{OSHL}	Gate-Gate Skew HL		20	50		20	50		20	50		(Notes 2, 4)
t_{OST}	Gate-Gate LH-HL Skew		30	60		30	60		30	60		(Notes 3, 4)
t_S	Setup Time SEL to $CLKIN_n$	300			300			300			ps	
t_H	Setup Time SEL to $CLKIN_n$	0			0			0			ps	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	275	510	750	275	500	750	275	480	750	ps	*Figure 4*

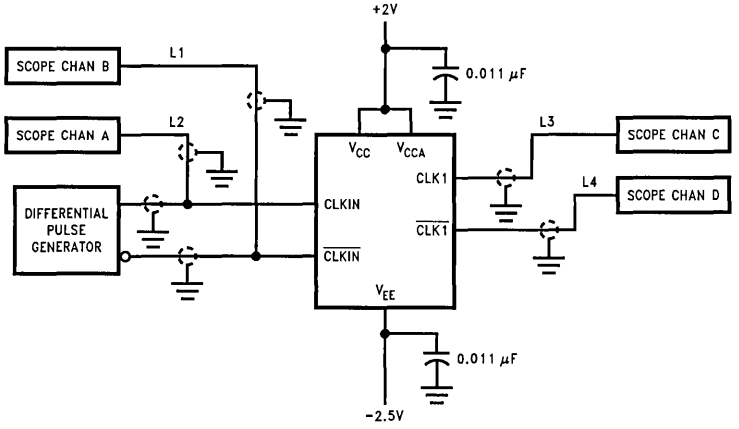
Note 1: t_{PS} describes opposite edge skews, i.e. the difference between the delay of a differential output signal pair's low to high and high to low propagation delays. With differential signal pairs, a low to high or high to low transition is defined as the transition of the true output or input pin.

Note 2: t_{OSLH} describes in-phase gate-to-gate differential propagation skews with all differential outputs going low to high; t_{OSHL} describes the same conditions except with the outputs going high to low.

Note 3: t_{OST} describes the maximum worst case difference in any of the t_{PS}, t_{OSLH} or t_{OST} delay paths combined.

Note 4: The skew specifications pertain to differential I/O paths.

Test Circuit



TL/F/10943–3

Note 1: Shown for testing CLKIN to CLK1 in the differential mode.

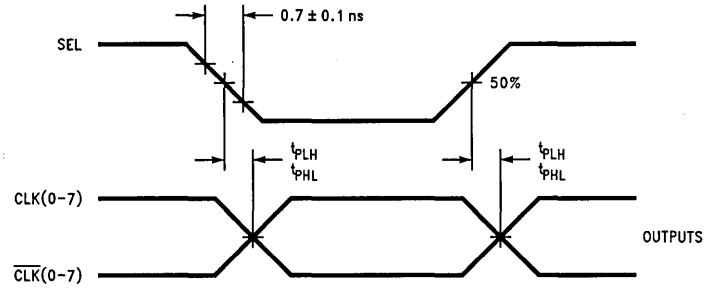
Note 2: L1, L2, L3 and L4 = equal length 50Ω impedance lines.

Note 3: All unused inputs and outputs are loaded with 50Ω in parallel with ≤3 pF to GND.

Note 4: Scope should have 50Ω input terminator internally.

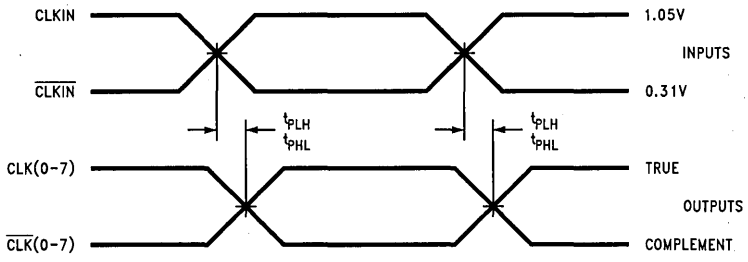
FIGURE 1. AC Test Circuit

Switching Waveforms



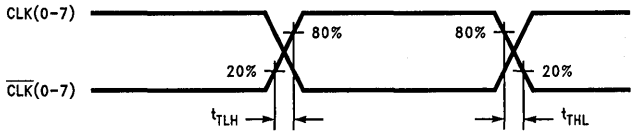
TL/F/10943–4

FIGURE 2. Propagation Delay, SEL to Outputs



TL/F/10943–5

FIGURE 3. Propagation Delay, CLKIN/$\overline{CLKIN}$ to Outputs



TL/F/10943–6

FIGURE 4. Transition Times

National Semiconductor

100311
Low Skew 1:9 Differential Clock Driver

General Description

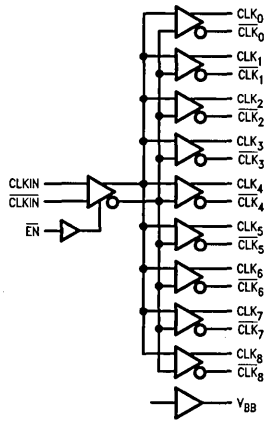
The 100311 contains nine low skew differential drivers, designed for generation of multiple, minimum skew differential clocks from a single differential input (CLKIN, $\overline{CLKIN}$). If a single-ended input is desired, the V_{BB} output pin may be used to drive the remaining input line. A HIGH on the enable pin ($\overline{EN}$) will force a LOW on all of the CLK_n outputs and a HIGH on all of the $\overline{CLK}_n$ output pins. The 100311 is ideal for distributing a signal throughout a system without worrying about the original signal becoming too corrupted by undesirable delays and skew. The 100311 is pin-for-pin compatible with the Motorola 100E111.

Features

- Low output to output skew
- 2000V ESD protection
- 1:9 low skew clock driver
- Differential inputs and outputs

Ordering Code: See Section 6

Logic Symbol



TL/F/10648–1

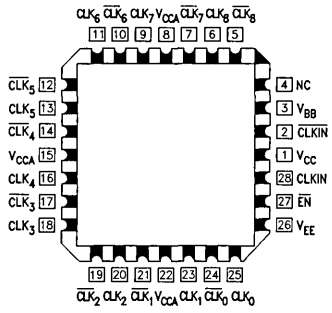
Pin Names	Description
CLKIN, $\overline{CLKIN}$	Differential Clock Inputs
$\overline{EN}$	Enable
CLK_{0-8}, $\overline{CLK}_{0-8}$	Differential Clock Outputs
V_{BB}	V_{BB} Output
NC	No Connect

Truth Table

CLKIN	$\overline{CLKIN}$	$\overline{EN}$	CLK_n	$\overline{CLK}_n$
L	H	L	L	H
H	L	L	H	L
X	X	H	L	H

Connection Diagram

28-Pin PCC



TL/F/10648–2

Absolute Maximum Ratings

Above which the useful life may be impaired (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature (T_{STG})	−65°C to +150°C
Maximum Junction Temperture (T_J)	
Ceramic	+175°C
Plastic	+150°C
Pin Potential to Ground Pin (V_{EE})	−7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Output Current (DC Output HIGH)	−50 mA
ESD (Note 2)	≥2000V

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: ESD testing conforms to MIL-STD-883, Method 3015.

Recommended Operating Conditions

Case Temperature (T_C)	
Commercial	0°C to +85°C
Industrial	−40°C to +85°C
Supply Voltage (V_{EE})	−5.7V to −4.2V

Commercial Version

DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions	
V_{OH}	Output HIGH Voltage	−1025	−955	−870	mV	V_{IN} = V_{IH} (Max) or V_{IL} (Min)	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830	−1705	−1620	mV		
V_{OHC}	Output HIGH Voltage	−1035			mV	V_{IN} = V_{IH} or V_{IL} (Max)	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610	mV		
V_{BB}	Output Reference Voltage	−1380	−1320	−1260	mV	I_{VBB} = −300 μA	
V_{DIFF}	Input Voltage Differential	150			mV	Required for Full Output Swing	
V_{CM}	Common Mode Voltage	V_{CC} − 2.0		V_{CC} − 0.5	V		
V_{IH}	Input High Voltage	−1165		−870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input Low Voltage	−1830		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = V_{IL} (Min)	
I_{IH}	Input HIGH Current CLKIN, $\overline{CLKIN}$ $\overline{EN}$			 100 250	μA	V_{IN} = V_{IH} (Max)	
I_{CBO}	Input Leakage Current	−10			μA	V_{IN} = V_{EE}	
I_{EE}	Power Supply Current	−115		−57	mA	Inputs Open	

Note 3: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

Commercial Version (Continued)

AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C			T_C = +25°C			T_C = +85°C			Units	Conditions
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
f_{max}	Max Toggle Frequency CLKIN to Q_n	750			750			750			MHz	
t_{PLH} t_{PHL}	Propagation Delay, $CLKIN_n$ to CLK_n											
	Differential	0.75	0.84	0.95	0.75	0.86	0.95	0.84	0.93	1.04	ns	*Figure 3*
	Single-Ended	0.65	0.90	1.05	0.67	0.93	1.17	0.74	1.06	1.24		
t_{PLH} t_{PHL}	Propagation Delay SEL to Output	0.75	1.03	1.20	0.80	1.05	1.25	0.85	1.12	1.35	ns	*Figure 2*
t_{PS}	LH–HL Skew		10	30		10	30		10	30	ps	Notes 1, 4
t_{OSLH}	Gate–Gate Skew LH		20	50		20	50		20	50		Notes 2, 4
t_{OSHL}	Gate–Gate Skew HL		20	50		20	50		20	50		Notes 2, 4
t_{OST}	Gate–Gate LH–HL Skew		30	60		30	60		30	60		Notes 3, 4
t_S	Setup Time EN_n to $CLKIN_n$	250			250			300			ps	
t_H	Hold Time EN_n to $CLKIN_n$	0			0			0			ps	
t_R	Release Time EN_n to $CLKIN_n$	300			300			300			ps	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	275	500	750	275	480	750	275	460	750	ps	*Figure 4*

Note 1: t_{PS} describes opposite edge skews, i.e. the difference between the delay of a differential output signal pair's low to high and high to low propagation delays. With differential signal pairs, a low to high or high to low transition is defined as the transition of the true output or input pin.

Note 2: t_{OSLH} describes in-phase gate-to-gate differential propagation skews with all differential outputs going low to high; t_{OSHL} describes the same conditions except with the outputs going high to low.

Note 3: t_{OST} describes the maximum worst case difference in any of the t_{PS}, t_{OSLH} or t_{OST} delay paths combined.

Note 4: The skew specifications pertain to differential I/O paths.

Note 5: f_{max} = the highest frequency at which output V_{OL}/V_{OH} levels still meet V_{IN} specifications. The F311 will function @ 1 GHz.

Industrial Version

DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND (Note 3)

Symbol	Parameter	T_C = −40°C		T_C = 0°C to +85°C		Units	Conditions	
		Min	Max	Min	Max			
V_{OH}	Output HIGH Voltage	−1085	−870	−1025	−870	mV	V_{IN} = V_{IH} (Max) or V_{IL} (Min)	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830	−1575	−1830	−1620	mV		
V_{OHC}	Output HIGH Voltage	−1095		−1035		mV	V_{IN} = V_{IH} or V_{IL} (Min)	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage		−1565		−1610	mV		
V_{BB}	Output Reference Voltage	−1395	−1255	−1380	−1260	mV	I_{VBB} = −300 μA	
V_{DIFF}	Input Voltage Differential	150		150		mV	Required for Full Output Swing	
V_{CM}	Common Mode Voltage	V_{CC} − 2.0	V_{CC} − 0.5	V_{CC} − 2.0	V_{CC} − 0.5	V		
V_{IH}	Input High Voltage	−1170	−870	−1165	−870	mV	Guaranteed HIGH Signal for All Inputs	

Industrial Version (Continued)

DC Electrical Characteristics (Continued)

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND (Note 3)

Symbol	Parameter	T_C = −40°C		T_C = 0°C to +85°C		Units	Conditions
		Min	Max	Min	Max		
V_{IL}	Input Low Voltage	−1830	−1480	−1830	−1475	mV	Guaranteed LOW Signal for All Inputs
I_{IL}	Input LOW Current	0.50		0.50		μA	V_{IN} = V_{IL} (Min)
I_{IH}	Input HIGH Current						V_{IN} = V_{IH} (Max)
	CLKIN, $\overline{CLKIN}$		100		100	μA	
	$\overline{EN}$		250		250		
I_{CBO}	Input Leakage Current	−10		−10		μA	V_{IN} = V_{EE}
I_{EE}	Power Supply Current	−115	−57	−115	−57	mA	Inputs Open
V_{PP}	Minimum Input Swing	150		150		mV	
V_{CMR}	Common Mode Range	V_{CC}−2.0	V_{CC}−0.5	V_{CC}−2.0	V_{CC}−0.5	V	

Note 3: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = −40°C			T_C = +25°C			T_C = +85°C			Units	Conditions
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
f_{max}	Max Toggle Frequency CLKIN to Q_n	750			750			750			MHz	
t_{PLH} t_{PHL}	Propagation Delay, $CLKIN_n$ to CLK_n											
	Differential	0.72	0.81	0.92	0.77	0.86	0.95	0.84	0.93	1.04	ns	*Figure 3*
	Single-Ended	0.62	0.89	1.02	0.67	0.93	1.17	0.74	1.06	1.24		
t_{PLH} t_{PHL}	Propagation Delay SEL to Output	0.70	0.97	1.20	0.80	1.05	1.25	0.85	1.12	1.35	ns	*Figure 2*
t_{PS}	LH−HL Skew		10	30		10	30		10	30	ps	Notes 1, 4
t_{OSLH}	Gate−Gate Skew LH		20	50		20	50		20	50		Notes 2, 4
t_{OSHL}	Gate−Gate Skew HL		20	50		20	50		20	50		Notes 2, 4
t_{OST}	Gate−Gate LH−HL Skew		30	60		30	60		30	60		Notes 3, 4
t_S	Setup Time EN_n to $CLKIN_n$	250			250			300			ps	
t_H	Hold Time EN_n to $CLKIN_n$	0			0			0			ps	
t_R	Release Time EN_n to $CLKIN_n$	300			300			300			ps	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	275	500	750	275	480	750	275	460	750	ps	*Figure 4*

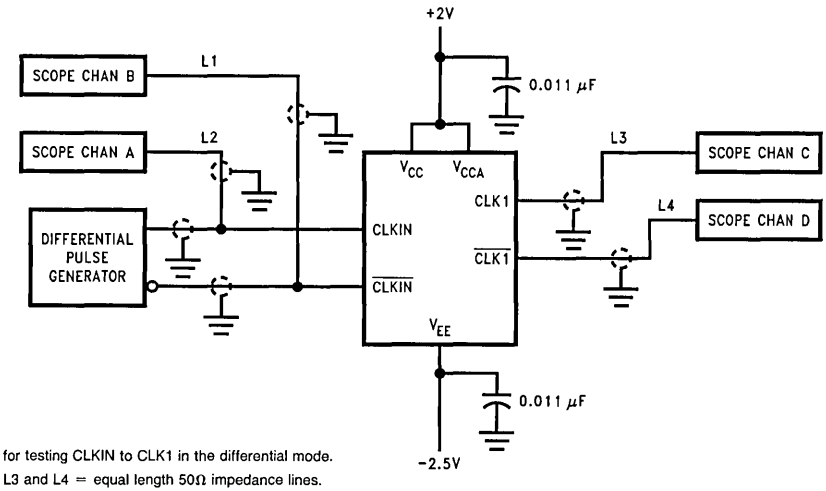
Note 1: t_{PS} describes opposite edge skews, i.e. the difference between the delay of a differential output signal pair's low to high and high to low propagation delays. With differential signal pairs, a low to high or high to low transition is defined as the transition of the true output or input pin.

Note 2: t_{OSLH} describes in-phase gate differential propagation skews with all differential outputs going low to high; t_{OSHL} describes the same conditions except with the outputs going high to low.

Note 3: t_{OST} describes the maximum worst case difference in any of the t_{PS}, t_{OSLH} or t_{OST} delay paths combined.

Note 4: The skew specifications pertain to differential I/O paths.

Test Circuit



Note 1: Shown for testing CLKIN to CLK1 in the differential mode.

Note 2: L1, L2, L3 and L4 = equal length 50Ω impedance lines.

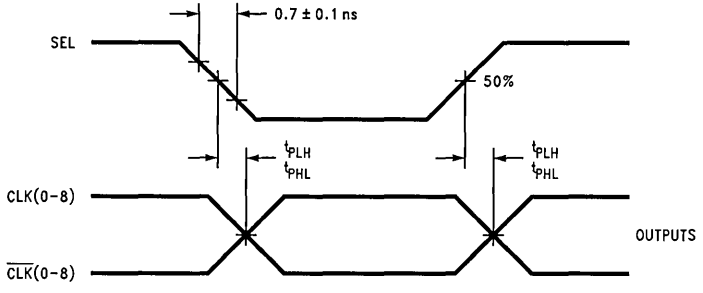
Note 3: All unused inputs and outputs are loaded with 50Ω in parallel with ≤ 3 pF to GND.

Note 4: Scope should have 50Ω input terminator internally.

TL/F/10648–3

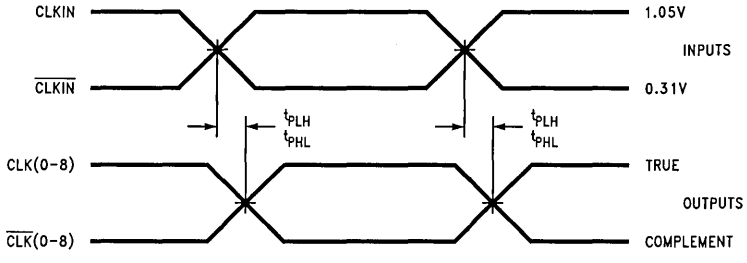
FIGURE 1. AC Test Circuit

Switching Waveforms



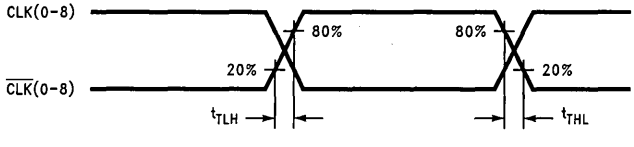
TL/F/10648–4

FIGURE 2. Propagation Delay, $\overline{EN}$ to Outputs



TL/F/10648–5

FIGURE 3. Propagation Delay, CLKIN/CLKIN to Outputs



TL/F/10648–6

FIGURE 4. Transition Times

National Semiconductor

100313
Low Power Quad Driver

General Description

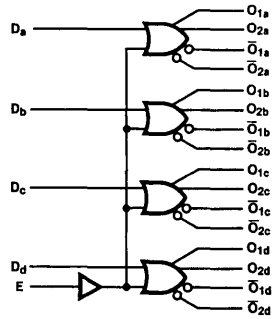
The 100313 is a monolithic quad driver with two OR and two NOR outputs and common enable. The common input is buffered to minimize input loading. If the D inputs are not used the Enable can be used to drive sixteen 50Ω lines. All inputs have 50 kΩ pull-down resistors and all outputs are buffered.

Features

- 50% power reduction of the 100113
- 2000V ESD protection
- Pin/function compatible with 100113 and 100112
- Voltage compensated operating range = −4.2V to −5.7V
- Available to MIL-STD-883
- Available to industrial grade temperature range

Ordering Code: See Section 6

Logic Symbol

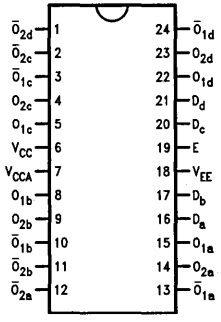


TL/F/10249–3

Pin Names	Description
D_a–D_d	Data Inputs
E	Enable Input
O_{na}–O_{nd}	Data Outputs
$\overline{O}_{na}$–$\overline{O}_{nd}$	Complementary Data Outputs

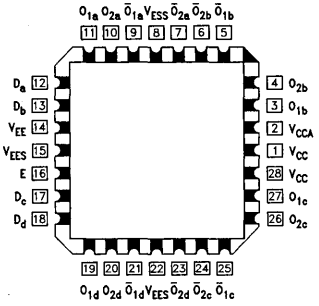
Connection Diagrams

24-Pin DIP/SOIC



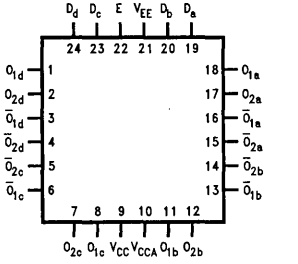
TL/F/10249–1

28-Pin PCC



TL/F/10249–4

24-Pin Flatpak



TL/F/10249–2

Absolute Maximum Ratings

Above which the useful life may be impaired (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature (T_{STG})	−65°C to +150°C
Maximum Junction Temperature (T_J)	
Ceramic	+175°C
Plastic	+150°C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Output Current (DC Output HIGH)	−50 mA
ESD (Note 2)	≥2000V

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: ESD testing conforms to MIL-STD-883, Method 3015.

Recommended Operating Conditions

Case Temperature (T_C)	
Commercial	0°C to +85°C
Industrial	−40°C to +85°C
Military	−55°C to +125°C
Supply Voltage (V_{EE})	−5.7V to −4.2V

Commercial Version

DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions	
V_{OH}	Output HIGH Voltage	−1025	−955	−870	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830	−1705	−1620			
V_{OHC}	Output HIGH Voltage	−1035			mV	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610			
V_{IH}	Input HIGH Voltage	−1165		−870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1830		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	
I_{IH}	Input HIGH Current Data Enable			 350 240	μA	V_{IN} = $V_{IH\ (Max)}$	
I_{EE}	Power Supply Current	−59		−29	mA	Inputs Open	

Note 3: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DIP AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Data to Output	0.55	1.30	0.55	1.30	0.55	1.40	ns	*Figures 1* and *2* (Note 1)
t_{PLH} t_{PHL}	Propagation Delay Enable to Output	0.80	1.80	0.80	1.80	0.80	1.90	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.30	0.45	1.30	0.45	1.30	ns	*Figures 1* and *2*

Note 1: The propagation delay specified is for single output switching. Delays may vary up to 150 ps with multiple outputs switching.

Commercial Version (Continued)

SOIC, PCC and Cerpak AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Data to Output	0.55	1.20	0.55	1.20	0.55	1.30	ns	*Figures 1* and *2* (Note 2)
t_{PLH} t_{PHL}	Propagation Delay Enable to Output	0.80	1.70	0.80	1.70	0.80	1.80	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.30	0.45	1.30	0.45	1.30	ns	*Figures 1* and *2*
t_{OSHL}	Maximum Skew Common Edge Output-to-Output Variation Data to Output Path		280		280		280	ps	PCC Only (Note 1)
t_{OSHL}	Maximum Skew Common Edge Output-to-Output Variation Enable to Output Path		290		290		290	ps	PCC Only (Note 1)
t_{OSLH}	Maximum Skew Common Edge Output-to-Output Variation Data to Output Path		330		330		330	ps	PCC Only (Note 1)
t_{OSLH}	Maximum Skew Common Edge Output-to-Output Variation Enable to Output Path		360		360		360	ps	PCC Only (Note 1)
t_{OST}	Maximum Skew Opposite Edge Output-to-Output Variation Data to Output Path		330		330		330	ps	PCC Only (Note 1)
t_{OST}	Maximum Skew Opposite Edge Output-to-Output Variation Enable to Output Path		360		360		360	ps	PCC Only (Note 1)
t_{PS}	Maximum Skew Pin (Signal) Transition Variation Data to Output Path		200		200		200	ps	PCC Only (Note 1)
t_{PS}	Maximum Skew Pin (Signal) Transition Variation Enable to Output Path		200		200		200	ps	PCC Only (Note 1)

Note 1: Output-to-Output Skew is defined as the absolute value of the difference between the actual propagation delay for any outputs within the same packaged device. The specifications apply to any outputs switching in the same direction either HIGH to LOW (t_{OSHL}), or LOW to HIGH (t_{OSLH}), or in opposite directions both HL and LH (t_{OST}). Parameters t_{OST} and t_{PS} guaranteed by design.

Note 2: The propagation delay specified is for single output switching. Delays may vary up to 150 ps with multiple outputs switching.

Industrial Version

PCC DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = −40°C to +85°C (Note 3)

Symbol	Parameter	T_C = −40°C		T_C = 0°C to +85°C		Units	Conditions	
		Min	Max	Min	Max			
V_{OH}	Output HIGH Voltage	−1085	−870	−1025	−870	mV	V_{IN} = $V_{IH(Max)}$ or $V_{IL(Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830	−1575	−1830	−1620			
V_{OHC}	Output HIGH Voltage	−1095		−1035		mV	V_{IN} = $V_{IH(Min)}$ or $V_{IL(Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage		−1565		−1610			
V_{IH}	Input HIGH Voltage	−1170	−870	−1165	−870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1830	−1480	−1830	−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50		0.50		μA	V_{IN} = $V_{IL(Min)}$	
I_{IH}	Input HIGH Current Data Enable		 350 240		 350 240	μA	V_{IN} = $V_{IH(Max)}$	
I_{EE}	Power Supply Current	−59	−29	−59	−29	mA	Inputs Open	

Note 3: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

Industrial Version (Continued)

PCC AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = −40°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Data to Output	0.55	1.20	0.55	1.20	0.55	1.30	ns	*Figures 1* and *2* (Note 1)
t_{PLH} t_{PHL}	Propagation Delay Enable to Output	0.80	1.70	0.80	1.70	0.80	1.80	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.30	0.45	1.30	0.45	1.30	ns	*Figures 1* and *2*

Note 1: The propagation delay specified is for single output switching. Delays may vary up to 150 ps with multiple outputs switching.

Military Version

DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = −55°C to +125°C

Symbol	Parameter	Min	Max	Units	T_C	Conditions		Notes
V_{OH}	Output HIGH Voltage	−1025	−870	mV	0°C to +125°C	V_{IN} = V_{IH} (Max) or V_{IL}(Min)	Loading with 50Ω to −2.0V	1, 2, 3
		−1085	−870	mV	−55°C			
V_{OL}	Output LOW Voltage	−1830	−1620	mV	0°C to +125°C			
		−1830	−1555	mV	−55°C			
V_{OHC}	Output HIGH Voltage	−1035		mV	0°C to +125°C	V_{IN} = V_{IH} (Min) or V_{IL} (Max)	Loading with 50Ω to −2.0V	1, 2, 3
		−1085		mV	−55°C			
V_{OLC}	Output LOW Voltage		−1610	mV	0°C to +125°C			
			−1555	mV	−55°C			
V_{IH}	Input HIGH Voltage	−1165	−870	mV	−55°C to +125°C	Guaranteed HIGH Signal for All Inputs		1, 2, 3, 4
V_{IL}	Input LOW Voltage	−1830	−1475	mV	−55°C to +125°C	Guaranteed LOW Signal for All Inputs		1, 2, 3, 4
I_{IL}	Input LOW Current	0.50		μA	−55°C to +125°C	V_{EE} = −4.2V V_{IN} = V_{IL} (Min)		1, 2, 3
I_{IH}	Input HIGH Current Data Enable		350 240	μA	0°C to +125°C	V_{EE} = −5.7V V_{IN} = V_{IH} (Max)		1, 2, 3
	Data Enable		500 340	μA	−55°C			
I_{EE}	Power Supply Current	−65	−20	mA	−55°C to +125°C	Inputs Open		1, 2, 3

Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals −55°C), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 2: Screen tested 100% on each device at −55°C, +25°C, and +125°C, Subgroups 1, 2, 3, 7, and 8.

Note 3: Sample tested (Method 5005, Table I) on each manufactured lot at −55°C, +25°C, and +125°C, Subgroups A1, 2, 3, 7, and 8.

Note 4: Guaranteed by applying specified input condition and testing V_{OH}/V_{OL}.

Military Version (Continued)

AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = −55°C		T_C = +25°C		T_C = +125°C		Units	Conditions	Notes
		Min	Max	Min	Max	Min	Max			
t_{PLH} t_{PHL}	Propagation Delay Data to Output	0.30	2.00	0.30	1.80	0.30	2.30	ns	*Figures 1* and *2*	1, 2, 3, 5
t_{PLH} t_{PHL}	Propagation Delay Enable to Output	0.50	2.40	0.60	2.30	0.60	2.70	ns		
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.30	2.00	0.30	1.90	0.30	2.00	ns		4

Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals −55°C), then testing immediately after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

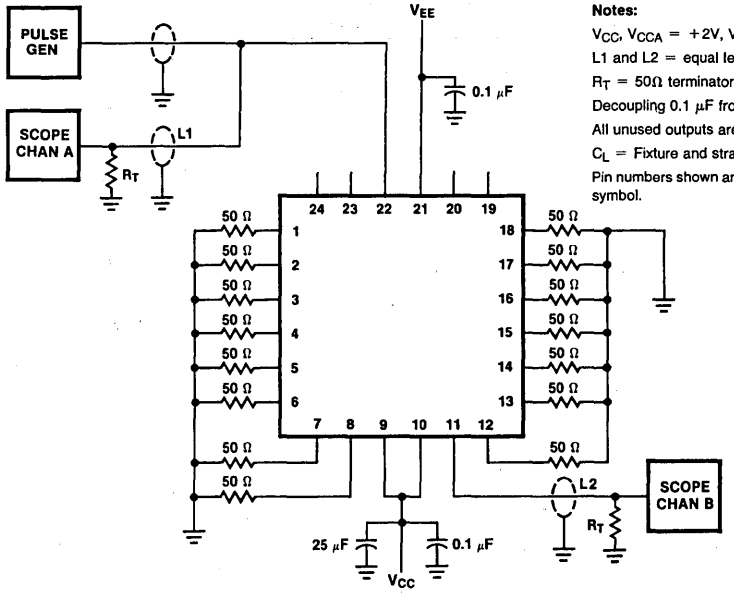
Note 2: Screen tested 100% on each device at +25°C, Subgroup A9.

Note 3: Sample tested (Method 5005, Table 1) on each manufactured lot at +25°C, Subgroup A9, and at +125°C and −55°C temperatures, Subgroups A10 and A11.

Note 4: Not tested at +25°C, +125°C, and −55°C temperature (design characterization data).

Note 5: The propagation delay specified is for single output switching. Delays may vary up to 150 ps with multiple outputs switching.

Test Circuitry

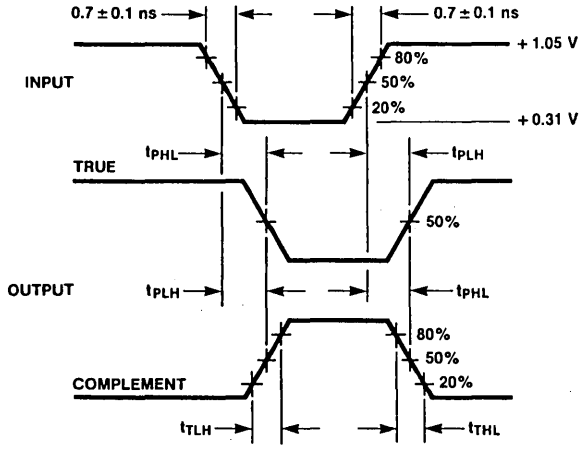


Notes:
V_{CC}, V_{CCA} = +2V, V_{EE} = −2.5V.
L1 and L2 = equal length 50Ω impedance lines.
R_T = 50Ω terminator internal to scope.
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}.
All unused outputs are loaded with 50Ω to GND.
C_L = Fixture and stray capacitance ≤ 3 pF.
Pin numbers shown are for flatpak; for DIP see logic symbol.

TL/F/10249–5

FIGURE 1. AC Test Circuit

Switching Waveforms



TL/F/10249–6

FIGURE 2. Propagation Delay and Transition Times

National Semiconductor

100314
Low Power Quint Differential Line Receiver

General Description

The 100314 is a monolithic quint differential line receiver with emitter-follower outputs. An internal reference supply (V_{BB}) is available for single-ended reception. When used in single-ended operation the apparent input threshold of the true inputs is 25 mV to 30 mV higher (positive) than the threshold of the complementary inputs. Unlike other F100K ECL devices, the inputs do not have input pull-down resistors.

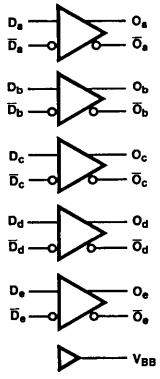
Active current sources provide common-mode rejection of 1.0V in either the positive or negative direction. A defined output state exists if both inverting and non-inverting inputs are at the same potential between V_{EE} and V_{CC}. The defined state is logic HIGH on the $\overline{O}_a$–$\overline{O}_e$ outputs.

Features

- 35% power reduction of the 100114
- 2000V ESD protection
- Pin/function compatible with 100114
- Voltage compensated operating range = −4.2V to −5.7V
- Available to MIL-STD-883
- Available to industrial grade temperature range

Ordering Code: See Section 6

Logic Symbol

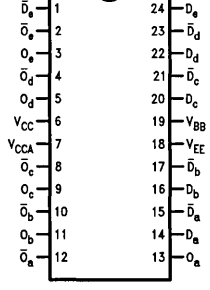


TL/F/10260–1

Pin Names	Description
D_a–D_e	Data Inputs
$\overline{D}_a$–$\overline{D}_e$	Inverting Data Inputs
O_a–O_e	Data Outputs
$\overline{O}_a$–$\overline{O}_e$	Complementary Data Outputs

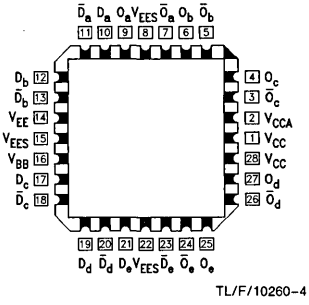
Connection Diagrams

24-Pin DIP/SOIC



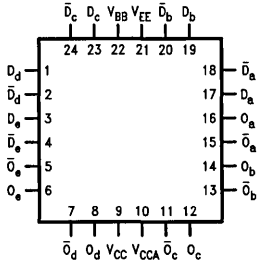
TL/F/10260–2

28-Pin PCC



TL/F/10260–4

24-Pin Quad Cerpak



TL/F/10260–3

Absolute Maximum Ratings

Above which the useful life may be impaired (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature (T_{STG})	−65°C to +150°C
Maximum Junction Temperture (T_J)	
Ceramic	+175°C
Plastic	+150°C
Pin Potential to Ground Pin (V_{EE})	−7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Output Current (DC Output HIGH)	−50 mA
ESD (Note 2)	≥2000V

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: ESD testing conforms to MIL-STD-883, Method 3015.

Recommended Operating Conditions

Case Temperature (T_C)	
Commercial	0°C to +85°C
Industrial	−40°C to +85°C
Military	−55°C to +125°C
Supply Voltage (V_{EE})	−5.7V to −4.2V

Commercial Version

DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions	
V_{OH}	Output HIGH Voltage	−1025	−955	−870	mV	V_{IN} = V_{IH} (Max) or V_{IL} (Min)	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830	−1705	−1620	mV		
V_{OHC}	Output HIGH Voltage	−1035			mV	V_{IN} = V_{IH} or V_{IL} (Max)	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610	mV		
V_{BB}	Output Reference Voltage	−1380	−1320	−1260	mV	I_{VBB} = −250 μA	
V_{DIFF}	Input Voltage Differential	150			mV	Required for Full Output Swing	
V_{CM}	Common Mode Voltage	V_{CC} − 2.0		V_{CC} − 0.5	V		
V_{IH}	Single-Ended Input High Voltage	−1110		−870	mV	Guaranteed HIGH Signal for All Inputs (with one input tied to V_{BB}) V_{BB} (Max) + V_{DIFF}	
V_{IL}	Single-Ended Input Low Voltage	−1830		−1530	mV	Guaranteed LOW Signal for All Inputs (with one input tied to V_{BB}) V_{BB} (Min) − V_{DIFF}	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = V_{IL} (Min)	
I_{IH}	Input HIGH Current			240	μA	V_{IN} = $V_{IH\,(Max)}$, D_a−D_e = V_{BB}, $\overline{D}_a$−$\overline{D}_e$ = $V_{IL(Min)}$	
I_{CBO}	Input Leakage Current	−10			μA	V_{IN} = V_{EE}, D_a−D_e = V_{BB}, $\overline{D}_a$−$\overline{D}_e$ = $V_{IL\,(Min)}$	
I_{EE}	Power Supply Current	−60		−30	mA	D_a−D_e = V_{BB}, $\overline{D}_a$−$\overline{D}_e$ = $V_{IL\,(Min)}$	

Note 3: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

Commercial Version (Continued)

DIP AC Electrical Characteristics V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
f_{MAXFS}	Toggle Frequency (Full Swing)	250		250		250		MHz	(Note 2)
f_{MAXRS}	Toggle Frequency (Reduced Swing)	700		700		700		MHz	(Note 3)
t_{PLH} t_{PHL}	Propagation Delay Data to Output	0.65	1.90	0.65	2.00	0.70	2.00	ns	*Figures 1* and *2*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.35	1.20	0.35	1.20	0.35	1.20	ns	

SOIC, PCC and Cerpak AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
f_{MAXFS}	Toggle Frequency (Full Swing)	250		250		250		MHz	(Note 2)
f_{MAXRS}	Toggle Frequency (Reduced Swing)	700		700		700		MHz	(Note 3)
t_{PLH} t_{PHL}	Propagation Delay Data to Output	0.65	1.70	0.65	1.80	0.70	1.80	ns	*Figures 1* and *2*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.35	1.10	0.35	1.10	0.35	1.10	ns	
t_{PLH} t_{PHL}	Propagation Delay Data to Output	0.70	1.50	0.80	1.60	0.90	1.80	ns	PCC only
t_{OSHL}	Maximum Skew Common Edge Output-to-Output Variation Data to Output Path		280		280		280	ps	PCC only (Notes 1 and 4)
t_{OSLH}	Maximum Skew Common Edge Output-to-Output Variation Data to Output Path		330		330		330	ps	PCC only (Notes 1 and 4)
t_{OST}	Maximum Skew Opposite Edge Output-to-Output Variation Data to Output Path		330		330		330	ps	PCC only (Notes 1 and 4)
t_{PS}	Maximum Skew Pin (Signal) Transition Variation Data to Output Path		320		320		320	ps	PCC only (Notes 1 and 4)

Note 1: Output-to-Output Skew is defined as the absolute value of the difference between the actual propagation delay for any outputs within the same packaged device. The specifications apply to any outputs switching in the same direction either HIGH to LOW (t_{OSHL}), or LOW to HIGH (t_{OSLH}), or in opposite directions both HL and LH (t_{OST}). Parameters t_{OST} and t_{PS} guaranteed by design.

Note 2: Maximum toggle frequency at which V_{OH} and V_{OL} DC specifications are maintained.

Note 3: Maximum toggle frequency at which outputs maintain 150 mV swing.

Note 4: All skews calculated using input crossing point to output crossing point propagation delays.

Industrial Version

PCC DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = −40°C to +85°C (Note 1)

Symbol	Parameter	T_C = −40°C		T_C = 0°C to +85°C		Units	Conditions	
		Min	Max	Min	Max			
V_{OH}	Output HIGH Voltage	−1085	−870	−1025	−870	mV	V_{IN} = V_{IH} (Max) or V_{IL} (Min)	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830	−1575	−1830	−1620	mV		

Industrial Version (Continued)

PCC DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = −40°C to +85°C (Note 1) (Continued)

Symbol	Parameter	T_C = −40°C		T_C = 0°C to +85°C		Units	Conditions	
		Min	Max	Min	Max			
V_{OHC}	Output HIGH Voltage	−1095		−1035		mV	V_{IN} = V_{IH} or V_{IL} (Min)	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage		−1565		−1610	mV		
V_{BB}	Output Reference Voltage	−1395	−1255	−1380	−1260	mV	I_{VBB} = −250 μA	
V_{DIFF}	Input Voltage Differential	150		150		mV	Required for Full Output Swing	
V_{CM}	Common Mode Voltage	V_{CC} − 2.0	V_{CC} − 0.5	V_{CC} − 2.0	V_{CC} − 0.5	V		
V_{IH}	Single-Ended Input High Voltage	−1115	−870	−1110	−870	mV	Guaranteed HIGH Signal for All Inputs (with one input tied to V_{BB}) V_{BB} (Max) + V_{DIFF}	
V_{IL}	Single-Ended Input Low Voltage	−1830	−1535	−1830	−1530	mV	Guaranteed LOW Signal for All Inputs (with one input tied to V_{BB}) V_{BB} (Min) − V_{DIFF}	
I_{IL}	Input LOW Current	0.50		0.50		μA	V_{IN} = V_{IL} (Min)	
I_{IH}	Input HIGH Current		240		240	μA	V_{IN} = V_{IH} (Max), D_a–D_e = V_{BB}, $\overline{D}_a$–$\overline{D}_e$ = V_{IL} (Min)	
I_{CBO}	Input Leakage Current	−10		−10		μA	V_{IN} = V_{EE}, D_a–D_e = V_{BB} $\overline{D}_a$–$\overline{D}_e$ = V_{IL} (Min)	
I_{EE}	Power Supply Current	−60	−30	−60	−30	mA	D_a–D_e = V_{BB}, $\overline{D}_a$–$\overline{D}_e$ = V_{IL} (Min)	

Note 1: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

PCC AC Electrical Characteristics V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = −40°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
f_{MAXFS}	Toggle Frequency (Full Swing)	250		250		250		MHz	(Note 2)
f_{MAXRS}	Toggle Frequency (Reduced Swing)	700		700		700		MHz	(Note 3)
t_{PLH} t_{PHL}	Propagation Delay Data to Output	0.65	1.70	0.65	1.80	0.70	1.80	ns	*Figures 1* and *2*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.20	1.40	0.35	1.10	0.35	1.10	ns	

Military Version

DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = −55°C to +125°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	T_C	Conditions		Notes
V_{OH}	Output HIGH Voltage	−1025		−870	mV	0°C to +125°C	V_{IN} = V_{IH} (Max) or V_{IL} (Min)	Loading with 50Ω to −2.0V	1, 2, 3
		−1085		−870	mV	−55°C			
V_{OL}	Output LOW Voltage	−1830		−1620	mV	0°C to +125°C			
		−1830		−1555	mV	−55°C			

Military Version (Continued)

DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = −55°C to +125°C (Note 3) (Continued)

Symbol	Parameter	Min	Typ	Max	Units	T_C	Conditions		Notes
V_{OHC}	Output HIGH Voltage	−1035			mV	0°C to +125°C	V_{IN} = V_{IH} (Max) or V_{IL} (Min)	Loading with 50Ω to −2.0V	1, 2, 3
		−1085			mV	−55°C			
V_{OLC}	Output LOW Voltage			−1610	mV	0°C to +125°C			
				−1555	mV	−55°C			
V_{BB}	Output Reference Voltage			−1260	mV	0°C to +125°C	I_{VBB} = 0 μA, V_{EE} = 4.2V		1,2,3
		−1380		−1260	mV	0°C to +125°C	I_{VBB} = −250 μA, V_{EE} = −5.7V		1, 2, 3
		−1396			mV	−55°C	I_{VBB} = −350 μA, V_{EE} = −5.7V		
V_{DIFF}	Input Voltage Differential	150			mV	−55°C to +125°C	Required for Full Output Swing		1, 2, 3
V_{CM}	Common Mode Voltage	V_{CC} − 2.0		V_{CC} − 0.5	V	−55°C to +125°C			1, 2, 3
V_{IH}	Single-Ended Input High Voltage	−1165		−870	mV	−55°C to +125°C	Guaranteed HIGH Signal for All Inputs (with $\overline{D_n}$ tied to V_{BB})		1, 2, 3, 4
V_{IL}	Single-Ended Input Low Voltage	−1830		−1475	mV	−55°C to +125°C	Guaranteed LOW Signal for All Inputs (with $\overline{D_n}$ tied to V_{BB})		1, 2, 3, 4
I_{IH}	Input HIGH Current			50	μA	0°C to +125°C	V_{IN} = $V_{IH\,(Max)}$, D_a–D_e = V_{BB}, $\overline{D}_a$–$\overline{D}_e$ = $V_{IL\,(Min)}$		1, 2, 3
				70	μA	−55°C			
I_{CBO}	Input Leakage Current	−10			μA	−55°C to +125°C	V_{IN} = V_{EE}, D_a–D_e = V_{BB}, $\overline{D}_a$–$\overline{D}_e$ = $V_{IL\,(Min)}$		1, 2, 3
I_{EE}	Power Supply Current	−65		−25	mA	−55°C to +125°C	D_a–D_e = V_{BB}, $\overline{D}_a$–$\overline{D}_e$ = $V_{IL\,(Min)}$		1, 2, 3

Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals −55°C), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 2: Screen tested 100% on each device at −55°C, +25°C, and +125°C, Subgroups 1, 2, 3, 7, and 8.

Note 3: Sample tested (Method 5005, Table I) on each manufactured lot at −55°C, +25°C, and +125°C, Subgroups A1, 2, 3, 7, and 8.

Note 4: Guaranteed by applying specified input condition and testing V_{OH}/V_{OL}.

AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = −55°C		T_C = +25°C		T_C = +125°C		Units	Conditions	Notes
		Min	Max	Min	Max	Min	Max			
t_{PLH} t_{PHL}	Propagation Delay Data to Output	0.40	2.30	0.60	2.20	0.60	2.70	ns	*Figures 1* and *2*	1, 2, 3
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.20	1.40	0.20	1.40	0.20	1.40	ns		4

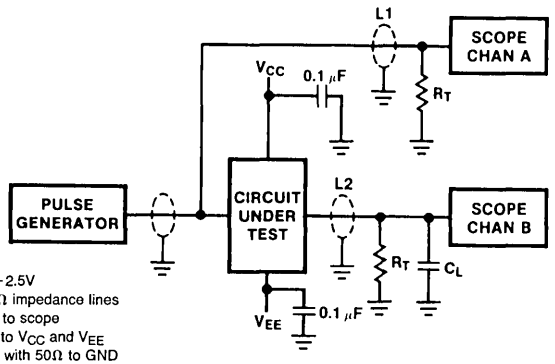
Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals −55°C), then testing immediately after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 2: Screen tested 100% on each device at +25°C temperature only, Subgroup A9.

Note 3: Sample tested (Method 5005, Table I) on each manufactured lot at +25°C, Subgroup A9, and at +125°C and −55°C temperatures, Subgroups A10 and A11.

Note 4: Not tested at +25°C, +125°C and −55°C temperature (design characterization data).

Test Circuit

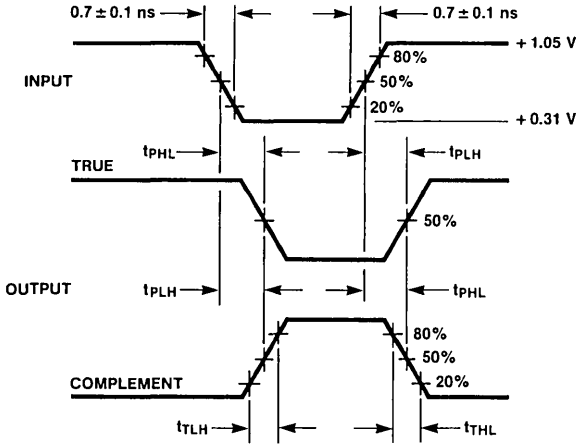


Notes: V_{CC}, V_{CCA} = +2V, V_{EE} = −2.5V
L1 and L2 = equal length 50Ω impedance lines
R_T = 50Ω terminator internal to scope
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
All unused outputs are loaded with 50Ω to GND
C_L = Fixture and stray capacitance ≤ 3 pF

TL/F/10260–5

FIGURE 1. AC Test Circuit

Switching Waveforms



TL/F/10260–6

FIGURE 2. Propagation Delay and Transition Times

National Semiconductor

100315
Low-Skew Quad Clock Driver

General Description

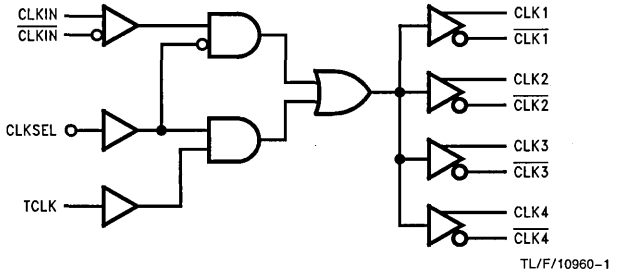
The 100315 contains four low skew differential drivers, designed for generation of multiple, minimum skew differential clocks from a single differential input. This device also has the capability to select a secondary single-ended clock source for use in lower frequency system level testing. The 100315 is a 300 Series redesign of the 100115 clock driver.

Features

- Low output to output skew (≤50 ps)
- Differential inputs and outputs
- Small outline package (SOIC)
- Secondary clock available for system level testing
- 2000V ESD protection
- Voltage compensated operating range: −4.2V to −5.7V
- Military and industrial grades available

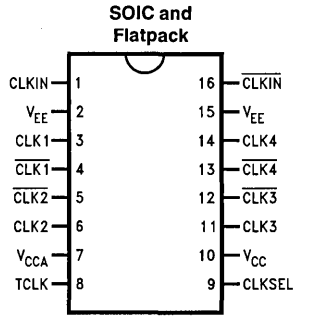
Ordering Code: See Section 6

Logic Diagram



TL/F/10960–1

Connection Diagram



TL/F/10960–2

Pin Names	Description
CLKIN, $\overline{\text{CLKIN}}$	Differential Clock Inputs
CLK_{1-4}, $\overline{CLK}_{1-4}$	Differential Clock Outputs
TCLK	Test Clock Input†
CLKSEL	Clock Input Select†

†TCLK and CLKSEL are single-ended inputs, with internal 50 kΩ pulldown resistors.

Truth Table

CLKSEL	CLKIN	$\overline{\text{CLKIN}}$	TCLK	CLK_N	$\overline{CLK_N}$
L	L	H	X	L	H
L	H	L	X	H	L
H	X	X	L	L	H
H	X	X	H	H	L

L = Low Voltage Level
H = High Voltage Level
X = Don't Care

Absolute Maximum Ratings

Above which the useful life may be impaired (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Maximum Junction Temperature (T_J)	
Plastic	+150°C
Ceramic	+175°C
Case Temperature under Bias (T_C)	0°C to +85°C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
Input Voltage (DC)	V_{CC} to +0.5V
Output Current (DC Output HIGH)	−50 mA
Operating Range (Note 2)	−5.7V to −4.2V
ESD (Note 2)	≥2000V

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: ESD testing conforms to MIL-STD-883, Method 3015.

Recommended Operating Conditions

Case Temperature (T_C)	
Commercial	0°C to +85°C
Industrial	−40°C to +85°C
Military	−55°C to +125°C
Supply Voltage (V_{EE})	−5.7V to −4.2V

Commercial Version

DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions	
V_{OH}	Output HIGH Voltage	−1025	−955	−870	mV	V_{IN} = $V_{IH(Max)}$ or $V_{IL(Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830	−1705	−1620			
V_{OHC}	Output HIGH Voltage	−1035			mV	V_{IN} = $V_{IH(Min)}$ or $V_{IL(Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610			
V_{IH}	Single-Ended Input HIGH Voltage	−1165		−870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Single-Ended Input LOW Voltage	−1830		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL(Min)}$	
I_{IH}	Input High Current					V_{IN} = $V_{IH(Max)}$	
	CLKIN, $\overline{\text{CLKIN}}$			150	μA		
	TCLK			250	μA		
	CLKSEL			250	μA		
V_{DIFF}	Input Voltage Differential	150			mV	Required for Full Output Swing	
V_{CM}	Common Mode Voltage	V_{CC} − 2V		V_{CC} − 0.5V	V		
I_{CBO}	Input Leakage Current	−10			μA	V_{IN} = V_{EE}	
I_{EE}	Power Supply Current	−67		−35	mA		

Note 3: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Commercial Version (Continued)

AC Electrical Characteristics V_{EE} = −4.2V to −4.8V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
f_{MAX}	Maximum Clock Frequency	750		750		750		MHz	
t_{PLH} t_{PHL}	Propagation Delay CLKIN, $\overline{CLKIN}$ to $CLK_{(1-4)}$, $\overline{CLK_{(1-4)}}$ Differential Single-Ended	 0.59 0.59	 0.79 0.99	 0.62 0.62	 0.82 1.02	 0.67 0.67	 0.87 1.07	ns	*Figures 1, 3*
t_{PLH} t_{PHL}	Propagation Delay, TCLK to $CLK_{(1-4)}$, $\overline{CLK_{(1-4)}}$	0.50	1.20	0.50	1.20	0.50	1.20	ns	*Figures 1, 2*
t_{PLH} t_{PHL}	Propagation Delay, CLKSEL to $CLK_{(1-4)}$, $\overline{CLK_{(1-4)}}$	0.80	1.60	0.80	1.60	0.80	1.60	ns	*Figures 1, 2*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.30	0.80	0.30	0.80	0.30	0.80	ns	*Figures 1, 4*
t_{OST} DIFF	Maximum Skew Opposite Edge Output-to-Output Variation Data to Output Path		50		50		50	ps	(Note 1)

Note 1: Output-to-Output Skew is defined as the absolute value of the difference between the actual propagation delay for any outputs within the same packaged device. The specifications apply to any outputs switching in the same direction either HIGH to LOW (t_{OSHL}), or LOW to HIGH (t_{OSLH}), or in opposite directions both HL and LH (t_{OST}). Parameters t_{OST} and t_{PS} guaranteed by design.

Industrial Version

DC Electrical Characteristics V_{EE} = −4.2V to −5.7, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = −40°C		T_C = 0°C to +85°C		Units	Conditions	
		Min	Max	Min	Max			
V_{OH}	Output HIGH Voltage	−1085	−870	−1025	−870	mV	V_{IN} = $V_{IH(Max)}$ or $V_{IL(Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830	−1575	−1830	−1620	mV	V_{IN} = $V_{IH(Min)}$ or $V_{IL(Max)}$	
V_{OHC}	Output HIGH Voltage	−1095		−1035		mV	V_{IN} = $V_{IH(Max)}$ or $V_{IL(Min)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage		−1565		−1610	mV	V_{IN} = $V_{IH(Min)}$ or $V_{IL(Max)}$	
V_{IH}	Single-Ended Input HIGH Voltage	−1170	−870	−1165	−870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Single-Ended Input LOW Voltage	−1830	−1480	−1830	−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50		0.50		μA	V_{IN} = $V_{IL(Min)}$	

Industrial Version (Continued)

DC Electrical Characteristics V_{EE} = −4.2V to −5.7, V_{CC} = V_{CCA} = GND (Continued)

Symbol	Parameter	T_C = −40°C		T_C = 0°C to +85°C		Units	Conditions
		Min	Max	Min	Max		
I_{IH}	Input HIGH Current						
	CLKIN, $\overline{CLKIN}$		107		107	µA	V_{IN} = $V_{IH\ (Max)}$
	TCLK		300		300	µA	
	CLKSEL		260		260	µA	
V_{DIFF}	Input Voltage Differential	150		150		mV	Required for Full Output Swing
V_{CM}	Common Mode Voltage	V_{CC} − 2V		V_{CC} − 0.5V		V	
I_{CBO}	Input Leakage Current	−10		−10		µA	V_{IN} = V_{EE}
I_{EE}	Power Supply Current	−70	−30	−70	−30	mA	

AC Electrical Characteristics V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = −40°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
f_{MAX}	Maximum Clock Frequency	750		750		750		MHz	
t_{PLH} t_{PHL}	Propagation Delay CLKIN, $\overline{CLKIN}$ to $CLK_{(1-4)}$, $\overline{CLK}_{(1-4)}$							ns	*Figures 1, 3*
	Differential	0.59	0.99	0.62	0.82	0.67	0.87		
	Single-Ended	0.59	0.99	0.62	1.02	0.67	1.07		
t_{PLH} t_{PHL}	Propagation Delay, TCLK to $CLK_{(1-4)}$, $\overline{CLK}_{(1-4)}$	0.50	1.20	0.50	1.20	0.50	1.20	ns	*Figures 1, 2*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.30	0.80	0.30	0.80	0.30	0.80	ns	
t_{OST} DIFF	Maximum Skew Opposite Edge Output-to-Output Variation to Output Path		50		50		50	ps	(Note 1)

Note 1: Output-to-Output Skew is defined as the absolute value of the difference between the actual propagation delay for any outputs within the same package device. The specifications apply to any outputs switching in the same direction either HIGH to LOW (t_{OSHL}), or LOW to HIGH (t_{OSLH}), or in opposite directions both HL and LH (t_{OST}). Parameters t_{OST} and t_{PS} guaranteed by design.

Military Version—Preliminary

DC Electrical Characteristics V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	T_C	Conditions		Notes
V_{OH}	Output HIGH Voltage	−1025		−870	mV	0°C to +125°C	V_{IN} = $V_{IH(Max)}$ or $V_{IL(Min)}$	Loading with 50Ω to −2.0V	1, 2, 3
		−1085		−870	mV	−55°C			
V_{OL}	Output LOW Voltage	−1830		−1620	mV	0°C to +125°C			
		−1830		−1555	mV	−55°C			
V_{OHC}	Output HIGH Voltage	−1035			mV	0°C to +125°C	V_{IN} = $V_{IH(Min)}$ or $V_{IL(Max)}$	Loading with 50Ω to −2.0V	1, 2, 3
		−1085			mV	−55°C			
V_{OLC}	Output LOW Voltage			−1610	mV	0°C to +125°C			
				−1555	mV	−55°C			

Military Version—Preliminary (Continued)

DC Electrical Characteristics V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND (Note 3) (Continued)

Symbol	Parameter	Min	Typ	Max	Units	T_C	Conditions	Notes
V_{DIFF}	Input Voltage Differential	150			mV	−55°C to +125°C	Required for Full Output Swing	1, 2, 3
V_{CM}	Common Mode Voltage	V_{CC} − 2.0		V_{CC} − 0.5	V	−55°C to +125°C		1, 2, 3
V_{IH}	Single-Ended Input High Voltage	−1165		−870	mV	−55°C to +125°C	Guaranteed HIGH Signal for All Inputs	1, 2, 3, 4
V_{IL}	Single-Ended Input Low Voltage	−1830		−1475	mV	−55°C to +125°C	Guaranteed LOW Signal for All Inputs	1, 2, 3, 4
I_{IH}	Input HIGH Current CLKIN, $\overline{CLKIN}$			120	μA	−55°C to +125°C	V_{IN} = $V_{IH(Max)}$	1, 2, 3
	TCLK			350	μA			
	CLKSEL			300	μA			
I_{CBO}	Input Leakage Current	−10			μA	−55°C to +125°C	V_{IN} = V_{EE}	1, 2, 3
I_{EE}	Power Supply Current, Normal	−90		−30	mA	−55°C to +125°C		1, 2, 3

Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals −55°C), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 2: Screen tested 100% on each device at −55°C, +25°C, and +125°C, Subgroups 1, 2, 3, 7, and 8.

Note 3: Sample tested (Method 5005, Table I) on each manufactured lot at −55°C, +25°C, and +125°C, Subgroups A1, 2, 3, 7, and 8.

Note 4: Guaranteed by applying specified input condition and testing V_{OH}/V_{OL}.

AC Electrical Characteristics V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = −55°C		T_C = +25°C		T_C = +125°C		Units	Conditions	Notes
		Min	Max	Min	Max	Min	Max			
t_{PLH} t_{PHL}	Propagation Delay CLKIN, $\overline{CLKIN}$ to $CLK_{(1-4)}$, $\overline{CLK}_{(1-4)}$	0.61	0.81	0.61	0.81	0.60	0.83	ns	*Figures 1* and *2*	1, 2, 3
t_{PLH} t_{PHL}	Propagation Delay, TCLK to $CLK_{(1-4)}$, $\overline{CLK}_{(1-4)}$	0.50	1.20	0.50	1.20	0.50	1.20	ns		
t_{SG-G}	Skew Gate to Gate (Note 5)		100		100		100	ps		4
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.35	0.80	0.30	0.75	0.25	0.75	ns		

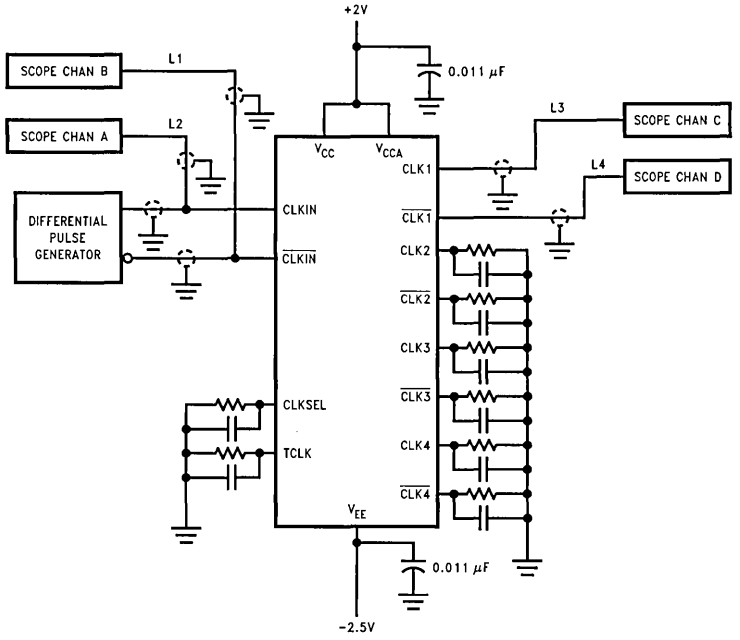
Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals −55°C, then testing immediately after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 2: Screen tested 100% on each device at +25°C temperature only, Subgroup A9.

Note 3: Sample tested (Method 5005, Table I) on each manufactured lot at +25°C, Subgroup A9, and at +125°C and −55°C temperatures, Subgroups A10 and A11.

Note 4: Not tested at +25°C, +125°C and −55°C temperature (design characterization data).

Note 5: Maximum output skew for any one device.



TL/F/10960–3

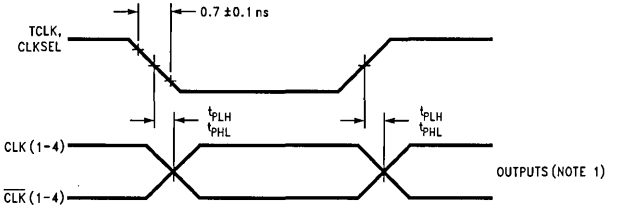
Note 1: Shown for testing CLKIN to CLK1 in the differential mode.

Note 2: L1, L2, L3 and L4 = equal length 50Ω impedance lines.

Note 3: All unused inputs and outputs are loaded with 50Ω in parallel with ≤3 pF to GND.

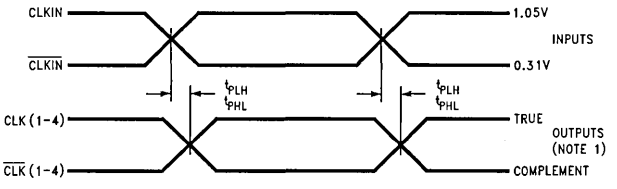
Note 4: Scope should have 50Ω input terminator internally.

FIGURE 1. AC Test Circuit



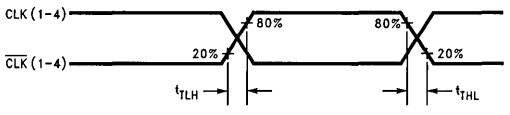
TL/F/10960–4

FIGURE 2. Propagation Delay, TCLK, CLKSEL to Outputs



TL/F/10960–5

FIGURE 3. Propagation Delay, CLKIN/$\overline{\text{CLKIN}}$ to Outputs



TL/F/10960–6

FIGURE 4. Transition Times

Note 1: The output to output skew, which is defined as the difference in the propagation delays between each of the four outputs on any one 100115 shall not exceed 75 ps.

National Semiconductor

100316
Low Power Quad Differential Line Driver with Cut-Off

General Description

The 100316 is a quad differential line driver with output cut-off capability. The outputs are designed to drive a doubly terminated 50Ω transmission line (25Ω equivalent impedance) in an ECL backplane. The 100316 is ideal for driving low noise, differential ECL backplanes. A LOW on the output enable (OE) will set both the true and complementary outputs into a high impedance or cut-off state, isolating them from the backplane. The cut-off state is designed to be more negative than a normal ECL LOW state.

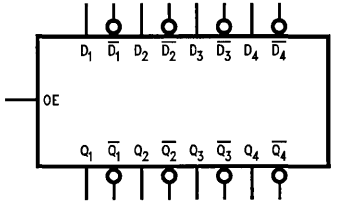
Unlike most 100K devices, the data inputs (D_n, $\overline{D}_n$) do not have input pull-down resistors. An internal reference supply (V_{BB}) is available for single-ended operation.

Features

- Differential inputs and outputs
- Output cut-off capability
- Drives 25Ω load
- V_{BB} available for single-ended operation
- 2000V ESD protection
- Voltage compensated operating range = −4.2V to −5.7V
- Available to industrial grade temperature range

Ordering Code: See Section 6

Logic Symbol

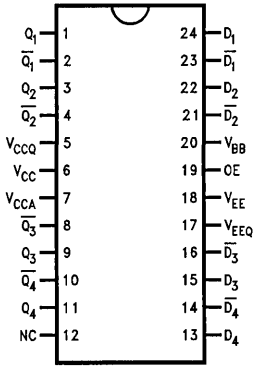


TL/F/10922–1

Pin Names	Description
D_n	Data Inputs
Q_n	Data Outputs
$\overline{Q}_n$	Complementary Data Outputs
OE	Output Enable

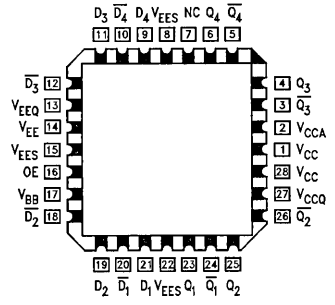
Connection Diagrams

24-Pin DIP



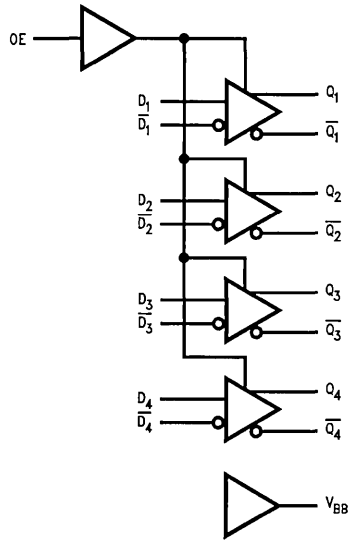
TL/F/10922–2

28-Pin PCC



TL/F/10922–3

Logic Diagram



TL/F/10922–5

Truth Table

Inputs			Outputs	
D_n	$\overline{D}_n$	OE	Q_n	$\overline{Q}_n$
L	H	H	L	H
H	L	H	H	L
X	X	L	Cut-Off	Cut-Off

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Cut-Off = Lower-than-Low State

Absolute Maximum Ratings

Above which the useful life may be impaired (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature (T_{STG})	−65°C to +150°C
Maximum Junction Temperature (T_J)	
Ceramic	+175°C
Plastic	+150°C
Pin Potential to Ground Pin (V_{EE})	−7.0V to 0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Output Current (DC Output HIGH)	−100 mA
ESD (Note 2)	≥2000V

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Function operation under these conditions is not implied.

Note 2: ESD testing conforms to MIL-STD-883, Method 3015.

Recommended Operating Conditions

Case Temperature (T_C)	
Commercial	0°C to +85°C
Industrial	−40°C to +85°C
Military	−55°C to +125°C
Supply Voltage (V_{EE})	−5.7V to −4.2V

Commercial Version

DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions	
V_{OH}	Output HIGH Voltage	−1025	−955	−870	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 25Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830	−1705	−1620	mV		
V_{OHC}	Output HIGH Voltage	−1035			mV	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	Loading with 25Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610	mV		
V_{OLZ}	Cut-Off LOW Voltage			−1950	mV	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	OE = LOW
V_{BB}	Output Reference Voltage	−1380	−1320	−1260	mV	I_{VBB} = −1 mA	
V_{DIFF}	Input Voltage Differential	150			mV	Required for Full Output Swing	
V_{CM}	Common Mode Voltage	V_{CC} − 2.0		V_{CC} − 0.5	V		
V_{IH}	Single-Ended Input High Voltage	−1110		−870	mV	Guaranteed HIGH Signal for All Inputs (with one input tied to V_{BB}) $V_{BB\ (Max)}$ + V_{DIFF}	
V_{IL}	Single-Ended Input Low Voltage	−1830		−1530	mV	Guaranteed LOW Signal for All Inputs (with one input tied to V_{BB}) $V_{BB\ (Min)}$ − V_{DIFF}	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	
I_{IH}	Input HIGH Current D_N			250	μA	V_{IN} = $V_{IH\ (Max)}$, D_1 = V_{BB}, $\overline{D}_1$ = $V_{IL\ (Min)}$	
I_{IHZ}	Input HIGH Current OE			360	μA	V_{IN} = $V_{IH\ (Max)}$, D_1 = V_{BB}, $\overline{D}_1$ = $V_{IL\ (Min)}$	
I_{CBO}	Input Leakage Current	−10			μA	V_{IN} = V_{EE}, D_1 = V_{BB}, $\overline{D}_1$ = $V_{IL\ (Min)}$	
I_{EE}	Power Supply Current, Normal	−85		−30	mA	D_1 = V_{BB}, $\overline{D}_1$ = $V_{IL\ (Min)}$	
I_{EEZ}	Power Supply Current, Cut-Off	−152		−75	mA	D_1–D_4 = V_{BB}, $\overline{D}_1$–$\overline{D}_4$ = $V_{IL\ (Min)}$, OE = LOW	

Note 3: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

Commercial Version (Continued)

DIP AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Data to Output	0.65	2.30	0.65	2.30	0.65	2.30	ns	
t_{PZH} t_{PHZ}	Propagation Delay OE to Output	1.80 1.20	4.20 3.10	1.80 1.20	4.20 3.10	1.80 1.20	4.20 3.10	ns	*Figures 1* and *2*
t_{TLH} t_{THL}	Transition Time, D_N to Q_N 20% to 80%, 80% to 20%	0.45	1.70	0.45	1.70	0.45	1.70	ns	

PCC AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Data to Output	0.65	2.10	0.65	2.10	0.65	2.10	ns	
t_{PZH} t_{PHZ}	Propagation Delay OE to Output	1.8 1.2	4.00 2.90	1.8 1.2	4.00 2.90	1.8 1.2	4.00 2.90	ns	*Figures 1* and *2*
t_{TLH} t_{THL}	Transition Time, D_N to Q_N 20% to 80%, 80% to 20%	0.45	1.50	0.45	1.50	0.45	1.50	ns	

Industrial Version

PCC DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND (Note 3)

Symbol	Parameter	T_C = −40°C		T_C = 0°C to +85°C		Units	Conditions	
		Min	Max	Min	Max			
V_{OH}	Output HIGH Voltage	−1085	−870	−1025	−870	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 25Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830	−1585	−1830	−1620	mV		
V_{OHC}	Output HIGH Voltage	−1095		−1035		mV	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	Loading with 25Ω to −2.0V
V_{OLC}	Output LOW Voltage		−1575		−1610	mV		
V_{OLZ}	Cut-Off LOW Voltage		−1900		−1950	mV	OE = LOW, V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	
V_{BB}	Output Reference Voltage	−1395	−1255	−1380	−1260	mV	I_{VBB} = −1 mA	
V_{DIFF}	Input Voltage Differential	150		150		mV	Required for Full Output Swing	
V_{CM}	Common Mode Voltage	V_{CC} − 2.0	V_{CC} − 0.5	V_{CC} − 2.0	V_{CC} − 0.5	V		
V_{IH}	Single-Ended Input High Voltage	−1115	−870	−1110	−870	mV	Guaranteed HIGH Signal for All Inputs (with one input tied to V_{BB}) $V_{BB\ (Max)}$ + V_{DIFF}	
V_{IL}	Single-Ended Input Low Voltage	−1830	−1535	−1830	−1530	mV	Guaranteed LOW Signal for All Inputs (with one input tied to V_{BB}) $V_{BB\ (Min)}$ − V_{DIFF}	
I_{IL}	Input LOW Current	0.50		0.50		μA	V_{IN} = $V_{IL\ (Min)}$	
I_{IH}	Input HIGH Current, D_N		240		240	μA	V_{IN} = $V_{IH\ (Max)}$, D_1 = V_{BB}, $\overline{D}_1$ = $V_{IL\ (Min)}$	
I_{IHZ}	Input HIGH Current, OE		360		360			
I_{CBO}	Input Leakage Current	−10		−10		μA	V_{IN} = V_{EE}, D_1 = V_{BB}, $\overline{D}_1$ = $V_{IL\ (Min)}$	
I_{EE}	Power Supply Current, Normal	−85	−30	−85	−30	mA	D_1 = V_{BB}, $\overline{D}_1$ = $V_{IL\ (Min)}$	
I_{EEZ}	Power Supply Current, Cut-Off	−152	−75	−152	−75	mA	D_1–D_4 = V_{BB}, $\overline{D}_1$–$\overline{D}_4$ = $V_{IL\ (Min)}$, OE = LOW	

Note 3: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

PCC AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = −40°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Data to Output	0.65	2.10	0.65	2.10	0.65	2.10	ns	*Figures 1* and *2*
t_{PZH} t_{PHZ}	Propagation Delay OE to Output	1.80 1.20	4.00 2.90	1.80 1.20	4.00 2.90	1.80 1.20	4.00 2.90	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.50	0.45	1.50	0.45	1.50	ns	

Military Version—Preliminary

DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	T_C	Conditions		Notes
V_{OH}	Output HIGH Voltage	−1025		−870	mV	0°C to +125°C	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 25Ω to −2.0V	1, 2, 3
		−1085		−870	mV	−55°C			
V_{OL}	Output LOW Voltage	−1830		−1620	mV	0°C to +125°C			
		−1830		−1555	mV	−55°C			
V_{OHC}	Output HIGH Voltage	−1035			mV	0°C to +125°C	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	Loading with 25Ω to −2.0V	1, 2, 3
		−1085			mV	−55°C			
V_{OLC}	Output LOW Voltage			−1610	mV	0°C to +125°C			
				−1555	mV	−55°C			
V_{OLZ}	Cut-Off LOW Voltage			−1900	mV	0°C to +125°C	OE = LOW V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$		1, 2, 3
				−1950	mV	−55°C			
V_{BB}	Output Reference Voltage			−1260	mV	0°C to +125°C	I_{VBB} = 0 μA, V_{EE} = 4.2V		1, 2, 3
		−1380	−1320	−1260	mV	0°C to +125°C	I_{VBB} = −250 μA, V_{EE} = −5.7V		1, 2, 3
		−1396			mV	−55°C	I_{VBB} = −350 μA, V_{EE} = −5.7V		
V_{DIFF}	Input Voltage Differential	150			mV	−55°C to +125°C	Required for Full Output Swing		1, 2, 3
V_{CM}	Common Mode Voltage	V_{CC} − 2.0		V_{CC} − 0.5	V	−55°C to +125°C			1, 2, 3
V_{IH}	Single-Ended Input High Voltage	−1165		−870	mV	−55°C to +125°C	Guaranteed HIGH Signal for All Inputs (with $\overline{D_n}$ tied to V_{BB})		1, 2, 3, 4
V_{IL}	Single-Ended Input Low Voltage	−1830		−1475	mV	−55°C to +125°C	Guaranteed LOW Signal for All Inputs (with $\overline{D_n}$ tied to V_{BB})		1, 2, 3, 4
I_{IH}	Input HIGH Current, D_N			75	μA	0°C to +125°C	V_{IN} = $V_{IH\ (Max)}$, D_1 = V_{BB}, $\overline{D}_1$ = $V_{IL\ (Min)}$		1, 2, 3
				95	μA	−55°C			
I_{IHZ}	Input HIGH Current, OE			360	μA	−55°C to +125°C	V_{IN} = $V_{IH\ (Max)}$, D_1 = V_{BB}, $\overline{D}_1$ = $V_{IL\ (Min)}$		1, 2, 3
I_{CBO}	Input Leakage Current	−10			μA	−55°C to +125°C	V_{IN} = V_{EE}, D_1 = V_{BB}, $\overline{D}_1$ = $V_{IL\ (Min)}$		1, 2, 3
I_{EE}	Power Supply Current, Normal	−90		−30	mA	−55°C to +125°C	D_1 = V_{BB}, $\overline{D}_1$ = $V_{IL\ (Min)}$		1, 2, 3
I_{EEZ}	Power Supply Current, Cut-Off	−180		−75	mA	−55°C to +125°C	D_1−D_2 = V_{BB}, $\overline{D}_1$−$\overline{D}_2$ = $V_{IL\ (Min)}$, OE = LOW		1, 2, 3

Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals −55°C), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 2: Screen tested 100% on each device at −55°C, +25°C, and +125°C, Subgroups 1, 2, 3, 7, and 8.

Note 3: Sample tested (Method 5005, Table I) on each manufactured lot at −55°C, +25°C, and +125°C, Subgroups A1, 2, 3, 7, and 8.

Note 4: Guaranteed by applying specified input condition and testing V_{OH}/V_{OL}.

Military Version—Preliminary (Continued)

AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = −55°C		T_C = +25°C		T_C = +125°C		Units	Conditions	Notes
		Min	Max	Min	Max	Min	Max			
t_{PLH} t_{PHL}	Propagation Delay Data to Output	0.40	2.50	0.50	2.40	0.50	2.90	ns	*Figures 1* and *2*	1, 2, 3
t_{PZH} t_{PHZ}	Propagation Delay OE to Output	0.70 0.70	4.20 3.20	0.70 0.70	4.20 3.20	0.70 0.70	4.20 3.20	ns		
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.20	1.70	0.20	1.70	0.20	1.50	ns		4

Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals −55°C), then testing immediately after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 2: Screen tested 100% on each device at +25°C temperature only, Subgroup A9.

Note 3: Sample tested (Method 5005, Table I) on each manufactured lot at +25°C, Subgroup A9, and at +125°C and −55°C temperatures, Subgroups A10 and A11.

Note 4: Not tested at +25°C, +125°C and −55°C temperature (design characterization data).

Test Circuitry

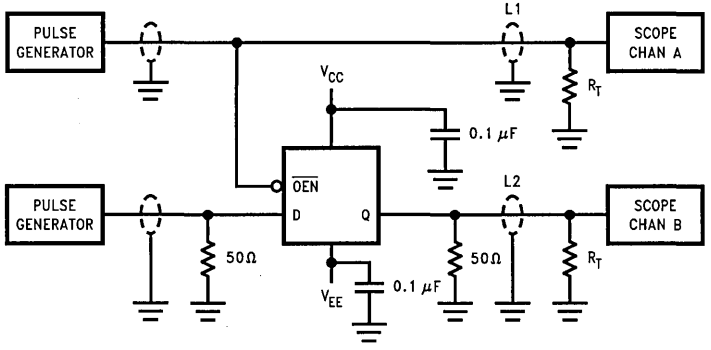


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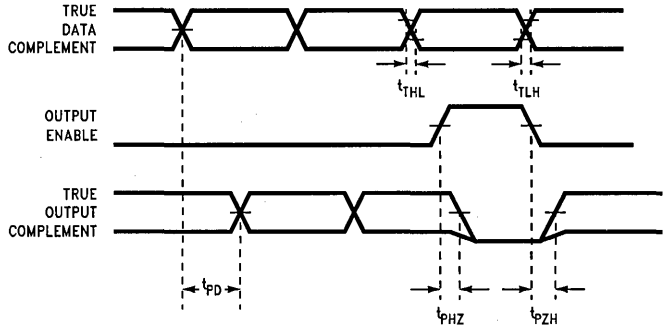
FIGURE 1. AC Test Circuit

Notes:
V_{CC}, V_{CCA} = +2V, V_{EE} = −2.5V
L1 and L2 = equal length 50Ω impedance lines
R_T = 50Ω terminator internal to scope
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
All unused outputs are loaded with 25Ω to GND
C_L = Fixture and stray capacitance ≤ 3 pF

Switching Waveforms



TL/F/10922–7

FIGURE 2. Propagation Delay, Cut-Off and Transition Times

National Semiconductor

100319
Low Power Hex Line Driver with Cut-Off

General Description

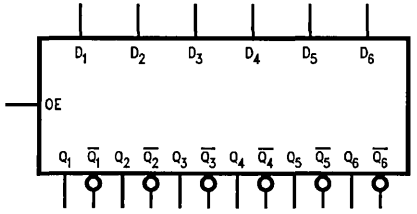
The 100319 is a Hex Line Driver with output cut-off capability. The 100319 has single ended ECL inputs and differential ECL outputs, designed to drive a differential, doubly terminated 50Ω transmission line (25Ω equivalent impedance) in an ECL backplane. A LOW on the Output Enable (OE) will set both the true and complementary outputs, to a high impedance or cut-off state. The cut-off state is designed to be more negative than a normal ECL LOW state.

Features

- Differential outputs
- Output cut-off capability
- Drives a 25Ω ECL load
- 2000V ESD protection
- Voltage compensated range = −4.2V to −5.7V
- Available to industrial grade temperature range

Ordering Code: See Section 6

Logic Symbol



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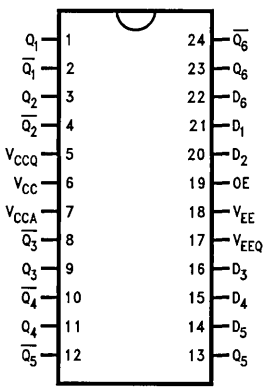
Pin Names	Description
D_n	Data Inputs
Q_n	Data Outputs
$\overline{Q}_n$	Complementary Data Outputs
OE	Output Enable

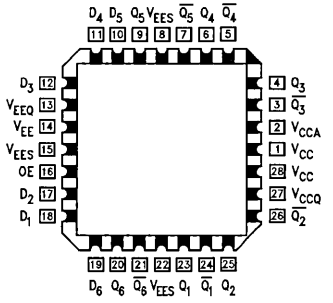
Connection Diagrams

24-Pin DIP



TL/F/10923–2

28-Pin PCC



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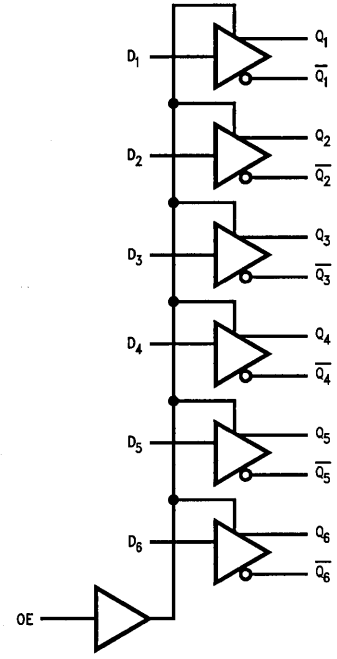
Logic Diagram



TL/F/10923–5

Truth Table

Inputs		Outputs	
D_n	OE	Q_n	$\overline{Q_n}$
L	H	L	H
H	H	H	L
X	L	Cut-Off	Cut-Off

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Cut-off = Lower-than-Low State

Absolute Maximum Ratings

Above which the useful life may be impaired (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature (T_{STG})	−65°C to +150°C
Maximum Junction Temperture (T_J)	
Ceramic	+175°C
Plastic	+150°C
Pin Potential to Ground Pin (V_{EE})	−7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Output Current (DC Output HIGH)	−100 mA
ESD (Note 2)	≥2000V

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: ESD testing conforms to MIL-STD-883, Method 3015.

Recommended Operating Conditions

Case Temperature (T_C)	
Commercial	0°C to +85°C
Industrial	−40°C to +85°C
Military	−55°C to +125°C
Supply Voltage (V_{EE})	−5.7V to −4.2V

Commercial Version

DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions	
V_{OH}	Output HIGH Voltage	−1025	−955	−870	mV	V_{IN} = $V_{IH(Max)}$ or $V_{IL(Min)}$	Loading with 25Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830	−1705	−1620	mV		
V_{OHC}	Output HIGH Voltage	−1035			mV	V_{IN} = $V_{IH(Min)}$ or $V_{IL(Max)}$	Loading with 25Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610	mV		
V_{OLZ}	Cut-Off LOW Voltage			−1950	mV	V_{IN} = $V_{IH(Min)}$ or $V_{IL(Max)}$	OE = LOW
V_{IH}	Input HIGH Voltage	−1110		−870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1830		−1530	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current			100	μA	V_{IN} = $V_{IL(Min)}$	
I_{IH}	Input HIGH Current			360	μA	V_{IN} = $V_{IH(Max)}$	
I_{EE}	Power Supply Current, Normal	−119		−30	mA		
I_{EEZ}	Power Supply Current, Cut-Off	−219		−75	mA	Inputs Open, OE = LOW	

Note 3: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

Commercial Version (Continued)

DIP AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Data to Output	0.65	2.30	0.65	2.30	0.65	2.30	ns	*Figures 1* and *2*
t_{PZH} t_{PHZ}	Propagation Delay OE to Output	1.8 1.2	4.3 3.1	1.8 1.2	4.3 3.1	1.8 1.2	4.3 3.1	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.50	0.45	1.50	0.45	1.50	ns	

PCC AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Data to Output	0.65	2.10	0.65	2.10	0.65	2.10	ns	*Figures 1* and *2*
t_{PZH} t_{PHZ}	Propagation Delay OE to Output	1.8 1.2	4.1 2.9	1.8 1.2	4.1 2.9	1.8 1.2	4.1 2.9	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.30	0.45	1.30	0.45	1.30	ns	

Industrial Version

PCC DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND (Note 3)

Symbol	Parameter	T_C = −40°C		T_C = 0°C to +85°C		Units	Conditions	
		Min	Max	Min	Max			
V_{OH}	Output HIGH Voltage	−1085	−870	−1025	−870	mV	V_{IN} = $V_{IH(Max)}$ or $V_{IL(Min)}$	Loading with 25Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830	−1575	−1830	−1620	mV		
V_{OHC}	Output HIGH Voltage	−1095		−1035		mV	V_{IN} = $V_{IH(Min)}$ or $V_{IL(Max)}$	Loading with 25Ω to −2.0V
V_{OLC}	Output LOW Voltage		−1565		−1610	mV		
V_{IH}	Input HIGH Voltage	−1115	−870	−1110	−870	mV	Guaranteed HIGH Signal for All Inputs	

Industrial Version (Continued)

PCC DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND (Note 3) (Continued)

Symbol	Parameter	T_C = −40°C		T_C = 0°C to +85°C		Units	Conditions	
		Min	Max	Min	Max			
V_{OLZ}	Cut-Off LOW Voltage		−1900		−1950	mV	V_{IN} = $V_{IH(Min)}$ or $V_{IL(Max)}$	OE = LOW
V_{IL}	Input LOW Voltage	−1830	−1535	−1830	−1530	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current		130		100	μA	V_{IN} = $V_{IL(Min)}$	
I_{IH}	Input HIGH Current		360		360	μA	V_{IN} = $V_{IH(Max)}$	
I_{EE}	Power Supply Current, Normal	−119	−30	−119	−30	mA		
I_{EEZ}	Power Supply Current, Cut-Off	−219	−75	−219	−75	mA	Inputs Open OE = LOW	

Note 3: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

PCC AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = −40°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Data to Output	0.65	2.10	0.65	2.10	0.65	2.10	ns	*Figures 1* and *2*
t_{PZH} t_{PHZ}	Propagation Delay OE to Output	1.8 1.2	4.1 2.9	1.8 1.2	4.1 2.9	1.8 1.2	4.1 2.9	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.30	0.45	1.30	0.45	1.30	ns	

Military Version—Preliminary

DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	T_C	Conditions		Notes
V_{OH}	Output HIGH Voltage	−1025		−870	mV	0°C to +125°C	V_{IN} = $V_{IH(Max)}$ or $V_{IL(Min)}$	Loading with 25Ω to −2.0V	1, 2, 3
		−1085		−870	mV	−55°C			
V_{OL}	Output LOW Voltage	−1830		−1620	mV	0°C to +125°C			
		−1830		−1555	mV	−55°C			
V_{OHC}	Output HIGH Voltage	−1035			mV	0°C to +125°C	V_{IN} = $V_{IH(Min)}$ or $V_{IL(Max)}$	Loading with 25Ω to −2.0V	1, 2, 3
		−1085			mV	−55°C			
V_{OLC}	Output LOW Voltage			−1610	mV	0°C to +125°C			
				−1555	mV	−55°C			
V_{OLZ}	Cut-Off LOW Voltage			−1900	mV	0°C to +125°C	V_{IN} = $V_{IH(Min)}$ or $V_{IL(Max)}$	OE = LOW	1, 2, 3
				−1950	mV	−55°C			

Military Version—Preliminary (Continued)

DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND (Note 3) (Continued)

Symbol	Parameter	Min	Typ	Max	Units	T_C	Conditions	Notes
V_{IH}	Input HIGH Voltage	−1165		−870	mV	−55°C to +125°C	Guaranteed HIGH Signal for All Inputs	1, 2, 3, 4
V_{IL}	Input LOW Voltage	−1830		−1475	mV	−55°C to +125°C	Guaranteed LOW Signal for All Inputs	1, 2, 3, 4
I_{IH}	Input HIGH Current			50	μA	0°C to +125°C	V_{IN} = $V_{IH(Max)}$	1, 2, 3
				70	μA	−55°C		
I_{EE}	Power Supply Current,	−70		−40	mA	−55°C to +125°C		
I_{EEZ}	Power Supply Current, Cut-Off	−180		−130	mA	−55°C to +125°C	Inputs Open, OE = LOW	1, 2, 3

Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals −55°C), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 2: Screen tested 100% on each device at −55°C, +25°C, and +125°C, Subgroups 1, 2, 3, 7, and 8.

Note 3: Sample tested (Method 5005, Table I) on each manufactured lot at −55°C, +25°C, and +125°C, Subgroups A1, 2, 3, 7, and 8.

Note 4: Guaranteed by applying specified input condition and testing V_{OH}/V_{OL}.

AC Electrical Characteristics—Preliminary

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = −55°C		T_C = +25°C		T_C = +125°C		Units	Conditions	Notes
		Min	Max	Min	Max	Min	Max			
t_{PLH} t_{PHL}	Propagation Delay Data to Output	0.40	2.50	0.50	2.40	0.50	2.90	ns	*Figures 1* and *2*	1, 2, 3
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.20	1.70	0.20	1.70	0.20	1.50	ns		4

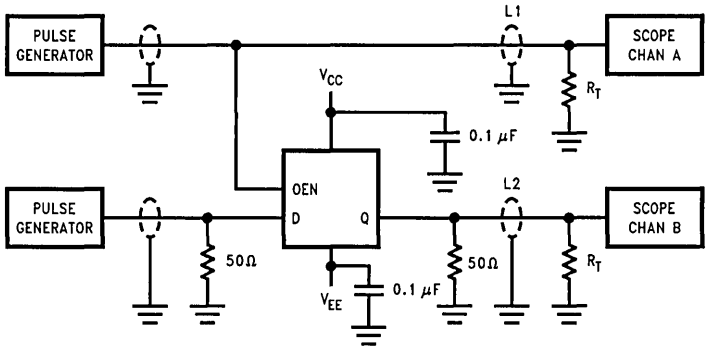
Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals −55°C), then testing immediately after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 2: Screen tested 100% on each device at +25°C temperature only, Subgroup A9.

Note 3: Sample tested (Method 5005, Table I) on each manufactured lot at +25°C, Subgroup A9, and at +125°C and −55°C temperatures, Subgroups A10 and A11.

Note 4: Not tested at +25°C, +125°C and −55°C temperature (design characterization data).

Test Circuitry

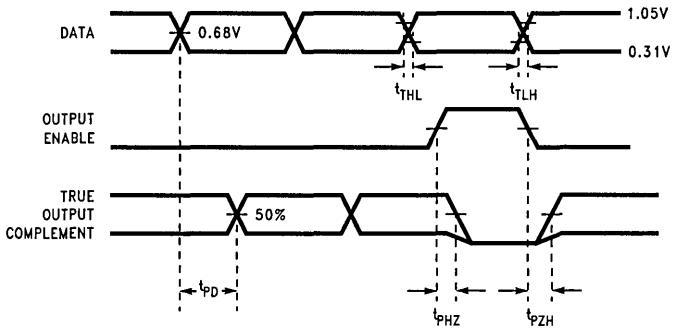


TL/F/10923–6

FIGURE 1. AC Test Circuit

Notes:
V_{CC}, V_{CCA} = +2V, V_{EE} = −2.5V
L1 and L2 = equal length 50Ω impedance lines
R_T = 50Ω terminator internal to scope
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
All unused outputs are loaded with 25Ω to GND
C_L = Fixture and stray capacitance ≤ 3 pF

Switching Waveforms



TL/F/10923–7

NOTE: The output AC measurement point for cut-off propagation delay testing = the 50% voltage point between active V_{OL} and V_{OH}.

FIGURE 2. Propagation Delay, Cut-Off and Transition Times

National Semiconductor

100321
Low Power 9-Bit Inverter

General Description

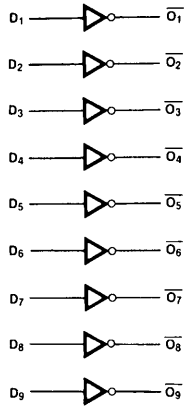
The 100321 is a monolithic 9-bit inverter. The device contains nine inverting buffer gates with single input and output. All inputs have 50 kΩ pull-down resistors.

Features

- 30% power reduction of the 100121
- 2000V ESD protection
- Pin/function compatible with 100121
- Voltage compensated operating range = −4.2V to −5.7V
- Available to industrial grade temperature range
- Available to MIL-STD-883

Ordering Code: See Section 6

Logic Symbol

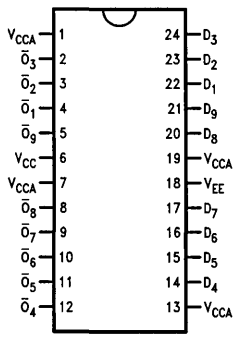


TL/F/10609–1

Pin Names	Description
D_1–D_9	Data Inputs
$\overline{O}_1$–$\overline{O}_9$	Data Outputs

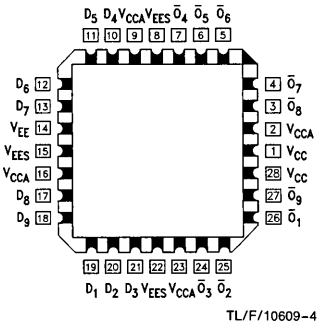
Connection Diagrams

24-Pin DIP



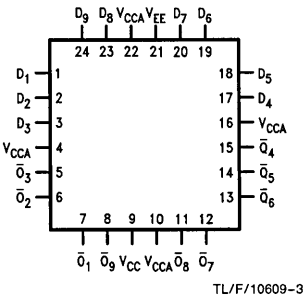
TL/F/10609–2

28-Pin PCC



TL/F/10609–4

24-Pin Quad Cerpak



TL/F/10609–3

Absolute Maximum Ratings

Above which the useful life may be impaired (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature (T_{STG})	−65°C to +150°C
Maximum Junction Temperature (T_J)	
Ceramic	+175°C
Plastic	+150°C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Output Current (DC Output HIGH)	−50 mA
ESD (Note 2)	≥2000V

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functonal operation under these conditions is not implied.

Note 2: ESD testing conforms to MIL-STD-883, Method 3015.

Recommended Operating Conditions

Case Temperature (T_C)	
Commercial	0°C to +85°C
Industrial	−40°C to +85°C
Military	−55°C to +125°C
Supply Voltage (V_{EE})	−5.7V to −4.2V

Commercial Version

DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions	
V_{OH}	Output HIGH Voltage	−1025	−955	−870	mV	V_{IN} = V_{IH} (Max) or V_{IL} (Min)	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830	−1705	−1620	mV		
V_{OHC}	Output HIGH Voltage	−1035			mV	V_{IN} = V_{IH} (Min) or V_{IL} (Max)	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610	mV		
V_{IH}	Input HIGH Voltage	−1165		−870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1830		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = V_{IL} (Min)	
I_{IH}	Input HIGH Current			240	μA	V_{IN} = V_{IH} (Max)	
I_{EE}	Power Supply Current	−65		−30	mA	Inputs Open	

Note 3: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DIP AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Data to Output	0.45	1.45	0.45	1.45	0.45	1.55	ns	*Figures 1* and *2* (Note 1)
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.35	1.20	0.35	1.20	0.35	1.20	ns	*Figures 1* and *2*

Note 1: The propagation delay specified is for single output switching. Delays may vary up to 200 ps with multiple outputs switching.

Commercial Version (Continued)

PCC and Cerpak AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Data to Output	0.45	1.25	0.45	1.25	0.45	1.35	ns	*Figures 1* and *2* (Note 2)
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.35	1.10	0.35	1.10	0.35	1.10	ns	*Figures 1* and *2*
t_{OSHL}	Maximum Skew Common Edge Output-to-Output Variation Data to Output Path		220		220		220	ps	PCC only (Note 1)
t_{OSLH}	Maximum Skew Common Edge Output-to-Output Variation Data to Output Path		270		270		270	ps	PCC only (Note 1)
t_{OST}	Maximum Skew Opposite Edge Output-to-Output Variation Data to Output Path		320		320		320	ps	PCC only (Note 1)
t_{PS}	Maximum Skew Pin (Signal) Transition Variation Data to Output Path		230		230		230	ps	PCC only (Note 1)

Note 1: Output-to-Output Skew is defined as the absolute value of the difference between the actual propagation delay for any outputs within the same packaged device. The specifications apply to any outputs switching in the same direction either HIGH to LOW (t_{OSHL}), or LOW to HIGH (t_{OSLH}), or in opposite directions both HL and LH (t_{OST}). Parameters t_{OST} and t_{PS} guaranteed by design.

Note 2: The propagation delay specified is for single output switching. Delays may vary up to 200 ps with multiple outputs switching.

Industrial Version

PCC DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = −40°C to +85°C (Note 1)

Symbol	Parameter	T_C = −40°C		T_C = 0°C to +85°C		Units	Conditions	
		Min	Max	Min	Max			
V_{OH}	Output HIGH Voltage	−1085	−870	−1025	−870	mV	V_{IN} = V_{IH} (Max) or V_{IL} (Min)	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830	−1575	−1830	−1620	mV		
V_{OHC}	Output HIGH Voltage	−1095		−1035		mV	V_{IN} = V_{IH} (Min) or V_{IL} (Max)	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage		−1565		−1610	mV		
V_{IH}	Input HIGH Voltage	−1170	−870	−1165	−870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1830	−1480	−1830	−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50		0.50		μA	V_{IN} = V_{IL} (Min)	
I_{IH}	Input HIGH Current		300		240	μA	V_{IN} = V_{IH} (Max)	
I_{EE}	Power Supply Current	−65	−30	−65	−30	mA	Inputs Open	

Note 1: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

Industrial Version (Continued)

PCC AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = −40°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Data to Output	0.45	1.25	0.45	1.25	0.45	1.35	ns	*Figures 1* and *2* (Note 1)
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.30	1.20	0.35	1.10	0.35	1.10	ns	*Figures 1* and *2*

Note 1: The propagation delay specified is for single output switching. Delays may vary up to 200 ps with multiple outputs switching.

Military Version

DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = −55°C to +125°C

Symbol	Parameter	Min	Max	Units	T_C	Conditions		Notes
V_{OH}	Output HIGH Voltage	−1025	−870	mV	0°C to +125°C	V_{IN} = V_{IH} (Max) or V_{IL} (Min)	Loading with 50Ω to −2.0V	1, 2, 3
		−1085	−870	mV	−55°C			
V_{OL}	Output LOW Voltage	−1830	−1620	mV	0°C to +125°C			
		−1830	−1555	mV	−55°C			
V_{OHC}	Output HIGH Voltage	−1035		mV	0°C to +125°C	V_{IN} = V_{IH} (Min) or V_{IL} (Max)	Loading with 50Ω to −2.0V	1, 2, 3
		−1085		mV	−55°C			
V_{OLC}	Output LOW Voltage		−1610	mV	0°C to +125°C			
			−1555	mV	−55°C			
V_{IH}	Input HIGH Voltage	−1165	−870	mV	−55°C to +125°C	Guaranteed HIGH Signal for All Inputs		1, 2, 3, 4
V_{IL}	Input LOW Voltage	−1830	−1475	mV	−55°C to +125°C	Guaranteed LOW Signal for All Inputs		1, 2, 3, 4
I_{IL}	Input LOW Current	0.50		μA	−55°C to +125°C	V_{EE} = −4.2V V_{IN} = V_{IL} (Min)		1, 2, 3
I_{IH}	Input HIGH Current		240	μA	0°C to +125°C	V_{EE} = −5.7V V_{IN} = V_{IH} (Max)		1, 2, 3
			340	μA	−55°C			
I_{EE}	Power Supply Current	−70	−25	mA	−55°C to +125°C	Inputs Open		1, 2, 3

Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals −55°C), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 2: Screen tested 100% on each device at −55°C, +25°C, and +125°C, Subgroups 1, 2, 3, 7, and 8.

Note 3: Sample tested (Method 5005, Table 1) on each manufactured lot at −55°C, +25°C and +125°C, Subgroups A1, 2, 3, 7, and 8.

Note 4: Guaranteed by applying specified input condition and testing V_{OH}/V_{OL}.

Military Version (Continued)

AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = −55°C		T_C = +25°C		T_C = +125°C		Units	Conditions	Notes
		Min	Max	Min	Max	Min	Max			
t_{PLH} t_{PHL}	Propagation Delay Data to Output	0.30	1.80	0.40	1.60	0.40	1.80	ns	*Figures 1* and *2*	1, 2, 3, 5
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.30	1.20	0.30	1.20	0.30	1.20	ns		4

Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals −55°C), then testing immediately after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

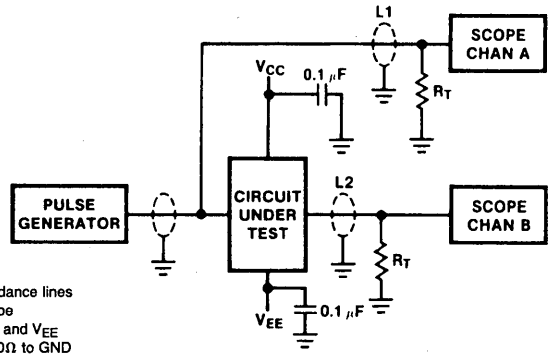
Note 2: Screen tested 100% on each device at +25°C temperature only, Subgroup A9.

Note 3: Sample tested (Method 5005, Table 1) on each mfg. lot at +25°C, Subgroup A9, and at +125°C and −55°C temperatures, Subgroups A10 and A11.

Note 4: Not tested at +25°C, +125°C, and −55°C temperature (design characterization data).

Note 5: The propagation delay specified is for single output switching. Delays may vary up to 200 ps with multiple outputs switching.

Test Circuitry



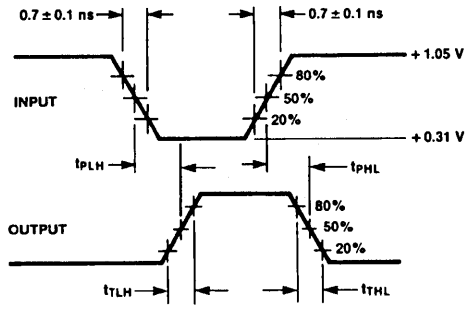
Notes:

V_{CC}, V_{CCA} = +2V, V_{EE} = −2.5V
L1 and L2 = equal length 50Ω impedance lines
R_T = 50Ω terminator internal to scope
Decoupling 0.1 µF from GND to V_{CC} and V_{EE}
All unused outputs are loaded with 50Ω to GND
C_L = Fixture and stray capacitance ≤ 3 pF

TL/F/10609–5

FIGURE 1. AC Test Circuit

Switching Waveforms



TL/F/10609–6

FIGURE 2. Propagation Delay and Transition Times

National Semiconductor

100322
Low Power 9-Bit Buffer

General Description

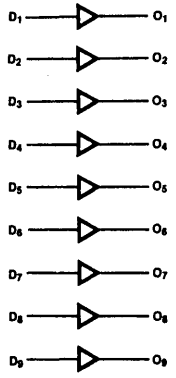
The 100322 is a monolithic 9-bit buffer. The device contains nine non-inverting buffer gates with single input and output. All inputs have 50 kΩ pull-down resistors and all outputs are buffered.

Features

- 30% power reduction of the 100122
- 2000V ESD protection
- Pin/function compatible with 100122
- Voltage compensated operating range = −4.2V to −5.7V
- Available to MIL-STD-883
- Available to industrial grade temperature range

Ordering Code: See Section 6

Logic Symbol

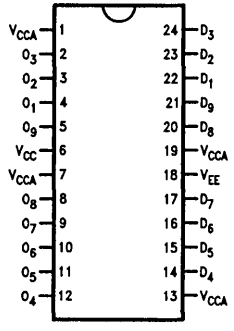


TL/F/10608–1

Pin Names	Description
D_1, D_9	Data Inputs
O_1, O_9	Data Outputs

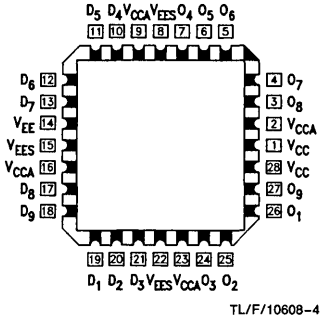
Connection Diagrams

24-Pin DIP



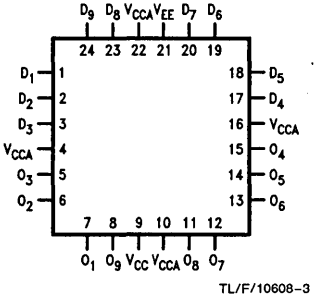
TL/F/10608–2

28-Pin PCC



TL/F/10608–4

24-Pin Quad Cerpak



TL/F/10608–3

Absolute Maximum Ratings

Above which the useful life may be impaired. (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature (T_{STG})	−65°C to +150°C
Maximum Junction Temperature (T_J)	
Ceramic	+175°C
Plastic	+150°C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Output Current (DC Output HIGH)	−50 mA
ESD (Note 2)	≥2000V

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: ESD testing conforms to MIL-STD-883, Method 3015.

Recommended Operating Conditions

Case Temperature (T_C)	
Commercial	0°C to +85°C
Industrial	−40°C to +85°C
Military	−55°C to +125°C
Supply Voltage (V_{EE})	−5.7V to −4.2V

Commercial Version DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions	
V_{OH}	Output HIGH Voltage	−1025	−955	−870	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830	−1705	−1620			
V_{OHC}	Output HIGH Voltage	−1035			mV	V_{IN} = $V_{IH(Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610			
V_{IH}	Input HIGH Voltage	−1165		−870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1830		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	
I_{IH}	Input HIGH Current			240	μA	V_{IN} = $V_{IH\ (Max)}$	
I_{EE}	Power Supply Current	−65		−30	mA	Inputs Open	

Note 3: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DIP AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Data to Output	0.45	1.45	0.45	1.45	0.45	1.55	ns	*Figures 1* and *2* (Note 1)
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.35	1.20	0.35	1.20	0.35	1.20	ns	*Figures 1* and *2*

Note 1: The propagation delay specified is for single output switching. Delays may vary up to 200 ps with multiple outputs switching.

PCC and Cerpak AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Data to Output	0.45	1.25	0.45	1.25	0.45	1.35	ns	*Figures 1* and *2* (Note 2)
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.35	1.10	0.35	1.10	0.35	1.10	ns	*Figures 1* and *2*
t_{OSHL}	Maximum Skew Common Edge Output-to-Output Variation Data to Output Path		200		200		200	ps	PCC Only (Note 1)
t_{OSLH}	Maximum Skew Common Edge Output-to-Output Variation Data to Output Path		200		200		200	ps	PCC Only (Note 1)
t_{OST}	Maximum Skew Opposite Edge Output-to-Output Variation Data to Output Path		260		260		260	ps	PCC Only (Note 1)
t_{PS}	Maximum Skew Pin (Signal) Transition Variation Data to Output Path		200		200		200	ps	PCC Only (Note 1)

Note 1: Output-to-Output Skew is defined as the absolute value of the difference between the actual propagation delay for any outputs within the same packaged device. The specifications apply to any outputs switching in the same direction either HIGH to LOW (t_{OSHL}), or LOW to HIGH (t_{OSLH}), or in opposite directions both HL and LH (t_{OST}). Parameters t_{OST} and t_{PS} guaranteed by design.

Note 2: The propagation delay specified is for single output switching. Delays may vary up to 200 ps with multiple outputs switching.

Industrial Version

PCC DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = −40°C to +85°C (Note 3)

Symbol	Parameter	T_C = −40°C		T_C = 0°C to +85°C		Units	Conditions	
		Min	Max	Min	Max			
V_{OH}	Output HIGH Voltage	−1085	−870	−1025	−870	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830	−1575	−1830	−1620			
V_{OHC}	Output HIGH Voltage	−1095		−1035		mV	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage		−1565		−1610			
V_{IH}	Input HIGH Voltage	−1170	−870	−1165	−870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1830	−1480	−1830	−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50		0.50		μA	V_{IN} = $V_{IL\ (Min)}$	
I_{IH}	Input HIGH Current		300		240	μA	V_{IN} = $V_{IH\ (Max)}$	
I_{EE}	Power Supply Current	−65	−30	−65	−30	mA	Inputs Open	

Note 3: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

PCC AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = −40°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Data to Output	0.45	1.25	0.45	1.25	0.45	1.35	ns	*Figures 1* and *2* (Note 1)
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.30	1.20	0.35	1.10	0.35	1.10	ns	*Figures 1* and *2*

Note 1: The propagation delay specified is for single output switching. Delays may vary up to 200 ps with multiple outputs switching.

Military Version
DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C

Symbol	Parameter	Min	Max	Units	T_C	Conditions		Notes
V_{OH}	Output HIGH Voltage	−1025	−870	mV	0°C to +125°C	V_{IN} = V_{IH} (Max) or V_{IL} (Min)	Loading with 50Ω to −2.0V	1, 2, 3
		−1085	−870	mV	−55°C			
V_{OL}	Output LOW Voltage	−1830	−1620	mV	0°C to +125°C			
		−1830	−1555	mV	−55°C			
V_{OHC}	Output HIGH Voltage	−1035		mV	0°C to +125°C	V_{IN} = V_{IH} (Max) or V_{IL} (Min)	Loading with 50Ω to −2.0V	1, 2, 3
		−1085		mV	−55°C			
V_{OLC}	Output LOW Voltage		−1610	mV	0°C to +125°C			
			−1555	mV	−55°C			
V_{IH}	Input HIGH Voltage	−1165	−870	mV	−55°C to +125°C	Guaranteed HIGH Signal for All Inputs		1, 2, 3, 4
V_{IL}	Input HIGH Voltage	−1830	−1475	mV	−55°C to +125°C	Guaranteed LOW Signal for All Inputs		1, 2, 3, 4
I_{IL}	Input LOW Current	0.50		μA	−55°C to +125°	V_{EE} = −4.2V V_{IN} = V_{IL} (Min)		1, 2, 3
I_{IH}	Input HIGH Current		240	μA	0°C to +125°C	V_{EE} = −5.7V V_{IN} = V_{IH} (Max)		1, 2, 3
			340	μA	−55°C			
I_{EE}	Power Supply Current	−70	−25	mA	−55°C to +125°C	Inputs Open		1, 2, 3

Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals −55°C), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 2: Screen tested 100% on each device at −55°C, +25°C, and +125°C, Subgroups 1, 2, 3, 7, and 8.

Note 3: Sample tested (Method 5005, Table I) on each manufactured lot at −55°C, +25°C, and +125°C, Subgroups A1, 2, 3, 7, and 8.

Note 4: Guaranteed by applying specified input condition and testing V_{OH}/V_{OL}.

AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = −55°C		T_C = +25°C		T_C = +125°C		Units	Conditions	Notes
		Min	Max	Min	Max	Min	Max			
t_{PLH} t_{PHL}	Propagation Delay Data to Output	0.30	1.80	0.40	1.60	0.40	1.80	ns	*Figures 1* and *2*	1, 2, 3, 5
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.30	1.20	0.30	1.20	0.30	1.20	ns		4

Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals −55°C), then testing immediately after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 2: Screen tested 100% on each device at +25°C, only Subgroup A9.

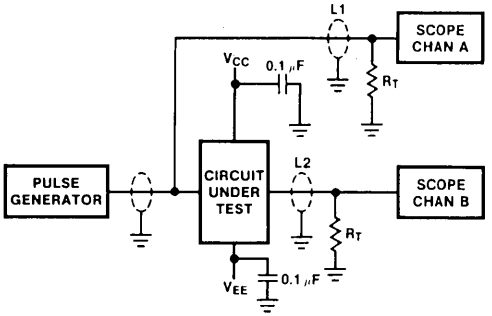
Note 3: Sample tested (Method 5005, Table I) on each manufactured lot at +25°C, Subgroup A9, and at +125°C and −55°C temperatures, Subgroups A10 and A11.

Note 4: Not tested at +25°C, +125°C, and −55°C temperature (design characterization data).

Note 5: The propagation delay specified is for single output switching. Delays may vary up to 200 ps with multiple outputs switching.

Test Circuit

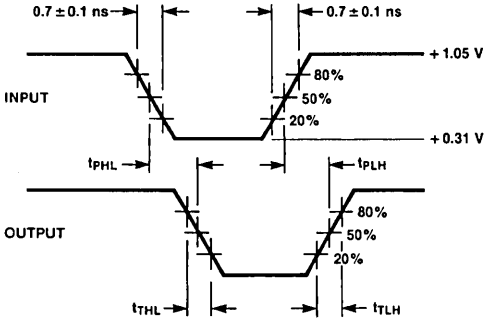
Notes:
V_{CC}, V_{CCA} = +2V, V_{EE} = −2.5V
L1 and L2 = equal length 50Ω impedance lines
R_T = 50Ω terminator internal to scope
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
All unused outputs are loaded with 50Ω to GND
C_L = Fixture and stray capacitance ≤ 3 pF



TL/F/10608–5

FIGURE 1. AC Test Circuit

Switching Waveforms



TL/F/10608–6

FIGURE 2. Propagation Delay and Transition Times

National Semiconductor

100323
Low Power Hex Bus Driver

General Description

The 100323 is a monolithic device containing six bus drivers capable of driving terminated lines with terminations as low as 25Ω. To reduce crosstalk, each output has its own respective ground connection. Transition times were designed to be longer than on other F100K devices. The driver itself performs the positive logic AND of a data input (D_1–D_6) and the OR of two select inputs (E and either DE_1, DE_2, or DE_3).

Enabling of data is possible in multiples of two, i.e., 2, 4 or all 6 paths. All inputs have 50 kΩ pull-down resistors.

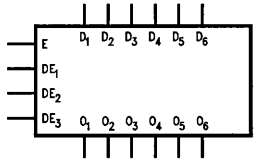
The output voltage LOW level is designed to be more negative than normal ECL outputs (cut off state). This allows an emitter-follower output transistor to turn off when the termination supply is −2.0V and thus present a high impedance to the data bus.

Features

- 50% power reduction of the 100123
- 2000V ESD protection
- −4.2V to −5.7V operating range
- Drives 25Ω load

Ordering Code: See Section 6

Logic Symbol

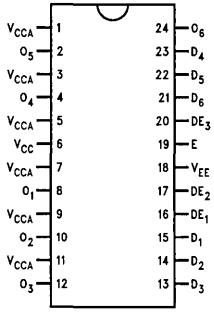


TL/F/9877–7

Pin Names	Description
D_1–D_6	Data Inputs
DE_1–DE_3	Dual Enable Inputs
E	Common Enable Input
O_1–O_6	Data Outputs

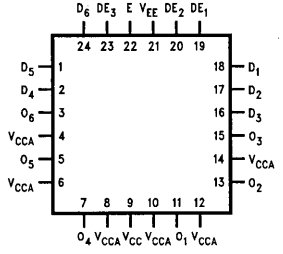
Connection Diagrams

24-Pin DIP



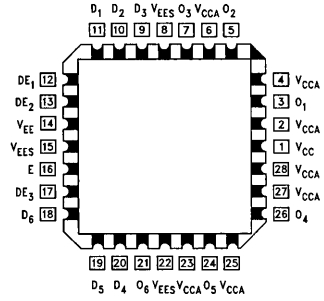
TL/F/9877–3

24-Pin Quad Cerpak



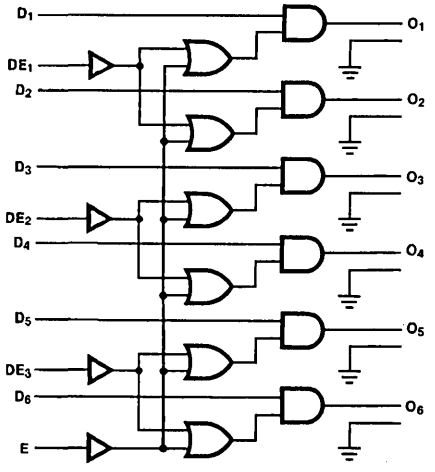
TL/F/9877–4

28-Pin PCC



TL/F/9877–2

Logic Diagram



TL/F/9877–1

Truth Table

E	DE_n	D_n	D_{n+1}	O_n	O_{n+1}
L	L	X	X	Cutoff	Cutoff
X	H	L	L	Cutoff	Cutoff
X	H	L	H	Cutoff	H
X	H	H	L	H	Cutoff
X	H	H	H	H	H
H	X	L	L	Cutoff	Cutoff
H	X	L	H	Cutoff	H
H	X	H	L	H	Cutoff
H	X	H	H	H	H

H = High
Cutoff = Lower-than-LOW state
L = Low
X = Don't Care

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Maximum Junction Temperature	
Ceramic	+175°C
Plastic	+150°C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Output Current (DC Output High)	−50 mA
ESD	≥2000V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: ESD testing conforms to MIL-STD-883, Method 3015.

Recommended Operating Conditions

Case Temperature	
Commercial	0°C to +85°C
Military	−55°C to +125°C
Supply Voltage (V_{EE})	−5.7V to −4.2V

Commercial Version

DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions	
V_{IH}	Input HIGH Voltage	−1165		−870	mV	Guaranteed High Signal for ALL Inputs	
V_{IL}	Input LOW Voltage	−1830		−1475	mV	Guaranteed Low Signal for ALL Inputs	
V_{OH}	Output HIGH Voltage	−1025	−955	−870	mV	V_{IN} = $V_{IH\ (max)}$ or $V_{IL\ (min)}$	Loading with 25Ω to −2.0V
V_{OHC}	Output HIGH Voltage	−1035			mV	V_{IN} = $V_{IH\ (min)}$ or $V_{IL\ (max)}$	Loading with 25Ω to −2.0V
V_{OLZ}	Cut-Off LOW Voltage			−1950	mV	V_{IN} = $V_{IH\ (min)}$ or $V_{IL\ (max)}$	Loading with 25Ω to −2.0V
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (min)}$	
I_{IH}	Input HIGH Current			240	μA	V_{IN} = $V_{IH\ (max)}$	
I_{EE}	Power Supply Current	−121	−91	−57	mA	Inputs Open	

Note 3: The specified limits represent "worst case" values for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DIP AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PZH} t_{PHZ}	Propagation Delay Data to Output	1.90 1.30	3.60 2.70	1.90 1.30	3.60 2.70	2.00 1.50	3.80 2.70	ns	*Figures 1* and *2*
t_{PZH} t_{PHZ}	Propagation Delay Dual Enable to Output	1.90 1.60	3.60 3.00	1.90 1.60	3.60 3.00	2.00 1.70	3.90 3.40	ns	
t_{PZH} t_{PHZ}	Propagation Delay Common Enable to Output	1.80 1.50	3.50 2.90	1.80 1.50	3.50 2.90	2.00 1.60	3.80 3.00	ns	
t_{TZH} t_{THZ}	Transition Time 20% to 80%, 80% to 20%	0.50 0.35	1.80 1.40	0.50 0.35	1.80 1.40	0.50 0.35	1.80 1.40	ns	

Commercial Version (Continued)

PCC and Cerpak AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PZH} t_{PHZ}	Propagation Delay Data to Output	1.90 1.30	3.40 2.50	1.90 1.30	3.40 2.50	2.00 1.50	3.60 2.70	ns	*Figures 1* and *2*
t_{PZH} t_{PHZ}	Propagation Delay Dual Enable to Output	1.90 1.60	3.40 2.80	1.90 1.60	3.40 2.80	2.00 1.70	3.70 3.00	ns	
t_{PZH} t_{PHZ}	Propagation Delay Common Enable to Output	1.80 1.50	3.30 2.70	1.80 1.50	3.30 2.70	2.00 1.60	3.60 2.80	ns	
t_{TZH} t_{THZ}	Transition Time 20% to 80%, 80% to 20%	0.50 0.35	1.70 1.30	0.50 0.35	1.70 1.20	0.50 0.35	1.70 1.30	ns	

Note: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

Military Version—Preliminary

DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = −55°C to +125°C

Symbol	Parameter	Min	Max	Units	T_C	Conditions		Notes
V_{OH}	Output HIGH Voltage	−1025	−870	mV	0°C to +125°C	V_{IN} = $V_{IH\ (max)}$ or $V_{IL\ (min)}$	Loading with 25Ω to −2.0V	1, 2, 3
		−1085	−870	mV	−55°C			
V_{OHC}	Output HIGH Voltage	−1035		mV	0°C to +125°C	V_{IN} = $V_{IH\ (min)}$ or $V_{IL\ (max)}$	Loading with 25Ω to −2.0V	1, 2, 3
		−1085		mV	−55°C			
V_{OLC}	Output LOW Voltage		−1610	mV	0°C to +125°C			
			−1555	MV	−55°C			
V_{OLZ}	Cut-Off LOW Voltage		−1950	mV	0°C to +125°C	V_{IN} = $V_{IH\ (min)}$ or $V_{IL\ (max)}$	Loading with 25Ω to −2.0V	1, 2, 3
			−1850		−55°C			
V_{IH}	Input HIGH Voltage	−1165	−870	mV	−55°C to +125°C	Guaranteed HIGH Signal for All Inputs		1, 2, 3, 4
V_{IL}	Input LOW Voltage	−1830	−1475	mV	−55°C to +125°C	Guaranteed LOW Signal for All Inputs		1, 2, 3, 4
I_{IL}	Input LOW Current	0.50		μA	−55°C to +125°C	V_{EE} = 4.2V, V_{IN} = $V_{IL\ (min)}$		1, 2, 3
I_{IH}	Input HIGH Current		240	μA	0°C to +125°C	V_{EE} = −5.7V, V_{IN} = $V_{IH\ (max)}$		1, 2, 3
			340	μA	−55°C			
I_{EE}	Power Supply Current	−145	−55	mA	−55°C to +125°C	Inputs Open V_{EE} = −4.2V to −4.8V		1, 2, 3
		−150				V_{EE} = −4.2V to −5.7V		

Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals −55°C), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 2: Screen tested 100% on each device at −55°C, +25°C, and +125°C, Subgroups 1, 2, 3, 7, and 8.

Note 3: Sample tested (Method 5005, Table I) on each manufactured lot at −55°C, +25°C, and +125°C, Subgroups A1, 2, 3, 7, and 8.

Note 4: Guaranteed by applying specified input condition and testing V_{OH}/V_{OL}.

Military Version—Preliminary (Continued)

AC Electrical Characteristics—All Packages

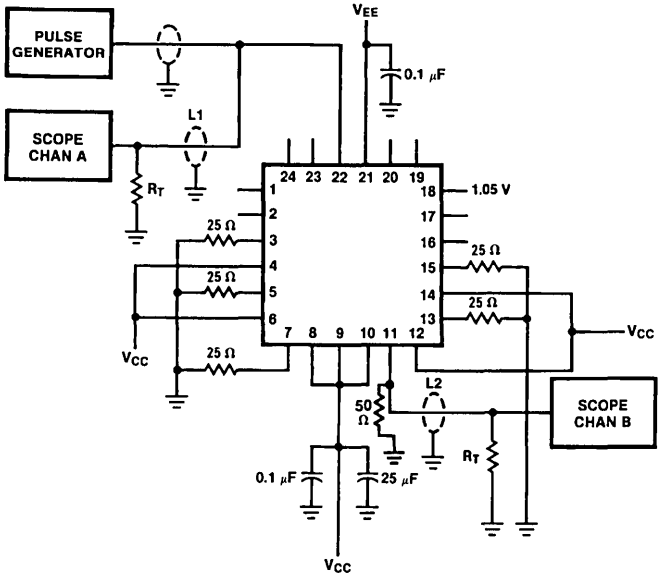
V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = −55°C		T_C = +25°C		T_C = +125°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PZH} t_{PHZ}	Propagation Delay Data to Output	1.70 1.10	4.00 3.10	1.70 1.10	4.00 3.10	1.80 1.30	4.20 3.10	ns	
t_{PZH} t_{PHZ}	Propagation Delay Data Enable to Output	1.70 1.40	4.00 3.40	1.70 1.40	4.00 3.40	1.80 1.50	4.30 3.80	ns	*Figures 1* and *2*
t_{PZH} t_{PHZ}	Propagation Delay Common Enable to Output	1.60 1.30	3.90 3.30	1.60 1.30	3.90 3.30	1.80 1.40	4.20 3.40	ns	
t_{TZH} t_{THZ}	Transition Time 20% to 80%, 80% to 20%	0.40 0.25	2.20 1.80	0.40 0.25	2.20 1.80	0.40 0.25	2.20 1.80	ns	

Note 1: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 2: Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

Test Circuitry



Notes:

V_{CC}, V_{CCA} = +2V, V_{EE} = −2.5V

L1 and L2 = equal length 50Ω impedance lines

R_T = 50Ω terminator internal to scope

Decoupling 0.1 μF from GND to V_{CC} and V_{EE}

All unused outputs are loaded with 25Ω to GND

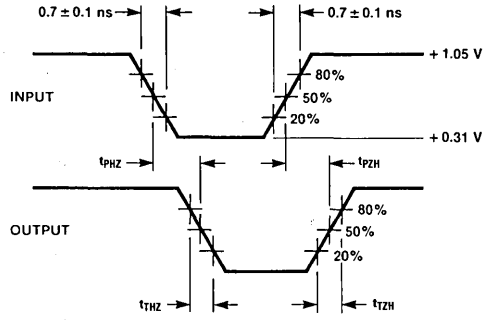
C_L = Fixture and stray capacitance ≤ 3 pF

Pin numbers shown are for flatpak; for DIP see logic symbol

TL/F/9877–5

FIGURE 1. AC Test Circuit

Timing Waveform



TL/F/9877–6

FIGURE 2. Propagation Delay and Transition Times

National Semiconductor

100324
Low Power Hex TTL-to-ECL Translator

General Description

The 100324 is a hex translator, designed to convert TTL logic levels to 100K ECL logic levels. The inputs are compatible with standard or Schottky TTL. A common Enable (E), when LOW, holds all inverting outputs HIGH and holds all true outputs LOW. The differential outputs allow each circuit to be used as an inverting/non-inverting translator, or as a differential line driver. The output levels are voltage compensated over the full −4.2V to −5.7V range.

When the circuit is used in the differential mode, the 100324, due to its high common mode rejection, overcomes voltage gradients between the TTL and ECL ground systems. The V_{EE} and V_{TTL} power may be applied in either order.

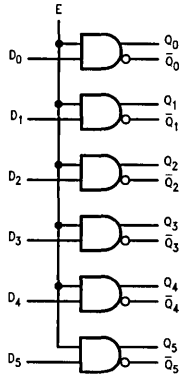
The 100324 is pin and function compatible with the 100124 with similar AC performance, but features power dissipation roughly half of the 100124 to ease system cooling requirements.

Features

- Pin/function compatible with 100124
- Meets 100124 AC specifications
- 50% power reduction of the 100124
- Differential outputs
- 2000V ESD protection
- −4.2V to −5.7V operating range
- Available to MIL-STD-883
- Available to industrial grade temperature range

Ordering Code: See Section 6

Logic Diagram

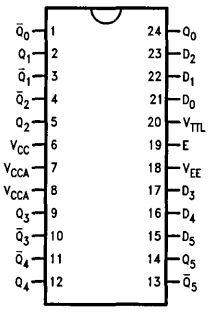


TL/F/9878–4

Pin Names	Description
D_0–D_5	Data Inputs
E	Enable Input
Q_0–Q_5	Data Outputs
$\overline{Q}_0$–$\overline{Q}_5$	Complementary Data Outputs

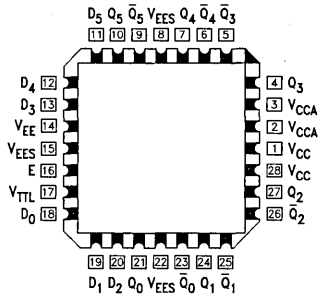
Connection Diagrams

24-Pin DIP/SOIC



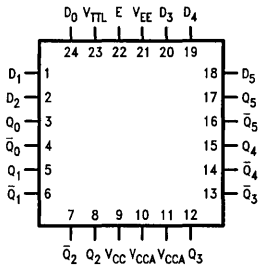
TL/F/9878–1

28-Pin PCC



TL/F/9878–3

24-Pin Quad Cerpak



TL/F/9878–2

Absolute Maximum Ratings

Above which the useful life may be impaired. (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature (T_{STG})	−65°C to +150°C
Maximum Junction Temperature (T_J)	
Ceramic	+175°C
Plastic	+150°C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
V_{TTL} Pin Potential to Ground Pin	−0.5V to +6.0V
Input Voltage (DC)	−0.5V to +6.0V
Output Current (DC Output HIGH)	−50 mA
ESD (Note 2)	≥2000V

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: ESD testing conforms to MIL-STD-883, Method 3015.

Recommended Operating Conditions

Case Temperature (T_C)	
Commercial	0°C to +85°C
Industrial	−40°C to +85°C
Military	−55°C to +125°C
Supply Voltage (V_{EE})	−5.7V to −4.2V

Commercial Version

DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3), V_{TTL} = +4.5V to +5.5V

Symbol	Parameter	Min	Typ	Max	Units	Conditions	
V_{OH}	Output HIGH Voltage	−1025	−955	−870	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830	−1705	−1620			
V_{OHC}	Output HIGH Voltage	−1035			mV	V_{IN} = $V_{IH(Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610			
V_{IH}	Input HIGH Voltage	2.0		5.0	V	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	0		0.8	V	Guaranteed LOW Signal for All Inputs	
V_{CD}	Input Clamp Diode Voltage	−1.2			V	I_{IN} = −18 mA	
I_{IH}	Input HIGH Current Data Enable			 20 120	μA	V_{IN} = +2.4V, All Other Inputs V_{IN} = GND	
	Input HIGH Current Breakdown Test, All Inputs			1.0	mA	V_{IN} = +5.5V, All Other Inputs = GND	
I_{IL}	Input LOW Current Data Enable	 −0.9 −5.4			mA	V_{IN} = +0.4V, All Other Inputs V_{IN} = V_{IH}	
I_{EE}	V_{EE} Power Supply Current	−70	−45	−22	mA	All Inputs V_{IN} = +4.0V	
I_{TTL}	V_{TTL} Power Supply Current		25	38	mA	All Inputs V_{IN} = GND	

Note 3: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

Commercial Version (Continued)

DIP AC Electric Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, V_{TTL} = +4.5V to +5.5V

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Data and Enable to Output	0.50	3.00	0.50	2.90	0.50	3.00	ns	*Figures 1* and *2*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.80	0.45	1.80	0.45	1.80	ns	

SOIC, PCC and Cerpak AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, V_{TTL} = +4.5V to +5.5V

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Data and Enable to Output	0.50	2.80	0.50	2.70	0.50	2.80	ns	*Figures 1* and *2*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.70	0.45	1.70	0.45	1.70	ns	
t_{OSHL}	Maximum Skew Common Edge Output-to-Output Variation Data to Output Path		0.95		0.95		0.95	ns	PCC Only (Note 1)
t_{OSLH}	Maximum Skew Common Edge Output-to-Output Variation Data to Output Path		0.70		0.70		0.70	ns	PCC Only (Note 1)
t_{OST}	Maximum Skew Opposite Edge Output-to-Output Variation Data to Output Path		1.60		1.60		1.60	ns	PCC Only (Note 1)
t_{PS}	Maximum Skew Pin (Signal) Transition Variation Data to Output Path		1.20		1.20		1.20	ns	PCC Only (Note 1)

Note 1: Output-to-Output Skew is defined as the absolute value of the difference between the actual propagation delay for any outputs within the same packaged device. The specifications apply to any outputs switching in the same direction either HIGH to LOW (t_{OSHL}), or LOW to HIGH (t_{OSLH}), or in opposite directions both HL and LH (t_{OST}). Parameters t_{OST} and t_{PS} guaranteed by design.

Industrial Version

PCC DC Electrical Characteristics (Note)

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = −40°C to +85°C, V_{TTL} = +4.5V to +5.5V

Symbol	Parameter	T_C = −40°C		T_C = 0°C to +85°C		Units	Conditions	
		Min	Max	Min	Max			
V_{OH}	Output HIGH Voltage	−1085	−870	−1025	−870	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830	−1575	−1830	−1620			
V_{OHC}	Output HIGH Voltage	−1095		−1035		mV	V_{IN} = $V_{IH(Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage		−1565		−1610			
V_{IH}	Input HIGH Voltage	2.0	5.0	2.0	5.0	V	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	0	0.8	0	0.8	V	Guaranteed LOW Signal for All Inputs	
V_{CD}	Input Clamp Diode Voltage	−1.2		−1.2		V	I_{IN} = −18 mA	
I_{IH}	Input HIGH Current Data Enable		20 120		20 120	μA	V_{IN} = +2.4V, All Other Inputs V_{IN} = GND	
	Input HIGH Current Breakdown Test, All Inputs		1.0		1.0	mA	V_{IN} = +5.5V, All Other Inputs = GND	
I_{IL}	Input LOW Current Data Enable	 −0.9 −5.4		 −0.9 −5.4		mA	V_{IN} = +0.4V, All Other Inputs V_{IN} = V_{IH}	
I_{EE}	V_{EE} Power Supply Current	−70	−22	−70	−22	mA	All Inputs V_{IN} = +4.0V	
I_{TTL}	V_{TTL} Power Supply Current		38		38	mA	All Inputs V_{IN} = GND	

Note: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

PCC AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, V_{TTL} = +4.5V to +5.5V

Symbol	Parameter	T_C = −40°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Data and Enable to Output	0.50	2.80	0.50	2.70	0.50	2.80	ns	*Figures 1* and *2*
t_{TLH} t_{THL}	Transition Times 20% to 80%, 80% to 20%	0.35	1.80	0.45	1.70	0.45	1.70	ns	*Figures 1* and *2*

Military Version

DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = −55°C to +125°C, V_{TTL} = +4.5V to +5.5V

Symbol	Parameter	Min	Max	Units	T_C	Conditions		Notes
V_{OH}	Output HIGH Voltage	−1025	−870	mV	0°C to +125°C	V_{IN} = V_{IH} (Max) or V_{IL} (Min)	Loading with 50Ω to −2.0V	1, 2, 3
		−1085	−870	mV	−55°C			
V_{OL}	Output LOW Voltage	−1830	−1620	mV	0°C to +125°C			
		−1830	−1555	mV	−55°C			
V_{OHC}	Output HIGH Voltage	−1035		mV	0°C to +125°C	V_{IN} = V_{IH} (Max) or V_{IL} (Min)	Loading with 50Ω to −2.0V	1, 2, 3
		−1085		mV	−55°C			
V_{OLC}	Output LOW Voltage		−1610	mV	0°C to +125°C			
			−1555	mV	−55°C			
V_{IH}	Input HIGH Voltage	2.0	5.0	V	−55°C to +125°C	Over V_{TTL}, V_{EE}, T_C Range		1, 2, 3, 4
V_{IL}	Input LOW Voltage	0.0	0.8	V	−55°C to +125°C	Over V_{TTL}, V_{EE}, T_C Range		1, 2, 3, 4
I_{IH}	Input HIGH Current Breakdown Test		20	μA	−55°C to +125°C	V_{IN} = +2.7V		1, 2, 3
			100	μA	−55°C to +125°C	V_{IN} = +7.0V		
I_{IL}	Input LOW Current Data Enable	 −0.9 −5.4		mA	−55°C to +125°C	V_{IN} = +0.4V		1, 2, 3
V_{FCD}	Input Clamp Diode Voltage		−1.2	V	−55°C to +125°C	I_{IN} = −18 mA		1, 2, 3
I_{EE}	V_{EE} Power Supply Current	−70	−22	mA	−55°C to +125°C	All Inputs V_{IN} = +4.0V		1, 2, 3
I_{TTL}	V_{TTL} Power Supply Current		38	mA	−55°C to +125°C	All Inputs V_{IN} = GND		1, 2, 3

Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals −55°C), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 2: Screen tested 100% on each device at −55°C, +25°C, and +125°C, Subgroups 1, 2, 3, 7, and 8.

Note 3: Sample tested (Method 5005, Table I) on each manufactured lot at −55°C, +25°C, and +125°C, Subgroups A1, 2, 3, 7, and 8.

Note 4: Guaranteed by applying specified input condition and testing V_{OH}/V_{OL}.

AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, V_{TTL} = +4.5V to +5.5V

Symbol	Parameter	T_C = −55°C		T_C = +25°C		T_C = +125°C		Units	Conditions	Notes
		Min	Max	Min	Max	Min	Max			
t_{PLH} t_{PHL}	Propagation Delay Data and Enable to Output	0.50	3.00	0.50	2.90	0.30	3.30	ns	*Figures 1* and *2*	1, 2, 3,
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.35	1.80	0.45	1.80	0.45	1.80	ns		4

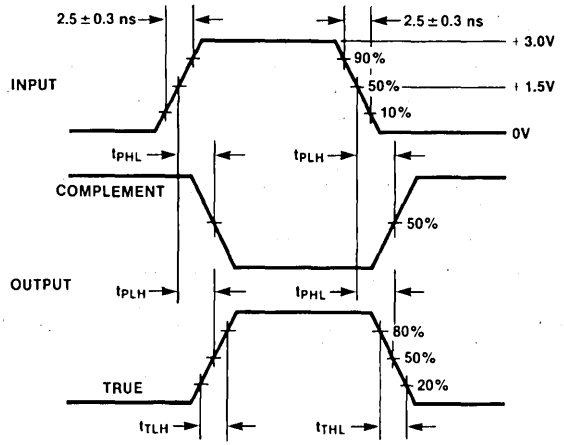
Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals −55°C), then testing immediately after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 2: Screen tested 100% on each device at +25°C temperature only, Subgroup A9.

Note 3: Sample tested (Method 5005, Table I) on each manufactured lot at +25°C, Subgroup A9, and at +125°C and −55°C temperatures, Subgroups A10 and A11.

Note 4: Not tested at +25°C, +125°C, and −55°C temperature (design characterization data).

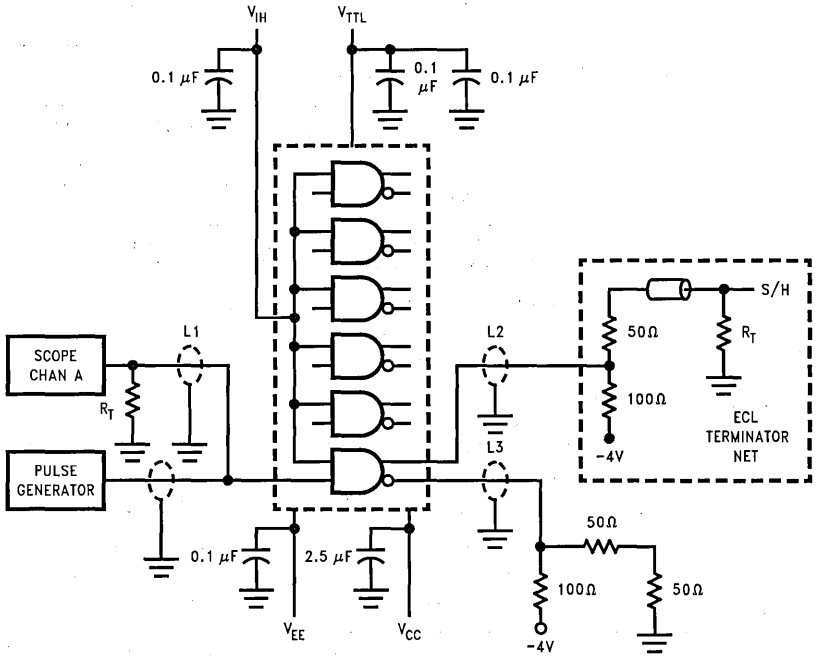
Switching Waveform



TL/F/9878–6

FIGURE 1. Propagation Delay and Transition Times

Test Circuit



TL/F/9878–5

FIGURE 2. AC Test Circuit

Notes:

V_{CC}, V_{CCA} = 0V, V_{EE} = −4.5V, V_{TTL} = +5.0V, V_{IH} = +3.0V

L1, L2 and L3 = equal length 50Ω impedance lines

R_T = 50Ω terminator internal to scope

Decoupling 0.1 μF from GND to V_{CC}, V_{EE} and V_{TTL}

All unused outputs are loaded with 50Ω to −2V or with equivalent ECL terminator network

C_L = Fixture and stray capacitance ≤ 3 pF

National Semiconductor

100325
Low Power Hex ECL-to-TTL Translator

General Description

The 100325 is a hex translator for converting F100K logic levels to TTL logic levels. Differential inputs allow each circuit to be used as an inverting, non-inverting or differential receiver. An internal reference voltage generator provides V_{BB} for single-ended operation, or for use in Schmitt trigger applications. All inputs have 50kΩ pull-down resistors. When the inputs are either unconnected or at the same potential the outputs will go low.

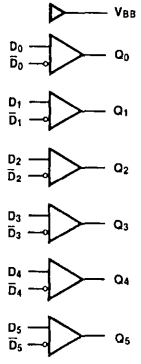
When used in single-ended operation the apparent input threshold of the true inputs is 20mV to 40mV higher (positive) than the threshold of the complementary inputs. The V_{EE} and V_{TTL} power may be applied in either order.

Features

- Pin/function compatible with 100125
- Meets 100125 AC specifications
- 50% power reduction of the 100125
- Differential inputs with built in offset
- Standard FAST® outputs
- 2000V ESD protection
- −4.2V to −5.7V operating range
- Available to industrial grade temperature range
- Available to MIL-STD-883

Ordering Code: See Section 6

Logic Diagram

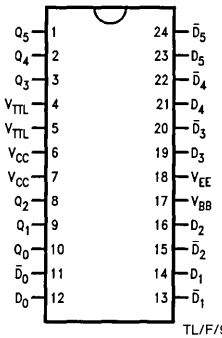


TL/F/9879-4

Pin Names	Description
D_0–D_5	Data Inputs
$\overline{D}_0$–$\overline{D}_5$	Inverting Data Inputs
Q_0–Q_5	Data Outputs

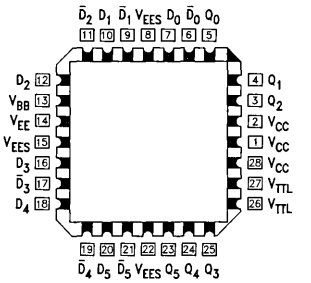
Connection Diagrams

24-Pin DIP/SOIC



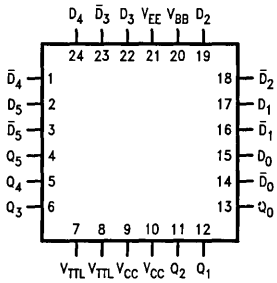
TL/F/9879-1

28-Pin PCC



TL/F/9879-3

24-Pin Quad Cerpak



TL/F/9879-2

Absolute Maximum Ratings

Above which the useful life may be impaired. (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature (T_{STG})	−65°C to +150°C
Maximum Junction Temperature (T_J)	
Ceramic	+175°C
Plastic	+150°C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
V_{TTL} Pin Potential to Ground Pin	−0.5V to +6.0V
Input Voltage (DC)	V_{EE} to +0.5V
Voltage Applied to Output in HIGH State (with V_{CC} = 0V)	−0.5V to V_{CC}
Current Applied to Output in LOW State (Max)	twice the rated I_{OL} (mA)
ESD (Note 2)	≥2000V

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: ESD testing conforms to MIL-STD-883, Method 3015.

Recommended Operating Conditions

Case Temperature (T_C)	
Commercial	0°C to +85°C
Industrial	−40°C to +85°C
Military	−55°C to +125°C
Supply Voltage (V_{EE})	−5.7V to −4.2V

Truth Table

Inputs		Outputs
D_n	$\overline{D}_n$	Q_n
L	H	L
H	L	H
L	L	L
H	H	L
Open	Open	L
V_{EE}	V_{EE}	L
L	V_{BB}	L
H	V_{BB}	H
V_{BB}	L	H
V_{BB}	H	L

H = HIGH Voltage Level
L = LOW Voltage Level

Commercial Version

DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = GND, V_{TTL} = +4.5V to 5.5V, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions	
V_{BB}	Output Reference Voltage	−1380	−1320	−1260	mV	I_{VBB} = −2.1 mA	
V_{IH}	Single-Ended Input HIGH Voltage	−1165		−870	mV	Guaranteed HIGH Signal for All Inputs (with One Input Tied to V_{BB})	
V_{IL}	Single-Ended Input LOW Voltage	−1830		−1475	mV	Guaranteed LOW Signal for All Inputs (with One Input Tied to V_{BB})	
V_{OH}	Output HIGH Voltage	2.5			V	I_{OH} = −2.0 mA	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$
V_{OL}	Output LOW Voltage			0.5	V	I_{OL} = 20 mA	
V_{DIFF}	Input Voltage Differential	150			mV	Required for Full Output Swing	
V_{CM}	Common Mode Voltage	V_{CC} − 2.0		V_{CC} − 0.5	V		

Commercial Version (Continued)

DC Electrical Characteristics (Continued)

V_{EE} = −4.2V to −5.7V, V_{CC} = GND, V_{TTL} = +4.5V to 5.5V, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
I_{IH}	Input HIGH Current			350	μA	$V_{IN} = V_{IH\,(Max)}$, D_0–$D_5 = V_{BB}$, $\overline{D_0}$–$\overline{D_5} = V_{IL\,(Min)}$
I_{IL}	Input LOW Current	0.5			μA	$V_{IN} = V_{IL\,(Min)}$, D_0–$D_5 = V_{BB}$
I_{OS}	Output Short-Circuit Current	−150		−60	mA	V_{OUT} = GND*
I_{EE}	V_{EE} Power Supply Current	−37	−27	−17	mA	D_0–$D_5 = V_{BB}$
I_{TTL}	V_{TTL} Power Supply Current		45	65	mA	D_0–$D_5 = V_{BB}$

*Test one output at a time.

Note 3: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DIP AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = GND, V_{TTL} = +4.5V to +5.5V

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Data to Output	0.80	3.50	0.90	3.70	1.00	4.00	ns	C_L = 15 pF *Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay Data to Output	1.60	4.30	1.70	4.50	1.80	4.80	ns	C_L = 50 pF *Figures 1* and *3*

SOIC, PCC and Cerpak AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = GND, V_{TTL} = +4.5V to +5.5V

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Data to Output	0.80	3.30	0.90	3.50	1.00	3.80	ns	C_L = 15 pF *Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay Data to Output	1.60	4.10	1.70	4.30	1.80	4.60	ns	C_L = 50 pF *Figures 1* and *3*
t_{OSHL}	Maximum Skew Common Edge Output-to-Output Variation Data to Output Path		0.65		0.65		0.65	ns	PCC Only (Note 1)
t_{OSLH}	Maximum Skew Common Edge Output-to-Output Variation Data to Output Path		0.65		0.65		0.65	ns	PCC Only (Note 1)
t_{OST}	Maximum Skew Opposite Edge Output-to-Output Variation Data to Output Path		2.20		2.20		2.20	ns	PCC Only (Note 1)
t_{PS}	Maximum Skew Pin (Signal) Transition Variation Data to Output Path		2.10		2.10		2.10	ns	PCC Only (Note 1)

Note 1: Output-to-Output Skew is defined as the absolute value of the difference between the actual propagation delay for any outputs within the same packaged device. The specifications apply to any outputs switching in the same direction either HIGH to LOW (t_{OSHL}), or LOW to HIGH (t_{OSLH}), or in opposite directions both HL and LH (t_{OST}). Parameters t_{OST} and t_{PS} guaranteed by design.

Industrial Version

PCC DC Electrical Characteristics (Note)

V_{EE} = −4.2V to −5.7V, V_{CC} = GND, T_C = −40°C to +85°C

Symbol	Parameter	T_C = −40°C		T_C = 0°C to +85°C		Units	Conditions	
		Min	Max	Min	Max			
V_{BB}	Output Reference Voltage	−1395	−1255	−1380	−1260	mV	I_{VBB} = −2.1 mA	
V_{IH}	Single-Ended Input HIGH Voltage	−1170	−870	−1165	−870	mV	Guaranteed HIGH Signal for All Inputs (with One Input Tied to V_{BB})	
V_{IL}	Single-Ended Input LOW Voltage	−1830	−1480	−1830	−1475	mV	Guaranteed LOW Signal for All Inputs (with One Input Tied to V_{BB})	
V_{OH}	Output HIGH Voltage	2.5		2.5		V	I_{OH} = −2.0 mA	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$
V_{OL}	Output LOW Voltage		0.5		0.5	V	I_{OL} = 20 mA	
V_{DIFF}	Input Voltage Differential	150		150		mV	Required for Full Output Swing	
V_{CM}	Common Mode Voltage	V_{CC} − 2.0	V_{CC} − 0.5	V_{CC} − 2.0	V_{CC} − 0.5	V		
I_{IH}	Input HIGH Current		450		350	μA	V_{IN} = $V_{IH\ (Max)}$, D_0–D_5 = V_{BB}, $\overline{D_0}$–$\overline{D_5}$ = $V_{IL\ (Min)}$	
I_{IL}	Input LOW Current	0.5		0.5		μA	V_{IN} = $V_{IL\ (Min)}$, D_0–D_5 = V_{BB}	
I_{OS}	Output Short-Circuit Current	−150	−60	−150	−60	mA	V_{OUT} = GND*	
I_{EE}	V_{EE} Power Supply Current	−37	−15	−37	−17	mA	D_0–D_5 = V_{BB}	
I_{TTL}	V_{TTL} Power Supply Current		65		65	mA	D_0–D_5 = V_{BB}	

*Test one output at a time.

Note: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

PCC AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = GND, V_{TTL} = +4.5V to +5.5V

Symbol	Parameter	T_C = −40°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Data to Output	0.80	3.30	0.90	3.50	1.00	3.80	ns	C_L = 15 pF *Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay Data to Output	1.60	4.10	1.70	4.30	1.80	4.60	ns	C_L = 50 pF *Figures 1* and *3*

Military Version

DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = −55°C to +125°C, C_L = 50 pF, V_{TTL} = +4.5V to +5.5V

Symbol	Parameter	Min	Max	Units	T_C	Conditions		Notes
V_{BB}	Output Reference Voltage	−1380	−1260	mV	0°C to +125°C	I_{VBB} = −3 μA, V_{EE} = −4.2V		1, 2, 3
						I_{VBB} = −2.1 mA	V_{EE} = −5.7V	
		−1396	−1260		−55°C	I_{VBB} = −3 mA		
V_{IH}	Input HIGH Voltage	−1165	−870	mV	−55°C to +125°C	Guaranteed HIGH Signal for All Inputs (with One Input Tied to V_{BB})		1, 2, 3, 4
V_{IL}	Input LOW Voltage	−1830	−1475	mV	−55°C to +125°C	Guaranteed LOW Signal for All Inputs (with One Input Tied to V_{BB})		1, 2, 3, 4
V_{OH}	Output HIGH Voltage	2.5		mV	0°C to +125°C	I_{OH} = −2.0 mA	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	1, 2, 3
		2.4			−55°C			
V_{OL}	Output LOW Voltage		0.5	mV	−55°C to +125°C	I_{OL} = 20 mA		
V_{DIFF}	Input Voltage Differential	150		mV	−55°C to +125°C	Required for Full Output Swing		1, 2, 3
V_{CM}	Common Mode Voltage	−2000	−500	mV	−55°C to +125°C			1, 2, 3, 4
I_{IH}	Input HIGH Current		350	μA	0°C to +125°C	V_{IN} = $V_{IH\ (Max)}$, D_0–D_5 = V_{BB}, $\overline{D}_0$–$\overline{D}_5$ = $V_{IL\ (Min)}$		1, 2, 3
			500		−55°C			
I_{IL}	Input LOW Current	0.50		μA	−55°C to +125°C	V_{IN} = $V_{IL\ (Min)}$, D_0–D_5 = V_{BB}		1, 2, 3
I_{OS}	Output Short Circuit Current	−150	−60	mA	−55°C to +125°C	V_{OUT} = GND Test One Output at a Time		1, 2, 3
I_{CEX}	Output HIGH Leakage Current		250	μA	−55°C to +125°C	V_{OUT} = 5.5V		1, 2, 3
I_{EE}	V_{EE} Power Supply Current	−35	−12	mA	−55°C to +125°C	D_0–D_5 = V_{BB}		1, 2, 3
I_{TTL}	V_{TTL} Power Supply Current		65	mA	−55°C to +125°C	D_0–D_5 = V_{BB}		1, 2, 3

Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals −55°C), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 2: Screen tested 100% on each device at −55°C, +25°C, and +125°C, Subgroups 1, 2, 3, 7, and 8.

Note 3: Sample tested (Method 5005, Table I) on each manufactured lot at −55°C, + 25°C, and +125°C, Subgroups A1, 2, 3, 7, and 8.

Note 4: Guaranteed by applying specified input condition and testing V_{OH}/V_{OL}.

AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = GND, V_{TTL} = +4.5V to +5.5V

Symbol	Parameter	T_C = −55°C		T_C = +25°C		T_C = +125°C		Units	Conditions	Notes
		Min	Max	Min	Max	Min	Max			
t_{PLH} t_{PHL}	Propagation Delay Data to Output	1.50	5.00	1.60	4.70	1.70	5.70	ns	C_L = 50 pF *Figures 1* and *3*	1, 2, 3

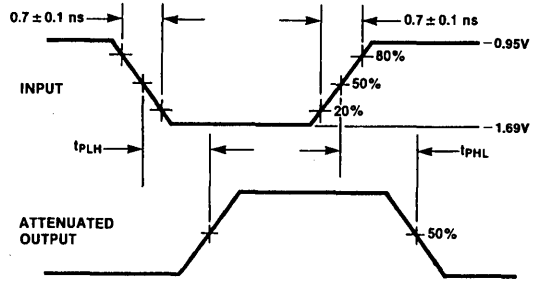
Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals −55°C), then testing immediately after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 2: Screen tested 100% on each device at +25°C, temperature only, Subgroup A9.

Note 3: Sample tested (Method 5005, Table I) on each manufactured lot at +25°C, Subgroup A9, and at +125°C and −55°C temperatures, Subgroups A10 and A11.

Note 4: Not tested at +25°C, +125°C, and −55°C temperature (design characterization data).

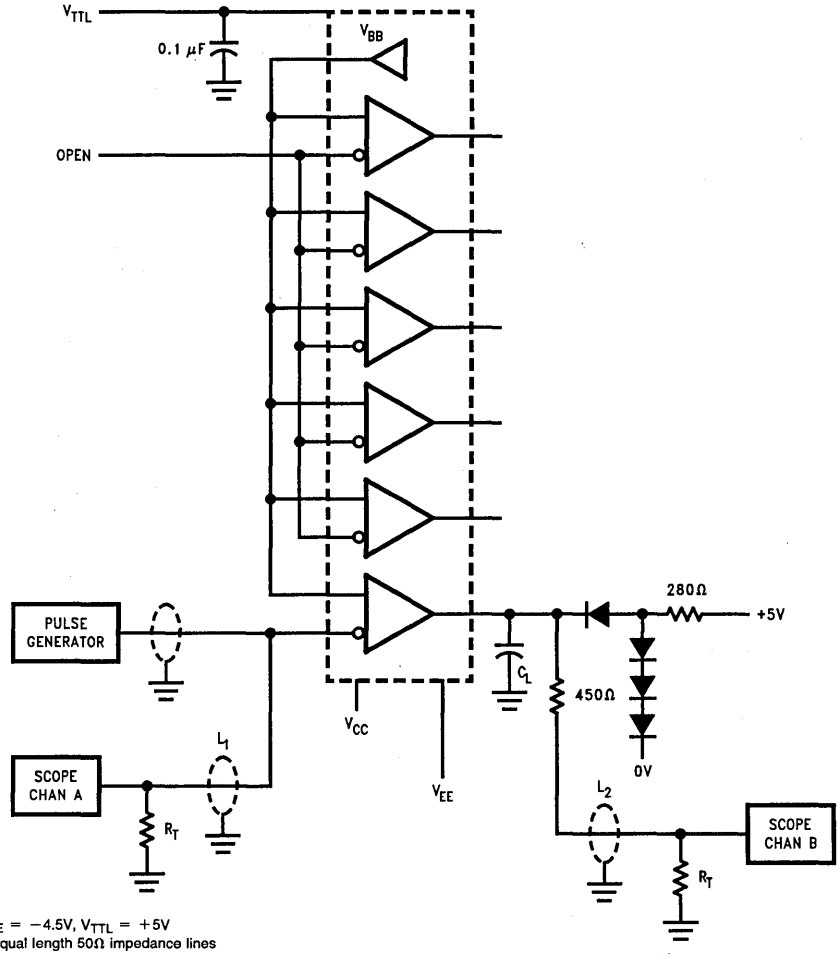
Switching Waveform



TL/F/9879-6

FIGURE 1. Propagation Delay

Test Circuits

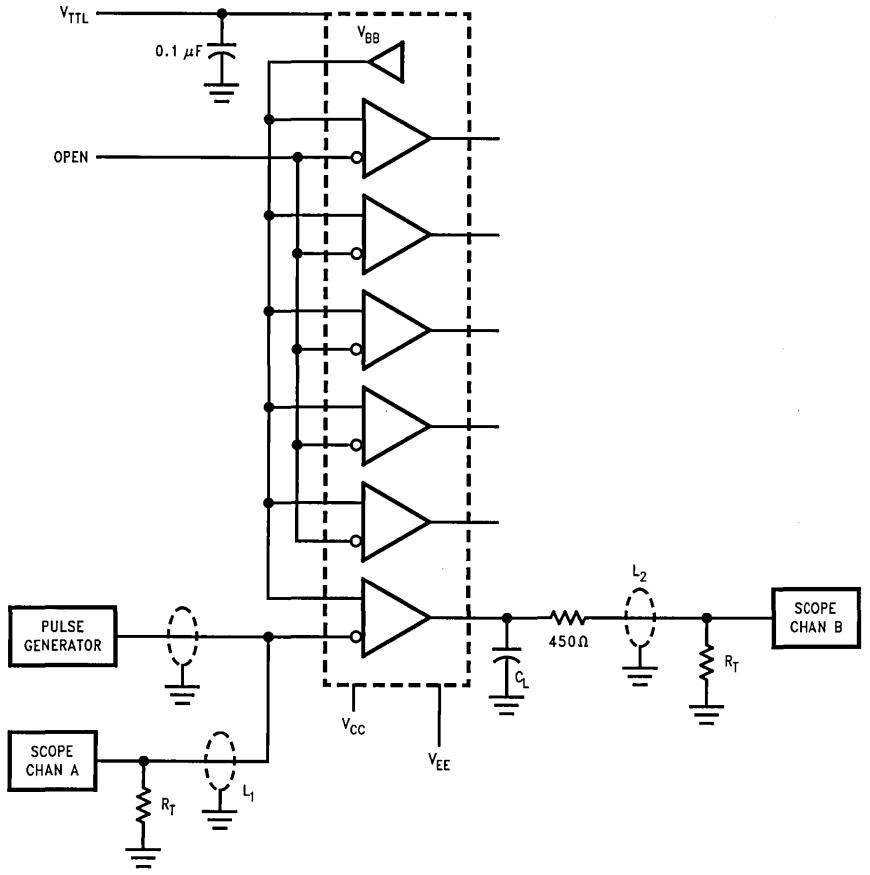


TL/F/9879-5

Notes:
V_{CC} = 0V, V_{EE} = −4.5V, V_{TTL} = +5V
L1 and L2 = equal length 50Ω impedance lines
R_T = 50Ω terminator internal to scope
Decoupling 0.1 μF from GND to V_{CC}, V_{EE} and V_{TTL}
All unused outputs are loaded with 500Ω to GND
C_L = Fixture and stray capacitance = 15 pF

FIGURE 2. AC Test Circuit for 15 pF Loading

Test Circuits (Continued)



TL/F/9879-8

Notes:
V_{CC} = 0V, V_{EE} = −4.5V, V_{TTL} = +5V
L1 and L2 = equal length 50Ω impedance lines
R_T = 50Ω terminator internal to scope
Decoupling 0.1 μF from GND to V_{CC}, V_{EE} and V_{TTL}
All unused outputs are loaded with 500Ω to GND
C_L = Fixture and stray capacitance = 50 pF

FIGURE 3. AC Test Circuit for 50 pF Loading

National Semiconductor

100328
Low Power Octal ECL/TTL Bi-Directional Translator with Latch

General Description

The 100328 is an octal latched bi-directional translator designed to convert TTL logic levels to 100K ECL logic levels and vice versa. The direction of this translation is determined by the DIR input. A LOW on the output enable input (OE) holds the ECL outputs in a cut-off state and the TTL outputs at a high impedance level. A HIGH on the latch enable input (LE) latches the data at both inputs even though only one output is enabled at the time. A LOW on LE makes the 100328 transparent.

The cut-off state is designed to be more negative than a normal ECL LOW level. This allows the output emitter-followers to turn off when the termination supply is −2.0V, presenting a high impedance to the data bus. This high impedance reduces termination power and prevents loss of low state noise margin when several loads share the bus.

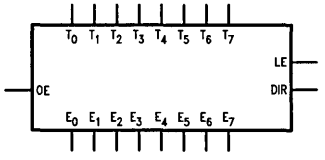
The 100328 is designed with FAST® TTL output buffers, featuring optimal DC drive and capable of quickly charging and discharging highly capacitive loads. All inputs have 50 kΩ pull-down resistors.

Features

- Identical performance to the 100128 at 50% of the supply current
- Bi-directional translation
- 2000V ESD protection
- Latched outputs
- FAST® TTL outputs
- TRI-STATE® outputs
- Voltage compensated operating range = −4.2V to −5.7V
- Available to industrial grade temperature range
- Available to MIL-STD-883

Ordering Code: See Section 6

Logic Symbol



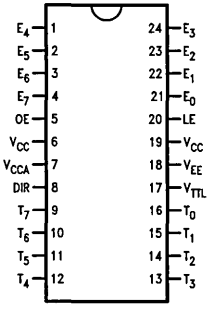
TL/F/10219–1

Pin Names	Description
E_0–E_7	ECL Data I/O
T_0–T_7	TTL Data I/O
OE	Output Enable Input
LE	Latch Enable Input
DIR	Direction Control Input

All pins function at 100K ECL levels except for T_0–T_7.

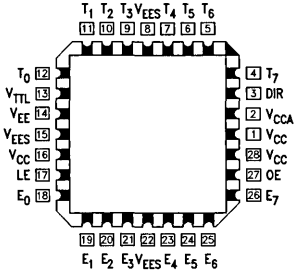
Connection Diagrams

24-Pin DIP/SOIC



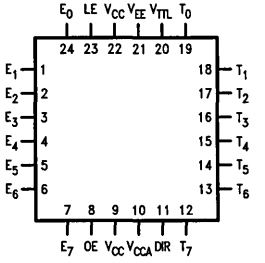
TL/F/10219–2

28-Pin PCC



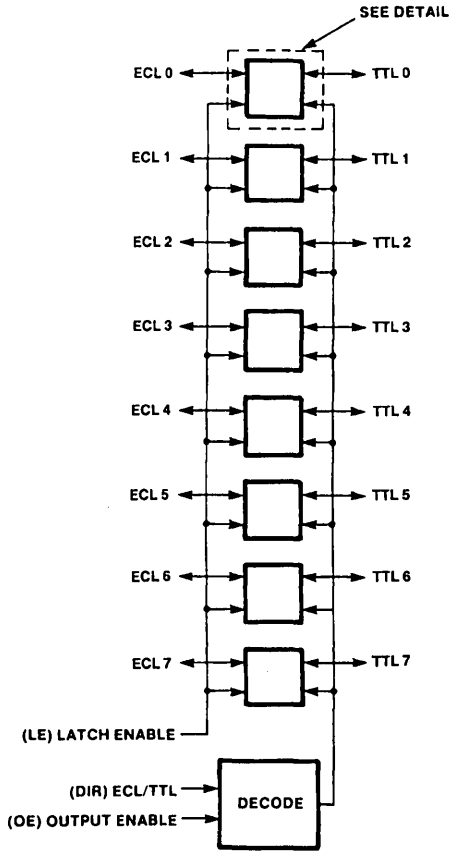
TL/F/10219–3

24-Pin Quad Cerpak



TL/F/10219–4

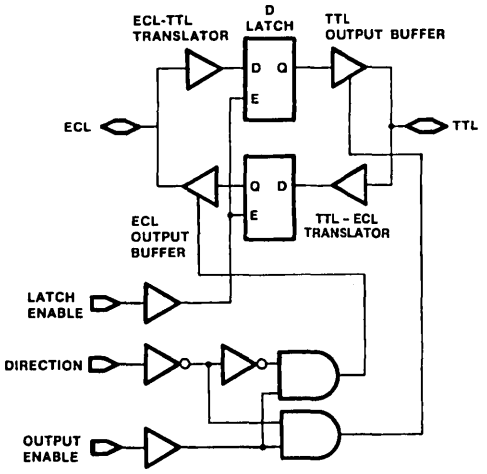
Functional Diagram



TL/F/10219–5

Note: LE, DIR, and OE use ECL logic levels

Detail



TL/F/10219–6

Truth Table

OE	DIR	LE	ECL Port	TTL Port	Notes
L	X	L	LOW (Cut-Off)	Z	
L	L	H	Input	Z	1, 3
L	H	H	LOW (Cut-Off)	Input	2, 3
H	L	L	L	L	1, 4
H	L	L	H	H	1, 4
H	L	H	X	Latched	1, 3
H	H	L	L	L	2, 4
H	H	L	H	H	2, 4
H	H	H	Latched	X	2, 3

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High Impedance

Note 1: ECL input to TTL output mode.

Note 2: TTL input to ECL output mode.

Note 3: Retains data present before LE set HIGH.

Note 4: Latch is transparent.

2

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature (T_{STG})	−65°C to +150°C
Maximum Junction Temperature (T_J)	
Ceramic	+175°C
Plastic	+150°C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
V_{TTL} Pin Potential to Ground Pin	−0.5V to +6.0V
ECL Input Voltage (DC)	V_{EE} to +0.5V
ECL Output Current (DC Output HIGH)	−50 mA
TTL Input Voltage (Note 3)	−0.5V to +6.0V
TTL Input Current (Note 3)	−30 mA to +5.0 mA
Voltage Applied to Output in HIGH State TRI-STATE Output	−0.5V to +5.5V
Current Applied to TTL Output in LOW State (Max)	Twice the Rated I_{OL} (mA)
ESD (Note 2)	≥2000V

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: ESD testing conforms to MIL-STD-883, Method 3015.

Note 3: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Case Temperature (T_C)	
Commercial	0°C to +85°C
Industrial	−40°C to +85°C
Military	−55°C to +125°C
ECL Supply Voltage (V_{EE})	−5.7V to −4.2V
TTL Supply Voltage (V_{TTL})	+4.5V to +5.5V

Commercial Version

TTL-to-ECL DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C, V_{TTL} = +4.5V to +5.5V (Note 4)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{OH}	Output HIGH Voltage	−1025	−955	−870	mV	V_{IN} = $V_{IH(Max)}$ or $V_{IL(Min)}$ Loading with 50Ω to − 2V
V_{OL}	Output LOW Voltage	−1830	−1705	−1620	mV	
	Cutoff Voltage		−2000	−1950	mV	OE or DIR Low, V_{IN} = $V_{IH(Max)}$ or $V_{IL(Min)}$, Loading with 50Ω to −2V
V_{OHC}	Output HIGH Voltage Corner Point High	−1035			mV	V_{IN} = $V_{IH(Min)}$ or $V_{IL(Max)}$ Loading with 50Ω to −2V
V_{OLC}	Output LOW Voltage Corner Point Low			−1610	mV	
V_{IH}	Input HIGH Voltage	2.0		5.0	V	Over V_{TTL}, V_{EE}, T_C Range
V_{IL}	Input LOW Voltage	0		0.8	V	Over V_{TTL}, V_{EE}, T_C Range
I_{IH}	Input HIGH Current			70	μA	V_{IN} = +2.7V
	Breakdown Test			1.0	mA	V_{IN} = +5.5V
I_{IL}	Input LOW Current	−700			μA	V_{IN} = +0.5V
V_{FCD}	Input Clamp Diode Voltage	−1.2			V	I_{IN} = −18 mA
I_{EE}	V_{EE} Supply Current	−159 −169		−75 −75	mA	LE Low, OE and DIR High Inputs Open V_{EE} = −4.2V to −4.8V V_{EE} = −4.2V to −5.7V

Note 4: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

Commercial Version (Continued)

ECL-to-TTL DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C, C_L = 50 pF, V_{TTL} = +4.5V to +5.5V (Note)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{OH}	Output HIGH Voltage	2.7 2.4	3.1 2.9		V V	I_{OH} = −3 mA, V_{TTL} = 4.75V I_{OH} = −3 mA, V_{TTL} = 4.50V
V_{OL}	Output LOW Voltage		0.3	0.5	V	I_{OL} = 24 mA, V_{TTL} = 4.50V
V_{IH}	Input HIGH Voltage	−1165		−870	mV	Guaranteed HIGH Signal for All Inputs
V_{IL}	Input LOW Voltage	−1830		−1475	mV	Guaranteed LOW Signal for All Inputs
I_{IH}	Input HIGH Current			350	μA	V_{IN} = V_{IH} (Max)
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = V_{IL} (Min)
I_{OZHT}	TRI-STATE Current Output High			70	μA	V_{OUT} = +2.7V
I_{OZLT}	TRI-STATE Current Output Low	−700			μA	V_{OUT} = +0.5V
I_{OS}	Output Short-Circuit Current	−150		−60	mA	V_{OUT} = 0.0V, V_{TTL} = +5.5V
I_{TTL}	V_{TTL} Supply Current			74 49 67	mA mA mA	TTL Outputs LOW TTL Outputs HIGH TTL Outputs in TRI-STATE

DIP TTL-to-ECL AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{TTL} = +4.5V to +5.5V, V_{CC} = V_{CCA} = GND (Note)

Symbol	Parameter	T_C = 0°C		T_C = 25°C		T_C = 85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	T_N to E_n (Transparent)	1.1	3.5	1.1	3.6	1.1	3.8	ns ns	*Figures 1 & 2*
t_{PLH} t_{PHL}	LE to E_n	1.7	3.6	1.7	3.7	1.9	3.9	ns ns	*Figures 1 & 2*
t_{PZH}	OE to E_n (Cutoff to High)	1.3	4.2	1.5	4.4	1.7	4.8	ns	*Figures 1 & 2*
t_{PHZ}	OE to E_n (High to Cutoff)	1.5	4.5	1.6	4.5	1.6	4.6	ns	*Figures 1 & 2*
t_{PHZ}	DIR to E_n (High to Cutoff)	1.6	4.3	1.6	4.3	1.7	4.5	ns	*Figures 1 & 2*
t_{set}	T_n to LE	1.1		1.1		1.1		ns	*Figures 1 & 2*
t_{hold}	T_n to LE	1.1		1.1		1.1		ns	*Figures 1 & 2*
t_{pw}(H)	Pulse Width LE	2.1		2.1		2.1		ns	*Figures 1 & 2*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.6	1.6	0.6	1.6	0.6	1.6	ns	*Figures 1 & 2*

Note: The specified limits represent the "worst" case value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

Commercial Version (Continued)

DIP ECL-to-TTL AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{TTL} = +4.5V to +5.5V, V_{CC} = V_{CCA} = GND, C_L = 50 pF

Symbol	Parameter	T_C = 0°C		T_C = 25°C		T_C = 85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	E_n to T_n (Transparent)	2.3	5.6	2.4	5.6	2.6	5.9	ns	*Figures 3 & 4*
t_{PLH} t_{PHL}	LE to T_n	3.1	7.2	3.1	7.2	3.3	7.7	ns	*Figures 3 & 4*
t_{PZH} t_{PZL}	OE to T_n (Enable Time)	3.4 3.8	8.45 9.2	3.7 4.0	8.95 9.2	4.0 4.3	9.7 9.95	ns	*Figures 3 & 5*
t_{PHZ} t_{PLZ}	OE to T_n (Disable Time)	3.2 3.0	8.95 7.7	3.3 3.4	8.95 8.7	3.5 4.1	9.2 9.95	ns	*Figures 3 & 5*
t_{PHZ} t_{PLZ}	DIR to T_n (Disable Time)	2.7 2.8	8.2 7.45	2.8 3.1	8.7 7.95	3.1 4.0	8.95 9.2	ns	*Figures 3 & 6*
t_{set}	E_n to LE	1.1		1.1		1.1		ns	*Figures 3 & 4*
t_{hold}	E_n to LE	2.1		2.1		2.6		ns	*Figures 3 & 4*
t_{pw}(H)	Pulse Width LE	4.1		4.1		4.1		ns	*Figures 3 & 4*

SOIC, PCC and Cerpak TTL-to-ECL AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{TTL} = +4.5V to +5.5V

Symbol	Parameter	T_C = 0°C		T_C = 25°C		T_C = 85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	T_n to E_n (Transparent)	1.1	3.3	1.1	3.4	1.1	3.6	ns ns	*Figures 1 & 2*
t_{PLH} t_{PHL}	LE to E_n	1.7	3.4	1.7	3.5	1.9	3.7	ns ns	*Figures 1 & 2*
t_{PZH}	OE to E_n (Cutoff to High)	1.3	4.0	1.5	4.2	1.7	4.6	ns	*Figures 1 & 2*
t_{PHZ}	OE to E_n (High to Cutoff)	1.5	4.3	1.6	4.3	1.6	4.4	ns	*Figures 1 & 2*
t_{PHZ}	DIR to E_n (High to Cutoff)	1.6	4.1	1.6	4.1	1.7	4.3	ns	*Figures 1 & 2*
t_{set}	T_n to LE	1.0		1.0		1.0		ns	*Figures 1 & 2*
t_{hold}	T_n to LE	1.0		1.0		1.0		ns	*Figures 1 & 2*
t_{pw}(H)	Pulse Width LE	2.0		2.0		2.0		ns	*Figures 1 & 2*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.6	1.6	0.6	1.6	0.6	1.6	ns	*Figures 1 & 2*
t_{OSHL}	Maximum Skew Common Edge Output-to-Output Variation Data to Output Path		200		200		200	ps	PCC Only (Note 1)
t_{OSLH}	Maximum Skew Common Edge Output-to-Output Variation Data to Output Path		200		200		200	ps	PCC Only (Note 1)
t_{OST}	Maximum Skew Opposite Edge Output-to-Output Variation Data to Output Path		650		650		650	ps	PCC Only (Note 1)
t_{ps}	Maximum Skew Pin (Signal) Transition Variation Data to Output Path		650		650		650	ps	PCC Only (Note 1)

Note 1: Output-to-Output Skew is defined as the absolute value of the difference between the actual propagation delay for any outputs within the same packaged device. The specifications apply to any outputs switching in the same direction either HIGH to LOW (t_{OSHL}), or LOW to HIGH (t_{OSLH}), or in opposite directions both HL and LH (t_{OST}). Parameters t_{OST} and t_{ps} guaranteed by design.

Commercial Version (Continued)

SOIC, PCC and Cerpak ECL-to-TTL AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{TTL} = +4.5V to +5.5V, C_L = 50 pF

Symbol	Parameter	T_C = 0°C		T_C = 25°C		T_C = 85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	E_n to T_n (Transparent)	2.3	5.4	2.4	5.4	2.6	5.7	ns	*Figures 3 & 4*
t_{PLH} t_{PHL}	LE to T_n	3.1	7.0	3.1	7.0	3.3	7.5	ns	*Figures 3 & 4*
t_{PZH} t_{PZL}	OE to T_n (Enable Time)	3.4 3.8	8.25 9.0	3.7 4.0	8.75 9.0	4.0 4.3	9.5 9.75	ns	*Figures 3 & 5*
t_{PHZ} t_{PLZ}	OE to T_n (Disable Time)	3.2 3.0	8.75 7.5	3.3 3.4	8.75 8.5	3.5 4.1	9.0 9.75	ns	*Figures 3 & 5*
t_{PHZ} t_{PLZ}	DIR to T_n (Disable Time)	2.7 2.8	8.0 7.25	2.8 3.1	8.5 7.75	3.1 4.0	8.75 9.0	ns	*Figures 3 & 6*
t_{set}	E_n to LE	1.0		1.0		1.0		ns	*Figures 3 & 4*
t_{hold}	E_n to LE	2.0		2.0		2.5		ns	*Figures 3 & 4*
t_{pw}(H)	Pulse Width LE	4.0		4.0		4.0		ns	*Figures 3 & 4*
t_{OSHL}	Maximum Skew Common Edge Output-to-Output Variation Data to Output Path		600		600		600	ps	PCC Only (Note 1)
t_{OSLH}	Maximum Skew Common Edge Output-to-Output Variation Data to Output Path		850		850		850	ps	PCC Only (Note 1)
t_{OST}	Maximum Skew Opposite Edge Output-to-Output Variation Data to Output Path		1350		1350		1350	ps	PCC Only (Note 1)
t_{ps}	Maximum Skew Pin (Signal) Transition Variation Data to Output Path		950		950		950	ps	PCC Only (Note 1)

Note 1: Output-to-Output Skew is defined as the absolute value of the difference between the actual propagation delay for any outputs within the same packaged device. The specifications apply to any outputs switching in the same direction either HIGH to LOW (t_{OSHL}), or LOW to HIGH (t_{OSLH}), or in opposite directions both HL and LH (t_{OST}). Parameters t_{OST} and t_{ps} guaranteed by design.

Industrial Version

PCC TTL-to-ECL DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = −40°C to +85°C, V_{TTL} = +4.5V to +5.5V (Note)

Symbol	Parameter	T_C = −40°C		T_C = 0°C to +85°C		Units	Conditions
		Min	Max	Min	Max		
V_{OH}	Output HIGH Voltage	−1085	−870	−1025	−870	mV	V_{IN} = $V_{IH(Max)}$ or $V_{IL(Min)}$ Loading with 50Ω to −2V
V_{OL}	Output LOW Voltage	−1830	−1575	−1830	−1620	mV	
	Cutoff Voltage		−1900		−1950	mV	OE or DIR Low, V_{IN} = $V_{IH(Max)}$ or $V_{IL(Min)}$, Loading with 50Ω to −2V
V_{OHC}	Output HIGH Voltage Corner Point High	−1095		−1035		mV	V_{IN} = $V_{IH(Min)}$ or $V_{IL(Max)}$ Loading with 50Ω to −2V
V_{OLC}	Output LOW Voltage Corner Point Low		−1565		−1610	mV	
V_{IH}	Input HIGH Voltage	2.0	5.0	2.0	5.0	V	Over V_{TTL}, V_{EE}, T_C Range
V_{IL}	Input LOW Voltage	0	0.8	0	0.8	V	Over V_{TTL}, V_{EE}, T_C Range
I_{IH}	Input HIGH Current		70		70	μA	V_{IN} = +2.7V
	Breakdown Test		1.0		1.0	mA	V_{IN} = +5.5V
I_{IL}	Input LOW Current	−700		−700		μA	V_{IN} = +0.5V
V_{FCD}	Input Clamp Diode Voltage	−1.2		−1.2		V	I_{IN} = −18 mA
I_{EE}	V_{EE} Supply Current						LE Low, OE and DIR High Inputs Open
		−159	−70	−159	−75	mA	V_{EE} = −4.2V to −4.8V
		−169	−70	−169	−75		V_{EE} = −4.2V to −5.7V

PCC ECL-to-TTL DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = −40°C to +85°C, C_L = 50 pF, V_{TTL} = +4.5V to +5.5V (Note)

Symbol	Parameter	T_C = −40°C		T_C = 0°C to +85°C		Units	Conditions
		Min	Max	Min	Max		
V_{OH}	Output HIGH Voltage	2.7		2.7		V	I_{OH} = −3 mA, V_{TTL} = 4.75V
		2.4		2.4		V	I_{OH} = −3 mA, V_{TTL} = 4.50V
V_{OL}	Output LOW Voltage		0.5		0.5	V	I_{OL} = 24 mA, V_{TTL} = 4.50V
V_{IH}	Input HIGH Voltage	−1170	−870	−1165	−870	mV	Guaranteed HIGH Signal for All Inputs
V_{IL}	Input LOW Voltage	−1830	−1480	−1830	−1475	mV	Guaranteed LOW Signal for All Inputs
I_{IH}	Input HIGH Current		425		350	μA	V_{IN} = V_{IH} (Max)
I_{IH}	Input LOW Current	0.50		0.50		μA	V_{IN} = V_{IH} (Min)
I_{OZHT}	TRI-STATE Current Output High		70		70	μA	V_{OUT} = +2.7V
I_{OZLT}	TRI-STATE Current Output Low	−700		−700		μA	V_{OUT} = +0.5V
I_{OS}	Output Short-Circuit Current	−150	−60	−150	−60	mA	V_{OUT} = 0.0V, V_{TTL} = +5.5V
I_{TTL}	V_{TTL} Supply Current		74		74	mA	TTL Outputs LOW
			49		49	mA	TTL Outputs HIGH
			67		67	mA	TTL Outputs in TRI-STATE

Note: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

Industrial Version (Continued)

PCC TTL-to-ECL AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{TTL} = +4.5V to +5.5V

Symbol	Parameter	T_C = −40°C		T_C = 25°C		T_C = 85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	T_n to E_n (Transparent)	1.0	3.3	1.1	3.4	1.1	3.6	ns ns	*Figures 1 & 2*
t_{PLH} t_{PHL}	LE to E_n	1.7	3.4	1.7	3.5	1.9	3.7	ns ns	*Figures 1 & 2*
t_{PZH}	OE to E_n (Cutoff to High)	1.2	4.0	1.5	4.2	1.7	4.6	ns	*Figures 1 & 2*
t_{PHZ}	OE to E_n (High to Cutoff)	1.5	4.5	1.6	4.3	1.6	4.4	ns	*Figures 1 & 2*
t_{PHZ}	DIR to E_n (High to Cutoff)	1.6	4.1	1.6	4.1	1.7	4.3	ns	*Figures 1 & 2*
t_{set}	T_n to LE	2.5		1.0		1.0		ns	*Figures 1 & 2*
t_{hold}	T_n to LE	1.0		1.0		1.0		ns	*Figures 1 & 2*
$t_{pw}(H)$	Pulse Width LE	2.5		2.0		2.0		ns	*Figures 1 & 2*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.4	2.3	0.6	1.6	0.6	1.6	ns	*Figures 1 & 2*

PCC ECL-to-TTL AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{TTL} = +4.5V to +5.5V, C_L = 50 pF

Symbol	Parameter	T_C = 0°C		T_C = 25°C		T_C = 85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	E_n to T_n (Transparent)	2.3	5.4	2.4	5.4	2.6	5.7	ns	*Figures 3 & 4*
t_{PLH} t_{PHL}	LE to T_n	3.1	7.4	3.1	7.0	3.3	7.5	ns	*Figures 3 & 4*
t_{PZH} t_{PZL}	OE to T_n (Enable Time)	3.4 3.7	8.3 9.0	3.7 4.0	8.75 9.0	4.0 4.3	9.5 9.75	ns	*Figures 3 & 5*
t_{PHZ} t_{PLZ}	OE to T_n (Disable Time)	3.2 3.0	9.0 7.5	3.3 3.4	8.75 8.5	3.5 4.1	9.0 9.75	ns	*Figures 3 & 5*
t_{PHZ} t_{PLZ}	DIR to T_n (Disable Time)	2.7 2.8	8.0 7.3	2.8 3.1	8.5 7.75	3.1 4.0	8.75 9.0	ns	*Figures 3 & 6*
t_{set}	E_n to LE	2.5		1.0		1.0		ns	*Figures 3 & 4*
t_{hold}	E_n to LE	2.3		2.0		2.5		ns	*Figures 3 & 4*
$t_{pw}(H)$	Pulse Width LE	4.0		4.0		4.0		ns	*Figures 3 & 4*

Military Version

TTL-to-ECL DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = −55°C to +125°C, V_{TTL} = +4.5V to +5.5V

Symbol	Parameter	Min	Max	Units	T_C	Conditions		Notes
V_{OH}	Output HIGH Voltage	−1025	−870	mV	0°C to +125°C	V_{IN} = V_{IH} (Max) or V_{IL} (Min)	Loading with 50Ω to −2.0V	1, 2, 3
		−1085	−870	mV	−55°C			
V_{OL}	Output LOW Voltage	−1830	−1620	mV	0°C to +125°C			
		−1830	−1555	mV	−55°C			
	Cutoff Voltage		−1950	mV	0°C to +125°C	OE or DIR Low		
			−1850	mV	−55°C			
V_{OHC}	Output HIGH Voltage	−1035		mV	0°C to +125°C	V_{IN} = V_{IH} (Min) or V_{IL} (Max)	Loading with 50Ω0 to −2.0V	1, 2, 3
		−1085		mV	−55°C			
V_{OLC}	Output LOW Voltage		−1610	mV	0°C to +125°C			
			−1555	mV	−55°C			
V_{IH}	Input HIGH Voltage	2.0		V	−55°C to +125°C	Over V_{TTL}, V_{EE}, T_C Range		1, 2, 3, 4
V_{IL}	Input LOW Voltage		0.8	V	−55°C to +125°C	Over V_{TTL}, V_{EE}, T_C Range		1, 2, 3, 4
I_{IH}	Input HIGH Current		70	μA	−55°C to 125°C	V_{IN} = +2.7V		1, 2, 3
	Breakdown Test		1.0	mA	−55°C to +125°C	V_{IN} = +5.5V		
I_{IL}	Input LOW Current	−1.0		mA	−55°C to +125°C	V_{IN} = +0.5V		1, 2, 3
V_{FCD}	Input Clamp Diode Voltage	−1.2		V	−55°C to +125° C	I_{IN} = −18 mA		1, 2, 3
I_{EE}	V_{EE} Supply Current	−165 −175	−65 −65	mA	−55°C to +125°C	LE Low, OE and DIR High Inputs Open V_{EE} = −4.2V to −4.8V V_{EE} = −4.2V to −5.7V		1, 2, 3

Military Version (Continued)

ECL-to-TTL DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = −55°C to +125°C, C_L = 50 pF, V_{TTL} = +4.5V to + 5.5V

Symbol	Parameter	Min	Max	Units	T_C	Conditions	Notes
V_{OH}	Output HIGH Voltage	2.5 2.4		mV	0°C to +125°C −55°C	I_{OH} = −1 mA, V_{TTL} = 4.50V I_{OH} = −3 mA, V_{TTL} = 4.50V	1, 2, 3
V_{OL}	Output LOW Voltage		0.5	mV	−55°C +125°C	I_{OL} = 24 mA, V_{TTL} = 4.50V	
V_{IH}	Input HIGH Voltage	−1165	−870	mV	−55°C +125°C	Guaranteed HIGH Signal for All Inputs	1, 2, 3, 4
V_{IL}	Input LOW Voltage	−1830	−1475	mV	−55°C to +125°C	Guaranteed LOW Signal for All Inputs	1, 2, 3, 4
I_{IH}	Input HIGH Current		350 500	μA	0°C to +125°C	V_{EE} = −5.7V V_{IN} = V_{IH} (Max)	1, 2, 3
I_{IL}	Input LOW Current	0.50		μA	−55°C to +125°C	V_{EE} = −4.2V V_{IN} = V_{IL} (Min)	1, 2, 3
I_{OZHT}	TRI-STATE Current Output High		70	μA	−55°C to +125°C	V_{OUT} = +2.7V	1, 2, 3
I_{OZLT}	TRI-STATE Current Output Low	−1.0		mA	−55°C to +125°C	V_{OUT} = +0.5V	1, 2, 3
I_{OS}	Output Short-Circuit CURRENT	−150	−60	mA	−55°C to +125°C	V_{OUT} = 0.0V, V_{TTL} = +5.5V	1, 2, 3
I_{TTL}	V_{TTL} Supply Current		75 50 70	mA mA mA	−55°C to +125°C	TTL Outputs Low TTL Output High TTL Output in TRI-STATE	1, 2, 3

Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals −55°C), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 2: Screen tested 100% on each device at −55°C, +25°C, and +125°C, Subgroups, 1, 2 3, 7, and 8.

Note 3: Sample tested (Method 5005, Table I) on each manufactured lot at −55°C, +25°C, and +125°C, Subgroups A1, 2, 3, 7, and 8.

Note 4: Guaranteed by applying specified input condition and testing V_{OH}/V_{OL}.

TTL-to-ECL AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{TTL} = +4.5V to +5.5V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = −55°C		T_C = 25°C		T_C = +125°C		Units	Conditions	Notes
		Min	Max	Min	Max	Min	Max			
t_{PLH} t_{PHL}	T_N to E_n (Transparent)	0.8	3.4	1.1	3.6	0.8	3.7	ns ns	*Figures 1 & 2*	1, 2, 3
t_{PLH} t_{PHL}	LE to E_n	1.2	3.8	1.4	3.7	1.1	3.8	ns ns	*Figures 1 & 2*	
t_{PZH}	OE to E_n (Cutoff to HIGH)	0.8	3.6	1.5	4.0	2.0	5.2	ns	*Figures 1 & 2*	
t_{PHZ}	OE to E_n (HIGH to Cutoff)	1.5	4.6	1.6	4.2	1.6	4.3	ns	*Figures 1 & 2*	
t_{PHZ}	DIR to E_n (HIGH to Cutoff)	1.6	4.7	1.6	4.3	1.7	4.3	ns	*Figures 1 & 2*	1, 2, 3
t_{set}	T_n to LE	2.5		2.0		2.5		ns	*Figures 1 & 2*	4
t_{hold}	T_n to LE	2.5		2.0		2.5		ns	*Figures 1 & 2*	
t_{pw}(H)	Pulse Width LE	2.5		2.0		2.5		ns	*Figures 1 & 2*	4
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.4	2.3	0.5	2.1	0.4	2.4	ns	*Figures 1 & 2*	4

Military Version (Continued)

ECL-to-TTL AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{TTL} = +4.5V to +5.5V, V_{CC} = V_{CCA} = GND, C_L = 50 pF

Symbol	Parameter	T_C = −55°C		T_C = 25°C		T_C = +125°C		Units	Conditions	Notes
		Min	Max	Min	Max	Min	Max			
t_{PLH} t_{PHL}	E_n to T_n (Transparent)	2.1	6.0	2.0	5.6	2.2	6.3	ns	*Figures 3 & 4*	1, 2, 3
t_{PLH} t_{PHL}	LE to T_n	3.1	7.0	3.1	6.5	3.3	7.5	ns	*Figures 3 & 4*	
t_{PZH} t_{PZL}	OE to T_n (Enable Time)	3.2 3.6	8.0 8.0	3.7 4.0	8.0 8.5	4.0 4.3	9.2 9.6	ns	*Figures 3 & 5*	1, 2, 3
t_{PHZ} t_{PLZ}	OE to T_n (Disable Time)	3.2 3.0	8.5 8.0	3.3 3.4	8.0 7.5	3.5 4.1	8.4 10.0	ns	*Figures 3 & 5*	
t_{PHZ} t_{PLZ}	DIR to T_n (Disable Time)	2.6 2.7	7.0 7.0	2.6 3.1	7.0 7.0	2.9 4.0	8.0 10.0	ns	*Figures 3 & 6*	
t_{set}	E_n to LE	2.5		2.0		2.5		ns	*Figures 3 & 4*	4
t_{hold}	E_n to LE	3.0		2.5		3.0		ns	*Figures 3 & 4*	
t_{pw}(H)	Pulse Width LE	2.5		2.0		5.0		ns	*Figures 3 & 4*	4

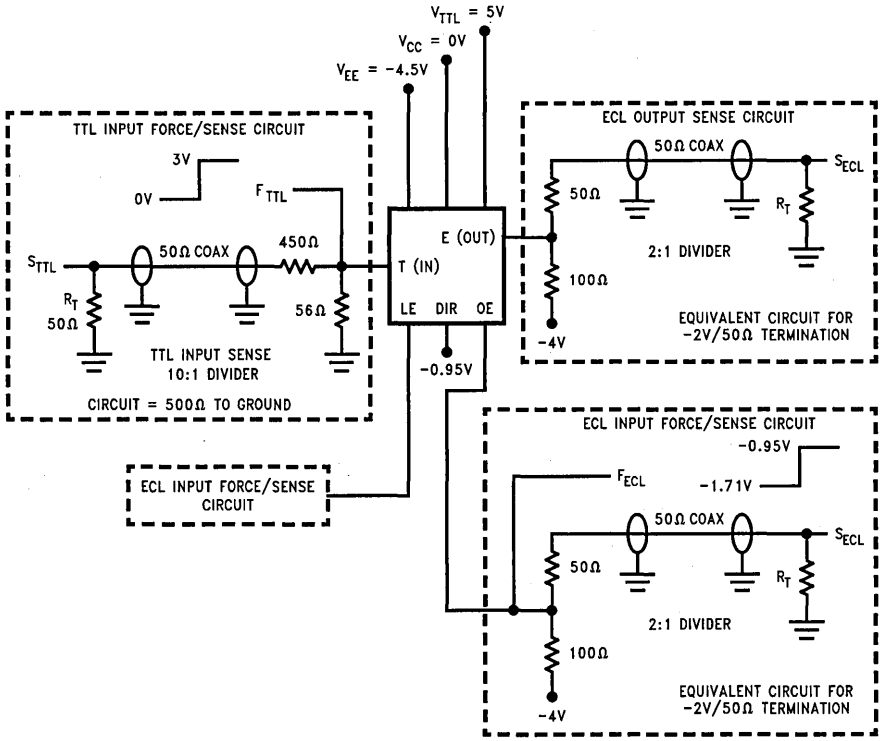
Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals −55°C), then testing immediately after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 2: Screen tested 100% on each device at +25°C, temperature only, Subgroup A9.

Note 3: Sample tested (Method 5005, Table I) on each mfg. lot at +25°C, Subgroup A9, and at +125°C and −55°C temperatures, Subgroups A10 and A11.

Note 4: Not tested at +25°C, +125°C and −55°C temperature (design characterization data).

Test Circuitry (TTL-to-ECL)



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Note 1: $R_t = 50\Omega$ termination. When an input or output is being monitored by a scope, R_t is supplied by the scope's 50Ω resistance. When an input or output is not being monitored, an external 50Ω resistance must be applied to serve as R_t.

Note 2: TTL and ECL force signals are brought to the DUT via 50Ω coax lines.

Note 3: V_{TTL} is decoupled to ground with 0.1 μF to ground, V_{EE} is decoupled to ground with 0.01 μF and V_{CC} is connected to ground.

Note 4: For ECL input pins, the equivelent force/sense circuitry is optional.

FIGURE 1. TTL-to-ECL AC Test Circuit

Switching Waveforms (TTL-to-ECL)

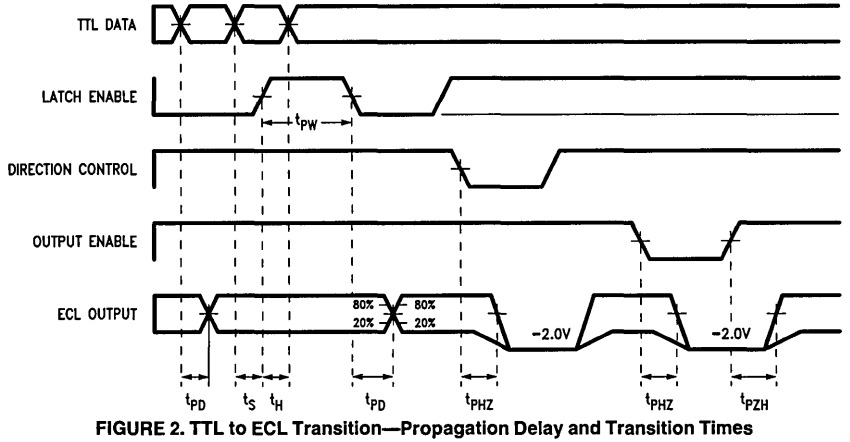

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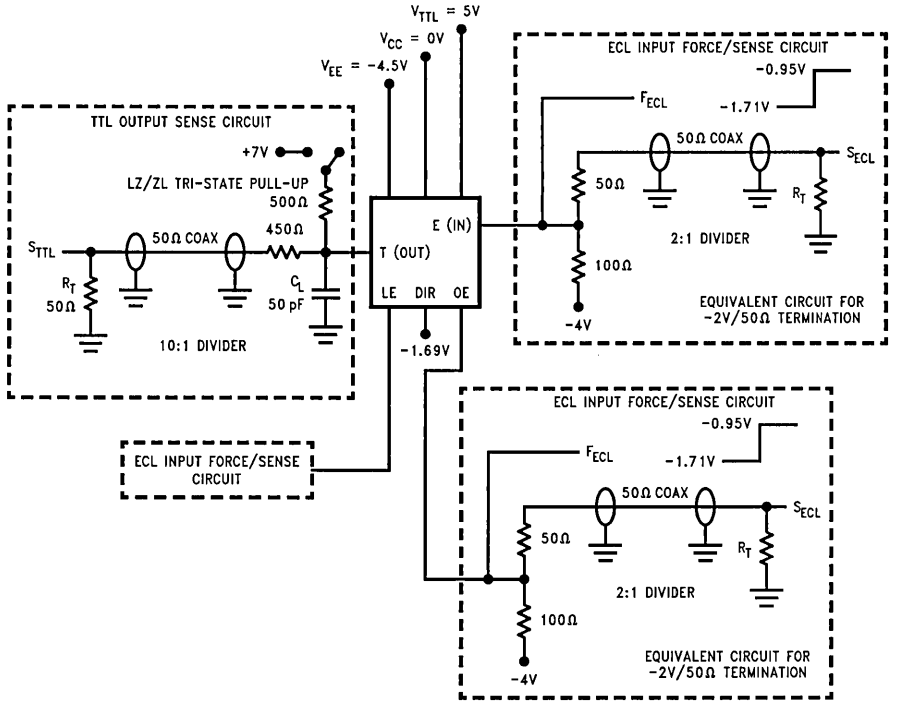
FIGURE 2. TTL to ECL Transition—Propagation Delay and Transition Times

Test Circuitry (ECL-to-TTL)



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Note 1: R_t = 50Ω termination. When an input or output is being monitored by a scope, R_t is supplied by the scope's 50Ω resistance. When an input or output is not being monitored, an external 50Ω resistance must be applied to serve as R_t.

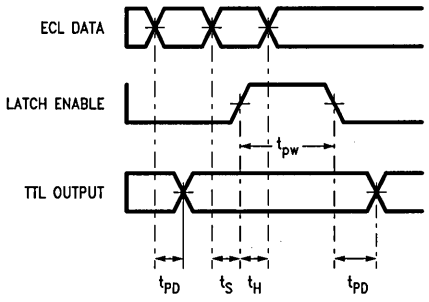
Note 2: The TTL Tri-State pull up switch is connected to +7V only for ZL and LZ tests.

Note 3: TTL and ECL force signals are brought to the DUT via 50Ω coax lines.

Note 4: V_{TTL} is decoupled to ground with 0.1 μF, V_{EE} is decoupled to ground with 0.01 μF and V_{CC} is connected to ground.

FIGURE 3. ECL-to-TTL AC Test Circuit

Switching Waveforms (ECL-to-TTL)



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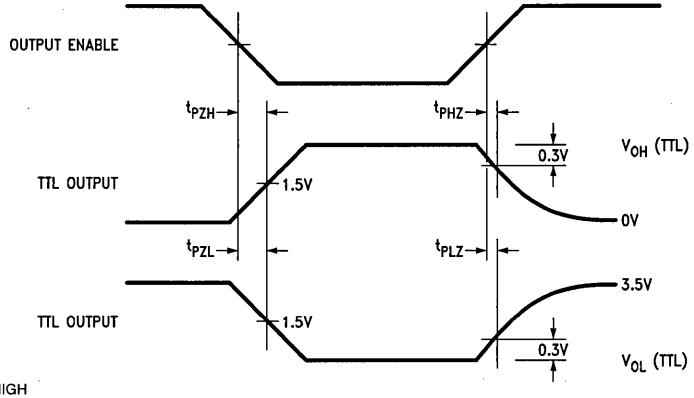
Note: DIR is LOW, and OE is HIGH

FIGURE 4. ECL-to-TTL Transition—Propagation Delay and Transition Times



Note: DIR is LOW, LE is HIGH

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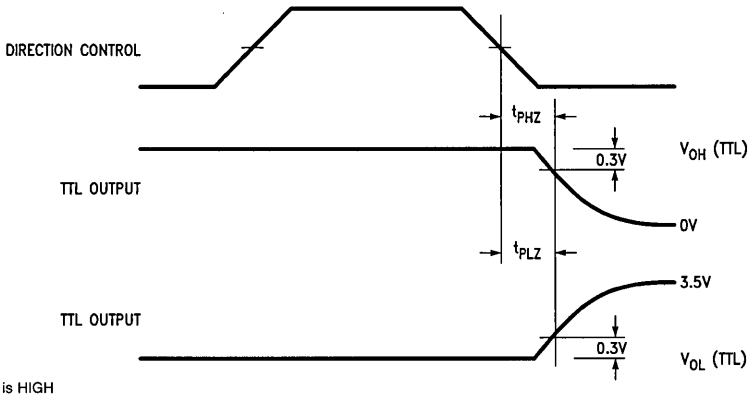
FIGURE 5. ECL-to-TTL Transition, OE to TTL Output, Enable and Disable Times



Note: OE is HIGH, LE is HIGH

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FIGURE 6. ECL-to-TTL Transition, DIR to TTL Output, Disable Time

Applications

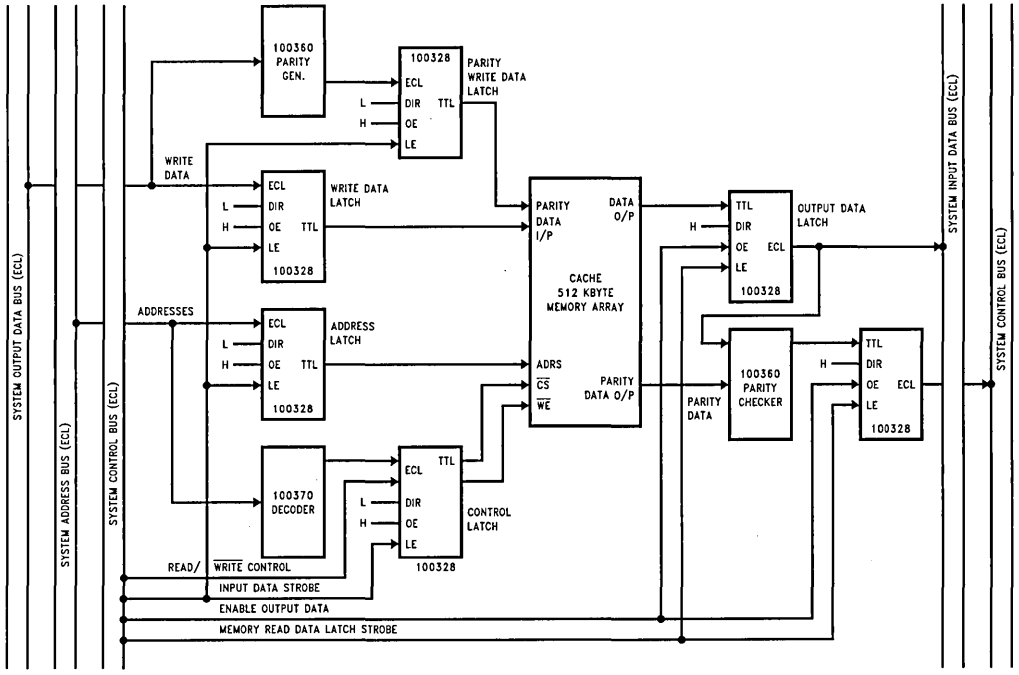

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FIGURE 7. Applications Diagram—MOS/TTL SRAM Interface Using 100328 ECL–TTL Latched Translator

National Semiconductor

100329
Low Power Octal ECL/TTL Bidirectional Translator with Register

General Description

The 100329 is an octal registered bidirectional translator designed to convert TTL logic levels to 100K ECL logic levels and vice versa. The direction of the translation is determined by the DIR input. A LOW on the output enable input (OE) holds the ECL outputs in a cut-off state and the TTL outputs at a high impedance level. The outputs change synchronously with the rising edge of the clock input (CP) even though only one output is enabled at the time.

The cut-off state is designed to be more negative than a normal ECL LOW level. This allows the output emitter-followers to turn off when the termination supply is −2.0V, presenting a high impedance to the data bus. This high impedance reduces the termination power and prevents loss of low state noise margin when several loads share the bus.

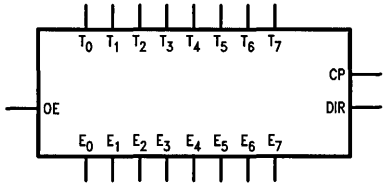
The 100329 is designed with FAST® TTL output buffers, featuring optimal DC drive and capable of quickly charging and discharging highly capacitive loads. All inputs have 50 kΩ pull-down resistors.

Features

- Bidirectional translation
- ECL high impedance outputs
- Registered outputs
- FAST TTL outputs
- TRI-STATE® outputs
- Voltage compensated operating range = −4.2V to −5.7V
- Available to MIL-STD-883

Ordering Code: See Section 6

Logic Symbol



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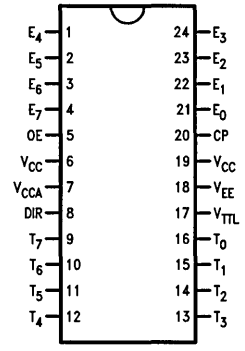
Pin Names	Description
E_0–E_7	ECL Data I/O
T_0–T_7	TTL Data I/O
OE	Output Enable Input
CP	Clock Pulse Input (Active Rising Edge)
DIR	Direction Control Input

All pins function at 100K ECL levels except for T_0–T_7.

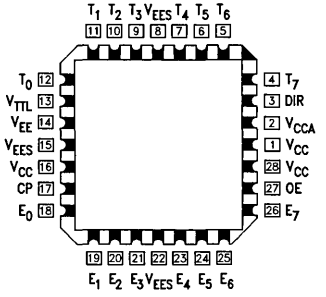
Connection Diagrams

24-Pin DIP



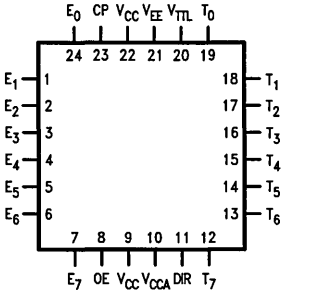
TL/F/10583–2

28-Pin PCC



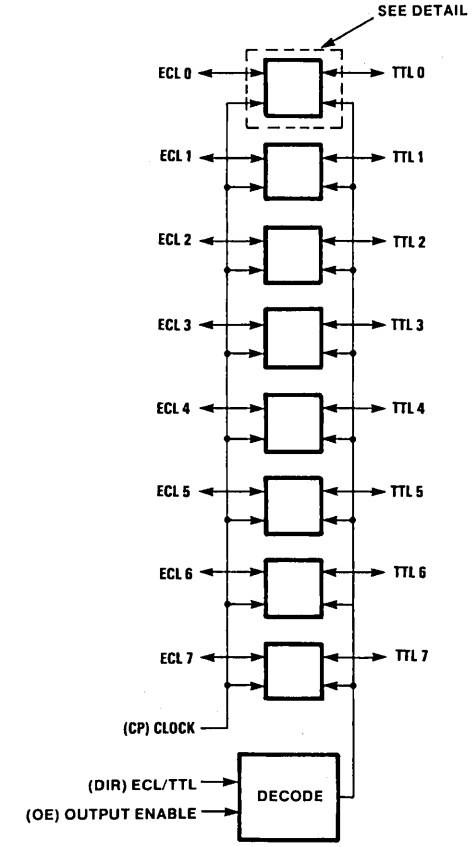
TL/F/10583–3

24-Pin Quad Cerpak



TL/F/10583–4

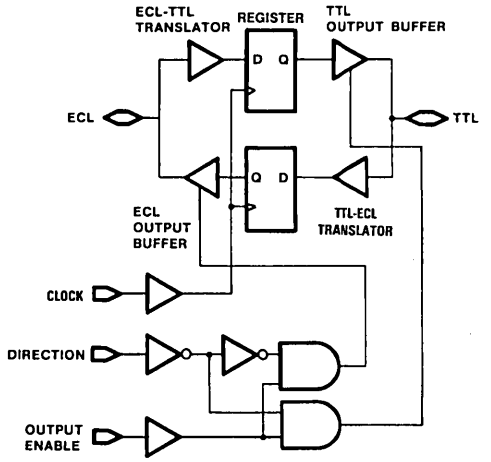
Functional Diagram



Note: DIR and OE use ECL logic levels

TL/F/10583–5

Detail



TL/F/10583–6

Truth Table

OE	DIR	CP	ECL Port	TTL Port	Notes
L	L	X	Input	Z	1, 3
L	H	X	LOW (Cut-Off)	Input	2, 3
H	L	⌐⌐	L	L	1
H	L	⌐⌐	H	H	1
H	L	L	X	NC	1, 3
H	H	⌐⌐	L	L	2
H	H	⌐⌐	H	H	2
H	H	L	NC	X	2, 3

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High Impedance
⌐⌐ = LOW-to-HIGH Clock Transition
NC = No Change

Note 1: ECL input to TTL output mode.

Note 2: TTL input to ECL output mode.

Note 3: Retains data present before CP.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature (T_{STG})	−65°C to +150°C
Maximum Junction Temperature (T_j)	
Ceramic	+175°C
Plastic	+150°C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
V_{TTL} Pin Potential to Ground Pin	−0.5V to +6.0V
ECL Input Voltage (DC)	V_{EE} to +0.5V
ECL Output Current (DC Output HIGH)	−50 mA
TTL Input Voltage (Note 3)	−0.5V to +6.0V
TTL Input Current (Note 3)	−30 mA to +5.0 mA
Voltage Applied to Output in HIGH State TRI-STATE Output	−0.5V to +5.5V
Current Applied to TTL Output in LOW State (Max)	Twice the Rated I_{OL} (mA)
ESD (Note 2)	≥2000V

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: ESD testing conforms to MIL-STD-883, Method 3015.

Note 3: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Case Temperature (T_C)	
Commercial	0°C to +85°C
Military	−55°C to +125°C
ECL Supply Voltage (V_{EE})	−5.7V to −4.2V
TTL Supply Voltage (V_{TTL})	+4.5V to +5.5V

Commercial Version

TTL-to-ECL DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C, V_{TTL} = +4.5V to +5.5V (Note 4)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{OH}	Output HIGH Voltage	−1025	−955	−870	mV	V_{IN} = V_{IH} (Max) or V_{IL} (Min) Loading with 50Ω to −2V
V_{OL}	Output LOW Voltage	−1830	−1705	−1620	mV	
	Cutoff Voltage		−2000	−1950	mV	OE or DIR LOW, V_{IN} = V_{IH} (Max) or V_{IL} (Min) Loading with 50Ω to −2V
V_{OHC}	Output HIGH Voltage Corner Point HIGH	−1035			mV	V_{IN} = V_{IH} (Min) or V_{IL} (Max) Loading with 50Ω to −2V
V_{OLC}	Output LOW Voltage Corner Point LOW			−1610	mV	
V_{IH}	Input HIGH Voltage	2.0		5.0	V	Over V_{TTL}, V_{EE}, T_C Range
V_{IL}	Input LOW Voltage	0		0.8	V	Over V_{TTL}, V_{EE}, T_C Range
I_{IH}	Input HIGH Current			70	μA	V_{IN} = +2.7V
	Breakdown Test			1.0	mA	V_{IN} = +5.5V
I_{IL}	Input LOW Current	−700			μA	V_{IN} = +0.5V
V_{FCD}	Input Clamp Diode Voltage	−1.2			V	I_{IN} = −18 mA
I_{EE}	V_{EE} Supply Current	−189 −199		−94 −94	mA	LE LOW, OE and DIR HIGH Inputs Open V_{EE} = −4.2V to −4.8V V_{EE} = −4.2V to −5.7V

Note 4: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

Commercial Version (Continued)

ECL-to-TTL DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C, C_L = 50 pF, V_{TTL} = +4.5V to +5.5V (Note)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{OH}	Output HIGH Voltage	2.7 2.4	3.1 2.9		V V	I_{OH} = −3 mA, V_{TTL} = 4.75V I_{OH} = −3 mA, V_{TTL} = 4.50V
V_{OL}	Output LOW Voltage		0.3	0.5	V	I_{OL} = 24 mA, V_{TTL} = 4.50V
V_{IH}	Input HIGH Voltage	−1165		−870	mV	Guaranteed HIGH Signal for All Inputs
V_{IL}	Input LOW Voltage	−1830		−1475	mV	Guaranteed LOW Signal for All Inputs
I_{IH}	Input HIGH Current			350	μA	V_{IN} = V_{IH} (Max)
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = V_{IL} (Min)
I_{OZHT}	TRI-STATE Current Output HIGH			70	μA	V_{OUT} = +2.7V
I_{OZLT}	TRI-STATE Current Output LOW	−700			μA	V_{OUT} = +0.5V
I_{OS}	Output Short-Circuit Current	−150		−60	mA	V_{OUT} = 0.0V, V_{TTL} = +5.5V
I_{TTL}	V_{TTL} Supply Current			74 49 67	mA mA mA	TTL Outputs LOW TTL Outputs HIGH TTL Outputs in TRI-STATE

DIP TTL-to-ECL AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{TTL} = +4.5V to +5.5V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = 25°C		T_C = 85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
f_{max}	Max Toggle Frequency	350		350		350		MHz	
t_{PLH} t_{PHL}	CP to E_n	1.7	3.6	1.7	3.7	1.9	3.9	ns	*Figures 1 & 2*
t_{PZH}	OE to E_n (Cutoff to HIGH)	1.3	4.2	1.5	4.4	1.7	4.8	ns	*Figures 1 & 2*
t_{PHZ}	OE to E_n (HIGH to Cutoff)	1.5	4.5	1.6	4.5	1.6	4.6	ns	*Figures 1 & 2*
t_{PHZ}	DIR to E_n (HIGH to Cutoff)	1.6	4.3	1.6	4.3	1.7	4.5	ns	*Figures 1 & 2*
t_{set}	T_n to CP	1.1		1.1		1.1		ns	*Figures 1 & 2*
t_{hold}	T_n to CP	1.7		1.7		1.9		ns	*Figures 1 & 2*
t_{pw}(H)	Pulse Width CP	2.1		2.1		2.1		ns	*Figures 1 & 2*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.6	1.6	0.6	1.6	0.6	1.6	ns	*Figures 1 & 2*

Note: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

Commercial Version (Continued)

DIP ECL-to-TTL AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{TTL} = +4.5V to +5.5V, V_{CC} = V_{CCA} = GND, C_L = 50 pF

Symbol	Parameter	T_C = 0°C		T_C = 25°C		T_C = 85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
f_{max}	Max Toggle Frequency	125		125		125		MHz	
t_{PLH} t_{PHL}	CP to T_n	3.1	7.2	3.1	7.2	3.3	7.7	ns	*Figures 3 & 4*
t_{PZH} t_{PZL}	OE to T_n (Enable Time)	3.4 3.8	8.45 9.2	3.7 4.0	8.95 9.2	4.0 4.3	9.7 9.95	ns	*Figures 3 & 5*
t_{PHZ} t_{PLZ}	OE to T_n (Disable Time)	3.2 3.0	8.95 7.7	3.3 3.4	8.95 8.7	3.5 4.1	9.2 9.95	ns	*Figures 3 & 5*
t_{PHZ} t_{PLZ}	DIR to T_n (Disable Time)	2.7 2.8	8.2 7.45	2.8 3.1	8.7 7.95	3.1 4.0	8.95 9.2	ns	*Figures 3 & 6*
t_{set}	E_n to CP	1.1		1.1		1.1		ns	*Figures 3 & 4*
t_{hold}	E_n to CP	2.1		2.1		2.6		ns	*Figures 3 & 4*
t_{pw}(H)	Pulse Width CP	4.1		4.1		4.1		ns	*Figures 3 & 4*

PCC and Cerpak TTL-to-ECL AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{TTL} = +4.5V to +5.5V

Symbol	Parameter	T_C = 0°C		T_C = 25°C		T_C = 85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
f_{max}	Max Toggle Frequency	350		350		350		MHz	
t_{PLH} t_{PHL}	CP to E_n	1.7	3.4	1.7	3.5	1.9	3.7	ns	*Figures 1 & 2*
t_{PZH}	OE to E_n (Cutoff to HIGH)	1.3	4.0	1.5	4.2	1.7	4.6	ns	*Figures 1 & 2*
t_{PHZ}	OE to E_n (HIGH to Cutoff)	1.5	4.3	1.6	4.3	1.6	4.4	ns	*Figures 1 & 2*
t_{PHZ}	DIR to E_n (HIGH to Cutoff)	1.6	4.1	1.6	4.1	1.7	4.3	ns	*Figures 1 & 2*
t_{set}	T_n to CP	1.0		1.0		1.0		ns	*Figures 1 & 2*
t_{hold}	T_n to CP	1.7		1.7		1.9		ns	*Figures 1 & 2*
t_{pw}(H)	Pulse Width CP	2.0		2.0		2.0		ns	*Figures 1 & 2*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.6	1.6	0.6	1.6	0.6	1.6	ns	*Figures 1 & 2*
t_{OSHL}	Maximum Skew Common Edge Output-to-Output Variation Data to Output Path		200		200		200	ps	PCC Only (Note 1)
t_{OSLH}	Maximum Skew Common Edge Output-to-Output Variation Data to Output Path		200		200		200	ps	PCC Only (Note 1)
t_{OST}	Maximum Skew Opposite Edge Output-to-Output Variation Data to Output Path		650		650		650	ps	PCC Only (Note 1)
t_{PS}	Maximum Skew Pin (Signal) Transition Variation Data to Output Path		650		650		650	ps	PCC Only (Note 1)

Note 1: Output-to-Output Skew is defined as the absolute value of the difference between the actual propagation delay for any outputs within the same packaged device. The specifications apply to any outputs switching in the same direction either HIGH to LOW (t_{OSHL}), or LOW to HIGH (t_{OSLH}), or in opposite directions both HL and LH (t_{OST}). Parameters t_{OST} and t_{PS} guaranteed by design.

Commercial Version (Continued)

PCC and Cerpak ECL-to-TTL AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{TTL} = +4.5V to +5.5V, C_L = 50 pF

Symbol	Parameter	T_C = 0°C		T_C = 25°C		T_C = 85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
f_{max}	Max Toggle Frequency	125		125		125		MHz	
t_{PLH} t_{PHL}	CP to T_n	3.1	7.0	3.1	7.0	3.3	7.5	ns	*Figures 3 & 4*
t_{PZH} t_{PZL}	OE to T_n (Enable Time)	3.4 3.8	8.25 9.0	3.7 4.0	8.75 9.0	4.0 4.3	9.5 9.75	ns	*Figures 3 & 5*
t_{PHZ} t_{PLZ}	OE to T_n (Disable Time)	3.2 3.0	8.75 7.5	3.3 3.4	8.75 8.5	3.5 4.1	9.0 9.75	ns	*Figures 3 & 5*
t_{PHZ} t_{PLZ}	DIR to T_n (Disable Time)	2.7 2.8	8.0 7.25	2.8 3.1	8.5 7.75	3.1 4.0	8.75 9.0	ns	*Figures 3 & 6*
t_{set}	E_n to CP	1.0		1.0		1.0		ns	*Figures 3 & 4*
t_{hold}	E_n to CP	2.0		2.0		2.5		ns	*Figures 3 & 4*
$t_{pw}(H)$	Pulse Width CP	4.0		4.0		4.0		ns	*Figures 3 & 4*
t_{OSHL}	Maximum Skew Common Edge Output-to-Output Variation Data to Output Path		600		600		600	ps	PCC Only (Note 1)
t_{OSLH}	Maximum Skew Common Edge Output-to-Output Variation Data to Output Path		850		850		850	ps	PCC Only (Note 1)
t_{OST}	Maximum Skew Opposite Edge Output-to-Output Variation Data to Output Path		1350		1350		1350	ps	PCC Only (Note 1)
t_{PS}	Maximum Skew Pin (Signal) Transition Variation Data to Output Path		950		950		950	ps	PCC Only (Note 1)

Note 1: Output-to-Output Skew is defined as the absolute value of the difference between the actual propagation delay for any outputs within the same packaged device. The specifications apply to any outputs switching in the same direction either HIGH to LOW (t_{OSHL}), or LOW to HIGH (t_{OSLH}), or in opposite directions both HL and LH (t_{OST}). Parameters t_{OST} and t_{PS} guaranteed by design.

Military Version

TTL-to-ECL DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = −55°C to +125°C, V_{TTL} = +4.5V to +5.5V

Symbol	Parameter	Min	Max	Units	T_C	Conditions		Notes
V_{OH}	Output HIGH Voltage	−1025	−870	mV	0°C to +125°C	V_{IN} = V_{IH} (Max) or V_{IL} (Min)	Loading with 50Ω to −2.0V	1, 2, 3
		−1085	−870	mV	−55°C			
V_{OL}	Output LOW Voltage	−1830	−1620	mV	0°C to +125°C			
		−1830	−1555	mV	−55°C			
	Cutoff Voltage		−1950	mV	0°C to +125°C	OE or DIR LOW		
			−1850	mV	−55°C			
V_{OHC}	Output HIGH Voltage	−1035		mV	0°C to +125°C	V_{IN} = V_{IH} (Min) or V_{IL} (Max)	Loading with 50Ω to −2.0V	1, 2, 3
		−1085		mV	−55°C			
V_{OLC}	Output LOW Voltage		−1610	mV	0°C to +125°C			
			−1555	mV	−55°C			
V_{IH}	Input HIGH Voltage	2.0		V	−55°C to +125°C	Over V_{TTL}, V_{EE}, T_C Range		1, 2, 3, 4
V_{IL}	Input LOW Voltage		0.8	V	−55°C to +125°C	Over V_{TTL}, V_{EE}, T_C Range		1, 2, 3, 4
I_{IH}	Input HIGH Current		70	μA	−55°C to +125°C	V_{IN} = +2.7V		1, 2, 3
	Breakdown Test		1.0	mA	−55°C to +125°C	V_{IN} = +5.5V		
I_{IL}	Input LOW Current	−1.0		mA	−55°C to +125°C	V_{IN} = +0.5V		1, 2, 3
V_{FCD}	Input Clamp Diode Voltage	−1.2		V	−55°C to +125°C	I_{IN} = −18 mA		1, 2, 3
I_{EE}	V_{EE} Supply Current	−210 −220	−70 −70	mA	−55°C to +125°C	LE LOW, OE and DIR HIGH Inputs Open V_{EE} = −4.2V to −4.8V V_{EE} = −4.2V to −5.7V		1, 2, 3

Military Version (Continued)

ECL-to-TTL DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = −55°C to +125°C, C_L = 50 pF, V_{TTL} = +4.5V to +5.5V

Symbol	Parameter	Min	Max	Units	T_C	Conditions	Notes
V_{OH}	Output HIGH Voltage	2.5 2.4		mV	−55°C to +125°C	I_{OH} = −1 mA, V_{TTL} = 4.50V I_{OH} = −3 mA, V_{TTL} = 4.50V	1, 2, 3
V_{OL}	Output LOW Voltage		0.5	mV	−55°C to +125°C	I_{OL} = 24 mA, V_{TTL} = 4.50V	
V_{IH}	Input HIGH Voltage	−1165	−870	mV	−55°C to +125°C	Guaranteed HIGH Signal for All Inputs	1, 2, 3, 4
V_{IL}	Input LOW Voltage	−1830	−1475	mV	−55°C to +125°C	Guaranteed LOW Signal for All Inputs	1, 2, 3, 4
I_{IH}	Input HIGH Current		350	μA	0°C to +125°C	V_{EE} = −5.7V V_{IN} = V_{IH} (Max)	1, 2, 3
			500	μA	−55°C		
I_{IL}	Input LOW Current	0.50		μA	−55°C to +125°C	V_{EE} = −4.2V V_{IN} = V_{IL} (Min)	1, 2, 3
I_{OZHT}	TRI-STATE Current Output HIGH		70	μA	−55°C to +125°C	V_{OUT} = +2.7V	1, 2, 3
I_{OZLT}	TRI-STATE Current Output LOW		−1.0	mA	−55°C to +125°C	V_{OUT} = +0.5V	1, 2, 3
I_{OS}	Output Short-Circuit Current	−150	−60	mA	−55°C to +125°C	V_{OUT} = 0.0V, V_{TTL} = +5.5V	1, 2, 3
I_{TTL}	V_{TTL} Supply Current		75 50 70	mA mA mA	−55°C to +125°C	TTL Outputs LOW TTL Outputs HIGH TTL Outputs in TRI-STATE	1, 2, 3

Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals −55°C), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 2: Screen tested 100% on each device at −55°C, +25°C, and +125°C, Subgroups 1, 2, 3, 7, and 8.

Note 3: Sample tested (Method 5005, Table I) on each manufactured lot at −55°C, +25°C, and +125°C, Subgroups A1, 2, 3, 7, and 8.

Note 4: Guaranteed by applying specified input condition and testing V_{OH}/V_{OL}.

Military Version (Continued)

TTL-to-ECL AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{TTL} = +4.5V to +5.5V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = −55°C		T_C = 25°C		T_C = +125°C		Units	Conditions	Notes
		Min	Max	Min	Max	Min	Max			
f_{max}	Max Toggle Frequency	250		250		250		MHz		4
t_{PLH} t_{PHL}	CP to E_n	1.3	3.8	1.6	3.7	1.9	4.3	ns	*Figures 1 & 2*	1, 2, 3
t_{PZH}	OE to E_n (Cutoff to HIGH)	1.0	4.3	1.5	4.4	1.7	9.0	ns	*Figures 1 & 2*	
t_{PHZ}	OE to E_n (HIGH to Cutoff)	1.5	5.0	1.6	4.5	1.6	5.0	ns	*Figures 1 & 2*	
t_{PHZ}	DIR to E_n (HIGH to Cutoff)	1.6	4.7	1.6	4.3	1.7	4.7	ns	*Figures 1 & 2*	
t_{set}	T_n to CP	2.5		2.0		2.5		ns	*Figures 1 & 2*	4
t_{hold}	T_n to CP	2.5		2.0		2.5		ns	*Figures 1 & 2*	
t_{pw}(H)	Pulse Width CP	2.5		2.0		2.5		ns	*Figures 1 & 2*	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.4	2.3	0.5	2.1	0.4	2.4	ns	*Figures 1 & 2*	

ECL-to-TTL AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{TTL} = +4.5V to +5.5V, V_{CC} = V_{CCA} = GND, C_L = 50 pF

Symbol	Parameter	T_C = −55°C		T_C = 25°C		T_C = +125°C		Units	Conditions	Notes
		Min	Max	Min	Max	Min	Max			
f_{max}	Max Toggle Frequency	200		200		100		MHz		4
t_{PLH} t_{PHL}	CP to T_n	3.1	8.0	3.1	7.3	3.3	8.0	ns	*Figures 3 & 4*	1, 2, 3
t_{PZH} t_{PZL}	OE to T_n (Enable Time)	3.4 3.7	9.1 9.5	3.7 4.0	9.0 9.3	4.0 4.3	10.1 10.4	ns	*Figures 3 & 5*	
t_{PHZ} t_{PLZ}	OE to T_n (Disable Time)	3.2 3.0	10.0 9.8	3.3 3.4	9.0 8.8	3.5 4.1	9.3 10.4	ns	*Figures 3 & 5*	
t_{PHZ} t_{PLZ}	DIR to T_n (Disable Time)	2.6 2.7	9.5 8.7	2.8 3.1	8.8 8.0	3.0 4.0	9.0 9.6	ns	*Figures 3 & 6*	
t_{set}	E_n to CP	2.5		2.0		2.5		ns	*Figures 3 & 4*	4
t_{hold}	E_n to CP	3.0		2.5		3.0		ns	*Figures 3 & 4*	
t_{pw}(H)	Pulse Width CP	2.5		2.5		5.0		ns	*Figures 3 & 4*	

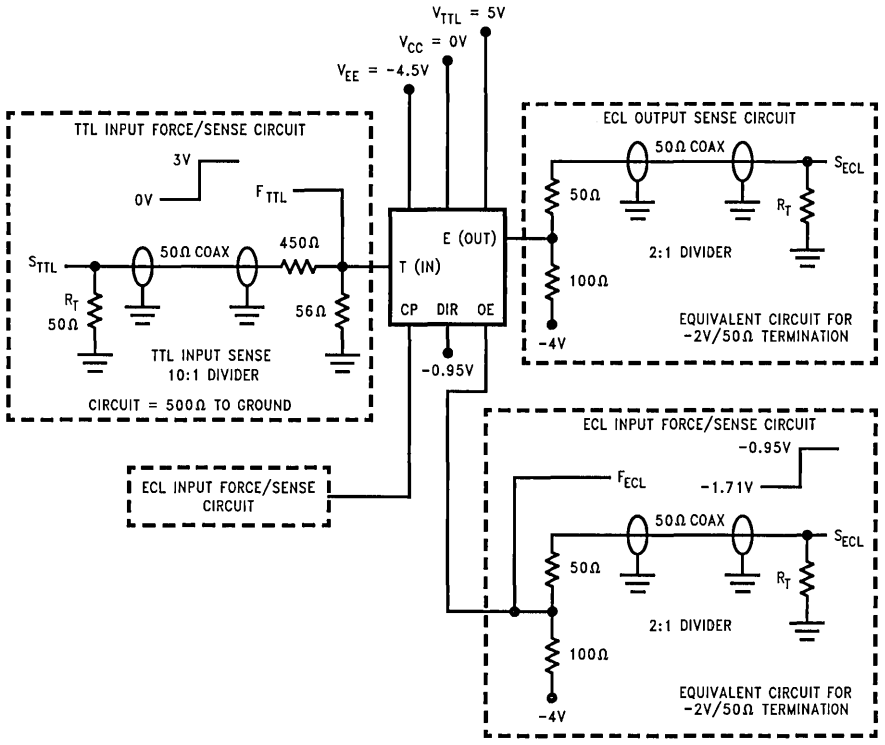
Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals −55°C), then testing immediately after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 2: Screen tested 100% on each device at +25°C temperature latched only, Subgroup A9.

Note 3: Sample tested (Method 5005, Table I) on each manufactured lot at +25°C, Subgroup A9, and at +125°C and −55°C temperatures, Subgroups A10 and A11.

Note 4: Not tested at +25°C, +125°C, and −55°C temperature (design characterization data).

Test Circuitry (TTL-to-ECL)



TL/F/10583–7

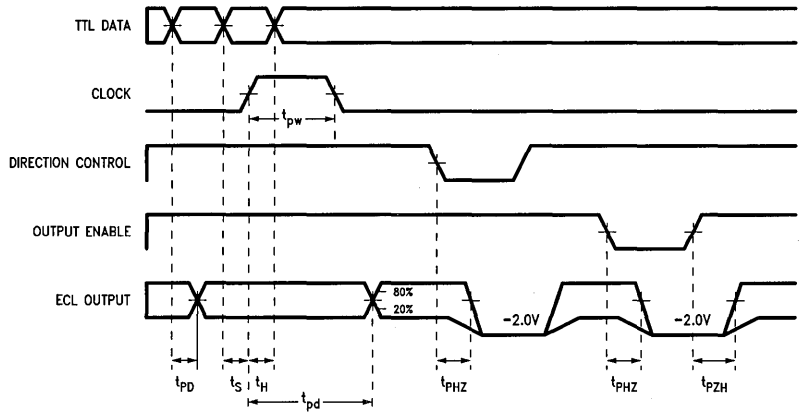
Note 1: R_T = 50Ω termination resistive load. When an input or output is being monitored by a scope, R_T is supplied by the scope's 50Ω input resistance. When an input or output is not being monitored, an external 50Ω resistance must be applied to serve as R_T.

Note 2: TTL and ECL force signals are brought to the DUT via 50Ω coax lines.

Note 3: V_{TTL} is decoupled to ground with 0.1 μF, V_{EE} is decoupled to ground with 0.01 μF and V_{CC} is connected to ground.

FIGURE 1. TTL-to-ECL AC Test Circuit

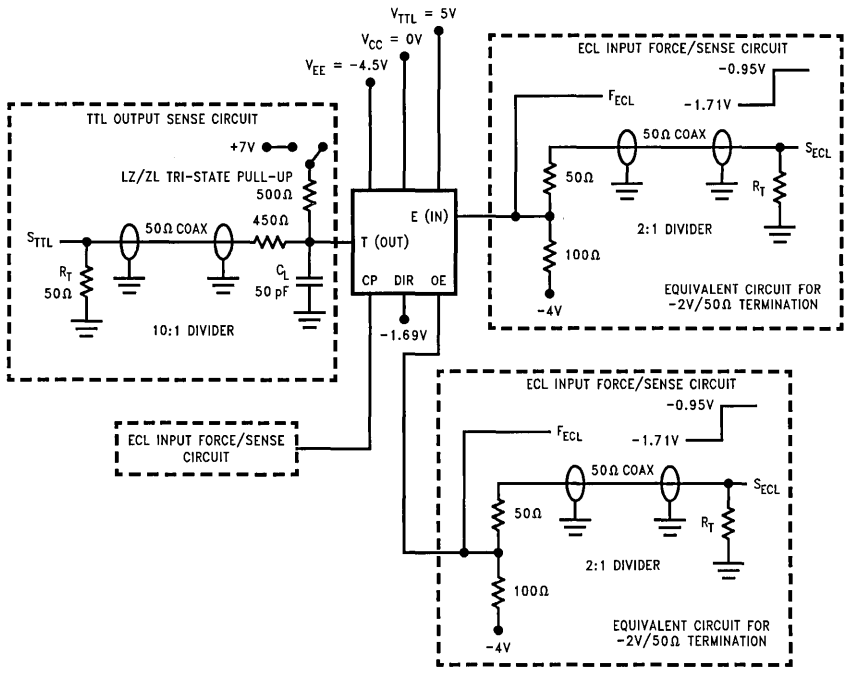
Switching Waveforms (TTL-to-ECL)



TL/F/10583–9

FIGURE 2. TTL to ECL Transition—Propagation Delay and Transition Times

Test Circuitry (ECL-to-TTL)



TL/F/10583–10

Note 1: R_T = 50Ω termination resistive load. When an input or output is being monitored by a scope, R_T is supplied by the scope's 50Ω input resistance. When an input or output is not being monitored, an external 50Ω resistance must be applied to serve as R_T.

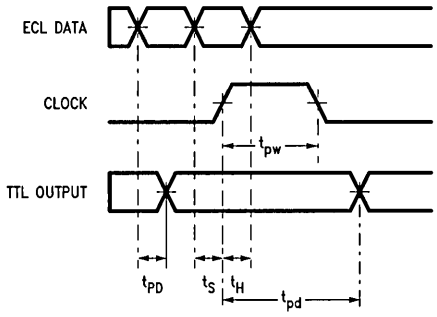
Note 2: The TTL TRI-STATE pull-up switch is connected to +7V only for ZL and LZ tests.

Note 3: TTL and ECL force signals are brought to the DUT via 50Ω coax lines.

Note 4: V_{TTL} is decoupled to ground with 0.1 μF, V_{EE} is decoupled to ground with 0.01 μF and V_{CC} is connected to ground.

FIGURE 3. ECL-to-TTL AC Test Circuit

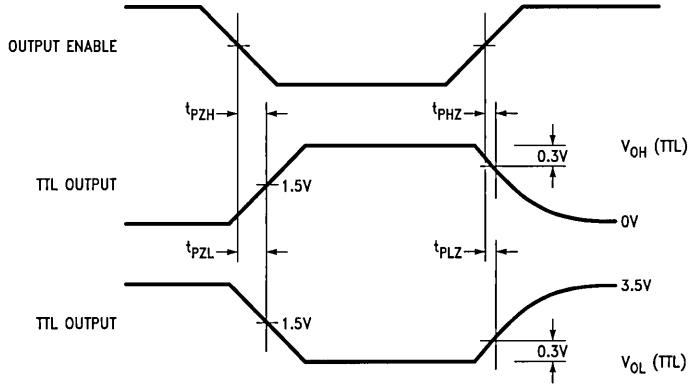
Switching Waveforms (ECL-to-TTL)



Note: DIR is LOW, OE is HIGH

TL/F/10583–11

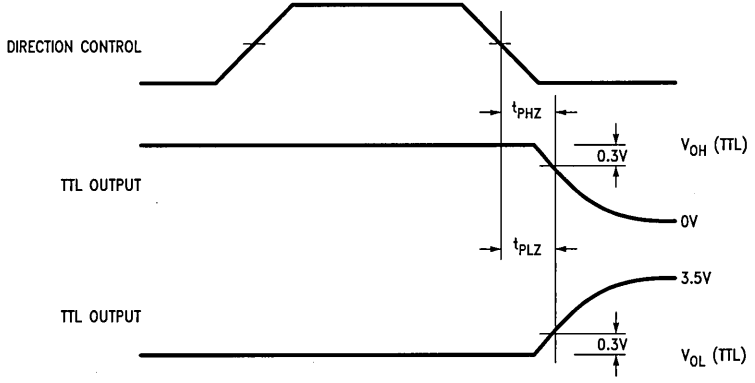
FIGURE 4. ECL-to-TTL Transition—Propagation Delay and Transition Times



Note: DIR is LOW

TL/F/10583–12

FIGURE 5. ECL-to-TTL Transition, OE to TTL Output, Enable and Disable Times



Note: OE is HIGH

TL/F/10583–13

FIGURE 6. ECL-to-TTL Transition, DIR to TTL Output, Disable Time

National Semiconductor

100331
Low Power Triple D Flip-Flop

General Description

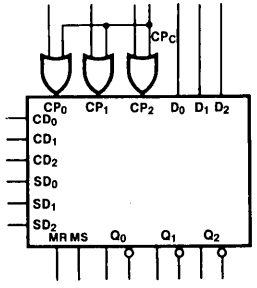
The 100331 contains three D-type, edge-triggered master/slave flip-flops with true and complement outputs, a Common Clock (CP_C), and Master Set (MS) and Master Reset (MR) inputs. Each flip-flop has individual Clock (CP_n), Direct Set (SD_n) and Direct Clear (CD_n) inputs. Data enters a master when both CP_n and CP_C are LOW and transfers to a slave when CP_n or CP_C (or both) go HIGH. The Master Set, Master Reset and individual CD_n and SD_n inputs override the Clock inputs. All inputs have 50 kΩ pull-down resistors.

Features

- 35% power reduction of the 100131
- 2000V ESD protection
- Pin/function compatible with 100131
- Voltage compensated operating range = −4.2V to −5.7V
- Available to industrial grade temperature range
- Available to MIL-STD-883

Ordering Code: See Section 6

Logic Symbol

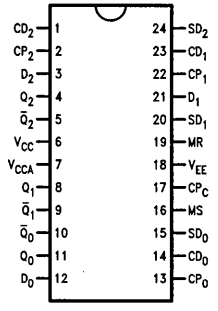


TL/F/10262–1

Pin Names	Description
CP_0–CP_2	Individual Clock Inputs
CP_C	Common Clock Input
D_0–D_2	Data Inputs
CD_0–CD_2	Individual Direct Clear Inputs
SD_n	Individual Direct Set Inputs
MR	Master Reset Input
MS	Master Set Input
Q_0-Q_2	Data Outputs
$\overline{Q}_0$–$\overline{Q}_2$	Complementary Data Outputs

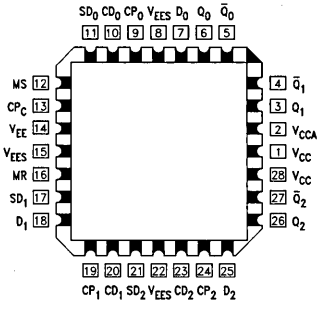
Connection Diagrams

24-Pin DIP/SOIC



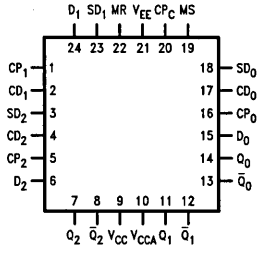
TL/F/10262–2

28-Pin PCC



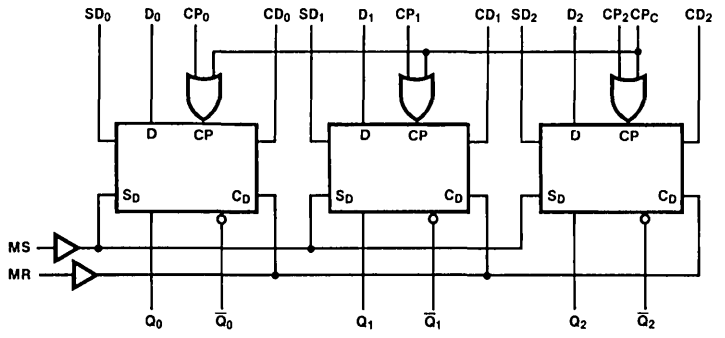
TL/F/10262–4

24-Pin Quad Cerpak



TL/F/10262–3

Logic Diagram



TL/F/10262–5

Truth Tables (Each Flip-Flop)

Synchronous Operation

Inputs					Outputs
D_n	CP_n	CP_C	MS SD_n	MR CD_n	$Q_n(t+1)$
L	↗	L	L	L	L
H	↗	L	L	L	H
L	L	↗	L	L	L
H	L	↗	L	L	H
X	L	L	L	L	Qn(t)
X	H	X	L	L	Qn(t)
X	X	H	L	L	Qn(t)

Asynchronous Operation

Inputs					Outputs
D_n	CP_n	CP_C	MS SD_n	MR CD_n	$Q_n(t+1)$
X	X	X	H	L	H
X	X	X	L	H	L
X	X	X	H	H	U

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
U = Undefined
t = Time before CP Positive Transition
t + 1 = Time after CP Positive Transition
↗ = LOW to HIGH Transition

Absolute Maximum Ratings

Above which the useful life may be impaired (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature (T_{STG})	−65°C to +150°C
Maximum Junction Temperature (T_J)	
Ceramic	+175°C
Plastic	+150°C
Pin Potential to Ground Pin (V_{EE})	−7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Output Current (DC Output HIGH)	−50 mA
ESD (Note 2)	≤ 2000V

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: ESD testing conforms to MIL-STD-883, Method 3015.

Recommended Operating Conditions

Case Temperature (T_C)	
Commercial	0°C to +85°C
Industrial	−40°C to +85°C
Military	−55°C to +125°C
Supply Voltage (V_{EE})	−5.7V to −4.2V

Commercial Version

DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions	
V_{OH}	Output HIGH Voltage	−1025	−955	−870	mV	V_{IN} = V_{IH} (Max) or V_{IL} (Min)	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830	−1705	−1620	mV		
V_{OHC}	Output HIGH Voltage	−1035			mV	V_{IN} = V_{IH} (Min) or V_{IL} (Max)	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610	mV		
V_{IH}	Input HIGH Voltage	−1165		−870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1830		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.5			μA	V_{IN} = V_{IL} (Min)	
I_{IH}	Input HIGH Current			240	μA	V_{IN} = V_{IH} (Max)	
I_{EE}	Power Supply Current	−122		−65	mA	Inputs Open	

Note 3: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

Commercial Version (Continued)

DIP AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND (Continued)

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions	
		Min	Max	Min	Max	Min	Max			
f_{max}	Toggle Frequency	375		375		375		MHz	*Figures 2* and *3*	
t_{PLH} t_{PHL}	Propagation Delay CP_C to Output	0.75	2.00	0.75	2.00	0.75	2.00	ns	*Figures 1* and *3*	
t_{PLH} t_{PHL}	Propagation Delay CP_n to Output	0.75	2.00	0.75	2.00	0.75	2.00	ns		
t_{PLH} t_{PHL}	Propagation Delay CD_n, SD_n to Output	0.70	1.70	0.70	1.70	0.70	1.80	ns	CP_n, CP_C = L	*Figures 1* and *4*
t_{PLH} t_{PHL}		0.70	2.00	0.70	2.00	0.70	2.00		CP_n, CP_C = H	
t_{PLH} t_{PHL}	Propagation Delay MS, MR to Output	1.10	2.60	1.10	2.60	1.10	2.60	ns	CP_n, CP_C = L	
t_{PLH} t_{PHL}		1.10	2.80	1.10	2.80	1.10	2.80		CP_n, CP_C = H	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.35	1.30	0.35	1.30	0.35	1.30	ns	*Figures 1, 3* and *4*	
t_S	Setup Time D_n	0.40		0.40		0.40		ns	*Figure 5*	
	CD_n, SD_n (Release Time)	1.30		1.30		1.30			*Figure 4*	
	MS, MR (Release Time)	2.30		2.30		2.30				
t_H	Hold Time D_n	0.5		0.5		0.7		ns	*Figure 5*	
$t_{pw}(H)$	Pulse Width HIGH CP_n, CP_C, CD_n, SD_n, MR, MS	2.00		2.00		2.00		ns	*Figures 3* and *4*	

SOIC, PCC and Cerpak AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions	
		Min	Max	Min	Max	Min	Max			
f_{max}	Toggle Frequency	400		400		400		MHz	*Figures 2* and *3*	
t_{PLH} t_{PHL}	Propagation Delay CP_C to Output	0.75	1.80	0.75	1.80	0.75	1.80	ns	*Figures 1* and *3*	
t_{PLH} t_{PHL}	Propagation Delay CP_n to Output	0.75	1.80	0.75	1.80	0.75	1.80	ns		
t_{PLH} t_{PHL}	Propagation Delay CD_n, SD_n to Output	0.70	1.50	0.70	1.50	0.70	1.60	ns	CP_n, CP_C = L	*Figures 1* and *4*
t_{PLH} t_{PHL}		0.80	1.80	0.70	1.80	0.70	1.80		CP_n, CP_C = H	
t_{PLH} t_{PHL}	Propagation Delay MS, MR to Output	1.10	2.40	1.10	2.40	1.10	2.40	ns	CP_n, CP_C = L	
t_{PLH} t_{PHL}		1.10	2.60	1.10	2.60	1.10	2.60		CP_n, CP_C = H	

Commercial Version (Continued)

SOIC, PCC and Cerpak AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND (Continued)

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions	
		Min	Max	Min	Max	Min	Max			
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.35	1.10	0.35	1.10	0.35	1.10	ns	*Figures 1, 3* and *4*	
t_S	Setup Time D_n	0.30		0.30		0.30		ns	*Figure 5*	
	CD_n, SD_n (Release Time) MS, MR (Release Time)	1.20 2.20		1.20 2.20		1.20 2.20			*Figure 4*	
t_H	Hold Time D_n	0.5		0.5		0.7		ns	*Figure 5*	
$t_{pw}(H)$	Pulse Width HIGH CP_n, CP_C, CD_n, SD_n, MR, MS	2.00		2.00		2.00		ns	*Figures 3* and *4*	
t_{PLH} t_{PHL}	Propagation Delay CP_C to Output	0.75	1.40	0.75	1.40	0.80	1.50	ns	*Figures 1* and *3* PCC Only	
t_{PLH} t_{PHL}	Propagation Delay CP_n to Output	0.70	1.40	0.75	1.40	0.80	1.50	ns		
t_{PLH} t_{PHL}	Propagation Delay CD_n, SD_n to Output	0.70	1.50	0.70	1.50	0.80	1.60	ns	CP_n, CP_C = L PCC Only	*Figures 1* and *4*
t_{PLH} t_{PHL}		0.80	1.70	0.80	1.70	0.80	1.80		CP_n, CP_C = H PCC Only	
t_{PLH} t_{PHL}	Propagation Delay MS, MR to Output	1.10	2.00	1.10	2.00	1.20	2.10	ns	CP_n, CP_C = L PCC Only	
t_{PLH} t_{PHL}		1.20	2.10	1.20	2.10	1.30	2.20		CP_n, CP_C = H PCC Only	
t_{OSHL}	Maximum Skew Common Edge Output-to-Output Variation Common Clock to Output Path		100		100		100	ps	PCC Only (Note 1)	
t_{OSHL}	Maximum Skew Common Edge Output-to-Output Variation CP_n to Output Path		235		235		235	ps	PCC Only (Note 1)	
t_{OSLH}	Maximum Skew Common Edge Output-to-Output Variation Common Clock to Output Path		120		120		120	ps	PCC Only (Note 1)	
t_{OSLH}	Maximum Skew Common Edge Output-to-Output Variation CP_n to Output Path		275		275		275	ps	PCC Only (Note 1)	
t_{OST}	Maximum Skew Opposite Edge Output-to-Output Variation Common Clock to Output Path		125		125		125	ps	PCC Only (Note 1)	
t_{OST}	Maximum Skew Opposite Edge Output-to-Output Variation CP_n to Output Path		265		265		265	ps	PCC Only (Note 1)	
t_{ps}	Maximum Skew Pin (Signal) Transition Variation Common Clock to Output Path		90		90		90	ps	PCC Only (Note 1)	
t_{ps}	Maximum Skew Pin (Signal) Transition Variation CP_n to Output Path		90		90		90	ps	PCC Only (Note 1)	

Note 1: Output-to-Output Skew is defined as the absolute value of the difference between the actual propagation delay for any outputs within the same packaged device. The specifications apply to any outputs switching in the same direction either HIGH to LOW (t_{OSHL}), or LOW to HIGH (t_{OSLH}), or in opposite directions both HL and LH (t_{OST}). Parameters t_{OST} and t_{ps} guaranteed by design.

Industrial Version

PCC DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = −40°C to +85°C (Note)

Symbol	Parameter	T_C = −40°C		T_C = 0°C to +85°C		Units	Conditions	
		Min	Max	Min	Max			
V_{OH}	Output HIGH Voltage	−1085	−870	−1025	−870	mV	V_{IN} = V_{IH} (Max) or V_{IL} (Min)	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830	−1575	−1830	−1620	mV		
V_{OHC}	Output HIGH Voltage	−1095		−1035		mV	V_{IN} = V_{IH} (Min) or V_{IL} (Max)	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage		−1565		−1610	mV		
V_{IH}	Input HIGH Voltage	−1170	−870	−1165	−870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1830	−1480	−1830	1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.5		0.5		μA	V_{IN} = V_{IL} (Min)	
I_{IH}	Input HIGH Current		300		240	μA	V_{IN} = V_{IH} (Max)	
I_{EE}	Power Supply Current	−122	−60	−122	−65	mA	Inputs Open	

Note: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

PCC AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = −40°C		T_C = +25°C		T_C = +85°C		Units	Conditions	
		Min	Max	Min	Max	Min	Max			
f_{max}	Toggle Frequency	375		400		400		MHz	*Figures 2* and *3*	
t_{PLH} t_{PHL}	Propagation Delay CP_C to Output	0.75	1.80	0.75	1.80	0.75	1.80	ns	*Figures 1* and *3*	
t_{PLH} t_{PHL}	Propagation Delay CP_n to Output	0.70	1.80	0.75	1.80	0.75	1.80	ns		
t_{PLH} t_{PHL}	Propagation Delay CD_n, SD_n to Output	0.60	1.50	0.70	1.50	0.70	1.60	ns	CP_n, CP_C = L	*Figures 1* and *4*
		0.70	1.80	0.70	1.80	0.70	1.80		CP_n, CP_C = H	
t_{PLH} t_{PHL}	Propagation Delay MS, MR to Output	1.10	2.40	1.10	2.40	1.10	2.40	ns	CP_n, CP_C = L	
		1.10	2.60	1.10	2.60	1.10	2.60		CP_n, CP_C = H	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.20	1.40	0.35	1.10	0.35	1.10	ns	*Figures 1, 3* and *4*	
t_S	Setup Time D_n CD_n, SD_n (Release Time) MS, MR (Release Time)	 1.00 1.50 2.50		 0.30 1.20 2.20		 0.30 1.20 2.20		ns	*Figure 5* *Figure 4*	
t_H	Hold Time D_n	0.7		0.5		0.7		ns	*Figure 5*	
t_{pw}(H)	Pulse Width HIGH CP_n, CP_C, CD_n, SD_n, MR, MS	2.00		2.00		2.00		ns	*Figures 3* and *4*	

Military Version

DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = −55°C to +125°C

Symbol	Parameter	Min	Max	Units	T_C	Conditions		Notes
V_{OH}	Output HIGH Voltage	−1025	−870	mV	0°C to +125°C	V_{IN} = V_{IH} (Max) or V_{IL} (Min)	Loading with 50Ω to −2.0V	1, 2, 3
		−1085	−870	mV	−55°C			
V_{OL}	Output LOW Voltage	−1830	−1620	mV	0°C to +125°C			
		−1830	−1555	mV	−55°C			
V_{OHC}	Output HIGH Voltage	−1035		mV	0°C to +125°C	V_{IN} = V_{IH} (Min) or V_{IL} (Max)	Loading with 50Ω to −2.0V	1, 2, 3
		−1085		mV	−55°C			
V_{OLC}	Output LOW Voltage		−1610	mV	0°C to +125°C			
			−1555	mV	−55°C			
V_{IH}	Input HIGH Voltage	−1165	−870	mV	−55°C to +125°C	Guaranteed HIGH Signal for all Inputs		1, 2, 3, 4
V_{IL}	Input LOW Voltage	−1830	−1475	mV	−55°C to +125°C	Guaranteed LOW Signal for all Inputs		1, 2, 3, 4
I_{IL}	Input LOW Current	0.50		μA	−55°C to +125°C	V_{EE} = −4.2V V_{IN} = V_{IL} (Min)		1, 2, 3
I_{IH}	Input HIGH Current		240	μA	0°C to +125°C	V_{EE} = −5.7V V_{IN} = V_{IH} (Max)		1, 2, 3
			340	μA	−55°C			
I_{EE}	Power Supply Current	−130	−50	mA	−55°C to +125°C	Inputs Open		1, 2, 3

Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals −55°C), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 2: Screen tested 100% on each device at −55°C, +25°C, and +125°C, Subgroups, 1, 2, 3, 7 and 8.

Note 3: Sampled tested (Method 5005, Table I) on each manufactured lot at −55°C, +25°C, and +125°C, Subgroups A1, 2, 3, 7 and 8.

Note 4: Guaranteed by applying specified input condition and testing V_{OH}/V_{OL}.

Military Version (Continued)

AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = −55°C		T_C = +25°C		T_C = +125°C		Units	Conditions		Notes
		Min	Max	Min	Max	Min	Max				
f_{max}	Toggle Frequency	400		400		400		MHz	*Figures 2* and *3*		4
t_{PLH} t_{PHL}	Propagation Delay CP_C to Output	0.50	2.20	0.60	2.00	0.50	2.40	ns	*Figures 1* and *3*		1, 2, 3
t_{PLH} t_{PHL}	Propagation Delay CP_n to Output	0.50	2.20	0.60	2.00	0.50	2.40	ns			
t_{PLH} t_{PHL}	Propagation Delay CD_n, SD_n to Output	0.50	2.20	0.60	2.00	0.50	2.40	ns	CP_n, CP_C = L	*Figures 1* and *4*	
t_{PLH} t_{PHL}		0.50	2.40	0.60	2.10	0.50	2.50		CP_n, CP_C = H		
t_{PLH} t_{PHL}	Propagation Delay MS, MR to Output	0.70	2.70	0.80	2.60	0.80	2.90	ns	CP_n, CP_C = L		
t_{PLH} t_{PHL}		0.70	2.90	0.80	2.80	0.80	3.10		CP_n, CP_C = H		
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.20	1.40	0.20	1.40	0.20	1.40	ns	*Figures 1, 3* and *4*		
t_s	Setup Time D_n	1.00		0.80		0.90		ns	*Figure 5*		4
	CD_n, SD_n (Release Time)	1.50		1.30		1.60			*Figure 4*		
	MS, MR (Release Time)	2.50		2.30		2.50					
t_h	Hold Time D_n	1.50		1.30		1.60		ns	*Figure 5*		
t_{pw}(H)	Pulse Width HIGH CP_n, CP_C, CD_n, SD_n, MR, MS	2.00		2.00		2.00		ns	*Figures 3* and *4*		

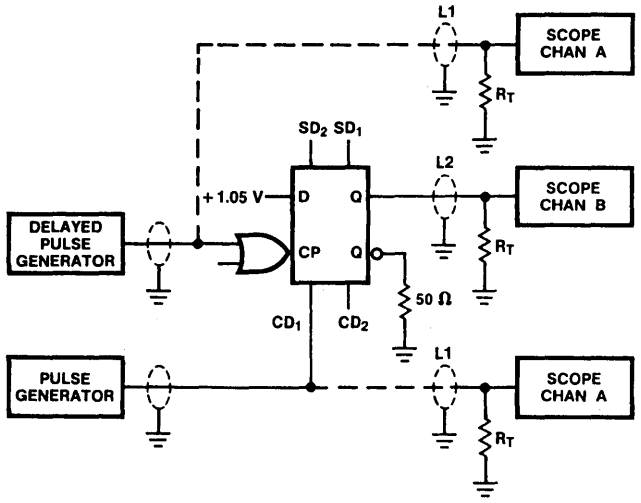
Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals −55°C), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 2: Screen tested 100% on each device at +25°C. Temperature only, Subgroup A9.

Note 3: Sample tested (Method 5005, Table I) on each Mfg. lot at +25°C, Subgroup A9, and at +125°C, and −55°C Temp., Subgroups A10 and A11.

Note 4: Not tested at +25°C, +125°C and −55°C Temperature (design characterization data).

Test Circuits



TL/F/10262–6

FIGURE 1. AC Test Circuit

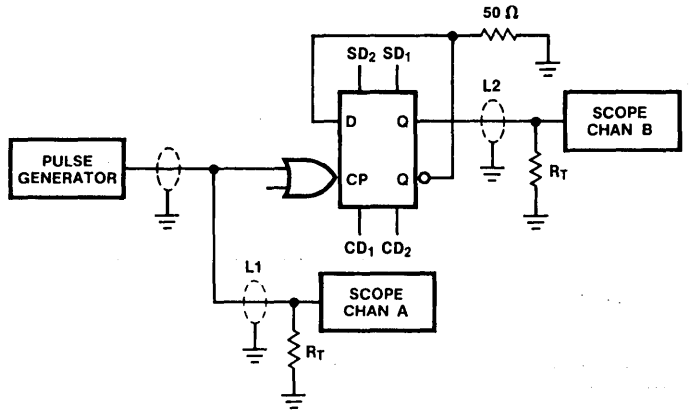


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FIGURE 2. Toggle Frequency Test Circuit

Notes:

V_{CC}, V_{CCA} = +2V, V_{EE} = −2.5V

L1 and L2 = Equal length 50Ω impedance lines

R_T = 50Ω terminator internal to scope

Decoupling 0.1 μF from GND to V_{CC} and V_{EE}

All unused outputs are loaded with 50Ω to GND

C_L = Fixture and stray capacitance ≤ 3 pF

Switching Waveforms

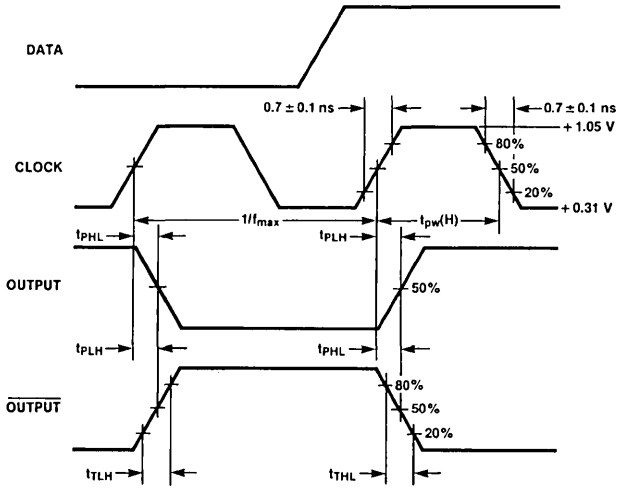

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FIGURE 3. Propagation Delay (Clock) and Transition Times

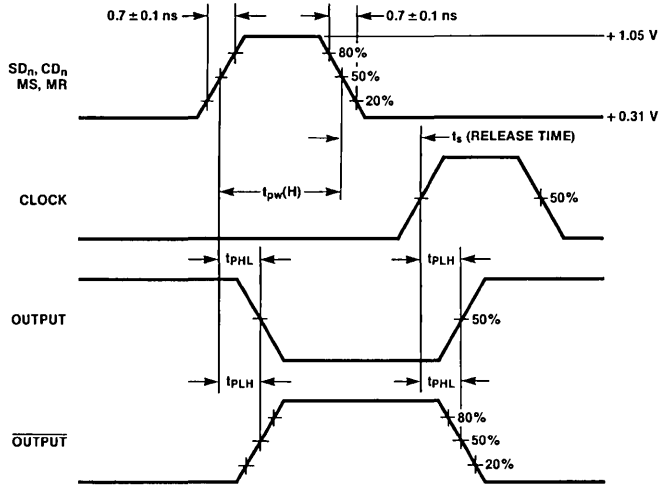

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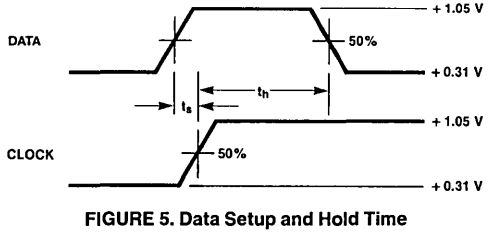
FIGURE 4. Propagation Delay (Resets)



TL/F/10262–10

FIGURE 5. Data Setup and Hold Time

Note: t_s is the minimum time before the transition of the clock that information must be present at the data input.

Note: t_h is the minimum time after the transition of the clock that information must remain unchanged at the data input.

National Semiconductor

100336
Low Power 4-Stage Counter/Shift Register

General Description

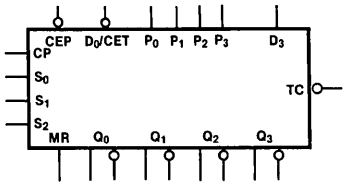
The 100336 operates as either a modulo-16 up/down counter or as a 4-bit bidirectional shift register. Three Select (S_n) inputs determine the mode of operation, as shown in the Function Select table. Two Count Enable ($\overline{CEP}$, $\overline{CET}$) inputs are provided for ease of cascading in multistage counters. One Count Enable ($\overline{CET}$) input also doubles as a Serial Data (D_0) input for shift-up operation. For shift-down operation, D_3 is the Serial Data input. In counting operations the Terminal Count ($\overline{TC}$) output goes LOW when the counter reaches 15 in the count/up mode or 0 (zero) in the count/down mode. In the shift modes, the $\overline{TC}$ output repeats the Q_3 output. The dual nature of this $\overline{TC}/Q_3$ output and the $D_0/\overline{CET}$ input means that one interconnection from one stage to the next higher stage serves as the link for multistage counting or shift-up operation. The individual Preset (P_n) inputs are used to enter data in parallel or to preset the counter in programmable counter applications. A HIGH signal on the Master Reset (MR) input overrides all other inputs and asynchronously clears the flip-flops. In addition, a synchronous clear is provided, as well as a complement function which synchronously inverts the contents of the flip-flops. All inputs have 50 kΩ pull-down resistors.

Features

- 40% power reduction of the 100136
- 2000V ESD protection
- Pin/function compatible with 100136
- Voltage compensated operating range = −4.2V to −5.7V
- Available to industrial grade temperature range
- Available to MIL-STD-883

Ordering Code: See Section 6

Logic Symbol

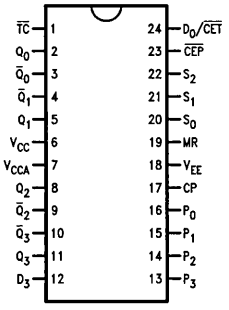


TL/F/10584–1

Pin Names	Description
CP	Clock Pulse Input
$\overline{CEP}$	Count Enable Parallel Input (Active LOW)
$D_0/\overline{CET}$	Serial Data Input/Count Enable Trickle Input (Active LOW)
S_0–S_2	Select Inputs
MR	Master Reset Input
P_0–P_3	Preset Inputs
D_3	Serial Data Input
$\overline{TC}$	Terminal Count Output
Q_0–Q_3	Data Outputs
$\overline{Q}_0$–$\overline{Q}_3$	Complementary Data Outputs

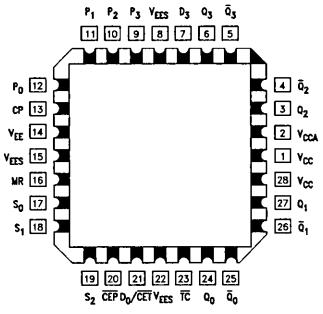
Connection Diagrams

24-Pin DIP/SOIC



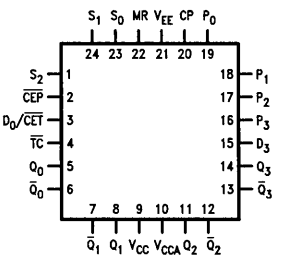
TL/F/10584–2

28-Pin PCC



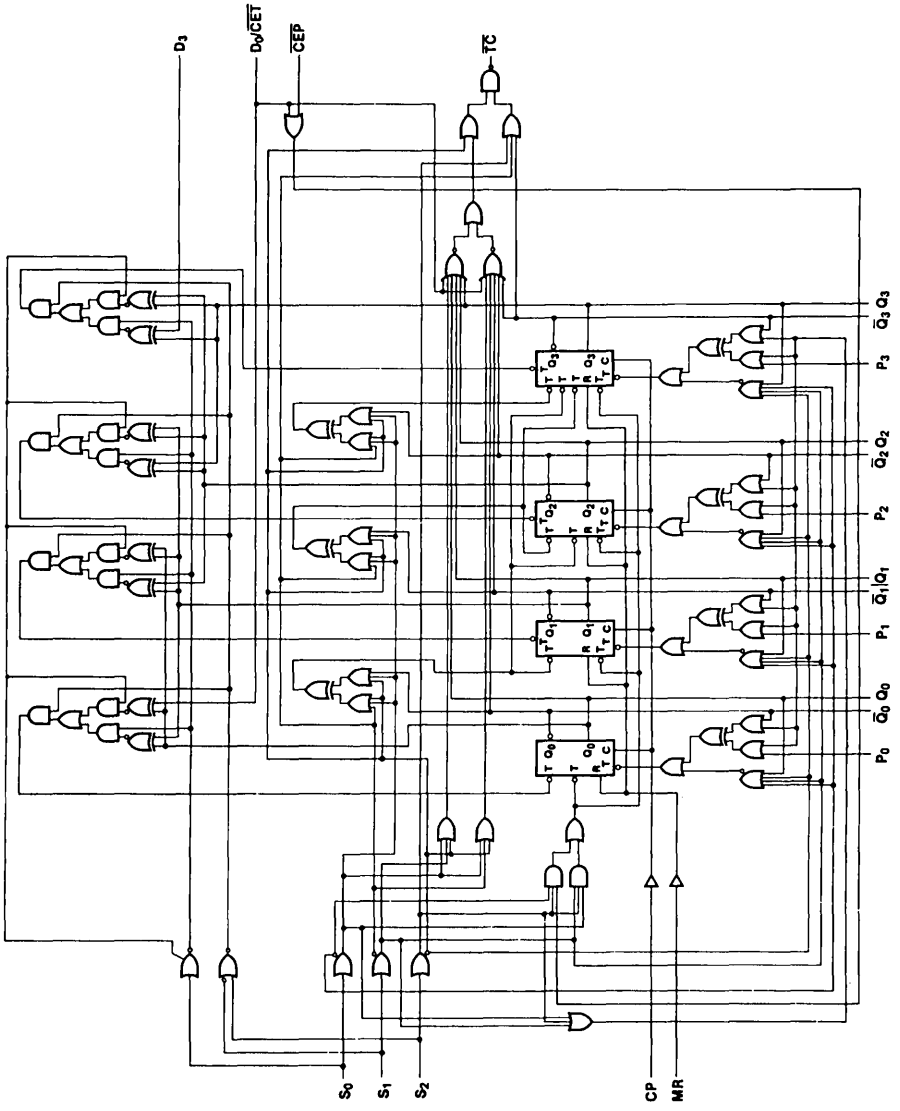
TL/F/10584–4

24-Pin Quad Cerpak



TL/F/10584–3

Logic Diagram



TL/F/10584–5

Function Select Table

S_2	S_1	S_0	Function
L	L	L	Parallel Load
L	L	H	Complement
L	H	L	Shift Left
L	H	H	Shift Right
H	L	L	Count Down
H	L	H	Clear
H	H	L	Count Up
H	H	H	Hold

Truth Table

Q_0 = LSB

Inputs								Outputs					
MR	S_2	S_1	S_0	$\overline{CEP}$	$D_0/\overline{CET}$	D_3	CP	Q_3	Q_2	Q_1	Q_0	$\overline{TC}$	Mode
L	L	L	L	X	X	X	↗	P_3	P_2	P_1	P_0	L	Preset (Parallel Load)
L	L	L	H	X	X	X	↗	$\overline{Q}_3$	$\overline{Q}_2$	$\overline{Q}_1$	$\overline{Q}_0$	L	Invert
L	L	H	L	X	X	X	↗	D_3	Q_3	Q_2	Q_1	D_3	Shift to LSB
L	L	H	H	X	X	X	↗	Q_2	Q_1	Q_0	D_0	Q_3*	Shift to MSB
L	H	L	L	L	L	X	↗	(Q_{0-3}) minus 1				①	Count Down
L	H	L	L	H	L	X	X	Q_3	Q_2	Q_1	Q_0	①	Count Down with $\overline{CEP}$ not active
L	H	L	L	X	H	X	X	Q_3	Q_2	Q_1	Q_0	H	Count Down with $\overline{CET}$ not active
L	H	L	H	X	X	X	↗	L	L	L	L	H	Clear
L	H	H	L	L	L	X	↗	(Q_{0-3}) plus 1				②	Count Up
L	H	H	L	H	L	X	X	Q_3	Q_2	Q_1	Q_0	②	Count Up with $\overline{CEP}$ not active
L	H	H	L	X	H	X	X	Q_3	Q_2	Q_1	Q_0	H	Count Up with $\overline{CET}$ not active
L	H	H	H	X	X	X	X	Q_3	Q_2	Q_1	Q_0	H	Hold
H	L	L	L	X	X	X	X	L	L	L	L	L	Asynchronous Master Reset
H	L	L	H	X	X	X	X	L	L	L	L	L	
H	L	H	L	X	X	X	X	L	L	L	L	L	
H	L	H	H	X	X	X	X	L	L	L	L	L	
H	H	L	L	X	L	X	X	L	L	L	L	L	
H	H	L	L	X	H	X	X	L	L	L	L	H	
H	H	L	H	X	X	X	X	L	L	L	L	H	
H	H	H	L	X	X	X	X	L	L	L	L	H	
H	H	H	H	X	X	X	X	L	L	L	L	H	

① = L if Q_0–Q_3 = LLLL
H if Q_0–$Q_3 \neq$ LLLL

② = L if Q_0–Q_3 = HHHH
H if Q_0–$Q_3 \neq$ HHHH

H = HIGH Voltage Level

L = LOW Voltage Level

X = Don't Care

↗ = LOW-to-HIGH Transition

*Before the clock, $\overline{TC}$ is Q_3
After the clock, $\overline{TC}$ is Q_2

Absolute Maximum Ratings

Above which the useful life may be impaired. (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature (T_{STG})	−65°C to +150°C
Maximum Junction Temperature (T_J)	
Ceramic	+175°C
Plastic	+150°C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Output Current (DC Output HIGH)	−50 mA
ESD (Note 2)	≥2000V

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: ESD testing conforms to MIL-STD-883, Method 3015.

Recommended Operating Conditions

Case Temperature (T_C)	
Commercial	0°C to +85°C
Industrial	−40°C to +85°C
Military	−55°C to +125°C
Supply Voltage (V_{EE})	−5.7V to −4.2V

Commercial Version

DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions	
V_{OH}	Output HIGH Voltage	−1025	−955	−870	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830	−1705	−1620	mV		
V_{OHC}	Output HIGH Voltage	−1035			mV	V_{IN} = $V_{IH(Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610	mV		
V_{IH}	Input HIGH Voltage	−1165		−870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1830		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = V_{IL} (Min)	
I_{IH}	Input HIGH Current			240	μA	V_{IN} = V_{IH} (Max)	
I_{EE}	Power Supply Current	−165		−80		Inputs Open	

Note 3: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

Commercial Version (Continued)

DIP AC Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
f_{shift}	Shift Frequency	300		300		300		MHz	*Figures 2* and *3*
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n, $\overline{Q}_n$	1.00	2.00	1.00	2.00	1.00	2.00	ns	*Figures 1* and *3* (Note 1)
t_{PLH} t_{PHL}	Propagation Delay CP to $\overline{TC}$ (Shift)	2.10	3.50	2.10	3.50	2.10	3.70	ns	*Figures 1, 7, 8* (Note 1)
t_{PLH} t_{PHL}	Propagation Delay CP to $\overline{TC}$ (Count)	2.40	4.40	2.40	4.40	2.60	4.70	ns	*Figures 1* and *9* (Note 1)
t_{PLH} t_{PHL}	Propagation Delay MR to Q_n, $\overline{Q}_n$	1.40	2.50	1.40	2.50	1.50	2.60	ns	*Figures 1* and *4* (Note 1)
t_{PLH} t_{PHL}	Propagation Delay MR to $\overline{TC}$ (Count)	2.80	5.10	2.90	5.20	3.10	5.50	ns	*Figures 1, 12* (Note 1)
t_{PHL}	Propagation Delay MR to $\overline{TC}$ (Shift)	2.40	4.00	2.40	4.00	2.50	4.10	ns	*Figures 1, 10, 11* (Note 1)
t_{PLH} t_{PHL}	Propagation Delay $D_0/\overline{CET}$ to $\overline{TC}$	1.80	3.10	1.80	3.10	1.90	3.30	ns	*Figures 1* and *5* (Note 1)
t_{PLH} t_{PHL}	Propagation Delay S_n to $\overline{TC}$	1.90	4.10	1.90	4.10	2.10	4.40	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.35	1.20	0.35	1.20	0.35	1.20	ns	*Figures 1* and *3*
t_S	Setup Time								
	D_3	1.00		1.00		1.00			
	P_n	1.50		1.50		1.50			
	$D_0/\overline{CET}$	1.30		1.30		1.30		ns	*Figures 6* and *4*
	$\overline{CEP}$	1.40		1.40		1.40			
	S_n	3.40		3.40		3.40			
	MR (Release Time)	2.60		2.60		2.60			
t_H	Hold Time								
	D_3	0.40		0.40		0.40			
	P_n	0.30		0.30		0.30			
	$D_0/\overline{CET}$	0.30		0.30		0.30		ns	*Figure 6*
	$\overline{CEP}$	0.20		0.20		0.20			
	S_n	0.10		0.10		0.10			
$t_{pw}(H)$	Pulse Width HIGH CP, MR	2.00		2.00		2.00		ns	*Figures 3* and *4*

Note 1: The propagation delay specified is for single output switching. Delays may vary up to 250 ps with multiple outputs switching.

Commercial Version (Continued)

SOIC, PCC and Cerpak AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
f_{shift}	Shift Frequency	350		350		350		MHz	*Figures 2* and *3*
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n, $\overline{Q}_n$	1.00	1.80	1.00	1.80	1.00	1.80	ns	*Figures 1* and *2* (Note 2)
t_{PLH} t_{PHL}	Propagation Delay CP to $\overline{TC}$ (Shift)	2.10	3.30	2.10	3.30	2.10	3.50	ns	*Figures 1, 7, 8* (Note 2)
t_{PLH} t_{PHL}	Propagation Delay CP to $\overline{TC}$ (Count)	2.40	4.20	2.40	4.20	2.60	4.50	ns	*Figures 1* and *9* (Note 2)
t_{PLH} t_{PHL}	Propagation Delay MR to Q_n, $\overline{Q}_n$	1.40	2.30	1.40	2.30	1.50	2.40	ns	*Figures 1* and *4* (Note 2)
t_{PLH} t_{PHL}	Propagation Delay MR to $\overline{TC}$ (Count)	2.80	4.90	2.90	5.00	3.10	5.30	ns	*Figures 1* and *12* (Note 2)
t_{PHL}	Propagation Delay MR to $\overline{TC}$ (Shift)	2.40	3.80	2.40	3.80	2.50	3.90	ns	*Figures 1, 10, 11* (Note 2)
t_{PLH} t_{PHL}	Propagation Delay $D_0/\overline{CET}$ to $\overline{TC}$	1.80	2.90	1.80	2.90	1.90	3.10	ns	*Figures 1* and *5* (Note 2)
t_{PLH} t_{PHL}	Propagation Delay S_n to $\overline{TC}$	1.90	3.90	1.90	3.90	2.10	4.20	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.35	1.10	0.35	1.10	0.35	1.10	ns	*Figures 1* and *3*
t_S	Setup Time D_3 P_n $D_0/\overline{CET}$ $\overline{CEP}$ S_n MR (Release Time)	 0.90 1.40 1.20 1.30 3.30 2.50		 0.90 1.40 1.20 1.30 3.30 2.50		 0.90 1.40 1.20 1.30 3.30 2.50		ns	*Figures 4* and *6*
t_H	Hold Time D_3 P_n $D_0/\overline{CET}$ $\overline{CEP}$ S_n	 0.30 0.20 0.20 0.10 0.00		 0.30 0.20 0.20 0.10 0.00		 0.30 0.20 0.20 0.10 0.00		ns	*Figure 6*
$t_{pw}(H)$	Pulse Width HIGH CP, MR	2.00		2.00		2.00		ns	*Figures 3* and *4*
t_{OSHL}	Maximum Skew Common Edge Output-to-Output Variation Clock to Output Path		200		200		200	ps	PCC Only (Note 1)
t_{OSLH}	Maximum Skew Common Edge Output-to-Output Variation Clock to Output Path		200		200		200	ps	PCC Only (Note 1)
t_{OST}	Maximum Skew Opposite Edge Output-to-Output Variation Clock to Output Path		230		230		230	ps	PCC Only (Note 1)
t_{ps}	Maximum Skew Pin (Signal) Transition Variation Clock to Output Path		245		245		245	ps	PCC Only (Note 1)

Note 1: Output-to-Output Skew is defined as the absolute value of the difference between the actual propagation delay for any outputs within the same packaged device. The specifications apply to any outputs switching in the same direction either HIGH to LOW (t_{OSHL}), or LOW to HIGH (t_{OSLH}), or in opposite directions both HL and LH (t_{OST}). Parameters t_{OST} and t_{ps} guaranteed by design

Note 2: The propagation delay specified is for single output switching. Delays may vary up to 250 ps with multiple outputs switching.

Industrial Version

PCC DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = −40°C to +85°C (Note 1)

Symbol	Parameter	T_C = −40°C		T_C = 0°C to +85°C		Units	Conditions	
		Min	Max	Min	Max			
V_{OH}	Output HIGH Voltage	−1085	−870	−1025	−870	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830	−1575	−1830	−1620	mV		
V_{OHC}	Output HIGH Voltage	−1095		−1035		mV	V_{IN} = $V_{IH(Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage		−1565		−1610	mV		
V_{IH}	Input HIGH Voltage	−1170	−870	−1165	−870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1830	−1480	−1830	−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50		0.50		μA	V_{IN} = V_{IL} (Min)	
I_{IH}	Input HIGH Current		240		240	μA	V_{IN} = V_{IH} (Max)	
I_{EE}	Power Supply Current	−165	−75	−165	−80	mA	Inputs Open	

Note 1: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

Industrial Version (Continued)

PCC AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = −40°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
f_{shift}	Shift Frequency	325		350		350		MHz	*Figures 2* and *3*
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n, $\overline{Q}_n$	1.00	1.80	1.00	1.80	1.00	1.80	ns	*Figures 1* and *3* (Note 1)
t_{PLH} t_{PHL}	Propagation Delay CP to $\overline{TC}$ (Shift)	2.00	3.30	2.10	3.30	2.10	3.50	ns	*Figures 1, 7, 8* (Note 1)
t_{PLH} t_{PHL}	Propagation Delay CP to $\overline{TC}$ (Count)	2.40	4.20	2.40	4.20	2.60	4.50	ns	*Figures 1* and *9* (Note 1)
t_{PLH} t_{PHL}	Propagation Delay MR to Q_n, $\overline{Q}_n$	1.40	2.30	1.40	2.30	1.50	2.40	ns	*Figures 1* and *4* (Note 1)
t_{PLH} t_{PHL}	Propagation Delay MR to $\overline{TC}$ (Count)	2.80	4.90	2.90	5.00	3.10	5.30	ns	*Figures 1 and 12* (Note 1)
t_{PHL}	Propagation Delay MR to $\overline{TC}$ (Shift)	2.40	3.80	2.40	3.80	2.50	3.90	ns	*Figures 1, 10, 11* (Note 1)
t_{PLH} t_{PHL}	Propagation Delay $D_0/\overline{CET}$ to $\overline{TC}$	1.70	2.90	1.80	2.90	1.90	3.10	ns	*Figures 1* and *5* (Note 1)
t_{PLH} t_{PHL}	Propagation Delay S_n to $\overline{TC}$	1.80	3.90	1.90	3.90	2.10	4.20	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.20	1.90	0.35	1.10	0.35	1.10	ns	*Figures 1* and *3*
t_s	Setup Time								
	D_3	1.40		0.90		0.90			
	P_n	1.70		1.40		1.40			
	$D_0/\overline{CET}$	1.80		1.20		1.20		ns	*Figure 6*
	$\overline{CEP}$	1.80		1.30		1.30			
	S_n	3.30		3.30		3.30			
	MR (Release Time)	2.60		2.50		2.50			
t_h	Hold Time								
	D_3	0.90		0.30		0.30			
	P_n	1.00		0.20		0.20			
	$D_0/\overline{CET}$	0.70		0.20		0.20		ns	*Figure 6*
	$\overline{CEP}$	0.60		0.10		0.10			
	S_n	0.00		0.00		0.00			
$t_{pw}(H)$	Pulse Width HIGH CP, MR	2.20		2.00		2.00		ns	*Figures 3* and *4*

Note 1: The propagation delay specified is for single output switching. Delays may vary up to 250 ps with multiple outputs switching.

Military Version

DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = −55°C to +125°C

Symbol	Parameter	Min	Max	Units	T_C	Conditions		Notes
V_{OH}	Output HIGH Voltage	−1025	−870	mV	0°C to +125°C	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V	1, 2, 3
		−1085	−870	mV	−55°C			
V_{OL}	Output LOW Voltage	−1830	−1620	mV	0°C to +125°C			
		−1830	−1555	mV	−55°C			
V_{OHC}	Output HIGH Voltage	−1035		mV	0°C to +125°C	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V	1, 2, 3
		−1085		mV	−55°C			
V_{OLC}	Output LOW Voltage		−1610	mV	0°C to +125°C			
			−1555	mV	−55°C			
V_{IH}	Input HIGH Voltage	−1165	−870	mV	−55°C to +125°C	Guaranteed HIGH Signal for All Inputs		1, 2, 3, 4
V_{IL}	Input LOW Voltage	−1830	−1475	mV	−55°C to +125°C	Guaranteed LOW Signal for All Inputs		1, 2, 3, 4
I_{IL}	Input LOW Current	0.50		µA	−55°C to +125°C	V_{EE} = −4.2V V_{IN} = $V_{IL\ (Min)}$		1, 2, 3
I_{IH}	Input HIGH Current		240	µA	0°C to +125°C	V_{EE} = −5.7V V_{IN} = $V_{IH(Max)}$		1, 2, 3
			340	µA	−55°C			
I_{EE}	Power Supply Current	−185 −195	−70 −70	mA	−55°C to +125°C	Inputs Open V_{EE} = −4.2V to −4.8V V_{EE} = −4.2V to −5.7V		1, 2, 3

Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals −55°C), then testing immediately without allowing for the junction temperature to stablize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 2: Screen tested 100% on each device at −55°C, +25°C, and +125°C, Subgroups 1, 2, 3, 7, and 8.

Note 3: Sample tested (Method 5005, Table I) on each manufactured lot at −55°C, +25°C, +125°C, Subgroups A1, 2, 3, 7, and 8.

Note 4: Guaranteed by applying specified input conditon and testing V_{OH}/V_{OL}.

Military Version (Continued)

AC Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = −55°C		T_C = +25°C		T_C = +125°		Units	Conditions	Notes
		Min	Max	Min	Max	Min	Max			
f_{shift}	Shift Frequency	325		325		325		MHz	*Figures 2* and *3*	4
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n, $\overline{Q}_n$	0.40	2.30	0.50	2.20	0.40	2.50	ns	*Figures 1* and *3*	1, 2, 3, 5
t_{PLH} t_{PHL}	Propagation Delay CP to $\overline{TC}$ (Shift)	1.30	3.90	1.70	3.80	1.70	4.20	ns	*Figures 1, 7, 8*	
t_{PLH} t_{PHL}	Propagation Delay CP to $\overline{TC}$ (Count)	1.20	4.60	1.50	4.60	1.60	5.20	ns	*Figures 1* and *9*	1, 2, 3, 5
t_{PLH} t_{PHL}	Propagation Delay MR to Q_n, $\overline{Q}_n$	0.60	2.90	0.80	2.80	0.90	3.20	ns	*Figures 1* and *4*	1, 2, 3, 5
t_{PLH} t_{PHL}	Propagation Delay MR to $\overline{TC}$ (Count)	2.30	5.20	2.70	5.20	2.90	5.90	ns	*Figures 1, 12*	
t_{PHL}	Propagation Delay MR to $\overline{TC}$ (Shift)	2.10	4.30	2.20	4.10	2.40	4.70	ns	*Figures 1, 10, 11*	1, 2, 3, 5
t_{PLH} t_{PHL}	Propagation Delay $D_0/\overline{CET}$ to $\overline{TC}$	0.70	3.20	1.00	3.20	1.30	4.10	ns	*Figures 1* and *5*	1, 2, 3, 5
t_{PLH} t_{PHL}	Propagation Delay S_n to $\overline{TC}$	1.30	4.10	1.50	4.20	1.70	4.90	ns		
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.20	1.90	0.20	1.80	0.20	2.00	ns	*Figures 1* and *3*	4
t_s	Setup Time									
	D_3	1.40		1.40		1.40				
	P_n	1.70		1.70		1.70				
	$D_0/\overline{CET}$	1.80		1.80		1.80		ns	*Figure 6*	4
	$\overline{CEP}$	1.80		1.80		1.80				
	S_n	3.30		3.30		3.30				
	MR (Release Time)	2.60		2.60		2.60				
t_h	Hold Time									
	D_3	0.90		0.90		0.90				
	P_n	1.00		1.00		1.00				
	$D_0/\overline{CET}$	0.70		0.70		0.70		ns	*Figure 6*	4
	$\overline{CEP}$	0.60		0.60		0.60				
	S_n	0.00		0.00		0.00				
$t_{pw}(H)$	Pulse Width HIGH CP	1.60		1.60		1.60		ns	*Figures 3* and *4*	4
	MR	2.00		2.00		2.00				

Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals −55°C), then testing immediately after power-up. This provides "cold start" specs which can be considered a worst case condition at cold tempertures.

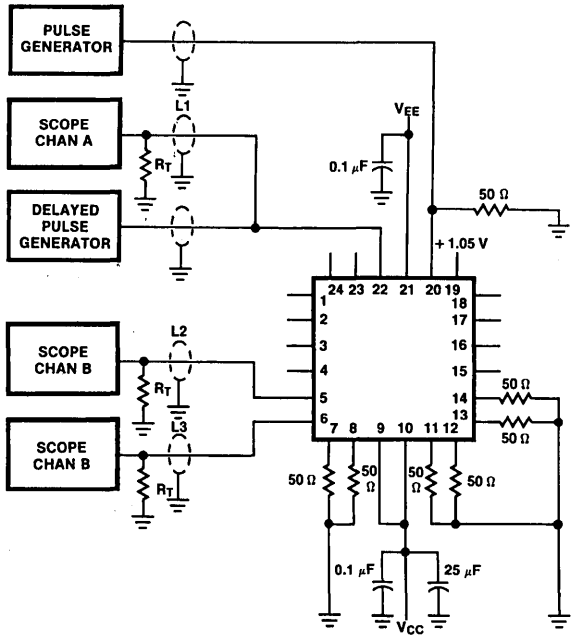
Note 2: Screen tested 100% on each device at +25°C temperature only, Subgroups A9.

Note 3: Sample tested (Method 5005, Table I) on each manufactured lot at +25°C, Subgroups A9, and at +125°C and −55°C temperatures, Subgroups A10 and A11.

Note 4: Not tested at +25°C, +125°C, and −55°C temperature (design characterization data).

Note 5: The propagation delay specified is for single output switching. Delays may vary up to 250 ps with multiple outputs switching.

Test Circuitry



Notes:

V_{CC}, V_{CCA} = +2V, V_{EE} = −2.5V

L1, L2 and L3 = equal length 50Ω impedance lines

R_T = 50Ω terminator internal to scope

Decoupling 0.1 μF from GND to V_{CC} and V_{EE}

All unused outputs are loaded with 50Ω to GND

C_L = Fixture and stray capacitance ≤ 3 pF

Pin numbers shown are for flatpak; for DIP see logic symbol

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FIGURE 1. AC Test Circuit

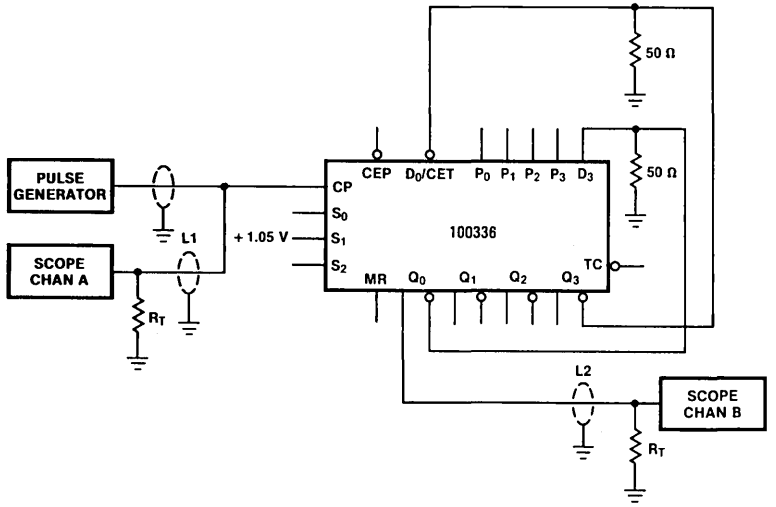

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FIGURE 2. Shift Frequency Test Circuit (Shift Left)

Notes:

For shift right mode, +1.05V is applied at S_0.

The feedback path from output to input should be as short as possible.

Switching Waveforms

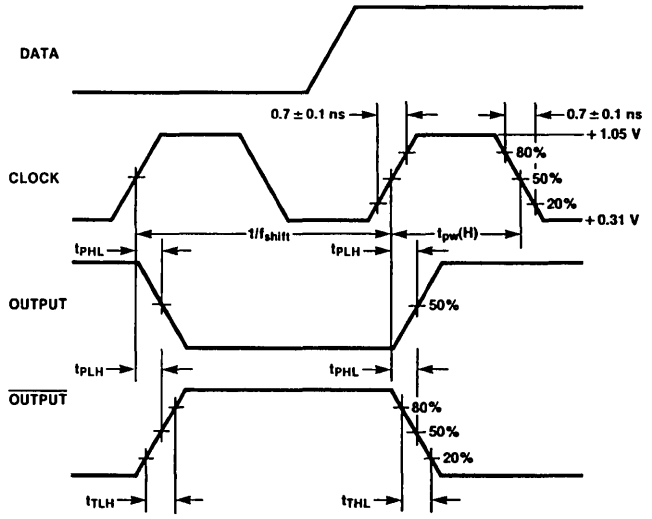

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FIGURE 3. Propagation Delay (Clock) and Transition Times

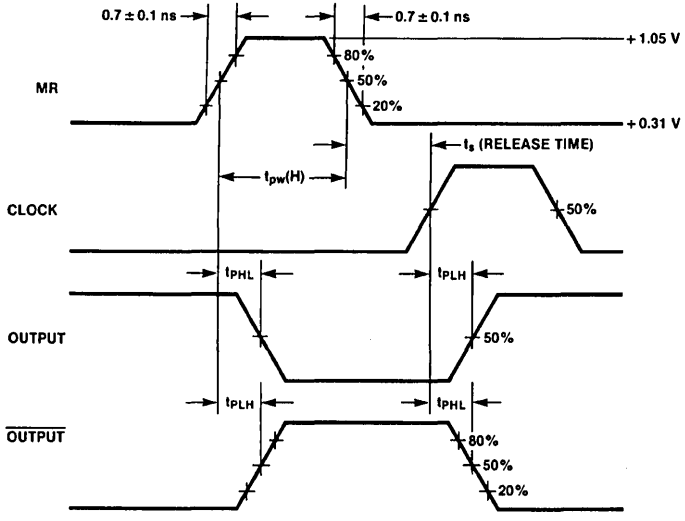

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FIGURE 4. Propagation Delay (Reset)

Switching Waveforms (Continued)

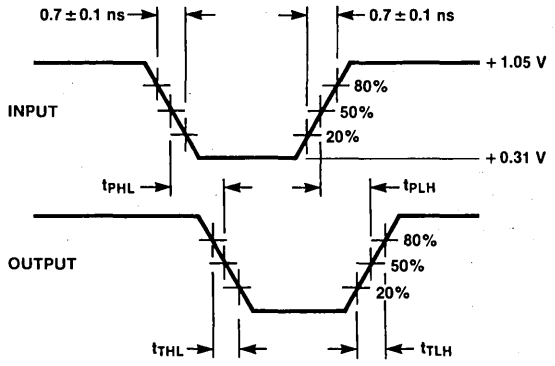

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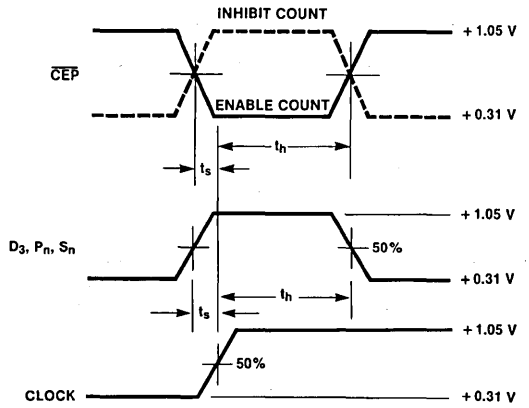
FIGURE 5. Propagation Delay (Serial Data, Selects)



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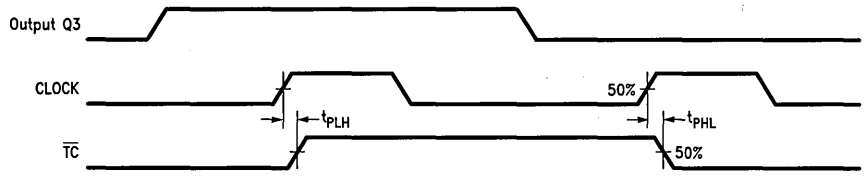
Notes:

t_s is the minimum time before the transition of the clock that information must be present at the data input.
t_h is the minimum time after the transition of the clock that information must remain unchanged at the data input.

FIGURE 6. Setup and Hold Time



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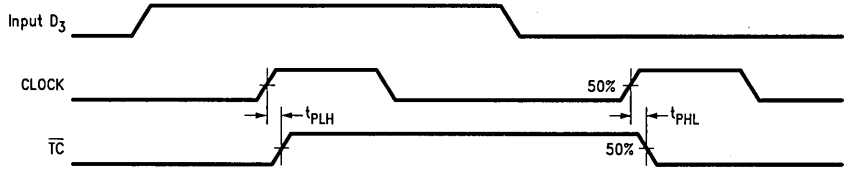
Note: Shift Right Mode; S_0 = H, S_1 = H, S_2 = L.

FIGURE 7. Propagation Delay, Clock to Terminal Count (Shift Right Mode)

Switching Waveforms (Continued)



Note: Shift Left Mode; S_0 = L, S_1 = H, S_2 = L.

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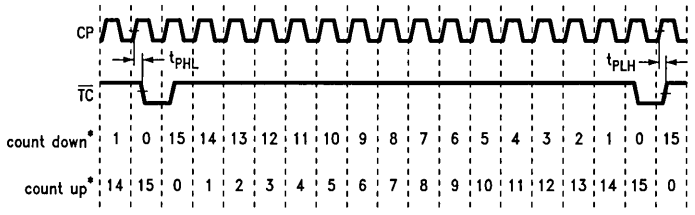
FIGURE 8. Propagation Delay, Clock to Terminal Count (Shift Left Mode)



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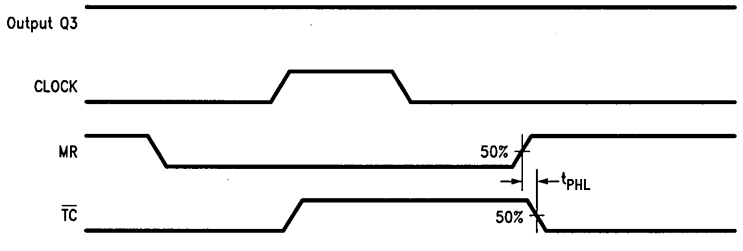
Note:

*Decimal representation of binary outputs.

Count Up: S_0 = L, S_1 = H, S_2 = H; Count Down: S_0 = L, S_1 = L, S_2 = H.

Measurement taken at 50% point of waveform.

FIGURE 9. Propagation Delay, Clock to Terminal Count (Count Up and Count Down Modes)



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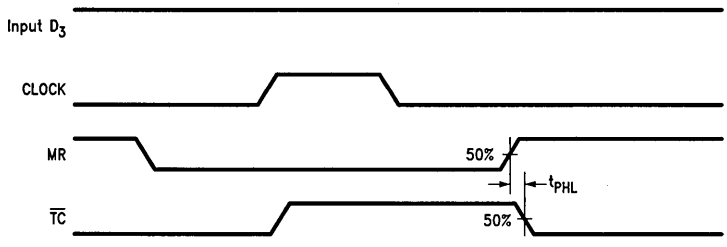
Note: Shift Right Mode; S_0 = H, S_1 = H, S_2 = L.

FIGURE 10. Propagation Delay, Master Reset to Terminal Count (Shift Right Mode)

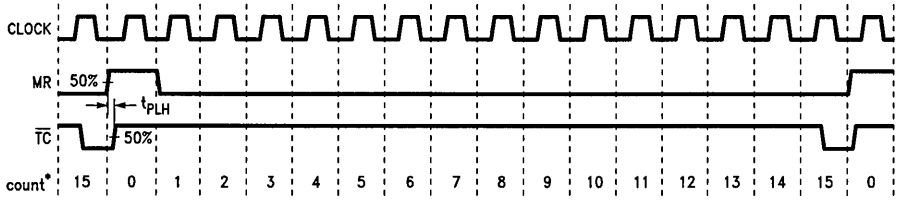
Switching Waveforms (Continued)



TL/F/10584–19

Note: Shift Left Mode; S_0 = L, S_1 = H, S_2 = L.

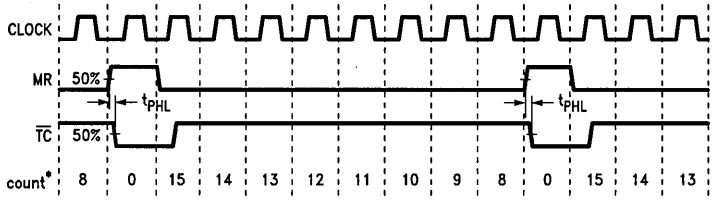
FIGURE 11. Propagation Delay, Master Reset to Terminal Count (Shift Left Mode)



TL/F/10584–20

Note:

*Decimal representation of binary outputs. Count Up Mode: S_0 = L, S_1 = H, S_2 = H.



TL/F/10584–21

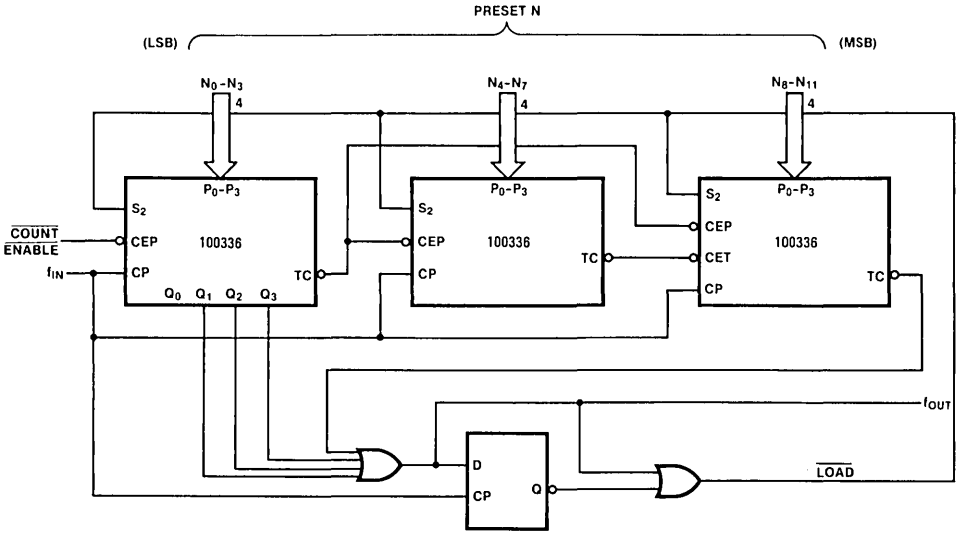
Note:

*Decimal representation of binary outputs. Count Down Mode: S_0 = L, S_1 = L, S_2 = H.

FIGURE 12. Propagation Delay, Master Reset to Terminal Count (Count Up and Count Down Modes)

Applications

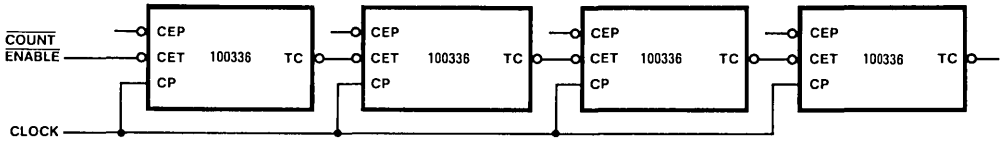
3-Stage Divider, Preset Count Down Mode



Note: If $S_0 = S_1 = S_2$ = LOW, then T_C = LOW

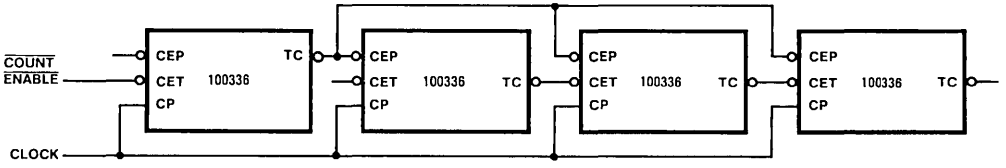
TL/F/10584–12

Slow Expansion Scheme



TL/F/10584–13

Fast Expansion Scheme



TL/F/10584–14

National Semiconductor

100341
Low Power 8-Bit Shift Register

General Description

The 100341 contains eight edge-triggered, D-type flip-flops with individual inputs (P_n) and outputs (Q_n) for parallel operation, and with serial inputs (D_n) and steering logic for bidirectional shifting. The flip-flops accept input data a setup time before the positive-going transition of the clock pulse and their outputs respond a propagation delay after this rising clock edge.

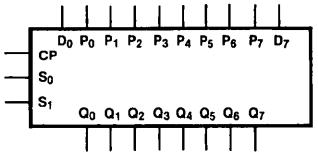
The circuit operating mode is determined by the Select inputs S_0 and S_1, which are internally decoded to select either "parallel entry", "hold", "shift left" or "shift right" as described in the Truth Table. All inputs have 50 kΩ pull-down resistors.

Features

- 35% power reduction of the 100141
- 2000V ESD protection
- Pin/function compatible with 100141
- Voltage compensated operating range = −4.2V to −5.7V
- Available to industrial grade temperature range

Ordering Code: See Section 6

Logic Symbol

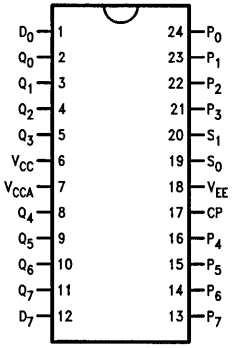


TL/F/9880–1

Pin Names	Description
CP	Clock Input
S_0, S_1	Select Inputs
D_0, D_7	Serial Inputs
P_0–P_7	Parallel Inputs
Q_0–Q_7	Data Outputs

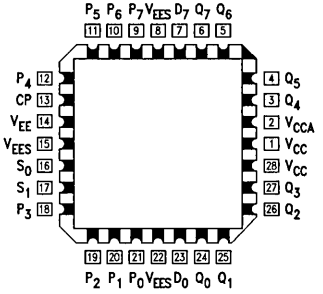
Connection Diagrams

24-Pin DIP/SOIC



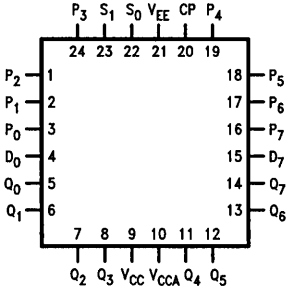
TL/F/9880–2

28-Pin PCC



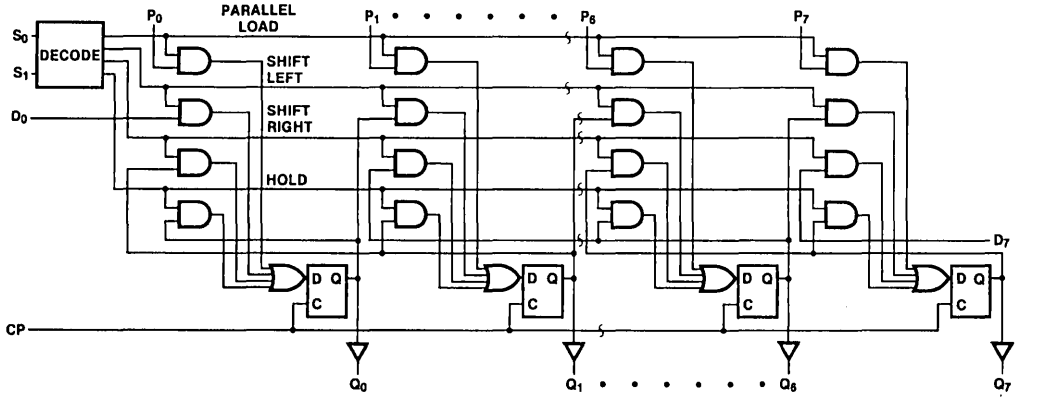
TL/F/9880–4

24-Pin Quad Cerpak



TL/F/9880–3

Logic Diagram



TL/F/9880–5

Truth Table

Function	Inputs					Outputs							
	D_7	D_0	S_1	S_0	CP	Q_7	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1	Q_0
Load Register	X	X	L	L	↗	P_7	P_6	P_5	P_4	P_3	P_2	P_1	P_0
Shift Left	X	L	L	H	↗	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1	Q_0	L
Shift Left	X	H	L	H	↗	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1	Q_0	H
Shift Right	L	X	H	L	↗	L	Q_7	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1
Shift Right	H	X	H	L	↗	H	Q_7	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1
Hold	X	X	H	H	X	No Change							
Hold	X	X	X	X	H								
Hold	X	X	X	X	L								

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
↗ = LOW-to-HIGH Transition

Absolute Maximum Ratings

Above which the useful life may be impaired (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature (T_{STG})	−65°C to +150°C
Maximum Junction Temperature (T_J)	
Ceramic	+175°C
Plastic	+150°C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Output Current (DC Output HIGH)	−50 mA
ESD (Note 2)	≥2000V

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: ESD testing conforms to MIL-STD-883, Method 3015.

Recommended Operating Conditions

Case Temperature (T_C)	
Commercial	0°C to +85°C
Industrial	−40°C to +85°C
Military	−55°C to +125°C
Supply Voltage (V_{EE})	−5.7V to −4.2V

Commercial Version

DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions	
V_{OH}	Output HIGH Voltage	−1025	−955	−870	mV	V_{IN} = V_{IH} (Max) or V_{IL} (Min)	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830	−1705	−1620	mV		
V_{OHC}	Output HIGH Voltage	−1035			mV	V_{IN} = V_{IH} (Min) or V_{IL} (Max)	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610	mV		
V_{IH}	Input HIGH Voltage	−1165		−870	mV	Guaranteed HIGH Signal for all Inputs	
V_{IL}	Input LOW Voltage	−1830		−1475	mV	Guaranteed LOW Signal for all Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = V_{IL} (Min)	
I_{IH}	Input HIGH Current			240	μA	V_{IN} = V_{IH} (Max)	
I_{EE}	Power Supply Current					Inputs Open	
		−157		−75	mA	V_{EE} = −4.2V to −4.8V	
		−167		−75	mA	V_{EE} = −4.2V to −5.7V	

Note 3: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

Commercial Version (Continued)

DIP AC Electrical Characteristics V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
f_{max}	Max Clock Frequency	400		400		400		MHz	*Figures 2* and *3*
t_{PLH} t_{PHL}	Propagation Delay CP to Output	0.90	1.90	1.00	2.00	1.00	2.10	ns	*Figures 1* and *3* (Note 1)
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.35	1.30	0.35	1.30	0.35	1.30	ns	*Figures 1* and *3*
t_S	Setup Time D_n, P_n S_n	 0.65 1.60		 0.65 1.60		 0.65 1.60		ns	*Figure 4*
t_H	Hold D_n, P_n S_n	 0.80 0.60		 0.80 0.60		 0.80 0.60		ns	
t_{pw}(H)	Pulse Width HIGH CP	2.00		2.00		2.00		ns	*Figure 3*

Note 1: The propagation delay specified is for the switching of a single output. Delays may vary up to 0.40 ns if multiple outputs are switching simultaneously.

SOIC, PCC and Cerpak AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
f_{max}	Max Clock Frequency	425		425		425		MHz	*Figures 2* and *3*
t_{PLH} t_{PHL}	Propagation Delay CP to Output	0.90	1.70	1.00	1.80	1.00	1.90	ns	*Figures 1* and *3* (Note 2)
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.35	1.20	0.35	1.20	0.35	1.20	ns	*Figures 1* and *3*
t_S	Setup Time D_n, P_n S_n	 0.55 1.50		 0.55 1.50		 0.55 1.50		ns	*Figure 4*
t_H	Hold Time D_n, P_n S_n	 0.70 0.50		 0.70 0.50		 0.70 0.50		ns	
t_{pw}(H)	Pulse Width HIGH CP	2.00		2.00		2.00		ns	*Figure 3*
t_{OSHL}	Maximum Skew Common Edge Output-to-Output Variation Clock to Output Path		200		200		200	ps	PCC Only (Note 1)
t_{OSLH}	Maximum Skew Common Edge Output-to-Output Variation Clock to Output Path		200		200		200	ps	PCC Only (Note 1)
t_{OST}	Maximum Skew Opposite Edge Output-to-Output Variation Clock to Output Path		250		250		250	ps	PCC Only (Note 1)
t_{ps}	Maximum Skew Pin (Signal) Transition Variation Clock to Output Path		250		250		250	ps	PCC Only (Note 1)

Note 1: Output-to-Output Skew is defined as the absolute value of the difference between the actual propagation delay for any outputs within the same packaged device. The specifications apply to any outputs switching in the same direction either HIGH to LOW (t_{OSHL}), or LOW to HIGH (t_{OSLH}), or in opposite directions both HL and LH (t_{OST}). Parameters t_{OST} and t_{ps} guaranteed by design

Note 2: The propagation delay specified is for the switching of a single output. Delays may vary up to 0.40 ns if multiple outputs are switching simultaneously.

Industrial Version

PCC DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = −40°C to +85°C (Note 1)

Symbol	Parameter	T_C = −40°C		T_C = 0°C to +85°C		Units	Conditions	
		Min	Max	Min	Max			
V_{OH}	Output HIGH Voltage	−1085	−870	−1025	−870	mV	V_{IN} = V_{IH}(Max) or V_{IL} (Min)	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830	−1575	−1830	−1620	mV		
V_{OHC}	Output HIGH Voltage	−1095		−1035		mV	V_{IN} = V_{IH} (Min) or V_{IL} (Max)	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage		−1565		−1610	mV		
V_{IH}	Input HIGH Voltage	−1170	−870	−1165	−870	mV	Guaranteed HIGH Signal for all Inputs	
V_{IL}	Input LOW Voltage	−1830	−1480	−1830	−1475	mV	Guaranteed LOW Signal for all Inputs	
I_{IL}	Input LOW Current	0.50		0.50		μA	V_{IN} = V_{IL} (Min)	
I_{IH}	Input HIGH Current		240		240	μA	V_{IN} = V_{IH} (Max)	
I_{EE}	Power Supply Current						Inputs Open	
		−157	−75	−157	−75	mA	V_{EE} = −4.2V to −4.8V	
		−167	−75	−167	−75	mA	V_{EE} = −4.2V to −5.7V	

Note 1: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

Industrial Version (Continued)

PCC AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = −40°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
f_{max}	Max Clock Frequency	425		425		425		MHz	*Figures 2* and *3*
t_{PLH} t_{PHL}	Propagation Delay CP to Output	0.90	1.80	1.00	1.80	1.00	1.90	ns	*Figures 1* and *3* (Note 1)
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.30	1.90	0.35	1.20	0.35	1.20	ns	*Figures 1* and *3*
t_s	Setup Time D_n, P_n S_n	0.60 1.70		0.55 1.50		0.55 1.50		ns	*Figure 4*
t_h	Hold Time D_n, P_n S_n	0.90 0.50		0.70 0.50		0.70 0.50		ns	*Figure 4*
t_{pw}(H)	Pulse Width HIGH CP	2.00		2.00		2.00		ns	*Figure 3*

Note 1: The propagation delay specified is for the switching of a single output. Delays may vary up to 0.40 ns if multiple outputs are switching simultaneously.

Military Version

DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = −55°C to +125°C

Symbol	Parameter	Min	Max	Units	T_C	Conditions		Notes
V_{OH}	Output HIGH Voltage	−1025	−870	mV	0°C to +125°C	V_{IN} = V_{IH} (Max) or V_{IL} (Min)	Loading with 50Ω to −2.0V	1, 2, 3
		−1085	−870	mV	−55°C			
V_{OL}	Output LOW Voltage	−1830	−1620	mV	0°C to +125°C			
		−1830	−1555	mV	−55°C			
V_{OHC}	Output HIGH Voltage	−1035		mV	0°C to +125°C	V_{IN} = V_{IH} (Min) or V_{IL} (Max)	Loading with 50Ω to −2.0V	1, 2, 3
		−1085		mV	−55°C			
V_{OLC}	Output LOW Voltage		−1610	mV	0°C to +125°C			
			−1555	mV	−55°C			
V_{IH}	Input HIGH Voltage	−1165	−870	mV	−55°C to +125°C	Guaranteed HIGH Signal for All Inputs		1, 2, 3, 4
V_{IL}	Input LOW Current	−1830	−1475	mV	−55°C to +125°C	Guaranteed LOW Signal for All Inputs		1, 2, 3, 4
I_{IL}	Input LOW Current	0.50		μA	−55°C to +125°C	V_{EE} = −4.2V V_{IN} = V_{IL} (Min)		1, 2, 3
I_{IH}	Input High Current		240	μA	0°C to +125°C	V_{EE} = −5.7V V_{IN} = V_{IH} (Max)		1, 2, 3
			340	μA	−55°C			
I_{EE}	Power Supply Current	−168 −178	−55 −55	mA mA	−55°C to +125°C	Inputs Open V_{EE} = −4.2V to −4.8V V_{EE} = −4.2V to −5.7V		1, 2, 3

Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals −55°C), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specifications which can be considered a worst case condition at cold temperatures.

Note 2: Screen tested 100% on each device at −55°C, +25°C and +125°C, Subgroups 1, 2, 3, 7, and 8.

Note 3: Sample tested (Method 5005, Table I) on each manufactured lot at −55°C, +25°C, and +125°C, Subgroups A1, 2, 3, 7, and 8.

Note 4: Guaranteed by applying specified input condition and testing V_{OH}/V_{OL}.

Military Version (Continued)

AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = −55°C		T_C = +25°C		T_C = +125°C		Units	Conditions	Notes
		Min	Max	Min	Max	Min	Max			
f_{max}	Max Clock Frequency	400		400		300		MHz	*Figures 2* and *3*	4
t_{PLH} t_{PHL}	Propagation Delay CP to Output	0.50	2.50	0.70	2.30	0.70	2.80	ns	*Figures 1* and *3*	1, 2, 3, 5
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.30	1.90	0.30	1.80	0.30	1.90	ns		
t_s	Setup Time D_n, P_n S_n	0.60 1.70		0.60 1.60		0.60 2.40		ns	*Figure 4*	4
t_h	Hold Time D_n, P_n S_n	0.90 0.50		0.90 0.50		0.90 0.50		ns		
t_{pw}(H)	Pulse Width HIGH CP	2.00		2.00		2.00		ns	*Figure 3*	

Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals −55°C), then testing immediately after power-up. This provides "cold start" specifications which can be considered a worst case condition at cold temperatures.

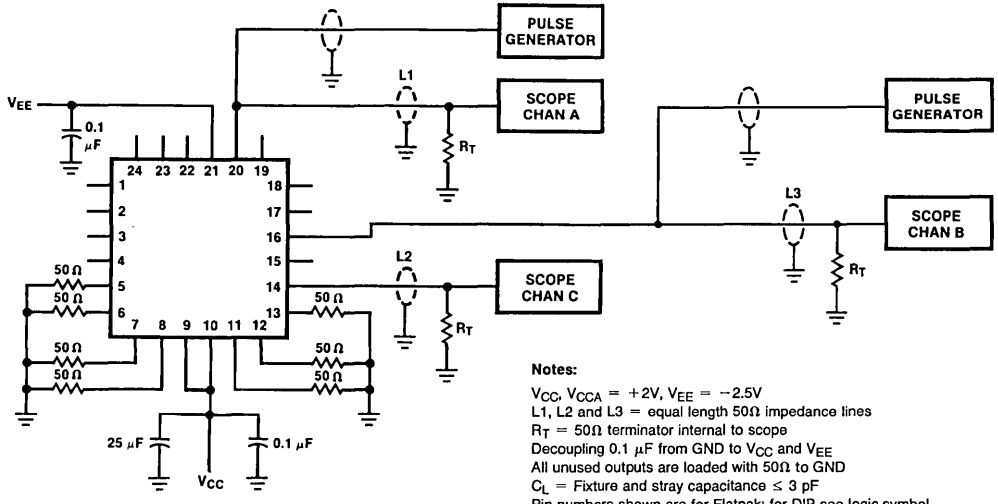
Note 2: Screen tested 100% on each device at +25°C temperature only, Subgroup A9.

Note 3: Sample tested (Method 5005, Table 1) on each manufactured lot at +25°C, Subgroup A9, and at +125°C and −55°C temperatures, Subgroups A10 and A11.

Note 4: Not tested at +25°C, +125°C and −55°C temperature (design characterization data).

Note 5: The propagation delay specified is for the switching of a single output. Delays may vary up to 0.40 ns if multiple outputs are switching simultaneously.

Test Circuitry

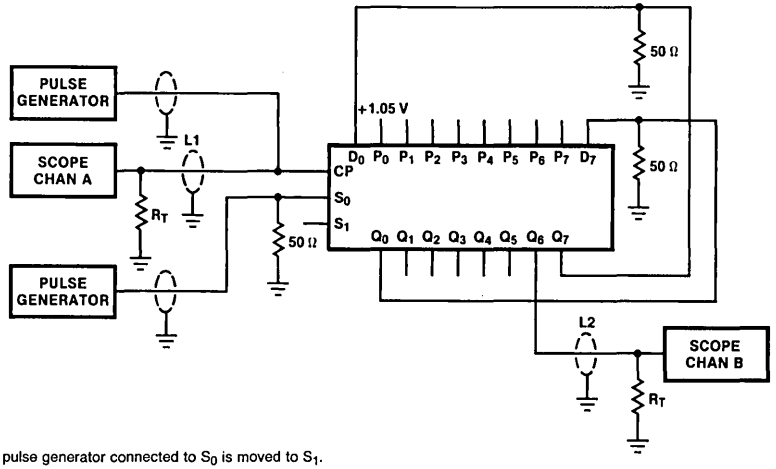


Notes:

V_{CC}, V_{CCA} = +2V, V_{EE} = −2.5V
L1, L2 and L3 = equal length 50Ω impedance lines
R_T = 50Ω terminator internal to scope
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
All unused outputs are loaded with 50Ω to GND
C_L = Fixture and stray capacitance ≤ 3 pF
Pin numbers shown are for Flatpak; for DIP see logic symbol

TL/F/9880–6

FIGURE 1. AC Test Circuit



Notes:

For shift right mode pulse generator connected to S_0 is moved to S_1.

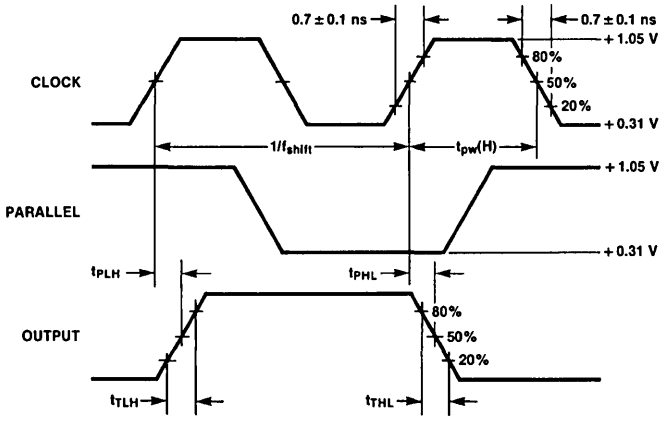
Pulse generator connected to S_1 has a LOW frequency 99% duty cycle, which allows occasional parallel load.

The feedback path from output to input should be as short as possible.

TL/F/9880–7

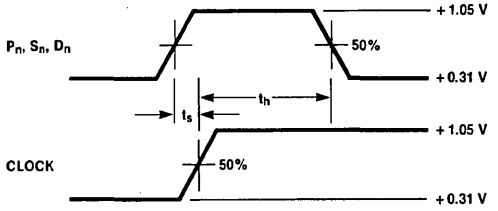
FIGURE 2. Shift Frequency Test Circuit (Shift Left)

Switching Waveforms



TL/F/9880–8

FIGURE 3. Propagation Delay and Transition Times



TL/F/9880–9

Notes:

t_s is the minimum time before the transition of the clock that information must be present at the data input.

t_h is the minimum time after the transition of the clock that information must remain unchanged at the data input.

FIGURE 4. Setup and Hold Times

National Semiconductor

100343
Low Power 8-Bit Latch

General Description

The 100343 contains eight D-type latches, individual inputs, (D_n), outputs (Q_n), a common enable pin ($\overline{E}$), and a latch enable pin ($\overline{LE}$). A Q output follows its D input when both $\overline{E}$ and $\overline{LE}$ are LOW. When either $\overline{E}$ or $\overline{LE}$ (or both) are HIGH, a latch stores the last valid data present on its D input prior to $\overline{E}$ or $\overline{LE}$ going HIGH.

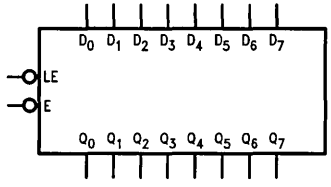
The 100343 outputs are designed to drive a 50Ω termination resistor to −2.0V. All inputs have 50 kΩ pull-down resistors.

Features

- Low power operation
- 2000V ESD protection
- Voltage compensated operating range = −4.2V to −5.7V
- Available to industrial grade temperature range
- Available to MIL-STD-883

Ordering Code: See Section 6

Logic Symbol

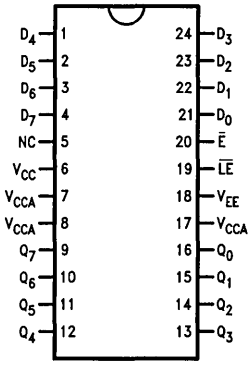


TL/F/10250–1

Pin Names	Description
D_0–D_7	Data Inputs
$\overline{E}$	Enable Input
$\overline{LE}$	Latch Enable Input
Q_0–Q_7	Data Inputs
NC	No Connect

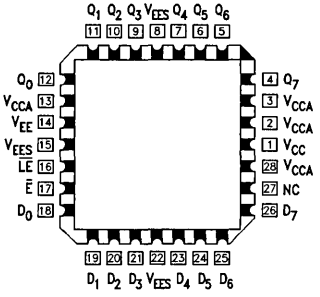
Connection Diagrams

24-Pin DIP



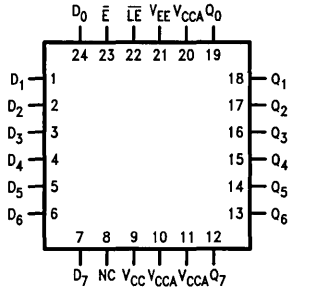
TL/F/10250–2

28-Pin PCC



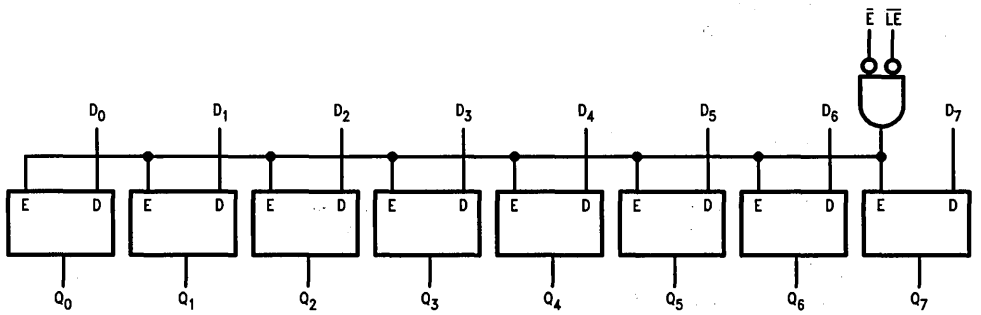
TL/F/10250–4

24-Pin Quad Cerpak



TL/F/10250–3

Logic Diagram



TL/F/10250–5

Truth Table

Inputs			Outputs
D_n	$\overline{E}$	$\overline{LE}$	Q_n
L	L	L	L
H	L	L	H
X	H	X	Latched*
X	X	H	Latched*

*Retains data present before either $\overline{LE}$ or $\overline{E}$ went HIGH
H = HIGH voltage level
L = LOW voltage level
X = Dont's care

Absolute Maximum Ratings

Above which the useful life may be impared (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature (T_{STG})	−65°C to +150°C
Maximum Junction Temperature (T_J)	
Ceramic	+175°C
Plastic	+150°C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Output Current (DC Output HIGH)	−50 mA
ESD (Note 2)	≥2000V

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: ESD testing conforms to MIL-STD-883, Method 3015.

Recommended Operating Conditions

Case Temperature (T_C)	
Commercial	0°C to +85°C
Industrial	−40°C to +85°C
Military	−55°C to +125°C
Supply Voltage (V_{EE})	−5.7V to −4.2V

Commercial Version

DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions	
V_{OH}	Output HIGH Voltage	−1025	−955	−870	mV	V_{IN} = V_{IH} (Max) or V_{IL} (Min)	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830	−1705	−1620	mV		
V_{OHC}	Output HIGH Voltage	−1035			mV	V_{IN} = V_{IH} (Min) or V_{IL} (Max)	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610	mV		
V_{IH}	Input HIGH Voltage	−1165		−870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1830		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = V_{IL} (Min)	
I_{IH}	Input HIGH Current			240	μA	V_{IN} = V_{IH} (Max)	
I_{EE}	Power Supply Current	−95 −97		−55 −55	mA	Inputs Open V_{EE} = −4.2V to −4.8V V_{EE} = −4.2V to −5.7V	

Note 3: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DIP AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay D_n to Output	0.80	2.00	0.80	2.00	0.80	2.20	ns	*Figures 1, 2, 3* (Note 1)
t_{PLH} t_{PHL}	Propagation Delay $\overline{LE}$, $\overline{E}$ to Output	1.40	2.90	1.40	2.90	1.60	3.10	ns	*Figures 1, 2, 3* (Note 1)
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	2.00	0.45	2.00	0.45	2.00	ns	*Figures 1, 3*
t_s	Setup Time D_0–D_7	1.0		1.0		1.1		ns	*Figures 1, 4*
t_h	Hold Time D_0–D_7	0.1		0.1		0.1		ns	*Figures 1, 4*
t_{pw}(H)	Pulse Width HIGH $\overline{LE}$, $\overline{E}$	2.00		2.00		2.00		ns	*Figures 1, 4*

Note 1: The propagation delay specified is for single output switching. Delays may vary up to 300 ps with multiple outputs switching.

Commercial Version (Continued)

PCC and Cerpack AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay D_n to Output	0.80	1.80	0.80	1.80	0.80	2.00	ns	*Figures 1, 2, 3* (Note 2)
t_{PLH} t_{PHL}	Propagation Delay $\overline{LE}$, $\overline{E}$ to Output	1.40	2.70	1.40	2.70	1.60	2.90	ns	*Figures 1, 2, 3* (Note 2)
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.90	0.45	1.90	0.45	1.90	ns	*Figures 1, 3*
t_s	Setup Time D_0–D_7	0.90		0.90		1.00		ns	*Figures 1, 4*
t_h	Hold Time D_0–D_7	0.0		0.0		0.0		ns	*Figures 1, 4*
t_{pw}(H)	Pulse Width HIGH $\overline{LE}$, $\overline{E}$	2.00		2.00		2.00		ns	*Figures 1, 4*
t_{OSHL}	Maximum Skew Common Edge Output-to-Output Variation Data to Output Path		340		340		340	ps	PCC Only (Note 1)
t_{OSLH}	Maximum Skew Common Edge Output-to-Output Variation Data to Output Path		440		440		440	ps	PCC Only (Note 1)
t_{OST}	Maximum Skew Opposite Edge Output-to-Output Variation Data to Output Path		480		480		480	ps	PCC Only (Note 1)
t_{PS}	Maximum Skew Pin (Signal) Transition Variation Data to Output Path		300		300		300	ps	PCC Only (Note 1)

Note 1: Output-to-Output Skew is defined as the absolute value of the difference between the actual propagation delay for any outputs within the same packaged device. The specifications apply to any outputs switching in the same direction either HIGH to LOW (t_{OSHL}), or LOW to HIGH (t_{OSLH}), or in opposite directions both HL and LH (t_{OST}). Parameters t_{OST} and t_{PS} guaranteed by design.

Note 2: The propagation delay specified is for single output switching. Delays may vary up to 300 ps with multiple outputs switching.

Industrial Version

PCC DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = −40°C to +85°C (Note 3)

Symbol	Parameter	T_C = −40°C		T_C = 0°C to +85°C		Units	Conditions	
		Min	Max	Min	Max			
V_{OH}	Output HIGH Voltage	−1085	−870	−1025	−870	mV	V_{IN} = V_{IH} (Max) or V_{IL} (Min)	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830	−1575	−1830	−1620	mV		
V_{OHC}	Output HIGH Voltage	−1095		−1035		mV	V_{IN} = V_{IH} (Min) or V_{IL} (Max)	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage		−1565		−1610	mV		
V_{IH}	Input HIGH Voltage	−1170	−870	−1165	−870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1830	−1480	−1830	−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50		0.50		μA	V_{IN} = V_{IL} (Min)	
I_{IH}	Input HIGH Current		240		240	μA	V_{IN} = V_{IH} (Max)	
I_{EE}	Power Supply Current	−95 −97	−50 −50	−95 −97	−55 −55	mA	Inputs Open V_{EE} = −4.2V to −4.8V V_{EE} = −4.2V to −5.7V	

Note 3: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

PCC AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = −40°C		T_C = +25°C		T_C = +85°C		Units	
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay D_n to Output	0.80	1.80	0.80	1.80	0.80	2.00	ns	*Figures 1, 2, 3* (Note 1)
t_{PLH} t_{PHL}	Propagation Delay $\overline{LE}$, $\overline{E}$ to Output	1.40	2.70	1.40	2.70	1.60	2.90	ns	*Figures 1, 2, 3* (Note 1)
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.40	2.50	0.45	1.90	0.45	1.90	ns	*Figures 1, 3*
t_s	Setup Time D_0–D_7	0.60		0.90		1.00		ns	*Figures 1, 4*
t_h	Hold Time D_0–D_7	0.8		0.0		0.0		ns	*Figures 1,4*
t_{pw}(H)	Pulse Width HIGH $\overline{LE}$, $\overline{E}$	2.40		2.00		2.00		ns	*Figures 1, 4*

Note 1: The propagation delay specified is for single output switching. Delays may vary up to 300 ps with multiple outputs switching.

Military Version

DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = −55°C to +125°C

Symbol	Parameter	Min	Max	Units	T_C	Conditions		Notes
V_{OH}	Output HIGH Voltage	−1025	−870	mV	0°C to +125°C	V_{IN} = V_{IH} (Max) or V_{IL} (Min)	Loading with 50Ω to −2.0V	1, 2, 3
		−1085	−870	mV	−55°C			
V_{OL}	Output LOW Voltage	−1830	−1620	mV	0°C to +125°C			
		−1830	−1555	mV	−55°C			
V_{OHC}	Output HIGH Voltage	−1035		mV	0°C to +125°C	V_{IN} = V_{IH} (Max) or V_{IL} (Min)	Loading with 50Ω to −2.0V	1, 2, 3
		−1085		mV	−55°C			
V_{OLC}	Output LOW Voltage		−1610	mV	0°C to +125°C			
			−1555	mV	−55°C			
V_{IH}	Input HIGH Voltage	−1165	−870	mV	−55°C to +125°C	Guaranteed HIGH Signal for All Inputs		1, 2, 3, 4
V_{IL}	Input LOW Voltage	−1830	−1475	mV	−55°C to +125°C	Guaranteed LOW Signal for All Inputs		1, 2, 3, 4
I_{IL}	Input LOW Current	0.50		μA	−55°C to +125°C	V_{EE} = −4.2V V_{IN} = V_{IL} (Min)		1, 2, 3
I_{EE}	Power Supply Current	−100 −105	−35 −35	mA mA	−55 to +125°C	V_{EE} = −4.2V to −4.8V V_{EE} = −4.2V to −5.7V		1, 2, 3
I_{IH}	Input HIGH Current		240	μA	0°C to +125°C	V_{EE} = −5.7V V_{IN} = V_{IH} (Max)		1, 2, 3
			340	μA	−55°C			
I_{EE}	Power Supply Current	−100 −105	−35 −35	mA	−55°C to +125°C	Inputs Open V_{EE} = −4.2V to −4.8V V_{EE} = −4.2V to −5.7V		1, 2, 3

Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals −55°C), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 2: Screen tested 100% on each device at −55°C, +25°C, and +125°C, Subgroups 1, 2, 3, 7, and 8.

Note 3: Sample tested (Method 5005, Table I) on each manufactured lot at −55°C, +25°C, and +125°C, Subgroups A1, 2, 3, 7, and 8.

Note 4: Guaranteed by applying specified input condition and testing V_{OH}/V_{OL}.

Military Version (Continued)

AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = −55°C		T_C = +25°C		T_C = +125°C		Units	Conditions	Notes
		Min	Max	Min	Max	Min	Max			
t_{PLH} t_{PHL}	Propagation Delay D_n to Output	0.50	2.70	0.50	2.30	0.50	2.80	ns	*Figures 1, 2, 3*	1, 2, 3, 5
t_{PLH} t_{PHL}	Propagation Delay $\overline{LE}$, $\overline{E}$ to Output	0.90	3.40	1.0	3.10	1.10	3.90	ns	*Figures 1, 2, 3*	1, 2, 3, 5
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.40	2.50	0.40	2.40	0.40	2.70	ns	*Figures 1, 3*	4
t_s	Setup Time D_0–D_7	0.60		0.60		0.60		ns	*Figures 1, 4*	4
t_h	Hold Time D_0–D_7	1.50		1.50		1.70		ns	*Figures 1, 4*	4
t_{pw}(H)	Pulse Width HIGH $\overline{LE}$, $\overline{E}$	2.40		2.40		2.40		ns	*Figures 1, 4*	4

Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals −55°C), then testing immediately after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

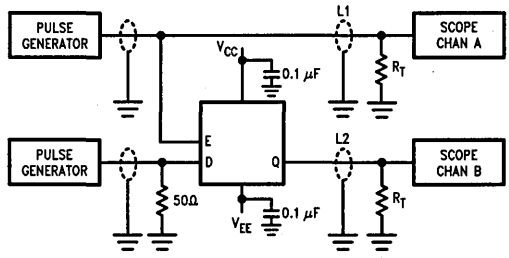
Note 2: Screen tested 100% on each device at +25°C temperature only, Subgroup A9.

Note 3: Sample tested (Method 5005, Table I) on each manufactured lot at +25°C, Subgroup A9, and at +125°C and −55°C temperatures, Subgroups A10 and A11.

Note 4: Not tested at +25°C, +125°C, and −55°C temperature (design characterization data).

Note 5: The propagation delay specified is for single output switching. Delays may vary up to 300 ps with multiple outputs switching.

Test Circuitry



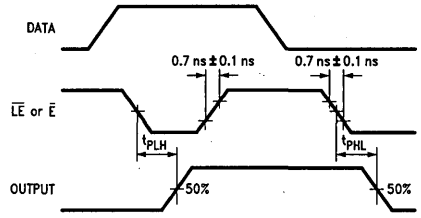
TL/F/10250–6

FIGURE 1. AC Test Circuit

Notes:

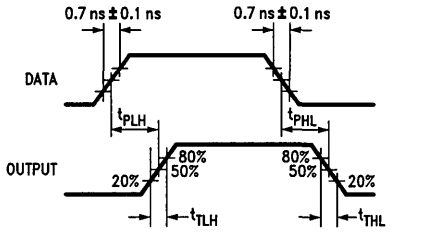
V_{CC}, V_{CCA} = +2V, V_{EE} = −2.5V
L1 and L2 = equal length 50Ω impedance lines
R_T = 50Ω terminator internal to scope
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
All unused outputs are loaded with 50Ω to GND
C_L = Fixture and stray capacitance ≤ 3 pF

Switching Waveforms



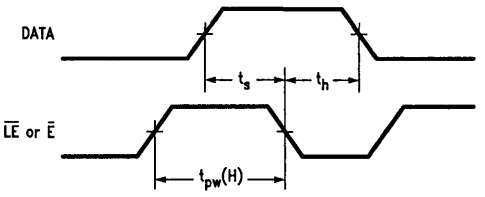
TL/F/10250–7

FIGURE 2. Propagation Delays



TL/F/10250–8

FIGURE 3. Propagation and Transition Times



TL/F/10250–9

FIGURE 4. Setup, Hold and Pulse Width Times

National Semiconductor

100344
Low Power 8-Bit Latch with Cut-Off Drivers

General Description

The 100344 contains eight D-type latches, individual inputs (D_n), outputs (Q_n), a common enable pin ($\overline{E}$), latch enable ($\overline{LE}$), and output enable pin ($\overline{OEN}$). A Q output follows its D input when both $\overline{E}$ and $\overline{LE}$ are LOW. When either $\overline{E}$ or $\overline{LE}$ (or both) are HIGH, a latch stores the last valid data present on its D input prior to $\overline{E}$ or $\overline{LE}$ going HIGH.

A HIGH on $\overline{OEN}$ holds the outputs in a cut-off state. The cut-off state is designed to be more negative than a normal ECL LOW level. This allows the output emitter-followers to turn off when the termination supply is −2.0V, presenting a high impedance to the data bus. This high impedance reduces termination power and prevents loss of low state noise margin when several loads share the bus.

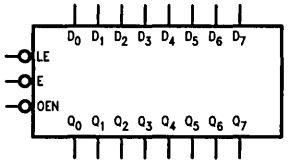
The 100344 outputs are designed to drive a doubly terminated 50Ω transmission line (25Ω load impedance). All inputs have 50 kΩ pull-down resistors.

Features

- Cut-off drivers
- Drives 25Ω load
- Low power operation
- 2000V ESD protection
- Voltage compensated operating range = −4.2V to −5.7V
- Available to MIL-STD-883

Ordering Code: See Section 6

Logic Symbol

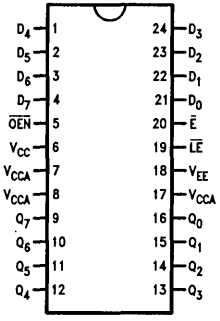


TL/F/9883-4

Pin Names	Description
D_0–D_7	Data Inputs
$\overline{E}$	Enable Input
$\overline{LE}$	Latch Enable Input
$\overline{OEN}$	Output Enable Input
Q_0–Q_7	Data Outputs

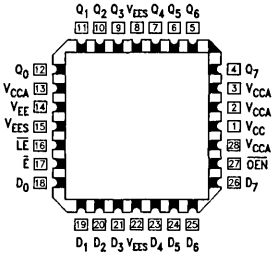
Connection Diagrams

24-Pin DIP



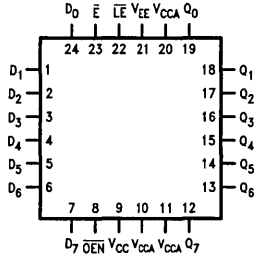
TL/F/9883-1

28-Pin PCC



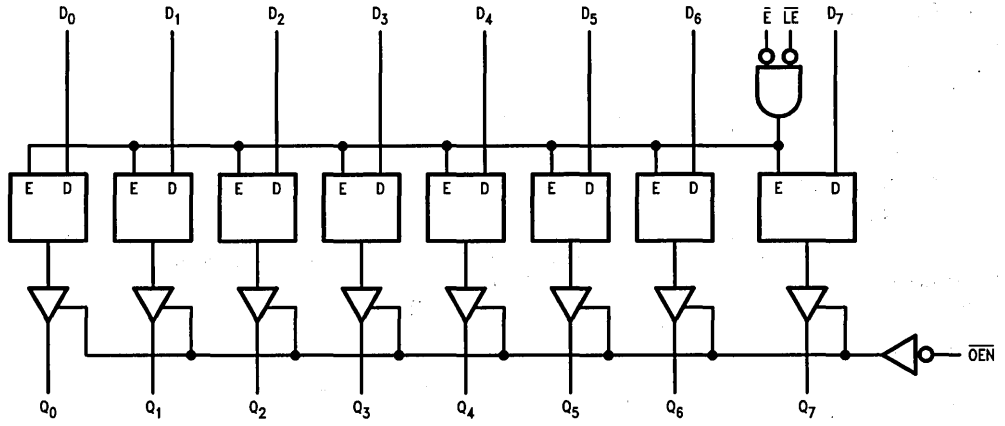
TL/F/9883-3

24-Pin Quad Cerpak



TL/F/9883-2

Logic Diagram



TL/F/9883–5

Truth Table

Inputs				Outputs
D_n	$\overline{E}$	$\overline{LE}$	$\overline{OEN}$	Q_n
L	L	L	L	L
H	L	L	L	H
X	H	X	L	Latched*
X	X	H	L	Latched*
X	X	X	H	Cutoff

*Retains data present before either $\overline{LE}$ or $\overline{E}$ go HIGH.

H = HIGH Voltage level
L = LOW Voltage level
Cutoff = lower-than-LOW state
X = Don't Care

Absolute Maximum Ratings

Above which the useful life may be impaired (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature (T_{STG})	−65°C to +150°C
Maximum Junction Temperature (T_J)	
Ceramic	+175°C
Plastic	+150°C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Output Current (DC Output HIGH)	−100 mA
ESD (Note 2)	≥2000V

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: ESD testing conforms to MIL-STD-883, Method 3015.

Recommended Operating Conditions

Case Temperature (T_C)	
Commercial	0°C to +85°C
Industrial	−40°C to +85°
Military	−55°C to +125°C
Supply Voltage (V_{EE})	−5.7V to −4.2V

Commercial Version

DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions	
V_{OH}	Output HIGH Voltage	−1025	−955	−870	mV	V_{IN} = V_{IH} (Max) or V_{IL} (Min)	Loading with 25Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830	−1705	−1620	mV		
V_{OHC}	Output HIGH Voltage	−1035			mV	V_{IN} = V_{IH} (Min) or V_{IL} (Max)	Loading with 25Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610	mV		
V_{OLZ}	Cutoff LOW Voltage			−1950	mV	V_{IN} = V_{IH} (Min) or V_{IL} (Max)	$\overline{OEN}$ = HIGH
V_{IH}	Input HIGH Voltage	−1165		−870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1830		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = V_{IL} (Min)	
I_{IH}	Input HIGH Current			240	μA	V_{IN} = V_{IH} (Max)	
I_{EE}	Power Supply Current	−178 −185		−85 −85	mA	Inputs Open V_{EE} = −4.2V to −4.8V V_{EE} = −4.2V to −5.7V	

Note 3: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DIP AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay D_n to Output	0.90	2.10	0.90	2.10	1.00	2.30	ns	*Figures 1, 2* (Note 1)
t_{PLH} t_{PHL}	Propagation Delay $\overline{LE}$, $\overline{E}$ to Output	1.60	3.10	1.60	3.10	1.80	3.40	ns	*Figures 1, 4* (Note 1)
t_{PZH} t_{PHZ}	Propagation Delay $\overline{OEN}$ to Output	1.60 1.00	4.20 2.70	1.60 1.00	4.20 2.70	1.60 1.00	4.20 2.70	ns	*Figures 1, 2* (Note 1)
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	2.00	0.45	2.00	0.45	2.00	ns	*Figures 1, 3*

Note 1: The propagation delay specified is for single output switching. Delays may vary up to 300 ps with multiple outputs switching.

Commercial Version (Continued)

DIP AC Electrical Characteristics (Continued)

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_S	Setup Time D_0–D_7	1.00		1.00		1.10		ns	*Figures 1, 3*
t_H	Hold Time D_0–D_7	0.10		0.10		0.10		ns	*Figures 1, 3*
$t_{pw}(H)$	Pulse Width HIGH $\overline{LE}$, $\overline{E}$	2.00		2.00		2.00		ns	*Figures 1, 3*

PCC and Cerpak AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay D_n to Output	0.90	1.90	0.90	1.90	1.00	2.10	ns	*Figures 1, 2* (Note 2)
t_{PLH} t_{PHL}	Propagation Delay $\overline{LE}$, $\overline{E}$ to Output	1.60	2.90	1.60	2.90	1.80	3.20	ns	*Figures 1, 4* (Note 2)
t_{PZH} t_{PHZ}	Propagation Delay $\overline{OEN}$ to Output	1.60 1.00	4.00 2.50	1.60 1.00	4.00 2.50	1.60 1.00	4.00 2.50	ns	*Figures 1, 2* (Note 2)
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.90	0.45	1.90	0.45	1.90	ns	*Figures 1, 3*
t_S	Setup Time D_0–D_7	0.90		0.90		1.00		ns	*Figures 1, 3*
t_H	Hold Time D_0–D_7	0.00		0.00		0.00		ns	*Figures 1, 3*
$t_{pw}(H)$	Pulse Width HIGH $\overline{LE}$, $\overline{E}$	2.00		2.00		2.00		ns	*Figures 1, 3*
t_{OSHL}	Maximum Skew Common Edge Output-to-Output Variation Data to Output Path		330		330		330	ps	PCC Only (Note 1)
t_{OSLH}	Maximum Skew Common Edge Output-to-Output Variation Data to Output Path		330		330		330	ps	PCC Only (Note 1)
t_{OST}	Maximum Skew Opposite Edge Output-to-Output Variation Data to Output Path		330		330		330	ps	PCC Only (Note 1)
t_{ps}	Maximum Skew Pin (Signal) Transition Variation Data to Output Path		230		230		230	ps	PCC Only (Note 1)

Note 1: Output-to-Output Skew is defined as the absolute value of the difference between the actual propagation delay for any outputs within the same packaged device. The specifications apply to any outputs switching in the same direction either HIGH to LOW (t_{OSHL}), or LOW to HIGH (t_{OSLH}), or in opposite directions both HL and LH (t_{OST}). Parameters t_{OST} and t_{ps} guaranteed by design.

Note 2: The propagation delay specified is for single output switching. Delays may vary up to 300 ps with multiple outputs switching.

Military Version

DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = −55°C to +125°C

Symbol	Parameter	Min	Max	Units	T_C	Conditions		Notes
V_{OH}	Output HIGH Voltage	−1025	−870	mV	0°C to +125°C	V_{IN} = V_{IH} (Max) or V_{IL} (Min)	Loading with 25Ω to −2.0V	1, 2, 3
		−1085	−870	mV	−55°C			
V_{OL}	Output LOW Voltage	−1830	−1620	mV	0°C to +125°C			
		−1830	−1555	mV	−55°C			
V_{OHC}	Output HIGH Voltage	−1035		mV	0°C to +125°C	V_{IN} = V_{IH} (Min) or V_{IL} (Max)	Loading with 25Ω to −2.0V	1, 2, 3
		−1085		mV	−55°C			
V_{OLC}	Output LOW Voltage		−1610	mV	0°C to +125°C			
			−1555	mV	−55°C			
V_{OLZ}	Cutoff LOW Voltage		−1950	mV	0°C to +125°C	V_{IN} = V_{IH} (MIN) or V_{IL} (Max)	$\overline{OEN}$ = HIGH	1, 2, 3
			−1850		−55°C			
V_{IH}	Input HIGH Voltage	−1165	−870	mV	−55°C to +125°C	Guaranteed HIGH Signal for All Inputs		1, 2, 3, 4
V_{IL}	Input LOW Voltage	−1830	−1475	mV	−55°C to +125°C	Guaranteed LOW Signal for All Inputs		1, 2, 3, 4
I_{IL}	Input LOW Current	0.50		μA	−55°C to +125°C	V_{EE} = −4.2V V_{IN} = V_{IL} (Min)		1, 2, 3
I_{IH}	Input HIGH Current		240	μA	0°C to +125°C	V_{EE} = −5.7V V_{IN} = V_{IH} (Max)		1, 2, 3
			340	μA	−55°C			
I_{EE}	Power Supply Current	−195 −205	−65 −65	mA	−55°C to +125°C	Inputs Open V_{EE} = −4.2V to −4.8V V_{EE} = −4.2V to −5.7V		1, 2, 3

Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals −55°C), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 2: Screen tested 100% on each device at −55°C, +25°C, and +125°C, Subgroups 1, 2, 3, 7, and 8.

Note 3: Sample tested (Method 5005, Table I) on each manufactured lot at −55°C, +25°C, and +125°C, Subgroups A1, 2, 3, 7, and 8.

Note 4: Guaranteed by applying specified input condition and testing V_{OH}/V_{OL}.

Military Version (Continued)

AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = −55°C		T_C = +25°C		T_C = +125°C		Units	Conditions	Notes
		Min	Max	Min	Max	Min	Max			
t_{PLH} t_{PHL}	Propagation Delay D_n to Output	0.50	2.60	0.70	2.60	0.70	3.10	ns	*Figures 1, 2*	1, 2, 3, 5
t_{PLH} t_{PHL}	Propagation Delay $\overline{LE}$, $\overline{E}$ to Output	0.80	3.30	1.00	3.30	1.10	3.80	ns	*Figures 1, 4*	1, 2, 3, 5
t_{PZH} t_{PHZ}	Propagation Delay $\overline{OEN}$ to Output	1.00 0.70	4.60 3.00	1.10 0.70	4.20 2.80	1.20 0.70	4.40 3.20	ns	*Figures 1, 2*	1, 2, 3, 5
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.40	2.50	0.40	2.40	0.40	2.70	ns	*Figures 1, 3*	4
t_s	Setup Time D_0–D_7	1.50		1.50		1.70		ns	*Figures 1, 3*	4
t_h	Hold Time D_0–D_7	0.60		0.60		0.60		ns	*Figures 1, 3*	4
t_{pw}(H)	Pulse Width HIGH $\overline{LE}$, $\overline{E}$	2.40		2.40		2.40		ns	*Figures 1, 3*	4

Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals −55°C), then testing immediately after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 2: Screen tested 100% on each device at +25°C temperature only, Subgroup A9.

Note 3: Sample tested (Method 5005, Table I) on each manufactured lot at +25°C, Subgroup A9, and at +125°C and −55°C temperatures, Subgroups A10 and A11.

Note 4: Not tested at +25°C, +125°C, and −55°C temperature (design characterization data).

Note 5: The propagation delay specified is for single output switching. Delays may vary up to 300 ps with multiple outputs switching.

Test Circuitry

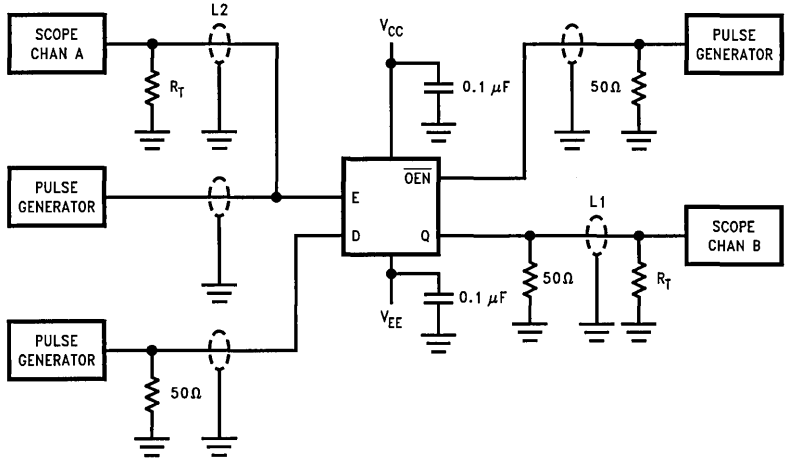


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FIGURE 1. AC Test Circuit

Notes:

V_{CC}, V_{CCA} = +2V, V_{EE} = −2.5V
L1 and L2 = equal length 50Ω impedance lines
R_T = 50Ω terminator internal to scope
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
All unused outputs are loaded with 25Ω to GND
C_L = Fixture and stray capacitance ≤ 3 pF

Switching Waveforms

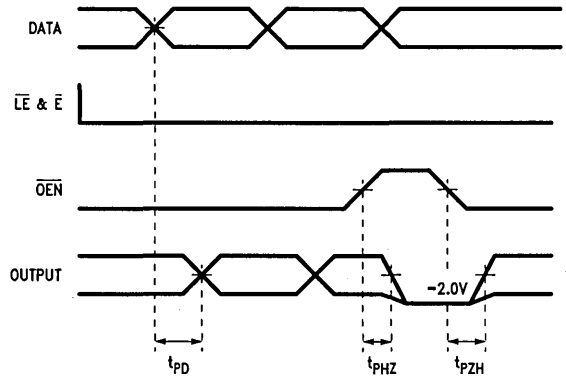

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FIGURE 2. Propagation Delay and Cutoff Times

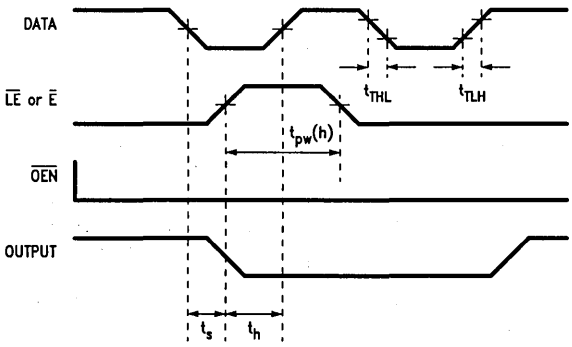

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FIGURE 3. Setup, Hold and Pulse Width Times

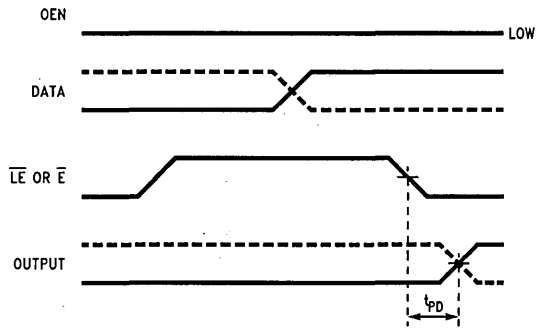

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FIGURE 4. Propagation Delay $\overline{LE}$, $\overline{E}$ to Q

National Semiconductor

100350
Low Power Hex D-Latch

General Description

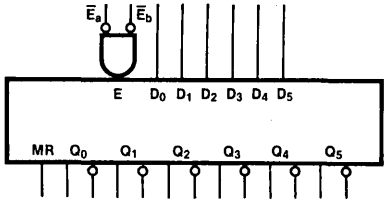
The 100350 contains six D-type latches with true and complement outputs, a pair of common Enables ($\overline{E}_a$ and $\overline{E}_b$), and a common Master Reset (MR). A Q output follows its D input when both $\overline{E}_a$ and $\overline{E}_b$ are LOW. When either $\overline{E}_a$ or $\overline{E}_b$ (or both) are HIGH, a latch stores the last valid data present on its D input before $\overline{E}_a$ or $\overline{E}_b$ went HIGH. The MR input overrides all other inputs and makes the Q outputs LOW. All inputs have 50 kΩ pull-down resistors.

Features

- 20% power reduction of the 100150
- 2000V ESD protection
- Pin/function compatible with 100150
- Voltage compensated operating range = −4.2V to −5.7V

Ordering Code: See Section 6

Logic Symbol



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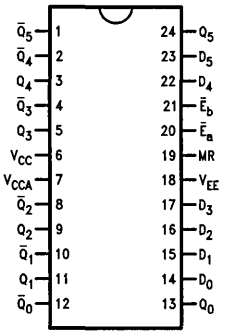
Pin Names	Description
D_0–D_5	Data Inputs
$\overline{E}_a$, $\overline{E}_b$	Common Enable Inputs (Active LOW)
MR	Asynchronous Master Reset Input
Q_0–Q_5	Data Outputs
$\overline{Q}_0$–$\overline{Q}_5$	Complementary Data Outputs

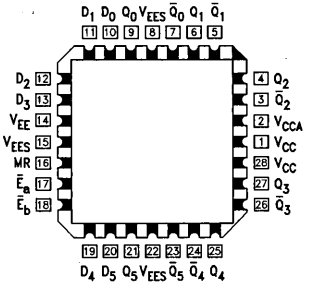
Connection Diagrams

24-Pin DIP



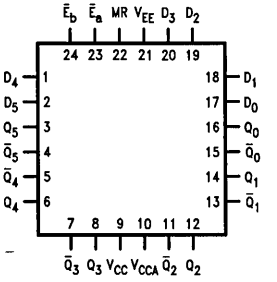
TL/F/9884–1

28-Pin PCC



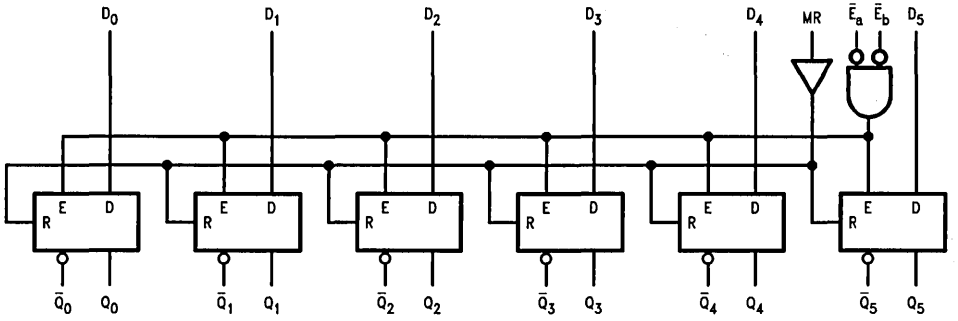
TL/F/9884–3

24-Pin Quad Cerpak



TL/F/9884–2

Logic Diagram



TL/F/9884–4

Truth Tables (Each Latch)

Latch Operation

Inputs				Outputs
D_n	$\overline{E}_a$	$\overline{E}_b$	MR	Q_n
L	L	L	L	L
H	L	L	L	H
X	H	X	L	Latched*
X	X	H	L	Latched*

*Retains data present before $\overline{E}$ positive transition

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

Asynchronous Operation

Inputs				Outputs
D_n	$\overline{E}_a$	$\overline{E}_b$	MR	Q_n
X	X	X	H	L

Absolute Maximum Ratings

Above which the useful life may be impaired. (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature (T_{STG})	−65°C to +150°C
Maximum Junction Temperature (T_J)	
Ceramic	+175°C
Plastic	+150°C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Output Current (DC Output HIGH)	−50 mA
ESD (Note 2)	≥2000V

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: ESD testing conforms to MIL-STD-883, Method 3015.

Recommended Operating Conditions

Case Temperature (T_C)	
Commercial	0°C to +85°C
Military	−55°C to +125°C
Supply Voltage (V_{EE})	−5.7V to −4.2V

Commercial Version

DC Electrical Characteristics

V_{EE} = −4.5V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions	
V_{OH}	Output HIGH Voltage	−1025	−955	−870	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830	−1705	−1620			
V_{OHC}	Output HIGH Voltage	−1035			mV	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610			
V_{IH}	Input HIGH Voltage	−1165		−870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1830		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	
I_{IH}	Input HIGH Current				μA	V_{IN} = $V_{IH\ (Max)}$	
	MR			240			
	D_n			240			
	$\overline{E}_a$, $\overline{E}_b$			240			
I_{EE}	Power Supply Current				mA	Inputs Open	
		−89		−44		V_{EE} = −4.2V to −4.8V	
		−93		−44		V_{EE} = −4.2V to −5.7V	

Note 3: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

Commercial Version (Continued)

DIP AC Electrical Characteristics V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay D_n to Output (Transparent Mode)	0.50	1.40	0.50	1.40	0.50	1.50	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}_a$, $\overline{E}_b$ to Output	0.75	1.85	0.75	1.85	0.75	2.05	ns	
t_{PLH} t_{PHL}	Propagation Delay MR to Output	0.90	2.10	0.90	2.10	0.90	2.10	ns	*Figures 1* and *3*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.35	1.30	0.35	1.30	0.35	1.30	ns	*Figures 1* and *2*
t_s	Setup Time D_0–D_5 MR (Release Time)	1.00 1.60		1.00 1.60		1.00 1.60		ns	*Figures 3* and *4*
t_h	Hold Time, D_0–D_5	0.40		0.40		0.40		ns	*Figure 4*
$t_{pw}(L)$	Pulse Width LOW $\overline{E}_a$, $\overline{E}_b$	2.00		2.00		2.00		ns	*Figure 2*
$t_{pw}(H)$	Pulse Width HIGH, MR	2.00		2.00		2.00		ns	*Figure 3*

PCC and Cerpak AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay D_n to Output (Transparent Mode)	0.50	1.20	0.50	1.20	0.50	1.30	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}_a$, $\overline{E}_b$ to Output	0.75	1.65	0.75	1.65	0.75	1.85	ns	
t_{PLH} t_{PHL}	Propagation Delay MR to Output	0.90	1.90	0.90	1.90	0.90	1.90	ns	*Figures 1* and *3*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.35	1.10	0.35	1.10	0.35	1.10	ns	*Figures 1* and *2*
t_s	Setup Time D_0–D_5 MR (Release Time)	0.90 1.50		0.90 1.50		0.90 1.50		ns	*Figures 3* and *4*
t_h	Hold Time, D_0–D_5	0.30		0.30		0.30		ns	*Figure 4*
$t_{pw}(L)$	Pulse Width LOW $\overline{E}_a$, $\overline{E}_b$	2.00		2.00		2.00		ns	*Figure 2*
$t_{pw}(H)$	Pulse Width HIGH, MR	2.00		2.00		2.00		ns	*Figure 3*

Military Version—Preliminary

DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = −55°C to +125°C

Symbol	Parameter	Min	Max	Units	T_C	Conditions		Notes
V_{OH}	Output HIGH Voltage	−1025	−870	mV	0°C to +125°C	V_{IN} = V_{IH}(Max) or V_{IL} (Min)	Loading with 50Ω to −2.0V	1, 2, 3
		−1085	−870	mV	−55°C			
V_{OL}	Output LOW Voltage	−1830	−1620	mV	0°C to +125°C			
		−1830	−1555	mV	−55°C			
V_{OHC}	Output HIGH Voltage	−1035		mV	0°C to +125°C	V_{IN} = V_{IH}(Min) or V_{IL} (Min)	Loading with 50Ω to −2.0V	1, 2, 3
		−1085		mV	−55°C			
V_{OLC}	Output LOW Voltage		−1610	mV	0°C to +125°C			
			−1555	mV	−55°C			
V_{IH}	Input HIGH Voltage	−1165	−870	mV	−55°C to +125°C	Guaranteed HIGH Signal for All Inputs		1, 2, 3, 4
V_{IL}	Input LOW Voltage	−1830	−1475	mV	−55°C to +125°C	Guaranteed LOW Signal for All Inputs		1, 2, 3, 4
I_{IL}	Input LOW Current	0.50		μA	−55°C to +125°C	V_{EE} = −4.2V V_{IN} = V_{IL} (Min)		1, 2, 3
I_{IH}	Input HIGH Current MR D_n $\overline{E}_a$, $\overline{E}_b$		 300 250 520	μA	0°C to +125°C	V_{EE} = −5.7V V_{IN} = V_{IH} (Max)		1, 2, 3
	MR D_n $\overline{E}_a$, $\overline{E}_b$		450 350 750	μA	−55°C			
I_{EE}	Power Supply Current	−138	−64	mA	−55°C to +125°C	Inputs Open		1, 2, 3

Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals −55°C), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 2: Screen tested 100% on each device at −55°C, +25°C, and +125°C, Subgroups 1, 2, 3, 7, and 8.

Note 3: Sample tested (Method 5005, Table I) on each manufactured lot at −55°C, +25°C, and +125°C, Subgroups A1, 2, 3, 7, and 8.

Note 4: Guaranteed by applying specified input condition and testing V_{OH}/V_{OL}.

Military Version-Preliminary (Continued)

AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = −55°C		T_C = +25°C		T_C = +125°C		Units	Conditions	Notes
		Min	Max	Min	Max	Min	Max			
t_{PLH} t_{PHL}	Propagation Delay D_n to Output (Transparent Mode)	0.45	1.50	0.50	1.40	0.50	1.50	ns	*Figures 1* and *2*	1, 2, 3
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}_a$, $\overline{E}_b$ to Output	0.75	2.05	0.75	1.85	0.75	2.05	ns		
t_{PLH} t_{PHL}	Propagation Delay MR to Output	0.80	2.40	0.90	2.40	0.90	2.60	ns	*Figures 1* and *3*	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.70	0.45	1.60	0.45	1.60	ns	*Figures 1* and *2*	
t_S	Setup Time D_0-D_5 MR (Release Time)	0.70 2.10		0.70 2.10		0.70 2.10		ns	*Figures 1* and *2*	
t_H	Hold Time, D_0-D_5	0.70		0.70		0.70		ns	*Figure 4*	4
t_{pw}(L)	Pulse Width LOW $\overline{E}_a$, $\overline{E}_b$	2.00		2.00		2.00		ns	*Figure 2*	
t_{pw}(L)	Pulse Width HIGH, MR	2.00		2.00		2.00		ns	*Figure 3*	

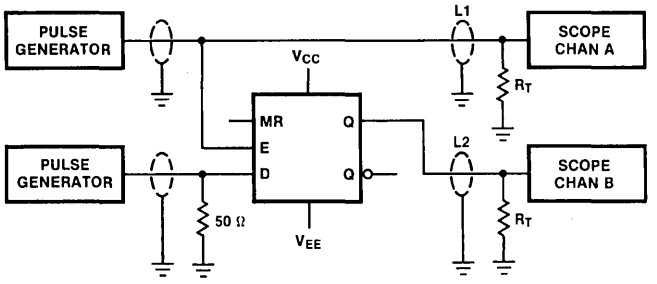
Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals −55°C), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 2: Screen tested 100% on each device at +25°C, temperature only, Subgroup A9.

Note 3: Sample tested (Method 5005, Table I) on each Mfg. lot at +25°C, Subgroup A9, and at +125°C, and −55°C temp., Subgroups A10 and A11.

Note 4: Not tested at +25°C, +125°C, and −55°C temperature (design characterization data).

Test Circuit



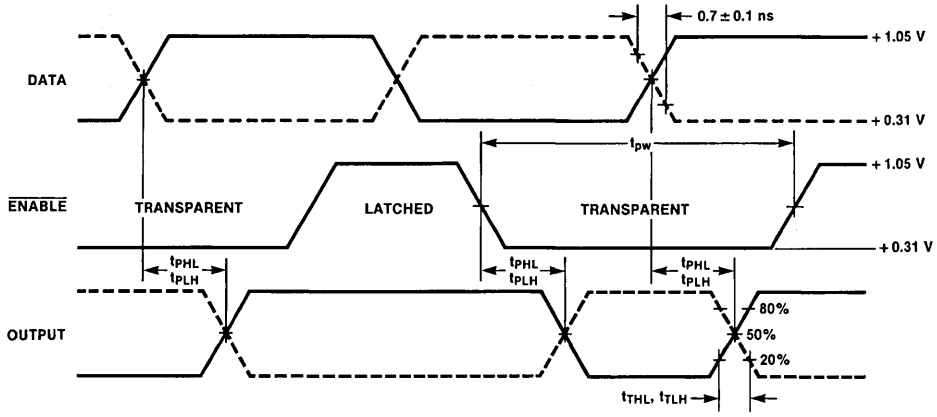
TL/F/9884–5

FIGURE 1. AC Test Circuit

Notes:

V_{CC}, V_{CCA} = +2V, V_{EE} = −2.5V
L1 and L2 = equal length 50Ω impedance lines
R_T = 50Ω terminator internal to scope
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
All unused outputs are loaded with 50Ω to GND
C_L = Fixture and stray capacitance ≤ 3 pF

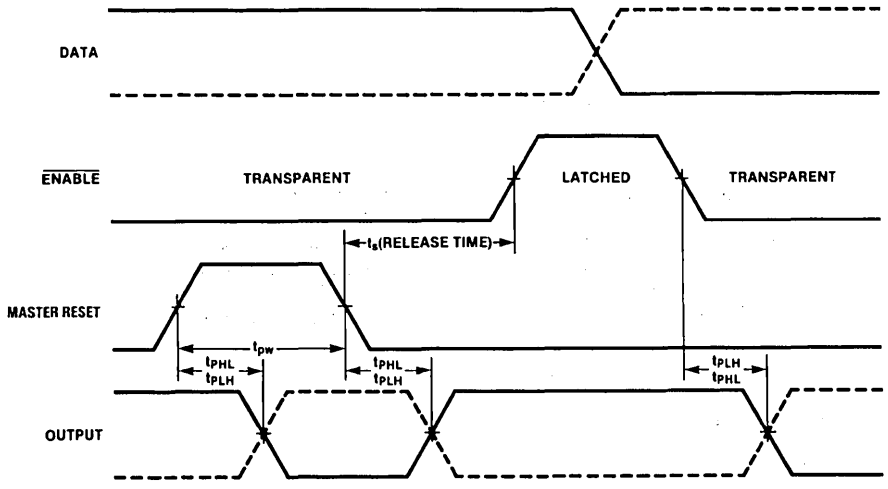
Switching Waveforms



TL/F/9884–6

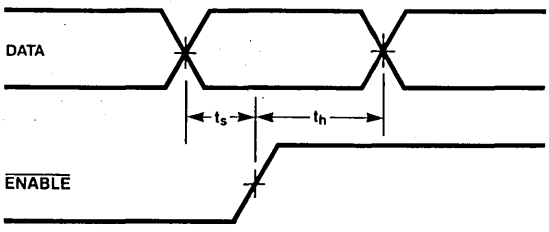
FIGURE 2. Enable Timing

Switching Waveforms (Continued)



TL/F/9884–7

FIGURE 3. Reset Timing



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Notes:

t_s is the minimum time before the transition of the enable that information must be present at the data input.
t_h is the minimum time after the transition of the enable that information must remain unchanged at the data input.

FIGURE 4. Data Setup and Hold Time

National Semiconductor

100351
Low Power Hex D Flip-Flop

General Description

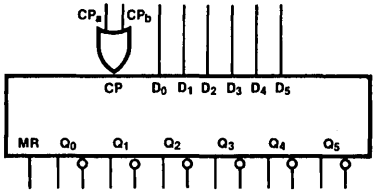
The 100351 contains six D-type edge-triggered, master/slave flip-flops with true and complement outputs, a pair of common Clock inputs (CP_a and CP_b) and common Master Reset (MR) input. Data enters a master when both CP_a and CP_b are LOW and transfers to the slave when CP_a and CP_b (or both) go HIGH. The MR input overrides all other inputs and makes the Q outputs LOW. All inputs have 50 kΩ pull-down resistors.

Features

- 40% power reduction of the 100151
- 2000V ESD protection
- Pin/function compatible with 100151
- Voltage compensated operating range: −4.2V to −5.7V
- Available to industrial grade temperature range

Ordering Code: See Section 6

Logic Symbol

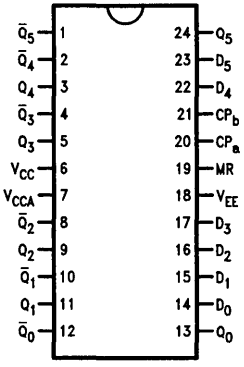


TL/F/9885–11

Pin Names	Description
D_0–D_5	Data Inputs
CP_a, CP_b	Common Clock Inputs
MR	Asynchronous Master Reset Input
Q_0–Q_5	Data Outputs
$\overline{Q}_0$–$\overline{Q}_5$	Complementary Data Outputs

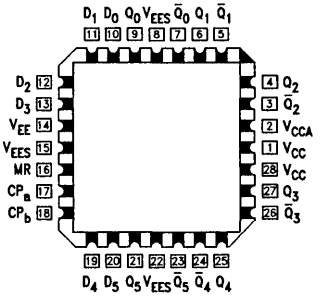
Connection Diagrams

24-Pin DIP/SOIC



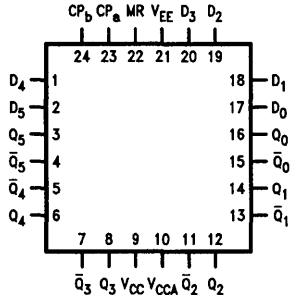
TL/F/9885–1

28-Pin PCC



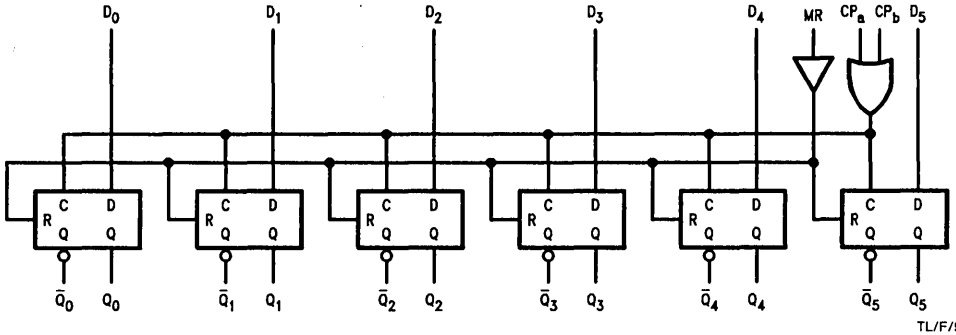
TL/F/9885–3

24-Pin Quad Cerpak



TL/F/9885–2

Logic Diagram



TL/F/9885–4

Truth Tables (Each Flip-flop)

Synchronous Operation

Inputs				Outputs
D_n	CP_a	CP_b	MR	$Q_n(t+1)$
L	↗	L	L	L
H	↗	L	L	H
L	L	↗	L	L
H	L	↗	L	H
X	H	↗	L	$Q_n(t)$
X	↗	H	L	$Q_n(t)$
X	L	L	L	$Q_n(t)$

Asynchronous Operation

Inputs				Outputs
D_n	CP_a	CP_b	MR	$Q_n(t+1)$
X	X	X	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
t = Time before CP positive transition
t+1 = Time after CP positive transition
↗ = LOW-to-HIGH transition

Absolute Maximum Ratings

Above which the useful life may be impaired (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature (T_{STG})	−65°C to +150°C
Maximum Junction Temperature (T_J)	
Ceramic	+175°C
Plastic	+150°C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Output Current (DC Output HIGH)	−50 mA
ESD (Note 2)	≥2000V

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: ESD testing conforms to MIL-STD-883, Method 3015.

Recommended Operating Conditions

Case Temperature (T_C)	
Commercial	0°C to +85°C
Industrial	−40°C to +85°C
Military	−55°C to +125°C
Supply Voltage (V_{EE})	−5.7V to −4.2V

Commercial Version

DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions	
V_{OH}	Output HIGH Voltage	−1025	−955	−870	mV	V_{IN} = V_{IH} (Max) or V_{IL} (Min)	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830	−1705	−1620			
V_{OHC}	Output HIGH Voltage	−1035			mV	V_{IN} = V_{IH} (Min) or V_{IL} (Max)	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610			
V_{IH}	Input HIGH Voltage	−1165		−870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1830		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = V_{IL} (Min)	
I_{IH}	Input HIGH Current MR D_0–D_5 CP_a, CP_b			 350 240 350	μA	V_{IN} = V_{IH} (Max)	
I_{EE}	Power Supply Current	−129		−62	mA	Inputs Open	

Note 3: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DIP AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
f_{max}	Toggle Frequency	375		375		375		MHz	*Figures 2* and *3*
t_{PLH} t_{PHL}	Propagation Delay CP_a, CP_b to Output	0.80	2.00	0.80	2.0	0.90	2.10	ns	*Figures 1* and *3*
t_{PLH} t_{PHL}	Propagation Delay MR to Output	1.10	2.30	1.10	2.30	1.20	2.40	ns	*Figures 1* and *4*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.35	1.20	0.35	1.20	0.35	1.20	ns	*Figures 1* and *3*

Commercial Version (Continued)

DIP AC Electrical Characteristics (Continued)

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_S	Setup Time D_0–D_5 MR (Release Time)	 0.40 1.60		 0.40 1.60		 0.40 1.60		ns	*Figure 5* *Figure 4*
t_H	Hold Time D_0–D_5	0.80		0.80		0.80		ns	*Figure 5*
$t_{pw}(H)$	Pulse Width HIGH CP_a, CP_b, MR	2.00		2.00		2.00		ns	*Figures 3* and *4*

SOIC, PCC and Cerpak AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
f_{max}	Toggle Frequency	375		375		375		MHz	*Figures 2* and *3*
t_{PLH} t_{PHL}	Propagation Delay CP_a, CP_b to Output	0.80	1.80	0.80	1.80	0.90	1.90	ns	*Figures 1* and *3*
t_{PLH} t_{PHL}	Propagation Delay MR to Output	1.10	2.10	1.10	2.10	1.20	2.20	ns	*Figures 1* and *4*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.70	0.45	1.60	0.45	1.70	ns	*Figures 1* and *3*
t_S	Setup Time D_0–D_5 MR (Release Time)	 0.30 1.50		 0.30 1.50		 0.30 1.50		ns	*Figure 5* *Figure 4*
t_H	Hold Time D_0–D_5	0.80		0.80		0.80		ns	*Figure 5*
$t_{pw}(H)$	Pulse Width HIGH CP_a, CP_b, MR	2.00		2.00		2.00		ns	*Figures 3* and *4*
t_{OSHL}	Maximum Skew Common Edge Output-to-Output Variation Clock to Output Path		220		220		220	ps	PCC only (Note 1)
t_{OSLH}	Maximum Skew Common Edge Output-to-Output Variation Clock to Output Path		210		210		210	ps	PCC only (Note 1)
t_{OST}	Maximum Skew Opposite Edge Output-to-Output Variation Clock to Output Path		240		240		240	ps	PCC only (Note 1)
t_{PS}	Maximum Skew Pin (Signal) Transition Variation Clock to Output Path		230		230		230	ps	PCC only (Note 1)

Note 1: Output-to-Output Skew is defined as the absolute value of the difference between the actual propagation delay for any outputs within the same packaged device. The specifications apply to any outputs switching in the same direction either HIGH to LOW (t_{OSHL}), or LOW to HIGH (t_{OSLH}), or in opposite directions both HL and LH (t_{OST}). Parameters t_{OST} and t_{PS} guaranteed by design.

Industrial Version

PCC DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 1)

Symbol	Parameter	T_C = −40°C		T_C = 0° to +85°C		Units	Conditions	
		Min	Max	Min	Max			
V_{OH}	Output HIGH Voltage	−1085	−870	−1025	−870	mV	V_{IN} = V_{IH} (Max) or V_{IL} (Min)	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830	−1575	−1830	−1620			
V_{OHC}	Output HIGH Voltage	−1095		−1035		mV	V_{IN} = V_{IH} (Min) or V_{IL} (Max)	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage		−1565		−1610			
V_{IH}	Input HIGH Voltage	−1170	−870	−1165	−870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1830	−1480	−1830	−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50		0.50		μA	V_{IN} = V_{IL} (Min)	
I_{IH}	Input HIGH Current MR D_0–D_5 CP_a, CP_b		 350 240 350		 350 240 350	μA	V_{IN} = V_{IH} (Max)	
I_{EE}	Power Supply Current	−129	−62	−129	−62	mA	Inputs Open	

Note 1: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

PCC AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = −40°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
f_{max}	Toggle Frequency	375		375		375		MHz	*Figures 2* and *3*
t_{PLH} t_{PHL}	Propagation Delay CP_a, CP_b to Output	0.80	1.80	0.80	1.80	0.90	1.90	ns	*Figures 1* and *3*
t_{PLH} t_{PHL}	Propagation Delay MR to Output	1.10	2.10	1.10	2.10	1.20	2.20	ns	*Figures 1* and *4*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.70	0.45	1.60	0.45	1.70	ns	*Figures 1* and *3*
t_S	Setup Time D_0–D_5 MR (Release Time)	 0.60 2.20		 0.30 1.50		 0.30 1.50		ns	*Figure 5* *Figure 4*
t_H	Hold Time D_0–D_5	0.60		0.90		0.90		ns	*Figure 5*
t_{pw}(H)	Pulse Width HIGH CP_a, CP_b, MR	2.00		2.00		2.00		ns	*Figures 3* and *4*

Military Version—Preliminary

DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = −55°C to +125°C

Symbol	Parameter	Min	Max	Units	T_C	Conditions		Notes
V_{OH}	Output HIGH Voltage	−1025	−870	mV	0°C to +125°C	V_{IN} = V_{IH} (Max) or V_{IL} (Min)	Loading with 50Ω to −2.0V	1, 2, 3
		−1085	−870	mV	−55°C			
V_{OL}	Output LOW Voltage	−1830	−1620	mV	0°C to +125°C			
		−1830	−1555	mV	−55°C			
V_{OHC}	Output HIGH Voltage	−1035		mV	0°C to +125°C	V_{IN} = V_{IH} (Min) or V_{IL} (Max)	Loading with 50Ω to −2.0V	1, 2, 3
		−1085		mV	−55°C			
V_{OLC}	Output LOW Voltage		−1610	mV	0°C to +125°C			
			−1555	mV	−55°C			
V_{IH}	Input HIGH Voltage	−1165	−870	mV	−55°C to +125°C	Guaranteed HIGH Signal for All Inputs		1, 2, 3, 4
V_{IL}	Input LOW Voltage	−1830	−1475	mV	−55°C to +125°C	Guaranteed LOW Signal for All Inputs		1, 2, 3, 4
I_{IL}	Input LOW Current	0.50		μA	−55°C to +125°C	V_{EE} = −4.2V V_{IN} = V_{IL} (Min)		1, 2, 3
I_{IH}	Input HIGH Current CP, MR D_0–D_5		350 240	μA	0°C to +125°C	V_{EE} = −5.7V V_{IN} = V_{IH} (Max)		1, 2, 3
	CP, MR D_0–D_5		500 340	μA	−55°C			
I_{EE}	Power Supply Current	−135	−50	mA	−55°C to +125°C	Inputs Open		1, 2, 3

Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals −55°C), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 2: Screen tested 100% on each device at −55°C, +25°C, and +125°C, Subgroups 1, 2, 3, 7, and 8.

Note 3: Sample tested (Method 5005, Table I) on each manufactured lot at −55°C, +25°C, and +125°C, Subgroups A1, 2, 3, 7, and 8.

Note 4: Guaranteed by applying specified input condition and testing V_{OH}/V_{OL}.

Military Version—Preliminary (Continued)

AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = −55°C		T_C = +25°C		T_C = +125°C		Units	Conditions	Notes
		Min	Max	Min	Max	Min	Max			
f_{max}	Toggle Frequency	375		375		375		MHz	*Figures 2* and *3*	4
t_{PLH} t_{PHL}	Propagation Delay CP_a, CP_b to Output	0.50	2.40	0.60	2.20	0.60	2.60	ns	*Figures 1* and *3*	1, 2, 3
t_{PLH} t_{PHL}	Propagation Delay MR to Output	0.70	2.70	0.80	2.60	0.80	2.90	ns	*Figures 1* and *4*	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.20	1.60	0.20	1.60	0.20	1.60	ns	*Figures 1* and *3*	4
t_s	Setup Time D_0–D_5 MR (Release Time)	 0.90 1.60		 0.80 1.80		 0.90 2.60		ns	*Figure 5* *Figure 4*	
t_h	Hold Time D_0–D_5	1.50		1.40		1.60		ns	*Figure 5*	
$t_{pw}(H)$	Pulse Width HIGH CP_a, CP_b, MR	2.00		2.00		2.00		ns	*Figures 3* and *4*	

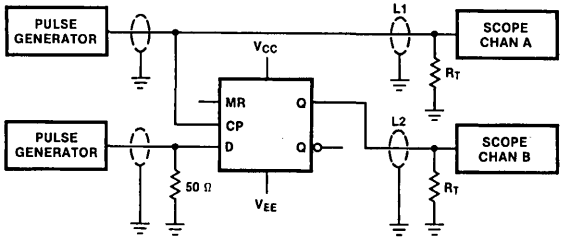
Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals −55°C), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 2: Screen tested 100% on each device at +25°C, Temperature only, Subgroup A9.

Note 3: Sample tested (Method 5005, Table 1) on each Mfg. lot at +25°C, Subgroup A9, and at +125°C, and −55°C Temperature, Subgroups A10 and A11.

Note 4: Not tested at +25°C, +125°C and −55°C Temperature (design characterization data).

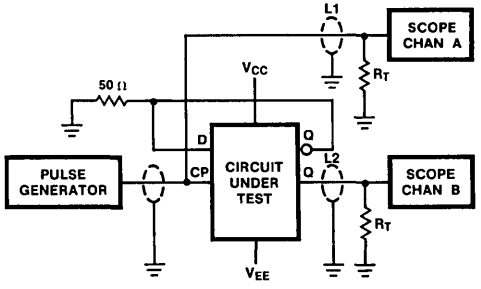
Test Circuitry



Notes:
V_{CC}, V_{CCA} = +2V, V_{EE} = −2.5V
L1 and L2 = equal length 50Ω impedance lines
R_T = 50Ω terminator internal to scope
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
All unused outputs are loaded with 50Ω to GND
C_L = Fixture and stray capacitance ≤ 3 pF

TL/F/9885–5

FIGURE 1. AC Test Circuit

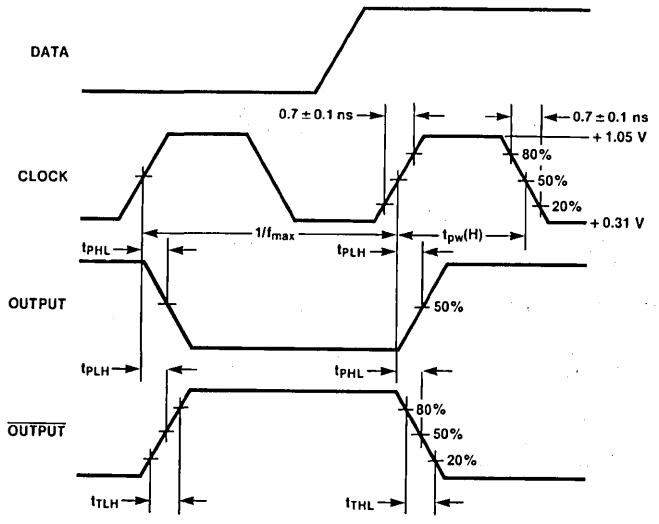


Notes:
V_{CC}, V_{CCA} = +2V, V_{EE} = −2.5V
L1 and L2 = equal length 50Ω impedance lines
R_T = 50Ω terminator internal to scope
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
All unused outputs are loaded with 50Ω to GND
C_L = Jig and stray capacitance ≤ 3 pF

TL/F/9885–6

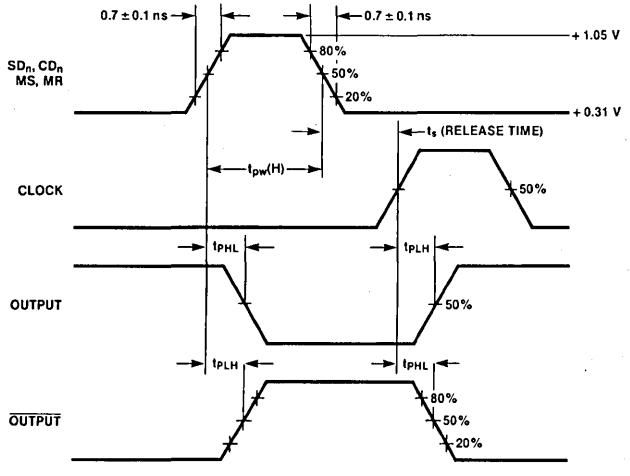
FIGURE 2. Toggle Frequency Test Circuit

Switching Waveforms



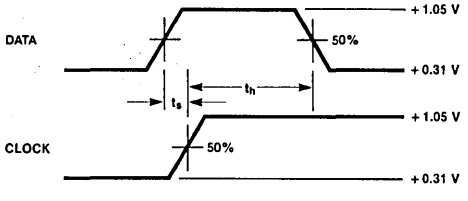
TL/F/9885–7

FIGURE 3. Propagation Delay (Clock) and Transition Times



TL/F/9885–8

FIGURE 4. Propagation Delay (Reset)



TL/F/9885–9

Notes:

t_s is the minimum time before the transition of the clock that information must be present at the data input.

t_h is the minimum time after the transition of the clock that information must remain unchanged at the data input.

FIGURE 5. Setup and Hold Time

National Semiconductor

100352
Low Power 8-Bit Buffer with Cut-Off Drivers

General Description

The 100352 contains an 8-bit buffer, individual inputs (Dn), outputs (Qn), and a data output enable pin ($\overline{OEN}$). A Q output follows its D input when the $\overline{OEN}$ pin is LOW. A HIGH on $\overline{OEN}$ holds the outputs in a cut-off state. The cut-off state is designed to be more negative than a normal ECL LOW level. This allows the output emitter-followers to turn off when the termination supply is −2.0V, presenting a high impedance to the data bus. This high impedance reduces termination power and prevents loss of low state noise margin when several loads share the bus.

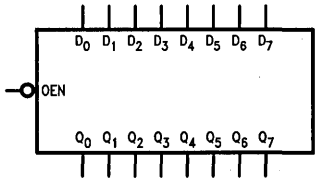
The 100352 outputs are designed to drive a doubly terminated 50Ω transmission line (25Ω load impedance). All inputs have 50 kΩ pull-down resistors.

Features

- Cut-off drivers
- Drives 25Ω load
- Low power operation
- 2000V ESD protection
- Voltage compensated operating range = −4.2V to −5.7V
- Available to industrial grade temperature range
- Available to MIL-STD-883

Ordering Code: See Section 6

Logic Symbol

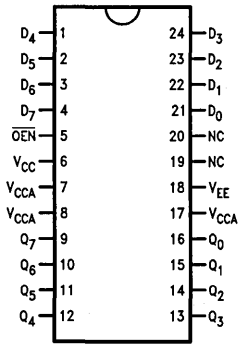


TL/F/10248–1

Pin Names	Description
D_0–D_7	Data Inputs
$\overline{OEN}$	Output Enable Input
Q_0–Q_7	Data Outputs
NC	No Connect

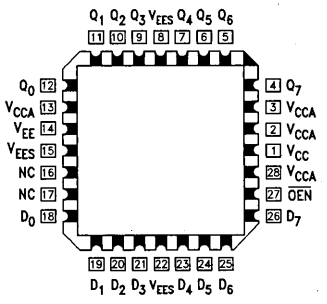
Connection Diagrams

24-Pin DIP



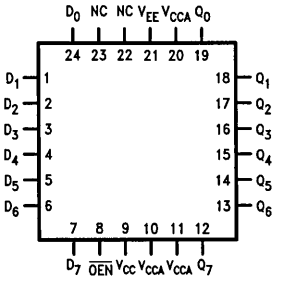
TL/F/10248–2

28-Pin PCC



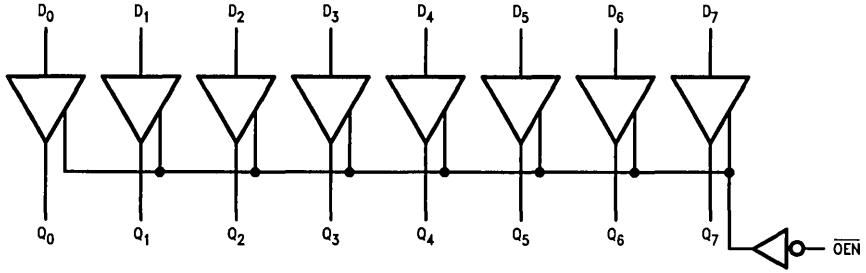
TL/F/10248–4

24-Pin Quad Cerpak



TL/F/10248–3

Logic Diagram



TL/F/10248–5

Truth Table

Inputs		Outputs
Dn	$\overline{OEN}$	Qn
L	L	L
H	L	H
X	H	Cutoff

H = HIGH Voltage Level
L = LOW Voltage Level
Cutoff = Lower-than-LOW State
X = Don't Care

Absolute Maximum Ratings

Above which the useful life may be impaired (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature (T_{STG})	−65°C to +150°C
Maximum Junction Temperature (T_J)	
Ceramic	+175°C
Plastic	+150°C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Output Current (DC Output HIGH)	−100 mA
ESD (Note 2)	≥2000V

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: ESD testing conforms to MIL-STD-883, Method 3015.

Recommended Operating Conditions

Case Temperature (T_C)	
Commercial	0°C to +85°C
Industrial	−40°C to +85°C
Military	−55°C to +125°C
Supply Voltage (V_{EE})	−5.7V to −4.2V

Commercial Version

DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions	
V_{OH}	Output HIGH Voltage	−1025	−955	−870	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 25Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830	−1705	−1620			
V_{OHC}	Output HIGH Voltage	−1035			mV	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	Loading with 25Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610			
V_{OLZ}	Cut-Off LOW Voltage			−1950	mV	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	$\overline{OEN}$ = HIGH
V_{IH}	Input HIGH Voltage	−1165		−870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1830		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	
I_{IH}	Input HIGH Current			240	μA	V_{IN} = $V_{IH\ (Max)}$	
I_{EE}	Power Supply Current	−138 −143		−70 −70	mA	Inputs Open V_{EE} = −4.2V to −4.8V V_{EE} = −4.2V to −5.7V	

Note 3: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DIP AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Dn to Output	0.70	2.00	0.70	2.00	0.70	2.20	ns	*Figures 1, 2* (Note 4)
t_{PZH}	Propagation Delay	1.60	4.20	1.60	4.20	1.60	4.20	ns	*Figures 1, 2* (Note 4)
t_{PHZ}	$\overline{OEN}$ to Output	1.00	2.70	1.00	2.70	1.00	2.70		
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	2.00	0.45	2.00	0.45	2.00	ns	*Figures 1, 2*

Note 4: The propagation delay specified is for single output switching. Delays may vary up to 300 ps with multiple outputs switching.

Commercial Version (Continued)

PCC and Cerpak AC Electrical Characteristics

V_{EE} = 4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Dn to Output	0.70	1.80	0.70	1.80	0.70	2.00	ns	*Figures 1, 2* (Note 2)
t_{PZH} t_{PHZ}	Propagation Delay $\overline{OEN}$ to Output	1.60 1.00	4.00 2.50	1.60 1.00	4.00 2.50	1.60 1.00	4.00 2.50	ns	*Figures 1, 2* (Note 2)
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.90	0.45	1.90	0.45	1.90	ns	*Figures 1, 2*
t_{OSHL}	Maximum Skew Common Edge Output-to-Output Variation Data to Output Path		230		230		230	ps	PCC only (Note 1)
t_{OSLH}	Maximum Skew Common Edge Output-to-Output Variation Data to Output Path		240		240		240	ps	PCC only (Note 1)
t_{OST}	Maximum Skew Opposite Edge Output-to-Output Variation Data to Output Path		350		350		350	ps	PCC only (Note 1)
t_{PS}	Maximum Skew Pin (Signal) Transition Variation Data to Output Path		350		350		350	ps	PCC only (Note 1)

Note 1: Output-to-Output Skew is defined as the absolute value of the difference between the actual propagation delay for any outputs within the same packaged device. The specifications apply to any outputs switching in the same direction either HIGH to LOW (t_{OSHL}), or LOW to HIGH (t_{OSLH}), or in opposite directions both HL and LH (t_{OST}). Parameters t_{OST} and t_{PS} guaranteed by design.

Note 2: The propagation delay specified is for single output switching. Delays may vary up to 300 ps with multiple outputs switching.

Industrial Version

PCC DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = −40°C to +85°C (Note 3)

Symbol	Parameter	T_C = −40°C		T_C = 0°C to +85°C		Units	Conditions	
		Min	Max	Min	Max			
V_{OH}	Output HIGH Voltage	−1085	−870	−1025	−870	mV	V_{IN} = $V_{IH(Max)}$ or $V_{IL(Min)}$	Loading with 25Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830	−1575	−1830	−1620			
V_{OHC}	Output HIGH Voltage	−1095		−1035		mV	V_{IN} = $V_{IH(Min)}$ or $V_{IL(Max)}$	Loading with 25Ω to −2.0V
V_{OLC}	Output LOW Voltage		−1565		−1610			
V_{OLZ}	Cut-Off LOW Voltage		−1950		−1950	mV	V_{IN} = $V_{IH(Min)}$ or V_{IL} (Max)	$\overline{OEN}$ = HIGH
V_{IH}	Input HIGH Voltage	−1170	−870	−1165	−870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1830	−1480	−1830	−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50		0.50		μA	V_{IN} = $V_{IL(Min)}$	
I_{IH}	Input HIGH Current		340		240	μA	V_{IN} = $V_{IH(Max)}$	
I_{EE}	Power Supply Current	−138 −143	−60 −60	−138 −143	−70 −70	mA	Inputs Open V_{EE} = −4.2V to −4.8V V_{EE} = −4.2V to −5.7V	

Note 3: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

Industrial Version (Continued)

PCC AC Electrical Characteristics

V_{EE} = 4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = −40°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Dn to Output	0.60	1.80	0.70	1.80	0.70	2.00	ns	*Figures 1, 2* (Note 1)
t_{PZH} t_{PHZ}	Propagation Delay $\overline{OEN}$ to Output	1.40 1.00	4.40 2.50	1.60 1.00	4.00 2.50	1.60 1.00	4.00 2.50	ns	*Figures 1, 2* (Note 1)
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.40	2.50	0.45	1.90	0.45	1.90	ns	*Figures 1, 2*

Note 1: The propagation delay specified is for single output switching. Delays may vary up to 300 ps with multiple outputs switching.

Military Version

DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = −55°C to +125°C

Symbol	Parameter	Min	Max	Units	T_C	Conditions		Notes
V_{OH}	Output HIGH Voltage	−1025	−870	mV	0°C to +125°C	V_{IN} = $V_{IH(Max)}$ or $V_{IL(Min)}$	Loading with 25Ω to −2.0V	1, 2, 3
		−1085	−870	mV	−55°C			
V_{OL}	Output LOW Voltage	−1830	−1620	mV	0°C to +125°C			
		−1830	−1555	mV	−55°C			
V_{OHC}	Output HIGH Voltage	−1035		mV	0°C to +125°C	V_{IN} = $V_{IH(Min)}$ or $V_{IL(Max)}$	Loading with 25Ω to −2.0V	1, 2, 3
		−1085		mV	−55°C			
V_{OLC}	Output LOW Voltage		−1610	mV	0°C to +125°C			
			−1555	mV	−55°C			
V_{OLZ}	Cut-Off LOW Voltage		−1950	mV	0°C to +125°C	V_{IN} = $V_{IH(Min)}$, or $V_{IL(Max)}$	$\overline{OEN}$ = HIGH	1, 2, 3
			−1850		−55°C			
V_{IH}	Input HIGH Voltage	−1165	−870	mV	−55°C to +125°C	Guaranteed HIGH signal for All inputs		1, 2, 3, 4
V_{IL}	Input LOW Voltage	−1830	−1475	mV	−55°C to +125°C	Guaranteed LOW signal for All inputs		1, 2, 3, 4
I_{IL}	Input LOW Current	0.50		μA	−55°C to +125°C	V_{EE} = 4.2V V_{IN} = $V_{IL(Min)}$		1, 2, 3
I_{IH}	Input HIGH Current		240	μA	0°C to + 125°C	V_{EE} = −5.7V V_{IN} = $V_{IH(Max)}$		1, 2, 3
			340	μA	−55°C			
I_{EE}	Power Supply Current	−145 −150	−55	mA	−55°C to +125°C	Inputs Open V_{EE} = −4.2V to −4.8V V_{EE} = −4.2V to −5.7V		1, 2, 3

Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals −55°C), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 2: Screen tested 100% on each device at −55°C, +25°C, and +125°C, Subgroups 1, 2, 3, 7, and 8.

Note 3: Sample tested (Method 5005, Table I) on each manufactured lot at −55°C, +25°C, and +125°C, Subgroups A1, 2, 3, 7, and 8.

Note 4: Guaranteed by applying specified input condition and testing V_{OH}/V_{OL}.

Military Version (Continued)

AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = −55°C		T_C = +25°C		T_C +125°C		Units	Conditions	Notes
		Min	Max	Min	Max	Min	Max			
t_{PLH} t_{PHL}	Propagation Delay Dn to Output	0.30	2.60	0.50	2.40	0.50	2.70	ns	*Figures 1, 2*	1, 2, 3, 5
t_{PZH} t_{PHZ}	Propagation Delay $\overline{OEN}$ to Output	1.20 0.70	4.40 3.00	1.40 0.70	4.20 2.80	1.20 0.70	4.40 3.20	ns	*Figures 1, 2*	1, 2, 3, 5
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.40	2.50	0.40	2.40	0.40	2.70	ns	*Figures 1, 2*	4

Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals −55°C), then testing immediately after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

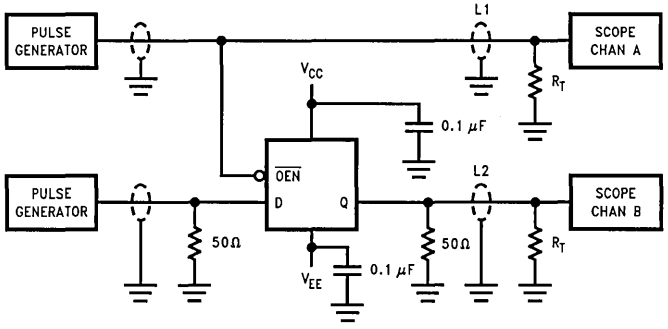
Note 2: Screen tested 100% on each device at +25°C temperature only, Subgroup A9.

Note 3: Sample tested (Method 5005, Table I) on each manufactured lot at +25°C, Subgroup A9, and at +125°C and −55°C temperatures, Subgroups A10 and A11.

Note 4: Not tested at +25°C, +125°C, and −55°C temperature (design characterization data).

Note 5: The propagation delay specified is for single output switching. Delays may vary up to 300 ps with multiple outputs switching.

Test Circuitry

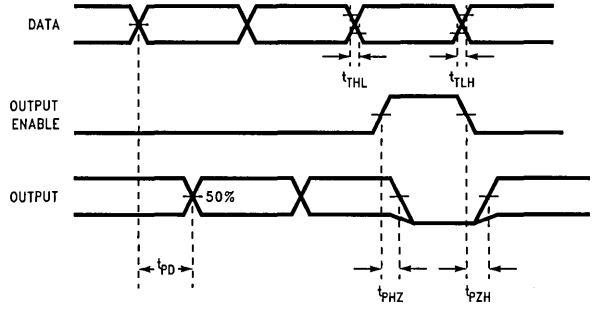


TL/F/10248–6

FIGURE 1. AC Test Circuit

Notes:
V_{CC}, V_{CCA} = +2V, V_{EE} = −2.5V
L1 and L2 = equal length 50Ω impedance lines
R_T = 50Ω terminator internal to scope
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
All unused outputs are loaded with 25Ω to GND
C_L = Fixture and stray capacitance ≤ 3 pF

Switching Waveforms



TL/F/10248–7

Note: The output AC measurement point for cut-off propagation delay testing = the 50% voltage point between active V_{OL} and V_{OH}.

FIGURE 2. Propagation Delay, Cut-Off and Transition Times

National Semiconductor

100353
Low Power 8-Bit Register

General Description

The 100353 contains eight D-type edge triggered, master/slave flip-flops with individual inputs (D_n), true outputs (Q_n), a clock input (CP), and a common clock enable pin ($\overline{CEN}$). Data enters the master when CP is LOW and transfers to the slave when CP goes HIGH. When the $\overline{CEN}$ input goes HIGH it overrides all other inputs, disables the clock, and the Q outputs maintain the last state.

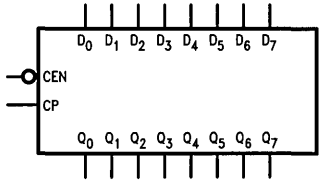
The 100353 output drivers are designed to drive 50Ω termination to −2.0V. All inputs have 50 kΩ pull-down resistors.

Features

- Low power operation
- 2000V ESD protection
- Voltage compensated operating range = −4.2V to −5.7V
- Available to industrial grade temperature range

Ordering Code: See Section 6

Logic Symbol

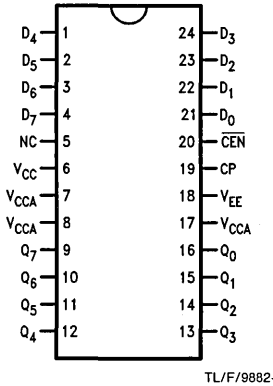


TL/F/9882–4

Pin Names	Description
D_0–D_7	Data Inputs
$\overline{CEN}$	Clock Enable Input
CP	Clock Input (Active Rising Edge)
Q_0–Q_7	Data Outputs
NC	No Connect

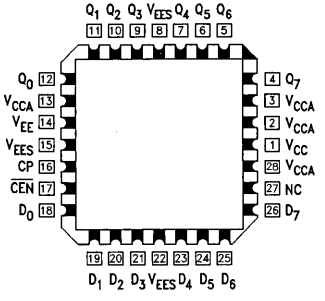
Connection Diagrams

24-Pin DIP



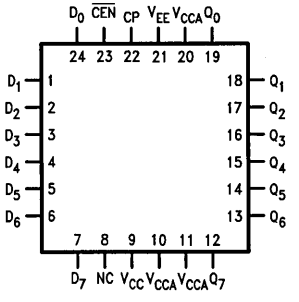
TL/F/9882–1

28-Pin PCC



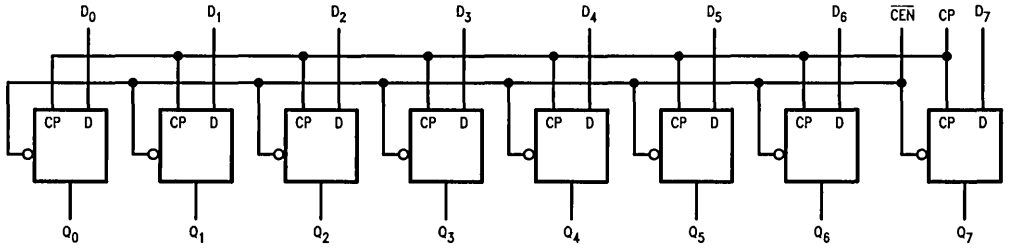
TL/F/9882–3

24-Pin Quad Cerpak



TL/F/9882–2

Logic Diagram



TL/F/9862–5

Truth Table

Inputs			Outputs
D_n	$\overline{CEN}$	CP	Q_n
L	L	⌐	L
H	L	⌐	H
X	X	L	NC
X	X	H	NC
X	H	X	NC

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
NC = No Change
⌐ = LOW to HIGH Transition

Absolute Maximum Ratings

Above which the useful life may be impared (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature (T_{STG})	−65°C to +150°C
Maximum Junction Temperature (T_J)	
Ceramic	+175°C
Plastic	+150°C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
Input Voltage (DC)	V_{EE} to + 0.5V
Output Current (DC Output HIGH)	−50 mA
ESD (Note 2)	≥2000V

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: ESD testing conforms to MIL-STD-883, Method 3015.

Recommended Operating Conditions

Case Temperature (T_C)	
Commercial	0°C to +85°C
Industrial	−40°C to +85°C
Military	−55°C to +125°C
Supply Voltage (V_{EE})	−5.7V to −4.2V

Commercial Version

DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions	
V_{OH}	Output HIGH Voltage	−1025	−955	−870	mV	V_{IN} = V_{IH} (Max) or V_{IL} (Min)	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830	−1705	−1620	mV		
V_{OHC}	Output HIGH Voltage	−1035			mV	V_{IN} = V_{IH} (Min) or V_{IL} (Max)	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610	mV		
V_{IH}	Input HIGH Voltage	−1165		−870	mV	Guaranteed HIGH Signal for all Inputs	
V_{IL}	Input LOW Voltage	−1830		−1475	mV	Guaranteed LOW Signal for all Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = V_{IL} (Min)	
I_{IH}	Input HIGH Current			240	μA	V_{IN} = V_{IH}(Max)	
I_{EE}	Power Supply Current	−119		−61	mA	Inputs Open; V_{EE} = −4.2V to −4.8V	
		−122		−61		V_{EE} = −4.2V to −5.7V	

Note 3: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DIP AC Electrical Characteristics V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
f_{max}	Toggle Frequency	425		425		425		MHz	*Figures 1, 2*
t_{PLH} t_{PHL}	Propagation Delay CP to Output	1.40	3.00	1.40	3.00	1.50	3.10	ns	*Figures 1, 2* (Note 4)
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	2.00	0.45	2.00	0.45	2.00	ns	*Figures 1, 2*
t_s	Setup Time								
	D_n	1.10		1.10		1.10		ns	*Figures 1, 3*
	$\overline{CEN}$ (Disable Time)	0.40		0.40		0.40			
	$\overline{CEN}$ (Release Time)	1.10		1.10		1.10			
t_h	Hold Time								
	D_n	0.10		0.10		0.10		ns	*Figures 1, 4*
t_{pw}(H)	Pulse Width HIGH								
	CP	2.00		2.00		2.00		ns	*Figures 1, 2*

Note 4: The propagation delay specified is for single output switching. Delays may vary up to 300 ps with multiple outputs switching.

Commercial Version (Continued)

PCC and Cerpack AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
f_{max}	Toggle Frequency	425		425		425		MHz	*Figures 1, 2*
t_{PLH} t_{PHL}	Propagation Delay CP to Output	1.40	2.80	1.40	2.80	1.50	2.90	ns	*Figures 1, 2* (Note 2)
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.90	0.45	1.90	0.45	1.90	ns	*Figures 1, 2*
t_s	Setup Time D_n $\overline{CEN}$ (Disable Time) $\overline{CEN}$ (Release Time)	 1.00 0.30 1.00		 1.00 0.30 1.00		 1.00 0.30 1.00		ns	*Figures 1, 3*
t_h	Hold Time D_n	0		0		0		ns	*Figures 1, 4*
$t_{pw}(H)$	Pulse Width HIGH CP	2.00		2.00		2.00		ns	*Figures 1, 2*
t_{OSHL}	Maximum Skew Common Edge Output-to-Output Variation Data to Output Path		200		200		200	ps	PCC Only (Note 1)
t_{OSLH}	Maximum Skew Common Edge Output-to-Output Variation Data to Output Path		200		200		200	ps	PCC Only (Note 1)
t_{OST}	Maximum Skew Opposite Edge Output-to-Output Variation Data to Output Path		260		260		260	ps	PCC Only (Note 1)
t_{PS}	Maximum Skew Pin (Signal) Transition Variation Data to Output Path		280		280		280	ps	PCC Only (Note 1)

Note 1: Output-to-Output Skew is defined as the absolute value of the difference between the actual propagation delay for any outputs within the same packaged device. The specifications apply to any outputs switching in the same direction either HIGH to LOW (t_{OSHL}), or LOW to HIGH (t_{OSLH}), or in opposite directions both HL and LH (t_{OST}). Parameters t_{OST} and t_{PS} guaranteed by design.

Note 2: The propagation delay specified is for single output switching. Delays may vary up to 300 ps with multiple outputs switching.

Industrial Version

PCC DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = −40°C to +85°C (Note 1)

Symbol	Parameter	T_C = −40°C		T_C = 0°C to +85°C		Units	Conditions	
		Min	Max	Min	Max			
V_{OH}	Output HIGH Voltage	−1085	−870	−1025	−870	mV	V_{IN} = V_{IH} (Max) or V_{IL} (Min)	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830	−1575	−1830	−1620	mV		
V_{OHC}	Output HIGH Voltage	−1095		−1035		mV	V_{IN} = V_{IH} (Min) or V_{IL} (Max)	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage		−1565		−1610	mV		
V_{IH}	Input HIGH Voltage	−1170	−870	−1165	−870	mV	Guaranteed HIGH Signal for all Inputs	
V_{IL}	Input LOW Voltage	−1830	−1480	−1830	−1475	mV	Guaranteed LOW Signal for all Inputs	
I_{IL}	Input LOW Current	0.50		0.50		μA	V_{IN} = V_{IL} (Min)	
I_{IH}	Input HIGH Current		240		240	μA	V_{IN} = V_{IH} (Max)	
I_{EE}	Power Supply Current	−119 −122	−61 −61	−119 −122	−61 −61	mA	Inputs Open V_{EE} = −4.2V to −4.8V V_{EE} = −4.2V to −5.7V	

Note 1: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

PCC AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = −40°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
f_{max}	Toggle Frequency	425		425		425		MHz	*Figures 1, 2*
t_{PLH} t_{PHL}	Propagation Delay CP to Output	1.40	2.80	1.40	2.80	1.50	2.90	ns	*Figures 1, 2* (Note 2)
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.40	2.50	0.45	1.90	0.45	1.90	ns	*Figures 1, 2*
t_s	Setup Time D_n $\overline{CEN}$ (Disable Time) $\overline{CEN}$ (Release Time)	 0.60 0.90 1.40		 1.00 0.30 1.00		 1.00 0.30 1.00		ns	*Figures 1, 3*
t_h	Hold Time D_n	0.30		0		0		ns	*Figures 1, 4*
t_{pw}(H)	Pulse Width HIGH CP	2.00		2.00		2.00		ns	*Figures 1, 2*

Note 2: The propagation delay specified is for single output switching. Delays may vary up to 300 ps with multiple outputs switching.

Military Version—Preliminary

DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = −55°C to +125°C

Symbol	Parameter	Min	Max	Units	T_C	Conditions	Notes
V_{OH}	Output HIGH Voltage	−1025	−870	mV	0°C to +125°C	V_{IN} = V_{IH} (Max) or V_{IL} (Min) Loading with 50Ω to −2.0V	1, 2, 3
		−1085	−870	mV	−55°C		
V_{OL}	Output LOW Voltage	−1830	−1620	mV	0°C to +125°C		
		−1830	−1555	mV	−55°C		
V_{OHC}	Output HIGH Voltage	−1035		mV	0°C to +125°C	V_{IN} = V_{IH} (Min) or V_{IL} (Max) Loading with 50Ω to −2.0V	1, 2, 3
		−1085		mV	−55°C		
V_{OLC}	Output LOW Voltage		−1610	mV	0°C to +125°C		
			−1555	mV	−55°C		
V_{IH}	Input HIGH Voltage	−1165	−870	mV	−55°C to +125°C	Guaranteed HIGH Signal for all Inputs	1, 2, 3, 4
V_{IL}	Input LOW Voltage	−1830	−1475	mV	−55°C to +125°C	Guaranteed LOW Signal for all Inputs	1, 2, 3, 4
I_{IL}	Input LOW Current	0.50		μA	−55°C to +125°C	V_{EE} = −4.2V V_{IN} = V_{IL} (Min)	1, 2, 3
I_{IH}	Input HIGH Current		240	μA	0°C to +125°C	V_{EE} = −5.7V V_{IN} = V_{IH} (Max)	1, 2, 3
			340	μA	−55°C		
I_{EE}	Power Supply Current	−125 −130	−50	mA	−55°C to +125°C	Inputs Open V_{EE} = −4.2V to −4.8V V_{EE} = −4.2V to −5.7V	1, 2, 3

Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals −55°C), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 2: Screen tested 100% on each device at −55°C, +25°C, and +125°C, Subgroups 1, 2, 3, 7, and 8.

Note 3: Sample tested (Method 5005, Table I) on each manufactured lot at −55°C, +25°C, and +125°C, Subgroups A1, 2, 3, 7, and 8.

Note 4: Guaranteed by applying specified input condition and testing V_{OH}/V_{OL}.

Military Version—Preliminary (Continued)

AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = −55°C		T_C = +25°C		T_C = +125°C		Units	Conditions	Notes
		Min	Max	Min	Max	Min	Max			
f_{max}	Toggle Frequency	400		400		400		MHz	*Figures 1, 2*	4
t_{PLH} t_{PHL}	Propagation Delay CP to Output	0.70	3.30	0.80	3.10	0.80	3.80	ns	*Figures 1, 2*	1, 2, 3, 5
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.40	2.50	0.40	2.40	0.40	2.70	ns		4
t_s	Setup Time									
	D_n	0.60		0.60		0.60				
	$\overline{CEN}$ (Disable Time)	0.90		0.70		0.90		ns	*Figures 1, 3*	4
	$\overline{CEN}$ (Release Time)	1.40		1.40		2.10				
t_h	Hold Time D_n	0.30		0.30		0.30		ns	*Figures 1, 4*	4
t_{pw}(H)	Pulse Width HIGH CP	2.00		2.00		2.00		ns	*Figures 1, 2*	4

Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals −55°C), then testing immediately after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

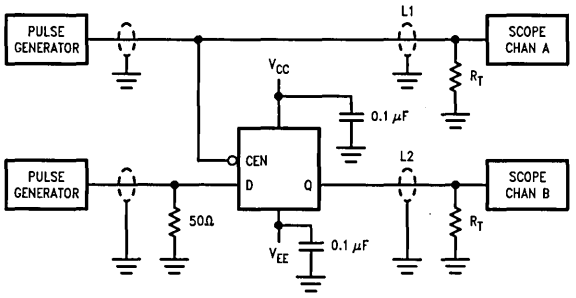
Note 2: Screen tested 100% on each device at +25°C temperature only, Subgroup A9.

Note 3: Sample tested (Method 5005, Table I) on each manufactured lot at +25°C, Subgroup A9, and at +125°C and −55°C, temperatures, Subgroups A10 and A11.

Note 4: Not tested at +25°C, +125°C, and −55°C temperature (design characterization data).

Note 5: The propagation delay specified is for single output switching. Delays may vary up to 300 ps with multiple outputs switching.

Test Circuitry



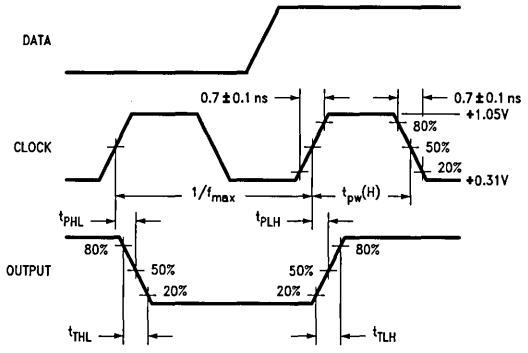
TL/F/9882–6

FIGURE 1. AC, Toggle Frequency Test Circuit

Notes:

V_{CC}, V_{CCA} = +2V, V_{EE} = −2.5V
L1 and L2 = equal length 50Ω impedance lines
R_T = 50Ω terminator internal to scope
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
All unused outputs are loaded with 50Ω to GND
C_L = Fixture and stray capacitance ≤ 3 pF

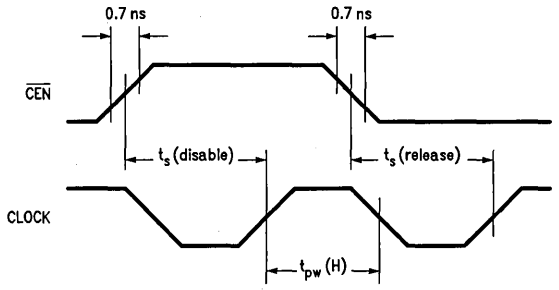
Switching Waveforms



TL/F/9882–8

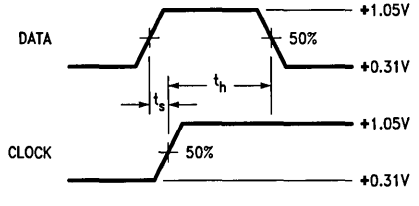
FIGURE 2. Propagation Delay (Clock) and Transition Times

Switching Waveforms (Continued)



TL/F/9882–9

FIGURE 3. Setup and Pulse Width Times



TL/F/9882–10

FIGURE 4. Data Setup and Hold Time

Note 1: t_s is the minimum time before the transition of the clock that information must be present at the data input.

Note 2: t_h is the minimum time after the transition of the clock that information must remain unchanged at the data input.

National Semiconductor

100354
Low Power 8-Bit Register with Cut-Off Drivers

General Description

The 100354 contains eight D-Type edge triggered, master/slave flip-flops with individual inputs (D_n), true outputs (Q_n), a clock input (CP), an output enable pin ($\overline{OEN}$), and a common clock enable pin ($\overline{CEN}$). Data enters the master when CP is LOW and transfers to the slave when CP goes HIGH. When the $\overline{CEN}$ input goes HIGH it overrides all other inputs, disables the clock, and the Q outputs maintain the last state.

A Q output follows its D input when the $\overline{OEN}$ pin is LOW. A HIGH on $\overline{OEN}$ holds the outputs in a cut-off state. The cut-off state is designed to be more negative than a normal ECL LOW level. This allows the output emitter-followers to turn off when the termination supply is −2.0V, presenting a high impedance to the data bus. This high impedance reduces termination power and prevents loss of low state noise margin when several loads share the bus.

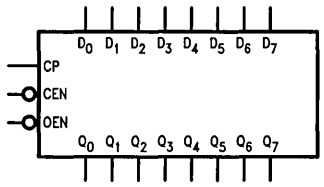
The 100354 outputs are designed to drive a doubly terminated 50Ω transmission line (25Ω load impedance). All inputs have 50 kΩ pull-down resistors.

Features

- Cut-off drivers
- Drives 25Ω load
- Low power operation
- 2000V ESD protection
- Voltage compensated operating range = −4.2V to −5.7V
- Available to industrial grade temperature range

Ordering Code: See Section 6

Logic Symbol

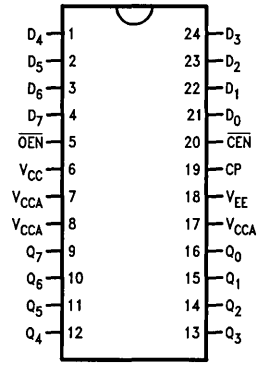


TL/F/10610–1

Pin Names	Description
D_0–D_7	Data Inputs
$\overline{CEN}$	Clock Enable Input
CP	Clock Input (Active Rising Edge)
$\overline{OEN}$	Output Enable Input
Q_0–Q_7	Data Outputs

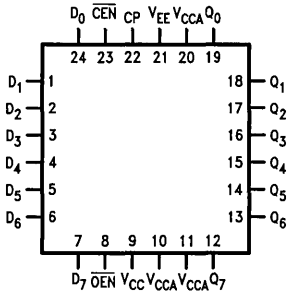
Connection Diagrams

24-Pin DIP



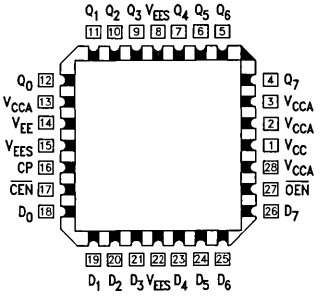
TL/F/10610–2

24-Pin Quad Cerpak



TL/F/10610–3

28-Pin PCC



TL/F/10610–4

Absolute Maximum Ratings

Above which the useful life may be impaired. (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature (T_{STG})	−65°C to +150°C
Maximum Junction Temperature (T_J)	
Ceramic	+175°C
Plastic	+150°C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Output Current (DC Output HIGH)	−100 mA
ESD (Note 2)	≥2000V

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: ESD testing conforms to MIL-STD-883, Method 3015.

Recommended Operating Conditions

Case Temperature (T_C)	
Commercial	0°C to +85°C
Industrial	−40°C to +85°C
Military	−55°C to +125°C
Supply Voltage (V_{EE})	−5.7V to −4.2V

Commercial Version

DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions	
V_{OH}	Output HIGH Voltage	−1025	−955	−870	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 25Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830	−1705	−1620			
V_{OHC}	Output HIGH Voltage	−1035			mV	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	Loading with 25Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610			
V_{OLZ}	Cutoff LOW Voltage			−1950	mV	V_{IN} = V_{IH} (Min) or V_{IL} (Max)	$\overline{OEN}$ = HIGH
V_{IH}	Input HIGH Voltage	−1165		−870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1830		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	
I_{IH}	Input HIGH Current			240	μA	V_{IN} = $V_{IH\ (Max)}$	
I_{EE}	Power Supply Current	−202		−105	mA	Inputs Open V_{EE} = −4.2V to −4.8V	
		−209		−105		V_{EE} = −4.2V to −5.7V	

Note 3: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

Commercial Version (Continued)

DIP AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
f_{Max}	Toggle Frequency	250		250		250		MHz	*Figures 1* and *4*
t_{PLH} t_{PHL}	Propagation Delay CP to Output	1.40	3.00	1.40	3.00	1.50	3.10	ns	*Figures 1* and *4* (Note 1)
t_{PZH} t_{PHZ}	Propagation Delay $\overline{OEN}$ to Output	1.60 1.00	4.20 2.70	1.60 1.00	4.20 2.70	1.60 1.00	4.20 2.70	ns	*Figures 3* and *7* (Note 1)
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	2.00	0.45	2.00	0.45	2.00	ns	*Figures 1* and *4*
t_S	Setup Time D_n $\overline{CEN}$ (Disable Time) $\overline{CEN}$ (Release Time)	 1.10 0.40 1.10		 1.10 0.40 1.10		 1.10 0.40 1.10		ns	*Figures 2* and *5*
t_H	Hold Time D_n	 0.10		 0.10		 0.10		ns	*Figures 1* and *6*
t_{pw}(H)	Pulse Width High CP	 2.00		 2.00		 2.00		ns	*Figures 1* and *4*

Note 1: The propagation delay specified is for single output switching. Delays may vary up to 300 ps with multiple outputs switching.

PCC and Cerpak AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
f_{Max}	Toggle Frequency	250		250		250		MHz	*Figures 1* and *4*
t_{PLH} t_{PHL}	Propagation Delay CP to Output	1.40	2.80	1.40	2.80	1.50	2.90	ns	*Figures 1* and *4* (Note 2)
t_{PZH} t_{PHZ}	Propagation Delay $\overline{OEN}$ to Output	1.60 1.00	4.00 2.50	1.60 1.00	4.00 2.50	1.60 1.00	4.00 2.50	ns	*Figures 3* and *7* (Note 2)
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.90	0.45	1.90	0.45	1.90	ns	*Figures 1* and *4*
t_S	Setup Time D_n $\overline{CEN}$ (Disable Time) $\overline{CEN}$ (Release Time)	 1.00 0.30 1.00		 1.00 0.30 1.00		 1.00 0.30 1.00		ns	*Figures 2* and *5*
t_H	Hold Time D_n	 0.00		 0.00		 0.00		ns	*Figures 1* and *6*
$t_{pw}(H)$	Pulse Width High CP	 2.00		 2.00		 2.00		ns	*Figures 1* and *4*
t_{OSHL}	Maximum Skew Common Edge Output-to-Output Variation Clock to Output Path		 280		 280		 280	ps	PCC Only (Note 1)
t_{OSLH}	Maximum Skew Common Edge Output-to-Output Variation Clock to Output Path		 340		 340		 340	ps	PCC Only (Note 1)
t_{OST}	Maximum Skew Opposite Edge Output-to-Output Variation Clock to Output Path		 340		 340		 340	ps	PCC Only (Note 1)
t_{PS}	Maximum Skew Pin (Signal) Transition Variation Clock to Output Path		 250		 250		 250	ps	PCC Only (Note 1)

Note 1: Output-to-Output Skew is defined as the absolute value of the difference between the actual propagation delay for any outputs within the same packaged device. The specifications apply to any outputs switching in the same direction either HIGH to LOW (t_{OSHL}), or LOW to HIGH (t_{OSLH}), or in oppostie directions both HL and LH (t_{OST}). Parameters t_{OST} and t_{PS} guaranteed by design.

Note 2: The propagation delay specified is for single output switching. Delays may vary up to 300 ps with multiple outputs switching.

Industrial Version

PCC DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = −40°C to +85°C (Note 1)

Symbol	Parameter	T_C = −40°C		T_C = 0° to +85°C		Units	Conditions	
		Min	Max	Min	Max			
V_{OH}	Output HIGH Voltage	−1085	−870	−1025	−870	mV	V_{IN} = V_{IH} (Max) or V_{IL} (Min)	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830	−1575	−1830	−1620			
V_{OHC}	Output HIGH Voltage	−1095		−1035		mV	V_{IN} = V_{IH} (Min) or V_{IL} (Max)	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage		−1565		−1610			
V_{OLZ}	Cutoff LOW Voltage		−1900		−1950	mV	V_{IN} = V_{IH} (Min) or V_{IL} (Max)	$\overline{OEN}$ = HIGH
V_{IH}	Input HIGH Voltage	−1170	−870	−1165	−870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1830	−1480	−1830	−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50		0.50		μA	V_{IN} = V_{IL} (Min)	
I_{IH}	Input HIGH Current		240		240	μA	V_{IN} = V_{IH} (Max)	
I_{EE}	Power Supply Current	−202 −209	−105 −105	−202 −209	−105 −105	mA	Inputs Open V_{EE} = −4.2V to −4.8V V_{EE} = −4.2V to −5.7V	

Note 1: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

PCC AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = −40°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
f_{Max}	Toggle Frequency	250		250		250		MHz	*Figures 1* and *4*
t_{PLH} t_{PHL}	Propagation Delay CP to Output	1.40	2.80	1.40	2.80	1.50	2.90	ns	*Figures 1* and *4* (Note 2)
t_{PZH} t_{PHZ}	Propagation Delay $\overline{OEN}$ to Output	1.50 1.00	4.10 2.50	1.60 1.00	4.00 2.50	1.60 1.00	4.00 2.50	ns	*Figures 3* and *7* (Note 2)
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.90	0.45	1.90	0.45	1.90	ns	*Figures 1* and *4*
t_S	Setup Time D_n $\overline{CEN}$ (Disable Time) $\overline{CEN}$ (Release Time)	 1.00 0.30 1.00		 1.00 0.30 1.00		 1.00 0.30 1.00		ns	*Figures 2* and *5*
t_H	Hold Time D_n	 0.00		 0.00		 0.00		ns	*Figures 1* and *6*
t_{pw}(H)	Pulse Width High CP	 2.00		 2.00		 2.00		ns	*Figures 1* and *4*

Note 2: The propagation delay specified is for single output switching. Delays may vary up to 300 ps with multiple outputs switching.

Military Version—Preliminary

DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = −55°C to +125°C

Symbol	Parameter	Min	Max	Units	T_C	Conditions		Notes
V_{OH}	Output HIGH Voltage	−1025	−870	mV	0°C to +125°C	V_{IN} = V_{IH} (Max) or V_{IL} (Min)	Loading with 25Ω to −2.0V	1, 2, 3
		−1085	−870	mV	−55°C			
V_{OL}	Output LOW Voltage	−1830	−1620	mV	0°C to +125°C			
		−1830	−1555	mV	−55°C			
V_{OHC}	Output HIGH Voltage	−1035		mV	0°C to +125°C	V_{IN} = V_{IH} (Min) or V_{IL} (Max)	Loading with 25Ω to −2.0V	1, 2, 3
		−1085		mV	−55°C			
V_{OLC}	Output LOW Voltage		−1610	mV	0°C to +125°C			
			−1555	mV	−55°C			
V_{OLZ}	Cutoff LOW Voltage		−1950	mV	0°C to +125°C	V_{IN} = V_{IH} (Min) or V_{IL} (Max)	$\overline{OEN}$ = HIGH	1, 2, 3
			−1850		−55°C			
V_{IH}	Input HIGH Voltage	−1165	−870	mV	−55°C to +125°C	Guaranteed HIGH Signal for All Inputs		1, 2, 3, 4
V_{IL}	Input LOW Voltage	−1830	−1475	mV	−55°C to +125°C	Guaranteed LOW Signal for All Inputs		1, 2, 3, 4
I_{IL}	Input LOW Current	0.50		μA	−55°C to +125°	V_{EE} = −4.2V V_{IN} = V_{IL} (Min)		1, 2, 3
I_{IH}	Input HIGH Current		240	μA	0°C to +125°C	V_{EE} = −5.7V V_{IN} = V_{IH} (Max)		1, 2, 3
			340	μA	−55°C			
I_{EE}	Power Supply Current	−215 −225	−85 −85	mA	−55°C to +125°C	Inputs Open V_{EE} = −4.2V to −4.8V V_{EE} = −4.2V to −5.7V		1, 2, 3

Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals −55°C), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 2: Screen tested 100% on each device at −55°C, +25°C, and +125°C, Subgroups 1, 2, 3, 7, and 8.

Note 3: Sample tested (Method 5005, Table I) on each manufactured lot at −55°C, +25°C, and +125°C, Subgroups A1, 2, 3, 7, and 8.

Note 4: Guaranteed by applying specified input condition and testing V_{OH}/V_{OL}.

Military Version—Preliminary (Continued)

AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = −55°C		T_C = +25°C		T_C = +125°C		Units	Conditions	Notes
		Min	Max	Min	Max	Min	Max			
f_{Max}	Toggle Frequency	200		250		200		MHz	*Figures 1* and *4*	4
t_{PLH} t_{PHL}	Propagation Delay CP to Output	0.9	3.70	1.0	3.20	1.20	3.90	ns	*Figures 1* and *4*	1, 2, 3, 5
t_{PZH} t_{PHZ}	Propagation Delay $\overline{OEN}$ to Output	1.20 0.70	5.0 3.0	1.60 0.70	4.20 2.80	1.40 0.70	4.30 3.20	ns	*Figures 3* and *7*	1, 2, 3, 5
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.40	2.50	0.40	2.40	0.40	2.70	ns	*Figures 1* and *4*	4
t_S	Setup Time D_n $\overline{CEN}$ (Disable Time) $\overline{CEN}$ (Release Time)	 1.30 0.60 1.30		 1.30 0.60 1.30		 1.30 0.60 1.30		ns	*Figures 2* and *5*	4
t_H	Hold Time D_n	0.30		0.30		0.30		ns	*Figures 1* and *6*	4
t_{pw}(H)	Pulse Width HIGH CP	2.4		2.4		2.4		ns	*Figures 1* and *4*	4

Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals −55°C), then testing immediately after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

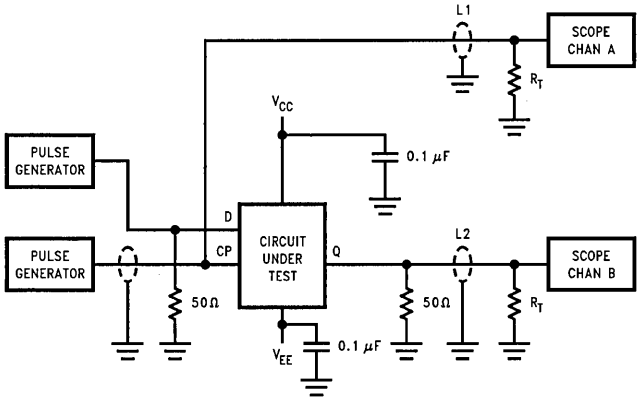
Note 2: Screen tested 100% on each device at +25°C, temperature only, Subgroup A9.

Note 3: Sample tested (Method 5005, Table I) on each manufactured lot at +25°C, Subgroup A9, and at +125°C and −55°C temperatures, Subgroups A10 and A11.

Note 4: Not tested at +25°C, +125°C, and −55°C temperature (design characterization data).

Note 5: The propagation delay specified is for single output switching. Delays may vary up to 300 ps with multiple outputs switching.

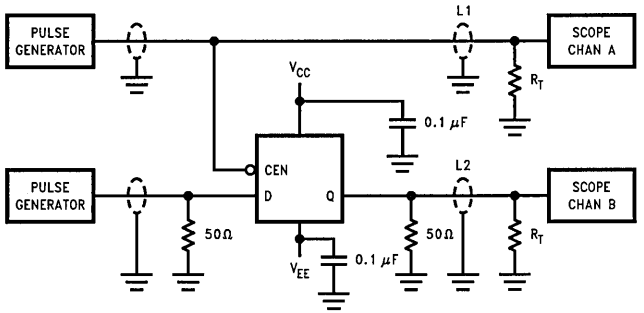
Test Circuitry



TL/F/10610–5

FIGURE 1. Toggle Frequency Test Circuit

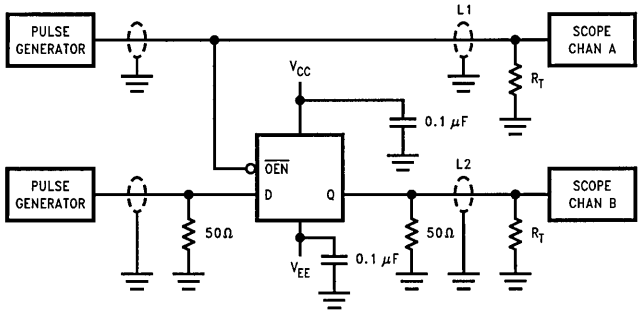
Notes:
V_{CC}, V_{CCA} = +2V, V_{EE} = −2.5V
L1 and L2 = equal length 50Ω impedance lines
R_T = 50Ω terminator internal to scope
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
All unused outputs are loaded with 25Ω to GND
C_L = Fixture and stray capacitance ≤ 3 pF



TL/F/10610–6

FIGURE 2. AC Test Circuit

Notes:
V_{CC}, V_{CCA} = +2V, V_{EE} = −2.5V
L1 and L2 = equal length 50Ω impedance lines
R_T = 50Ω terminator internal to scope
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
All unused outputs are loaded with 25Ω to GND
C_L = Fixture and stray capacitance ≤ 3 pF

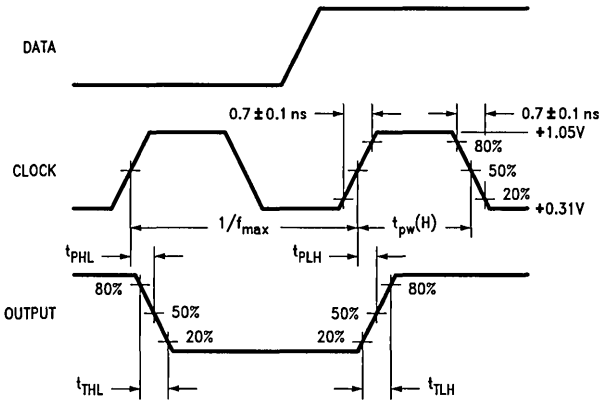


TL/F/10610–7

FIGURE 3. AC Test Circuit

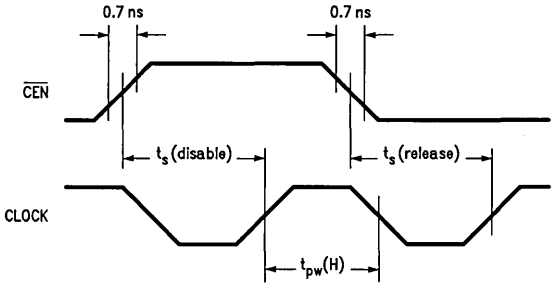
Notes:
V_{CC}, V_{CCA} = +2V, V_{EE} = −2.5V
L1 and L2 = equal length 50Ω impedance lines
R_T = 50Ω terminator internal to scope
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
All unused outputs are loaded with 25Ω to GND
C_L = Fixture and stray capacitance ≤ 3 pF

Switching Waveforms



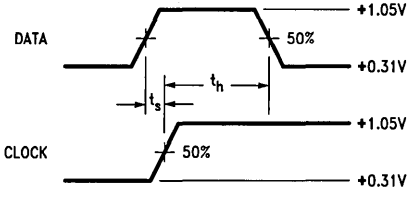
TL/F/10610–8

FIGURE 4. Propagation Delay (Clock) and Transition Times



TL/F/10610–9

FIGURE 5. Setup and Pulse Width Times



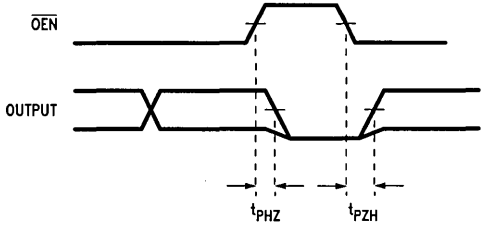
TL/F/10610–10

FIGURE 6. Data Setup and Hold Time

Notes:

t_s is the minimum time before the transition of the clock that information must be present at the data input.

t_h is the minimum time after the transition of the clock that information must remain unchanged at the data input.



TL/F/10610–11

Note: The output AC measurement point for cut-off propagation delay testing = the 50% voltage point between active V_{OL} and V_{OH}.

FIGURE 7. Cutoff Times

National Semiconductor

100355
Low Power Quad Multiplexer/Latch

General Description

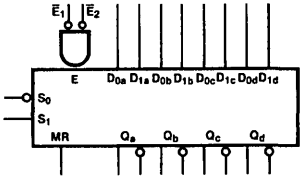
The 100355 contains four transparent latches, each of which can accept and store data from two sources. When both Enable ($\overline{E}_n$) inputs are LOW, the data that appears at an output is controlled by the Select (S_n) inputs, as shown in the Operating Mode table. In addition to routing data from either D_0 or D_1, the Select inputs can force the outputs LOW for the case where the latch is transparent (both Enables are LOW) and can steer a HIGH signal from either D_0 or D_1 to an output. The Select inputs can be tied together for applications requiring only that data be steered from either D_0 or D_1. A positive-going signal on either Enable input latches the outputs. A HIGH signal on the Master Reset (MR) input overrides all the other inputs and forces the Q outputs LOW. All inputs have 50 kΩ pulldown resistors.

Features

- Greater than 40% power reduction of the 100155
- 2000V ESD protection
- Pin/function compatible with 100155
- Voltage compensated operating range = −4.2V to −5.7V
- Available to MIL-STD-883
- Available to industrial grade temperature range

Ordering Code: See Section 6

Logic Symbol

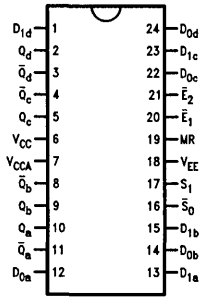


TL/F/10147–1

Pin Names	Description
$\overline{E}_1$, $\overline{E}_2$	Enable Inputs (Active LOW)
$\overline{S}_0$, S_1	Select Inputs
MR	Master Reset
D_{na}–D_{nd}	Data Inputs
Q_a–Q_d	Data Outputs
$\overline{Q}_a$–$\overline{Q}_d$	Complementary Data Outputs

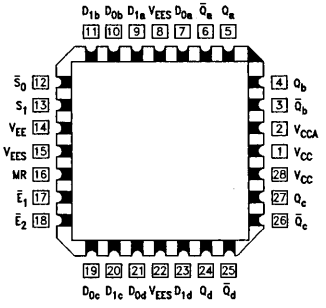
Connection Diagrams

24-Pin DIP



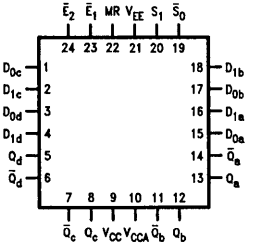
TL/F/10147–2

28-Pin PCC



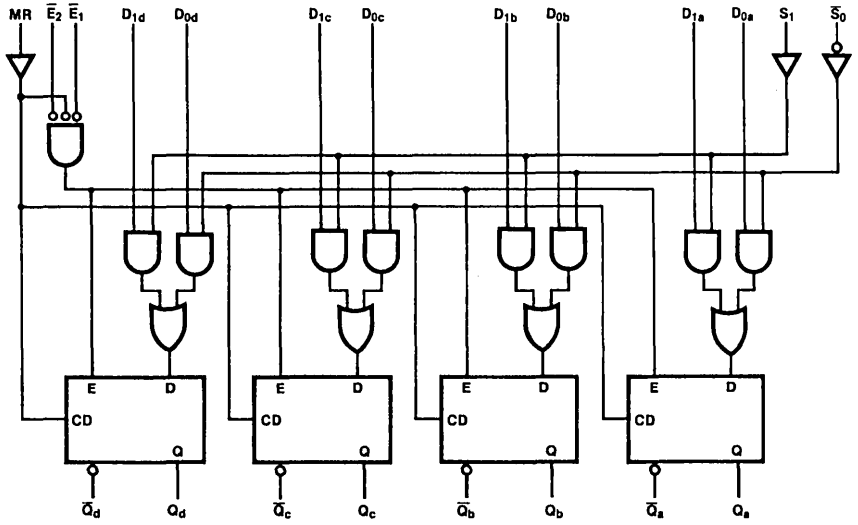
TL/F/10147–4

24-Pin Quad Cerpak



TL/F/10147–3

Logic Diagram



TL/F/10147–5

Operating Mode Table

Controls				Outputs
$\overline{E}_1$	$\overline{E}_2$	S_1	$\overline{S}_0$	Q_n
H	X	X	X	Latched*
X	H	X	X	Latched*
L	L	L	L	D_{0x}
L	L	H	L	$D_{0x} + D_{1x}$
L	L	L	H	L
L	L	H	H	D_{1x}

*Stores data present before $\overline{E}$ went HIGH
H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

Truth Table

Inputs							Outputs	
MR	$\overline{E}_1$	$\overline{E}_2$	S_1	$\overline{S}_0$	D_{1x}	D_{0x}	$\overline{Q}_x$	Q_x
H	X	X	X	X	X	X	H	L
L	L	L	H	H	H	X	L	H
L	L	L	H	H	L	X	H	L
L	L	L	L	L	X	H	L	H
L	L	L	L	L	X	L	H	L
L	L	L	L	H	X	X	H	L
L	L	L	H	L	H	X	L	H
L	L	L	H	L	X	H	L	H
L	L	L	H	L	L	L	H	L
L	H	X	X	X	X	X	Latched*	
L	X	H	X	X	X	X	Latched*	

Absolute Maximum Ratings

Above which the useful life may be impaired. (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature (T_{STG})	−65°C to +150°C
Maximum Junction Temperature (T_J)	
Ceramic	+175°C
Plastic	+150°C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Output Current (DC Output HIGH)	−50 mA
ESD (Note 2)	≥2000V

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: ESD testing conforms to MIL-STD-883, Method 3015.

Recommended Operating Conditions

Case Temperature (T_C)	
Commercial	0°C to +85°C
Industrial	−40°C to +85°C
Military	−55°C to +125°C
Supply Voltage (V_{EE})	−5.7V to −4.2V

Commercial Version

DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions	
V_{OH}	Output HIGH Voltage	−1025	−955	−870	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830	−1705	−1620	mV		
V_{OHC}	Output HIGH Voltage	−1035			mV	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610	mV		
V_{IH}	Input HIGH Voltage	−1165		−870	mV	Guaranteed HIGH Signal for ALL Inputs	
V_{IL}	Input LOW Voltage	−1830		−1475	mV	Guaranteed LOW Signal for ALL Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	
I_{IH}	Input HIGH Current $\overline{S}_0$, S_1 $\overline{E}_1$, $\overline{E}_2$ D_{na}–D_{nd} MR			 220 350 340 430	μA	V_{IN} = $V_{IH\ (Max)}$	
I_{EE}	Power Supply Current	−87		−40	mA	Inputs Open	

Note 3: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

Commercial Version (Continued)

DIP AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay D_{na}–D_{nd} to Output (Transparent Mode)	0.60	1.90	0.60	1.90	0.70	2.00	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay $\overline{S}_0$, S_1 to Output (Transparent Mode)	1.00	2.60	1.00	2.60	1.20	2.70	ns	
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}_1$, $\overline{E}_2$ to Output	0.80	2.00	0.80	2.00	0.80	2.10	ns	
t_{PLH} t_{PHL}	Propagation Delay MR to Output	0.80	2.30	0.80	2.30	0.80	2.30	ns	*Figures 1* and *3*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.60	1.40	0.60	1.40	0.60	1.40	ns	*Figures 1* and *2*
t_S	Setup Time D_{na}–D_{nd} $\overline{S}_0$, S_1 MR (Release Time)	0.90 1.70 1.50		0.90 1.70 1.50		0.90 1.70 1.50		ns	*Figure 4* *Figure 3*
t_H	Hold Time D_{na}–D_{nd} $\overline{S}_0$, S_1	0.40 0.00		0.40 0.00		0.40 0.00		ns	*Figure 4*
t_{pw} (L)	Pulse Width LOW $\overline{E}_1$, $\overline{E}_2$	2.00		2.00		2.00		ns	*Figure 2*
t_{pw} (H)	Pulse Width HIGH MR	2.00		2.00		2.00		ns	*Figure 3*

Commercial Version (Continued)

PCC and Cerpak AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay D_{na}–D_{nd} to Output (Transparent Mode)	0.60	1.70	0.60	1.70	0.70	1.80	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay $\overline{S}_0$, S_1 to Output (Transparent Mode)	1.00	2.40	1.00	2.40	1.20	2.50	ns	
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}_1$, $\overline{E}_2$ to Output	0.80	1.80	0.80	1.80	0.80	1.90	ns	
t_{PLH} t_{PHL}	Propagation Delay MR to Output	0.80	2.10	0.80	2.10	0.80	2.10	ns	*Figures 1* and *3*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.60	1.30	0.60	1.30	0.60	1.30	ns	*Figures 1* and *2*
t_S	Setup Time D_{na}–D_{nd} $\overline{S}_0$, S_1 MR (Release Time)	0.80 1.60 1.40		0.80 1.60 1.40		0.80 1.60 1.40		ns	*Figure 4* *Figure 3*
t_H	Hold Time D_{na}–D_{nd} $\overline{S}_0$, S_1	0.30 −0.10		0.30 −0.10		0.30 −0.10		ns	*Figure 4*
t_{pw} (L)	Pulse Width LOW $\overline{E}_1$, $\overline{E}_2$	2.00		2.00		2.00		ns	*Figure 2*
t_{pw} (H)	Pulse Width HIGH MR	2.00		2.00		2.00		ns	*Figure 3*
t_{OSHL}	Maximum Skew Common Edge Output-to-Output Variation Data to Output Path		330		330		330	ps	PCC only (Note 1)
t_{OSLH}	Maximum Skew Common Edge Output-to-Output Variation Data to Output Path		370		370		370	ps	PCC only (Note 1)
t_{OST}	Maximum Skew Opposite Edge Output-to-Output Variation Data to Output Path		370		370		370	ps	PCC only (Note 1)
tps	Maximum Skew Pin (Signal) Transition Variation Data to Output Path		270		270		270	ps	PCC only (Note 1)

Note 1: Output-to-Output Skew is defined as the absolute value of the difference between the actual propagation delay for any outputs within the same packaged device. The specifications apply to any outputs switching in the same direction either HIGH to LOW (t_{OSHL}), or LOW to HIGH (t_{OSLH}), or in opposite directions both HL and LH (t_{OST}). Parameters t_{OST} and tps guaranteed by design.

Industrial Version

PCC DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = −40°C to +85°C (Note 1)

Symbol	Parameter	T_C = −40°C		T_C = 0°C to +85°C		Units	Conditions	
		Min	Max	Min	Max			
V_{OH}	Output HIGH Voltage	−1085	−870	−1025	−870	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830	−1575	−1830	−1620	mV		
V_{OHC}	Output HIGH Voltage	−1095		−1035		mV	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage		−1565		−1610	mV		
V_{IH}	Input HIGH Voltage	−1170	−870	−1165	−870	mV	Guaranteed HIGH Signal for ALL Inputs	
V_{IL}	Input LOW Voltage	−1830	−1480	1830	1475	mV	Guaranteed LOW Signal for ALL Inputs	
I_{IL}	Input LOW Current	0.50		0.50		μA	V_{IN} = $V_{IL\ (Min)}$	
I_{IH}	Input HIGH Current $\overline{S}_0$, S_1 $\overline{E}_1$, $\overline{E}_2$ D_{na}–D_{nd} MR		 300 350 340 430		 220 350 340 430	μA	V_{IN} = $V_{IH\ (Max)}$	
I_{EE}	Power Supply Current	−87	−40	−87	−40	mA	Inputs Open	

Note 1: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

PCC AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = −40°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay D_{na}–D_{nd} to Output (Transparent Mode)	0.60	1.70	0.60	1.70	0.70	1.80	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay $\overline{S}_0$, S_1 to Output (Transparent Mode)	1.00	2.40	1.00	2.40	1.20	2.50	ns	
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}_1$, $\overline{E}_2$ to Output	0.80	1.80	0.80	1.80	0.80	1.90	ns	
t_{PLH} t_{PHL}	Propagation Delay MR to Output	0.80	2.10	0.80	2.10	0.80	2.10	ns	*Figures 1* and *3*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.40	1.90	0.60	1.30	0.60	1.30	ns	*Figures 1* and *2*
t_S	Setup Time D_{na}–D_{nd} $\overline{S}_0$, S_1 MR (Release Time)	 0.90 2.40 1.50		 0.80 1.60 1.40		 0.80 1.60 1.40		ns	*Figure 4* *Figure 3*
t_H	Hold Time D_{na}–D_{nd} $\overline{S}_0$, S_1	 0.40 0.00		 0.30 −0.10		 0.30 −0.10		ns	*Figure 4*
t_{pw} (L)	Pulse Width LOW $\overline{E}_1$, $\overline{E}_2$	2.00		2.00		2.00		ns	*Figure 2*
t_{pw} (H)	Pulse Width HIGH MR	2.00		2.00		2.00		ns	*Figure 3*

Military Version

DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = −55°C to +125°C

Symbol	Parameter	Min	Max	Units	T_C	Conditions		Notes
V_{OH}	Output HIGH Voltage	−1025	−870	mV	0°C to +125°C	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V	1,2,3
		−1085	−870	mV	−55°C			
V_{OL}	Output LOW Voltage	−1830	−1620	mV	0°C to +125°C			
		−1830	−1555	mV	−55°C			
V_{OHC}	Output HIGH Voltage	−1035		mV	0°C to +125°C	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V	1,2,3
		−1085		mV	−55°C			
V_{OLC}	Output LOW Voltage		−1610	mV	0°C to +125°C			
			−1555	mV	−55°C			
V_{IH}	Input HIGH Voltage	−1165	−870	mV	−55°C to +125°C	Guaranteed HIGH Signal for ALL Inputs		1,2,3,4
V_{IL}	Input LOW Voltage	−1830	−1475	mV	−55°C to +125°C	Guaranteed LOW Signal for ALL Inputs		1,2,3,4
I_{IL}	Input LOW Current	0.50		μA	−55°C to +125°C	V_{EE} = −4.2V V_{IN} = $V_{IL\ (Min)}$		1,2,3
I_{IH}	Input HIGH Current					V_{EE} = −5.7V V_{IN} = $V_{IH\ (Max)}$		1,2,3
	$\overline{S}_0$, S_1		220	μA	0°C to +125°C			
	$\overline{E}_1$, $\overline{E}_2$		350					
	D_{na}–D_{nd}		340					
	MR		430					
	$\overline{S}_0$, S_1		320	μA	−55°C			
	$\overline{E}_1$, $\overline{E}_2$		500					
	D_{na}–D_{nd}		490					
	MR		630					
I_{EE}	Power Supply Current	−95	−32	mA	−55°C to +125°C	Inputs Open		1,2,3

Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals −55°C), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 2: Screen tested 100% on each device at −55°C, +25°C, and +125°C Temp., Subgroups 1, 2, 3, 7, and 8.

Note 3: Sample tested (Method 5005, Table 1) on each Mfg. lot at +25°, +125°C, and −55°C Temp., Subgroups 1, 2, 3, 7, and 8.

Note 4: Guaranteed by applying specified input condition and testing V_{OH}/V_{OL}.

Military Version (Continued)

AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = −55°C		T_C = +25°C		T_C = +125°C		Units	Conditions	Notes
		Min	Max	Min	Max	Min	Max			
t_{PLH} t_{PHL}	Propagation Delay D_{na}–D_{nd} to Output (Transparent Mode)	0.40	2.30	0.50	2.20	0.50	2.60	ns	*Figures 1* and *2*	1,2,3
t_{PLH} t_{PHL}	Propagation Delay $\overline{S}_0$, S_1 to Output (Transparent Mode)	0.60	3.00	0.80	2.70	0.80	3.20	ns		
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}_1$, $\overline{E}_2$ to Output	0.50	2.60	0.60	2.30	0.70	2.70	ns		
t_{PLH} t_{PHL}	Propagation Delay MR to Output	0.60	2.80	0.70	2.60	0.70	2.90	ns	*Figures 1* and *3*	1,2,3
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.40	1.90	0.40	1.90	0.40	1.90	ns	*Figures 1* and *2*	4
t_S	Setup Time D_{na}–D_{nd} $\overline{S}_0$, S_1 MR (Release Time)	 0.90 2.40 1.50		 0.90 2.40 1.50		 0.90 2.40 1.50		ns	*Figure 4* *Figure 3*	4
t_H	Hold Time D_{na}–D_{nd} $\overline{S}_0$, S_1	 0.40 0.00		 0.40 0.00		 0.40 0.00		ns	*Figure 4*	4
t_{pw} (L)	Pulse Width LOW $\overline{E}_1$, $\overline{E}_2$	2.00		2.00		2.00		ns	*Figure 2*	4
t_{pw} (H)	Pulse Width HIGH MR	2.00		2.00		2.00		ns	*Figure 3*	4

Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals −55°C), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 2: Screen tested 100% on each device at +25°C, Temperature only, Subgroup A9.

Note 3: Sample tested (Method 5005, Table 1) on each Mfg. lot at +25°, Subgroup A9, and at +125°C, and −55°C Temp., Subgroups A10 & A11.

Note 4: Not tested at +25°C, +125°C and −55°C Temperature (design characterization data).

Test Circuit

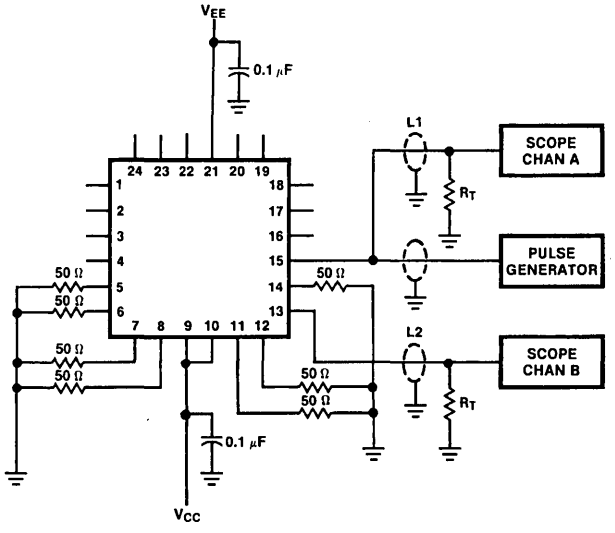


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FIGURE 1. AC Test Circuit (Using Quad Cerpak)

Notes:

V_{CC}, V_{CCA} = +2V, V_{EE} = −2.5V
L1 and L2 = equal length 50Ω impedance lines
R_T = 50Ω terminator internal to scope
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
All unused outputs are loaded with 50Ω to GND
C_L = Fixture and stray capacitance ≤ 3 pF
Pin numbers shown are for flatpak; for DIP see logic symbol

Switching Waveforms

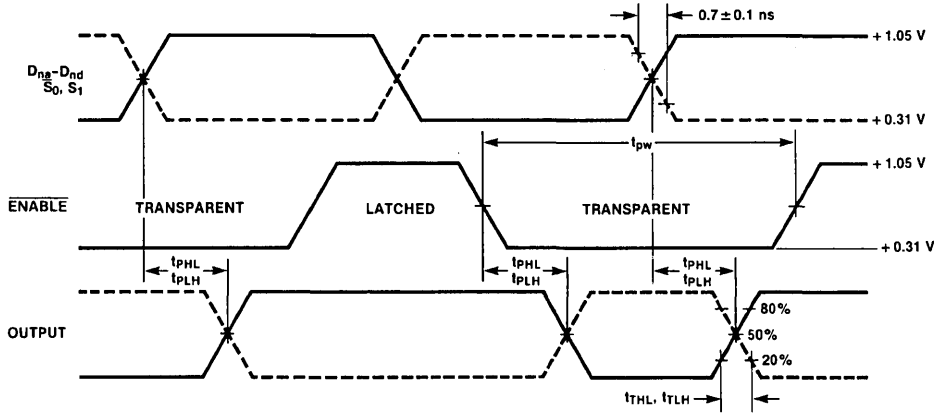

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FIGURE 2. Enable Timing

Switching Waveforms (Continued)

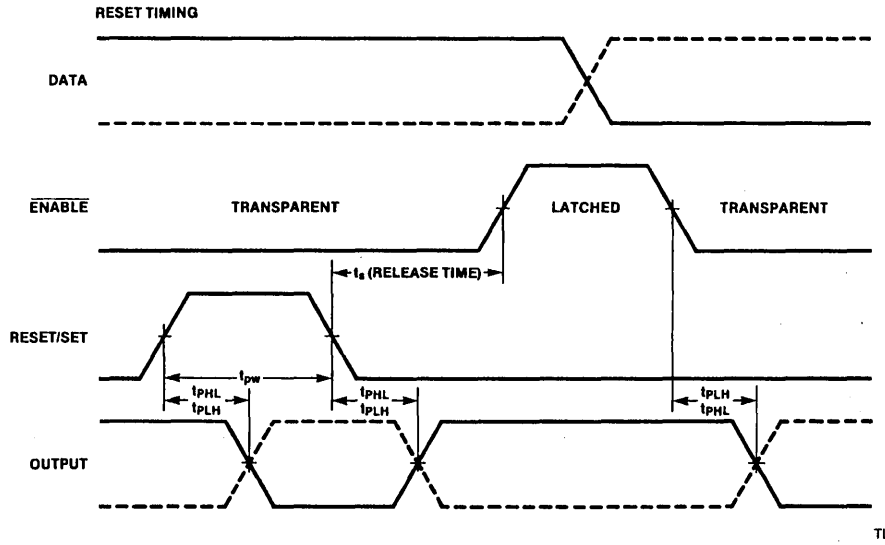

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FIGURE 3. Reset Timing

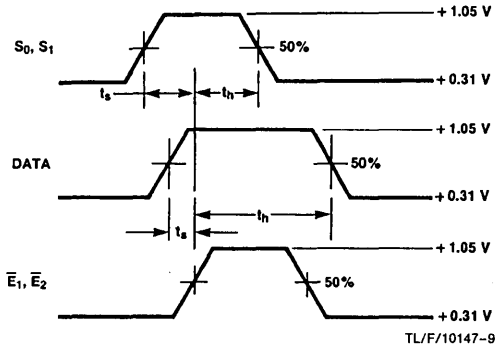

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FIGURE 4. Data Setup and Hold Times

Notes:

t_s is the minimum time before the transition of the enable that information must be present at the data input.

t_h is the minimum time after the transition of the enable that information must remain unchanged at the data input.

National Semiconductor

100360
Low Power Dual Parity Checker/Generator

General Description

The 100360 is a dual parity checker/generator. Each half has nine inputs; the output is HIGH when an even number of inputs are HIGH. One of the nine inputs (I_a or I_b) has the shorter through-put delay and is therefore preferred as the expansion input for generating parity for 16 or more bits.

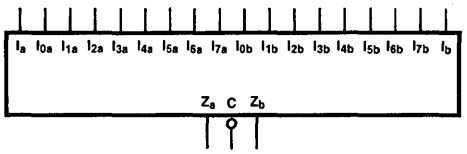
The 100360 also has a Compare ($\overline{C}$) output which allows the circuit to compare two 8-bit words. The $\overline{C}$ output is LOW when the two words match, bit for bit. All inputs have 50 kΩ pulldown resistors.

Features

- Lower power than 100160
- 2000V ESD protection
- Pin/function compatible with 100160
- Voltage compensated operating range = −4.2V to −5.7V
- Min to Max propagation delay 35% tighter than 100160
- Available to industrial grade temperature range

Ordering Code: See Section 6

Logic Symbol

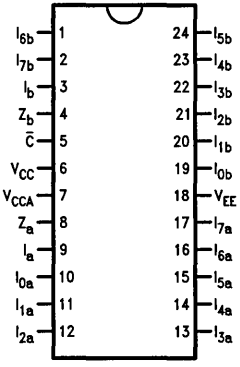


TL/F/10611–1

Pin Names	Description
I_a, I_b, I_{na}, I_{nb}	Data Inputs
Z_a, Z_b	Parity Odd Outputs
$\overline{C}$	Compare Output

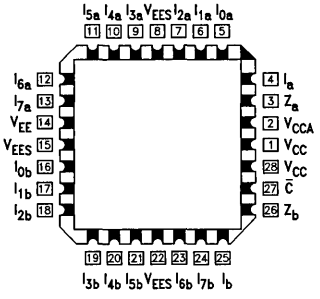
Connection Diagrams

24-Pin DIP



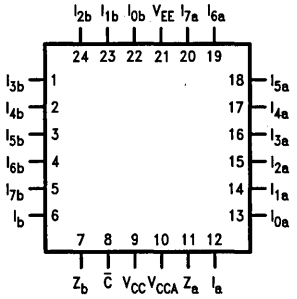
TL/F/10611–2

28-Pin PCC



TL/F/10611–4

24-Pin Quad Cerpak



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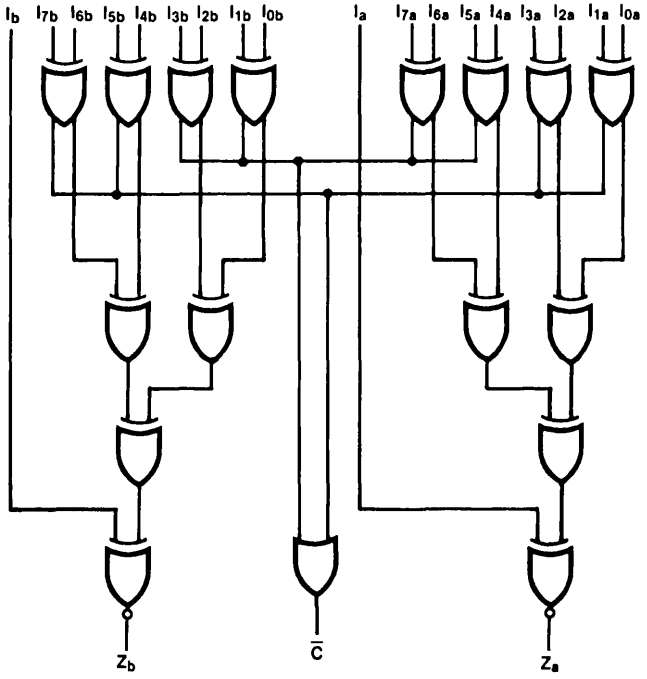
Logic Diagram



TL/F/10611–5

Truth Table (Each Half)

Sum of HIGH Inputs	Output Z
Even	HIGH
Odd	LOW

Comparator Function

$$\overline{C} = (I_{0a} \oplus I_{1a}) + (I_{2a} \oplus I_{3a}) + (I_{4a} \oplus I_{5a}) + (I_{6a} \oplus I_{7a}) + (I_{0b} \oplus I_{1b}) + (I_{2b} \oplus I_{3b}) + (I_{4b} \oplus I_{5b}) + (I_{6b} \oplus I_{7b})$$

Absolute Maximum Ratings

Above which the useful life may be impaired (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature (T_{STG})	−65°C to +150°C
Maximum Junction Temperature (T_J)	
Ceramic	+175°C
Plastic	+150°C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Output Current (DC Output HIGH)	−50 mA
ESD (Note 2)	≥2000V

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: ESD testing conforms to MIL-STD-883, Method 3015.

Recommended Operating Conditions

Case Temperature (T_C)	
Commercial	0°C to +85°C
Industrial	−40°C to +85°C
Military	−55°C to +125°C
Supply Voltage (V_{EE})	−5.7V to −4.2V

Commercial Version

DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions	
V_{OH}	Output HIGH Voltage	−1025	−955	−870	mV	V_{IN} = V_{IH} (Max) or V_{IL} (Min)	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830	−1705	−1620	mV		
V_{OHC}	Output HIGH Voltage	−1035			mV	V_{IN} = V_{IH} (Min) or V_{IL} (Max)	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610	mV		
V_{IH}	Input HIGH Voltage	−1165		−870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1830		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = V_{IL} (Min)	
I_{IH}	Input HIGH Current I_a, I_b I_{na}, I_{nb}			 340 240	μA	V_{IN} = V_{IH} (Max)	
I_{EE}	Power Supply Current	−100		−50	mA	Inputs Open	

Note 3: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DIP AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay I_{na}, I_{nb} to Z_a, Z_b	1.10	2.75	1.10	2.75	1.10	2.75	ns	*Figures 1 & 2*
t_{PLH} t_{PHL}	Propagation Delay I_{na}, I_{nb} to $\overline{C}$	1.10	2.80	1.10	2.80	1.10	2.80	ns	
t_{PLH} t_{PHL}	Propagation Delay I_a, I_b to Z_a, Z_b	0.50	1.20	0.60	1.30	0.60	1.30	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.35	1.10	0.35	1.10	0.35	1.10	ns	

Commercial Version (Continued)

PCC and Cerpak AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay I_{na}, I_{nb} to Z_a, Z_b	1.10	2.75	1.10	2.75	1.10	2.75	ns	*Figures 1 & 2*
t_{PLH} t_{PHL}	Propagation Delay I_{na}, I_{nb} to $\overline{C}$	1.10	2.80	1.10	2.80	1.10	2.80	ns	
t_{PLH} t_{PHL}	Propagation Delay I_a, I_b to Z_a, Z_b	0.50	1.20	0.60	1.30	0.60	1.30	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.35	1.10	0.35	1.10	0.35	1.10	ns	

Industrial Version

PCC DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = −40°C to +85°C (Note 1)

Symbol	Parameter	T_C = −40°C		T_C = 0°C to +85°C		Units	Conditions	
		Min	Max	Min	Max			
V_{OH}	Output HIGH Voltage	−1085	−870	−1025	−870	mV	V_{IN} = V_{IH} (Max) or V_{IL} (Min)	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830	−1575	−1830	−1620	mV		
V_{OHC}	Output HIGH Voltage	−1095		−1035		mV	V_{IN} = V_{IH} (Min) or V_{IL} (Max)	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage		−1565		−1610	mV		
V_{IH}	Input HIGH Voltage	−1170	−870	−1165	−870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1830	−1480	−1830	−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50		0.50		μA	V_{IN} = V_{IL} (Min)	
I_{IH}	Input HIGH Current Ia, Ib Ina, Inb		 340 240		 340 240	μA	V_{IN} = V_{IH} (Max)	
I_{EE}	Power Supply Current	−100	−50	−100	−50	mA	Inputs Open	

Note 1: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

Industrial Version (Continued)

PCC AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = −40°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay I_{na}, I_{nb} to Z_a, Z_b	1.00	2.75	1.10	2.75	1.10	2.75	ns	*Figures 1 & 2*
t_{PLH} t_{PHL}	Propagation Delay I_{na}, I_{nb} to $\overline{C}$	1.00	2.80	1.10	2.80	1.10	2.80	ns	
t_{PLH} t_{PHL}	Propagation Delay I_a, I_b to Z_a, Z_b	0.50	1.20	0.60	1.30	0.60	1.30	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.35	1.10	0.35	1.10	0.35	1.10	ns	

Military Version — Preliminary

DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = −55°C to +125°C

Symbol	Parameter	Min	Max	Units	T_C	Conditions		Notes
V_{OH}	Output HIGH Voltage	−1025	−870	mV	0°C to +125°C	V_{IN} = V_{IH} (Max) or V_{IL} (Min)	Loading with 50Ω to −2.0V	1, 2, 3
		−1085	−870	mV	−55°C			
V_{OL}	Output LOW Voltage	−1830	−1620	mV	0°C to +125°C			
		−1830	−1555	mV	−55°C			
V_{OHC}	Output HIGH Voltage	−1035		mV	0°C to +125°C	V_{IN} = V_{IH} (Min) or V_{IL} (Max)	Loading with 50Ω to −2.0V	1, 2, 3
		−1085		mV	−55°C			
V_{OLC}	Output LOW Voltage		−1610	mV	0°C to +125°C			
			−1555	mV	−55°C			
V_{IH}	Input HIGH Voltage	−1165	−870	mV	−55°C to +125°C	Guaranteed HIGH Signal for All Inputs		1, 2, 3, 4
V_{IL}	Input LOW Voltage	−1830	−1475	mV	−55°C to +125°C	Guaranteed LOW Signal for All Inputs		1, 2, 3, 4
I_{IL}	Input LOW Current	0.50		μA	−55°C to +125°C	V_{EE} = −4.2V V_{IN} = V_{IL} (Min)		1, 2, 3
I_{IH}	Input HIGH Current I_a, I_b I_{na}, I_{nb}		340 240	μA	0°C to +125°C	V_{EE} = −5.7V V_{IN} = V_{IH} (Max)		1, 2, 3
	I_a, I_b I_{na}, I_{nb}		490 340	μA	−55°C			
I_{EE}	Power Supply Current	−110	−50	mA	−55°C to +125°C	Inputs Open		1, 2, 3

Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals −55°C), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 2: Screen tested 100% on each device at −55°C, +25°C, and +125°C, Subgroups 1, 2, 3, 7, and 8.

Note 3: Sample tested (Method 5005, Table I) on each manufactured lot at −55°C, +25°C, and +125°C, Subgroups A1, 2, 3, 7, and 8.

Note 4: Guaranteed by applying specified input condition and testing V_{OH}/V_{OL}.

Military Version — Preliminary (Continued)

AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = −55°C		T_C = +25°C		T_C = +125°C		Units	Conditions	Notes
		Min	Max	Min	Max	Min	Max			
t_{PLH} t_{PHL}	Propagation Delay I_{na}, I_{nb} to Z_a, Z_b	1.00	2.95	1.00	2.95	1.00	2.95	ns	*Figures 1 & 2*	1, 2, 3
t_{PLH} t_{PHL}	Propagation Delay I_{na}, I_{nb} to $\overline{C}$	1.00	3.00	1.00	3.00	1.00	3.00	ns		
t_{PLH} t_{PHL}	Propagation Delay I_a, I_b to Z_a, Z_b	0.40	1.40	0.50	1.50	0.50	1.50	ns		
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.35	1.10	0.35	1.10	0.35	1.10	ns		4

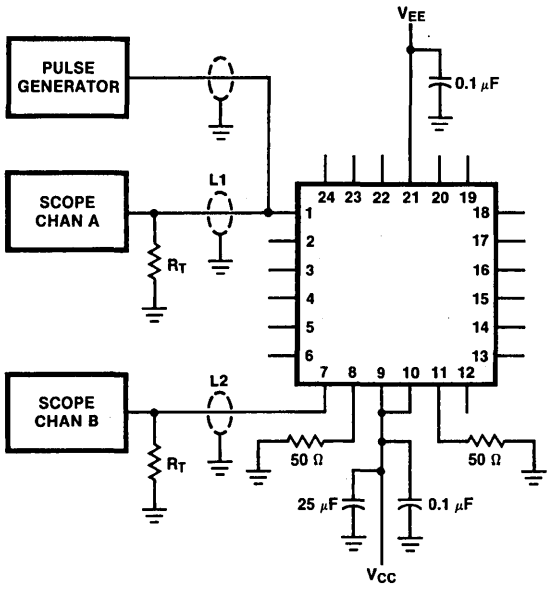
Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals −55°C), then testing immediately after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 2: Screen tested 100% on each device at +25°C temperature only, Subgroup A9.

Note 3: Sample tested (Method 5005, Table I) on each mfg. lot at +25°C, Subgroup A9, and at +125°C and −55°C temperatures, Subgroups A10 and A11.

Note 4: Not tested at +25°C, +125°C, and −55°C temperature (design characterization data).

Test Circuitry

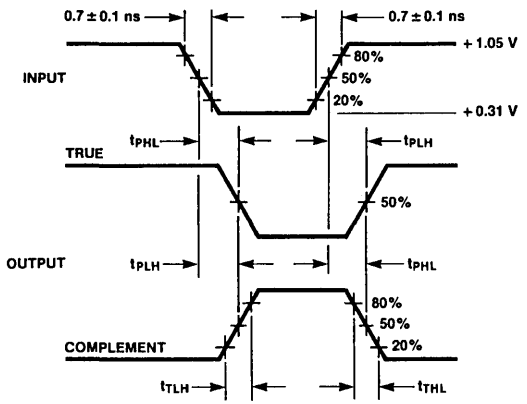


TL/F/10611–6

FIGURE 1. AC Test Circuit

Notes:
V_{CC}, V_{CCA} = +2V, V_{EE} = −2.5V
L1 and L2 = equal length 50Ω impedance lines
R_T = 50Ω terminator internal to scope
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
All unused outputs are loaded with 50Ω to GND
C_L = Fixture and stray capacitance ≤ 3 pF
Pin numbers shown are for flatpak; for DIP see logic symbol

Switching Waveforms



TL/F/10611–7

FIGURE 2. Propagation Delay and Transition Times

National Semiconductor

100363
Low Power Dual 8-Input Multiplexer

General Description

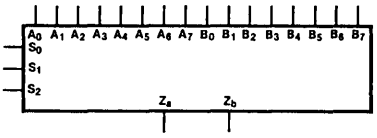
The 100363 is a dual 8-input multiplexer. The Data Select (S_n) inputs determine which bit (A_n and B_n) will be presented at the outputs (Z_a and Z_b respectively). The same bit (0–7) will be selected for both the Z_a and Z_b output. All inputs have 50 kΩ pulldown resistors.

Features

- 50% power reduction of the 100163
- 2000V ESD protection
- Pin/function compatible with 100163
- Voltage compensated operating range = −4.2V to −5.7V
- Available to MIL-STD-883
- Available to industrial grade temperature range

Ordering Code: See Section 6

Logic Symbol

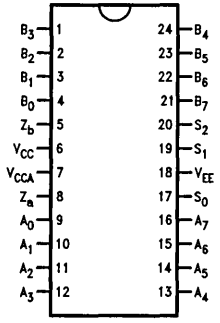


TL/F/10612–1

Pin Names	Description
S_0–S_2	Data Select Inputs
A_0–A_7	A Data Inputs
B_0–B_7	B Data Inputs
Z_a, Z_b	Data Outputs

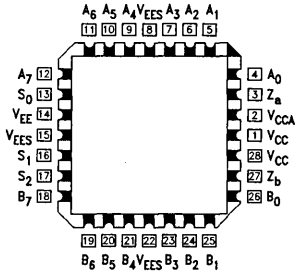
Connection Diagrams

24-Pin DIP



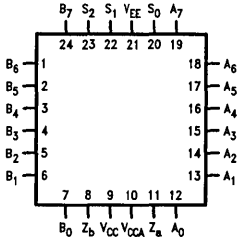
TL/F/10612–2

28-Pin PCC



TL/F/10612–4

24-Pin Quad Cerpak



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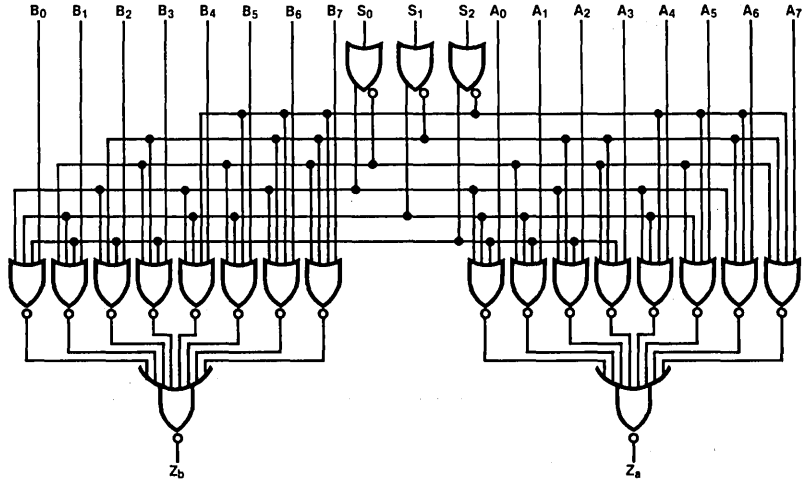
Logic Diagram



TL/F/10612–5

Truth Table

Inputs											Outputs
Select			Data								
S_2	S_1	S_0	A_7 B_7	A_6 B_6	A_5 B_5	A_4 B_4	A_3 B_3	A_2 B_2	A_1 B_1	A_0 B_0	Z_a Z_b
L L	L L	L L								L H	L H
L L	L L	H H							L H		L H
L L	H H	L L						L H			L H
L L	H H	H H					L H				L H
H H	L L	L L				L H					L H
H H	L L	H H			L H						L H
H H	H H	L L		L H							L H
H H	H H	H H	L H								L H

H = HIGH Voltage Level
L = LOW Voltage Level
Blank = X = Don't Care

Absolute Maximum Ratings

Above which the useful life may be impared (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature (T_{STG})	−65°C to +150°C
Maximum Junction Temperature (T_J)	
Ceramic	+175°C
Plastic	+150°C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
Input Voltage (DC)	V_{EE} to + 0.5V
Output Current (DC Output HIGH)	−50 mA
ESD (Note 2)	≥2000V

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: ESD testing conforms to MIL-STD-883, Method 3015.

Recommended Operating Conditions

Case Temperature (T_C)	
Commercial	0°C to +85°C
Industrial	−40°C to +85°C
Military	−55°C to +125°C
Supply Voltage (V_{EE})	−5.7V to −4.2V

Commercial Version

DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions	
V_{OH}	Output HIGH Voltage	−1025	−955	−870	mV	V_{IN} = V_{IH} (Max) or V_{IL} (Min)	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830	−1705	−1620	mV		
V_{OHC}	Output HIGH Voltage	−1035			mV	V_{IN} = V_{IH} (Min) or V_{IL} (Max)	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610	mV		
V_{IH}	Input HIGH Voltage	−1165		−870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1830		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = V_{IL} (Min)	
I_{IH}	Input HIGH Current S_n A_n, B_n			 265 340	μA	V_{IN} = V_{IH} (Max)	
I_{EE}	Power Supply Current	−80		−40	mA	Inputs Open	

Note 3: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DIP AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay A_0–A_7, B_0–B_7 to Output	0.70	1.65	0.80	1.70	0.80	1.80	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay S_0–S_2 to Output	1.30	2.60	1.40	2.70	1.40	2.70	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.30	0.45	1.30	0.45	1.30	ns	

Commercial Version (Continued)

PCC and Cerpak AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay A_0–A_7, B_0–B_7 to Output	0.70	1.65	0.80	1.70	0.80	1.80	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay S_0–S_2 to Output	1.30	2.60	1.40	2.70	1.40	2.70	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.30	0.45	1.30	0.45	1.30	ns	

Industrial Version

DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = −40°C to +85°C (Note 1)

Symbol	Parameter	T_C = −40°C		T_C = 0°C to +85°C		Units	Conditions	
		Min	Max	Min	Max			
V_{OH}	Output HIGH Voltage	−1085	−870	−1025	−870	mV	V_{IN} = V_{IH} (max) or V_{IL} (min)	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830	−1575	−1830	−1620	mV		
V_{OHC}	Output HIGH Voltage	−1095		−1035		mV	V_{IN} = V_{IH} (min) or V_{IL} (max)	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage		−1565		−1610	mV		
V_{IH}	Input HIGH Voltage	−1170	−870	−1165	−870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1830	−1480	−1830	−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50		0.50		μA	V_{IN} = V_{IL} (min)	
I_{IH}	Input HIGH Current					μA	V_{IN} = V_{IH} (Max)	
	S_n		265		265			
	A_n, B_n		380		340			
I_{EE}	Power Supply Current	−80	−35	−80	−40	mA	Inputs Open	

Note 1: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = −40°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay A_0–A_7, B_0–B_7 to Output	0.60	1.65	0.80	1.70	0.80	1.80	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay S_0–S_2 to Output	1.20	2.60	1.40	2.70	1.40	2.70	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.30	1.90	0.45	1.30	0.45	1.30	ns	

Military Version

DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = −55°C to +125°C

Symbol	Parameter	Min	Max	Units	T_C	Conditions		Note
V_{OH}	Output HIGH Voltage	−1025	−870	mV	0°C to +125°C	V_{IN} = V_{IH} (Max) or V_{IL} (Min)	Loading with 50Ω to −2.0V	1, 2, 3
		−1085	−870	mV	−55°C			
V_{OL}	Output LOW Voltage	−1830	−1620	mV	0°C to +125°C			
		−1830	−1555	mV	−55°C			
V_{OHC}	Output HIGH Voltage	−1035		mV	0°C to +125°C	V_{IN} = V_{IH} (Min) or V_{IL} (Max)	Loading with 50Ω to −2.0V	1, 2, 3
		−1085		mV	−55°C			
V_{OLC}	Output LOW Voltage		−1610	mV	0°C to +125°C			
			−1555	mV	−55°C			
V_{IH}	Input HIGH Voltage	−1165	−870	mV	−55°C to +125°C	Guaranteed HIGH Signal for All Inputs		1, 2, 3, 4
V_{IL}	Input LOW Voltage	−1830	−1475	mV	−55°C to +125°C	Guaranteed LOW Signal for All Inputs		1, 2, 3, 4
I_{IL}	Input LOW Current	0.50		μA	−55°C to +125°C	V_{EE} = −4.2V V_{IN} = V_{IL} (Min)		1, 2, 3
I_{IH}	Input HIGH Current S_n A_n, B_n		265 340	μA	0°C to +125°C	V_{EE} = −5.7V V_{IN} = V_{IH} (Max)		1, 2, 3
	 S_n A_n, B_n		385 490	μA	−55°C			
I_{EE}	Power Supply Current	−87	−30	mA	−55°C to +125°C	Inputs Open		1, 2, 3

Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals −55°C), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 2: Screen tested 100% on each device at −55°C, +25°C, and +125°C, Subgroups 1, 2, 3, 7, and 8.

Note 3: Sample tested (Method 5005, Table I) on each manufactured lot at −55°C, +25°C, and +125°C, Subgroups A1, 2, 3, 7, and 8.

Note 4: Guaranteed by applying specified input condition and testing V_{OH}/V_{OL}.

Military Version (Continued)

AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = −55°C		T_C = +25°C		T_C = +125°C		Units	Conditions	Notes
		Min	Max	Min	Max	Min	Max			
t_{PLH} t_{PHL}	Propagation Delay A_0–A_7, B_0–B_7 to Output	0.50	2.40	0.60	2.30	0.70	3.00	ns	*Figures 1* and *2*	1, 2, 3
t_{PLH} t_{PHL}	Propagation Delay S_0–S_2 to Output	0.80	3.00	0.90	2.80	0.80	3.40	ns		
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.30	1.90	0.40	1.80	0.30	2.10	ns		4

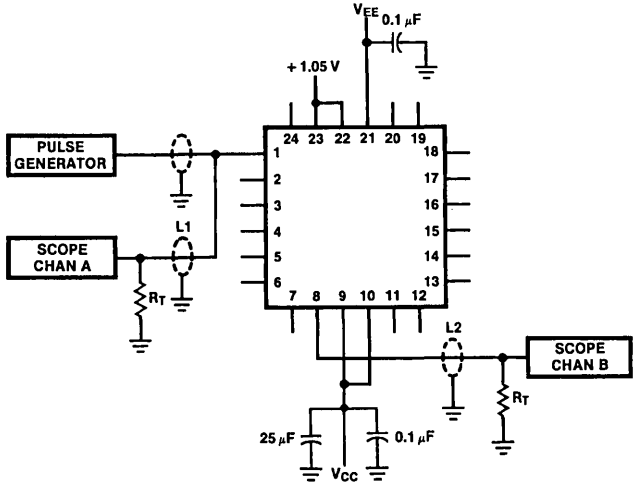
Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals −55°C), then testing immediately after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 2: Screen tested 100% on each device at +25°C temperature only, Subgroup A9.

Note 3: Sample tested (Method 5005, Table I) on each manufactured lot at +25°C, Subgroup A9, and at +125°C and −55°C, temperatures, Subgroups A10 and A11.

Note 4: Not tested at +25°C, +125°C, and −55°C temperature (design characterization data).

Test Circuitry

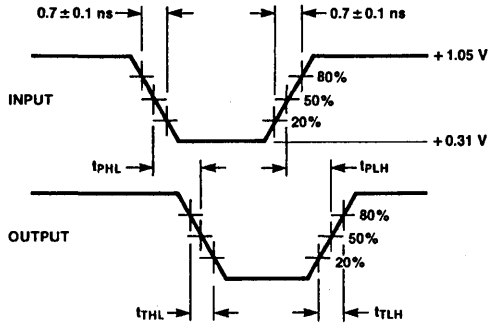


TL/F/10612–6

FIGURE 1. AC Test Circuit

Notes:
V_{CC}, V_{CCA} = +2V, V_{EE} = −2.5V
L1 and L2 = equal length 50Ω impedance lines
R_T = 50Ω terminator internal to scope
Decoupling 0.1 µF from GND to V_{CC} and V_{EE}
All unused outputs are loaded with 50Ω to GND
C_L = Fixture and stray capacitance ≤ 3 pF
Pin numbers shown are for flatpak; for DIP see logic symbol

Switching Waveforms



TL/F/10612–7

FIGURE 2. Propagation Delay and Transition Times

National Semiconductor

100364
Low Power 16-Input Multiplexer

General Description

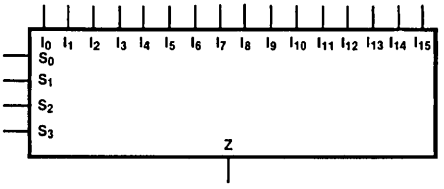
The 100364 is a 16-input multiplexer. Data paths are controlled by four Select lines (S_0–S_3). Their decoding is shown in the truth table. Output data polarity is the same as the seleted input data. All inputs have 50 kΩ pulldown resistors.

Features

- 35% power reduction of the 100164
- 2000V ESD protection
- Pin/function compatible with 100164
- Voltage compensated operating range = −4.2V to −5.7V
- Available to industrial grade temperature range
- Available to MIL-STD-883

Ordering Code: See Section 6

Logic Symbol

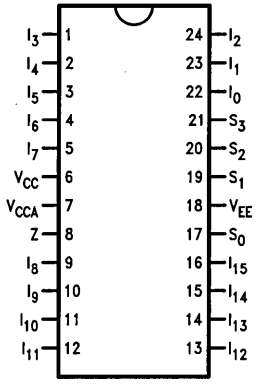


TL/F/10265–1

Pin Names	Description
I_0–I_{15}	Data Inputs
S_0–S_3	Select Inputs
Z	Data Output

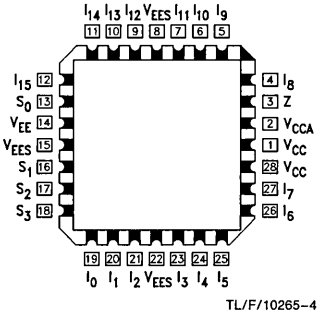
Connection Diagrams

24-Pin DIP



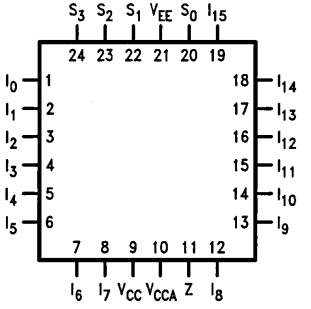
TL/F/10265–2

28-Pin PCC



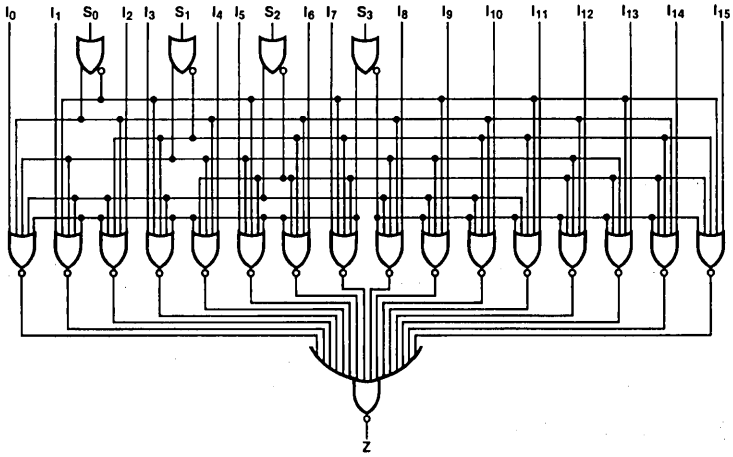
TL/F/10265–4

24-Pin Quad Cerpak



TL/F/10265–3

Logic Diagram



TL/F/10265–5

Truth Table

Select Inputs				Output
S_0	S_1	S_2	S_3	Z
L	L	L	L	I_0
H	L	L	L	I_1
L	H	L	L	I_2
H	H	L	L	I_3
L	L	H	L	I_4
H	L	H	L	I_5
L	H	H	L	I_6
H	H	H	L	I_7
L	L	L	H	I_8
H	L	L	H	I_9
L	H	L	H	I_{10}
H	H	L	H	I_{11}
L	L	H	H	I_{12}
H	L	H	H	I_{13}
L	H	H	H	I_{14}
H	H	H	H	I_{15}

H = HIGH Voltage Level
L = LOW Voltage Level

Absolute Maximum Ratings

Above which the useful life may be impaired (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature (T_{STG})	−65°C to +150°C
Maximum Junction Temperature (T_J)	
Ceramic	+175°C
Plastic	+150°C
Pin Potential to Ground Pin (V_{EE})	−7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Output Current (DC Output HIGH)	−50 mA
ESD (Note 2)	≥ 2000V

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: ESD testing conforms to MIL-STD-883, Method 3015.

Recommended Operating Conditions

Case Temperature (T_C)	
Commercial	0°C to +85°C
Industrial	−40°C to +85°C
Military	−55°C to +125°C
Supply Voltage (V_{EE})	−5.7V to −4.2V

Commercial Version

DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions	
V_{OH}	Output HIGH Voltage	−1025	−955	−870	mV	V_{IN} = V_{IH} (Max) or V_{IL} (Min)	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830	−1705	−1620	mV		
V_{OHC}	Output HIGH Voltage	−1035			mV	V_{IN} = V_{IH} (Min) or V_{IL} (Max)	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610	mV		
V_{IH}	Input HIGH Voltage	−1165		−870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1830		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.5			μA	V_{IN} = V_{IL} (Min)	
I_{IH}	Input HIGH Current			300	μA	V_{IN} = V_{IH} (Max)	
I_{EE}	Power Supply Current	−89		−45	mA	Inputs Open	

Note 3: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operate under "worst case" conditions.

DIP AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay I_0–I_{15} to Output	0.90	2.00	0.90	2.00	0.90	2.10	ns	*Figures 1, 2*
t_{PLH} t_{PHL}	Propagation Delay S_0, S_1 to Output	1.40	2.80	1.40	2.80	1.50	2.90	ns	
t_{PLH} t_{PHL}	Propagation Delay S_2, S_3 to Output	1.00	2.20	1.00	2.20	1.10	2.40	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.35	1.20	0.35	1.20	0.35	1.20	ns	

Commercial Version (Continued)

PCC and Cerpak AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay I_0–I_{15} to Output	0.90	1.80	0.90	1.80	0.90	1.90	ns	*Figures 1, 2*
t_{PLH} t_{PHL}	Propagation Delay S_0, S_1 to Output	1.40	2.60	1.40	2.60	1.50	2.70	ns	
t_{PLH} t_{PHL}	Propagation Delay S_2, S_3 to Output	1.00	2.00	1.00	2.00	1.10	2.20	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.35	1.10	0.35	1.10	0.35	1.10	ns	

Industrial Version

PCC DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = −40°C to +85°C (Note 3)

Symbol	Parameter	T_C = −40°C		T_C = 0°C to +85°C		Units	Conditions	
		Min	Max	Min	Max			
V_{OH}	Output HIGH Voltage	−1085	−870	−1025	−870	mV	V_{IN} = V_{IH} (Max) or V_{IL} (Min)	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830	−1575	−1830	−1620	mV		
V_{OHC}	Output HIGH Voltage	−1095		−1035		mV	V_{IN} = V_{IH} (Min) or V_{IL} (Max)	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage		−1565		−1610	mV		
V_{IH}	Input HIGH Voltage	−1170	−870	−1165	−870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1830	−1480	−1830	−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.5		0.5		μA	V_{IN} = V_{IL} (Min)	
I_{IH}	Input HIGH Current		325		325	μA	V_{IN} = V_{IH} (Max)	
I_{EE}	Power Supply Current	−89	−45	−89	−45	mA	Inputs Open	

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life imparied. Functional operation under these conditions is not implied.

Note 2: ESD testing conforms to MIL-STD-883, Method 3015.

Note 3: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

Industrial Version (Continued)

PCC AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = −40°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay I_0–I_{15} to Output	0.90	1.80	0.90	1.80	0.90	1.90	ns	*Figures 1, 2*
t_{PLH} t_{PHL}	Propagation Delay S_0, S_1 to Output	1.20	2.60	1.40	2.60	1.50	2.70	ns	
t_{PLH} t_{PHL}	Propagation Delay S_2, S_3 to Output	0.80	2.10	1.00	2.00	1.10	2.20	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.20	1.20	0.35	1.10	0.35	1.10	ns	

Military Version

DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = −55°C to +125°C

Symbol	Parameter	Min	Max	Units	T_C	Conditions		Notes
V_{OH}	Output HIGH Voltage	−1025	−870	mV	0°C to +125°C	V_{IN} = V_{IH} (Max) or V_{IL} (Min)	Loading with 50Ω to −2.0V	1, 2, 3
		−1085	−870	mV	−55°C			
V_{OL}	Output LOW Voltage	−1830	−1620	mV	0°C to +125°C			
		−1830	−1555	mV	−55°C			
V_{OHC}	Output HIGH Voltage	−1035		mV	0°C to +125°C	V_{IN} = V_{IH} (Min) or V_{IL} (Max)	Loading with 50Ω to −2.0V	1, 2, 3
		−1085		mV	−55°C			
V_{OLC}	Output LOW Voltage		−1610	mV	0°C to +125°C			
			−1555	mV	−55°C			
V_{IH}	Input HIGH Voltage	−1165	−870	mV	−55°C to +125°C	Guaranteed HIGH Signal for All Inputs		1, 2, 3, 4
V_{IL}	Input LOW Voltage	−1830	−1475	mV	−55°C to +125°C	Guaranteed LOW Signal for All Inputs		1, 2, 3, 4
I_{IL}	Input LOW Current	0.50		μA	−55°C to +125°C	V_{EE} = −4.2V V_{IN} = V_{IL} (Min)		1, 2, 3
I_{IH}	Input HIGH Current		300	μA	0°C to +125°C	V_{EE} = −5.7V V_{IN} = V_{IH} (Max)		1, 2, 3
			450	μA	−55°C			
I_{EE}	Power Supply Current	−95	−35	mA	−55°C to +125°C	Inputs Open		1, 2, 3

Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals −55°C), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 2: Screen tested 100% on each device at −55°C, +25°C, and +125°C, Subgroups, 1, 2, 3, 7 and 8.

Note 3: Sampled tested (Method 5005, Table I) on each manufactured lot at −55°C, +25°C, and +125°C, Subgroups A1, 2, 3, 7 and 8.

Note 4: Guaranteed by applying specified input condition and testing V_{OH}/V_{OL}.

Military Version (Continued)

AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = −55°C		T_C = 25°C		T_C = +125°C		Units	Conditions	Notes
		Min	Max	Min	Max	Min	Max			
t_{PLH} t_{PHL}	Propagation Delay I_0–I_{15} to Output	0.50	2.60	0.60	2.40	0.60	2.80	ns	*Figures 1, 2*	1, 2, 3
t_{PLH} t_{PHL}	Propagation Delay S_0, S_1 to Output	0.70	3.30	0.90	3.10	1.00	3.50	ns		
t_{PLH} t_{PHL}	Propagation Delay S_2, S_3 to Output	0.50	2.90	0.70	2.60	0.60	3.00	ns		
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.20	1.20	0.20	1.20	0.20	1.20	ns		4

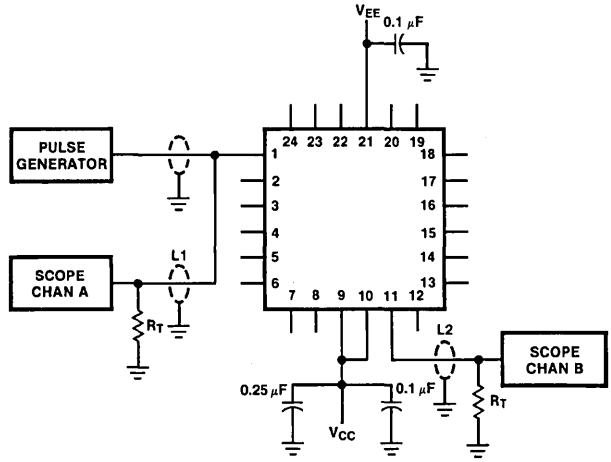
Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals −55°C), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 2: Screen tested 100% on each device at +25°C, temperature only, Subgroup A9.

Note 3: Sample tested (Method 5005, Table I) on each Mfg. lot at +25°C, Subgroup A9, and at +125°C, and −55°C temp., Subgroups A10 and A11.

Note 4: Not tested at +25°C, +125°C and −55°C temperature (design characterization data).

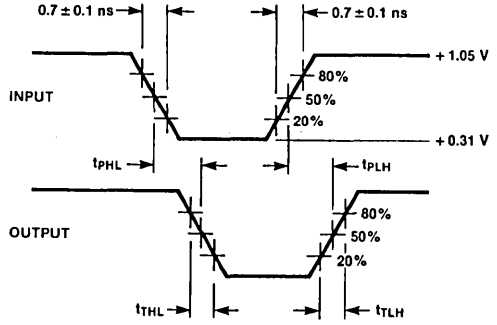
Test Circuit



TL/F/10265–6

FIGURE 1. AC Test Circuit

Switching Waveforms



TL/F/10265–7

FIGURE 2. Propagation Delay and Transition Times

Notes:

V_{CC}, V_{CCA} = +2V, V_{EE} = −2.5V

L1 and L2 = Equal length 50Ω impedance lines

R_T = 50Ω terminator internal to scope

Decoupling 0.1 μF from GND to V_{CC} and V_{EE}

All unused outputs are loaded with 50Ω to GND

C_L = Fixture and stray capacitance ≤ 3 pF

Pin numbers shown are for flatpak; for DIP see logic symbol

National Semiconductor

100370
Low Power Universal Demultiplexer/Decoder

General Description

The 100370 universal demultiplexer/decoder functions as either a dual 1-of-4 decoder or as a single 1-of-8 decoder, depending on the signal applied to the Mode Control (M) input. In the dual mode, each half has a pair of active-LOW Enable ($\overline{E}$) inputs. Pin assignments for the $\overline{E}$ inputs are such that in the 1-of-8 mode they can easily be tied together in pairs to provide two active-LOW enables ($\overline{E}_{1a}$ to $\overline{E}_{1b}$, $\overline{E}_{2a}$ to $\overline{E}_{2b}$). Signals applied to auxiliary inputs H_a, H_b and H_c determine whether the outputs are active HIGH or active LOW. In the dual 1-of-4 mode the Address inputs are A_{0a}, A_{1a} and A_{0b}, A_{1b} with A_{2a} unused (i.e., left open, tied to V_{EE} or with LOW signal applied). In the 1-of-8 mode, the Address inputs are A_{0a}, A_{1a}, A_{2a} with A_{0b} and A_{1b} LOW or open. All inputs have 50 kΩ pulldown resistors.

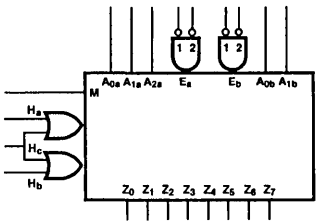
Features

- 35% power reduction of the 100170
- 2000V ESD protection
- Pin/function compatible with 100170
- Voltage compensated operating range = −4.2V to −5.7V

Ordering Code: See Section 6

Logic Symbols

Single 1-of-8 Application



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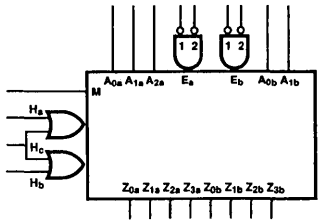
Dual 1-of-4 Application

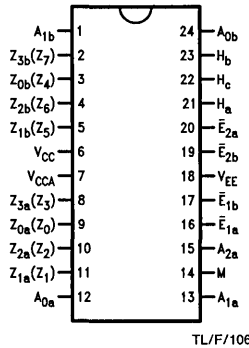


TL/F/10649–4

Pin Names	Description
A_{na}, A_{nb}	Address Inputs
$\overline{E}_{na}$, $\overline{E}_{nb}$	Enable Inputs
M	Mode Control Input
H_a	Z_0–Z_3 ($\overline{Z}_{0a}$–$\overline{Z}_{3a}$) Polarity Select Input
H_b	Z_4–Z_7 ($\overline{Z}_{0b}$–$\overline{Z}_{3b}$) Polarity Select Input
H_c	Common Polarity Select Input
Z_0–Z_7	Single 1-of-8 Data Outputs
Z_{na}, Z_{nb}	Dual 1-of-4 Data Outputs

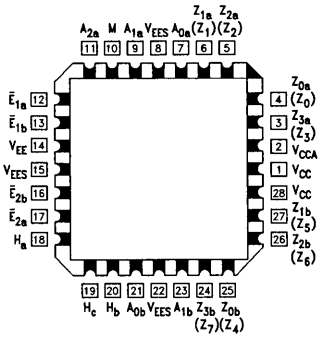
Connection Diagrams

24-Pin DIP



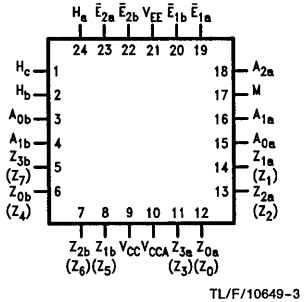
TL/F/10649–2

28-Pin PCC



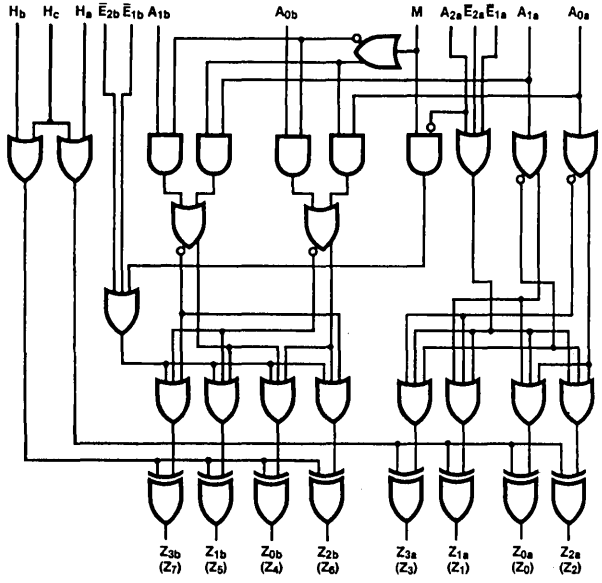
TL/F/10649–5

24-Pin Quad Cerpak



TL/F/10649–3

Logic Diagram



Note: (Z_n) for 1-of-4 applications.

TL/F/10649–6

Truth Tables

Dual 1-of-4 Mode (M = A_{2a} = H_c = LOW)

Inputs				Active HIGH Outputs (H_a and H_b Inputs HIGH)				Active LOW Outputs (H_a and H_b Inputs LOW)			
$\overline{E}_{1a}$ $\overline{E}_{1b}$	$\overline{E}_{2a}$ $\overline{E}_{2b}$	A_{1a} A_{1b}	A_{0a} A_{0b}	Z_{0a} Z_{0b}	Z_{1a} Z_{1b}	Z_{2a} Z_{2b}	Z_{3a} Z_{3b}	Z_{0a} Z_{0b}	Z_{1a} Z_{1b}	Z_{2a} Z_{2b}	Z_{3a} Z_{3b}
H	X	X	X	L	L	L	L	H	H	H	H
X	H	X	X	L	L	L	L	H	H	H	H
L	L	L	L	H	L	L	L	L	H	H	H
L	L	L	H	L	H	L	L	H	L	H	H
L	L	H	L	L	L	H	L	H	H	L	H
L	L	H	H	L	L	L	H	H	H	H	L

Single 1-of-8 Mode (M = HIGH; A_{0b} = A_{1b} = H_a = H_b = LOW)

Inputs					Active HIGH Outputs* (H_c Input HIGH)							
$\overline{E}_1$	$\overline{E}_2$	A_{2a}	A_{1a}	A_{0a}	Z_0	Z_1	Z_2	Z_3	Z_4	Z_5	Z_6	Z_7
H	X	X	X	X	L	L	L	L	L	L	L	L
X	H	X	X	X	L	L	L	L	L	L	L	L
L	L	L	L	L	H	L	L	L	L	L	L	L
L	L	L	L	H	L	H	L	L	L	L	L	L
L	L	L	H	L	L	L	H	L	L	L	L	L
L	L	L	H	H	L	L	L	H	L	L	L	L
L	L	H	L	L	L	L	L	L	H	L	L	L
L	L	H	L	H	L	L	L	L	L	H	L	L
L	L	H	H	L	L	L	L	L	L	L	H	L
L	L	H	H	H	L	L	L	L	L	L	L	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
*for H_c = LOW, output states are complemented
$\overline{E}_1$ = $\overline{E}_{1a}$ and $\overline{E}_{1b}$ wired; $\overline{E}_2$ = $\overline{E}2_{2a}$ and $\overline{E}_{2b}$ wired

Absolute Maximum Ratings

Above which the useful life may be impaired. (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature (T_{STG})	−65°C to +150°C
Maximum Junction Temperature (T_J)	
Ceramic	+175°C
Plastic	+150°C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Output Current (DC Output HIGH)	−50 mA
ESD (Note 2)	≥2000V

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: ESD testing conforms to MIL-STD-883, Method 3015.

Recommended Operating Conditions

Case Temperature (T_C)	
Commercial	0°C to +85°C
Industrial	−40°C to +85°C
Military	−55°C to +125°C
Supply Voltage (V_{EE})	−5.7V to −4.2V

Commercial Version

DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions	
V_{OH}	Output HIGH Voltage	−1025	−955	−870	mV	V_{IN} = V_{IH} (Max) or V_{IL} (Min)	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830	−1705	−1620	mV		
V_{OHC}	Output HIGH Voltage	−1035			mV	V_{IN} = V_{IH} (Min) or V_{IL} (Max)	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610	mV		
V_{IH}	Input HIGH Voltage	−1165		−870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1830		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = V_{IL} (Min)	
I_{IH}	Input HIGH Current			240	μA	V_{IN} = V_{IH} (Max)	
I_{EE}	Power Supply Current	−95		−50	mA	Inputs Open	

Note 3: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

Commercial Version (Continued)

Ceramic Dual-In-Line Package AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}_{na}$, $\overline{E}_{nb}$ to Output	0.75	1.85	0.75	1.85	0.85	2.05	ns	
t_{PLH} t_{PHL}	Propagation Delay A_{na}, A_{nb} to Output	0.75	2.20	0.75	2.20	0.75	2.30	ns	
t_{PLH} t_{PHL}	Propagation Delay H_a, H_b, H_c to Output	0.75	2.20	0.75	2.20	0.75	2.20	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay M to Output	1.10	2.70	1.10	2.70	1.10	3.00	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.40	1.30	0.40	1.30	0.40	1.30	ns	

PCC and Cerpak AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}_{na}$, $\overline{E}_{nb}$ to Output	0.75	1.65	0.75	1.65	0.85	1.85	ns	
t_{PLH} t_{PHL}	Propagation Delay A_{na}, A_{nb} to Output	0.75	2.00	0.75	2.00	0.75	2.10	ns	
t_{PLH} t_{PHL}	Propagation Delay H_a, H_b, H_c to Output	0.75	2.00	0.75	2.00	0.75	2.00	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay M to Output	1.10	2.50	1.10	2.50	1.10	2.80	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.40	1.20	0.40	1.20	0.40	1.20	ns	

Industrial Version

PCC DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = −40°C to +85°C (Note 3)

Symbol	Parameter	T_C = −40°C		T_C = 0°C to +85°C		Units	Conditions	
		Min	Typ	Min	Max			
V_{OH}	Output HIGH Voltage	−1085	−870	−1025	−870	mV	V_{IN} = V_{IH} (Max) or V_{IL} (Min)	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830	−1575	−1830	−1620	mV		
V_{OHC}	Output HIGH Voltage	−1095		−1035		mV	V_{IN} = V_{IH} (Min) or V_{IL} (Max)	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage		−1565		−1610	mV		
V_{IH}	Input HIGH Voltage	−1170	−870	−1165	−870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1830	−1480	−1830	−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50		0.50		μA	V_{IN} = V_{IL} (Min)	
I_{IH}	Input HIGH Current		300		240	μA	V_{IN} = V_{IH} (Max)	
I_{EE}	Power Supply Current	−95	−50	−95	−50	mA	Inputs Open	

Note 3: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

PCC AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = −40°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}_{na}$, $\overline{E}_{nb}$ to Output	0.75	1.65	0.75	1.65	0.85	1.85	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay A_{na}, A_{nb} to Output	0.65	2.00	0.75	2.00	0.75	2.10	ns	
t_{PLH} t_{PHL}	Propagation Delay H_a, H_b, H_c to Output	0.70	2.00	0.75	2.00	0.75	2.00	ns	
t_{PLH} t_{PHL}	Propagation Delay M to Output	1.10	2.50	1.10	2.50	1.10	2.80	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.40	1.30	0.40	1.20	0.40	1.20	ns	

Military Version—Preliminary

DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = −55°C to +125°C

Symbol	Parameter	Min	Max	Units	T_C	Conditions		Notes
V_{OH}	Output HIGH Voltage	−1025	−870	mV	0°C to +125°C	V_{IN} = V_{IH} (Max) or V_{IL} (Min)	Loading with 50Ω to −2.0V	1, 2, 3
		−1085	−870	mV	−55°C			
V_{OL}	Output LOW Voltage	−1830	−1620	mV	0°C to +125°C			
		−1830	−1555	mV	−55°C			
V_{OHC}	Output HIGH Voltage	−1035		mV	0°C to +125°C	V_{IN} = V_{IH} (Min) or V_{IL} (Max)	Loading with 50Ω to −2.0V	1, 2, 3
		−1085		mV	−55°C			
V_{OLC}	Output LOW Voltage		−1610	mV	0°C to +125°C			
			−1555	mV	−55°C			
V_{IH}	Input HIGH Voltage	−1165	−870	mV	−55°C to +125°C	Guaranteed HIGH Signal for All Inputs		1, 2, 3, 4
V_{IL}	Input LOW Voltage	−1830	−1475	mV	−55°C to +125°C	Guaranteed LOW Signal for All Inputs		1, 2, 3, 4
I_{IL}	Input LOW Current	0.50		μA	−55°C to +125°C	V_{EE} = −4.2V V_{IN} = V_{IL} (Min)		1, 2, 3
I_{IH}	Input HIGH Current H_c, A_{0a}, A_{1a}, A_{2a} All Others		310 250	μA	0°C to +125°C	V_{EE} = −5.7V V_{IN} = V_{IH} (Max)		1, 2, 3
	H_c, A_{0a}, A_{1a}, A_{2a} All Others		465 350	μA	−55°C			
I_{EE}	Power Supply Current	−110	−70	mA	−55°C to +125°C	Inputs Open		1, 2, 3

Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals −55°C, then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 2: Screen tested 100% on each device at −55°C, +25°C, and +125°C, Subgroups 1, 2, 3, 7, and 8.

Note 3: Sample tested (Method 5005, Table I) on each manufactured lot at −55°C, +25°C, and +125°C, Subgroups A1, 2, 3, 7, and 8.

Note 4: Guaranteed by applying specific input condition and testing V_{OH}/V_{OL}.

Military Version—Preliminary (Continued)

AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = −55°C		T_C = +25°C		T_C = +125°C		Units	Conditions	Notes
		Min	Max	Min	Max	Min	Max			
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}_{na}$, $\overline{E}_{nb}$ to Output	0.90	2.30	0.90	2.20	0.90	2.30	ns	*Figures 1* and *2*	1, 2, 3
t_{PLH} t_{PHL}	Propagation Delay A_{na}, A_{nb} to Output	1.00	2.80	1.00	2.70	1.00	2.90	ns		
t_{PLH} t_{PHL}	Propagation Delay H_a, H_b, H_c to Output	1.00	3.00	1.00	2.90	1.00	3.00	ns		
t_{PLH} t_{PHL}	Propagation Delay M to Output	1.50	3.90	1.60	3.80	1.60	3.90	ns		
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.70	0.45	1.70	0.45	1.80	ns		4

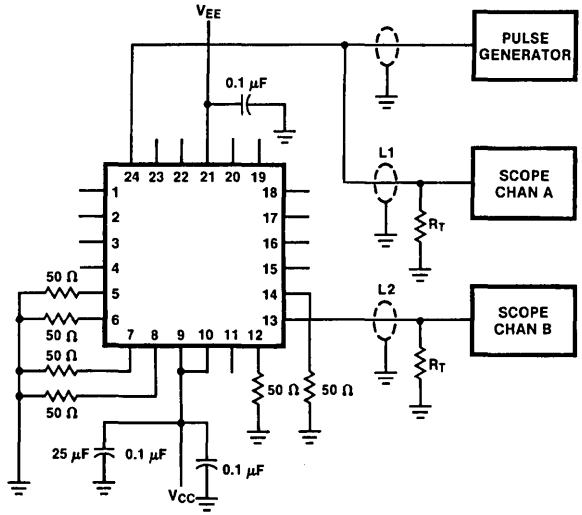
Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals −55°C), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 2: Screen tested 100% on each device at +25°C, temperature only, Subgroup A9.

Note 3: Sample tested (Method 5005, Table I) on each Mfg. lot at +25°C, Subgroup A9, and at +125°C, and −55°C Temp., Subgroups A10 and A11.

Note 4: Not tested at +25°C, +125°C and −55°C Temperature (design characterization data).

Test Circuit



TL/F/10649–7

FIGURE 1. AC Test Circuit

Notes:
V_{CC}, V_{CCA} = +2V, V_{EE} = −2.5V
L1 and L2 = equal length 50Ω impedance lines
R_T = 50Ω terminator internal to scope
Decoupling 0.1 µF from GND to V_{CC} and V_{EE}
All unused outputs are loaded with 50Ω to GND
C_L = Fixture and stray capacitance ≤ 3 pF
Pin numbers shown are for flatpak; for DIP see logic symbol

Switching Waveforms

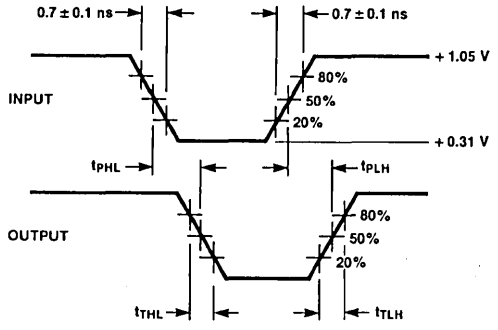


FIGURE 2. Propagation Delay and Transition Times

National Semiconductor

100371
Low Power Triple 4-Input Multiplexer with Enable

General Description

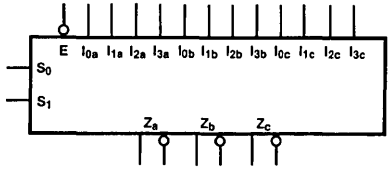
The 100371 contains three 4-input multiplexers which share a common decoder (inputs S_0 and S_1). Output buffer gates provide true and complement outputs. A HIGH on the Enable input ($\overline{E}$) forces all true outputs LOW (see Truth Table). All inputs have 50 kΩ pull-down resistors.

Features

- 35% power reduction of the 100171
- 2000V ESD protection
- Pin/function compatible with 100171
- Voltage compensated operating range = −4.2V to −5.7V
- Available to industrial grade temperature range

Ordering Code: See Section 6

Logic Symbol

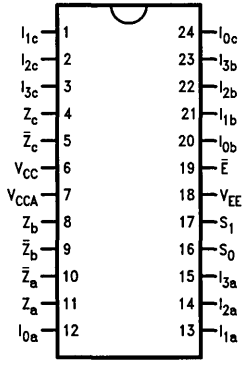


TL/F/10048–1

Pin Names	Description
I_{0x}–I_{3x}	Data Inputs
S_0, S_1	Select Inputs
$\overline{E}$	Enable Input (Active LOW)
Z_a–Z_c	Data Outputs
$\overline{Z}_a$–$\overline{Z}_c$	Complementary Data Outputs

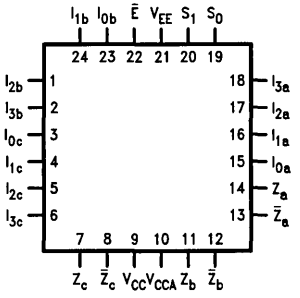
Connection Diagrams

24-Pin DIP/SOIC



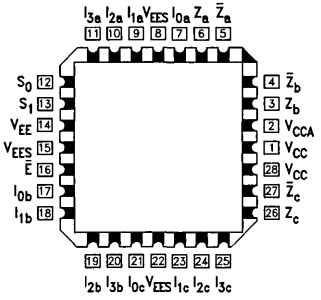
TL/F/10048–2

24-Pin Quad Cerpak



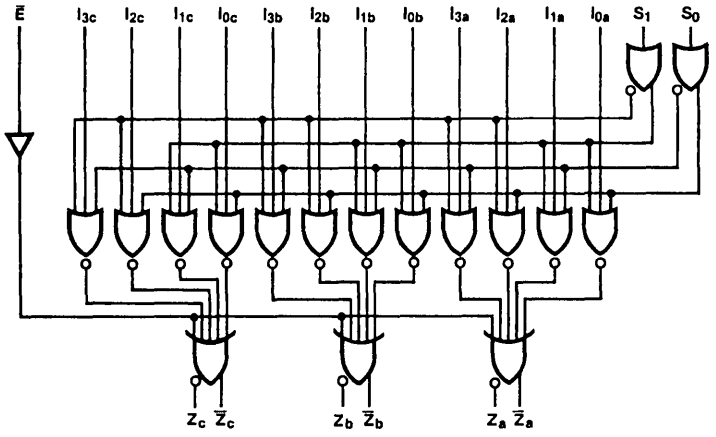
TL/F/10048–3

28-Pin PCC



TL/F/10148–4

Logic Diagram



TL/F/10148–5

Truth Table

Inputs			Outputs
$\overline{E}$	S_0	S_1	Z_n
L	L	L	I_{0x}
L	H	L	I_{1x}
L	L	H	I_{2x}
L	H	H	I_{3x}
H	X	X	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

Absolute Maximum Ratings

Above which the useful life may be impaired. (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature (T_{STG})	−65°C to +150°C
Maximum Junction Temperature (T_J)	
Ceramic	+175°C
Plastic	+150°C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Output current (DC Output HIGH)	−50 mA
ESD (Note 2)	≥2000V

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: ESD testing conforms to MIL-STD-883, Method 3015.

Recommended Operating Conditions

Case Temperature (T_C)	
Commercial	0°C to +85°C
Industrial	−40°C to +85°C
Military	−55°C to +125°C
Supply Voltage (V_{EE})	−5.7V to −4.2V

Commercial Version

DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions	
V_{OH}	Output HIGH Voltage	−1025	−955	−870	mV	V_{IN} = V_{IH} (Max) or V_{IL} (Min)	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830	−1705	−1620	mV		
V_{OHC}	Output HIGH Voltage	−1035			mV	V_{IN} = V_{IH} (Min) or V_{IL} (Max)	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610	mV		
V_{IH}	Input HIGH Voltage	−1165		−870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1830		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = V_{IL} (Min)	
I_{IH}	Input HIGH Current I_{0X}–I_{3X} S_0, S_1, $\overline{E}$			 340 300	μA	V_{IN} = V_{IH} (Max)	
I_{EE}	Power Supply Current	−75		−39	mA	Inputs Open	

Note 3: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

Commercial Version— (Continued)

DIP AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay I_{0x}–I_{3x} to Output	0.45	1.50	0.45	1.50	0.45	1.60	ns	*Figures 1* and *2* (Note 1)
t_{PLH} t_{PHL}	Propagation Delay S_0, S_1 to Output	0.90	2.40	0.90	2.40	1.00	2.60	ns	
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to Output	0.65	2.30	0.65	2.30	0.75	2.40	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.35	1.20	0.35	1.20	0.35	1.20	ns	*Figures 1* and *2*

Note 1: The propagation delay specified is for single output switching. Delays may vary up to 300 ps with multiple outputs switching.

SOIC, PCC and Cerpak AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay I_{0x}–I_{3x} to Output	0.45	1.30	0.45	1.30	0.45	1.40	ns	*Figures 1* and *2* (Note 2)
t_{PLH} t_{PHL}	Propagation Delay S_0, S_1 to Output	0.90	2.20	0.90	2.20	1.00	2.40	ns	
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to Output	0.65	2.10	0.65	2.10	0.75	2.20	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.35	1.10	0.35	1.10	0.35	1.10	ns	*Figures 1* and *2*
t_{OSHL}	Maximum Skew Common Edge Output-to-Output Variation Data to Output Path		400		400		400	ps	PCC only (Note 1)
t_{OSLH}	Maximum Skew Common Edge Output-to-Output Variation Data to Output Path		490		490		490	ps	PCC only (Note 1)
t_{OST}	Maximum Skew Opposite Edge Output-to-Output Variation Data to Output Path		490		490		490	ps	PCC only (Note 1)
t_{PS}	Maximum Skew Pin (Signal) Transition Variation Data to Output Path		430		430		430	ps	PCC only (Note 1)

Note 1: Output-to-Output Skew is defined as the absolute value of the difference between the actual propagation delay for any outputs within the same packaged device. The specifications apply to any outputs switching in the same direction either HIGH to LOW (t_{OSHL}), or LOW to HIGH (t_{OSLH}), or in opposite directions both HL and LH (t_{OST}). Parameters t_{OST} and t_{PS} guaranteed by design.

Note 2: The propagation delay specified is for single output switching. Delays may vary up to 300 ps with multiple outputs switching.

Industrial Version

PCC DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = −40°C to +85°C (Note 1)

Symbol	Parameter	T_C = −40°C		T_C = 0°C to +85°C		Units	Conditions	
		Min	Max	Min	Max			
V_{OH}	Output HIGH Voltage	−1085	−870	−1025	−870	mV	V_{IN} = V_{IH} (Max) or V_{IL} (Min)	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830	−1575	−1830	−1620	mV		
V_{OHC}	Output HIGH Voltage	−1095		−1035		mV	V_{IN} = V_{IH} (Min) or V_{IL} (Max)	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage		−1565		−1610	mV		
V_{IH}	Input HIGH Voltage	−1170	−870	−1165	−870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1830	−1480	−1830	−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50		0.50		μA	V_{IN} = V_{IL} (Min)	
I_{IH}	Input HIGH Current							
	I_{0X}–I_{3X}		340		340	μA	V_{IN} = V_{IH} (Max)	
	S_0, S_1, $\overline{E}$		300		300			
I_{EE}	Power Supply Current	−75	−35	−75	−39	mA	Inputs Open	

Note 1: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

PCC AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = −40°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay I_{0X}–I_{3X} to Output	0.40	1.30	0.45	1.30	0.45	1.40	ns	*Figures 1* and *2* (Note 2)
t_{PLH} t_{PHL}	Propagation Delay S_0, S_1 to Output	0.70	2.20	0.90	2.20	1.00	2.40	ns	
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to Output	0.65	2.10	0.65	2.10	0.75	2.20	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.20	1.60	0.35	1.10	0.35	1.10	ns	*Figures 1* and *2*

Note 2: The propagation delay specified is for single output switching. Delays may vary up to 300 ps with multiple outputs switching.

Military Version—Preliminary

DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = −55°C to +125°C

Symbol	Parameter	Min	Max	Units	T_C	Conditions		Notes
V_{OH}	Output HIGH Voltage	−1025	−870	mV	0°C to +125°C	V_{IN} = V (Max) or V_{IL} (Min)	Loading with 50Ω to −2.0V	1, 2, 3
		−1085	−870	mV	−55°C			
V_{OL}	Output LOW Voltage	−1830	−1620	mV	0°C to +125°C			
		−1830	−1555	mV	−55°C			
V_{OHC}	Output HIGH Voltage	−1035		mV	0°C to +125°C	V_{IN} = V_{IH} (Min) or V_{IL} (Max)	Loading with 50Ω to −2.0V	1, 2, 3
		−1085		mV	−55°C			
V_{OLC}	Output LOW Voltage		−1610	mV	0°C to +125°C			
			−1555	mV	−55°C			
V_{IH}	Input HIGH Voltage	−1165	−870	mV	−55°C to +125°C	Guaranteed HIGH Signal for All Inputs		1, 2, 3, 4
V_{IL}	Input LOW Voltage	−1830	−1475	mV	−55°C to +125°C	Guaranteed LOW Signal for All Inputs		1, 2, 3, 4
I_{IL}	Input LOW Current	0.50		μA	−55°C to +125°C	V_{EE} = −4.2V V_{IN} = V_{IL} (Min)		1, 2, 3
I_{IH}	Input HIGH Current I_{0X}–I_{3X} S_0, S_1, $\overline{E}$		340 300	μA	0°C to +125°C	V_{EE} = −5.7V V_{IN} = V_{IH} (Max)		1, 2, 3
	I_{0X}–I_{3X} S_0, S_1, $\overline{E}$		490 450	μA	−55°C			
I_{EE}	Power Supply Current	−80	−30	mA	−55°C to +125°C	Inputs Open		1, 2, 3

Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals −55°C), then testing immediately without allowing for the junction temperature to stabilize due to heat dissapation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 2: Screen tested 100% on each device at −55°C, +25°C, and +125°C, Subgroups 1, 2, 3, 7, and 8.

Note 3: Sample tested (Method 5005, Table I) on each manufactured lot at −55°C, +25°C, and +125°C, Subgroups 1, 2, 3, 7, and 8.

Note 4: Guaranteed by applying specified input condition and testing V_{OH}/V_{OL}.

Military Version—Preliminary (Continued)

AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = −55°C		T_C = +25°C		T_C = +125°C		Units	Conditions	Notes
		Min	Max	Min	Max	Min	Max			
t_{PLH} t_{PHL}	Propagation Delay I_{0x}–I_{3x} to Output	0.30	1.90	0.40	1.70	0.30	2.00	ns	*Figures 1* and *2*	1, 2, 3, 5
t_{PLH} t_{PHL}	Propagation Delay S_0, S_1 to Output	0.40	2.70	0.60	2.40	0.50	2.90	ns		
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to Output	0.50	2.70	0.60	2.40	0.50	2.90	ns		
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.20	1.60	0.30	1.50	0.20	1.60	ns		4

Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals −55°C), then testing immediately after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 2: Screen tested 100% on each device at +25°C temperature only, Subgroup A9.

Note 3: Sample tested (Method 5005, Table 1) on each mfg. lot at +25°C, Subgroup A9, and at +125°C and −55°C temperatures, Subgroups A10 and A11.

Note 4: Not tested at +25°C, +125°C and −55°C temperature (design characterization data).

Note 5: The propagation delay specified is for single output switching. Delays may vary up to 300 ps with multiple outputs switching.

Test Circuitry

Notes:

V_{CC}, V_{CCA} = +2V, V_{EE} = −2.5V

L1 and L2 = equal length 50Ω impedance lines

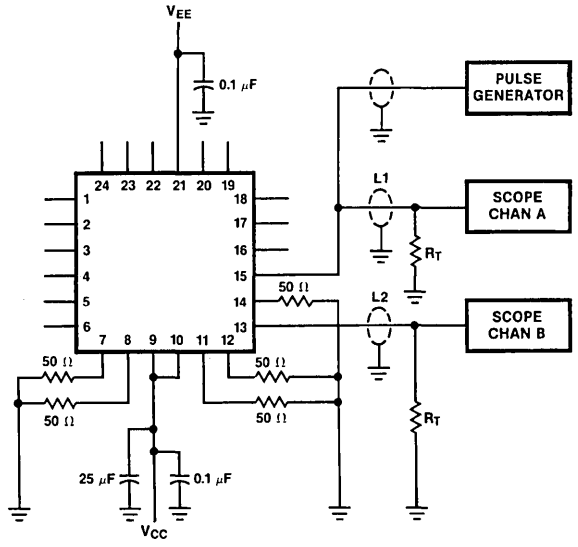
R_T = 50Ω terminator internal to scope

Decoupling 0.1 μF from GND to V_{CC} and V_{EE}

All unused outputs are loaded with 50Ω to GND

C_L = Fixture and stray capacitance ≤ 3 pF

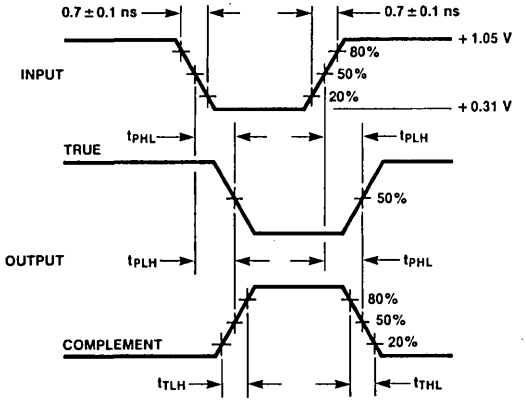
Pin numbers shown are for flatpak; for DIP see logic symbol



TL/F/10148–6

FIGURE 1. AC Test Circuit

Switching Waveforms



TL/F/10148–7

FIGURE 2. Propagation Delay and Transition Times

National Semiconductor

ADVANCE INFORMATION

100389
Single Supply Hex CMOS-to-ECL Translator with Cutoff Drivers

General Description

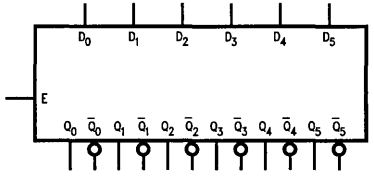
The 100389 is a hex translator for converting CMOS logic levels to positive referenced F100K ECL logic levels (or PECL). This translator is designed to operrate from a single +5V supply, eliminating the need for a separate −5V supply. The differential outputs of the 100389 due to its high common mode rejection, overcomes voltages gradients between the CMOS and ECL ground systems.

A LOW on the input enable pin (E) sets the true outputs to a LOW state and the inverting outputs to a HIGH state.

Features

- Operates from a single +5V supply
- Differential ECL outputs
- 2000V ESD protection

Logic Symbol

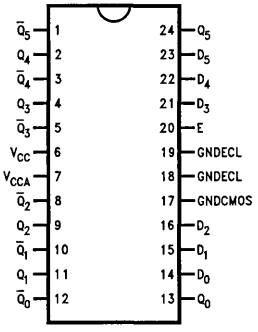


TL/F/10999–1

Pin Names	Description
D_0–D_5	Data Inputs (CMOS)
Q_0–Q_5	Data Outputs (PECL)
$\overline{Q}_0$–$\overline{Q}_5$	Inverting Data Outputs (PECL)
E	Enable Input (CMOS)

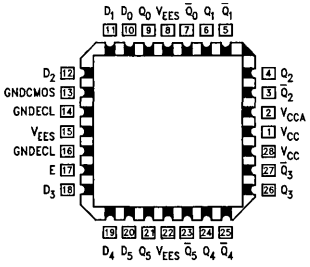
Connection Diagrams

24-Pin DIP/SOIC



TL/F/10999–2

28-Pin PCC



TL/F/10999–3

National Semiconductor

100390
Low Power Single Supply Hex ECL-to-TTL Translator

General Description

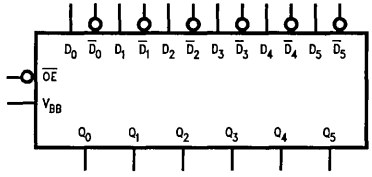
The 100390 is a hex translator for converting F100K logic levels to TTL logic levels. Unlike other level translators, the 100390 operates using only one +5V supply. Differential inputs allow each circuit to be used as an inverting, non-inverting, or differential receiver. An internal reference generator provides V_{BB} for single-ended operation. The standard FAST® TRI-STATE® outputs are enabled by a common active low TTL compatible $\overline{OE}$ input. Partitioned V_{CC}s on chip are brought out on separate power pins, allowing the noisy TTL V_{CC} power plane to be isolated from the relatively quiet ECL V_{CC}. The 100390 is ideal for applications limited to a single +5V supply, allowing for easy ECL to TTL Interfacing.

Features

- Operates from a single +5V supply
- TRI-STATE outputs
- 2000V ESD protection
- V_{BB} supplied for single-ended operation

Ordering Code: See Section 6

Logic Symbols

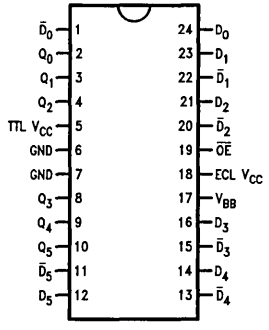


TL/F/10897–1

Pin Names	Description
D_0–D_5	Data Inputs (PECL)
$\overline{D}_0$–$\overline{D}_5$	Inverting Data Inputs (PECL)
Q_0–Q_5	Data Outputs (TTL)
$\overline{OE}$	Output Enable (TTL)
V_{BB}	Reference Voltage (PECL)

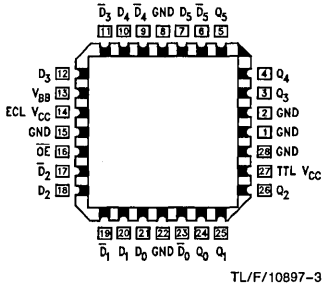
Connection Diagrams

24-Pin DIP/SOIC



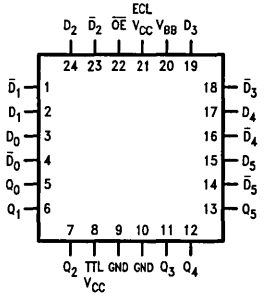
TL/F/10897–2

28-Pin PCC



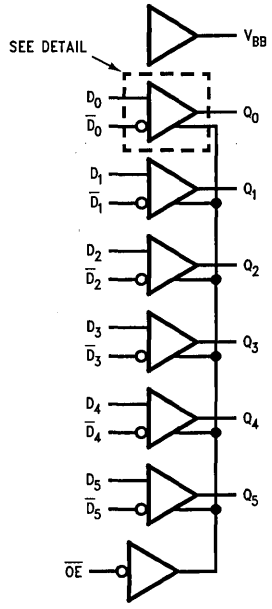
TL/F/10897–3

24-Pin Quad Cerpak



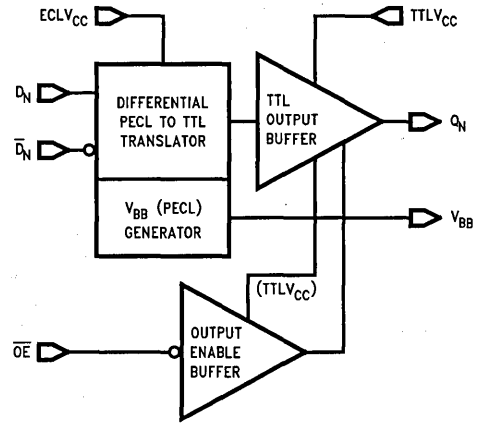
TL/F/10897–4

Logic Diagram



TL/F/10897–5

Detail



TL/F/10897–11

Truth Table

Data Inputs (PECL)		Control Input (TTL)	TTL Outputs	Comments
D_n	$\overline{D_n}$	$\overline{OE}$	Q_n	
X	X	H	Z	Outputs Disable
L	H	L	L	Differential Operation
H	L	L	H	Differential Operation
L	L	L	U	Invalid Input States
H	H	L	U	Invalid Input States
OPEN	OPEN	L	U	Invalid Input States
L	V_{BB}	L	L	Single Ended Operation
H	V_{BB}	L	H	Single Ended Operation
V_{BB}	L	L	H	Single Ended Operation
V_{BB}	H	L	L	Single Ended Operation
V_{BB}	OPEN	L	H	Single Ended Operation
OPEN	V_{BB}	L	L	Single Ended Operation

H = HIGH Voltage Level
L = LOW Voltage Level
Z = HIGH Impedance
U = Undefined

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Maximum Junction Temperature	
Ceramic	+175°C
Plastic	+150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
TTL Input Voltage (Note 2)	−0.5V to +7.0V
TTL Input Current (Note 2)	−30 mA to +5.0 mA
V_{BB} Output Current	−5.0 mA to +1.0 mA
ECL Input Potential	GND to ECL V_{CC} + 0.5V
V_{CC} Differential ECL V_{CC} to TTL V_{CC}	−1.0V to +1.0V
Voltage Applied to Output in High State (with V_{CC} = 0V) TRI-STATE Output	−0.5V to +5.5V
Current Applied to Output in Low State (Max)	Twice the Rated I_{OL} (mA)
ESD Last Passing Voltage (Min)	2000V

Recommended Operating Conditions

Case Temperature	0°C to +85°C
Supply Voltage	+4.75V to +5.25V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics ECL V_{CC} = +5.0V ±5%, TTL V_{CC} = +5.0V ±5%, GND = 0V

Symbol	Parameter		Min	Max	Units	Conditions
V_{IH}	Input HIGH Voltage	Data	ECL V_{CC} − 1.165	ECL V_{CC} − 0.870	V	Guaranteed HIGH Signal for ALL Inputs (with One Input Tied to V_{BB})
		$\overline{OE}$	2.0		V	Guaranteed HIGH Signal (TTL)
V_{IL}	Input LOW Voltage	Data	ECL V_{CC} − 1.830	ECL V_{CC} − 1.475	V	Guaranteed LOW Signal for ALL Inputs (with One Input Tied to V_{BB})
		$\overline{OE}$		0.8	V	Guaranteed LOW Signal (TTL)
V_{BB}	Output Reference Voltage		ECL V_{CC} − 1.38	ECL V_{CC} − 1.26	V	I_{BB} = 0.0 mA or −1.0 mA
V_{OH}	Output HIGH Voltage (TTL)		2.7		V	I_{OH} = −3 mA
V_{OL}	Output LOW Voltage (TTL)			0.5	V	I_{OL} = 24 mA
I_{IH}	Input HIGH Current	Data		50	μA	$V_{IN} = V_{IH}$(Max), D_0–D_5 = V_{BB}, $\overline{D_0}$–$\overline{D_5}$ = V_{IL}(Min)
		$\overline{OE}$		20	μA	V_{IN} = 2.7V (TTL)
I_{IL}	Input LOW Current	$\overline{OE}$		−200	μA	V_{IN} = 0.5V (TTL)
I_{BVI}	Input Breakdown Current	$\overline{OE}$		10	μA	V_{IN} = 7.0V (TTL)
I_{CBO}	Input Leakage Current		−10		μA	V_{IN} = GND, D_0–D_5 = V_{BB} $\overline{D_0}$–$\overline{D_5}$ = V_{IL}(Min)
I_{OZH}	TRI-STATE Current Output HIGH			50	μA	V_{OUT} = +2.7V
I_{OZL}	TRI-STATE Current Output LOW			−50	μA	V_{OUT} = +0.5V
I_{CC}	ECL Supply Current		13	30	mA	
I_{CCZ}	TTL Supply Current		10	20	mA	TRI-STATE
I_{CCL}	TTL Supply Current		8	17	mA	Low State
I_{CCH}	TTL Supply Current HIGH		0.4	2.0	mA	HIGH State
I_{OS}	Output Short-Circuit Current		−150	−60	mA	V_{OUT} = 0.0V, V_{CC} = +5.25
V_{Diff}	Differential Input Voltage		150		mV	Required for Full Output Swing
V_{CM}	Common Mode Voltage		ECL V_{CC} − 2.0	ECL V_{CC} − 0.5	V	
V_{CD}	Clamp Diode Voltage			−1.2	V	I_{IN} = −18 mA

DIP AC Electrical Characteristics

V_{CC} = 5.0V ±5%; T_C = 0°C to +85°C

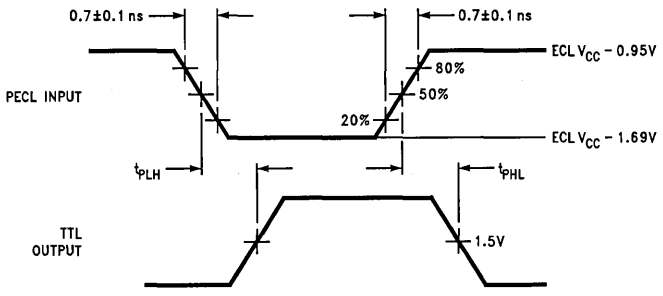
Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Fig. No.
		Min	Max	Min	Max	Min	Max		
F_{MAX}	Maximum Clock Frequency	100		100		100		MHz	
t_{PLH} t_{PHL}	Propagation Delay Data to Output	3.3	6.4	3.3	6.1	3.3	6.1	ns	1
t_{PZH} t_{PZL}	Output Enable Time	2.7 2.3	4.8 3.9	2.7 2.3	4.8 3.9	3.0 2.6	5.1 4.3	ns	2
t_{PHZ} t_{PLZ}	Output Disable Time	2.3 2.0	4.6 3.6	2.3 2.0	4.6 3.6	2.3 2.0	4.6 3.6	ns	2

SOIC, Cerpak and PCC Package AC Electrical Characteristics

V_{CC} = 5.0V ±5%; T_C = 0°C to +85°C

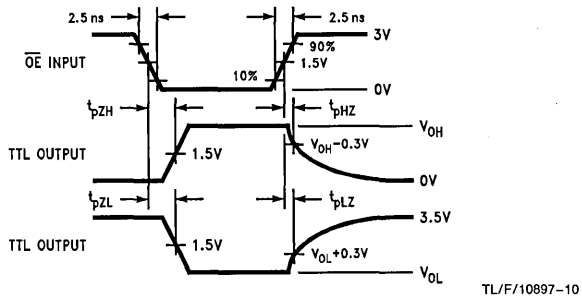
Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Fig. No.
		Min	Max	Min	Max	Min	Max		
F_{MAX}	Maximum Clock Frequency	100		100		100		MHz	
t_{PLH} t_{PHL}	Propagation Delay Data to Output	3.3	6.2	3.3	5.9	3.3	5.9	ns	1
t_{PZH} t_{PZL}	Output Enable Time	2.7 2.3	4.6 3.7	2.7 2.3	4.6 3.7	3.0 2.6	4.9 4.1	ns	2
t_{PHZ} t_{PLZ}	Output Disable Time	2.3 2.0	4.4 3.4	2.3 2.0	4.4 3.4	2.3 2.0	4.4 3.4	ns	2

Switching Waveforms



TL/F/10897–6

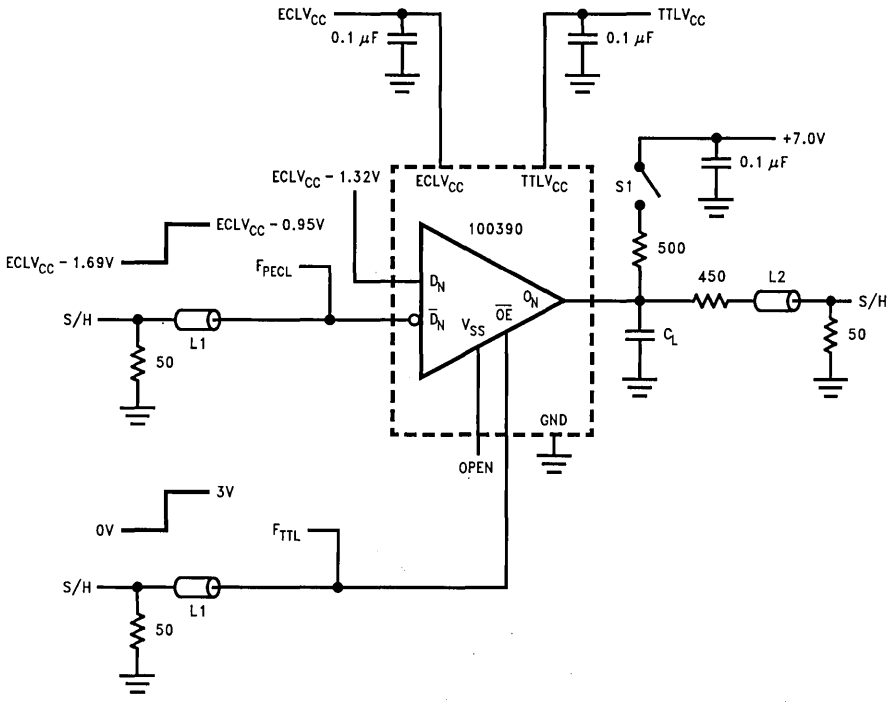
FIGURE 1. Data to Output Propagation Delay



TL/F/10897–10

FIGURE 2. Enable/Disable Propagation Delay

Test Circuit



TL/F/10897–7

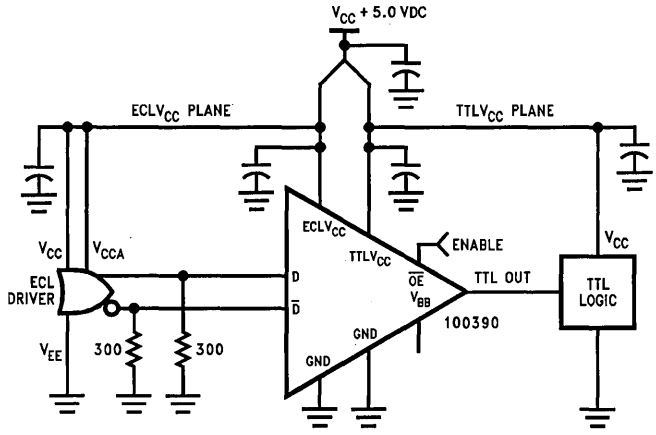
FIGURE 3. AC Test Circuit

Notes:
GND = 0V, ECL V_{CC} = +5V, TTL V_{CC} = +5V
L1 and L2 = equal length 50Ω impedance lines
50Ω terminators are internal to S/H measurement unit
Decoupling 0.1 μF from GND to ECL V_{CC} and TTL V_{CC}
All unused outputs are loaded with 500Ω to GND
C_L = Fixture and stray capacitance = 50 pF
Switch S1 is open for t_{PLH}, t_{PHL}, t_{PHZ} and t_{PZH} tests
Switch S1 is closed only for t_{PLZ} and t_{PZL} tests

Application Notes

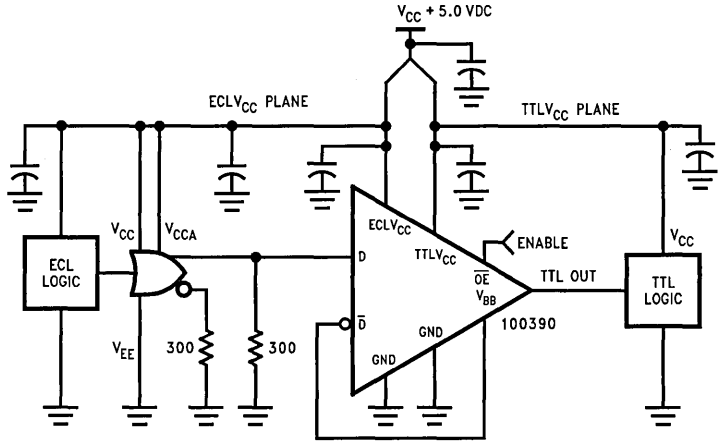
1. Device performance will be enhanced by the use of dual V_{CC} power planes as illustrated in the Application *Figures 4* and *5*. This will minimize the coupling of TTL switching noise into the primary reference to the ECL circuitry and take full advantage of the 100390's on chip V_{CC} partitioning.
2. The device's partitioned V_{CC} may be operated from two 5V, 5% tolerance, supplies provided that they are ramped up/down together so that the max differential is 1V. This is to prevent overstress to internal ESD diodes. If the ECL driver to the F390 is powered from a separate supply, it must obey this sequence rule also.
3. Glitch-free power up, independent of Data input levels, is achieved if TTL logic HIGH is held on the Output Enable pin during ramping up/down of the V_{CC} supply.
4. Undefined output states can occur for some invalid combinations. See Truth Table. This should be avoided to prevent possible oscillation or increased power consumption due to TTL outputs biased into a quasi state with both pullup and pulldown stages partially on. TRI-STATEing the outputs will counteract the effects of invalid input states.
5. Pins 8, 15, and 22 on the 28-pin PCC package are tied to the chip's substrate and are named GNDs. These pins are electrically common to the ground pins 1, 2, and 28. For best thermal performance, tie the GND pins to the circuit ground plane. They may be tied to an electrically isolated thermal dissipation plane or may float.
6. *Figure 4* illustrates typical differential input operation.
7. *Figure 5* illustrates typical single-ended input operation.

Application Notes (Continued)



TL/F/10897–8

FIGURE 4



TL/F/10897–9

FIGURE 5

National Semiconductor

100391
Low Power Single Supply Hex TTL-to-ECL Translator

General Description

The 100391 is a hex translator for converting TTL logic levels to F100K ECL logic levels. The unique feature of this translator, is the ability to do this translation using only one +5V supply. The differential outputs allow each circuit to be used as an inverting/non-inverting translator, or as a differential line driver. A common enable (E), when low, holds all inverting outputs HIGH and all non-inverting inputs LOW.

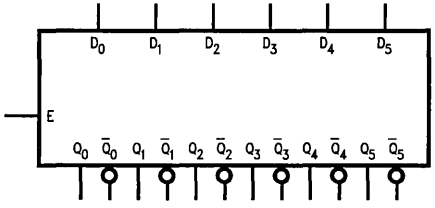
The 100391 is ideal for those mixed ECL/TTL applications which only have a +5V supply available. When used in the differential mode, the 100391, due to its high common mode rejection, overcomes voltage gradients between the TTL and ECL ground systems.

Features

- Operates from a single +5V supply
- Differential ECL outputs
- 2000V ESD protection
- Companion chip to 100390 hex ECL-to-TTL translator

Ordering Code: See Section 6

Logic Symbol

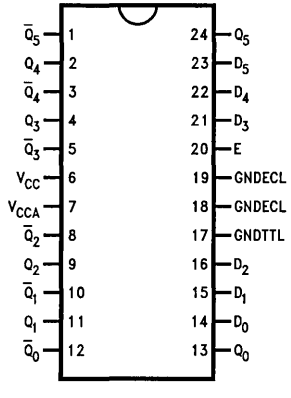


TL/F/10939–1

Pin Names	Description
D_0–D_5	Data Inputs (TTL)
Q_0–Q_5	Data Outputs (PECL)
$\overline{Q}_0$–$\overline{Q}_5$	Inverting Data Outputs (PECL)
E	Enable Input (TTL)

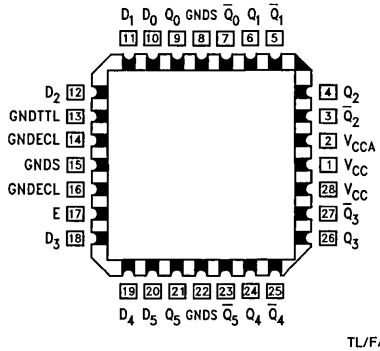
Connection Diagrams

24-Pin DIP and SOIC



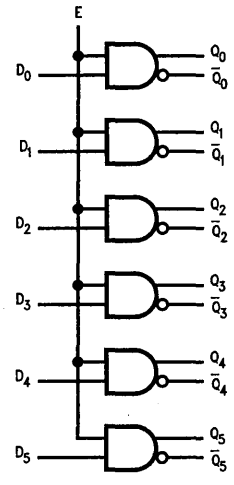
TL/F/10939–2

28-Pin PCC



TL/F/10939–3

Logic Diagram



TL/F/10939–5

Truth Table

Inputs		Outputs	
D_n	E	Q_n	$\overline{Q}_n$
H	H	H	L
L	H	L	H
H	L	L	H
L	L	L	H

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature (T_{STG})	−65°C to +150°C
Maximum Junction Temperature (T_J)	
Ceramic	+175°C
Plastic	+150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
ECL Output Current (DC Output HIGH)	−50 mA
TTL Input Voltage (Note 3)	−0.5V to +7.0V
TTL Input Current (Note 3)	−30 mA to +5.0 mA
ESD (Last Passing Voltage) (Min) (Note 2)	2000V

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: ESD testing conforms to MIL-STD-883, Method 3015.

Note 3: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Case Temperature (T_C)	
Commercial	0°C to +85°C
Military	−55°C to +125°C
Supply Voltage (V_{CC})	4.5V to 5.5V
Commercial	

Commercial Version

TTL-to-ECL DC Electrical Characteristics V_{CC} = +5.0V ±10%, GND = 0V

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{OH}	Output HIGH Voltage	V_{CC} − 1025	V_{CC} − 955	V_{CC} − 870	mV	V_{IN} = $V_{IH\ (max)}$ or $V_{IL\ (min)}$ Loading with 50Ω to V_{CC} − 2V
V_{OL}	Output LOW Voltage	V_{CC} − 1890	V_{CC} − 1705	V_{CC} − 1620	mV	
V_{OHC}	Output HIGH Voltage Corner Point High	V_{CC} −1035			mV	V_{IN} = $V_{IH\ (min)}$ or $V_{IL\ (max)}$ Loading with 50Ω to V_{CC} − 2V
V_{OLC}	Output LOW Voltage Corner Point Low			V_{CC} − 1610	mV	
V_{IH}	Input HIGH Voltage	2.0		5.0	V	Over V_{TTL}, V_{EE}, T_C Range
V_{IL}	Input LOW Voltage	0		0.8	V	Over V_{TTL}, V_{EE}, T_C Range
I_{IH}	Input HIGH Current			10	μA	V_{IN} = +2.7V
	Breakdown Test			20	μA	V_{IN} = +5.5V
I_{IL}	Input LOW Current D_n E	 −0.8 −4.2			mA	V_{IN} = +0.5V
V_{FCD}	Input Clamp Diode Voltage	−1.2			V	I_{IN} = −18 mA
I_{CC}	V_{CC} Supply Current	32		69	mA	Inputs Open

Note 4: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DIP Package AC Electrical Characteristics

V_{CC} = 5.0V ±10%

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Data to Output	0.30	1.40	0.35	1.30	0.40	1.30	ns	*Figures 1, 2*
t_{PLH} t_{PHL}	Propagation Delay Enable to Output	0.40	1.50	0.45	1.40	0.50	1.40	ns	*Figures 1, 2*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.35	1.70	0.35	1.70	0.35	1.70	ns	*Figures 1, 2*

SOIC and PCC Package AC Electrical Characteristics

V_{CC} = 5.0V ±10%

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Data to Output	0.30	1.40	0.35	1.30	0.40	1.30	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay Enable to Output	0.40	1.50	0.45	1.40	0.50	1.40	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.35	1.70	0.35	1.70	0.35	1.70	ns	
t_{OSHL}	Maximum Skew Common Edge Output-to-Output Variation Data to Output Path		750		750		750	ps	PCC Only (Note 1)
t_{OSLH}	Maximum Skew Common Edge Output-to-Output Variation Data to Output Path		700		700		700	ps	PCC Only (Note 1)
t_{OST}	Maximum Skew Opposite Edge Output-to-Output Variation Data to Output Path		450		450		450	ps	PCC Only (Note 1)
t_{PS}	Maximum Skew Pin (Signal) Transition Variation Data to Output Path		525		525		525	ps	PCC Only (Note 1)

Note 1: Output-to-Output Skew is defined as the absolute value of the difference between the actual propagation delay for any outputs within the same packaged device. The specifications apply to any outputs switching in the same direction either HIGH to LOW (t_{OSHL}), or LOW to HIGH (t_{OSLH}), or in opposite directions both HL and LH (t_{OST}). Parameters t_{OST} and t_{PS} guaranteed by design.

Industrial Version

DC Electrical Characteristics

V_{CC} = +5.0V ±10%, GND = 0V (Note 1)

Symbol	Parameter	T_C = −40°C		T_C = 0°C to +85°C		Units	Conditions
		Min	Max	Min	Max		
V_{OH}	Output HIGH Voltage	V_{CC} − 1085	V_{CC} − 870	V_{CC} − 1025	V_{CC} − 870	mV	V_{IN} = $V_{IH\ (max)}$ or $V_{IL\ (min)}$
V_{OL}	Output LOW Voltage	V_{CC} − 1890	V_{CC} − 1575	V_{CC} − 1890	V_{CC} − 1620	mV	Loading with 50Ω to V_{CC} − 2V
V_{OHC}	Output HIGH Voltage Corner Point High	V_{CC} − 1095		V_{CC} − 1035		mV	V_{IN} = $V_{IH\ (min)}$ or $V_{IL\ (max)}$ Loading with 50Ω to V_{CC} − 2V
V_{OLC}	Output LOW Voltage Corner Point High		V_{CC} − 1565		V_{CC} − 1610	mV	
V_{IH}	Input HIGH Voltage	2.0	5.0	2.0	5.0	V	
V_{IL}	Input LOW Voltage	0	0.8	0	0.8	V	
I_{IH}	Input HIGH Current		10		10	μA	V_{IN} = +2.7V
	Breakdown Test		20		20	μA	V_{IN} = +5.5V
I_{IL}	Input LOW Current D_n E	 −0.8 −4.2		 −0.8 −4.2		mA	V_{IN} = +0.5V
V_{FCD}	Input Clamp Diode Voltage	−1.2		−1.2		V	I_{IN} = −18 mA
I_{CC}	V_{CC} Supply Current	29	69	29	69	mA	Inputs Open

PCC AC Electrical Characteristics

V_{CC} = +5.0V ±10%, GND = 0V

Symbol	Parameter	T_C = −40°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Data to Output	0.20	1.50	0.35	1.30	0.40	1.30	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay Enable to Output	0.35	1.60	0.45	1.40	0.50	1.40	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.35	1.70	0.35	1.70	0.35	1.70	ns	

Note 1: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

Military Version-Preliminary

TTL-to-ECL DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = −55°C to +125°C, V_{TTL} = +4.5V to +5.5V

Symbol	Parameter	Min	Max	Units	T_C	Conditions		Notes
V_{OH}	Output HIGH Voltage	V_{CC} − 1025	V_{CC} − 870	mV	0°C to +125°C	V_{IN} = $V_{IH\ (max)}$ or $V_{IL\ (min)}$	Loading with 50Ω to V_{CC} − 2.0V	1, 2, 3
		V_{CC} − 1085	V_{CC} − 870	mV	−55°C			
V_{OL}	Output LOW Voltage	V_{CC} − 1830	V_{CC} − 1620	mV	0°C to +125°C			
		V_{CC} − 1830	V_{CC} − 1555	mV	−55°C			
V_{OHC}	Output HIGH Voltage	V_{CC} − 1035		mV	0°C to +125°C	V_{IN} = $V_{IH\ (min)}$ or $V_{IL\ (max)}$	Loading with 50Ω to V_{CC} − 2.0V	1, 2, 3
		V_{CC} − 1085		mV	−55°C			
V_{OLC}	Output LOW Voltage		V_{CC} − 1610	mV	0°C to +125°C			
			V_{CC} − 1555	mV	−55°C			
V_{IH}	Input HIGH Voltage	2.0		V	−55°C to +125°C			1, 2, 3, 4
V_{IL}	Input LOW Voltage		0.8	V	−55°C to +125°C			1, 2, 3, 4
I_{IH}	Input HIGH Current		70	μA	−55°C to 125°C	V_{IN} = +2.7V		1, 2, 3
I_{IL}	Input LOW Current	−1.0		mA	−55°C to +125°C	V_{IN} = +0.5V		1, 2, 3
V_{FCD}	Input Clamp Diode Voltage	−1.2		V	−55°C to +125°C	I_{IN} = −18 mA		1, 2, 3
I_{CC}	V_{CC} Supply Current	20	70	mA	−55°C to +125°C	Inputs Open		1, 2, 3

AC Electrical Characteristics V_{CC} = +5.0 ± 10%, GND = 0V

Symbol	Parameter	T = −55°C		T = +25°C		T = +125°C		Units	Conditions	Notes
		Min	Max	Min	Max	Min	Max			
t_{PLH} t_{PHL}	Propagation Delay Data and Enable to Output	0.40	2.50	0.50	2.10	0.50	2.10	ns	Figures 1, 2	1, 2, 3
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.30	2.00	0.30	2.00	0.30	2.00	ns	Figures 1, 2	1, 2, 3

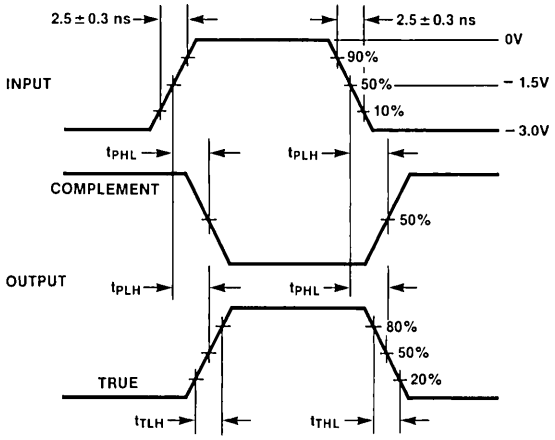
Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals −55°C), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold termperatures.

Note 2: Screen tested 100% on each device at −55°C, +25°C and +125°C, Subgroups 1, 2, 3, 7 and 8.

Note 3: Sample tested (Method 5005, Table I) on each manufactured lot at −55°C, +25°C and +125°C, Subgroups A1, 2, 3, 7 and 8.

Note 4: Guaranteed by applying specified input condition and testing V_{OH}/V_{OL}.

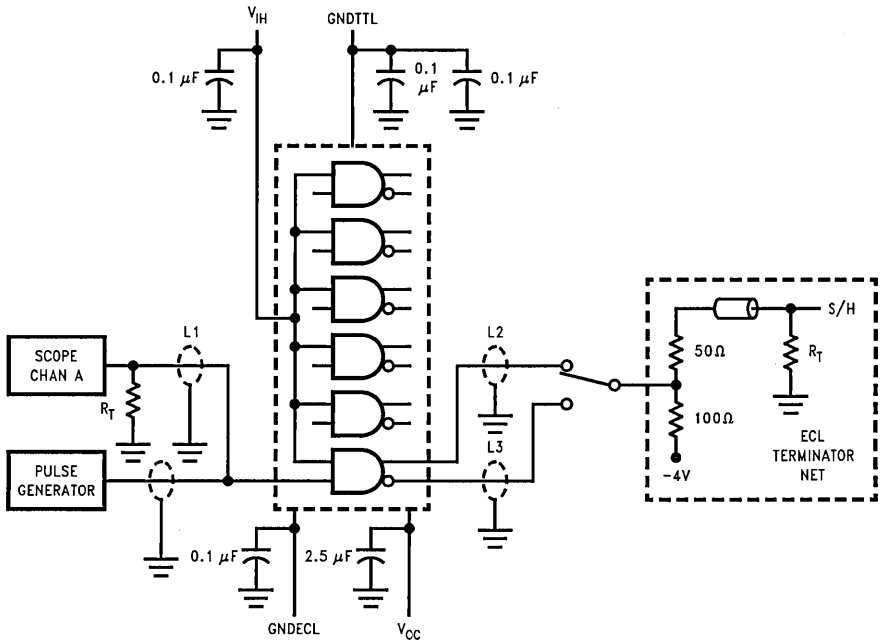
Switching Waveforms



TL/F/10939–6

FIGURE 1. Propagation Delay and Transition Times

Test Circuit



TL/F/10939–7

FIGURE 2. AC Test Circuit

Notes:

$V_{CC} = V_{CCA} = +2V$, GNDECL = GNDTTL = 3.0V
$V_{IH} = 0V$, $V_{IL} = -3V$
L1, L2 and L3 = equal length 50Ω impedance lines
R_T = 50Ω terminator internal to scope
Decoupling 0.1 μF from GND to V_{CC}, V_{EE} and V_{TTL}
All unused outputs are loaded with 50Ω to GND
C_L = Fixture and stray capacitance ≤ 3 pF

National Semiconductor

ADVANCE INFORMATION

100392
Single Supply Quint CMOS-to-ECL Translator with Cutoff Drivers

General Description

The 100392 is a quint translator for converting CMOS logic levels to positive referenced F100K ECL logic levels (or PECL). This translator is designed to operate from a single +5V supply, eliminating the need for a separate −5V supply. The differential outputs of the 100392, due to its high common mode rejection, overcomes voltage gradients between the CMOS and ECL ground systems.

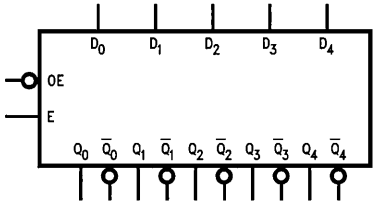
A LOW on the input enable pin (E) sets the true outputs to a LOW state and the inverting outputs to a HIGH state. A HIGH on the output enable pin (OE) sets both true and inverting outputs to a cutoff or high impedance state.

The outputs of the 100392 are designed to drive a double terminated 50Ω differential transmission line (25Ω load impedance).

Features

- Drives 25Ω load with cutoff capability
- Operates from a single +5V supply
- Differential ECL outputs
- 2000V ESD protection

Logic Symbol

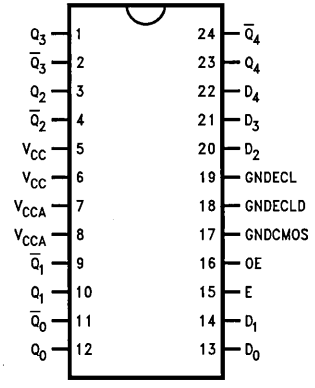


TL/F/10951–1

Pin Names	Description
D_0–D_4	Data Inputs (CMOS)
Q_0–Q_4	Data Outputs (PECL)
$\overline{Q}_0$–$\overline{Q}_4$	Inverting Data Outputs (PECL)
E	Enable Input (CMOS)
OE	Output Enable Input (CMOS)

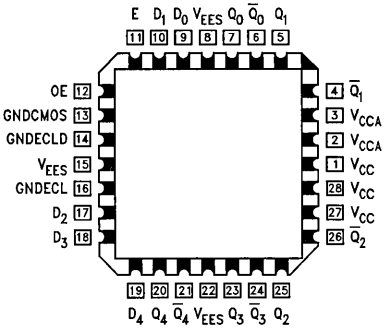
Connection Diagrams

24-Pin DIP/SOIC



TL/F/10951–2

28-Pin PCC



TL/F/10951–3

National Semiconductor

100393
Low Power 9-Bit ECL-to-TTL Translator with Latches

General Description

The 100393 is a 9-bit translator for converting F100K logic levels to FAST® TTL logic levels. A LOW on the latch enable (LE) latches the data at the input state. A HIGH on the LE makes the latches transparent. A HIGH on either the ECL or TTL output enable ($\overline{OE}$ ECL or $\overline{OE}$ TTL), holds the outputs in a high impedance state.

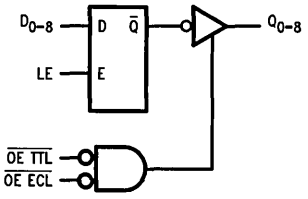
The 100393 is designed with FAST® TTL, 64 mA outputs for Bus Driving capability. All ECL inputs have 50 kΩ pull down resistors. When the inputs are either unconnected or at the same potential, the outputs will go LOW.

Features

- 64 mA I_{OL} drive capability
- 2000V ESD protection
- −4.2V to −5.7V operating range
- Latched outputs
- FAST® TTL outputs

Ordering Code: See Section 6

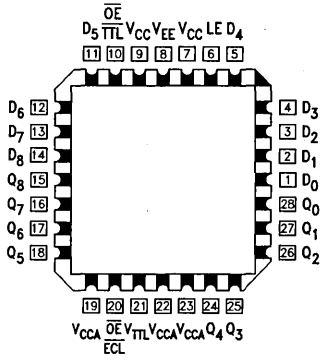
Logic Symbol



TL/F/10650–1

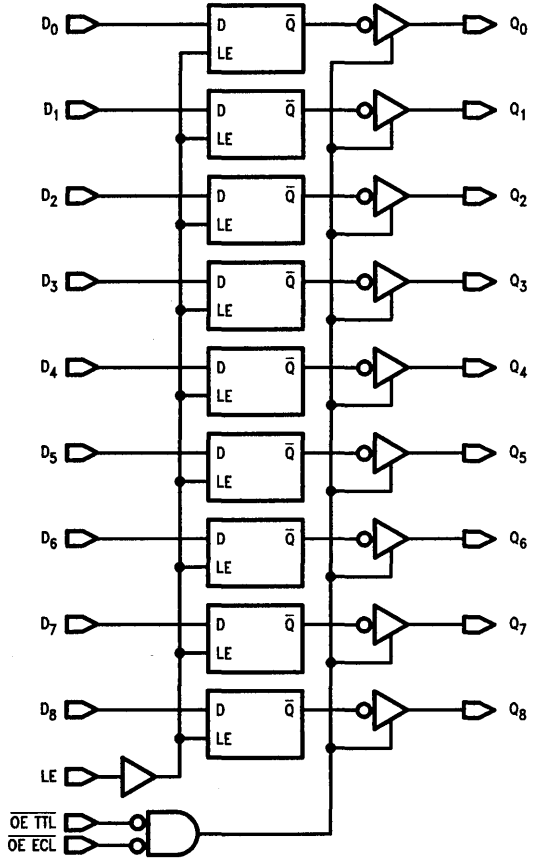
Pin Names	Description
D_0–D_8	Data Inputs (ECL)
Q_0–Q_8	Data Outputs (TTL)
LE	Latch Enable Input (ECL)
$\overline{OE}$ TTL	Output Enable (TTL)
$\overline{OE}$ ECL	Output Enable (ECL)

Connection Diagram



TL/F/10650–2

Logic Diagram



TL/F/10650–3

Truth Table

Inputs				Outputs
$\overline{OE}$ TTL	$\overline{OE}$ ECL	LE	D_N	Q_N
L	L	H	L	L
L	L	H	H	H
L	L	L	X	Latched
H	X	X	X	Z
X	H	X	X	Z

H = High Voltage Level
L = Low Voltage Level
X = Don't Care
Z = High Impedance

Absolute Maximum Ratings

Above which the useful life may be impaired (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature (T_{STG})	−65°C to +150°C
Maximum Junction Temperature (T_J)	+150°C
Case Temperature under Bias (T_C)	0°C to +85°C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
V_{TTL} Pin Potential to Ground Pin	−0.5V to +6.0V
ECL Input Voltage (DC)	V_{EE} to +0.5V
TTL Input Voltage	−0.5V to +7.0V
Output Current (DC Output HIGH)	+130 mA
ESD (Note 2)	≥2000V

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2. ESD testing conforms to MIL-STD-883, Method 3015.

Recommended Operating Conditions

Case Temperature (T_C)	0°C to +85°C
Supply Voltage	
V_{EE}	−5.7V to −4.2V
V_{TTL}	+4.5V to +5.5V

DC Electrical Characteristics

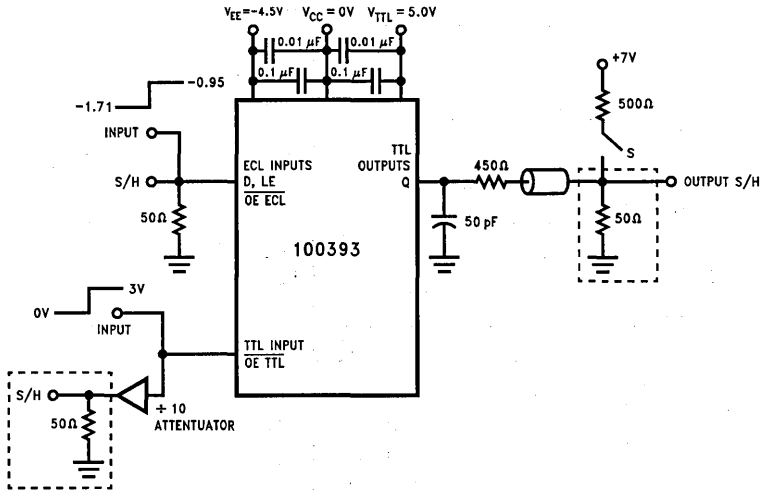
V_{EE} = −4.2V to −5.7V; V_{CC} = V_{CCA} = GND, V_{TTL} = +4.5V to +5.5V, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter		Min	Typ	Max	Units	Conditions	
V_{OH}	Output HIGH Voltage		2.5 2.0			V	I_{OH} = −1 mA I_{OH} = −15 mA	V_{IN} = V_{IL} (Min) or V_{IH} (Max)
V_{OL}	Output LOW Voltage				0.55 0.50	V	I_{OL} = 64 mA I_{OL} = 24 mA	V_{IN} = V_{IL} (Min) or V_{IH} (Max)
V_{IH}	Input HIGH Voltage	ECL Inputs	−1165		−870	mV	Guaranteed HIGH Signal for All Inputs	
		$\overline{OE}$ TTL	2.0			V		
V_{IL}	Input LOW Voltage	ECL Inputs	−1830		−1475	mV	Guaranteed LOW Signal for All Inputs	
		$\overline{OE}$ TTL			0.8	V		
I_{BVI}	Input Breakdown Current				10	μA	V_{BI} = 7.0V	
I_{IH}	ECL Input HIGH Current	ECL Inputs			240	μA	V_{IN} = V_{IH} (Max)	
		$\overline{OE}$ ECL			350			
	TTL Input HIGH Current	$\overline{OE}$ TTL			5.0	μA	V_{IN} = 2.7V	
I_{IL}	ECL Input LOW Current	ECL Inputs	0.5			μA	V_{IN} = V_{IL} (Min)	
	TTL Input LOW Current	$\overline{OE}$ TTL			−50	μA	V_{IN} = 0.5V	
I_{CEX}	Output HIGH Leakage Current				250	μA		
I_{OS}	Output Short-Circuit Current		−100		−225	mA	V_{OUT} = 0.0V, V_{TTL} = +5.5V	
I_{OZH}	TRI-STATE Current Output HIGH				+50	μA	V_{OUT} = +2.7V	
I_{OZL}	TRI-STATE Current Output LOW				−50	μA	V_{OUT} = 0.5V	
V_{FCD}	Input Clamp Diode Voltage				−1.2	V	I_{IN} = −18 mA	
I_{EE}	V_{EE} Power Supply Current		−39		−18	mA	Inputs Open	
I_{CCH}	V_{TTL} Power Supply Current HIGH				29	mA		
I_{CCL}	V_{TTL} Power Supply Current LOW				65	mA		
I_{CCZ}	V_{TTL} Power Supply Current TRI-STATE				49	mA		

Note 3. The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

AC Electrical Characteristics V_{EE} = −4.2V to −5.7V, V_{CC} = GND, V_{TTL} = +4.5V to +5.5V

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Data to Output	2.3	4.8	2.3	4.8	2.3	5.3	ns	*Figures 1, 2*
t_{PLH} t_{PHL}	Propagation Delay LE to Output	2.3	5.6	2.3	5.6	2.3	6.4	ns	*Figures 1, 2*
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ TTL ↓ to Q_N	2.0 3.5	5.5 8.0	2.0 3.5	5.5 8.0	2.0 3.5	5.5 8.0	ns	*Figure 3*
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ TTL ↑ to Q_N	2.0 2.0	6.0 5.5	2.0 2.0	6.0 5.0	2.0 2.0	6.0 5.0	ns	*Figure 3*
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ ECL ↑ to Q_N	2.4 3.2	5.6 8.5	2.4 3.2	5.6 8.5	2.4 3.2	5.6 8.5	ns	*Figure 4*
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ ECL ↓ to Q_N	2.4 3.2	6.0 7.6	2.4 3.2	6.0 7.6	2.4 3.2	6.0 7.6	ns	*Figure 4*
t_s	Setup Time, D_N to LE	0.7		0.7		0.7		ns	*Figures 1, 2*
t_h	Hold Time, D_N to LE	1.3		1.3		1.3		ns	*Figures 1, 2*
t_{pw} (L)	Pulse Width LOW, LE	2.0		2.0		2.0		ns	*Figures 1, 2*



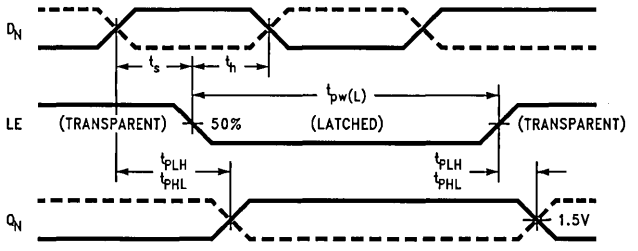
Switch Positions for Parameter Testing

Parameter	S-Position
t_{PLH}, t_{PHL}	Open
t_{PHZ}, t_{PZH}	Open
t_{PLZ}, t_{PZL}	Closed

TL/F/10650–4

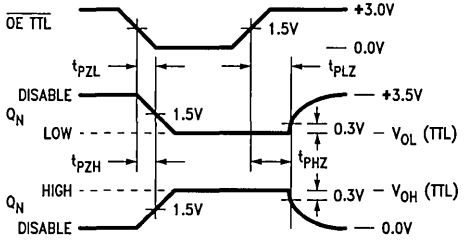
FIGURE 1. AC Test Setup

Switching Waveforms



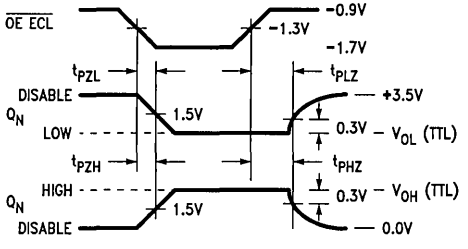
TL/F/10650–5

FIGURE 2. Propagation Delays, Setup and Hold Times, and Pulse Width



TL/F/10650–6

FIGURE 3. Enable and Disable Waveforms, $\overline{OE}$ TTL



TL/F/10650–7

FIGURE 4. Enable and Disable Waveforms, $\overline{OE}$ ECL

National Semiconductor

100395
Low Power 9-Bit ECL-to-TTL Translator with Registers

General Description

The 100395 is a 9-bit translator for converting F100K logic levels to FAST® TTL logic levels. A high on the output enable ($\overline{OE}$) holds the TTL outputs in a high impedance state. Two separate clock inputs are available for multiplexing and system level testing.

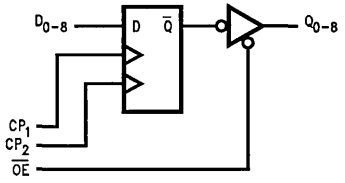
The 100395 is designed with FAST TTL 64 mA outputs for bus driving capability. All inputs have 50 kΩ pull down resistors. When the inputs are either unconnected or at the same potential, the outputs will go LOW.

Features

- 64 mA I_{OL} drive capability
- 2000V ESD protection
- −4.2V to −5.7V operating range
- Registered outputs
- FAST TTL outputs

Ordering Code: See Section 6

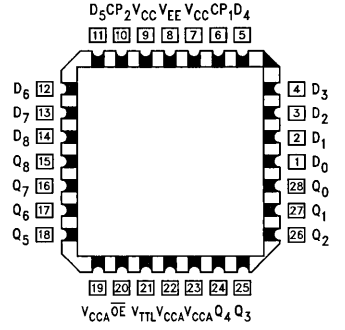
Logic Symbol



TL/F/10651–1

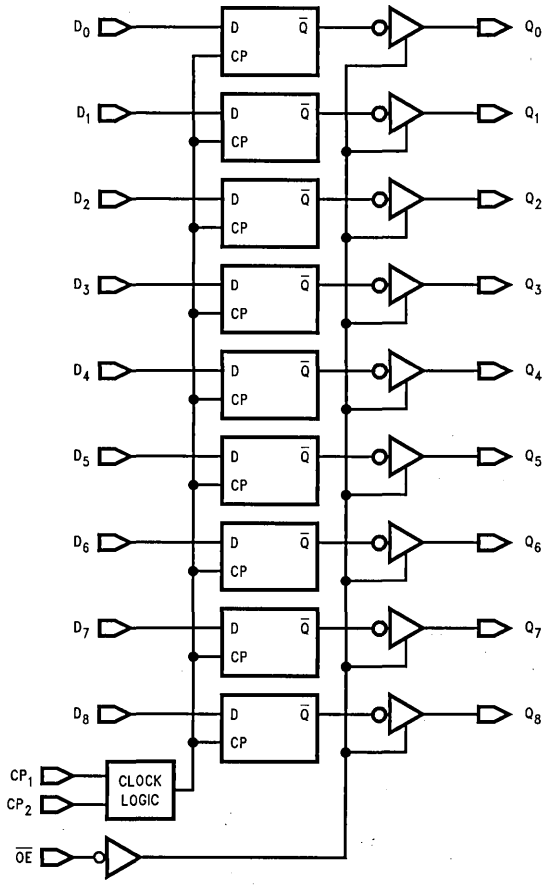
Pin Names	Description
D_0–D_8	Data Inputs (ECL)
Q_0–Q_8	Data Outputs (TTL)
$\overline{OE}$	Output Enable
CP_1, CP_2	Clock Inputs

Connection Diagram



TL/F/10651–2

Logic Diagram



TL/F/10651–3

Truth Table

Inputs				Outputs
CP_1	CP_2	$\overline{OE}$	D_N	Q_N
↓	L	L	L	L
L	↓	L	L	L
↓	L	L	H	H
L	↓	L	H	H
H	X	X	X	NC
X	H	X	X	NC
L	L	X	X	NC
X	X	H	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High Impedance
NC = No Change

Absolute Maximum Ratings

Above which the useful life may be impaired (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature (T_{STG})	−65°C to +150°C
Maximum Junction Temperature (T_J)	+150°C
Case Temperature under Bias (T_C)	0°C to +85°C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
V_{TTL} Pin Potential to Ground Pin	−0.5V to +6.0V
ECL Input Voltage (DC)	V_{EE} to +0.5V
TTL Input Voltage	−0.5V to +7.0V
Output Current (DC Output HIGH)	+130 mA
ESD (Note 2)	≥ 2000V

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: ESD testing conforms to MIL-STD-883, Method 3015.

Recommended Operating Conditions

Case Temperature (T_C)	0°C to +85°C
Supply Voltage	
V_{EE}	−5.7V to −4.2V
V_{TTL}	+4.5V to +5.5V

Commercial Version

DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions	
V_{OH}	Output HIGH Voltage	2.4			V	I_{OH} = −15 mA	V_{IN} = V_{IH} (Max) or V_{IL} (Min)
V_{OL}	Output LOW Voltage			0.55	V	I_{OL} = 64 mA	
V_{IH}	Input HIGH Voltage	−1165		−870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1830		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.5			μA	V_{IN} = V_{IL} (Min)	
I_{IH}	Input HIGH Current			240	μA	V_{IN} = V_{IH} (Max)	
I_{OZL}	TRI-STATE® Current Output High			−50	μA	V_{OUT} = +0.4V	
I_{OZH}	TRI-STATE Current Output Low			+50	μA	V_{OUT} = +2.7V	
I_{CEX}	Output High Leakage Current			250	μA	V_{OUT} = V_{CC}	
I_{OS}	Output Short-Circuit Current	−100		−225	mA		
I_{EE}	V_{EE} Power Supply Current	−67		−29	mA	Inputs Open	
I_{CCH}	V_{TTL} Power Supply Current High			29	mA		
I_{CCL}	V_{TTL} Power Supply Current Low			65	mA		
I_{CCZ}	V_{TTL} Power Supply Current TRI-STATE			49	mA		

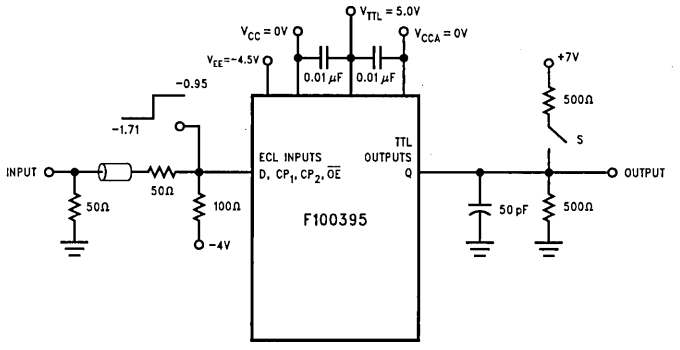
Note 3: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

PCC, AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = GND, V_{TTL} = +4.5V to +5.5V

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Clock to Output	2.30 3.00	5.00 5.60	2.30 3.00	5.00 5.60	2.30 3.40	5.00 6.40	ns	*Figures 1, 2*
t_{PZL} t_{PZH}	Output Enable Time $\overline{OE}$ ↓ to Q_N	3.20 2.40	7.60 5.60	3.20 2.40	7.60 5.60	3.20 2.40	7.60 5.60	ns	*Figures 1, 3*
t_{PLZ} t_{PHZ}	Output Disable Time $\overline{OE}$ ↑ to Q_N	3.20 2.40	7.60 5.60	3.20 2.40	7.60 5.60	3.20 2.40	7.60 5.60	ns	*Figures 1, 3*
t_H	Data to CP, $\overline{EN}$ Hold Time	1.5 1.5		1.5 1.5		1.5 1.5		ns	*Figures 1, 2*
t_S	Data to CP $\overline{EN}$ Setup Time	0.5 0.5		0.5 0.5		0.5 0.5		ns	*Figures 1, 2*
$t_{pw}(H)$	Clock Pulse Width	2.0		2.0		2.0		ns	*Figures 1, 2*

Test Circuit



TL/F/10651–4

Switch Positions for Parameter Testing

Parameter	S-Position
t_{PLH}, t_{PHL}	Open
t_{PHZ}, t_{PZH}	Open
t_{PLZ}, t_{PZL}	Closed

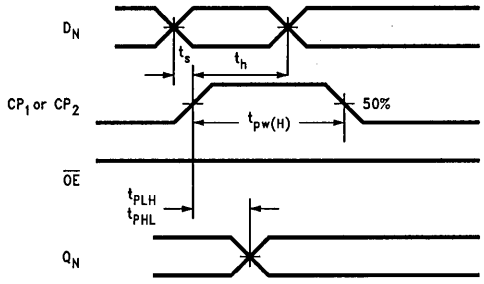
Notes:

V_{CC} = 0V, V_{CCA} = 0V, V_{EE} = −4.5V, V_{TTL} = +5V.

All unused outputs are loaded with 500Ω to GND. Decoupling capacitors are necessary in the test and end application environment. When V_{CC} and V_{CCA} are common to a single power plane, typically 0.0V, decouple V_{TTL} to that plane with one 0.01 μF capacitor.

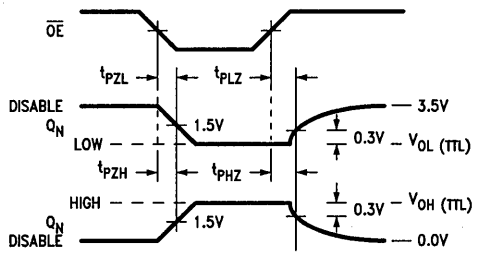
FIGURE 1. AC Test Circuit

Switching Waveforms



TL/F/10651–5

FIGURE 2. Propagation Delay and Transition Times



TL/F/10651–6

FIGURE 3. Enable and Disable Waveforms, $\overline{OE}$ to Q_N

National Semiconductor

100397
Quad Differential ECL/TTL Translating Transceiver with Latch

General Description

The 100397 is a quad latched transceiver designed to convert TTL logic levels to differential F100K ECL logic levels and vice versa. This device was designed with the capability of driving a differential 25Ω ECL load with cutoff capability, and will sink a 64 mA TTL load. The 100397 is ideal for mixed technology applications utilizing either an ECL or TTL backplane.

The direction of translation is set by the direction control pin (DIR). The DIR pin on the 100397 accepts F100K ECL logic levels. An ECL LOW on DIR sets up the ECL pins as inputs and TTL pins as outputs. An ECL HIGH on DIR sets up the TTL pins as inputs and ECL pins as outputs.

A LOW on the output enable input pin (OE) holds the ECL output in a cut-off state and the TTL outputs at a high impedance level. A HIGH on the latch enable input (LE) latches the data at both inputs even though only one output is enabled at the time. A LOW on LE makes the latch transparent.

The cut-off state is designed to be more negative than a normal ECL LOW level. This allows the output emitter-followers to turn off when the termination supply is −2.0V, presenting a high impedance to the data bus. This high impedance reduces termination power and prevents loss of low state noise margin when several loads share the bus.

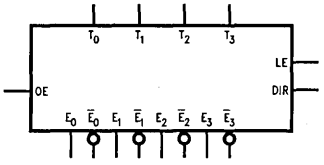
The 100397 is designed with FAST® TTL output buffers, featuring optimal DC drive and capable of quickly charging and discharging highly capacitive loads. All inputs have 50 KΩ pull-down resistors.

Features

- Differential ECL input/output structure
- 64 mA FAST TTL outputs
- 25Ω differential ECL outputs with cut-off
- Bi-directional translation
- 2000V ESD protection
- Latched outputs
- TRI-STATE® outputs
- Voltage compensated operating range = −4.2V to −5.7V

Ordering Code: See Section 6

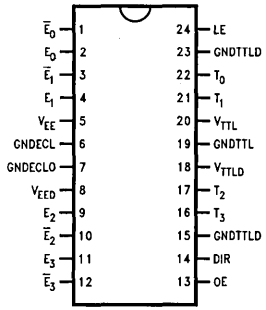
Logic Symbol



TL/F/10971–1

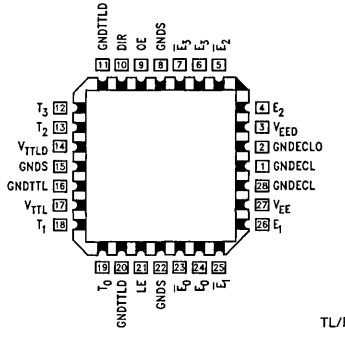
Connection Diagrams

24-Pin DIP



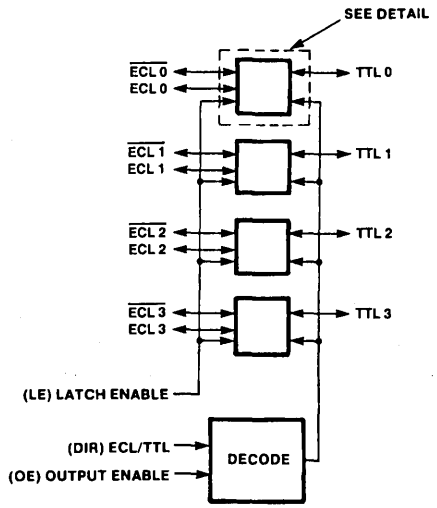
TL/F/10971–2

28-Pin PCC



TL/F/10971–3

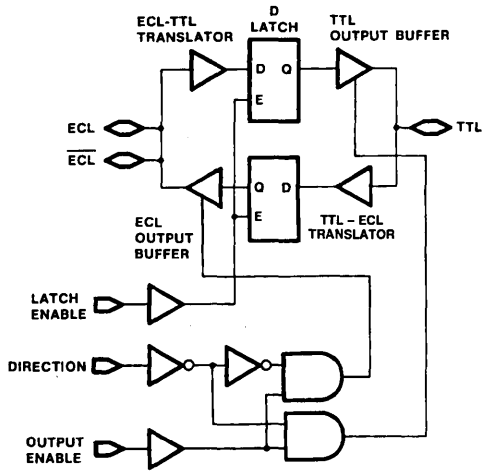
Functional Diagram



TL/F/10971–5

Note: LE, DIR, and OE use ECL logic levels

Detail



TL/F/10971–6

Pin Names	Description
E_0–E_3	ECL Data I/O
$\overline{E}_0$–$\overline{E}_3$	Complementary ECL Data I/O
T_0–T_3	TTL Data I/O
OE	Output Enable Input (ECL Levels)
LE	Latch Enable Input (ECL Levels)
DIR	Direction Control Input (ECL levels)
GNDECL	ECL Ground
GNDECLO	ECL Output Ground
GNDS	ECL Ground-to-Substrate
V_{EE}	ECL Quiescent Power Supply
V_{EED}	ECL Dynamic Power Supply
GNDTTL	TTL Quiescent Ground
GNDTTLD	TTL Dynamic Ground
V_{TTL}	TTL Quiescent Power Supply
V_{TTLD}	TTL Dynamic Power Supply

All pins function at 100K ECL levels except for T_0–T_3.

Truth Table

LE	DIR	OE	ECL Port	TTL Port	Notes
0	0	0	LOW (Cut-Off)	Z	
0	0	1	Input	Output	1, 4
0	1	0	LOW (Cut-Off)	Z	
0	1	1	Output	Input	2, 4
1	0	0	Input	Z	1, 3
1	0	1	Latched	X	1, 3
1	1	0	LOW (Cut-Off)	Input	2, 3
1	1	1	Latched	X	2, 3

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High Impedance

Note 1: ECL input to TTL output mode.

Note 2: TTL input to ECL output mode.

Note 3: Retains data present before LE set HIGH.

Note 4: Latch is transparent.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature (T_{STG})	−65°C to +150°C
Maximum Junction Temperature (T_J)	
Ceramic	+175°C
Plastic	+150°C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
V_{TTL} Pin Potential to Ground Pin	−0.5V to +6.0V
ECL Input Voltage (DC)	V_{EE} to +0.5V
ECL Output Current (DC Output HIGH)	−50 mA
TTL Input Voltage (Note 3)	−0.5V to +7.0V
TTL Input Current (Note 3)	−30 mA to +5.0 mA
Voltage Applied to Output in HIGH State TRI-STATE Output	−0.5V to +5.5V
Current Applied to TTL Output in LOW State (Max)	Twice the Rated I_{OL} (mA)
ESD (Note 2)	≥2000V

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: ESD testing conforms to MIL-STD-883, Method 3015.

Note 3: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Case Temperature (T_C)	
Commercial	0°C to +85°C
Industrial	−40°C to +85°C
Military	−55°C to +125°C
ECL Supply Voltage (V_{EE})	−5.7V to −4.2V
TTL Supply Voltage (V_{TTL})	+4.5V to +5.5V

Commercial Version

TTL-to-ECL DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, GND = 0V, T_C = 0°C to +85°C, V_{TTL} = +4.5V to +5.5V (Note 4)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{OH}	Output HIGH Voltage	−1025	−955	−870	mV	V_{IN} = $V_{IH(Max)}$ or $V_{IL(Min)}$ Loading with 50Ω to − 2V
V_{OL}	Output LOW Voltage	−1830	−1705	−1620	mV	
	Cutoff Voltage		−2000	−1950	mV	OE and LE Low, DIR High V_{IN} = $V_{IH(Max)}$ or V_{IL}(Min), Loading with 50Ω to −2V
V_{OHC}	Output HIGH Voltage Corner Point High	−1035			mV	V_{IN} = $V_{IH(Min)}$ or $V_{IL(Max)}$ Loading with 50Ω to −2V
V_{OLC}	Output LOW Voltage Corner Point Low			−1610	mV	
V_{IH}	Input HIGH Voltage	2.0		5.0	V	Over V_{TTL}, V_{EE}, T_C Range
V_{IL}	Input LOW Voltage	0		0.8	V	Over V_{TTL}, V_{EE}, T_C Range
I_{IH}	Input HIGH Current			5.0	μA	V_{IN} = +2.7V
I_{BVIT}	Input HIGH Current Breakdown (I/O)			0.5	mA	V_{IN} = 5.5V
I_{IL}	Input LOW Current	−1.0			mA	V_{IN} = +0.5V
V_{FCD}	Input Clamp Diode Voltage	−1.2			V	I_{IN} = −18 mA
I_{EE}	V_{EE} Supply Current	−99		−50		LE Low, OE and DIR High Inputs Open
I_{EEZ}	V_{EE} Supply Current	−159		−90		LE and OE Low, Dir High Inputs Open

Note 4: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

Commercial Version (Continued)

ECL-to-TTL DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, GND = 0V, T_C = 0°C to +85°C, C_L = 50 pF, V_{TTL} = +4.5V to +5.5V (Note 4)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{OH}	Output HIGH Voltage	2.7 2.4	3.1 2.9		V V	I_{OH} = −3 mA, V_{TTL} = 4.75V I_{OH} = −3 mA, V_{TTL} = 4.50V
V_{OL}	Output LOW Voltage		0.3	0.5	V	I_{OL} = 24 mA, V_{TTL} = 4.50V
V_{IH}	Input HIGH Voltage	−1165		−870	mV	Guaranteed HIGH Signal for All Inputs
V_{IL}	Input LOW Voltage	−1830		−1475	mV	Guaranteed LOW Signal for All Inputs
V_{DIFF}	Input Voltage Differential	150			mV	Required for Full Output Swing
V_{CM}	Common Mode Voltage	GNDECL − 2.0		GNDECL − 0.5	V	
I_{IH}	Input HIGH Current E_0–E_3, $\overline{E}_0$–$\overline{E}_3$ OE, LE, DIR			 240 35	 μA	V_{IN} = $V_{IH(Max)}$
I_{CEX}	Output HIGH Leakage Current			50	μA	V_{OUT} = V_{TTL}
I_{ZZ}	Bus Drainage Test			500	μA	V_{OUT} = 5.25V V_{TTL} = 0.0V
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL(Min)}$
I_{OZHT}	TRI-STATE Current Output High			70	μA	V_{OUT} = +2.7V
I_{OZLT}	TRI-STATE Current Output Low	−650			μA	V_{OUT} = +0.5V
I_{OS}	Output Short-Circuit Current	−100		−225	mA	V_{OUT} = 0.0V, V_{TTL} = +5.5V
I_{TTL}	V_{TTL} Supply Current			39 27 39	mA mA mA	TTL Outputs LOW TTL Outputs HIGH TTL Outputs in TRI-STATE

Note 4: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

Commercial Version (Continued)

DIP and PCC TTL-to-ECL AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{TTL} = +4.5V to +5.5V

Symbol	Parameter	T_C = 0°C		T_C = 25°C		T_C = 85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
F_{Max}	Maximum Clock Frequency	180		180		180		MHz	
t_{PLH} t_{PHL}	T_n to E_n, $\overline{E}_n$ (Transparent)	0.9	2.1	0.8	2.2	0.7	2.5	ns	*Figures 1, 3*
t_{PLH} t_{PHL}	LE to E_n, $\overline{E}_n$	1.2	2.3	1.3	2.4	1.4	2.5	ns	*Figures 1, 3*
t_{PZH}	OE to E_n, $\overline{E}_n$ (Cutoff to High)	2.5	4.5	2.5	4.5	2.5	4.6	ns	*Figures 1, 3*
t_{PHZ}	OE to E_n, $\overline{E}_n$ (High to Cutoff)	2.1	3.8	2.3	4.0	2.5	4.5	ns	*Figures 1, 3*
t_{PHZ}	DIR to E_n, $\overline{E}_n$ (High to Cutoff)	2.0	3.5	2.1	3.7	2.3	4.2	ns	*Figures 1, 3*
t_S	T_n to LE	0.8		0.8		0.8		ns	*Figure 1, 3*
t_H	T_n to LE	0.6		0.6		0.6		ns	*Figures 1, 3*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.8	2.8	0.8	2.8	0.8	2.8	ns	*Figures 1, 3*

DIP and PCC ECL-to-TTL AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{TTL} = +4.5V to +5.5V, C_L = 50 pF

Symbol	Parameter	T_C = 0°C		T_C = 25°C		T_C = 85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
F_{Max}	Maximum Clock Frequency	75		75		75		MHz	
t_{PLH} t_{PHL}	E_n, $\overline{E}_n$ to T_n (Transparent)	1.7	4.9	1.7	5.1	1.8	5.8	ns	*Figures 2, 4*
t_{PLH} t_{PHL}	LE to T_n	2.2 3.3	4.0 5.2	2.2 3.4	4.0 5.4	2.3 3.8	4.1 6.1	ns	*Figures 2, 4*
t_{PZH} t_{PZL}	OE to T_n (Enable Time)	3.2 4.9	5.6 8.3	3.3 5.1	5.7 8.5	3.6 5.6	6.3 9.2	ns	*Figures 2, 5*
t_{PHZ} t_{PLZ}	OE to T_n (Disable Time)	3.6 3.4	8.6 6.9	3.5 3.5	8.3 6.7	3.5 3.6	7.5 6.7	ns	*Figures 2, 5*
t_{PHZ} t_{PLZ}	DIR to T_n (Disable Time)	3.5 3.4	8.1 6.8	3.5 3.4	8.1 6.7	3.5 3.6	7.6 6.7	ns	*Figures 2, 6*
t_S	E_n, $\overline{E}_n$ to LE	0.6		0.6		0.6		ns	*Figures 2, 4*
t_H	E_n, $\overline{E}_n$ to LE	0.7		0.7		0.7		ns	*Figures 2, 4*
$t_{PW}(L)$	Pulse Width LE	2.0		2.0		2.0		ns	*Figures 2, 4*

Industrial Version

TTL-to-ECL DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, GND = 0V, T_C = −40°C to +85°C, V_{TTL} = +4.5V to +5.5V (Note 1)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{OH}	Output HIGH Voltage	−1085	−955	−870	mV	V_{IN} = $V_{IH(Max)}$ or $V_{IL(Min)}$ Loading with 50Ω to −2V
V_{OL}	Output LOW Voltage	−1830	−1705	−1575	mV	
	Cutoff Voltage		−2000	−1900	mV	OE and LE Low, DIR High V_{IN} = $V_{IH(Max)}$ or $V_{IL(Min)}$, Loading with 50Ω to −2V
V_{OHC}	Output HIGH Voltage Corner Point High	−1095			mV	V_{IN} = $V_{IH(Min)}$ or $V_{IL(Max)}$ Loading with 50Ω to −2V
V_{OLC}	Output LOW Voltage Corner Point Low			−1565	mV	
V_{IH}	Input HIGH Voltage	2.0		5.0	V	Over V_{TTL}, V_{EE}, T_C Range
V_{IL}	Input LOW Voltage	0		0.8	V	Over V_{TTL}, V_{EE}, T_C Range
I_{IH}	Input HIGH Current			5.0	μA	V_{IN} = +2.7V
I_{BVIT}	Input HIGH Current Breakdown (I/O)			0.5	mA	V_{IN} = 5.5V
I_{IL}	Input LOW Current	−1.0			mA	V_{IN} = +0.5V
V_{FCD}	Input Clamp Diode Voltage	−1.2			V	I_{IN} = −18 mA
I_{EE}	V_{EE} Supply Current	−99		−40		LE Low, OE and DIR High Inputs Open
I_{EEZ}	V_{EE} Supply Current	−159		−90		LE and OE Low, Dir High Inputs Open

Note 1: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

Industrial Version (Continued)

ECL-to-TTL DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, GND = 0V, T_C = −40°C to +85°C, C_L = 50 pF, V_{TTL} = +4.5V to +5.5V (Note 1)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{OH}	Output HIGH Voltage	2.7 2.4	3.1 2.9		V V	I_{OH} = −3 mA, V_{TTL} = 4.75V I_{OH} = −3 mA, V_{TTL} = 4.50V
V_{OL}	Output LOW Voltage		0.3	0.5	V	I_{OL} = 24 mA, V_{TTL} = 4.50V
V_{IH}	Input HIGH Voltage	−1170		−870	mV	Guaranteed HIGH Signal for All Inputs
V_{IL}	Input LOW Voltage	−1830		−1480	mV	Guaranteed LOW Signal for All Inputs
V_{DIFF}	Input Voltage Differential	150			mV	Required for Full Output Swing
V_{CM}	Common Mode Voltage	GNDECL − 2.0		GNDECL − 0.5	V	
I_{IH}	Input HIGH Current E_0–E_3, $\overline{E}_0$–$\overline{E}_3$ OE, LE, DIR			 300 35	 μA	V_{IN} = $V_{IH(Max)}$
I_{CEX}	Output HIGH Leakage Current			50	μA	V_{OUT} = V_{TTL}
I_{ZZ}	Bus Drainage Test			500	μA	V_{OUT} = 5.25V V_{TTL} = 0.0V
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL(Min)}$
I_{OZHT}	TRI-STATE Current Output High			70	μA	V_{OUT} = +2.7V
I_{OZLT}	TRI-STATE Current Output Low	−650			μA	V_{OUT} = +0.5V
I_{OS}	Output Short-Circuit Current	−100		−225	mA	V_{OUT} = 0.0V, V_{TTL} = +5.5V
I_{TTL}	V_{TTL} Supply Current			39 27 39	mA mA mA	TTL Outputs LOW TTL Outputs HIGH TTL Outputs in TRI-STATE

Note 1: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

Industrial Version (Continued)

PCC TTL-to-ECL AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{TTL} = +4.5V to +5.5V

Symbol	Parameter	T_C = −40°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
F_{Max}	Maximum Clock Frequency	180		180		180		MHz	
t_{PLH} t_{PHL}	T_n to E_n, $\overline{E}_n$ (Transparent)	0.9	2.4	0.8	2.2	0.7	2.5	ns	*Figures 1, 3*
t_{PLH} t_{PHL}	LE to E_n, $\overline{E}_n$	1.2	2.3	1.3	2.4	1.4	2.5	ns	*Figures 1, 3*
t_{PZH}	OE to E_n, $\overline{E}_n$ (Cutoff to High)	1.9	3.8	2.5	4.5	2.5	4.6	ns	*Figures 1, 3*
t_{PHZ}	OE to E_n, $\overline{E}_n$ (High to Cutoff)	2.5	4.7	2.3	4.0	2.5	4.5	ns	*Figures 1, 3*
t_{PHZ}	DIR to E_n, $\overline{E}_n$ (High to Cutoff)	1.8	3.5	2.1	3.7	2.3	4.2	ns	*Figures 1, 3*
t_S	T_n to LE	0.8		0.8		0.8		ns	*Figures 1, 3*
t_H	T_n to LE	0.6		0.6		0.6		ns	*Figures 1, 3*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.8	2.8	0.8	2.8	0.8	2.8	ns	*Figures 1, 3*

PCC ECL-to-TTL AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{TTL} = +4.5V to +5.5V, C_L = 50 pF

Symbol	Parameter	T_C = −40°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
F_{Max}	Maximum Clock Frequency	75		75		75		MHz	
t_{PLH} t_{PHL}	E_n, $\overline{E}_n$ to T_n (Transparent)	1.7	4.9	1.7	5.1	1.8	5.8	ns	*Figures 2, 4*
t_{PLH} t_{PHL}	LE to T_n	2.2 3.3	4.3 5.2	2.2 3.4	4.0 5.4	2.3 3.8	4.1 6.1	ns	*Figures 2, 4*
t_{PZH} t_{PZL}	OE to T_n (Enable Time)	3.1 4.8	5.6 8.3	3.3 5.1	5.7 8.5	3.6 5.6	6.3 9.2	ns	*Figures 2, 5*
t_{PHZ} t_{PLZ}	OE to T_n (Disable Time)	3.5 3.2	9.2 7.3	3.5 3.5	8.3 6.7	3.5 3.6	7.5 6.7	ns	*Figures 2, 5*
t_{PHZ} t_{PLZ}	DIR to T_n (Disable Time)	3.5 3.2	8.8 7.2	3.5 3.4	8.1 6.7	3.5 3.6	7.6 6.7	ns	*Figures 2, 6*
t_S	E_n, $\overline{E}_n$ to LE	0.6		0.6		0.6		ns	*Figures 2, 4*
t_H	E_n, $\overline{E}_n$ to LE	0.7		0.7		0.7		ns	*Figures 2, 4*
$t_{PW}(L)$	Pulse Width LE	2.0		2.0		2.0		ns	*Figures 2, 4*

Military Version—Preliminary

TTL-to-ECL DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, GND = 0V, T_C = −55°C to +125°C, V_{TTL} = +4.5V to +5.5V

Symbol	Parameter	Min	Max	Units	T_C	Conditions		Notes
V_{OH}	Output HIGH Voltage	−1025	−870	mV	0°C to +125°C	V_{IN} = V_{IH} (Max) or V_{IL} (Min)	Loading with 50Ω to −2.0V	1, 2, 3
		−1085	−870	mV	−55°C			
V_{OL}	Output LOW Voltage	−1830	−1620	mV	0°C to +125°C			
		−1830	−1555	mV	−55°C			
	Cutoff Voltage		−1950	mV	0°C to +125°C	OE or DIR Low		
			−1850	mV	−55°C			
V_{OHC}	Output HIGH Voltage	−1035		mV	0°C to +125°C	V_{IN} = V_{IH} (Min) or V_{IL} (Max)	Loading with 50Ω to −2.0V	1, 2, 3
		−1085		mV	−55°C			
V_{OLC}	Output LOW Voltage		−1610	mV	0°C to +125°C			
			−1555	mV	−55°C			
V_{IH}	Input HIGH Voltage	2.0		V	−55°C to +125°C	Over V_{TTL}, V_{EE}, T_C Range		1, 2, 3, 4
V_{IL}	Input LOW Voltage		0.8	V	−55°C to +125°C	Over V_{TTL}, V_{EE}, T_C Range		1, 2, 3, 4
I_{IH}	Input HIGH Current		70	μA	−55°C to 125°C	V_{IN} = +2.7V		1, 2, 3
	Breakdown Test		1.0	mA	−55°C to +125°C	V_{IN} = +5.5V		
I_{IL}	Input LOW Current	−1.0		mA	−55°C to +125°C	V_{IN} = +0.5V		1, 2, 3
V_{FCD}	Input Clamp Diode Voltage	−1.2		V	−55°C to +125° C	I_{IN} = −18 mA		1, 2, 3
I_{EE}	V_{EE} Supply Current	−165 −175	−65 −65	mA	−55°C to +125°C	LE Low, OE and DIR High Inputs Open V_{EE} = −4.2V to −4.8V V_{EE} = −4.2V to −5.7V		1, 2, 3

Military Version—Preliminary (Continued)

ECL-to-TTL DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, GND = 0V, T_C = −55°C to +125°C, C_L = 50 pF, V_{TTL} = +4.5V to + 5.5V

Symbol	Parameter	Min	Max	Units	T_C	Conditions	Notes
V_{OH}	Output HIGH Voltage	2.5 2.4		mV	0°C to +125°C −55°C	I_{OH} = −1 mA, V_{TTL} = 4.50V I_{OH} = −3 mA, V_{TTL} = 4.50V	1, 2, 3
V_{OL}	Output LOW Voltage		0.5	mV	−55°C to +125°C	I_{OL} = 24 mA, V_{TTL} = 4.50V	
V_{IH}	Input HIGH Voltage	−1165	−870	mV	−55°C to +125°C	Guaranteed HIGH Signal for All Inputs	1, 2, 3, 4
V_{IL}	Input LOW Voltage	−1830	−1475	mV	−55°C to +125°C	Guaranteed LOW Signal for All Inputs	1, 2, 3, 4
I_{IH}	Input HIGH Current		350 500	μA	0°C to +125°C	V_{EE} = −5.7V V_{IN} = $V_{IH(Max)}$	1, 2, 3
I_{IL}	Input LOW Current	0.50		μA	−55°C to +125°C	V_{EE} = −4.2V V_{IN} = $V_{IL(Min)}$	1, 2, 3
I_{OZHT}	TRI-STATE Current Output High		70	μA	−55°C to +125°C	V_{OUT} = +2.7V	1, 2, 3
I_{OZLT}	TRI-STATE Current Output Low	−1.0		mA	−55°C to +125°C	V_{OUT} = +0.5V	1, 2, 3
I_{OS}	Output Short-Circuit CURRENT	−150	−60	mA	−55°C to +125°C	V_{OUT} = 0.0V, V_{TTL} = +5.5V	1, 2, 3
I_{TTL}	V_{TTL} Supply Current		75 50 70	mA mA mA	−55°C to +125°C	TTL Outputs Low TTL Output High TTL Output in TRI-STATE	1, 2, 3

Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals −55°C), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 2: Screen tested 100% on each device at −55°C, +25°C, and +125°C, Subgroups, 1, 2, 3, 7, and 8.

Note 3: Sample tested (Method 5005, Table I) on each manufactured lot at −55°C, +25°C, and +125°C, Subgroups A1, 2, 3, 7, and 8.

Note 4: Guaranteed by applying specified input condition and testing V_{OH}/V_{OL}.

TTL-to-ECL AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{TTL} = +4.5V to +5.5V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = −55°C		T_C = +25°C		T_C = +125°C		Units	Conditions	Notes
		Min	Max	Min	Max	Min	Max			
t_{PLH} t_{PHL}	T_n to E_n, $\overline{E}_n$ (Transparent)	1.0	3.9	1.1	3.6	1.1	4.0	ns	*Figures 1, 2*	1, 2, 3
t_{PLH} t_{PHL}	LE to E_n, $\overline{E}_n$	1.2	3.8	1.4	3.7	1.6	4.2	ns	*Figures 1, 2*	
t_{PZH}	OE to E_n, $\overline{E}_n$ (Cutoff to HIGH)	1.0	4.3	1.5	4.4	1.7	5.2	ns	*Figures 1, 2*	
t_{PHZ}	OE to E_n, $\overline{E}_n$ (HIGH to Cutoff)	1.5	5.1	1.6	4.5	1.6	5.1	ns	*Figures 1, 2*	
t_{PHZ}	DIR to E_n, $\overline{E}_n$ (HIGH to Cutoff)	1.6	4.7	1.6	4.3	1.7	4.9	ns	*Figures 1, 2*	1, 2, 3
t_{set}	T_n to LE	2.5		2.0		2.5		ns	*Figures 1, 2*	4
t_{hold}	T_n to LE	2.5		2.0		2.5		ns	*Figures 1, 2*	
t_{pw}(H)	Pulse Width LE	2.5		2.0		2.5		ns	*Figures 1, 2*	4
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.4	2.3	0.5	2.1	0.4	2.4	ns	*Figures 1, 2*	4

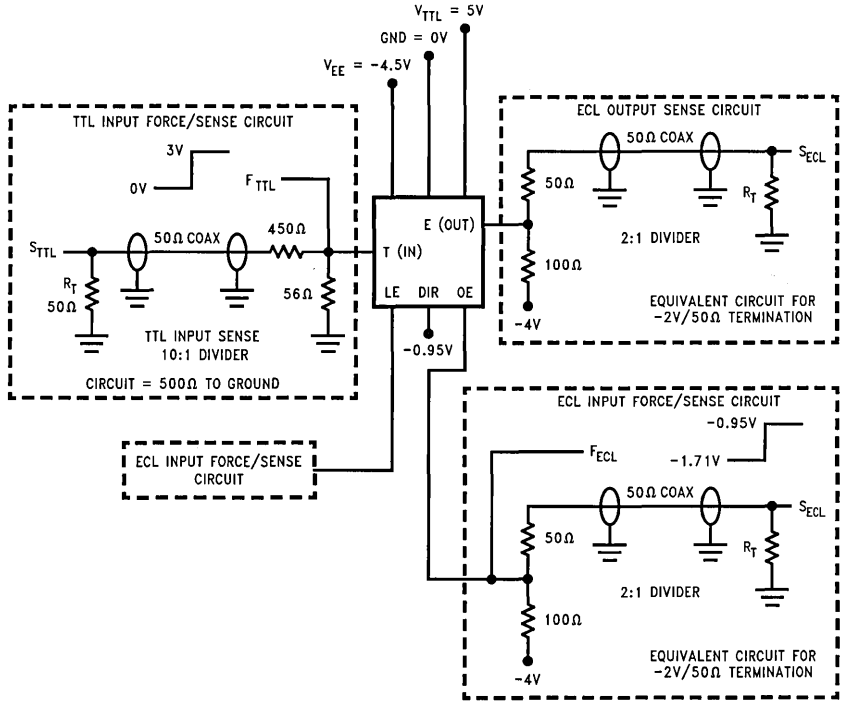
Military Version—Preliminary (Continued)

ECL-to-TTL AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{TTL} = +4.5V to +5.5V, GND = 0V, C_L = 50 pF

Symbol	Parameter	T_C = −55°C		T_C = 25°C		T_C = +125°C		Units	Conditions	Notes
		Min	Max	Min	Max	Min	Max			
t_{PLH} t_{PHL}	E_n, $\overline{E}_n$ to T_n (Transparent)	2.3	6.4	2.4	5.6	2.6	6.3	ns	*Figures 3, 4*	1, 2, 3
t_{PLH} t_{PHL}	LE to T_n	3.1	8.0	3.1	7.3	3.3	8.0	ns	*Figures 3, 4*	
t_{PZH} t_{PZL}	OE to T_n (Enable Time)	3.2 3.6	8.9 9.4	3.7 4.0	9.0 9.3	4.0 4.3	10.2 10.4	ns	*Figures 3, 5*	1, 2, 3
t_{PHZ} t_{PLZ}	OE to T_n (Disable Time)	3.2 3.0	9.9 9.7	3.3 3.4	9.0 8.8	3.5 4.1	9.4 10.6	ns	*Figures 3, 5*	
t_{PHZ} t_{PLZ}	DIR to T_n (Disable Time)	2.6 2.7	9.4 8.5	2.8 3.1	8.8 8.0	2.9 4.0	9.1 9.7	ns	*Figures 3, 6*	
t_{set}	E_n, $\overline{E}_n$ to LE	2.5		2.0		2.5		ns	*Figures 3, 4*	4
t_{hold}	E_n, $\overline{E}_n$ to LE	3.0		2.5		3.0		ns	*Figures 3, 4*	
t_{pw}(H)	Pulse Width LE	2.5		2.0		5.0		ns	*Figures 3, 4*	4

Test Circuitry (TTL-to-ECL)



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Note 1: R_t = 50Ω termination. When an input or output is being monitored by a scope, R_t is supplied by the scope's 50Ω resistance. When an input or output is not being moinitored, and external 50Ω resistance must be applied to serve as R_t.

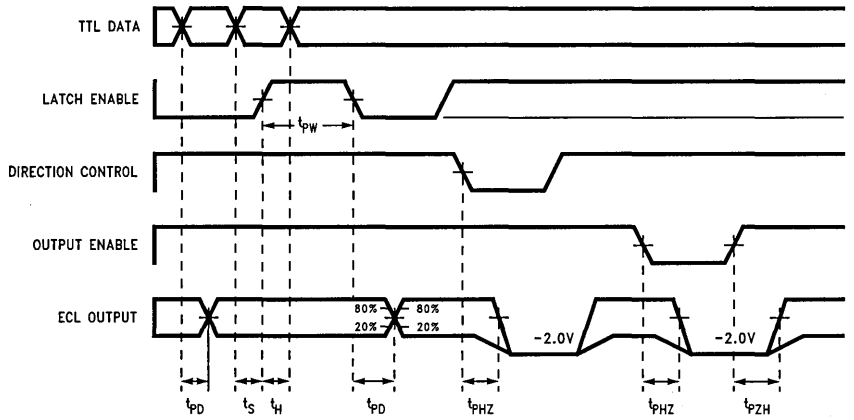
Note 2: TTL and ECL force signals are brought to the DUT via 50Ω coax lines.

Note 3: V_{TTL} is decoupled to grouond with 0.1 μF to ground, V_{EE} is decoupled to ground with 0.01 μF and GND is connected to ground.

Note 4: For ECL input pins, the equivelent force/sense circuitry is optional.

FIGURE 1. TTL-to-ECL AC Test Circuit

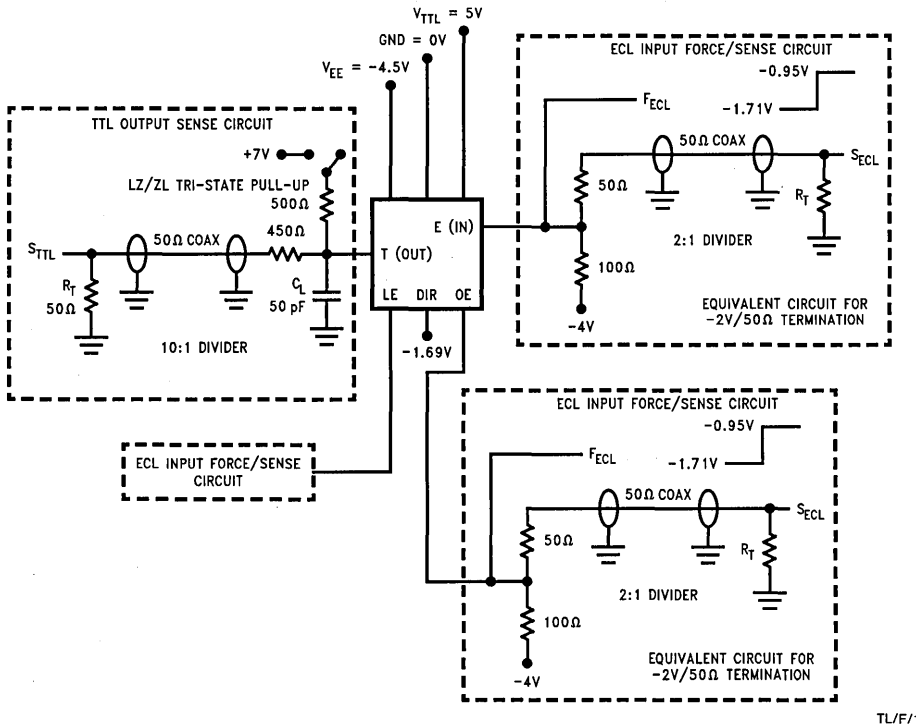
Switching Waveforms (TTL-to-ECL)



TL/F/10971–9

FIGURE 2. TTL to ECL Transition—Propagation Delay and Transition Times

Test Circuitry (ECL-to-TTL)



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Note 1: R_t = 50Ω termination. When an input or output is being monitored by a scope, R_t is supplied by the scope's 50Ω resistance. When an input or output is not being moinitored, and external 50Ω resistance must be applied to serve as R_t.

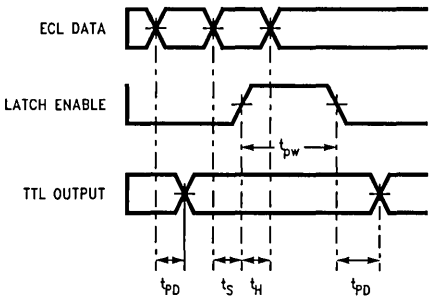
Note 2: The TTL Tri-State pull up switch is connected to +7V only for ZL and LZ tests.

Note 3: TTL and ECL force signals are brought to the DUT via 50Ω coax lines.

Note 4: V_{TTL} is decoupled to grouond with 0.1 μF to ground, V_{EE} is decoupled to ground with 0.01 μF and GND is connected to ground.

FIGURE 3. ECL-to-TTL AC Test Circuit

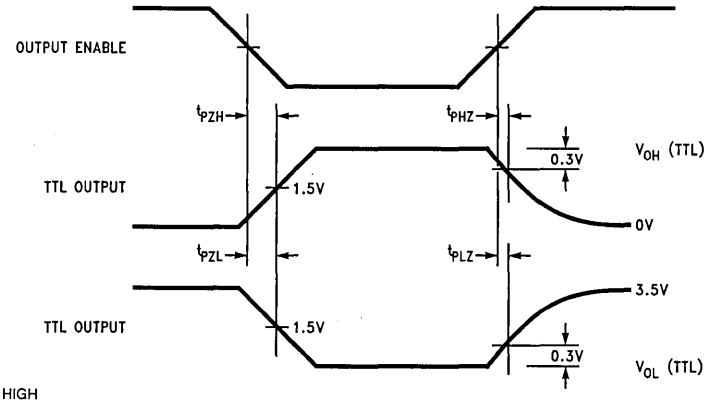
Switching Waveforms (Continued)



Note: DIR is LOW, and OE is HIGH

TL/F/10971–11

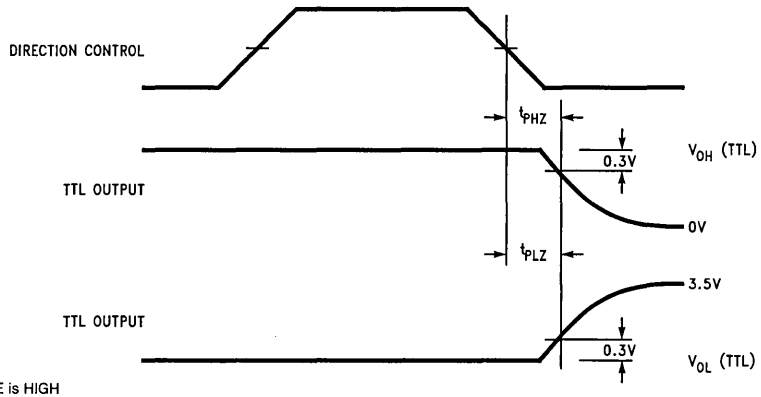
FIGURE 4. ECL-to-TTL Transition—Propagation Delay and Transition Times



Note: DIR is LOW, LE is HIGH

TL/F/10971–12

FIGURE 5. ECL-to-TTL Transition, OE to TTL Output, Enable and Disable Times

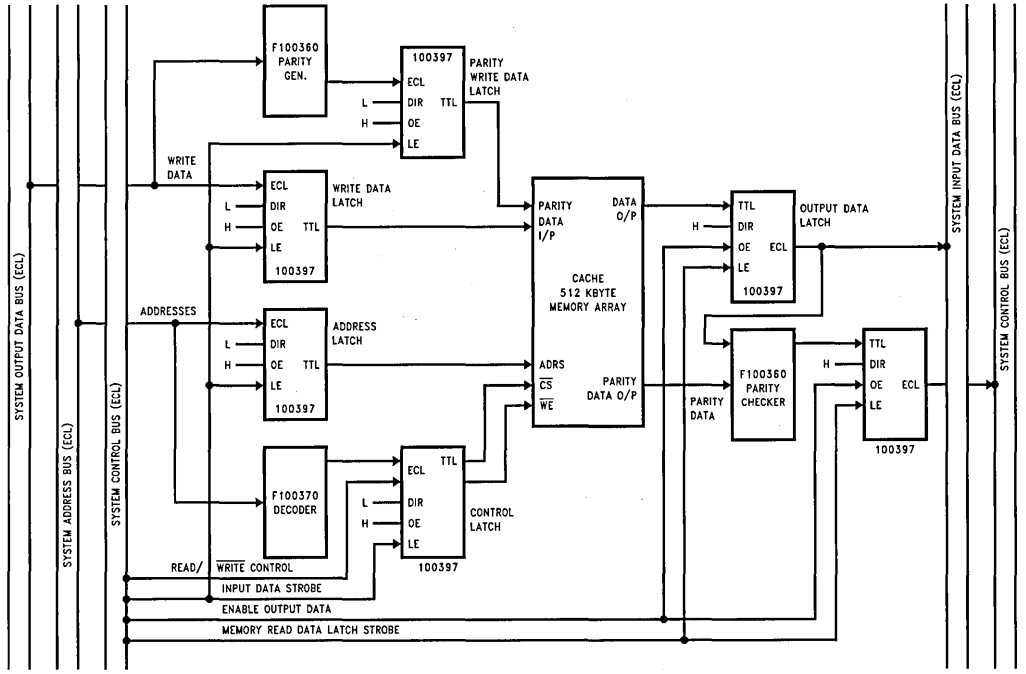


Note: OE is HIGH, LE is HIGH

TL/F/10971–13

FIGURE 6. ECL-to-TTL Transition, DIR to TTL Output, Disable Time

Applications



TL/F/10971–14

FIGURE 7. Applications Diagram—MOS/TTL SRAM Interface Using 100397 ECL-TTL Latched Translator

National Semiconductor

100398
Quad Differential ECL/TTL Translating Transceiver with Latch

General Description

The 100398 is a quad latched transceiver designed to convert TTL logic levels to differential F100K ECL logic levels and vice versa. This device was designed with the capability of driving a differential 25Ω ECL load with cutoff capability, and will sink a 64 mA TTL load. The 100398 is ideal for mixed technology applications utilizing either an ECL or TTL backplane.

The direction of translation is set by the direction control pin (DIR). The DIR pin on the 100398 accepts TTL logic levels. A TTL LOW on DIR sets up the ECL pins as inputs and TTL pins as outputs. A TTL HIGH on DIR sets up the TTL pins as inputs and ECL pins as outputs.

A LOW on the output enable input pin (OE) holds the ECL output in a cut-off state and the TTL outputs at a high impedance level. A HIGH on the latch enable input (LE) latches the data at both inputs even though only one output is enabled at the time. A LOW on LE makes the latch transparent.

The cut-off state is designed to be more negative than a normal ECL LOW level. This allows the output emitter-followers to turn off when the termination supply is −2.0V, presenting a high impedance to the data bus. This high impedance reduces termination power and prevents loss of low state noise margin when several loads share the bus.

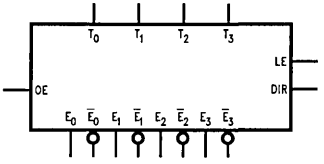
The 100398 is designed with FAST® TTL output buffers, featuring optimal DC drive and capable of quickly charging and discharging highly capacitive loads. All Inputs have 50 kΩ pull-down resistors.

Features

- Differential ECL input/output structure
- 64 mA FAST TTL outputs
- 25Ω differential ECL outputs with cut-off
- Bi-directional translation
- 2000V ESD protection
- Latched outputs
- TRI-STATE® outputs
- Voltage compensated operating range = −4.2V to −5.7V

Ordering Code: See Section 6

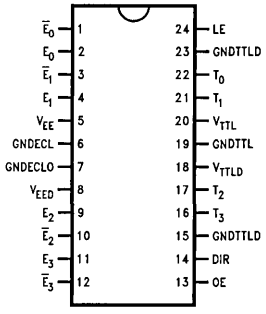
Logic Symbol



TL/F/10970–1

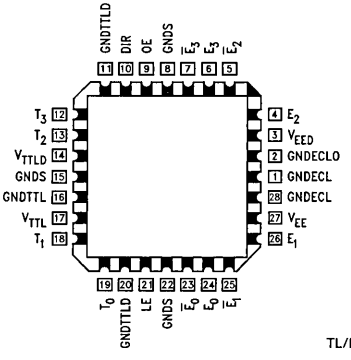
Connection Diagrams

24-Pin DIP



TL/F/10970–2

28-Pin PCC



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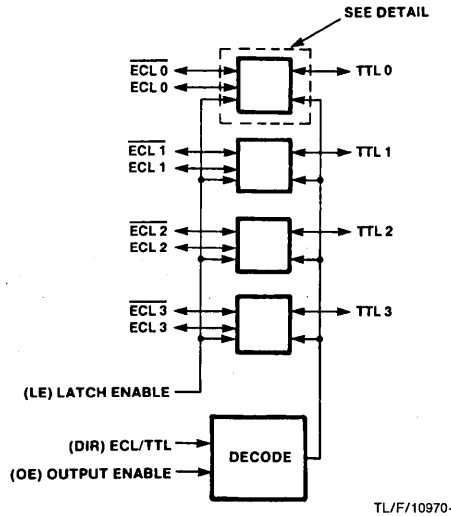
Functional Diagram



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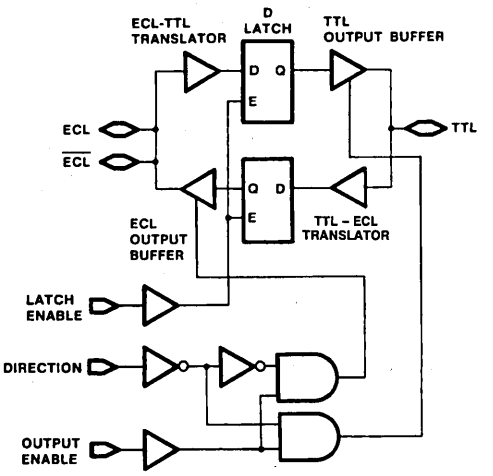
Note: LE, and OE use TTL logic levels

Detail



TL/F/10970–6

Pin Names	Description
E_0–E_3	ECL Data I/O
$\overline{E_0}$–$\overline{E_3}$	Complementary ECL Data I/O
T_0–T_3	TTL Data I/O
OE	Output Enable Input Levels
LE	Latch Enable Input Levels
DIR	Direction Control Input (TTL levels)
GNDECL	ECL Ground
GNDECLO	ECL Output Ground
GNDS	ECL Ground-to-Substrate
V_{EE}	ECL Quiescent Power Supply
V_{EED}	ECL Dynamic Power Supply
GNDTTL	TTL Quiescent Ground
GNDTTLD	TTL Dynamic Ground
V_{TTL}	TTL Quiescent Power Supply
V_{TTLD}	TTL Dynamic Power Supply

Truth Table

LE	DIR	OE	ECL Port	TTL Port	Notes
0	0	0	LOW (Cut-Off)	Z	
0	0	1	Input	Output	1, 4
0	1	0	LOW (Cut-Off)	Z	
0	1	1	Output	Input	2, 4
1	0	0	Input	Z	1, 3
1	0	1	Latched	X	1, 3
1	1	0	Low (Cut-Off)	Input	2, 3
1	1	1	Latched	X	2, 3

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High Impedance

Note 1: ECL input to TTL output mode.

Note 2: TTL input to ECL output mode.

Note 3: Retains data present before LE set HIGH.

Note 4: Latch is transparent.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature (T_{STG})	−65°C to +150°C
Maximum Junction Temperature (T_J)	
Ceramic	+175°C
Plastic	+150°C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
V_{TTL} Pin Potential to Ground Pin	−0.5V to +6.0V
ECL Input Voltage (DC)	V_{EE} to +0.5V
ECL Output Current (DC Output HIGH)	−50 mA
TTL Input Voltage (Note 4)	−0.5V to +7.0V
TTL Input Current (Note 4)	−30 mA to +5.0 mA
Voltage Applied to Output in HIGH State TRI-STATE Output	−0.5V to +5.5V
Current Applied to TTL Output in LOW State (Max)	Twice the Rated I_{OL} (mA)
ESD (Note 2)	≥2000V

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: ESD testing conforms to MIL-STD-883, Method 3015.

Recommended Operating Conditions

Case Temperature (T_C)	
Commercial	0°C to +85°C
Industrial	−40°C to +85°C
Military	−55°C to +125°C
ECL Supply Voltage (V_{EE})	−5.7V to −4.2V
TTL Supply Voltage (V_{TTL})	+4.5V to +5.5V

Commercial Version

TTL-to-ECL DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, GND = 0V, T_C = 0°C to +85°C, V_{TTL} = +4.5V to +5.5V (Note 4)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{OH}	Output HIGH Voltage	−1025	−955	−870	mV	V_{IN} = $V_{IH(Max)}$ or $V_{IL(Min)}$ Loading with 50Ω to −2V
V_{OL}	Output LOW Voltage	−1830	−1705	−1620	mV	
	Cutoff Voltage		−2000	−1950	mV	OE and LE Low, DIR High V_{IN} = $V_{IH(Max)}$ or $V_{IL(Min)}$, Loading with 50Ω to −2V
V_{OHC}	Output HIGH Voltage Corner Point High	−1035			mV	V_{IN} = $V_{IH(Min)}$ or $V_{IL(Max)}$ Loading with 50Ω to −2V
V_{OLC}	Output LOW Voltage Corner Point Low			−1610	mV	
V_{IH}	Input HIGH Voltage	2.0		5.0	V	Over V_{TTL}, V_{EE}, T_C Range
V_{IL}	Input LOW Voltage	0		0.8	V	Over V_{TTL}, V_{EE}, T_C Range
I_{IH}	Input HIGH Current			5.0	μA	V_{IN} = +2.7V
	Breakdown Test			0.5	mA	V_{IN} = +5.5V
I_{IL}	Input LOW Current	−700			μA	V_{IN} = +0.5V
V_{FCD}	Input Clamp Diode Voltage	−1.2			V	I_{IN} = −18 mA
I_{EE}	V_{EE} Supply Current	−99		−50	mA	LE Low, OE and DIR High Inputs Open
I_{EEZ}	V_{EE} Supply Current	−159		−90	mA	LE and OE Low, DIR High Inputs Open

Note 3: Either voltage limit or current limit is sufficient to protect inputs.

Note 4: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

Commercial Version (Continued)

ECL-to-TTL DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, GND = 0V, T_C = 0°C to +85°C, C_L = 50 pF, V_{TTL} = +4.5V to +5.5V (Note 4)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{OH}	Output HIGH Voltage	2.7 2.4	3.1 2.9		V V	I_{OH} = −3 mA, V_{TTL} = 4.75V I_{OH} = −3 mA, V_{TTL} = 4.50V
V_{OL}	Output LOW Voltage		0.3	0.5	V	I_{OL} = 24 mA, V_{TTL} = 4.50V
V_{IH}	Input HIGH Voltage	−1165		−870	mV	Guaranteed HIGH Signal for All Inputs
V_{IL}	Input LOW Voltage	−1830		−1475	mV	Guaranteed LOW Signal for All Inputs
V_{DIFF}	Input Voltage Differential	150			mV	Required for Full Output Swing
V_{CM}	Common Mode Voltage	GNDECL − 2.0		GNDECL − 0.5	V	
I_{IH}	Input HIGH Current			30	μA	V_{IN} = V_{IH} (Max)
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = V_{IL} (Min)
I_{OZHT}	TRI-STATE Current Output High			70	μA	V_{OUT} = +2.7V
I_{OZLT}	TRI-STATE Current Output Low	−650			μA	V_{OUT} = +0.5V
I_{OS}	Output Short-Circuit Current	−100		−225	mA	V_{OUT} = 0.0V, V_{TTL} = +5.5V
I_{CEX}	Output HIGH Leakage Current			50	μA	V_{OUT} = 5.5V
I_{ZZ}	Bus Drainage Test			500	μA	V_{OUT} = 5.25V
I_{TTL}	V_{TTL} Supply Current			39 27 39	mA mA mA	TTL Outputs LOW TTL Outputs HIGH TTL Outputs in TRI-STATE

Note 4: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DIP and PCC TTL-to-ECL AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{TTL} = +4.5V to +5.5V

Symbol	Parameter	T_C = 0°C		T_C = 25°C		T_C = 85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
F_{max}	Toggle Frequency	180		180		180		MHz	
t_{PLH} t_{PHL}	T_n to E_n, $\overline{E}_n$ (Transparent)	0.90	2.10	0.80	2.20	0.70	2.50	ns	*Figures 1, 3*
t_{PLH} t_{PHL}	LE to E_n, $\overline{E}_n$	1.40	2.70	1.50	2.70	1.80	3.10	ns	*Figures 1, 3*
t_{PZH}	OE to E_n, $\overline{E}_n$ (Cutoff to High)	2.90	8.00	2.80	6.90	2.80	5.80	ns	*Figures 1, 3*
t_{PHZ}	OE to E_n, $\overline{E}_n$ (High to Cutoff)	1.30	2.70	1.40	2.90	1.70	3.40	ns	*Figures 1, 3*
t_{PHZ}	DIR to E_n, $\overline{E}_n$ (High to Cutoff)	1.30	2.70	1.40	2.90	1.80	3.50	ns	*Figures 1, 3*
t_S	T_n to LE	0.70		0.70		0.70		ns	*Figures 1, 3*
t_H	T_n to LE	0.90		0.80		0.70		ns	*Figures 1, 3*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.50	0.45	1.50	0.45	1.50	ns	*Figures 1, 3*

Commercial Version (Continued)

DIP and PCC ECL-to-TTL AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{TTL} = +4.5V to +5.5V, C_L = 50 pF

Symbol	Parameter	T_C = 0°C		T_C = 25°C		T_C = 85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
F_{max}	Toggle Frequency	75		75		75		MHz	
t_{PLH} t_{PHL}	E_n, $\overline{E}_n$ to T_n (Transparent)	1.70	4.90	1.70	5.10	1.80	5.80	ns	*Figures 2, 4*
t_{PLH} t_{PHL}	LE to T_n	2.30 3.30	4.60 5.50	2.40 3.50	4.70 5.70	2.60 4.00	4.90 6.70	ns	*Figures 2, 4*
t_{PZH} t_{PZL}	OE to T_n (Enable Time)	2.30 4.10	4.90 7.90	2.10 4.10	4.70 7.80	2.00 4.20	4.30 7.80	ns	*Figures 2, 5*
t_{PHZ} t_{PLZ}	OE to T_n (Disable Time)	3.30 4.10	7.90 7.50	3.30 4.30	7.50 7.80	3.70 5.30	7.90 9.40	ns	*Figures 2, 5*
t_{PHZ} t_{PLZ}	DIR to T_n (Disable Time)	2.00 2.00	6.00 4.00	1.90 2.00	5.70 3.70	1.70 1.90	5.20 3.70	ns	*Figures 2, 6*
t_S	E_n, $\overline{E}_n$ to LE	0.50		0.50		0.50		ns	*Figures 2, 4*
t_H	E_n, $\overline{E}_n$ to LE	1.00		1.00		1.00		ns	*Figures 2, 4*

Industrial Version

TTL-to-ECL DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, GND = 0V, T_C = −40°C to +85°C, V_{TTL} = +4.5V to +5.5V (Note 1)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{OH}	Output HIGH Voltage	−1085	−955	−870	mV	V_{IN} = $V_{IH(Max)}$ or $V_{IL(Min)}$ Loading with 50Ω to −2V
V_{OL}	Output LOW Voltage	−1830	−1705	−1575	mV	
	Cutoff Voltage		−2000	−1900	mV	OE and LE Low, DIR High V_{IN}= $V_{IH(Max)}$ or $V_{IL(Min)}$, Loading with 50Ω to −2V
V_{OHC}	Output HIGH Voltage Corner Point High	−1095			mV	V_{IN} = $V_{IH(Min)}$ or $V_{IL(Max)}$ Loading with 50Ω to −2V
V_{OLC}	Output LOW Voltage Corner Point Low			−1565	mV	
V_{IH}	Input HIGH Voltage	2.0		5.0	V	Over V_{TTL}, V_{EE}, T_C Range
V_{IL}	Input LOW Voltage	0		0.8	V	Over V_{TTL}, V_{EE}, T_C Range
I_{IH}	Input HIGH Current			5.0	μA	V_{IN} = +2.7V
	Breakdown Test			0.5	mA	V_{IN} = +5.5V
I_{IL}	Input LOW Current	−700			μA	V_{IN} = +0.5V
V_{FCD}	Input Clamp Diode Voltage	−1.2			V	I_{IN} = −18 mA
I_{EE}	V_{EE} Supply Current	−99	−40		mA	LE Low, OE and DIR High Inputs Open

Note 1: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

Industrial Version (Continued)

ECL-to-TTL DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, GND = 0V, T_C = −40°C to +85°C, C_L = 50 pF, V_{TTL} = +4.5V to +5.5V (Note 1)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{OH}	Output HIGH Voltage	2.7 2.4	3.1 2.9		V V	I_{OH} = −3 mA, V_{TTL} = 4.75V I_{OH} = −3 mA, V_{TTL} = 4.50V
V_{OL}	Output LOW Voltage		0.3	0.5	V	I_{OL} = 24 mA, V_{TTL} = 4.50V
V_{IH}	Input HIGH Voltage	−1170		−870	mV	Guaranteed HIGH Signal for All Inputs
V_{IL}	Input LOW Voltage	−1830		−1480	mV	Guaranteed LOW Signal for All Inputs
V_{DIFF}	Input Voltage Differential	150			mV	Required for Full Output Swing
V_{CM}	Common Mode Voltage	GNDECL − 2.0		GNDECL − 0.5	V	
I_{IH}	Input HIGH Current			35	μA	V_{IN} = $V_{IH(Max)}$
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IH(Min)}$
I_{OZHT}	TRI-STATE Current Output High			70	μA	V_{OUT} = +2.7V
I_{OZLT}	TRI-STATE Current Output Low	−650			μA	V_{OUT} = +0.5V
I_{OS}	Output Short-Circuit Current	−100		−225	mA	V_{OUT} = 0.0V, V_{TTL} = +5.5V
I_{CEX}	Output HIGH Leakage Current			50	μA	V_{OUT} = 5.5V
I_{ZZ}	Bus Drainage Test			500	μA	V_{OUT} = 5.25V
I_{TTL}	V_{TTL} Supply Current			39 27 39	mA mA mA	TTL Outputs LOW TTL Outputs HIGH TTL Outputs in TRI-STATE

Note 1: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

PCC TTL-to-ECL AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{TTL} = +4.5V to +5.5V

Symbol	Parameter	T_C = −40°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
F_{max}	Toggle Frequency	180		180		180		MHz	
t_{PLH} t_{PHL}	T_n to E_n, $\overline{E}_n$ (Transparent)	0.90	2.40	0.80	2.20	0.70	2.50	ns	*Figures 1, 3*
t_{PLH} t_{PHL}	LE to E_n, $\overline{E}_n$	1.30	2.70	1.50	2.70	1.80	3.10	ns	*Figures 1, 3*
t_{PZH}	OE to E_n, $\overline{E}_n$ (Cutoff to High)	2.90	9.00	2.80	6.90	2.80	5.80	ns	*Figures 1, 3*
t_{PHZ}	OE to E_n, $\overline{E}_n$ (High to Cutoff)	1.10	2.70	1.40	2.90	1.70	3.40	ns	*Figures 1, 3*
t_{PHZ}	DIR to E_n, $\overline{E}_n$ (High to Cutoff)	1.10	2.70	1.40	2.90	1.80	3.50	ns	*Figures 1, 3*
t_S	T_n to LE	0.70		0.70		0.70		ns	*Figures 1, 3*
t_H	T_n to LE	0.90		0.90		0.90		ns	*Figures 1, 3*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	2.20	0.45	1.50	0.45	1.50	ns	*Figures 1, 3*

Industrial Version (Continued)

PCC ECL-to-TTL AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{TTL} = +4.5V to +5.5V, C_L = 50 pF

Symbol	Parameter	T_C = −40°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
F_{max}	Toggle Frequency	75		75		75		MHz	
t_{PLH} t_{PHL}	E_n, $\overline{E}_n$ to T_n (Transparent)	1.70	4.90	1.70	5.10	1.80	5.80	ns	*Figures 2, 4*
t_{PLH} t_{PHL}	LE to T_n	2.30 3.30	4.80 5.50	2.40 3.50	4.70 5.70	2.60 4.00	4.90 6.70	ns	*Figures 2, 4*
t_{PZH} t_{PZL}	OE to T_n (Enable Time)	2.30 4.10	5.50 8.20	2.10 4.10	4.70 7.80	2.00 4.20	4.30 7.80	ns	*Figures 2, 5*
t_{PHZ} t_{PLZ}	OE to T_n (Disable Time)	3.20 4.00	7.90 7.40	3.30 4.30	7.50 7.80	3.70 5.30	7.90 9.40	ns	*Figures 2, 5*
t_{PHZ} t_{PLZ}	DIR to T_n (Disable Time)	2.00 2.10	6.60 4.70	1.90 2.00	5.70 3.70	1.70 1.90	5.20 3.70	ns	*Figures 2, 6*
t_S	E_n, $\overline{E}_n$ to LE	0.50		0.50		0.50		ns	*Figures 2, 4*
t_H	E_n, $\overline{E}_n$ to LE	1.00		1.00		1.00		ns	*Figures 2, 4*

100398

Military Version—Preliminary

TTL-to-ECL DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, GND = 0V, T_C = −55°C to +125°C, V_{TTL} = +4.5V to +5.5V

Symbol	Parameter	Min	Max	Units	T_C	Conditions		Notes
V_{OH}	Output HIGH Voltage	−1025	−870	mV	0°C to +125°C	V_{IN} = V_{IH} (Max) or V_{IL} (Min)	Loading with 50Ω to −2.0V	1, 2, 3
		−1085	−870	mV	−55°C			
V_{OL}	Output LOW Voltage	−1830	−1620	mV	0°C to +125°C			
		−1830	−1555	mV	−55°C			
	Cutoff Voltage		−1950	mV	0°C to +125°C	OE or DIR Low		
			−1850	mV	−55°C			
V_{OHC}	Output HIGH Voltage	−1035		mV	0°C to +125°C	V_{IN} = V_{IH} (Min) or V_{IL} (Max)	Loading with 50Ω 0 to −2.0V	1, 2, 3
		−1085		mV	−55°C			
V_{OLC}	Output LOW Voltage		−1610	mV	0°C to +125°C			
			−1555	mV	−55°C			
V_{IH}	Input HIGH Voltage	2.0		V	−55°C to +125°C	Over V_{TTL}, V_{EE}, T_C Range		1, 2, 3, 4
V_{IL}	Input LOW Voltage		0.8	V	−55°C to +125°C	Over V_{TTL}, V_{EE}, T_C Range		1, 2, 3, 4
I_{IH}	Input HIGH Current		70	μA	−55°C to 125°C	V_{IN} = +2.7V		1, 2, 3
	Breakdown Test		1.0	mA	−55°C to +125°C	V_{IN} = +5.5V		
I_{IL}	Input LOW Current	−1.0		mA	−55°C to +125°C	V_{IN} = +0.5V		1, 2, 3
V_{FCD}	Input Clamp Diode Voltage	−1.2		V	−55°C to +125° C	I_{IN} = −18 mA		1, 2, 3
I_{EE}	V_{EE} Supply Current	−165 −175	−65 −65	mA	−55°C to +125°C	LE Low, OE and DIR High Inputs Open V_{EE} = −4.2V to −4.8V V_{EE} = −4.2V to −5.7V		1, 2, 3

Military Version—Preliminary (Continued)

ECL-to-TTL DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, GND = 0V, T_C = −55°C to +125°C, C_L = 50 pF, V_{TTL} = +4.5V to + 5.5V

Symbol	Parameter	Min	Max	Units	T_C	Conditions	Notes
V_{OH}	Output HIGH Voltage	2.5 2.4		mV	0°C to +125°C −55°C	I_{OH} = −1 mA, V_{TTL} = 4.50V I_{OH} = −3 mA, V_{TTL} = 4.50V	1, 2, 3
V_{OL}	Output LOW Voltage		0.5	mV	−55°C to +125°C	I_{OL} = 24 mA, V_{TTL} = 4.50V	
V_{IH}	Input HIGH Voltage	−1165	−870	mV	−55°C to +125°C	Guaranteed HIGH Signal for All Inputs	1, 2, 3, 4
V_{IL}	Input LOW Voltage	−1830	−1475	mV	−55°C to +125°C	Guaranteed LOW Signal for All Inputs	1, 2, 3, 4
I_{IH}	Input HIGH Current		350 500	μA	0°C to +125°C	V_{EE} = −5.7V V_{IN} = $V_{IH(Max)}$	1, 2, 3
I_{IL}	Input LOW Current	0.50		μA	−55°C to +125°C	V_{EE} = −4.2V V_{IN} = $V_{IL(Min)}$	1, 2, 3
I_{OZHT}	TRI-STATE Current Output High		70	μA	−55°C to +125°C	V_{OUT} = +2.7V	1, 2, 3
I_{OZLT}	TRI-STATE Current Output Low	−1.0		mA	−55°C to +125°C	V_{OUT} = +0.5V	1, 2, 3
I_{OS}	Output Short-Circuit Current	−150	−60	mA	−55°C to +125°C	V_{OUT} = 0.0V, V_{TTL} = +5.5V	1, 2, 3
I_{TTL}	V_{TTL} Supply Current		75 50 70	mA mA mA	−55°C to +125°C	TTL Outputs Low TTL Output High TTL Output in TRI-STATE	1, 2, 3

Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals −55°C), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 2: Screen tested 100% on each device at −55°C, +25°C, and +125°C, Subgroups, 1, 2, 3, 7, and 8.

Note 3: Sample tested (Method 5005, Table I) on each manufactured lot at −55°C, +25°C, and +125°C, Subgroups A1, 2, 3, 7, and 8.

Note 4: Guaranteed by applying specified input condition and testing V_{OH}/V_{OL}.

TTL-to-ECL AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{TTL} = +4.5V to +5.5V, GND = 0V

Symbol	Parameter	T_C = −55°C		T_C = +25°C		T_C = +125°C		Units	Conditions	Notes
		Min	Max	Min	Max	Min	Max			
t_{PLH} t_{PHL}	T_n to E_n, $\overline{E}_n$ (Transparent)	1.0	3.9	1.1	3.6	1.1	4.0	ns	*Figures 1, 2*	1, 2, 3
t_{PLH} t_{PHL}	LE to E_n, $\overline{E}_n$	1.2	3.8	1.4	3.7	1.6	4.2	ns	*Figures 1, 2*	
t_{PZH}	OE to E_n, $\overline{E}_n$ (Cutoff to HIGH)	1.0	4.3	1.5	4.4	1.7	5.2	ns	*Figures 1, 2*	1, 2, 3
t_{PHZ}	OE to E_n, $\overline{E}_n$ (HIGH to Cutoff)	1.5	5.1	1.6	4.5	1.6	5.1	ns	*Figures 1, 2*	
t_{PHZ}	DIR to E_n, $\overline{E}_n$ (HIGH to Cutoff)	1.6	4.7	1.6	4.3	1.7	4.9	ns	*Figures 1, 2*	
t_S	T_n to LE	2.5		2.0		2.5		ns	*Figures 1, 2*	4
t_H	T_n to LE	2.5		2.0		2.5		ns	*Figures 1, 2*	
$t_{PW(H)}$	Pulse Width LE	2.5		2.0		2.5		ns	*Figures 1, 2*	4
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.4	2.3	0.5	2.1	0.4	2.4	ns	*Figures 1, 2*	4

Military Version—Preliminary (Continued)

ECL-to-TTL AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{TTL} = +4.5V to +5.5V, GND = 0V, C_L = 50 pF

Symbol	Parameter	T_C = −55°C		T_C = +25°C		T_C = +125°C		Units	Conditions	Notes
		Min	Max	Min	Max	Min	Max			
t_{PLH} t_{PHL}	E_n, $\overline{E}_n$ to T_n (Transparent)	2.3	6.4	2.4	5.6	2.6	6.3	ns	*Figures 3, 4*	1, 2, 3
t_{PLH} t_{PHL}	LE to T_n	3.1	8.0	3.1	7.3	3.3	8.0	ns	*Figures 3, 4*	
t_{PZH} t_{PZL}	OE to T_n (Enable Time)	3.2 3.6	8.9 9.4	3.7 4.0	9.0 9.3	4.0 4.3	10.2 10.4	ns	*Figures 3, 5*	1, 2, 3
t_{PHZ} t_{PLZ}	OE to T_n (Disable Time)	3.2 3.0	9.9 9.7	3.3 3.4	9.0 8.8	3.5 4.1	9.4 10.6	ns	*Figures 3, 5*	
t_{PHZ} t_{PLZ}	DIR to T_n (Disable Time)	2.6 2.7	9.4 8.5	2.8 3.1	8.8 8.0	2.9 4.0	9.1 9.7	ns	*Figures 3, 6*	
t_S	E_n, $\overline{E}_n$ to LE	2.5		2.0		2.5		ns	*Figures 3, 4*	4
t_H	E_n, $\overline{E}_n$ to LE	3.0		2.5		3.0		ns	*Figures 3, 4*	
t_{PW}(H)	Pulse Width LE	2.5		2.0		5.0		ns	*Figures 3, 4*	4

Test Circuitry

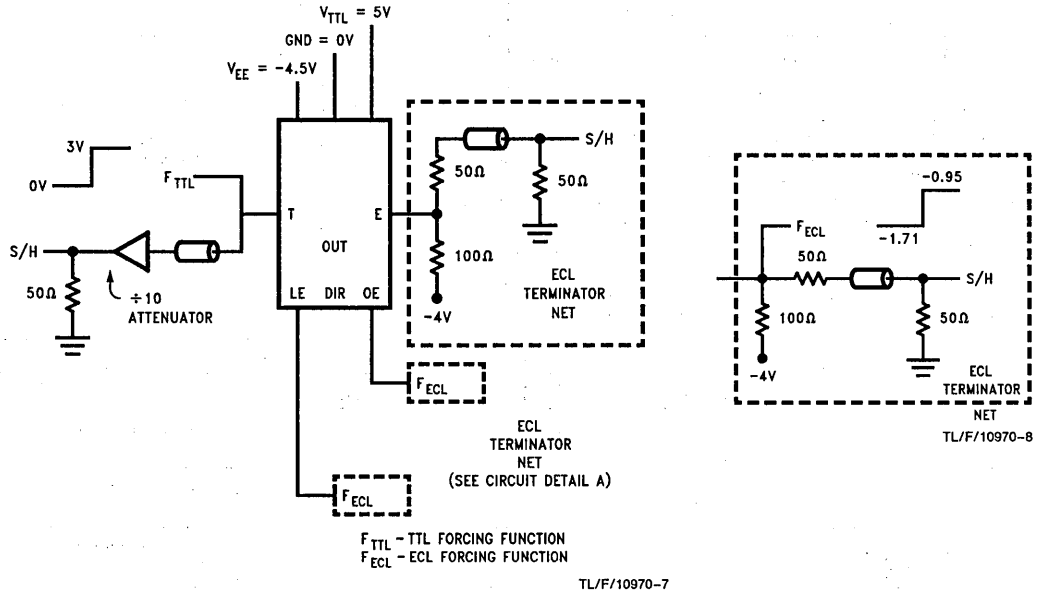
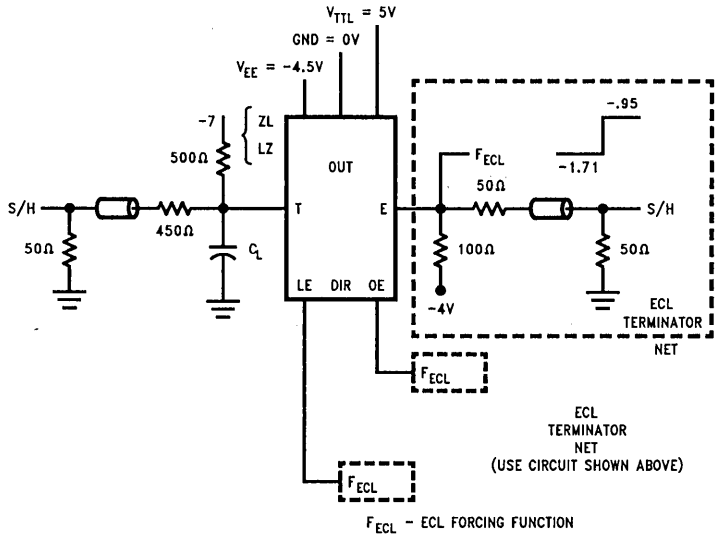


FIGURE 1. TTL-to-ECL AC Test Circuit

Test Circuitry (Continued)



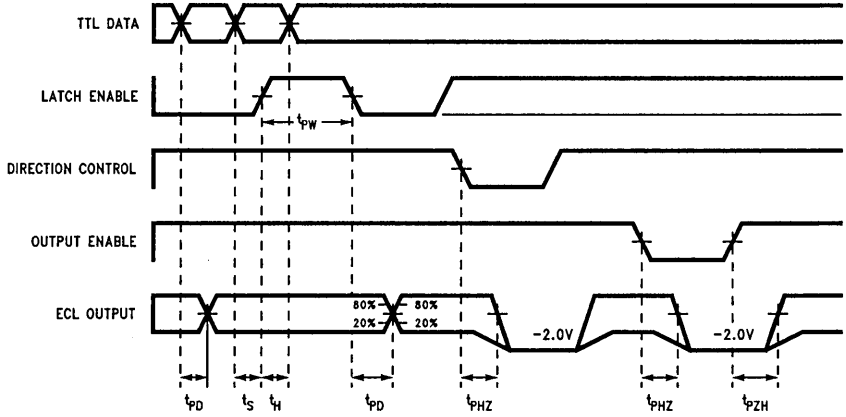
TL/F/10970–10

C_L = 50 pF including stray and jig capacitance.

Note: 50Ω to ground termination **must be included** on ECL I/O pins **not** monitored by a 50Ω scope to prevent oscillatory feedback.

FIGURE 2. ECL-to-TTL AC Test Circuit

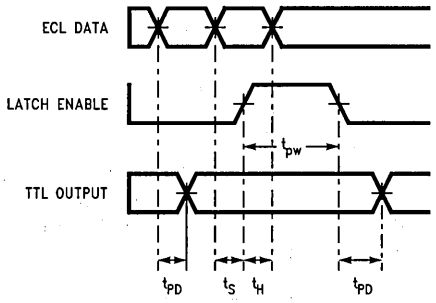
Switching Waveforms



TL/F/10970–9

FIGURE 3. TTL-to-ECL Transition—Propagation Delay and Transition Times

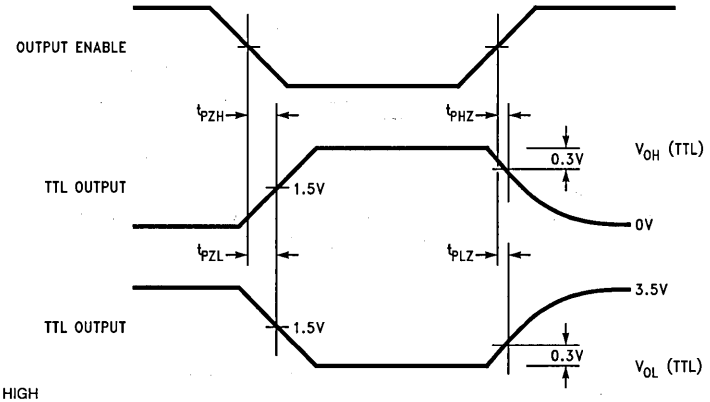
Switching Waveforms (Continued)



TL/F/10970–11

Note: DIR is LOW, and OE is HIGH

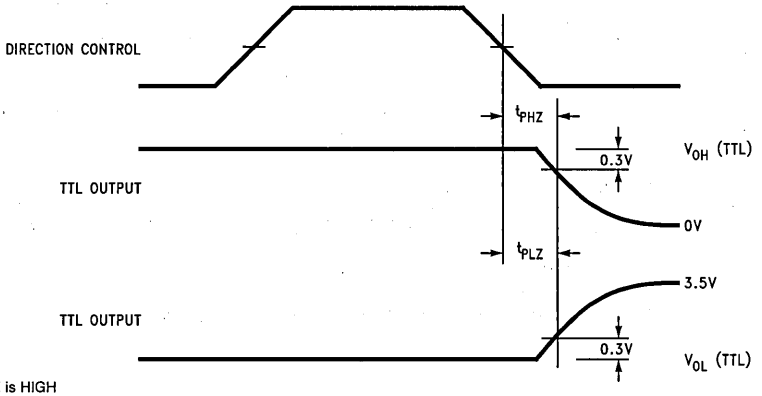
FIGURE 4. ECL-to-TTL Transition—Propagation Delay and Transition Times



Note: DIR is LOW, LE is HIGH

TL/F/10970–12

FIGURE 5. ECL-to-TTL Transition, OE to TTL Output, Enable and Disable Times

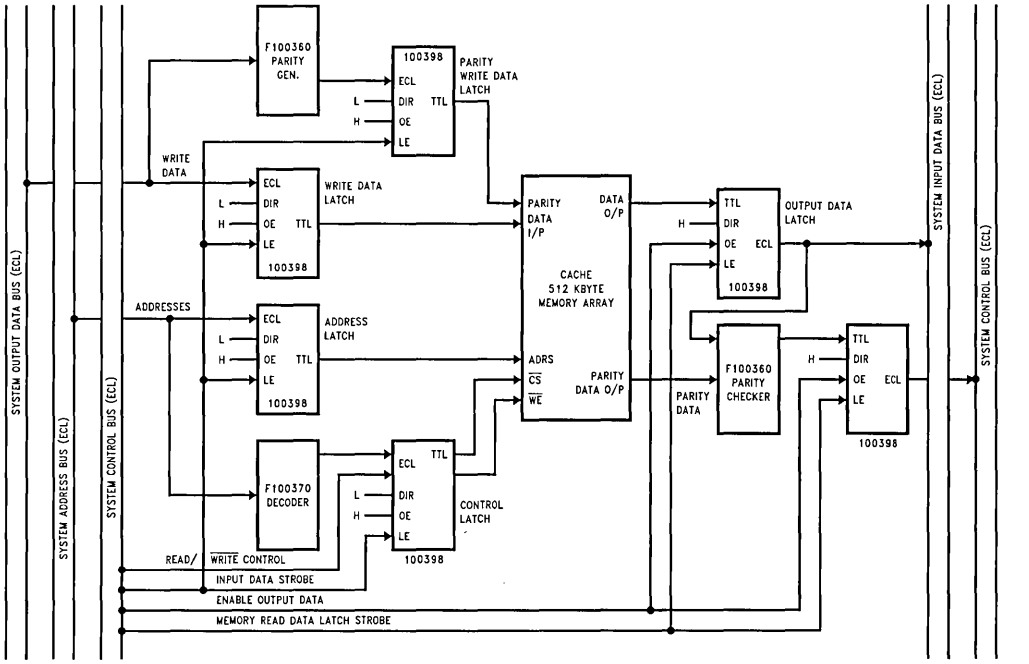


Note: OE is HIGH, LE is HIGH

TL/F/10970–13

FIGURE 6. ECL-to-TTL Transition, DIR to TTL Output, Disable Time

Applications



TL/F/10970–14

FIGURE 7. Applications Diagram—MOS/TTL SRAM Interface Using 100398 ECL–TTL Latched Translator

Section 3

F100K 100 Series Datasheets

Section 3 Contents

National Semiconductor

Not Intended For New Designs

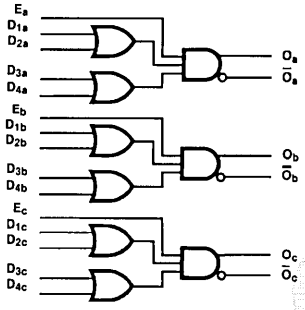
100117
Triple 2-Wide OA/OAI Gate

General Description

The 100117 is a monolithic triple 2-wide OR/AND gate with true and complement outputs. All inputs have 50 kΩ pull-down resistors and all outputs are buffered.

Ordering Code: See Section 6

Logic Symbol

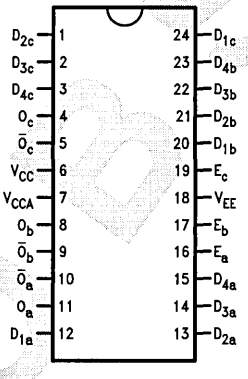


TL/F/9843–3

Pin Names	Description
D_{na}–D_{nc}	Data Inputs
E_a–E_c	Enable Inputs
O_a–O_c	Data Outputs
$\overline{O}_a$–$\overline{O}_c$	Complementary Data Outputs

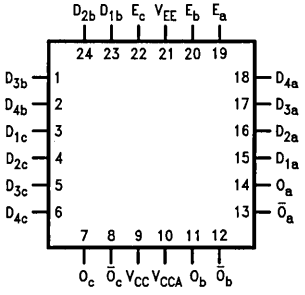
Connection Diagrams

24-Pin DIP



TL/F/9843–1

24-Pin Quad Cerpak



TL/F/9843–2

Absolute Maximum Ratings

Above which the useful life may be impaired. (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Maximum Junction Temperature (T_J)	+150°C
Case Temperature under Bias (T_C)	0°C to +85°C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Output Current (DC Output HIGH)	−50 mA
Operating Range (Note 2)	−5.7V to −4.2V

DC Electrical Characteristics

V_{EE} = −4.5V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1025	−955	−880	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1810	−1705	−1620			
V_{OHC}	Output HIGH Voltage	−1035			mV	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610			
V_{IH}	Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

DC Electrical Characteristics

V_{EE} = −4.2V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1020		−870	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1810		−1605			
V_{OHC}	Output HIGH Voltage	−1030			mV	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1595			
V_{IH}	Input HIGH Voltage	−1150		−870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

DC Electrical Characteristics

V_{EE} = −4.8V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1035		−880	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830		−1620			
V_{OHC}	Output HIGH Voltage	−1045			mV	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610			
V_{IH}	Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1830		−1490	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Parametric values specified at −4.2V to −4.8V.

Note 3: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 4: Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DC Electrical Characteristics

V_{EE} = −4.2V to −4.8V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C

Symbol	Parameter	Min	Typ	Max	Units	Conditions
I_{IH}	Input HIGH Current All Inputs			260	μA	V_{IN} = $V_{IH\ (Max)}$
I_{EE}	Power Supply Current	−79	−54	−37	mA	Inputs Open

DIP AC Electrical Characteristics

V_{EE} = −4.2V to −4.8V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Data to Output	0.90	2.60	0.90	2.50	0.90	2.60	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay Enable to Output	0.45	1.40	0.45	1.30	0.45	1.40	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.30	0.45	1.20	0.45	1.30	ns	

Cerpak AC Electrical Characteristics

V_{EE} = −4.2V to −4.8V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Data to Output	0.90	2.40	0.90	2.30	0.90	2.40	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay Enable to Output	0.45	1.20	0.45	1.10	0.45	1.20	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.20	0.45	1.10	0.45	1.20	ns	

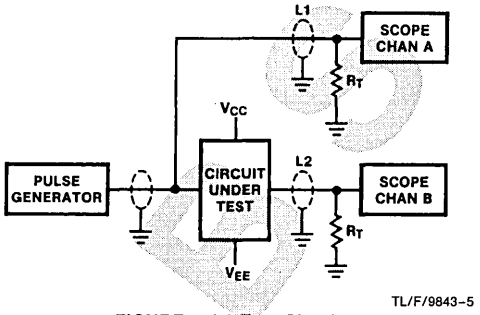


FIGURE 1. AC Test Circuit

Notes:
V_{CC}, V_{CCA} = +2V, V_{EE} = −2.5V
L1 and L2 = equal length 50Ω impedance lines
R_T = 50Ω terminator internal to scope
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
All unused outputs are loaded with 50Ω to GND
C_L = Fixture and stray capacitance ≤ 3 pF

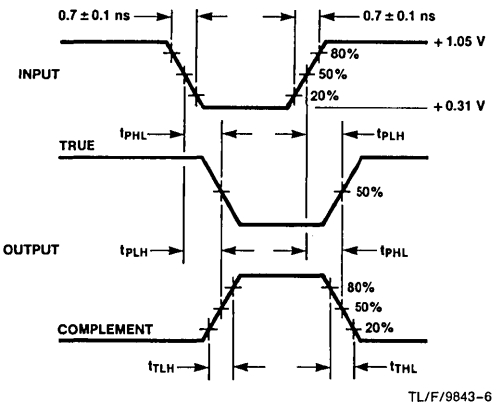


FIGURE 2. Propagation Delay and Transition Times

National Semiconductor

Not Intended For New Designs

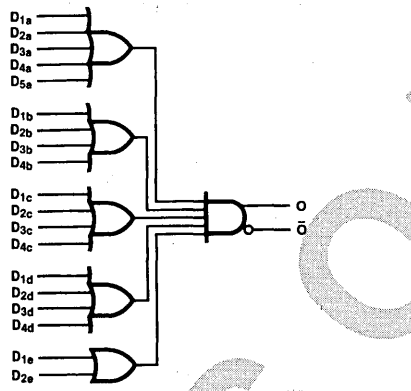
100118
5-Wide 5, 4, 4, 4, 2 OA/OAI Gate

General Description

The 100118 is a monolithic 5-wide 5, 4, 4, 4, 2 OR/AND gate with true complementary outputs. All inputs have 50 kΩ pull-down resistors and all outputs are buffered.

Ordering Code: See Section 6

Logic Symbol

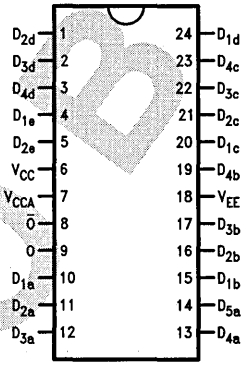


TL/F/9844–3

Pin Names	Description
D_{na}–D_{ne}	Data Inputs
O, $\overline{O}$	Data Outputs

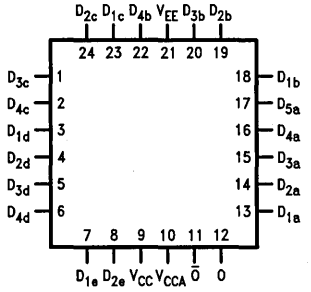
Connection Diagrams

24-Pin DIP



TL/F/9844–1

24-Pin Quad Cerpak



TL/F/9844–2

Absolute Maximum Ratings

Above which the useful life may be impaired. (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Maximum Junction Temperature (T_J)	+150°C
Case Temperature under Bias (T_C)	0°C to +85°C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Output Current (DC Output HIGH)	−50 mA
Operating Range (Note 2)	−5.7V to −4.2V

DC Electrical Characteristics

V_{EE} = −4.5V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1025	−955	−880	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1810	−1705	−1620			
V_{OHC}	Output HIGH Voltage	−1035			mV	V_{IN} = $V_{IH(Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610			
V_{IH}	Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

DC Electrical Characteristics

V_{EE} = −4.2V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1020		−870	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1810		−1605			
V_{OHC}	Output HIGH Voltage	−1030			mV	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1595			
V_{IH}	Input HIGH Voltage	−1150		−870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

DC Electrical Characteristics

V_{EE} = −4.8V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1035		−880	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830		−1620			
V_{OHC}	Output HIGH Voltage	−1045			mV	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610			
V_{IH}	Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1830		−1490	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Parametric values specified at −4.2V to −4.8V.

Note 3: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 4: Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DC Electrical Characteristics

V_{EE} = −4.2V to −4.8V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C

Symbol	Parameter	Min	Typ	Max	Units	Conditions
I_{IH}	Input HIGH Current All Inputs			350	μA	V_{IN} = $V_{IH\ (Max)}$
I_{EE}	Power Supply Current	−92	−69	−42	mA	Inputs Open

DIP AC Electrical Characteristics

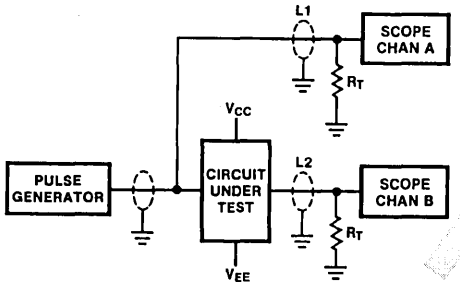
V_{EE} = −4.2V to −4.8V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Data to Output	0.85	2.50	0.95	2.50	0.95	2.70	ns	*Figures 1* and *2*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.60	0.45	1.50	0.45	1.60	ns	

Cerpak AC Electrical Characteristics

V_{EE} = −4.2V to −4.8V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Data to Output	0.85	2.30	0.95	2.30	0.95	2.50	ns	*Figures 1* and *2*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.50	0.45	1.40	0.45	1.50	ns	



TL/F/9844–5

FIGURE 1. AC Test Circuit

Notes:

V_{CC}, V_{CCA} = +2V, V_{EE} = −2.5V

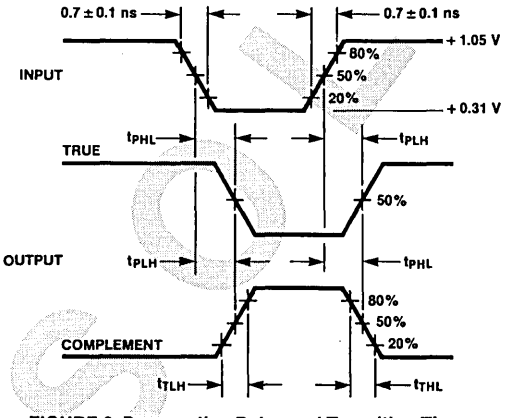
L1 and L2 = equal length 50Ω impedance lines

R_T = 50Ω terminator internal to scope

Decoupling 0.1 μF from GND to V_{CC} and V_{EE}

All unused outputs are loaded with 50Ω to GND

C_L = Fixture and stray capacitance ≤ 3 pF



TL/F/9844–6

FIGURE 2. Propagation Delay and Transition Times

National Semiconductor

Not Intended For New Designs

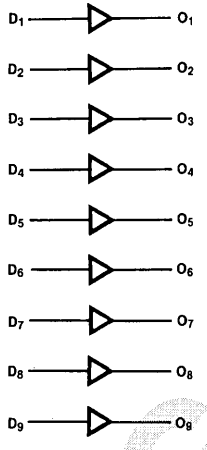
100126
9-Bit Backplane Driver

General Description

The 100126 contains nine independent, high-speed, buffer gates each with a single input and a single output. The gates are non-inverting. These buffers are useful in bus-oriented systems where minimal output loading or bus isolation is desired. The output transition times are longer to minimize noise when used as a backplane driver. All inputs have 50 kΩ pull-down resistors.

Ordering Code: See Section 6

Logic Symbol

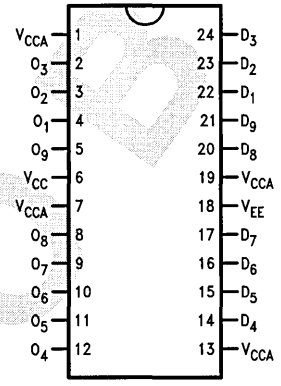


TL/F/9850–3

Pin Names	Description
D_1–D_9	Data Inputs
O_1–O_9	Data Outputs

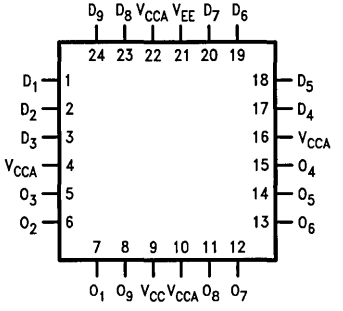
Connection Diagrams

24-Pin DIP



TL/F/9850–1

24-Pin Quad Cerpak



TL/F/9850–2

Absolute Maximum Ratings

Above which the useful life may be impaired. (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Maximum Junction Temperature (T_J)	+150°C
Case Temperature under Bias (T_C)	0°C to +85°C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Output Current (DC Output HIGH)	−50 mA
Operating Range (Note 2)	−5.7V to −4.2V

DC Electrical Characteristics

V_{EE} = −4.5V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1025	−955	−880	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1810	−1705	−1620			
V_{OHC}	Output HIGH Voltage	−1035			mV	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610			
V_{IH}	Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

DC Electrical Characteristics

V_{EE} = −4.2V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1020		−870	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1810		−1605			
V_{OHC}	Output HIGH Voltage	−1030			mV	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1595			
V_{IH}	Input HIGH Voltage	−1150		−870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

DC Electrical Characteristics

V_{EE} = −4.8V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1035		−880	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830		−1620			
V_{OHC}	Output HIGH Voltage	−1045			mV	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610			
V_{IH}	Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1830		−1490	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Parametric values specified at −4.2V to −4.8V.

Note 3: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 4: Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DC Electrical Characteristics

V_{EE} = −4.2V to −4.8V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C

Symbol	Parameter	Min	Typ	Max	Units	Conditions
I_{IH}	Input HIGH Current			350	μA	V_{IN} = $V_{IH\ (Max)}$
I_{EE}	Power Supply Current	−96	−70	−46	mA	Inputs Open

DIP AC Electrical Characteristics

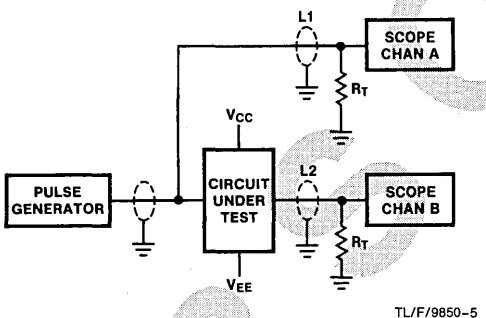
V_{EE} = −4.2V to −4.8V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Data to Output	1.05	2.75	1.05	2.75	1.05	2.75	ns	*Figures 1* and *2*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	1.15	3.40	1.15	3.40	1.05	3.40	ns	

Cerpak AC Electrical Characteristics

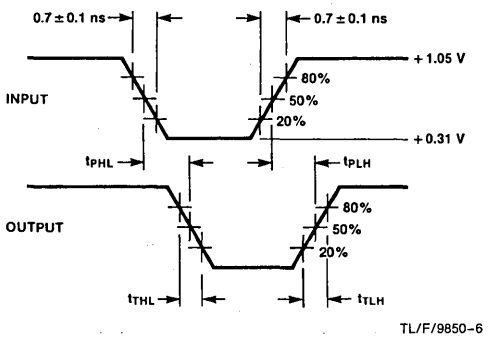
V_{EE} = −4.2V to −4.8V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Data to Output	1.05	2.55	1.05	2.55	1.05	2.55	ns	*Figures 1* and *2*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	1.15	3.30	1.15	3.30	1.05	3.30	ns	



TL/F/9850–5

FIGURE 1. AC Test Circuit



TL/F/9850–6

FIGURE 2. Propagation Delay and Transition Times

Notes:

V_{CC}, V_{CCA} = +2V, V_{EE} = −2.5V

L1 and L2 = equal length 50Ω impedance lines

R_T = 50Ω terminator internal to scope

Decoupling 0.1 μF from GND to V_{CC} and V_{EE}

All unused outputs are loaded with 50Ω to GND

C_L = Fixture and stray capacitance ≤ 3 pF

National Semiconductor

Not Intended For New Designs

100130
Triple D Latch

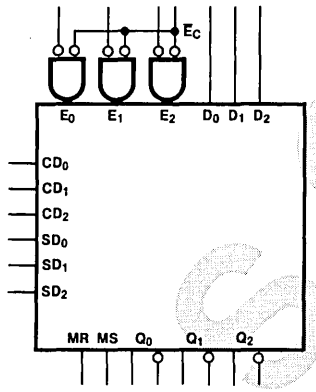
General Description

The 100130 contains three D-type latches with true and complement outputs and with Common Enable ($\overline{E}_C$), Master Set (MS) and Master Reset (MR) inputs. Each latch has its own Enable ($\overline{E}_n$), Direct Set (SD_n) and Direct Clear (CD_n) inputs. The Q output follows its Data (D) input when both $\overline{E}_n$ and $\overline{E}_C$ are LOW (transparent mode). When either $\overline{E}_n$ or $\overline{E}_C$ (or both) are HIGH, a latch stores the last valid data present on its D_n input before $\overline{E}_n$ or $\overline{E}_C$ goes HIGH.

Both Master Reset (MR) and Master Set (MS) inputs override the Enable inputs. The individual CD_n and SD_n also override the Enable inputs. All inputs have 50 kΩ pull-down resistors.

Ordering Code: See Section 6

Logic Symbol

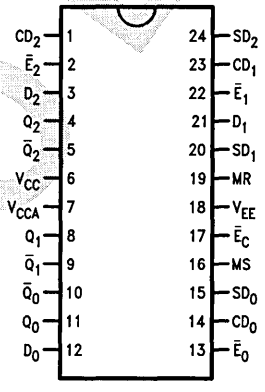


TL/F/9852–3

Pin Names	Description
CD_0–CD_2	Individual Direct Clear Inputs
SD_0–SD_2	Individual Direct Set Inputs
$\overline{E}_0$–$\overline{E}_2$	Individual Enable Inputs (Active LOW)
$\overline{E}_C$	Common Enable Input (Active LOW)
D_0–D_2	Data Inputs
MR	Master Reset Input
MS	Master Set Input
Q_0–Q_2	Data Outputs
$\overline{Q}_0$–$\overline{Q}_2$	Complementary Data Outputs

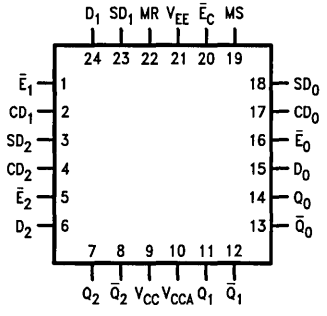
Connection Diagrams

24-Pin DIP



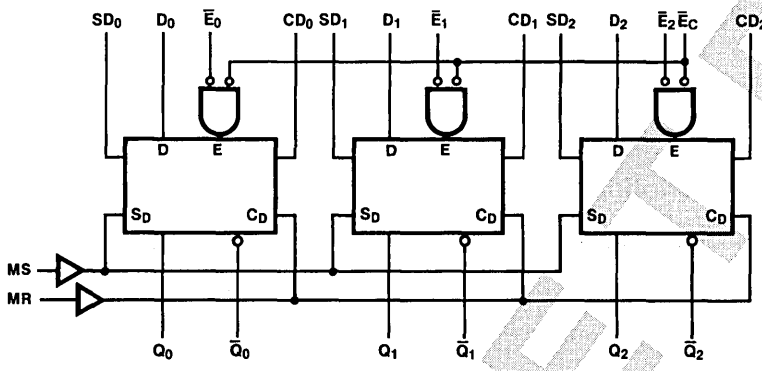
TL/F/9852–1

24-Pin Quad Cerpak



TL/F/9852–2

Logic Diagram



TL/F/9852–5

Truth Tables (Each Latch)

Latch Operation

Inputs					Outputs
D_n	$\overline{E}_n$	$\overline{E}_C$	MS SD_n	MR CD_n	Q_n
L	L	L	L	L	L
H	L	L	L	L	H
X	H	X	L	L	Latched*
X	X	H	L	L	Latched*

*Retains data presented before $\overline{E}$ positive transition

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
U = Undefined

Asynchronous Operation

Inputs					Outputs
D_n	$\overline{E}_n$	$\overline{E}_C$	MS SD_n	MR CD_n	Q_n
X	X	X	H	L	H
X	X	X	L	H	L
X	X	X	H	H	U

Absolute Maximum Ratings

Above which the useful life may be impaired. (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Maximum Junction Temperature (T_J)	+150°C
Case Temperature under Bias (T_C)	0°C to +85°C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Output Current (DC Output HIGH)	−50 mA
Operating Range (Note 2)	−5.7V to −4.2V

DC Electrical Characteristics

V_{EE} = −4.5V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1025	−955	−880	mV	V_{IN} = V_{IH} (Max) or V_{IL} (Min)	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1810	−1705	−1620			
V_{OHC}	Output HIGH Voltage	−1035			mV	V_{IN} = V_{IH} (Min) or V_{IL} (Max)	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610			
V_{IH}	Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = V_{IL} (Min)	

DC Electrical Characteristics

V_{EE} = −4.2V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1020		−870	mV	V_{IN} = V_{IH} (Max) or V_{IL} (Min)	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1810		−1605			
V_{OHC}	Output HIGH Voltage	−1030			mV	V_{IN} = V_{IH} (Min) or V_{IL} (Max)	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1595			
V_{IH}	Input HIGH Voltage	−1150		−870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = V_{IL} (Min)	

DC Electrical Characteristics

V_{EE} = −4.8V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1035		−880	mV	V_{IN} = V_{IH} (Max) or V_{IL} (Min)	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830		−1620			
V_{OHC}	Output HIGH Voltage	−1045			mV	V_{IN} = V_{IH} (Min) or V_{IL} (Max)	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610			
V_{IH}	Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1830		−1490	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = V_{IL} (Min)	

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Parametric values specified at −4.2V to −4.8V.

Note 3: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 4: Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DC Electrical Characteristics

V_{EE} = −4.2V to −4.8V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C

Symbol	Parameter	Min	Typ	Max	Units	Conditions
I_{IH}	Input HIGH Current					
	D_n			350		
	CD_n, SD_n			530	μA	V_{IN} = $V_{IH\ (Max)}$
	$\overline{E}_n$			240		
	$\overline{E}_C$, MR, MS			450		
I_{EE}	Power Supply Current	−149	−106	−74	mA	Inputs Open

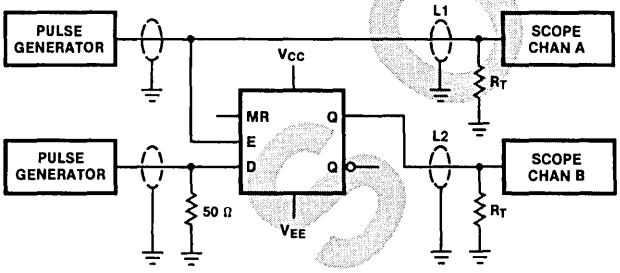
Ceramic Dual-In-Line Package AC Electrical Characteristics

V_{EE} = −4.2V to −4.8V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay D_n to Output (Transparent Mode)	0.50	1.80	0.50	1.70	0.50	1.90	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}_C$ to Output	0.65	2.10	0.75	2.00	0.75	2.10	ns	
t_{PLH} t_{PHL}	Propagation Delay CD_n, SD_n, $\overline{E}_n$ to Output	0.50	2.00	0.60	1.75	0.60	2.00	ns	*Figures 1, 2* and *3*
t_{PLH} t_{PHL}	Propagation Delay MS, MR to Output	1.10	2.50	1.10	2.40	1.10	2.60	ns	*Figures 1* and *2*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.60	0.45	1.60	0.45	1.60	ns	*Figures 1* and *2*
t_s	Setup Time								
	D_0–D_2	0.90		0.70		0.90			
	CD_n, SD_n (Release Time)	1.20		1.10		1.40		ns	*Figures 3* and *4*
	MR, MS (Release Time)	1.90		1.90		2.00			
t_h	Hold Time D_0–D_2	0.60		0.60		0.80		ns	*Figure 4*
$t_{pw}(L)$	Pulse Width LOW $\overline{E}_n$, $\overline{E}_C$	2.00		2.00		2.00		ns	*Figure 2*
$t_{pw}(H)$	Pulse Width HIGH CD_n, SD_n, MR, MS	2.00		2.00		2.00		ns	*Figure 3*

Cerpak AC Electrical Characteristics V_{EE} = −4.2V to −4.8V, V_{CC} = V_{CCA} = GND

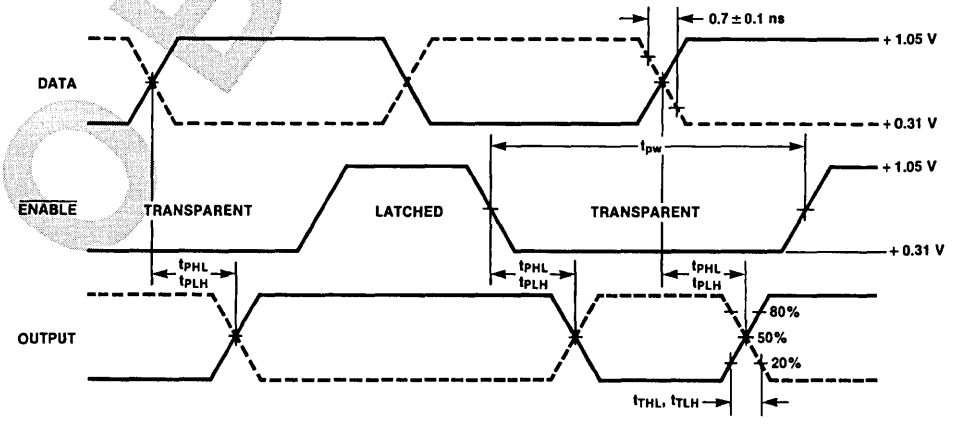
Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay D_n to Output (Transparent Mode)	0.50	1.60	0.50	1.50	0.50	1.70	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}_C$ to Output	0.65	1.90	0.75	1.80	0.75	1.90	ns	
t_{PLH} t_{PHL}	Propagation Delay CD_n, SD_n, $\overline{E}_n$ to Output	0.50	1.80	0.60	1.55	0.60	1.80	ns	*Figures 1, 2* and *3*
t_{PLH} t_{PHL}	Propagation Delay MS, MR to Output	1.10	2.30	1.10	2.20	1.10	2.40	ns	*Figures 1* and *3*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.50	0.45	1.50	0.45	1.50	ns	*Figures 1* and *2*
t_s	Setup Time D_0–D_2 CD_n, SD_n (Release Time) MR, MS (Release Time)	 0.80 1.10 1.80		 0.60 1.00 1.80		 0.80 1.30 2.00		ns	*Figures 3* and *4*
t_h	Hold Time D_0–D_2	0.50		0.50		0.70		ns	*Figure 4*
$t_{pw}(L)$	Pulse Width LOW $\overline{E}_n$, $\overline{E}_C$	2.00		2.00		2.00		ns	*Figure 2*
$t_{pw}(H)$	Pulse Width HIGH CD_n, SD_n, MR, MS	2.00		2.00		2.00		ns	*Figure 3*



Notes:
V_{CC}, V_{CCA} = +2V, V_{EE} = −2.5V
L1 and L2 = equal length 50Ω impedance lines
R_T = 50Ω terminator internal to scope
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
All unused outputs are loaded with 50Ω to GND
C_L = Fixture and stray capacitance ≤ 3 pF

TL/F/9852–6

FIGURE 1. AC Test Circuit



TL/F/9852–7

FIGURE 2. Enable Timing

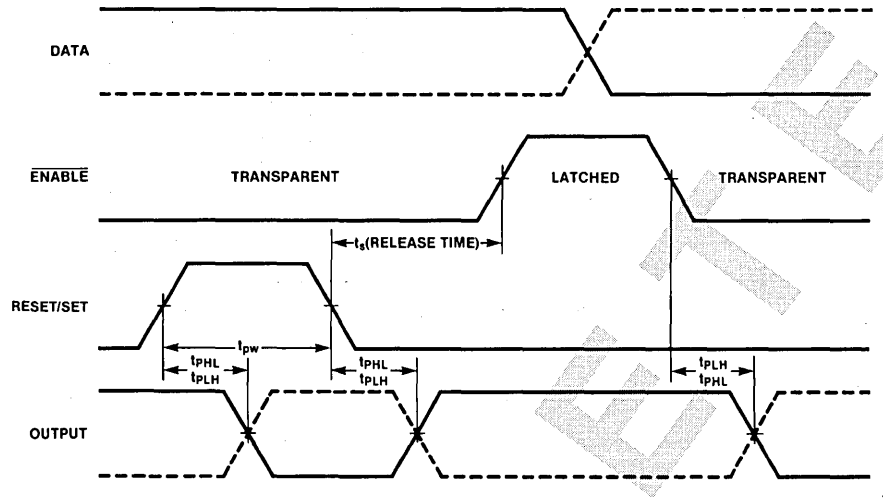
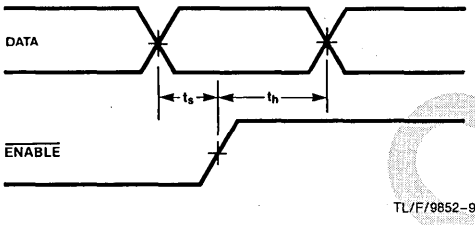


FIGURE 3. Reset Timing



Notes:
t_s is the minimum time before the transition of the enable that information must be present at the data input.
t_h is the minimum time after the transition of the enable that information must remain unchanged at the data input.

FIGURE 4. Data Setup and Hold Time

National Semiconductor

Not Intended For New Designs

100135
Triple J-K Flip-Flop

General Description

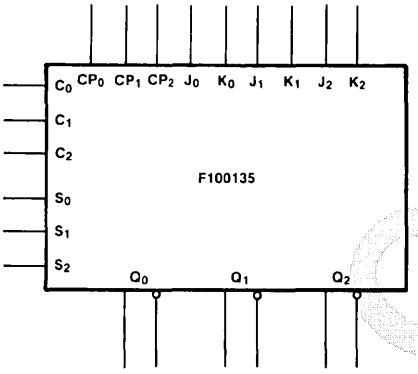
The 100135 contains three J-K, edge-triggered master-slave flip-flops with true and complement outputs. All have individual Clock (CP_n), Clear (C_n), and Set (S_n) inputs. Clocking occurs on the rising edge of CP_n. All inputs have 50 kΩ pull-down resistors.

Features

- Toggle frequency 750 MHz Typical
- Propagation delay 2.2 ns max
- Outputs specified to drive a 50Ω load

Ordering Code: See Section 6

Logic Symbol

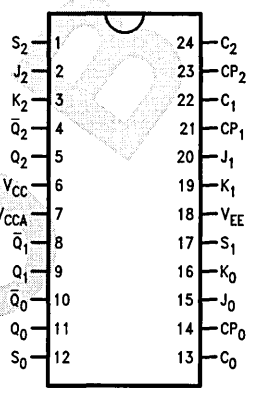


TL/F/9854–3

Pin Names	Description
J_0–J_2	J Inputs
K_0–K_2	K Inputs
S_0–S_2	Direct Set Inputs
C_0–C_2	Direct Clear Inputs
CP_0–CP_2	Clock Inputs
Q_0–Q_2	Data Outputs
$\overline{Q}_0$–$\overline{Q}_2$	Complementary Data Outputs

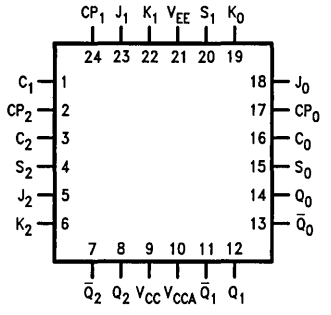
Connection Diagrams

24-Pin DIP



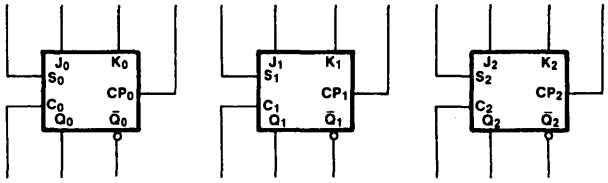
TL/F/9854–1

24-Pin Quad Cerpak



TL/F/9854–2

Logic Diagram



TL/F/9854–5

Truth Tables (Each Flip-Flop)

Synchronous Operation

Inputs					Outputs
J_n	K_n	CP_n	S_n	C_n	$Q_n(t+1)$
L	L	⌐	L	L	$Q_n(t)$
L	H	⌐	L	L	L
H	L	⌐	L	L	H
H	H	⌐	L	L	$\overline{Q_n(t)}$
X	X	H	L	L	$Q_n(t)$
X	X	L	L	L	$Q_n(t)$

Asynchronous Operation

Inputs					Outputs
J_n	K_n	CP_n	S_n	C_n	Q_n
X	X	X	H	L	H
X	X	X	L	H	L
X	X	X	H	H	U

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
U = Undefined
t = Time before CP Positive Transition
t + 1 = Time after CP Positive Transition
⌐ = LOW-to-HIGH Transition

Absolute Maximum Ratings

Above which the useful life may be impaired. (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Maximum Junction Temperature (T_J)	+150°C
Case Temperature under Bias (T_C)	0°C to +85°C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Output Current (DC Output HIGH)	−50 mA
Operating Range (Note 2)	−5.7V to −4.2V

DC Electrical Characteristics

V_{EE} = −4.5V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1025	−955	−880	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1810	−1705	−1620			
V_{OHC}	Output HIGH Voltage	−1035			mV	V_{IN} = $V_{IH(Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610			
V_{IH}	Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

DC Electrical Characteristics

V_{EE} = −4.2V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1020		−870	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1810		−1605			
V_{OHC}	Output HIGH Voltage	−1030			mV	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1595			
V_{IH}	Input HIGH Voltage	−1150		−870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

DC Electrical Characteristics

V_{EE} = −4.8V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1035		−880	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830		−1620			
V_{OHC}	Output HIGH Voltage	−1045			mV	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610			
V_{IH}	Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1830		−1490	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Parametric values specified at −4.2V to −4.8V.

Note 3: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 4: Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DC Electrical Characteristics

V_{EE} = −4.2V to −4.8V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C

Symbol	Parameter	Min	Typ	Max	Units	Conditions
I_{IH}	Input HIGH Current All Inputs			350	μA	V_{IN} = $V_{IH\ (Max)}$
I_{EE}	Power Supply Current	−195	−150	−90	mA	Inputs Open

Ceramic Dual-In-Line Package AC Characteristics

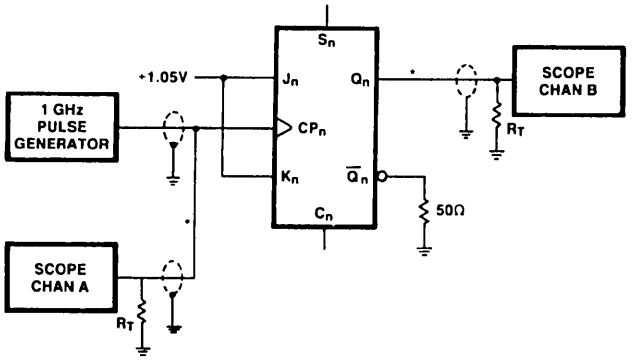
V_{EE} = −4.2V to −4.8V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
f_{max}	Toggle Frequency	600		600		600		MHz	*Figure 1*
t_{PLH} t_{PHL}	Propagation Delay CP_n to Output	0.70	2.20	0.70	2.00	0.70	2.20	ns	*Figures 2* and *3*
t_{PLH} t_{PHL}	Propagation Delay C_n, S_n to Output	0.90	1.80	0.90	2.00	0.90	2.40	ns	CP_n = L, CP_n = H
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.30	1.40	0.30	1.40	0.30	1.40	ns	
t_S	Setup Time J_n, K_n to CP_n C_n, S_n (Release Time)	0.90 1.50		0.70 1.30		0.90 1.50		ns	*Figures 2* and *3*
t_H	Hold Time J_n, K_n to CP_n	0.80		0.80		0.80		ns	
$t_{pw}(H)$	Pulse Width HIGH CP_n, C_n, S_n	2.00		2.00		2.00		ns	

Cerpak AC Characteristics

V_{EE} = −4.2V to −4.8V, V_{CC} = V_{CCA} = GND

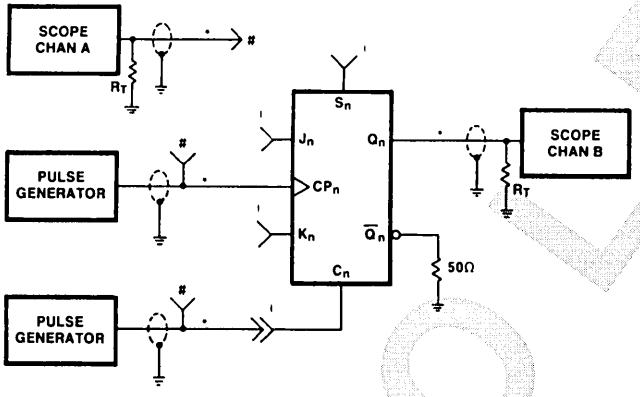
Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
f_{max}	Toggle Frequency	650		650		650		MHz	*Figure 1*
t_{PLH} t_{PHL}	Propagation Delay CP_n to Output	0.70	2.00	0.70	1.80	0.70	2.00	ns	*Figures 2* and *3*
t_{PLH} t_{PHL}	Propagation Delay C_n, S_n to Output	0.90	1.60	0.90	1.80	0.90	2.20	ns	CP_n = L, CP_n = H
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.30	1.30	0.30	1.30	0.30	1.30	ns	
t_S	Setup Time J_n, K_n to CP_n C_n, S_n (Release Time)	0.80 1.40		0.60 1.20		0.80 1.40		ns	*Figures 2* and *3*
t_H	Hold Time J_n, K_n to CP_n	0.70		0.70		0.70		ns	
$t_{pw}(H)$	Pulse Width HIGH CP_n, C_n, S_n	2.00		2.00		2.00		ns	



TL/F/9854–6

FIGURE 1. Toggle Frequency Test Circuit

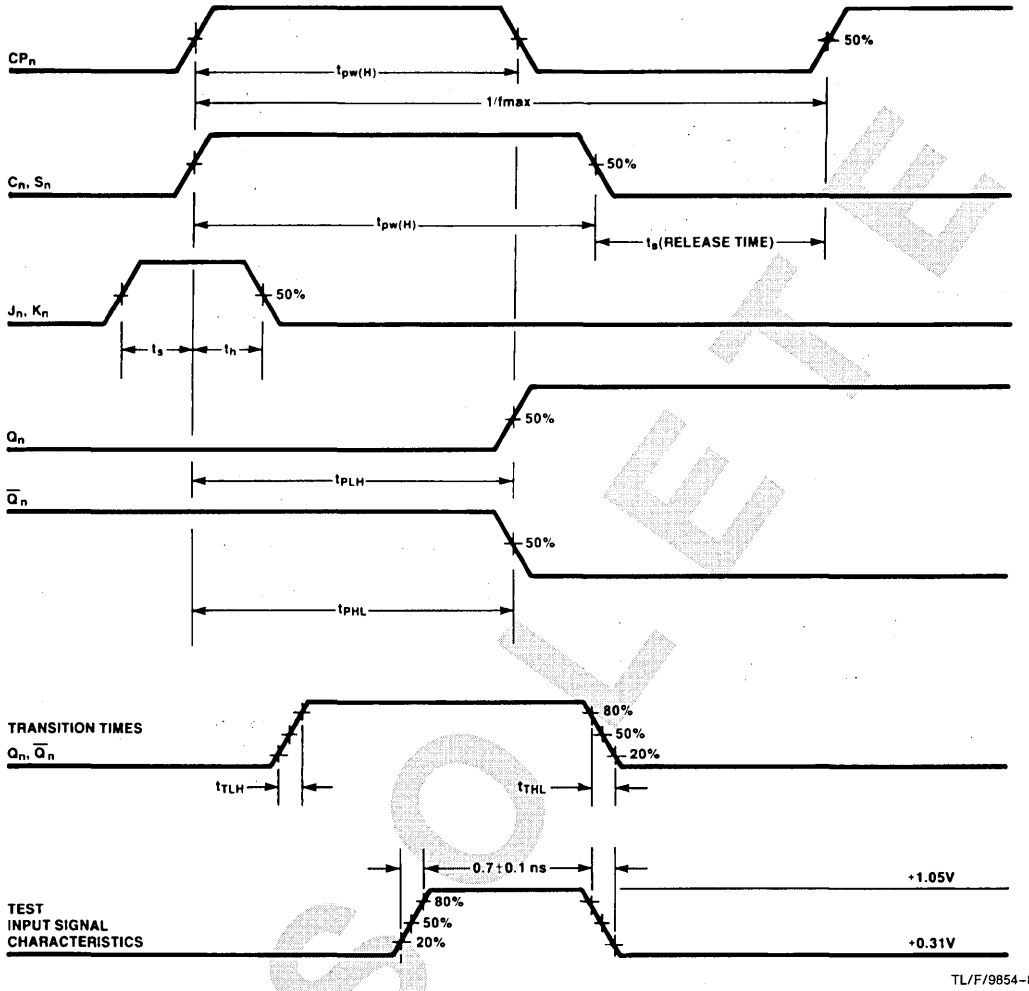
Notes:
$V_{CC} = V_{CCA} = +2V$
$V_{EE} = -2.5V$
* = equal electrical length 50Ω lines
$R_T = 50\Omega$ termination
Decouple power supplies with 0.1 μF from V_{CC} and V_{EE} to GND
C_L = Fixture and stray capacitance ≤ 3 pF
Load all unused outputs with 50Ω to GND
Set pulse generator output level for 740 mV p-p at a frequency of 10 MHz as measured at the clock input pin of the device under test. Do not readjust this voltage for frequencies up to f_{max}. The pad isolates the generator output for D.U.T. input impedance variations. Signal voltage measured at the D.U.T. input will vary as input impedance varies with frequency.



TL/F/9854–7

FIGURE 2. AC Test Circuit

Notes:
$V_{CC} = V_{CCA} = +2V$
$V_{EE} = -2.5V$
Decouple power supplies with 0.1 μF from V_{CC} and V_{EE} to GND
$R_T = 50\Omega$ termination
Load all unused outputs with 50Ω to GND
C_L = Fixture and stray capacitance ≤ 3 pF
* = equal electrical length 50Ω lines
# = Connect Scope CHAN A to pulse generator as required
† = Connect pulse generator to input under test; else connect input to voltage source set to +1.05 volts for logic HIGH or +0.31 volts for logic LOW
Consult truth table for appropriate logical condition



TL/F/9854–8

FIGURE 3. Propagation Delays and Setup and Hold Time

National Semiconductor

Not Intended For New Designs

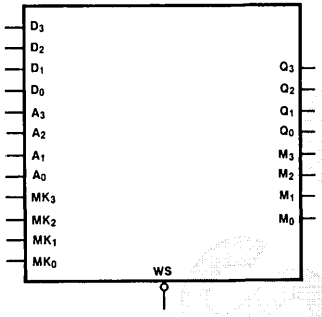
100142
4 x 4-Bit Content Addressable Memory

General Description

The 100142 is a 4 word by 4-bit Content Addressable Memory (CAM). Reading is accomplished when an address select input (A_0, A_7, A_2, A_3) is LOW and the write strobe input ($\overline{WS}$) is HIGH. The corresponding stored word appears on the data outputs (Q_0–Q_3). Writing can be performed to individual bits of a word or to the whole word. (A LOW on an address select input enables a 4-bit word.) A LOW on a bit mask input (MK_0, MK_1, MK_2, MK_3) enables a bit within all four 4-bit words. Write data is presented on the data inputs (D_0, D_1, D_2, D_3) and is latched into the addressed bit latch when the write strobe input ($\overline{WS}$) is LOW. Hence, the bit mask inputs are used to selectively store data bit-wise within an addressed word. During writing, the data input word is simultaneously compared to each of the stored memory words. A search/compare is performed by placing a LOW on the bit mask inputs and presenting a data pattern to the data inputs. Corresponding to the bit mask inputs, the match outputs (M_0–M_3) go LOW if a data bit of the pattern matches the respective stored bit. A HIGH on any bit mask input forces a LOW on the respective match output. Each input has a 50 kΩ (typical) pull-down resistor to V_{EE}.

Ordering Code: See Section 6

Logic Symbol

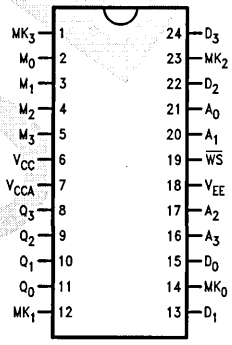


TL/F/9857–3

Pin Names	Description
MK_0–MK_3	Data Mask Inputs
A_0–A_3	Address Inputs
D_0–D_3	Data Inputs
$\overline{WS}$	Write Strobe Input
M_0–M_3	Match Outputs
Q_0–Q_3	Data Outputs

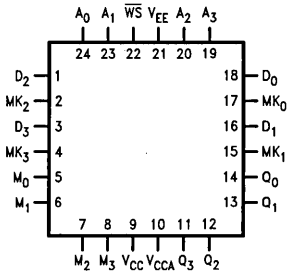
Connection Diagrams

24-Pin DIP



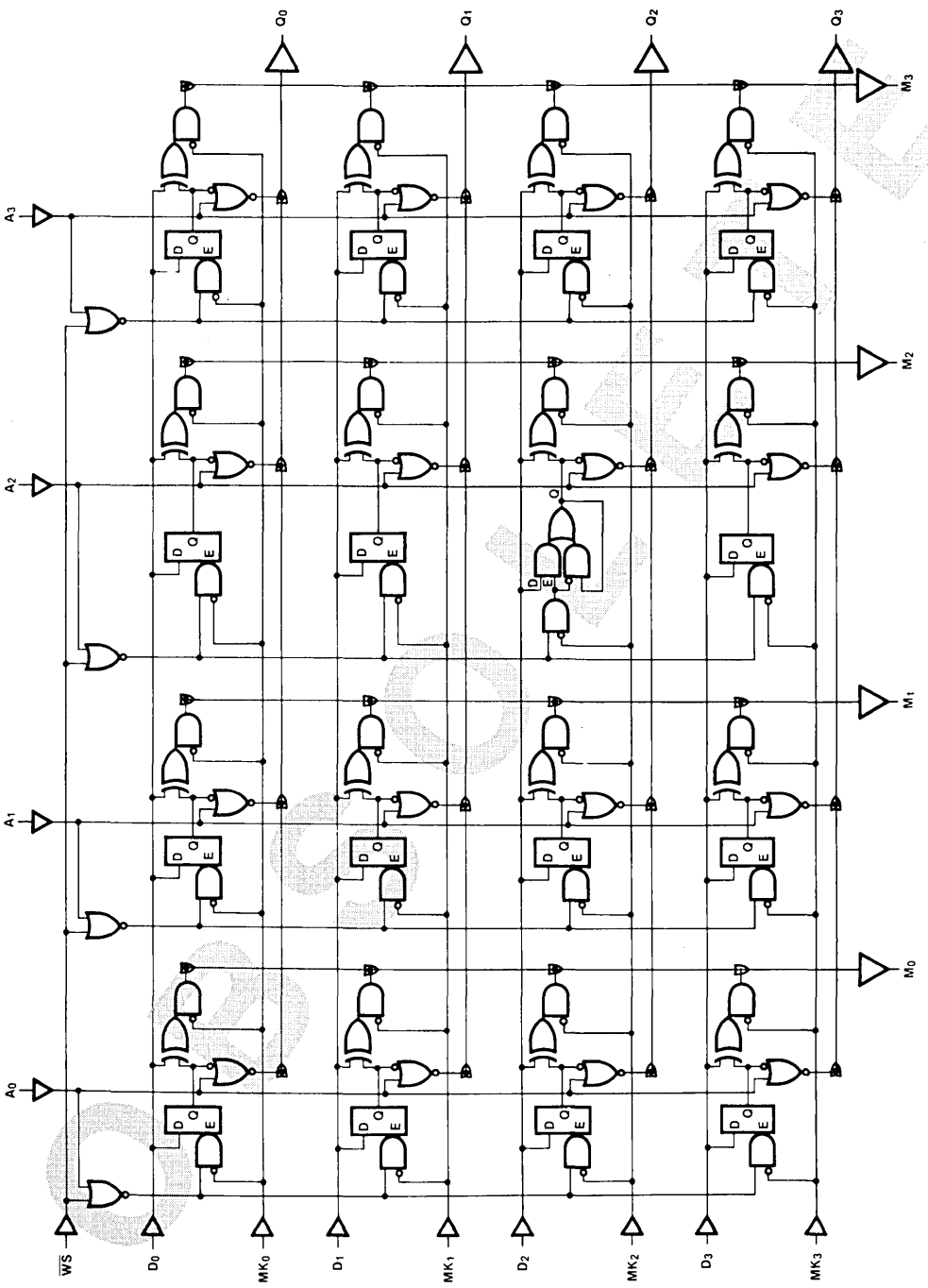
TL/F/9857–1

24-Pin Quad Cerpak



TL/F/9857–2

Logic Diagram



Truth Table

Operation	Inputs				Flip-Flop	Outputs	
	$\overline{WS}$	A_I	D_j	MK_j	Q_{ij}	M_i	Q_j
	$\overline{WS}$	A_0 A_1 A_2 A_3	D_0 D_1 D_2 D_3	MK_0 MK_1 MK_2 MK_3		M_0 M_1 M_2 M_3	Q_0 Q_1 Q_2 Q_3
Write Disabled	X X	H L	X X	X H	NC NC	X L	L $Q_{ij}n-1$
Write	L L	L L	H L	L L	H L	L L	H L
Read	H H	L L	X X	X X	H L	X X	H L
Match Masked	H	X	X	H	NC	L	X
Match Not Satisfied	H H H H	L H H L	H H L L	L L L L	L L H H	H H H H	L L L H
Match Satisfied	H H H H	L H H L	H H L L	L L L L	H H L L	L L L L	H L L L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
NC = No Change from Previous State
$\overline{WS}$ = Write Strobe
A_i = Address for ith Word
D_j = Data for jth Bit

MK_j = Data Mask for jth Bit
H = Mask
Q_{ij} = Cell State for ith Word, jth Bit
M_i = Match Output of ith Word
L = True
Q_j = Data Output of jth Bit
Q_{n-1} = Previous Cell State

Absolute Maximum Ratings

Above which the useful life may be impaired. (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Maximum Junction Temperature (T_J)	+150°C
Case Temperature under Bias (T_C)	0°C to +85°C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Output Current (DC Output HIGH)	−50 mA
Operating Range (Note 2)	−5.7V to −4.2V

DC Electrical Characteristics

V_{EE} = −4.5V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1025	−955	−880	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1810	−1705	−1620			
V_{OHC}	Output HIGH Voltage	−1035			mV	V_{IN} = $V_{IH(Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610			
V_{IH}	Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

DC Electrical Characteristics

V_{EE} = −4.2V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1020		−870	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1810		−1605			
V_{OHC}	Output HIGH Voltage	−1030			mV	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1595			
V_{IH}	Input HIGH Voltage	−1150		−870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

DC Electrical Characteristics

V_{EE} = −4.8V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1035		−880	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830		−1620			
V_{OHC}	Output HIGH Voltage	−1045			mV	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610			
V_{IH}	Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1830		−1490	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Parametric values specified at −4.2V to −4.8V.

Note 3: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 4: Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DC Electrical Characteristics

V_{EE} = −4.2V to −4.8V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C

Symbol	Parameter	Min	Typ	Max	Units	Conditions
I_{IH}	Input HIGH Current All Inputs			200	μA	V_{IN} = $V_{IH\ (Max)}$
I_{EE}	Power Supply Current	−288	−190	−114	mA	Inputs Open

Ceramic Dual-In-Line Package AC Electrical Characteristics

V_{EE} = −4.2V to −4.8V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{AD}	Address to Data Out	1.20	4.40	1.20	4.30	1.20	4.50	ns	*Figures 2* and *3*
t_{DM}	Data In to Match Out Time	1.60	3.70	1.60	3.60	1.60	3.80	ns	*Figure 5*
t_{MM}	Mask In to "Enable Partial" Match Out Time	1.20	3.90	1.20	3.90	1.20	4.00	ns	
t_{DD}	Data In to New Data Out	1.70	4.40	1.70	4.40	1.70	4.60	ns	*Figure 2*
t_{WD}	Write to New Data Out	2.50	5.40	2.50	5.20	2.30	5.10	ns	
t_{AM}	Address to Match	2.50	4.60	2.50	4.60	2.50	4.90	ns	
t_{MD}	Mask to Data	2.20	4.90	2.20	4.80	2.20	5.00	ns	
t_{WSM}	$\overline{WS}$ to Match	2.80	4.90	2.80	4.80	2.80	5.10	ns	
t_W	Write Pulse Width	1.30		1.30		1.30		ns	*Figure 1*
t_{AS}	Address Setup before Write Time	1.40		1.40		1.40		ns	
t_{AH}	Address Hold after Write Time	1.40		1.40		1.40		ns	
t_{DS}	Data In Setup before Write Time	0.60		0.60		0.60		ns	
t_{DH}	Data In Hold after Write Time	1.10		1.10		1.10		ns	
t_{MH}	Mask In Hold Write Time	2.50		2.50		2.50		ns	
t_{MS}	Mask In Setup Write Time	1.10		1.10		1.10		ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.50	2.30	0.50	2.30	0.50	2.30	ns	*Figure 2*

Cerpak AC Electrical Characteristics

V_{EE} = −4.2V to −4.8V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{AD}	Address to Data Out	1.20	4.20	1.20	4.10	1.20	4.30	ns	*Figures 2* and *3*
t_{DM}	Data In to Match Out Time	1.60	3.50	1.60	3.40	1.60	3.60	ns	*Figure 5*
t_{MM}	Mask In to "Enable Partial" Match Out Time	1.20	3.70	1.20	3.70	1.20	3.80	ns	
t_{DD}	Data In to New Data Out	1.70	4.20	1.70	4.20	1.70	4.40	ns	*Figure 2*
t_{WD}	Write to New Data Out	2.50	5.20	2.50	5.00	2.30	4.90	ns	
t_{AM}	Address to Match	2.50	4.40	2.50	4.40	2.50	4.70	ns	
t_{MD}	Mask to Data	2.20	4.70	2.20	4.60	2.20	4.80	ns	
t_{WSM}	$\overline{WS}$ to Match	2.80	4.70	2.80	4.60	2.80	4.90	ns	
t_W	Write Pulse Width	1.20		1.20		1.20		ns	*Figure 1*
t_{AS}	Address Setup before Write Time	1.30		1.30		1.30		ns	
t_{AH}	Address Hold after Write Time	1.30		1.30		1.30		ns	
t_{DS}	Data In Setup before Write Time	0.50		0.50		0.50		ns	
t_{DH}	Data In Hold after Write Time	1.00		1.00		1.00		ns	
t_{MH}	Mask In Hold Write Time	2.40		2.40		2.40		ns	
t_{MS}	Mask In Setup Write Time	1.00		1.00		1.00		ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.50	2.20	0.50	2.20	0.50	2.20	ns	*Figure 2*

Switching Waveforms

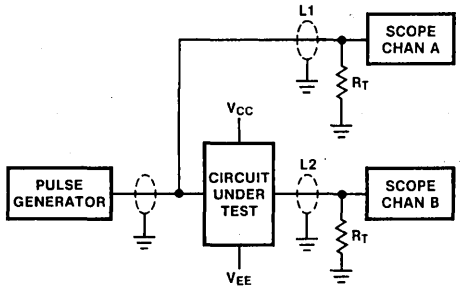


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FIGURE 1. AC Test Circuit

Note:

V_{CC}, V_{CCA} = +2V, V_{EE} = −2.5V
L1, L2 and L3 = equal length 50Ω impedance lines
R_T = 50Ω terminator internal to scope
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
All unused outputs are loaded with 50Ω to GND
C_L = Fixture and stray capacitance ≤ 3 pF

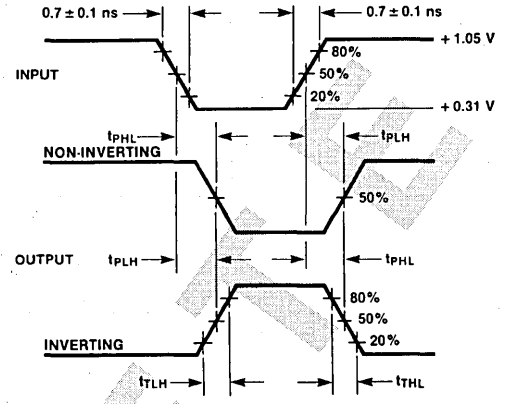

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FIGURE 2. Output Rise and Fall Times and Waveforms

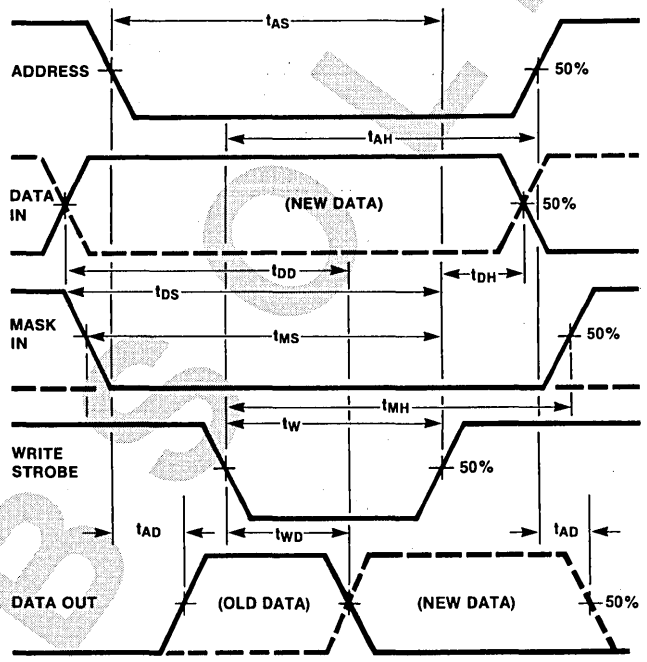

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FIGURE 3. Write Mode and Read/Write Mode Waveforms

Switching Waveforms (Continued)

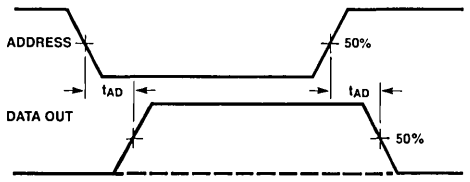

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FIGURE 4. Read Mode Waveforms

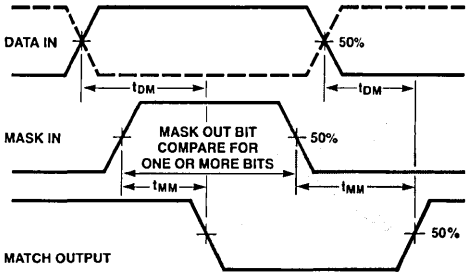

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FIGURE 5. Search Mode Waveforms

Application

The 100142 is an ideal choice for the register file unit of a bit-slice processor. *Figure 5* shows the configuration of four 100145s into a 16 x 16 register file. The write enbles (WE_1, WE_2) and output enables (OE_1, OE_2) are configured to allow access to one array of sixteen 16-bit registers or two arrays of sixteen 8-bit registers. Simultaneous read and write addressing is made possible with separate buses. Also, reading and then writing to the same address is easily and efficiently done by tying one write enable to an output enable.

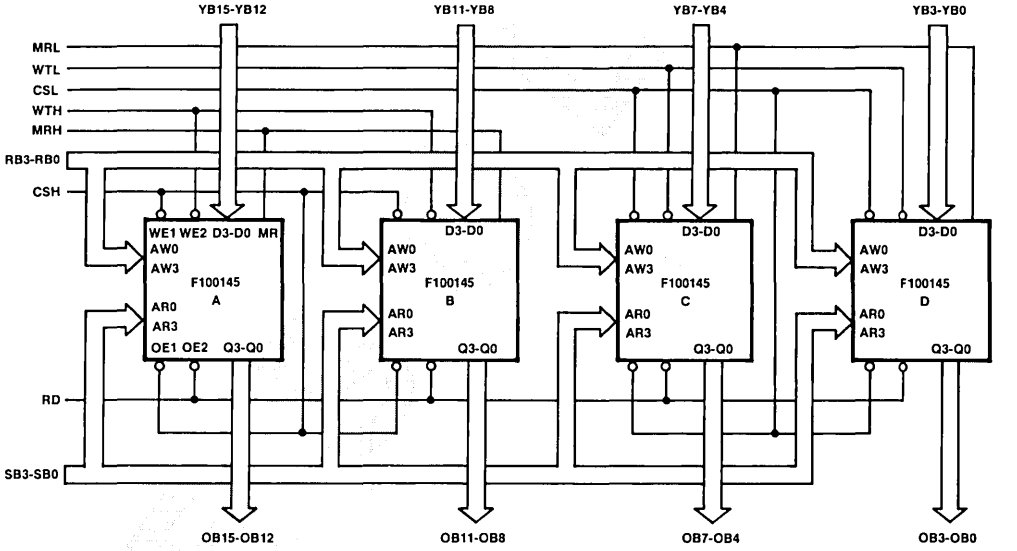

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FIGURE 5. 16 x 16 Register File (Two 16 x 8 Register Files)

National Semiconductor

Not Intended For New Designs

100156
Mask-Merge/Latch

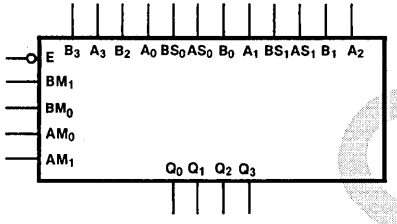
General Description

The 100156 merges two 4-bit words to form a 4-bit output word. The AM_n enable allows the merge of A into B by one, two or three places (per the AS_n value) from the left. The BM_n enable similarly allows the merge of B into A from the left (per the BS_n value). The B merge overrides the A merge when both are enabled. This means A first merges into B and B then merges into the A merge. If the B address is equal to or greater than the A address, then outputs are forced to B.

The merge outputs feed four latches, which have a common enable ($\overline{E}$) input. All inputs have a 50 kΩ (typical) pull-down resistor tied to V_{EE}.

Ordering Code: See Section 6

Logic Symbol



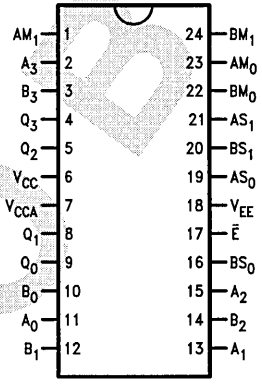
TL/F/9861–3

Pin Names	Description
$\overline{E}$	Latch Enable Input (Active LOW)
A_0–A_3	A Data Inputs
B_0–B_3	B Data Inputs
AM_0, AM_1	A Merge Enable Inputs
BM_0, BM_1	B Merge Enable Inputs
AS_0, AS_1	A Address Inputs
BS_0, BS_1	B Address Inputs
Q_0–Q_3	Data Outputs

Note:
When $\overline{E}$ is HIGH, Q_n outputs do not change.
When $\overline{E}$ is LOW, Q_n = A or B depending on which is selected.

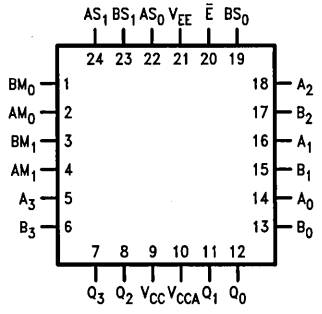
Connection Diagrams

24-Pin DIP



TL/F/9861–1

24-Pin Quad Cerpak



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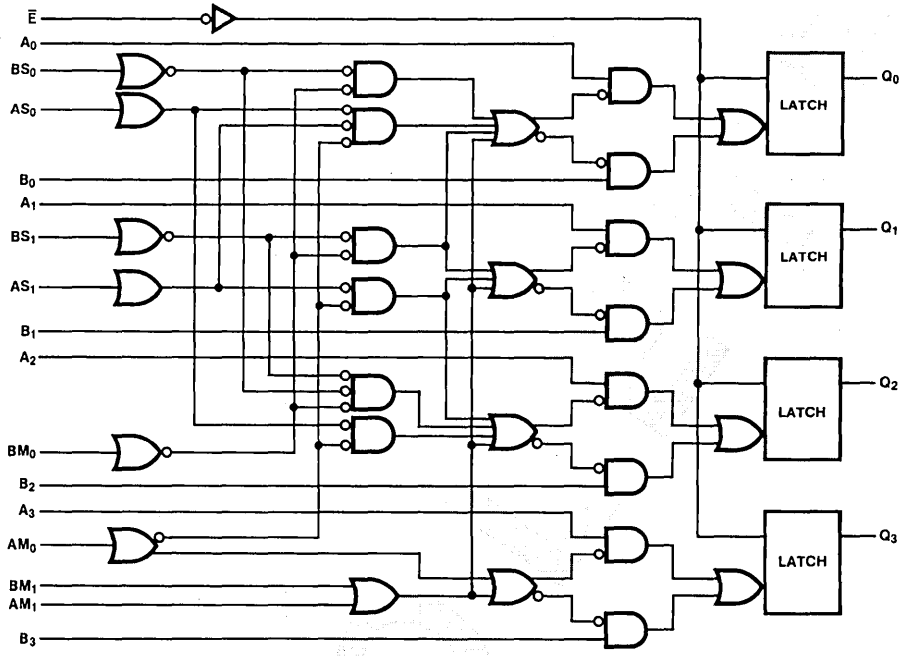
Logic Diagram



TL/F/9861–5

Truth Table

Inputs									Outputs				Remarks
Merge Enables				Addresses									
BM_1	BM_0	AM_1	AM_0	BS_1	BS_0	AS_1	AS_0	$\overline{E}$	Q_0	Q_1	Q_2	Q_3	
X	X	H	X	X	X	X	X	L	B_0	B_1	B_2	B_3	Select B
H	X	X	X	X	X	X	X	L	B_0	B_1	B_2	B_3	
L	L	L	L	X	X	X	X	L	A_0	A_1	A_2	A_3	Select A
L	L	L	H	X	X	L	L	L	B_0	B_1	B_2	B_3	Merge A → B
L	L	L	H	X	X	L	H	L	A_0	B_1	B_2	B_3	
L	L	L	H	X	X	H	L	L	A_0	A_1	B_2	B_3	
L	L	L	H	X	X	H	H	L	A_0	A_1	A_2	B_3	
L	H	L	L	L	L	X	X	L	A_0	A_1	A_2	A_3	Merge B → A
L	H	L	L	L	H	X	X	L	B_0	A_1	A_2	A_3	
L	H	L	L	H	L	X	X	L	B_0	B_1	A_2	A_3	
L	H	L	L	H	H	X	X	L	B_0	B_1	B_2	A_3	
L	H	L	H	L	L	L	H	L	A_0	B_1	B_2	B_3	Merge A → B
L	H	L	H	L	L	H	L	L	A_0	A_1	B_2	B_3	
L	H	L	H	L	L	H	H	L	A_0	A_1	A_2	B_3	
L	H	L	H	L	H	H	L	L	B_0	A_1	B_2	B_3	Merge A → B
L	H	L	H	L	H	H	H	L	B_0	A_1	A_2	B_3	then
L	H	L	H	H	L	H	H	L	B_0	B_1	A_2	B_3	Merge B → A
L	H	L	H	H	H	H	H	L	B_0	B_1	B_2	B_3	B Address ≥ A Address
L	H	L	H	H	H	H	L	L	B_0	B_1	B_2	B_3	
L	H	L	H	H	H	L	H	L	B_0	B_1	B_2	B_3	
L	H	L	H	H	H	L	L	L	B_0	B_1	B_2	B_3	
L	H	L	H	H	L	H	L	L	B_0	B_1	B_2	B_3	
L	H	L	H	H	L	L	H	L	B_0	B_1	B_2	B_3	
L	H	L	H	H	L	L	L	L	B_0	B_1	B_2	B_3	
L	H	L	H	L	H	L	L	L	B_0	B_1	B_2	B_3	
L	H	L	H	L	L	L	L	L	B_0	B_1	B_2	B_3	
X	X	X	X	X	X	X	X	H	Q_0	Q_1	Q_2	Q_3	Latch

Before Start	At Start	After End	At End

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

Absolute Maximum Ratings

Above which the useful life may be impaired. (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Maximum Junction Temperature (T_J)	+150°C
Case Temperature under Bias (T_C)	0°C to +85°C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Output Current (DC Output HIGH)	−50 mA
Operating Range (Note 2)	−5.7V to −4.2V

DC Electrical Characteristics

V_{EE} = −4.5V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1025	−955	−880	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1810	−1705	−1620			
V_{OHC}	Output HIGH Voltage	−1035			mV	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610			
V_{IH}	Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

DC Electrical Characteristics

V_{EE} = −4.2V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1020		−870	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1810		−1605			
V_{OHC}	Output HIGH Voltage	−1030			mV	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1595			
V_{IH}	Input HIGH Voltage	−1150		−870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

DC Electrical Characteristics

V_{EE} = −4.8V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1035		−880	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830		−1620			
V_{OHC}	Output HIGH Voltage	−1045			mV	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610			
V_{IH}	Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1830		−1490	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Parametric values specified at −4.2V to −4.8V.

Note 3: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 4: Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DC Electrical Characteristics

V_{EE} = −4.2V to −4.8V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C

Symbol	Parameter	Min	Typ	Max	Units	Conditions
I_{IH}	Input HIGH Current A_n, B_n, BM_n, AM_n, BS_n, AS_n, $\overline{E}$			265	μA	V_{IN} = $V_{IH\ (Max)}$
I_{EE}	Power Supply Current	−235	−161	−107	mA	Inputs Open

Ceramic Dual-In-Line Package AC Electrical Characteristics

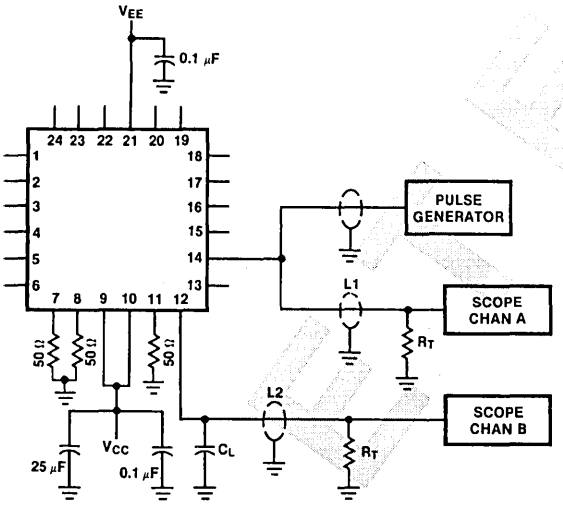
V_{EE} = −4.2V to −4.8V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay A_n, B_n to Outputs (Transparent Mode)	0.45	1.90	0.50	1.80	0.50	2.00	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to Outputs	1.00	2.50	1.00	2.40	1.00	2.50	ns	
t_{PLH} t_{PHL}	Propagation Delay AM_n, BM_n, AS_n, BS_n to Outputs (Transparent Mode)	1.20	3.70	1.20	3.70	1.20	3.80	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.90	0.45	1.80	0.45	1.90	ns	
t_S	Setup Time A_n, B_n AM_n, BM_n, AS_n, BS_n	0.80 2.90		0.80 2.90		0.80 2.90		ns	*Figure 3*
t_H	Hold Time A_n, B_n AM_n, BM_n, AS_n, BS_n	2.10 0.80		2.10 0.80		2.10 0.80		ns	
$t_{pw}(L)$	Pulse Width LOW $\overline{E}$	2.00		2.00		2.00		ns	*Figure 2*

Cerpak AC Electrical Characteristics

V_{EE} = −4.2V to −4.8V, V_{CC} = V_{CCA} = GND

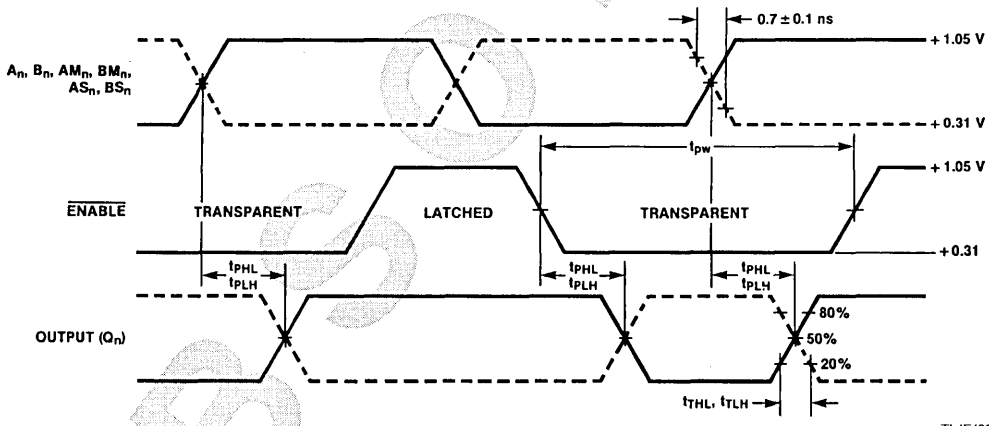
Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay A_n, B_n to Outputs (Transparent Mode)	0.45	1.70	0.50	1.60	0.50	1.80	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to Outputs	1.00	2.30	1.00	2.20	1.00	2.30	ns	
t_{PLH} t_{PHL}	Propagation Delay AM_n, BM_n, AS_n, BS_n to Outputs (Transparent Mode)	1.20	3.50	1.20	3.50	1.20	3.60	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.80	0.45	1.70	0.45	1.80	ns	
t_S	Setup Time A_n, B_n AM_n, BM_n, AS_n, BS_n	0.70 2.80		0.70 2.80		0.70 2.80		ns	*Figure 3*
t_H	Hold Time A_n, B_n AM_n, BM_n, AS_n, BS_n	2.00 0.70		2.00 0.70		2.00 0.70		ns	
$t_{pw}(L)$	Pulse Width LOW $\overline{E}$	2.00		2.00		2.00		ns	*Figure 2*



TL/F/9861–6

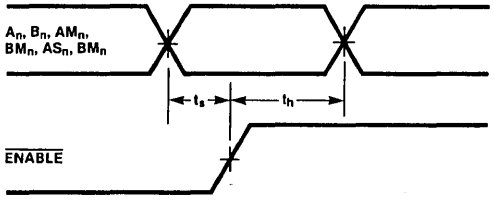
Notes:
V_{CC}, V_{CCA} = +2V, V_{EE} = −2.5V
L1 and L2 = equal length 50Ω impedance lines
R_T = 50Ω terminator internal to scope
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
All unused outputs are loaded with 50Ω to GND
C_L = Fixture and stray capacitance ≤ 3 pF
Pin numbers shown are for flatpak; for DIP see logic symbol

FIGURE 1. AC Test Circuit



TL/F/9861–7

FIGURE 2. Enable Timing



TL/F/9861–8

Notes:
t_s is the minimum time before the transition of the enable that information must be present at the designated input.
t_h is the minimum time after the transition of the enable that information must remain unchanged at the designated input.

FIGURE 3. Data Setup and Hold Times

National Semiconductor

Not Intended For New Designs

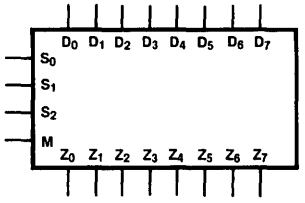
100158
8-Bit Shift Matrix

General Description

The 100158 contains a combinatorial network which performs the function of an 8-bit shift matrix. Three control lines (S_n) are internally decoded and define the number of places which an 8-bit word present at the inputs (D_n) is shifted to the left and presented at the outputs (Z_n). A Mode Control input (M) is provided which, if LOW, forces LOW all outputs to the right of the one that contains D_7. This operation is sometimes referred to as *LOW backfill.* If M is HIGH, an end-around shift is performed such that D_0 appears at the output to the right of the one that contains D_7. This operation is commonly referred to as *barrel shifting.* All inputs have 50 kΩ pull-down resistors.

Ordering Code: See Section 6

Logic Symbol

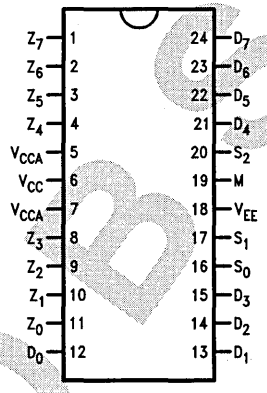


TL/F/9862–3

Pin Names	Description
D_0–D_7	Data Inputs
S_0–S_2	Select Inputs
M	Mode Control Input
Z_0–Z_7	Data Outputs

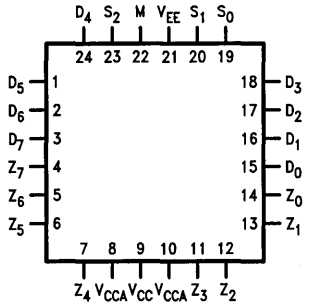
Connection Diagrams

24-Pin DIP



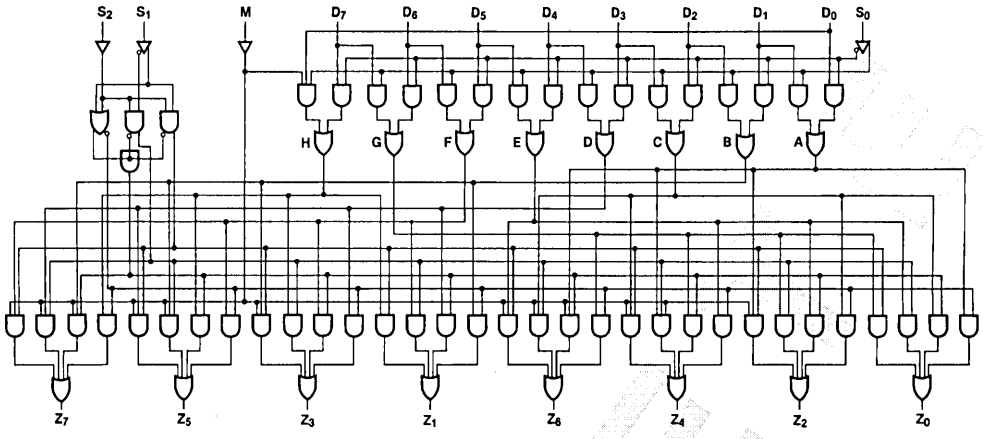
TL/F/9862–1

24-Pin Quad Cerpak



TL/F/9862–2

Logic Diagram



TL/F/9862–5

Truth Table

Inputs				Outputs							
M	S_0	S_1	S_2	Z_0	Z_1	Z_2	Z_3	Z_4	Z_5	Z_6	Z_7
X	L	L	L	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
L	H	L	L	D_1	D_2	D_3	D_4	D_5	D_6	D_7	L
L	L	H	L	D_2	D_3	D_4	D_5	D_6	D_7	L	L
L	H	H	L	D_3	D_4	D_5	D_6	D_7	L	L	L
L	L	L	H	D_4	D_5	D_6	D_7	L	L	L	L
L	H	L	H	D_5	D_6	D_7	L	L	L	L	L
L	L	H	H	D_6	D_7	L	L	L	L	L	L
L	H	H	H	D_7	L	L	L	L	L	L	L
H	H	L	L	D_1	D_2	D_3	D_4	D_5	D_6	D_7	D_0
H	L	H	L	D_2	D_3	D_4	D_5	D_6	D_7	D_0	D_1
H	H	H	L	D_3	D_4	D_5	D_6	D_7	D_0	D_1	D_2
H	L	L	H	D_4	D_5	D_6	D_7	D_0	D_1	D_2	D_3
H	H	L	H	D_5	D_6	D_7	D_0	D_1	D_2	D_3	D_4
H	L	H	H	D_6	D_7	D_0	D_1	D_2	D_3	D_4	D_5
H	H	H	H	D_7	D_0	D_1	D_2	D_3	D_4	D_5	D_6

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

Absolute Maximum Ratings

Above which the useful life may be impaired. (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Maximum Junction Temperature (T_J)	+150°C
Case Temperature under Bias (T_C)	0°C to +85°C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Output Current (DC Output HIGH)	−50 mA
Operating Range (Note 2)	−5.7V to −4.2V

DC Electrical Characteristics

V_{EE} = −4.5V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1025	−955	−880	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1810	−1705	−1620			
V_{OHC}	Output HIGH Voltage	−1035			mV	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610			
V_{IH}	Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

DC Electrical Characteristics

V_{EE} = −4.2V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1020		−870	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1810		−1605			
V_{OHC}	Output HIGH Voltage	−1030			mV	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1595			
V_{IH}	Input HIGH Voltage	−1150		−870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

DC Electrical Characteristics

V_{EE} = −4.8V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1035		−880	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830		−1620			
V_{OHC}	Output HIGH Voltage	−1045			mV	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610			
V_{IH}	Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1830		−1490	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Parametric values specified at −4.2V to −4.8V.

Note 3: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 4: Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DC Electrical Characteristics

V_{EE} = −4.2V to −4.8V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_C 0°C to +85°C

Symbol	Parameter	Min	Typ	Max	Units	Conditions
I_{IH}	Input HIGH Current All Inputs			220	μA	V_{IN} = $V_{IH\ (Max)}$
I_{EE}	Power Supply Current	−205	−140	−95	mA	Inputs Open

Ceramic Dual-In-Line Package AC Electrical Characteristics

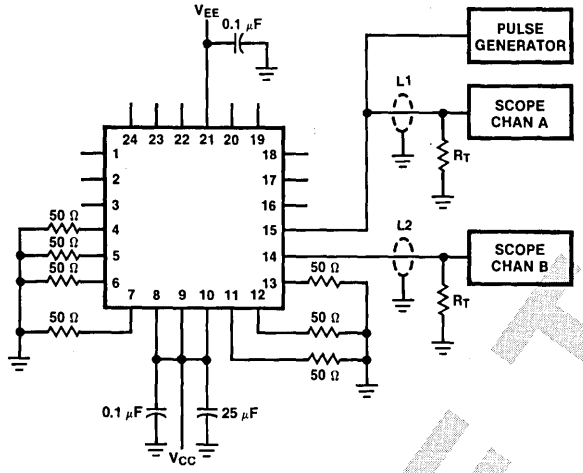
V_{EE} = −4.2V to −4.8V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay D_n to Output	1.10	2.80	1.10	2.70	1.10	2.80	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay M to Output	1.15	4.20	1.25	4.20	1.15	4.20	ns	
t_{PLH} t_{PHL}	Propagation Delay S_n to Output	1.70	4.20	1.70	4.20	1.70	4.20	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.50	2.30	0.50	2.30	0.50	2.30	ns	

Cerpak AC Electrical Characteristics

V_{EE} = −4.2V to −4.8V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay D_n to Output	1.10	2.60	1.10	2.50	1.10	2.60	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay M to Output	1.15	4.00	1.25	4.00	1.15	4.00	ns	
t_{PLH} t_{PHL}	Propagation Delay S_n to Output	1.70	4.00	1.70	4.00	1.70	4.00	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.50	2.20	0.50	2.20	0.50	2.20	ns	

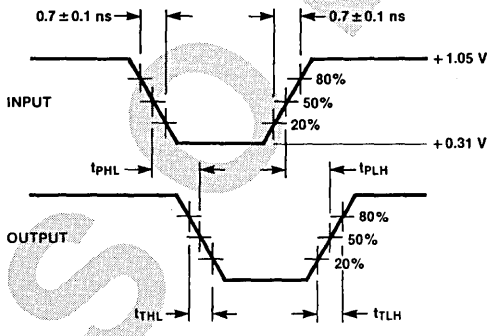


TL/F/9862–6

Notes:

V_{CC}, V_{CCA} = +2V, V_{EE} = −2.5V.
L1 and L2 = equal length 50Ω impedance lines.
R_T = 50Ω terminator internal to scope.
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}.
All unused outputs are loaded with 50Ω to GND.
C_L = fixture and stray capacitance ≤ 3 pF.
Pin numbers shown are for flatpak; for DIP refer to logic symbol.

FIGURE 1. AC Test Circuit



TL/F/9862–7

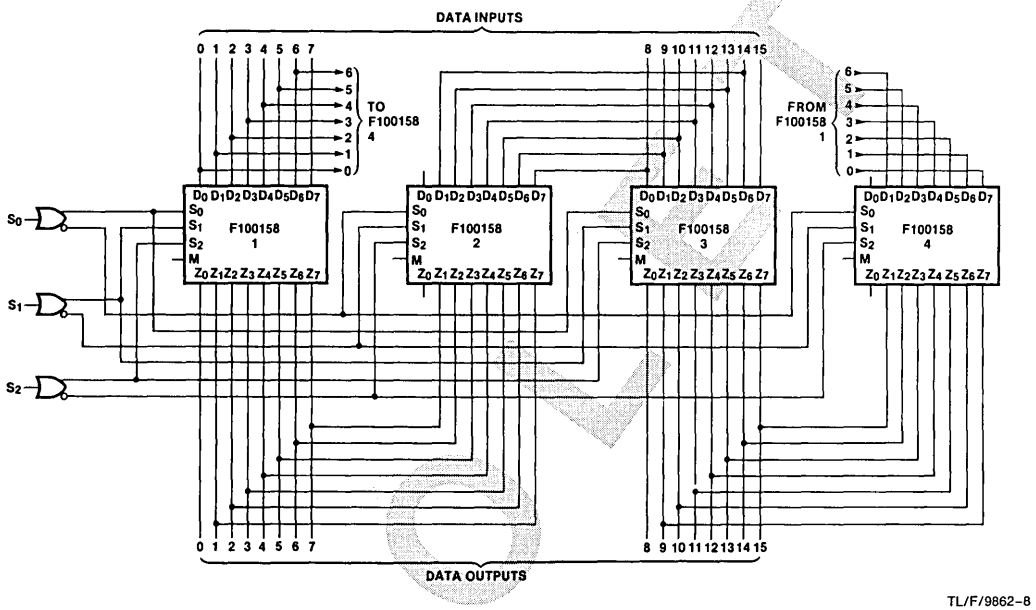
FIGURE 2. Propagation Delay and Transition Times

Applications

The following technique uses two ranks of 100158s to shift a 64-bit word from 0 to 63 places. Although two stage delays are required (one for each rank), the total shift takes only about 4 ns. This technique performs a bit shift on each 8-bit byte in the first rank and then a modulo-8 byte shift on the 64-bit word in the second rank.

Basic 16-Bit 0–7 Place Shifter

Figure 3 shows the basic 0–7 place shift technique which can be expanded to accommodate any word length. Each 8-bit byte requires a pair of 100158s operating in the LOW backfill mode. The address lines for each pair of ICs are driven out of phase by three OR gates. Inputs for the two ICs are taken from two bytes transposed in order; outputs are transposed and emitter-OR tied. One device shifts right from location 0 and the other shifts left from location 7. The bits shifted off one pair are picked up by the next pair of 100158s or—in the case of the last one in the rank—returned to the first device. The net result is a 0–7 place shift of the entire word.



TL/F/9862–8

FIGURE 3. Basic 16-Bit 0–7 Place Shifter

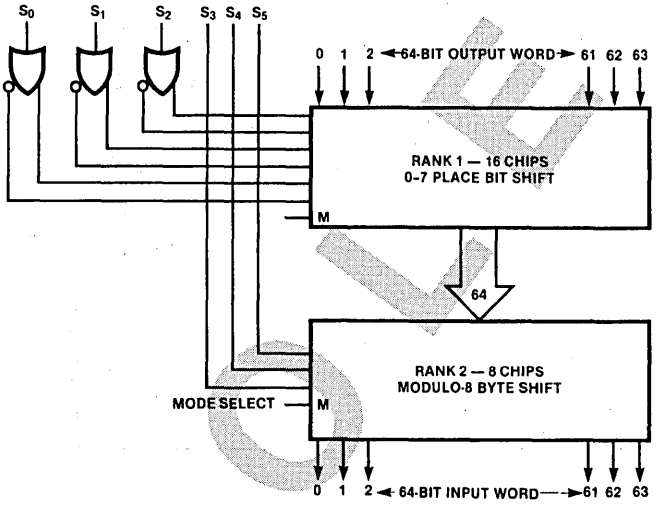
Applications (Continued)

Expanding to 64-Bit Word and 64-Place Shift

The basic 0–7 place shift technique can be expanded to accommodate a 64-bit word shifted from 0 to 63 places, however, two ranks of 100158s are required *(Figure 4)*. The first rank is identical to the one illustrated in *Figure 3* except it contains a total of 16 devices. The second rank consists of eight additional 100158s connected in the modulo-8 configuration shown in *Figure 5*.

The modulo-8 rank is used to simulate an 8-bit simultaneous shift since the 100158 cannot shift in 8-bit jumps. The modulo-8 configuration is achieved by wiring the first rank and the output device to the second rank as illustrated in *Figure 5*. The LSB of each output byte in the first rank is wired to one of the eight inputs of the first 100158 in the second rank. The next least significant bit of each first-rank 100158 pair, however, is connected to the inputs of the second 100158 in the second rank. The other first-ranked outputs are connected in a similar fashion to the remainder of the second-rank inputs. Ultimately, the outputs of the second rank must then be connected to reform the final usable 64-bit word so that the bits are again ordered from 0–63.

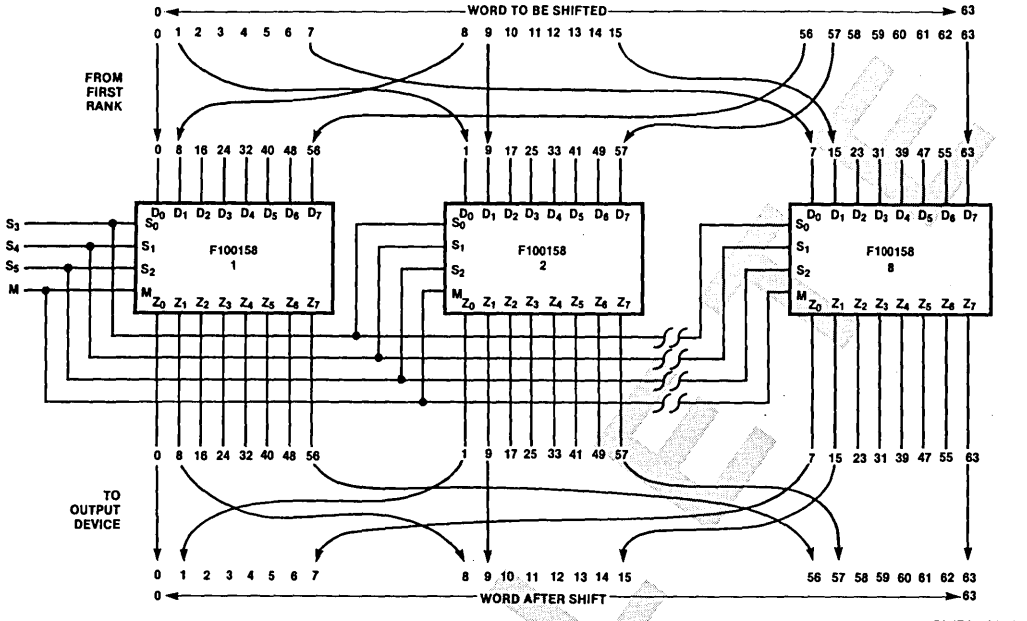
The effect is that each single-location shift in the second rank appears to be an eight place shift in the final word due to the way the inputs and outputs of the second rank are connected. The combination of the two ranks produces the 64-place shift of the entire word.



TL/F/9862–9

FIGURE 4. 64-Bit 0–63 Place Barrel Shifter

Applications (Continued)



TL/F/9862–10

FIGURE 5. Modulo-8 Shift

National Semiconductor

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100165
Universal Priority Encoder

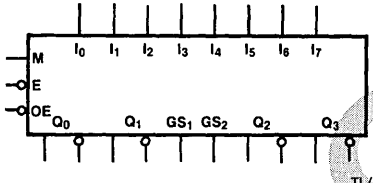
General Description

The 100165 contains eight input latches with a common Enable ($\overline{E}$) followed by encoding logic which generates the binary address of the highest priority input having a HIGH signal. The circuit operates as a dual 4-input encoder when the Mode Control (M) input is LOW, and as a single 8-input encoder when M is HIGH. In the 8-input mode, Q_0, Q_1 and Q_2 are the relevant outputs, I_0 is the highest priority input and GS_1 is the relevant Group Signal output. In the dual mode, Q_0, Q_1 and GS_1 operate with I_0–I_3. Q_2, Q_3 and GS_2 operate with I_4–I_7. A GS output goes LOW when its pertinent inputs are all LOW.

Inputs are latched when $\overline{E}$ goes HIGH. A HIGH signal on the Output Enable ($\overline{OE}$) input forces all Q outputs LOW and GS outputs HIGH. Expansion to accommodate more inputs can be done by connecting the GS output of a higher priority group to the $\overline{OE}$ input of the next lower priority group. All inputs have 50 kΩ pulldown resistors.

Ordering Code: See Section 6

Logic Symbol

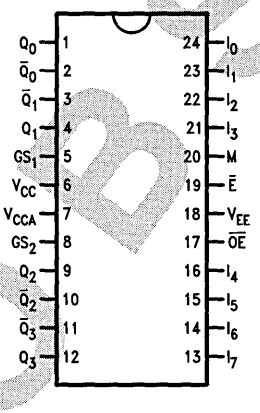


TL/F/9866–3

Pin Names	Description
I_0–I_7	Data Inputs
$\overline{E}$	Enable Input (Active LOW)
$\overline{OE}$	Output Enable Input (Active LOW)
M	Mode Control Input
GS_1–GS_2	Group Signal Outputs
Q_0–Q_3	Data Outputs
$\overline{Q}_0$–$\overline{Q}_3$	Complementary Data Outputs

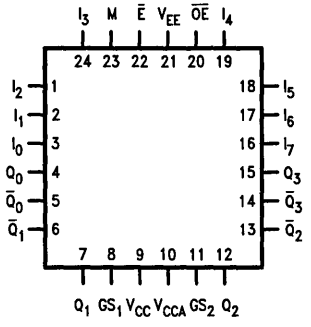
Connection Diagrams

24-Pin DIP



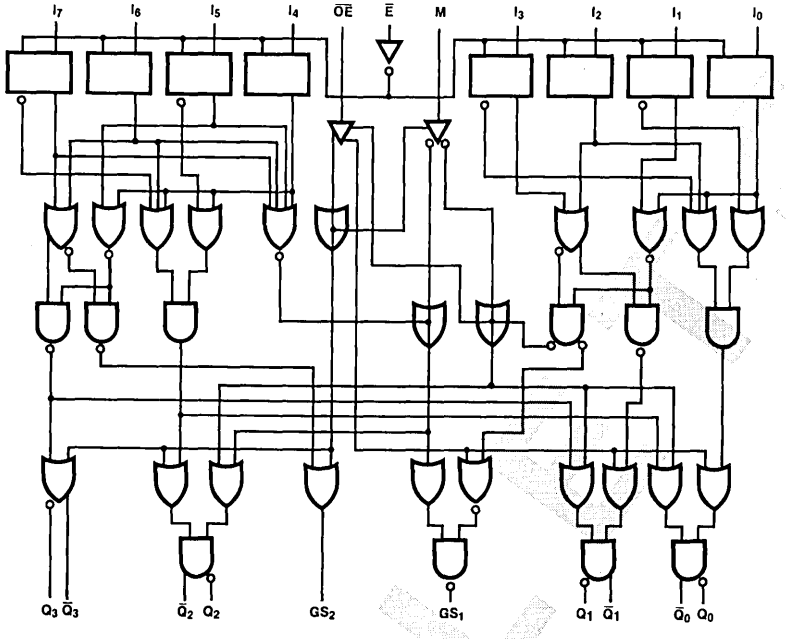
TL/F/9866–1

24-Pin Quad Cerpak



TL/F/9866–2

Logic Diagram



TL/F/9866–5

Truth Table

Inputs											Outputs					
$\overline{E}$	$\overline{OE}$	M	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	Q_0	Q_1	Q_2	Q_3	GS_1	GS_2
L	L	L	H	X	X	X					L	L			H	
L	L	L	L	H	X	X					H	L			H	
L	L	L	L	L	H	X					L	H			H	
L	L	L	L	L	L	H					H	H			H	
L	L	L	L	L	L	L					L	L			L	
L	L	L					H	X	X	X			L	L		H
L	L	L					L	H	X	X			H	L		H
L	L	L					L	L	H	X			L	H		H
L	L	L					L	L	L	H			H	H		H
L	L	L					L	L	L	L			L	L		L
L	L	H	H	X	X	X	X	X	X	X	L	L	L	L	H	H
L	L	H	L	H	X	X	X	X	X	X	H	L	L	L	H	H
L	L	H	L	L	H	X	X	X	X	X	L	H	L	L	H	H
L	L	H	L	L	L	H	X	X	X	X	H	H	L	L	H	H
L	L	H	L	L	L	L	H	X	X	X	L	L	H	L	H	H
L	L	H	L	L	L	L	L	H	X	X	H	L	H	L	H	H
L	L	H	L	L	L	L	L	L	H	X	L	H	H	L	H	H
L	L	H	L	L	L	L	L	L	L	H	H	H	H	L	H	H
L	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	H
X	H	X	X	X	X	X	X	X	X	X	L	L	L	L	H	H
H	L	L	X	X	X	X	X	X	X	X	Given by I_0–I_7 when $\overline{E}$ was LOW and M = L					
H	L	H	X	X	X	X	X	X	X	X	Given by I_0–I_7 when $\overline{E}$ was LOW and M = H					

H = HIGH Voltage Level
L = LOW Voltage Level
Blank = X = Don't Care

Absolute Maximum Ratings

Above which the useful life may be impaired. (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Maximum Junction Temperature (T_J)	+150°C
Case Temperature under Bias (T_C)	0°C to +85°C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Output Current (DC Output HIGH)	−50 mA
Operating Range (Note 2)	−5.7V to −4.2V

DC Electrical Characteristics

V_{EE} = −4.5V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1025	−955	−880	mV	V_{IN} = V_{IH} (Max) or V_{IL} (Min)	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1810	−1705	−1620			
V_{OHC}	Output HIGH Voltage	−1035			mV	V_{IN} = V_{IH} (Min) or V_{IL} (Max)	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610			
V_{IH}	Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = V_{IL} (Min)	

DC Electrical Characteristics

V_{EE} = −4.2V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1020		−870	mV	V_{IN} = V_{IH} (Max) or V_{IL} (Min)	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1810		−1605			
V_{OHC}	Output HIGH Voltage	−1030			mV	V_{IN} = V_{IH} (Min) or V_{IL} (Max)	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1595			
V_{IH}	Input HIGH Voltage	−1150		−870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = V_{IL} (Min)	

DC Electrical Characteristics

V_{EE} = −4.8V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1035		−880	mV	V_{IN} = V_{IH} (Max) or V_{IL} (Min)	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830		−1620			
V_{OHC}	Output HIGH Voltage	−1045			mV	V_{IN} = V_{IH} (Min) or V_{IL} (Max)	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610			
V_{IH}	Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1830		−1490	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = V_{IL} (Min)	

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Parametric values specified at −4.2V to −4.8V.

Note 3: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 4: Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DC Electrical Characteristics

V_{EE} = −4.2V to −4.8V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C

Symbol	Parameter	Min	Typ	Max	Units	Conditions
I_{IH}	Input HIGH Current All Inputs			230	μA	V_{IN} = $V_{IH\ (Max)}$
I_{EE}	Power Supply Current	−200	−140	−77	mA	Inputs Open

Ceramic Dual-In-Line Package AC Characteristics

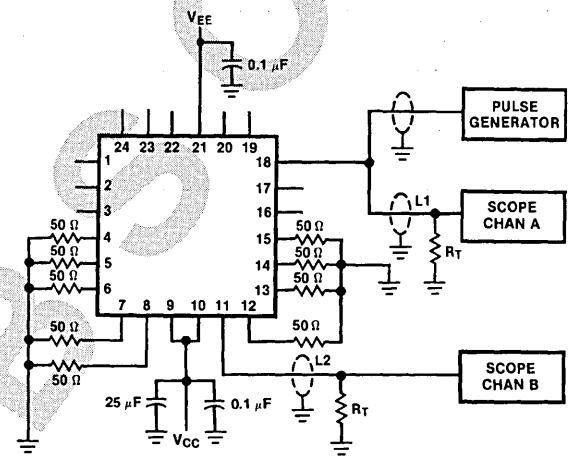
V_{EE} = −4.2V to −4.8V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Condition
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay I_0–I_7 to Q_0–Q_3, $\overline{Q}_0$–$\overline{Q}_3$ (Transparent Mode)	1.10	4.10	1.10	4.10	1.10	4.60	ns	*Figures 1* and *3*
t_{PLH} t_{PHL}	Propagation Delay I_0–I_7 to GS_1–GS_2 (Transparent Mode)	1.30	3.90	1.30	3.90	1.30	4.20	ns	
t_{PLH} t_{PHL}	Propagation Delay $\overline{OE}$ to Q_0–Q_3, $\overline{Q}_0$–$\overline{Q}_3$	1.00	3.00	1.00	3.00	1.10	3.30	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay $\overline{OE}$ to GS_1–GS_2	1.10	2.60	1.10	2.60	1.20	2.80	ns	
t_{PLH} t_{PHL}	Propagation Delay M to Q_0–Q_3, $\overline{Q}_0$–$\overline{Q}_3$	0.90	3.60	1.00	3.60	1.00	3.80	ns	
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to Q_0–Q_3, $\overline{Q}_0$–$\overline{Q}_3$	1.50	4.70	1.50	4.60	1.50	5.00	ns	*Figures 1* and *3*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.50	0.45	1.40	0.45	1.50	ns	*Figures 1, 2* and *3*
t_S	Setup Time I_0–I_7	1.00		0.90		1.00		ns	*Figure 4*
t_H	Hold Time I_0–I_7	1.20		1.20		1.20		ns	
$t_{pw}(L)$	Pulse Width LOW $\overline{E}$	2.00		2.00		2.00		ns	*Figure 3*

Cerpak AC Electrical Characteristics

V_{EE} = −4.2V to −4.8V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay I_0–I_7 to Q_0–Q_3, $\overline{Q}_0$–$\overline{Q}_3$ (Transparent Mode)	1.10	3.90	1.10	3.90	1.10	4.40	ns	*Figures 1* and *3*
t_{PLH} t_{PHL}	Propagation Delay I_0–I_7 to GS_1–GS_2 (Transparent Mode)	1.30	3.70	1.30	3.70	1.30	4.00	ns	
t_{PLH} t_{PHL}	Propagation Delay $\overline{OE}$ to Q_0–Q_3, $\overline{Q}_0$–$\overline{Q}_3$	1.00	2.80	1.00	2.80	1.10	3.10	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay $\overline{OE}$ to GS_1–GS_2	1.10	2.40	1.10	2.40	1.20	2.60	ns	
t_{PLH} t_{PHL}	Propagation Delay M to Q_0–Q_3, $\overline{Q}_0$–$\overline{Q}_3$	0.90	3.40	1.00	3.40	1.00	3.60	ns	
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to Q_0–Q_3, $\overline{Q}_0$–$\overline{Q}_3$	1.50	4.50	1.50	4.40	1.50	4.80	ns	*Figures 1* and *3*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.40	0.45	1.30	0.45	1.40	ns	*Figures 1*, *2* and *3*
t_S	Setup Time I_0–I_7	0.90		0.80		0.90		ns	*Figure 4*
t_H	Hold Time I_0–I_7	1.10		1.10		1.10		ns	
$t_{pw}(L)$	Pulse Width LOW $\overline{E}$	2.00		2.00		2.00		ns	*Figure 3*



TL/F/9866–6

FIGURE 1. AC Test Circuit

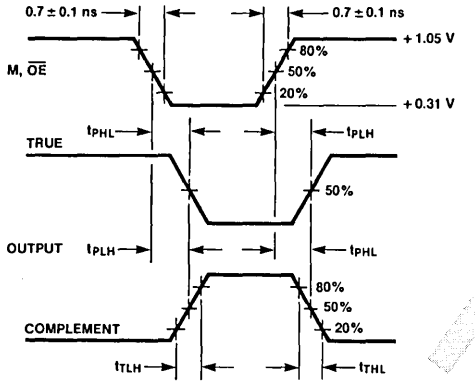


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FIGURE 2. Propagation Delay (M, $\overline{OE}$) and Transition Times

Notes:

V_{CC}, V_{CCA} = +2V, V_{EE} = −2.5V

L1 and L2 = equal length 50Ω impedance lines

R_T = 50Ω terminator internal to scope

Decoupling 0.1 μF from GND to V_{CC} and V_{EE}

All unused outputs are loaded with 50Ω to GND

C_L = Fixture and stray capacitance ≤ 3 pF

Pin numbers shown are for flatpak; for DIP see logic symbol

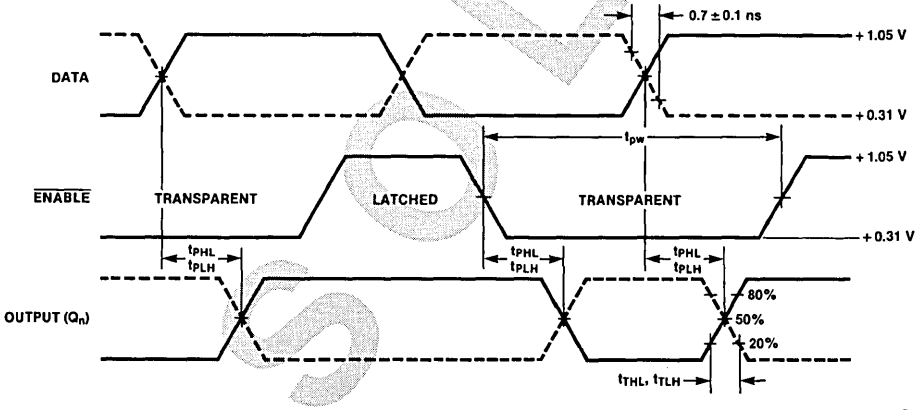

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FIGURE 3. Enable Timing

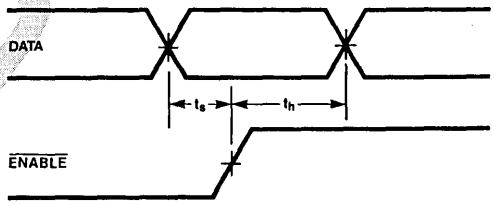

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FIGURE 4. Setup and Hold Times

Notes:

t_s is the minimum time before the transition of the enable that information must be present at the data input.

t_h is the minimum time after the transition of the enable that information must remain unchanged at the data input.

National Semiconductor

Not Intended For New Designs

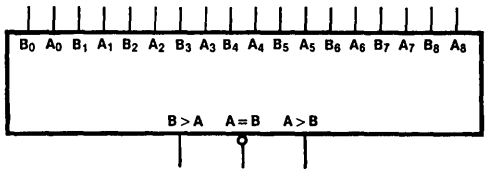
100166
9-Bit Comparator

General Description

The 100166 is a 9-bit magnitude comparator which compares the arithmetic value of two 9-bit words and indicates whether one word is greater than, or equal to, the other. Other functions can be generated by the wire-OR of the outputs. All inputs have 50 kΩ pulldown resistors.

Ordering Code: See Section 6

Logic Symbol

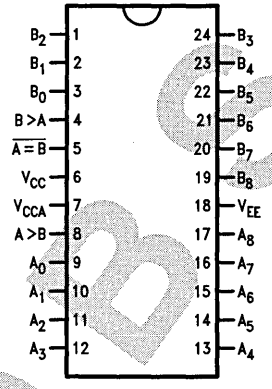


TL/F/9867–3

Pin Names	Description
A_0–A_8	A Data Inputs
B_0–B_8	B Data Inputs
A > B	A Greater than B Output
B > A	B Greater than A Output
$\overline{A = B}$	Complement A Equal to B Output (Active LOW)

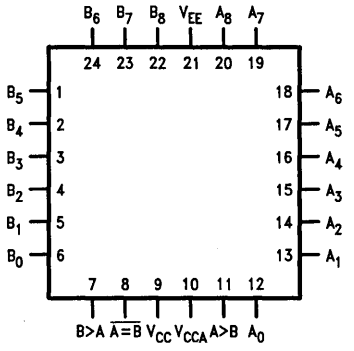
Connection Diagrams

24-Pin DIP



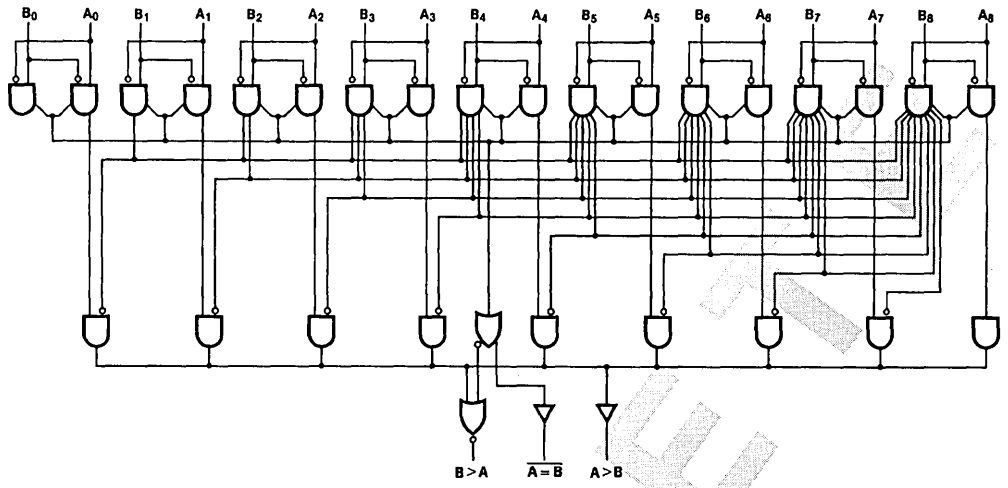
TL/F/9867–1

24-Pin Quad Cerpak



TL/F/9867–2

Logic Diagram



TL/F/9867–5

Truth Table

Inputs									Outputs		
A_8B_8	A_7B_7	A_6B_6	A_5B_5	A_4B_4	A_3B_3	A_2B_2	A_1B_1	A_0B_0	A > B	B > A	$\overline{A = B}$
H L									H	L	H
L H									L	H	H
$A_8 = B_8$	H L								H	L	H
$A_8 = B_8$	L H								L	H	H
$A_8 = B_8$	$A_7 = B_7$	H L							H	L	H
$A_8 = B_8$	$A_7 = B_7$	L H							L	H	H
$A_8 = B_8$	$A_7 = B_7$	$A_6 = B_6$	H L						H	L	H
$A_8 = B_8$	$A_7 = B_7$	$A_6 = B_6$	L H						L	H	H
$A_8 = B_8$	$A_7 = B_7$	$A_6 = B_6$	$A_5 = B_5$	H L					H	L	H
$A_8 = B_8$	$A_7 = B_7$	$A_6 = B_6$	$A_5 = B_5$	L H					L	H	H
$A_8 = B_8$	$A_7 = B_7$	$A_6 = B_6$	$A_5 = B_5$	$A_4 = B_4$	H L				H	L	H
$A_8 = B_8$	$A_7 = B_7$	$A_6 = B_6$	$A_5 = B_5$	$A_4 = B_4$	L H				L	H	H
$A_8 = B_8$	$A_7 = B_7$	$A_6 = B_6$	$A_5 = B_5$	$A_4 = B_4$	$A_3 = B_3$	H L			H	L	H
$A_8 = B_8$	$A_7 = B_7$	$A_6 = B_6$	$A_5 = B_5$	$A_4 = B_4$	$A_3 = B_3$	L H			L	H	H
$A_8 = B_8$	$A_7 = B_7$	$A_6 = B_6$	$A_5 = B_5$	$A_4 = B_4$	$A_3 = B_3$	$A_2 = B_2$	H L		H	L	H
$A_8 = B_8$	$A_7 = B_7$	$A_6 = B_6$	$A_5 = B_5$	$A_4 = B_4$	$A_3 = B_3$	$A_2 = B_2$	L H		L	H	H
$A_8 = B_8$	$A_7 = B_7$	$A_6 = B_6$	$A_5 = B_5$	$A_4 = B_4$	$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	H L	H	L	H
$A_8 = B_8$	$A_7 = B_7$	$A_6 = B_6$	$A_5 = B_5$	$A_4 = B_4$	$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	L H	L	H	H
$A_8 = B_8$	$A_7 = B_7$	$A_6 = B_6$	$A_5 = B_5$	$A_4 = B_4$	$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$	L	L	L

H = HIGH Voltage Level
L = LOW Voltage Level
Blank = Don't Care

Absolute Maximum Ratings

Above which the useful life may be impaired. (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Maximum Junction Temperature (T_J)	+150°C
Case Temperature under Bias (T_C)	0°C to +85°C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Output Current (DC Output HIGH)	−50 mA
Operating Range (Note 2)	−5.0V to −4.2V

DC Electrical Characteristics

V_{EE} = −4.5V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1025	−955	−880	mV	V_{IN} = V_{IH} (Max) or V_{IL} (Min)	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1810	−1705	−1620			
V_{OHC}	Output HIGH Voltage	−1035			mV	V_{IN} = V_{IH} (Min) or V_{IL} (Max)	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610			
V_{IH}	Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = V_{IL} (Min)	

DC Electrical Characteristics

V_{EE} = −4.2V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1020		−870	mV	V_{IN} = V_{IH} (Max) or V_{IL} (Min)	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1810		−1605			
V_{OHC}	Output HIGH Voltage	−1030			mV	V_{IN} = V_{IH} (Min) or V_{IL} (Max)	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1595			
V_{IH}	Input HIGH Voltage	−1150		−870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = V_{IL} (Min)	

DC Electrical Characteristics

V_{EE} = −4.8V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1035		−880	mV	V_{IN} = V_{IH} (Max) or V_{IL} (Min)	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830		−1620			
V_{OHC}	Output HIGH Voltage	−1045			mV	V_{IN} = V_{IH} (Min) or V_{IL} (Max)	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610			
V_{IH}	Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1830		−1490	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = V_{IL} (Min)	

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Parametric values specified at −4.2V to −4.8V.

Note 3: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 4: Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DC Electrical Characteristics

V_{EE} = −4.2V to −4.8V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C

Symbol	Parameter	Min	Typ	Max	Units	Conditions
I_{IH}	Input HIGH Current All Inputs			250	μA	V_{IN} = $V_{IH\ (Max)}$
I_{EE}	Power Supply Current	−238	−170	−119	mA	Inputs Open

Ceramic Dual-In-Line Package AC Electrical Characteristics

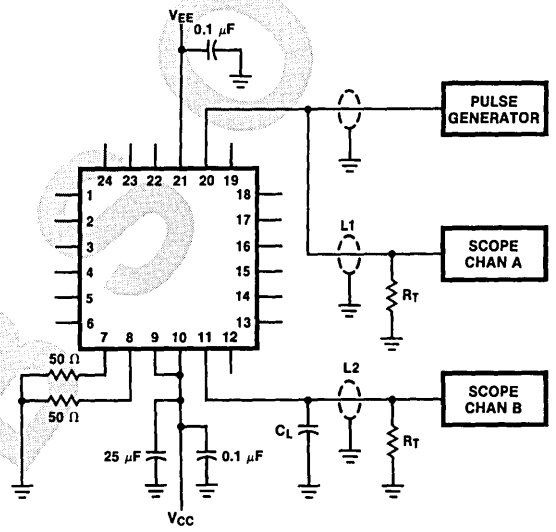
V_{EE} = −4.2V to −4.8V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Data to Output	1.40	3.50	1.40	3.50	1.40	3.90	ns	*Figures 1* and *2*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.55	0.45	1.50	0.45	1.50	ns	

Cerpak AC Electrical Characteristics

V_{EE} = −4.2V to −4.8V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Data to Output	1.40	3.30	1.40	3.30	1.40	3.70	ns	*Figures 1* and *2*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.45	0.45	1.40	0.45	1.40	ns	



TL/F/9867–6

FIGURE 1. AC Test Circuit

Notes:
V_{CC}, V_{CCA} = +2V, V_{EE} = −2.5V
L1 and L2 = equal length 50Ω impedance lines
R_T = 50Ω terminator internal to scope
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
All unused outputs are loaded with 50Ω to GND
C_L = Fixture and stray capacitance ≤ 3 pF
Pin numbers shown are for flatpak; for DIP see logic symbol

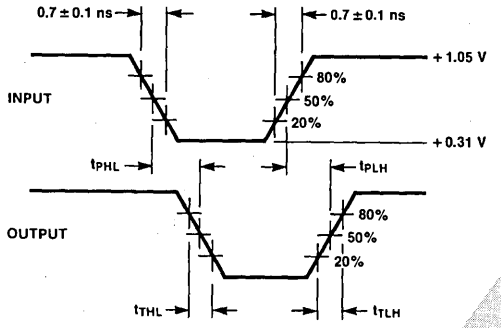


FIGURE 2. Propagation Delay and Transition Times

National Semiconductor

Not Intended For New Designs

100175
Quint Latch 100K In/10K Out

General Description

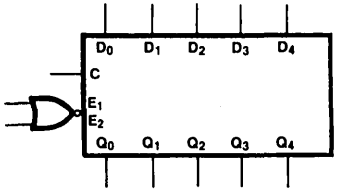
The 100175 is a 5-bit latch with temperature and voltage compensated 100K compatible inputs and voltage compensated 10K compatible outputs. Each latch has one data input and one output. All five latches share a common clear input and two enable inputs. All inputs have 50 kΩ pull-down resistors.

Features

- Outputs specified to drive a 50Ω load
- Available in 16-pin ceramic DIP
- 100K compatible inputs/10K compatible outputs

Ordering Code: See Section 6

Logic Symbol

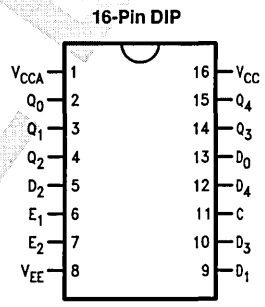


TL/F/9870–2

Pin Names	Description
D_0–D_4	100K Data Inputs
E_1, E_2	100K Enable Inputs
C	100K Common Clear Input
Q_0–Q_4	10K Data Outputs

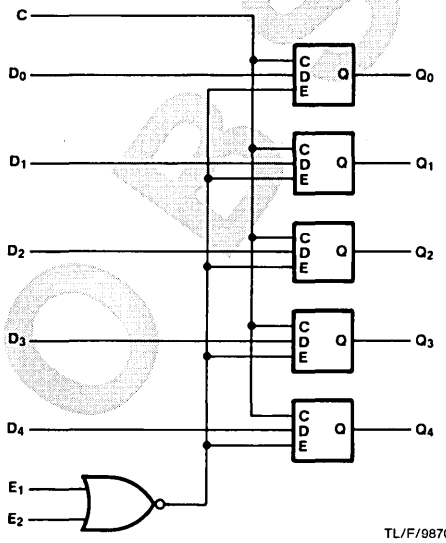
Connection Diagram

16-Pin DIP



TL/F/9870–1

Logic Diagram



TL/F/9870–3

Truth Table

Inputs				Output
D_n	E_1	E_2	C	Q_n
H	L	L	X	H
L	L	L	X	L
X	H	X	L	Q_{n-1}
X	X	H	L	Q_{n-1}
X	H	X	H	L
X	X	H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Q_{n-1} = Previous State

Absolute Maximum Ratings

Above which the useful life may be impaired

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature Under Bias (T_A)	−55°C to +125°C
Maximum Junction Temperature (T_J)	+150°C
Supply Voltage	−8V
Input Voltage (DC)	−5.2V to +0V
Output Current (DC Output HIGH)	−55 mA
Operating Range	−5.72V to −4.68V
Lead Temperature (Soldering, 10 sec.)	300°C

Recommended Operating Conditions

	Min	Typ	Max
Supply Voltage (V_{EE})	−5.72V	−5.2V	−4.68V
Ambient Temperature (T_A)	0°C		+75°C

DC Electrical Characteristics

V_{EE} = −5.2V, V_{CC} = V_{CCA} = GND, T_A = 0°C to +75°C (Notes 1, 2)

Symbol	Parameter	Temp	Min	Typ	Max	Units	Conditions	
V_{OH}	Output HIGH Voltage	T_A = 0°C	−1000		−840	mV	V_{IN} = V_{IH} (Max) or V_{IL} (Min)	Loading with 50Ω to −2.0V
		T_A = +25°C	−960		−810	mV		
		T_A = +75°C	−900		−720	mV		
V_{OL}	Output LOW Voltage	T_A = 0°C	−1870		−1665	mV	V_{IN} = V_{IH} (Max) or V_{IL} (Min)	
		T_A = +25°C	−1850		−1650	mV		
		T_A = +75°C	−1830		−1625	mV		
V_{OHC}	Output HIGH Voltage	T_A = 0°C	−1020			mV	V_{IN} = V_{IH} (Min) or V_{IL} (Max)	
		T_A = +25°C	−980			mV		
		T_A = +75°C	−920			mV		
V_{OLC}	Output LOW Voltage	T_A = 0°C			−1645	mV	V_{IN} = V_{IH} (Min) or V_{IL} (Max)	
		T_A = +25°C			−1630	mV		
		T_A = +75°C			−1605	mV		
V_{IH}	Input HIGH Voltage		−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage		−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IH}	Input HIGH Current				290		V_{IN} = V_{IH} (Max)	
I_{IL}	Input LOW Current		0.50			μA	V_{IN} = V_{IL} (Min)	
I_{EE}	V_{EE} Supply Current		−125	−90	−50	mA	Inputs Open	

Note 1: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 2: The specified limits shown in the DC Characteristics can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining transverse air flow of 2.5 meters/s (500 linear feet/min) over the device either mounted in the test socket or on the printed circuit board. Test voltage values are given in the DC Operating Conditions and defined in *Figure 4*.

DC Electrical Characteristics

V_{EE} = −4.68V, V_{CC} = V_{CCA} = GND, T_A = 0°C to +75°C (Notes 1, 2)

Symbol	Parameter	Temp	Min	Typ	Max	Units	Conditions
V_{OH}	Output HIGH Voltage	T_A = 0°C	−1000		−840	mV	V_{IN} = V_{IH} (Max) or V_{IL} (Min)
		T_A = +25°C	−960		−810	mV	
		T_A = +75°C	−900		−720	mV	
V_{OL}	Output LOW Voltage	T_A = 0°C	−1870		−1665	mV	V_{IN} = V_{IH} (Max) or V_{IL} (Min)
		T_A = +25°C	−1850		−1650	mV	
		T_A = +75°C	−1830		−1625	mV	
V_{OHC}	Output HIGH Voltage	T_A = 0°C	−1020			mV	V_{IN} = V_{IH} (Min) or V_{IL} (Max)
		T_A = +25°C	−980			mV	
		T_A = +75°C	−920			mV	
V_{OLC}	Output LOW Voltage	T_A = 0°C			−1645	mV	V_{IN} = V_{IH} (Min) or V_{IL} (Max)
		T_A = +25°C			−1630	mV	
		T_A = +75°C			−1605	mV	
							Loading with 50Ω to −2.0V
V_{IH}	Input HIGH Voltage		−1150		−880	mV	Guaranteed HIGH Signal for All Inputs
V_{IL}	Input LOW Voltage		−1810		−1475	mV	Guaranteed LOW Signal for All Inputs
I_{IH}	Input HIGH Current				290		V_{IN} = V_{IH} (Max)
I_{IL}	Input LOW Current		0.50			μA	V_{IN} = V_{IL} (Min)
I_{EE}	V_{EE} Supply Current		−125	−90	−50	mA	Inputs Open

Note 1: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 2: The specified limits shown in the DC Characteristics can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining transverse air flow of 2.5 meters/s (500 linear feet/min) over the device either mounted in the test socket or on the printed circuit board. Test voltage values are given in the DC Operating Conditions and defined in *Figure 4*.

DC Electrical Characteristics

V_{EE} = −5.72V, V_{CC} = V_{CCA} = GND, T_A = 0°C to +75°C (Notes 1, 2)

Symbol	Parameter	Temp	Min	Typ	Max	Units	Conditions
V_{OH}	Output HIGH Voltage	T_A = 0°C	−1000		−840	mV	V_{IN} = V_{IH} (Max) or V_{IL} (Min)
		T_A = +25°C	−960		−810	mV	
		T_A = +75°C	−900		−720	mV	
V_{OL}	Output LOW Voltage	T_A = 0°C	−1870		−1665	mV	V_{IN} = V_{IH} (Max) or V_{IL} (Min)
		T_A = +25°C	−1850		−1650	mV	
		T_A = +75°C	−1830		−1625	mV	
V_{OHC}	Output HIGH Voltage	T_A = 0°C	−1020			mV	V_{IN} = V_{IH} (Min) or V_{IL} (Max)
		T_A = +25°C	−980			mV	
		T_A = +75°C	−920			mV	
V_{OLC}	Output LOW Voltage	T_A = 0°C			−1645	mV	V_{IN} = V_{IH} (Min) or V_{IL} (Max)
		T_A = +25°C			−1630	mV	
		T_A = +75°C			−1605	mV	
							Loading with 50Ω to −2.0V
V_{IH}	Input HIGH Voltage		−1165		−880	mV	Guaranteed HIGH Signal for All Inputs
V_{IL}	Input LOW Voltage		−1810		−1490	mV	Guaranteed LOW Signal for All Inputs
I_{IH}	Input HIGH Current				290		V_{IN} = V_{IH} (Max)
I_{IL}	Input LOW Current		0.50			μA	V_{IN} = V_{IL} (Min)
I_{EE}	V_{EE} Supply Current		−125	−90	−50	mA	Inputs Open

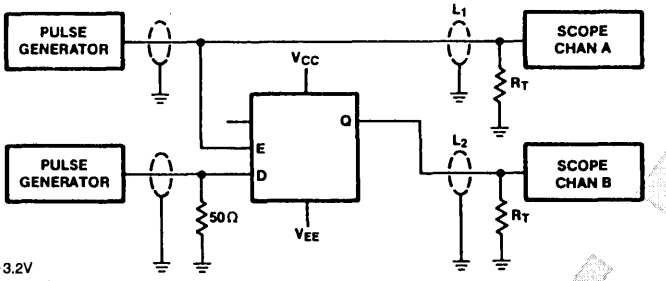
Note 1: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 2: The specified limits shown in the DC Characteristics can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining transverse air flow of 2.5 meters/s (500 linear feet/min) over the device either mounted in the test socket or on the printed circuit board. Test voltage values are given in the DC Operating Conditions and defined in *Figure 4.*

AC Electrical Characteristics

V_{EE} = −5.2V ±10%, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_A = 0°C		T_A = +25°C		T_A = +75°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PDLH} t_{PDHL}	Propagation Delay Data to Output	1.10	2.60	1.10	2.75	1.10	3.00	ns	*Figures 1 & 2*
t_{PDLH} t_{PDHL}	Propagation Delay Enable to Output	1.20	3.40	1.20	3.50	1.20	3.75	ns	*Figures 1 & 3*
t_{PDHL}	Propagation Delay Clear to Output	1.30	3.20	1.30	3.20	1.30	3.20	ns	*Figures 1, 3 & 4*
t_S	Setup Time D_0–D_4		2.50		2.50		2.50	ns	*Figures 1 & 5*
t_H	Hold Time D_0–D_4		0.50		0.50		0.50	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	1.10	3.25	1.20	3.25	1.20	3.50	ns	*Figures 1, 2, 3 & 4*

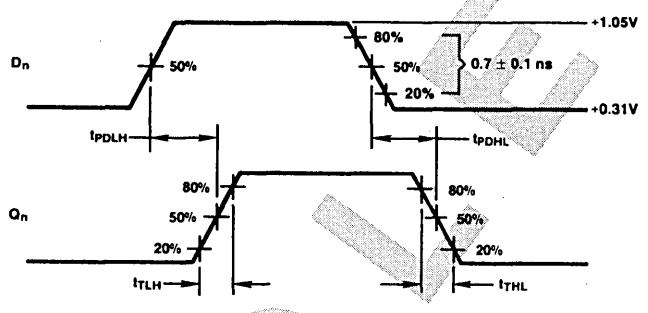


TL/F/9870–4

Notes:

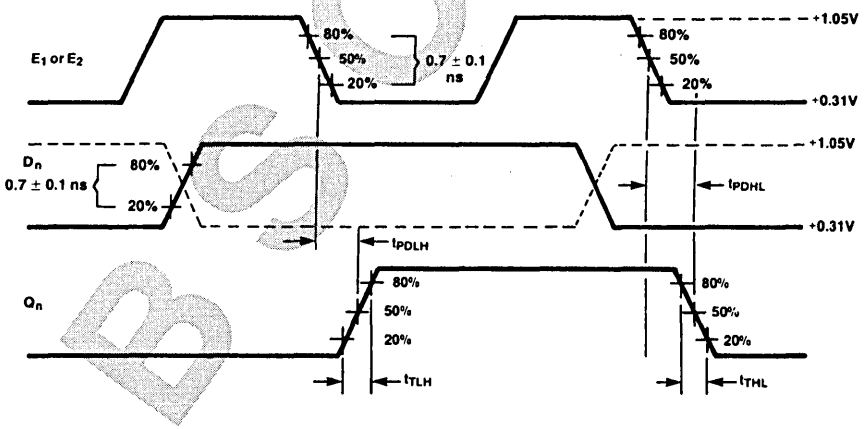
V_{CC}, V_{CCA} = +2V, V_{EE} = −3.2V
L1 and L2 = equal length 50Ω impedance lines
R_T = 50Ω terminator internal to scope
Decoupling 0.1 μf from GND to V_{CC} and V_{EE}
All unused outputs are loaded with 50Ω to GND
C_L = Fixture and stray capacitance ≤ 3 pF

FIGURE 1. AC Test Circuit



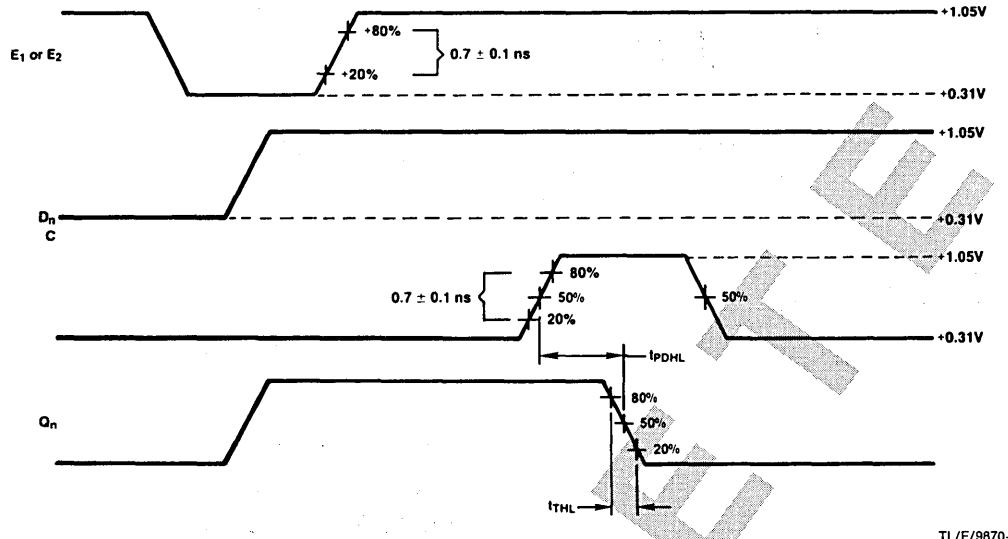
TL/F/9870–5

FIGURE 2. Data Propagation Delay @ T_A = +25°C



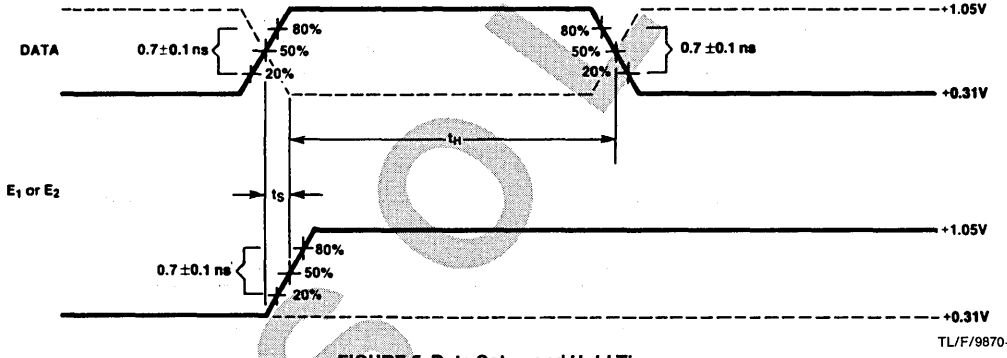
TL/F/9870–6

FIGURE 3. Enable Propagation Delay @ T_A = +25°C



TL/F/9870–7

FIGURE 4. Clear Propagation Delay @ $T_A = +25°C$



TL/F/9870–8

FIGURE 5. Data Setup and Hold Time

National Semiconductor

Not Intended For New Designs

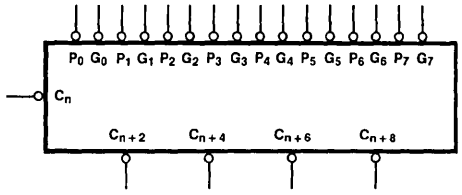
100179
Carry Lookahead Generator

General Description

The 100179 is a high-speed Carry Lookahead Generator intended for use with the 100180 6-bit fast Adder and the 100181 4-bit ALU. All inputs have 50 kΩ pulldown resistors.

Ordering Code: See Section 6

Logic Symbol

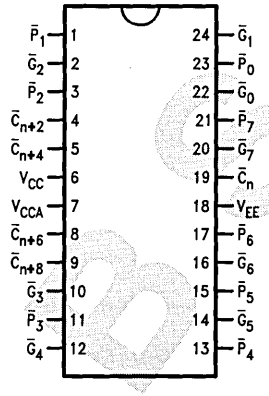


TL/F/9871–3

Pin Names	Description
$\overline{C}_n$	Carry Input (Active LOW)
$\overline{P}_0$–$\overline{P}_7$	Carry Propogate Inputs (Active LOW)
$\overline{G}_0$–$\overline{G}_7$	Carry Generate Inputs (Active LOW)
$\overline{C}_n + 2$, $\overline{C}_n + 4$ $\overline{C}_n + 6$, $\overline{C}_n + 8$	Carry Outputs

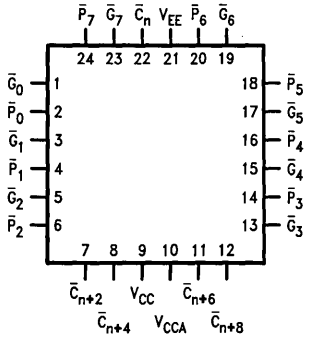
Connection Diagrams

24-Pin DIP



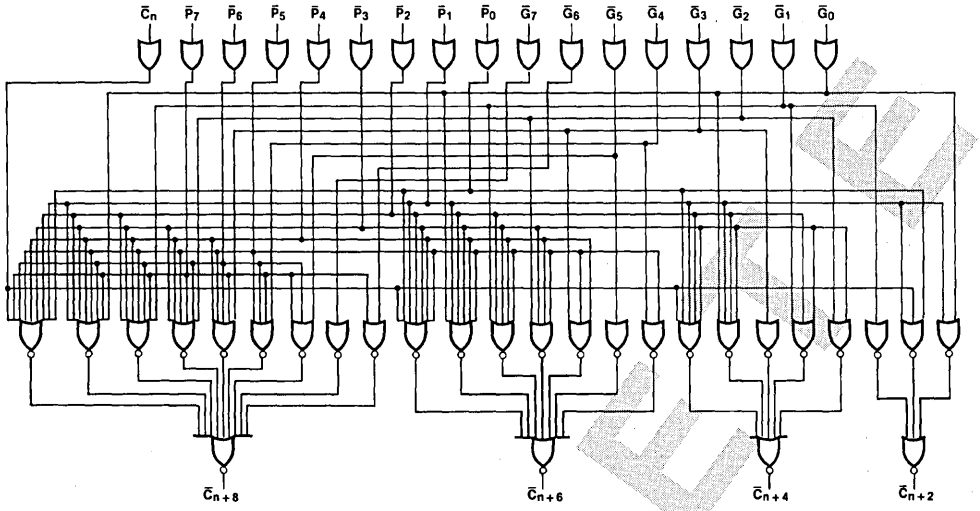
TL/F/9871–1

24-Pin Quad Cerpak



TL/F/9871–2

Logic Diagram



TL/F/9871–5

Truth Tables

$\overline{C}_{n+2}$ Output

Inputs					Output
$\overline{C}_n$	$\overline{G}_0$	$\overline{P}_0$	$\overline{G}_1$	$\overline{P}_1$	$\overline{C}_{n+2}$
X	X	X	L	X	L
X	L	X	X	L	L
L	X	L	X	L	L
All other combinations					H

$\overline{C}_{n+2} = \overline{G}_1 \bullet (\overline{P}_1 + \overline{G}_0) \bullet (\overline{P}_1 + \overline{P}_0 + \overline{C}_n)$

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

$\overline{C}_{n+4}$ Output

Inputs									Output
$\overline{C}_n$	$\overline{G}_0$	$\overline{P}_0$	$\overline{G}_1$	$\overline{P}_1$	$\overline{G}_2$	$\overline{P}_2$	$\overline{G}_3$	$\overline{P}_3$	$\overline{C}_{n+4}$
X	X	X	X	X	X	X	L	X	L
X	X	X	X	X	L	X	X	L	L
X	X	X	L	X	X	L	X	L	L
X	L	X	X	L	X	L	X	L	L
L	X	L	X	L	X	L	X	L	L
All other combinations									H

$\overline{C}_{n+4} = \overline{G}_3 \bullet (\overline{P}_3 + \overline{G}_2) \bullet (\overline{P}_3 + \overline{P}_2 + \overline{G}_1) \bullet (\overline{P}_3 + \overline{P}_2 + \overline{P}_1 + \overline{G}_0)$
$\bullet (\overline{P}_3 + \overline{P}_2 + \overline{P}_1 + \overline{P}_0 + \overline{C}_n)$

Truth Tables (Continued)

$\overline{C}_{n+6}$ Output

Inputs												Output
$\overline{C}_n$	$\overline{G}_0$	$\overline{P}_0$	$\overline{G}_1$	$\overline{P}_1$	$\overline{G}_2$	$\overline{G}_2$	$\overline{G}_3$	$\overline{P}_3$	$\overline{G}_4$	$\overline{P}_4$	$\overline{G}_5$	$\overline{P}_5$	$\overline{C}_{n+6}$
X	X	X	X	X	X	X	X	X	X	X	L	X	L
X	X	X	X	X	X	X	X	X	L	X	X	L	L
X	X	X	X	X	X	X	L	X	X	L	X	L	L
X	X	X	X	X	L	X	X	L	X	L	X	L	L
X	X	X	L	X	X	L	X	L	X	L	X	L	L
X	L	X	X	L	X	L	X	L	X	L	X	L	L
L	X	L	X	L	X	L	X	L	X	L	X	L	L
All other combinations													H

$\overline{C}_{n+6} = \overline{G}_5 \bullet (\overline{P}_5 + \overline{G}_4) \bullet (\overline{P}_5 + \overline{P}_4 + \overline{G}_3) \bullet (\overline{P}_5 + \overline{P}_4 + \overline{P}_3 + \overline{G}_2)$
$\bullet (\overline{P}_5 + \overline{P}_4 + \overline{P}_3 + \overline{P}_2 + \overline{G}_1) \bullet (\overline{P}_5 + \overline{P}_4 + \overline{P}_3 + \overline{P}_2 + \overline{P}_1 + \overline{G}_0)$
$\bullet (\overline{P}_5 + \overline{P}_4 + \overline{P}_3 + \overline{P}_2 + \overline{P}_1 + \overline{P}_0 + \overline{C}_n)$

$\overline{C}_{n+8}$ Output

Inputs																Output
$\overline{C}_n$	$\overline{G}_0$	$\overline{P}_0$	$\overline{G}_1$	$\overline{P}_1$	$\overline{G}_2$	$\overline{P}_2$	$\overline{G}_3$	$\overline{P}_3$	$\overline{G}_4$	$\overline{P}_4$	$\overline{G}_5$	$\overline{P}_5$	$\overline{G}_6$	$\overline{P}_6$	$\overline{G}_7$	$\overline{P}_7$	$\overline{C}_{n+8}$
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	L	X	L
X	X	X	X	X	X	X	X	X	X	X	X	X	L	X	X	L	L
X	X	X	X	X	X	X	X	X	X	X	L	X	X	L	X	L	L
X	X	X	X	X	X	X	X	X	L	X	X	L	X	L	X	L	L
X	X	X	X	X	X	X	L	X	X	L	X	L	X	L	X	L	L
X	X	X	X	X	L	X	X	L	X	L	X	L	X	L	X	L	L
X	X	X	L	X	X	L	X	L	X	L	X	L	X	L	X	L	L
X	L	X	X	L	X	L	X	L	X	L	X	L	X	L	X	L	L
L	X	L	X	L	X	L	X	L	X	L	X	L	X	L	X	L	L
All other combinations																	H

$\overline{C}_{n+8} = \overline{G}_7 \bullet (\overline{P}_7 + \overline{G}_6) \bullet (\overline{P}_7 + \overline{P}_6 + \overline{G}_5) \bullet (\overline{P}_7 + \overline{P}_6 + \overline{P}_5 + \overline{G}_4)$
$\bullet (\overline{P}_7 + \overline{P}_6 + \overline{P}_5 + \overline{P}_4 + \overline{G}_3) \bullet (\overline{P}_7 + \overline{P}_6 + \overline{P}_5 + \overline{P}_4 + \overline{P}_3 + \overline{G}_2)$
$\bullet (\overline{P}_7 + \overline{P}_6 + \overline{P}_5 + \overline{P}_4 + \overline{P}_3 + \overline{P}_2 + \overline{G}_1)$
$\bullet (\overline{P}_7 + \overline{P}_6 + \overline{P}_5 + \overline{P}_4 + \overline{P}_3 + \overline{P}_2 + \overline{P}_1 + \overline{G}_0)$
$\bullet (\overline{P}_7 + \overline{P}_6 + \overline{P}_5 + \overline{P}_4 + \overline{P}_3 + \overline{P}_2 + \overline{P}_1 + \overline{P}_0 + \overline{C}_n)$

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

Absolute Maximum Ratings

Above which the useful life may be impaired. (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Maximum Junction Temperature (T_J)	+150°C
Case Temperature under Bias (T_C)	0°C to +85°C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Output Current (DC Output HIGH)	−50 mA
Operating Range (Note 2)	−5.7V to −4.2V

DC Electrical Characteristics

V_{EE} = −4.5V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1025	−955	−880	mV	V_{IN} = V_{IH} (Max) or V_{IL} (Min)	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1810	−1705	−1620			
V_{OHC}	Output HIGH Voltage	−1035			mV	V_{IN} = V_{IH} (Min) or V_{IL} (Max)	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610			
V_{IH}	Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = V_{IL} (Min)	

DC Electrical Characteristics

V_{EE} = −4.2V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1020		−870	mV	V_{IN} = V_{IH} (Max) or V_{IL} (Min)	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1810		−1605			
V_{OHC}	Output HIGH Voltage	−1030			mV	V_{IN} = V_{IH} (Min) or V_{IL} (Max)	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1595			
V_{IH}	Input HIGH Voltage	−1150		−870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = V_{IL} (Min)	

DC Electrical Characteristics

V_{EE} = −4.8V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1035		−880	mV	V_{IN} = V_{IH} (Max) or V_{IL} (Min)	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830		−1620			
V_{OHC}	Output HIGH Voltage	−1045			mV	V_{IN} = V_{IH} (Min) or V_{IL} (Max)	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610			
V_{IH}	Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1830		−1490	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = V_{IL} (Min)	

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Parametric values specified at −4.2V to −4.8V.

Note 3: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 4: Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DC Electrical Characteristics

V_{EE} = −4.2V to −4.8V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C

Symbol	Parameter	Min	Typ	Max	Units	Conditions
I_{IH}	Input HIGH Current $\overline{C}_N$, $\overline{G}_0$–$\overline{G}_7$ $\overline{P}_0$–$\overline{P}_7$			 250 340	μA	V_{IN} = $V_{IH\ (Max)}$
I_{EE}	Power Supply Current	−220	−150	−100	mA	Inputs Open

Ceramic Dual-In-Line Package AC Electrical Characteristics

V_{EE} = −4.2V to −4.8V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay $\overline{C}_n$, $\overline{G}_0$–$\overline{G}_7$, $\overline{P}_0$–$\overline{P}_7$ to $\overline{C}_{n+x}$	1.10	2.90	1.10	2.90	1.10	3.00	ns	*Figures 1* and *2*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.80	0.45	1.80	0.45	1.80	ns	

Cerpak AC Electrical Characteristics

V_{EE} = −4.2V to −4.8V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay $\overline{C}_n$, $\overline{G}_0$–$\overline{G}_7$, $\overline{P}_0$–$\overline{P}_7$ to $\overline{C}_{n+x}$	1.10	2.70	1.10	2.70	1.10	2.80	ns	*Figures 1* and *2*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.70	0.45	1.70	0.45	1.70	ns	

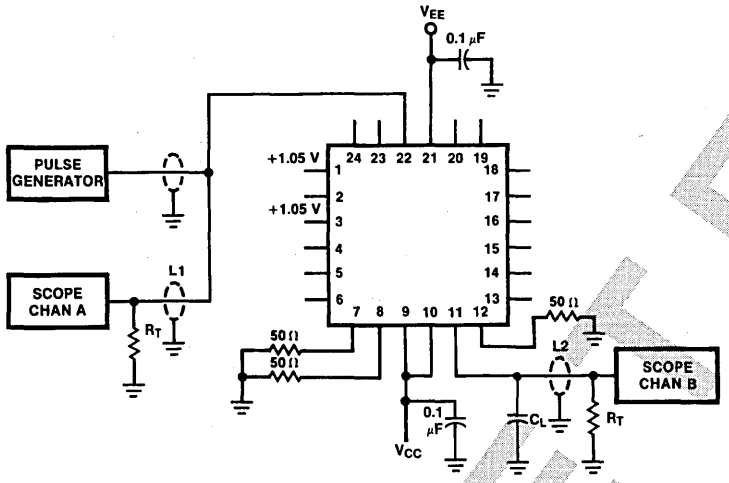


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FIGURE 1. AC Test Circuit

Notes:

V_{CC}, V_{CCA} = +2V, V_{EE} = −2.5V
L1 and L2 = equal length 50Ω impedance lines
R_T = 50Ω terminator internal to scope
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
All unused outputs are loaded with 50Ω to GND
C_L = Fixture and stray capacitance ≤ 3 pF
Pin numbers shown are for flatpak; for DIP see logic symbol

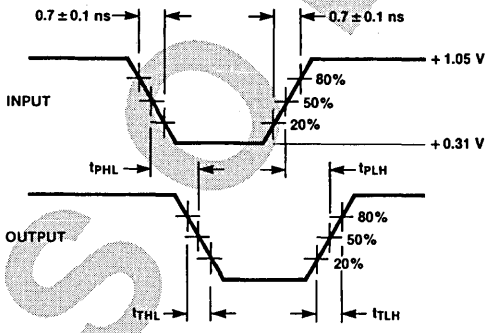

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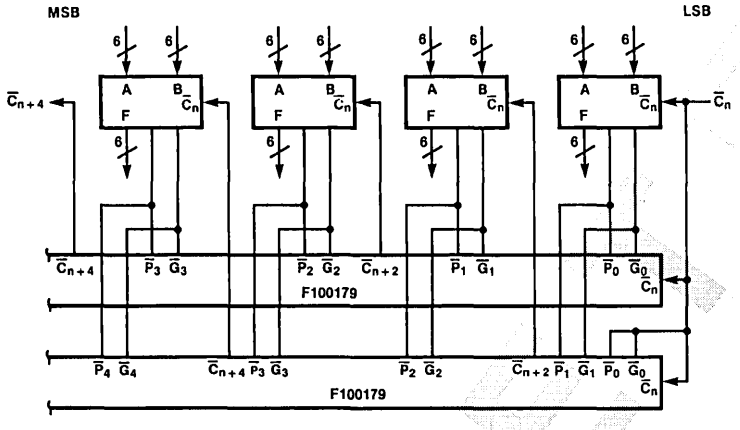
FIGURE 2. Propagation Delay and Transition Times

Applications

Fast Adder and Carry Lookahead



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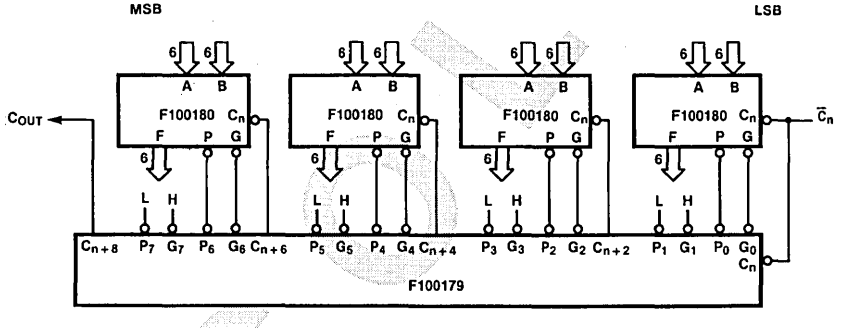
24-Bit Adder Using One Carry Lookahead



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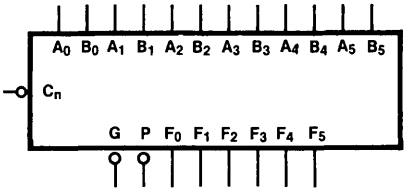
100180
High-Speed 6-Bit Adder

General Description

The 100180 is a high-speed 6-bit adder capable of performing a full 6-bit addition of two operands. Inputs for the adder are active-LOW Carry, Operand A, and Operand B; outputs are Function, active-LOW Carry Generate, and active-LOW Carry Propagate. When used with the 100179 Full Carry Lookahead as a second order lookahead block, the 100180 provides high-speed addition of very long words. All inputs have 50 kΩ pull-down resistors.

Ordering Code: See Section 6

Logic Symbol



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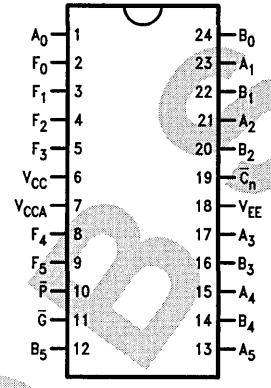
Pin Names	Description
A_0–A_5	Operand A Inputs
B_0–B_5	Operand B Inputs
$\overline{C}_n$	Carry Input (Active LOW)
$\overline{G}$	Carry Generate Output (Active LOW)
$\overline{P}$	Carry Propagate Output (Active LOW)
F_0–F_5	Function Outputs

Connection Diagrams

24-Pin DIP



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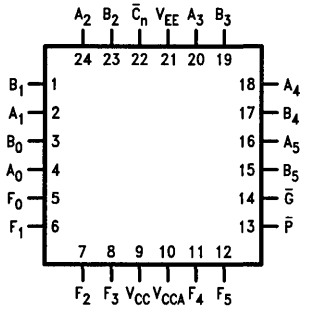
24-Pin Quad Cerpak



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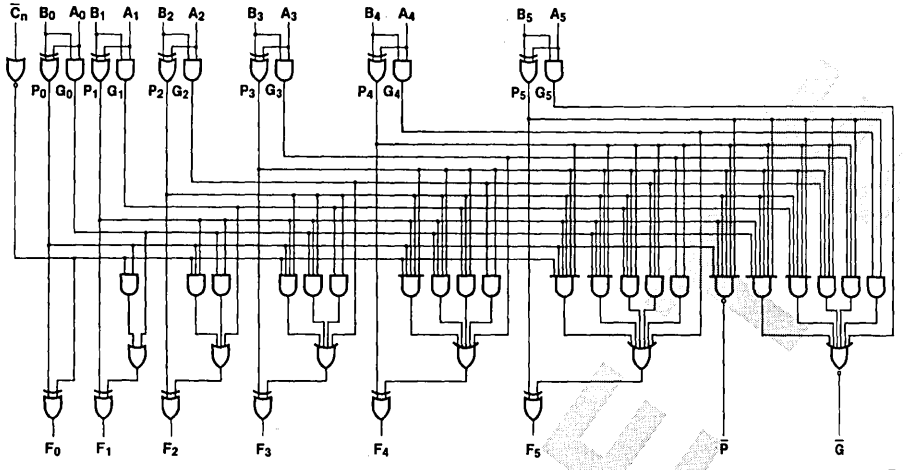
Logic Diagram



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Logic Equations

$P_i = A_i \oplus B_i$

$G_i = A_i B_i$

$i = 0, 1, 2, 3, 4, 5$

$F_0 = P_0 \oplus C_n$

$F_1 = P_1 \oplus (G_0 + P_0 C_n)$

$F_2 = P_2 \oplus (G_1 + P_1G_0 + P_1P_0C_n)$

$F_3 = P_3 \oplus (G_2 + P_2G_1 + P_2P_1G_0 + P_2P_1P_0C_n)$

$F_4 = P_4 \oplus (G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0 + P_3P_2P_1P_0C_n)$

$F_5 = P_5 \oplus (G_4 + P_4G_3 + P_4P_3G_2 + P_4P_3P_2G_1 + P_4P_3P_2P_1G_0 + P_4P_3P_2P_1P_0C_n)$

$\overline{P} = \overline{P_0P_1P_2P_3P_4P_5}$

$\overline{G} = \overline{G_5 + P_5G_4 + P_5P_4G_3 + P_5P_4G_3G_2 + P_5P_4P_3P_2G_1 + P_5P_4P_3P_2P_1G_0}$

Absolute Maximum Ratings

Above which the useful life may be impaired. (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Maximum Junction Temperature (T_J)	+150°C
Case Temperature under Bias (T_C)	0°C to +85°C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Output Current (DC Output HIGH)	−50 mA
Operating Range (Note 2)	−5.7V to −4.2V

DC Electrical Characteristics

V_{EE} = −4.5V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1025	−955	−880	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1810	−1705	−1620			
V_{OHC}	Output HIGH Voltage	−1035			mV	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610			
V_{IH}	Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

DC Electrical Characteristics

V_{EE} = −4.2V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1020		−870	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1810		−1605			
V_{OHC}	Output HIGH Voltage	−1030			mV	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1595			
V_{IH}	Input HIGH Voltage	−1150		−870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

DC Electrical Characteristics

V_{EE} = −4.8V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1035		−880	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830		−1620			
V_{OHC}	Output HIGH Voltage	−1045			mV	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610			
V_{IH}	Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1830		−1490	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Parametric values specified at −4.2V to −4.8V.

Note 3: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 4: Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DC Electrical Characteristics

V_{EE} = −4.2V to −4.8V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C

Symbol	Parameter	Min	Typ	Max	Units	Conditions
I_{IH}	Input HIGH Current All Inputs			220	μA	V_{IN} = $V_{IH\ (Max)}$
I_{EE}	Power Supply Current	−290	−195	−135	mA	Inputs Open

Ceramic Dual-In-Line Package AC Electrical Characteristics

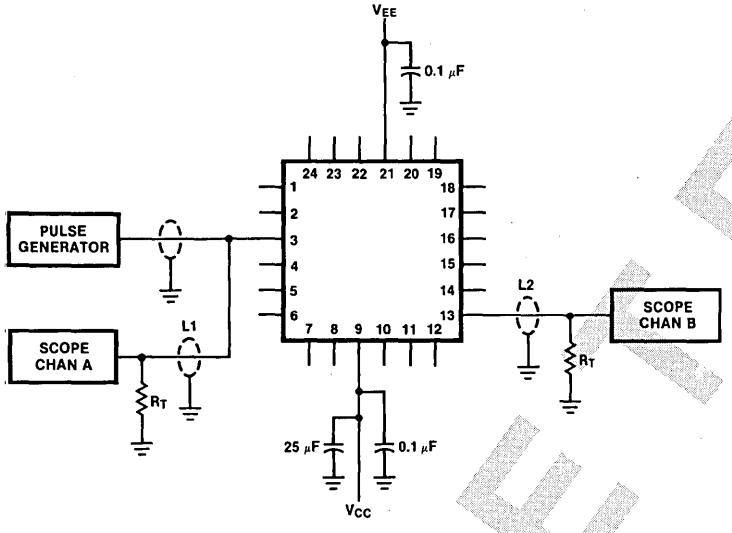
V_{EE} = −4.2V to −4.8V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay A_n, B_n to F_n	1.10	4.70	1.10	4.60	1.10	4.70	ns	
t_{PLH} t_{PHL}	Propagation Delay A_n, B_n to $\overline{P}$	1.00	3.00	1.00	3.00	1.00	3.30	ns	
t_{PLH} t_{PHL}	Propagation Delay A_n, B_n to $\overline{G}$	1.40	3.90	1.40	3.80	1.40	3.90	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay $\overline{C}_n$ to F_n	1.10	4.00	1.10	3.90	1.10	4.00	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	2.40	0.45	2.30	0.45	2.40	ns	

Cerpak AC Electrical Characteristics

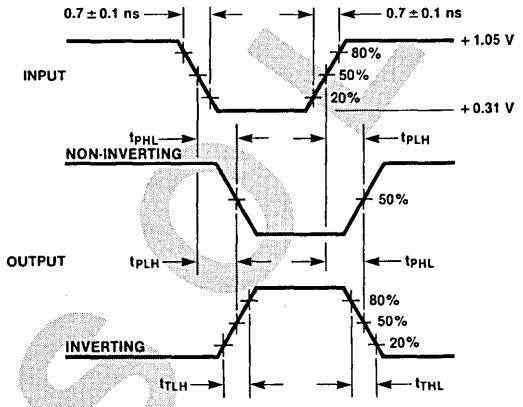
V_{EE} = −4.2V to −4.8V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay A_n, B_n to F_n	1.10	4.50	1.10	4.40	1.10	4.50	ns	
t_{PLH} t_{PHL}	Propagation Delay A_n, B_n to $\overline{P}$	1.00	2.80	1.00	2.80	1.00	3.10	ns	
t_{PLH} t_{PHL}	Propagation Delay A_n, B_n to $\overline{G}$	1.40	3.70	1.40	3.60	1.40	3.70	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay $\overline{C}_n$ to F_n	1.10	3.80	1.10	3.70	1.10	3.80	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	2.30	0.45	2.20	0.45	2.30	ns	



TL/F/9872–6

FIGURE 1. AC Test Circuit



TL/F/9872–7

FIGURE 2. Propagation Delay and Transition Times

Notes:

V_{CC}, V_{CCA} = +2V, V_{EE} = −2.5V

L1 and L2 = equal length 50Ω impedance lines

R_T = 50Ω terminator internal to scope

Decoupling 0.1 μF from GND to V_{CC} and V_{EE}

All unused outputs are loaded with 50Ω to GND

C_L = Fixture and stray capacitance ≤ 3 pF

Pin numbers shown are for flatpak; for DIP see logic symbol

National Semiconductor

Not Intended For New Designs

100181
4-Bit Binary/BCD Arithmetic Logic Unit

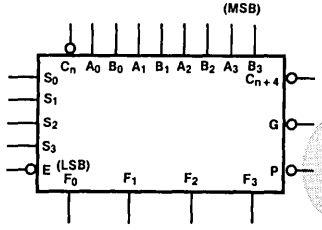
General Description

The 100181 performs eight logic operations and eight arithmetic operations on a pair of 4-bit words. The operating mode is determined by signals applied to the Select (S_n) inputs, as shown in the Function Select table. In addition to performing binary arithmetic, the circuit contains the necessary correction logic to perform BCD addition and subtraction. Output latches are provided to reduce overall package count and increase system operating speed. When the latches are not required, leaving the Enable ($\overline{E}$) input LOW makes the latches transparent.

The circuit uses internal lookahead carry to minimize delay to the F_n outputs and to the ripple Carry output, $\overline{C}_{n+4}$. Group Carry Lookahead Propagate ($\overline{P}$) and Generate ($\overline{G}$) outputs are also provided, which are independent of the Carry input $\overline{C}_n$. The $\overline{P}$ output goes LOW when a plus operation produces fifteen (nine for BCD) or when a minus operation produces zero. Similarly, $\overline{G}$ goes LOW when the sum of A and B is greater than fifteen (nine for BCD) in a plus mode, or when their difference is greater than zero in a minus mode. All inputs have 50 kΩ pull-down resistors.

Ordering Code: See Section 6

Logic Symbol

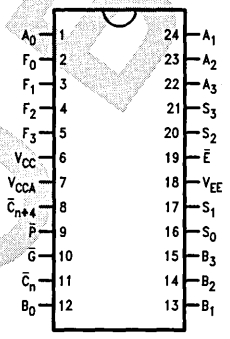


TL/F/9873–4

Pin Names	Description
A_0–A_3	Word A Operand Inputs
B_0–B_3	Word B Operand Inputs
$\overline{C}_n$	Carry Input (Active LOW)
S_0–S_3	Function Select Inputs
$\overline{E}$	Latch Enable Input (Active LOW)
$\overline{P}$	Carry Lookahead Propagate Output (Active LOW)
$\overline{G}$	Carry Lookahead Generate Output (Active LOW)
$\overline{C}_{n+4}$	Carry Output
F_0–F_3	Function Outputs

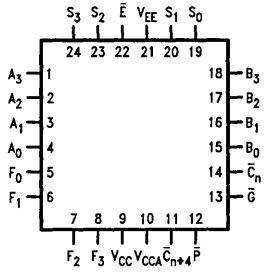
Connection Diagrams

24-Pin DIP



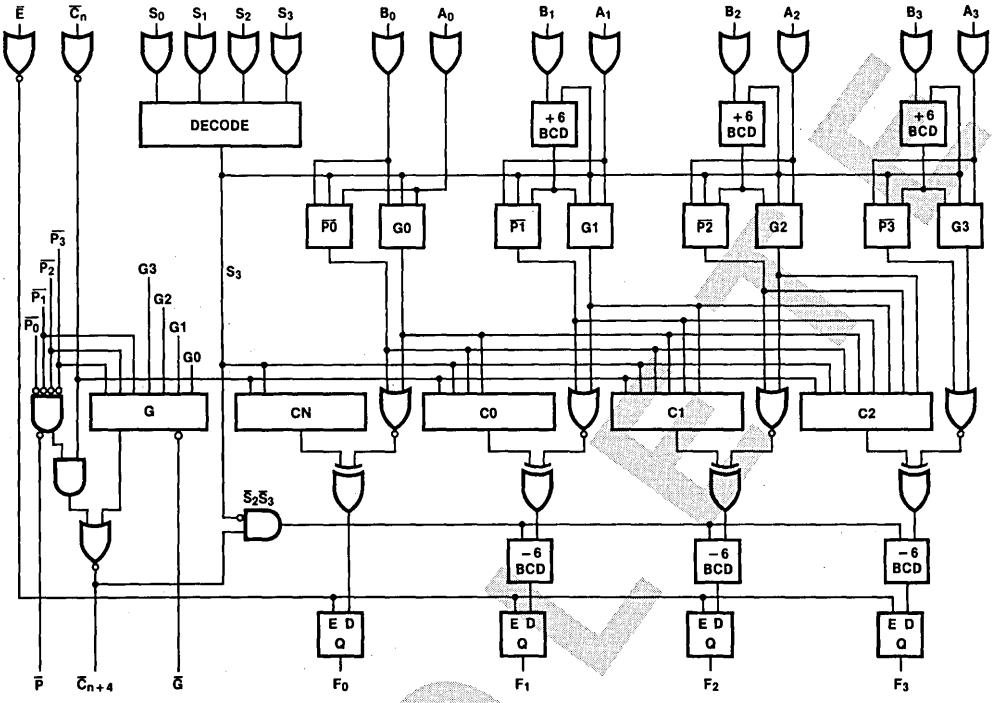
TL/F/9873–1

24-Pin Quad Cerpak



TL/F/9873–2

Logic Diagram



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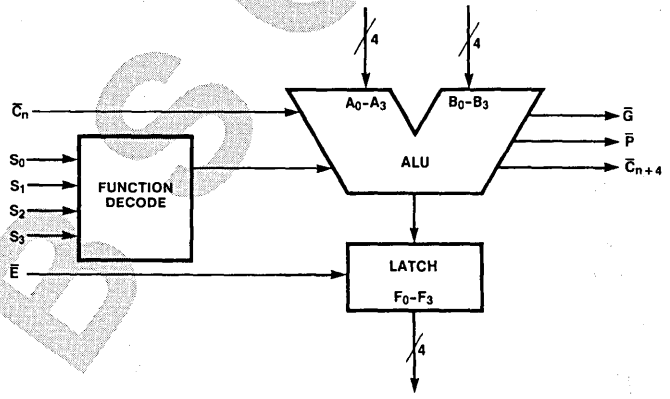
Block Diagram



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Functional Description

There are two modes of operation: Arithmetic and Logic. The S_3 input controls these two modes:

S_3 = LOW for Arithmetic mode

S_3 = HIGH for Logic mode

The arithmetic mode includes decimal and binary arithmetic operations. S_2 is the control input: with S_3 = LOW,

S_2 = LOW for Decimal Arithmetic (BCD)

S_2 = HIGH for Binary Arithmetic

DECIMAL ARITHMETIC OPERATION

Addition

F = A plus B plus C_n. Arguments A and B are directly applied to the inputs. The circuit automatically performs the "+6" and "−6" logic correction internally.

Subtraction

F = A minus B plus C_n. Arguments A and B are directly applied to the inputs. The circuit automatically takes the nines complement of B and adds "+6". A "−6" adjustment is made if the subtraction algorithm calls for it. If there is a carry out, the result is a positive number. With no carry out, the result is a negative number expressed in its nines complement form. Therefore, to perform a subtraction with results in the tens complement form, an initial carry should be forced into the lowest order bit, i.e., set $\overline{C}_n$ = LOW.

(tens complement of B) = (nines complement of B) + 1

F = B minus A plus C_n. Operation is similar to and results are the same as F = A minus B plus C_n.

BINARY ARITHMETIC OPERATION

Addition

F = A minus B plus C_n. Arguments A and B are directly applied to the inputs.

Subtraction

F = A minus B plus C_n. Arguments A and B are directly applied to the inputs. The circuit automatically takes the ones complement of B (by inverting B internally). If there is a carry out the result is a positive number. With no carry out, the result is a negative number expressed in its ones complement form. Therefore, to perform a subtraction with results in the twos complement form, an initial carry should forced into the lowest order bit, i.e., set $\overline{C}_n$ = LOW.

(twos complement of B) = (ones complement of B) + 1

F = B minus A plus C_n. Operation is similar and results are the same as F = A minus B plus C_n.

Function Table

S_3	S_2	S_1	S_0	F_n Function	G_n (n = 0 to 3)	P_n (n = 0 to 3)	Outputs		
					Internal Signals		$\overline{C}_{n+4}$	$\overline{G}$	$\overline{P}$
L	L	L	L	F_n = A plus B plus C_n (BCD)	A_nD_n	$A_n + D_n$	$\overline{C}_{n+4}$	$\overline{G}$	$\overline{P}$
L	L	L	H	F_n = A minus B plus C_n (BCD)	$A_n\overline{B}_n$	$A_n + \overline{B}_n$	$\overline{C}_{n+4}$	$\overline{G}$	$\overline{P}$
L	L	H	L	F_n = B minus A plus C_n (BCD)	$\overline{A}_nB_n$	$\overline{A}_n + B_n$	$\overline{C}_{n+4}$	$\overline{G}$	$\overline{P}$
L	L	H	H	F_n = 0 minus B plus C_n (BCD)	L	$\overline{B}_n$	$\overline{C}_{n+4}$	H	$\overline{P}$
L	H	L	L	F_n = A plus B plus C_n (Binary)	A_nB_n	$A_n + B_n$	$\overline{C}_{n+4}$	$\overline{G}$	$\overline{P}$
L	H	L	H	F_n = A minus B plus C_n (Binary)	$A_n\overline{B}_n$	$A_n + \overline{B}_n$	$\overline{C}_{n+4}$	$\overline{G}$	$\overline{P}$
L	H	H	L	F_n = B minus A plus C_n (Binary)	$\overline{A}_nB_n$	$\overline{A}_n + B_n$	$\overline{C}_{n+4}$	$\overline{G}$	$\overline{P}$
L	H	H	H	F_n = 0 minus B plus C_n (Binary)	L	$\overline{B}_n$	$\overline{C}_{n+4}$	H	$\overline{P}$
H	L	L	L	$F_n = A_nB_n + \overline{A}_n\overline{B}_n$	A_nB_n	$A_n + B_n$	$\overline{C}_{n+4}$	$\overline{G}$	$\overline{P}$
H	L	L	H	$F_n = A_n\overline{B}_n + \overline{A}_nB_n$	$A_n\overline{B}_n$	$A_n + \overline{B}_n$	$\overline{C}_{n+4}$	$\overline{G}$	$\overline{P}$
H	L	H	L	$F_n = A_n + B_n$	A_n	$\overline{B}_n$	$\overline{C}_{n+4}$	$\overline{G}_x$	$\overline{P}$
H	L	H	H	$F_n = A_n$	A_n	H	$\overline{C}_{n+4}$	$\overline{G}$	L
H	H	L	L	$F_n = \overline{B}_n$	L	B_n	$\overline{C}_{n+4}$	H	$\overline{P}$
H	H	L	H	$F_n = B_n$	L	$\overline{B}_n$	$\overline{C}_{n+4}$	H	$\overline{P}$
H	H	H	L	$F_n = A_nB_n$	L	$\overline{A}_n + \overline{B}_n$	$\overline{C}_{n+4}$	H	$\overline{P}$
H	H	H	H	F_n = LOW	L	H	$\overline{C}_n$	H	L

H = HIGH Voltage Level

L = LOW Voltage Level

$\overline{P} = \overline{P}_0 + \overline{P}_1 + \overline{P}_2 + \overline{P}_3$

$\overline{G} = \overline{G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0}$

$\overline{C}_{n+4} = \overline{G} \bullet (\overline{P} + \overline{C}_n)$

Arithmetic Operations

$F_n = \overline{G_n + \overline{P}_n} \oplus C_i \quad i = 0 \text{ to } 3$

Logic Operations

$F_n = G_n + \overline{P}_n$

Internal Equations for Carry Lookahead

(i = 0, 1, 2, 3)

$C_0 = C_n + S_3$

$C_1 = G_0 + P_0C_n + S_3$

$C_2 = G_1 + P_1G_0 + P_1P_0C_n + S_3$

$C_3 = G_2 + P_2G_1 + P_2P_1G_0 + P_2P_1P_0C_n + S_3$

Internal Equations for +6 Logic

$D_0 = B_0$

$D_1 = \overline{B}_1$

$D_2 = B_1B_2 + \overline{B}_1\overline{B}_2$

$D_3 = B_1 + B_2 + B_3$

$\overline{G}_x = \overline{G_3P_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0}$

Absolute Maximum Ratings

Above which the useful life may be impaired. (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Maximum Junction Temperature (T_J)	+150°C
Case Temperature under Bias (T_C)	0°C to +85°C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Output Current (DC Output HIGH)	−50 mA
Operating Range (Note 2)	−5.7V to −4.2V

DC Electrical Characteristics

V_{EE} = −4.5V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1025	−955	−880	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1810	−1705	−1620			
V_{OHC}	Output HIGH Voltage	−1035			mV	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610			
V_{IH}	Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

DC Electrical Characteristics

V_{EE} = −4.2V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1020		−870	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1810		−1605			
V_{OHC}	Output HIGH Voltage	−1030			mV	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1595			
V_{IH}	Input HIGH Voltage	−1150		−870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

DC Electrical Characteristics

V_{EE} = −4.8V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1035		−880	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830		−1620			
V_{OHC}	Output HIGH Voltage	−1045			mV	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610			
V_{IH}	Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1830		−1490	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Parametric values specified at −4.2V to −4.8V.

Note 3: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 4: Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DC Electrical Characteristics

V_{EE} = −4.2V to −4.8V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C

Symbol	Parameter	Min	Typ	Max	Units	Conditions
I_{IH}	Input HIGH Current S_n, $\overline{E}$ All Others			 350 250	μA	V_{IN} = $V_{IH\ (Max)}$
I_{EE}	Power Supply Current	−300	−210	−130	mA	Inputs Open

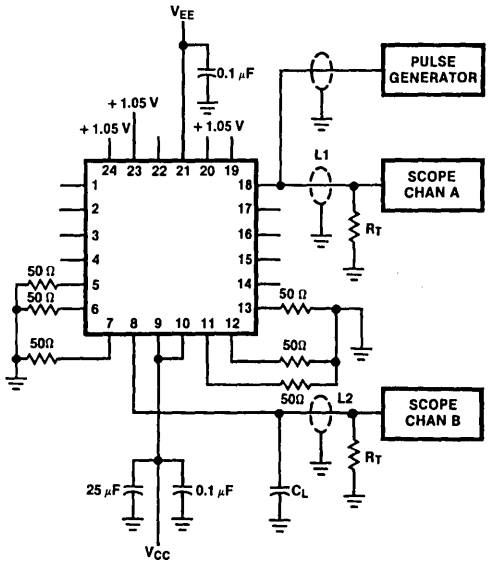
Ceramic Dual-In-Line Package AC Electrical Characteristics

V_{EE} = −4.2V to −4.8V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay A_n, B_n to F_n	2.00	6.90	2.10	6.80	2.30	7.40	ns	
t_{PLH} t_{PHL}	Propagation Delay A_n, B_n to $\overline{P}$, $\overline{G}$	1.40	4.70	1.40	4.40	1.40	4.70	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay A_n, B_n to $\overline{C}_{n+4}$	2.00	6.50	2.00	6.50	2.10	6.80	ns	
t_{PLH} t_{PHL}	Propagation Delay $\overline{C}_n$ to F_n	1.60	5.10	1.60	5.20	1.60	5.50	ns	
t_{PLH} t_{PHL}	Propagation Delay $\overline{C}_n$ to $\overline{C}_{n+4}$	1.30	3.00	1.40	3.00	1.40	3.10	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay S_n to F_n	1.40	8.80	1.50	8.60	1.50	9.00	ns	
t_{PLH} t_{PHL}	Propagation Delay S_n to $\overline{P}$, $\overline{G}$	1.70	7.40	2.00	5.90	2.00	6.50	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay S_n to $\overline{C}_{n+4}$	2.70	10.10	2.80	8.50	2.90	8.70	ns	
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to F_n	1.00	3.40	0.90	3.60	1.10	3.80	ns	*Figures 1* and *2*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	2.70	0.45	2.60	0.45	2.70	ns	*Figures 1* and *2*
t_s	Setup Time A_n, B_n S_n $\overline{C}_n$	 7.60 8.70 4.80		 7.60 8.50 5.00		 8.10 9.60 5.30		ns	*Figure 3*
t_h	Hold Time A_n, B_n S_n $\overline{C}_n$	 0.10 0.60 0.60		 0.10 0.60 0.60		 0.10 0.60 0.60		ns	
t_{pw}(L)	Pulse Width LOW $\overline{E}$	2.00		2.00		2.00		ns	*Figure 2*

Cerpak AC Electrical Characteristics $V_{EE} = -4.2V$ to $-4.8V$, $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_C = 0°C$		$T_C = +25°C$		$T_C = +85°C$		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay A_n, B_n to F_n	2.00	6.70	2.10	6.60	2.30	7.20	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay A_n, B_n to $\overline{P}$, $\overline{G}$	1.40	4.50	1.40	4.20	1.40	4.50	ns	
t_{PLH} t_{PHL}	Propagation Delay A_n, B_n to $\overline{C}_{n+4}$	2.00	6.30	2.00	6.30	2.10	6.60	ns	
t_{PLH} t_{PHL}	Propagation Delay $\overline{C}_n$ to F_n	1.60	4.90	1.60	5.00	1.60	5.30	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay $\overline{C}_n$ to $\overline{C}_{n+4}$	1.30	2.80	1.40	2.80	1.40	2.90	ns	
t_{PLH} t_{PHL}	Propagation Delay S_n to F_n	1.40	8.60	1.50	8.40	1.50	8.80	ns	
t_{PLH} t_{PHL}	Propagation Delay S_n to $\overline{P}$, $\overline{G}$	1.70	7.20	2.00	5.70	2.00	6.30	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay S_n to $\overline{C}_{n+4}$	2.70	9.90	2.80	8.30	2.90	8.50	ns	
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to F_n	1.00	3.20	0.90	3.40	1.10	3.60	ns	*Figures 1* and *2*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	2.60	0.45	2.50	0.45	2.60	ns	*Figures 1* and *2*
t_s	Setup Time A_n, B_n S_n $\overline{C}_n$	 7.50 8.60 4.70		 7.50 8.40 4.90		 8.00 9.50 5.20		ns	*Figure 3*
t_h	Hold Time A_n, B_n S_n $\overline{C}_n$	 0 0.50 0.50		 0 0.50 0.50		 0 0.50 0.50		ns	
$t_{pw}(L)$	Pulse Width LOW $\overline{E}$	2.00		2.00		2.00		ns	*Figure 2*



Notes:

V_{CC}, V_{CCA} = +2V, V_{EE} = −2.5V

L1 and L2 = equal length 50Ω impedance lines

R_T = 50Ω terminator internal to scope

Decoupling 0.1 μF from GND to V_{CC} and V_{EE}

All unused outputs are loaded with 50Ω to GND

C_L = Fixture and stray capacitance ≤ 3 pF

Pin numbers shown are for flatpak; for DIP see logic symbol

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FIGURE 1. AC Test Circuit

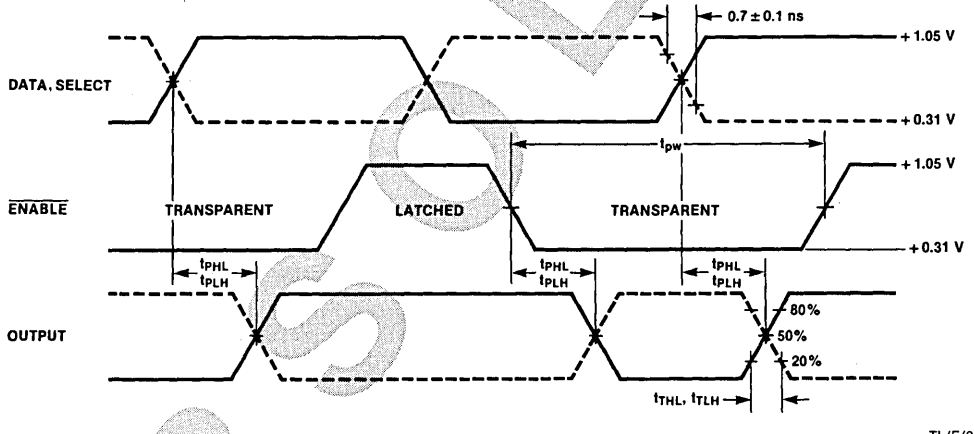

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FIGURE 2. Enable Timing

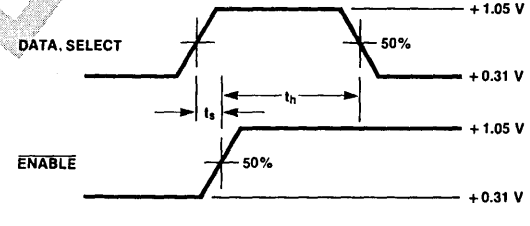

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FIGURE 3. Setup and Hold Times

Notes:

t_s is the minimum time before the transition of the enable that information must be present at the data input.

t_h is the minimum time after the transition of the enable that information must remain unchanged at the data input.

National Semiconductor

Not Intended For New Designs

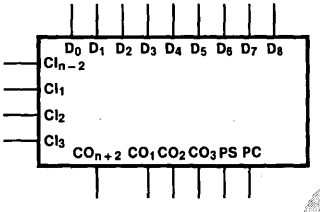
100182
9-Bit Wallace Tree Adder

General Description

The 100182 is a 9-bit Wallace tree adder. It is designed to assist in performing high-speed hardware multiplication. The device is designed to add 9 bits of data 1-bit-slice wide and handle the carry-ins from the previous slices. The 100182 is easily expanded and still maintains four levels of delay regardless of input string length. In conjunction with the 100183 Recode Multiplier, the 100179 Carry Lookahead, and the 100180 High-speed Adder, the 100182 assists in performing parallel multiplication of two signed numbers to produce a signed twos complement product. See 100183 data sheet for additional information. All inputs have 50 kΩ pull-down resistors.

Ordering Code: See Section 6

Logic Symbol

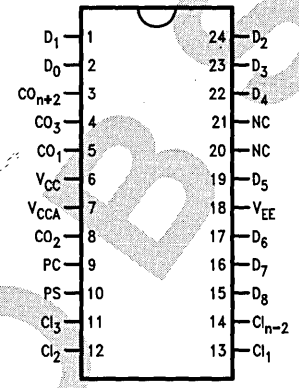


TL/F/9874–3

Pin Names	Description
D_0–D_8	Data Inputs
CI_1–CI_3, CI_{n-2}	Carry Inputs
CO_1–CO_3, CO_{n+2}	Carry Outputs
PS	Partial Sum Output
PC	Partial Carry Output

Connection Diagrams

24-Pin DIP



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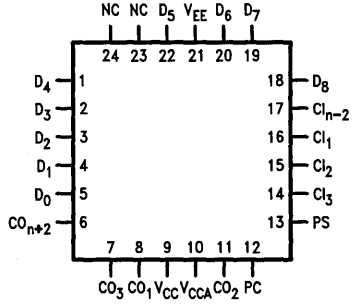
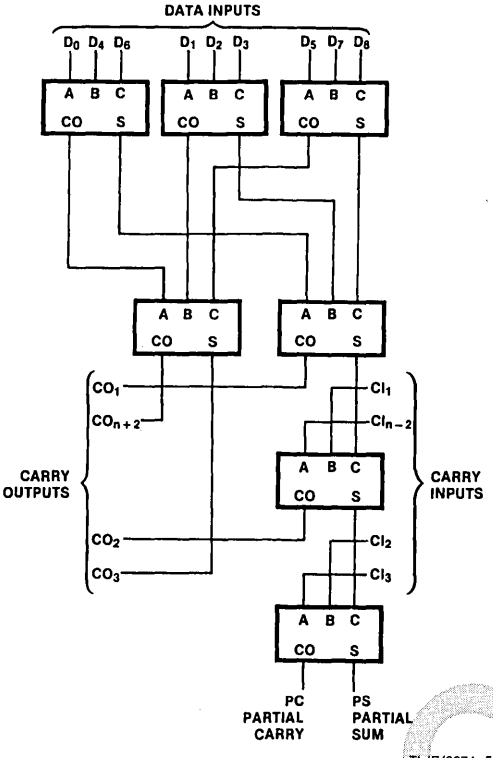
24-Pin Quad Cerpak



TL/F/9874–2

Logic Diagram



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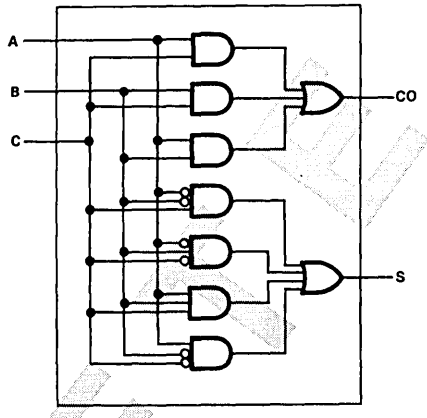
Adder Logic Diagram



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Adder Truth Table

Inputs			Outputs	
A	B	C	S	CO
L	L	L	L	L
L	L	H	H	L
L	H	L	H	L
L	H	H	L	H
H	L	L	H	L
H	L	H	L	H
H	H	L	L	H
H	H	H	H	H

Absolute Maximum Ratings

Above which the useful life may be impaired. (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Maximum Junction Temperature (T_J)	+150°C
Case Temperature under Bias (T_C)	0°C to +85°C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Output Current (DC Output HIGH)	−50 mA
Operating Range (Note 2)	−5.7V to −4.2V

DC Electrical Characteristics

V_{EE} = −4.5V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1025	−955	−880	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1810	−1705	−1620			
V_{OHC}	Output HIGH Voltage	−1035			mV	V_{IN} = $V_{IH(Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610			
V_{IH}	Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

DC Electrical Characteristics

V_{EE} = −4.2V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1020		−870	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1810		−1605			
V_{OHC}	Output HIGH Voltage	−1030			mV	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1595			
V_{IH}	Input HIGH Voltage	−1150		−870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

DC Electrical Characteristics

V_{EE} = −4.8V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1035		−880	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830		−1620			
V_{OHC}	Output HIGH Voltage	−1045			mV	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610			
V_{IH}	Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1830		−1490	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Parametric values specified at −4.2V to −4.8V.

Note 3: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 4: Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DC Electrical Characteristics

V_{EE} = −4.2V to −4.8V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C

Symbol	Parameter	Min	Typ	Max	Units	Conditions
I_{IH}	Input HIGH Current CI_1–CI_3, CI_{n-2} D_1, D_3, D_4, D_5, D_6, D_8			300	μA	V_{IN} = $V_{IH\ (Max)}$
	D_0, D_2, D_7			250		
I_{EE}	Power Supply Current	−260	−180	−125	mA	Inputs Open

Ceramic Dual-In-Line Package AC Electrical Characteristics

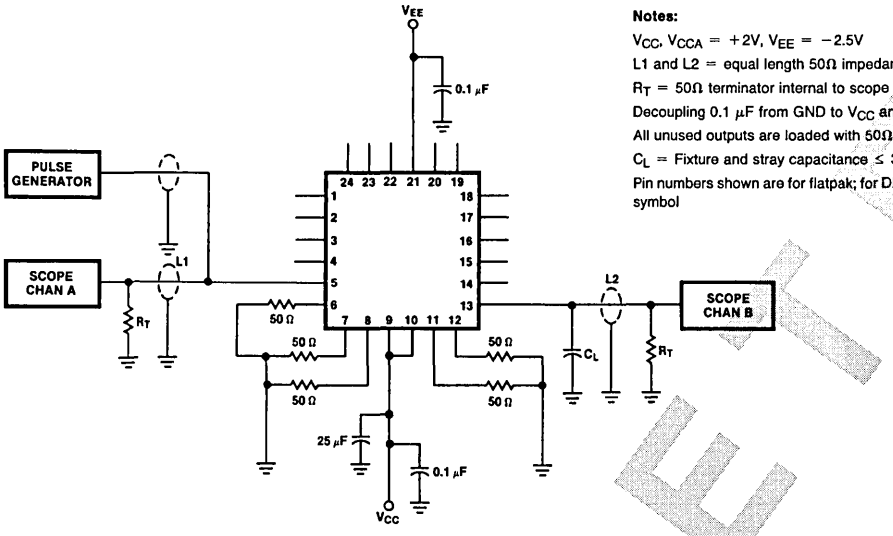
V_{EE} = −4.2V to −4.8V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay D_n to CO_{n+2}	1.40	4.50	1.40	4.50	1.50	4.70	ns	
t_{PLH} t_{PHL}	Propagation Delay D_n to CO_1	1.30	4.80	1.30	4.70	1.50	5.00	ns	
t_{PLH} t_{PHL}	Propagation Delay D_n to CO_2	2.20	6.20	2.20	6.10	2.30	6.40	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay D_n to CO_3	1.30	4.70	1.40	4.70	1.50	5.00	ns	
t_{PLH} t_{PHL}	Propagation Delay D_n to PS, PC	2.50	7.20	2.50	7.20	2.70	7.40	ns	
t_{PLH} t_{PHL}	Propagation Delay CI_{n-2}, CI_1 to CO_2	1.00	3.50	1.00	3.40	1.10	3.70	ns	
t_{PLH} t_{PHL}	Propagation Delay CI_{n-2}, CI_1 to PS, PC	1.50	4.50	1.50	4.45	1.60	4.60	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay CI_3, CI_2 to PS, PC	0.80	3.30	0.80	3.20	0.90	3.60	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.60	0.45	1.60	0.45	1.60	ns	*Figures 1* and *2*

Cerpak AC Electrical Characteristics

V_{EE} = −4.2V to −4.8V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay D_n to CO_{n+2}	1.40	4.30	1.40	4.30	1.50	4.50	ns	
t_{PLH} t_{PHL}	Propagation Delay D_n to CO_1	1.30	4.60	1.30	4.50	1.50	4.80	ns	
t_{PLH} t_{PHL}	Propagation Delay D_n to CO_2	2.20	6.00	2.20	5.90	2.30	6.20	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay D_n to CO_3	1.30	4.50	1.40	4.50	1.50	4.80	ns	
t_{PLH} t_{PHL}	Propagation Delay D_n to PS, PC	2.50	7.00	2.50	7.00	2.70	7.20	ns	
t_{PLH} t_{PHL}	Propagation Delay CI_{n-2}, CI_1 to CO_2	1.00	3.30	1.00	3.20	1.10	3.50	ns	
t_{PLH} t_{PHL}	Propagation Delay CI_{n-2}, CI_1 to PS, PC	1.50	4.30	1.50	4.25	1.60	4.40	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay CI_3, CI_2 to PS, PC	0.80	3.10	0.80	3.00	0.90	3.40	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.50	0.45	1.50	0.45	1.50	ns	*Figures 1* and *2*



Notes:

V_{CC}, V_{CCA} = +2V, V_{EE} = −2.5V

L1 and L2 = equal length 50Ω impedance lines

R_T = 50Ω terminator internal to scope

Decoupling 0.1 μF from GND to V_{CC} and V_{EE}

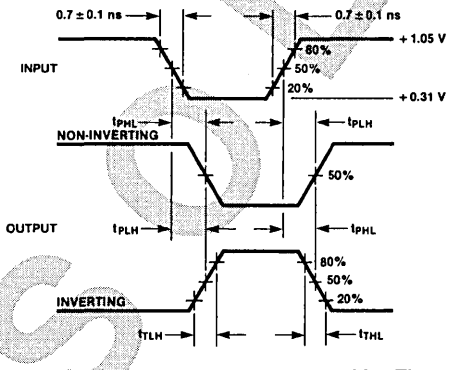
All unused outputs are loaded with 50Ω to GND

C_L = Fixture and stray capacitance ≤ 3 pF

Pin numbers shown are for flatpak; for DIP see logic symbol

TL/F/9874–7

FIGURE 1. AC Test Circuit

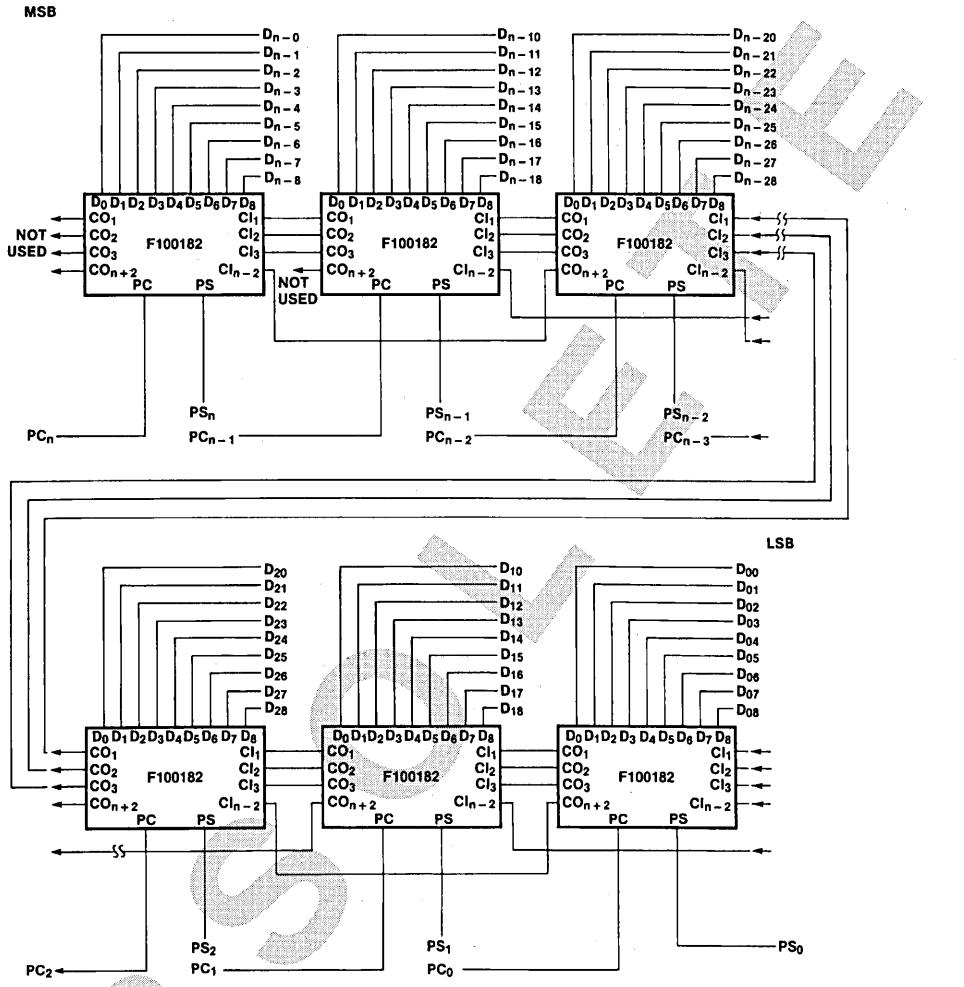


TL/F/9874–8

FIGURE 2. Propagation Delay and Transition Times

Application

Typical Horizontal Interconnection of 9-Bit Wallace Tree Adders F100182



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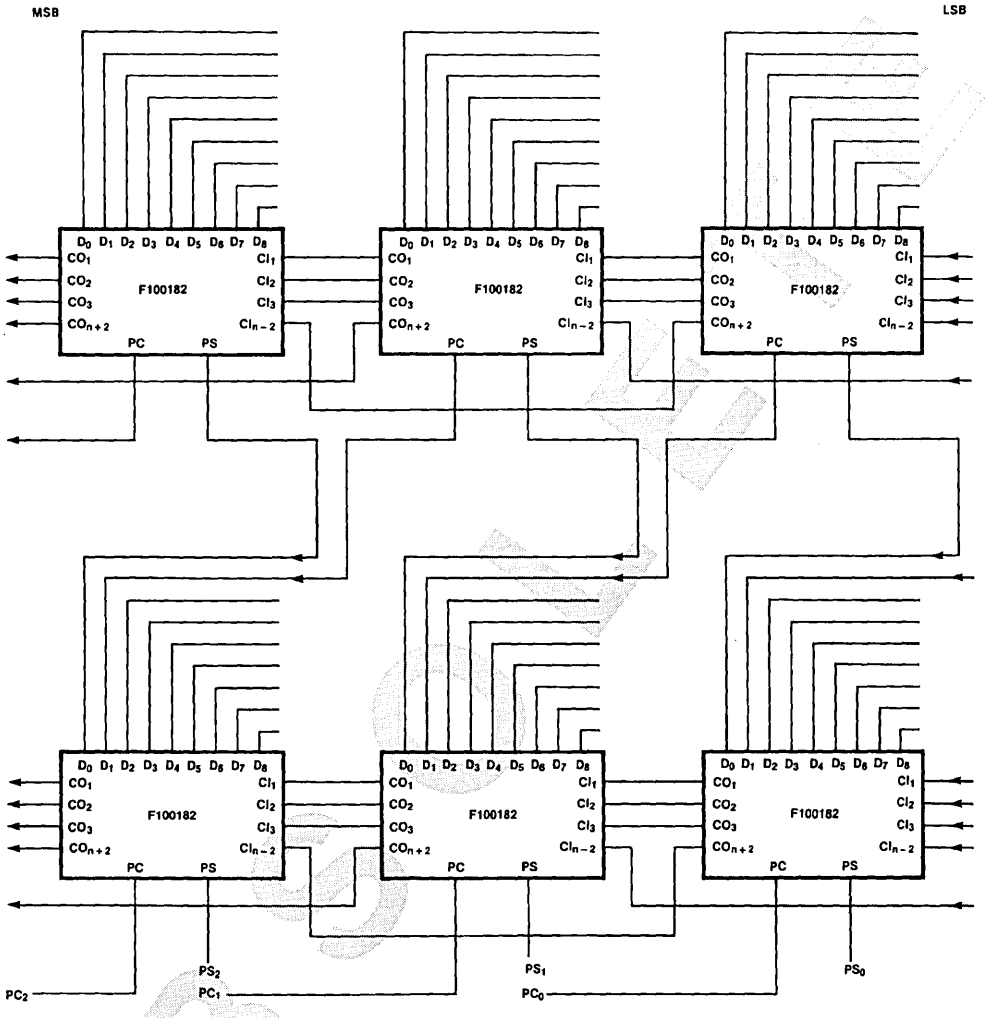
Application (Continued)

16-Bit Vertical Expansion of Wallace Tree Adders



TL/F/9874–10

National Semiconductor

Not Intended For New Designs

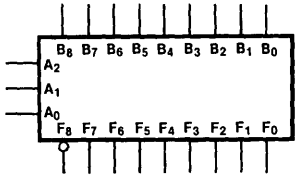
100183
2 x 8-Bit Recode Multiplier

General Description

The 100183 is a 2 x 8-bit recode multiplier designed to perform high-speed hardware multiplication. In conjunction with the 100182 Wallace Tree Adder, the 100179 Carry Lookahead, and the 100180 High-speed Adder, the 100183 performs parallel multiplication of two signed numbers in twos complement form to produce a signed twos complement product. All inputs have 50 kΩ pull-down resistors.

Ordering Code: See Section 6

Logic Symbol

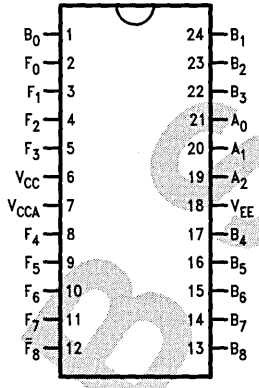


TL/F/9875–3

Pin Names	Description
A_0–A_2	Multiplier (Recode) Inputs
B_0–B_8	Multiplicand Inputs
F_0–F_7	Partial Product Outputs
$\overline{F}_8$	Sign Extension Output

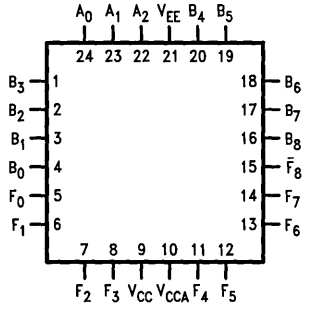
Connection Diagrams

24-Pin DIP



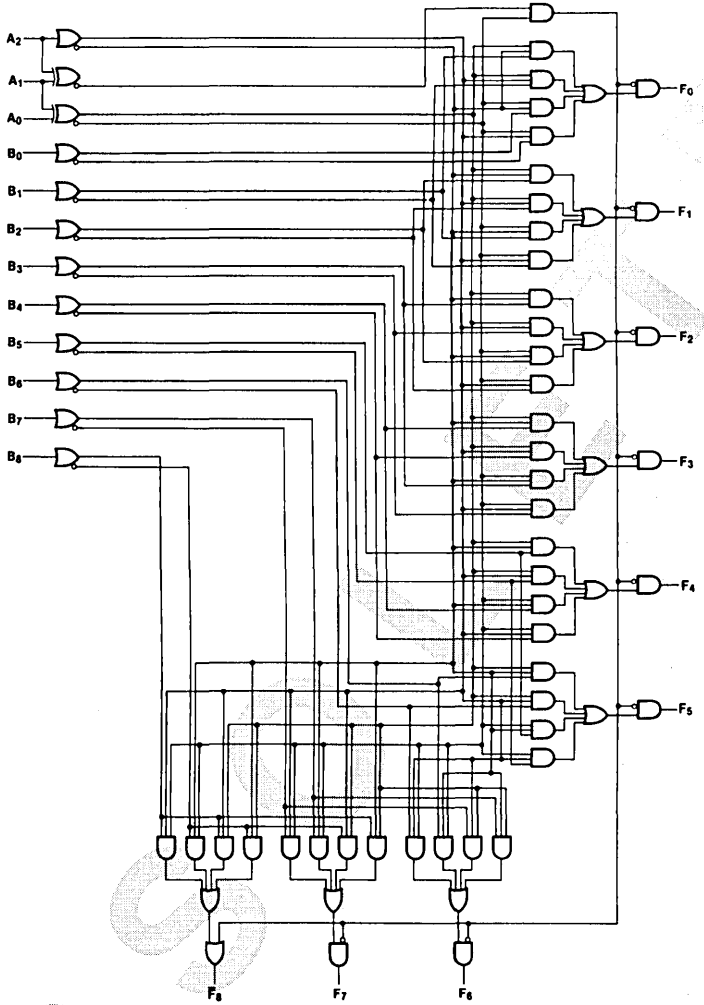
TL/F/9875–1

24-Pin Quad Cerpak



TL/F/9875–2

Logic Diagram



TL/F/9875–5

Truth Table

Inputs			Recode Mode	Outputs								
A_2	A_1	A_0		$\overline{F}_8$	F_7	F_6	F_5	F_4	F_3	F_2	F_1	F_0
L	L	L	0	H	L	L	L	L	L	L	L	L
L	L	H	+1	$\overline{B}_8$	B_8	B_7	B_6	B_5	B_4	B_3	B_2	B_1
L	H	L	+1	$\overline{B}_8$	B_8	B_7	B_6	B_5	B_4	B_3	B_2	B_1
L	H	H	+2	$\overline{B}_8$	B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0
H	L	L	−2	B_8	$\overline{B}_7$	$\overline{B}_6$	$\overline{B}_5$	$\overline{B}_4$	$\overline{B}_3$	$\overline{B}_2$	$\overline{B}_1$	$\overline{B}_0$
H	L	H	−1	B_8	$\overline{B}_8$	$\overline{B}_7$	$\overline{B}_6$	$\overline{B}_5$	$\overline{B}_4$	$\overline{B}_3$	$\overline{B}_2$	$\overline{B}_1$
H	H	L	−1	B_8	$\overline{B}_8$	$\overline{B}_7$	$\overline{B}_6$	$\overline{B}_5$	$\overline{B}_4$	$\overline{B}_3$	$\overline{B}_2$	$\overline{B}_1$
H	H	H	0	H	L	L	L	L	L	L	L	L

H = HIGH Voltage Level
L = LOW Voltage Level

Absolute Maximum Ratings

Above which the useful life may be impaired. (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Maximum Junction Temperature (T_J)	+150°C
Case Temperature under Bias (T_C)	0°C to +85°C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Output Current (DC Output HIGH)	−50 mA
Operating Range (Note 2)	−5.7V to −4.2V

DC Electrical Characteristics

V_{EE} = −4.5V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1025	−955	−880	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1810	−1705	−1620			
V_{OHC}	Output HIGH Voltage	−1035			mV	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610			
V_{IH}	Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

DC Electrical Characteristics

V_{EE} = −4.2V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1020		−870	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1810		−1605			
V_{OHC}	Output HIGH Voltage	−1030			mV	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1595			
V_{IH}	Input HIGH Voltage	−1150		−870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

DC Electrical Characteristics

V_{EE} = −4.8V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1035		−880	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830		−1620			
V_{OHC}	Output HIGH Voltage	−1045			mV	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610			
V_{IH}	Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1830		−1490	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Parametric values specified at −4.2V to −4.8V.

Note 3: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 4: Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DC Electrical Characteristics

V_{EE} = −4.2V to −4.8V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C

Symbol	Parameter	Min	Typ	Max	Units	Conditions
I_{IH}	Input HIGH Current B_0–B_8 A_0 A_1 A_2			 215 215 285 310	μA	V_{IN} = $V_{IH\ (Max)}$
I_{EE}	Power Supply Current	−250	−170	−115	mA	Inputs Open

Ceramic Dual-In-Line Package AC Electrical Characteristics

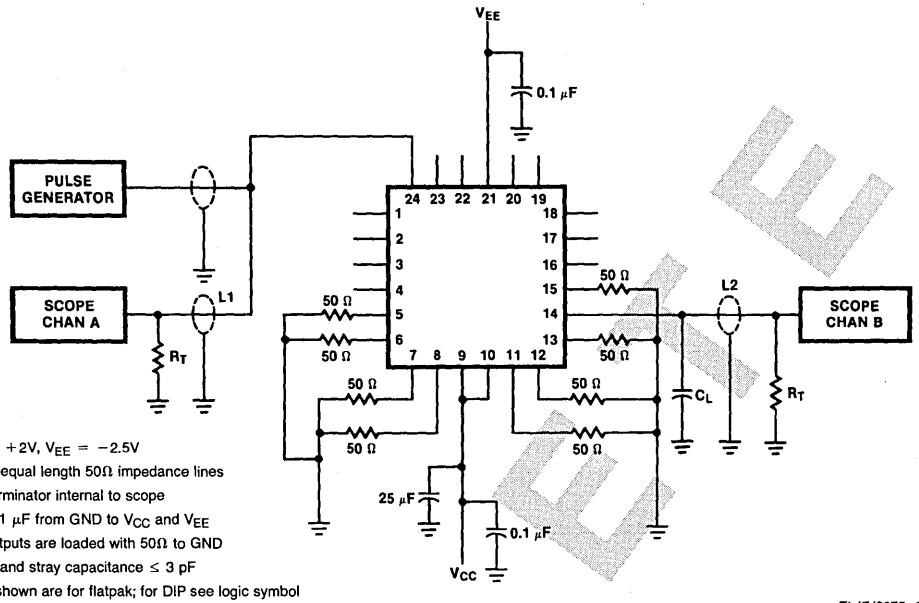
V_{EE} = −4.2V to −4.8V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay A_0–A_2 to F_0–F_7	1.10	3.90	1.10	3.80	1.10	4.20	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay A_0–A_2 to $\overline{F}_8$	0.90	3.20	1.00	3.10	1.00	3.60	ns	
t_{PLH} t_{PHL}	Propagation Delay B_0–B_8 to F_0–F_7	0.80	2.20	0.90	2.15	0.90	2.50	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay B_8 to $\overline{F}_8$	0.80	2.00	0.90	2.00	0.90	2.50	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	2.50	0.45	2.40	0.45	2.60	ns	*Figures 1* and *2*

Cerpak AC Electrical Characteristics

V_{EE} = −4.2V to −4.8V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay A_0–A_2 to F_0–F_7	1.10	3.70	1.10	3.60	1.10	4.00	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay A_0–A_2 to $\overline{F}_8$	0.90	3.00	1.00	2.90	1.00	3.40	ns	
t_{PLH} t_{PHL}	Propagation Delay B_0–B_8 to F_0–F_7	0.80	2.00	0.90	1.95	0.90	2.30	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay B_8 to $\overline{F}_8$	0.80	1.80	0.90	1.80	0.90	2.30	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	2.40	0.45	2.30	0.45	2.50	ns	*Figures 1* and *2*



Notes:

V_{CC}, V_{CCA} = +2V, V_{EE} = −2.5V

L1 and L2 = equal length 50Ω impedance lines

R_T = 50Ω terminator internal to scope

Decoupling 0.1 μF from GND to V_{CC} and V_{EE}

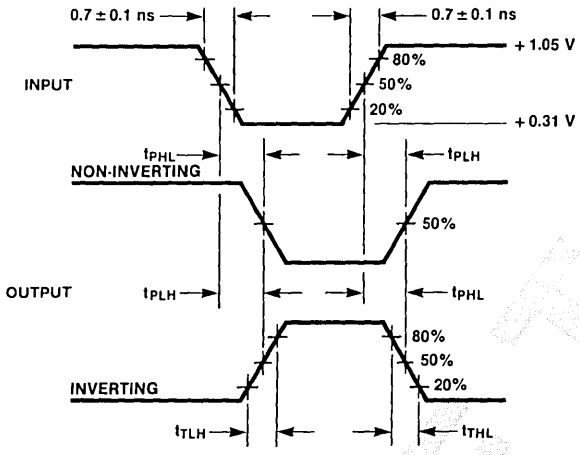
All unused outputs are loaded with 50Ω to GND

C_L = Fixture and stray capacitance ≤ 3 pF

Pin numbers shown are for flatpak; for DIP see logic symbol

TL/F/9875–6

FIGURE 1. AC Test Circuit



TL/F/9875–7

FIGURE 2. Propagation Delay and Transition Times

Application

100183 is a 2 x 8-bit recode multiplier that performs parallel multiplication using twos complement arithmetic. In multiplying, the multiplier is partitioned into recode groups, then each recode group operates on the multiplicand to provide a partial product at the same time. The 100183, 2 x 8-bit recode multiplier provides partial products in 3.6 ns.

The 100182, 9-Bit Wallace Tree Adder combines the partial products to obtain the partial sum and partial carries in an additional 10.7 ns. Then the Carry Lookahead generator and 6-bit adder combine the results of a 16 x 16-bit multiply for a total of 24.3 ns. The propagation delays and package count for implementing various size multipliers are listed in Tables I and II.

Multiplication of twos complement binary numbers is accomplished by first obtaining all the partial products. Then the weighted partial products are added together to yield the final result. In the Wallace Tree method of multiplication the sign bit is treated the same as the rest of the bits to obtain a signed result.

TABLE I. Propagation Delay Summation*

Array Size	Recode Multiplier 100183	Wallace Tree Adder 100182	High-speed Adder 100180	Carry Lookahead 100179		Total (Max) Delay
16 x 16	3.6	10.7	7.3	2.7	=	24.3 ns
17 x 17 thru 24 x 24	3.6	21.4	7.3	2.7	=	35.0 ns
25 x 25 thru 48 x 48	3.6	21.4	7.3	5.4	=	37.7 ns
49 x 49 thru 72 x 72	3.6	21.4	7.3	8.1	=	40.4 ns
73 x 73	3.6	32.1	7.3	10.8	=	53.8 ns

*Worst case, Flatpak

Application (Continued)

TABLE II. Package Count

	100102 100117	100183	100182	100180	100179		Total
16 x 16	6	16	32	6	2	=	62
18 x 18	7	27	38	6	2	=	70
24 x 24	9	36	60	8	2	=	115
32 x 32	11	64	96	11	4	=	186
36 x 36	13	80	116	12	4	=	225
64 x 64	24	256	328	22	6	=	634

For a quick review of the twos complement number format see Table III. Note that subtraction is accomplished by adding the negative number. An example of changing from a positive number to a negative number is shown.

1011 negative number-5

0100 bits inverted
+0001 add one
0101 Results 5

TABLE III. Twos Complement Format

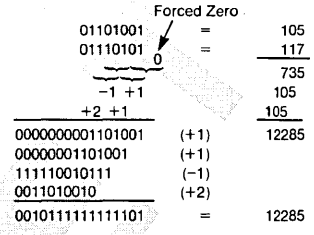
Sign Bit	Magnitude 2^2	2^1	2^0	Decimal Number
0	1	1	1	+7
0	1	1	0	+6
0	1	0	1	+5
0	1	0	0	+4
0	0	1	1	+3
0	0	1	0	+2
0	0	0	1	+1
0	0	0	0	+0
1	1	1	1	−1
1	1	1	0	−2
1	1	0	1	−3
1	1	0	0	−4
1	0	1	1	−5
1	0	1	0	−6
1	0	0	1	−7
1	0	0	0	−8

Multiplication Algorithm

In the multiplication algorithm used, the multiplier ($Y_n \ldots Y_0$) is partitioned into recode groups and each recode group operates on the multiplicand ($X_n \ldots X_0$) as in *Figure 4.* The 100183, 2 x 8-bit recode multiplier partitions the multiplier ($X_n \ldots X_0$) into groups of eight and the multiplicand ($Y_n \ldots Y_0$) into groups of two. Each recode group is two bits wide but requires three bits to determine the partial products. Table IV lists the significance of the various recode groups. The partial product is ±0, ±multiplicand, or ±two times the multiplicand. A forced zero is required to establish the least significant bit of the first recode group. By connecting recode multipliers in parallel the partial products are available at the same time. The weighted partial products ($A_n \ldots A_0$, $B_n \ldots B_0$) ... are added together using 100182, 9-bit Wallace Tree Adders. The results of the partial sum and partial carry are combined together using Carry Lookahead generators and 6-bit adders. An example of using recode multiplication is shown in *Figure 3:* multiplier (117_{10}) 01110101 times multiplicand (105_{10}) 01101001. The first recode group 010 requires adding the multiplicand; the second recode group 010 also requires adding the multiplicand; the third group 110 requires subtracting the multiplicand (the same as inverting each digit and adding 1); the fourth group 011 requires adding twice the multiplicand. Combining the results of four groups, 12285_{10}, we have the correct answer.

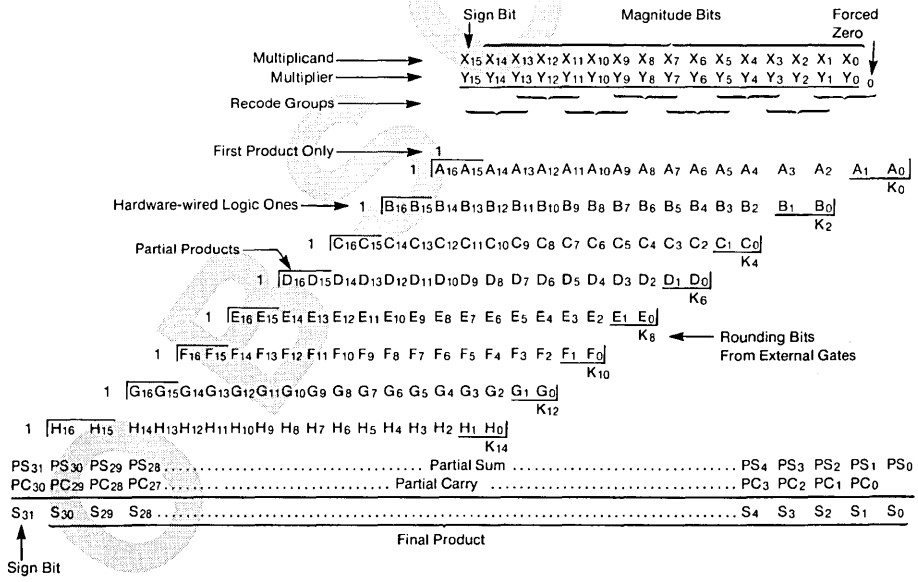
TABLE IV. Recode Product

Recode Group Y_{i+1}	Y_i	Y_{i-1}	Recode Value	Partial Product
0	0	0	+0	Add zero
0	0	1	+1	Add multiplicand
0	1	0	+1	Add multiplicand
0	1	1	+2	Add twice the multiplicand
1	0	0	−2	Subtract twice the multiplicand
1	0	1	−1	Subtract the multiplicand
1	1	0	−1	Subtract the multiplicand
1	1	1	−0	Subtract zero



TL/F/9875–8

FIGURE 3. Recode Multiplication Example



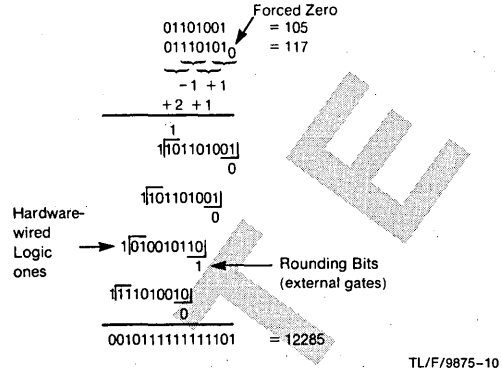
TL/F/9875–9

FIGURE 4. 16 x 16 Multiply

Hardware Implementation

For the hardware implementation of the 100183 recode multiplier the sign bit is connected to the B_8 input, and B_7 through B_0 are the magnitude bits. Two extend the word length greater than eight bits, the B_0 and B_8 inputs of adjacent devices are connected together (see *Figure 7*). The device outputs F_0 through F_7 are used as the partial products; these correspond to A_0 through A_7, or A_8 through A_{15}, or B_0 through B_7, etc. To reduce the hardware, the $\overline{F}_8$ bit (A_{16} in *Figure 7*) is used as the sign bit of the partial product. The sign bits are extended by using hardware wired logic "1s". The ones are located in front of each partial product with an extra "1" at the sign bit of the first partial product as in *Figure 4.* The logic "1s" are wired as inputs into the Wallace Tree Adders as shown in *Figure 6.* If the recode group requires the multiplicand to be added, then the 100183 outputs the correct partial products to be added. But when the recode group requires that the multiplicand be subtracted, then the 100183 outputs the ones complement. External gates are required to generate a "1" to be added to the ones complement to complete the twos complement for the partial product *(Figure 7).* These external gates generate the rounding bits, $K_0 \ldots K_n$, which are input to the Wallace Tree Adder. *Figures 4, 6* and *7* show the location. An example of multiplication which has the rounding bits and the hardware wired logic "1s" is shown in *Figure 5.*

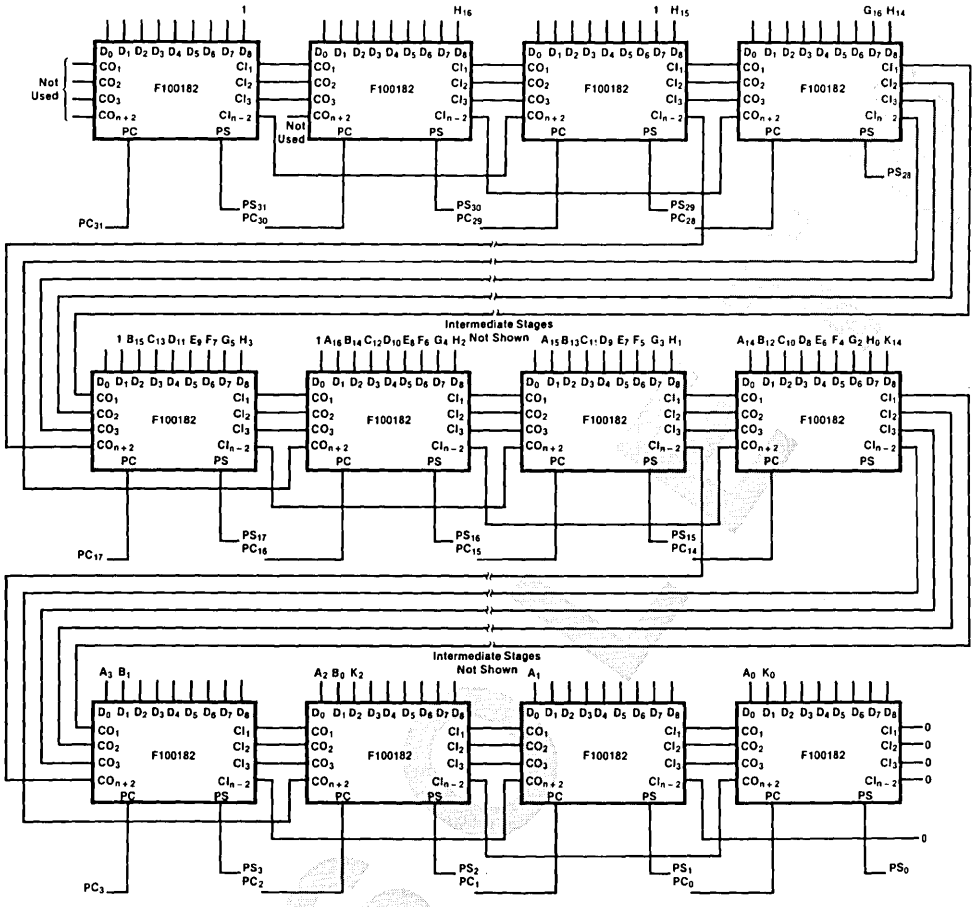
The weighted partial products are added together using 100182, 9-bit Wallace Tree Adders as shown in *Figure 6.* The output is a partial sum and partial carry which can be reduced to the final product using Carry Lookahead and 6-bit adders. See *Figure 8.*



TL/F/9875–10

FIGURE 5. Example of Multiplication Using Rounding Bits

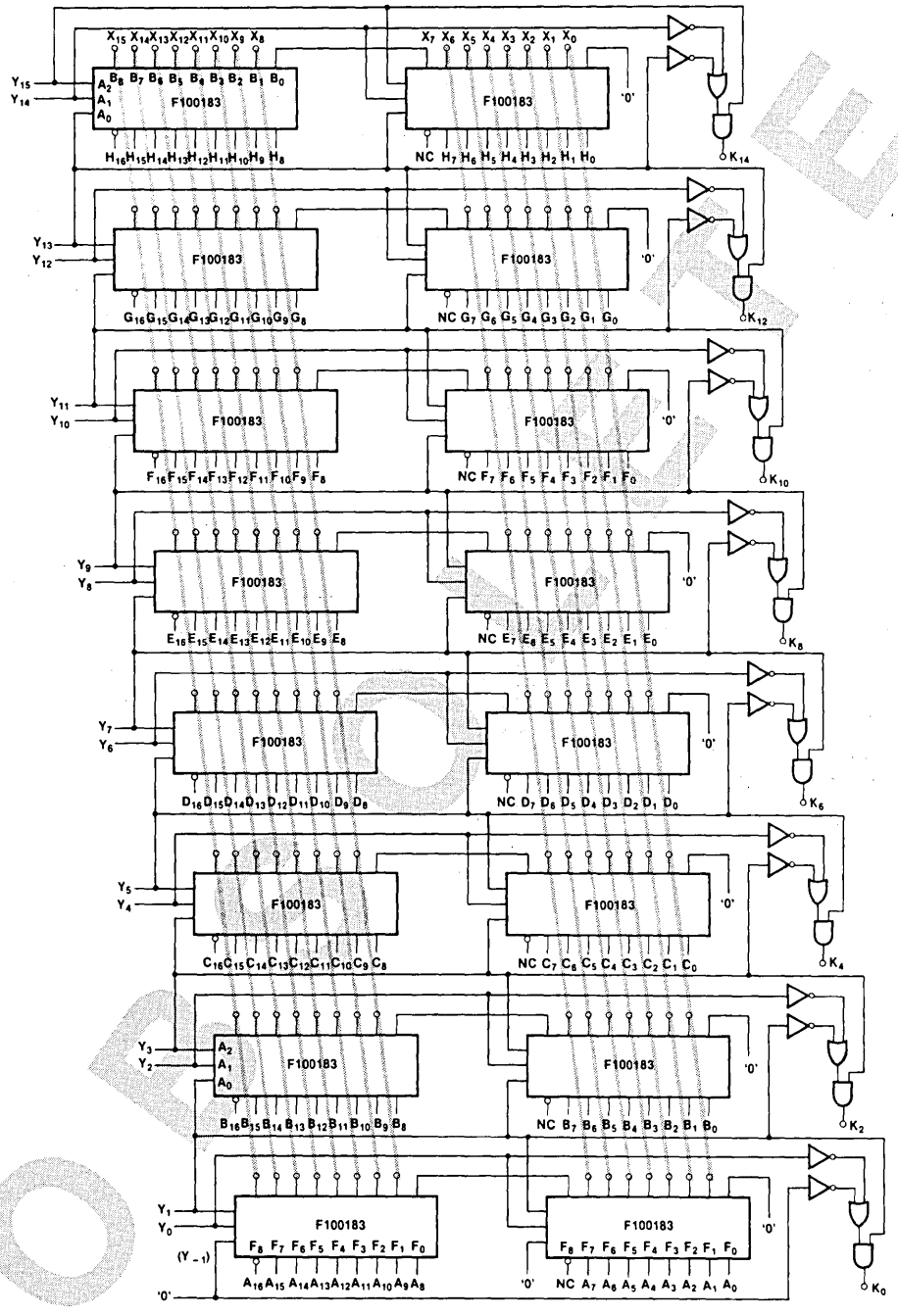
Hardware Implementation (Continued)



TL/F/9875–11

FIGURE 6. 100182 Hook-up for 16 x 16 Multiplier

Hardware Implementation (Continued)



TL/F/9875–12

FIGURE 7. 100183 Hook-Up for 16 x 16 Multiplier

Hardware Implementation (Continued)

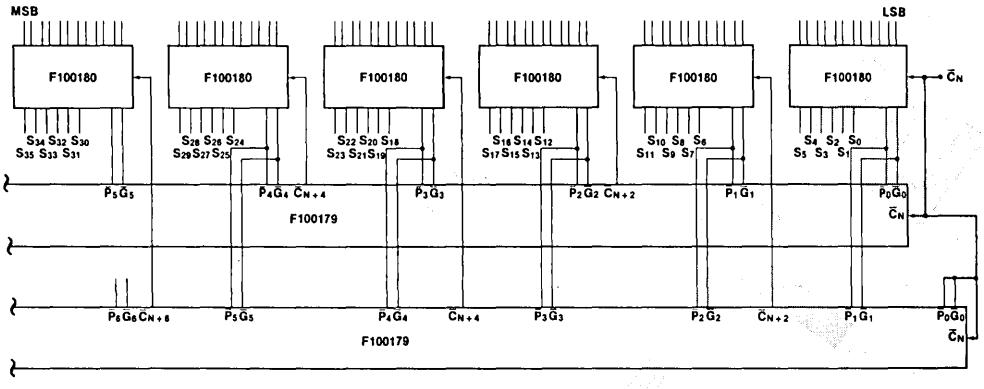


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FIGURE 8. Final Summation for 16 x 16 Multiplier

National Semiconductor

Not Intended For New Designs

100250
Quint Full Duplex Line Transceiver

General Description

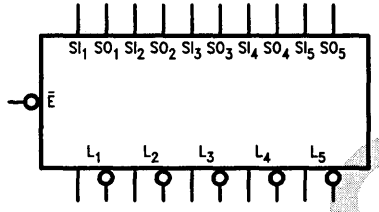
The 100250 is a quint line transceiver capable of simultaneously transmitting and receiving differential mode signals on a twisted pair line. Each transceiver has a signal input S_{IN}, a signal output S_{OUT} and two differential line inputs/outputs L and $\overline{L}$. Signals received from the lines L and $\overline{L}$ can be stored in an internal latch. The line outputs are designed to drive twisted pair lines. The $\overline{ENABLE}$ input is common to all five transceivers.

Features

- Full duplex operation
- Common mode noise immunity of ±1V

Ordering Code: See Section 6

Logic Symbol

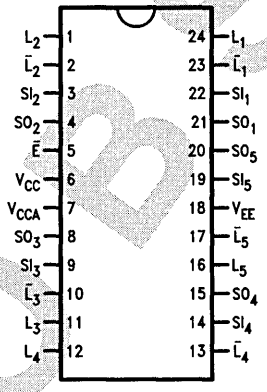


TL/F/9876–3

Pin Names	Description
$\overline{E}$	Common Enable
S_{In}	100K Signal Inputs
S_{On}	100K Signal Outputs
L_n, $\overline{L}_n$	Differential Line Inputs/Outputs

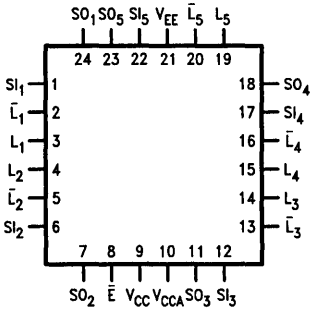
Connection Diagrams

24-Pin DIP



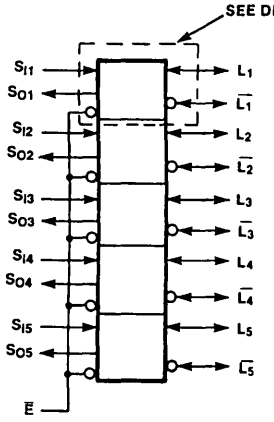
TL/F/9876–1

24-Pin Quad Cerpak

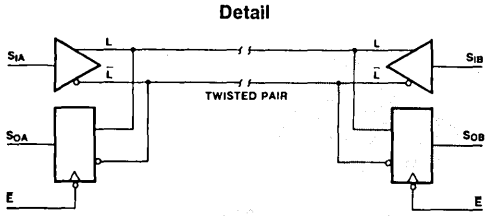


TL/F/9876–2

Logic Diagram



TL/F/9876-6



TL/F/9876-5

FIGURE 1. Interconnection of Two 100250 Circuits, Duplex Mode Operation

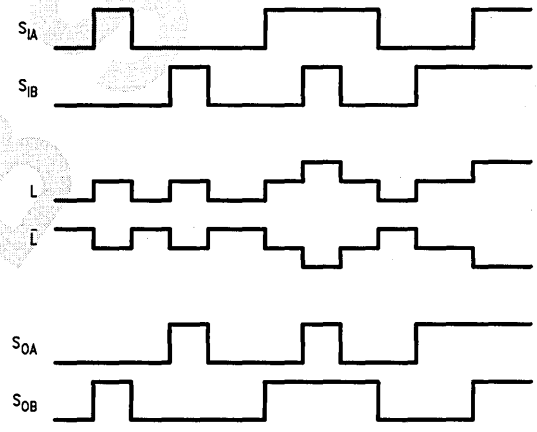
Truth Table

$\overline{E}$	S_{IA}	S_{IB}	S_{OA}	S_{OB}	L	$\overline{L}$
H	X	X	$S_{OA}(n-1)$	$S_{OB}(n-1)$	*	*
L	L	L	L	L	U_L	U_H
L	L	H	H	L	$(U_L + U_H)/2$	$(U_L + U_H)/2$
L	H	L	L	H	$(U_L + U_H)/2$	$(U_L + U_H)/2$
L	H	H	H	H	U_H	U_L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
n−1 = Previous State
* = Dependent on S_{IA} and S_{IB}

$U_L \approx -1.27V$
$U_H \approx -0.27V$
$(U_L + U_H)/2 \approx -0.77V$

Functional Waveform



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Absolute Maximum Ratings

Above which the useful life may be impaired. (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Maximum Junction Temperature (T_J)	+150°C
Case Temperature under Bias (T_C)	0°C to +85°C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Output Current (DC Output HIGH)	−50 mA
Operating Range (Note 2)	−5.7V to −4.2V

DC Electrical Characteristics

V_{EE} = −4.2V to −4.8V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C

Symbol	Parameter	Min	Typ	Max	Units	Conditions
I_{IH}	Input HIGH Current S_{In}			200	μA	V_{IN} = $V_{IH(Max)}$
	Input HIGH Current $\overline{E}$			250	μA	
I_{EE}	Power Supply Current	−300		−180	mA	Inputs Open

DC Electrical Characteristics

V_{EE} = −4.5V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1025	−955	−880	mV	V_{IN} = $V_{IH(Max)}$ or $V_{IL(Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1810	−1705	−1620	mV		
V_{OHC}	Output HIGH Voltage	−1035			mV	V_{IN} = $V_{IH(Min)}$ or $V_{IL(Max)}$	
V_{OLC}	Output LOW Voltage			−1610	mV		
V_{KH}	Line Output HIGH Voltage	−370		−220	mV	No Load	
V_{KL}	Line Output LOW Voltage	−1400		−1090	mV	V_{IN} = $V_{IH(Max)}$ or $V_{IL(Min)}$	
V_{IH}	Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL(Min)}$	

DC Electrical Characteristics

V_{EE} = −4.2V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1020		−870	mV	V_{IN} = $V_{IH(Max)}$ or $V_{IL(Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1810		−1605	mV		
V_{OHC}	Output HIGH Voltage	−1030			mV	V_{IN} = $V_{IH(Min)}$ or $V_{IL(Max)}$	
V_{OLC}	Output LOW Voltage			−1595	mV		
V_{KH}	Line Output HIGH Voltage	−350		−200	mV	No Load	
V_{KL}	Line Output LOW Voltage	−1300		−990	mV	V_{IN} = $V_{IH(Max)}$ or $V_{IL(Min)}$	
V_{IH}	Input HIGH Voltage	−1150		−870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL(Min)}$	

DC Electrical Characteristics

V_{EE} = −4.8V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1035		−880	mV	V_{IN} = $V_{IH(Max)}$ or $V_{IL(Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830		−1620	mV		
V_{OHC}	Output HIGH Voltage	−1045			mV	V_{IN} = $V_{IH(Min)}$ or $V_{IL(Max)}$	
V_{OLC}	Output LOW Voltage			−1610	mV		
V_{KH}	Line Output HIGH Voltage	−400		−250	mV	No Load	
V_{KL}	Line Output LOW Voltage	−1500		−1190	mV	V_{IN} = $V_{IH(Max)}$ or $V_{IL(Min)}$	
V_{IH}	Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1830		−1490	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL(Min)}$	

Note 1: Unless specified otherwise on individual data sheet.

Note 2: Parametric values specified at −4.2V to −4.8V.

Note 3: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 4: Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

Ceramic Dual-In-Line Package AC Electrical Characteristics

V_{EE} = −4.2V to −4.8V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C

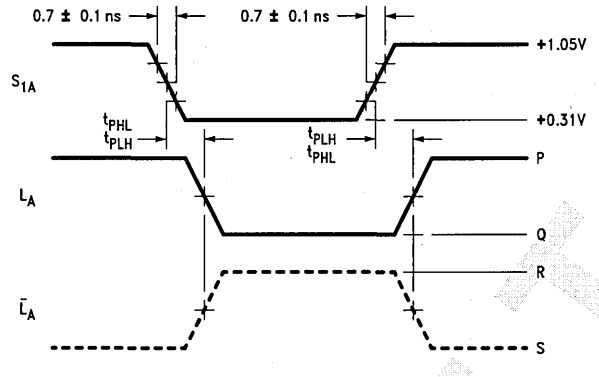
Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay S_I to L, $\overline{L}$	1.1	2.4	1.1	2.4	1.2	2.6	ns	*Figures 2* and *4*
t_{PLH} t_{PHL}	Propagation Delay L, $\overline{L}$ to S_O	1.2	2.8	1.2	2.9	1.3	3.0	ns	*Figures 3* and *5*
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to S_O	1.2	2.6	1.2	2.7	1.3	2.9	ns	*Figures 3* and *5*
t_{THL} t_{TLH}	Transition Time 20% to 80%, 80% to 20%	0.5	2.0	0.5	2.0	0.5	2.0	ns	
t_S	Setup Time L, $\overline{L}$	1.3		1.3		1.5		ns	*Figure 3*
t_H	Hold Time L, $\overline{L}$	1.3		1.3		1.5		ns	

Cerpak AC Electrical Characteristics

V_{EE} = −4.2V to −4.8V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C

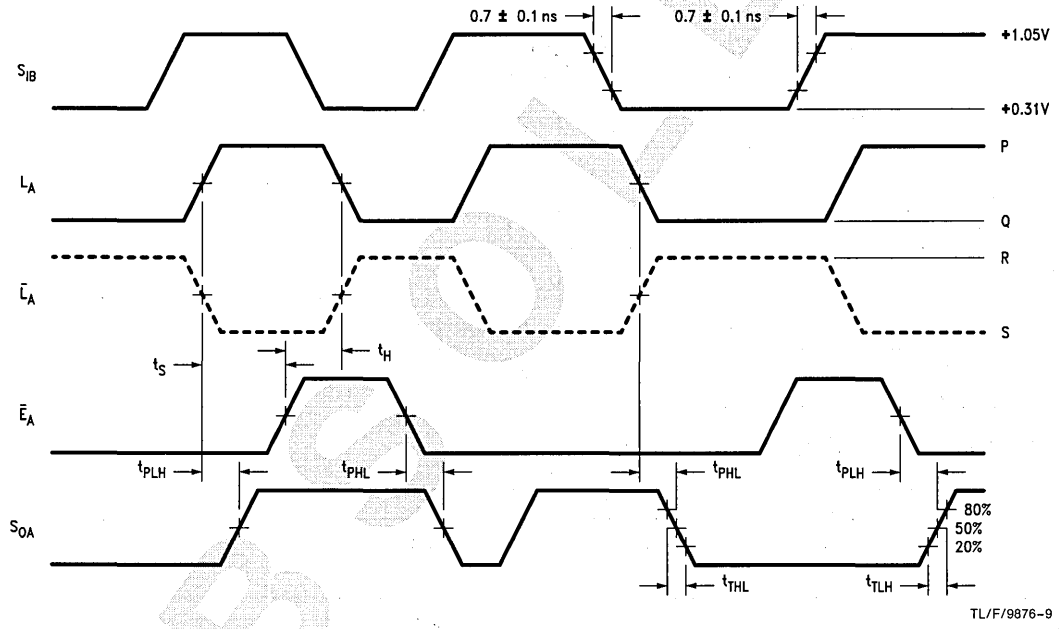
Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay S_I to L, $\overline{L}$	1.1	2.2	1.1	2.2	1.2	2.4	ns	*Figures 2* and *4*
t_{PLH} t_{PHL}	Propagation Delay L, $\overline{L}$ to S_O	1.2	2.6	1.2	2.7	1.3	2.8	ns	*Figures 3* and *5*
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to S_O	1.2	2.4	1.2	2.5	1.3	2.7	ns	*Figures 3* and *5*
t_{THL} t_{TLH}	Transition Time 20% to 80%, 80% to 20%	0.5	1.9	0.5	1.9	0.5	1.9	ns	
t_S	Setup Time L, $\overline{L}$	1.3		1.3		1.5		ns	*Figure 3*
t_H	Hold Time L, $\overline{L}$	1.3		1.3		1.5		ns	

Switching Waveforms



Notes: S_{IB} = L then P = $(U_L + U_H)/2$, Q = U_L, R = U_H, S = $(U_L + U_H)/2$
S_{IB} = H then P = U_H, Q = $(U_L + U_H)/2$, R = $(U_L + U_H)/2$, S = U_L
} L, $\bar{L}$ loaded with another F100250

FIGURE 2. S_I to Differential Line



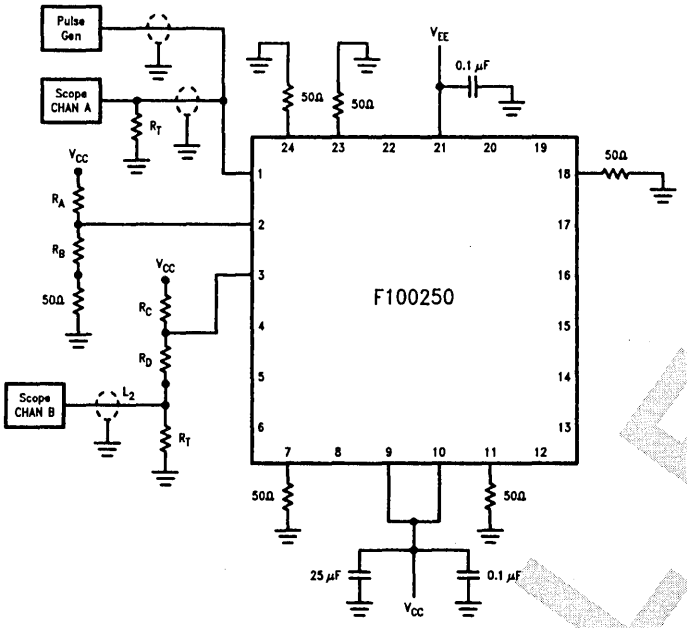
Notes: S_{IA} = L then P = $(U_L + U_H)/2$, Q = U_L, R = U_H, S = $(U_L + U_H)/2$
S_{IA} = H then P = U_H, Q = $(U_L + U_H)/2$, R = $(U_L + U_H)/2$, S = U_L
} L, $\bar{L}$ loaded with another F100250

t_S is the minimum time before the transition of the enable that information must be present at the data input.

t_H is the minimum time before the transition of the enable that information must remain unchanged at the data input.

FIGURE 3. Differential Line to S_O

Test Circuitry



Notes:

V_{CC}, V_{CCA} = +2V, V_{EE} = −2.5V
L1 and L2 = equal length 50Ω impedance lines.
R_T = 50Ω terminator internal to scope.
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}.
All unused outputs are loaded with 50Ω to GND.
C_L = fixture and stray capacitance ≤ 3 pF.
L and $\overline{L}$ terminated by 100250 or Thevenin equivalent.
Signal levels will be a percentage of full swing if using equivalent network.
R_A = 91Ω, R_B = 500Ω, R_C = 220Ω, R_D = 71.5Ω for S_{IB} = L.
R_A = 220Ω, R_B = 71.5Ω, R_C = 91Ω, R_D = 500Ω for S_{IB} = H.

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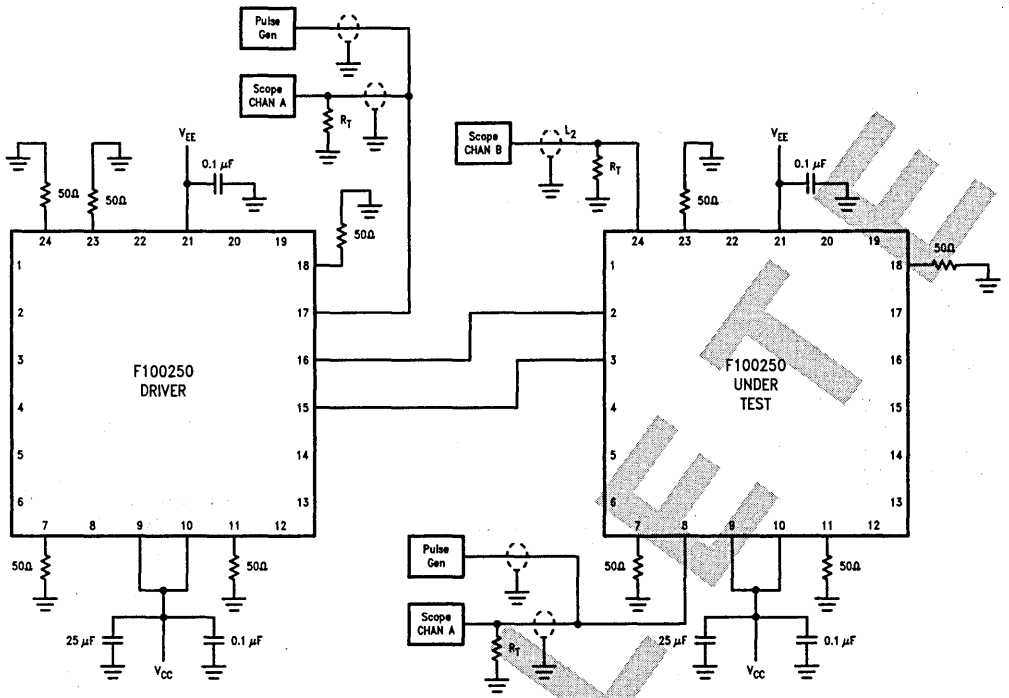
FIGURE 4. AC Test Circuit SI to Differential Line



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Notes:

V_{CC}, V_{CCA} = +2V, V_{EE} = −2.5V
L1 and L2 = equal length 50Ω impedance lines.
R_T = 50Ω terminator internal to scope.
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}.
All unused outputs are loaded with 50Ω to GND.
C_L = fixture and stray capacitance ≤ 3 pF.

FIGURE 5. AC Test Circuit Differential Line to S_O and $\overline{E}$ to S_O

Section 4

11C Datasheets

Section 4 Contents

National Semiconductor

Not Intended For New Designs

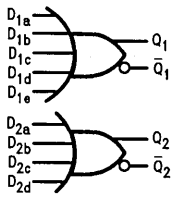
11C01
Dual 5-4 Input OR/NOR Gate

General Description

The 11C01 is a voltage-compensated ECL dual 5-4 input OR/NOR gate. The circuit has standard internal voltage compensation with DC parameters identical to 10K ECL devices.

Ordering Code: See Section 6

Logic Symbol

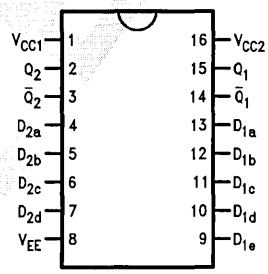


TL/F/9888–2

Pin Names	Description
D_{1a}–D_{1e}, D_{2a}–D_{2d}	Data Inputs
Q_1, $\overline{Q}_1$, Q_2, $\overline{Q}_2$	Outputs

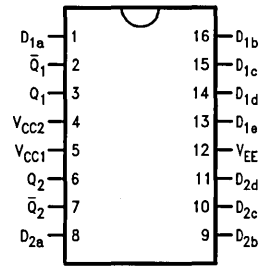
Connection Diagrams

16-Pin DIP



TL/F/9888–1

16-Pin Flatpak



TL/F/9888–3

Truth Tables

In					Out	
D_{1a}	D_{1b}	D_{1c}	D_{1d}	D_{1e}	Q_1	$\overline{Q}_1$
L	L	L	L	L	L	H
H	X	X	X	X	H	L
X	H	X	X	X	H	L
X	X	H	X	X	H	L
X	X	X	H	X	H	L
X	X	X	X	H	H	L

In				Out	
D_{2a}	D_{2b}	D_{2c}	D_{2d}	Q_2	$\overline{Q}_2$
L	L	L	L	L	H
H	X	X	X	H	L
X	H	X	X	H	L
X	X	H	X	H	L
X	X	X	H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

Absolute Maximum Ratings

Above which the useful life may be impaired

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Maximum Junction Temperature (T_J)	+150°C
Supply Voltage Range	−7.0V to GND
Input Voltage (DC)	V_{EE} to GND
Output Current (DC Output HIGH)	−50 mA
Operating Range	−5.5V to −4.75V
Lead Temperature (Soldering, 10 sec.)	300°C

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage (V_{EE})	−5.5	−5.2	−4.75	V
Ambient Temperature (T_A)	0		+75	°C

DC Electrical Characteristics

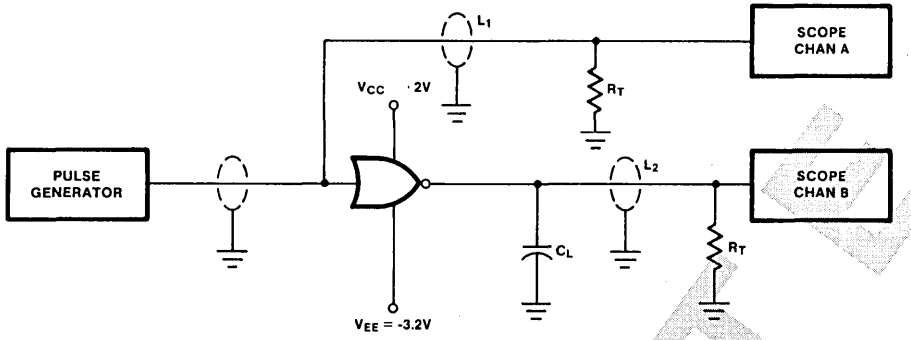
V_{EE} = −5.2V, V_{CC} = GND

Symbol	Parameter	Min	Typ	Max	Units	T_A	Conditions	
V_{OH}	Output Voltage HIGH	−1000 −960 −900		−840 −810 −720	mV	0°C +25°C +75°C	V_{IN} = $V_{IH(Max)}$ or $V_{IL(Min)}$ per Truth Table	Loading is 50Ω to −2.0V
V_{OL}	Output Voltage LOW	−1870 −1850 −1830		−1665 −1650 −1625	mV	0°C +25°C +75°C		
V_{OHC}	Output Voltage HIGH	−1020 −980 −920			mV	0°C +25°C +75°C	V_{IN} = $V_{IH(Min)}$ or $V_{IL(Max)}$ per Truth Table	
V_{OLC}	Output Voltage LOW			−1645 −1630 −1605	mV	0°C +25°C +75°C		
V_{IH}	Input Voltage HIGH	−1145 −1105 −1045		−840 −810 −720	mV	0°C +25°C +75°C	Guaranteed Input Voltage HIGH for All Inputs	
V_{IL}	Input Voltage LOW	−1870 −1850 −1830		−1490 −1475 −1450	mV	0°C +25°C +75°C	Guaranteed Input Voltage LOW for All Inputs	
I_{IH}	Input Current HIGH			350	μA	+25°C	V_{IN} = $V_{IH(Max)}$	
I_{IL}	Input Current LOW	0.5			μA	+25°C	V_{IN} = $V_{IL(Min)}$	
I_{EE}	Power Supply Current	−30	−24		mA	+25°C	Inputs and Outputs Open	

AC Electrical Characteristics

V_{EE} = −5.2V, T_A = +25°C

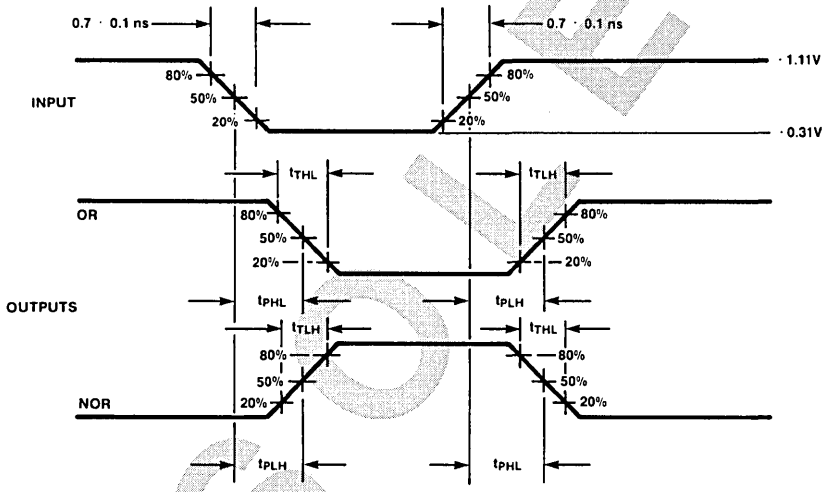
Symbol	Parameter	Flatpak			DIP			Units	Conditions
		Min	Typ	Max	Min	Typ	Max		
t_{PLH}	Propagation Delay LOW to HIGH	0.45	0.7	0.95	0.60	0.90	1.15	ns	See *Figure 1*
t_{PHL}	Propagation Delay HIGH to LOW	0.45	0.7	0.95	0.60	0.90	1.15	ns	
t_{TLH}	Output Transition Time LOW to HIGH (20% to 80%)		0.7	0.95		0.90	1.15	ns	
t_{THL}	Output Transition Time HIGH to LOW (80% to 20%)		0.7	0.95		0.90	1.15	ns	



Notes:

L1 and L2 = equal length 50Ω impedance lines
R_T = 50Ω Termination of scope
Decoupling 0.1 μF from GND to V_{EE} and V_{CC}
$C_L \leq 3$ pF

TL/F/9888–4



Notes:

Jig setup with no circuit under test
$V_{CC1} = V_{CC2} = +2.0V$
$V_{EE} = -3.2V$

TL/F/9888–5

FIGURE 1. Switching Circuit and Waveforms

National Semiconductor

Not Intended For New Designs

11C05
1 GHz Divide-By-Four Counter

General Description

The 11C05 is an ECL Divide-By-Four Counter with a maximum operating frequency above 1 GHz over the 0°C to +75°C temperature range. The input may be DC or AC (capacitively) coupled to the signal source. The emitter follower outputs (Q and $\overline{Q}$) are capable of driving 50Ω lines. The outputs are voltage-compensated and provide standard ECL output levels.

Ordering Code: See Section 6

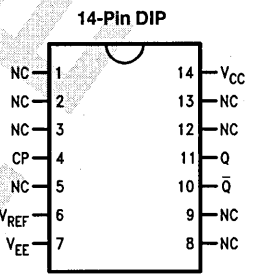
Logic Symbol

TL/F/9889–1

Pin Names	Description
CP	Clock Input
V_{REF}	Reference Input
Q, $\overline{Q}$	Counter Outputs

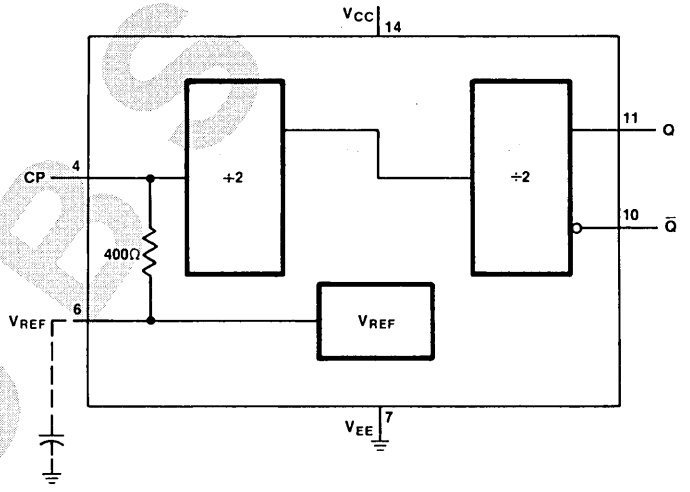
Connection Diagram

14-Pin DIP



TL/F/9889–2

Logic Diagram



TL/F/9889–3

Absolute Maximum Ratings

Above which the useful life may be impaired

Storage Temperature	−65°C to +150°C
Maximum Junction Temperature (T_J)	+150°C
Supply Voltage Range	−7.0V to GND
Input Voltage (DC)	V_{EE} to GND
Output Current (DC Output HIGH)	−50 mA
Operating Range	−5.5V to −4.75V
Lead Temperature (Soldering, 10 sec.)	300°C

Recommended Operating Conditions

	Min	Typ	Max
Supply Voltage (V_{EE})			
Commercial	−5.25V	−5.0V	−4.75V
Military	−5.5V	−5.0V	−4.75V
Ambient Temperature (T_A)			
Commercial	0°C		+75°C
Military	−55°C		+125°C

Commercial DC Electrical Characteristics

V_{EE} = 5.0V, V_{CC} = GND

Symbol	Parameter	Min	Typ	Max	Units	T_A	Conditions
V_{OH}	Output Voltage HIGH	−1060 −1025 −980	−995 −960 −910	−910 −880 −830	mV mV mV	0°C +25°C +75°C	V_{IN} = V_{IH} or V_{IL}, Loading 50Ω to −2V
V_{OL}	Output Voltage LOW	−1810	−1705	−1620	mV	0°C to +75°C	
V_{IH}	Input Voltage HIGH	−2.45 −2.50 −2.60			V V V	0°C +25°C +75°C	Guaranteed Input HIGH
V_{IL}	Input Voltage LOW			−3.25 −3.30 −3.40	V V V	0°C +25°C +75°C	Guaranteed Input LOW
I_{EE}	Power Supply Current	−90	−65		mA	+25°C	Input Open
V_{EE}	Supply Voltage Range	−5.25	−5.0	−4.75	V	0°C to +75°C	
V_{REF}	Input Reference Voltage		−2.9		V	+25°C	

Military DC Electrical Characteristics

V_{EE} = −5.0V, V_{CC} = GND

Symbol	Parameter	Min	Typ	Max	Units	T_A	Conditions
V_{OH}	Output Voltage HIGH	−1100 −980 −910	−1030 −910 −820	−950 −820 −720	mV mV mV	−55°C +25°C +125°C	V_{IN} = V_{IH} or V_{IL}, Loading 100Ω to −2V
V_{OL}	Output Voltage LOW	−1810	−1705	−1620	mV	−55°C to +125°C	
V_{IH}	Input Voltage HIGH	−2.35 −2.50 −2.70			V V V	−55°C +25°C +125°C	Guaranteed Input HIGH
V_{IL}	Input Voltage LOW			−3.15 −3.30 −3.50	V V V	−55°C +25°C +125°C	Guaranteed Input LOW
I_{EE}	Power Supply Current	−90	−65		mA	+25°C	Input Open
V_{EE}	Supply Voltage Range	−5.5	−5.0	−4.75	V	−55°C to +125°C	
V_{REF}	Input Reference Voltage		−2.9		V	+25°C	

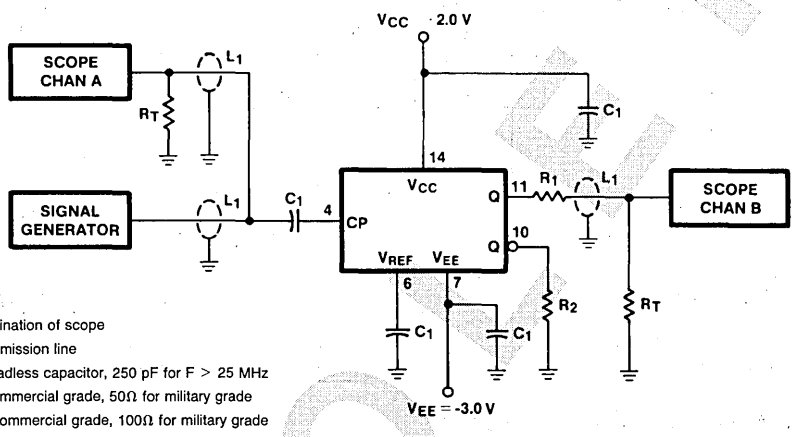
Commercial and Military AC Electrical Characteristics

V_{EE} = −5V, V_{CC} = GND, T_A −55°C to +125°C unless otherwise noted

Symbol	Parameter	Min	Typ	Max	Units	Conditions	
f_{COUNT}	Maximum Sinusoidal Input Frequency	1000			MHz	0°C to +75°C	AC Coupled 800 mV Peak-to-Peak Input (Note 2)
		950				−55°C to +125°C	
f_{COUNT}	Minimum Sinusoidal Input Frequency		25		MHz		
SR_{MIN}	Slew Rate of Squareware		50		V/μs	(Note 1)	

Note 1: Very low frequency operation is possible as long as sufficient slew rate of the input pulse edges is maintained.

Note 2: Input drive shall not exceed 1.5V peak-to-peak max.

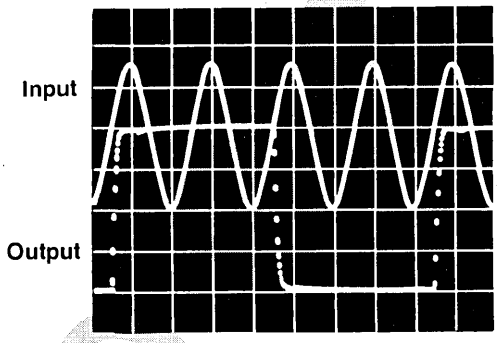


R_T = 50Ω termination of scope
L_1 = 50Ω transmission line
C_1 = 0.1 μF leadless capacitor, 250 pF for F > 25 MHz
R_1 = 0Ω for commercial grade, 50Ω for military grade
R_2 = 50Ω for commercial grade, 100Ω for military grade

TL/F/9889–4

FIGURE 1. AC Test Circuit

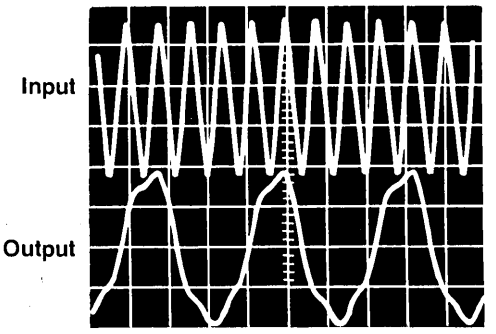
Horizontal Scale = ns/div
Vertical Scale = 200 mV/div



TL/F/9889–5

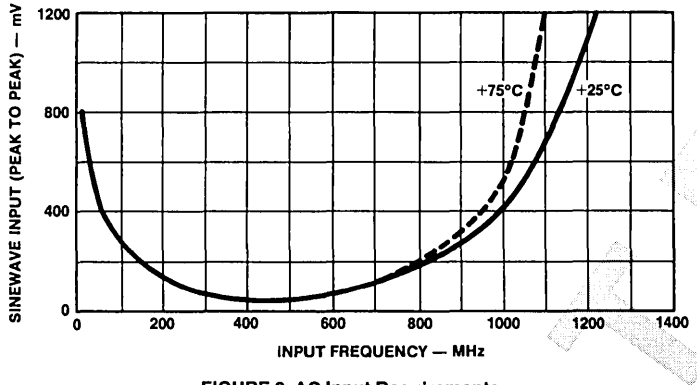
25 MHz Operation

Horizontal Scale = 1 ns/div
Vertical Scale = 200 mV/div



TL/F/9889–6

1.2 GHz Operation



TL/F/9889–7

FIGURE 2. AC Input Requirements

Note: Trigger amplitudes refer to the circuit end of the input cable as opposed to the signal generator end.

A DC coupled input should be designed to provide specified V_{IH} and V_{IL} levels. For AC coupling, an external resistor may or may not be necessary depending on the application. If an input signal is always present, only the capacitor is required because an internal 400Ω resistor connected between CP and V_{REF} centers the AC signal about mid-threshold. For applications in which an input signal is not always present, AC coupling requires that an external 10 KΩ resistor be connected between CP and V_{EE}. This offsets the input sufficiently to avoid extreme sensitivity to noise when no signal is present. Otherwise, noise triggering can lead to oscillation at about 450 MHz. For best operation, both outputs should be equally loaded.

National Semiconductor

Not Intended For New Designs

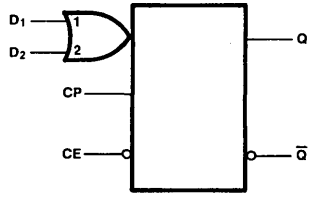
11C06
750 MHz D-Type Flip-Flop

General Description

The 11C06 is a high-speed ECL D-Type Master-Slave Flip-Flop capable of toggle rates over 750 MHz. Designed primarily for high-speed prescaling, it can also be used in any application which does not require preset inputs. The circuit is voltage-compensated, which makes input thresholds and output levels insensitive to V_{EE} variations. Complementary Q and $\overline{Q}$ outputs are provided, as are two Data inputs, Clock and Clock Enable inputs. The 11C06 is pin-compatible with the Motorola MC1690L but is a higher-frequency replacement.

Ordering Code: See Section 6

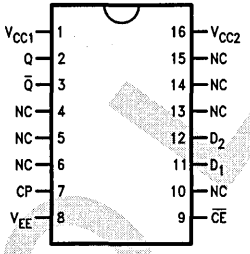
Logic Symbol



TL/F/9890–3

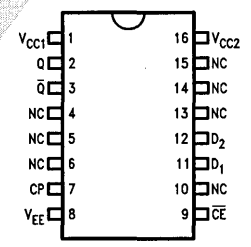
Connection Diagrams

16-Pin DIP



TL/F/9890–1

16-Pin Flatpak



TL/F/9890–2

Pin Names	Description
D_n	Data Input
CP	Clock Input
$\overline{CE}$	Clock Enable (Active LOW)
Q, $\overline{Q}$	Outputs

Truth Table

$\overline{CE}$	CP	D	Q_n
L	L	X	Q_{n-1}
L	H	X	Q_{n-1}
L	⌐	L	L
L	⌐	H	H
H	X	X	Q_{n-1}

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
⌐ = LOW to HIGH Transition
Q_{n-1} = Previous State

Absolute Maximum Ratings

Above which the useful life may be impaired

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Maximum Junction Temperature (T_J)	+150°C
Supply Voltage Range	−7.0V to GND
Input Voltage (DC)	V_{EE} to GND
Output Current (DC Output HIGH)	−50 mA
Operating Range	−5.7V to −4.7V
Lead Temperature (Soldering, 10 sec.)	300°C

Recommended Operating Conditions

	Min	Typ	Max
Supply Voltage (V_{EE})	−5.7V	−5.2V	−4.7V
Ambient Temperature (T_A)	0°C		+75°C

DC Electrical Characteristics

V_{EE} = −5.2V, V_{CC} = GND

Symbol	Parameter	Min	Typ	Max	Units	T_A	Conditions
V_{OH}	Output Voltage HIGH	−1000		−840	mV	0°C	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$ per Truth Table Loading 50Ω to −2V
		−960		−810	mV	+25°C	
		−900		−720	mV	+75°C	
V_{OL}	Output Voltage LOW	−1870		−1635	mV	0°C	
		−1850		−1620	mV	+25°C	
		−1830		−1595	mV	+75°C	
V_{OHC}	Output Voltage HIGH	−1020			mV	0°C	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$ for D_n Inputs Loading 50Ω to −2V
		−980			mV	+25°C	
		−920			mV	+75°C	
V_{OLC}	Output Voltage LOW			−1615	mV	0°C	
				−1600	mV	+25°C	
				−1575	mV	+75°C	
V_{IH}	Input Voltage HIGH	−1135		−840	mV	0°C	Guaranteed Input Voltage HIGH for All Inputs
		−1095		−810	mV	+25°C	
		−1035		−720	mV	+75°C	
V_{IL}	Input Voltage LOW	−1870		−1500	mV	0°C	Guaranteed Input Voltage LOW for All Inputs
		−1850		−1485	mV	+25°C	
		−1830		−1460	mV	+75°C	
I_{IH}	Input Current HIGH						V_{IN} = $V_{IH\ (Max)}$
	Clock Input			250	μA	+25°C	
	Data Input			270	μA	+25°C	
I_{IL}	Input Current LOW	0.5			μA	+25°C	V_{IN} = $V_{IH\ (Min)}$
I_{EE}	Power Supply Current	−59	−40		mA	+25°C	All Inputs Open

AC Electrical Characteristics

V_{EE} = −5.2V, V_{CC} = GND, T_A = +25°C

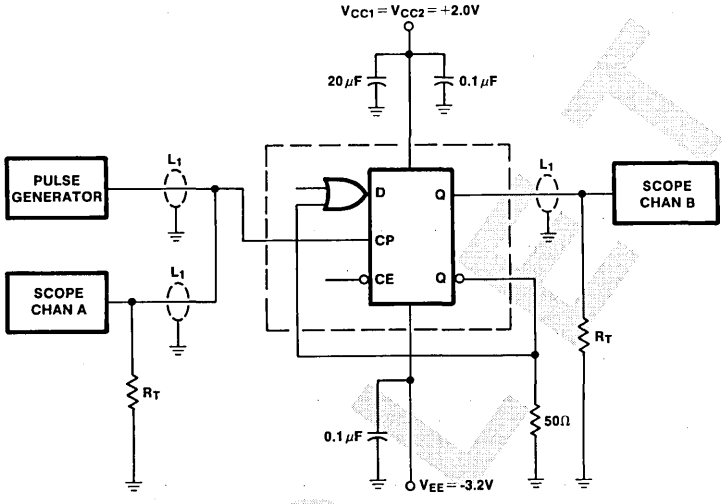
Symbol	Parameter	Min	Typ	Max	Units	Conditions
t_{PHL}	Propagation Delay (CP-Q)	0.7	1.0	1.2	ns	
t_{PLH}	Propagation Delay (CP-Q)	0.7	1.0	1.2	ns	
t_{TLH}	Transition Time 20% to 80%	0.5	0.8	1.0	ns	See *Figure 1*
t_{THL}	Transition Time 80% to 20%	0.5	0.8	1.0	ns	
t_S	Set-up Time		0.2		ns	
t_H	Hold Time		0.2		ns	
$f_{TOG\ (MAX)}$	Toggle Frequency (CP)	650	750		MHz	See *Figure 2*, Note

Note: The device is guaranteed for f_{TOG} (CP) ≥ 600 MHz, f_{TOG}(CE) ≥ 550 MHz over the 0°C to +75°C temperature range.

Functional Description

While the clock is LOW, the slave is held steady and the information on the D input is permitted to enter the master. The next transition from LOW to HIGH locks the master in its present state making it insensitive to the D input. This transition simultaneously connects the slave to the master causing the new information to appear on the outputs. Master and slave clock thresholds are internally offset in opposite directions to avoid race conditions or simultaneous master-slave changes when the clock has slow rise or fall times.

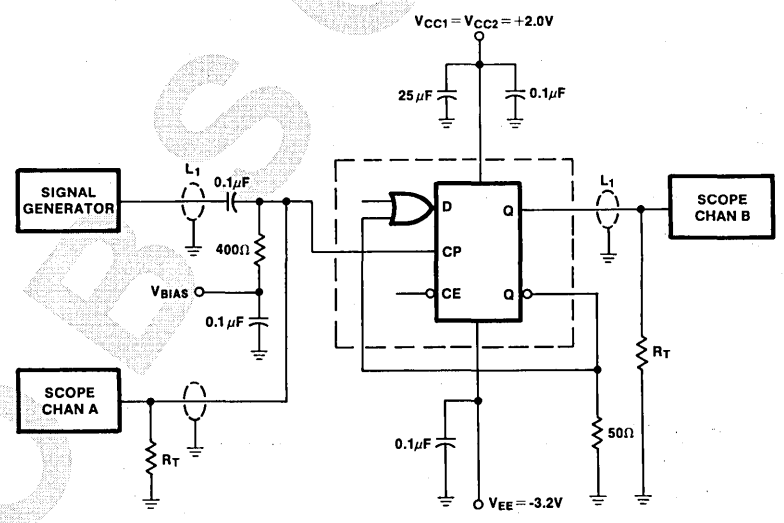
The CP and $\overline{CE}$ inputs are logically identical, but physical constraints associated with the Dual-In-Line package make the $\overline{CE}$ input slower at the upper end of the toggle range. To prevent new data from entering the master on the next CP LOW cycle, $\overline{CE}$ should go HIGH while CP is still HIGH.



TL/F/9890–4

R_T = 50Ω termination of scope
L_1 = 50Ω impedance lines
All input transition times are 2.0 ns ±0.2 ns

FIGURE 1. Propagation Delay (CP to Q)

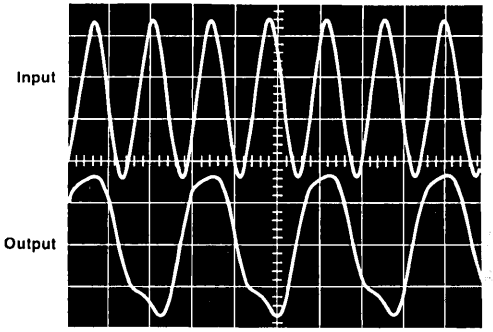


TL/F/9890–5

R_T = 50Ω termination of scope
L_1 = 50Ω impedance lines
Adjust V_{BIAS} for +0.7V baseline of 800 mV peak-to-peak sinewave input.
All input transition times are 2.0 ns ±0.2 ns

FIGURE 2. Toggle Frequency Test Circuit

Typical Waveforms



700 MHz Operation

TL/F/9890–6

Horizontal Scale = 1.0 ns/div
Vertical Scale = 200 mV/div

National Semiconductor

Not Intended For New Designs

11C70
Master-Slave D-Type Flip-Flop

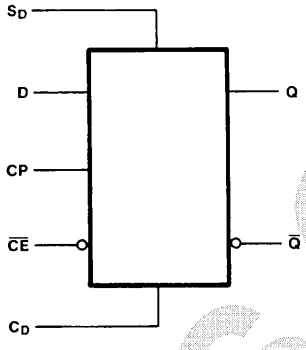
General Description

The 11C70 is a high-speed ECL D-Type Master-Slave Flip-Flop capable of toggle rates over 650 MHz. Designed primarily for communications and instrumentation, it can also be used in other digital applications and is fully compatible with 10K ECL. Asynchronous Direct Set and Direct Clear inputs are provided which override the clock.

The circuit is voltage-compensated, which makes output levels and input thresholds insensitive to V_{EE} variations. This also allows operation with ECL supply voltage V_{EE} of −5.2V or with TTL supply V_{CC} of +5.0V. Each input has an internal 50 kΩ pull-down resistor, which allows unused inputs to be left open. Open emitter-follower outputs accommodate a variety of loading and terminating schemes. The 11C70 is pin-compatible with the Motorola MC1670 but is a higher-frequency replacement.

Ordering Code: See Section 6

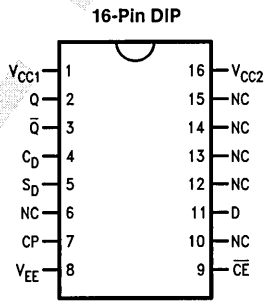
Logic Symbol



TL/F/9891–2

Connection Diagram

16-Pin DIP



TL/F/9891–1

Pin Names	Description
$\overline{CE}$	Clock Enable (Active LOW)
CP	Clock Pulse
D	Data Input
Q, $\overline{Q}$	Outputs
S_D	Direct Set
C_D	Direct Clear

Truth Table

Inputs					Q_{t+1}	Operation
S_D	C_D	D	$\overline{CE}$	CP		
H	L	X	X	X	H	Direct Set
L	H	X	X	X	L	Direct Clear
H	H	X	X	X	—	Intermediate
L	L	X	H	↗	Q_t	Disable Clock
L	L	H	L	↗	H	Clocked Set
L	L	L	L	↗	L	Clocked Clear

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
↗ = LOW to HIGH Transition
t, t+1 = Time Before and After Clock Positive Transition

Absolute Maximum Ratings

Above which the useful life may be impaired

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Maximum Junction Temperature (T_J)	+150°C
Supply Voltage Range	−7.0V to GND
Input Voltage (DC)	V_{EE} to GND
Output Current (DC Output HIGH)	−50 mA
Operating Range	−5.7V to −4.7V
Lead Temperature (Soldering, 10 sec.)	300°C

Recommended Operating Conditions

	Min	Typ	Max
Supply Voltage (V_{EE})	−5.7V	−5.2V	−4.7V
Ambient Temperature (T_A)	0°C		+75°C

DC Electrical Characteristics

V_{EE} = −5.2V, V_{CC} = GND

Symbol	Parameter	Min	Typ	Max	Units	T_A	Conditions
V_{OH}	Output Voltage HIGH	−1000		−840	mV	0°C	V_{IN} = V_{IHA} or V_{ILB} per Truth Table Loading 50Ω to −2V
		−960		−810	mV	+25°C	
		−900		−720	mV	+75°C	
V_{OL}	Output Voltage LOW	−1870		−1665	mV	0°C	
		−1850		−1620	mV	+25°C	
		−1850		−1595	mV	+75°C	
V_{OHC}	Output Voltage HIGH	−1020			mV	0°C	V_{IN} = V_{IHB} or V_{ILA} for D Input Loading 50Ω to −2V
		−980			mV	+25°C	
		−920			mV	+75°C	
V_{OLC}	Output Voltage LOW			−1615	mV	0°C	
				−1600	mV	+25°C	
				−1575	mV	+75°C	
V_{IH}	Input Voltage HIGH	−1135		−840	mV	0°C	Guaranteed Input Voltage HIGH for All Inputs
		−1095		−810	mV	+25°C	
		−1035		−720	mV	+75°C	
V_{IL}	Input Voltage LOW	−1870		−1500	mV	0°C	Guaranteed Input Voltage LOW for All Inputs
		−1850		−1485	mV	+25°C	
		−1830		−1460	mV	+75°C	
I_{IH}	Input Current HIGH					+25°C	V_{IN} = V_{IHA}
	Clock Input			250	μA		
	Data Input			270	μA		
	S_D and C_D			550	μA		
I_{IL}	Input Current LOW	0.5			μA	+25°C	V_{IN} = V_{IHB}
I_{EE}	Power Supply Current	−48			mA	+25°C	All Inputs Open

AC Electrical Characteristics

V_{EE} = −5.2V, V_{CC} = GND, T_A = +25°C

Symbol	Parameter	Min	Typ	Max	Units	Conditions
t_{PLH}, t_{PHL}	Propagation Delay (CP-Q)		1.1	1.4	ns	See *Figures 3* and *4*
t_{PLH}, t_{PHL}	Propagation Delay (S_D-$\overline{Q}$, C_D-Q)		1.3	1.7	ns	
t_{TLH}	Transition Time 20% to 80%		0.9	1.3	ns	
t_{THL}	Transition Time 80% to 20%		0.9	1.3	ns	
$f_{TOG\ (MAX)}$	Toggle Frequency (CP)	550	650		MHz	See *Figure 2*

Note: This device is guaranteed for $f_{TOG(max)} \geq$ 500 MHz over the 0°C to +75°C temperature range.

Functional Description

Master and slave clock thresholds are internally offset in opposite directions to avoid race conditions or simultaneous master-slave changes when the clock has slow rise or fall times. While the clock is LOW, the slave is in a HOLD condition and information present on the D input is gated into the master. When the clock goes HIGH, it locks the master into its present state, making it insensitive to the D input, causing the new information to appear on the outputs.

The CP and $\overline{CE}$ inputs are logically identical, but physical constraints associated with the Dual In-Line package make the $\overline{CE}$ input slower at the upper end of the toggle range. To prevent new data from entering the master on the next CP LOW cycle, $\overline{CE}$ should be HIGH while CP is still HIGH.

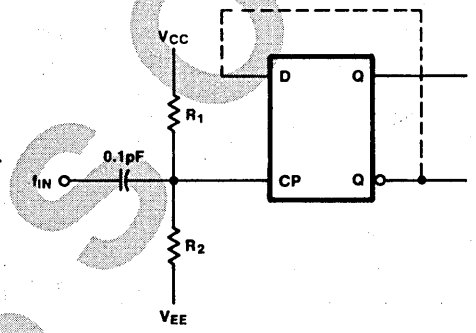
A HIGH signal on S_D or C_D will override the clocked inputs and force Q or $\overline{Q}$, respectively, to go HIGH. If both C_D and S_D are HIGH, the two output voltages will be somewhere between the HIGH and LOW levels and thus, cannot be usefully defined.

When the input signals for the 11C70 come from other ECL circuits, either 11CXX series or 10K types, these circuits will automatically provide appropriate signal swings, provided, of course, that these circuits are operated within their ratings and that due consideration is given to terminations appropriate to the particular application, as discussed in the F100K ECL Design Guide (Section 5 of Databook).

For applications where the clock signal comes from a circuit type other than ECL (in high frequency prescaling, for example) it is generally necessary to use external components to shift the signal levels and center them about the 11C70 input threshold region. A typical biasing scheme is shown in *Figure 1*. Resistors R1 and R2 are chosen such that the quiescent voltage at the CP input is −1.3V with respect to the V_{CC} terminal of the 11C70. Also indicated is the coupling from $\overline{Q}$ back to the D input to make a simple toggle. The clock source should be designed to provide a signal swing in the range of 400 mV to 1200 mV, peak-to-peak, over the specified frequency and temperature range. To avoid saturating the input transistor, and thus limiting the frequency capability, the positive peak of the clock should not be more positive than −0.4V with respect to V_{CC}.

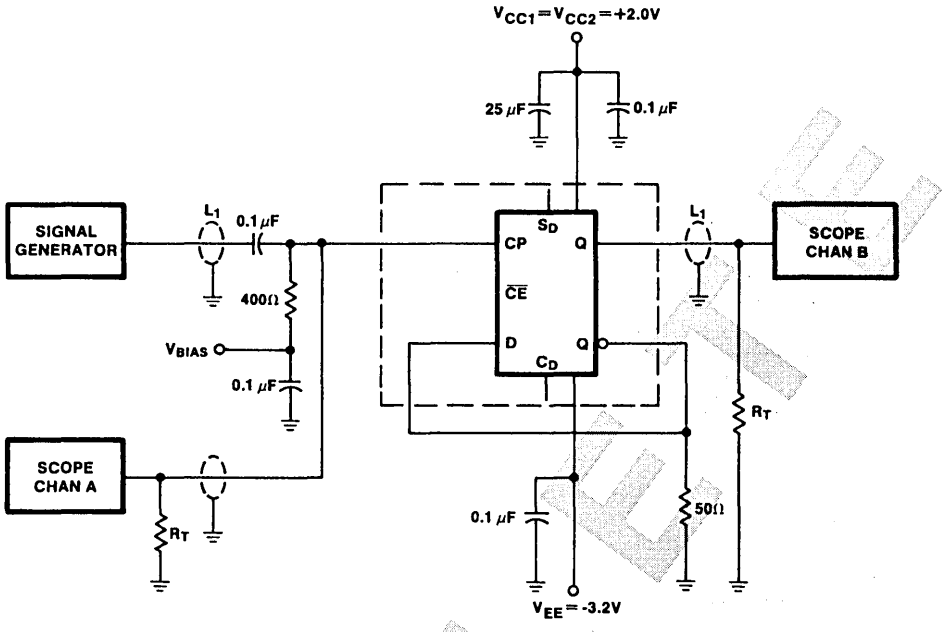
The 11C70 outputs have no internal pull-down resistors. When driving a microstrip line terminated at the far end by a resistor returned to −2V (w.r.t. V_{CC}), the quiescent I_{OH} current in the line performs the pull-down function when the output starts to go LOW. For series termination or for short unterminated lines, a 270Ω resistor to V_{EE} will provide adequate pull-down current. The outputs switch slightly faster when both outputs are equally loaded than if only one output is loaded. Equal and opposite changes in Q and $\overline{Q}$ load currents tend to cancel the effects of the small inductance of the V_{CC} pin.

The test arrangements illustrate the use of split power supplies, with a 2V V_{CC} and −3.2V V_{EE}. This is done as a matter of instrumentation convenience, since it allows the outputs to be connected via 50Ω cables directly to the sampling scope inputs, which have 50Ω internal terminations. By thus avoiding the use of probes, test correlation problems between supplier and user are minimized. In actual applications, only a single power supply is needed, and ground can be assigned to V_{CC}, as in ECL systems or to V_{EE} side as in TTL systems. RF bypass capacitors are recommended in either case.



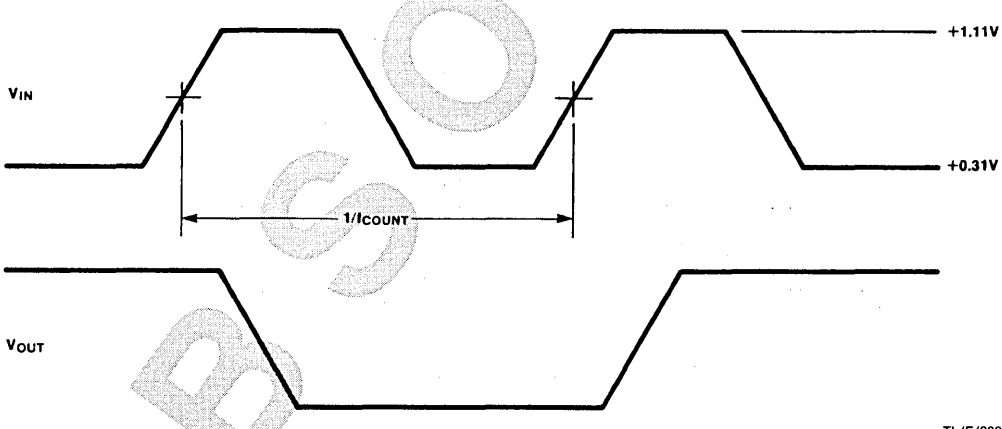
TL/F/9891–3

FIGURE 1. Input Biasing for AC Coupled Triggering



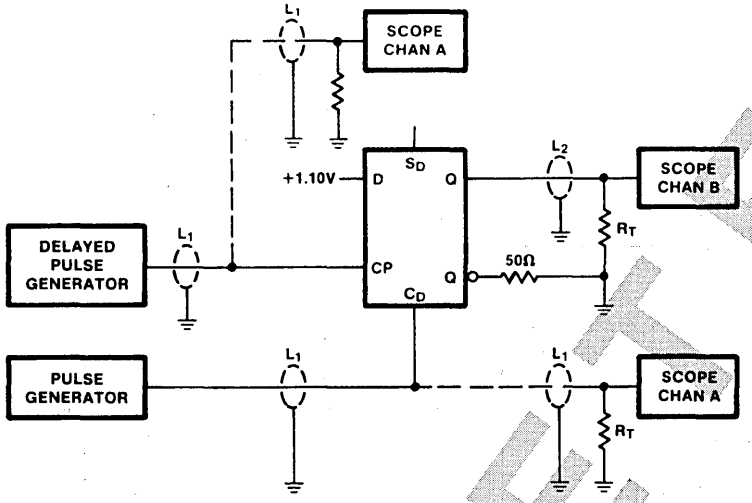
TL/F/9891–4

R_T = 50Ω termination of scope
L_1 = 50Ω impedance lines
Adjust V_{BIAS} for ±0.7V baseline of 800 mV peak-to-peak sinewave input



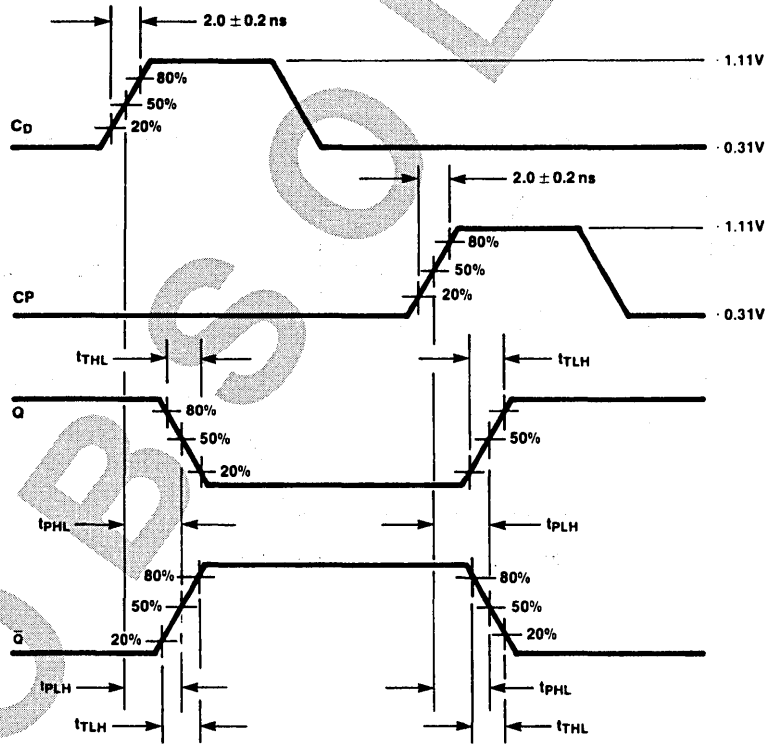
TL/F/9891–5

FIGURE 2. Toggle Frequency Test Circuit



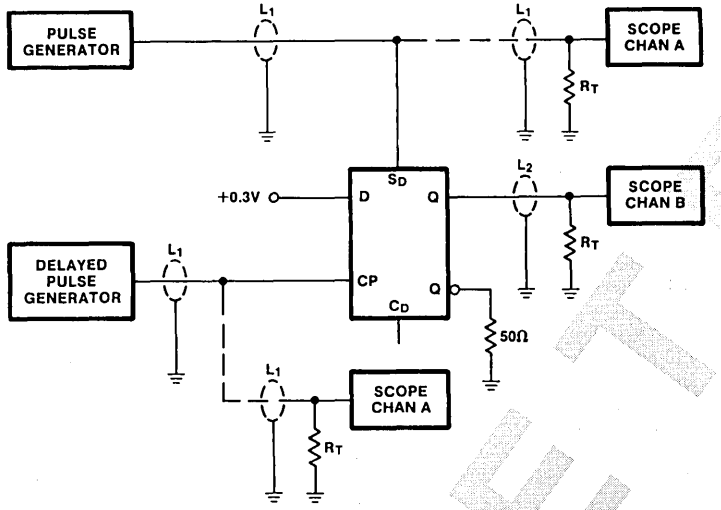
TL/F/9891–6

$V_{CC1} = V_{CC2} = +2.0V$
$V_{EE} = -3.2V$
$R_T = 50\Omega$ termination of scope
L_1, L_2 = equal 50Ω impedance lines
All input transition times are 2.0 ns ±0.2 ns



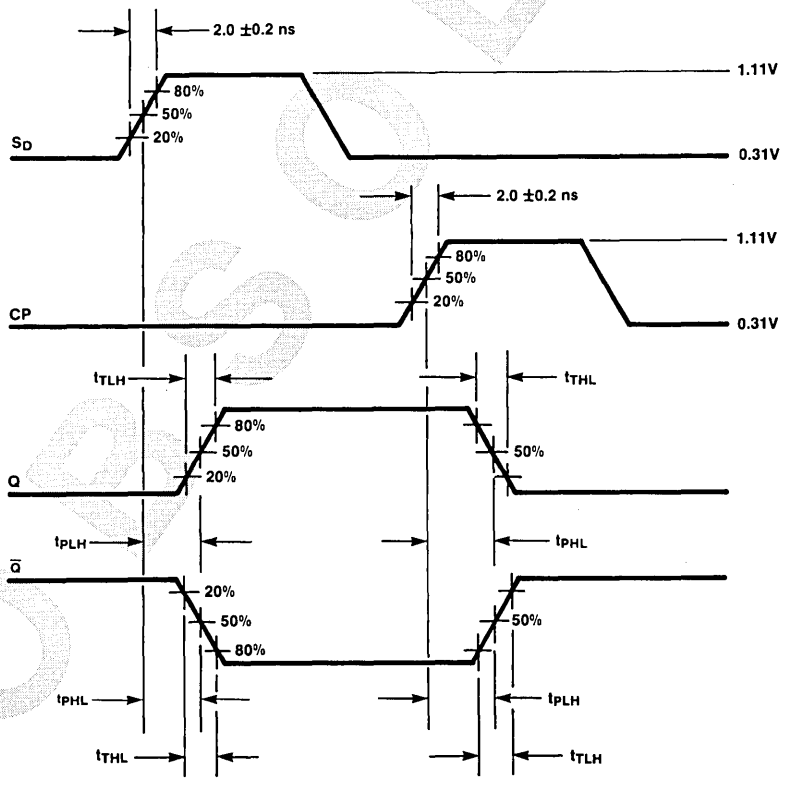
TL/F/9891–7

FIGURE 3. Propagation Delay and C_D Test Circuit



TL/F/9891–8

$V_{CC1} = V_{CC2} = +2.0V$
$V_{EE} = -3.2V$
$R_T = 50\Omega$ termination of scope
L_1, L_2 = equal 50Ω impedance lines
All input transition times are 2.0 ns ±0.2 ns



TL/F/9891–9

FIGURE 4. Propagation Delay and S_D Test Circuit

National Semiconductor

Not Intended For New Designs

11C90/11C91
650 MHz Prescalers

General Description

The 11C90 and 11C91 are high-speed prescalers designed specifically for communication and instrumentation applications. All discussions and examples in this data sheet are applicable to the 11C91 as well as the 11C90.

The 11C90 will divide by 10 or 11 and the 11C91 by 5 or 6, both over a frequency range from DC to typically 650 MHz. The division ratio is controlled by the Mode Control. The divide-by-10 or -11 capability allows the use of pulse swallowing techniques to control high-speed counting modulos by lower-speed circuits. The 11C90 may be used with either ECL or TTL power supplies.

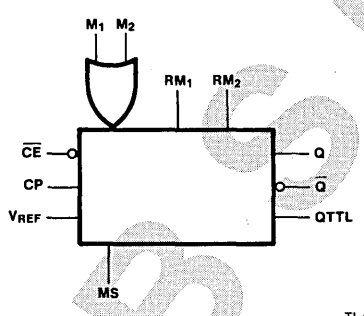
In addition to the ECL outputs Q and $\overline{Q}$, the 11C90 contains an ECL-to-TTL converter and a TTL output. The TTL output operates from the same V_{CC} and V_{EE} levels as the counter, but a separate pin is used for the TTL circuit V_{EE}. This minimizes noise coupling when the TTL output switches and also allows power consumption to be reduced by leaving the separate V_{EE} pin open if the TTL output is not used.

To facilitate capacitive coupling of the clock signal, a 400Ω resistor (V_{REF}) is connected internally to the V_{BB} reference. Connecting this resistor to the Clock Pulse input (CP) automatically centers the input about the switching threshold. Maximum frequency operation is achieved with a 50% duty cycle.

Each of the Mode Control inputs is connected to an internal 2 kΩ resistor with the other end uncommitted (RM_1 and RM_2). An M input can be driven from a TTL circuit operating from the same V_{CC} by connecting the free end of the associated 2 kΩ resistor to V_{CCA}. When an M input is driven from the ECL circuit, the 2 kΩ resistor can be left open or, if required, can be connected to V_{EE} to act as a pull-down resistor.

Ordering Code: See Section 6

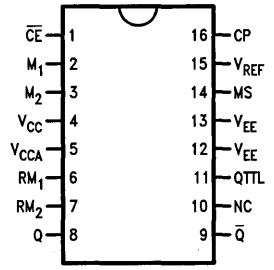
Logic Symbol



TL/F/9892–2

Connection Diagram

16-Pin DIP



TL/F/9892–1

Pin Names	Description
$\overline{CE}$	Count Enable Input (Active LOW)
CP	Clock Pulse Input
M_n	Count Modulus Control Input
MS	Asynchronous Master Set Input
Q, $\overline{Q}$	ECL Outputs
QTTL	TTL Output
RM_n	2 kΩ Resistor to M_n
V_{REF}	400Ω Resistor to V_{BB}

Absolute Maximum Ratings

Above which the useful life may be impaired

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Maximum Junction Temperature (T_J)	+150°C
Supply Voltage Range	−7.0V to GND
Input Voltage (DC)	V_{EE} to GND
Output Current (DC Output HIGH)	−50 mA
Operating Range	−5.7V to −4.7V
Lead Temperature (Soldering, 10 sec.)	300°C

Recommended Operating Conditions

	Min	Typ	Max
Ambient Temperature (T_A)			
Commercial	0°C		+75°C
Military	−55°C		+125°C
Supply Voltage (V_{EE})			
Commercial	−5.7V	−5.2V	−4.7V
Military	−5.7V	−5.2V	−4.7V

TTL Input/Output Operation

DC Electrical Characteristics

Over Operating Temperature and Voltage Range unless otherwise noted, Pins 12 and 13 = GND

Symbol	Parameter	Min	Typ (Note 3)	Max	Units	Conditions
V_{IH}	Input HIGH Voltage M_1 and M_2 Inputs		4.1		V	Guaranteed Input HIGH Threshold Voltage (Note 4), $V_{CC} = V_{CCA} = 5.0V$
V_{IL}	Input LOW Voltage M_1 and M_2 Inputs		3.3		V	Guaranteed Input LOW Threshold Voltage (Note 4), $V_{CC} = V_{CCA} = 5.0V$
V_{OH}	Output HIGH Voltage QTTL Output	2.3	3.3		V	$V_{CC} = V_{CCA} = Min$, $I_{OH} = -640\ \mu A$
V_{OL}	Output LOW Voltage QTTL Output		0.2	0.5	V	$V_{CC} = V_{CCA} = Min$, $I_{OL} = 20.0$ mA
I_{IL}	Input LOW Current M_1 and M_2 Inputs		−2.3	−5.0	mA	$V_{CC} = V_{CCA} = Max$, $V_{IN} = 0.4V$, Pins 6, 7 = V_{CC}
I_{SC}	Output Short Circuit Current	−20	−35	−80	mA	$V_{CC} = V_{CCA} = Max$, $V_{OUT} = 0.0V$, Pin 14 = V_{CC}

AC Electrical Characteristics

$V_{CC} = V_{CCA} = 5.0V$ Nominal, V_{EE} = GND, $T_A = +25°C$

Symbol	Parameter	Min	Typ	Max	Units	Conditions
t_{PLH} t_{PHL}	Propagation Delay, (50% to 50%) CP to QTTL	6	10	14	ns	See *Figure 1*
t_{PLH}	Propagation Delay, (50% to 50%) MS to QTTL		12	17	ns	
t_s	Mode Control Setup Time	4	2		ns	
t_h	Mode Control Hold Time	0	−2		ns	
t_{TLH}	Output Rise Time (20% to 80%)		10		ns	
t_{THL}	Output Fall Time (80% to 20%)		2		ns	
f_{MAX}	Count Frequency	550 600	650 650		MHz	−55°C to +125°C 0°C to +75°C Clock Input AC Coupled 350 mV Peak-to-Peak Sinewave (Note 5)

ECL Operation—Commercial Version

DC Electrical Characteristics

$V_{CC} = V_{CCA} = GND$, $V_{EE} = -5.2V$

Symbol	Parameter	Min	Typ	Max	Units	T_A	Conditions
V_{OH}	Output HIGH Voltage Q and $\overline{Q}$	−1060 −1025 −980	−995 −960 −910	−905 −880 −805	mV	0°C +25°C +75°C	Load = 50Ω to −2V
V_{OL}	Output LOW Voltage Q and $\overline{Q}$	−1820	−1705	−1620	mV	0°C to +75°C	
V_{IH}	Input HIGH Voltage	−1135 −1095 −1035		−840 −810 −720	mV	0°C +25°C +75°C	Guaranteed Input HIGH Signal (Note 6)
V_{IL}	Input LOW Voltage	−1870 −1850 −1830		−1500 −1485 −1460	mV	0°C +25°C +75°C	Guaranteed Input LOW Signal
I_{IH}	Input HIGH Current CP Input (Note 1) MS Input M_1 and M_2 Input			 400 400 250	 μA	 +25°C +25°C +25°C	$V_{IN} = V_{IHA}$
I_{IL}	Input LOW Current	0.5			μA	+25°C	$V_{IN} = V_{ILB}$
I_{EE}	Power Supply Current	−110 −119	−75		mA	0°C to +75°C	Pins 6, 7, 13 not connected
V_{EE}	Operating Supply Voltage Range	−5.7	−5.2	−4.7	V	0°C to +75°C	
V_{REF}	Reference Voltage	−1550		−1150	mV	+25°C	$V_{RM_1} = V_{RM_2} = -5.2V$ $I_N = -10.0\ \mu A$

AC Electrical Characteristics

$T_A = 0°C$ to $+75°C$, $V_{CC} = V_{CCA} = GND$, $V_{EE} = -5.2V$

Symbol	Parameter	0°C Typ	+25°C Min	+25°C Typ	+25°C Max	+75°C Typ	Units	Conditions
t_{PLH} t_{PHL}	Propagation Delay, (50% to 50%) CP to Q	1.8	1.3	2.0	3.0	2.5	ns	Output: $R_L = 50\Omega$ to $-2.0V$
t_{PLH}	Propagation Delay, (50% to 50%) MS to Q	3.7		4.0	6.0	4.5	ns	Input: $t_{ri} = t_{fi} = 2.0 \pm 0.1$ ns (20% to 80%) See *Figure 1*
t_s	Setup Time, M to CP	2.0	4.0	2.0		2.0	ns	
t_h	Hold Time, M to CP	−2.0	0.0	−2.0		−2.0	ns	
t_{TLH}	Output Rise Time (20% to 80%)	1.0		1.0	2.0	1.0	ns	
t_{THL}	Output Fall Time (80% to 20%)	1.0		1.0	2.0	1.0	ns	
f_{MAX}	Maximum Clock Frequency	650	600	650		625	MHz	AC Coupled Input 350 mV Peak-to-Peak. f_{MAX} is Guaranteed to be 575 MHz Min at 0°C to +75°C.

ECL Operation—Military Version

DC Electrical Characteristics

$V_{CC} = V_{CCA} = GND$, $V_{EE} = -5.2V$

Symbol	Parameter	Min	Typ	Max	Units	T_A	Conditions
V_{OH}	Output HIGH Voltage Q and $\overline{Q}$	−1100 −980 −910	−1030 −910 −820	−900 −820 −670	mV	−55°C +25°C +125°C	Load = 100Ω to −2V
V_{OL}	Output LOW Voltage Q and $\overline{Q}$	−1820	−1705	−1620	mV	−55°C to +125°C	
V_{IH}	Input HIGH Voltage	−1190 −1095 −975		−905 −810 −690	mV	−55°C +25°C +125°C	Guaranteed Input HIGH Signal (Note 6)
V_{IL}	Input LOW Voltage	−1890 −1850 −1800		−1525 −1485 −1435	mV	−55°C +25°C +125°C	Guaranteed Input LOW Signal
I_{IH}	Input HIGH Current CP Input (Note 1) MS Input M_1 and M_2 Input			 400 400 250	 μA	 +25°C +25°C +25°C	$V_{IN} = V_{IHA}$
I_{IL}	Input LOW Current	0.5			μA	+25°C	$V_{IN} = V_{ILB}$
I_{EE}	Power Supply Current	−110	−75		mA	+25°C	Pins 6, 7, 13 not connected
			−119		mA	−55°C to +125°C	
V_{EE}	Operating Supply Voltage Range	−5.7	−5.2	−4.7	V	−55°C to +125°C	
V_{REF}	Reference Voltage	−1550		−1150	mV	+25°C	$V_{RM_1} = V_{RM_2} = -5.2V$ $I_N = -10.0\ \mu A$

AC Electrical Characteristics

$T_A = -55°C$ to $+125°C$, $V_{CC} = V_{CCA} = GND$, $V_{EE} = -5.2V$

Symbol	Parameter	−55°C Typ	+25°C Min	+25°C Typ	+25°C Max	+125°C Typ	Units	Conditions
t_{PLH} t_{PHL}	Propagation Delay, (50% to 50%) CP to Q	1.5	1.3	2.0	3.0	3.0	ns	Output: $R_L = 50\Omega$ to −2.0V
t_{PLH}	Propagation Delay, (50% to 50%) MS to Q	3.5		4.0	6.0	5.0	ns	Input: $t_{ri} = t_{fi} = 2.0 \pm 0.1$ ns (20% to 80%) See *Figure 1*
t_s	Setup Time, M to CP	2.0	4.0	2.0		2.0	ns	
t_h	Hold Time, M to CP	−2.0	0.0	−2.0		−2.0	ns	
t_{TLH}	Output Rise Time (20% to 80%)	1.0		1.0	2.0	1.0	ns	
t_{THL}	Output Fall Time (80% to 20%)	1.0		1.0	2.0	1.0	ns	
f_{MAX}	Maximum Clock Frequency	700	600	650		600	MHz	AC Coupled Input 350 mV Peak-to-Peak. f_{MAX} is Guaranteed to be 550 MHz Min at −55°C to +125°C.

Note 1: Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.

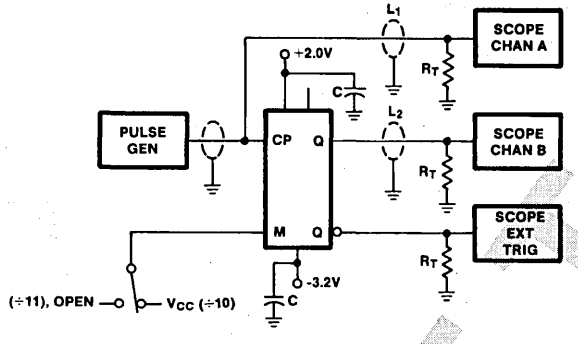
Note 2: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 3: Typical limits are at $V_{CC} = 5.0V$ and $T_A = +25°C$.

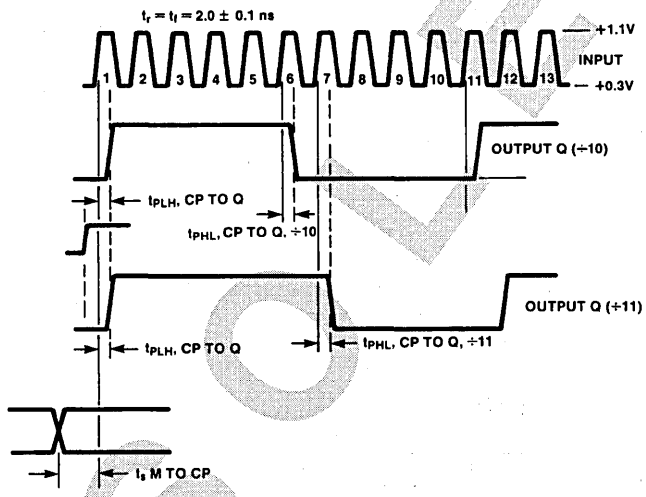
Note 4: The M_1 and M_2 threshold specifications are normally referenced to the V_{CC} potential, as shown in the ECL operation tables. Using V_{EE} (GND) as the reference, as in normal TTL practice, effectively makes the threshold vary directly with V_{CC}. Threshold is typically 1.3V below V_{CC} (e.g., +3.7V at $V_{CC} = +5V$). A signal swing about threshold of ±0.4V is adequate, which gives the state V_{IH} and V_{IL} values. The internal 2 kΩ resistors are intended to pull TTL outputs up to the required V_{IH} range, as discussed in the Functional Description and shown in *Figure 5.*

Note 5: TTL Output Signal swing is guaranteed at f_{MAX} over temperature range.

Note 6: M_1 or M_2 can be tied to V_{CC} for fixed divide-by-ten operation.



TL/F/9892–3



TL/F/9892–4

Conditions:

V_{CC} = +2.0V
V_{EE} = −3.2V
R_T = 50Ω (scope input impedance)
C_L = Jig and stray capacitance < 5.0 pF
l_1 = L_2 = equal 50Ω impedance lines
C = 0.1 pF

Note 7: Use high impedance to test QTTL.
Connect pin 13 to V_{EE}.

Note 8: For High frequency test use AC coupled input as in *Figure 3*.
Adjust input amplitude to 350 mV peak-to-peak.

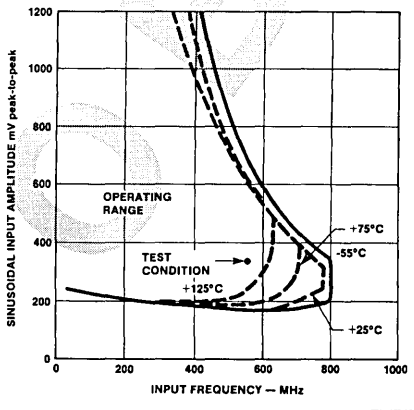
FIGURE 1. AC Test Circuit

Functional Description

The 11C90 contains four ECL Flip-Flops, an ECL to TTL converter and a Schottky TTL output buffer with an active pull-up. Three of the Flip-Flops operate as a synchronous shift counter driving the fourth Flip-Flop operating as an asynchronous toggle. The internal feedback logic is such that the TTL output and the Q ECL output are HIGH for six clock periods and LOW for five clock periods. The Mode Control (M) inputs can modify the feedback to make the output HIGH for five clock periods and LOW for five clock periods, as indicated in the Count Sequence Table.

The feedback logic is such that the instant the output goes HIGH, the circuit is already committed as to whether the output period will be 10 or 11 clock periods long. This means that subsequent changes in an M input signal, including decoding spikes, will have no effect on the current output period. The only timing restriction for an M input signal is that it be in the desired state at least a setup time before the clock that follows the HHLL state shown in the table. The allowable propagation delay through external logic to an M input is maximized by designing it to use the positive transition of the 11C90 output as its active edge. This gives an allowable delay of ten clock periods, minus the CP to Q delay of the 11C90 and the M to CP setup time. If the external logic uses the negative output transition as its active edge, the allowable delay is reduced to five clock periods minus the previously mentioned delay and setup time.

Capacitively coupled triggering is simplified by the 400Ω resistor which connects pin 15 to the internal V_{BB} reference. By connecting this to the CP input, as shown in *Figure 3*, the clock is automatically centered about the input threshold. A clock duty cycle of 50% provides the fastest operation, since the Flip-Flops are Master-Slave types with offset clock thresholds between master and slave. This feature ensures that the circuit will operate with clock waveforms having very slow rise and fall times, and thus, there is no maximum frequency restriction. Recommended minimum and maximum clock amplitude as a function of a frequency and temperature are shown in the graph labeled *Figure 2*. When the CP or any other input is driven from another ECL circuit, normal ECL termination methods are recommended. One method is indicated in *Figure 4*. Other ECL termination methods are discussed in the F100K ECL Design Guide (Section 5 of Databook).



TL/F/9892–5

FIGURE 2. AC Coupled Triggering Characteristics

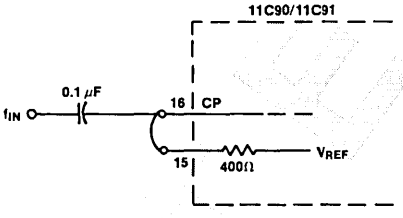


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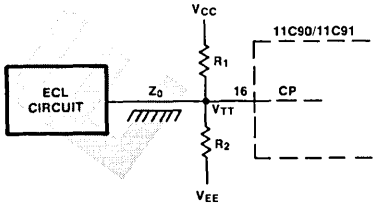
FIGURE 3. Capacitively Coupled Clocking



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$Z_O\Omega$	50	75	100
$R_1\Omega$	80.6	121	162
$R_2\Omega$	130	196	261

V_{EE} = −5.2V, V_{CC} = 0V, V_{TT} = −2.0V

FIGURE 4. Clocking by ECL Source via Terminated Line

When an M input is to be driven from a TTL output operating from the same V_{CC} and ground (V_{EE}), the internal 2 kΩ resistor can be used to pull the TTL output up as shown in *Figure 5*. Some types of TTL outputs will only pull up to within two diode drops of V_{CC}, which is not high enough for 11C90 inputs. The resistor will pull the signal up through the threshold region, although this final rise may be somewhat slow, depending on wiring capacitance. A resistor network that gives faster rise and also lower impedance is shown in *Figure 6*.

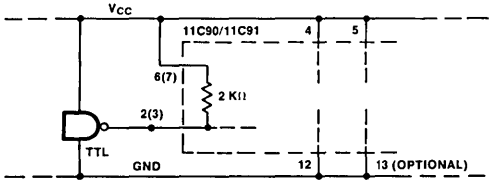

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FIGURE 5. Using Internal Pull-Up with TTL Source

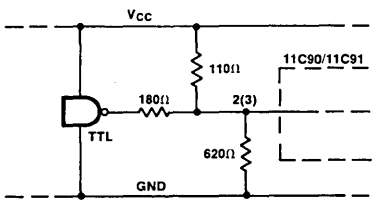

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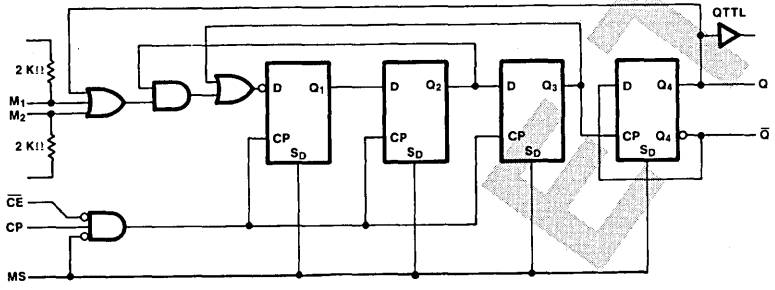
FIGURE 6. Faster Low Impedance TTL to ECL Interface

Functional Description (Continued)

The ECL outputs have no pull-down resistors and can drive series or parallel terminated transmission lines. For short interconnections that do not require impedance matching, a 270Ω to 510Ω resistor to V_{EE} can be used to establish the V_{OL} level. Both V_{CC} pins must always be used and should be connected together as close to the package as possible. Pin 12 must always be connected to the V_{EE} side of the supply, while pin 13 is required only if the TTL output is used. Low impedance V_{CC} and V_{EE} distribution and RF bypass capacitors are recommended to prevent crosstalk.

Logic Diagram 11C90



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Note: This diagram is provided for understanding of logic operation only. It should not be used for evaluation of propagation delays as many internal functions are achieved more efficiently than shown.

Count Sequence Table 11C90

	Q_1	Q_2	Q_3	Q_4(QTTL)	
	H	H	H	H	÷11
÷10	L	H	H	H	
	L	L	H	H	
	L	L	L	H	
	H	L	L	H	
	H	H	L	H	
	L	H	H	L	
	L	L	H	L	
	L	L	L	L	
	H	L	L	L	
	H	H	L	L	

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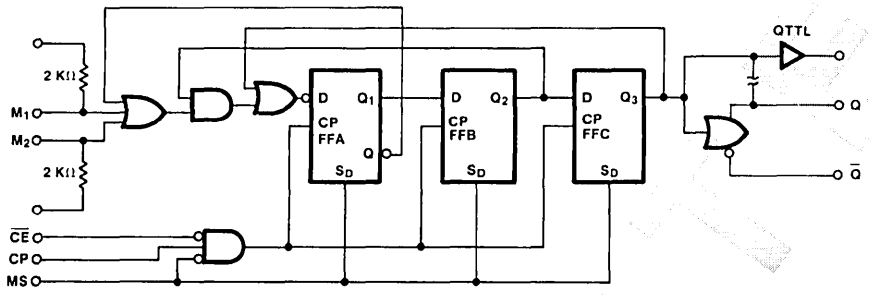
Note: A HIGH on MS forces all Qs HIGH.

Operating Mode Table 11C90

Inputs				Output Response
MS	$\overline{CE}$	M_1	M_2	
H	X	X	X	Set HIGH
L	H	X	X	Hold
L	L	L	L	÷11
L	L	H	X	÷10
L	L	X	H	÷10

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

Logic Diagram 11C91



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Count Sequence Table 11C91

	Q_1	Q_2	Q_3(QTTL)	
	H	H	H	÷6
÷5	L	H	H	
	L	L	H	
	L	L	L	
	H	L	L	
	H	H	L	

TL/F/9892–9

Note: A HIGH on MS forces all Qs HIGH.

Operating Mode Table 11C91

Inputs				Output Response
MS	$\overline{CE}$	M_1	M_2	
H	X	X	X	Set HIGH
L	H	X	X	Hold
L	L	L	L	÷6
L	L	X	H	÷5
L	L	H	X	÷5

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

Section 5

F100K ECL Design Guide and Application Notes

Section 5 Contents

National Semiconductor

Chapter 1
Circuit Basics

Introduction

ECL circuits, except for the simplest elements, are schematically formidable and many of the specified parameters are relatively unfamiliar to system designers. The relationships between external parameters and internal circuitry are best determined by individually examining the fundamental subcircuits of a simple element.

Basic ECL Switch

At the bottom of every ECL circuit, literally and figuratively, is a current source. In the basic ECL switch *(Figure 1-1)*, a logic operation consists of steering the current through either of two return paths to V_{CC}; the state of the switch can be detected from the resultant voltage drop across R1 or R2. The net voltage swing is determined by the value of the resistors and the magnitude of the current. Further, these two values are chosen to accomplish the charging and discharging of all of the parasitic capacitances at the desired switching rate.

Required Input Signal

The voltage swing required to control the state of the switch is relatively small due to the exponential change of emitter current with base-emitter voltage and to the differential mode of operation. For example, starting from a condition where the two base voltages are equal, which causes the current to divide equally between Q1 and Q2, an increase of V_{IN} by 125 mV causes essentially all of the current to flow through Q1. Conversely, decreasing V_{IN} by 125 mV causes essentially all of the current to flow through Q2. Thus the minimum signal swing required to accomplish switching is 250 mV centered about V_{BB}. The signal swing is made larger (approximately 750 mV) to provide noise immunity and to allow for differences between the V_{BB} of one circuit and the output voltage levels of another circuit driving it.

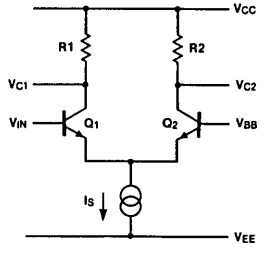

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FIGURE 1-1. Basic ECL Switch

Transition Region

If the voltage at the collector of Q1 is monitored while varying V_{IN} above and below the value of V_{BB}, the relationship between V_{C1} and V_{IN} appears as shown in *Figure 1-2*. Note that the horizontal axis of the graph is centered on V_{BB}; this emphasizes the importance of V_{BB} in fixing the location of the transition region. The shape of the transition (or threshold) region is governed by the transistor characteristics and the value of current to be switched. Both of these factors are determined by the circuit designer. The shape of the transition region is essentially invariant over a broad range of conditions, due to the matching of transistor characteristics inherent with IC technology and because the transistors are at the same temperature. The inherent matching of IC resistors assures equal voltage swings at the two collectors.

Emitter-Follower Buffers

In *Figure 1-2*, V_{C1} ranges from V_{CC} (ground) when Q1 is off to approximately −0.90V when Q1 is conducting all of the source current. To make these voltage levels compatible with the voltages required to drive the input of another current switch, emitter followers are added as shown in the buffered current switch *(Figure 1-3)*. In addition to translating V_{C1} and V_{C2} downward, the emitter followers also isolate the collector nodes from load capacitance and provide current gain. Since the output impedance of the emitter followers is low (approximately 7Ω), ECL circuits can drive transmission lines—coaxial cables, twisted pairs, and etched circuits—having characteristic impedances of 50Ω or more.

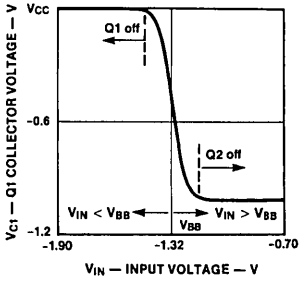

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FIGURE 1-2. V_{C1}–V_{IN} Transition Region

5

Emitter-Follower Buffers (Continued)

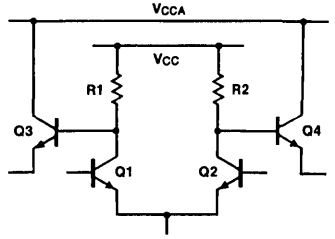

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FIGURE 1-3. Buffered Current Switch

In this buffered current switch, the collectors of Q3 and Q4 return to a separate ground lead, V_{CCA}. This separation insures that any changes in load currents during switching do not cause a change in V_{CC} through the small but finite inductance of the V_{CCA} bond wire. V_{CC} and V_{CCA} are joined together on the leadframe of the package. Outside the package, the V_{CC} and V_{CCA} leads should be connected to the common V_{CC} distribution.

For internal functions of complex circuits where loading is minimal, the buffer transistors are scaled down to maintain high switching speeds with modest source currents. For service as output buffers, the emitter followers are designed for a maximum rated output current of 50 mA. For standardization of testing, detailed specifications on guaranteed min/max output levels apply when an output is loaded with 50Ω returned to −2V. The emitter followers have no internal pull-down resistors; consequently, there is maximum design flexibility when optimizing line terminations and using wired-OR techniques for combinatorial logic or data bussing.

Multiple Inputs

The buffered switch of *Figure 1-3* is essentially an ECL line receiver circuit with the bases of both Q1 and Q2 available for receiving differential signals. With one input connected to the V_{BB} terminal, the switch can receive a signal transmitted in a single-ended mode or it can act as a buffer or logic inverter. To perform the OR and NOR of two or more functions, additional transistors are connected in parallel with Q1 as indicated in *Figure 1-4*. When any input is HIGH, its associated transistor conducts the source current and Q2 is turned off; this causes the collector of Q1 to go LOW and the collector of Q2 to go HIGH, with the emitters of Q3 and Q4 following the collectors of Q1 and Q2 respectively. When two or more inputs are HIGH, the results are the same. Thus, with a HIGH level defined as a True or logic "1" signal, Q3 provides the NOR of the inputs while Q4 simultaneously provides the OR. In addition to the logic design flexibility afforded by the availability of both the assertion and negation, the Q3 and Q4 outputs can drive both conductors of a differential pair for data transmission. Also shown in *Figure 1-4* are the pull-down resistors, nominally 50 kΩ, connected between ECL inputs and the negative supply. These resistors serve the purpose of holding unused inputs in the LOW state by sinking I_{CBO} current and preventing the build-up of charge on input capacitances. Accordingly, most non-essential ECL inputs are designed to be active HIGH. When such inputs are not used, the pull-down resistors eliminate the need for external wiring to hold them LOW.

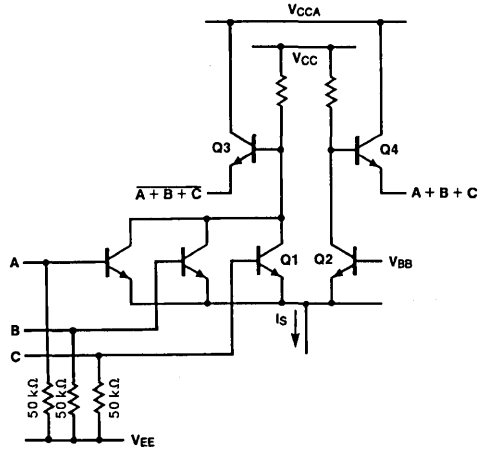

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FIGURE 1-4. Input Expansion by Parallel Transistors

Power Conservation, Complementary Functions

Power dissipation in an ECL circuit is due in part to the output load currents and in part to the internal operating currents. Load currents depend on system design factors and are discussed in Chapter 5. In the basic switch *(Figure 1-1)*, power dissipation is fixed by the source current and the supply voltage, whether the circuit is in a quiescent or transient state. There is no mechanism for causing a current spike such as occurs in TTL circuits, and thus the power dissipation is not a function of switching frequency.

A distinct advantage of the ECL switch is the ease of forming both the assertion and negation of a function without additional time delay or complexity. This is very significant in complex MSI functions, since it helps to maximize the efficiency of the internal logic while minimizing chip area and power consumption. Since most 100K ECL devices have complementary outputs, the system designer has similar opportunities to reduce package count and power consumption while enhancing logic efficiency and reducing throughput times.

Series Gating, Wired-AND

Quite often in ECL elements, the circuitry required to generate functions is much simpler than the detailed logic diagrams suggest. In addition to readily available complementary functions and the wired-OR option, other techniques providing high performance with low part count are series gating and wired collectors. These are illustrated in principle by the simplified schematics of *Figures 1-5* and *1-6*.

Series Gating, Wired-AND (Continued)

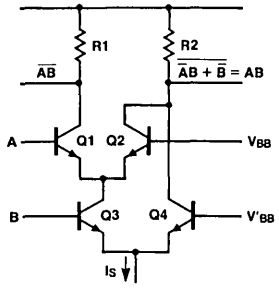

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FIGURE 1-5. Series/Parallel Gating

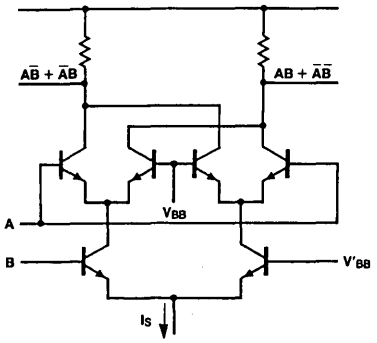

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FIGURE 1-6. Exclusive-OR/NOR

In *Figure 1-5*, if both A and B are HIGH, then Q1 and Q3 conduct and I_S flows through R1, making the collector of Q1 go LOW, thereby achieving the NAND of A and B. Connecting the collectors of Q2 and Q4 to the same load resistor provides the AND of A and B. If the collectors of Q3 and Q4 were interchanged, a different pair of functions of A and B would be produced. Similarly, a third functional pair is achieved by interchanging the collectors of Q1 and Q2. For Q3 and Q4 to operate at a lower voltage level than Q1 and Q2, the voltage level of B is translated downward from the normal ECL levels and V'_{BB} is similarly translated downward from the V_{BB} voltage. In the slightly more complex circuit in *Figure 1-6*, another pair of transistors is added to obtain the Exclusive-OR and Exclusive-NOR functions.

Connecting transistors in series is not limited to two levels of decision making; three levels are shown in the simplified schematic of an octal decoding tree *(Figure 1-7)*. If the three input signals are all HIGH, Q1 conducts through Q9 and Q13 to make the collector of Q1 LOW. In all, there are eight possible paths through which the source current can return to the positive supply. A LOW signal at the collector of any one of the transistors in the top row represents a unique combination of the three input signals. This 1-of-8 decoding circuit illustrates very clearly how ECL design techniques make the most efficient use of components and power to generate complex functions. This same set of switches, with the upper collectors wired in two sets of four collectors each, generates the binary sum and its complement of the three input signals.

The Current Source, Output Regulation

All elements of the F100K circuits use a transistor current source illustrated in *Figure 1-8*. Source current is determined by an internally generated reference voltage V_{CS}, the emitter resistor R_S and the base-emitter voltage of Q5. The reference voltage is designed to remain fixed with respect to the negative supply V_{EE}, which makes I_S independent of supply voltage.

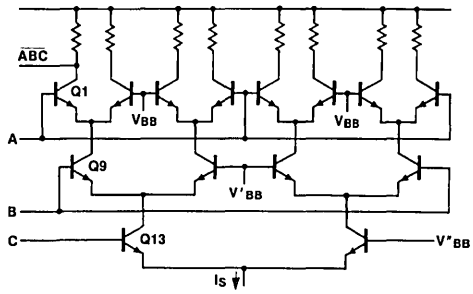

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FIGURE 1-7. Octal Decoding Tree

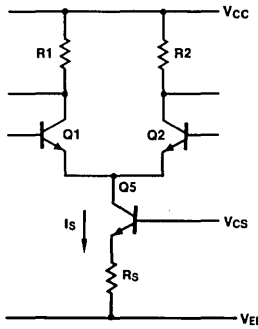

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FIGURE 1-8. Constant Current Source for a Switch

Regulating the current source (I_S) simplifies system design because output voltage and switching parameters are not sensitive to V_{EE} changes. Output voltage levels are determined primarily by the voltage drops across R1 and R2 resulting from the collector currents of Q1 and Q2. Since the collector current of the conducting transistor (Q1 or Q2) is determined by I_S and the transistor α, the voltage drop across the collector load resistor is not sensitive to V_{EE} variations. For example, a 1V change in V_{EE} changes the output level V_{OL} by only 10 mV.

Switching parameters are affected by transistor characteristics, the collector resistor (R1 or R2), stray capacitances, and the amount of current being switched. In other forms of ECL where source currents change with V_{EE}, switching parameters are directly affected. This sensitivity is essentially eliminated in F100K circuits by regulating I_S against V_{EE} changes.

Power dissipation in an ECL switch is the product of I_S and V_{EE}. By holding I_S constant with V_{EE}, incremental changes in dissipation are linear with V_{EE} changes. In non-regulated ECL, I_S increases with V_{EE} causing switch dissipation to change more rapidly with V_{EE}.

Threshold Regulation

As previously discussed, the input threshold region of an ECL switch is centered on the internal reference V_{BB}. In F100K circuits, the on-chip bias driver holds V_{BB} constant with respect to V_{CC}, thus minimizing changes in input thresholds with V_{EE}. For a V_{EE} change of 1V, for example, V_{BB} changes by approximately 25 mV.

With output voltage levels and input thresholds regulated, F100K circuits tolerate large differences in V_{EE} between a driving and a receiving circuit and still maintain good noise margins. For example, a driving circuit operated with −4.2V and receiving circuit operated with −5.7V experience no LOW state noise margin loss compared to a driver and receiver both with V_{EE} = −4.5V. This insensitivity to V_{EE} simplifies the design of system power distribution and regulation.

Temperature Compensation

In F100K circuits, input thresholds are made insensitive to temperature by regulating V_{BB}. Output voltage levels are made insensitive to temperature by a correction factor designed into the current source and by a simple network connected between the bases of the output transistors as shown in *Figure 1-9*.

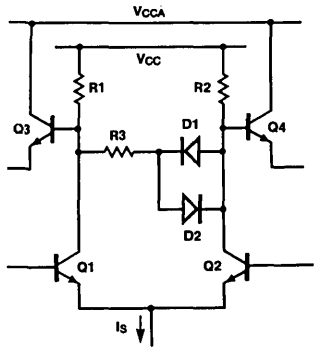

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FIGURE 1-9. Temperature Compensation

With Q1 conducting and Q2 off, most of the source current flows through R1, while a small amount flows through R2, D1 and R3. If the chip temperature increases, the source current is made to increase, causing an increase in the voltage drop of sufficient magnitude across R1 to offset the decrease in base-emitter voltage of Q3. The voltage drop across R1 increases with temperature at the rate of approximately 1.5 mV/°C, while the voltage drop across D1 decreases at the same rate. This means that there is a net voltage increase of 3 mV/°C across the series combination of R2 and R3. This increase is equally divided between the two resistors since R3 is equal to R2 (and R1); thus the voltage at the base of Q4 goes negative by 1.5 mV/°C, offsetting the decrease in the base-emitter voltage of Q4. When Q2 is on and Q1 is off, the same relationships apply except that most of the current flows through R2, and D2 conducts instead of D1. F100K 300 series change rates for V_{OH}, V_{BB}, and V_{OL} are approximately 0.06, 0.08 and 0.1 mV/°C, respectively.

The stabilization of output levels against changes in temperature provides significant advantages to both the user and manufacturer. In testing, an extended thermal stabilization period is not required, nor is an elaborate air cooling arrangement necessary to obtain correlation of test results between user and supplier. In a system, the output signal swing of a circuit does not depend on its temperature, therefore temperature differences do not cause a mismatch in signal levels between various locations. With temperature gradients thus eliminated as a system constraint, the design of the cooling system is greatly simplified.

Noise Margins

The most conservative values of ECL noise margins are based on the DC test conditions and limits listed on the data sheets. Acceptance limits on V_{OH} and V_{OL} are identified on a symbolic waveform in *Figure 1-10*, with the boundaries of the input threshold region also identified. The HIGH-state noise margin is usually defined as the difference between $V_{OH(Min)}$ and $V_{IH(Min)}$, with the LOW-state margin defined as the difference between $V_{OL(Max)}$ and $V_{IL(Max)}$. These two differences are identified as V_{NH} and V_{NL} respectively. The worst case input and output test points are also identified on the OR gate transfer function shown in *Figure 1-11*. The transition region indicated by the solid line is applicable when the internal reference V_{BB} has the design center value of −1.32V for F100K circuits. The transition regions indicated by the dashed lines represent the lot-to-lot displacement resulting from the normal production tolerances on V_{BB}, which amount to ±40 mV for F100K circuits. Using F100K circuit values as an example, the dashed curve on the right correlates with a V_{BB} value of −1.280V, and the input test voltage $V_{IH(Min)}$ is −1.165V, for a net difference of 115 mV. Similarly, the dashed curve on the left applies when V_{BB} is −1.360V with $V_{IL(Max)}$ specified as −1.475V, which also gives a net difference of 115 mV. The points V_{OHC} and V_{OLC} are commonly referred to as the *corner points* because of their location on the transfer function of worst case circuits.

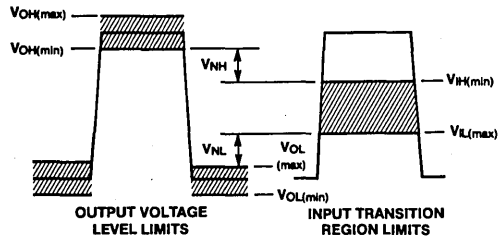

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FIGURE 1-10. Identifying Specification Limits on Input and Output Voltage Levels

In actual system operation, the noise margins V_{NH} and V_{NL} are quite conservative because of the way $V_{IH(Min)}$ and $V_{IL(Max)}$ are defined. From the transfer function of *Figure 1-11*, for example, $V_{IH(Min)}$ is defined as a value of input voltage which causes a worst-case output to decrease from $V_{OH(Min)}$ to V_{OHC} This change in V_{OH} amounts to only 10 mV for F100K circuits. Thus, if a worst case OR gate has a quiescent input of $V_{OH(Min)}$, a superimposed negative-going disturbance of amplitude V_{NH} causes an output change of only 10 mV, assuming that the time duration of the disturbance is sufficient for the OR gate to respond fully. In

Noise Margins (Continued)

contrast, a system fault does not occur unless the superimposed noise at the OR input is of sufficient amplitude to cause the output response to extend into the threshold region(s) of the load(s) driven by the OR gate. In general, noise becomes intolerable when it propagates through a string of gates and arrives at the input of a regenerative circuit (flip-flop, counter, shift register, etc.) with sufficient amplitude to reach the V_{BB} level.

The critical requirement for propagating either a signal or noise through a string of gates is that each output must exhibit an excursion to the V_{BB} level of the next gate in the string, assuming, of course, that the time duration is sufficient to allow full response. If the excursion at the input of a particular gate either falls short or exceeds V_{BB}, the effect on its output response is magnified by the voltage gain of the gate. On the voltage transfer function of a gate, the slope in the transition region is not, strictly speaking, constant. However, for input signal excursions of about ±50 mV on either side of V_{BB}, a value of 5.5 may be used for the voltage gain. For example, if the noise (or signal) excursion at the input of a gate falls short of V_{BB} by 20 mV, the gate output response is 110 mV less. Another useful relationship is that if the input voltage of a gate is equal to V_{BB}, the output voltage is also equal to V_{BB}, within perhaps 30 mV.

To determine the combined effects of circuit and system parameters on noise propagation through a string of gates, refer to *Figure 1-12*. The voltages V_1 and V_2 represent differences in ground potential, while V_3 and V_4 are V_{EE} differences. The output of gate A is in the quiescent LOW state and V_{PL} is a positive-going disturbance voltage. Now, how large can V_{PL} be without causing propagation through gate C? For a starting point, assume all three gates are identical with typical parameters; V_{EE} is −4.5V, the ground drops are zero, and there are no temperature gradients. Voltage parameters of F100K circuits are used. With typical circuits and the idealized environment, the maximum tolerable value of V_{PL} for propagation is the difference between the nominal V_{BB} of −1.320V and nominal V_{OL} of −1.705V, or 385 mV. The following steps treat each non-ideal factor separately and the required reduction in V_{PL} is calculated.

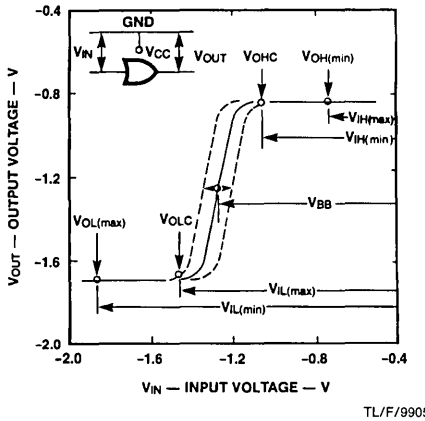

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FIGURE 1-11. Location of Test Points and Threshold on a Transfer Function

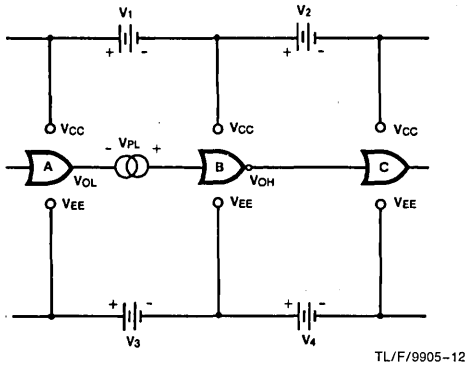

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FIGURE 1-12. Arrangement for Noise Propagation Analysis

Non-Typical V_{BB} of Gate B: Specifications provide for V_{BB} variations of ±40 mV. If the V_{BB} of gate B is 40 mV more negative than nominal, V_{PL} must be reduced by the same amount.

$\Delta V_{PL} = -40$ mV

$V_{PL} = 385 - 40 = 345$ mV

Non-Typical V_{OL} of Gate A: V_{OL} limits are −1.620V to −1.830V corresponding to the $\pm 3\sigma$ points on the distribution. Statistically, this means that 98% of the circuits have V_{OL} values of −1.650V or lower. Since this value differs from the nominal V_{OL} by 55 mV, V_{PL} must be reduced accordingly.

$\Delta V_{PL} = -55$ mV

$V_{PL} = 345 - 55 = 290$ mV

Difference in Ground (V_{CC}) Potential between Gates A and B: Since the V_{CC} lead of Gate B is the reference potential for input voltages, V_1 in the polarity shown effectively makes the V_{OL} of Gate A more positive. Minimizing ground drops is one of the system designer's tasks *(Chapter 5)* and its effect on noise margins emphasizes its importance. For this analysis, a value of 30 mV is assumed.

$\Delta V_{PL} = 30$ mV

$V_{PL} = 290 - 30 = 260$ mV

Difference in V_{EE} between Gates A and B: In the polarity shown, V_3 reduces the supply voltage for Gate A since it is assumed that Gate B has V_{EE} of −4.5V. The indicated polarities of V_1 and V_3 seem to be in conflict if it is assumed that V_3 represents only ohmic drops along the V_{EE} bus. Since V_3 may, however, be caused by the use of different power supplies or regulators as well as by ohmic drops, the polarities may exist as indicated. In any actual situation, the designer can usually predict the directions of supply current flow by observation of the physical arrangement. As mentioned earlier, a 1V change in V_{EE} causes a V_{OL} change 30 mV, or 3%. Assuming a value of 0.5V for V_3 and adding the 30 mV of V_1, the net reduction in supply voltage for Gate A is 0.53V. Using 3% of this reduction as the change in V_{OL} gives a positive V_{OL} shift of 16 mV, which is a reduction of noise margin.

$\Delta V_{PL} = -16$ mV

$V_{PL} = 260 - 16 = 244$ mV

If the net supply voltage of Gate A is assumed to be −4.5V, then V_1 and V_3 cause Gate B to have a greater supply voltage. This, in turn, causes the V_{BB} of Gate B to go more negative at the rate of 25 mV/V of V_{EE} change, or 2.5%.

Noise Margins (Continued)

Thus, for the same values of V_1 and V_3, the required reduction of V_{PL} is only 13 mV instead of the 16 mV computed above.

Non-Typical V_{BB} of Gate B: This was considered earlier for its effect at the input of Gate B. It must also be considered for its effect on the excursions of the output voltage of Gate B. Since the net input voltage of Gate B ($V_{OL} + V_{PL}$) reaches the V_{BB} level of Gate B, the output excursion also extends to the V_{BB} level and perhaps 30 mV beyond (more negative). This means that the output excursion of Gate B could be 90 mV more negative than the nominal V_{BB} of Gate C. This excess excursion must be divided by the voltage gain of Gate B to determine exactly how much V_{PL} must be reduced as compensation.

$\Delta V_{PL} = -90/5.5 = -16$ mV

$V_{PL} = 244 - 16 = 228$ mV

Non-Typical V_{BB} of Gate C: The V_{BB} of Gate C could be 40 mV more positive than the nominal value of −1.320V. Dividing by the voltage gain of Gate B gives the necessary reduction of V_{PL}.

$\Delta V_{PL} = -40/5.5 = -7$ mV

$V_{PL} = 228 - 7 = 221$ mV

Difference in V_{CC} Potential between Gates B and C: For the polarity shown, V_2 makes the net voltage at the C input more negative with respect to the V_{CC} lead of Gate C. Assume 30 mV for V_2 as was done for V_1.

$\Delta V_{PL} = -30/5.5 = -5.0$ mV

$V_{PL} = 217 - 5 = 212$ mV

Difference in V_{EE} between Gates B and C: In the polarity shown, V_4 reduces the supply voltage for Gate C, as does V_2. As previously mentioned, V_{BB} changes with V_{EE} at a rate of 25 mV/V, or 2.5%. Assuming a value of 0.5V for V_4, as was done for V_2, adding V_2 gives a net V_{EE} reduction of 0.53V. This makes the V_{BB} of Gate C about 13 mV more positive, with respect to its own V_{CC} lead. This must be divided by the gain of Gate B to determine the effect on the permissible value of V_{PL}.

$\Delta V_{PL} = -13/5.5 \cong -2$ mV

$V_{PL} = 212 - 2 = 210$ mV

At this point the more conservatively defined V_{NL} *(Figure 1-10)* should be evaluated and compared with V_{PL}. Subtracting the values of $V_{OL(Max)}$ and $V_{IL(Max)}$, a value of 145 mV for V_{NL} is obtained.

The primary advantage of using V_{NH} and V_{NL} as the limits of tolerable noise is that they provide for simultaneous appearance of noise on inputs and outputs. Whatever the system designer's preference regarding noise margin definitions, the important factor is to recognize that the ΔV_{CC} and ΔV_{EE} between devices decrease the noise margins and therefore should be minimized.

References

1. Marley, R.R., "On-Chip Temperature Compensation for ECL", *Electronic Products*, (March 1, 1971).
2. Marley, R.R., "Design Considerations of Temperature Compensated ECL," *IEEE International Convention*, (March, 1971).
3. Widlar, R.J., "Local IC Regulator for Logic Circuits," *Computer Design*, (May, 1971).
4. Widlar, R.J., "New Developments in IC Voltage Regulators," *ISSCC Digest of Technical Papers*, (February, 1970).
5. Muller, H.H., Owens, W.K., Verhofstadt, P.W.J., "Fully Compensated ECL," *ISSCC Digest of Technical Papers*, (February, 1973).

National Semiconductor

Chapter 2
Logic Design

Introduction

The F100K family is comprised of SSI, MSI, LSI, logic functions, gate arrays, BiCMOS SRAMs, and PALs. The latest addition to the F100K family is the 300 Series. 300 Series devices are functionally equivalent redesigns of existing F100K devices, but with added enhancements such as: lower power, PCC packaging, extended operating voltage range, military versions and ESD protection of 2000V (minimum).

This chapter covers basic gates and flip-flops, as well as applications using MSI functions. In most cases a 300 Series redesign is available in place of the referenced 100 Series part. Refer to the Applications section of this databook for the latest publications using ECL logic. Gate Arrays, PALs, and MSI are covered in separate publications. All BiCMOS SRAM applications are included in the Memory Databook.

National F100K ECL logic symbols use the positive logic or "active-HIGH" option of MIL-STD-806B. Logic '1' or "active-High" is the more positive voltage, nearest ground (typically −0.955V). Logic '0' or "active-LOW" is the more negative level, nearest V_{EE} (typically −1.705V).

OR/NOR Gates

The most basic F100K ECL circuit is the OR/NOR gate *(Figure 2-1)*. If the input (A or B) voltages are more negative than the reference voltage V_{BB}, Q1 and Q2 are cut off (nonconducting) and Q3 conducts, holding the collector of Q3 LOW. Since the base of Q4 is LOW, the pull-down resistor or terminator connected to its emitter makes the OR output LOW. The base of Q5 is HIGH (near ground) and its emitter pulls the NOR output HIGH. If either input is more positive than V_{BB}, Q1 or Q2 conducts and Q3 is cut off. This makes the base of Q4 HIGH, resulting in a HIGH at the OR output. At the same time, the base of Q5 is LOW and the pull-down resistors or terminator pulls the NOR output LOW. Detailed information concerning F100K ECL circuit basics may be found in Chapter 1.

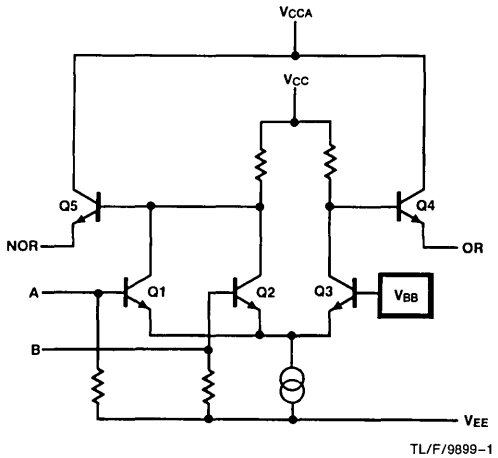

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FIGURE 2-1. Basic ECL Gate

The F100K family includes two OR/NOR-gate devices. The 100301 is a triple 5-input OR/NOR and the 100302 is a quint 2-input OR/NOR with common enable. One element of the 100302 is shown in *Figure 2-2*; the corresponding truth table is Table 2-1.

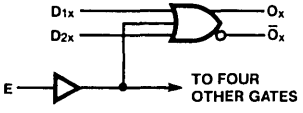

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FIGURE 2-2. 100302 OR/NOR Gate

TABLE 2-1. 100302 Truth Table

D_{1x}	D_{2x}	E	O_x	$\overline{O}_x$
L	L	L	L	H
L	L	H	H	L
L	H	L	H	L
L	H	H	H	L
H	L	L	H	L
H	L	H	H	L
H	H	L	H	L
H	H	H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level

Wired-OR Function

A wired-OR function can be implemented simply by connecting the appropriate outputs external to the package (see *Figure 2-3*). Each output is buffered so that the internal logic is not affected by the wire-OR. This is a positive logic OR, not to be confused with a DTL wired-AND or the internal series gating used for some ECL functions. This wired-OR is especially useful in implementing data busses. For further information see Chapter 4.

Wired-OR Function (Continued)

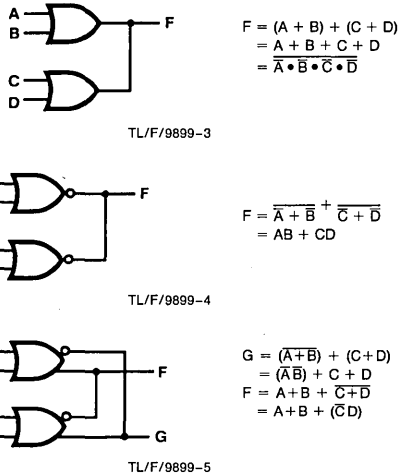

FIGURE 2-3. Wired-OR Function

AND Function

The positive logic AND function is directly available in F100K ECL (100304). There are two other approaches which can be taken to solve the problem of implementing an AND.

The first solution is indicated in *Figure 2-4*. A positive logic OR gate can be redrawn as a negative logic AND gate. To take advantage of this requires active-LOW input terms; but, since practically every F100K circuit provides complementary outputs, this should not be a problem.

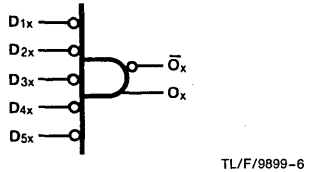

FIGURE 2-4. 100301 Redrawn as AND/NAND Gate

Exclusive-OR/Exclusive-NOR Gate

The 100307 is a quint exclusive OR/NOR gate. In addition to providing the exclusive-OR/exclusive-NOR of the five input pairs, a comparison output is available. If the five pairs of inputs are identical, bit by bit, then the common output will be LOW.

Flip-Flops and Latches

Flip-flops and latches are treated together due to their similarity. The only difference is that latch outputs follow the inputs whenever the enable is LOW, whereas a flip-flop changes output states only on the LOW-to-HIGH clock transition.

The advantage of an edge-triggered flip-flop is that the outputs are stable except while the clock is rising; a latch has better data-to-output propagation delay while the enable is kept active.

Both latches and flip-flops are available three to a package with individual as well as common controls and six to a package with only common controls. There are a total of three parts as indicated below.

	Triple w/Individual Controls	Hex w/Common Controls
Flip-Flops	100331	100351
Latches		100350

Figure 2-5 shows the equivalent logic diagram of ⅓ of an 100331. The internal clock is the OR of two clock inputs, one common to the other two flip-flops. The OR clock input permits common or individual control of the three flip-flops. In addition, one input may be used as a clock input and the other as an active-LOW enable.

When the clock is LOW, the slave is held steady and the information on the D input is permitted to enter the master. The transition from LOW to HIGH locks the master in its present state making it insensitive to the D input. This transition simultaneously connects the slave to the master, causing the new information to appear at the outputs. Master and slave clock thresholds are internally offset in opposite directions to avoid race conditions or simultaneous master/slave changes when the clock has slow rise or fall times.

The Clear and Set Direct for each flip-flop are the OR of two inputs, one common to the other two flip-flops. The output levels of a flip-flop are unpredictable if both the Set and Clear Direct inputs are active.

The outputs of all F100K flip-flops and latches are buffered. This means that they can be OR-wired; noise appearing on the outputs cannot affect the state of the internal latches.

Table 2-2 is the truth table for the 100331 flip-flop.

TABLE 2-2. 100331 Truth Table

D_n	CP_n	CP_c	MS SD_n	MR CD_n	$Q_{n(t+1)}$
L	↗	L	L	L	L
H	↗	L	L	L	H
L	L	↗	L	L	L
H	L	↗	L	L	H
X	H	X	L	L	$Q_n(t)$
X	X	H	L	L	$Q_n(t)$
X	X	X	H	L	H
X	X	X	L	H	L
X	X	X	H	H	U

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
U = Undefined
t, t + 1 = Time before and after CP positive transition

If eight flip-flops are desired, such as for pipeline register applications, the 100341 Shift Register can be used. Neither reset nor complementary outputs are available. The Select inputs may be used to mechanize a clock enable as shown in *Figure 2-6*.

Flip-Flops and Latches (Continued)

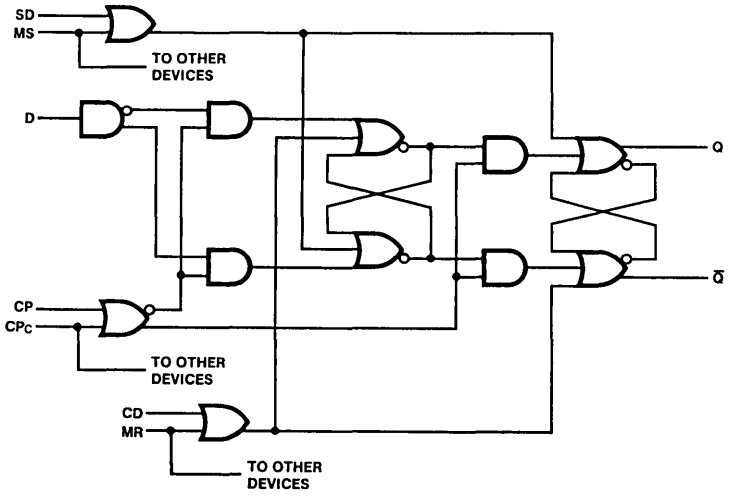

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FIGURE 2-5. 100331 D Flip-Flop

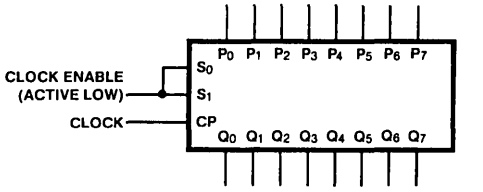

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FIGURE 2-6. 100341 as Octal D Flip-Flop

Counters

The 100336 operates either as a modulo-16 up/down counter or as a 4-bit bidirectional shift register. It has three Select inputs which determine the mode of operation as shown in Table 2-3. In addition, a Terminal Count output, and two Count Enables are provided for easy expansion to longer counters. A detailed truth table for the 100336 is included in the specification sheet. To achieve the highest possible speed, complementary outputs should be equally terminated, i.e., if Q_2 is used, $\overline{Q}_2$ should be equally terminated even if not used. If neither output of a particular stage is used, then both outputs can be left open.

TABLE 2-3. 100336 Function Select Table

S_2	S_1	S_0	Function
L	L	L	Parallel Load
L	L	H	Complement
L	H	L	Shift to LSB
L	H	H	Shift to MSB
H	L	L	Count Down
H	L	H	Clear
H	H	L	Count Up
H	H	H	Hold

H = HIGH Voltage Level
L = LOW Voltage Level

VARIABLE MODULUS COUNTERS

A 100336 can act as a programmable divider by presetting it via the parallel inputs, counting down to minimum and then presetting it again to start the next cycle. *Figure 2-7* shows a one-stage counter capable of dividing by 2 to 15. S_0 and S_1 are unconnected (therefore LOW) and the counter thus is in either the Count Down or Parallel Load mode, depending on whether S_2 is HIGH or LOW, respectively. $\overline{CEP}$ and $\overline{CET}$ are also LOW, enabling counting when S_2 is HIGH. Immediately after the counter is preset to N, which must be greater than one, the $\overline{LOAD}$ signal goes HIGH and the 100336 starts counting down on the next clock. When it counts down to one, the $\overline{LOAD}$ signal goes LOW and presetting will occur on the next clock rising edge. Generating the $\overline{LOAD}$ signal on the count of one, rather than zero, makes up for the clock pulse used in presetting.

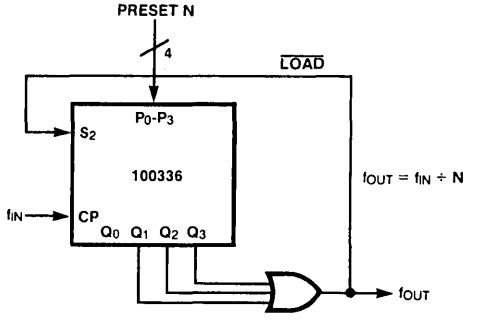

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FIGURE 2-7. 1-Stage Counter

Counters (Continued)

A 3-stage programmable divider is shown in *Figure 2-8*. The $\overline{TC}$ output of the first stage enables counting in the upper stages, while the $\overline{TC}$ output of the second stage also enables counting in the third stage. The D-input signal to the flip-flop is normally HIGH and thus $\overline{Q}$ is normally LOW. When both the second and third stage counters have counted down to zero, the $\overline{TC}$ output of the third stage goes LOW. When the first stage subsequently counts down to one, the D signal goes LOW, as does $\overline{LOAD}$. Presetting thus occurs on the next clock and $\overline{Q}$ goes HIGH to end the $\overline{LOAD}$ signal and permit counting to resume on the next clock.

In *Figure 2-7*, the maximum clock frequency is determined by the sum of the propagation delays from CP to Q and the OR gate, plus the setup time from S to CP. The maximum frequency is approximately 220 MHz for typical units or 170 MHz for worst-case units. In *Figure 2-8* the critical path is CP to Q of the first stage plus both OR gates, plus the S to CP set-up time of the counters. Typical and worst-case maximum frequencies are 190 MHz and 140 MHz respectively.

INTERCONNECTING COUNTERS

The terminal count and count enable connections provide an easy method of interconnecting the 100336 counter to achieve longer counts. *Figure 2-9* shows a method that uses few connections but has a drawback. The counters are fully synchronous, since the clock arrives at all devices at the same time; the only drawback is that the count enables have to "trickle" down the chain. This results in a lower maximum counting rate since it drastically increases the set-up time from enable to clock.

Figure 2-10 shows a method for partially overcoming these drawbacks. The enable to clock set-up is now one $\overline{CET}$ to

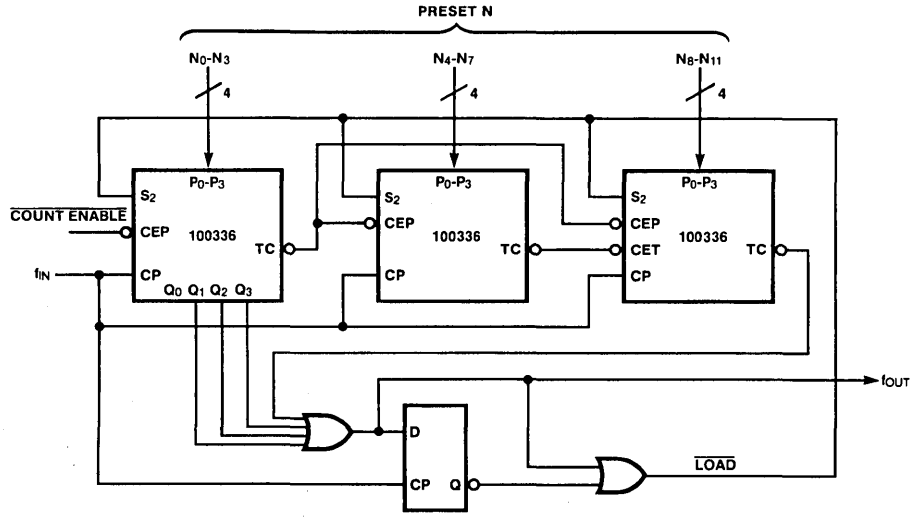

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FIGURE 2-8. 3-Stage Programmable Divider

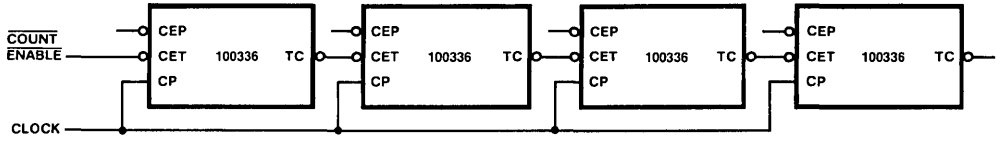

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FIGURE 2-9. Slow Expansion Scheme

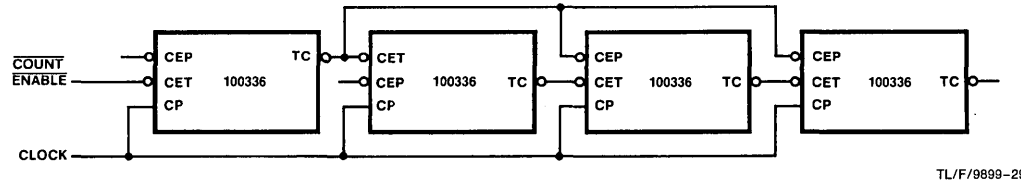

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FIGURE 2-10. Fast Expansion Scheme

Counters (Continued)

$\overline{TC}$ propagation delay plus one $\overline{CEP}$ to CP set-up. The count speed is thus increased. This is best seen by assuming that all stages except the second are at terminal count. At the next clock pulse, the second counter reaches terminal count and the first stage exits terminal count. The command to suppress counting in the third and fourth (and subsequent) stages arrives very quickly (via $\overline{CEP}$). The terminal count from the second stage propagates via $\overline{TC}$ and $\overline{CEP}$ to the high order stages, but has a full 15 counts to do so.

DECODING OUTPUTS

Since the complementary outputs from each stage are available, it is an easy matter to decode any value. (Clearly, if many values needed to be decoded one would choose a decoder chip.) *Figure 2-11* shows a 100336 and ⅓ 100301 interconnected to decode 1001 (NINE). Both complementary outputs of NINE are available and there is a spare input on the decoding gate.

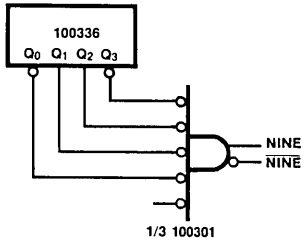

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FIGURE 2-11. Decoding States of 100336

Shift Registers

The 100341 is an 8-bit universal shift register. It can be used for parallel-to-serial or serial-to-parallel conversion and it will shift left or right. The truth table is shown in Table 2-4.

TABLE 2-4. 100341 Truth Table

S_1	S_0	CP	Mode
L	L	⎍	Parallel Load
L	H	⎍	Shift to MSB ($Q_0 \rightarrow Q_7$)
H	L	⎍	Shift to LSB ($Q_7 \rightarrow Q_0$)
H	H	X	Hold

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

Figure 2-12 shows the 100341 used as a 7-bit serial-to-parallel converter. When Initialize (INIT) becomes active, the next clock pulse presets the register to '10000000', and Register-Full (REG-FULL) becomes inactive. Each time a data bit becomes available, Data-Available (DATA-AVAIL) must be made active during one clock LOW-to-HIGH transition. This clocks the bit into the register moves the flag bit closer to Q_0. When the seventh data bit is entered, the flag bit reaches Q_0 and REG-FULL becomes active. The seven data bits may be removed at this time (Q_1 to Q_7) and the conversion is complete.

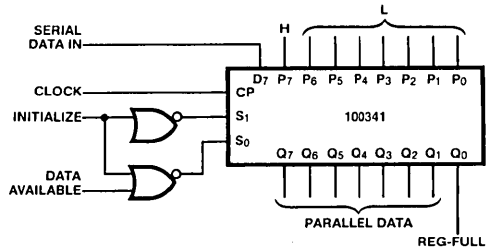

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FIGURE 2-12. Serial-to-Parallel Conversion

Table 2-5 summarizes the control inputs and corresponding 100341 modes for this circuit.

TABLE 2-5. Select Inputs Truth Table

INIT	DATA-AVAIL	S_1	S_0	Mode
L	L	H	H	Hold
L	H	H	L	Shift to LSB
H	L	L	L	Preset
H	H	L	L	(Illegal)

H = HIGH Voltage Level
L = LOW Voltage Level

Figure 2-14 shows a parallel-to-serial converter using the 100336 counter. *Figure 2-13* shows the associated timing diagram. Each time the external device has taken a bit of data, it makes the signal Serial-Data-Accept (SERIAL-DATA-ACPT) HIGH. The shift register shifts right which makes the next bit available and the counter counts up. The Serial-Data-Accept term must be synchronized with the clock. The counter counts to eight after the eighth data bit has been accepted and Parallel-Data-Request (PARALLEL-DATA-RQST) becomes active HIGH. When the device supplying data makes the next byte available, Parallel-Data-Ready (PARALLEL-DATA-RDY) goes HIGH. On the next clock pulse the shift register loads the new data byte and the counter clears to zero. Table 2-6 shows the operating mode as a function of the control inputs.

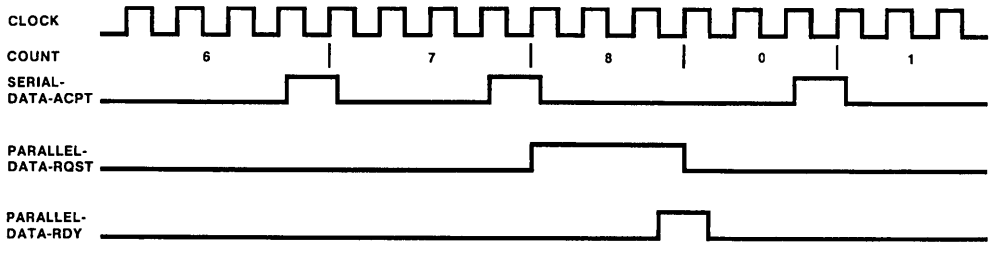

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FIGURE 2-13. Timing Diagram Parallel-to-Serial Converter

Shift Registers (Continued)

TABLE 2-6. Parallel-to-Serial Converter Truth Table

PARALLEL-DATA-RDY	SERIAL-DATA-ACPT	Shift Register			Counter			
		S_1	S_0	Mode	S_0	S_1	S_2	Mode
L	L	H	H	Hold	H	H	H	Hold
L	H	H	L	Shift to LSB	L	H	H	Count Up
H	L	L	L	Load	H	L	H	Clear

H = HIGH Voltage Level
L = LOW Voltage Level

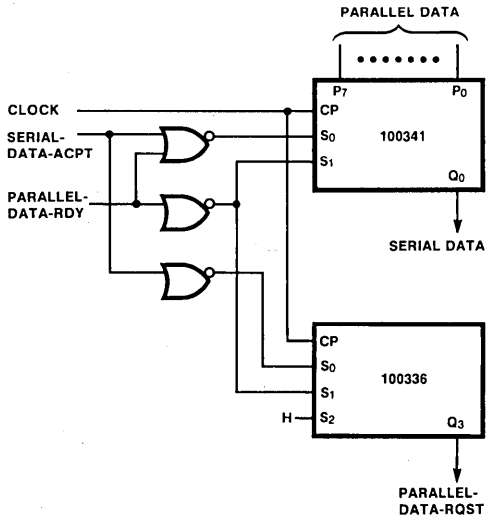

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FIGURE 2-14. Parallel-to-Serial Converter

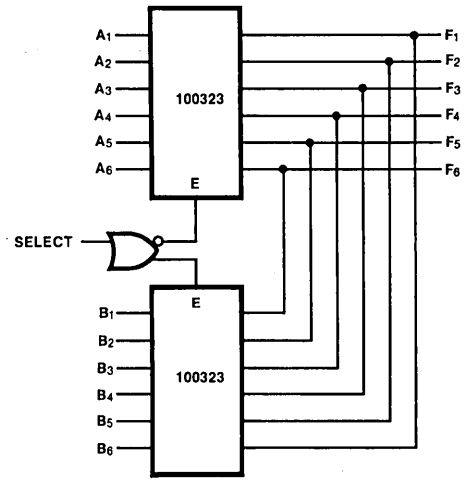

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FIGURE 2-15. Wired-OR Multiplexer

Multiplexers

Multiplexers send one of several inputs to a single output. The function can be implemented with standard gates or bus drivers and the wired-OR connection. *Figure 2-15* shows the 100323 Hex Bus Driver used as a wired-OR multiplexer. The 100323 devices could be in physically different parts of the system, since they can drive double-terminated busses.

The 100355 is a quad 2-input multiplexer with transparent latches. The device has two select terms and can accept data from either, neither, or both (OR) sources.

The 100363 is a dual 8-input multiplexer with common selects. The 100364 is a single 16-input multiplexer.

The 100363 and 100364 do not feature complementary outputs or an enable for wired-ORing. The 100371 is a triple 4-input multiplexer with enable and complementary outputs.

Figure 2-16 shows an 100364 multiplexer and 100336 connected to convert 16-bit parallel data to single-bit serial data. A gate is added to provide complementary serial data. If the input data is stable, then the output data is stable from 6.4 ns after a clock until 2.5 ns after the next clock. This would insure valid data 50% of the time at a clock rate of 100 MHz. Terminal Count on the counter can be used as a term to indicate the last bit is being transmitted. This can be used as a clock enable to the register containing the parallel data. The propagation delay through the register is masked by the propagation delay through the counter.

Multiplexers (Continued)

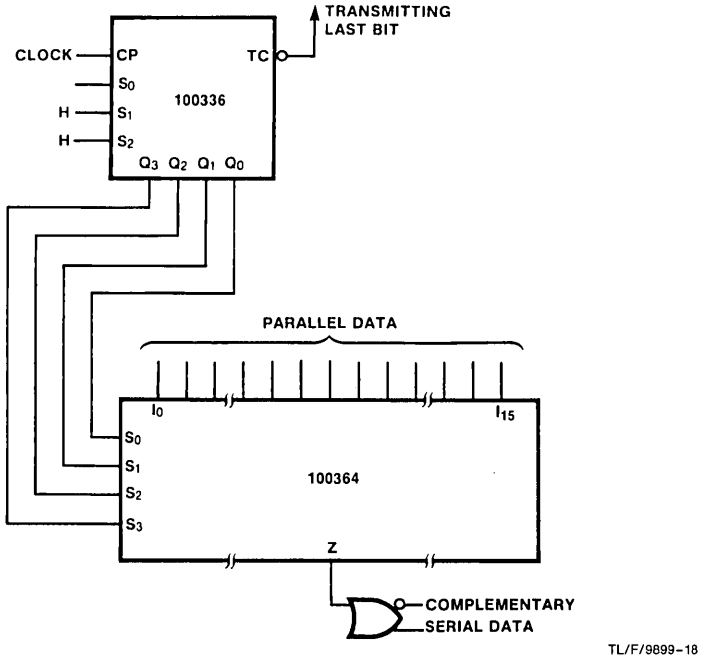

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FIGURE 2-16. Parallel-to-Serial Data Transmission

Decoder

The 100370 is a universal demultiplexer/decoder. It can function as either a dual 1-of-4 decoder or as a single 1-of-8 decoder. The outputs can be either active HIGH or active LOW.

If the M input is LOW, then the 100370 is configured as a dual 1-of-4 decoder. Both A_{2a} and H_c must be LOW. Table 2-7 is a truth table for each half of the 100370; the two halves are completely independent. The truth table is shown for active-HIGH outputs; for active-LOW outputs, H_x is made LOW.

TABLE 2-7 Dual 1-of-4 Mode Truth Table

Inputs				Active-HIGH Outputs (H_a and H_b Inputs HIGH)			
$\overline{E}_{1a}$ $\overline{E}_{1b}$	$\overline{E}_{2a}$ $\overline{E}_{2b}$	A_{1a} A_{1b}	A_{0a} A_{0b}	Z_{0a} Z_{0b}	Z_{1a} Z_{1b}	Z_{2a} Z_{2b}	Z_{3a} Z_{3b}
H	X	X	X	L	L	L	L
X	H	X	X	L	L	L	L
L	L	L	L	H	L	L	L
L	L	L	H	L	H	L	L
L	L	H	L	L	L	H	L
L	L	H	H	L	L	L	H

M = A_{2a} = H_c = LOW
H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

TABLE 2-8. Single 1-of-8 Mode Truth Table

Inputs					Active-HIGH Outputs (H_c Input HIGH)							
$\overline{E}_1$	$\overline{E}_2$	A_{2a}	A_{1a}	A_{0a}	Z_0	Z_1	Z_2	Z_3	Z_4	Z_5	Z_6	Z_7
H	X	X	X	X	L	L	L	L	L	L	L	L
X	H	X	X	X	L	L	L	L	L	L	L	L
L	L	L	L	L	H	L	L	L	L	L	L	L
L	L	L	L	H	L	H	L	L	L	L	L	L
L	L	L	H	L	L	L	H	L	L	L	L	L
L	L	L	H	H	L	L	L	H	L	L	L	L
L	L	H	L	L	L	L	L	L	H	L	L	L
L	L	H	L	H	L	L	L	L	L	H	L	L
L	L	H	H	L	L	L	L	L	L	L	H	L
L	L	H	H	H	L	L	L	L	L	L	L	H

M = HIGH;
A_{0b} = A_{1b} = H_a = H_b = LOW
E_1 = E_{1a} and E_{1b} Wired; E_2 = E_{2a} and E_{2b} Wired
H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

If the M input is HIGH, then the 100370 is configured as a single 1-of-8 decoder. A_{0b}, A_{1b}, H_a, and H_b must all be LOW. Table 2-8 is a truth table for the 100370 in single 1-of-8 mode. The truth table is shown for active-HIGH outputs; for active-LOW outputs, H_C is mode LOW.

5

Decoder (Continued)

Figure 2-17 and Table 2-9 show a universal decimal decoder and the decode table, respectively. The sense of the outputs can be easily modified. The entire decoder may be enabled with a LOW at the Function input.

Figure 2-18 shows a scheme to decode five lines with a 1-of-32 decoder. Inputs A_0, A_1, and A_2 are connected to the address select inputs of all four decoders in parallel. Both the true and complement of the two high order addresses are formed and then ANDed together at the decoder enable inputs.

Figure 2-19 shows a 1-of-64 decoder which uses the LOW outputs of one 100370 to enable one-of-eight 100370 devices whose address inputs are connected together. The unused enable inputs may be used to enable all 64 outputs. The 64 outputs may be either active HIGH or LOW. The propagation delay from address to any output is 4.5 ns maximum.

TABLE 2-9. Output Selection

A_0–A_3 Weighted Input	Selected Output per Input Code				
	8421	5421	Excess 3	Excess 3 Gray	2421
0	0	0	3	2	0
1	1	1	4	6	1
2	2	2	5	7	2
3	3	3	6	5	3
4	4	4	7	4	4
5	5	8	8	12	11
6	6	9	9	13	12
7	7	10	10	15	13
8	8	11	11	14	14
9	9	12	12	10	15

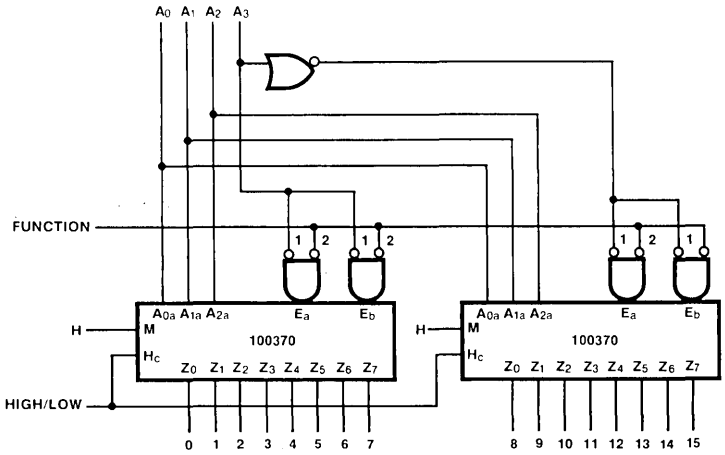

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FIGURE 2-17. Universal Decimal Decoder

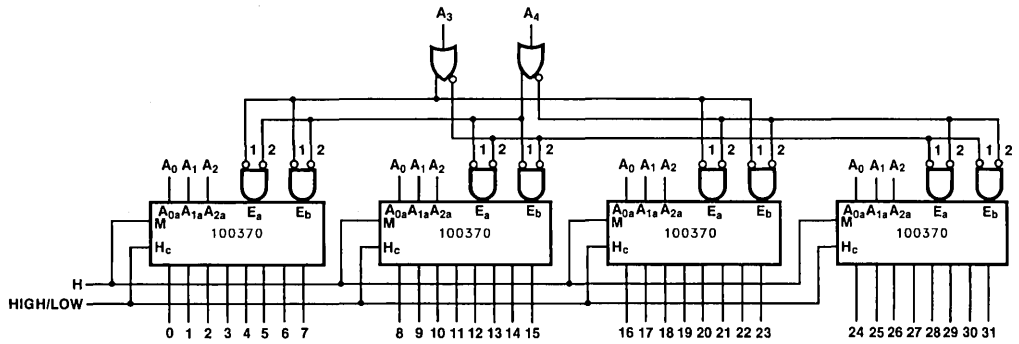

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FIGURE 2-18. 1-of-32 Decoder

Decoder (Continued)

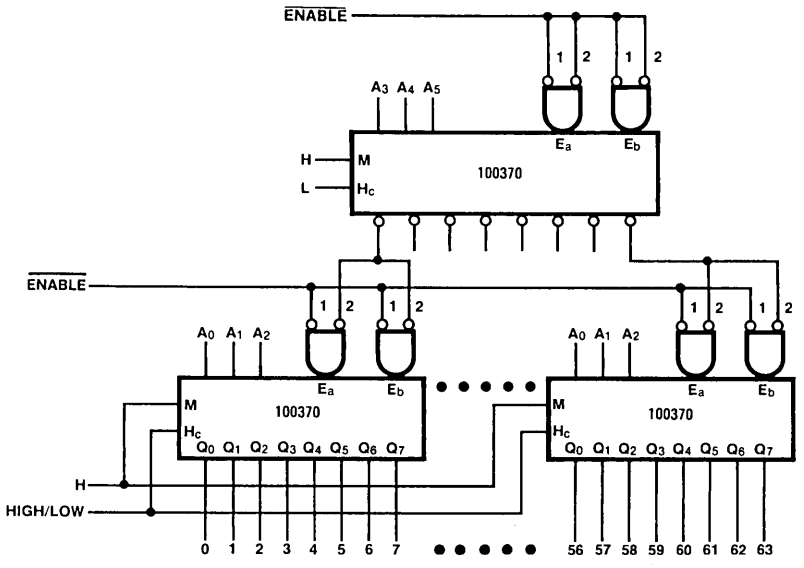

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FIGURE 2-19. 1-of-64 Decoder

Parity Generator/Checker

The 100360 is a dual 9-bit parity checker/generator. The output (of each section) is HIGH when an even number of inputs are HIGH. Thus, to generate odd parity on eight bits, the ninth input would be held HIGH. One of the nine inputs on each half has a shorter propagation (I_a, I_b) delay and is thus preferred for expansion.

Figure 2-20 shows how to build a 16-bit parity checker using a single 100360. The typical propagation delay from the longest input is 4.05 ns. This circuit can be turned into a parity generator by replacing "P" at input I_b with a LOW or HIGH for even or odd parity, respectively.

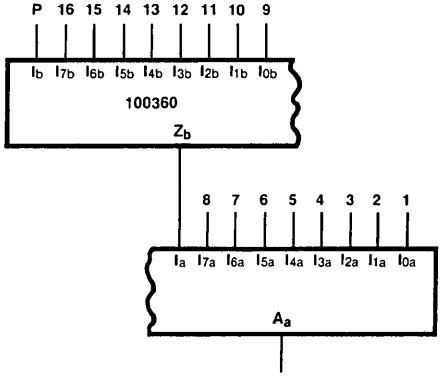

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FIGURE 2-20. 16-Bit Parity Checker/Generator

TTL/F100K Interfacing—Translators

The problem of mixing F100K ECL logic levels with TTL logic levels can be easily overcome with the use of level translators. Level translators are designed to convert the input level of one logic family to a level which is consistent with that of another logic family. This enables designers to take advantage of the high speeds offered by F100K ECL in critical system paths and to use other logic families in areas where speed is not as essential. National's wide range of level translators offer designers a solution for most level translation applications.

For more information on translators, see Application Note 784 "F100K ECL Dual Rail Translators" and Application Note 780 "Operating ECL from a Single Positive Supply".

10K/F100K Interfacing

The problem caused by mixing 10K ECL and F100K ECL is illustrated in *Figures 2-21* and *2-22*. 10K output levels and input thresholds vary with temperature whereas F100K levels and thresholds remain essentially constant. This means that the noise margins vary with temperature, even if the temperatures of the driving and receiving circuits track. Perhaps the worst case is shown in *Figure 2-22*, which illustrates F100K driving 10K.

At +75°C, the high margins are seen to be less than 100 mV. Clearly this would not represent acceptable DC margins in any real system.

If the use of 10K ECL in an F100K system is unavoidable, it is recommended that all interfacing be done differentially. This is illustrated in *Figure 2-23* which is applicable for either direction.

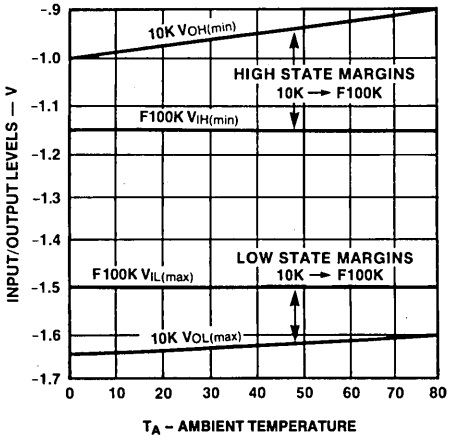

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FIGURE 2-21. 10K ECL Driving 100K ECL

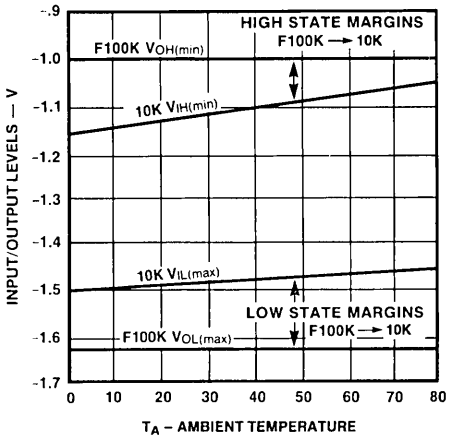

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FIGURE 2-22. 100K ECL Driving 10K ECL

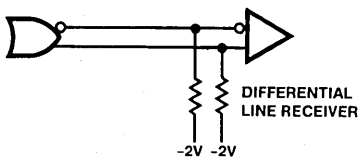

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FIGURE 2-23. Interfacing 10K and F100K

National Semiconductor

Chapter 3
Transmission Line Concepts

Introduction

The interactions between wiring and circuitry in high-speed systems are more easily determined by treating the interconnections as transmission lines. A brief review of basic concepts is presented and simplified methods of analysis are used to examine situations commonly encountered in digital systems. Since the principles and methods apply to any type of logic circuit, normalized pulse amplitudes are used in sample waveforms and calculations.

Simplifying Assumptions

For the great majority of interconnections in digital systems, the resistance of the conductors is much less than the input and output resistance of the circuits. Similarly, the insulating materials have very good dielectric properties. These circumstances allow such factors as attenuation, phase distortion, and bandwidth limitations to be ignored. With these simplifications, interconnections can be dealt with in terms of characteristic impedance and propagation delay.

Characteristic Impedance

The two conductors that interconnect a pair of circuits have distributed series inductance and distributed capacitance between them, and thus constitute a transmission line. For any length in which these distributed parameters are constant, the pair of conductors have a characteristic impedance Z_0. Whereas quiescent conditions on the line are determined by the circuits and terminations, Z_0 is the ratio of transient voltage to transient current passing by a point on the line when a signal charge or other electrical disturbance occurs. The relationship between transient voltage, transient current, characteristic impedance, and the distributed parameters is expressed as follows:

$$\frac{V}{I} = Z_0 = \sqrt{\frac{L_0}{C_0}} \qquad (3\text{-}1)$$

where L_0 = inductance per unit length, C_0 = capacitance per unit length. Z_0 is in ohms, L_0 in Henries, C_0 in Farads.

Propagation Velocity

Propagation velocity ν and its reciprocal, delay per unit length δ, can also be expressed in terms of L_0 and C_0. A consistent set of units is nanoseconds, microhenries and picofarads, with a common unit of length.

$$\nu = \frac{1}{\sqrt{L_0 C_0}} \qquad \delta = \sqrt{L_0 C_0} \qquad (3\text{-}2)$$

Equations 3-1 and *3-2* provide a convenient means of determining the L_0 and C_0, of a line when delay, length and impedance are known. For a length l and delay T, δ is the ratio T/l. To determine L_0 and C_0, combine *Equations 3-1* and *3-2*.

$$L_0 = \delta Z_0 \qquad (3\text{-}3)$$

$$C_0 = \frac{\delta}{Z_0} \qquad (3\text{-}4)$$

More formal treatments of transmission line characteristics, including loss effects, are available from many sources.[1-3]

Termination and Reflection

A transmission line with a terminating resistor is shown in *Figure 3-1*. As indicated, a positive step function voltage travels from left to right. To keep track of reflection polarities, it is convenient to consider the lower conductor as the voltage reference and to think in terms of current flow in the top conductor only. The generator is assumed to have zero internal impedance. The initial current I_1 is determined by V_1 and Z_0.

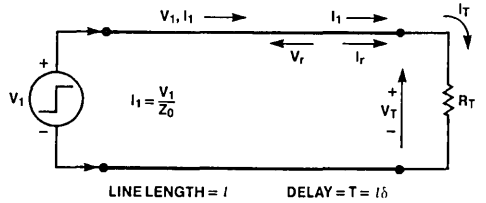

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FIGURE 3-1. Assigned Polarities and Directions for Determining Reflections

If the terminating resistor matches the line impedance, the ratio of voltage to current traveling along the line is matched by the ratio of voltage to current which must, by Ohm's law, always prevail at R_T. From the viewpoint of the voltage step generator, no adjustment of output current is ever required; the situation is as though the transmission line never existed and R_T had been connected directly across the terminals of the generator. From the R_T viewpoint, the only thing the line did was delay the arrival of the voltage step by the amount of time T.

When R_T is not equal to Z_0, the initial current starting down the line is still determined by V_1 and Z_0 but the final steady state current, after all reflections have died out, is determined by V_1 and R_T (ohmic resistance of the line is assumed to be negligible). The ratio of voltage to current in the initial wave is not equal to the ratio of voltage to current demanded by R_T. Therefore, at the instant the initial wave arrives at R_T, another voltage and current wave must be generated so that Ohm's law is satisfied at the line-load interface. This *reflected* wave, indicated by V_r and I_r in *Figure 3-1*, starts to return toward the generator. Applying

Termination and Reflection (Continued)

Kirchoff's laws to the end of the line at the instant the initial wave arrives, results in the following.

$$I_1 + I_r = I_T = \text{current into } R_T \qquad (3\text{-}5)$$

Since only one voltage can exist at the end of the line at this instant of time, the following is true:

$$V_1 + V_r = V_T$$

$$\text{thus} \quad I_T = \frac{V_T}{R_T} = \frac{V_1 + V_r}{R_T} \qquad (3\text{-}6)$$

$$\text{also} \quad I_1 = \frac{V_1}{Z_0} \text{ and } I_r = -\frac{V_r}{Z_0}$$

with the minus sign indicating that V_r is moving toward the generator.

Combining the foregoing relationships algebraically and solving for V_r yields a simplified expression in terms of V_1, Z_0 and R_T.

$$\frac{V_1}{Z_0} - \frac{V_r}{Z_0} = \frac{V_1 + V_r}{R_T} = \frac{V_1}{R_T} + \frac{V_r}{R_T}$$

$$V_1\left(\frac{1}{Z_0} - \frac{1}{R_T}\right) = V_r\left(\frac{1}{R_T} + \frac{1}{Z_0}\right) \qquad (3\text{-}7)$$

$$V_r = V_1\left(\frac{R_T - Z_0}{R_T + Z_0}\right) = \rho_L V_1$$

The term in parenthesis is called the coefficient of reflection ρ. With R_T ranging between zero (shorted line) and infinity (open line), the coefficient ranges between -1 and $+1$ respectively. The subscript L indicates that ρ refers to the coefficient at the load end of the line.

Equation 3-7 expresses the amount of voltage sent back down the line, and since

$$V_T = V_1 + V_r \qquad (3\text{-}8)$$

then $V_T = V_1(1 + \rho_L)$.

V_T can also be determined from an expression which does not require the preliminary step of calculating ρ_L. Manipulating $(1 + \rho_L)$ results in

$$1 + \rho_L = 1 + \frac{R_T - Z_0}{R_T + Z_0} = 2\left(\frac{R_T}{R_T + Z_0}\right)$$

Substituting in *Equation 3-8* gives

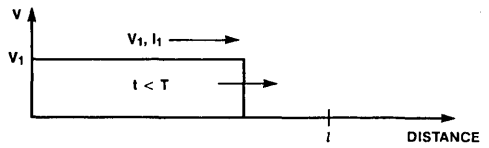
$$V_T = 2\left(\frac{R_T}{R_T + Z_0}\right)V_1 \qquad (3\text{-}9)$$

The foregoing has the same form as a simple voltage divider involving a generator V_1 with internal impedance Z_0 driving a load R_T, except that the amplitude of V_T is doubled.

The arrow indicating the direction of V_r in *Figure 3-1* correctly indicates the V_r direction of travel, but the direction of I_r flow depends on the V_r polarity. If V_r is positive, I_r flows toward the generator, opposing I_1. This relationship between the polarity of V_r and the direction of I_r can be deduced by noting in *Equation 3-7* that if V_r is positive it is because R_T is greater than Z_0. In turn, this means that the initial current I_r is larger than the final quiescent current, dictated by V_1 and R_T. Hence, I_r must oppose I_1 to reduce the line current to the final quiescent value. Similar reasoning shows that if V_r is negative, I_r flows in the same direction as I_1.

It is sometimes easier to determine the effect of V_r on line conditions by thinking of it as an independent voltage generator in series with R_T. With this concept, the direction of I_r is immediately apparent; its magnitude, however, is the ratio of V_r to Z_0, i.e., R_T is already accounted for in the magnitude of V_r. The relationships between incident and reflected signals are represented in *Figure 3-2* for both cases of mismatch between R_T and Z_0.

The incident wave is shown in *Figure 3-2a*, before it has reached the end of the line. In *Figure 3-2b*, a positive V_r is returning to the generator. To the left of V_r the current is still I_1, flowing to the right, while to the right of V_r the net current in the line is the difference between I_1 and I_r. In *Figure 3-2c*, the reflection coefficient is negative, producing a negative V_r. This, in turn, causes an increase in the amount of current flowing to the right behind the V_r wave.



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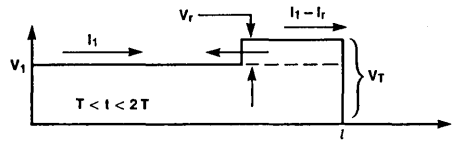
a. Incident Wave



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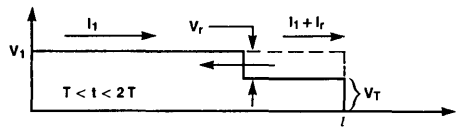
b. Reflected Wave for $R_T > Z_0$



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c. Reflected Wave for $R_T < Z_0$

FIGURE 3-2. Reflections for $R_T \neq Z_0$

Source Impedance, Multiple Reflections

When a reflected voltage arrives back at the source (generator), the reflection coefficient at the source determines the response to V_r. The coefficient of reflection at the source is governed by Z_0 and the source resistance R_S.

$$\rho_S = \frac{R_S - Z_0}{R_S + Z_0} \qquad (3\text{-}10)$$

If the source impedance matches the line impedance, a reflected voltage arriving at the source is not reflected back toward the load end. Voltage and current on the line are stable with the following values.

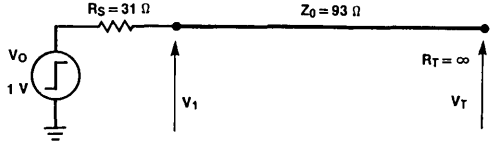
$$V_T = V_1 + V_r \text{ and } I_T = I_1 - I_r \qquad (3\text{-}11)$$

If neither source impedance nor terminating impedance matches Z_0, multiple reflections occur; the voltage at each end of the line comes closer to the final steady state value with each succeeding reflection. An example of a line mismatched on both ends is shown in *Figure 3-3*. The source is a step function of 1V amplitude occurring at time t_0. The initial value of V_1 starting down the line is 0.75V due to the voltage divider action of Z_0 and R_S. The time scale in the photograph shows that the line delay is approximately 6 ns. Since neither end of the line is terminated in its characteristic impedance, multiple reflections occur.

The amplitude and persistence of the ringing shown in *Figure 3-3* become greater with increasing mismatch between the line impedance and source and load impedances. Reducing R_S *(Figure 3-3)* to 13Ω increases ρ_S to −0.75V, and the effects are illustrated in *Figure 3-4*. The initial value of V_T is 1.8V with a reflection of 0.9V from the open end. When this reflection reaches the source, a reflection of 0.9V × −0.75V starts back toward the open end. Thus, the second increment of voltage arriving at the open end is negative going. In turn, a negative-going reflection of 0.9V × −0.75V starts back toward the source. This negative increment is again multiplied by −0.75 at the source and returned toward the open end. It can be deduced that the difference in amplitude between the first two positive peaks observed at the open end is

$$V_T - V'_T = (1 + \rho_L) V_1 - (1 + \rho_L) V_1 \rho^2_L \rho^2_S = (1 + \rho_L) V_1 (1 - \rho^2_L \rho^2_S). \qquad (3\text{-}12)$$

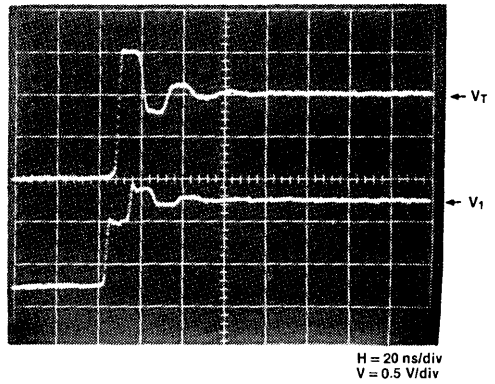
The factor $(1 - \rho^2_L \rho^2_S)$ is similar to the damping factor associated with lumped constant circuitry. It expresses the attenuation of successive positive or negative peaks of ringing.



TL/F/9900–5

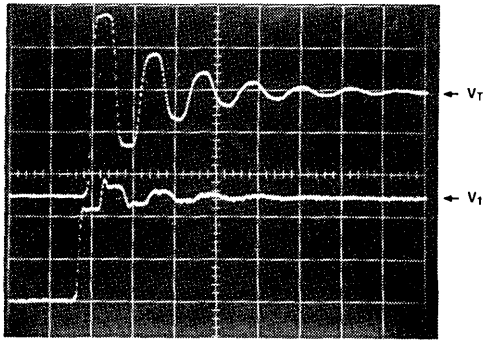
$$\rho_S = \frac{31 - 93}{31 + 93} = -0.5 \qquad \rho_L = \frac{\infty - 93}{\infty + 93} = +1$$

$$\text{Initially: } V_1 = \frac{Z_0}{Z_0 + R_S} \bullet V_O = \frac{93}{124} \bullet 1 = 0.75V$$



TL/F/9900–6

FIGURE 3-3. Multiple Reflections Due to Mismatch at Load and Source



TL/F/9900–7

FIGURE 3-4. Extended Ringing when R_S of *Figure 3-3* is Reduced to 13Ω

Lattice Diagram

In the presence of multiple reflections, keeping track of the incremental waves on the line and the net voltage at the ends becomes a bookkeeping chore. A convenient and systematic method of indicating the conditions which combines magnitude, polarity and time utilizes a graphic construction called a lattice diagram.[4] A lattice diagram for the line conditions of *Figure 3-3* is shown in *Figure 3-5*.

The vertical lines symbolize discontinuity points, in this case the ends of the line. A time scale is marked off on each line in increments of 2T, starting at t_0 for V_1 and T for V_T. The diagonal lines indicate the incremental voltages traveling between the ends of the line; solid lines are used for positive voltages and dashed lines for negative. It is helpful to write the reflection and transmission multipliers ρ and (1 + ρ) at each vertical line, and to tabulate the incremental and net voltages in columns alongside the vertical lines. Both the lattice diagram and the waveform photograph show that V_1 and V_T asymptotically approach 1V, as they must with a 1V source driving an open-ended line.

Lattice Diagram (Continued)

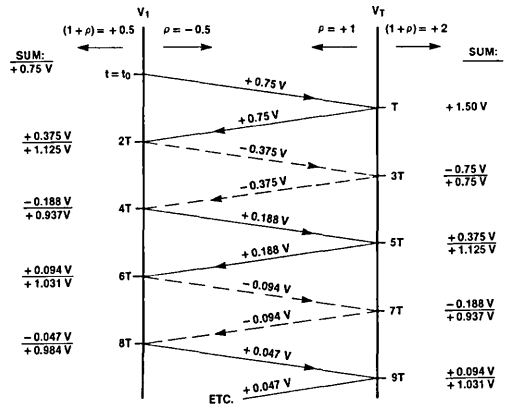


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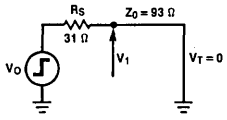
FIGURE 3-5. Lattice Diagram for the Circuit of *Figure 3-3*

Shorted Line

The open-ended line in *Figure 3-3* has a reflection coefficient of +1 and the successive reflections tend toward the steady state conditions of zero line current and a line voltage equal to the source voltage. In contrast, a shorted line has a reflection coefficient of −1 and successive reflections must cause the line conditions to approach the steady state conditions of zero voltage and a line current determined by the source voltage and resistance.

Shorted line conditions are shown in *Figure 3-6a* with the reflection coefficient at the source end of the line also negative. A negative coefficient at both ends of the line means that any voltage approaching either end of the line is reflected in the opposite polarity. *Figure 3-6b* shows the response to an input step-function with a duration much longer than the line delay. The initial voltage starting down the line is about +0.75V, which is inverted at the shorted end and returned toward the source as −0.75V. Arriving back at the source end of the line, this voltage is multiplied by $(1 + \rho_S)$, causing a −0.37V net change in V_1. Concurrently, a reflected voltage of +0.37V (−0.75V times ρ_S of −0.5) starts back toward the shorted end of the line. The voltage at V_1 is reduced by 50% with each successive round trip of reflections, thus leading to the final condition of zero volts on the line.

When the duration of the input pulse is less than the delay of the line, the reflections observed at the source end of the line constitute a train of negative pulses, as shown in *Figure 3-6c*. The amplitude decreases by 50% with each successive occurrence as it did in *Figure 3-6b*.

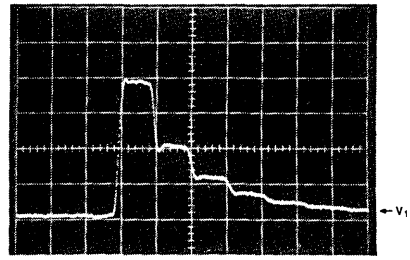


TL/F/9900–9

$\rho_S = -0.5$

$$\rho_L = \frac{0 - 93}{0 + 93} = -1$$

a. Reflection Coefficients for Shorted Line



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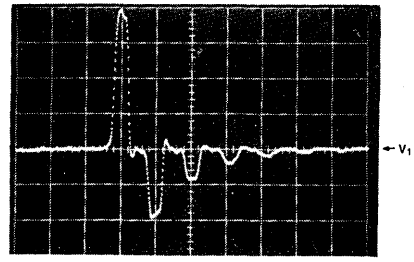
b. Input Pulse Duration ≫ Line Delay



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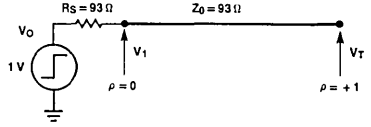
c. Input Pulse Duration < Line Delay

FIGURE 3-6. Reflections of Long and Short Pulses on a Shorted Line

Series Termination

Driving an open-ended line through a source resistance equal to the line impedance is called series termination. It is particularly useful when transmitting signals which originate on a PC board and travel through the backplane to another board, with the attendant discontinuities, since reflections coming back to the source are absorbed and ringing thereby controlled. *Figure 3-7* shows a 93Ω line driven from a 1V generator through a source impedance of 93Ω. The photograph illustrates that the amplitude of the initial signal sent down the line is only half of the generator voltage, while the voltage at the open end of the line is doubled to full amplitude ($1 + \rho_L = 2$). The reflected voltage arriving back at the source raises V_1 to the full amplitude of the generator signal. Since the reflection coefficient at the source is zero, no further changes occur and the line voltage is equal to the generator voltage. Because the initial signal on the line is only half the normal signal swing, the loads must be connected at or near the end of the line to avoid receiving a 2-step input signal.

An ECL output driving a series terminated line requires a pull-down resistor to V_{EE}, as indicated in *Figure 3-8*. The resistor R_0 shown in *Figure 3-8* symbolizes the output resistance of the ECL gate. The relationships between R_0, R_S, R_E and Z_0 are discussed in Chapter 4.



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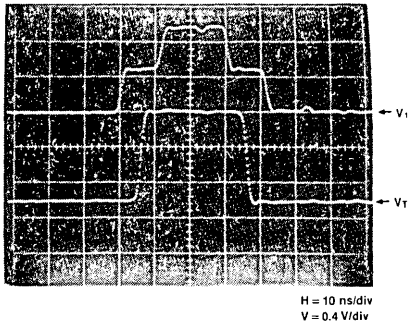

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FIGURE 3-7. Series Terminated Line and Waveforms

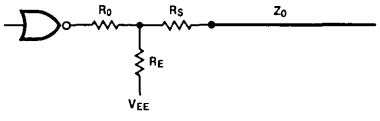

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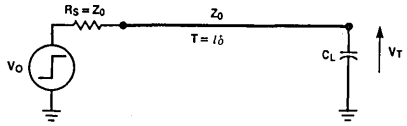
FIGURE 3-8. ECL Element Driving a Series Terminated Line

Extra Delay with Termination Capacitance

Designers should consider the effect of the load capacitance at the end of the line when using series termination. *Figure 3-9* shows how the output waveform changes with increasing load capacitance. *Figure 3-9b* shows the effect of load capacitances of 0, 12, 24, 48 pF. With no load, the delay between the 50% points of the input and output is just the line delay T. A capacitive load at the end of the line causes an extra delay ΔT due to the increase in rise time of the output signal. The midpoint of the output is used as a criterion because the propagation delay of an ECL circuit is measured between the 50% points of the input and output signals.



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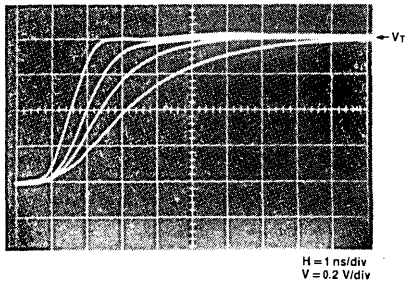
a. Series Terminated Line with Load Capacitance



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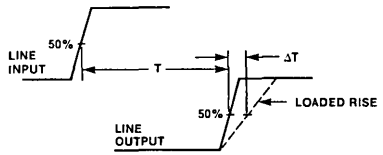
b. Output Rise Time Increase with Increasing Load Capacitance



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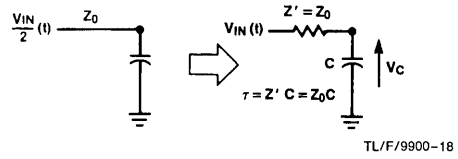
c. Extra Delay ΔT Due to Rise Time Increase

FIGURE 3-9. Extra Delay with Termination Capacitance

Extra Delay with Termination Capacitance (Continued)



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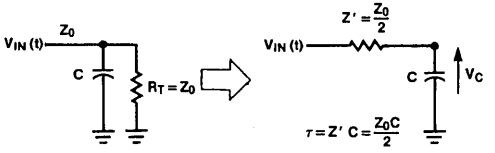
a. Thevenin Equivalent for Series Terminated Case



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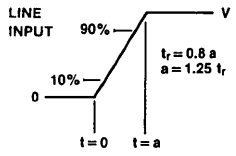
b. Thevenin Equivalent for Parallel Terminated Case



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$$v_{in}(t) = \frac{V}{a}[\,tu(t) - (t-a)u(t-a)]$$

$$u(t) = \begin{matrix} 0 \text{ for } t < O \\ 1 \text{ for } t > O \end{matrix}$$

$$u(t-a) = \begin{matrix} 0 \text{ for } t < a, \\ 1 \text{ for } t > a \end{matrix}$$

$$V_{IN}(S) = \frac{V}{as^2}(1 - e^{-as})$$

$$V_C(S) = \frac{V}{ar} \bullet \frac{1}{s^2(s + 1/\tau)}(1 - e^{-as})$$

$$v_c(t) = \frac{V}{a}[t - \tau(1 - e^{-t/\tau})]\,u(t)$$

$$-\frac{V}{a}[(t-a)$$

$$-\tau(1 - e^{-\frac{t-a}{\tau}})]\,u(t-a)$$

c. Equations for Input and Output Voltages

FIGURE 3-10. Determining the Effect of End-of-Line Capacitance

The increase in propagation delay can be calculated by using a ramp approximation for the incident voltage and characterizing the circuit as a fixed impedance in series with the load capacitance, as shown in *Figure 3-10*. One general solution serves both series and parallel termination cases by using an impedance Z′ and a time constant τ, defined in *Figure 3-10a* and *3-10b*. Calculated and observed increases in delay time to the 50% point show close agreement when τ is less than half the ramp time. At large ratios of τ/a (where a = ramp time), measured delays exceed calculated values by approximately 7%. *Figure 3-11*, based on measured values, shows the increase in delay to the 50% point as a function of the Z′C time constant, both normalized to the 10% to 90% rise time of the input signal. As an example of using the graph, consider a 100Ω series terminated line with 30 pF load capacitance at the end of the line and a no-load rise time of 3 ns for the input signal. From *Figure 3-10a*, Z′ is equal to 100Ω; the ratio $Z'C/t_r$ is 1. From the graph, the ratio $\Delta T/t_r$ is 0.8. Thus the increase in the delay to the 50% point of the output waveform is 0.8 t_r, or 2.4 ns, which is then added to the no-load line delay T to determine the total delay.

Had the 100Ω line in the foregoing example been parallel rather than series terminated at the end of the line, Z′ would be 50Ω. The added delay would be only 1.35 ns with the same 30 pF loading at the end. The added delay would be only 0.75 ns if the line were 50Ω and parallel terminated. The various trade-offs involving type of termination, line impedance, and loading are important considerations for critical delay paths.

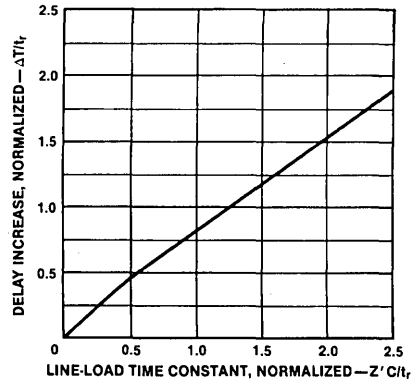

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FIGURE 3-11. Increase in 50% Point Delay Due to Capacitive Loading at the End of the Line, Normalized to T_r

Distributed Loading Effects on Line Characteristics

When capacitive loads such as ECL inputs are connected along a transmission line, each one causes a reflection with a polarity opposite to that of the incident wave. Reflections from two adjacent loads tend to overlap if the time required for the incident wave to travel from one load to the next is equal to or less than the signal rise time.[5] *Figure 3-12a* illustrates an arrangement for observing the effects of capacitive loading, while *Figure 3-12b* shows an incident wave followed by reflections from two capacitive loads. The two capacitors causing the reflections are separated by a distance requiring a travel time of 1 ns. The two reflections return to the source 2 ns apart, since it takes 1 ns longer for the incident wave to reach the second capacitor and an additional 1 ns for the second reflection to travel back to the source. In the upper trace of *Figure 3-12b*, the input signal rise time is 1 ns and there are two distinct reflections, although the trailing edge of the first overlaps the leading edge of the second. The input rise time is longer in the middle trace, causing a greater overlap. In the lower trace, the 2 ns input rise time causes the two reflections to merge and appear as a single reflection which is relatively constant (at $\approx -10\%$) for half its duration. This is about the same reflection that would occur if the 93Ω line had a middle section with an impedance reduced to 75Ω.

With a number of capacitors distributed all along the line of *Figure 3-12a*, the combined reflections modify the observed input waveform as shown in the top trace of *Figure 3-12c*. The reflections persist for a time equal to the 2-way line delay (15 ns), after which the line voltage attains its final value. The waveform suggests a line terminated with a resistance greater than its characteristic impedance ($R_T >$ Z_0). This analogy is strengthened by observing the effect of reducing R_T from 93Ω to 75Ω, which leads to the middle waveform of *Figure 3-12c*. Note that the final (steady state) value of the line voltage is reduced by about the same amount as that caused by the capacitive reflections. In the lower trace of *Figure 3-12c* the source resistance R_S is reduced from 93Ω to 75Ω, restoring both the initial and final line voltage values to the same amplitude as the final value in the upper trace. From the standpoint of providing a desired signal voltage on the line and impedance matching at either end, the effect of distributed capacitive loading can be treated as a reduction in line impedance.

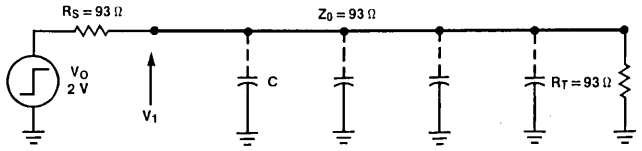
The reduced line impedance can be calculated by considering the load capacitance C_L as an increase in the intrinsic line capacitance C_0 along that portion of the line where the loads are connected.[6] Denoting this length of line as l, the distributed value C_D of the load capacitance is as follows.

$$C_D = \frac{C_L}{l}$$

C_D is then added to C_0 in *Equation 3-1* to determine the reduced line impedance Z_0.

$$Z'_0 = \sqrt{\frac{L_0}{C_0 + C_D}} = \sqrt{\frac{L_0}{C_0\left(1 + \frac{C_D}{C_0}\right)}} \qquad (3\text{-}13)$$

$$Z'_0 + \frac{\sqrt{\frac{L_0}{C_0}}}{\sqrt{1 + \frac{C_D}{C_0}}} = \frac{Z_0}{\sqrt{1 + \frac{C_D}{C_0}}}$$



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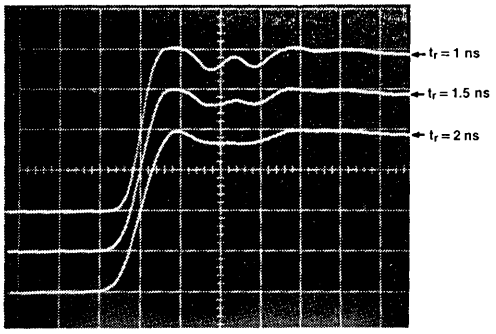
a. Arrangement for Observing Capacitive Loading Effects



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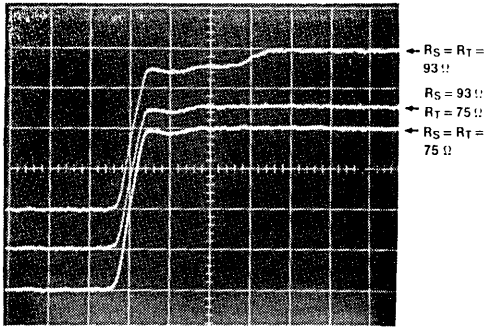
b. Capacitive Reflections Merging as Rise Time Increases



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c. Matching the Altered Impedance of a Capacitively Loaded Line

FIGURE 3-12. Capacitive Reflections and Effects on Line Characteristics

Distributed Loading Effects on Line Characteristics (Continued)

In the example of *Figure 3-12c*, the total load capacitance is 33 pF while the total intrinsic line capacitance $/C_0$ is 60 pF. (Note that the ratio C_D/C_0 is the same as $C_L//C_0$.) The calculated value of the reduced impedance is thus

$$Z'_0 = \frac{93}{\sqrt{1+\frac{33}{60}}} = \frac{93}{\sqrt{1.55}} = 75\Omega \qquad (3\text{-}14)$$

This correlates with the results observed in *Figure 3-12c* when R_T and R_S are reduced to 75Ω.

The distributed load capacitance also increases the line delay, which can be calculated from *Equation 3-2*.

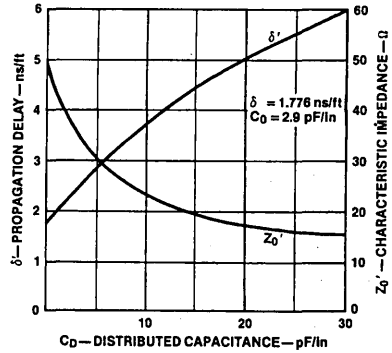
$$\delta' = \sqrt{L_0 (C_0 + C_D)} = \sqrt{L_0 C_0}\sqrt{1+\frac{C_D}{C_0}} = \delta\sqrt{1+\frac{C_D}{C_0}} \qquad (3\text{-}15)$$

The line used in the example of *Figure 3-12c* has an intrinsic delay of 6 ns and a loaded delay of 7.5 ns which checks with *Equation 3-15*.

$$/\delta' = /\delta\sqrt{1.55} = 6\sqrt{1.55} = 7.5\text{ ns} \qquad (3\text{-}16)$$

Equation 3-15 can be used to predict the delay for a given line and load. The ratio C_D/C_0 (hence the loading effect) can be minimized for a given loading by using a line with a high intrinsic capacitance C_0.

A plot of Z' and δ' for a 50Ω line as a function of C_D is shown in *Figure 3-13*. This figure illustrates that relatively modest amounts of load capacitance will add appreciably to the propagation delay of a line. In addition, the characteristic impedance is reduced significantly.



TL/F/9900–25

FIGURE 3-13. Capacitive Loading Effects on Line Delay and Impedance

Worst case reflections from a capacitively loaded section of transmission line can be accurately predicted by using the modified impedance of *Equation 3-9*.[6] When a signal originates on an unloaded section of line, the effective reflection coefficient is as follows.

$$\rho = \frac{Z'_0 - Z_0}{Z'_0 + Z_0} \qquad (3\text{-}17)$$

Mismatched Lines

Reflections occur not only from mismatched load and source impedances but also from changes in line impedance. These changes could be caused by bends in coaxial cable, unshielded twisted-pair in contact with metal, or mismatch between PC board traces and backplane wiring. With the coax or twisted-pair, line impedance changes run about 5% to 10% and reflections are usually no problem since the percent reflection is roughly half the percent change in impedance. However, between PC board and backplane wiring, the mismatch can be 2 or 3 to 1. This is illustrated in *Figure 3-14* and analyzed in the lattice diagram of *Figure 3-15*. Line 1 is driven in the series terminated mode so that reflections coming back to the source are absorbed.

The reflection and transmission at the point where impedances differ are determined by treating the downstream line as though it were a terminating resistor. For the example of *Figure 3-14*, the reflection coefficient at the intersection of lines 1 and 2 for a signal traveling to the right is as follows.

$$\rho_{12} = \frac{Z_2 - Z_1}{Z_2 + Z_1} = \frac{93 - 50}{143} = +0.3 \qquad (3\text{-}18)$$

Thus the signal reflected back toward the source and the signal continuing along line 2 are, respectively, as follows.

$$V_{1r} = \rho_{12} V_1 = +0.3V_1 \qquad (3\text{-}19a)$$

$$V_2 = (1 + \rho_{12}) V_1 = +1.3\, V_1 \qquad (3\text{-}19b)$$

At the intersection of lines 2 and 3, the reflection coefficient for signals traveling to the right is determined by treating Z_3 as a terminating resistor.

$$\rho_{23} = \frac{Z_3 - Z_2}{Z_3 + Z_2} = \frac{39 - 93}{132} = -0.41 \qquad (3\text{-}20)$$

When V_2 arrives at this point, the reflected and transmitted signals are as follows.

$$V_{2r} = \rho_{23} V_2 = -0.41\, V_2 = (-0.41)(1.3)\, V_1 = -0.53\, V_1 \qquad (3\text{-}21a)$$

$$V_3 = (1 + \rho_{23}) V_2 = 0.59\, V_2 = (0.59)(1.3)\, V_1 = 0.77\, V_1 \qquad (3\text{-}21b)$$

Voltage V_3 is doubled in magnitude when it arrives at the open-ended output, since ρ_L is +1. This effectively cancels the voltage divider action between R_S and Z_1.

$$V_4 = (1 + \rho_L) V_3 = (1 + \rho_L)(1 + \rho_{23}) V_2 = (1 + \rho_L)(1 + \rho_{23})(1 + \rho_{12}) V_1 = (1 + \rho_L)(1 + \rho_{23})(1 + \rho_{12})\frac{V_0}{2} \qquad (3\text{-}22)$$

$$V_4 = (1 + \rho_{23})(1 + \rho_{12}) V_O$$

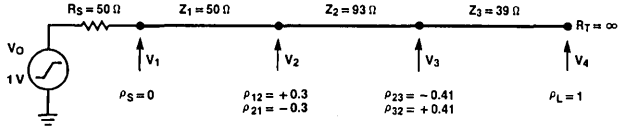
Thus, *Equation 3-22* is the general expression for the initial step of output voltage for three lines when the input is series terminated and the output is open-ended.

Mismatched Lines (Continued)

Note that the reflection coefficients at the intersections of lines 1 and 2 and lines 2 and 3 in *Figure 3-15* have reversed signs for signals traveling to the left. Thus the voltage reflected from the open output and the signal reflecting back and forth on line 2 both contribute additional increments of output voltage in the same polarity as V_O. Lines 2 and 3 have the same delay time; therefore, the two aforementioned increments arrive at the output simultaneously at time 5T on the lattice diagram *(Figure 3-15)*.

In the general case of series lines with different delay times, the vertical lines on the lattice diagram should be spaced apart in the ratio of the respective delays. *Figure 3-16* shows this for a hypothetical case with delay ratios 1:2:3. For a sequence of transmission lines with the highest impedance line in the middle, at least three output voltage increments with the same polarity as V_O occur before one can occur of opposite polarity. On the other hand, if the middle line has the lowest impedance, the polarity of the second increment of output voltage is the opposite of V_O. The third increment of output voltage has the opposite polarity, for the time delay ratios of *Figure 3-16*.

When transmitting logic signals, it is important that the initial step of line output voltage pass through the threshold region of the receiving circuit, and that the next two increments of output voltage augment the initial step. Thus in a series terminated sequence of three mismatched lines, the middle line should have the highest impedance.



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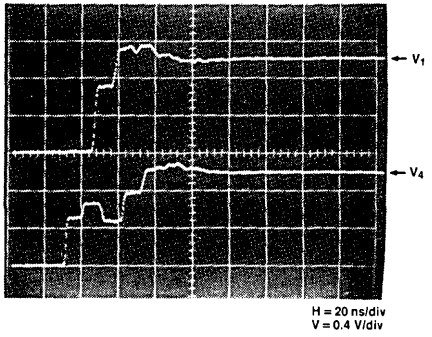

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FIGURE 3-14. Reflections from Mismatched Lines

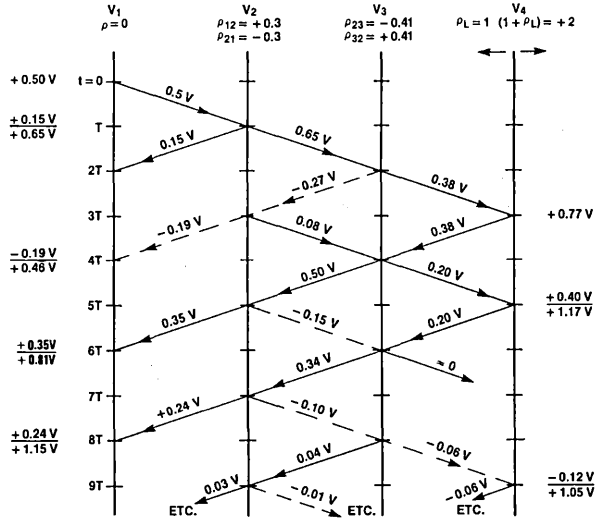

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FIGURE 3-15. Lattice Diagram for the Circuit of *Figure 3-14*

Mismatched Lines (Continued)

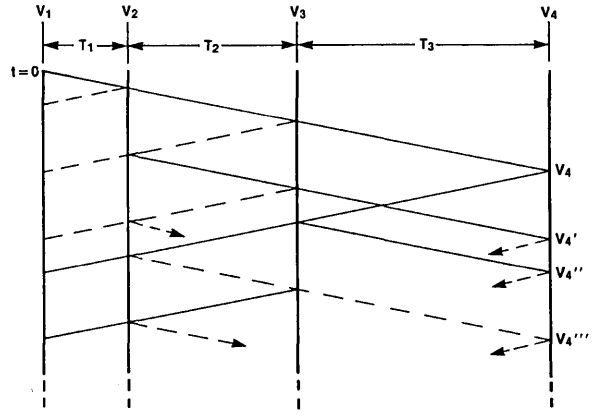

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FIGURE 3-16. Lattice Diagram for Three Lines with Delay Ratios 1:2:3

Rise Time versus Line Delay

When the 2-way line delay is less than the rise time of the input wave, any reflections generated at the end of the line are returned to the source before the input transition is completed. Assuming that the generator has a finite source resistance, the reflected wave adds algebraically to the input wave while it is still in transition, thereby changing the shape of the input. This effect is illustrated in *Figure 3-17*, which shows input and output voltages for several comparative values of rise time and line delay.

In *Figure 3-17b* where the rise time is much shorter than the line delay, V_1 rises to an initial value of 1V. At time T later, V_T rises to 0.5V, i.e., $1 + \rho_L = 0.5$. The negative reflection arrives back at the source at time 2T, causing a net change of -0.4V, i.e., $(1 + \rho_S)(-0.5) = -0.4$.

The negative coefficient at the source changes the polarity of the other 0.1V of the reflection and returns it to the end of the line, causing V_T to go positive by another 50 mV at time 3T. The remaining 50 mV is inverted and reflected back to the source, where its effect is barely distinguishable as a small negative change at time 4T.

In *Figure 3-17c*, the input rise time (0% to 100%) is increased to such an extent that the input ramp ends just as the negative reflection arrives back at the source end. Thus the input rise time is equal to 2T.

The input rise time is increased to 4T in *Figure 3-17d*, with the negative reflection causing a noticeable change in input slope at about its midpoint. This change in slope is more visible in the double exposure photo of *Figure 3-17e*, which shows V_1 (t_r still set for 4T) with and without the negative reflection. The reflection was eliminated by terminating the line in its characteristic impedance.

The net input voltage at any particular time is determined by adding the reflection to the otherwise unaffected input. It must be remembered that the reflection arriving back at the input at a given time is proportional to the input voltage at a time 2T earlier. The value of V_1 in *Figure 3-17d* can be calculated by starting with the 1V input ramp.

$$V_1 = \frac{1}{t_r} \bullet t \quad \text{for } 0 \le t \le 4T \tag{3-23}$$

$$= 1\text{V} \quad \text{for } t \ge 4T$$

The reflection from the end of the line is

$$V_r = \frac{\rho_L (t - 2T)}{t_r}; \tag{3-24}$$

the portion of the reflection that appears at the input is

$$V'_r = \frac{(1 + \rho_S)\,\rho_L (t - 2T)}{t_r}; \tag{3-25}$$

the net value of the input voltage is the sum.

$$V'_1 = \frac{t}{t_r} + \frac{(1 + \rho_S) + \rho_L (t - 2T)}{t_r} \tag{3-26}$$

The peak value of the input voltage in *Figure 3-17d* is determined by substituting values and letting t equal 4T.

$$V'_1 = 1 + \frac{(0.8)(-0.5)(4T - 2T)}{t_r} \tag{3-27}$$

$$= 1 - 0.4\,(0.5) = 0.8\text{V}$$

After this peak point, the input ramp is no longer increasing but the reflection is still arriving. Hence the net value of the input voltage decreases. In this example, the later reflections are too small to be detected and the input voltage is thus stable after time 6T. For the general case of repeated reflections, the net voltage $V_{1(t)}$ seen at the driven end of the line can be expressed as follows, where the signal caused by the generator is $V_{1(t)}$.

Rise Time versus Line Delay (Continued)

$$V'_{1(t)} = V_{1(t)} \quad \text{for } 0 < t < 2T$$

$$V'_{1(t)} = V_{1(t)} + (1 + \rho_S)\,\rho_L\,V_{1(t-2T)} \quad \text{for } 2T < t < 4T$$

$$V'_{1(t)} = V_{1(t)} + (1 + \rho_S)\,\rho_L\,V_{1(t-2T)} + (1 + \rho_S)\,\rho_S\rho_L^2\,V_{1(t-4T)} \quad \text{for } 4T < t < 6T \qquad (3\text{-}28)$$

$$V'_{1(t)} = V_{1(t)} + (1 + \rho_S)\,\rho_L\,V_{1(t-2T)} + (1 + \rho_S)\,\rho_S\rho_L^2\,V_{1(t-4T)} + (1 + \rho_S)\,\rho_S^2\rho_L^3\,V_{1(t-6T)} \quad \text{for } 6T < t < 8T, \text{ etc.}$$

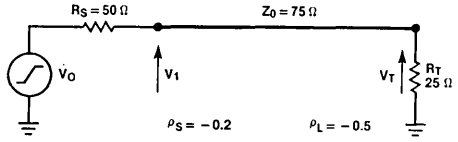
The voltage at the output end of the line is expressed in a similar manner.

$$V_{T(t)} = 0 \quad \text{for } 0 < t < T$$

$$V_{T(t)} = (1 + \rho_L)\,V_{1(t-T)} \quad \text{for } T < t < 3T$$

$$V_{T(t)} = (1 + \rho_L)\,V_{1(t-T)} + (1 + \rho_L)\,\rho_S\rho_L\,V_{1(t-3T)} \quad \text{for } 3T < t < 5T \qquad (3\text{-}29)$$

$$V_{T(t)} = (1 + \rho_L)\,V_{1(t-T)} + (1 + \rho_L)\,\rho_S\rho_L V_{1(t-3T)} + (1 + \rho_L)\,\rho_S^2\rho_L^2\,V_{1(t-5T)} \quad \text{for } 5T < t < 7T, \text{ etc.}$$



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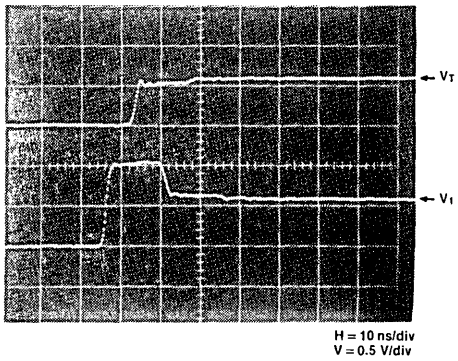
a. Test Arrangement for Rise Time Analysis



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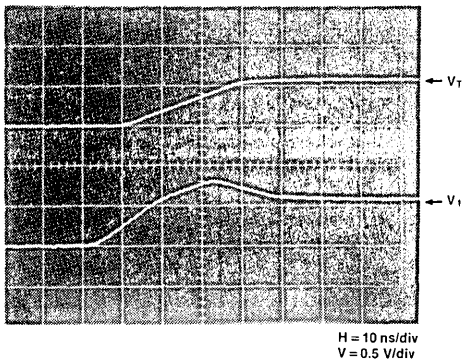
b. Line Voltages for $t_r \ll T$



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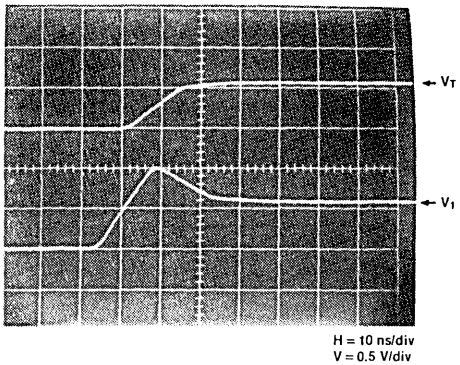
d. Line Voltages for $t_r = 4T$



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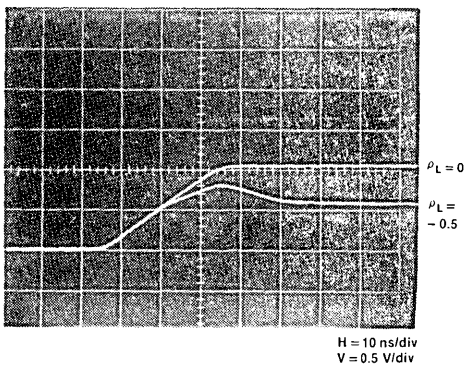
c. Line Voltages for $t_r = 2T$



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e. Input Voltage with and without Reflection

FIGURE 3-17. Line Voltages for Various Ratios of Rise Time to Line Delay

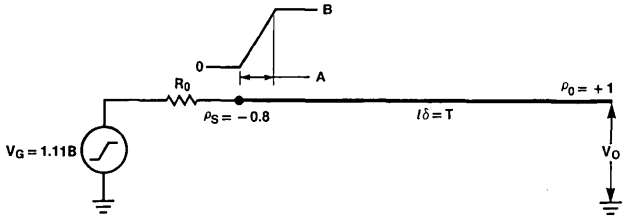
Ringing

Multiple reflections occur on a transmission line when neither the signal source impedance nor the termination (load) impedance matches the line impedance. When the source reflection coefficient ρ_S and the load reflection coefficient ρ_L are of opposite polarity, the reflections alternate in polarity. This causes the signal voltage to oscillate about the final steady state value, commonly recognized as ringing.

When the signal rise time is long compared to the line delay, the signal shape is distorted because the individual reflections overlap in time. The basic relationships among rise time, line delay, overshoot and undershoot are shown in a simplified diagram, *Figure 3-18*. The incident wave is a ramp of amplitude B and rise duration A. The reflection coefficient at the open-ended line output is +1 and the source reflection coefficient is assumed to be −0.8, i.e., $R_0 = Z_0/9$.

Figure 3-18b shows the individual reflections treated separately. Rise time A is assumed to be three times the line delay T. The time scale reference is the line output and the first increment of output voltage V_O rises to 2B in the time interval A. Simultaneously, a positive reflection (not shown) of amplitude B is generated and travels to the source, whereupon it is multiplied by −0.8 and returns toward the end of the line. This negative-going ramp starts at time 2T (twice the line delay) and doubles to −1.6B at time 2T + A.

The negative-going increment also generates a reflection of amplitude −0.8B which makes the round trip to the source and back, appearing at time 4T as a positive ramp rising to +1.28B at time 4T + A. The process of reflection and re-reflection continues, and each successive increment changes in polarity and has an amplitude of 80% of the preceding increment.



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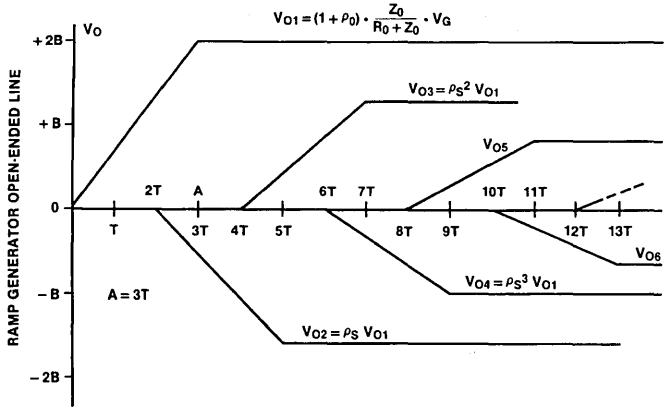
a. Ramp Generator Driving Open-Ended Line



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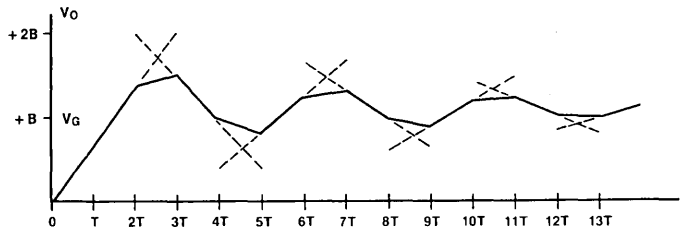
b. Increments of Output Voltage Treated Individually



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c. Net Output Signal Determined by Superposition

FIGURE 3-18. Basic Relationships Involved in Ringing

Ringing (Continued)

In *Figure 3-18c*, the output increments are added algebraically by superposition. The starting point of each increment is shifted upward to a voltage value equal to the algebraic sum of the quiescent levels of all the preceding increments (i.e., 0, 2B, 0.4B, 1.68B, etc.). For time intervals when two ramps occur simultaneously, the two linear functions add to produce a third ramp that prevails during the overlap time of the two increments.

It is apparent from the geometric relationships, that if the ramp time A is less than twice the line delay, the first output increment has time to rise to the full 2B amplitude and the second increment reduces the net output voltage to 0.4B. Conversely, if the line delay is very short compared to the ramp time, the excursions about the final value V_G are small.

Figure 3-18c shows that the peak of each excursion is reached when the earlier of the two constituent ramps reaches its maximum value, with the result that the first peak occurs at time A. This is because the earlier ramp has a greater slope (absolute value) than the one that follows.

Actual waveforms such as produced by ECL or TTL do not have a constant slope and do not start and stop as abruptly as the ramp used in the example of *Figure 3-18*. Predicting the time at which the peaks of overshoot and undershoot occur is not as simple as with ramp excitation. A more rigorous treatment is required, including an expression for the driving waveform which closely simulates its actual shape. In the general case, a peak occurs when the sum of the slopes of the individual signal increment is zero.

Summary

The foregoing discussions are by no means an exhaustive treatment of transmission line characteristics. Rather, they are intended to focus attention on the general methods used to determine the interactions between high-speed logic circuits and their interconnections. Considering an interconnection in terms of distributed rather than lumped inductance and capacitance leads to the line impedance concept, i.e., mismatch between this characteristic impedance and the terminations causes reflections and ringing.

Series termination provides a means of absorbing reflections when it is likely that discontinuities and/or line impedance changes will be encountered. A disadvantage is that the incident wave is only one-half the signal swing, which limits load placement to the end of the line. ECL input capacitance increases the rise time at the end of the line, thus increasing the effective delay. With parallel termination, i.e., at the end of the line, loads can be distributed along the line. ECL input capacitance modifies the line characteristics and should be taken into account when determining line delay.

References

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2. Skilling, H., *Electric Transmission Lines*, McGraw-Hill, (1951).
3. Matick, R., *Transmission Lines for Digital and Communication Networks*, McGraw-Hill, (1969).
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5. "Time Domain Reflectometry", *Hewlett-Packard Journal*, Vol. 15, No. 6, (February 1964).
6. Feller, A., Kaupp H., and Digiacoma, J., "Crosstalk and Reflections in High-Speed Digital Systems", *Proceedings, Fall Joint Computer Conference*, (1965).

National Semiconductor

Chapter 4
System Considerations

Introduction

All of National's ECL input and output impedances are designed to accommodate various methods of driving and terminating interconnections. Controlled wiring impedance makes it possible to use simplified equivalent circuits to determine limiting conditions. Specific guidelines and recommendations are based on assumed worst-case combinations. Many of the recommendations may seem conservative, compared to typical observations, but the intent is to help the designer achieve a reliable system in a reasonable length of time with a minimum amount of redesign.

PC Board Transmission Lines

Strictly speaking, transmission lines are not always required for F100K ECL but, when used, they provide the advantages of predictable interconnect delays as well as reflection and ringing control through impedance matching. Two common types of PC board transmission lines are microstrip and stripline, *Figure 4-1*. Stripline requires multilayer construction techniques; microstrip uses ordinary double-clad boards. Other board construction techniques are wire wrap, stitch weld and discrete wired.

Stripline, *Figure 4-1b*, is used where packing density is a high priority because increasing the interconnect layers provides short signal paths. Boards with as many as 22 layers have been used in ECL systems.

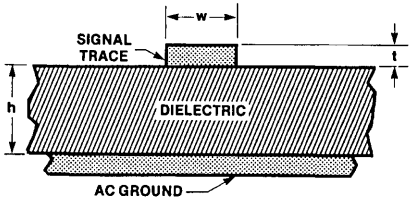
Microstrip offers easier fabrication and higher propagation velocity than stripline, but the routing for a complex system may require more design effort. In *Figure 4-1a*, the ground plane can be a part of the V_{EE} distribution as long as adequate bypassing from V_{EE} to V_{CC} (ground) is provided. Also, signal routing is simplified and an extra voltage plane is obtained by bonding two microstrip structures back to back, *Figure 4-1c*.

Microstrip

Equation 4-1 relates microstrip characteristic impedance to the dielectric constant and dimensions.[1] Electric field fringing requires that the ground extend beyond each edge of the signal trace by a distance no less than the trace width.

$$Z_0 = \left(\frac{60}{\sqrt{0.475\,\epsilon_r + 0.67}}\right) \ln\left(\frac{4h}{0.67\,(0.8\,w + t)}\right) = \left(\frac{87}{\sqrt{\epsilon_r + 1.41}}\right) \ln\left(\frac{5.98\,h}{0.8\,w + t}\right) \quad \textbf{(4-1)}$$

where h = dielectric thickness, w = trace width, t = trace thickness, ϵ_r = board material dielectric constant relative to air.



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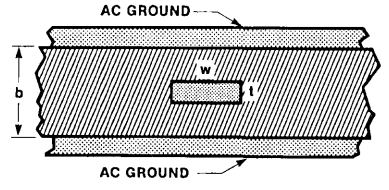
a. Microstrip



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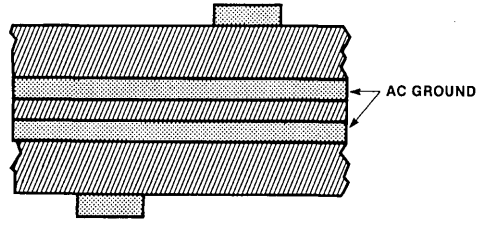
b. Stripline



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c. Composite Microstrip

FIGURE 4-1. Transmission Lines on Circuit Boards

PC Board Transmission Lines (Continued)

Equation 4-1 was developed from the impedance formula for a wire over ground plane transmission line, Equation 4-2.

$$Z_0 = \left(\frac{60}{\sqrt{\epsilon_r}}\right) \ln\left(\frac{4h}{d}\right) \quad \textbf{(4-2)}$$

where d = wire diameter, h = distance from ground to wire center.

Comparing Equation 4-1 and 4-2, the term 0.67 (0.8 w + t) shows the equivalence between a round wire and a rectangular conductor. The term 0.475 ϵ_r + 0.67 is the *effective* dielectric constant for microstrip ϵ_e, considering that a microstrip line has a compound dielectric consisting of the board material and air. The effective dielectric constant is determined by measuring propagation delay per unit of line length and using the following relationship.

$$\delta = 1.0167 \bullet \sqrt{\epsilon_e}\ \text{ns/ft} \quad \textbf{(4-3)}$$

where δ = propagation delay, ns/ft.

Propagation delay is a property of the dielectric material rather than line width or spacing. The coefficient 1.0167 is the reciprocal of the velocity of light in free space. Propagation delay for microstrip lines on glass-filled G-10 epoxy boards is typically 1.77 ns/ft, yielding an effective dielectric constant of 3.03.

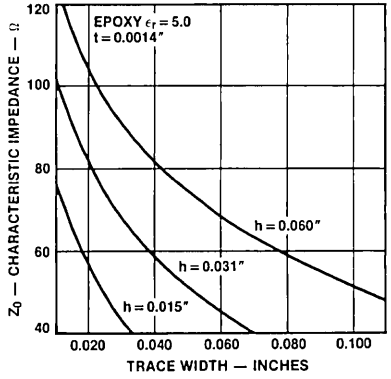

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FIGURE 4-2. Microstrip Impedance Versus Trace Width, G-10 Epoxy

Using ϵ_r = 5.0 in Equation 4-1, *Figure 4-2* provides microstrip line impedance as a function of width for several G-10 epoxy board thicknesses. *Figure 4-3* shows the related C_0 values, useful for determining capacitive loading effects on line characteristics, (Equation 3-15).

System designers should ascertain tolerances on board dimensions, dielectric constant and trace width etching in order to determine impedance variations. If conformal coating is used the effective dielectric constant of microstrip is increased, depending on the coating material and thickness.

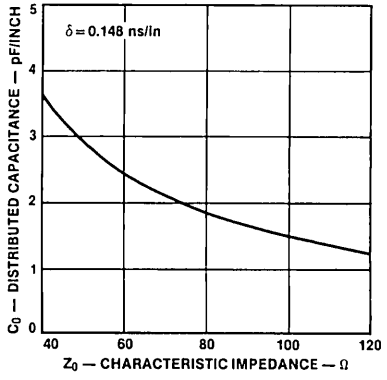

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FIGURE 4-3. Microstrip Distributed Capacitance Versus Impedance, G-10 Epoxy

Stripline

Stripline conductors are totally embedded. As a result, the board material determines the dielectric constant. G-10 epoxy boards have a typical propagation delay of 2.26 ns/ft. Equation 4-4 is used to calculate stripline impedances.[1,2]

$$Z_0 = \left(\frac{60}{\sqrt{\epsilon_r}}\right) \ln\left(\frac{4b}{0.67\,\pi\,(0.8\,w + t)}\right) \quad \textbf{(4-4)}$$

where b = distance between ground planes, w = trace width, t = trace thickness, w/(b-t) < 0.35 and t/b < 0.25.

Figure 4-4 shows stripline impedance as a function of trace width, using Equation 4-4 and various ground plane separations for G-10 glass-filled epoxy boards. Related values of C_0 are plotted in *Figure 4-5*.

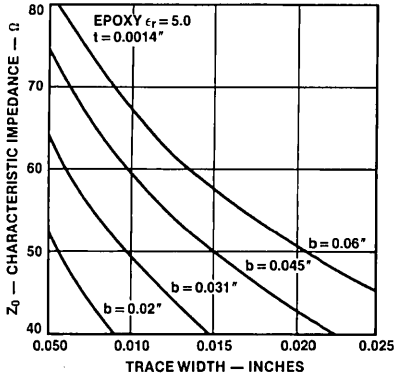

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FIGURE 4-4. Stripline Impedance Versus Trace Width, G-10 Epoxy

PC Board Transmission Lines (Continued)

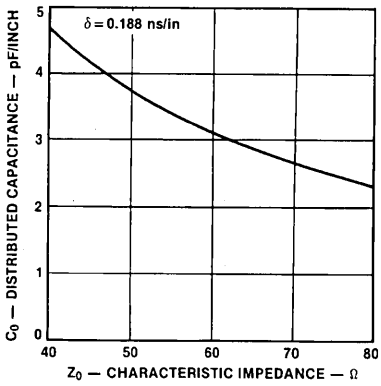

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FIGURE 4-5. Stripline Distributed Capacitance Versus Impedance, G-10 Epoxy

Wire Wrap

Wire-wrap boards are commercially available with five voltage planes, positions for several 24-pin Dual-In-Line Packages (DIP), terminating resistors, and decoupling capacitors. The devices are mounted on socket pins and interconnected with twisted pair wiring. One wire at each end of the twisted pair is wrapped around a signal pin, the other around a ground pin. The #30 insulated wire is uniformly twisted to provide a nominal 93Ω impedance line. Positions for Single-In-Line Package (SIP) terminating resistors are close to the inputs to provide good termination characteristics.

Discrete Wired

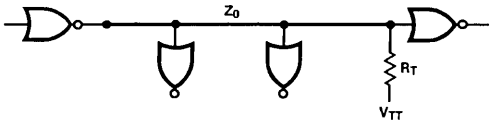
Custom Multiwire* boards are available with integral power and ground planes. Wire is placed on a controlled thickness above the ground plane to obtain a nominal impedance line of 55Ω. Then holes are drilled through the wire and board. Copper is deposited in the drilled holes by an additive-electrolysis process which bonds each wire to the wall of the holes. Devices are soldered on the board to make connection to the wires.

*Multiwire is a registered trademark of the Multiwire Corporation.

Parallel Termination

Terminating a line at the receiving end with a resistance equal to the characteristic line impedance is called parallel termination, *Figure 4-6a.* F100K circuits do not have internal pull-down resistors on outputs, so the terminating resistor must be returned to a voltage more negative than V_{OL} to establish the LOW-state output voltage from the emitter follower. A −2V termination return supply is commonly used. This minimizes power consumption and correlates with standard test specifications for ECL circuits. A pair of resistors connected in series between ground (V_{CC}) and the V_{EE} supply can provide the Thevenin equivalent of a single resistor to −2V if a separate termination supply is not available, *Figure 4-6b.* The average power dissipation in the Thevenin equivalent resistors is about 10 times the power dissipation in the single resistor returned to −2V, as shown in *Figures 5-10* and *5-13.* For either parallel termination method, decoupling capacitors are required between the supply and ground (Chapter 6).

a. Parallel Termination



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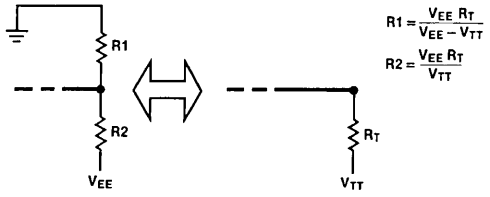
b. Thevenin Equivalent of R_T and V_{TT}



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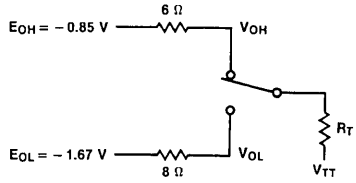
c. Equivalent Circuit for Determining Approximate V_{OH} and V_{OL} Levels



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d. F100K Output Characteristic with Terminating Resistor R_T Returned to V_{TT} = −2.0V

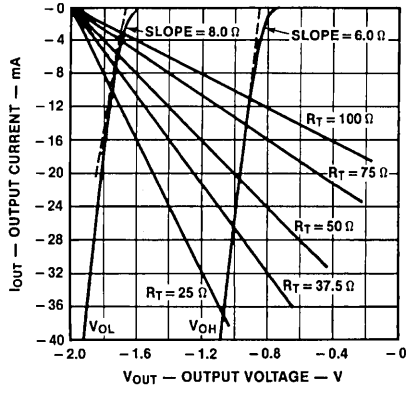

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FIGURE 4-6. Parallel Termination

PC Board Transmission Lines (Continued)

F100K output transistors are designed to drive low-impedance loads and have a maximum output current rating of 50 mA. The circuits are specified and tested with a 50Ω load returned to −2V. This gives nominal output levels of −0.955V at 20.9 mA and −1.705V at 5.9 mA. Output levels will be different with other load currents because of the transistor output resistance. This resistance is nonlinear with load current since it is due, in part, to the base-emitter voltage of the emitter follower, which is logarithmic with output current. With the standard 50Ω load, the effective source resistance is approximately 6Ω in the HIGH state and 8Ω in the LOW state.

The foregoing values of output voltage, output current, and output resistance are used to estimate quiescent output levels with different loads. An equivalent circuit is shown in *Figure 4-6c*. The ECL circuit is assumed to contain two internal voltage sources E_{OH} and E_{OL} with series resistances of 6Ω and 8Ω respectively. The values shown for E_{OH} and E_{OL} are −0.85V and −1.67V respectively.

The linearized portion of the F100K output characteristic can be represented by two equations:

For V_{OH}: $V_{OUT} = -850 - 6\,I_{OUT}$
For V_{OL}: $V_{OUT} = -1670 - 8\,I_{OUT}$

where I_{OUT} is in mA, V_{OUT} is in mV.

If the range of I_{OUT} is confined between 8 mA to 40 mA for V_{OH}, and 2 mA to 16 mA for V_{OL}, the output voltage can be estimated within ±10 mV *(Figure 4-6d)*.

An ECL output can drive two or more lines in parallel, provided the maximum rated current is not exceeded. Another consideration is the effect of various loads on noise margins. For example, two parallel 75Ω terminations to −2V (*Figure 4-6d*) give output levels of approximately −1.000V and −1.716V. Noise margins are thus 35 mV less in the HIGH state and 11 mV more in the LOW state, compared to 50Ω load conditions. Conversely, a single 75Ω load to −2V causes noise margins 38 mV greater in the HIGH state and 11 mV less in the Low state, compared to a 50Ω load.

The magnitude of reflections from the terminated end of the line depends on how well the termination resistance R_T matches the line impedance Z_0. The ratio of the reflected voltage to the incident voltage V_i is the reflection coefficient ρ.

$$\frac{V_r}{V_i} = \rho = \frac{R_T - Z_0}{R_T + Z_0} \qquad \textbf{(4-5)}$$

The initial signal swing at the termination is the sum of the incident and reflected voltages. The ratio of termination signal to incident signal is thus:

$$\frac{V_T}{V_i} = 1 + \rho = \frac{2R_T}{R_T + Z_0} \qquad \textbf{(4-6)}$$

The degree of reflections which can be tolerated varies in different situations, but to allow for worst-case circuits, a good rule of thumb is to limit reflections to 15% to prevent excursions into the threshold region of the ECL inputs connected along the line. The range of permissible values of R_T as a function of Z_0 and the reflection coefficient limitations can be determined by rearranging Equation 4-5.

$$R_T = Z_0 \frac{1 + \rho}{1 - \rho} \qquad \textbf{(4-7)}$$

Using 15% reflection limits as examples, the range of the R_T/Z_0 ratio is as follows.

$$\frac{1.15}{0.85} > \frac{R_T}{Z_0} > \frac{0.85}{1.15} \quad 1.35 > \frac{R_T}{Z_0} > 0.74 \qquad \textbf{(4-8)}$$

The permissible range of the R_T/Z_0 ratio determines the tolerance ranges for R_T and Z_0. For example, using the foregoing ratio limits, R_T tolerances of ±10% allow Z_0 tolerance limits of +22% and −19%; R_T tolerances of ±5% allow Z_0 tolerance limits of +28% and −23%.

An additional requirement on the maximum value of R_T is related to the value of quiescent I_{OH} current needed to insure sufficient negative-going signal swing when the ECL driver switches from the HIGH state to the LOW state. The npn emitter-follower output of the ECL circuit cannot act as a voltage source driver for negative-going transitions. When the voltage at the base of the emitter follower starts going negative as a result of an internal state change, the output current of the emitter follower starts to decrease. The transmission line responds to the decrease in current by producing a negative-going change in voltage. The ratio of the voltage change to the current change is, of course, the characteristic impedance Z_0. Since the maximum decrease in current that the line can experience is from I_{OH} to zero, the maximum negative-going transition which can be produced is the product $I_{OH}\,Z_0$.

If the $I_{OH}\,Z_0$ product is greater than the normal negative-going signal swing, the emitter follower responds by limiting the current change, thereby controlling the signal swing. If, however, the $I_{OH}\,Z_0$ product is too small, the emitter follower is momentarily turned off due to insufficient forward bias of its base-emitter junctions, causing a discontinuous negative-going edge such as the one shown in *Figure 4-14*. In the output-LOW state the emitter follower is essentially nonconducting for V_{OL} values more positive than about −1.55V. Using this value as a criterion and expressing I_{OH} and V_{OH} in terms of the equivalent circuit of *Figure 4-6c*, an upper limit on the value of R_T can be developed.

$$\Delta V = I_{OH}Z_0 > 1.55 - |V_{OH}|$$

$$\left(\frac{E_{OH} - V_{TT}}{R_0 + R_T}\right) Z_0 > 1.55 - \left|\frac{V_{TT}\,R_0 = E_{OH}R_T}{R_0 + R_T}\right|$$

$$R_T < \frac{(E_{OH} - V_{TT})\,Z_0 - (1.55 - |V_{TT}|)\,R_0}{1.55 - |E_{OH}|} \qquad \textbf{(4-9)}$$

For a V_{TT} of −2V, R_0 of 6Ω and E_{OH} of −0.85V, Equation 4-9 reduces to

$R_T < 1.64\,Z_0 + 3.86\Omega$

For $Z_0 = 50\Omega$, the emitter follower cuts off during a negative-going transition if R_T exceeds 86Ω. Changing the voltage level criteria to −1.60V to insure continuous conduction in the emitter follower gives an upper limit of 77Ω for a 50Ω line. For a line terminated at the receiving end with a resistance to −2V, a rough rule-of-thumb is that termination resistance should not exceed line impedance by more than 50%. This insures a satisfactory negatve-going signal swing to ECL inputs connected along the line. The quiescent V_{OL} level, after all reflections have damped out, is determined by R_T and the ECL output characteristic.

Input Impedance

The input impedance of ECL circuits is predominately capacitive. A single-function input has an effective value of about 2.5 pF for F100K flatpak, as determined by its effect on reflected and transmitted signals on transmission lines.

Input Impedance (Continued)

In practical calculations, a value of 3 pF should be used. Approximately one third of this capacitance is attributed to the internal circuitry and two thirds to the flatpak pin and internal bonding.

For F100K flatpak circuits, multiple input lines may appear to have up to 4 pF to 5 pF but never more. For example, in the 100302, an input is connected internally to all five gates, but because of the philosophy of buffering these types of inputs in the F100K family this input appears as a unit load with a capacitance of approximately 2.5 pF. For applications such as a data bus, with two or more outputs connected to the same line, the capacitance of a passive-LOW output can be taken as 3 pF.

Capacitive loads connected along a transmission line increase the propagation delay of a signal along the line. The modified delay can be determined by treating the load capacitance as an increase in the intrinsic distributed capacitance of the line, discussed in Chapter 3. The intrinsic capacitance of any stubs which connect the inputs to the line should be included in the load capacitance. The intrinsic capacitance per unit length for G-10 epoxy boards is shown in *Figure 4-3* and *4-5* for microstrip and stripline respectively. For other dielectric materials, the intrinsic capacitance C_0 can be determined by dividing the intrinsic delay δ (Equation 4-3) by the line impedance Z_0.

The length of a stub branching off the line to connect an input should be limited to insure that the signal continuing along the line past the stub has a continuous rise, as opposed to a rise (or fall) with several partial steps. The point where a stub branches off the line is a low impedance point. This creates a negative coefficient of reflection, which in turn reduces the amplitude of the incident wave as it continues beyond the branch point. If the stub length is short enough, however, the first reflection returning from the end of the stub adds to the attenuated incident wave while it is still rising. The sum of the attenuated incident wave and the first stub reflection provides a step-free signal, although its rise time will be longer than that of the original signal. Satisfactory signal transitions can be assured by restricting stub lengths according to the recommendations for unterminated lines *(Figure 4-10)*. The same considerations apply when the termination resistance is not connected at the end of the line; a section of line continuing beyond the termination resistance should be treated as an unterminated line and its length restricted accordingly.

Series Termination

Series termination requires a resistor between the driver and transmission line, *Figure 4-7*. The receiving end of the line has no termination resistance. The series resistor value should be selected so that when added to the driver source resistance, the total resistance equals the line impedance. The voltage divider action between the net series resistance and the line impedance causes an incident wave of half amplitude to start down the line. When the signal arrives at the unterminated end of the line, it doubles and is thus restored to a full amplitude. Any reflections returning to the source are absorbed without further reflection since the line and source impedance match. This feature, source absorption, makes series termination attractive for interconnection paths involving impedance discontinuities, such as occur in backplane wiring.

A disadvantage of series termination is that driven inputs must be near the end of the line to avoid receiving a 2-step signal. The initial signal at the driver end is half amplitude, rising to full amplitude only after the reflection returns from the open end of the line. In *Figure 4-7*, one load is shown connected at point D, aways from the line end. This input receives a full amplitude signal with a continuous edge if the distance l to the open end of the line is within recommended lengths for unterminated line *(Figure 4-10)*.

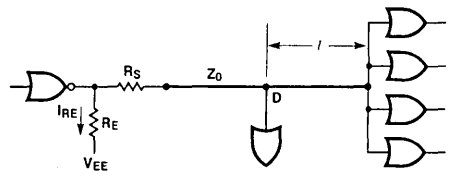

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FIGURE 4-7. Series Termination

The signal at the end has a slower rise time that the incident wave because of capacitive loading. The increase in rise time to the 50% point effectively increases the line propagation delay, since the 50% point of the signal swing is the input signal timing reference point. This added delay as a function of the product line impedance and load capacitance is discussed in Chapter 3.

Quiescent V_{OH} and V_{OL} levels are established by resistor R_E *(Figure 4-7)*, which also acts with V_{EE} to provide the negative-going drive into R_S and Z_0 when the driver output goes to the LOW state. To determine the appropriate R_E value, the driver output can be treated as a simple mechanical switch which opens to initiate the negative-going swing. At this instant, Z_O acts as a linear resistor returned to V_{OH}. Thus the components form a simple circuit of R_E, R_S and Z_0 in a series, connected between V_{EE} and V_{OH}. The initial current in this series circuit must be sufficient to introduce a 0.38V transient into the line, which then doubles at the load end to give 0.75V swing.

$$I_{RE} = \frac{V_{OH} - V_{EE}}{R_E + P_S + Z_0} \geq \frac{0.38}{Z_0} \qquad \textbf{(4-10)}$$

Any I_{OH} current flowing in the line before the switch opens helps to generate the negative swing. This current may be quite small, however, and should be ignored when calculating R_E.

Increasing the minimum signal swing into the line by 30% to 0.49V insures sufficient pull-down current to handle reflection currents caused by impedance discontinuities and load capacitance. The appropriate R_E value is determined from the following relationship.

$$\frac{V_{OH} - V_{EE}}{R_E + R_S + Z_0} \geq \frac{0.49}{Z_0} \qquad \textbf{(4-11)}$$

For the R_E range normally used, quiescent V_{OH} averages approximately 0.955V and $V_{EE} = -4.5V$. The value of R_S is equal to Z_0 minus R_0 (R_0 averages 7Ω). Inserting these values and rearranging Equation 4-11 gives the following.

$$R_E \leq 5.23\, Z_0 + 7\Omega \qquad \textbf{(4-12)}$$

Power dissipation in R_E is listed in *Figure 5-14*. The power dissipation in R_E is greater than in R_T of a parallel termination to −2V, but still less than the two resistors of the Thevenin equivalent parallel termination, see *Figure 5-10, 5-13* and *5-14*.

The number of driven inputs on a series terminated line is limited by the voltage drop across R_S in the quiescent HIGH state, caused by the finite input currents of the ECL loads. I_{IH} values are specified on data sheets for various types of

Series Termination (Continued)

inputs, with a worst-case value of 265 μA for simple gate inputs. The voltage drop subtracts from the HIGH-state noise margin as outlined in *Figure 4-8a*.

However, there is more HIGH-state noise margin initially, because there is less I_{OH} with the R_E load than with the standard 50Ω load to −2V. This makes V_{OH} more positive; the increase ranges from 43 mV for a 50Ω line to 82 mV for a 100Ω line. Using this V_{OH} increase as a limit on the voltage drop across R_S assures that the HIGH-state noise margin is as good as in the parallel terminated case. Dividing the V_{OH} increase by $R_S + R_0 (= Z_0)$ gives the allowed load input current (Ix in *Figure 4-8a*). This works out to 0.86 mA for a 50Ω line, 0.92 mA for a 75Ω line and 0.82 mA for a 100Ω line. Load input current greater than these values can be tolerated at some sacrifice in noise margin. If, for example, an additional 50 mV loss is feasible, the maximum values of current become 1.86 mA, 1.59 mA and 1.32 mA for 50Ω, 75Ω and 100Ω lines respectively.

An ECL output can drive more than one series terminated line, as suggested in *Figure 4-8b*, if the maximum rated output current of 50 mA is not exceeded. Also, driving two or more lines requires a lower R_E value. This makes the quiescent I_{OH} higher and consequently V_{OH} lower, due to the voltage drop across R_0. This voltage drop decreases the HIGH-state noise margin, which may become the limiting factor (rather than the maximum rated current), depending on the particular application.

The appropriate R_E value can be determined using Equation 4-13 for $V_{EE} = -4.5V$.

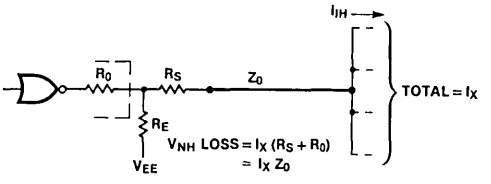
$$\frac{1}{R_E} \geq \frac{1}{6.23\,Z_1 - R_{S1}} + \frac{1}{6.23\,Z_2 - R_{S2}} + \frac{1}{6.23\,Z_3 - R_{S3}} \qquad \textbf{(4-13)}$$

Circuits with multiple outputs (such as the 100313) provide an alternate means of driving several lines simultaneous *(Figure 4-8c)*. Note, each output should be treated individually when assiging load distribution, line impedance, and R_E value.

Unterminated Lines

Lines can be used without series or parallel termination if the line delay is short compared to the signal rise time. Ringing occurs because the reflection coefficient at the open (receiving) end of the line is positive (nominally +1) while the reflection coefficient at the driving end is negative (approximately −0.8). These opposite polarity reflection coefficients cause any change in signal voltage to be reflected back and forth, with a polarity change each time the signal is reflected from the driver. Net voltage change on the line is thus a succession of increments with alternating polarity and decreasing magnitude. The algebraic sum of these increments if the observed ringing. The general relationships among rise time, line delay, overshoot and undershoot are discussed in Chapter 3, using simple waveforms for clarity.

Excessive overshoot on the positive-going edge of the signal drives input transistors into saturation. Although this does not damage an ECL input, it does cause excessive recovery times and makes propagation delays unpredictable. Undershoot (following the overshoot) must also be limited to prevent signal excursions into the threshold region of the loads. Such excursions could cause exaggerated transition times at the driven circuit outputs, and could also cause multiple triggering of sequential circuits. Signal swing, exclusive of ringing, is slightly greater on unterminated lines than on parallel terminated lines; I_{OH} is less and I_{OL} is greater with the R_E load, *(Figure 4-9a)* making V_{OH} higher and V_{OL} lower.



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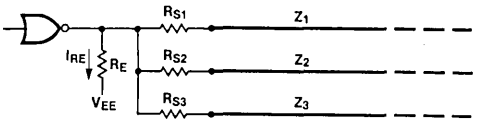
a. Noise Margin Loss Due to Load Input Current



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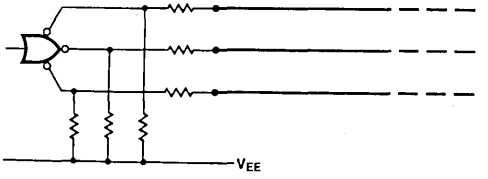
b. Driving Several Lines from one Output



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c. Using Multiple Output Element for Load Sharing

FIGURE 4-8. Loading Considerations for Series Termination

For worst case combinations of driver output and load input characteristics, a 35% overshoot limit insures that system speed is not compromised either by saturating an input on overshoot or extending into the threshold region on the following undershoot.

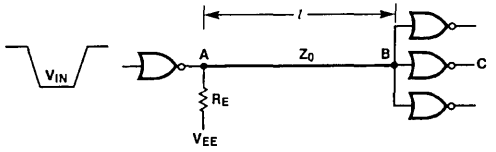
For distributed loading, ringing is satisfactorily controlled if the 2-way modified line delay does not exceed the 20% to 80% rise time of the driver output. This relationship can be expressed as follows, using the symbols from Chapter 3 and incorporating the effects of load capacitance on line delay.

$$t_r = 2T' = 2\ell\delta' = 2\ell\delta\sqrt{1 + \frac{C_L}{\ell C_0}}$$

Rearranging terms yields the quadratic equation:

$$\ell^2_{max} + \frac{C_L}{C_0}\ell_{max} + \frac{t_r^2}{4\delta^2} = 0 \qquad \textbf{(4-14)}$$

Unterminated Lines (Continued)



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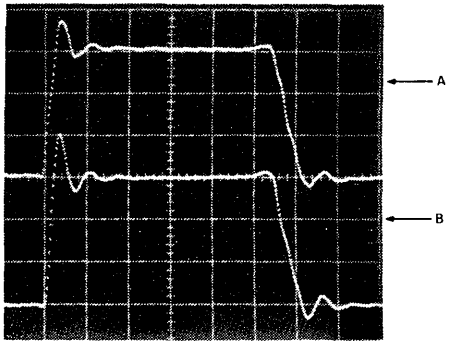
a. Unterminated Line



H = 10 ns/div
V = 0.3 V/div

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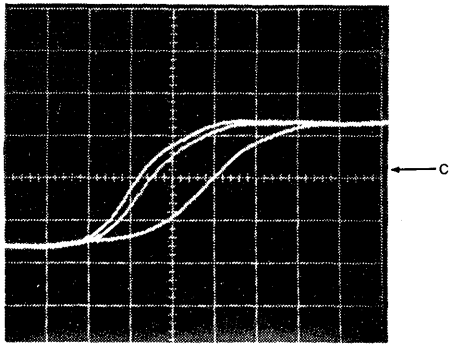
b. Line Voltages Showing Stair-step Trailing Edges



H = 1 ns/div
V = 0.3 V/div

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c. Load Gate Output Showing Net Propagation Increase for Increasing Values of R_E: 330Ω, 510Ω, 1 kΩ

FIGURE 4-9. Effect on R_E Value on Trailing-Edge Propagation

The shorter the rise time, the shorter the permissible line length. For F100K ECL, the minimum rise time from 20% to 80% is specified as 0.4 ns. Using this rise time and 3 pF per fan-out load, calculated maximum line lengths for G-10 epoxy microstrip are listed in *Figure 4-10*. The length (ℓ) in the table is the distance from the terminating resistor to the input of the device(s). For other combinations of rise time, impedance, fan-out or line characteristics (δ and C_0), maximum lengths are also calculated using Equation 4-14.

Z_0	Number of Fan-Out Loads			
	1	2	3	4
50	0.94*	0.68	0.52	0.41
62	0.87	0.59	0.44	0.34
75	0.79	0.52	0.37	0.29
90	0.72	0.45	0.32	0.25
100	0.68	0.41	0.29	0.22

*Length in inches.
Unit load = 3 pF, δ = 0.148 ns/inch

FIGURE 4-10. F100K Maximum Worst-Case Line Lengths for Unterminated Microstrip, Distributed Loading

Resistor R_E must provide the current for the negative-going signal at the driver output. Line input and output waveforms are noticeably affected if R_E is too large, as shown in *Figure 4-9b*. The negative-going edge of the signal falls in stair-step fashion, with three distinct steps visible at point A. The waveform at point B shows a step in the middle of the negative-going swing. The effect of different R_E values on the net propagation time through the line and the driven loads is evident in *Figure 4-9c* which shows the output signal of one driven gate in a multiple exposure photograph. The horizontal sweep (time axis) was held constant with respect to the input signal of the driver. The earliest of the three output signals occurs with an R_E value of 330Ω. Changing R_E to 510Ω increases the net propagation delay by 0.3 ns, the horizontal offset between the first and second signals. Changing R_E to 1 kΩ produces a much greater increase in net propagation delay, indicating that the negative-going signal at B contains several steps. In practice, a satisfactory negative-going signal results when the R_E value is chosen to give an initial negative-going step of 0.6V at the driving end of the line. This gives an upper limit on the value of R_E, as shown in Equation 4-15.

$$\text{initial step} = \Delta I \bullet Z_0 = \frac{(V_{OH} - V_{EE})\, Z_0}{R_E + Z_0} \geq 0.6$$

$$R_E = \leq 5\, Z_0 \text{ (at } V_{EE} = 4.5V) \qquad \textbf{(4-15)}$$

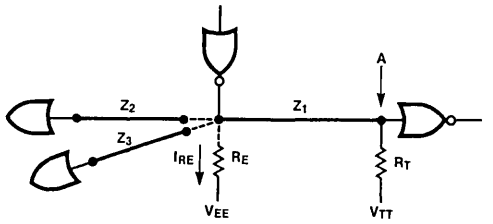
Unterminated Lines (Continued)

An ECL output can drive two or more unterminated lines, provided each line length and loading combination is within the recommended constraints. The appropriate R_E value is determined from Equation 4-15, using the parallel impedance of the two or more lines for Z_0.

An ECL output can simultaneously drive terminated and unterminated lines, although the negative-going edge of the signal shows two or more distinct steps when the stubs are long unless some extra pull-down current is provided. *Figure 4-11a* shows an ECL circuit driving a parallel terminated line, with provision for connecting two worst-case unterminated lines to the driver output. Waveforms at the termination resistor (point A) are shown in the multiple exposure photograph of *Figure 4-11b*. The upper trace shows a normal signal without stubs connected to the driver. The middle trace shows the effect of connecting one stub to the driver. The step in the negative-going edge indicates that the quiescent I_{OH} current through R_T is not sufficient to cause a full signal for both lines. The relationship between the quiescent I_{OH} current through R_T and the negative-going signal swing was discussed earlier in connection with parallel termination.

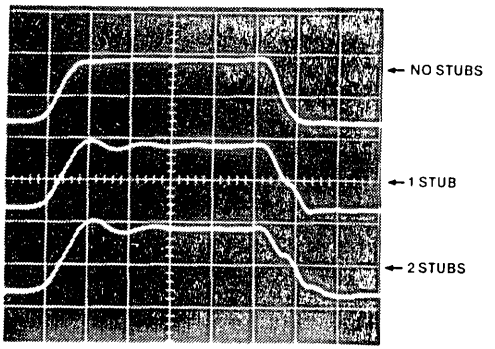
The bottom trace in *Figure 4-11* shows the effect of connecting two stubs to the driver output. The steps in trailing edge are smaller and more pronounced. The deteriorated trailing edge of either the middle or lower waveform increas-

a. Multiple Lines



TL/F/9901–19

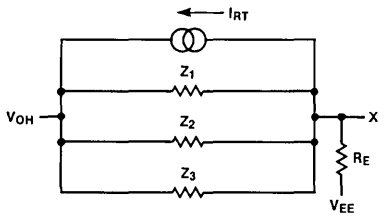
b. Waveforms at Termination Point A



H = 5 ns/div
V = 0.5 V/div

TL/F/9901–20

c. Equivalent Circuit for Determining Initial Negative Voltage Step at the Driver Output



TL/F/9901–21

FIGURE 4-11. Driving Terminated and Unterminated Lines in Parallel

Unterminated Lines (Continued)

es the switching time of the cirucit connected to point A. If this extra delay cannot be tolerated, additional pull-down current must be provided. One method uses a resistor to V_{EE} as suggested in *Figure 4-11a*. The initial negative-going step at point A should be about 0.7V to insure a good fall rate through the threshold region of the driven gate. The initial step at the driver output should also be 0.7V. If the driver output is treated as a switch that opens to initiate the negative-going signal, the equivalent circuit of *Figure 4-11c* can be used to determine the initial voltage step at the driver output (point X). The value of the current source I_{RT} is the quiescent I_{OH} current through R_T. Using Z' to denote the parallel impedance of the transmission lines and ΔV for the desired voltage step at X, the appropriate value of R_E can be determined from the following equation, using absolute values to avoid polarity confusion.

$$R_E = \left(|V_{EE}| - |V_{OH}| - \Delta V|\right) \bullet \left(\frac{Z'}{|\Delta V| - |I_{RT}|Z'}\right)$$

For a sample calculation, assume that R_T and the line impedances are each 100Ω, V_{OH} is −0.955V, ΔV is 0.750V, V_{EE} is −4.5V and V_{TT} is −2V. I_{RT} is thus 10.45 mA and the calculated value of R_E is 232Ω. In practice, this value is on the conservative side and can be increased to the next larger (10%) standard value with no appreciable sacrifice in propagation through the gate at point A.

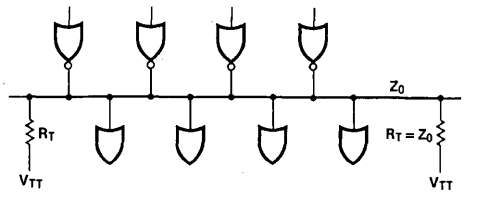
Again, the foregoing example is based on worst-case stub lengths (the longest permissible). With shorter stubs, the effects are less pronounced and a point is reached where extra pull-down current is not required because the reflection from the end of the stub arrives back at the driver while the original signal is still falling. Since the reflection is also negative going, it combines with and reinforces the falling signal at the driver, eliminating the steps. The net result is a smoothly falling signal but with increased fall time compared to the stubless condition.

The many combinations of line impedance and load make it practically impossible to define just with stub length begins to cause noticeable steps in the falling signal. A rough rule-of-thumb would be to limit the stub length to one-third of the values given in *Figure 4-10*.

Data Bussing

Data bussing involves connecting two or more outputs and one or more inputs to the same signal line, *(Figure 4-12)*. Any one of the several drivers can be enabled and can apply data to the line. Load inputs connected to the line thus receive data from the selected source. This method of steering data from place to place simplifies wiring and tends to minimize package count. Only one of the drivers can be enabled at a given time; all other driver outputs must be in the LOW or CUT-OFF state. Termination resistors matching the line impedance are connected to both ends of the line to prevent reflections. *For calculating the modified delay of the line (Chapter 3) the capacitance of a LOW (unselected) driver output should be taken as 3 pF.*

An output driving the line sees an impedance equal to half the line impedance. Similarly, the quiescent I_{OH} current is higher than with a single termination. For line impedance less than 100Ω, the I_{OH} current is greater than the data sheet test value, with a consequent reduction of HIGH-state noise margin. This loss can be eliminated if necessary by using multiple output gates (100313) and paralleling two



TL/F/9901–22

FIGURE 4-12. Data Bus or Party Line

outputs for each driver. In the quiescent LOW state, termination current is shared among all the output transistors on the line. This sharing makes V_{OL} more positive than if only one output were conducting all of the current. For example, a 100Ω line terminated at both ends represents a net 50Ω DC load, which is the same as the data sheet condition for V_{OL}. If one worst-case output were conducting all the current, the V_{OL} would be −1.705V. If another output with identical DC characteristics shares the load current equally, the V_{OL} level shifts upward by about 25 mV. Connecting two additional outputs for a total of four with the same characteristics shifts V_{OL} upward another 22 mV. Connecting four more identical outputs shifts V_{OL} upward another 20 mV. Thus the V_{OL} shift for eight outputs having identical worst-case V_{OL} characteristics is approximately 67 mV. In practice, the probability of having eight circuits with worst-case V_{OL} characteristics is quite low. The output with the highest V_{OL} tends to conduct most of the current. This limits the upward shift to much less than the theoretical worst-case value. In addition, the LOW-state noise margin is specified greater than the HIGH-state margin to allow for V_{OL} shift when outputs are paralleled. Exclusive use of devices with CUT-OFF DRIVERS on the bus (i.e., 100352) will eliminate low state current sharing and preserve the low state noise margins.

In some instances a single termination is satisfactory for a data bus, provided certain conditions are fulfilled. The single termination is connected in the middle of the line. This requires that for each half of the line, from the termination to the end, the line length and loading must comply with the same restrictions as unterminated lines to limit overshoot and undershoot to acceptable levels. The termination should be connected as near as possible to the electrical mid-point of the line, in terms of the modified line delay from the termination to either end. Another restriction is that the time between successive transitions, i.e., the nominal bit time, should not be less than 15 ns. This allows time for the major reflections to damp out and limits additive reflections to a minor level.

Wired-OR

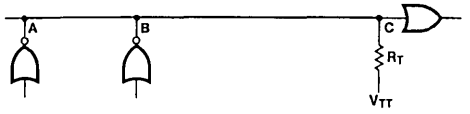
In general-purpose wired-OR logic connections, where two or more driver outputs are expected to be in the HIGH state simultaneously, it is important to minimize the line length between the participating driver outputs, and to place the termination as close as possible to the mid-point between the two most widely separated sources. This minimizes the negative-going disturbances which occur when one HIGH output turns off while other outputs remain HIGH. The driver output going off represents a sudden decrease in line current, which in turn generates a negative-going voltage on the line. A finite time is required for the other driver outputs (quiescently HIGH) to supply the extra current. The net re-

Wired-OR (Continued)

sult is a "V" shaped negative glitch whose amplitude and duration depend on three factors: current that the off-going output was conducting, the line impedance, and the line length between outputs. If the separation between outputs is kept within about ½ inch, the transient will not propagate through the driven load circuits.

If a wired-OR connection cannot be short, it may be necessary to design the logic so that the signal on the line is not sampled for some time after the normal propagation delay (output going negative) of the element being switched. Normal propagation delay is defined as the case where the element being switched is the only one on the line in the HIGH state, resulting in the line going LOW when the element switches. In this case, the propagation delay is measured from the 50% point on the input signal of the off-going element to the 50% point of the signal at the input farthest away from the output being switched. The extra wiring time required in the case of a severe negative glitch is, in a worst-case physical arrangement, twice the line delay between the off-going output and the nearest quiescently HIGH output, plus 2 ns.

An idea of how the extra waiting time varies with physical arrangement can be obtained by qualitatively comparing the signal paths in *Figure 4-13*. With the outputs at A and B quiescently HIGH, the duration of the transient observed at C is longer if B is the off-going output than if A is the off-going element. This is because the negative-going voltage generated at B must travel to A, whereupon the corrective signal is generated, which subsequently propagates back toward C. Thus the corrective signal lags behind the initial transient, as observed at C, by twice the line delay between A and B. On the other hand, if the output at A generates the negative-going transient, the corrective response starts when the transient reaches point B. Consequently, the transient duration observed at C is shorter by twice the line delay from A to B.



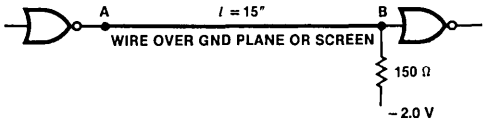
TL/F/9901–23

FIGURE 4-13. Relative to Wired-OR Propagation

Backplane Interconnections

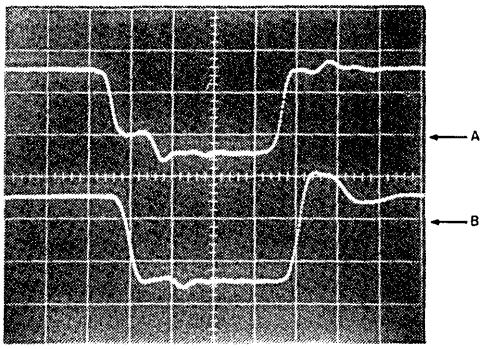
Several types of interconnections can be used to transmit a signal between logic boards. The factors to be considered when selecting a particular interconnection for a given application are cost, impedance discontinuities, predictability of propagation delay, noise environment, and bandwidth. Single-ended transmission over an ordinary wire is the most economical but has the least predictable impedance and propagation delay. At the opposite end of the scale, coaxial cable is the most costly but has the best electrical characteristics. Twisted pair and similar parallel wire interconnection cost and quality fall in between.

For single-wire transmission through the backplane, a ground plane or ground screen (Chapter 5) should be provided to establish a controlled impedance. A wire over a ground plane or screen has a typical impedance of 150Ω with variations on the order of ±33%, depending primarily on the distance from ground and the configuration of the ground. *Figure 4-14* illustrates the effects of impedance variations with a 15-inch wire parallel terminated with 150Ω to −2V. *Figure 4-14b* shows source and receiver waveforms when the wire is in contact with a continuous ground plane.



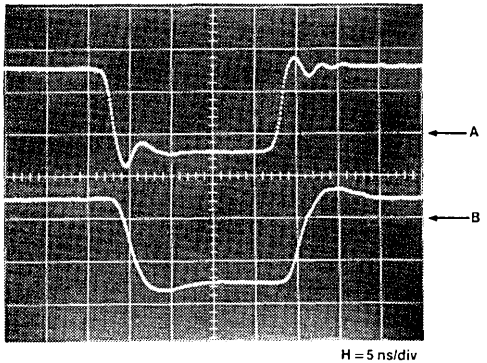
TL/F/9901–24

a. Wire over Ground Plane or Screen



TL/F/9901–25

b. Wire in Contact with Ground Plane



TL/F/9901–26

c. Wire Spaced ⅛" from Ground Screen

FIGURE 4-14. Parallel Terminated Backplane Wire

Backplane Interconnections (Continued)

The negative-going signal at the source shows an initial step of only 80% of a full signal swing. This occurs because the quiescent HIGH-state current I_{OH} (about 7 mA) multiplied by the impedance of the wire (approximately 90Ω) is less than the normal signal swing, and this condition allows the driver emitter follower to turn off. The negative-going signal at the receiving end is greater by 25% ($1 + \rho = 1.25$). The receiving end mismatch causes a negative-going reflection which returns to the source and establishes the V_{OL} level. The positive-going signal at the source shows a normal signal swing, with the receiving end exhibiting approximately 25% overshoot.

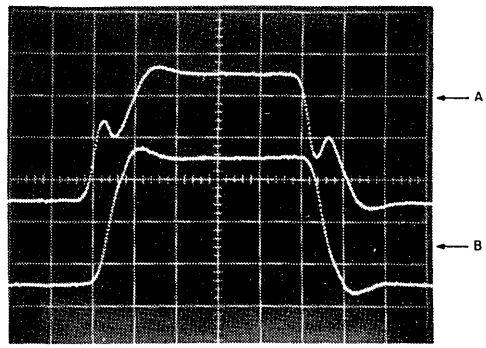
Figure 4-14c shows waveforms for a similar arrangement, but with the wire about ⅛ inch from a ground screen. The impedance of the wire is greater than 150Ω termination, but small variations in impedance along the wire cause intermediate reflections which tend to lengthen the rise and fall times of the signal. As a result, the received signal does not exhibit pronounced changes in slope as would be expected if a 200Ω constant impedance line were terminated with 150Ω.

Series source resistance can also be used with single wire interconnections to absorb reflection. *Figure 4-15a* shows a 16-inch wire with a ground screen driven through a source resistance of 100Ω. The waveforms *(Figure 4-15b)* show that although reflections are generated, they are largely absorbed by the series resistor, and the signal received at the load exhibits only slight changes and overshoot. Series termination techniques can also be used when the signal into the wire comes from the PC board transmission line. *Figure 4-16a* illustrates a 12-inch wire over a ground screen, with 12-inch microstrip lines at either end of the wire. The output is heavily loaded (fan-out of 8) and the combination of impedances produces a variety of reflections at the input to the first microstrip line, shown in the upper trace of *Figure 4-16b*. The lower trace shows the final output; a comparison between the two traces shows the effectiveness of damping in maintaining an acceptable signal at the output. *Figure 4-16c* shows the signals at the input to the driving gate and at the output of the load gate, with a net through-put time of 8.5 ns. The circuit in *Figure 4-16a* is a case of mismatched transmission lines, discussed in Chapter 3.

Signal propagation along a single wire tends to be fast because the dielectric medium is mostly air. However, impedance variations along a wire cause intermediate reflections which tend to increase rise and fall times, effectively increasing propagation delay. Effective propagation delays are in the range of 1.5 to 2.0 ns per foot of wire. Load capacitance at the receiving end also increases rise and fall time (Chapter 3), further increasing the effective propagation delay.

TL/F/9901–27

a. Wire over Ground Screen

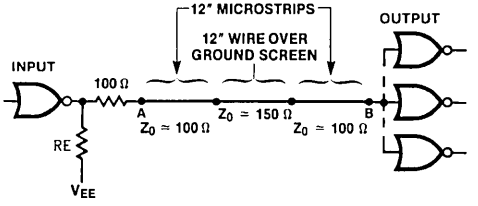


TL/F/9901–28

b. Series Terminated Waveform

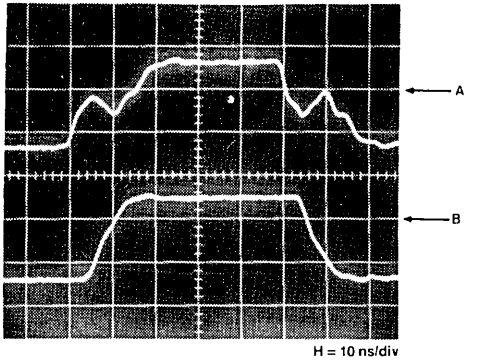
FIGURE 4-15. Series Terminated Backplane Wire

Backplane Interconnections (Continued)



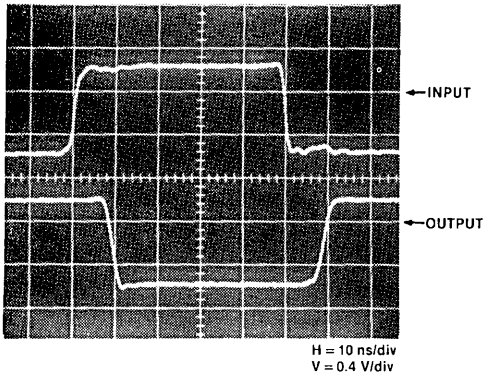
TL/F/9901–29

a. Backplane Wire Interconnecting PC Board Lines



TL/F/9901–30

b. Signals into the First Microstrip and at the Loads



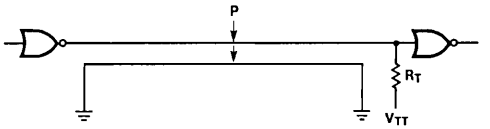
TL/F/9901–31

c. Input to Driving Gate and Output of Load Gate

FIGURE 4-16. Signal Path with Sequence of Microstrip, Wire, Microstrip

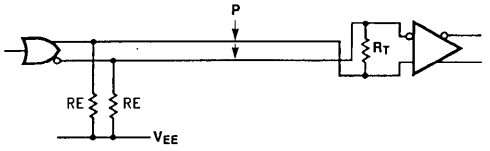
Better control of line impedance and faster propagation can be achieved with a twisted pair. A twisted pair of AWG 26 Teflon* insulated wires, two twists per inch, exhibits a propagation delay of 1.33 ns/ft and an impedance of 115Ω. Twisted pair lines are available in a variety of sizes, impedances and multiple-pair cables. *Figure 4-17a* illustrates single-ended driving and receiving. In addition to improved propagation velocity, the magnetic fields of the two conductors tend to cancel, minimizing noise coupled into adjacent wiring.

*Teflon is a registered trademark of E.I. du Pont de Nemours Conpany.



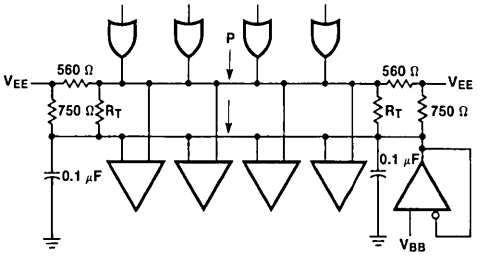
TL/F/9901–32

a. Single-ended Twisted Pair



TL/F/9901–33

b. Differential Transmission Reception



TL/F/9901–34

c. Backplane Data Bus

FIGURE 4-17. Twisted Pair Connections

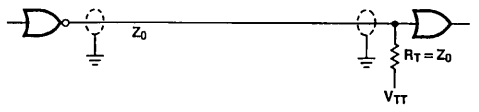
Differential line driving and receiving complementary gates as the driver and a 100314 line receiver is illustrated in *Figure 4-17b*. Differential operation provides high noise immunity, since common mode input voltages between −0.5V and −2.0V are rejected. The differential mode is recommended for communication between different parts of a system, because it effectively nullifies ground voltage differences. For long runs between cabinets or near high power transients, interconnections using shielded twisted pair are recommended.

Twisted pair lines can be used to implement party line type data transfer in the backplane, as indicated in *Figure 4-17c*. Only one driver should be enabled at a given time; the other outputs must be in the V_{OL} state. The V_{BB} reference voltage is available on pin 22 of the flatpak and pin 19 of the dual-in-line package for the 100314.

In the differential mode, a twisted pair can send high-frequency symmetrical signals, such as clock pulses, of 100 MHz over distances of 50 to 100 feet. For random data, however, bit rate capability is reduced by a factor of four or five due to line rise effects on time jitter.[3]

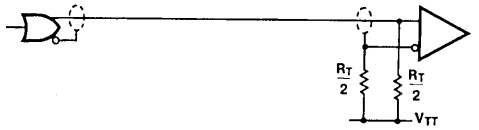
Backplane Interconnections (Continued)

Coaxial cable offers the highest frequency capability. In addition, the outer conductor acts as a shield against noise, while the uniformity of characteristics simplifies the task of matching time delays between different parts of the system. In the single-ended mode, *Figure 4-18a,* 50 MHz signals can be transferred over distances of 100 feet. For 100 MHz operation, lengths should be 50 feet or less. In the differential mode, *Figures 4-18b, c,* the line receiver can recover smaller signals, allowing 100 MHz signals to be transferred up to 100 feet. The dual cable arrangement of *Figure 4-18c* provides maximum noise immunity. The delay of coaxial cables depends on the type of dielectric material, with typical delays of 1.52 ns/ft for polyethylene and 1.36 ns/ft for cellular polyethylene.



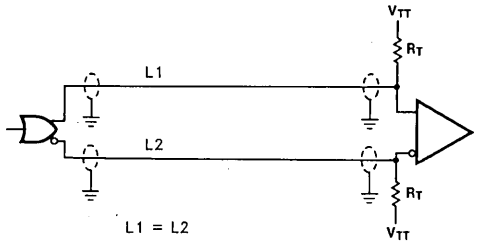
TL/F/9901–35

a. Single-Ended Coaxial Transmission



TL/F/9901–36

b. Differential Coaxial Transmission



TL/F/9901–37

c. Differential Transmission with Grounded Shields

FIGURE 4-18. Coaxial Cable Connections

References

1. Kaupp, H. R., "Characteristics of Microstrip Transmission Lines," *IEEE Transaction on Electronic Computers*, Vol. EC-16 (April, 1967).
2. Harper, C. A., *Handbook of Wiring, Cabling and Interconnections for Electronics.* New York: McGraw-Hill, 1972.
3. True, K. M., "Transmission Line Interface Elements," *The TTL Applications Handbook,* Chapter 14 (August 1973), pp. 14-1–14-14.

National Semiconductor

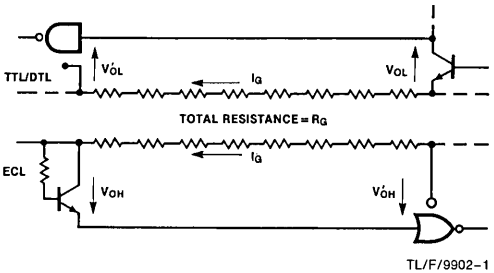
Chapter 5
Power Distribution and Thermal Considerations

Introduction

High-speed circuits generally consume more power than similar low-speed circuits. At the system level, this means that the power supply distribution system must handle the larger current flow; the larger power dissipation places a greater demand on the cooling system. The direct current (DC) voltage drop along ground busses affects noise margins for all types of ECL circuits. Voltage drops along V_{EE} busses have only a slight effect on F100K circuits, but they require consideration to obtain the performance available from the family.

Logic Circuit Ground, V_{CC}

The positive potential V_{CC} and V_{CCA} in ECL circuits is the reference voltage for output voltages and input thresholds and should therefore be the ground potential. When two circuits are connected in a single-ended mode, any difference in ground potentials decreases the noise margins, as discussed in *Chapter 1*. This effect for TTL/DTL circuits, as well as for ECL circuits, is illustrated in *Figure 5-1*. The following analysis assumes some average value of current flowing through the distributed resistance along the ground path between two circuits. For the indicated direction of I_G, the shift in ground potential *decreases* the LOW-state noise margin of the TTL/DTL circuits and the HIGH-state noise margin of the ECL circuits. If I_G is flowing in the opposite direction, it *increases* these noise margins, but *decreases* the noise margins when the drivers are in the opposite state. For tabulation of ground currents in ECL, the designs must include termination currents as well as I_{EE} operating currents. ECL logic boards which use microstrip or stripline techniques generally have large areas of ground metal. This causes the ground resistance to be quite low and thus minimizes noise margin loss between pairs of circuits on the same board.



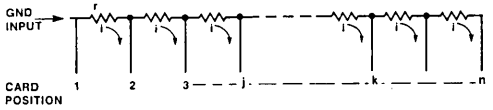
TL/F/9902–1

TTL/DTL	ECL
$V'_{OL} = V_{OL} = + I_G R_G$	$V'_{OH} = V_{OH} + I_G R_G$

$I_G R_G = (V'_{OL} - V_{OL})$ = Noise Margin Decrease = $I_G R_G = (V'_{OH} - V_{OH})$

FIGURE 5-1. Effect of Ground Resistance on Noise Margins

In practice, two communicating circuits might be located on widely separated PC cards with other PC cards in between. The net resistance then includes the incremental resistance of the ground distribution bus from card to card, while the ground current is successively increased by the contribution from each card. *Figure 5-2* illustrates a distribution bus for a row of cards with incremental resistances along the bus.



TL/F/9902–2

r = Incremental Bus Resistance between Positions
i = Average Ground Current per Card

FIGURE 5-2. Ground Shift Along a Row of PC Cards

The ground shift can be estimated by first determining an average value of current per card based on the number of packages, the mix of SSI and MSI, and the number and types of terminations. With n cards in the row, an average ground current (i) per card, and an incremental bus resistance (r) between card positions, the bus voltage drops between the various positions can be determined as follows:

between positions 1 and 2: $v_{1-2} = (n-1)\,ir$

between positions 1 and 3: $v_{1-3} = (n-1)\,ir + (n-2)\,ir$

between positions 1 and 4: $v_{1-4} = (n-1)\,ir + (n-2)\,ir + (n-3)\,ir$

between 1 and n:

$$v_{1-n} = ir\,\{(n-1) + (n-2) + (n-3) + \ldots + [n-(n-1)]\}$$
$$= ir\,[1 + 2 + 3 + \ldots + (n-1)]$$
$$v_{1-n} = ir \sum_{1}^{n-1} n$$

For a row of 15 cards, for example, the total ground shift between positions 1 and 15 is expressed as in Equation 5-1.

$$v_{1-15} = ir \sum_{1}^{14} n = ir\,(1 + 2 + 3 + \ldots + 13 + 14) \quad (5\text{-}1)$$
$$= 105\ ir$$

Logic Circuit Ground, V_{CC} (Continued)

The ground shift between any two card positions j and k can be determined as follows for the general case.

$$v_{j-k} = (n - j)\,ir + [n - (j + 1)]\,ir + [n - (j + 2)]\,ir + \ldots + \{n - [j + (k\text{-}j\text{-}1)]\}\,ir$$

$$= (k - j)\,nir - ir\{j + (j + 1) + (j + 2) + \ldots + [j + (k\text{-}j\text{-}1)]\} \quad (5\text{-}2)$$

$$v_{j-k} = (k - j)\,nir - ir\sum_{j}^{k-1} n = ir\left[(k - j)\,n - \sum_{j}^{k-1} n\right]$$

In a row of 15 cards, the ground shift between positions four and nine, for example, is determined as follows.

$$v_{j-k} = ir\,[(9 - 4)\,15 - (4 + 5 + 6 + 7 + 8)] \quad (5\text{-}3)$$
$$= ir\,(75 - 30) = 45\,ir$$

The ground shift between the same number of positions further down the row is less because of the decreasing current along the row. Consider the ground shift between card positions 10 and 15.

$$v_{10-15} = ir\,[(15 - 10)15 - (10 + 11 + 12 + 13 + 14)] \quad (5\text{-}4)$$
$$= ir\,(75 - 60) = 15\,ir$$

These examples illustrate several principles the designer should consider regarding the ground distribution bus and assignment of card positions. The bus resistance should be kept as low as possible by making the cross-sectional areas as large as practical. Logic cards which represent the heaviest current drain should be located nearest the end where ground comes into the row of cards. Cards with single-ended logic wiring between them should be assigned to positions as close together as possible. Conversely, if the ground shift between two card positions represents an unacceptable loss of noise margin, then the differential transmission and reception method i.e., twisted pair, should be used for logic wiring between them, thereby eliminating ground shift as a noise margin factor.

Conductor Resistances

Conductors with large cross-sectional areas are required to maintain low voltage drops along power busses. For convenience, *Figure 5-3* lists the resistance per foot and the cross-sectional area for more common sizes of annealed copper wire. Other characteristics and a complete list of sizes can be found in standard wire tables. A useful rule-of-thumb regarding resistances and, hence, areas is: as gauge numbers increase, resistance doubles with every third gauge number; e.g., the resistance per foot of #10 wire is 1 mΩ, for #13 wire it is 2 mΩ. Similarly, the resistance per foot of #0 wire is 0.078 mΩ, which is half that of #2 wire.

For calculations involving conductors having rectangular cross sections, it is often convenient to work with sheet resistance, particularly for power distribution on PC cards. Copper resistivity is usually given in ohm-centimeters, indicating the resistance between opposing faces of a 1 cm cube. The sheet resistance of a conductor is obtained by dividing the resistivity by the conductor thickness. These relationships follow.

AWG B & S Gauge	Resistance mΩ Per Foot	Cross-Sectional Area Square Inches
#2	0.156	5.213×10^{-2}
#6	0.395	2.062×10^{-2}
#10	0.999	8.155×10^{-3}
#12	1.588	5.129×10^{-3}
#18	6.385	1.276×10^{-3}
#22	16.14	5.046×10^{-4}
#26	40.81	1.996×10^{-4}
#30	103.2	7.894×10^{-5}

FIGURE 5-3. Resistance and Cross-Sectional Area of Several Sizes of Annealed Copper Wire

Copper resistivity = $\rho = 1.724 \times 10^{-6}\ \Omega$cm @ 20°C

Resistance of a conductor = $\rho\frac{l}{A} = \rho\frac{l}{tw}$

where: l = length t = thickness w = width

Sheet resistance $\rho_S = \frac{\rho}{t}\ \Omega$ per $\frac{l}{w}$

The length/width ratio (l/w) is dimensionless; therefore, the resistance of a length of conductor of uniform thickness can be calculated by first determining the number of "squares," then multiplying by the sheet resistance. For example, a conductor one-eighth inch wide and three inches long has 24 squares; its resistance is 24 times the sheet resistance. Since many thickness dimensions are given in inches, it is convenient to express the resistivity in ohm-inch, as follows.

$\rho(\Omega\text{in.}) = \rho(\Omega\text{cm}) \div 2.54 = 6.788 \times 10^{-7}\ \Omega$in.

The use of sheet resistance and the "squares" concept is illustrated by calculating the resistance of the conductor shown in *Figure 5-4*. Assume the conductor is a 1 oz. copper cladding with a 0.0012 inch minimum thickness on a PC card.

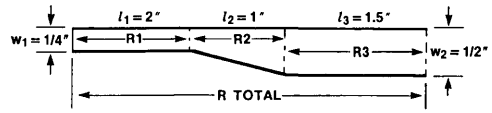


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FIGURE 5-4. Conductor of Uniform Thickness but Non-Uniform Cross Section

Sheet resistance = $\rho_S = \frac{\rho}{t}$

$= 5.657 \times 10^{-4}\ \Omega$ per square

The number of squares S for the rectangular sections are as follows.

$$S1 = \frac{l_1}{w_1} = 8 \qquad S_3 = \frac{l_3}{w_2} = 3$$

The middle average segment of the conductor has a trapezoidal shape. The average of w_1 and w_2 can be used as the effective width, within 1% accuracy, if the w_2/w_1 ratio is 1.5 or less. Otherwise, a more exact result is obtained as follows.

$$S_2 = \frac{l_2}{w_2 - w_1}\ln\left(\frac{w_2}{w_1}\right) = 4\ln 2 = 2.77\ \text{squares} \quad (5\text{-}5)$$

$$\text{Total } R = R_1 + R_2 + R_3 = \rho_s(S_1 + S_2 + S_3)$$
$$= 7.51\ \text{m}\Omega$$

Conductor Resistances (Continued)

As another example, assume that a 1 oz. trace must carry a 200 mA current six inches with a voltage drop less than 10 mV.

$$R_{max} = \frac{V_{max}}{I} = \frac{0.01}{0.2} = 0.05\Omega$$

$$0.05 = \rho_s \frac{l}{w} \qquad (5\text{-}6)$$

$$\frac{w}{l} = 20\,\rho_s$$

$$w = 120\,\rho_s = (120)\,5.657 \times 10^{-4} = 67.9 \times 10^{-3}$$

$\therefore$ minimum trace width, w = 68 mils

At a higher current level, consider the voltage drop in a conductor 20 mils thick, 1.25 inches wide and 3 feet long carrying a 50A current.

$$\rho_s = \frac{6.788 \times 10^{-7}}{2 \times 10^{-2}} = 3.364 \times 10^{-5}\ \Omega \text{ per square}$$

$$V = IR - (50)\,(3.364 \times 10^{-5})\frac{36}{1.25} \qquad (5\text{-}7)$$

$$= 0.0484 = 48.4 \text{ mV}$$

Sheet resistances for various copper thicknesses are listed in *Figure 5-5*. Standard thicknesses and tolerances for copper cladding are tabulated in *Figure 5-6* and resistance per foot as a function of width is shown in *Figure 5-7*.

Weight or Thickness	Sheet Resistance Ω per Square	Thickness	Sheet Resistance Ω per Square
2 oz.	2.715×10^{-4}	0.02 in.	3.364×10^{-5}
3 oz.	1.886×10^{-4}	0.05 in.	1.358×10^{-5}
5 oz.	1.077×10^{-4}	1/16 in.	1.086×10^{-5}
0.01 in.	6.788×10^{-5}	1/4 in.	2.715×10^{-6}

FIGURE 5-5. Sheet Resistance for Various Thicknesses of Copper

Nominal Thickness		Nominal Weight	Tolerances By	
in.	mm	oz/ft²	Weight, %	in.
0.0007	0.0178	½	+10	+0.0002
0.0014	0.0355	1	+10	+0.0004 −0.0002
0.0028	0.0715	2	+10	+0.0007 −0.0003
0.0042	0.1065	3	+10	+0.0006
0.0056	0.1432	4	+10	+0.0006
0.0070	0.1780	5	+10	+0.0007
0.0084	0.2130	6	+10	+0.0008
0.0098	0.2460	7	+10	+0.001
0.014	0.3530	10	+10	+0.0014
0.0196	0.4920	14	+10	+0.002

FIGURE 5-6. Thickness and Tolerances for Copper Cladding

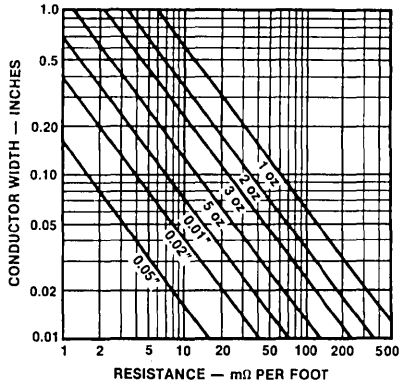

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FIGURE 5-7. Conductor Resistance vs Thickness and Width

Temperature Coefficient

The resistances in *Figures 5-3, 5-5,* and *5-7*, as well as those used in the sample calculations, are 20°C values. Since copper resistivity has a temperature coefficient of approximately 0.4%/°C, the resistance at a temperature (T) can be determined as follows.

$$R_T = R_{20°C}\,[1 + 0.004\,(T + 20°C)]$$

At 55°C: (5-8)

$$R = R_{20°C}\,[1 + 0.004\,(55°C - 20°C)] = 1.14\,R_{20°C}$$

When specifying power bus dimensions for PC cards containing many IC packages, designers should bear in mind that excessive current densities can cause the copper temperature to rise appreciably. *Figure 5-8* illustrates the ohmic heating effect of various current densities.[1]

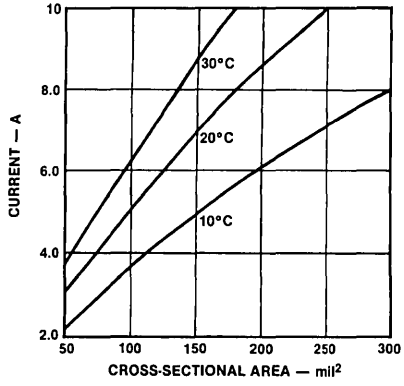

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FIGURE 5-8. Temperature Rise with Current Density in PC Board Traces

Distribution Impedance

Power busses should have low AC impedance, as well as low DC resistance, to prevent propagation of extraneous disturbances along the distribution system. As far as current or voltage changes are concerned, power and ground busses appear as transmission lines; thus their impedances can be affected by shape, spacing and dielectric. The effect of geometry on impedance is illustrated in the two arrangements of *Figure 5-9*. The same cross-sectional area of copper is used, but the two round wires have an impedance of about 75Ω while the flat conductors have an impedance determined as follows.

$$Z_0 = \frac{377\,d}{\sqrt{\epsilon}\,h} \text{ for } \frac{d}{h} < 0.1$$

With a Mylar®* or Teflon®* dielectric (ϵ = 2.3) two mils thick, impedance of the flat conductor pair is only 0.5Ω. Power line impedance can be reduced by periodically connecting RF-type capacitors across the line.

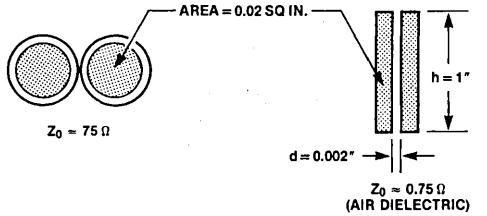

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FIGURE 5-9. Effect of Geometry on Power Bus Impedance

*Mylar and Teflon are registered trademarks of E.I. du Pont de Nemours Company.

Ground on PC Cards

It is essential to assign one layer of copper cladding almost exclusively to ground. This provides low-impedance, non-interfering return paths for the current changes which travel along signal traces when the IC outputs change state. These currents flow from the V_{CCA} pins of the IC packages, through the output transistors, then into the loads and the stray capacitances. These stray capacitances exist from an output to V_{EE}, output to ground, and to other signal lines. Thus, displacement currents through stray capacitances flow in many paths, but must ultimately return through ground to the output transistor where they originated. To reduce the length and impedance of the return path, the ground metal should cover as large an area as possible and one decoupling capacitor should be provided for every one to two IC packages. Additional capacitors may be needed for multiple output devices. These capacitors should be ceramic, monolithic or other RF types in the 0.01 μF to 0.1 μF range.

The load current returning to an IC package through ground metal is predictable, both in magnitude and in the return path. Since the magnetic and capacitive coupling between a signal trace and the underlying ground provides the transmission line characteristic, it follows that the load current flowing through the signal trace is accompanied by a ground return current equal in magnitude but opposite in direction. For example, in a 50Ω terminator I_{OL} is 5.9 mA, I_{OH} is 20.9 mA. Then signal change will cause about 15 mA current change and, as this current change propagates along the signal trace, a current of −15 mA advances along the ground directly underneath the signal trace. Therefore, if there is an interruption in the ground, the return current is forced to go around it. The 15 mA current change can be reduced by terminating the complementary output of the signal. Then a signal change will direct the current from true output to the complement output reducing the Δ currents in the ground plane. When it is necessary to interrupt the ground plane, the interruptions should be kept as short as possible; every effort should be made to locate them away from overlying signal lines. When the ground plane is interrupted for short signal lines between packages, these lines should be at right angles to signal lines on the other side to minimize coupling. V_{EE} and V_{TT} distribution lines can also act as the return side of transmission lines, as long as decoupling capacitors to ground are placed in the immediate areas where the signal return current must continue through ground.

Several connections along the edge of a PC card should be assigned to ground to accommodate backplane signal ground. These should be spaced at one-half to one inch intervals to minimize the average path length for signal return currents and to simulate a distributed connection to the backplane signal ground.

Not enough emphasis can be placed on the requirement for a good ground. All input signals are referenced to internal V_{BB} and the V_{BB} is referenced to V_{CC} (ground). Any variation from one side of the board to the other affects the noise margins. To help eliminate some of the variations a separate V_{CCA} is provided on F100K ECL circuits to power the output drivers and leave the V_{CC} going to internal circuitry unaffected.

Backplane Construction

In order to take complete advantage of the speeds inherent in F100K ECL it is desirable to construct the backplane as a multilayer printed circuit board. Generally, two internal layers are devoted to ground and V_{EE} and the signals occupy the outside layers. Where power densities are very high, it may be necessary to supplement the power layers with external busses (see Backplane Interconnections, *Chapter 4*).

If it is necessary to use wires to augment the interconnection provided by the traces, less critical signals should use the wires. The wires will exhibit an impedance which can be calculated with the wire-over-ground formula

$$Z_0 = \frac{138}{\sqrt{\epsilon}} \operatorname{Log}_{10} \frac{4h}{d} \qquad (5\text{-}9)$$

where d is diameter, h is distance to ground, and ϵ is dielectric constant.

Bear in mind that if the ground plane is buried inside the board, then both h and ϵ are made up of multiple components.

Termination Supply, V_{TT}

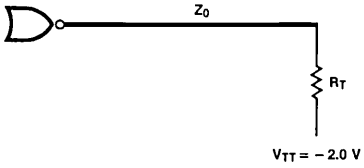
A separate return voltage for the termination resistors offers a way to minimize power dissipation in systems extensively using parallel termination techniques. A −2V V_{TT} value represents an optimum speed/power trade-off, allowing sufficient termination current to discharge load capacitances while minimizing the average power consumption. *Figure 5-10* shows the average values of current, IC power dissipation and resistor power dissipation for various values of the termination resistor R_T returned to −2V. Average values are determined by calculating the output HIGH and output LOW values, then taking the average. These 50% duty cy-

Termination Supply, V_{TT} (Continued)

cle values are useful in determining the current drain on the −2V supply and the contribution to dissipation on the logic boards. Peak values of termination current are approximately 60% greater than the average values listed.

DC regulation of the −2V supply is not critical; a variation of ±5% causes a change in output levels of ±12 mV for 50Ω terminations or ±7 mV for 100Ω terminations.

The high frequency characteristics of the V_{TT} distribution are extremely important. Ideally, a solid voltage plane should be devoted to V_{TT}. If this is not feasible, the V_{TT} distribution should form a grid using orthogonal traces. In any case, decoupling capacitors to ground should be used to reduce the high frequency impedance.



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R_T Ω	I_{avg} mA	$P_{D\ (avg)}$ mW	
		IC Output	Resistor
50	13.6	17.9	9.3
62	11.0	14.6	7.9
75	9.1	12.2	6.8
90	7.6	10.3	5.8
100	6.8	9.2	5.3
150	4.5	6.2	3.7

FIGURE 5-10. Average Current and Power Dissipation for Parallel Termination to −2V

If the terminators used are in Single In-line Packages (SIP) or Dual-In-line Packages (DIP) as opposed to discrete resistors, particular attention must be given to decoupling in order to maintain a solid V_{TT} voltage inside the package. This is necessary to avoid crosstalk due to mutual inductance to V_{TT}. SIPs have been developed which have multiple V_{TT} connections and on-board decoupling capacitors.

V_{EE} Supply

The value of V_{EE} is not critical for F100K since all circuits in the family operate over the range of −4.2V to −5.7V. Decoupling capacitors to ground should be used on each card, as previously discussed in connection with the ground on PC cards. In addition, each card should used 1 μF to 10 μF decoupling capacitors near the points where V_{EE} enters the card.

The current drain for the V_{EE} supply for each circuit type can be determined from the data sheet specifications. For V_{EE} values other than −4.5V, the current drain varies as shown in *Figure 5-11*. This graph is made from data from the 100301.

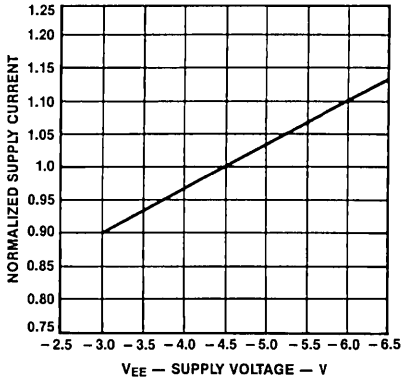

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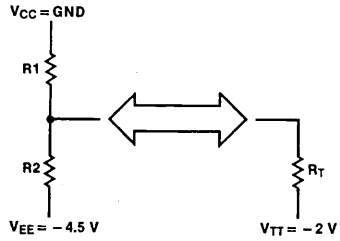
FIGURE 5-11. Supply Current vs Supply Voltage for 100301

Series dividers used to obtain Thevenin equivalent parallel terminations increase the current load on the V_{EE} supply, as do the pull-down resistors to V_{EE} used with series termination. Average V_{EE} current and resistor dissipation for Thevenin equivalent terminations are listed in *Figure 5-13* for several representative values of equivalent resistance. The average values apply for 50% duty cycle. Peak current values are approximately 11% greater. Dissipation in the IC output transistor is the same as in *Figure 5-10*. Average dissipation and I_{EE} current for several values of pull-down resistance to V_{EE} are listed in *Figure 5-14*. The R_E values are appropriate for series termination of transmission lines with impedances listed in the Z_0 column, determined from Equation 4-12. Peak current values are approximately 12% greater than average values.

Figures 5-10, 13 and *14* show that the Thevenin equivalent parallel termination method leads to ten times as much dissipation in the resistors as in the single resistor returned to −2V. Similarly, the dissipation in R_E for series termination is three times the dissipation in the parallel termination resistor to −2V.

V_{EE} Supply (Continued)



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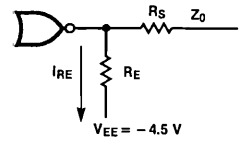
R_T Ω	$R_{1\Omega}$ = 1.80 R_T	$R_{2\Omega}$ = 2.25 R_T	$I_{EE\ (avg)}$ mA	$P_{D\ (avg)}$ mW Resistors
50	90.9	113	28.2	109
62	113	140	22.7	87.9
75	133	169	18.8	72.7
82	147	182	17.2	66.5
90	162	205	15.7	60.5
100	182	226	14.1	54.5
120	215	274	11.7	45.4
150	274	340	9.4	36.3

FIGURE 5-13. Series Divider for Thevenin Equivalent Terminations



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Z_0 Ω	R_E Ω	$I_{EE\ (avg)}$ mA	$P_{D\ (avg)}$ mW	
			IC Output	R_E
50	267	9.8	12.9	25.8
62	332	7.9	10.4	20.6
75	402	6.5	8.6	16.8
90	475	5.4	7.1	13.9
100	536	4.9	6.5	12.7
120	634	4.1	5.4	10.6
150	787	3.2	4.2	8.1

FIGURE 5-14. Average Current and Power Dissipation Using Pull-Down Resistor to V_{EE}

Reference

1. Harper, C.A., Editor, *Handbook of Wiring, Cabling and Interconnecting for Electronics*, McGraw-Hill, 1972.

National Semiconductor

Chapter 6
Testing Techniques

Introduction

The purpose of this chapter is to assist personnel involved with incoming inspection and qualification testing, by discussing the various methods and techniques used in testing ECL devices.

Testing includes verifying functionality, checking DC parametric limits and measuring AC performance. These tasks are particularly difficult for ECL devices in light of the broad range of products: RAMs, PROMs, gate arrays, and logic circuits. Correlation between supplier and user is extremely important. Recognizing the differences between high-volume instantaneous testing, as performed by the supplier, and the user's concern for long term performance in a given operating environment, National guarantees the data sheet limits as specified, although testing may be performed by alternate methods.

Tester Selection

Although many makes and types of automatic test systems are available and in use today, not all are capable of testing ECL RAMs, PROMs, logic and gate arrays.

Logic and gate array testers require DC Accuracy, subnanosecond AC test capability, and the ability to change software for each device. Software capability and the number of test pins available are major considerations in choosing a gate array tester. Functional, DC and threshold tests are successfully performed on automatic test equipment, but subnanosecond propagation delays are difficult to measure accurately.

The use of dedicated testers to perform high-volume memory testing is very common. Testers containing hardware addressing capability are usually the most efficient. Although basic DC testing is similar for any device type, RAM and PROM functional testing usually require special addressing capabilities to test for pattern sensitivity. The pattern generators and output comparators must have minimum skew to obtain maximum tester accuracy. Functional and AC tests are performed simultaneously; then, DC and threshold tests are performed.

The following considerations must be taken into account when selecting a tester.

Noise

Since the voltage swing on ECL input and output levels is only about 800 mV, it is very important that the power supplies and voltage drivers be extremely clean and free of spikes, hum, or any other type of noise.

DC Resolution

The threshold measurements ($V_{IH\ (Min)}$, $V_{IL\ (Max)}$) require that input voltage be extremely accurate and repeatable, i.e., if the $V_{IL\ (Max)}$ is specified as -1.475V, a voltage source of -1.475 ± 5 mV is not adequate to accurately test the part. Ideally, the driver and the output comparators should have an accuracy of ± 1 mV.

Current Capability

Since ECL is noted for high current requirements, power supplies for V_{EE} should be capable of supplying current with a 25% reserve over the highest powered parts. This reserve should be included because power supplies tend to get noisy when approaching the current clamp. Some ECL LSI parts dissipate over 4.5W; therefore, with a V_{EE} of -4.5V, the power supply must provide well over 1A.

Edge Rates

When testing edge-triggered sequential logic parts such as flip-flops and shift registers, it is important that the rise and fall times of the clock pulses be fast, clean and free from overshoot. If the clock edges are not adequate, the deficiency can be overcome using a Schmitt trigger as shown in *Figure 6-1.*

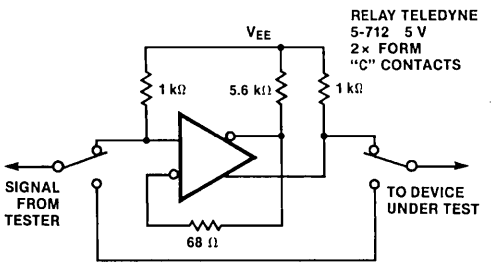

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FIGURE 6-1. Typical Schmitt Trigger Circuit

The 68Ω resistor provides hysteresis by positive feedback, thus improving the edge rates. When energized, the relay provides a path to bypass the Schmitt trigger, so the input currents of the device under test can be measured.

Functional Testing

The functional operation and truth table for all device types are checked using automatic test equipment. For memory devices, pattern sensitivity and AC characteristics are also tested automatically. Functional testing is usually performed before DC testing. Logic parts are functionally tested in all modes of operation. The inputs are driven using typical V_{IH} and V_{IL} values. The outputs are compared against relaxed V_{OH} and V_{OL} limits. The V_{IH}, V_{IL}, V_{OH} and V_{OL} limits are tested during DC testing.

DC Testing

An automatic tester is used to test all DC parameters listed on the individual data sheet for each input and output. The device may have to be preconditioned to obtain the correct output logic state. The cable length should be kept to a minimum to insure signal integrity.

Threshold Measurements

Threshold measurement on an automatic tester is probably the most difficult DC test and the test most prone to oscillation. When testing, take one input at a time to threshold; all other inputs remain at full V_{IH} or V_{IL} levels. For example, to test a flip-flop, make sure the output is LOW before test, take the data pin to HIGH threshold, and apply the clock pulse. Verify that the HIGH has been transferred to the output. Next, apply LOW threshold to the data input and clock it through; use hard levels on the clock (full V_{IH} and V_{IL}). Check that the output pin goes LOW.

Bench Testing

Occasionally, it is necessary to obtain data not easily available from an automatic tester. This is accomplished by testing devices in a universal test board. The typical test circuit board is double-clad copper. All input/output pins go to single-pole, triple-throw switches so that V_{IH}, V_{IL} or a 50Ω terminating resistor can be connected. Leadless 0.05 μF capacitors decouple all pins to V_{CC} (+2V) at the socket pins. Access to the device under test is made via banana sockets to the X-Y plotter.

V_{IH}/V_{OUT} Plot—The input ramp supply is 0V to −2V varied by a multi-turn potentiometer. The input voltage (V_{IN}) versus output voltage (V_{OUT}) is plotted on an X-Y recorder using the test setup shown in *Figure 6-2*.

V_{OUT}/I_{OUT} Plot—The output voltage (V_{OUT}) versus output current (I_{OUT}) can be plotted using the test setup shown in *Figure 6-3*.

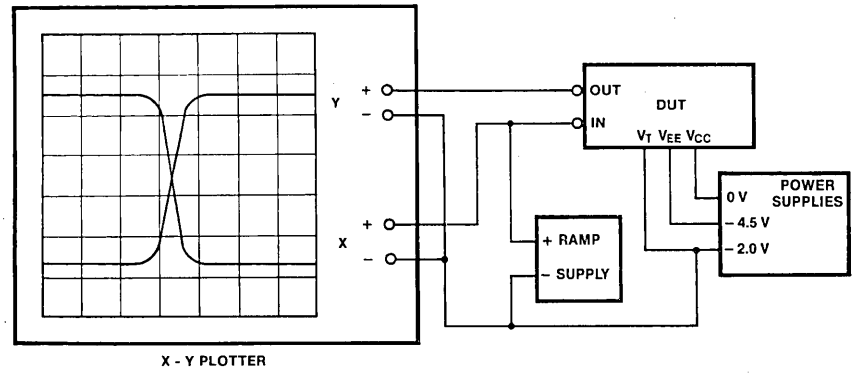

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FIGURE 6-2. V_{IN}/V_{OUT} Transfer Characteristics

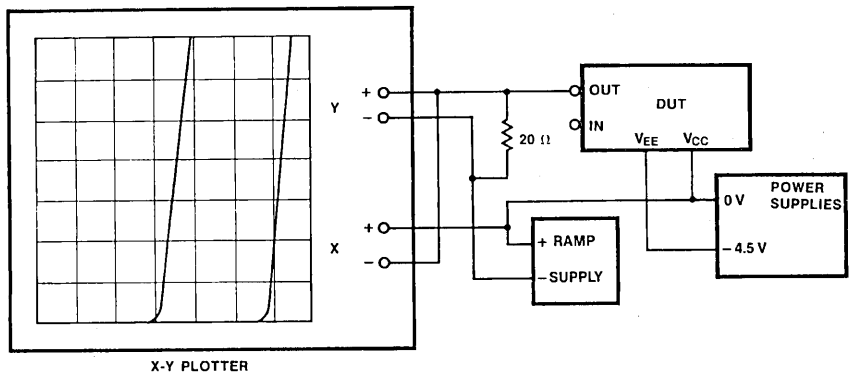

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FIGURE 6-3. V_{OUT}/I_{OUT} Characteristics

AC Testing

Because few automatic measurements systems have sufficient accuracy to perform subnanosecond testing, AC testing of ECL is one of the most difficult tests to accomplish. To obtain subnanosecond accuracy usually requires special test fixtures and equipment. The physical location of the test fixture, the input driver and the output comparator is very important.

Depending upon the accuracy and repeatability of the automatic tester, a bench setup may be required for correlation. Comparing an air line with known propagation delay to the test setup is recommended.

AC Test Fixtures

Test fixture design plays a pivotal role in insuring that undistorted waveforms are applied to the Device Under Test (D.U.T.) and that the device output can be monitored correctly.

Board Construction and Layout

ECL AC bench test fixtures are built on a double-clad printed circuit board or on a multilayer printed circuit board with semi-rigid coax. The power planes are shorted at the device and brought out to banana sockets with the decoupling capacitors at the device. Transmission lines of 50Ω are maintained from soldered-on BNC or SMA connectors to the D.U.T. Sense lines from the D.U.T. output and input pins to the connectors must be of electrically equal length. For input pins, care must be taken to insure that the force and sense lines are brought directly to the point that makes contact with the D.U.T. For output pins, only the output sense lines are used to monitor the signals. The force lines are disconnected at the device to minimize signal distortion. Special care must be taken to minimize crosstalk and stray capacitance in the area of the D.U.T. For correlation, flatpaks are not tested in sockets but are clamped to the traces of a multilayer PC board. Dual in-line devices are plugged into individual pin sockets instead of normal test sockets. Due to equipment limitations and for correlation, the amplitude, offset, rise and fall time are set up with no device in the test socket.

The bench test fixture to measure toggle frequency utilizes the principles described in the preceding paragraph except that the feedback path between the output and data input is as short as possible.

Output Termination

All outputs should be terminated with 50Ω ±1% resistors. This is especially important for complementary outputs.

When bench testing, the device is offset by +2V; V_{EE} is −2.5V; V_{CC}, V_{CCA} is +2V. Then the 50Ω input impedance of the sampling oscilloscope acts as the termination resistor to 0V. The input and output coaxial cable to the oscilloscope should be cut to exactly the same electrical length.

Decoupling

Not enough emphasis can be put on the importance of good decoupling on the D.U.T. because oscillations can give erroneous test results. A sampling scope should be used to make sure that oscillation is not occurring.

The value of capacitors used depends on the type of tester used and the frequency of test. Some testers use pulse test; in other words, for each individual test in a program, V_{EE} is powered up and down. On this type of tester, electrolytic-type (i.e., large value) capacitors cannot be used because of the time constant needed to charge the capacitor.

Always start with the minimum decoupling needed to achieve good results, perhaps merely a capacitor between V_{CC} and V_{EE}. Capacitors should be placed as close as possible to the D.U.T. to eliminate as much inductance as possible. Only low-inductance capacitors should be used; leadless monolithic ceramic capacitors are very effective.

There are no rigid decoupling rules, and each device type may have its own decoupling requirements. A typical decoupling technique that works well on most F100K devices is to place 0.01 μF to 0.1 μF monolithic ceramic capacitors in the following locations.

- If no offset is used:
  between V_{EE} (−4.5V) and V_{CC}, V_{CCA} (0V)
  between V_{TT} (−2V) and ground (0V)
- If +2V offset is used:
  between V_{CC}, V_{CCA} (+2V) and ground (0V)
  between V_{EE} (−2.5V) and ground (0V)
- In most cases, V_{CCA} and V_{CC} should be shorted as close to the D.U.T. as possible. However, if the V_{CCA} and V_{CC} pins are physically separated, individual decoupling capacitors may be necessary.
- For DC test only place a 0.001 μF capacitor:
  between an input pin and V_{EE}
  between an output pin and V_{CCA}

Decoupling problems will appear mainly at threshold test. If certain outputs fail, try the decoupling technique, described in the preceding paragraph, on those outputs and the associated inputs. With testers that use the power-hold method, such as the Sentry®, large electrolytics can be used in parallel with smaller (0.01 μF) disk capacitors for the high-frequency bypass.

ELECTROSTATIC DISCHARGE

Introduction

The study of ESD failures began in earnest back when system designers, faced with very expensive assembly and post-assembly rework, began investigating system failures in great detail. In the course of their study, they checked all the records to determine which devices has passed earlier testing, but had failed once in the system. The data clearly indicated that something in the handling process resulted in higher attrition rates among the devices. Reliability physicists examined the failed devices in minute detail, in some cases subjecting them to examination under high powered scanning electron microscopes.

The problem was found to be one of electrical overstress, and further investigation determined that the cause of the overstress was a phenomenon called electrostatic discharge (or ESD).

Explanation of How ESD Occurs

The concept of electrostatic discharge is easily understood. Electrostatic energy is static electricity, a stationary charge which can build up in either a nonconductive material or in an ungrounded conductive material. This charge can occur in one of two ways, either through polarization, which occurs when a conductive material is exposed to a magnetic field, or triboelectric effects, which occur when two surfaces contact and then separate, leaving one positively charged and one negatively charged. Friction between two materials increases triboelectric charge by increasing the surface area that comes in contact. A good example of this phenomenon would be the charge one accumulates walking across a nylon carpet. The discharge occurs when one reaches for a doorknob or other conductive surface. The types of ESD with which we will be concerned fall into the category of triboelectric effects. Within this category, various materials have differing potentials for charge. Asbestos, nylon, human and animal hair and wool have a high positive triboelectric potential. Silicon has one of the highest negative triboelectric potentials, followed by such materials as polyurethane, polyester and rayon. Cotton, wood, steel and paper all tend to be relatively neutral, which makes cotton clothing and steel table tops excellent ESD protective materials in environments where ESD problems can be anticipated.

The intensity of the charge is inversely proportional to the relative humidity. As humidity decreases, ESD problems increase. For example, walking across a carpet will generate a 1.5 kV charge at 90%RH, but will generate 35 kV at 10%RH. When an object storing a static charge comes in contact with another object, the charge will attempt to find a path to ground, discharging into the contacted object. Although the current level is extremely low (typically less than 0.1 nanoamp), the voltage can be as high as 35-50 kV.

The degree of damage caused by electrostatic discharge is a function of the size of the charge (which is determined by the capacitance of the charged object) and the rate at which it is discharged (determined by the resistance into which it is discharged). This relationship can be shown with a waveform (*Figure 6-4*) that utilizes what is termed a double exponential decay pulse. With such a pulse, 99% of the energy will be dissipated in five time constants, with each time constant established by the resistance and capacitance mentioned above. Where both are low, the discharge rate will be rapid enough to cause damage if the object into which discharge occurs is a semiconductor. As resistance and capacitance increase, both the discharge rate and the risk of damage decrease.

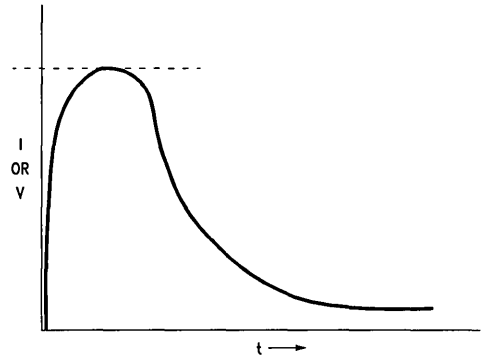

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FIGURE 6-4. Ideal RC Waveform

It is estimated that the value of devices lost to ESD could run as high as $1 billion per year. Most electrostatic damage is caused by the handling of devices by personnel who have not taken adequate precautions. One would expect this in light of the fact that the capacitance of the human body ranges from 50 to 200 pF. The ESD characteristics of work surfaces and of materials passing through the area should not be ignored, however, in an attempt to concentrate on the human effect.

Types of ESD Damage

The damage caused by ESD results from the charge's tendency to seek the shortest path to ground, overstressing any electrical interfaces in that path. There are several different types of damage that result, and each of these tends to be typical of specific component technologies and elements.

Dielectric Breakdown

Dielectric breakdown occurs when the voltage across an oxide exceeds its dielectric breakdown strength. The single most important factor in this breakdown is the oxide thickness *(Figure 6-5)*. Thinner oxide is more susceptible to electrostatic punch-through, which leaves a permanent low-resistance short through the oxide. Where there are pin holes or other weaknesses in the oxide, damage will be possible at lower charge levels. It should be noted that semiconductor manufacturers have reduced oxide thicknesses as they have reduced the overall size of the devices. ESD sensitivity has therefore increased dramatically.

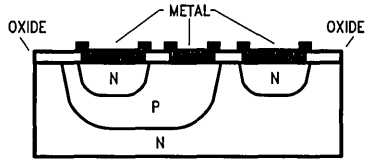

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FIGURE 6-5. Bipolar Transistor

Electrostatic charge which does not actually result in a breakdown can cause lattice damage in the oxide, lowering its ability to withstand subsequent ESD exposure. A weakened lattice will also have a lower breakdown threshold voltage, and this mechanism is voltage dependent.

Thermal Secondary Breakdown or Junction Burnout

Junction burnout is a significant failure mechanism for bipolar devices, and tends to be power dependent rather than voltage dependent. The interface (or junction) between a P-type diffusion and an N-type diffusion normally has a positive temperature coefficient at low temperatures (that is, increased temperature will result in increased resistance). When a reverse-biased pulse is applied, the junction dissipates heat in its very narrow depletion region, and the temperature increases rapidly. If enough energy is applied, the temperature of the junction will reach a point at which the temperature coefficient of the silicon will turn negative (that is, at which increased temperature will result in **decreased** resistance). Since the area of the junction is not uniform, hot spots occur. When the melting temperature of silicon (1415°C) is reached as a result of the ensuing thermal runaway condition, junction melting occurs in the localized area. If there is an additional energy available after the initiation of melt, the hot spot can grow into a filament short. The longer the pulse, the wider the resultant filament short.

After the occurrence of the transient, the silicon will resolidify. In a relatively short pulse, a hot spot may form, but not grow completely across the junction. As a result, the damage may not manifest itself immediately as a junction short but will appear at a later time as a result of electromigration. Shrinking geometries will decrease junction areas, and this should increase the susceptibility of these devices to ESD related junction problems.

Metallization Melt

Semiconductor interconnect metallization typically has a small cross-sectional area and limited current carrying capability. As feature sizes continue to be reduced, metallization cross-section will be reduced as well. Reducing metallization line width by half and metallization thickness by half reduces the current carrying capability of that metallization stripe by 75%. Metallization melt, which is a power-dependent failure mechanism, is more likely to occur during short duration, high current pulses, since the only available heat sink (the bonding pad) is nearby and the heat dissipated in the metallization does not have time to flow into the surrounding areas. It can also occur as a side effect during junction melt.

Latent Failures

Immediate failure resulting from ESD exposure is easily determined: the device no longer works. A failed device may be removed from the lot or from the subassembly in which it is installed, and it represents no further reliability risk to the system. There are, however, devices which have been exposed to ESD but which have not immediately failed. Unfortunately, there has never been sufficient data dealing with the long-term reliability of devices which have survived ESD exposure, although some experts feel that two to five devices are degraded for every one that fails. It should be obvious from an examination of the failure mechanisms described above that there can be significant degradation without immediate failure. Damage can manifest itself in either a shortening of the device's lifetime (a possible cause for many of the infant mortality failures seen during burn-in) or in electrical performance shifts, many of which cause the device to fail electrical test limits.

ESD Protective Measures

It should be obvious then that there are three principal considerations when dealing with ESD. The first is that the device should be designed in a manner that minimizes ESD sensitivity and incorporates some ESD protective features. The second is that both manufacturers and users must understand the ESD susceptibility of the devices with which they are dealing. Thirdly, both user and manufacturer must understand the generation of and sources of ESD charges well enough to establish proper precautions throughout their plants.

Device Design

The continuing development of faster and more complex ICs makes it unlikely that we will see a return to thicker oxide layers or larger junctions. Early ICs used fairly simple clamping diodes on the inputs to protect them against voltage transients in the system. Similar, but more complex protective networks can be employed to provide ESD protection. An example of such circuitry is shown in *Figure 6-6* as it is employed in the design of the F100K 300 Series family. Electrostatic discharge (ESD) protection diodes were added to all 300 Series designs specifically in the circuit paths that were most prone to ESD damage on F100K 100 Series products: input-to-V_{CC}, input-to-V_{EE}, and output-to-V_{CC}.

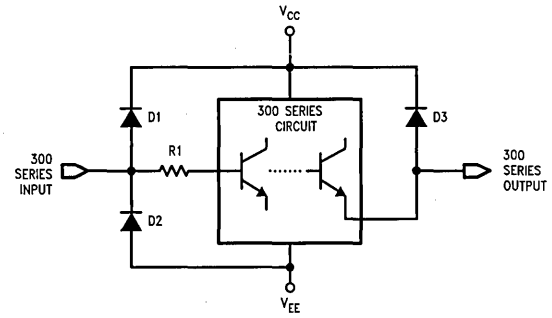

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FIGURE 6-6. 300 Series ESD Protection Circuitry

These diodes (D1, D2 and D3) are utilized to shunt the current caused by an ESD voltage pulse away from either the input or output circuitry. Depending on the polarity of the ESD voltage, the diodes either become forward-biased, directing the current into the supply, or go into reverse breakdown, directing the current into the substrate. Either way the ESD-caused current is shunted away from the input and output transistors, avoiding damage to the circuitry. The diodes are designed to be rugged enough to guarantee 2000V of ESD protection on all 300 Series products (they typically withstand up to 4000V). Even in providing this protection level, these diodes have a negligible impact on input capacitance. Addition of these diodes typically adds only tenths of picofarads to each product's input capacitance.

Assessing ESD Tolerance Levels

As awareness of the importance of addressing ESD concerns spread, many experts felt that ESD testing had to be uniform if results were to be shared. Method 3015 of MIL-STD-883 was created for the purpose of allowing manufacturers to assess the ESD tolerance levels of the devices they offered and to allow users to determine the ESD sensitivity of the parts with which they were assembling systems. Method 3015 has established a test circuit (see *Figure 6-7*) which approximates the resistance and capacitance found in the human body (which continues to provide the major source of destructive ESD). The testing is performed by charging the capacitor in the test circuit and then discharging that capacitor into the unit under test. After testing, a device will be classified as either Class 1, those devices which exhibit ESD-induced failure or degradation at levels between zero volts and 1,999V; or Class 2, those which may exhibit ESD sensitivity at levels between 2,000V and 3,999V; or Class 3, those devices which may exhibit ESD sensitivity at levels above 4,000V but have passed all testing up to that level. This testing is performed on a sample basis at initial device qualification and need not be repeated unless the device is redesigned. The testing is considered destructive, even for those devices which do not fail.

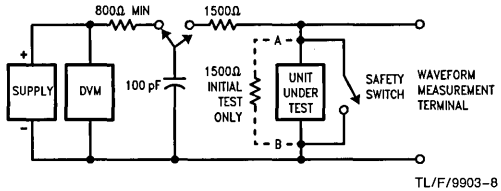

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FIGURE 6-7. ESD Test Circuit

A device may be characterized as Class 1 in lieu of testing at a manufacturer's discretion. Some manufacturers, concerned with the possibility of latent damage due to inadequate protection of devices which test as Class 2, and concerned that static charges resulting from handling can run as high as 50 kV, have elected to treat all of their devices as Class 1, thus ensuring that consistent implementation of common handling procedures will provide maximum protection for all devices.

Data generated by an RADC study of electrostatic discharge susceptibility (VZAP-1, Spring 1983) would seem to support that kind of a conservative approach. The data (see *Figure 6-8*) shows the point at which failure first occurred for a given device. It indicates that there are a number of devices which can be expected to fail between 2 kV and 5 kV, but few that will survive beyond 10 kV.

Those devices which are classified as Class 1 must be marked with one equilateral triangle, and those classified as Class 2 must be marked with two equilateral triangles to identify them as static sensitive. (Class 3 devices will have no top mark designator.)

TABLE I. Device ESD Failure Threshold Classification

MIL Class	ESD Tolerance	Top Mark Designation
Class 1	0V to 1,999V	One triangle (i.e., ▲)
Class 2	2,000V to 3,995V	Two triangles (i.e., ▲▲)
Class 3	4,000V and above	No mark

ESD Precautionary Measures

ESD protective measures fall into two categories: those which shield the device from ESD and those which control the occurrence of ESD. ESD shielding can be accomplished by either grounding all of the device leads together, thus providing a more direct path to ground, or by surrounding the device with insulating material that would keep ESD from reaching the device. The first method is most practical during device assembly and environmental test, the second during shipment and storage. However, neither can be utilized during electrical testing.

Most of the handling of ICs, however, occurs during electrical testing. Testing cannot be performed if the device's leads are shorted together, nor can it take place if the device is within an insulated container. Control of ESD during testing is therefore extremely important. This is accomplished through the grounding of all potential sources of ESD. Stainless steel work surfaces connected to ground

through an appropriate resistive element provide a harmless bleed-off of any charge that occurs. Requiring that all personnel who handle devices wear ground straps can effectively eliminate the human body and its clothing as sources of ESD. It is also important to minimize the handling of devices. This can be partially accomplished through the use of automated test handlers, which allow the devices to be loaded into the testers from ESD-protective rails and returned to those rails from the tester. Equally important is the elimination of any unnecessary testing or test insertions. Semiconductor manufacturers have decreased the number of test insertions for many devices by combining parametric, functional and switching tests onto a single insertion test program. Users have minimized handling by relying more heavily on the testing performed by their vendors and by eliminating incoming testing. Pick-and-place systems and other automated board assembly hardware have also helped to minimize device handling. Most systems manufacturers have also implemented procedures that minimize the handling of boards and subassemblies in order to ensure that devices receive no potentially damaging exposure to ESD after board assembly.

Effective control of ESD, however, cannot be accomplished unless the entire work area is designed around ESD concerns. At the National Mil/Aero facilities, all work areas in which parts may be handled or through which parts may pass have ESD-protective flooring in addition to grounded work surfaces, ground straps for all operators, and other protective features. This level of attention to detail is essential to the minimization of ESD problems.

Summary

Electrostatic discharge will continue to be a major concern for those who use semiconductor devices. As device geometries continue to shrink, the ESD sensitivity of devices will increase. Only through proper handling and packaging, and through proper attention to ESD concerns will we be able to ensure that long term reliability of key systems is not negatively affected by ESD problems.

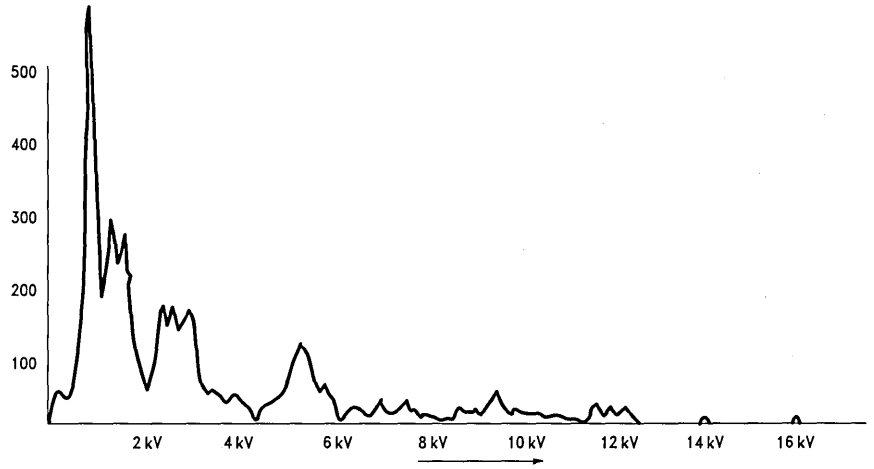

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FIGURE 6-8. Failure Rate at Ascending ESD Voltages

National Semiconductor

Chapter 7
300 Series Package Qualification

INTRODUCTION

In order to facilitate migration from the original F100K ECL 100 Series (1001XX) family to the F100K ECL 300 Series (1003XX) family, National Semiconductor has published this guide to 300 Series qualification. Much of the focus is toward the secondary migration of ceramic to plastic packaging.

This guide contains thermal comparison data by package type, AC comparison data by package type, input capacitance comparison data by package type, and other valuable information for use in qualifying the 300 Series for your application.

The original F100K 100 Series family (1001XX) was the accepted standard for subnanosecond logic used in high-speed next-generation systems. The main features were:

- High speed: 750 ps internal gate delays
- Temperature compensation (signal levels, noise margins)
- Complementary outputs (with no sacrifice of speed)
- High common mode noise rejection (differential line receivers)
- Easy-to-use edge rates (1V/ns)
- High fanout capability
- Wired-OR capability
- Low EMI
- Low impedance drive capability (25Ω, 50Ω)
- Optimum I/O pin assignment (side power pins, outputs adjacent to GND)

But, while perfectly adequate for its original intended purpose (supercomputers, mainframes, etc.), the 100 Series had several limitations that gave some system designers reasons to avoid utilizing the superior performance of F100K ECL. Some of those problem areas were power consumption, limited temperature and voltage ranges, the absence of ESD protection, limited packaging options, incompatibility with +5.0V systems, and no military product availability.

F100K 300 Series ECL was introduced with plastic packaging options to retain all the traditional benefits and high performance of the original 100 Series, along with some key enhancements:

- **POWER REDUCTION:** 300 Series power consumption was reduced by 30%–50% from original 100 Series levels (even while increasing the specified voltage range from −4.8V to −5.7V). This improvement has lowered F100K power-per-bit to the same or less than 10K/10KH ECL levels. Also, ECL power levels are constant over frequency, making 300 Series the low-power bipolar alternative above 45 MHz, and the overall low-power alternative (including both Bipolar TTL and CMOS logic families) above 60 MHz.
- **EXTENDED TEMPERATURE RANGE:** The 300 Series has been designed to operate at Commercial (0°C to +85°C), Industrial (−40°C to +85°C), and Military (−55°C to +125°C) temperature ranges.
- **EXTENDED VOLTAGE RANGE:** The 300 Series has been designed to operate over an extended voltage range of −4.2V to −5.7V, spanning the voltage ranges of all ECL logic families, and also making it possible to operate ECL in a +5.0V system.
- **NEW OUTPUT SKEW SPECS:** The improvements to the 300 Series circuitry that have increased the temperature and voltage ranges also make it possible to specify several output skew parameters on the PCC package which guarantee the level of pin-to-pin skew and output duty cycle degradation.
- **ESD PROTECTION:** The 300 Series has been designed to have a minimum of 2,000V of electrostatic discharge (ESD) protection, which helps eliminate "walking wounded" at incoming test, and even ESD-related board failures.
- **INCREASED PACKAGING OPTIONS:** The 300 Series is now offered in 28-lead Plastic Chip Carrier (PCC), 24-lead 400 mil Plastic DIP (PDIP), and 24-lead 300 mil SOIC. The availability of plastic packaging allows National Semiconductor to set initial PDIP and SOIC pricing significantly below historic F100K ECL pricing.
- **+5.0V COMPATIBILITY:** The increased voltage range of the 300 Series allows it to be operated in a +5.0V system. Also, several Single-Rail Positive ECL (PECL) devices, which translate from differential ECL operated at +5.0V to traditional TTL-compatible levels, have been developed.
- **MILITARY AVAILABILITY:** The 300 Series is in complete compliance with the requirements of MIL-STD-883 for Class B devices. Also, DESC has initiated Standard Military Drawings (SMD's) for the 300 Series.

An F100K 300 Series device is easily identified by the device numbering scheme. A typical F100K 100 Series device was referred to as 1001XX, 300 Series devices are referred to as 1003XX. For example, the 100101 has been replaced by the 100301. This naming convention carries throughout the whole family.

POWER REDUCTION

New Process

F100K 300 Series ECL is fabricated using an advanced isoplanar technology called FAST-LSI. FAST-LSI includes many improvements over FAST-Z (the process used for the

original F100K 100 Series ECL), which enhance performance, manufacturability, and reliability. Both processes are descendants of Fairchild's Isoplanar II oxide-isolated process which yielded the industry standard FAST® family of products.

Power Comparison (1001XX vs 1003XX)

Parasitic capacitances and resistances are reduced due to smaller geometries, allowing significant power reduction, up to 50% lower than FAST-Z. Dual-Supply (ECL, TTL) Level Translators were prime candidates for power reduction since they have a high supply voltage across the part (nominally 9.5V, 5V TTL plus 4.5V ECL). The 1003XX replacements for the 1001XX level translators (100124, 100125, 100128) all exhibit a 50% power reduction from the 1001XX part.

For more information on the FAST-LSI process, refer to the Family Overview.

Decreased Junction Temperature

With the lower power of the 300 Series, there is a reduction in junction temperature when converting from 100 Series in ceramic packaging to 300 Series in plastic packaging. This factor, combined with the inherent flat power requirements over frequency of ECL circuitry, enable designers to use ECL in plastic in high performance systems which have significant power constraints and little or no airflow, such as desktop workstations. *Figure 7-1* compares the junction temperatures of the original 100 Series packaged in CDIP with 300 Series ECL packaged in PDIP, PCC, and SOIC. *Figure 7-1* represents worst case conditions: zero airflow, power current at the maximum limit, and a 70°C ambient temperature.

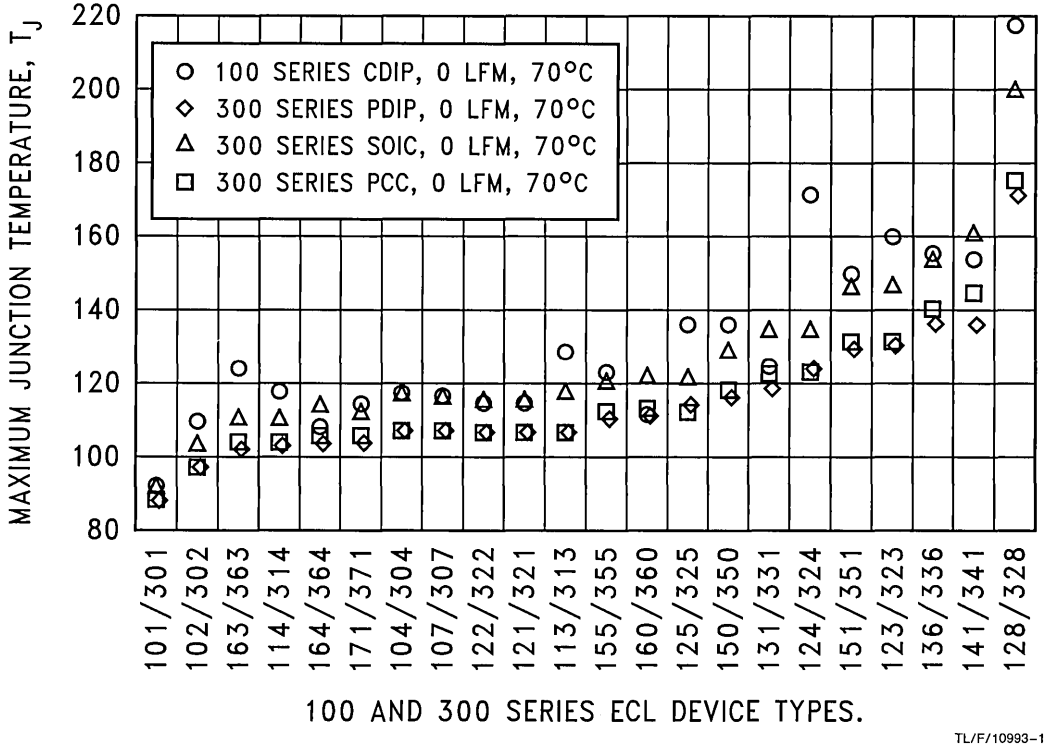

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FIGURE 7-1. Junction Temperature Comparison (Ceramic vs Plastic Packaging)

The Effect of Airflow on Junction Temperature

A small amount of airflow significantly decreases the thermal resistance of the plastic packages. *Figure 7-2* shows the impact of airflow on the thermal resistance of the PDIP package. Most of the benefit from adding airflow is realized in the first 225 linear feet per minute (LFPM). The reduction in thermal resistance due to the increase in airflow significantly reduces the device junction temperature. *Figure 7-3* is identical to *Figure 7-1*, with the exception of a moderate airflow of 225 LFPM.

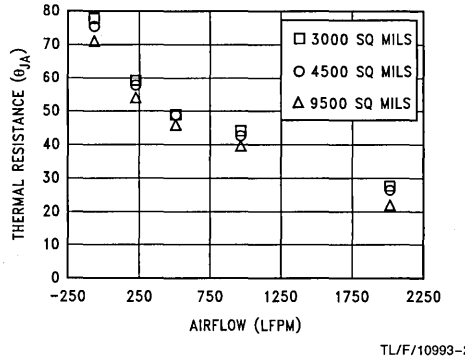

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FIGURE 7-2. θ_{JA} vs Airflow for 4 Die Areas

The junction temperatures in *Figures 7-1* through *7-3* are based on the worst possible case of power dissipation, which assumes that the device is being operated at the maximum power supply voltage (−5.7V) and that the power supply current is marginal to the extreme maximum current limit. Using nominal power dissipation (−4.5V supply voltage with typical power supply current) significantly reduces the calculated junction temperature increase with respect to ambient.

As an example, at 70°C ambient, the 100324SC has a worst case junction temperature of 135°C, whereas its nominal junction temperature is 112°C.

Family Performance Comparisons

No matter what the frequency or duty cycle is, ECL circuitry draws constant DC power, eliminating the noise margin jeopardy associated with the dynamic switching currents of other technologies. When an internal ECL gate switches, the gate current is simply redirected from one side of the gate to the other, yielding no net change in power requirements, even at frequencies of 50 MHz–250 MHz or more. In addition, the complementary output buffers of ECL are similar in that there is no dynamic switching current, which results in no ground bounce. *Figure 7-4* compares power consumption over frequency on several octal registers (100353, 74ALS374, 74F374, and 74AC374). This graph shows that the power requirements of the 300 Series 100353 are less than all of the other technologies above 60 MHz.

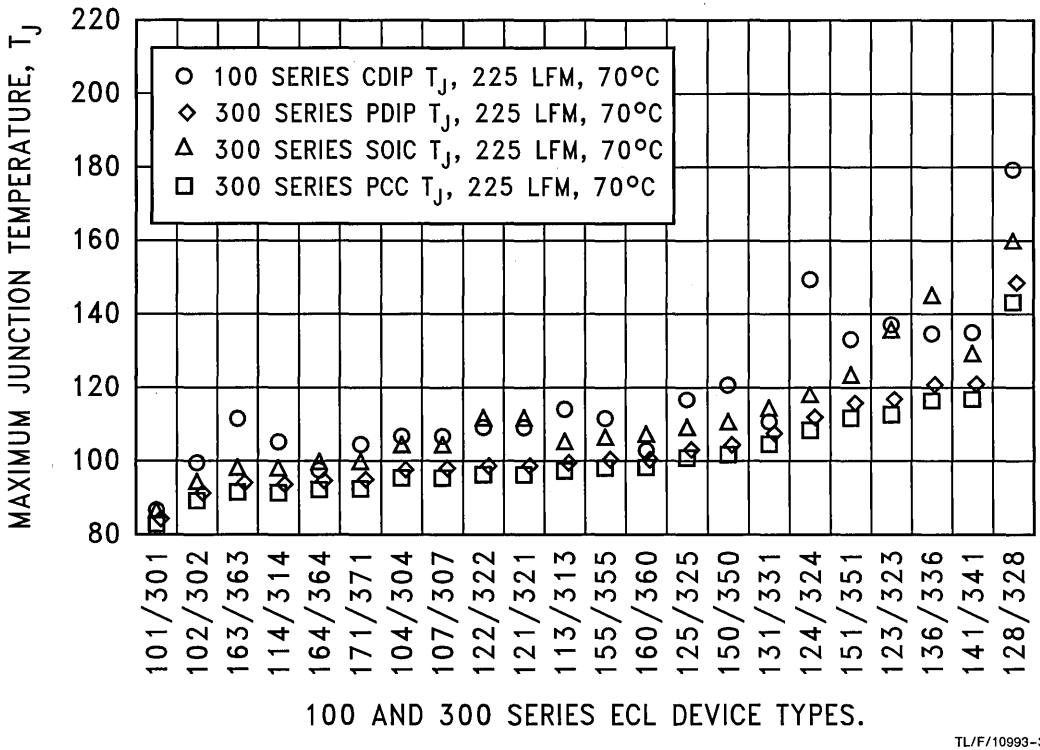

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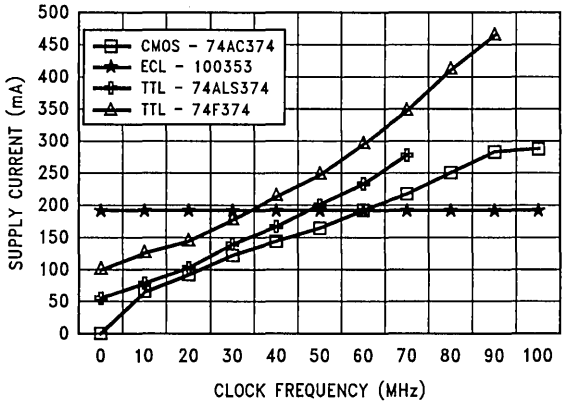
FIGURE 7-3. Junction Temperature Comparison (Ceramic vs Plastic Packaging)



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Note: I_{CC} measured in test jig, 25°C, C_L = 50 pF, 50% duty cycle, all outputs switching. ECL current = I_{CC} + I_{TT}.

FIGURE 7-4. Power Comparison by Technology

Speed-Power Product over Frequency

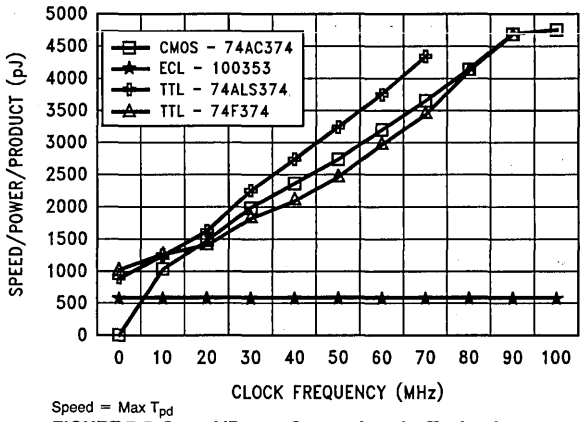
The speed-power product is one generally accepted measure of overall device performance. When the power numbers from *Figure 7-4* are weighted with the device speed performance (in *Figure 7-5*, effectively producing a plot of speed-power product over frequency), the benefits of ECL become even more evident. At frequencies greater than 5 MHz, ECL exhibits the lowest speed-power product.

EXTENDED VOLTAGE RANGE AND IMPROVED NOISE MARGIN

F100K 300 Series ECL was designed with a more stabilized voltage reference generator, which allows all products to offer a single set of DC Input/Output specifications across a wider supply range (−4.2V to −5.7V) than the original F100K 100 Series (see *Figure 7-6*).

Regardless of whether the designer's system is F100K input/output levels at a nominal −4.5V, F100K input/output levels at a nominal −5.2V, 10K input/output levels at a nominal −5.2V or ECL operated on a nominal +5.0V rail, the single set of 300 Series DC input/output specifications guarantee full operation. This allows easy interconnectivity with ECL ASICS, RAM's, 10K- and 10 KH-compatible logic, and +5.0V TTL devices. As usual, if F100K ECL is driving a 10K ECL input (non-temperature-compensated), care must be taken when operating at ambient temperatures above 55°C.

ECL has an inherent insensitivity to power supply (V_{EE}) variations, since ECL is referenced to ground (V_{CC}), unregulated power supplies do not cause changes in input thresholds or output levels.



Speed = Max T_{pd}

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FIGURE 7-5. Speed/Power Comparison by Technology

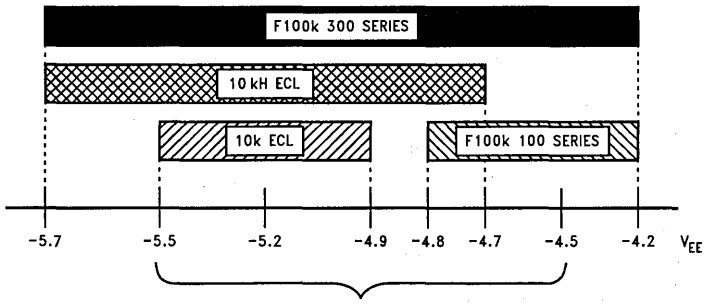

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FIGURE 7-6. 300 Series (Extended Specified Voltage Range)

This single set of DC specifications increases 300 Series noise margin to a minimum of 140 mV compared to 115 mV of the original 100 Series (see *Figure 7-7*).

OUTPUT SKEW

ECL Skew

ECL is inherently low skew due to several factors. The differential pair circuitry of ECL keeps the skew between "true" and "complement" outputs to a minimum. The lack of dynamic current demands during switching eliminates the skew associated with power supply pin impedance and its associated "ground bounce" effects. Lastly, ECL is not a saturating logic, so LH-to-HL skew is also minimized.

Addition of Skew Specifications

Several skew specifications, chosen based on system performance demands, have been added to the 300 Series ECL PCC AC datasheet specifications for most devices to enable ECL designers to take advantage of ECL low skew. The parameters (t_{OSLH}, t_{OSHL}, t_{OST} and t_{PS}) relate back to a specific system requirement which helps the designer to compensate for pin-to-pin skew and output duty cycle degradation. (For a more detailed explanation, refer to the Family Overview Section.)

THERMAL CONSIDERATIONS

To calculate the operating junction temperature (T_J) of F100K ECL 300 Series devices, one can use either of the two equations listed below, depending on whether the ambient temperature (T_A) or case temperature (T_C) is known:

$$T_J = T_A + (P_D \times \theta_{JA})$$

$$T_J = T_C + (P_D \times \theta_{JC})$$

One can see that the junction temperature of a device is dependent on thermal factors in the environment (T_A or T_C), the power dissipation of the device itself (P_D), and package-dependent thermal resistance coefficients (θ_{JA} or θ_{JC}).

Calculating Device Power Dissipation

The device power dissipation P_D is a function of the maximum absolute value of device power ($V_{EE\ MAX}$), the maximum absoulte value I_{EE} limit ($I_{EE\ MAX}$), the number of loaded outputs in the high state (nh), and the number of loaded outputs in the low state (nl), as follows:

$$P_D = (V_{EE\ MAX} \times I_{EE\ MAX}) + (nh \times [V_{OH} \times I_{OH}]) + (nl \times [V_{OL} \times I_{OL}])$$

$V_{EE\ MAX}$ is defined either by the worst case power supply voltage in a specific application, or it can be taken from the databook absolute value maximum limit (−5.7V). $I_{EE\ MAX}$ is taken from the databook device specification.

The second and third factors of the power dissipation (P_D) equation depend on the output loading scheme used; for the standard 50Ω to −2V ECL load, this term results in 27 mW per complementary output pair (14 mW for the output at V_{OH}, and 13 mW for the output at V_{OL}). *Figures 5-10* and *5-14* in Chapter 5 of this databook list output power dissipation figures for multiple combinations of parallel and serial output terminations. P_D for single-ended ECL outputs should be calculated with the outputs in the high state, which is worst case.

θ_{JA} and θ_{JC} are package-dependent thermal resistance coefficients derived empirically in the National Semiconductor Packaging Development Laboratory in compliance with MIL-STD-883 Method 1012. The laboratory presents data on each package using several die sizes to generate a family of curves. The data is taken at several airflows. From the thermal resistance charts (*Figures 7-8* through *7-12*), increased airflow reduces the thermal resistance. Increase die size also reduces the thermal resistance, which is convenient since die size corresponds in general with device power. Table 7-1 contains die areas of 1003XX devices to use in conjunction with the thermal resistance charts in *Figures 7-8* through *7-12*.

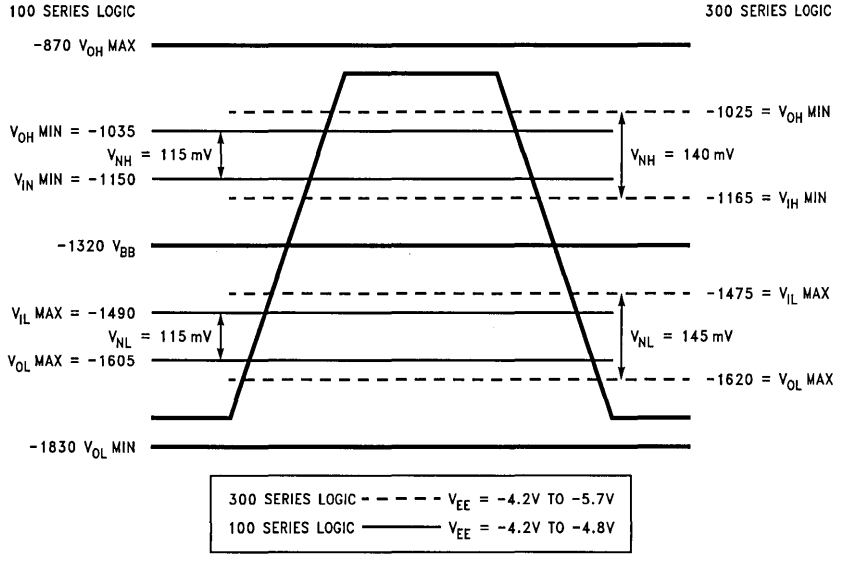

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FIGURE 7-7. 300 Series Improved Noise Margins

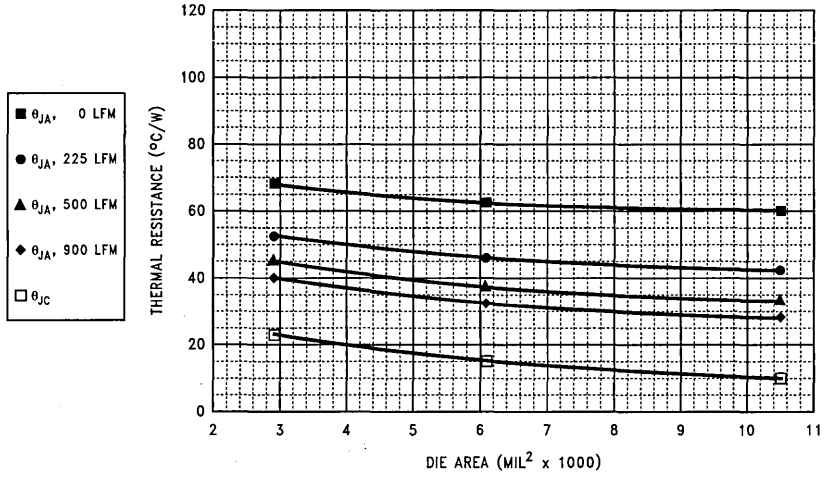

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FIGURE 7-8. Thermal Resistance by Die Area (Ceramic 400 mil DIP (CDIP))

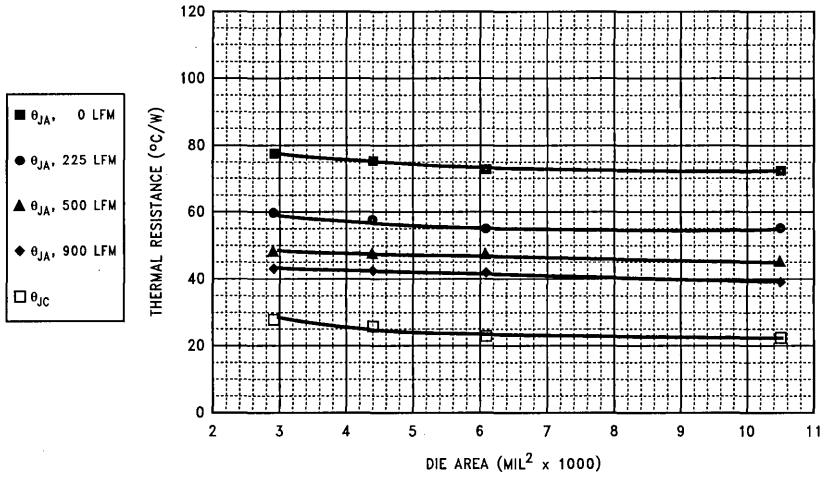

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FIGURE 7-9. Thermal Resistance by Die Area (Plastic 400 mil DIP (PDIP))

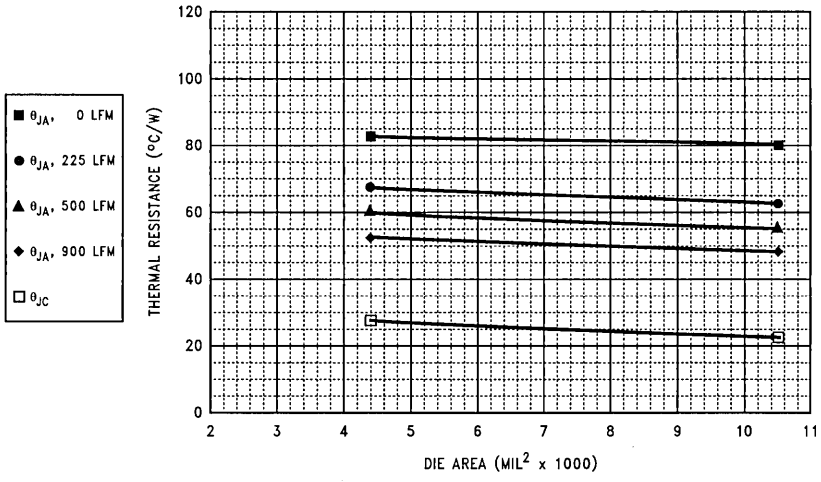

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FIGURE 7-10. Thermal Resistance by Die Area (Small Outline IC (SOIC))

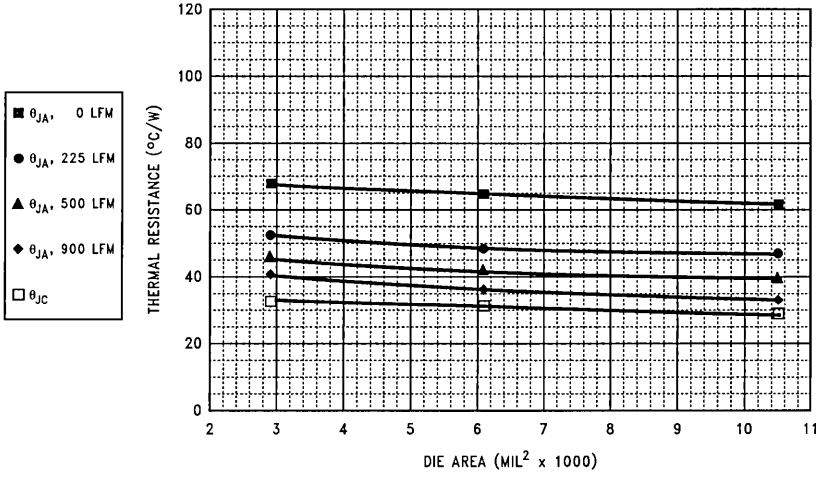

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FIGURE 7-11. Thermal Resistance by Die Area (Plastic Chip Carrier (PCC))

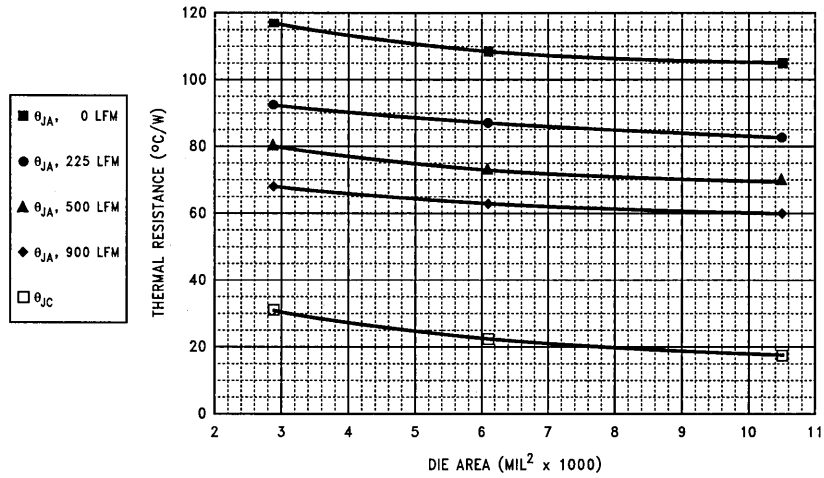

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FIGURE 7-12. Thermal Resistance by Die Area (Ceramic Quad Flat Pack (QFP))

TABLE 7-1. F100K 300 Series Die Area

Part Type	Area = Mil²
100301	4422
100302	4422
100304	3843
100307	3843
100310	5670
100311	5670
100313	4422
100314	4422
100315	2401
100316	4420
100319	4420
100321	2907
100322	2907
100323	4420
100324	4422
100325	5475
100328	9309
100329	9309
100331	5325
100336	10494
100341	6106
100343	6230
100344	6230
100350	4636
100351	4636
100352	6230
100353	6230
100354	6230
100355	4891
100360	4422
100363	5032
100364	5032
100370	5110
100371	4422
100389	5767
100390	3905
100391	5767
100392	5767
100393	8736
100395	8736
100397	6622
100398	6622

Case Temperture vs Ambient Temperature: What is the Difference?

F100K ECL Logic is specified over a case temperature range, as opposed to an ambient temperature range. There is a critical difference between case temperature and ambient temperature that can not be overlooked, and can be shown with the following example:

Looking at a 300 Series device with typical power dissipation and thermal resistance figures:

θ_{JA}	θ_{JC}	P_D
68°C/W	32°C/W	0.5 W

At T_A = 70°C, the junction temperature is calculated as:

$$T_J = T_A + (P_D \times \theta_{JA})$$
$$= 70°C + (0.5\ W \times 68°C/W)$$
$$= 70°C + 34°C$$
$$= 104°C$$

Using the same T_J of 104°C to work back toward a T_C, you get:

$$T_C = T_J - (P_D \times \theta_{JC})$$
$$= 104°C - (0.5\ W \times 32°C/W)$$
$$= 104°C - 16°C$$
$$= 88°C$$

So, on this device at a T_J of 104°C, T_C is 18°C higher than T_A (88°C vs 70°C). *Figure 7-13* shows that the difference between T_C and T_A increases linearly with increasing P_D—everything else being equal, a 1.0W device in the above scenario would have a 36°C difference (2 × 18°C) between T_C and T_A.

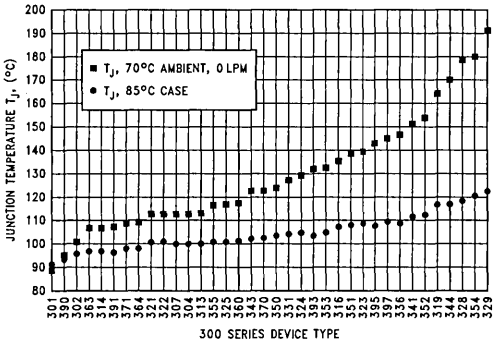

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FIGURE 7-13. Case vs Ambient Temperature 24-Lead PDIP

The difference between T_C and T_A decreases with increasing airflow. In fact, T_C is the temperature of the case when measured at 2000 LFM (closely approximates infinite airflow).

PACKAGING OPTIONS

The low power designs of 300 Series ECL, combined with the manufacturability of the FAST-LSI process, have enabled the 300 Series to be offered in packaging that takes up less board space than the standard 400-mil DIP of the original 100 Series, namely the 28-lead Plastic Chip Carrier (PCC) and 24-lead 300-mil SOIC. These plastic package solutions can dramatically increase board density and reduce user cost compared to the package offerings of the original 100 Series.

The required board space for the 24-lead PCC is 113% less than that for 24-lead 400-mil DIP packages. The SOIC is a 103% reduction compared to the DIP.

The new 24-lead 400 mil Plastic DIP is intended as a drop-in replacement cost reduction for all users of "100 Series" or "300 Series" 24-lead 400 mil Ceramic DIP.

PACKAGE COMPARISONS

A comparison between the SOIC, PDIP, CDIP, and PCC packages (prop delays, input capacitance) is provided here to assist in the transition from ceramic to plastic packaging.

AC Comparisons

Two devices were selected for the AC comparison: the 100304 is a simple ECL gate in which inputs and outputs are found on both side pins and corner pins of the dual-in-line packages, and the 100325 is an ECL-TTL level translator which represents the dynamic current switching effects of TTL outputs.

The results show that there is less than 100 ps of difference in the 100304 $D_n \rightarrow O_n$ propagation delay between all four packages (see *Figure 7-14*).

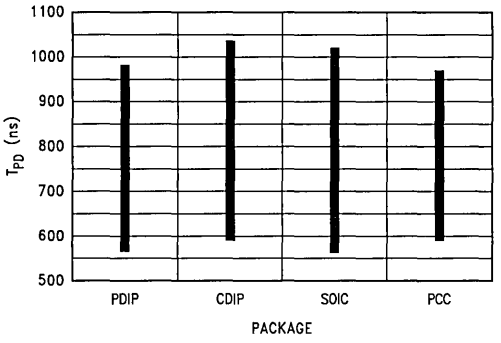

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FIGURE 7-14. Propagation Delay Comparison by Package, 100304

Figure 7-15 shows that the CDIP package exhibits a 130 ps–150 ps spread between side pins and corner pins, whereas the PDIP package reduces that to 90 ps, indicating that dual-in-line packaging has an inherent pin-to-pin skew.

Due to the complementary nature of ECL circuitry and its flat power requirements over its frequency range, the effects of differences in power supply lead inductance and capacitance are minimized. Therefore, the minimal difference between packages, and the extremely low output skew displayed in *Figures 7-14* and *7-15*, should be expected. Once dynamic supply current effects are eliminated, the difference in propagation delay measurements between packages are mainly due to differences in package lead length, and measurement accuracy.

Figure 7-16 shows that there is less than 300 ps difference between the four packages on a 3 ns measurement on the 100325, even with its TTL outputs.

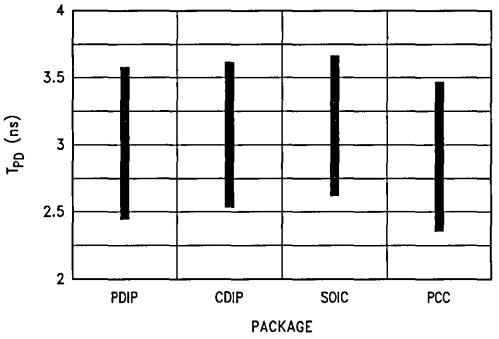

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FIGURE 7-16. Propagation Delay Comparison by Package, 100325

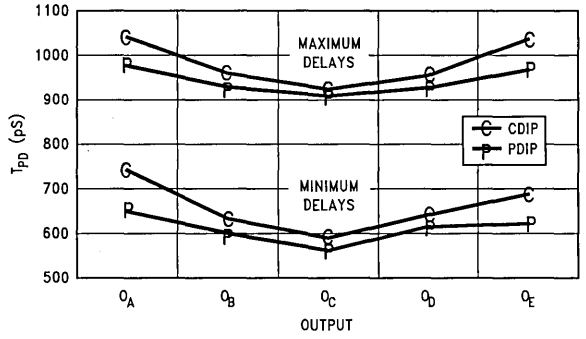

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FIGURE 7-15. Propagation Delay Comparison PDIP vs CDIP, 100304

Figure 7-17 shows that the differences between corner pins and side pins on a 100325 in a DIP package are negligible, although the outputs (Q3, Q4, and Q5) closest to the TTL supply (V_{TTL}) pins have a somewhat tighter range of values than the outputs (Q0, Q1 and Q2) closest to the ground (V_{CC}) pins.

This data shows that there is negligible difference in AC propagation delay between the CDIP, PDIP, SOIC and PCC packages.

Figures 7-18 and *7-20* show that the PCC package is an electrically symmetrical package, all outputs exhibit similar propagation delays. *Figures 7-19* and *7-21* show that the SOIC package exhibits similar characteristics to the PDIP package (typically longer delays on corner pins, as opposed to side pins).

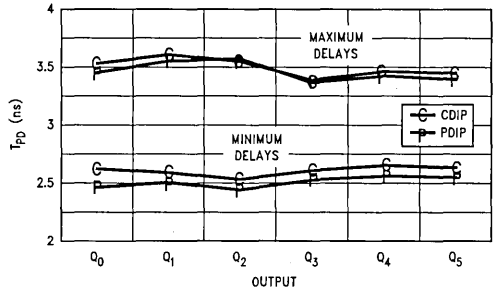

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FIGURE 7-17. Propagation Delay Comparison PDIP vs CDIP, 100325

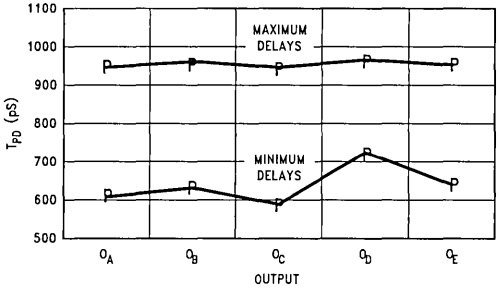

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FIGURE 7-18. Propagation Delay Comparison PCC, 100304

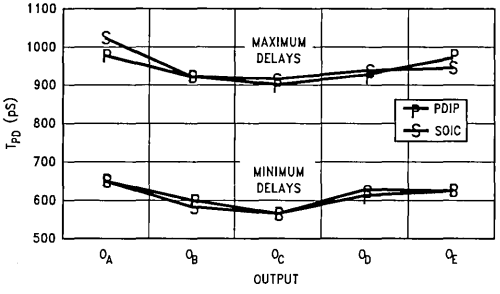

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FIGURE 7-19. Propagation Delay Comparison PDIP vs SOIC, 100304

Input Capacitance Comparisons

Input capacitance differences were also measured between packages. The 100304 was used for the input capacitance comparison. *Figure 7-22* shows that one of the reasons for in-line package corner pins exhibiting longer propagation delays is due to an increase in lead capacitance on the corner pins.

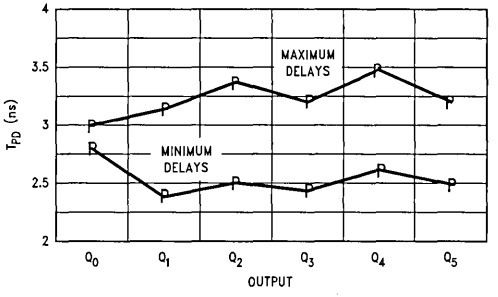

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FIGURE 7-20. Propagation Delay Comparison PCC, 100325

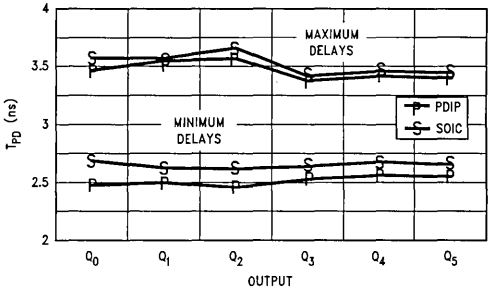

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FIGURE 7-21. Propagation Delay Comparison PDIP vs SOIC, 100325

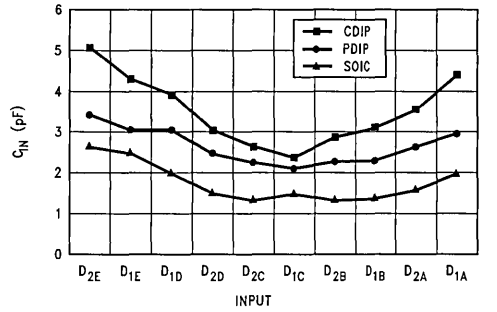

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FIGURE 7-22. Input Capacitance Dual-In-Line Packages, 100304

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Chapter 8
Quality Assurance and Reliability

Introduction

F100K ECL is manufactured to strict quality and reliability standards. Product conformance to these standards is insured by careful monitoring of the following functions: (1) incoming quality inspection, (2) process quality control, (3) quality assurance, and (4) reliability.

Incoming Quality Inspection

Purchased piece parts and raw materials must conform to purchase specifications. Major monitoring programs are the inspection of package piece parts, inspection of raw silicon wafers, and inspection of bulk chemicals and materials. Two other important functions of incoming quality inspection are to provide real-time feedback to vendors and in-house engineering, and to define and initiate quality improvement programs.

Package Piece Parts Inspection

Each shipment of package piece parts is inspected and accepted or rejected based on AQL sampling plans. Inspection tests include both inherent characteristics and functional use tests. Inherent characteristics include physical dimensions, color, plating quality, material purity, and material density. Functional use tests for various package piece parts include die attach, bond pull, seal, lid torque, salt atmosphere, lead fatigue, solderability, and mechanical strength. In these tests, the piece parts are sent through process steps that simulate package assembly. The units are then destructively tested to determine whether or not they meet the required quality and reliability levels.

Silicon Wafer Inspection

Each shipment of raw silicon wafers is accepted or rejected based on AQL sampling plans. Raw silicon wafers are subjected to non-destructive and destructive tests. Included in the testing are flatness, physical dimensions, resistivity, oxygen and carbon content, and defect densities. The test results are used to accept or reject the lot.

Bulk Chemical and Material Inspection

Bulk chemicals and materials play an important role in any semiconductor process. To insure that the bulk chemicals and materials used in processing F100K wafers are the highest quality, they are stringently tested for trace impurities and particulate or organic contamination. Mixtures are also analyzed to verify their chemical make-up.

Incoming inspection is only the first step in determining the acceptability of bulk chemicals and materials. After acceptance, detailed documentation is maintained to correlate process results to various vendors and to any variations found in mixture consistency.

Process Quality Control

Process quality is maintained by establishing and maintaining effective controls for monitoring the wafer fabrication process, reporting the results of the monitors, and initiating valid measurement techniques for improving quality and reliability levels.

Methods of Control

The process quality control program utilizes the following methods of control: (1) process audits, (2) environmental monitors, (3) process monitors, (4) lot acceptance inspections, (5) process qualifications, and (6) process integrity audits. These methods of control, defined below, characterize visually and electrically the wafer fabrication operation.

Process Audit—Audits concerning manufacturing operator conformance to specification. These are performed on all operations critical to product quality and reliability.

Environmental Monitor—Monitors concerning the process environment, i.e., water purity, air temperature/humidity, and particulate count.

Process Monitor—Periodic inspection at designated process steps for verification of manufacturing inspection and maintenance of process average. These inspections provide both attribute and variables data.

Lot Acceptance—Lot by lot sampling. This sampling method is reserved for those operations deemed as critical and, as such, requiring special attention.

Process Qualification—Complete distributional analysis is run to specified tolerance averages and standard deviations. These qualifications are typically conducted on deposition and evaporation processes, i.e., epi, aluminum, vapox, and backside gold.

Process Integrity Audit—Special audits conducted on oxidation and metal evaporation processes (CV drift—oxidation; SEM evaluation—metal evaporation).

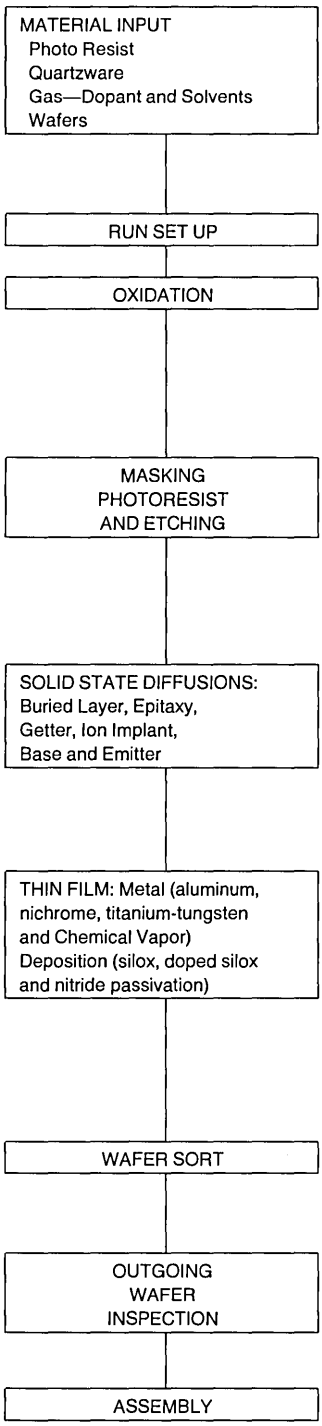
Data Reporting

Process quality control data is recorded on an attribute or variable basis as required; control charts are maintained on a regular basis. This data is reviewed at periodic intervals and serves as the basis for judging the acceptability of specific processes. Summary data from the various process quality control operations are relayed to cognizant line, engineering and management personnel in real time so that, if appropriate, the necessary corrective actions can be immediately taken.

Process Flow

Figure 8-1 shows the integration of the various methods of control into the wafer fabrication process flow. The process flow chart contains examples of the process quality controls and inspections utilized in the manufacturing operation.

Process Quality Control (Continued)



Process Controls (Examples)

- A. Environmental
- B. Chemical supplies
- C. Substrate examination (resistivity, flatness, thickness, crystal perfection, etc.)
- D. Photoresist evaluation
- E. Mask inspections

- A. Process audit

- A. Process audit/qualification
- B. Environmental
- C. Process monitors (thickness, pinhole and crack measurements)
- D. C V Plotting
- E. Calibration

- A. Process audits
- B. Environmental
- C. Visual examinations
- D. Photoresist evaluation (preparation, storage, application, baking, development and removal)
- E. Etchant controls
- F. Exposure controls (intensity, uniformity)

- A. Process audits/qualification
- B. Environmental
- C. Temperature profiling
- D. Quartz cleaning
- E. Calibration
- F. Electrical tests (resistivity, breakdown voltages, etc.)

- A. Process audits/qualification
- B. Environmental
- C. Visual examinations
- D. Epitaxy controls (thickness, resistivity cleaning, visual examination)
- E. Metallization controls (thickness, temperature cleaning, SEM, C V plotting)
- F. Glassivation controls (thickness, dopant concentration, pinhole and crack measurements)

- A. Process audit
- B. Environmental
- C. Visual examinations

- A. Process audit
- B. Inspection

FIGURE 8-1. Process Flow Chart

Quality Assurance

To assure that all product shipped meets both internal National specifications for standard product and customer specifications in the case of negotiated specs, a number of QA inspections throughout the assembly process flow *(Figure 8-2)* are required. A flow, much more detailed than the one presented in *Figure 8-2*, governs the assembly of the devices and the performance of the environmental, mechanical and electrical tests.

Reliability

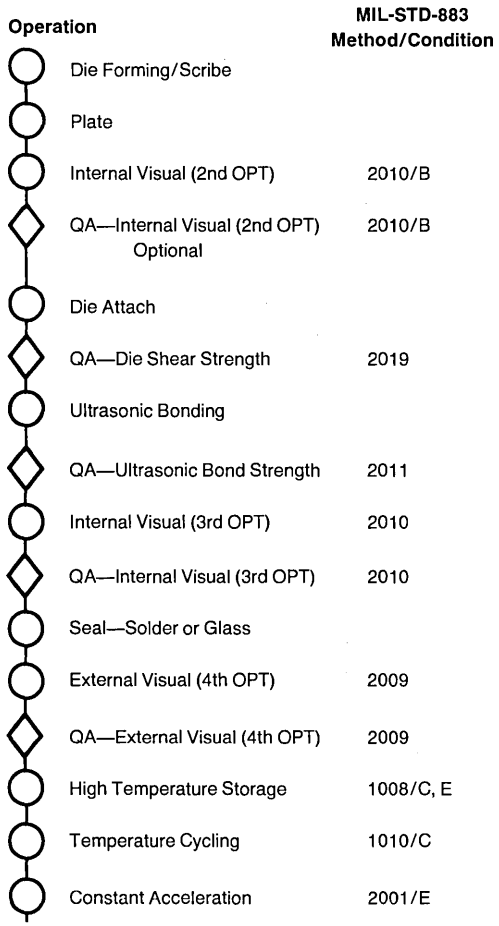
A number of programs, among them qualification testing, reliability monitoring, failure analysis, and reliability data collection and presentation, are maintained.

Qualification Programs

All products receive reliability qualification prior to the product being released for shipment. Qualification is required for (1) new product designs, (2) new fabrication processes or (3) new packages or assembly processes. Stress tests are run and the results are evaluated against existing reliability levels. These results must be better than or equal to current product for the new product to receive qualification.

New Product Designs—Receive, as a minimum, +125°C operating life tests. Readouts are normally scheduled at 168 hours, 1168 hours and 2168 hours. The samples stressed are electrically good units from initial wafer runs. Additional life testing, consisting of high-temperature operating life test, 85/85 humidity bias tests and bias pressure pot (BPTH) tests, may be run as deemed necessary. Redesigns of existing device layouts are considered to be new product designs, and full qualification is necessary.

New Fabrication Processes—Qualifications are designed to evaluate the new process against the current process. Stress tests consist of operating life test, high-temperature operating life test, 85/85 humidity bias test and/or biased



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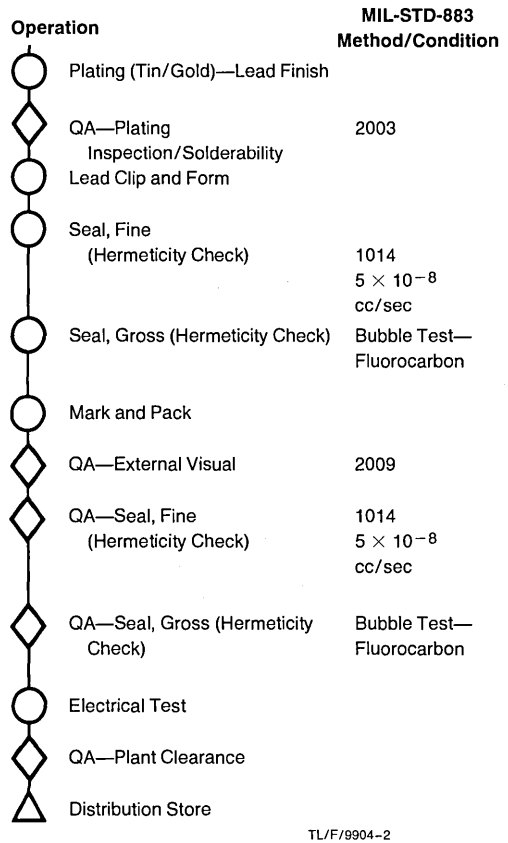

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FIGURE 8-2. Generalized Process Flow

Reliability (Continued)

pressure pot (BPTH) test. In addition, package environment tests may be performed. Evaluations are performed on various products throughout the development stages of the new process. Units stressed are generally from split wafer runs. All processing is performed as a single wafer lot up to the new process steps, where the lot is split for the new and the current process steps. Then the wafers are recombined, and again processed as a single wafer lot. This allows for controlled evaluation of the new process against the standard process. Both significant modifications to existing process and transferring existing products to new fabrication plants are treated as a new process.

New Packages or Assembly Processes—Qualifications are performed for new package designs, changes to existing piece parts, changes in piece part vendors, and significant modification to assembly process methods. In general, samples from three assembly runs are stressed to a matrix shown in Table 8-1. In addition, +100°C operating life tests, 85/85 humidity bias tests, biased pressure pot (BPTH) tests and unbiased pressure pot tests are performed.

Reliability Monitors

Reliability testing of mature products is performed to establish device failure rates, and to identify problems occurring in production. Samples are obtained on a regular basis from production. These units are stressed with operating life tests or package environmental tests. The results of these tests are summarized and reported on a monthly basis. When a problem is identified, the respective engineering group is notified, and production is stopped until corrective action is taken.

Current testing levels are in excess of 14,000 units per year stressed with operating life tests, and 23,000 units per year stressed with package environmental tests.

Failure Analysis

Failure analysis is performed on all units failing reliability stress tests. Failure analysis is offered as a service to support manufacturing and engineering, and to support customer returns and customer requested failure studies. The failure analysis procedure used has been established to provide a technique of sequential analysis. This technique is based on the premise that each step of analysis will provide information of the failure without destroying information to be obtained from subsequent steps. The ultimate purpose is to uncover all underlying failure mechanisms through complete, in-depth, defect analysis. The procedure places great emphasis on electrical analysis, both external before decapsulation, and internal micro-probing. Visual examinations with high magnification microscopes or SEM analysis are used to confirm failure mechanisms. Results of the failure analysis are recorded and, if abnormalities are found, reported to engineering and/or manufacturing.

Data Collection and Presentation

Product reliability is controlled by first stressing the product, and then feeding back results to manufacturing and engineering. This feedback takes two forms. There is a formal monthly Reliability Summary distributed to all groups. The summary shows current product failure rates, highlights problem areas, and shows the status of qualification and corrective action programs. Less formal feedback is obtained by including reliability personnel at all product meetings, which gives high visibility to the reliability aspects of various products. As a customer service, product reliability data is compiled and made available upon request.

TABLE 8-1. Package Environmental Stress Matrix

Test	MIL-STD-883	
	Method	Condition
GROUP B		
Subgroup 1 Physical Dimensions	2016	
Subgroup 2 Resistance to Solvents	2015	
Subgroup 3 Solderability	2003	Soldering Temperature of 260 ± 10°C
Subgroup 5 Bond Strength (1) Thermocompression (2) Ultrasonic or Wedge	2011	 (1) Test Condition C or D (2) Test Condition C or D
GROUP C		
Subgroup 2 Temperature Cycling Constant Acceleration Seal (a) Fine (b) Gross Visual Examination End-Point Electrical Parameters	 1010 2001 1014	 Test Condition C (−65°C to +150°C) Test Condition E (30 kg), Y_1 Orientation and X_1 Orientation Test Condition D (20 kg) for Packages over 5 gram weight or with Seal Ring Greater than 2 inches

Reliability (Continued)

TABLE 8-1. Package Environmental Stress Matrix (Continued)

Test	MIL-STD-883	
	Method	**Condition**
GROUP D		
Subgroup 1		
Physical Dimensions	2016	
Subgroup 2		
Lead Integrity	2004	Test Condition B2 (Lead Fatigue)
Seal	1014	As Applicable
(a) Fine		
(b) Gross		
Lid Torque	2024	As Applicable
Subgroup 3		
Thermal Shock	1011	Test Condition B (−55°C to +125°C) 15 Cycles Minimum
Temperature Cycling	1010	Test Condition C (−65°C to +150°C) 100 Cycles Minimum
Moisture Resistance	1004	
Seal	1014	
(a) Fine		
(b) Gross		
Visual Examination		
End-Point Electrical Parameters		
Subgroup 4		
Mechanical Shock	2002	Test Condition B (1500g, 0.5 ms)
Vibration, Variable Frequency	2007	Test Condition A (20g)
Constant Acceleration	2001	Same as Group C, Subgroup 2
Seal		
(a) Fine		
(b) Gross		
Visual Examination		
End-Point Electrical Parameters		
Subgroup 5		
Salt Atmosphere	1009	Test Condition A Minimum (24 Hours)
Seal	1014	As Applicable
(a) Fine		
(b) Gross		
Visual Examination		
Subgroup 6		
Internal Water-Vapor Content	1018	
Subgroup 7		
Adhesion of Lead Finish	2025	

Terminating F100K ECL Inputs

National Semiconductor
Application Note 682
The ECL Applications Staff

INTRODUCTION

Many F100K designs require that certain inputs be preset to a HIGH or LOW level. Because of the construction of the F100K input circuitry, a LOW can be realized by simply leaving the input OPEN. However, a HIGH must be terminated in a special way, as simply tying the input to V_{CC}/V_{CCA} is unacceptable.

DESIGN CONSIDERATIONS

The ranges of V_{IH} and V_{IL} across V_{EE} ($-4.2V$ to $-5.7V$ for F100K ECL 300 Series) are -870 mV to -1165 mV and -1475 mV to -1830 mV respectively.

By staying within these ranges, the input conditions are assured. *Figure 1* shows the voltage versus current for the F100K input transistor. If the input is tied to V_{CC}/V_{CCA} the input transistor saturates (Point D) which can damage internal circuitry. The best V_{IH} to realize a HIGH is a voltage drop of 0.9V below V_{CC}/V_{CCA}. As can be seen from the graph, this locates the quiescent point on the flat part of the curve (Point C) midway within the acceptable range of V_{IH}. *Figure 2* shows three ways in which a HIGH can be realized on the input. These circuits allow the user to maintain constant input signals at optimum levels of V_{EE} and temperature. Each circuit can handle multiple fanouts, the number depending upon the maximum current capability of the circuit. The designer should be aware that although *Figures 2A, 2B* and *2C* supply ECL compatible signal levels, they differ in power consumption and susceptibility to changes in temperature and V_{EE}.

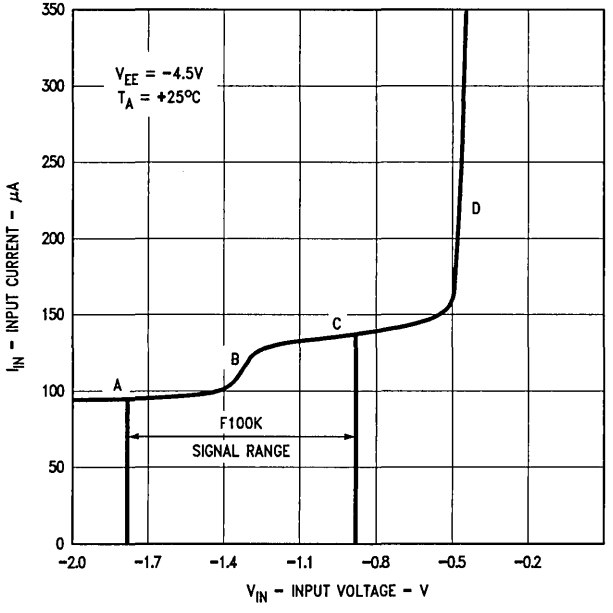
For designs where there are multiple unused inputs and extra logic gates available, fanout from the unused gates is possible. As an example of this, one gate of the 100302 is capable of driving ten quiescent inputs at voltage and current levels typical of F100K as shown in *Figure 3.*

Figure 4 shows, in more detail, the F100K pull-up scheme and the input circuitry. Although the circuits of *Figure 2* are good examples, a detailed circuit analysis must include the 50 kΩ input resistor. In *Figure 4A*, the resistor (R_D) which sets the diode biasing current is in parallel with the 50 kΩ input resistor. Likewise, the circuit of *Figure 4B* shows that R_2 is in parallel with the input resistor.

The point to emphasize is never tie an F100K input to V_{CC}/V_{CCA} in order to realize a HIGH preset. Instead, the following is recommended:

- For a LOW level—leave input open or tie to V_{EE}.
- For a HIGH level—tie input to a diode drop or 0.9V **below** V_{CC}/V_{CCA}.

Remember also that the 50 kΩ input resistor must be considered in the circuit parameter calculations.



A—50 kΩ Pull-Down Current
B—Transition (Switching) Region
C—Base Current plus 50 kΩ
D—Input Transistor Saturation

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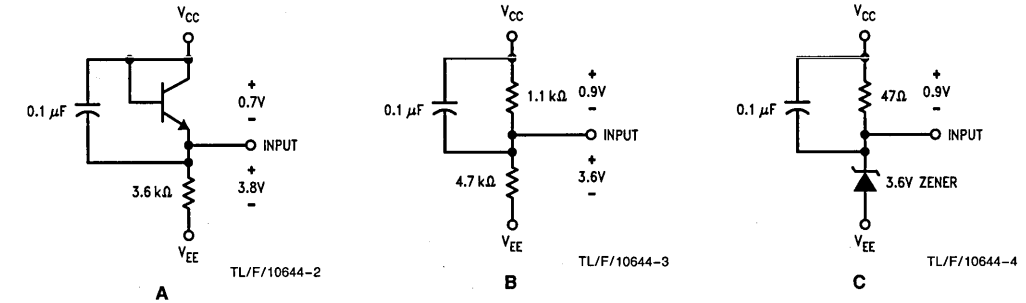
FIGURE 1. Input Characteristics



Note: Nominal values are shown.

FIGURE 2. Equivalent Circuits for HIGH Termination

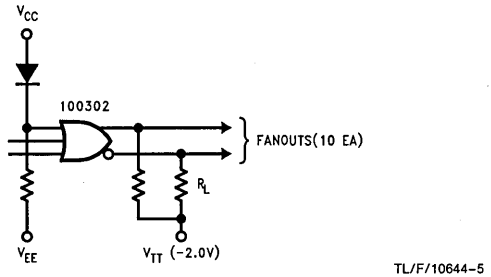


FIGURE 3. Utilizing Unused Gates to Terminate Multiple HIGHs and LOWs

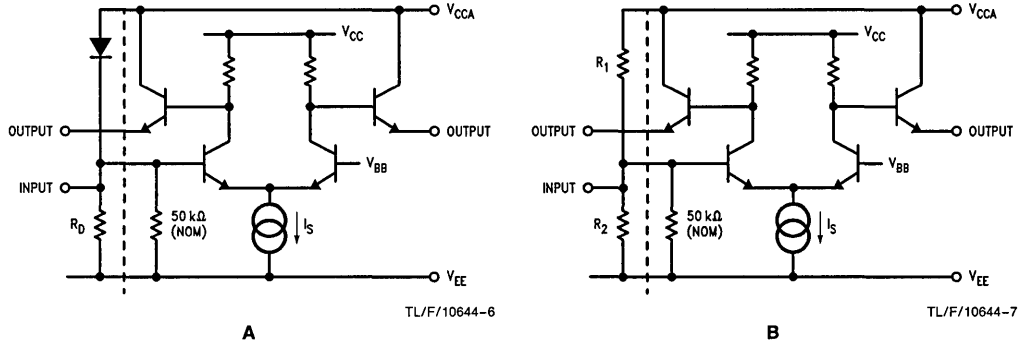


FIGURE 4. Pull-Up Circuit Examples

300 MHz Dual Eight-Way Multiplexer/Demultiplexer

National Semiconductor
Application Note 683
The ECL Applications Staff

INTRODUCTION

High speed multiplexing and demultiplexing is an integral part of the fast expanding telecommunications market, and can be used successfully in inter-computer and intra-computer wide-path communications. The National family of F100K ECL components provides an excellent solution to this design problem. This applications note describes a data transmission scheme that can transfer information at the rate of 75 Mbytes per second using only four twisted pair transmission lines.

Using 100341 8-Bit Shift Registers as parallel to serial and serial to parallel converters it is possible to design a simple mux/demux that can operate at speeds as high as 300 MHz *(Figure 1)*. The data to be multiplexed onto the transmission lines are applied as 16 bits (2 bytes) in parallel to the inputs of the 100341s where they are loaded into the registers under control of a synchronization pulse (SYNC). The mode of the 100341s is then changed to shift right and the data is transmitted on the output lines at the clock rate. When the last bit has been shifted out, the register is loaded with the next data to be transmitted.

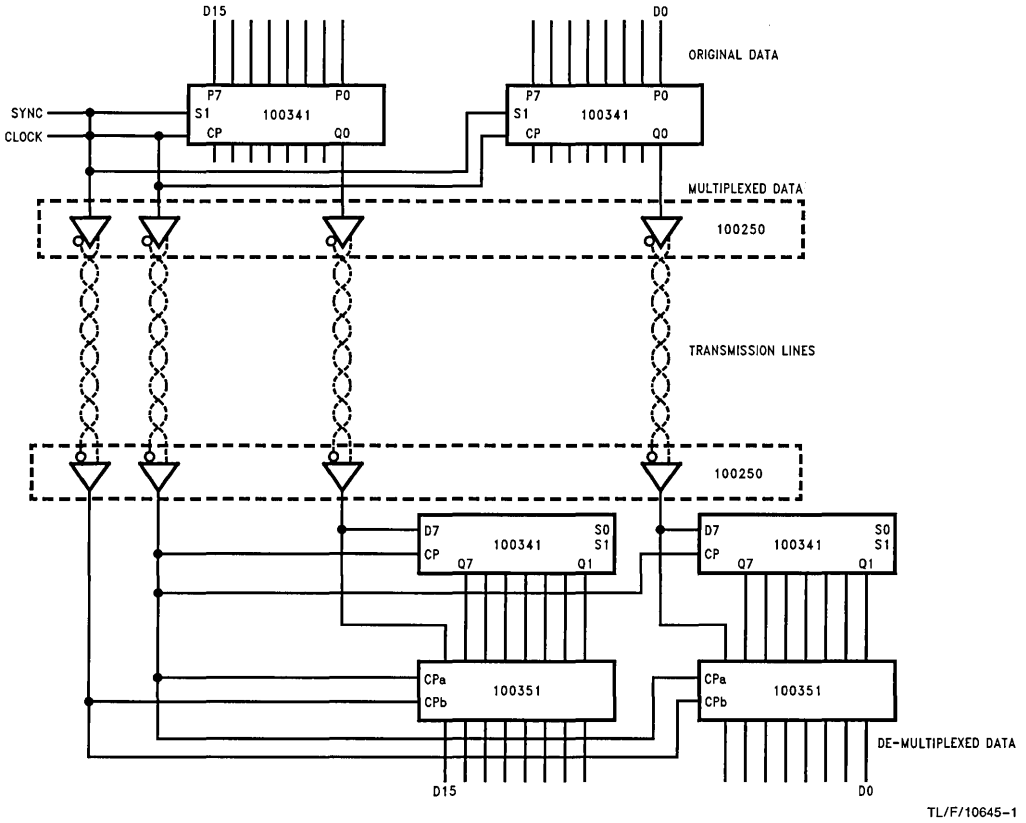


FIGURE 1. 300 MHz Dual Eight-Way Multiplexer/Demultiplexer

The clock signal (CLOCK) is a free-running 300 MHz square wave and the synchronization signal (SYNC) goes low for one clock cycle in every eight. These two signals are transmitted along with the data to facilitate synchronized reception at the other end.

At the receiving end, the 100341s are used as simple shift registers that accomplish the task of demultiplexing the data. The SYNC signal controls the loading of the 100351 receiver registers.

CLOCK AND SYNC GENERATION

The CLOCK signal in this application is a 300 MHz square wave generated with a voltage controlled oscillator coupled with a phase-locked loop. However, any available clock signal may be used at a frequency of DC to 300 MHz.

The SYNC signal is generated with the use of another 100341 connected as in *Figure 2*. This circuit is self starting, requiring no initialization for proper operation. When the SYNC signal is low, the data present at the parallel load inputs (P0–P7) are loaded into the register on the next clock pulse. When SYNC goes high (as a result of loading the high value on P0), the mode of the 100341 is changed to shift right and the low loaded from P7 is shifted across the 100341 and appears on the SYNC wire eight cycles later. This in turn causes the 100341 to load again and the cycle repeats. The SYNC signal is high for seven clock cycles and low for one cycle, allowing it to be used as the synchronization pulse for the mux/demux circuit.

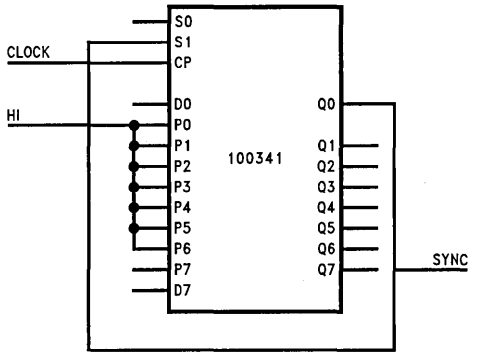


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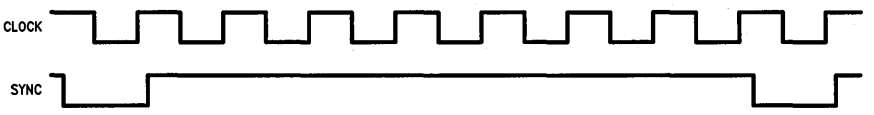
FIGURE 2. SYNC Pulse Generator

CLOCK AND SYNC WAVEFORMS



TL/F/10645–3

100336 Four-Stage Counter/Shift Register

National Semiconductor
Application Note 684
ECL Applications Staff

INTRODUCTION

Many system designs require bi-directional counting and shifting functions. In most cases these functions are separate and unique requirements within the system design. For this reason, separate catalog parts are available. In some cases however, there is a requirement to have a device that will allow both counting and shifting functions. This is especially true in arithmetic, timing, sequential, or communication applications. National offers a very versatile counter/shift register in the 100336. This application note describes its function in detail and offers some simple uses.

DESCRIPTION

The 100336 contains four synchronous, presettable flip-flops. Synchronous operation is provided by having all flip-flops clocked simultaneously so that all output changes coincide. This mode of operation eliminates counting spikes on the outputs which are normally associated with asynchronous counters. The clock input is buffered and triggers the four flip-flops on the rising (positive-going) edge.

The counters are fully programmable allowing the outputs to be set to either a HIGH (1) or LOW (0). As presetting is synchronous, setting low levels on the select inputs (S_0–S_2) (see Table I) disables the counter and causes the outputs to agree with the parallel inputs (P_3–P_0) on the next rising edge of the clock. Loading is accomplished regardless of the levels of the two enables ($\overline{CEP}$, $\overline{CET}$).

TABLE I. Function Select Table

S_2	S_1	S_0	Function
L	L	L	Parallel Load
L	L	H	Complement
L	H	L	Shift Left
L	H	H	Shift Right
H	L	L	Count Down
H	L	H	Clear
H	H	L	Count Up
H	H	H	Hold

The 100336 features both synchronous and asynchronous clear functions. The synchronous clear is performed by setting a binary five (101B) at the select inputs. On the next rising edge of the clock, the outputs will be forced LOW (0000) regardless of the levels at the enable inputs. A buffered asynchronous master reset (MR) is provided to clear all outputs LOW (0000) regardless of the levels of the clock, select, or enable inputs.

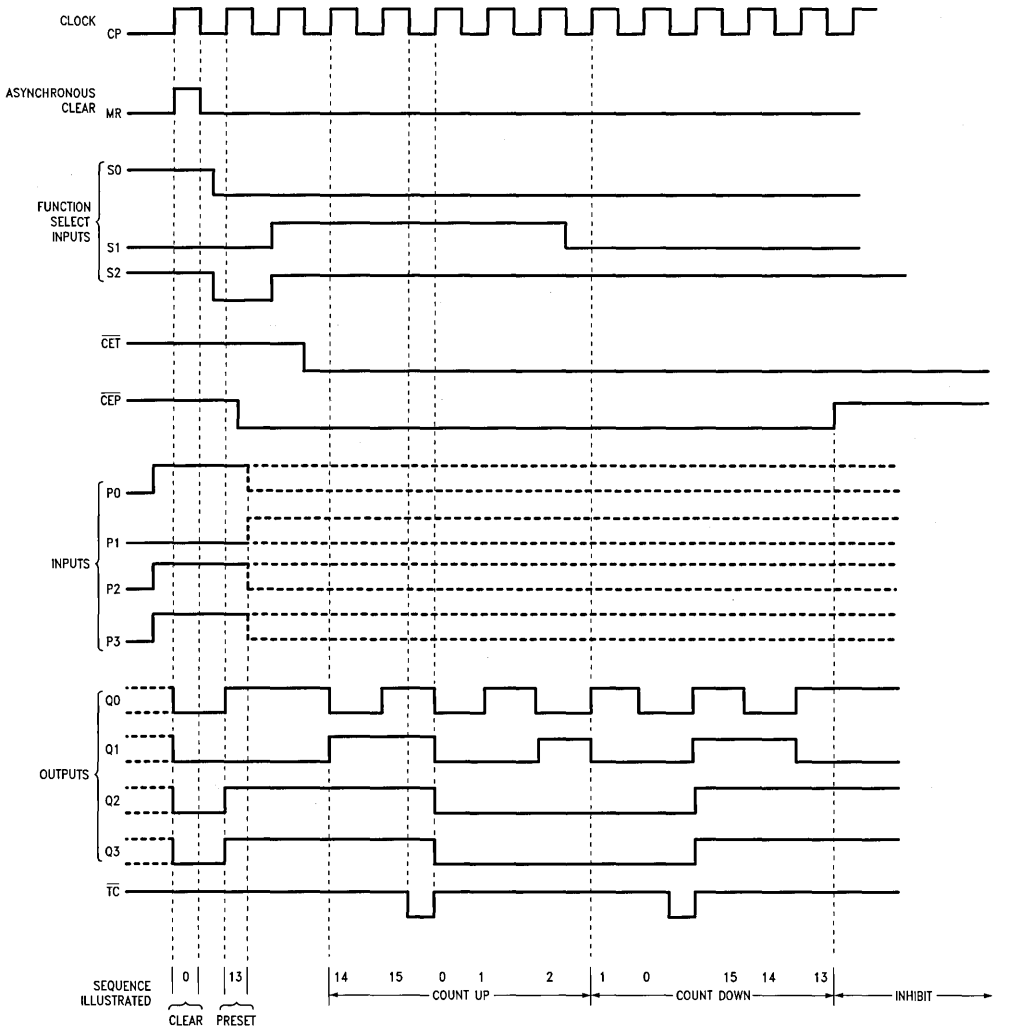
Count up/count down functions are selected with the select inputs (S_2–S_0). These are synchronous operations and the outputs will increment/decrement in value on the rising edge of the clock. Both count enable inputs ($\overline{CEP}$, $\overline{CET}$) must be true (LOW) to count. The terminal count output ($\overline{TC}$) becomes active-LOW when the count reaches zero in the DOWN mode or fifteen in the UP mode. Its duration is approximately equal to one period of the clock. The $\overline{TC}$ output is not recommended for use as a clock or synchronous reset for flip-flops. See *Figure 1* for timing relationships in UP/DOWN counting.

In simple ripple-carry cascading applications the terminal count $\overline{TC}$ is fed forward to enable the trickle enable ($\overline{CET}$) input. This method is increasingly inefficient as the counting chain lengthens. The upper limit of the clock frequency is determined by the clock-to-terminal-count delay of the first stage, the cumulative trickle-enable ($\overline{CET}$)-to-terminal-count delay of the intermediate stages, and the trickle-enable-to-clock delay of the last stage. For faster counting rates a carry-lookahead scheme is necessary. In this scheme the ripple delay through the intermediate stages commences with the same clock that causes the first stage to change over from MAX to MIN in the UP mode, or from MIN to MAX in the DOWN mode. Since the final count cycle takes 16 clocks to complete, there is ample time for the ripple to propagate through the intermediate stages. The critical timing that limits the counting rate is the clock-to-terminal-count of the first stage plus the parallel-enable-to-clock ($\overline{CEP}$) setup time of the last stage. *Figure 2* shows the connections for the fast-carry counting scheme.

TYPICAL CLEAR, LOAD, AND COUNT SEQUENCES

Illustrated below is the following sequence:

1. Clear outputs to zero.
2. Load (Preset) to binary thirteen.
3. Count up to fourteen, fifteen, carry, zero, one, and two.
4. Count down to one, zero, borrow, fifteen, fourteen, and thirteen.
5. Inhibit counting.



Note: A MR overrides enables, data, and count inputs.

FIGURE 1. 100336 Used as Binary Up/Down Counter

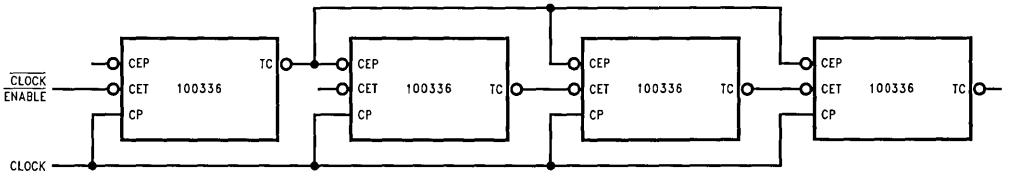


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FIGURE 2. Fast Carry Counting Scheme

Shift right/left modes are performed by making the appropriate selection on the selection inputs (S_2–S_0). Each rising edge of the clock will cause the outputs to shift once in the direction which is selected. For shift-left operation, input D_3 is used as the serial input. For shift-right operation, input $\overline{CET}/D_0$ is used as the serial input. During shift operation the terminal count output reflects the level at the Q_3 output and the enables are "don't cares". See *Figure 3* for shift operation timing relationships and shift sequences.

The 100336 provides two special modes of operation. The complement mode performs a one's complement of the outputs (Q_3–Q_0) on the rising edge of the clock input regardless of the levels at the enable inputs. The hold feature is asynchronous and simply stops counting or shifting operations. Both complement and hold are performed with proper selection of the select inputs. For a complete truth table of the 100336 operation, refer to Table II.

DESIGN CONSIDERTIONS

Presetting the parallel inputs (P_3–P_0) may require a mixture of HIGH's and LOW's. A LOW may be preset by leaving the respective input open as the 100336 has a 50 kΩ resistor to V_{EE} on the parallel inputs. A HIGH must never be made by tying the input to V_{CC}/V_{CCA}. This saturates the input transistor. Instead the input is set at a diode drop below V_{CC}/V_{CCA} for a preset HIGH. See Applications Note 682.

Unused output pairs ($\overline{Q}_n/Q_n$) may be left unterminated. However, unused single outputs should be terminated to balance current switching in the outputs. For further details on system design considerations refer to the *F100K ECL Design Guide.* For AC/DC performance specifications and critical timing parameters refer to the 100336 datasheet.

APPLICATIONS

Figures 4 and *5* demonstrate the use of the 100336 as UP/DOWN BCD counters. One additional gate is required to detect the limit count. Notice the alternate gate methods in *Figure 4.* The 100304 shows the classical AND/NAND design similar to TTL and the 100302 shows the OR/NOR design of ECL.

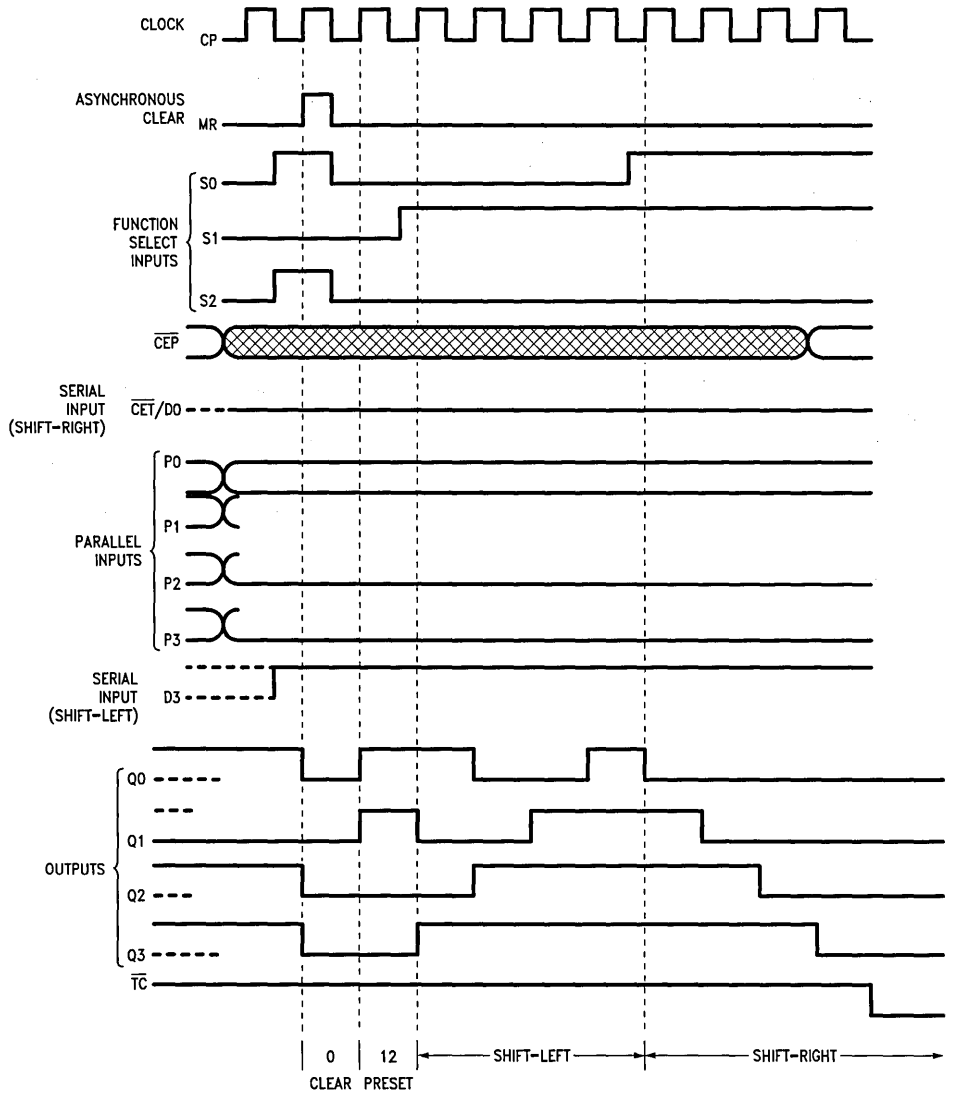
Figure 6 incorporates the use of a 100331 triple D-type flip-flop. By using one stage of the 100331, a 50/50 duty cycle can be realized from the divider.

An 8-bit parallel-to-serial shifter can be constructed by cascading two 100336's as shown in *Figure 7.* The third counter reloads another 8-bit data word after eight serial counts.

TYPICAL, CLEAR, LOAD, AND COUNT SEQUENCES

Illustrated below is the following sequence:

1. Clear outputs to zero.
2. Load (preset) to binary twelve.
3. Shift-left using D_3 as serial input.
4. Shift-right using $\overline{CET}/D_0$ as serial input.



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Note 1: In shift-right mode $\overline{TC}$ follows the Q_3 output.

Note 2: In shift-left mode $\overline{TC}$ follows the D_3 input.

Note 3: $\overline{CEP}$ is a "don't care" during shifting.

FIGURE 3. 100336 Used as Bi-Directional Shift Register

Truth Table

Q_0 = LSB

TABLE II. Truth Table

Inputs								Outputs					
MR	S_2	S_1	S_0	$\overline{CEP}$	$D_0/\overline{CET}$	D_3	CP	Q_3	Q_2	Q_1	Q_0	$\overline{TC}$	Mode
L	L	L	L	X	X	X	↗	P_3	P_2	P_1	P_0	L	Preset (Parallel Load)
L	L	L	H	X	X	X	↗	$\overline{Q}_3$	$\overline{Q}_2$	$\overline{Q}_1$	$\overline{Q}_0$	L	Invert
L	L	H	L	X	X	X	↗	D_3	Q_3	Q_2	Q_1	D_3	Shift Left
L	L	H	H	X	X	X	↗	Q_2	Q_1	Q_0	D_0	Q_3*	Shift Right
L	H	L	L	L	L	X	↗	(Q_0–Q_3) minus 1				①	Count Down
L	H	L	L	H	L	X	X	Q_3	Q_2	Q_1	Q_0	①	Count Down with $\overline{CEP}$ not active
L	H	L	L	X	H	X	X	Q_3	Q_2	Q_1	Q_0	H	Count Down with $\overline{CET}$ not active
L	H	L	H	X	X	X	↗	L	L	L	L	H	Clear
L	H	H	L	L	L	X	↗	(Q_0–Q_3) plus 1				②	Count Up
L	H	H	L	H	L	X	X	Q_3	Q_2	Q_1	Q_0	②	Count Up with $\overline{CEP}$ not active
L	H	H	L	X	H	X	X	Q_3	Q_2	Q_1	Q_0	H	Count Up with $\overline{CET}$ not active
L	H	H	H	X	X	X	X	Q_3	Q_2	Q_1	Q_0	H	Hold
H	L	L	L	X	X	X	X	L	L	L	L	L	Asynchronous Master Reset
H	L	L	H	X	X	X	X	L	L	L	L	L	
H	L	H	L	X	X	X	X	L	L	L	L	L	
H	L	H	H	X	X	X	X	L	L	L	L	L	
H	H	L	L	X	L	X	X	L	L	L	L	L	
H	H	L	L	X	H	X	X	L	L	L	L	H	
H	H	L	H	X	X	X	X	L	L	L	L	H	
H	H	H	L	X	X	X	X	L	L	L	L	H	
H	H	H	H	X	X	X	X	L	L	L	L	H	

① = L if Q_0–Q_3 = LLLL
H if Q_0–Q_3 ≠ LLLL

② = L if Q_0–Q_3 = HHHH
H if Q_0–Q_3 ≠ HHHH

H = HIGH Voltage Level

L = LOW Voltage Level

X = Don't Care

↗ = LOW-to-HIGH Transition

*Before the clock, $\overline{TC}$ is Q_3
After the clock, $\overline{TC}$ is Q_2

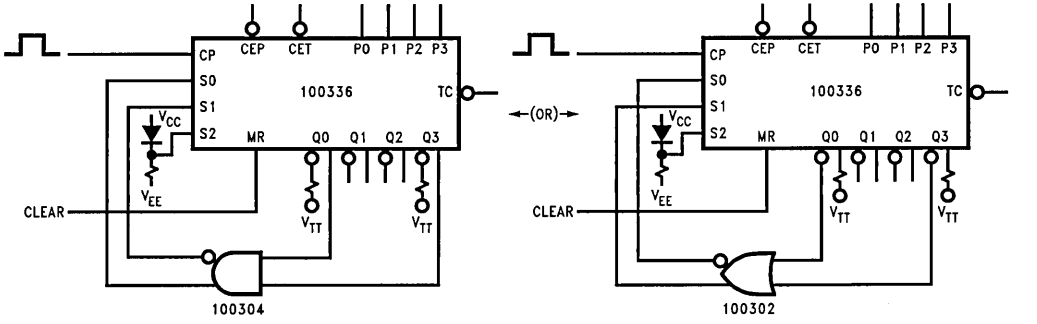

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FIGURE 4. BCD Up Counter (0–9)

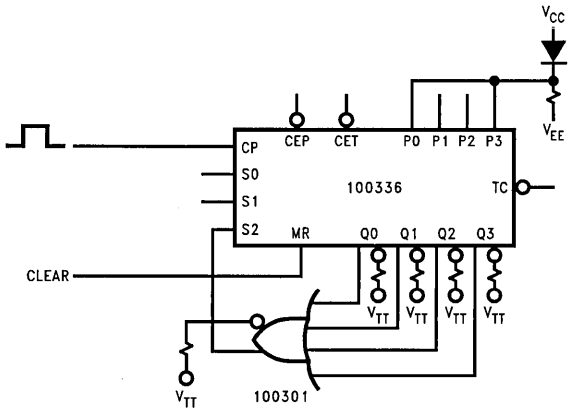

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FIGURE 5. BCD Down Counter (9–0)

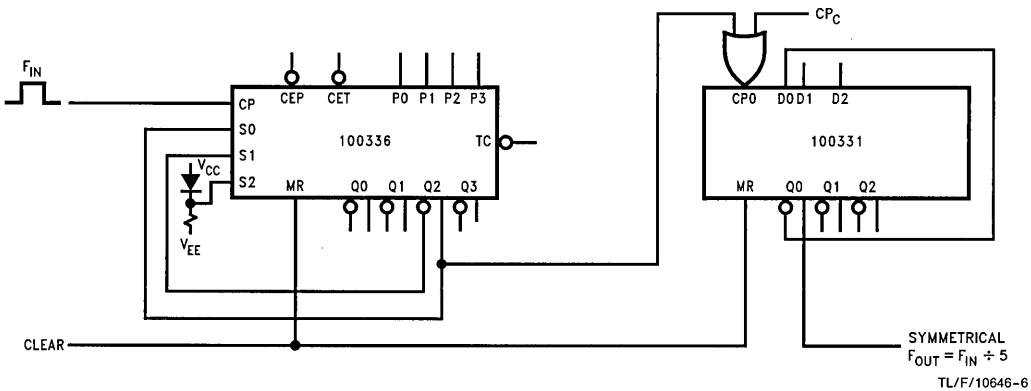

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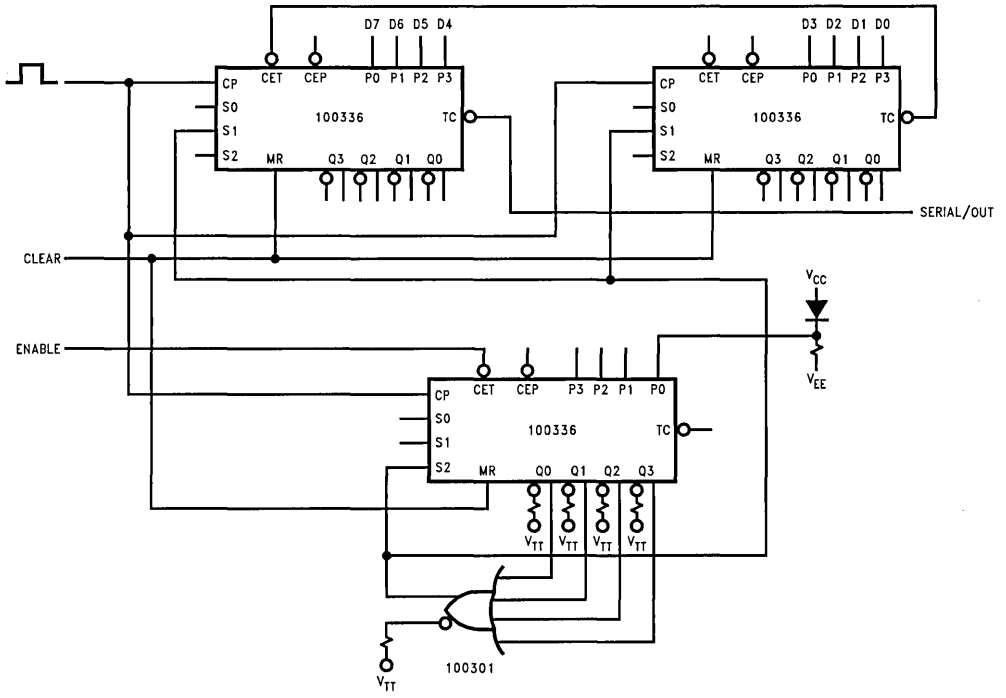
FIGURE 6. Divide by Five



TL/F/10646–7

FIGURE 7. 8-Bit Shift Left

ECL Backplane Design

National Semiconductor
Application Note 768
Doug Bush
Applications Engineer

INTRODUCTION

Designers are constantly trying to improve the performance of their systems. In many applications, this can be accomplished by increasing the speed of the system backplane. As system bandwidth requirements exceed 50 MHz, ECL is the logic of choice over TTL. ECL devices are designed for transmission line applications which means that ringing, reflections, and noise are minimized. These problems are not easily handled with TTL devices. ECL devices are the fastest in common use today and have increased steadily in popularity over the past 10 years with the additional speed requirements of many systems. With this popularity have come improvements such as increased reliability, power reduction, and better ESD protection.

ECL devices today offer the flexibility of single-ended or differential backplanes. National Semiconductor has responded to the increasing need for ECL backplanes by introducing octal registers, latches and translators. The registers and latches offer the flexibility to drive a 25Ω (with cutoff) or 50Ω load impedance. The 25Ω drivers are intended to drive a 50Ω transmission line which is doubly terminated in its characteristic impedance, or a single low impedance 25Ω line. Considerations such as transmission line media (microstrip, stripline, coaxial, twisted pair, etc.) terminations, connectors, power planes and loading effects must all be understood to design the optimum system.

ECL/TTL PERFORMANCE PARAMETERS

There are several advantages associated with using ECL. ECL is a non-saturating logic, as opposed to TTL, which results in much faster switching speeds for drivers tied to the backplane. The ECL circuit contains a differential amplifier with its outputs being a function of the difference between two input voltages; where one is a reference voltage (V_{BB}) and the other (V_{IN}) is a logic HIGH or LOW (see *Figure 1*). The differential inputs determine which path the constant current (I_S) will flow. An internal reference circuit establishes a stable V_{BB} voltage of −1.32V. When a LOW level (−1.730V typical) signal is applied to V_{IN}, Q1 "cuts off". Transistor Q2 is turned on with collector current through the Q2 branch being supplied by the current source (I_S). This sets up a LOW level on **A** and a HIGH level on the compliment output as long as the output is properly terminated.

A HIGH level (−0.970V typical) applied to V_{IN} will then turn on Q1 and "cutoff" Q2. This will set up a HIGH voltage level on **A** and a LOW level on its compliment. Since the current is nearly constant at all times, even during switching, current spikes are minimized on the power supply. This is an important feature of ECL (unlike TTL) because the power requirement is unaffected by frequency. ECL becomes more favorable at frequencies above 50 MHz with a 50% duty cycle. The outputs of ECL devices require typically an external termination resistor and termination voltage (V_{TT}) to develop the proper output voltage levels.

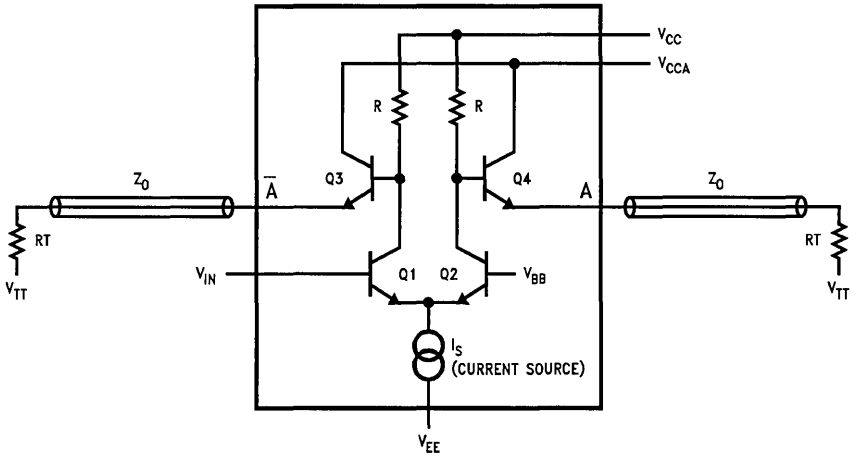


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FIGURE 1. ECL Gate

ECL outputs are perfectly suited to drive transmission lines. With an output impedance of 6Ω to 8Ω and rise times less than 1 ns, reflections are minimized resulting in a clean signal.

A comparison of the approximate input and output capacitance values for non-I/O IC's shows that TTL devices generally run higher than ECL devices. These parameters are important because they in part determine the amount of loading that will be present on the backplane. With reduced loading on the backplane comes increased speed.

	ECL (PCC)	TTL (PDIP)
Input Capacitance	3.0 pF	5.0 pF
Output Capacitance	3.0 pF	5.0 pF

ECL also has the ability to drive low impedance transmission lines (i.e., 25Ω). As the transmission line impedance decreases, the speed of the transmitted signal increases. The lower impedance also reduces the effects of noise. The National Semiconductor F100K 300 Series octal devices were specifically designed for this type of application.

ECL TERMINAL SCHEMES

Parallel Termination

Termination of ECL outputs can be accomplished in several different ways. The most common way is to terminate the emitter follower output in the transmission line characteristic impedance (Z_O) to a V_{TT} voltage of −2.0V as shown in *Figure 1*. This method is used with $Z_O = 50\Omega$) to set specifications for most of the F100K 300 Series devices.

Thevenin Termination

The Thevenin equivalent termination method (shown in *Figure 2*) requires one resistor be connected between the end of the line to be terminated and the V_{CC} rail, with another placed between the end of the line and the V_{EE} supply. This method will of course eliminate the need for a −2.0V V_{TT} supply, but the penalty is that the power dissipated will increase nearly eight times from the previous method. Several designers avoid this method for exactly that reason.

Series Termination

An alternate way to terminate the output is by a series termination scheme. With this arrangement, a resistor pair is placed directly at the output of the driver (shown in *Figure 3*). The series damping resistor (RS) should be chosen such that;

$$Z_O = RS + R_{OUT}$$

where: Z_O = characteristic impedance of the transmission line

R_{OUT} = output resistance of the gate

RS = series damping resistor

The value of R_{OUT} for the F100K 300 Series devices is 6Ω when the output is conditioned to a HIGH level, and 8Ω when conditioned to a LOW level. An average value of 7Ω is used when calculating the value of RS. The RE resistor in this termination scheme is used to discharge the line when the driven output goes into a low condition. To ensure that the proper amount of current needed is available, RE is chosen by the formula:

$$RE < Z_O\,[(V_{OH} - V_{EE})/0.49] - RS - Z_O$$

The table (shown in *Figure 3*) gives the resistor values of RS and RE max for V_{EE} = −4.5V) needed for several different characteristic impedance transmission lines.

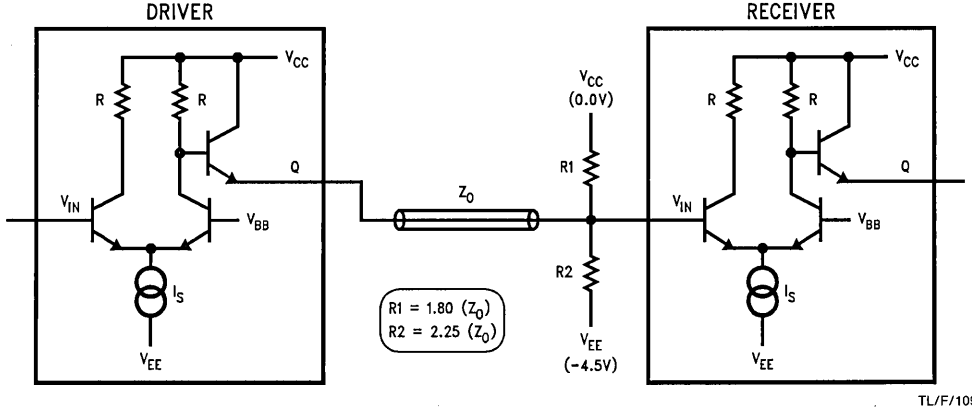

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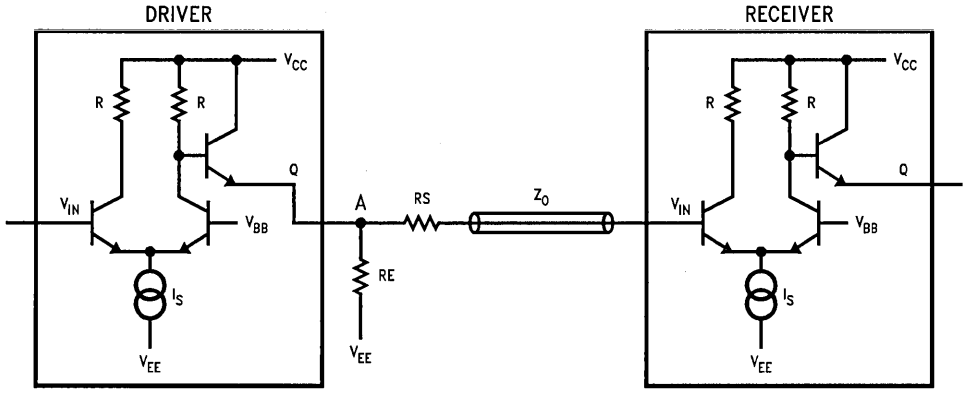
FIGURE 2. Thevenin Termination



TL/F/10910–3

Z_O Ohms	RS Ohms	RE Ohms
50	43	269
75	68	404
100	93	542
120	113	661

FIGURE 3. Series Termination Scheme

The advantages of the series termination method is that an additional V_{TT} supply is not required (unlike parallel termination), and all reflections back to the driver are absorbed by the series resistor (RS). This makes series termination ideal for situations in which ringing and overshoots are present on the transmission line. A voltage divider action occurs at the beginning of the transmission line (marked **A** in *Figure 3*) which means that only half the amplitude of the driver output will be present along the line until the signal reaches the end of the transmission line. For this reason, loads should not be distributed along the line. For parallel and thevenin terminations, the full amplitude is seen on the line at all times.

Although there are other termination schemes available, the ones discussed above are the easiest, cost effective and most popular.

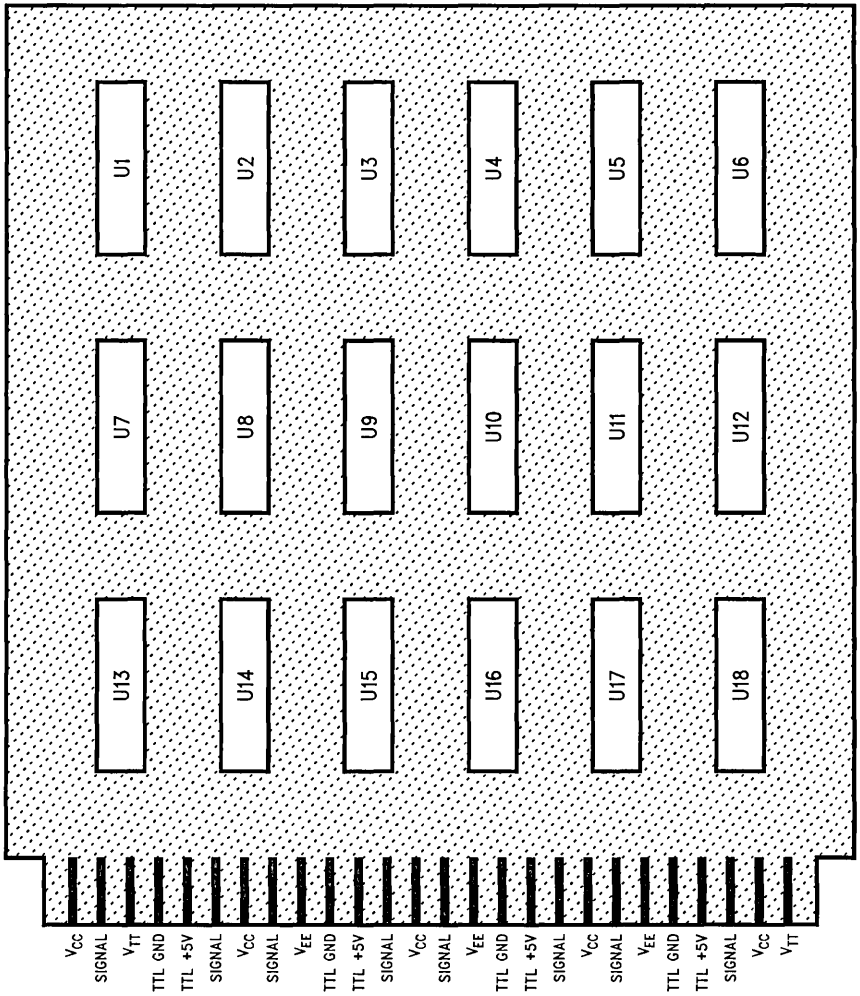
BOARD DESIGN CONSIDERATIONS

As with any good design, transmission line media, power/ground distribution, connectors, board layout, decoupling, and thermal effects must all be considered.

When designing a backplane with F100K 300 Series ECL logic, a controlled impedance transmission line is recommended. If the transmission line characteristic impedance is not matched along the line, reflections will occur. Available transmission line media include microstrip, stripline, coax, ribbon cable, and twisted pair to name a few. The most popular transmission line media for ECL is microstrip and stripline. Stripline is embedded within the layers of the PC board between two ground layers, while microstrip is run on the top and/or bottom layers of the board. Microstrip and stripline enable the designer to have very accurate and controlled impedances. This becomes important when determining delays and terminations within a designed system. It is important to remember that all transmission line types mentioned have a distinct propagation delay/unit length associated with them. As an example, microstrip lines on G10/FR4 boards have a propagation delay of approximately 1.77 ns/ft.

In order to transfer ECL signals from one board to another, a connector is needed. In most cases, the connector will cause impedance discontinuities. In order to keep reflections and signal distortions at a minimum, the discontinuity should be as small as possible. Although impedance matched connectors are expensive, the distortions that result are nearly negligible. Connectors also have a capacitance associated with them on the order of 1 pF–3 pF. This capacitance will of course have a direct effect on the backplane loading. When using edge connectors to interface data from a motherboard and a daughter card, several pins (>10%) should be dedicated to power and ground in order to maintain signal and power fidelity from one board to another. An example of this is shown in *Figure 4*.

When using a PC board with ECL and TTL logic together, the most noise will generally be found at the TTL ground. Since ECL logic levels are referenced directly from the V_{CC} line, it is critical to have a dedicated ECL V_{CC} plane that is stable and noise free. For this reason, the TTL ground and ECL V_{CC} planes are placed as far from each other as possible. Variations on V_{TT} and V_{EE} are more tolerable. *Figure 5* shows a typical layout for an eight layer TTL/ECL PC board. Signals are run on both sides of the board for ease of connecting signals.



TL/F/10910–4

FIGURE 4. PC Board Pin Distribution

LAYER 1	Signal
LAYER 2	TTL Ground
LAYER 3	TTL +5V
LAYER 4	V_{TT}
LAYER 5	Signal/Thermal
LAYER 6	ECL −4.5V (V_{EE})
LAYER 7	ECL 0.0V (V_{CC})
LAYER 8	Signal

FIGURE 5. PC Board Power Planes

Inductance is always present in any conductor. As the rate of change in current through an inductor increases, the greater the induced voltage will be since V = L(dI/dt). With digital systems changing logic levels, a change in current will inevitably occur and produce unwanted voltage drops. Oscillations are also connected with additional inductance present in digital circuits. This implies that inductance in board design should be kept at a minimum.

Inductance is very dependant on geometry, with solid sheet conductors being the best for keeping inductance at the lowest possible level. This is the reason why planes (as in *Figure 5*) instead of grids, combs, or traces are used for power and ground. It is best to mount IC's directly over ground planes and connect the device ground pins to it whenever possible. It is also recommended that decoupling capacitors of 0.01 μF to 0.01 μF be placed between V_{EE} and V_{CC}, and between V_{TT} and V_{CC}.

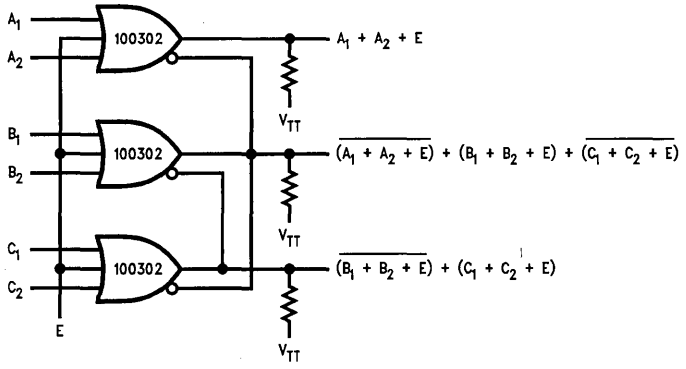
The power required for different IC's will vary, meaning that the heat dissipated by each will change. In order to maintain gate junction temperatures, cooling devices may be necessary. As an example, planes can be used as thermal mass resulting in an effective heat sink. Cooling is important because if junction temperatures exceed manufacturer specifications, circuits can fail, degrade, or function incorrectly.

SYSTEM DESIGN CONSIDERATIONS

Wired-OR Configuration

F100K 300 Series devices have an emitter follower configuration on each output. The open emitter outputs of several devices can be tied together to create a Wired-OR configuration. An example of this is shown in *Figure 6*. This configuration has the advantage of obtaining the OR operation without using an external gate, thus reducing the package count of the design. The Wired-OR also saves on power by reducing the number of terminations needed (one termination for each Wired-OR grouping), and increases the speed of the system by removing the additional propagation delay that would have been inherent with an additional OR gate. Since ringing and undershoots are functions of the transmission line intrinsic capacitance and inductance, it is important to minimize these by using the shortest trace lengths possible.

Although the Wired-OR allows for additional levels of logic, there is a penalty. This penalty is a reduction in the LOW level noise margin. As the number of outputs tied together increases, the V_{OL} level rises significantly. With a single output in the LOW state of approximately $-1.70V$ driving a 50Ω impedance terminated in $-2.0V$, a typical I_{OL} current of 6.0 mA flows. In the Wired-OR state with four outputs tied together (all in the LOW state), the I_{OL} current supplied by each output is nearly equal. The decreased current being supplied by each output transistor due to current sharing results in a reduction of the V_{BE} junction voltage which in turn raises the V_{OL} level. As a rule of thumb, the V_{OL} level will be raised approximately 25 mV for every two outputs that are tied together on a bus. It should also be mentioned that the V_{OH} levels will rise as the number of outputs tied together increases and thus the high level noise margin increases. This effect is usually ignored since V_{OH} is moving away from the threshold.



TL/F/10910–5

FIGURE 6. Wired-OR Configuration

Cutoff Drivers

The V_{OL} noise margin degradation found in Wired-OR networks can be avoided by using Nationals octal cutoff driver devices. When the output enable (see *Figure 7*) of the cutoff driver is brought to a HIGH level, the base of the output transistor is biased to a level of −1.5V to −1.6V which in turn "cuts it off". This implies that a cutoff output will not source any current. With this, the HIGH and LOW level noise margins will not change from the non Wired-OR situation. With the output in the cutoff state, an output capacitance of 3 pF is present on the backplane.

Loading Effects

As the number of devices tied to the backplane increases, distributed loading effects due to gate input and output capacitance need to be considered. The additional capacitance on the backplane reduces the effective characteristic impedance of the transmission line. This change indicates that in order to avoid reflections and terminate the line properly, a new terminating resistor needs to be calculated. The characteristic impedance for a lossless transmission line is calculated by:

$$Z_O = \sqrt{(L_O/C_O)}$$

Where: L_O = intrinsic inductance/unit length
C_O = intrinsic capacitance/unit length
C_D = distributed capacitance

With the effects of distributed loading on the transmission line, the effective characteristic impedance becomes:

$$Z'_O = \sqrt{(L_O/(C_O + C_D))} = Z_O \div \sqrt{(1 + C_D/C_O)}$$

As an example, consider the distributed loading scheme shown in *Figure 8*. A 50Ω microstrip line, 10 inches long, on glass epoxy board (Er = 5.0), is used as the transmission line with five equally spaced distributed loads.

$$C_O = t_{PD}/Z_O = 0.148 \text{ ns/inch} \div 50\Omega = 2.96 \text{ pF/inch}$$

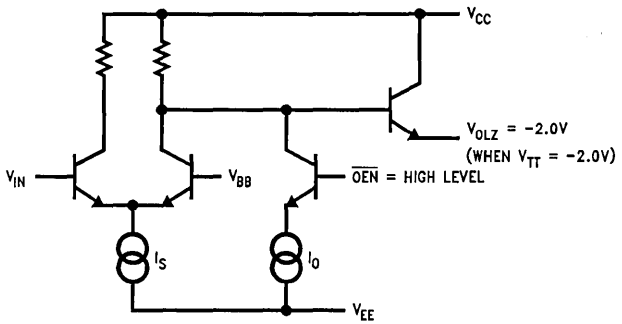
With an input impedance of approximately 3.0 pF/gate (for PLCC devices);

$$C_D = Z_O \div \sqrt{(1 + C_D/C_O)} = 5 \text{ (3.0 pF)/10 inches} = 1.5 \text{ pF/inch}$$

This gives an effective transmission line impedance of

$$Z'_O = Z_O \div \sqrt{(C_O + C_D)} = 50 \div \sqrt{(1 + (1.5/2.96))} = 40.7\Omega$$

This implies that in order to terminate the transmission line properly, a terminating resistor (RT) of 40Ω is required.



TL/F/10910–6

FIGURE 7. ECL Cutoff Driver

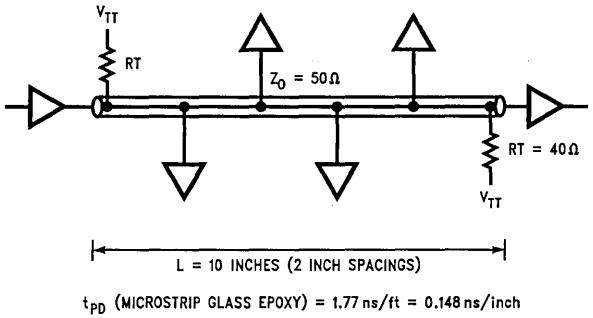


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FIGURE 8. Distributed Loading Example

APPLICATION EXAMPLES

In order to transfer data efficiently on an ECL backplane, ECL drivers receivers, translators, and transceivers are required. Single ended ECL backplane devices include the following:

- 100328 Octal ECL/TTL Bidirectional Translator with Latch
- 100329 Octal ECL/TTL Bidirectional Translator with Register
- 100343 Octal Latch (50Ω drive)
- 100344 Octal Latch with Cutoff Drivers (25Ω drive)
- 100352 Octal Buffer with Cutoff Drivers (25Ω drive)
- 100353 Octal Register (50Ω drive)
- 100354 Octal Register with Cutoff Drivers (25Ω drive)

Differential ECL backplane devices include the following:

- 100314 Quint Differential Line Receiver
- 100316 Quad Low Skew Differential Cutoff Driver (25Ω drive)
- 100319 Hex Single-Ended Input, Differential Output Cutoff Driver (25Ω drive)
- 100324 Hex TTL-to-ECL Translator
- 100325 Hex ECL-to-TTL Translator
- 100397 Quad Differential ECL/TTL Bidirectional Translator/Driver with Cutoff (25Ω drive)
- 100398 Quad Differential ECL/TTL Bidirectional Translator/Driver with Cutoff (25Ω drive), with TTL Control

Single-Ended ECL Backplane

A single-ended ECL backplane implies that signals are transmitted as a voltage on a single line referenced to AC ground. In the example shown in *Figure 9*, several listeners and talkers are tied to the common backplane. The 50Ω transmission line is terminated at both ends of the line in its characteristic impedance of 50Ω. This, in effect, requires a 25Ω driver. This need is satisfied with National Semiconductors 100344 octal latch with 25Ω cutoff drive, 100352 octal buffer with 25Ω cutoff drive, and the 100354 octal register with 25Ω cutoff drive. When designing such a system, the effects of connectors, transmission line delay, and load capacitance should all be considered as discussed previously.

Differential ECL Backplane

A single-ended backplane is susceptible to ground potential differences at the ends of the line thus creating distorted signals being transmitted or received. For this reason, a single-ended backplane is not recommended for noisy environments. Differential line driving (as shown in *Figure 10*) has a high noise rejection which results in a more reliable data transmission. Common mode voltages of $\leq -2.0V$ are rejected with an input voltage differential of 150 mV required for full output swing. (Please refer to V_{CM} specification for the 100314 in the F100K ECL Databook.)

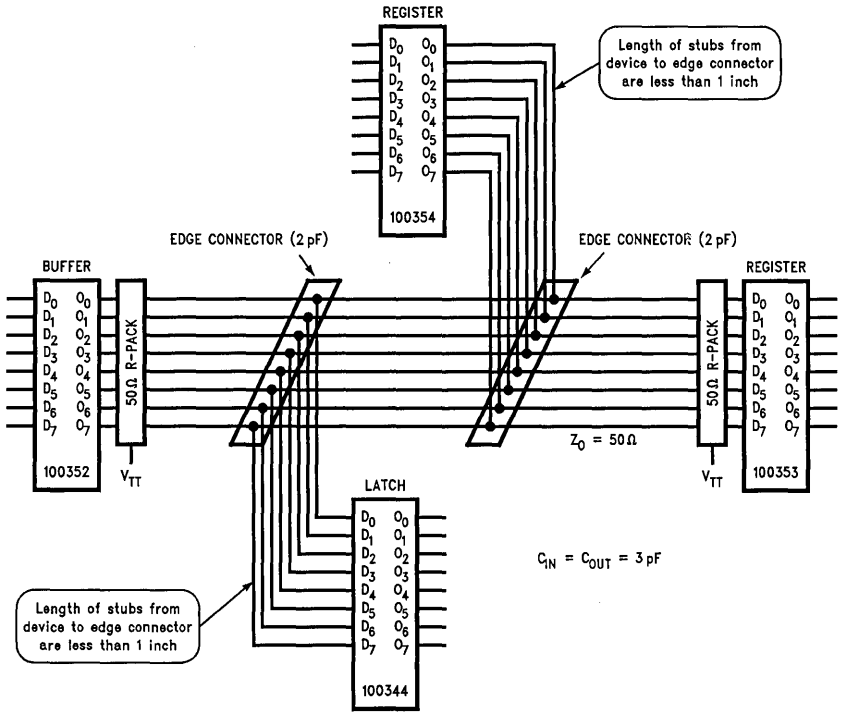

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FIGURE 9. Single-Ended ECL Backplane

The differential line driver and receivers communicate over a pair of wires where one is a HIGH voltage level and the other must be a LOW. If external noise occurs near the differential line, both wires will obtain the same distortions. Since the noise present on both of the lines is the same, the signal received at the terminated end of the line will not be effected because it is obtained by the difference of the signals on the lines. The difference of two lines will be the same with or without the noise problem.

The advantage of a differential line driving scheme is the clean transmission of signals in noisy or industrial environments. As the differential line driving application in *Figure 10* shows, in order to isolate unused outputs from the line 25Ω cutoff drivers are required. With the introduction of National Semiconductors 100316 quad differential 25Ω cutoff driver, 100319 hex single-ended input, differential output 25Ω cutoff driver, and 100397/100398 ECL/TTL quad bidirectional translators/drivers with latch and ECL 25Ω cutoff drive, this type of application is now possible. The 100397 has ECL control pins while the 100398 offers TTL control pins.

ECL Transceiver

Although an ECL transceiver does not currently exist, creating one is rather simple when using 25Ω cutoff driver devices as shown in *Figure 11*. This device could be used to communicate between a single-ended or differential ECL bus and other circuitry. The circuit shown uses two 100352 devices configured to give a transceiver operation. The function table for the operation of the transceiver is shown in *Figure 11*. In order to transmit data from A to B, $\overline{OEN}_2$ is HIGH while $\overline{OEN}_1$ is LOW. The HIGH level on $\overline{OEN}_2$ "cuts off" the bottom driver and allows for data transfer from A to B. To transfer data from B to A, $\overline{OEN}_1$ is held HIGH with $\overline{OEN}_2$ at a LOW level. When both output enable pins are at a HIGH level, both 100352 devices are in the cutoff state which results in a lower than low V_{OLZ} state (V_{OLZ} = −2.0V) at points A and B.

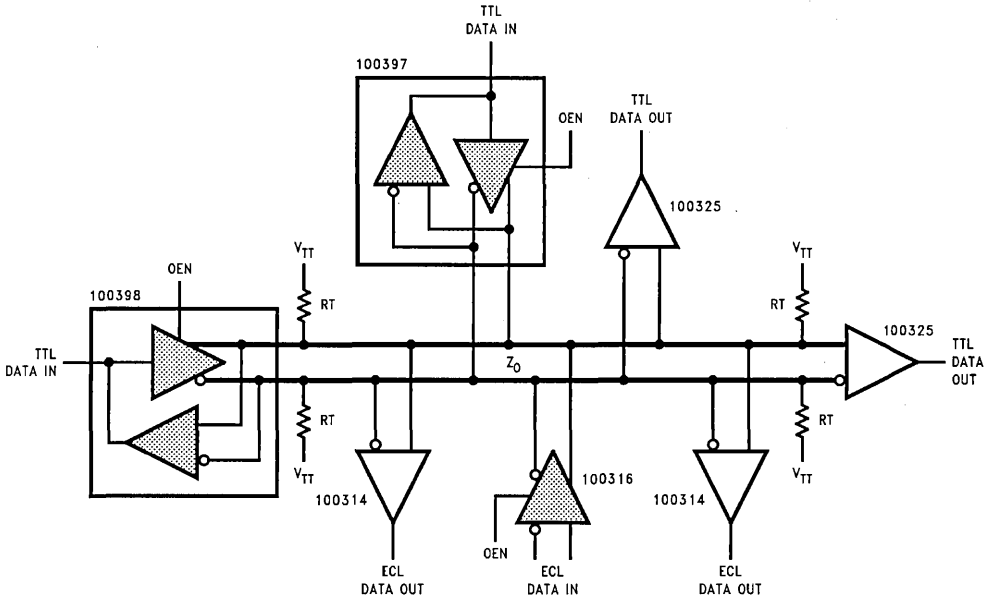

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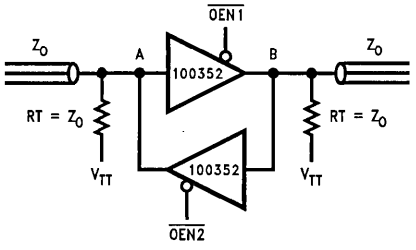
FIGURE 10. Differential ECL Backplane (1-Bit)



Truth Table

$\overline{OEN}_1$	$\overline{OEN}_2$	Outputs
L	L	A, B HIGH
L	H	Bus A Data to Bus B
H	L	Bus B Data to Bus A
H	H	A, B, Cutoff (V_{OLZ})

TL/F/10910–10

FIGURE 11. ECL Transceiver

Operating ECL from a Single Positive Supply

National Semiconductor
Application Note 780
John Davis

INTRODUCTION

ECL is normally specified for operation with a negative V_{EE} power source and a negative V_{TT} termination supply. This is the optimum operating configuration for ECL but not the only one. Operating ECL from a positive V_{CC} supply is a practical alternative that is gaining in popularity. Positive referenced ECL, or PECL as it is referred to, has been implemented in various mixed signal ASIC for use in the Video Graphics and Communications fields and is used in clock distribution as well. New single supply translator chips are becoming available to facilitate the interface of PECL logic levels to TTL and back again. Logic designers who strive for maximum speed in a system, now can easily replace sections of TTL logic with ECL and operate in PECL fashion from the common TTL V_{CC} supply.

STANDARD NEGATIVE SUPPLY ECL OPERATION AND WHY

Figure 1 shows F100K logic elements operating in standard negative supply ECL configuration. The most positive potential is the primary voltage reference for ECL operation. Standard ECL input and output levels are therefore negative potentials referenced to the stable passive Ground (0V). The inherent F100K voltage compensation permits stable input and output levels over a broad range of V_{EE}'s; i.e., −4.2 to −5.7 VDC for 300 Series F100K. Thus ECL logic operating from a −4.2V V_{EE} is compatible to logic operating from a −5.7V supply assuming both are referenced to a common 0V Ground.

Since ECL logic outputs only source currents that originate from the potential applied to its V_{CC}/V_{CCA} pins, the use of a 0V low impedance and low inductance ground potential is the optimum choice for operation. The use of a continuous copper ground plane as the primary ECL reference is the ideal source for the high frequency transient currents demanded by the logic during switching. Note that despite the ideal nature of a ground plane as the primary ECL reference, when mixing TTL (or other noisy circuitry) into ECL systems, the recommendation is to reference the TTL to a separate ground plane. This is to keep the high transient TTL switching energy out of the primary ECL reference and preserve ECL noise margins.

When F100K ECL output signal interconnection lengths are direct and short enough, transmission line effects may be ignored and then only a RE output biasing resistor is required for logic operation. Please refer to section seven of the "F100K ECL Logic Databook and Design Guide" for a more detailed explanation of transmission line effects and ECL termination techniques. The RE resistor provides bias to keep the ECL emitter follower output transistor on for both high and low logic states. The RE resistor is normally connected between the ECL output and the most negative potential (V_{EE}) thus permitting "single" supply operation.

The V_{EE} potential will ideally be distributed to the ECL logic from a power plane or bus which has low DC series resistance and low AC impedance. The low AC impedance is essential to supply the transient energy needed during switching. Although the inherent nature of ECL by design is to maintain essentially constant I_{EE} current even during switching, the charging and discharging of internal and external capacitances and the switching currents in the RE resistors place transient demands on V_{EE}. The degree to which the user can maintain complementary balance of ECL output loading will greatly influence the nature of the transient I_{EE} demands.

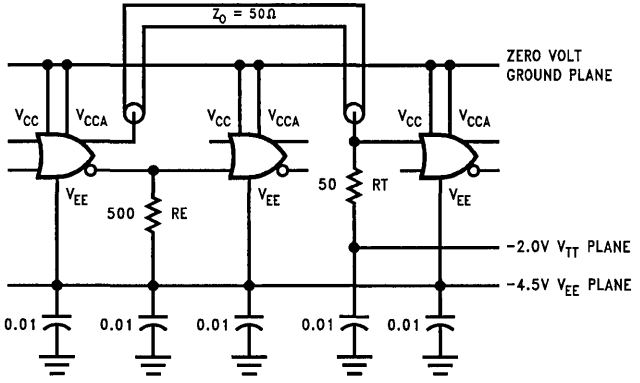


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FIGURE 1. ECL Standard Operation from a Negative V_{EE} Supply

F100K 300 Series Voltage Levels Specified for Standard Negative V_{EE} Supply Operation

Level	Min	Typ	Max	Units
V_{OH}	−1.025	−0.955	−0.87	VDC
V_{IH}	−1.165		−0.87	VDC
V_{BB}		−1.320		VDC
V_{IL}	−1.83		−1.475	VDC
V_{OL}	−1.83	−1.705	−1.62	VDC

Conditions: V_{CC}/V_{CCA} = 0.0 VDC Ground
V_{EE} = −4.2 to −5.7 VDC
RT = 50Ω; V_{TT} = −2.0 VDC
All Levels W.R.T. Ground

The usual recommendation for the V_{EE} plane is to bypass every ECL device at its V_{EE} pin with a good RF quality ceramic capacitor. The point at which the RE resistors return to the V_{EE} plane should also be bypassed particularly if it is a single return from a multiple resistor R-PAK. Values from 0.01 μF to 0.10 μF of the "High K Class II Dielectric" ceramic Z5U grade capacitor are recommended for commercial applications. The lower series inductance inherent in the leadless chip style capacitor is preferred over leaded types for highest frequency performance. The "Mid K Class II Dielectric" ceramic X7R grade capacitor offers acceptable bypass operating characteristics over the broader temperature range of −55°C to +125°C.

Bulk bypassing of the V_{EE} plane with a 1 μF to 10 μF is recommended at the point where the V_{EE} supply connects to the plane. Aluminum or Tantalum Electrolytic capacitors are usually used for bulk bypassing. Miniaturized surface mount Electrolytic capacitors are available for use in high density component applications.

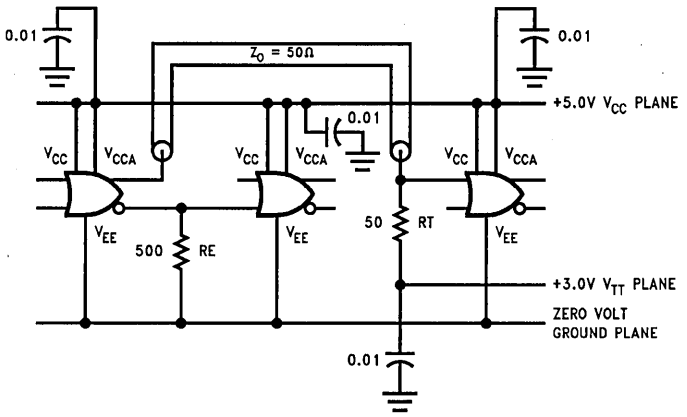
In typical ECL system designs, some inter-connection lengths will exceed the critical values and force the consideration of transmission line effects. The most common high performance and power efficient termination scheme requires the use of a negative 2.0V V_{TT} termination supply. A single RT resistor in conjunction with the V_{TT} supply will terminate each output's transmission line in its characteristic impedance and will also provide optimum bias to the ECL output transistor.

The V_{TT} potential will ideally be distributed to the RT terminators from a power plane which has low DC series resistance and low AC impedance. The low AC impedance is essential to supply the transient energy in the termination resistors during switching. Bypassing V_{TT} wherever RT resistors return to the V_{TT} plane is essential to maintaining the low AC impedance of the plane. Capacitor recommendations for bypassing V_{TT} are the same as for V_{EE} above.

The regulation of the V_{TT} supply is not critical. A variation of ±5% from nominal causes typically only ±12 mV variation in output levels for 50Ω terminations or ±7 mV variation for 100Ω terminations. Note that in standard ECL configuration, the V_{TT} supply need only sink current into its negative terminal (single ended V_{TT} operation with positive terminal grounded). V_{TT} here will typically be a simple series regulated supply. If the need for single negative supply operation is paramount, a less power efficient Thevenin termination scheme can be used between the V_{CC}/V_{CCA} and V_{EE} planes and selective use of series damping in conjunction with RE resistors may also be implemented.

THE PECL TRANSFORMATION

Transforming ECL from negative supply to positive supply operations is conceptually quite easy. Just offset all standard ECL operating potentials by a positive amount equal to an absolute value within the normal V_{EE} operating range. For F100K 300 Series the normal V_{EE} range is −4.5 to −5.7 VDC. A 5V offset fits nicely within the range and happens to match the nominal potential for TTL systems. Thus V_{EE} becomes the 0V ground with V_{CC}/V_{CCA} offset to +5V and V_{TT} (if required) offset to +3 VDC. *Figure 2* illustrates the transformation (from *Figure 1*).



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F100K 300 Series Voltage Levels Specified for Positive V_{CC} Supply [PECL] Operation

Level	Min	Typ	Max	Units
V_{OH}	V_{CC} − 1.025	V_{CC} − 0.955	V_{CC} − 0.87	VDC
V_{IH}	V_{CC} − 1.165		V_{CC} − 0.87	VDC
V_{BB}		V_{CC} − 1.320		VDC
V_{IL}	V_{CC} − 1.83		V_{CC} − 1.475	VDC
V_{OL}	V_{CC} − 1.83	V_{CC} − 1.705	V_{CC} − 1.62	VDC

Conditions: V_{CC}/V_{CCA} = 4.2 to 5.7 VDC
V_{EE} = 0.0V to Ground
RT = 50Ω; V_{TT} = V_{CC} − 2.0 VDC
All Levels W.R.T. Ground

FIGURE 2. ECL Operation from a Positive V_{CC} Supply [PECL]

CONSIDERATIONS FOR PECL OPERATION

All the considerations previously discussed for standard operation still apply; i.e., solid isolated and well bypassed reference planes, etc. Some additional considerations apply for PECL operation.

PECL input and output levels are referenced to the active positive V_{CC} rail that is variable and subject to line and load regulation. PECL level compatibility between sub-systems or systems can be difficult if precise V_{CC} distribution and accuracy are not maintained throughout. Differential PECL signal transmission and reception between systems may be necessary to ease the V_{CC} accuracy burden.

This active positive V_{CC} potential is the primary reference for PECL levels and the source of PECL switching currents. The distribution of V_{CC} to PECL logic is just as important as is the ground distribution to the standard ECL configuration. V_{CC} should be delivered from a continuous copper plane with liberal use of high frequency decoupling capacitors at each PECL device's V_{CC}/V_{CCA} pins.

If TTL or other noisy circuitry is to share the V_{CC}, a separate powerplane should be provided. TTL switching transients should be isolated from the PECL V_{CC} plane to preserve PECL noise immunity. Again, differential PECL operation may be warranted for situations where noise control is limited and good common mode noise rejection is required.

The various requirements for output termination and bias previously discussed for standard ECL applies directly to PECL operation. Note that the nominal +3V V_{TT} supply in PECL mode is required to sink current into its positive terminal (single ended V_{TT} operation with negative terminal grounded) from the emitter follower outputs throught the RT resistors. A current sinking V_{TT} supply will be necessary if operated single ended to ground. The V_{TT} supply should track the V_{CC} supply keeping a nominal 2V offset to assure optimum biasing of the outputs.

The V_{EE} for PECL operation is 0V or ground potential and should be distributed from a continuous copper plane in consideration of handling the transients switching currents from the RE bias resistors. Although the PECL V_{EE} plane will be somewhat tolerant of TTL noise, the recommendation is to isolate TTL transient switching energy in a separate TTL ground plane.

POWERPLANES

The dedication and organization of powerplanes is essential to successful ECL system design.

Figure 3 illustrates an optimum powerplane implementation for Standard ECL operation on a printed circuit mother board in conjunction with TTL circuitry. *Figure 4* shows an optimum powerplane configuration for PECL operation. Note that the dedication and positioning of separate ECL and TTL powerplanes is intended to preserve ECL noise immunity when operating in a mixed signal environment.

Copper Plane 1	Signal
2	TTL 0V Ground
3	TTL +5V V_{CC}
4	Auxillary GND/Power/Thermal
5	ECL − 2V V_{TT}
6	ECL − 4.5V V_{EE}
7	ECL 0V Ground
8	Signal

FIGURE 3. Powerplane Layup for Standard ECL Operation

Copper Plane 1	Signal
2	TTL 0V Ground
3	TTL +5V V_{CC}
4	Auxillary GND/Power/Thermal
5	ECL + 3V V_{TT}
6	ECL 0V V_{EE}/Ground
7	ECL + 5V V_{CC}
8	Signal

FIGURE 4. Powerplane Layup for Positive Referenced ECL

The optimum multiple powerplane approach may not be feasible for some designs. Logic and powerplane partitioning (islands) can be used to control noise when ECL and TTL must share the same powerplane. *Figure 5* illustrates the basic concept where areas of a system board are organized by logic type and share the same horizontal powerplane. Low pass filters are usually used to help isolate high frequency signals in sections of the shared plane.

POWER SUPPLY SEQUENCING CONSIDERATIONS

In logic systems where multiple independent power supplies are used, or where two independently powered systems are connected logically, some consideration must be given to supply sequencing. This is particularly true for ECL/PECL logic due to placement of ESD (Electrostatic Discharge) protection diodes on the inputs and outputs. *Figure 6* shows the typical ESD diode placement in a F100K 300 Series device. *Figures 7a* and *7b* illustrate independently powered ECL driver and receiver operating with an independent ground referenced V_{TT} termination supply.

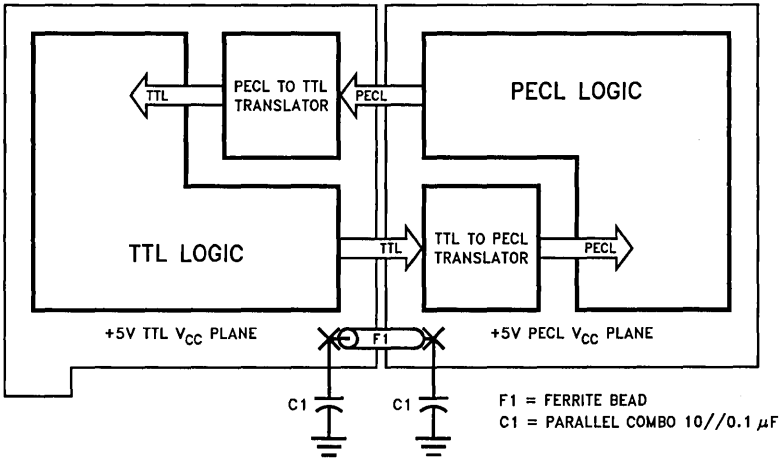

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FIGURE 5. Powerplane and Logic Partitioning

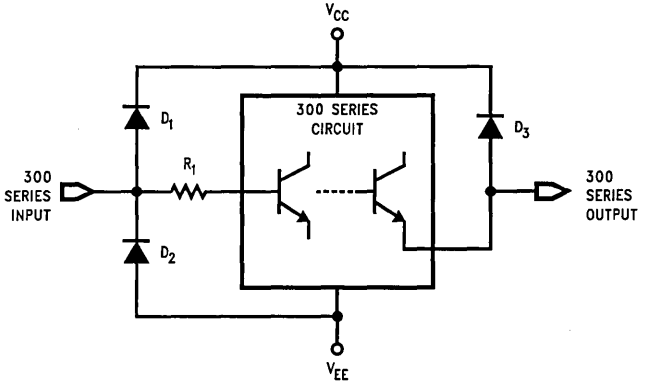

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FIGURE 6. F100K 300 Series ESD Diode Circuit Placement

When the devices (*Figure 7a*) are operated in Standard ECL fashion, V_{EE1} may be off while V_{EE2} and V_{TT} remain on without causing a forward bias potential on any of the ESD diodes. Note that both the true and complement outputs of the ECL1 driver will source logic one current simultaneously to the V_{TT} supply when V_{EE1} is off while V_{TT} remains on. Emitter follower transistors of ECL1 are biased on to a logic high level by the V_{TT}/RT even in absence of V_{EE1}. The potential for V_{TT} current overload exists under these circumstances.

When V_{EE2} is powered off and V_{TT} remains on, the low rail input ESD diode of ECL2 (connected to V_{EE2}) will forward bias and conduct heavily as V_{TT} tries to re-power the V_{EE2} rail. The diode conduction will be limited by the RT resistor and the impedance of the off V_{EE2} supply in parallel with the ECL2 logic impedance. Although the ESD diode current density rating will typically support this current overstress, the recommendation is to avoid this by insuring that V_{EE2} and V_{TT} are ramped together and that V_{EE2} is never more positive than V_{TT} by 0.5V.

When the devices (*Figure 7b*) are operated in PECL fashion, there is a very clear forward bias hazard to ESD diodes when supplies are sequenced. If V_{CC2} is dropped before V_{CC1}, the positive referenced emitter followers of ECL1 will attempt to re-power up ECL2 through its high rail input ESD diode (connected to V_{CC}). The ECL emitter follower outputs are low impedance voltage sources (6Ω typical) and can source an incredible amount of current (greater than 200 mA each output). Thus V_{CC2} must never be more negative than V_{CC1} by 1.0V to avoid current overstress.

When V_{CC1} is powered off and V_{TT} and V_{EE2} remain on, the output ESD diode of ECL1 (connected to V_{CC1}) will forward bias and conduct heavily as V_{TT} tries to re-power the V_{CC1} rail. The diode conduction will be current limited by the RT resistor and the impedance of the off V_{CC1} supply in parallel with the ECL1 impedance. Although the ESD diode current density rating will typically support this current overstress, the recommendation is to avoid this by insuring that V_{TT} is never more positive than V_{CC1} by 0.5V.

If V_{CC1} and V_{CC2} are dropped while V_{TT} remains on, then V_{TT} tries to re-power both V_{CC} rails through the output ESD diode of ECL1 and the high rail input ESD diode of ECL2. The forward bias current is limited by the RT resistor and the V_{CC1}/V_{CC2} supply impedance in parallel with the collective logic impedance. This diode overstress is undesirable and should be avoided by insuring that V_{TT} is never more positive than V_{CC1} or V_{CC2} by more than 0.5V.

If V_{TT} is dropped before V_{CC1}, then increased load current can flow through the RT resistor from the emitter follower output of ECL1. Therefore V_{TT} ramping should be timed with V_{CC1} and V_{CC2}.

From the previous discussion, the most critical concern is that no PECL receiver should be powered down if driven directly by a powered up PECL driver without some form of current limiting. The inputs to the receiver must be current limited with external resistors of 100Ω or greater to be able to survive the overstress caused if V_{CC1} is ever permitted to be more positive than V_{CC2} by more than 1.0V. Although the use of current limiting resistors will alter the effective input edge rates and device propagation delays slightly, careful selection and placement of resistors will minimize device performance degradation. Use of surface mounted chip resistors located close to the input is recommended.

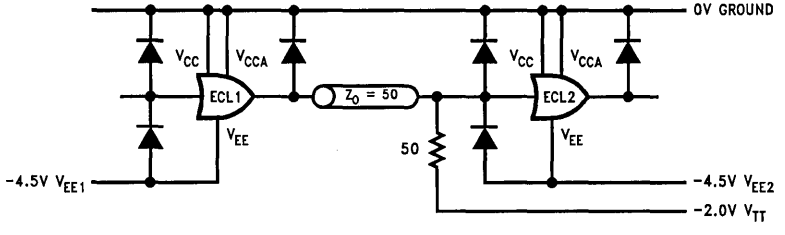

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FIGURE 7a. ESD Diodes in Standard ECL Operation

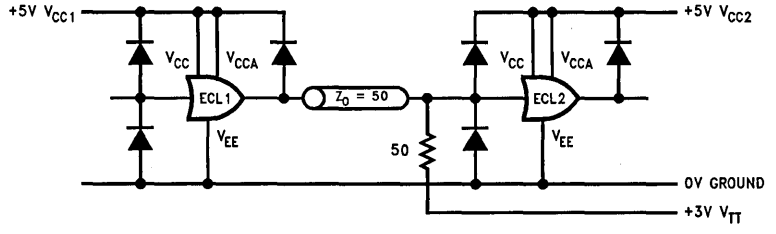

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FIGURE 7b. ESD Diodes in PECL Operation

DUAL SUPPLY TRANSLATORS—THE CONVENTIONAL APPROACH

Dual supply ECL-to-TTL and TTL-to-ECL IC translators have been in general use for several years. These devices perform the logic level translations between ECL operating from a negative V_{EE} supply and TTL operating from a positive V_{CC} supply. This approach naturally allows each logic family to operate in their conventional and Data Book specified manner. System designers typically are most comfortable with the dual supply aproach. This conventional method permits the use of the most familiar design practice for ECL and should easily yield reliable mixed signal system operation. The growing list of F100K 300 Series Dual Supply Translators, as shown in *Figure 8*, is testimony to the continued popularity and versatility of this approach.

Features	100324	100325	100328	100329	100393	100395	100397	100398
Data Bits	6	6	8	8	9	9	4	4
ECL-to-TTL		X	X	X	X	X	X	X
TTL-to-ECL	X		X	X			X	X
Flow-Thru	X	X						
Latched			X		X		X	X
Registered				X		X		
ECL Differential Input		X[1]					X	X
ECL Differential Output	X						X	X
ECL Output Drive (Ω)	50		50	50			25	25
ECL Cutoff (Hi Z)			X	X			X	X
TTL Output Drive (mA) (I_{OL}/I_{OH})		20/−2	23/−3	24/−3	64/−15	64/−15	64/−15	64/−15
TTL TRI-STATE®			X	X	X	X	X	X
ECL Control Pins			X	X	X	X	X	
TTL Control Pins	X				X			X
TPD E to T (ns Max)		4.8	5.9	7.7	5.3	6.4	5.8	5.8
TPD T to E (ns Max)	3.0		3.8	3.9			2.4	2.2
I_{EE} (mA Max)	−70	−37	−169	−199	−39	−67	−99	−99
I_{EE} (mA Max) (Cutoff)			−169	−199			−159	−159
I_{CC} (mA Max)	38	65	74	74	65	65	36	45

[1] V_{BB} provided for Single-ended Operation

FIGURE 8. Table of F100K 300 Series Dual Supply Translators

SINGLE SUPPLY TRANSLATORS—THE NEW WAVE APPROACH

Single Supply Translators that allow PECL-to-TTL or TTL-to-PECL interfaces are a recent addition to the F100K 300 Series ECL family. Development of these devices is motivated by the need for a convenient technique by which higher performance ECL logic can be integrated into existing TTL systems containing a single positive supply. These devices should also provide a vehicle for new lower cost designs of mixed signal single supply systems.

Figure 9 describes three such devices being offered in the F100K 300 Series family. The popularity of PECL operation is expected to grow significantly as designers become more familiar with the technique. As interest and usage of Single Supply Translators increase, the family of this type of device can be expected to expand.

A simple illustration of the ease with which the Single Supply Translator can accomplish the interface from TTL to PECL and back to TTL is shown in *Figure 10*. Note that the translator devices have on chip V_{CC} partitions that facilitate the use of dual powerplanes for the preservation of ECL noise immunity. Differential operation on the PECL side of the translator is recommended to be used to maximize noise immunity. A V_{BB} reference voltage output is provided on the 100390 device to facilitate single ended operation.

Features	100390	100391	100392	100389
Data Bits	6	6	5	6
ECL-to-TTL	X			
TTL-to-ECL		X		
CMOS-to-ECL			X	X
ECL Differential Input	X[2]			
ECL Differential Output		X	X	X
ECL Output Drive (Ω)		50	25	50
ECL Cutoff (Hi Z)			X	
TTL Output Drive (mA) (I_{OL}/I_{OH})	24/−3			
TTL TRI-STATE	X			
TTL Control Pins	X	X		
CMOS Control Pins			X	X
TPD E to T (ns Max)	6.4			
TPD T to E (ns Max)		1.7		
TPD C to E (ns Max)			TBD	TBD
I_{EE} (mA Max) (Cutoff)			TBD	
I_{CC} (mA Max)	48	60	TBD	TBD

[2] V_{BB} provided for Single-ended Operation

FIGURE 9. Table of F100K 300 Series Single Supply Translators

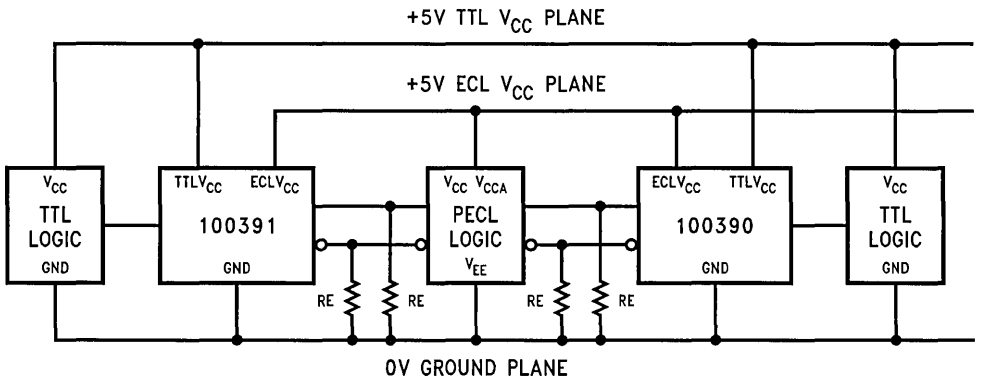

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FIGURE 10. Use of Single Supply Translators

F100K ECL Dual Rail Translators

National Semiconductor
Application Note 784
Doug Bush

INTRODUCTION

The complex electronic systems being designed today often require mixed technologies to incorporate the most efficient balance of performance, speed, power, and cost. In order for one technology to communicate with the other, an interface is needed. One of the most common mix of technolgies seen today is high speed ECL with the slower, but very popular TTL and CMOS. To make this interface as quick and clean as possible, level translators are used. This applications note will discuss ECL to TTL and TTL to ECL level translators available from National Semiconductor's F100K ECL 300 Series product line. Focus will be on Dual Rail Translators (translators which require both ECL and TTL power supplies for normal operation), their differentiating features and possible uses.

TRANSLATOR SELECTION

National Semiconductor offers translators of all different types. Table I shows the TTL to ECL and ECL to TTL translators that are presently available. The first 300 Series translators designed were the 100324 and 100325. With these devices, unidirectional translation is possible in either direction (TTL to ECL with the 100324, ECL to TTL with the 100325). As systems and data widths become larger, more bits need to be translated. This need was satisfied with the introduction of 8- and 9-bit translators. The 8-bit translators (100328, 100329) also offer bidirectional translation functionality for applications which require two way communication. In many cases, communication over significant distances is needed in noisy environments. To handle this situation, differential translators like the 100397 and 100398 are used. The 100397 and 100398 also offer bidirectional translation with differential ECL and 25Ω drive with cutoff. The 100397 uses ECL control pins while a separate option, the 100398, has TTL control pins. In applications where high output drive is needed after an ECL to TTL translation the 9-bit 100393, and 100395, or 4-bit 100397 and 100398 can be used. The 64 mA I_{OL} output current capability is ideal for driving long lines and achieving faster switching times by discharging the line it is tied to faster when in the LOW output state. These outputs are also capable of driving higher fanouts than the lower output current devices.

If the designer only has a +5V supply available (i.e., An additional ECL supply cannot be used), single rail translators can be used. For more information on single rail transla-

TABLE I. 300 Series Dual Rail Translators

Features	100324	100325	100328	100329	100393	100395	100397	100398
Data Bits	6	6	8	8	9	9	4	4
ECL to TTL		X	X	X	X	X	X	X
TTL to ECL	X		X	X			X	X
Latched			X		X		X	X
Registered				X		X		
ECL Differential	OUT	IN*					I/O	I/O
ECL Drive (Ohms)	50		50	50			25	25
ECL Cutoff			X	X			X	X
TTL Drive I_{OL}/I_{OH} (mA)		20/−2	24/−3	24/−3	64/−15	64/−15	64/−15	64/−15
TTL TRI-STATE®			X	X	X	X	X	X
ECL Control Pins			X	X	X	X	X	
TTL Control Pins	X				X			X
TPD ECL to TTL (ns Max)		4.8	5.9	7.7	5.3	6.4	5.7	5.7
TPD TTL to ECL (ns Max)	3.0		3.8	3.9			2.4	2.4
I_{EE} (mA Max)	−70	−37	−169	−199	−39	−67	−99	−99
I_{CC} (mA Max)	38	65	74	74	65	65	36	45

*V_{BB} output available for 100325

tion refer to applications note AN-780 "Operating ECL From a Single Positive Supply".

TRANSLATOR OPERATION SPEED ADVANTAGES

Designers who have primarily a TTL system will often use ECL in areas such as clock distribution, backplanes, and differential data transmission where speed is most important. This can be accomplished by level translating from TTL to ECL, performing the desired ECL operation, and then translating back to TTL. As intimidating as this approach sounds, the propagation delay savings gained can be very significant. Consider as an example the TTL "error capture circuit" shown in *Figure 1A* and the same function performed using ECL shown in *Figure 1B*. In *Figure 1A*, a TTL system with control lines CR0 and CR1 is being monitored for errors. The error capture circuit consists of a buffer, decoder, and six counters. The buffer transfers signals from the control lines to the inputs of the decoder. The decoder determines which type of error is present and then feeds into a 2 stage counter to keep track of how many times a particular error occurs.

Table II gives conditions for all possible levels on the control lines. When a counter reaches a terminal count of 256 for any type of error, a signal is fed to the TTL controller which initiates a service routine for that particular type of error. For the PDIP devices shown in *Figure 1A*, the maximum propagation delay at room temperature for the error capture circuit is approximately 51 ns.

TABLE II. System Errors

CR0	CR1	Z0	Z1	Z2	Z3	Operation
L	L	L	H	H	H	No Errors
H	L	H	L	H	H	Type 1 Error (T1)
L	H	H	H	L	H	Type 2 Error (T2)
H	H	H	H	H	H	Type 3 Error (T3)

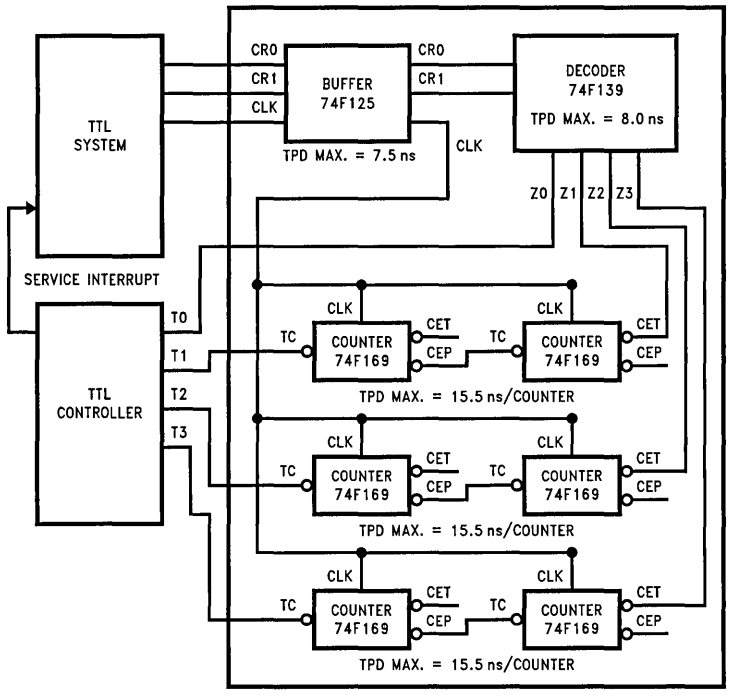

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FIGURE 1A. TTL Error Capture Circuit

A significant amount of time can be saved by using translators and performing the error capture with ECL. In *Figure 1B*, an ECL error capture solution is implemented. In this case, a 100324 TTL to ECL translator is used to buffer the control line signals and provide the required ECL voltage levels. Data is then fed into the 100370 decoder and inverted for counter input. As in the TTL circuit (see *Figure 1A*), when the count reaches 256 for any type of error, a signal is fed into the controller for service routine activation. The ECL signal is first converted to TTL by use of the 100325 before being transferred to the controller. The error circuit for *Figure 1B* has a maximum propagation delay (using CDIP package at 25°C) of approximately 20 ns.

A comparison of the ECL and TTL error capture circuits shows that ECL offers a 31 ns advantage in speed over the equivalent TTL design. This is a savings of more than half of the entire TTL timing budget. Another benefit of using ECL in high speed applications is that as frequency increases, TTL power increases while ECL power remains constant. In fact, as system bandwidth requirements exceed 50 MHz, ECL shows a power advantage over TTL. Since the translators in Table I have either TTL inputs or outputs, the power will increase slightly with frequency, but not as much as pure TTL devices.

POWER SUPPLY AND NOISE CONSIDERATIONS

The primary consideration with mixed voltage, dual rail translators is to insure maximum noise protection between the TTL and ECL ground. The ECL bandgap circuit (shown in *Figure 2A*) is used to generate internal reference voltages. The internally generated reference voltage used to set the input and output threshold levels is called V_{BB}. The potential generated to control the level of the active current source is called V_{CS}. These reference voltages (V_{BB} and V_{CS}) set up by the bandgap circuitry are referenced to the ECL ground (V_{CC}). Any noise on this ground will be injected into the reference voltages (V_{BB} and V_{CS}) producing reduced noise immunity. This implies that a stable, noise free ECL ground is needed.

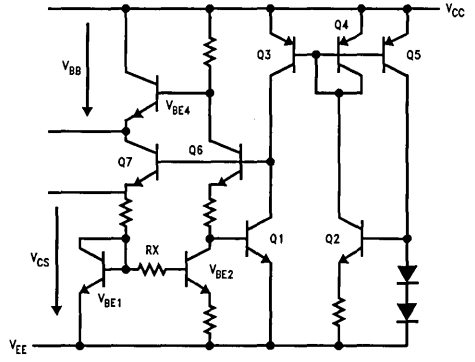

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FIGURE 2A. ECL Bandgap Circuit

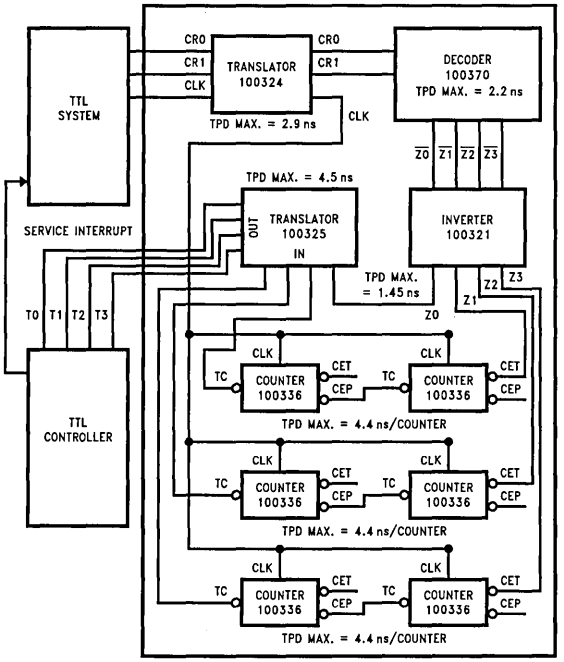

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FIGURE 1B. ECL Error Capture Circuit

Ground bounce has been a concern of TTL designers for many years. *Figure 2B* shows the TTL totem pole output structure. The intrinsic inductance in the ground lead (TTL GND) and power lead (V_{TTL}) are labeled as L1 and L2, respectively. In order to switch from HIGH to LOW, current (marked I1 in *Figure 2B*) must flow through Q3 and L2 to discharge the load capacitance. As this current changes, a voltage is developed across the inductor L2 (Recall: V2 = L2(dI2/dt). Since the inductor (L2) is between system ground and the device ground, there will be a voltage drop between them. This voltage difference between device and system ground will cause the device input and output levels to be offset because they are referenced to the internal device ground. The devices which are driving inputs or being driven by the outputs are referenced to the system ground (TTL GND in *Figure 2B*). This effect is known as ground bounce.

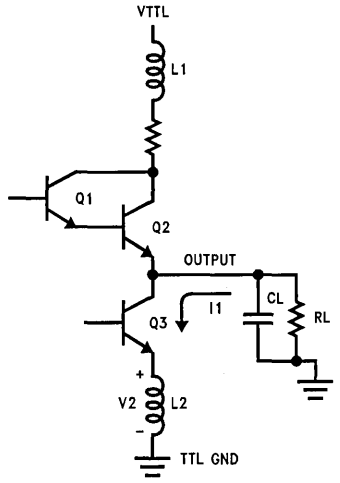

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FIGURE 2B. TTL Totem Pole Output

To insure maximum noise protection, it is recommended that the ECL and TTL ground planes on the printed circuit board (PCB) are run independently, and are only connected back at the low impedance source of the power supply. Likewise separate power planes will be used for the TTL positive supply (V_{TTL}), ECL negative supply (V_{EE}), and ECL output load power supply (V_T). This leads to five layers of a multi-layer PCB being dedicated to power planes. Additional layers, either internal or on the surface, can be used to run signal lines. *Figure 3* shows a typical layout for a seven layer TTL/ECL PCB. Signals are run on both sides of the board.

LAYER 1	Signal
LAYER 2	TTL Ground
LAYER 3	TTL +5V (V_{TTL})
LAYER 4	VT
LAYER 5	ECL −4.5V (V_{EE})
LAYER 6	ECL 0.0V (V_{CC})
LAYER 7	Signal

FIGURE 3. PC Board Power Planes

Consideration should be made with regard to the power up sequencing of translators. Table III describes the conditions observed for the various translators when ECL or TTL power is lost.

Control pins should be driven by power up referenced signals, so that during power up sequencing, the Output Enable pins are driven to the disable state.

DESIGN CONSIDERATIONS

Translator Pin Connections

Dual rail translation implies that both positive (V_{TTL}) and negative (V_{EE}) voltage supplies must be used. These voltages are typically +5V and −5V respectively. V_{CC} and V_{CCA} pins are used for the ground connection to 0V. In addition to the traditional ceramic DIP and Flatpak packages, the F100K 300 Series translators offer a 28-pin Plastic Leadless Chip Carrier (PLCC) package for surface mount capability to reduce board space. This package includes three V_{EES} pins which are used to dissipate heat from the package. These pins are connected internally through the substrate to V_{EE}. It is recommended that these pins be connected to the V_{EE} power plane and *NEVER* to V_{CC}, V_{CCA}, or V_{TTL}.

Translator Location

When using ECL with TTL or CMOS, it is important to group CMOS and TTL devices away from the ECL devices. This will reduce the possibility of corruption of ECL signals caused by noisy TTL or CMOS switching. Translators with TTL outputs should be grouped with the TTL devices on the printed circuit board (PCB), and translators with ECL outputs should be grouped with the ECL devices.

TABLE III. Output State Under Power Loss

Product	Loss of V_{TTL}		Loss of V_{EE}	
	ECL Output State	TTL Output State	ECL Output State	TTL Output State
100324	V_{OH}	N/A	V_{OH}	N/A
100325	N/A	HI-Z	N/A	HI-Z
100328	V_{OH}	HI-Z	V_{OH}	HI-Z
100329	V_{OH}	HI-Z	V_{OH}	HI-Z
100393	N/A	HI-Z	N/A	HI-Z
100395	N/A	HI-Z	N/A	HI-Z

APPLICATIONS

Some of the many uses for ECL/TTL translators are:

High Speed Cache Memory: *Figure 4* shows a two way set associative cache system. Data is transferred from the ECL memory to cache with the use of a single 8-bit 100328 bidirectional translator. Once the data reaches the cache, it can be moved to the microprocessor quickly for manipulation. Since the data bus is a two way communication system, a bidirectional translator is needed. The address bus, on the other hand, requires only a one way communication. This implies a unidirectional translator could be used to interface the address to ECL memory. It would take three hex 100324 devices for the 16-bit line shown in *Figure 4*, but to reduce package count two 8-bit 100329 devices are used. The ECL memory based system allows reading and writing access within one clock cycle. Since the memory is accessed quickly, the wait states produced by memory read and write are virtually eliminated which results in a faster operating system.

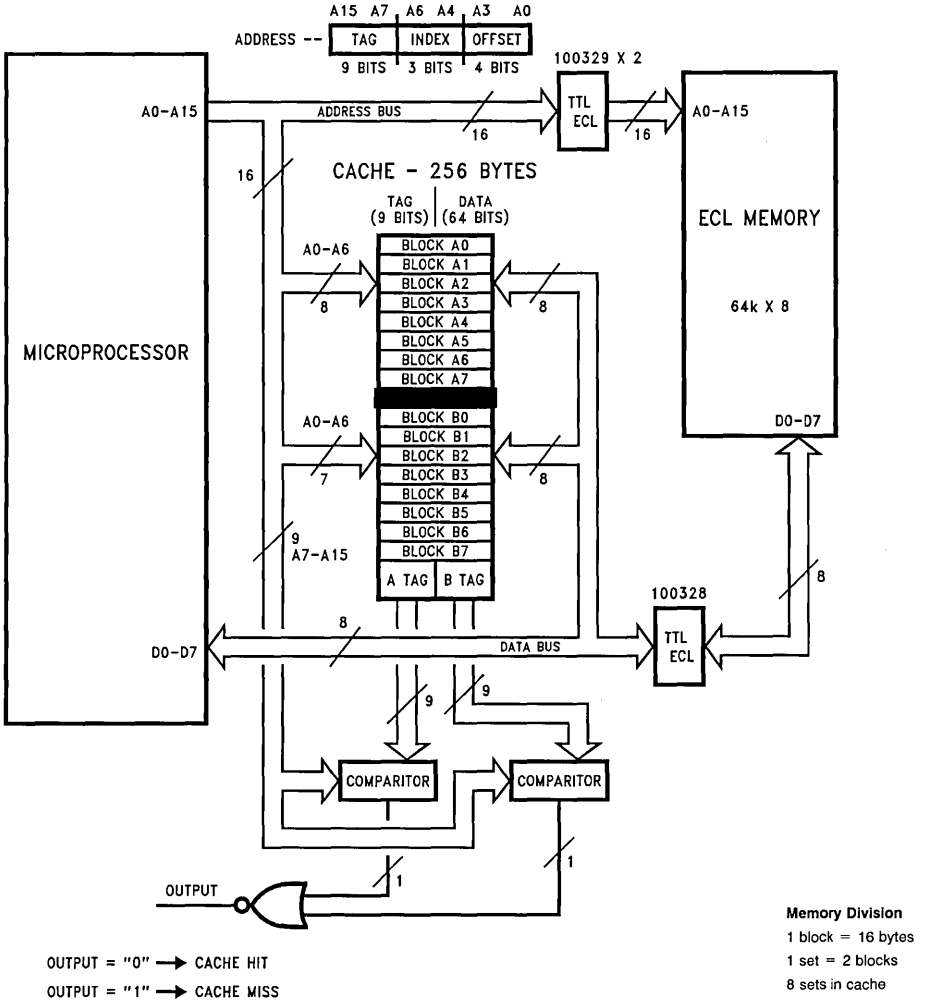

FIGURE 4. Two Way Set Associative Cache System

Peripheral Interface Applications: The 100393 and 100395 9-bit translators are ideal for translation applications where an 8-bit data bus with parity is used. An example of this situation is shown in *Figure 5*. In this case, ECL data and parity is transferred through an ECL controller and sent to the ECL-to-TTL translator. Data and parity is then converted to TTL levels and sent through a cable to the peripheral unit (such as a printer) for parity checking and data transfer. The 9-bit ECL-to-TTL translator (100393 or 100395) allows for an 8-bit data transfer and 1 bit for parity. The 9-bit function of the 100393 and 100395 also enables the translation to be performed with one chip which reduces chip count and board space. These translators also have a 64 mA output drive which is needed to drive the long length of cable associated with the printer hook up.

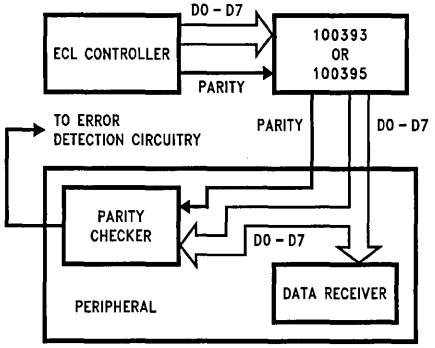

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FIGURE 5. Peripheral Interface Application

TTL/CMOS Dynamic Random Access Memories (DRAMs): In instances where high speed ECL CPUs are used, low power/low cost DRAMs can be addressed as bulk storage for non-speed critical operations by interfacing the ECL CPU with DRAM via the 100328/100329. This enables you to perform all of your high speed data processing tasks in ECL and use more readily available TTL/CMOS DRAMs for data storage.

High Speed Coprocessor: A high speed ECL coprocessor can be added to a lower speed processor for enhancement of high density computations. This will increase the speed and improve the overall system performance. The 100324 and 100325 would allow differential communication to the ECL coprocessor and the differential ECL signals give noise immunity from the surrounding TTL system.

ECL Bussing: All the translators give TTL systems the ability to use high speed and low EMI ECL backplanes. ECL backplane applications typically use mixed technologies off the backplane which means that quick and reliable translation is needed. Refer to the "ECL Backplane Design", applications note for additional information.

Graphics: The 100324/100328/100329 give TTL to ECL conversion for use in high speed ECL graphics applications. The graphics will be in parallel form in the TTL state, converted to ECL then turned into serial form by either the 100341/100336 shift registers, before being fed to a high speed graphics driver.

REFERENCES

D. Bush, "ECL Backplane Design", April 1991 Applications Note AN-768.

J. Davis, "Operating ECL From a Single Positive Supply", June 1991 Applications Note AN-780

W. Blood, "MECL System Design Handbook", Fourth Edition, 1988. Copyright Motorola, Inc.

"F100K ECL Logic Databook and Design Guide", 1990 Edition.

Taking Advantage of ECL Minimum-Skew Clock Drivers

National Semiconductor
Application Note 817
Jim Mears

CLOCK DISTRIBUTION BACKGROUND

Digital systems have tended from their inception toward incorporation of higher speed elements rather than architectural changes as the solution to the computational speed problem. One result of this has been mounting pressure on the semiconductor elements of these systems for higher speed and all that this implies. Not only the operating frequency and signal propagation delay but also the relative timing relationships of devices performing parallel tasks were challenged. As semiconductor process improvements pushed operating speeds higher, the evolution from individually-packaged to multiply-packaged gates helped reduce delay and speed differences among like devices. Even so, areas still existed where system designers demanded ever greater improvements in performance uniformity of digital logic elements. The synchronization signal generation system, often referred to as the clock system, is one area in need of such improvement.

Most digital logic systems employ some means of synchronizing the actions carried out by the system's elements. The precision with which these various elements are regulated can be shown to have a direct effect on the overall speed of the system. The less time variation that must be allocated to the logic elements in the signal path, the faster that operation may be executed. Therefore, the overall time to perform all operations may be reduced or the system speed may be increased. In addition, the coordinated timing of the synchronizing system itself must benefit from an equivalent reduction in relative timing of its elements, or else only limited overall benefit to system performance is possible.

CLOCK NETWORK ELEMENTS

The typical synchronizing or clock system consists of several closely related elements:

— a primary signal source, usually a precisely regulated, high frequency oscillator,

— frequency dividers to derive lower frequencies from the primary source,

— distribution amplifiers to boost signal power or supply separated loads,

— signal delay, duty-cycle alteration or re-synchronizing elements,

— interconnect wiring, connectors and signal distribution network,

— and a power source and distribution system for the semiconductor devices in the system.

Each of these elements contributes a degree of variability to the overall timing precision capability of the system. By virtue of the fact that the physical properties of each element can be controlled only within certain limits, the complete system will exhibit a variability somewhat larger than its elements taken individually. The effect of the variations contributed by the elements to the overall system variability is a physical fact that may be demonstrated mathematically.

Among the factors affecting variability are:

— physical size such as the length of wiring,

— electrical properties such as resistance and charge,

— internally generated and externally induced noise,

— and environmental factors like temperature and altitude.

The visible effect of variability on the system timing is popularly termed "skew". Similarly, the individual variabilities of each element are likewise termed "skew". The term "skew" is used also to describe the difference in delay between like paths taken by signals in a logic device or system. However, as with many useful terms when carelessly applied, the term "skew" can lead to some confusion unless it is more precisely defined.

When applied to the differences in propagation of electrical signals through like paths in a logic system, the term "skew" will be taken to mean "differential timing error". In terms of the overall effect on the desired timing performance of the affected system or device, "skew" will be defined as "a deviation or asymmetry from the mean or desired timing value". The latter meaning of skew will assume greater importance in the prediction and analysis of system timing errors to be covered later in this note.

MEETING THE SKEW CHALLENGE

Control of skew in systems is at best a difficult challenge for design engineers. At its worst, skew can be the thing that makes or breaks a design. So, to give engineers an advantage in controlling skew, National offers ECL devices specifically designed to minimize the device-related component of skew. In addition, the skew properties of these devices are specified and tested. This has been done to reduce the design effort required to compensate for device-related skew effects. The results are tighter system timing margins, more reliable operation and faster operating speeds. This means greater system through-put and information processing efficiency.

300-SERIES ECL—The Best Weapon Against Skew

300-Series ECL has some natural advantages in the war on skew. ECL differential amplifiers are minimum-skew by their very circuit configuration. The fundamental property of the differential amplifier used as a logic element is balanced switching. The amplifier, *Figure 1*, is symmetrical. This results in identical switching delays regardless of output. Following stages are added symmetrically, *Figure 2*, so that overall balance is maintained internally. 300-Series devices designed for minimum-skew also employ a unique die layout to preserve the basic amplifier balance.

Another advantage of 300-Series ECL is its precise, stable V_{BB} reference supply with wide operating power supply range. This reference is compensated for stability from the effects of changes in temperature or supply voltage. 300-Series minimum-skew devices operate from −4.2V to −5.7V supplies as do all other 300-Series logic devices. Ad-

vanced semiconductor processing, design and manufacturing result in uniquely low power consumption for this ECL family.

Augmenting the inherent balanced design of the amplifier, 300-Series minimum-skew devices feature differential inputs and outputs. Selected devices have an additional single-ended input and input selector for use as a test input or auxiliary main input. However, skew tolerances are wider when using the single-ended input. The differential outputs are fully buffered emitter-followers. They are designed to have symmetrical transitions and skew performance under symmetrical loading conditions. Some devices also make an external V_{BB} reference available for use in situations where the inputs must be separately biased.

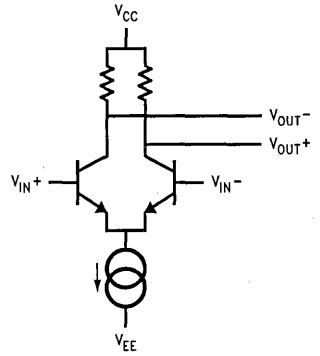

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FIGURE 1. ECL Differentical Amplifier

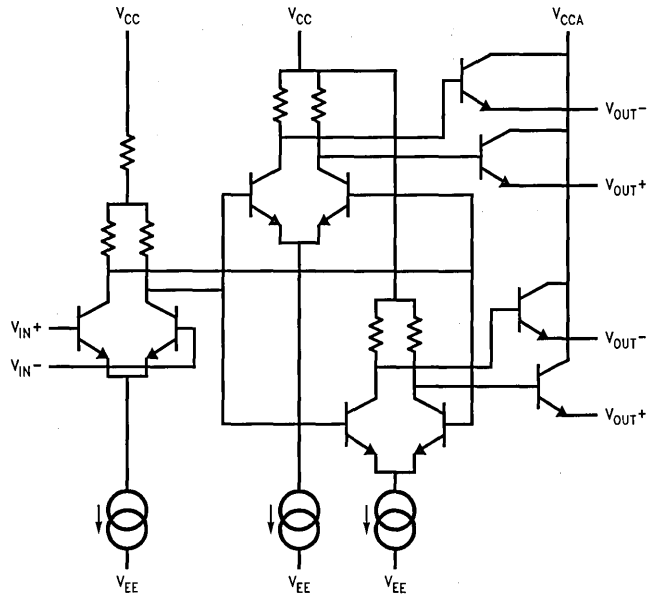

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FIGURE 2. ECL Buffered Amplifier

Skew can be adversly affected by packaging. For this reason National has chosen to supply F100K minimum-skew devices in packaging complementing their inherent performance. F100K devices are supplied in SOIC, PCC and flatpak packaging as appropriate for the intended class of service; commercial, industrial or military.

PACKAGE TYPE AND LAYOUT

Packaging and pinout also affect skew performance. Smaller, more symmetrical packaging like PLCC and SOIC types contribute less to skew than do DIP packages. Their smaller size reduces parasitic inductance, a contributor to noise and signal delay. Symmetrical pin layout equalizes path length for all signals from the die to the circuit board thereby reducing a skew component. And, additional output V_{CC} pins help reduce skew by providing extra paths for output signal return currents to ground.

TESTING

Despite careful design, packaging and advanced processing, skew performance is worth little unless its effect on device performance can be accurately known. Reliable skew values, guaranteed by test, are essential in predicting system performance. 300-Series ECL minimum-skew devices are fully tested and specified for all standard DC and AC parameters as well as all relevant skew parameters.

It should be appreciated that devices designed for minimum skew values of a few tens of picoseconds are difficult to test using ordinary IC test equipment. Therefore, National has developed advanced production test equipment capable of measuring the AC and skew characteristics of these high-performance devices. This results in more accurate and dependable data for design and greater uniformity of product.

SYSTEM DESIGN OBJECTIVES

The best way to take advantage of minimum-skew driver capabilities is through good system design. Minimum-skew specified devices cannot compensate for or improve on a poor system design. However, these devices can add extra margin to a good design. They also permit more predictable performance in well designed system environments.

The majority of problems that plague clock generation and distribution systems lies beyond the active devices and outside of their effect. These problems result from shortcomings in the signal transmission, power supply or mechanical systems. A good system design should give the minimum-skew driver a fighting chance to perform satisfactorily. This is the primary job of the system designer.

But, before the designer can effectively use these devices, a reasonable set of electrical and mechanical specification objectives for the overall system must first be developed. Next, the device specifications as they apply within the scope of the system specification must be understood thoroughly. Only then can devices with performance appropriate to the overall objectives be selected. Indeed, the process of resolving device and system objectives may reveal incompatibilities. Then either the system requirements or the choice of device must be changed. Lastly and most importantly, the active devices must not be over-worked or handicapped by improper load conditions or the system environment.

A good set of system objective specifications will incorporate all of the following considerations:

— A stable, adequate, noise-free and well isolated DC power supply and power distribution system,

— Noise-resistant and RFI/EMI-proof design and suppression techniques,

— A carefully designed signal transmission and distribution system,

— Appropriate and efficient printed circuit board layout,

— Adequate cooling for all power-dissipative devices,

— Environmental requirements like altitude, humidity, and temperature:

— The appropriate active devices for the required performance.

The sections that follow present design techniques and guidelines formulated around the above objective specifications. Colateral sources where more complete or additional design information may be found will be noted or may be found listed in the Appendix.

POWER SUPPLY NETWORK DESIGN OBJECTIVES

ECL minimum-skew devices can benefit especially from a well designed power supply system. Though not unique for minimum-skew devices, the design of ECL power supply systems must achieve several important objectives.

1. The power system must supply constant, noise-free voltage at adequate current levels to all active devices in the system.
2. The power system must appear as a virtual battery to each device. That is, it must effectively isolate devices such that each appears to be independently powered. Thus, noise signals resulting from operations going on within each device will not propagate to other devices through the power supply system.
3. The power supply system also must propagate without distortion the return or image currents for all signal-carrying transmission lines.
4. The power distribution planes within each printed circuit board (PCP) should act as electrostatic shields to reduce RFI radiation from the transmission line system.

These objectives can be adequately met if reasonable care is taken in the design of the power supply feed system, the supply isolation and bypassing and the organization and layout of the PCB's.

More information on power supply design considerations can be found in the "F100K ECL Logic Databook and Design Guide", Chapter 5.

POWER SUPPLY BYPASSING

The topic of power system bypassing is generally given inadequate treatment in logic applications literature. The common approach taken is to simply recommend that a 0.1 μF ceramic capacitor be used for every so many devices. In systems with frequencies predominating below 10 MHz and edge rates on the order of 1V/ns or slower, this prescription may be adequate. However, for systems with frequencies above 10 MHz and edge rates less than 1V/ns, the above prescription is bad medicine. The reasons are easy to explain but require a look at the role and objective of bypassing.

Bypassing serves two general roles in the power supply system—filtering and energy storage. Both of these are related by the fact that, in performing filtering, the capacitor stores and releases energy. To be more specific, the four goals of an efficient bypassing scheme are:

1. Reducing the internal impedance of the power distribution wiring system,
2. Low-pass filtering of the DC being supplied to each active device,

3. Isolating active devices from each other, and
4. Controlling noise due to transient current demands on the supply system.

These four goals are interrelated and are parts of the primary objective of having each active device appear as though powered by an internal, ideal battery. In fact, goals 2, 3 and 4 can be considered as results of achieving goal 1. Reducing the impedance of the power system conductors at all frequencies in the system pass-band helps accomplish all goals of efficient bypassing.

The "F100K ECL Logic Databook and Design Guide" (Section 7, Chapter 5) recommends multi-layer PCB construction with entire layers assigned to each supply voltage and ground. While this might appear to be an ideal power distribution method for DC, it increasingly deviates from the ideal as frequency increases. For frequencies below about 10 MHz, the internal impedance of power plane layers may be in the range of 1Ω to 10Ω depending upon geometry. At higher frequencies, and especially above 50 MHz to 100 MHz, skin and striction effects cause a ten-fold or greater increase in internal impedance. This means that current changes resulting from switching of the active devices at high frequencies can induce large voltages in the power planes. These noise voltages affect nearby circuits and signals on transmission lines. To eliminate this interference, a means is needed for decreasing the impedance of the planes at high frequencies.

Restricting the pass-band of a wire transmission system to frequencies approaching DC is termed low-pass filtering. Suitably sized capacitors placed at regular intervals on a wire transmission system form a low-pass filter. As frequency increases, the capacitor's reactance decreases. This reduces the amplitude of the signal as it traverses the transmission line. Therefore, the effect of noise generated by an IC on the power supply voltage of its near neighbors is reduced. In addition, lowering the internal impedance of the power plane system reduces radiated RFI and the effects of external interference sources on the power supply system. And, the power plane system will appear as a more nearly uniform AC ground for signal-carrying transmission lines in adjacent layers of the PCB.

Another property of the transmission line, low-pass filter is that it delays signals traveling on the line. In addition to attenuating AC signals and noise generated by the active devices, the signals are also delayed. This effectively increases the isolation between devices in the time-domain. Naturally, as the delay of the power supply transmission system increases, the closer the bypass capacitors must be to the noise source in order for them to be optimally effective.

Supply bypassing is generally less critical in F100K ECL systems than in 10K systems, especially since output load balancing can be used. Bypassing still must perform the functions mentioned previously, but the balanced switching of F100K results in a quieter overall system to begin with. The primary suppression role of bypassing is in controlling noise from unbalanced output switching on the power system.

The selection of bypassing components for F100K systems should be based on the expected operating frequencies of the various networks as well as the output transition rates. Also, the choice of balanced versus unbalanced output loading plays a major role.

Capacitors bypass or suppress frequencies best near their self resonant frequency, *Figure 3*. At this frequency the capacitor appears to be more nearly a short-circuit. Below resonance the capacitive component of reactance dominates. Above resonance the inductive component plays a bigger role. The effective impedance at resonance is the resistive component or ESR (equivalent series resistance). It is normally desirable to minimize the ESR so that the capacitor is a good short circuit. However, it may be more desirable to have some resistance in series with the capacitor in order to broaden the range of frequencies where the capacitor is effective.

In the time domain, the capacitor's behavior becomes more complex. Fast risetime transient pulses contain frequencies generally far above the capacitor's self-resonant frequency. During these pulses, the capacitor has an instantaneous impedance value ten or more times its ESR. For this reason, it is often desirable to "bandspread" the bypass capacitor by using several different capacitor values in parallel. An example of this is placing 0.1 μF, 10 nF and 1 nF ceramic chip capacitors in parallel. The capacitors may be attached to the PCB in a sandwich, "piggy-back" style, provided their lengths are equal. Leaded capacitors may be placed close together on the circuit board to achieve a similar result, also.

The signal frequencies being transmitted by the logic devices and the switching frequencies of device outputs are not the only signals that must be handled by the bypassing. There are also frequencies associated with the energy transfer between different functional groups of components on the PCB's and in the overall system. For instance, a memory system may be active at one-fourth of the rate of an associated CPU group. The peak energy exchange rate between the memory system and the power supply would be one-fourth that of the CPU and the supply. Though the memory may handle signals at the same frequency as the CPU during communications, the power supply system also sees the lower frequency as well. Therefore, the power supply system and the memory/CPU circuit board must have bypass capacitors for both sets of frequencies. For this reason, larger value capacitors, usually tantalum or similar electrolytic types, are found on circuit boards. These capacitors smooth energy transfers at lower frequencies.

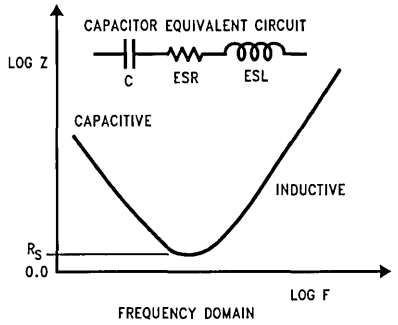
CLOCK SOURCE NOISE CONTROL

The clock system is normally the source of most high frequency noise in digital systems. Part of the overall design objective for the clock system is that it not create interference with other parts of the system.

Isolation of the clock source and its associated distribution amplifiers is an effective way of reducing such interference. Insertion of a ferrite choke in the power supply feed to the active devices forms a noise filter that reduces interference from these devices to other logic through the power system. The filter may take the form of a Pi-network or longitudinal choke as in *Figure 4*. In selecting the inductor, the core must have sufficient current rating to handle the load without saturation. Also, the core material should be capable of operating over the frequency range of the oscillator and associated components. Type 3B or 4B core materials are typical for ECL applications. Suitable 6-hole ferrite chokes are available from Fair-Rite, Siemens, Ferroxcube and others.

CLOCK NETWORK TOPOLOGIES

The choice of clock network topology is intimately a part of the architecture and partitioning of the system. To recom-



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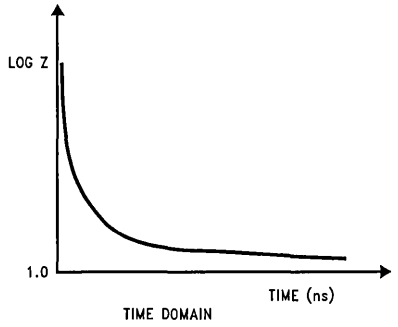

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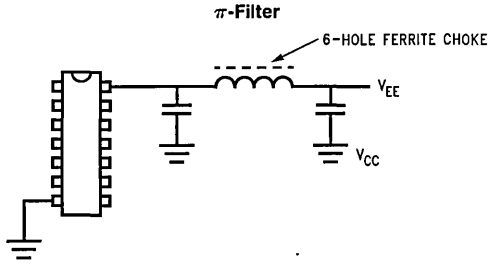
FIGURE 3. Capacitor Reactance



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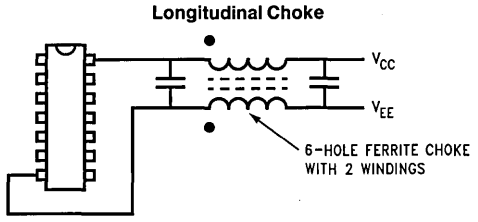

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FIGURE 4. Power Supply Isolation Techniques

mend a particular topology would be presumptive. Therefore, the scope of this discussion will be limited to more general considerations of the networks.

The general forms of networks suitable for clock distribution are: point-to-point, daisy-chain, radial (star), branching (tree), auxiliary main input and bus. Any of these can be implemented as single-wire-over-ground or balanced differential networks. The differential method has advantages of less suceptability to interference from noise, temperature effects, threshold shifts and common-mode signals. These, plus the network's inherent balance, mean lower skew. F100K is particularly suited to use in differential networks. It employs differential outputs on virtually all devices and differential inputs particularly on clock distribution devices.

Naturally, to benefit from the advantages of the differential network, its balance must be maintained. Loading and terminations should be applied equally to both conductors of the differential pair. If loading is not balanced, the propagation delay of each conductor will be different. This can lead to differences in the arrival time of the complementary signals thereby increasing skew.

Regardless of the network topology, the relationships of network impedance, drive capability, critical loading and termination must always be considered.

IMPEDANCE, LOADING AND INTERFERENCE

The equivalent generator resistance of the F100K output emitter follower is approximately 7Ω. With this low value, the output is nearly an ideal voltage source capable of driving almost any reasonable value of load impedance or transmission line type. High impedance transmission lines (above 50Ω) are difficult to achieve in practice on PCB's with thin dielectrics. However, high impedances are more common with twisted-pair lines. The propagation velocity of energy is more affected by capacitive loading on high impedance lines. And high impedance lines are more susceptable to crosstalk and noise interference.

Low impedances (less than 50Ω) require wide line widths, a problem where small packages and dense PCB layout are desirable. Also, lower impedances require more energy from the driver. For a given output type, this results in lower voltage swings into the line and higher DC and AC power since the termination value is lower, also. An advantage of lower impedances is that of their being less affected by capacitive loading and crosstalk.

The effect of loading versus line impedance is easily illustrated. A 50Ω line in FR-4 material has an unloaded propagation delay of about 56 ps/cm. Unloaded 25Ω and 100Ω lines in this material have the same delay. By adding only 1 pF/cm load to the 50Ω line, the delay is increased by 21 ps. The 25Ω line's delay increases 11 ps and the 100Ω line by 38 ps. Clearly, skew-versus-loading is easier to control if the line impedance is kept low. This is the reason that, from all practical standpoints, 50Ω is widely considered as the best line impedance choice.

Controlling the chosen impedance and skew in practical networks can be difficult in practice. This is particularly true where many loads need to be driven in precise phase relationship to a source. Ideally, it would be best to drive each load in a point-to-point connection. Except for the most exacting applications, this can be costly in terms of board space, power and components.

Series-terminated radial or star networks can be used in many cases to drive multiple loads from one output. As long as the load impedance driven does not exceed output drive capability, 2, 3 or 4 lines may be driven. Radial nets may also be driven from the end of another transmission line connected to the driver output. In this case, the impedance of the line between the driver output and the star-point must be less than the impedance of any line connected to it. Each line radiating from the star-point is driven through a series termination. The value of the resistor is chosen to give the minimum required voltage swing at the input connected at the receiving end of the line. More details for designing radial networks may be found in Chapter 4 of the "F100K Logic Databook and Design Guide".

Timing and skew are more difficult to control with the daisy-chain network and its bi-directional equivalent, the bus network. Differences in the individual load values attached to the net contribute to increased skew. This is especially true in parallel-path buses where there is another complicating factor. The bus is normally bi-directional. Whereas the daisy-chain net has one source and multiple loads, the bus has multiple sources. Delay from one source to a given destination, relative to another source to the same destination, may create difficult timing situations, especially where all sources share a common distributed clock. In such situations, consideration should be given to re-synchronization of the common clock relative to the other signals being transmitted from the particular location on the bus. This re-timed clock will then be properly synchronized to its related signals and a reduction in location-dependent skew on the bus will result.

TERMINATION NETWORKS

Minimum-skew drivers cannot correct the behavior of improperly terminated networks. In fact, operation of any driver-network combination is impaired by faulty termination. Faulty termination corrupts signals and contributes to skew, timing and noise problems. A brief look at the goals of basic series and parallel termination networks will clarify their use.

The goal of parallel termination is absorbtion of all transmitted energy at the network terminus with none reflected to the source. Any signal distortion occurring is solely due to reflections from the loads attached to the line. The parallel termination should have a resistive value close to that of the network's impedance to be optimally effective. Parallel terminations may be simply a single resistor from the terminus of the network to a voltage source (normally −2V) or they may be Thevenin networks equivalent to the single resistor and voltage source values.

The series termination operates on the principle of Ohm's Law. As a voltage divider, the goal of the series termination is to reduce the driver's output voltage transmitted into the line by about one-half. When this voltage (referred to as the incident wave voltage) reaches the opposite end or terminus of the network, which is unterminated and approximately an open circuit, the voltage level doubles. A receiver at the terminus of the line sees its full input voltage swing. However, receivers between the input and terminus ends see only the voltage transmitted into the line. All of the voltage arriving at the terminus is reflected back to the source with the same polarity as that of the incident wave voltage.

As this reflected wave voltage transits the line toward the source end, the voltage level along the line is raised to the full swing voltage of the driver's output. Only at the instant when this voltage wave reaches each input will that input see its full voltage swing. Therefore, intermediate loads experience a period where input voltage is at or near threshold level. Consequently, there is a delay of more than one line transit time until the input voltage reaches a proper level. For this reason, series terminations are used almost exclusively in point-to-point networks.

In some cases, networks may require combinations of series and parallel terminations to achieve satisfactory performance. Networks of this type must be carefully designed and tested on an individual basis to assure correct operation. The laws governing such networks are the same as for the basic networks and terminations. Further information on terminations, other network configurations and their design requirements can be found in the "F100K ECL Logic Databook and Design Guide", Chapter 4.

PC BOARD LAYOUT RECOMMENDATIONS

Proper PC board layout is high on the list of important considerations when using ECL minimum-skew devices. The performance enhancement offered by minimum-skew devices can be wasted by inadequate layout. So, a look at some additional layout recommendations aimed at maintaining the high performance that these ECL devices are capable is essential.

F100K ECL minimum-skew devices are available standardly in surface mount packaging. Devices use either SOIC and PCC packages. Each package type has its own unique mounting requirements. However, there are some common areas where both types can benefit from attention to layout. These areas are bypassing location, power and ground connections, differential line layout and power plane isolation.

Literature available from National Semiconductor is listed in the Appendix.

BYPASS CAPACITOR PLACEMENT

The placement of bypass capacitors is as important as their electrical characteristics. Placement and connection into the system can significantly alter the effectiveness and electrical performance of the bypassing elements. Ideally, the capacitor is placed as close as possible to the device requiring the bypass. Only an absolute minimum of wire length should connect the capacitor to the power planes or the IC leads. If surface mount capacitors are used, the mounting lands are connected directly to the power planes through vias and omit any extra wiring. *Figure 5* shows the recommended placement and connection methods for PCC layouts on conventional multi-layer PCB's. *Figure 6* shows the recommended application where SOIC packaging is used.

POWER AND GROUND CONNECTIONS

Power and ground connection paths must be kept short otherwise excess inductance is introduced in the IC's power leads. Excess inductance reduces the effectiveness of any associated bypassing and makes the power supply seen by the IC less stable. Where multiple power or ground pins are provided on the IC package, all should be connected to the appropriate supply potential. *Figure 7* shows examples of correct and incorrect power connections to PCC and SOIC packaged devices.

DIFFERENTIAL LINE LAYOUT

National's minimum-skew devices generally employ differential inputs and outputs as an aid in combating skew. When combined with properly designed differential transmission line layouts, precise system timing is possible. However, careless layout of differential lines can cause serious timing and skew problems. By observing a few simple rules, effective differential transmission systems can be easily designed.

1. Differential transmission lines must be organized in pairs. Lines originating at complementary outputs must be paired throughout their lengths. Additional spacing should be allowed between pairs in all layers. Approximately twice the spacing between the lines of the pair should be used between pairs.
2. Both lines of a differential pair must be of equal length. Changes of direction must be accompanied by either an equal and opposite change of direction or additional length must be added to the resulting shorter line.
3. Differential lines should be paired (run parallel) in the same layer. When a direction change dictates a change of layer, both conductors should change layers. In general, there should be an equal number of vias in each line as the result of layer changes. The width of the lines may be adjusted according to preserve line impedance.
4. Corners in lines with angles greater than 45° should be mitered or radiused to preserve impedance uniformity.

Figure 8 illustrates these rules with several ways in which differential lines may be implemented correctly and incorrectly.

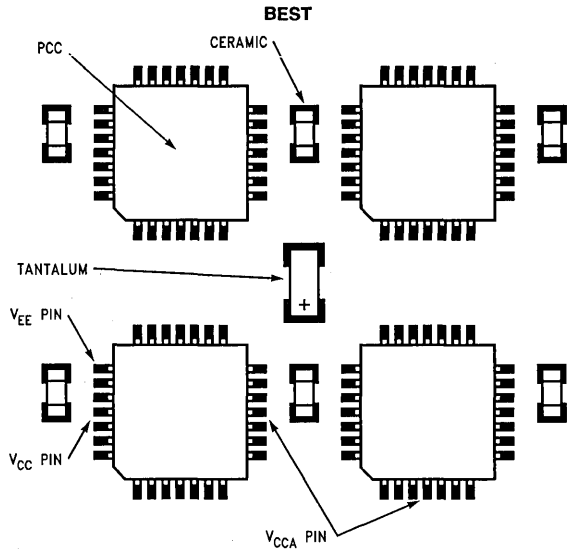
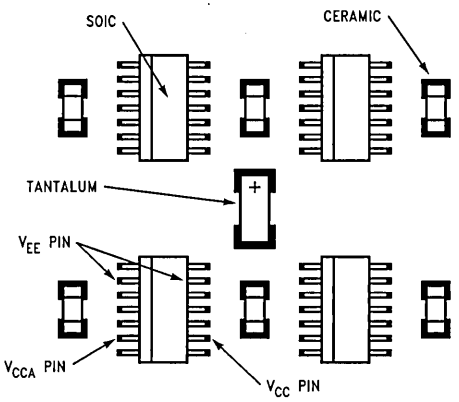


FIGURE 5. PCC Bypass Capacitor Placement

BEST



TL/F/10982–9

ACCEPTABLE

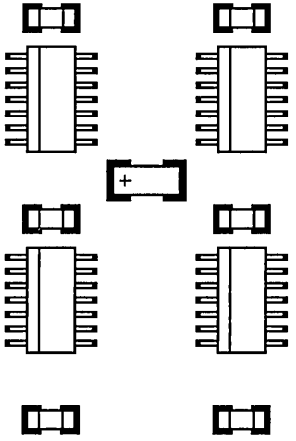


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FIGURE 6. SOIC Bypass Capacitor Placement

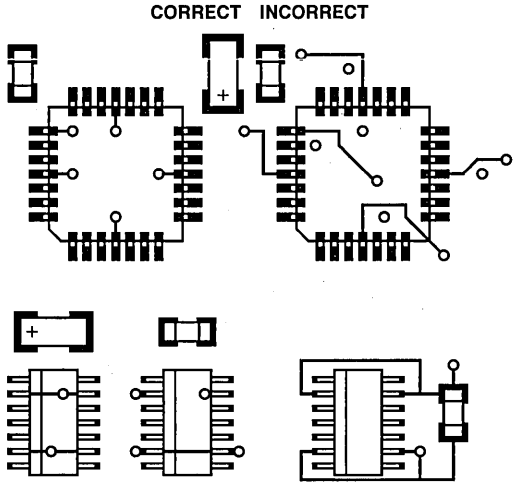

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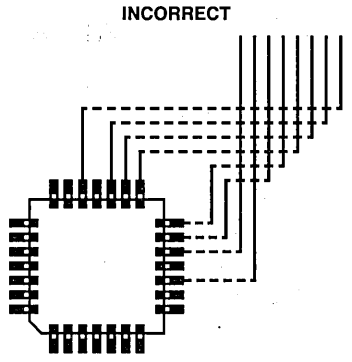
FIGURE 7. Power Pin Connection



TL/F/10982–12

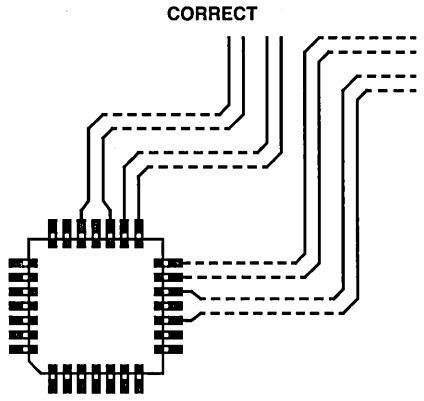


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FIGURE 8. Differential Line Layout

AVOIDING SKEW TOLERANCE BUILD-UP

There are additional steps that can be taken to avoid skew build-up. Perhaps the simplest is to observe the rule of equal loading and termination. Briefly stated, all matching delay paths must be loaded equally, both resistively and reactively. Complementary outputs must have equal resistive termination values. Capacitive loading must be equal for both outputs, also. This is especially true of differential lines.

For example and using the delay value for 50Ω lines mentioned previously, a loading difference of 5 pF between the conductors of a differential line can result in a skew of 105 ps, or about one-fifth of a risetime. When combined with other effects like crosstalk and impedance discontinuities, significant skew can occur.

Path delay distribution is another step that can be taken to avoid skew build-up, *Figure 9.* This means that, if a clock distribution path must pass through several amplifiers, steps should be taken to assure that the signal does not use the same path, pin-wise, through all amplifiers. To illustrate, assume that the path passes through three F100311, 1:9 differential drivers. The input pins in all cases are 28 (in) and 2 (in/). If the first output pair is 25 (D0) and 24 (D0/), then choose pins 23 (D1) and 22 (D1/) for amplifier #2 and pins 20 (D2) and 19 (D2/) for the third amplifier. Additional variation can be achieved by reversing the input phase through each amplifier. Of course, the output phase must be similarly reversed to match the input. These points may seem minor, but all contribute to reducing the mathematical probability of skew tolerance build-up.

TESTING MINIMUM-SKEW CLOCK SYSTEMS

As with all types of electronic systems, the performance of minimum-skew circuits must be verifyable and testable. The very nature of these systems calls for more care and precision in testing than other types of logic systems. And, greater precision is required from the test equipment and its use.

Certainly the oscilloscope is the most frequently used piece of test equipment for logic systems. While it does provide much information about the quality of signals, it may be the cause of error if improperly applied. Perhaps the single largest error source and the least recognized is the place where scope and circuit meet, the probe. To do justice to the subject of probing and probes in pulse application would require a book unto itself. One very useful book from Tektronix is "ABC's of Probes". In it are emphasized some essentials for choosing a suitable probe for the job. Some of these are:

— Compatibility with the scope system,

— Adequate bandwith and risetime capability exceeding that of the system to be tested,

— Low circuit loading, which implies low capacitance at the tip,

— High enough impedance so as to not unduly load the circuit being probed (This does not mean that FET probes are the best choice!),

— And delay matching when multiple probes are used for relative delay measurements.

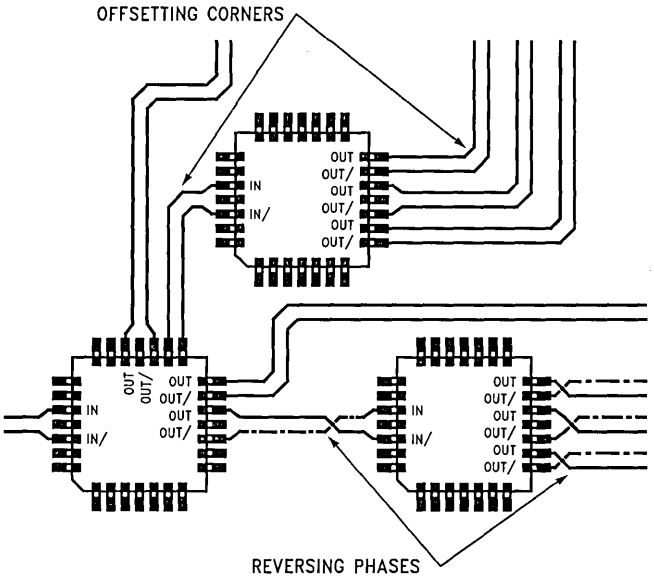

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FIGURE 9. Avoiding Skew Tolerance Buildup

The choice of scope is equally important and the list of its basic features is similar to that for the probe. Where the precise nature of the signal to be measured is unknown, the analog scope may provide the most useful information initially. While it does not have all of the sophistication of digital scopes, it offers fewer complications and a fidelity that is hard to beat. The digital scope, especially if it has storage capability, can be an asset where comparison of signals taken at different times and places in the circuit is important.

Additional useful information on scopes and in-circuit measurements may be found in the series "Troubleshooting Analog Circuits" by National Semiconductor's Bob Pease in "EDN" and available as a reprint from National.

A final consideration and one that is often overlooked is the incorporation of test points in the circuit. The increasing use of surface mount devices and dense layouts makes probing these circuits more difficult. Inclusion of test points or test connectors can ease the job considerably. Just remember to make sure that the test points do not corrupt the signals and are themselves designed for minimum-skew. Test points may even be provided by reserving one output of an ECL minimum-skew device at each critical point in the circuit. This provides isolation for the probe and minimal loading on the monitored circuit. And, of course it should go without saying that test points should be accessible without the need to mechanically or electrically alter normal operation of the equipment being tested.

APPENDIX

Available Literature

Application Notes

AN-467 — Surface Mount: From Design to Delivery

AN-468 — Wave Soldering of Surface Mount Components

AN-469 — Reliability of Small Outline Surface Mount Packages

AN-470 — Wave Soldering: Is SOIC Reliability Compromised?

Datasheets

113295-001 — Plastic Chip Carrier Technology

113615-001 — A Basic Guide to Surface Mounting of Electronic Components

Other Literature

570430-001 — Reliability Report Update Small Outline (SO) Package

570435-001 — Getting Started in Surface Mount

980040-001 — Reliability Report Update — Plastic Chip Carrier (PCC) Package

980045-001 — Reliability Report Update — Small Outline (SO) Package

980055-004 — Surface Mount Availability Guide

F100K ECL 100 Series to 300 Series Conversion Book

Troubleshooting Analog Circuits (EDN Article Series Reprint)

Databooks

400080 — Reliability Handbook

400028 — F100K ECL Logoic Databook and Design Guide

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"F100K ECL Logic Databook and Design Guide", National Semiconductor Corp., 1991

"Radiotron Designer's Handbook"; Fourth Ed.; F. Langford-Smith; Amalgamated Wireless Valve Co. Pty. Ltd.; Sydney, Australia; 1952

"The RF Capacitor Handbook"; 1st Ed.; American Technical Ceramics; 1979

"Traveling-Wave Engineering"; R.K. Moore; McGraw-Hill; 1960

"Communications Systems: An Introduction to Signals and Noise in Electrical Communications"; A. Bruce Carlson; McGraw-Hill; 1968

"Analysis, Transmission and Filtering of Signals"; M. Javid and E. Brenner; MrGraw-Hill; 1963

'ABC's of Probes"; Tektronix, Inc.; 1989

Electronic Circuit Calculations Simplifed, Part 4 - RC combinations in D.C. circuits"; S.W. Amos; "Wireless World"; 9/1975; pp. 423–426

'Electronic Circuit Calculations Simplified, Part 5 - RC combinations in A.C. circuits", S.W. Amos; "Wireless World"; 10/1975; pp. 475–478

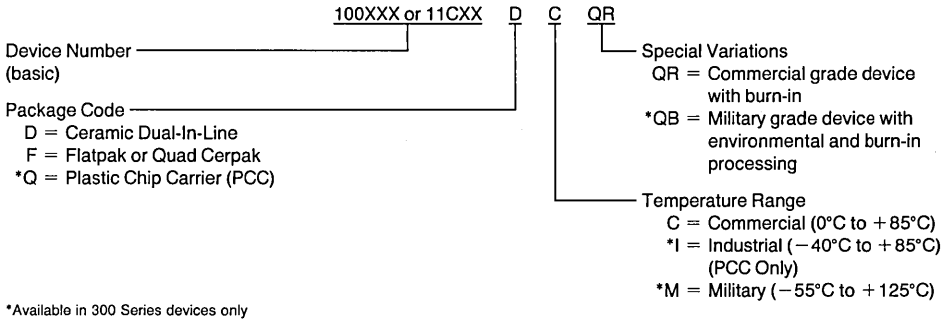
Section 6

Ordering Information and Physical Dimensions

Section 6 Contents

ORDER INFORMATION

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



*Available in 300 Series devices only

For most current packaging information, contact product marketing.

National Semiconductor

ECL Tape-and-Reel Specification

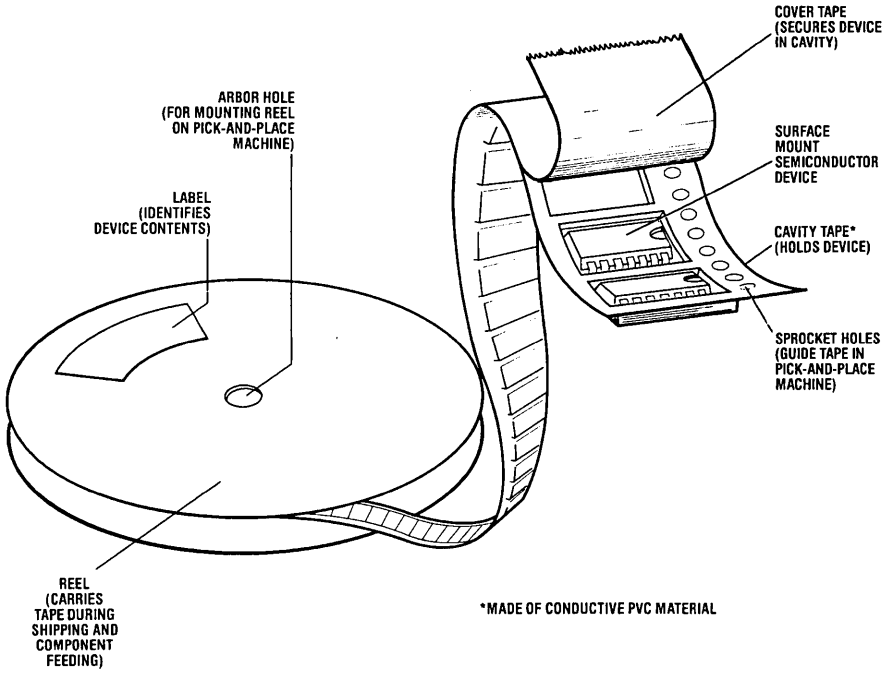
General Description

Tape-and-Reel is a new method for shipment of surface mount devices. This approach simplifies the handling of semiconductors for automated circuit board assembly systems. A Tape-and-Reel holds hundreds-to-thousands of surface mount devices (as compared with less than 100 devices in a rail), so that pick-and-place machines have to be reloaded less frequently. This savings in labor will further reduce manufacturing costs for automated circuit board assembly.

Features

- Conductive PVC material redeuces static charge build-up
- Fully meets proposed EIA standard RS-481A (taping of surface-mounted components for automatic placing)
- Fully compatible with National's surface mount package types
- Variable code density code 39 bar code label for Automated Inventory Management availability
- Mechanical samples of surface mount packages available in Tape-and-Reel for automated assembly process development
- Single Tape-and-Reel holds hundreds-to-thousands of surface mount semiconductors for additional labor savings
- Conductive cover Tape-and-Reel availability
- Reels individually packed

Tape-and-Reel Diagram



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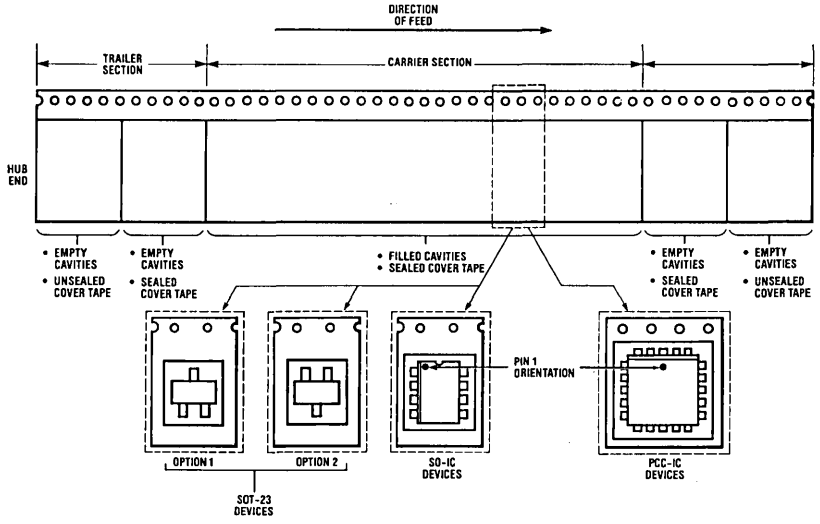
Tape-and-Reel Overview

TAPE FORMAT AND DEVICE ORIENTATION



TL/F/10995–2

MATERIALS

- Cavity Tape: Conductive PVC (less than 10^5 Ω/Sq)
- Cover Tape: Polyester
  1. Conductive Cover available
- Reel: 1. Solid 80 pt. Fibreboard (standard)
  2. Conductive Fibreboard available
  3. Conductive Plastic (PVC) available

LABEL

Human and machine readable label is provided on reel. A variable (C.P.I.) density code 39 is available. NSC STD Label (7.6 C.P.I.).

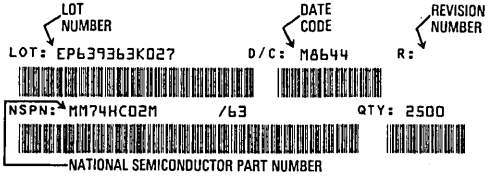
Field

Lot Number
Date Code
Revision Level
National Part No. I.D.
Quantity

Fields are separated by at least one blank space.

Future Tape-and-Reel packs will also include a smaller-size bar code label (high-density code 39) at the beginning of the tape. (This tape label is not available on current production.)

Example:



TL/F/10995–3

National Semiconductor will also offer additional labels containing information per your specific specification.

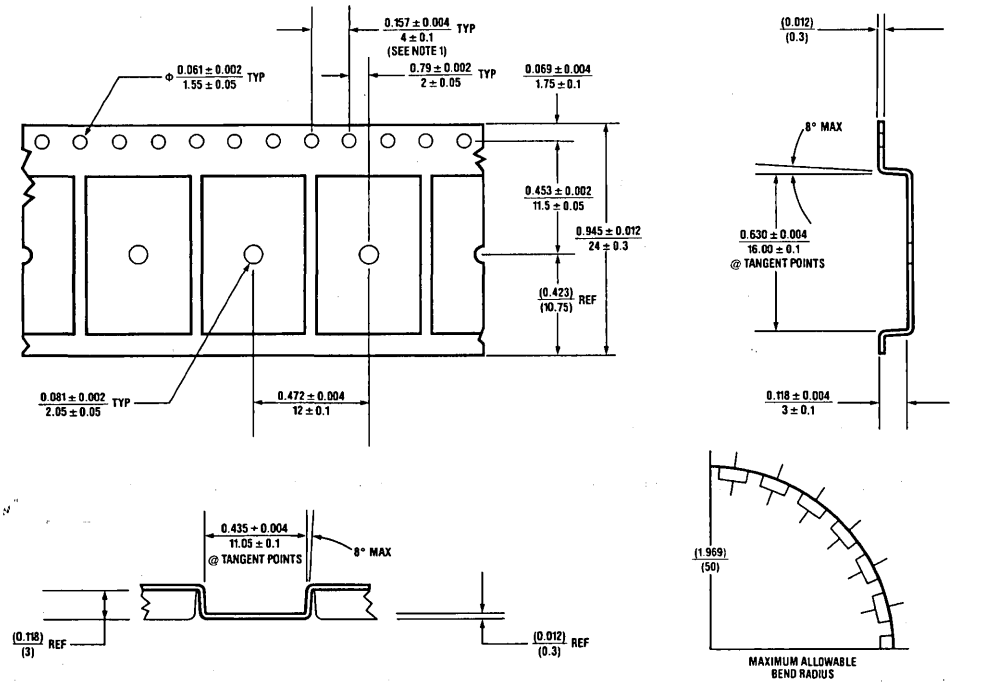
SO-24 (Wide)

TAPE FORMAT

Direction of Feed ↑

Tape Section	# Cavities	Cavity Status	Cover Tape Status
Leader (Start End)	5 (min)	Empty	Unsealed
	5 (min)	Empty	Sealed
Carrier	1000	Filled	Sealed
Trailer (Hub End)	2 (min)	Empty	Sealed
	2 (min)	Empty	Unsealed

TAPE DIMENSIONS



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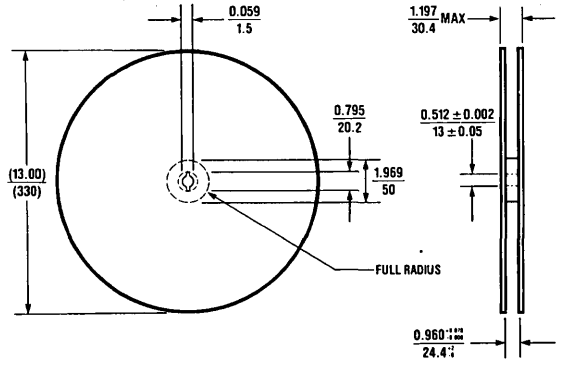
REEL DIMENSIONS



TL/F/10995–5

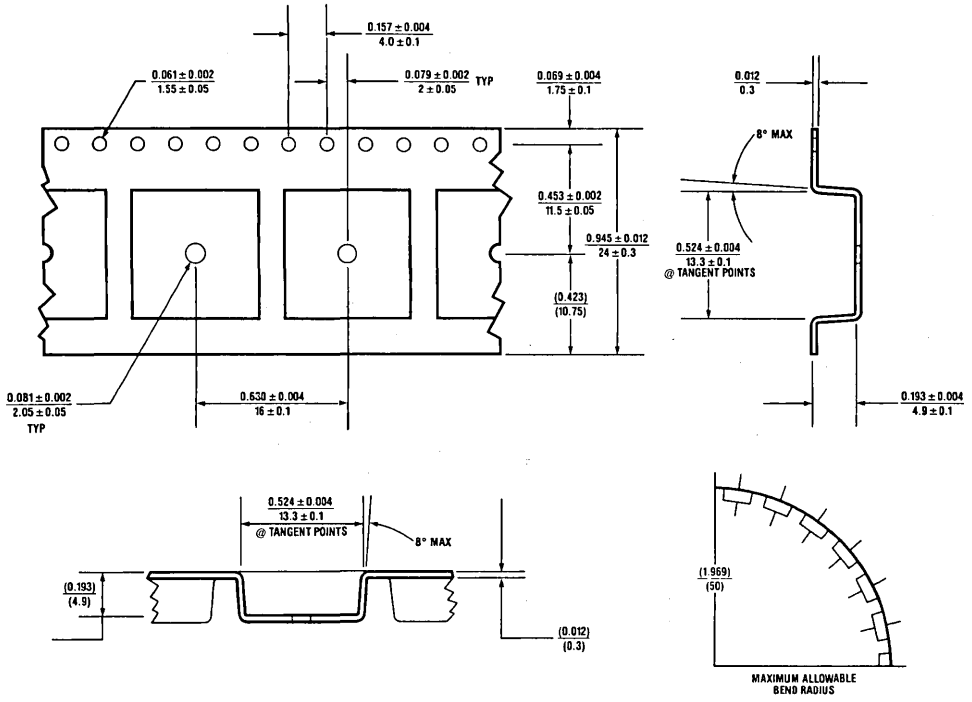
PLCC-28

TAPE FORMAT

Direction of Feed ↑

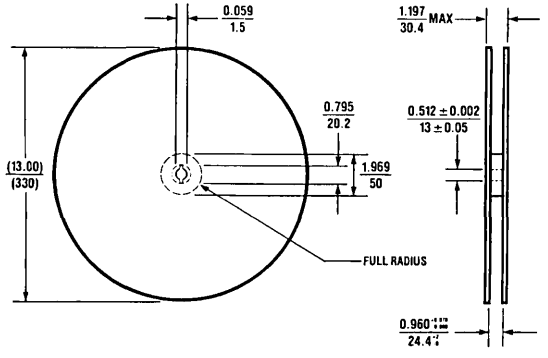
Tape Section	# Cavities	Cavity Status	Cover Tape Status
Leader (Start End)	5 (min)	Empty	Unsealed
	5 (min)	Empty	Sealed
Carrier	750	Filled	Sealed
Trailer (Hub End)	2 (min)	Empty	Sealed
	2 (min)	Empty	Unsealed

TAPE DIMENSIONS



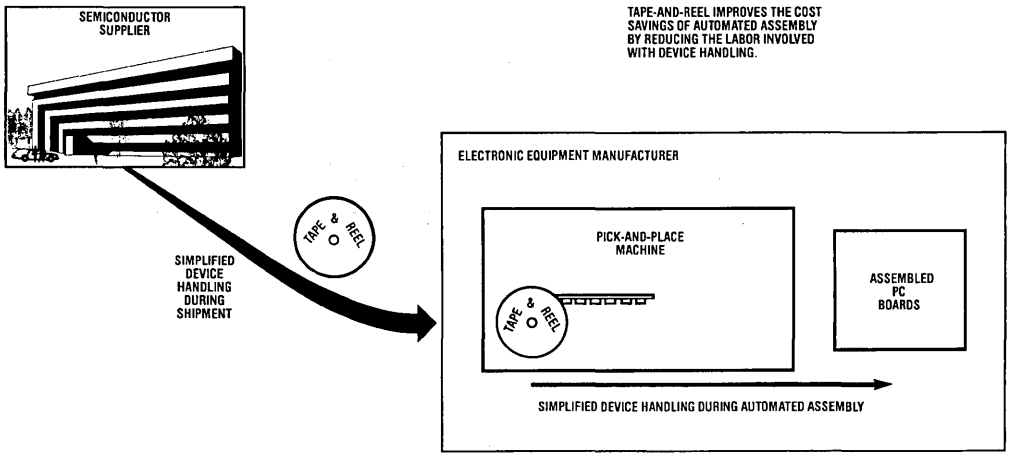
TL/F/10995–6

REEL DIMENSIONS



TL/F/10995–7

Application—Total System Saving



TL/F/10995–8

Cost pressures today are forcing many electronics manufacturers to automate their production lines. Surface mount technology plays a key role in this cost-savings trend because:

1. The mounting of devices on the PC board surface eliminates the expense of drilling holes;
2. The use of pick-and-place machines to assemble the PC boards greatly reduces labor costs;
3. The lighter and more compact assembled products resulting from the smaller dimensions of surface mount packages mean lower material costs.

Production processes now permit both surface mount and insertion mount components to be assembled on the same PC board.

Automated manufacturers can improve their cost savings by using Tape-and-Reel for surface mount devices. Simplified handling results because hundreds-to-thousands of semiconductors are carried on a single Tape-and-Reel pack (see the "Ordering Information" section for the exact quantities). With this higher device count per reel (when compared with less than 100 devices per rail), pick-and-place machines have to be re-loaded less frequently and lower labor costs result.

With Tape-and-Reel, manufacturers save twice—once from using surface mount technology for automated PC board assembly and again from less device handling during shipment and machine set-up.

Ordering Information

When you order a surface mount semiconductor, it will be in one of the 15 available surface mount package types (see Section 6 for the physical dimensions of the surface mount packages). Specifying the Tape-and-Reel method of shipment means that you will receive your devices in the following quantities per Tape-and-Reel pack:

		Device Quantity
Small Outline IC	SO-24 (Wide)	1000
Plastic Chip Carrier IC	PLCC-28	750

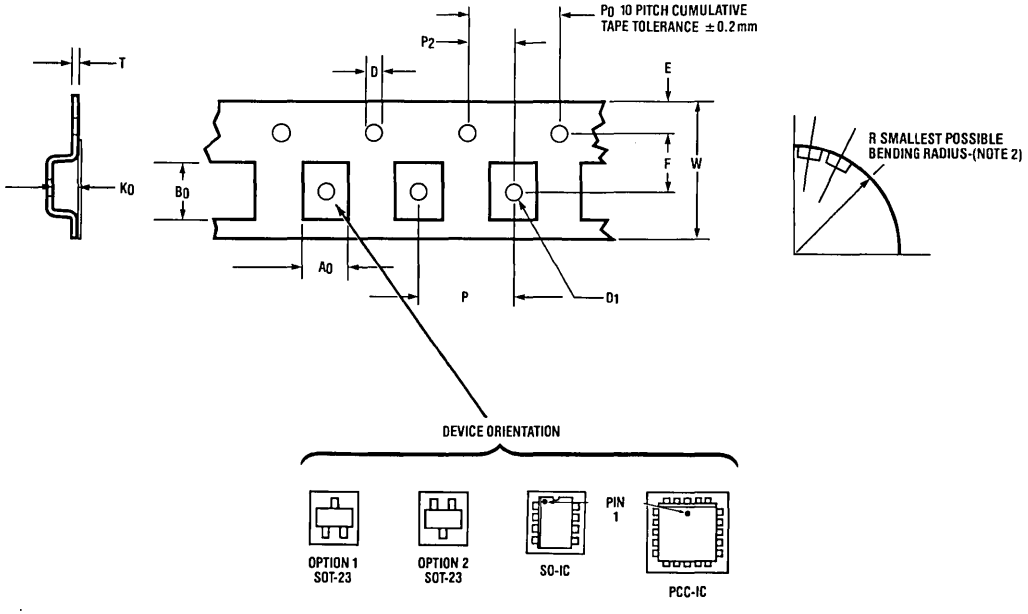
Appendix I—Short-Form Procurement Specification

TAPE FORMAT

→ Direction of Feed

	Trailer (Hub End)		Carrier	Leader (Start End)	
	Empty Cavities, min (Unsealed Cover Tape)	Empty Cavities, min (Sealed Cover Tape)	Filled Cavities (Sealed Cover Tape)	Empty Cavities, min Sealed Cover Tape)	Empty Cavities, min (Unsealed Cover Tape)
SMALL OUTLINE IC					
SO-24 (Wide)	2	2	1000	5	5
PLASTIC CHIP CARRIER IC					
PLCC-28	2	2	750	5	5

TAPE DIMENSIONS (24 Millimeter Tape or Less)



TL/F/10995–9

	W	P	F	E	P_2	P_0	D	T	A_0	B_0	K_0	D_1	R
SMALL OUTLINE IC													
SO-24 (Wide)	24 ± .30	12.0 ± .10	11.5 ± .10	1.75 ± .10	2.0 ± .05	4.0 ± .10	1.55 ± .05	.30 ± .10	10.9 ± .10	15.85 ± .10	3.0 ± .10	2.05 ± .05	50
PLASTIC CHIP CARRIER IC													
PLCC-28	24 ± .30	16.0 ± .10	11.5 ± .10	1.75 ± .10	2.0 ± .05	4.0 ± .10	1.55 ± .05	.30 ± .10	13.0 ± .10	13.0 ± .10	4.9 ± .10	2.05 ± .05	50

Note 1: A_0, B_0 and K_0 dimensions are measured 0.3 mm above the inside wall of the cavity bottom.

Note 2: Tape with components shall pass around a mandril radius R without damage.

Note 3: Cavity tape material shall be PVC conductive (less than 10^5 Ω/Sq).

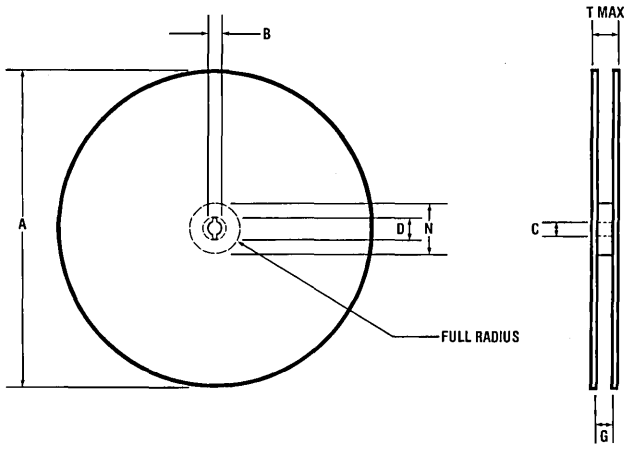
Note 4: Cover tape material shall be polyester (30–65 grams peel-back force).

Note 5: D_1 Dimension is centered within cavity.

Note 6: All dimensions are in millimeters.

Appendix I—Short-Form Procurement Specification (Continued)

REEL DIMENSIONS



TL/F/10995–10

		A (Max)	B (Min)	C	D (Min)	N (Min)	G	T (Max)
24 mm Tape	SO-24 (Wide)	(13.00)	0.059	0.512 ± 0.002	0.795	1.969	$0.960^{+0.078}_{-0.000}$	1.197
	PLCC-28	(330)	1.5	13 ± 0.05	20.2	50	24.4^{+2}_{-0}	30.4

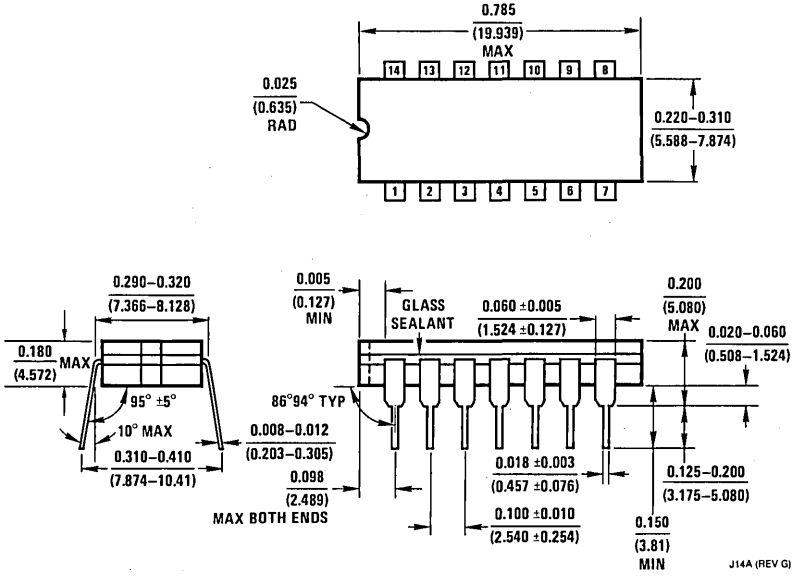
Units: Inches / Millimeters

Material: Paperboard (Non-Flaking)

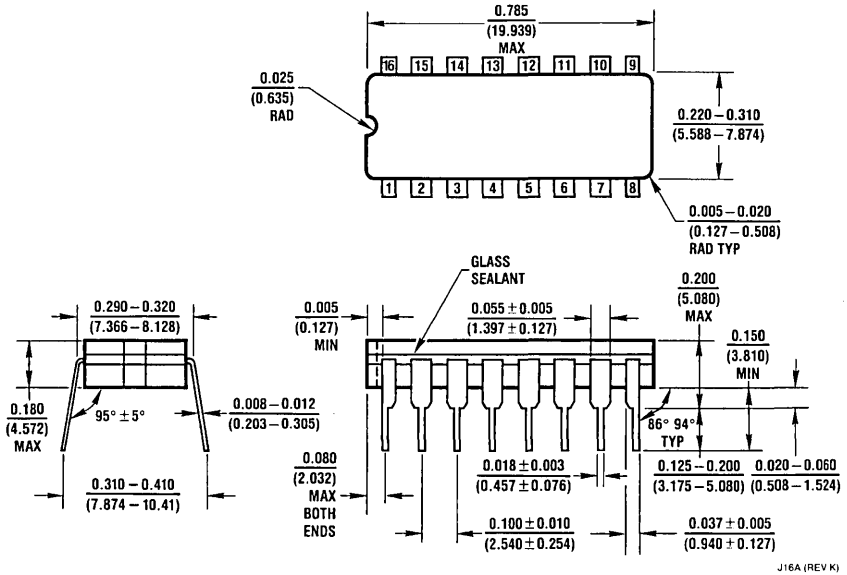
National Semiconductor

All dimensions are in inches (millimeters)

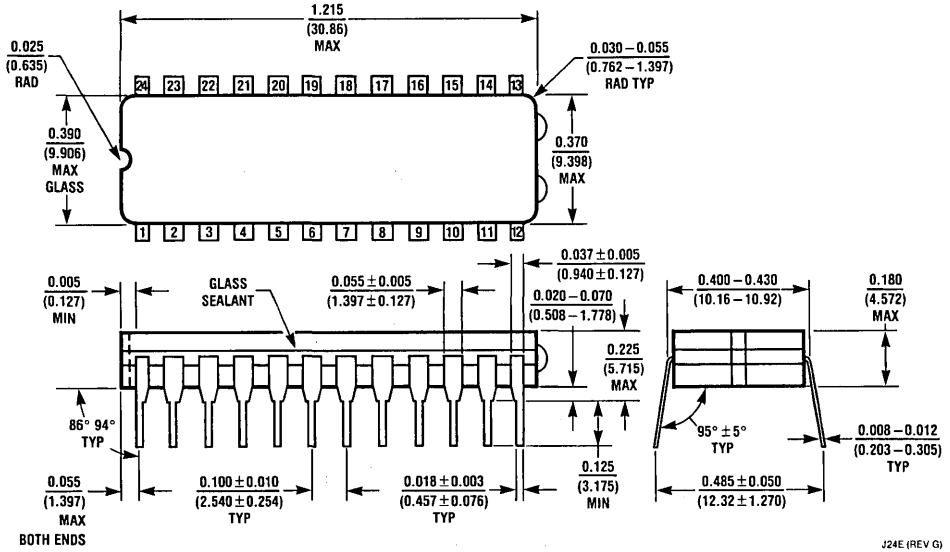
14 Lead Ceramic Dual In-Line Package (D)
NS Package Number J14A



16 Lead Ceramic Dual In-Line Package (D)
NS Package Number J16A

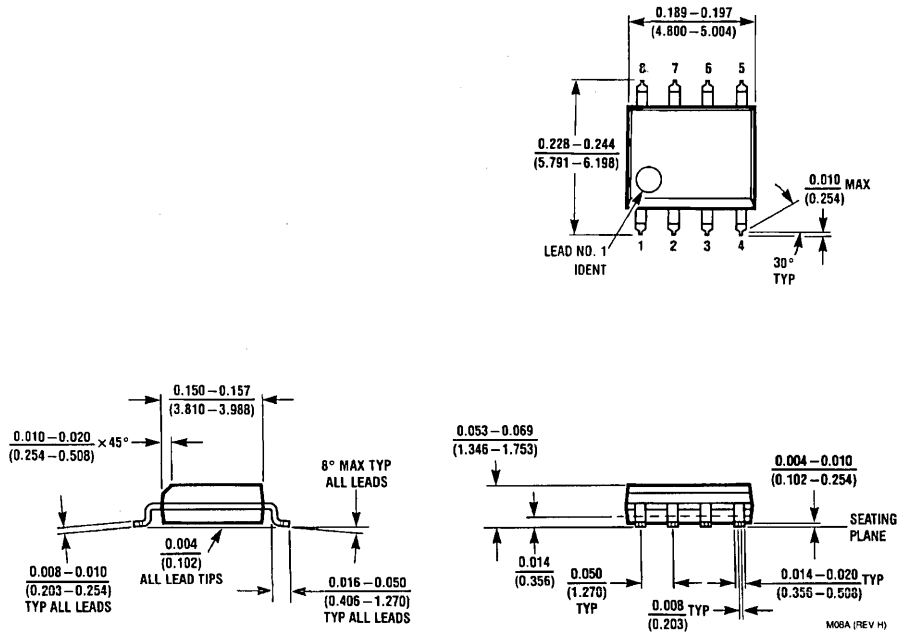


24 Lead Ceramic Dual In-Line Package (0.400" Wide) (D)
NS Package Number J24E



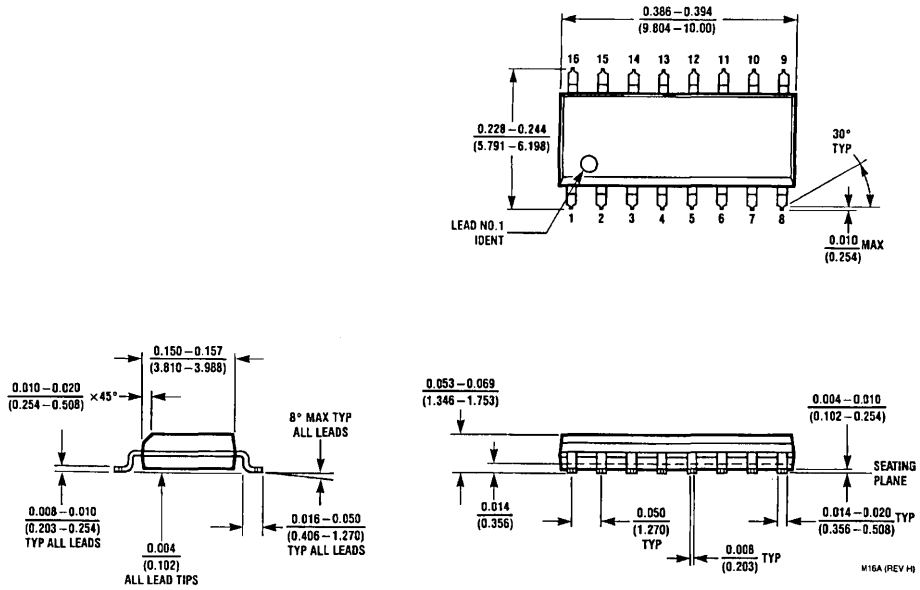
J24E (REV G)

8 Lead (0.150" Wide) Molded Small Outline Package (S)
NS Package Number M08A

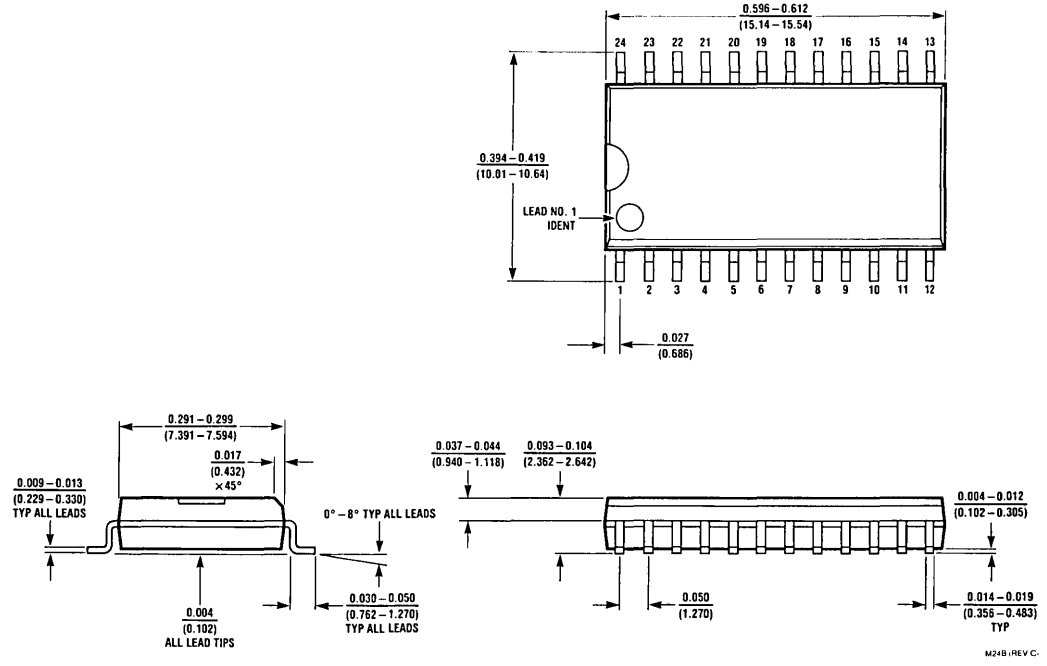


M08A (REV H)

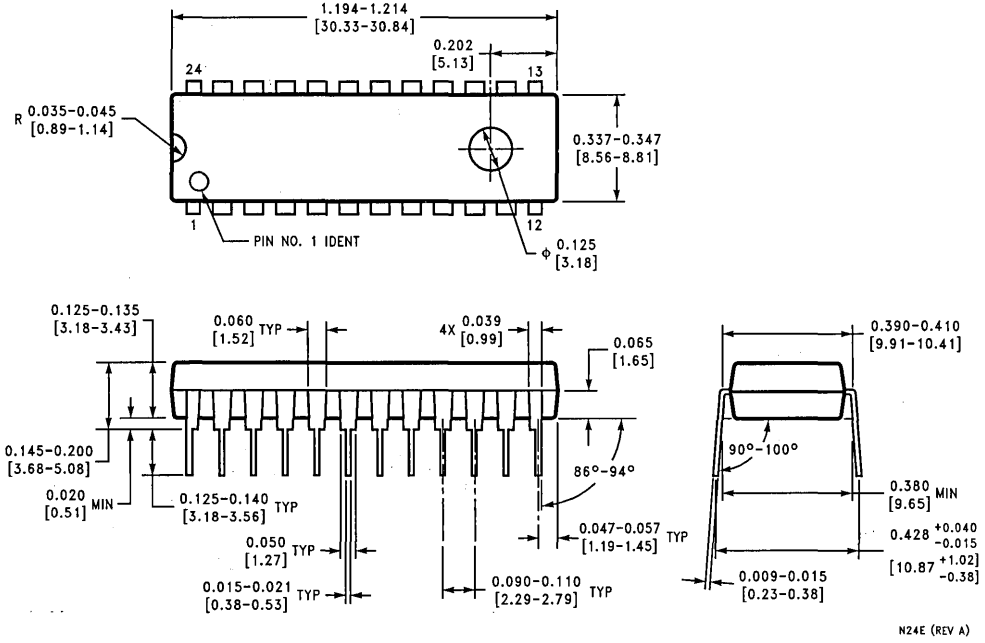
16 Lead Small Outline Integrated Circuit (S)
NS Package Number M16A



24 Lead (0.300" Wide) Molded Small Outline Package (S)
NS Package Number M24B

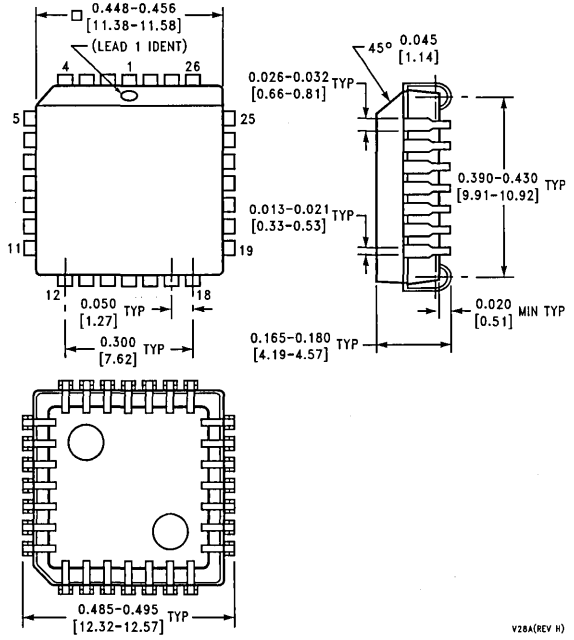


24 Lead Molded Dual In-Line Package (P)
NS Package Number N24E



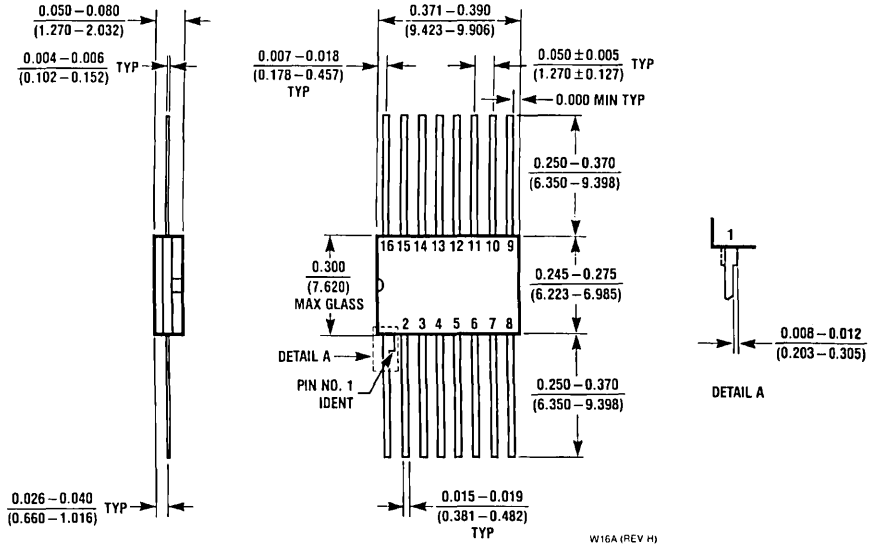
N24E (REV A)

28 Lead Plastic Chip Carrier (Q)
NS Package Number V28A



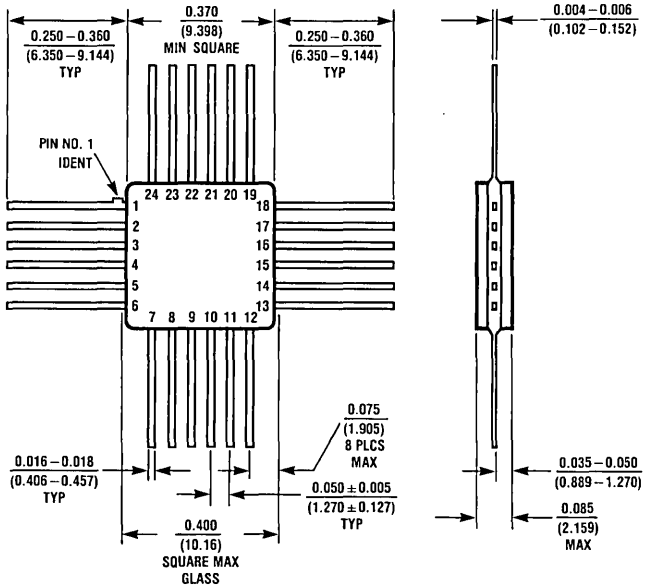
V28A(REV H)

16 Lead Ceramic Flatpak (F)
NS Package Number W16A



W16A (REV H)

24 Lead Quad Cerpak (F)
NS Package Number W24B



W24B (REV C)

NOTES

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Quiet Series: 54ACTQ/74ACTQXXX • 54FCT/74FCTXXX • FCTA: 54FCTXXXA/74FCTXXXA

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